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Comparative Evaluation of Advanced 3-level Inverter/Converter Topologies against 2-level Systems

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Outline

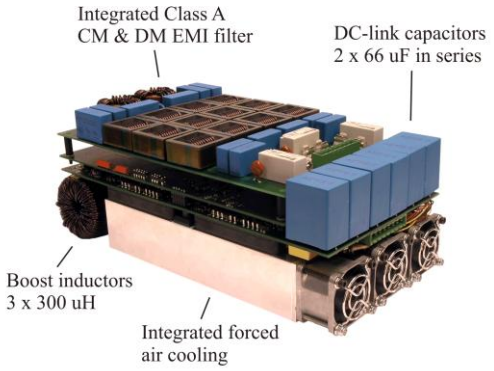
- Introduction
- 3-level T-type converter topology
- 3-level NPC topology with SiC diodes
- Modulation and DC-link balancing
- Comparison of passives
- Comparison of semiconductor chip area
- Optimization potential
- Summary

Introduction to the topic

- **3-phase 3-level topologies for low voltage applications - a bad idea?**

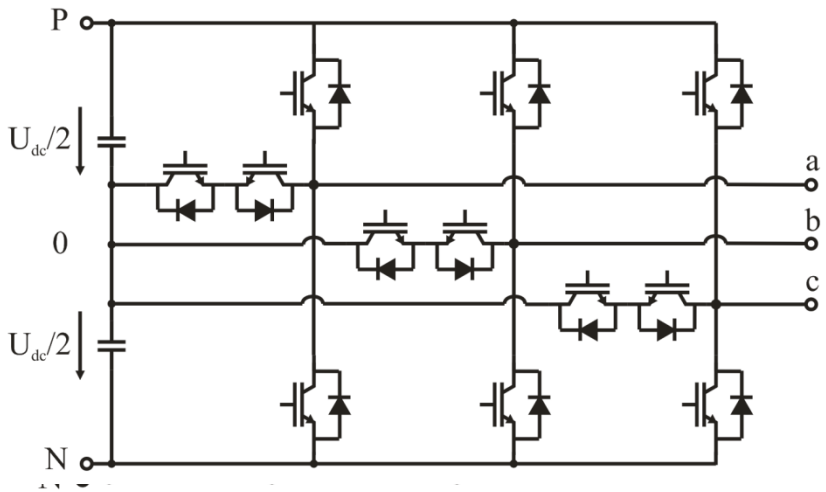
Contra	Pro
➢ *More semiconductors* ➢ *More gate drive units* ➢ *Increased complexity* ➢ *DC-link balancing* ➢ *Increased costs!*	➢ *High efficiency at increased switching frequency* ➢ *Smaller passives*

- **But is this the full story?**
  - *Alternative, suitable 3-level concepts*
  - *Enhancements with SiC diodes*
  - *Necessary semiconductor chip area*
  - *Optimization for operating point*
  - *AC-AC converter DC-link balancing*



Considered voltage source converter topologies

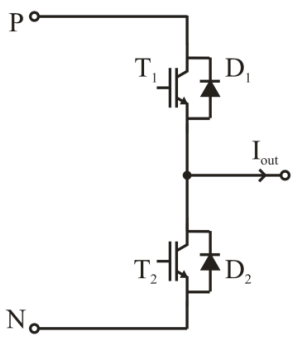
- **2-level VSC**
  - *Simple, low part count, robust, cheap*
  - *Reduction of switching losses with SiC diodes*
- **3-level T-type**
  - *3 bidirectional switches to middle voltage*
- **3-level NPC**
  - *Enhancement with SiC diodes?*
- **AC-AC converters**
  - *Advantages for DC-link balancing*

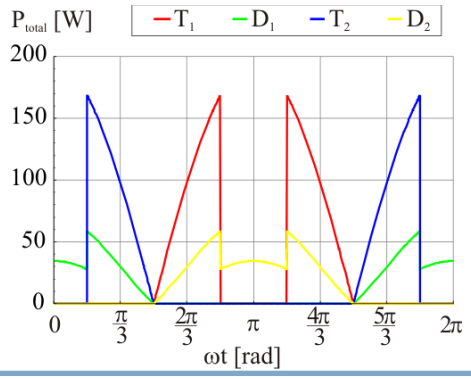


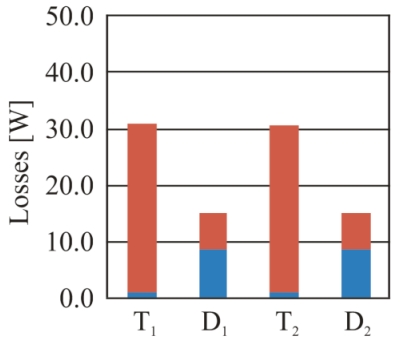
2-level voltage source converter

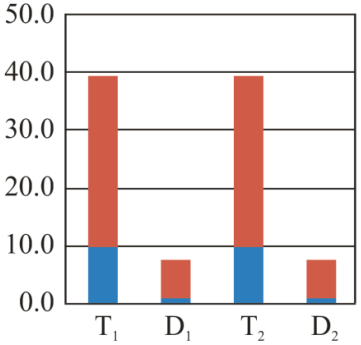
1200V IGBT: Infineon IKW25T120

Rectifier operation **Inverter operation**





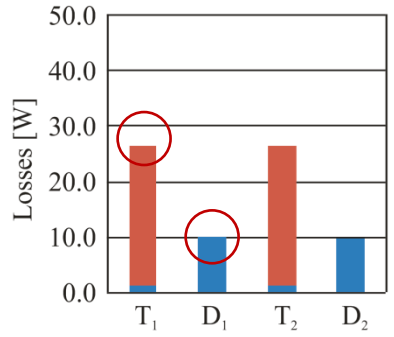


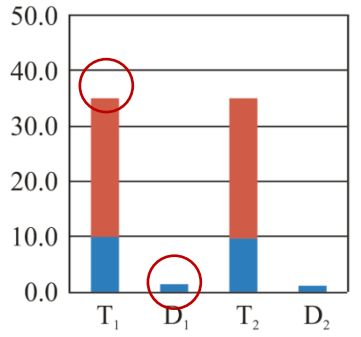


P_n = 10kW, U_{dc}=700V, $\hat{U}_n$=325V, $\hat{I}_n$=20.5A, φ=0/180°

Conduction losses Switching losses (32 kHz)

- **High switching losses**
- **Mean loss distribution is similar for rectifier and inverter operation**
- **Clear benefit from SiC diodes**

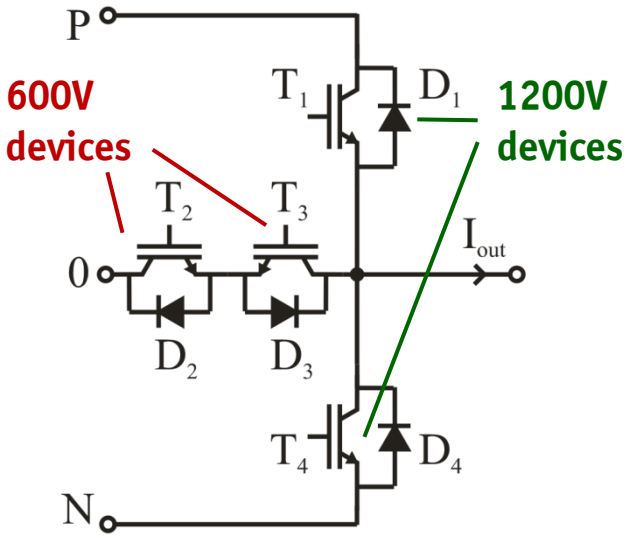




loss reduction: -25% **IKW25T120 + Cree C2D10120 scaled to 25A**

3-level T-type – An alternative VSC topology

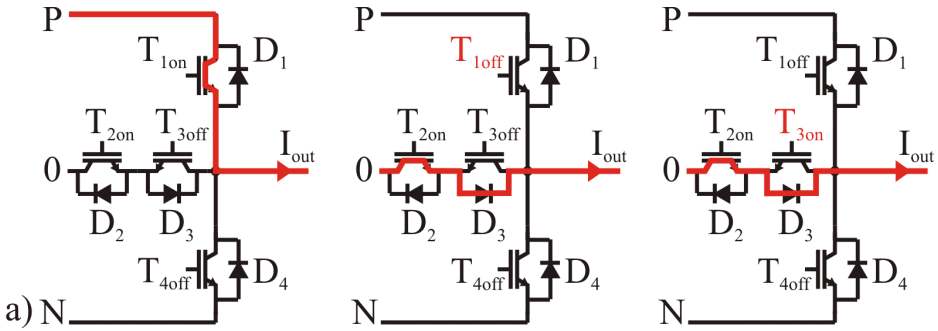
- Simple extension of the conventional 2-level topology to a 3-level topology?
- Bidirectional middle switch with two IGBTs in common emitter connection
- Combination of 1200V and 600V devices
  - *600V IGBT: low switching losses, low forward voltage drop*
  - *Only one more isolated gate drive supply per phase leg (compared to 2-level)*



T-type topology - commutation

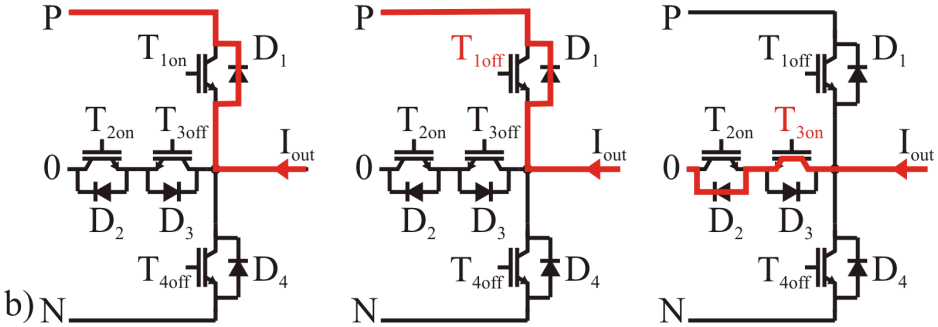
	T_1	T_2	T_3	T_4
P	1	1	0	0
0	0	1	1	0
N	0	0	1	1

- **Current independent commutation sequence**



Transition P ⟶ 0, $I_{out} > 0$

1) T_1 & T_2 closed, T_3 & T_4 open
2) T_1 opens -> I_{out} comm. to 0 over D_3 & T_2
3) T_3 closes after turn-on delay T_d



Transition P ⟶ 0, $I_{out} < 0$

1) T_1 & T_2 closed, T_3 & T_4 open
2) T_1 opens
3) T_3 closes after turn-on delay T_d
   I_{out} comm. to 0 over T_3 & D_2

T-type topology – loss calculation

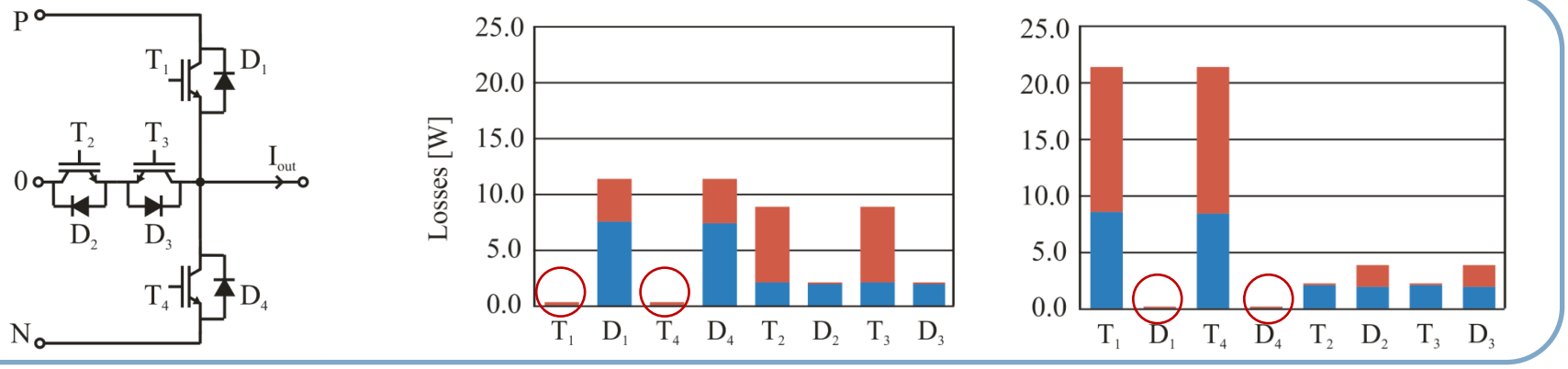
- Switching losses change because of mixed IGBT types
- Loss energy measured with T-type bridge leg test setup
- Reduced switching losses
  - ➢ Commutation voltage is only $U_{dc}/2$
- Distinct loss distribution profile depending on operating point

1200V IGBT: Infineon IKW25T120
600V IGBT: Infineon IKW30N60T

Element	Energy	Datasheet difference
1200V IGBT turn on	0.81 mJ	-19%
1200V IGBT turn off	1.27 mJ	-5%
1200V Diode turn off	0.64 mJ	+22%
600V IGBT turn on	0.68 mJ	+90%
600V IGBT turn off	0.42 mJ	+9%
600V Diode turn off	0.31 mJ	+85%

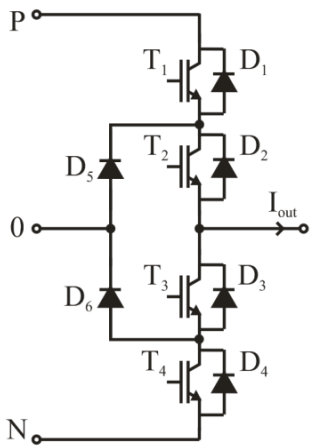
@ 300V, 20A, 125°C

Rectifier operation **Inverter operation**

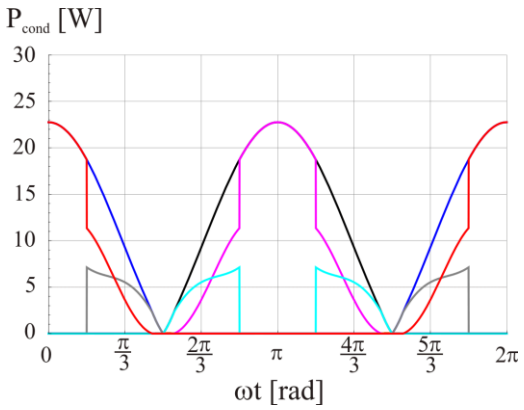


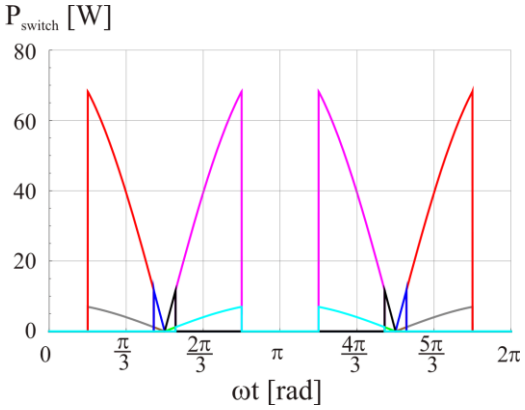
P_n = 10kW, $\hat{U}_n$=325V, $\hat{I}_n$=20.5A, φ=0/180°

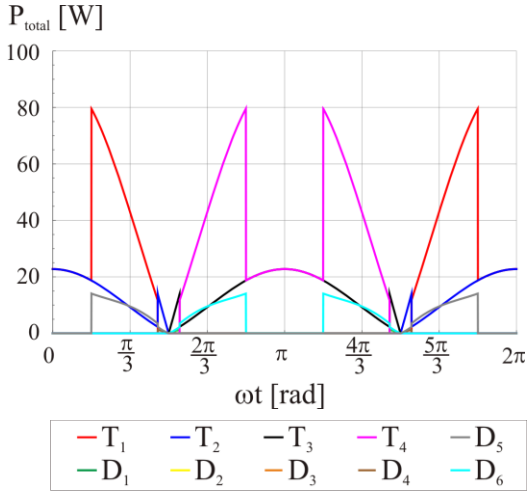
The 3-level NPC converter



- 600V devices: Low switching losses, low forward voltage drop
- Optimal clamping possible
  - *Reduction of switching losses*
  - *DC-link balancing is restricted*
- Can we improve the 3-level NPC converter?
  - *SiC diodes*
  - *Semiconductor chip area optimization*

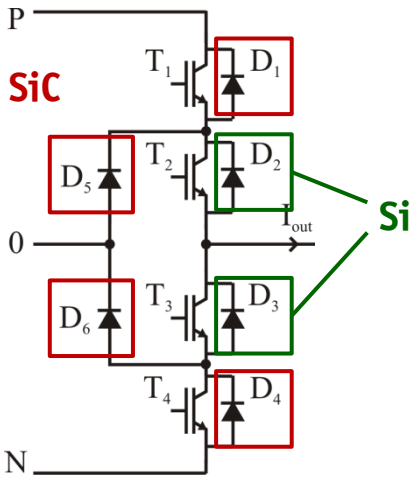


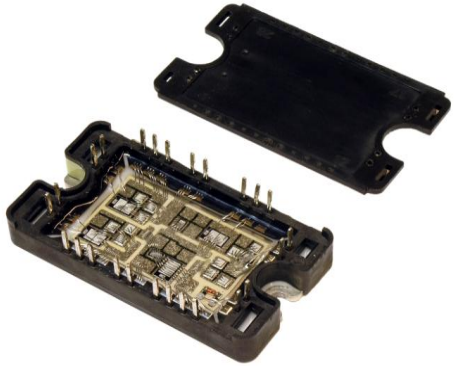




The 3-level NPC converter with SiC diodes

- **Should we replace all diodes with SiC?**
  - *Very expensive!*
  - *Increased conduction losses*
- **3-level NPC Modulation**
  - *Analysis of occuring loss energies*
  - *Direct transition P→N or N→P is omitted*
  - *D_2 and D_3 never show reverse recovery effect!*
    - ➢ *Leave it in conventional Si!*
- **Consider characteristic loss distribution**
  - *Inverter operation (solar inverter)*
    - ➢ *Replace only D_5 and D_6 with SiC diodes*
  - *Rectifier operation (pfc grid interface)*
    - ➢ *Replace only D_1 and D_4 with SiC diodes*





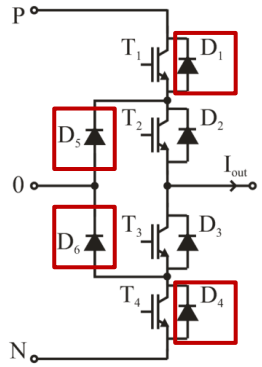
Custom SiC 3-level NPC bridge leg module

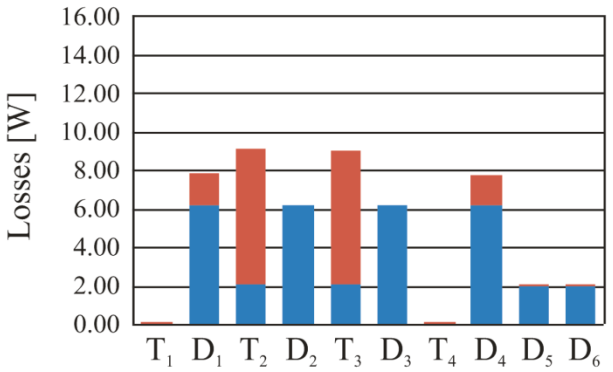
Average Device Losses

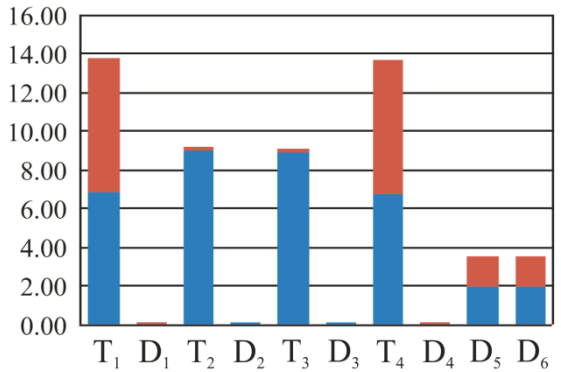
600V IGBT: Infineon IKW30N60T

Rectifier operation

Inverter operation



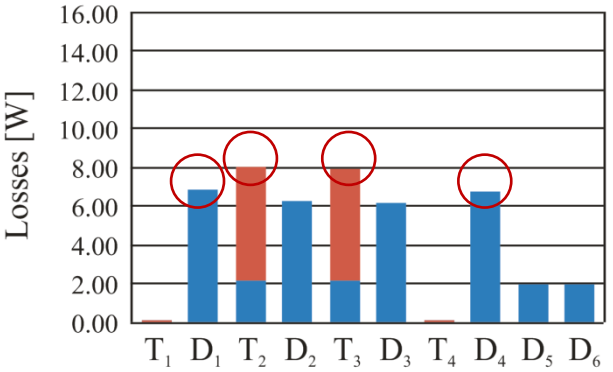


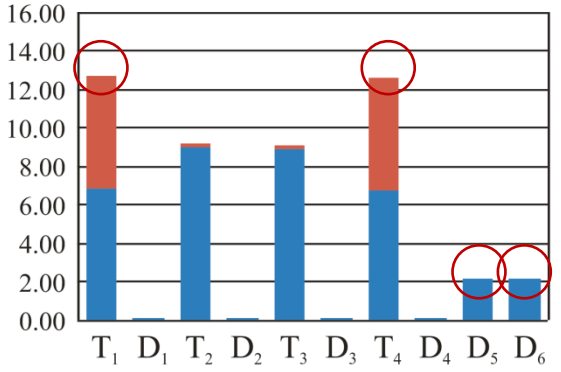


P_n = 10kW, U_{dc}=700V, $\hat{U}_n$=325V, $\hat{I}_n$=20.5A, φ=0/180°

Conduction losses Switching losses (48 kHz)

- Replace D_1 and D_4 with SiC
- Replace D_5 and D_6 with SiC



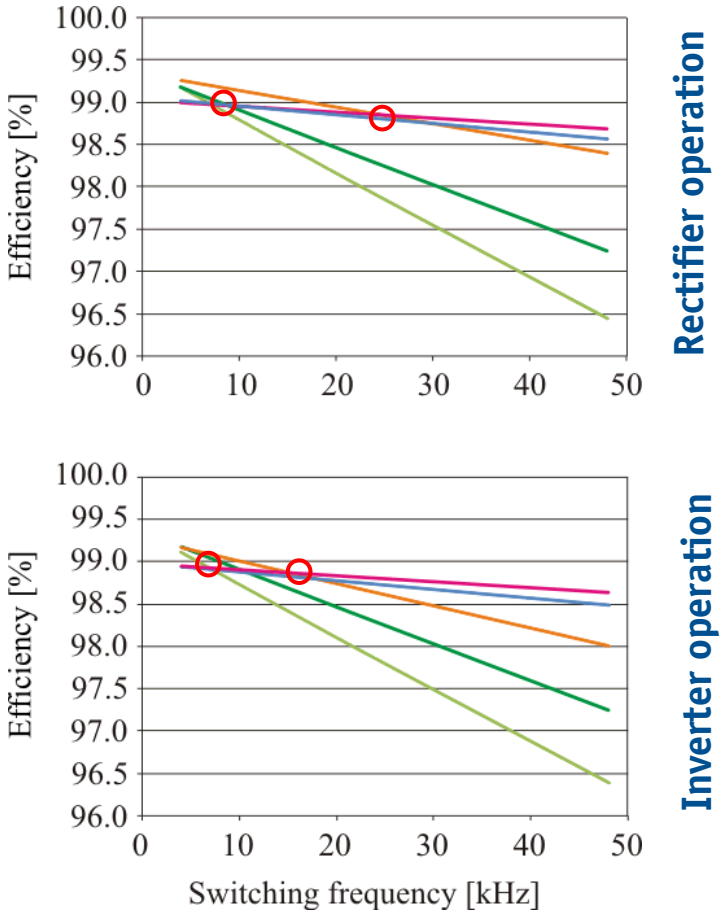


IKW30N60T + Cree CSD10060 scaled to 30A

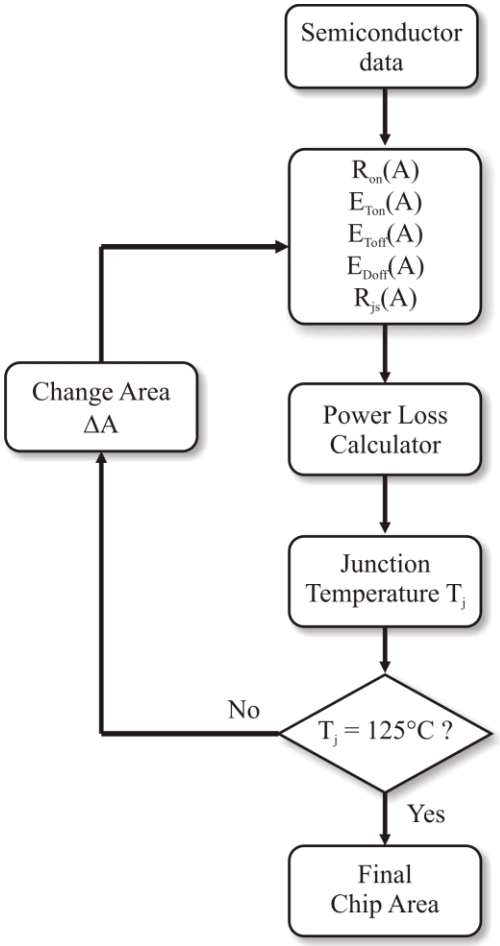
Simple Efficiency Comparison

P_n = 10kW, U_{dc}=700V, $\hat{U}_n$=325V, $\hat{I}_n$=20.5A, φ=0/180°

- 2-level is efficient for low switching frequency
- SiC diodes can extend f_s range
- T-type topology is very efficient for medium f_s (8 – 20 kHz)
- 3-level NPC efficiency has flattest dependency on f_s
- Suitable for high f_s
- SiC diodes make only sense for very high f_s (>50 kHz)



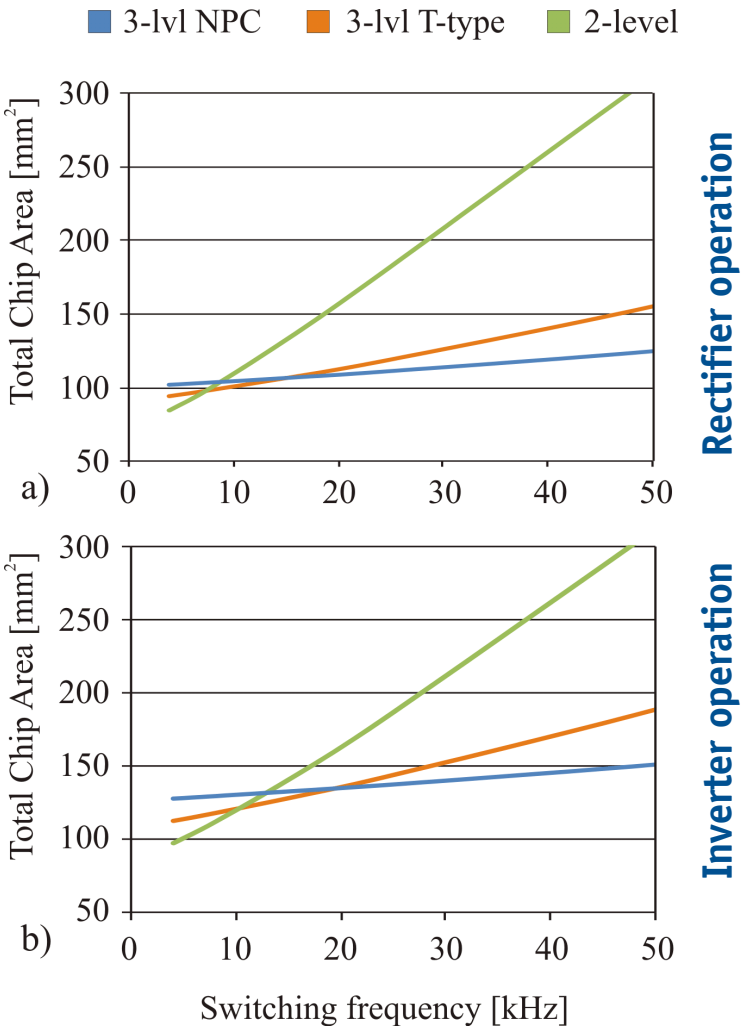
Comparison of semiconductor chip area



- Non-uniform distribution of losses over the semiconductor chips
- Low losses in a device
  - *Make chip smaller*
- High losses in a device
  - *Make chip bigger*
- Reach T_j=125°C in each chip
- Idea: **Operating point dependent chip size optimization**
  - *Fair topology comparison*
  - *Reduce module costs*
- Cheap mass market modules:
  - *Pure inverter/rectifier 3-level modules for fixed operating point (solar inverter/pfc)*

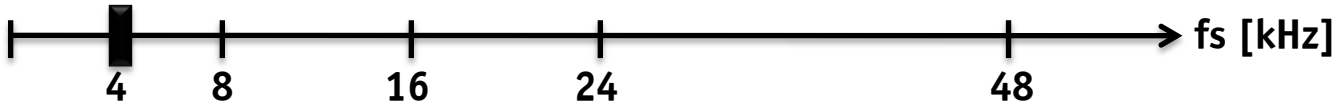
Optimization results for T_j = 125° C

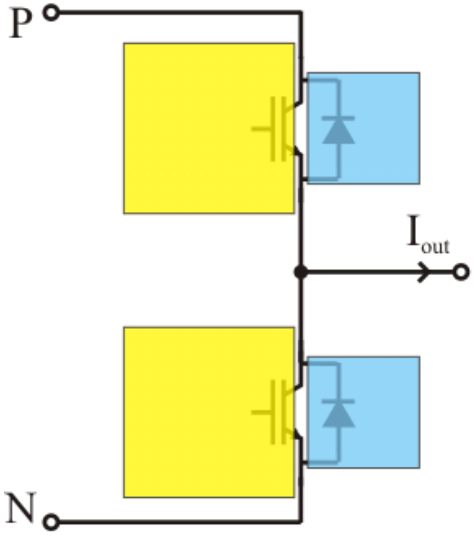
- 2-level topology
  - *Losses are concentrated in few chips*
  - *Chip size increases sharply with frequency*
  - *Total chip area of 2-level is smallest only for low switching freq. (f_s < 10 kHz)!*
- 3-level topologies
  - *Losses are distributed over many semiconductors*
  - *Chip size reduction possible*
  - *Losses increase only slightly with f_s*
  - *Distinct loss profile (Operating point)*
- Total semiconductor area:
- For f_s=35 kHz: $A_{2\text{-level}} \approx 2 * A_{3\text{-lvl NPC}}$!



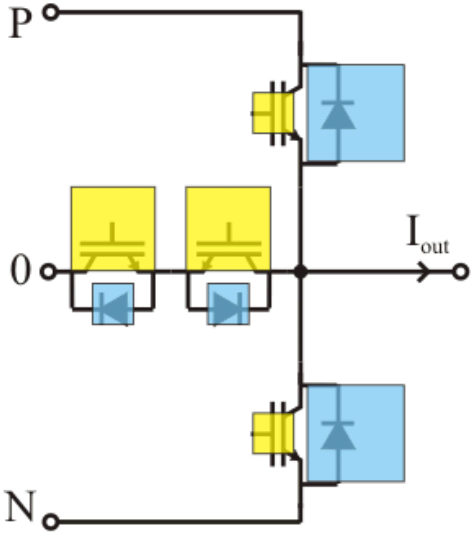
Necessary chip area for T_j=125°C (rectifier operation)

Switching frequency

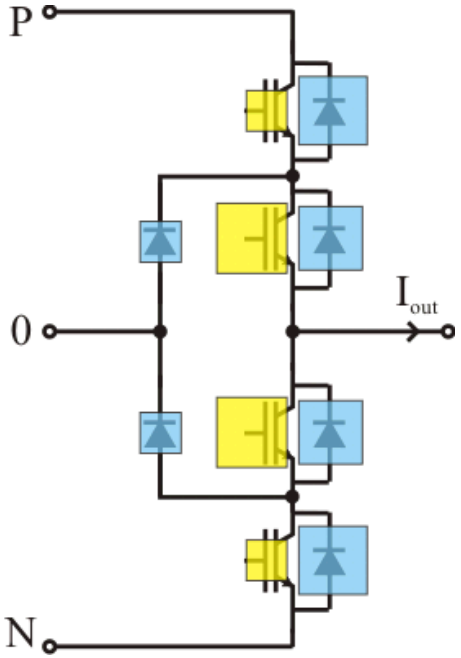




302.3 (+255%)



152.0 (+61%)

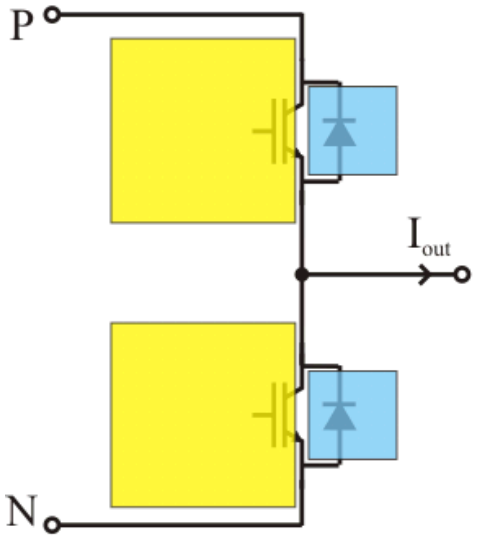


123.5 (+21%)

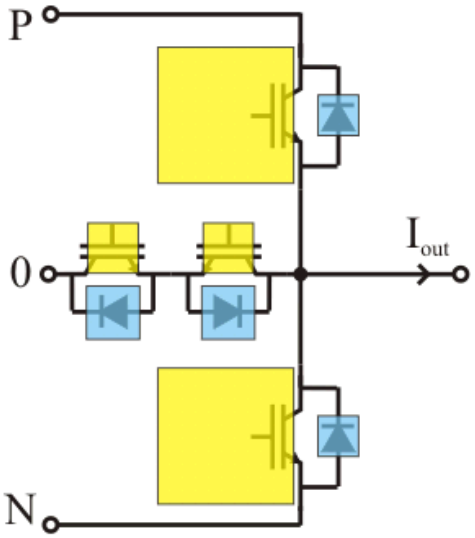
Total area [mm²] (3 phases)

Necessary chip area for T_j=125°C (inverter operation)

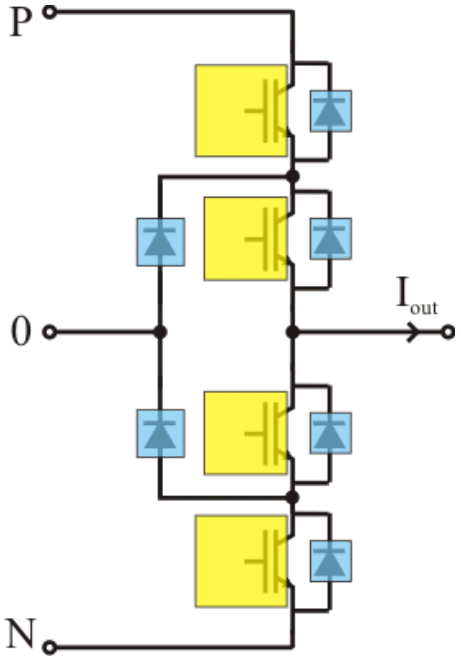
Switching frequency



303.4 (+209%)



185.2 (+64%)

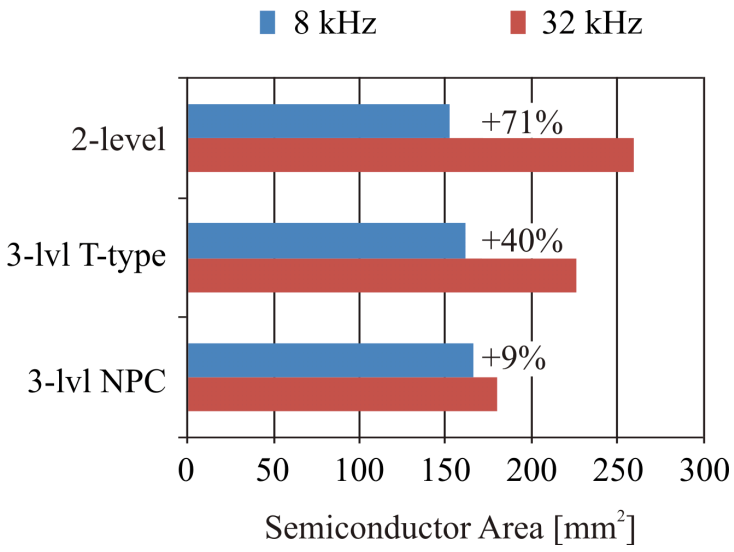


150.6 (+17%)

Total area [mm²] (3 phases)

Total semiconductor area for mixed mode operation (T_j=125°C)

- **General purpose module (mixed mode)**
  - *Take maximum chip die sizes from rectifier and inverter operation*
  - *Only a first approximation, more operating points have to be considered*
- **Increase of switching frequency over audible range (8 → 32 kHz)**
  - *Total semiconductor chip area increases by 70% for 2-level converter*
  - *Whereas the 3-lvl NPC total chip area increases only by 10%*



Passives – Boost inductor

- Boost inductor design for a max. current ripple of 20% $\hat{I}_n$
- 2-level:

$$L_{2lvl} = \frac{1}{f_s} \cdot d_{1,2lvl} \cdot \frac{2/3\, U_{dc} - \hat{U}_n}{\Delta i_{pp}}$$

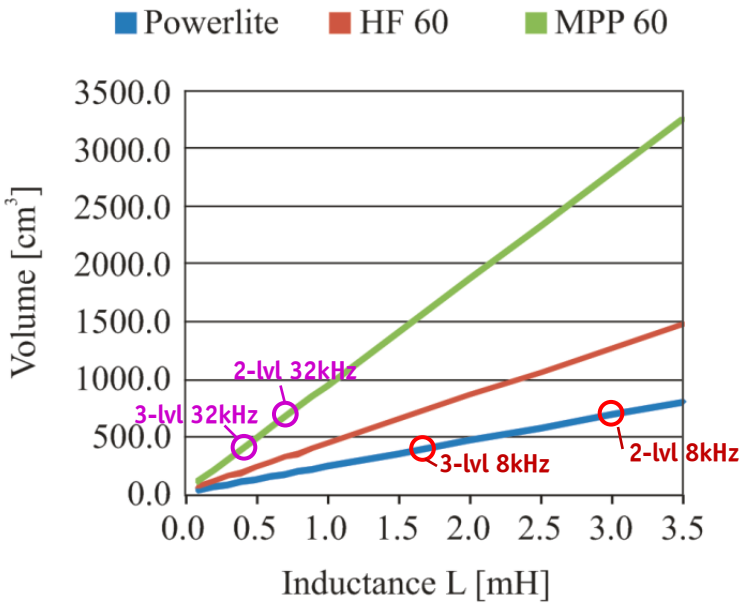
- 3-level:

$$L_{3lvl} = \frac{1}{f_s} \cdot d_{1,3lvl} \cdot \frac{2/3\, U_{dc} - \hat{U}_n}{\Delta i_{pp}}$$

- Ratio of inductances:

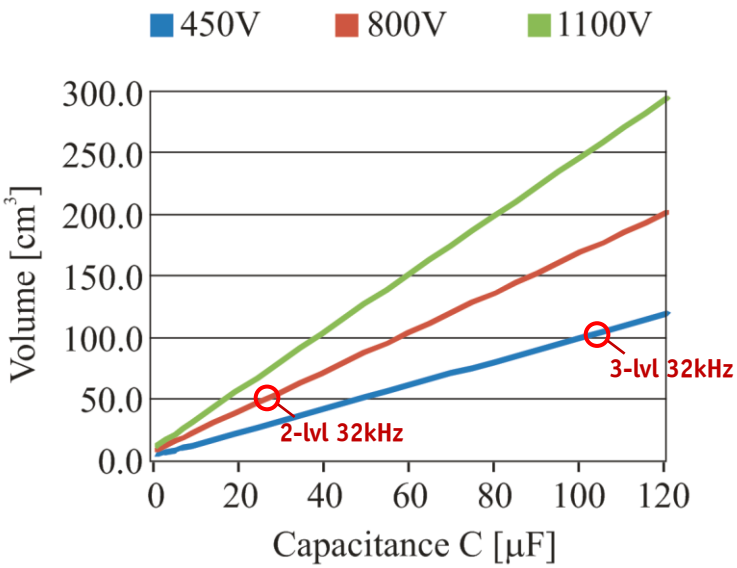
$$\frac{L_{3lvl}}{L_{2lvl}} = \frac{d_{1,3lvl}}{d_{1,2lvl}} = 55\%$$

- Volume of boost inductor can be reduced if same core material is used



Passives – DC-link capacitor

- DC-link capacitor can be designed for different aspects
  - *Energy related (control, plant)*
  - *Minimizing capacitor*
  - *Balancing (3-level)*
- 2-level:
  - $C_{dc,2lvl}$
- 3-level:
  - *Two times $2*C_{dc}$ in series: Sum of $4*C_{dc}$*
  - *Half voltage rating*
- **Total volume increases but is still small compared to the boost inductor volume**



3-level topology – Modulation

- **Space vector modulation for 3-level topology is "simple":**
  - *Main sector detection*
  - *Rotation of system to reference sector 1*
  - *Detection of subsector (rotations)*
  - *Calculation of Vector on-times*

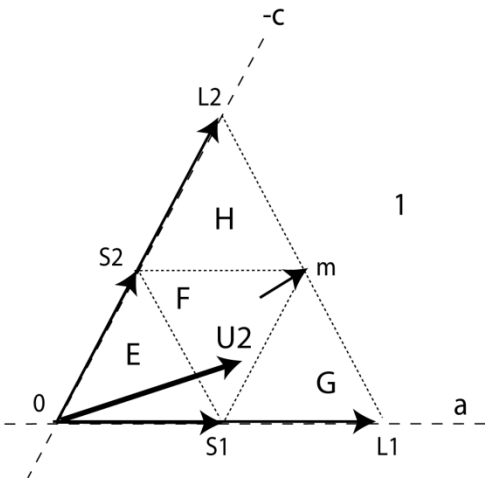
- **Space vector modulation [1]**

E
$$T_{s1} = \alpha \times 2 \times T_c \times \sin(60° - \theta)$$
$$T_{s2} = \alpha \times 2 \times T_c \times \sin\theta$$
$$T_0 = T_c - T_{s1} - T_{s2}$$

F
$$T_{s1} = T_c - \alpha \times 2 \times T_c \times \sin\theta$$
$$T_{s2} = T_c - \alpha \times 2 \times T_c \times \sin(60° - \theta)$$
$$T_m = \alpha \times 2 \times T_c \times \sin(60° + \theta) - T_c$$

G
$$T_{s1} = 2T_c - \alpha \times 2 \times T_c \times \sin(60° + \theta)$$
$$T_{L1} = \alpha \times 2 \times T_c \times \sin(60° - \theta) - T_c$$
$$T_m = \alpha \times 2 \times T_c \times \sin\theta$$

H
$$T_{s2} = 2T_c - \alpha \times 2 \times T_c \times \sin(60° + \theta)$$
$$T_{L2} = \alpha \times 2 \times T_c \times \sin\theta - T_c$$
$$T_m = \alpha \times 2 \times T_c \times \sin\theta(60° - \theta)$$



Space vector U_2 is always modulated with the 3 closest discrete space vectors

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Swiss Federal Institute of Technology Zurich

[1] Kaku, B.; Switching loss minimised space vector PWM method for IGBT three-level inverter , IEE Proceedings Electric Power Applications 1997.

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3-level voltage source rectifier – Optimal Clamping

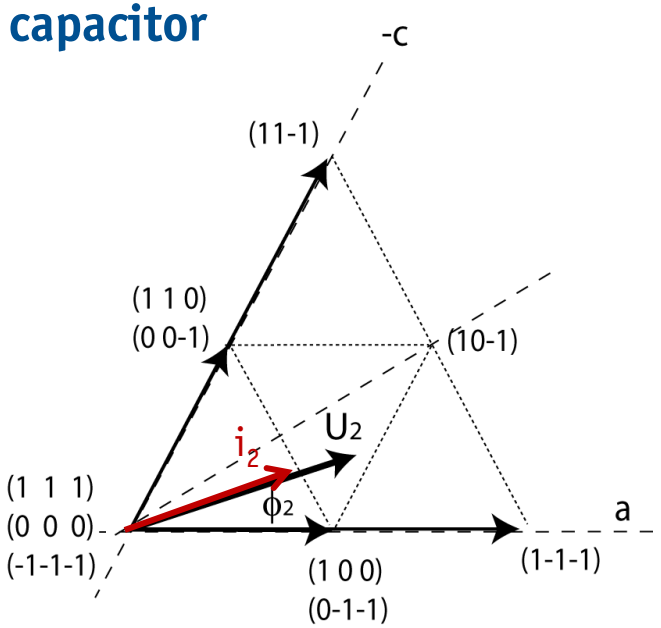
- Optimal clamping is possible
  - *Highest phase current is not switched*
  - *Switching losses get reduced by ≈30%*
- Vector Sequence defines clamping scheme
- Periodically loads top and bottom dc-link capacitor

  - $0 < f_2 < 30°$:
  - Phase A clamped to positive DC-link rail
  - i_A not switched at maximum amplitude

  (1 1 0) (1 0 0) (1 0-1) (1 0 0) (1 1 0)

  - $30° < f_2 < 60°$:
  - Phase C clamped to negative DC-link rail
  - i_C not switched at maximum amplitude

  (0-1-1) (0 0-1) (1 0-1) (0 0-1) (0-1-1)

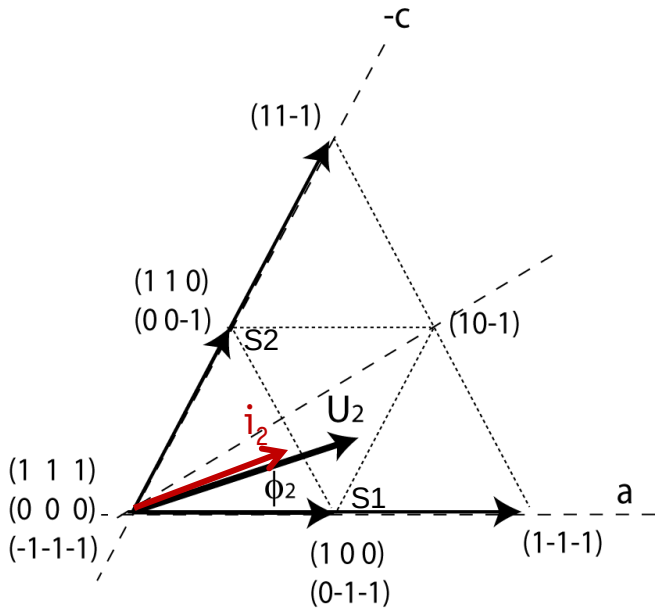


3-level voltage source rectifier - Balancing

- The DC-link capacitors may be loaded unbalanced
- Small vectors S1 and S2:
  - *Redundant vectors invert current flowing into capacitor mid-point*
  - *Alternative switching sequences exist:*

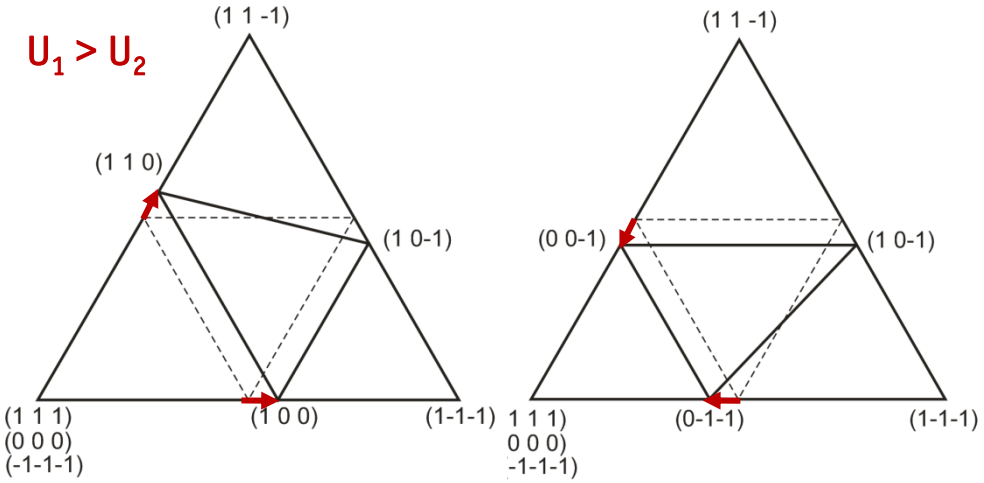
Charge C1: (1 1 0) (1 0 0) (1 0-1) (1 0 0) (1 1 0)
Charge C2: (0-1-1) (0 0-1) (1 0-1) (0 0-1) (0-1-1)

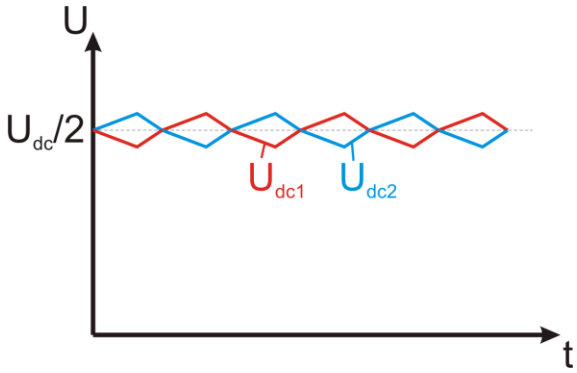
- Choose appropriate sequence depending on voltage unbalance with hysteresis controller
- Optimal clamping not always possible



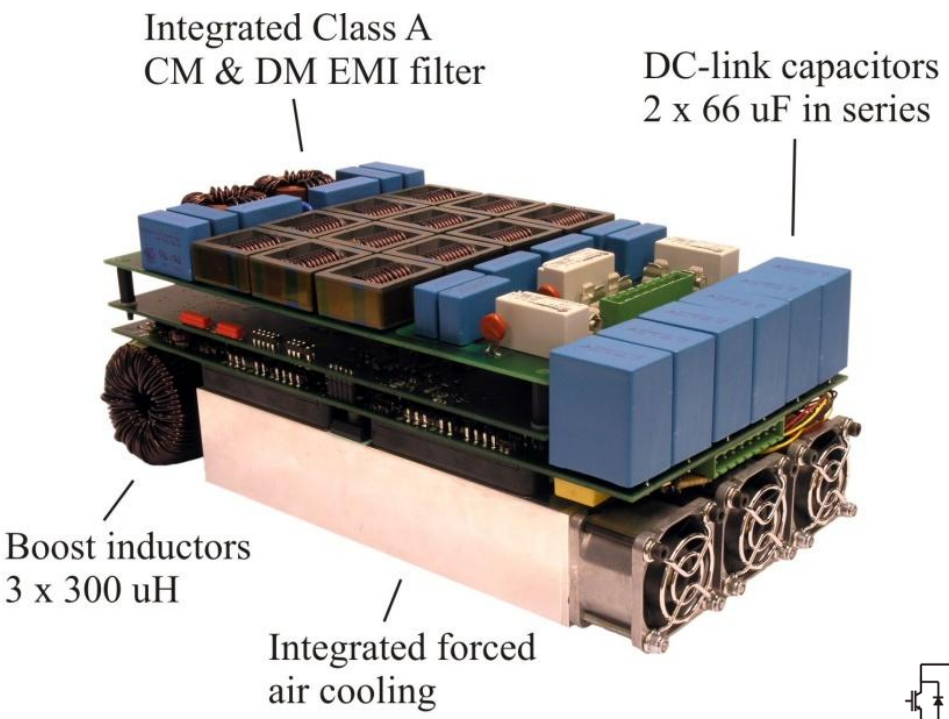
Modulation with link unbalance

- Active vectors move due to link unbalance
- Sector borders move
- Redundant middle vectors move in opposite direction
- Sector detection and on-time calculation can be adapted
- AC-AC converters:
  - Inverter stage
    - *optimal clamping (higher current amplitude)*
  - Rectifier stage
    - *Balancing*



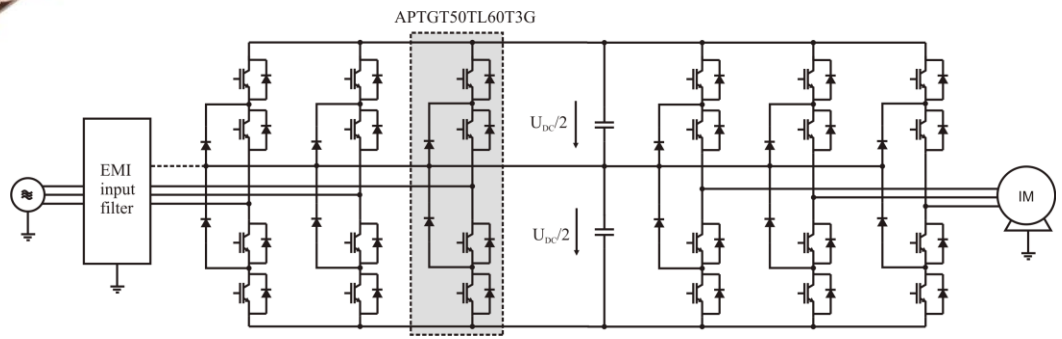


3LVL NPC – AC-AC back-to-back converter prototype

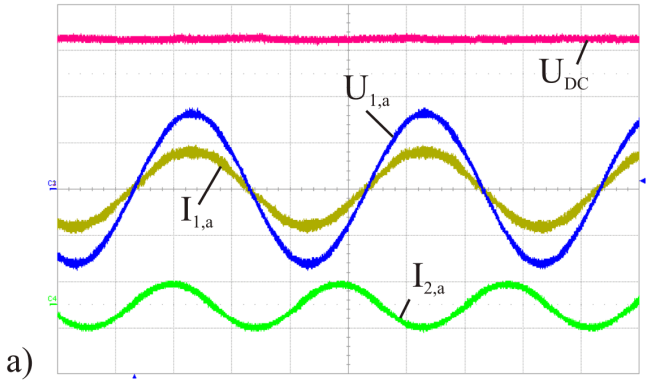


Specifications

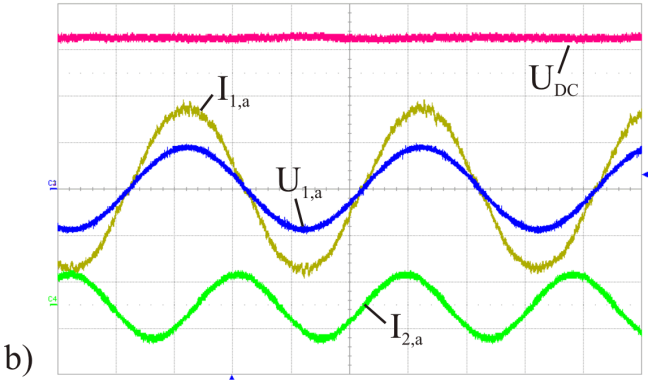
- P_n = 10 kW
- U_n = 230 V RMS
- U_{dc} =700 V
- f_n = 50 Hz ... 800 Hz
- f_s = 48 kHz
- Power density: 2.9 kW/l
- Weigth: 5 kg
- Efficiency: 96% (SiC 96.5%)
- CISPR Class A (B possible)



3LNPC-VLBBC Prototype 50Hz Operation



a)



b)

a) Operating conditions:

P_1=4kW, U1=230V, f_1=50 Hz, f_2=70 Hz

THD I_1 = 3.0%

THD I_2 = 2.2%

Scale: t=5ms/div, I_1=10A/div, I_2=24A/div, U_1=200V/div, U_{dc}=200V/div

b) Operating conditions:

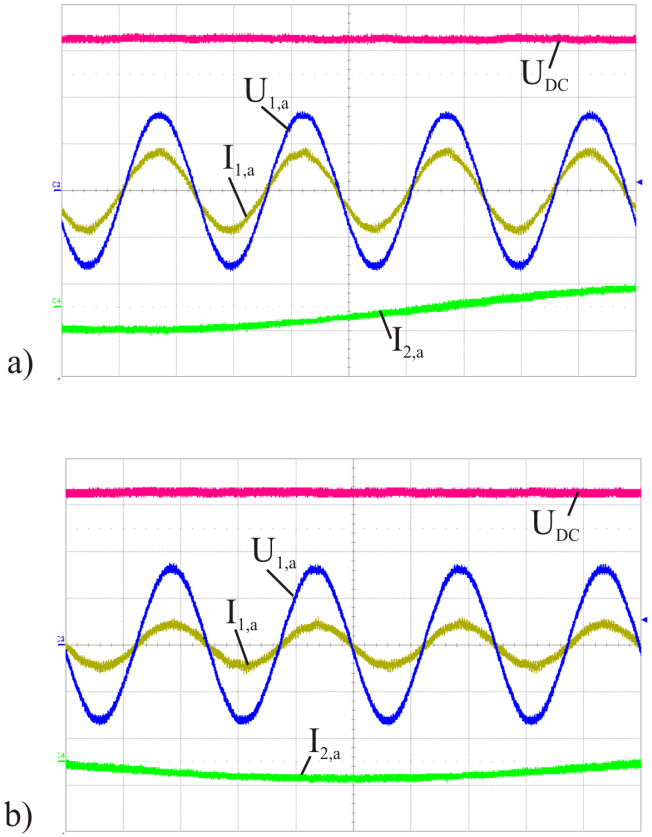
P_1=8kW, U_1=230V, f_1=50 Hz, f_2=70 Hz

THD I_1 = 3.5%

THD I_2 = 2.2%

Scale: t=5ms/div, I_1=10A/div, I_2=24A/div, U_1=350V/div, U_{dc}=200V/div

3LNPC-VLBBC Prototype 800Hz Operation



a) Operating conditions:

P_1=4kW, U_1=230V, f_1=800 Hz, f_2=70 Hz

THD I_1 = 2.9%

THD I_2 = 2.2%

Scale: t=500µs/div, I_1=10A/div, I_2=24A/div, U_1=200V/div, U_{dc}=200V/div

b) Operating conditions:

P_1=2kW, U_1=230V, f_1=800 Hz, f_2=70 Hz

Capacitive input filter current is fully compensated even at low power. Unity power factor is achieved.

Summary

- 3-phase 3-level converters could be used for low voltage applications with high switching frequency
- Desirable properties:
  - *High f_s possible ➔ high dynamics, no audible noise, slightly reduced passives (weight, costs)*
  - *High efficiency*
  - *Loss distribution over many chips*
  - *Only small chip area necessary ➔ costs could be reduced*
  - *Only small part count increase (3-level T-type)*
  - *High optimization potential for pure inverter / rectifier modules*
- Remaining drawbacks:
  - *Increased complexity*
  - *Increased part count (3-level NPC)*

Literature

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Thank You !

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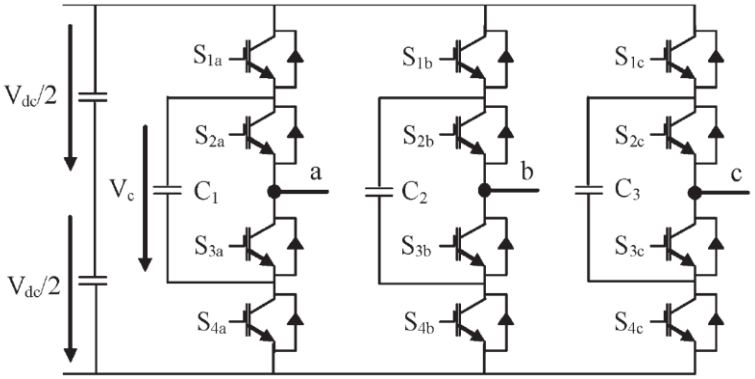
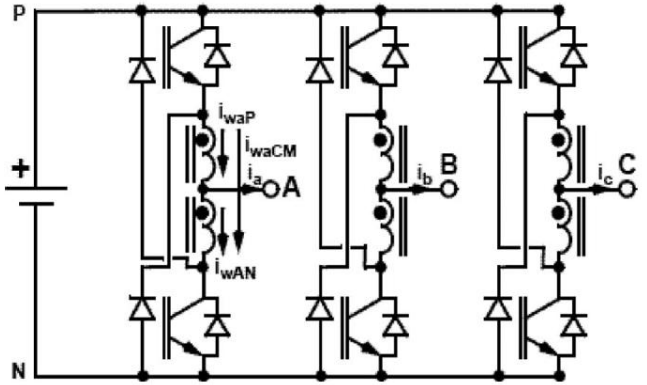
Alternative three-level concepts

Flying Capacitor 3-level converter



[1]

Coupled inductor 3-level converter



[2]

[1]: Fazel, S.S.; Bernet, S.; Krug, D.; Jalili, K.; , "Design and Comparison of 4-kV Neutral-Point-Clamped, Flying-Capacitor, and Series-Connected H-Bridge Multilevel Converters," *IEEE Transactions on Industry Applications,* , vol.43, no.4, pp.1032-1040, July-aug. 2007

[2]: Ewanchuk, J.; Salmon, J.; Knight, A.M.; , "Performance of a High-Speed Motor Drive System Using a Novel Multilevel Inverter Topology," *IEEE Transactions on Industry Applications,*, vol.45, no.5, pp.1706-1714, Sept.-oct. 2009