



Eidgenössische Technische Hochschule Zürich  
Swiss Federal Institute of Technology Zurich



**ECPE Roadmap  
2025 Workshop**

# Vision – Power Electronics 2025

**Johann W. Kolar**

Swiss Federal Institute of Technology (ETH) Zurich  
Power Electronic Systems Laboratory  
[www.pes.ee.ethz.ch](http://www.pes.ee.ethz.ch)



# Power Electronics 2.0

**Johann W. Kolar**

Swiss Federal Institute of Technology (ETH) Zurich  
Power Electronic Systems Laboratory  
[www.pes.ee.ethz.ch](http://www.pes.ee.ethz.ch)



# Outline

- ▶ **Evolution of Power Electronics**
- ▶ **Performance Trends / Enablers & Barriers / New Paradigms**
- ▶ **Characteristics of Power Electronics 2.0**
- ▶ **Conclusions**

## Evolution of Power Electronics



# History and Development of the Electronic Power Converter

E. F. W. ALEXANDERSON  
FELLOW AIEE

E. L. PHILLIPI  
NONMEMBER AIEE

**T**HE TERM “electronic power converter” needs some definition. The object may be to convert power from direct current to alternating current for d-c power transmission, or to convert power from one frequency into another, or to serve as a commutator for operating an a-c motor at variable speed, or for transforming high-voltage direct current into low-voltage direct current. Other objectives may be mentioned. It is thus evidently not the objective but the means which characterizes the electronic power converter. Other names have been used tentatively but have not been accepted. The emphasis is on electronic means and the term is limited to conversion of power as distinguished from electric energy for purposes of communication. Thus the name is a definition.

Paper 44-143, recommended by the AIEE committee on electronics for presentation at the AIEE summer technical meeting, St. Louis, Mo., June 26-30, 1944. Manuscript submitted April 25, 1944, made available for printing May 18, 1944.

E. F. W. ALEXANDERSON and E. L. PHILLIPI are with the General Electric Company, Schenectady, N. Y.

654 TRANSACTIONS

Alexanderson, Phillipi—Electronic Converter

ELECTRICAL ENGINEERING

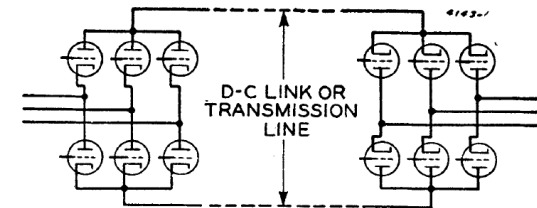


Figure 1. Electronic converter, dual-conversion type

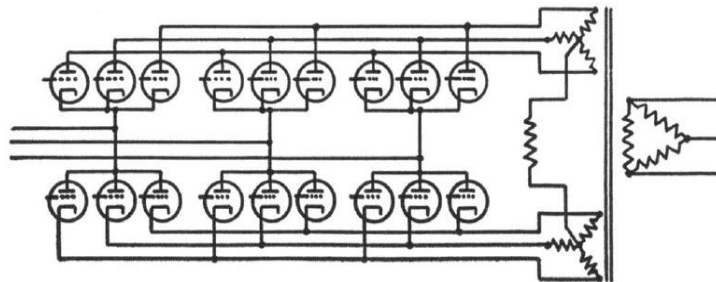


Figure 4 (left).  
Single-conversion-type  
frequency changer

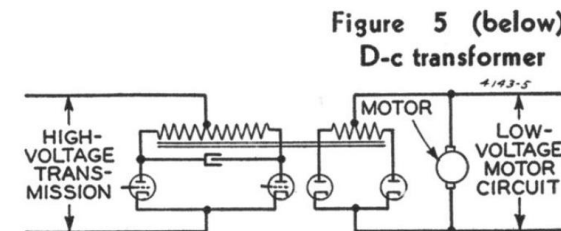


Figure 5 (below).  
D-c transformer



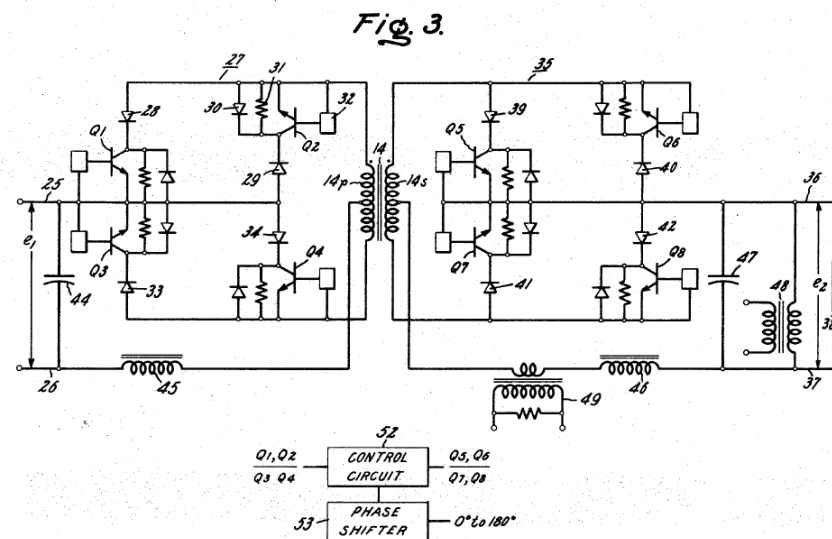
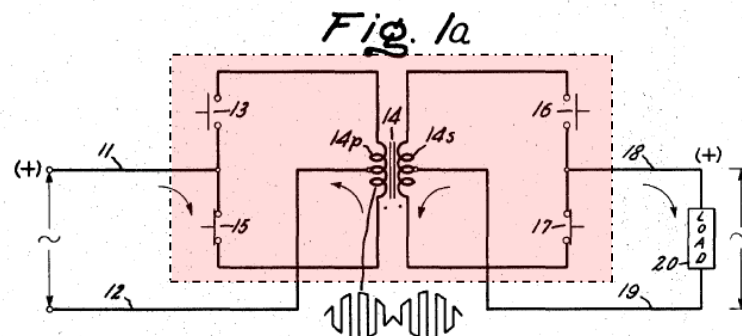
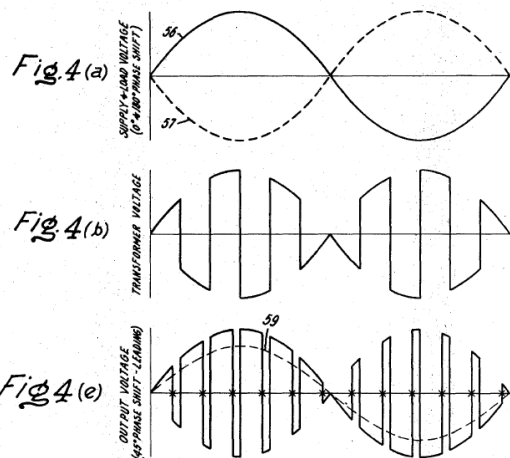
# United States Patent Office

3,517,300

Patented June 23, 1970

1970!

3,517,300  
**POWER CONVERTER CIRCUITS HAVING A  
HIGH FREQUENCY LINK**  
William McMurray, Schenectady, N.Y., assignor to Gen-  
eral Electric Company, a corporation of New York  
Filed Apr. 16, 1968, Ser. No. 721,817  
Int. Cl. H02m 5/16, 5/30  
U.S. Cl. 321—60 14 Claims



# United States Patent [19]

Brewster et al.

[11] 4,143,414

[45] Mar. 6, 1979

1979!

## [54] THREE PHASE AC TO DC VOLTAGE CONVERTER WITH POWER LINE HARMONIC CURRENT REDUCTION

[75] Inventors: Roger F. Brewster; Alfred H. Barrett, both of Santa Barbara, Calif.

[73] Assignee: General Motors Corporation, Detroit, Mich.

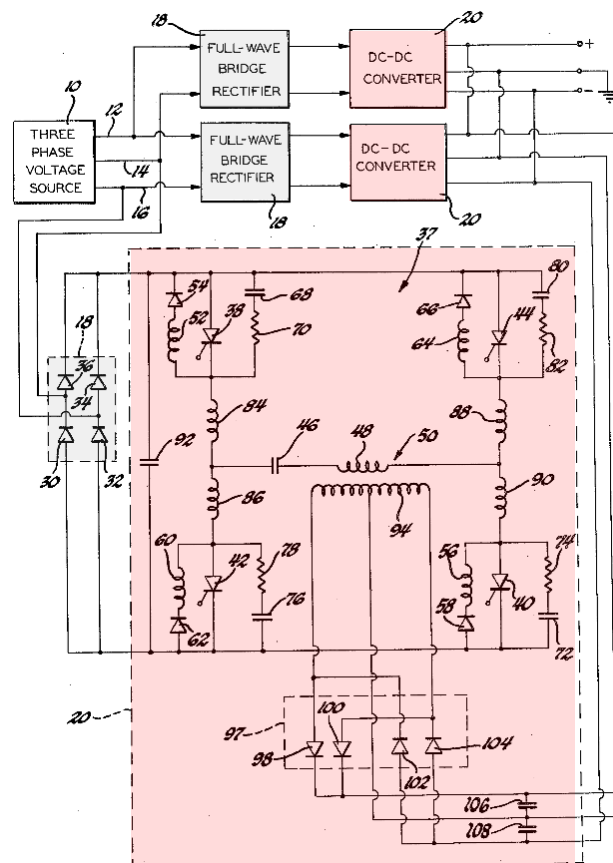
[21] Appl. No.: 894,739

[22] Filed: Apr. 10, 1978

## [57] ABSTRACT

A three phase AC to DC voltage converter includes separate single phase AC to DC converters for each phase of a three phase source with the DC voltage output of the three converters paralleled and controlled to provide necessary regulation. Each of the single phase AC to DC converters includes a full-wave bridge rectifier feeding a substantially resistive load including an inverter and a second single phase full-wave bridge rectifier. To the extent that each inverter and second single phase full-wave bridge rectifier approximate a resistive load, the source current harmonics are reduced. Additionally, the triplen harmonics produced in the three phase source lines by each of the three AC to DC converters are cancelled by the triplen harmonics produced in the three phase source lines by the remaining two AC to DC converters.

2 Claims, 1 Drawing Figure



## United States Patent [19]

**Mitchell**

[11] **4,412,277**

[45] **Oct. 25, 1983**

# 1983 !

[54] AC-DC CONVERTER HAVING AN IMPROVED POWER FACTOR

[75] Inventor: **Daniel M. Mitchell**, Cedar Rapids,  
Iowa

[73] Assignee: **Rockwell International Corporation,**  
El Segundo, Calif.

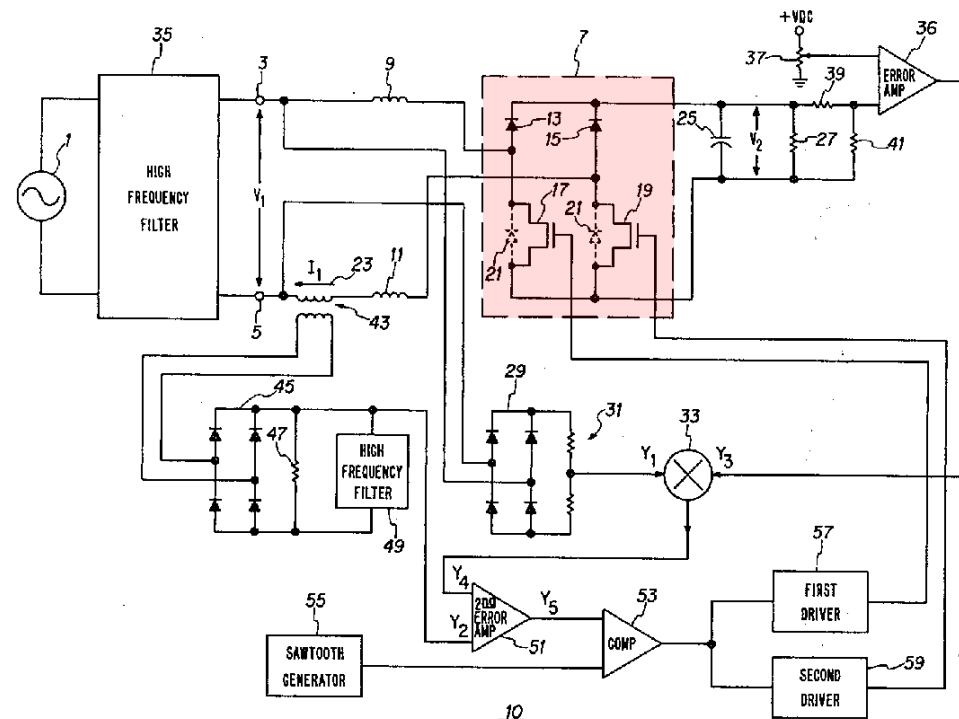
[21] Appl. No.: 414,757

[22] Filed: **Sep. 3, 1982**

[57] **ABSTRACT**

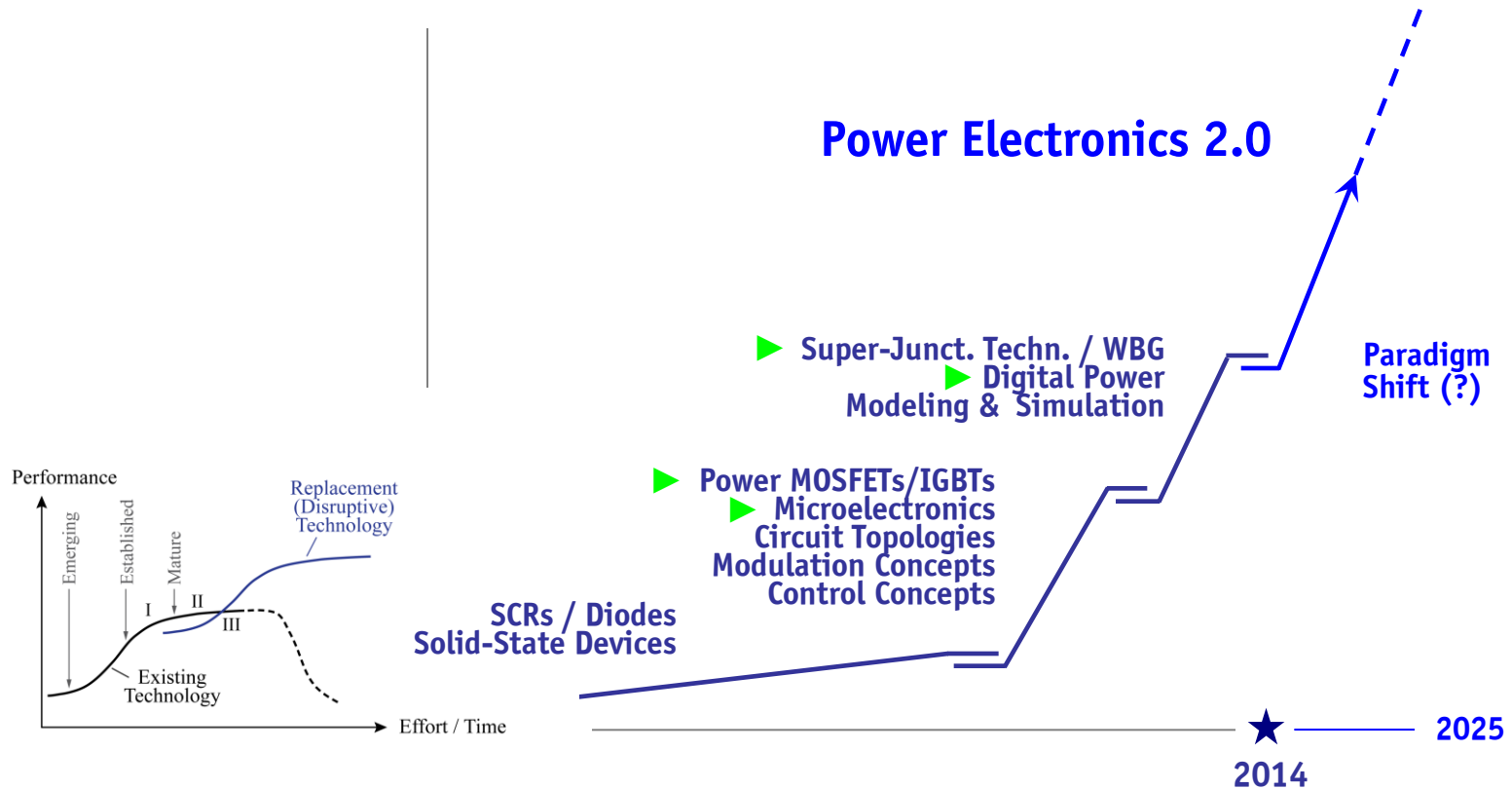
An AC to DC converter utilizes a first power converter for converting an AC signal to a DC signal under the control of a control signal. The control signal is generated by a control circuit that includes a first analog generator that provides a first signal that is analogous to the voltage of the AC signal that is to be converted. A second analog generator generates a second signal that is analogous to the current of the AC signal that is to be converted and a third analog generator generates a third signal that is analogous to the voltage of the DC output signal. The third signal and the first signal are multiplied together to obtain a fourth signal. The control signal is generated from the fourth signal and the second signal and is used to control the power converter such that the waveform of the current of the AC signal is limited to a sinusoidal waveform of the same frequency and phase as the AC signal.

### 8 Claims, 2 Drawing Figures





## ► Technology S-Curve



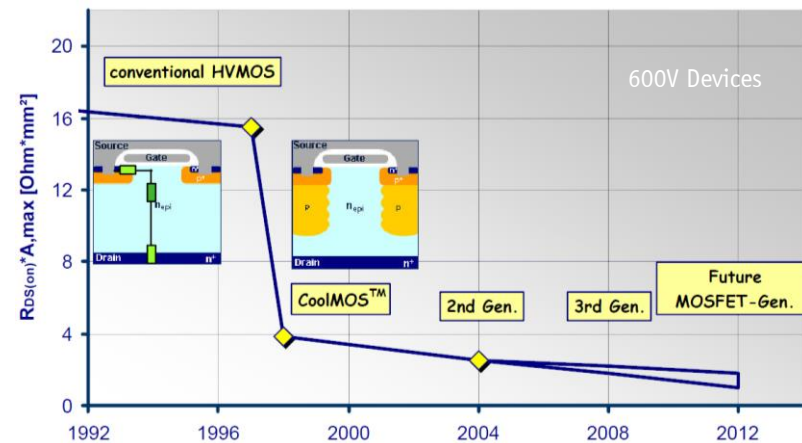
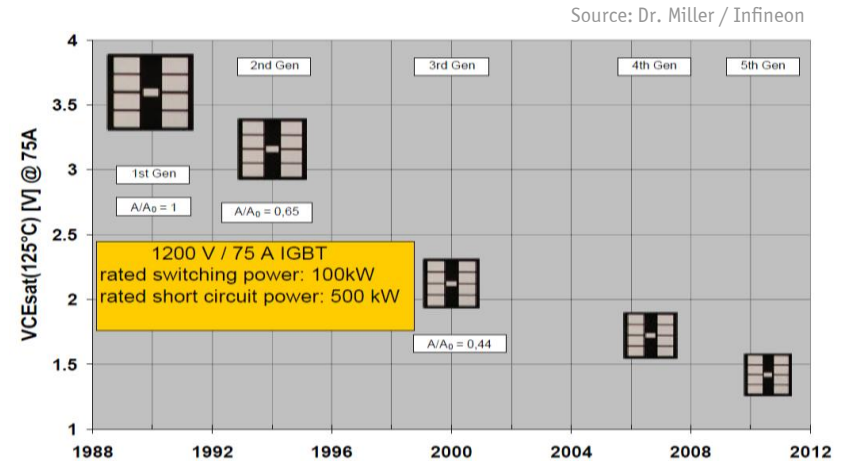
## ► Technology S-Curve

### ■ Sub-S-Curves

- Overall Development Defined by Improvement of Core Technologies

### ■ Importance

1. Power Semiconductors (incl. Package)
2. Microelectronics / Signal Processing
3. Topologies
4. Analysis / Modeling & Simulation

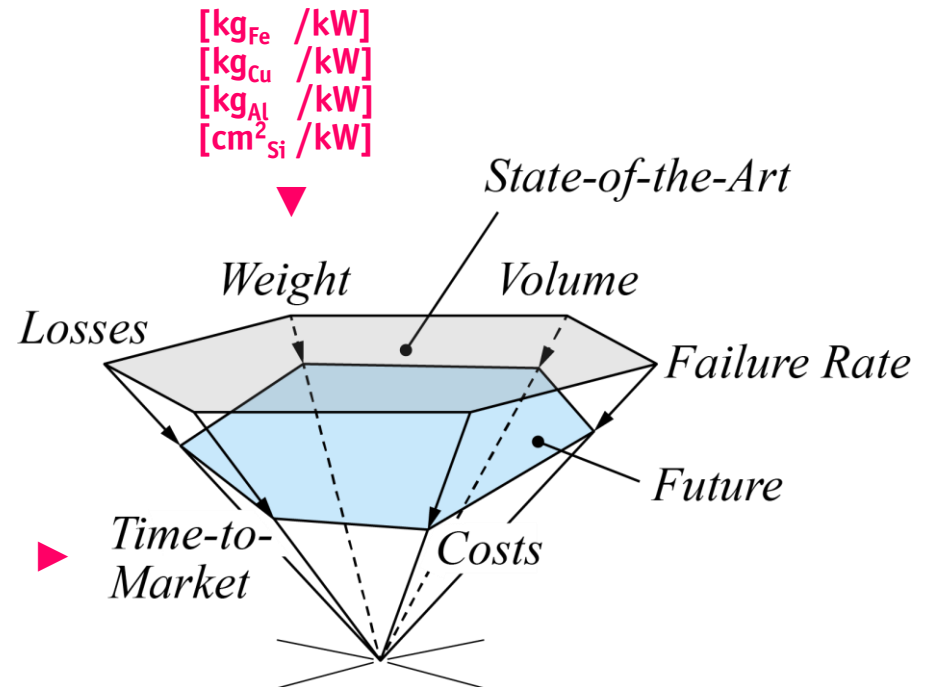


Performance Indices  
→ Coupling & Limits

## ► Power Electronics Converters Performance Trends

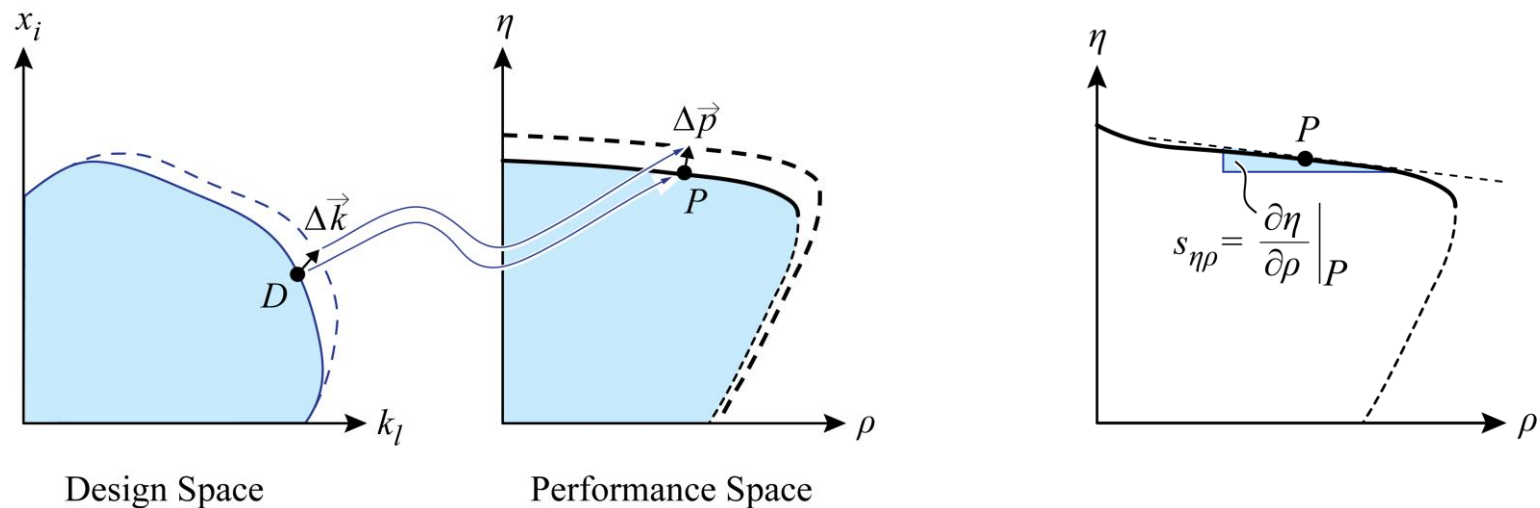
### ■ Performance Indices

- Power Density [kW/dm<sup>3</sup>]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/\$]
- Relative Losses [%]
- Failure Rate [h<sup>-1</sup>]



## ► Analysis of Performance Limits → Pareto Front

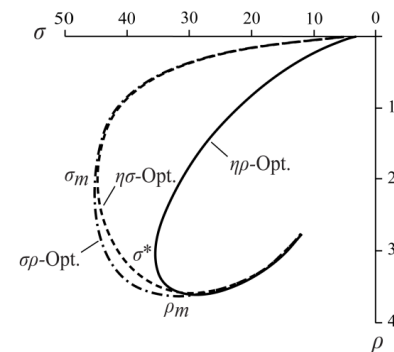
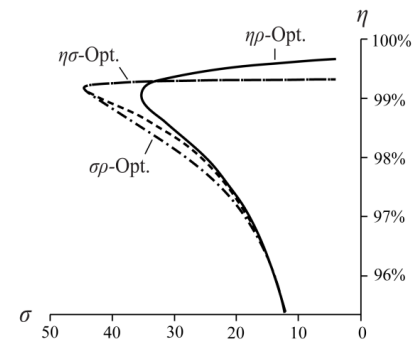
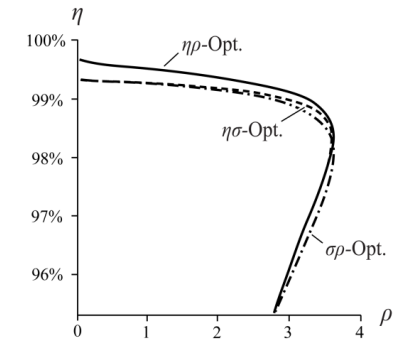
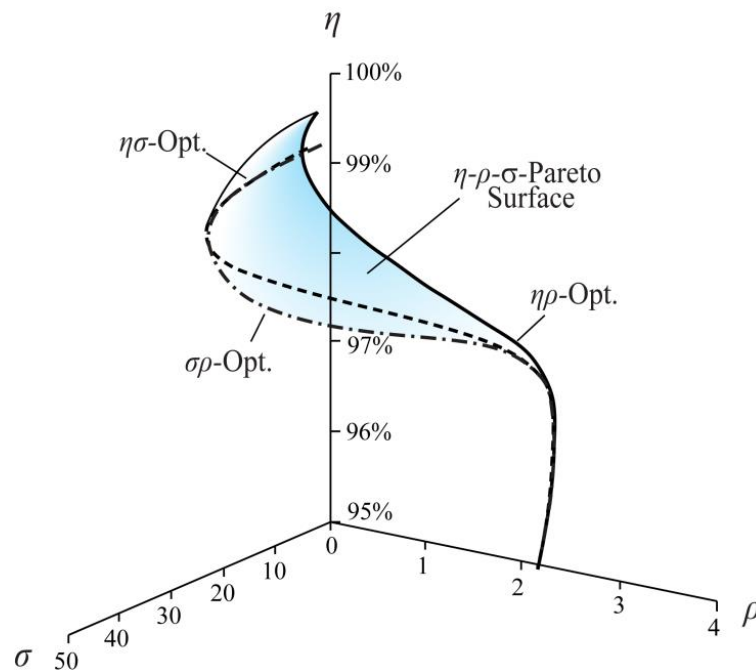
- **Sensitivity** to Technology Advancements (Example:  $\eta$ - $\rho$ -Pareto Front)
- Trade-off Analysis





## ► $\eta$ - $\rho$ - $\sigma$ -Pareto Surface

■  $\sigma$ : kW/\$



## Experimental Verification of Performance Limits

→ 3-ph. VIENNA Rectifier  
→ 1-ph. PFC Rectifiers

## ► Demonstrator #1 → 3-ph. VIENNA Rectifier

### ■ Specifications

$$U_{LL} = 3 \times 400 \text{ V}$$

$$f_N = 50 \text{ Hz} \dots 60 \text{ Hz or } 360 \text{ Hz} \dots 800 \text{ Hz}$$

$$P_o = 10 \text{ kW}$$

$$U_o = 2 \times 400 \text{ V}$$

$$f_s = 250 \text{ kHz}$$

### ■ Characteristics

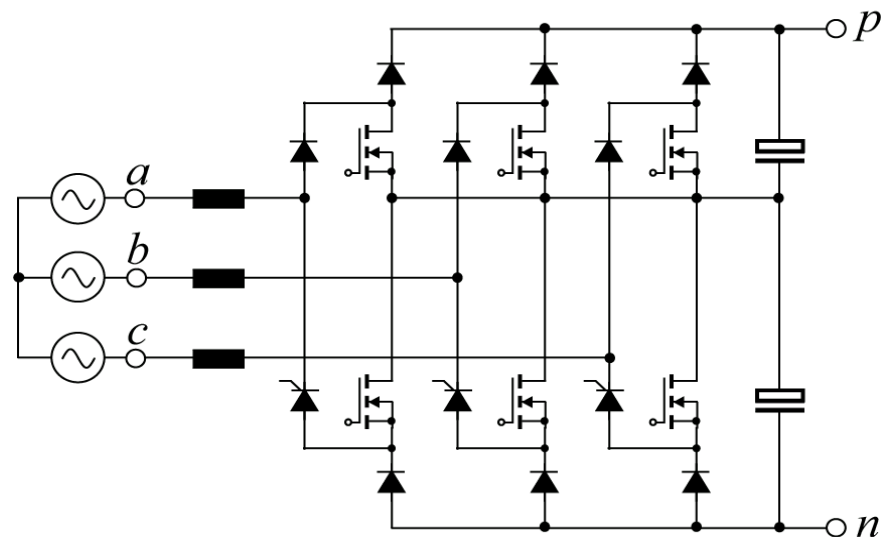
$$\eta = 96.8 \%$$

$$\text{THD}_i = 1.6 \% \text{ @ } 800 \text{ Hz}$$

$$10 \text{ kW/dm}^3$$

$$3.3 \text{ kg } (\approx 3 \text{ kW/kg})$$

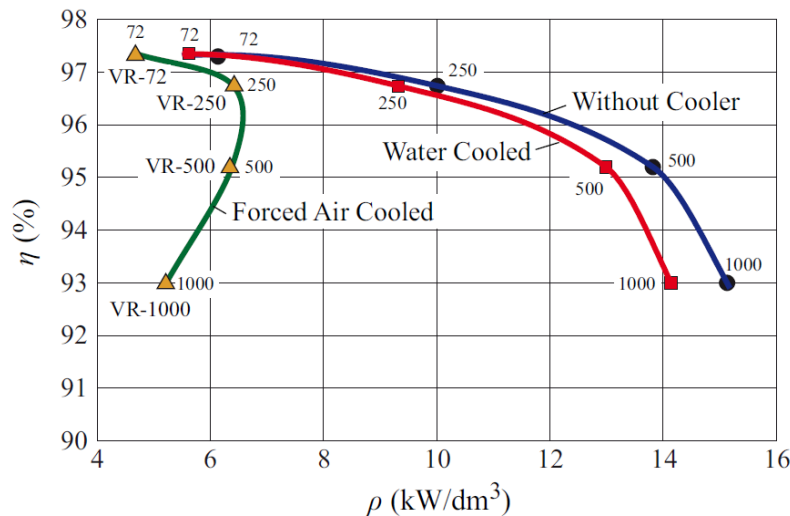
Dimensions: 195 x 120 x 42.7 mm<sup>3</sup>



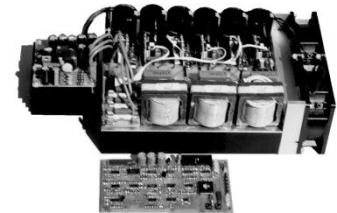
## ► Demonstrator #1 → 3-ph. VIENNA Rectifier

### ■ Experimental Evaluation of Generation 1 – 4 of VIENNA Rectifier Systems

— Switching Frequency of  $f_s = 250$  kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality THD<sub>i</sub>



$f_s = 50$  kHz  
 $\rho = 3$  kW/dm<sup>3</sup>



$f_s = 72$  kHz  
 $\rho = 4.6$  kW/dm<sup>3</sup>



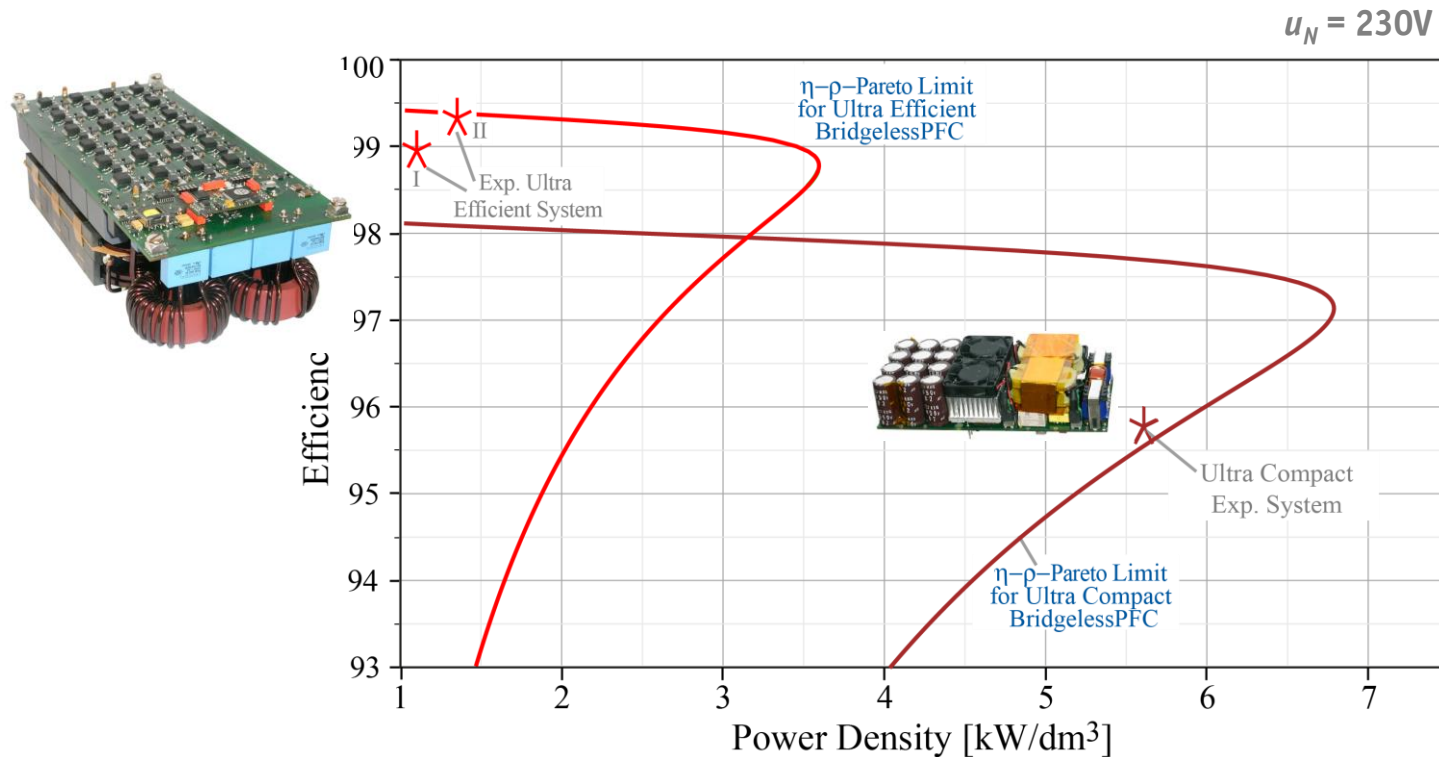
$f_s = 250$  kHz  
 $\rho = 10$  kW/dm<sup>3</sup>  
(164 W/in<sup>3</sup>)  
Weight = 3.4 kg



$f_s = 1$  MHz  
 $\rho = 14.1$  kW/dm<sup>3</sup>  
Weight = 1.1 kg



## ► Demonstrator #2 → 1-ph. Bridgeless PFC Rectifiers

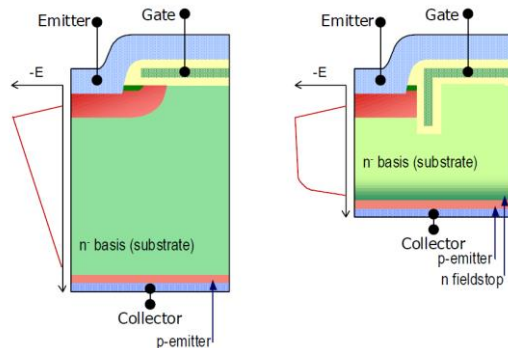


Power Density is Based on Net Volumes → Scaling by 0.6-0.8 Necessary

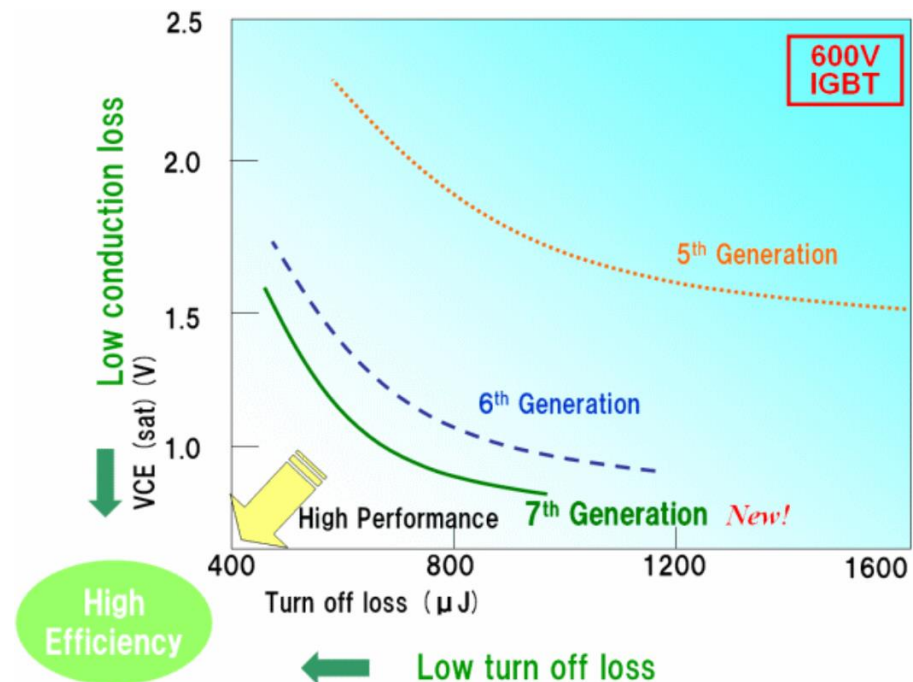


## ► Pareto Front of Power Semiconductors

### ■ Trade-Off Between Conduction and Switching Losses

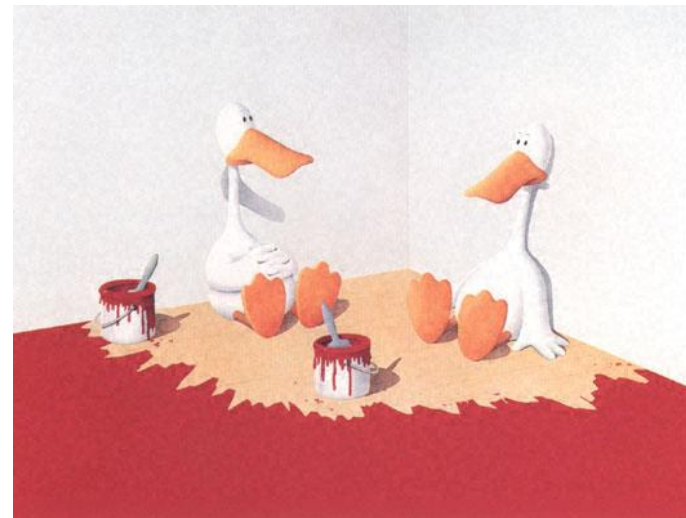
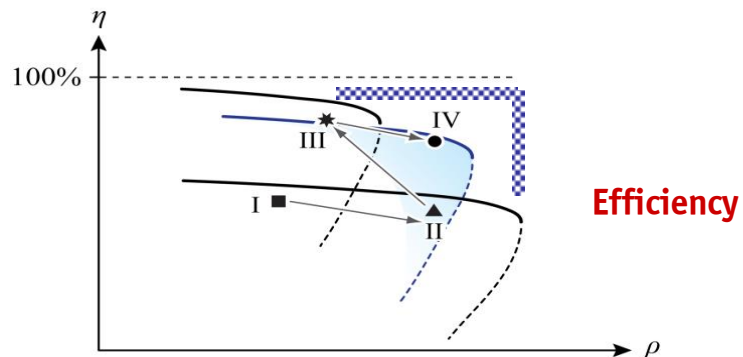


— Improvement Through Changes in Device Structure → E.g. Introduction of Trench Gate and Fieldstop Layer



## ► Observation

- “Standard” / Relatively High Performance Solutions for Nearly All Key Applications Existing Today !



- Very Limited Room for Further Perform. Improvement → only COST Reduction (!)

## ► General Remark

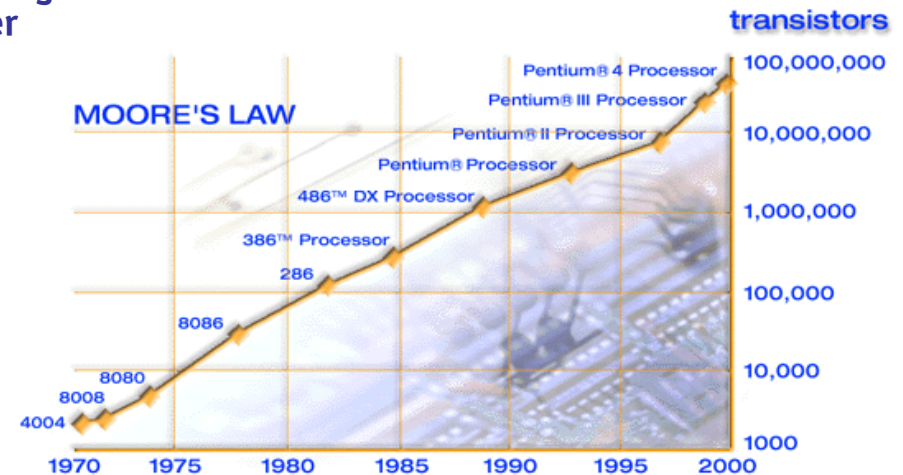
→ There is No “Moore's Law” in Power Electronics !

### ■ Example: Scaling Law of Transformers

$$A_{Core} A_{Wdg} = \frac{\sqrt{2}}{\pi} \frac{P_t}{k_W J_{rms} \hat{B}_{max} f}$$

$\hat{B}_{max}$  ... Very Slow Technology Progress  
 $J_{rms}$  ... Limited by Conductivity – No Change  
 $f$  ... Limited by HF Losses & Converter & General Thermal Limit

### ■ No Fundamentally New Concepts of Passives → We are Left with Progress in Material Science (Takes Decades)



## ► General Remark (2)

### ■ Expected (Slow) Technology Progress of Passives

Source: EPCOS

#### — Foil Capacitors

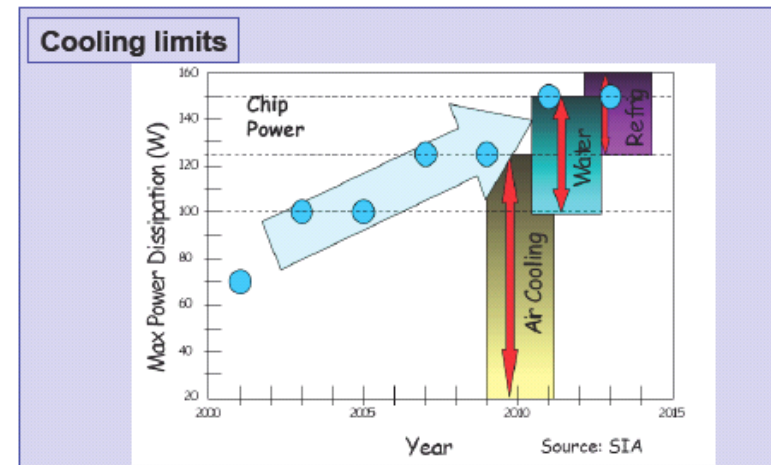
OPP = Oriented Polypropylene  
PHD = Advanced OPP  
COC = Cycloolefine Copolymers

	2000	2005	2010	2015
Energy Density	100%	100%	110%	120%
Film Material	OPP	PHD	COC	?
Max. Temperature	105 °C	115 °C	150 °C	160 °C
Self Inductance	60 nH	30 nH	15 nH	10 nH

#### — Cooling

Air Cooling  
Water Cooling  
Refrigeration Technologies

... similar for Magnetics





## Next Evolutional Step ?

“... Prediction is Very Difficult,  
Especially if it's About the Future ...”

(N. Bohr)



\_\_\_\_\_ **“Optimistic” View** \_\_\_\_\_→

# ► Optimistic View → Break Through (Shift) the Barriers !

## ■ Degrees of Freedom

- Topologies
- Modulation Schemes
- Control Schemes
- etc.

... only if not Fundamental  
Physical Properties

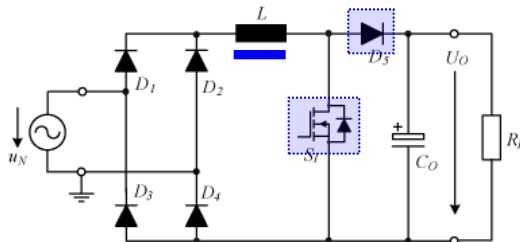


## ■ Remark: Designer's Point of View (Given Semiconductors & Base Materials)

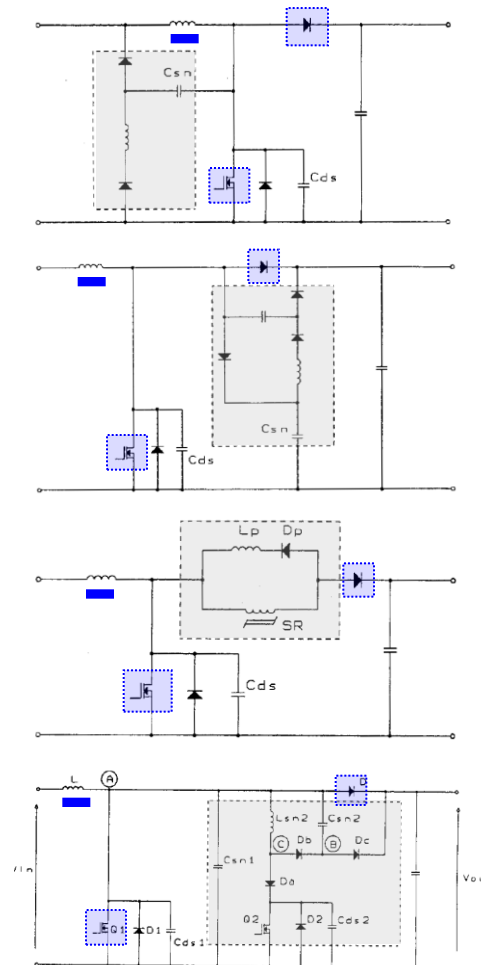


## ► "Snubbers" (1)

### — Example: 1-ph. Telekom Boost-Type PFC Rectifier



- Complexity Increases Exp. if "Natural" Limit of a Technology is Approached
- Next Step in Semiconductor Technologies Makes Snubbers Obsolete → SiC Diodes



R. Streit/  
D. Tollik 1992



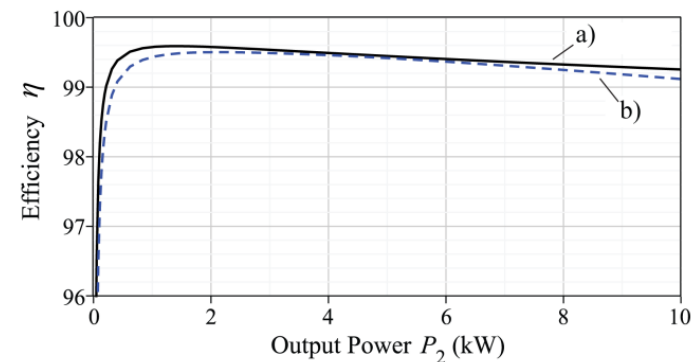
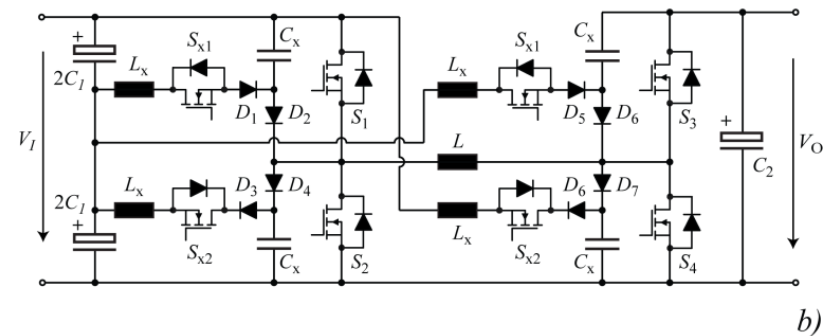
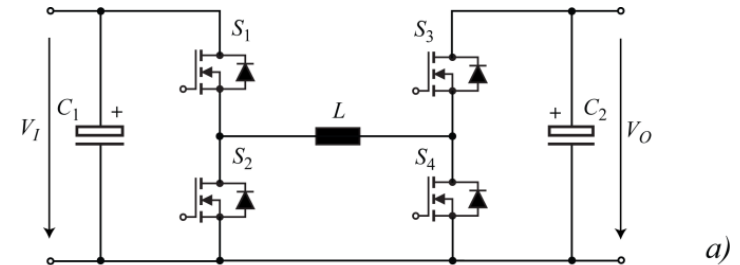
## ► "Snubbers" (2)

- Example: Non-Isolated Buck+Boost DC-DC Converter for Automotive Applications



98% Efficiency  
29kW/dm<sup>3</sup>

- Instead of Adding Aux. Circuits  
Change Operation of BASIC (!) Structure –  
"Natural" Performance Limit

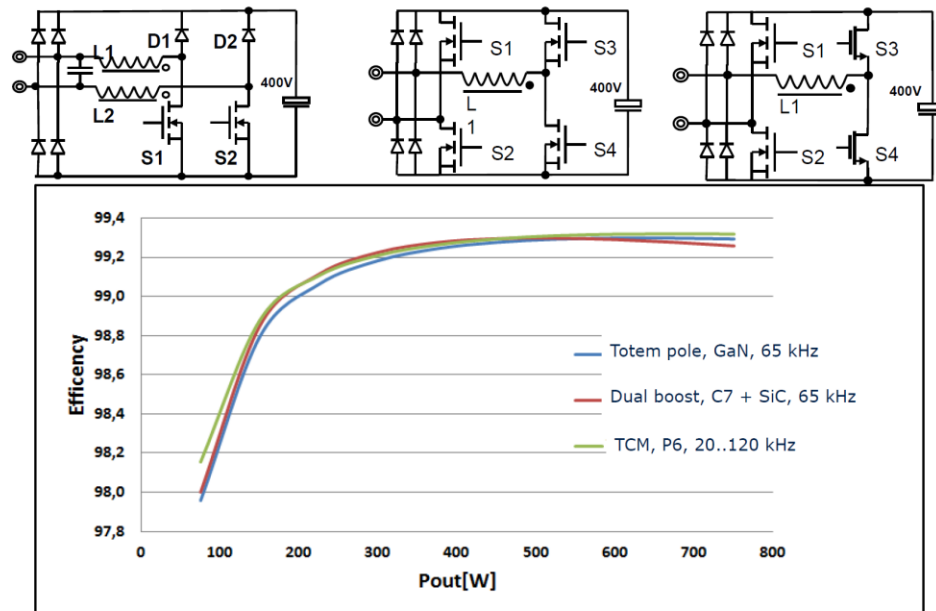




## ► New Converter Topologies

### — Another Indication for a “Natural” Performance Limit

Comparison of various PFC options: complexity of control vs better semiconductors



Source:

Dr. Gerald Deboy  
Plenary Presentation @  
IECON 2013, Vienna

- Minimum Performance Difference for Best Matching of Topology/Semicond./Modulation
- Only Use BASIC Topologies - Costs are THE Deciding Criteria (!)

## ► New Converter Topologies

### ■ Very Large Number of Options !

IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 7, NO. 1, JANUARY 1992

## — Example Topologies for Three-Element Resonant Converters

Rudolf P. Severns

### — 26 out of 48 Topologies are of Potential Interest

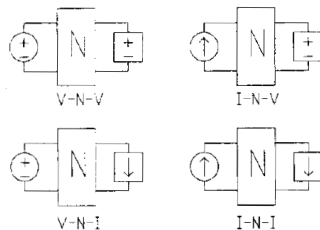


Fig. 13. Source-network-load combinations.

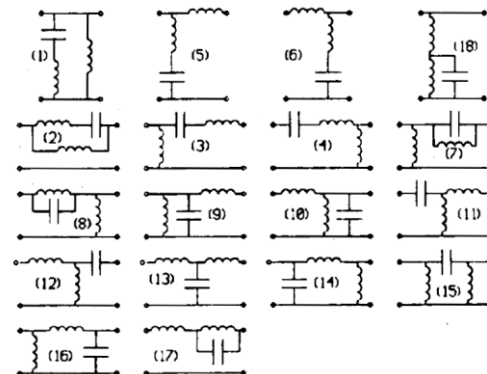


Fig. 17. Networks with 2L and 1C.

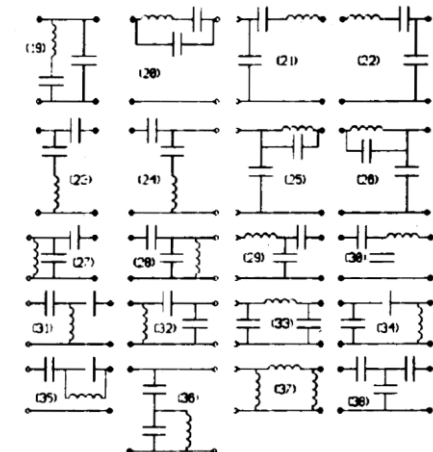


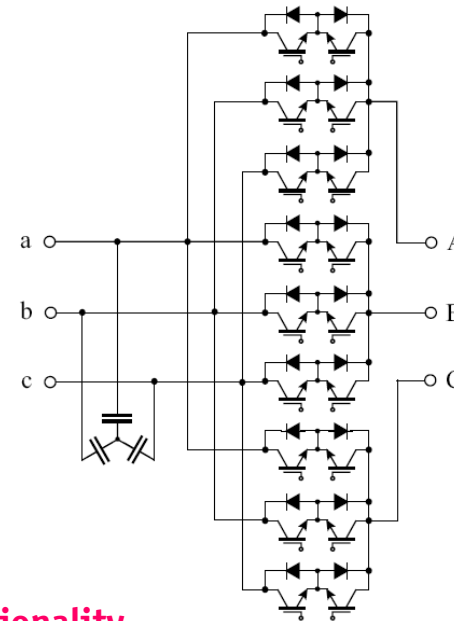
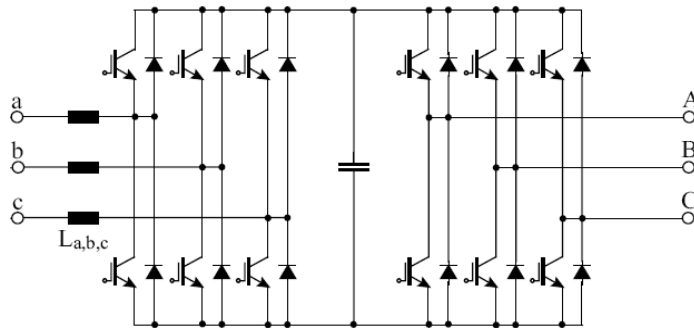
Fig. 18. Networks with 2C + 1L, 3C, and 3L.

### ■ Tools for Comprehensive Comparative Evaluation Urgently needed !



## ► Integration of Functions

- Examples:
  - \* Single-Stage Approaches / Matrix Converters
  - \* Multi-Functional Utilization (Machine as Inductor of DC/DC Conv.)
  - \* etc.

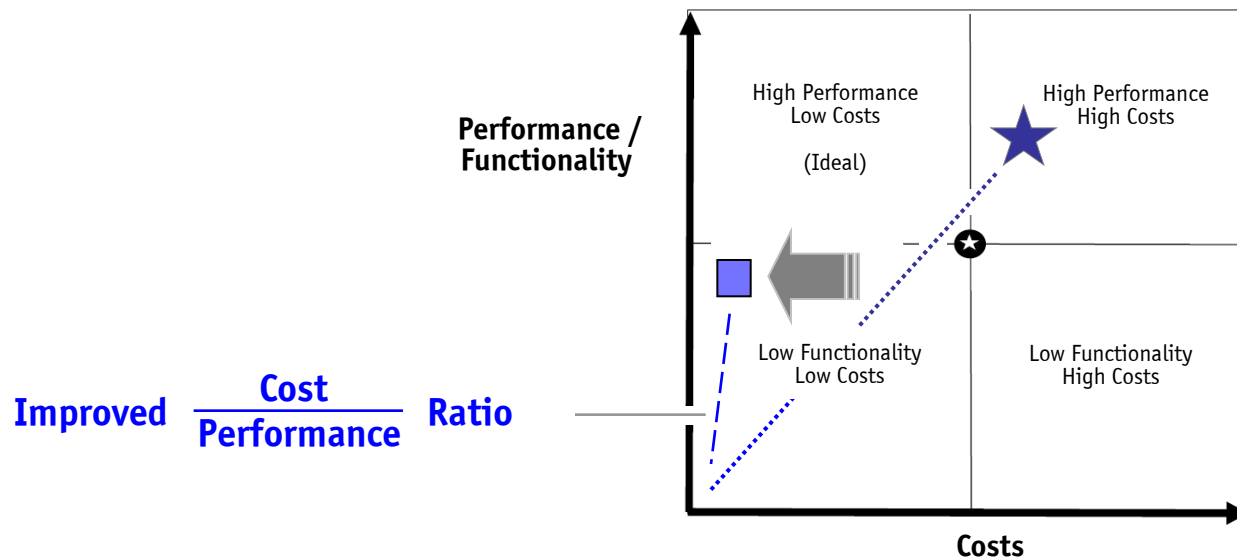


- Integration Restricts Controllability / Overall Functionality
- Frequently Lower Performance of Integrated Solution
- Basic Physical Properties remain Unchanged (e.g. Filtering Effort)



## ► Extreme Restriction of Functionality

- Highly Optimized Specific Functionality → High Performance for Specific Task
- Restriction of Functionality → Lower Costs



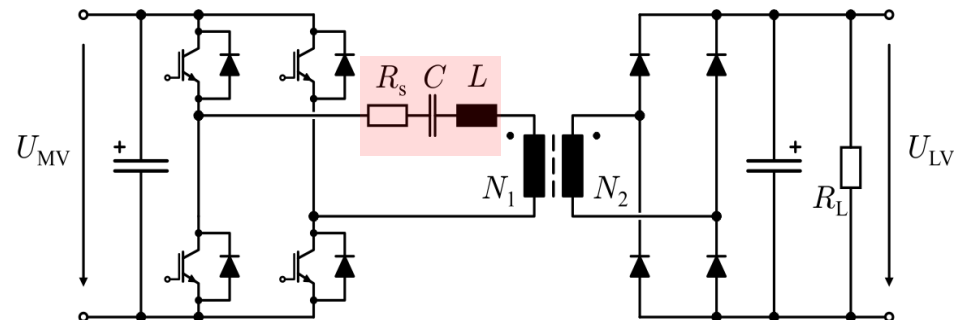
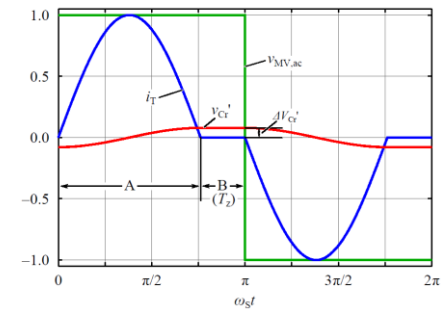
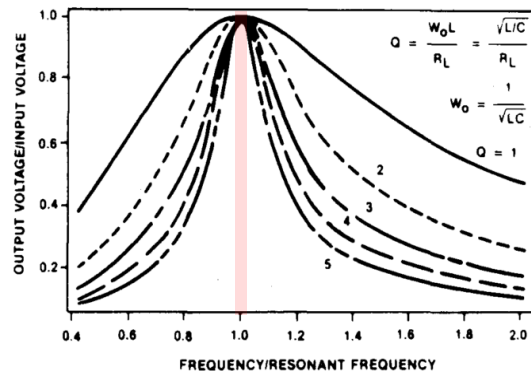
- Cost / Performance Ratio is a Key Metric for Industry Success (Sales Argument)



## ► Extreme Restriction of Functionality

- Example: **DC-Transformer** → Isolation @ Constant (Load Ind.) Voltage Transfer Ratio

Adopted e.g. by **VICOR** –  
“Sine Amplitude Converter” –  
for Factorized Power  
Architecture



- Resonant Frequ.  $\approx$  Switching Frequ. → Input/Output Voltage Ratio =  $N_1/N_2$  (Steigerwald, 1988)



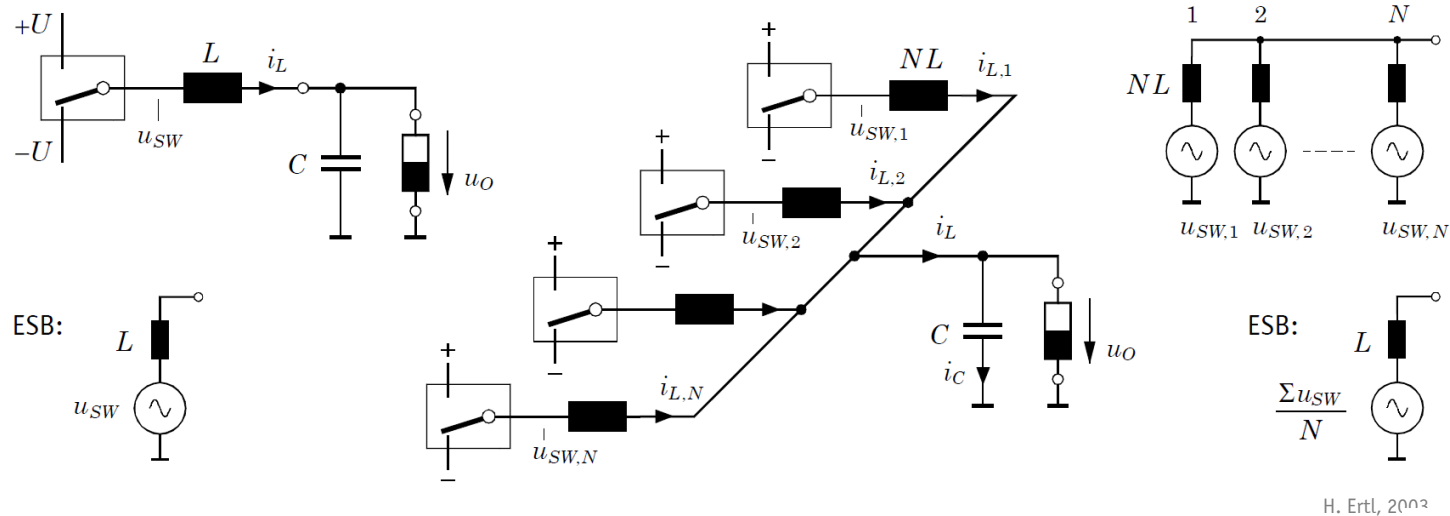
## Multi-Cell Converters

- Parallel Interleaving
- Series Interleaving

## ► Multi-Cell Converters (Homogeneous Power)

### ■ Example of Parallel Interleaving

- Breaks the Frequency Barrier
- Breaks the Impedance Barrier
- Breaks Cost Barrier - Standardization
- High Part Load Efficiency



- **Fully Benefits from Digital IC Technology** (Improving in Future)
- **Redundancy** → Allows Large Number of Units without Impairing Reliability





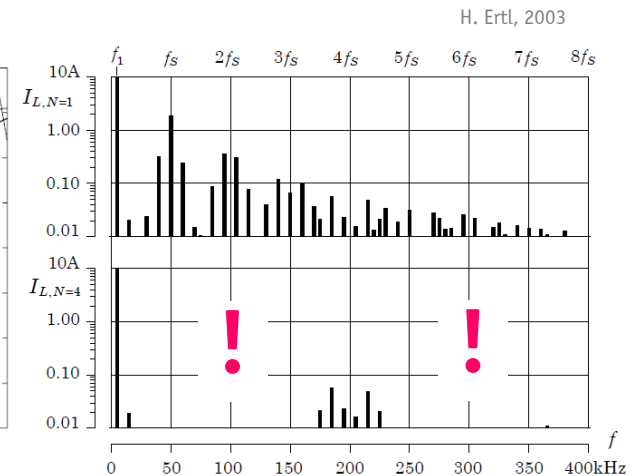
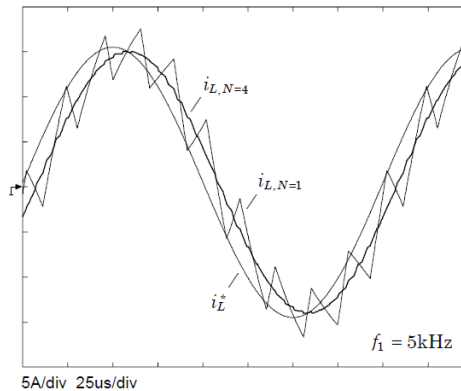
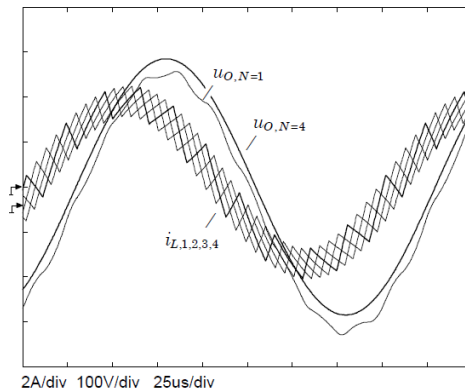
## ► Multi-Cell Converters

### ■ Basic Concept @ Example of Parallel Interleaving

— Multiplies Frequ. / Red. Ripple @ Same Switching Losses & Increases Control Dynamics

$$\Delta U_{\max,N} = \Delta U_{\max} \cdot \frac{1}{N^3}$$

$$\Delta I_{\max,N} = \frac{\Delta I_{\max}}{N^2}$$

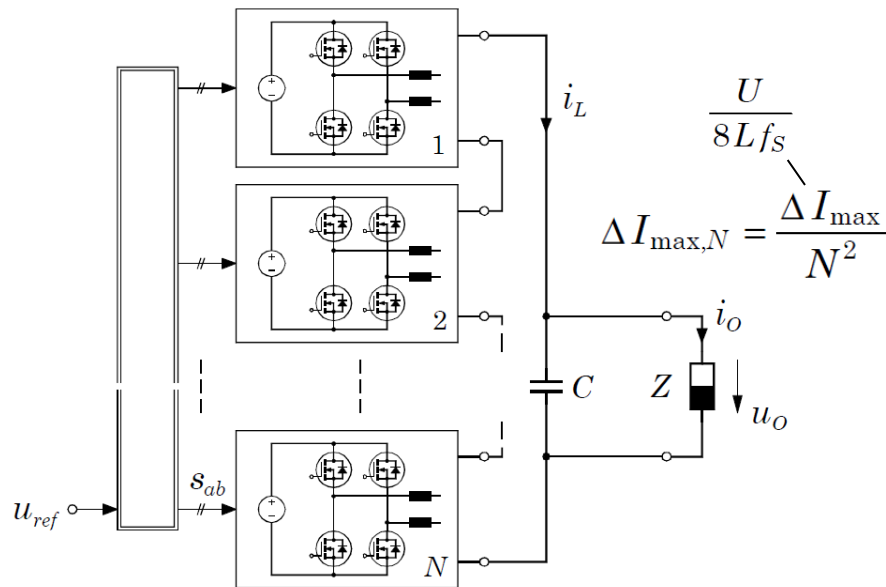


- Fully Benefits from Digital IC Technology (Improving in Future)
- Redundancy → Allows Large Number of Units without Impairing Reliability

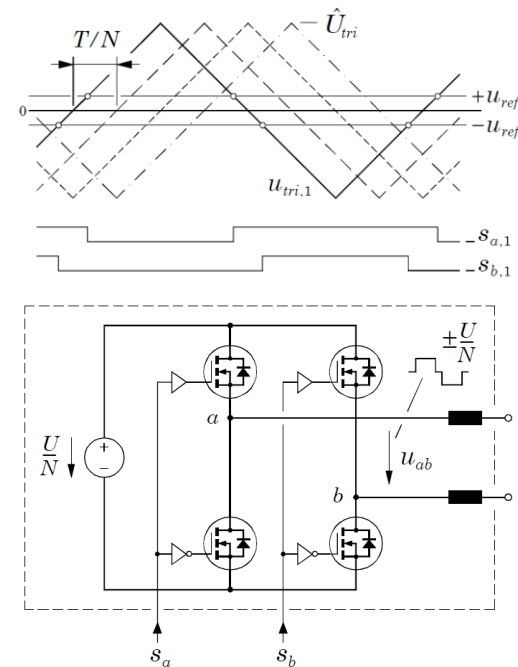
## ► Multi-Cell Converters

### ■ Example of Series Interleaving

$$\frac{\Delta U_{\max,N}}{U} = \frac{\pi^2}{32} \left[ \frac{f_0}{f_s} \right]^2 \cdot \frac{1}{N^3}$$



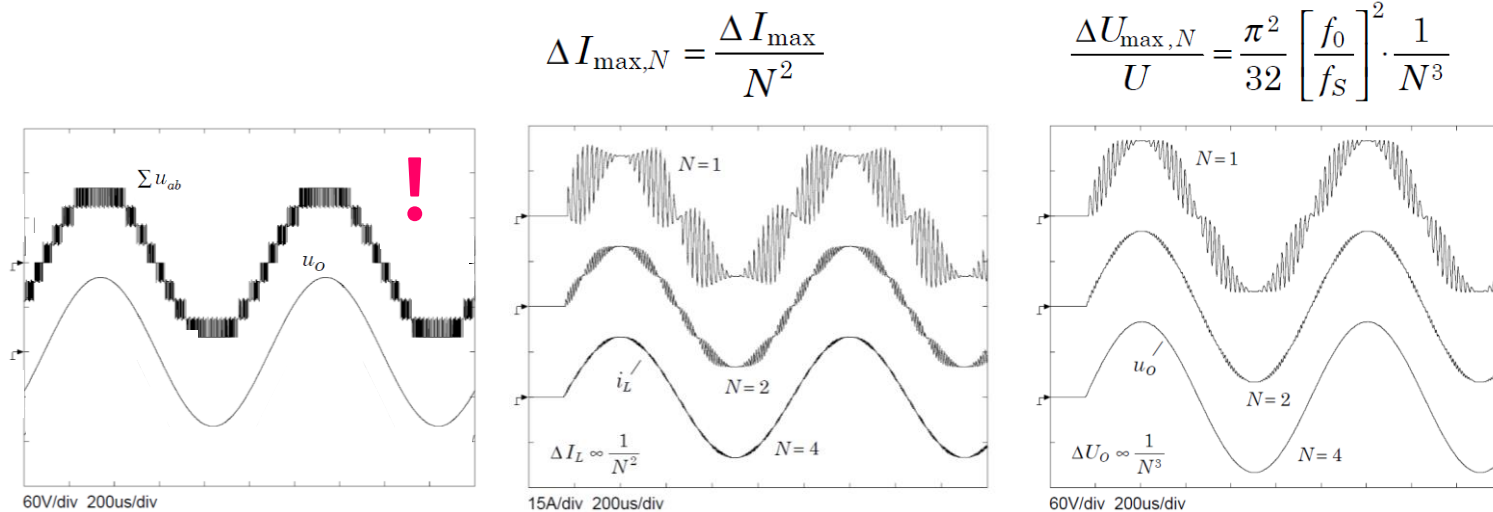
- Breaks the Frequency Barrier
- Breaks the Silicon Limit 1+1=2 NOT 4 (!)
- Breaks Cost Barrier - Standardization
- Extends LV Technology to HV



## ► Multi-Cell Converters

### ■ Example of Series Interleaving

— Multiplies Frequ. / Red. Ripple @ Same Switching Losses & Increases Control Dynamics



H. Ertl, 2003

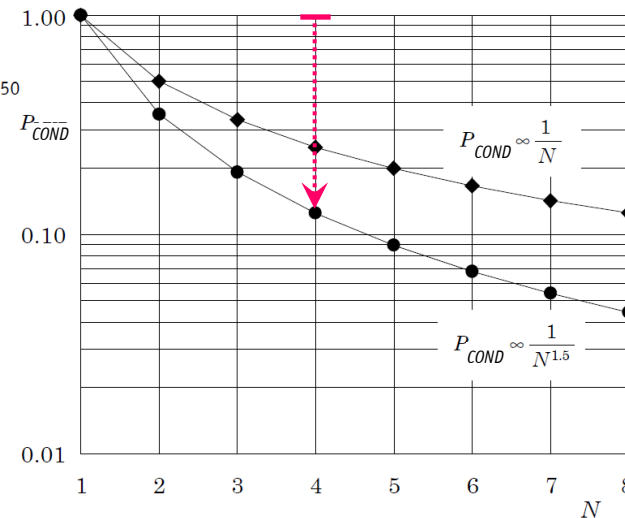
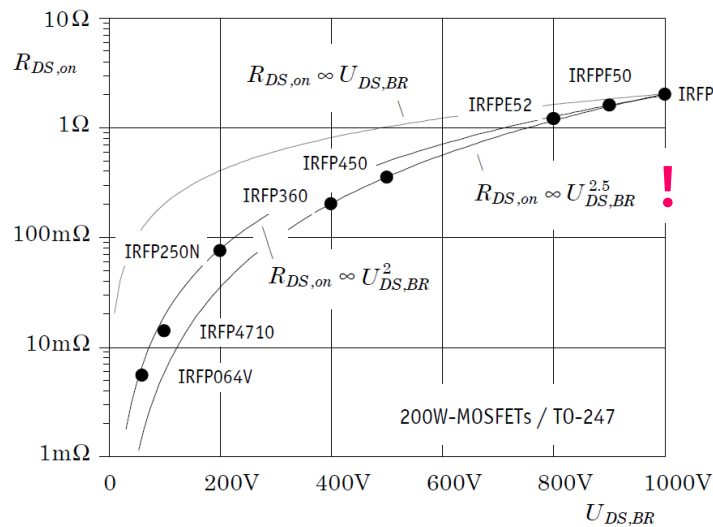
- Especially Advantageous for Ohmic On-State Behavior of Power Switches (!)
- Redundancy → Allows Large Number of Units without Impairing Reliability



## ► Multi-Cell Converters

### ■ Example of Series Interleaving

— Scaling of  $R_{DS,on}$  of MOSFETs with Blocking Voltage → Loss Red. by Factor of 8 for  $N=4$



H. Ertl, 2003

- Especially Advantageous for Ohmic On-State Behavior of Power Switches (!)
- Redundancy → Allows Large Number of Units without Impairing Reliability

## ► Multi-Cell Converters

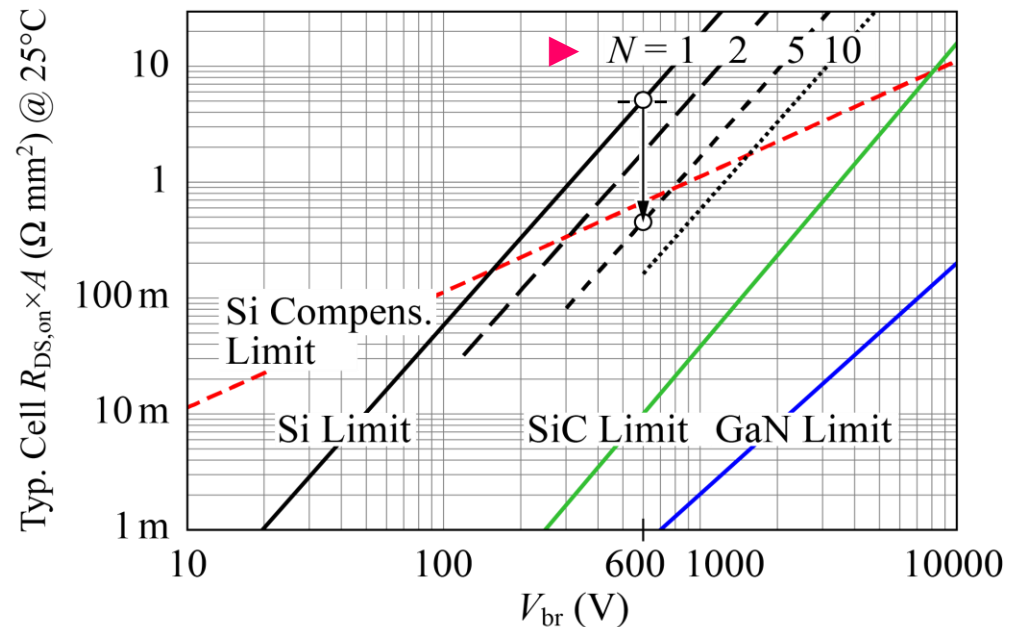
### ■ Series Connection of LV MOSFETs (LV Cells) Effectively *SHIFTS the Si-Limit* (!)

Assumption:

Chip Area of each LV  
Chip Equal to the Chip  
Area of the HV Chip

#### – Scaling of Specific On-State Resistance

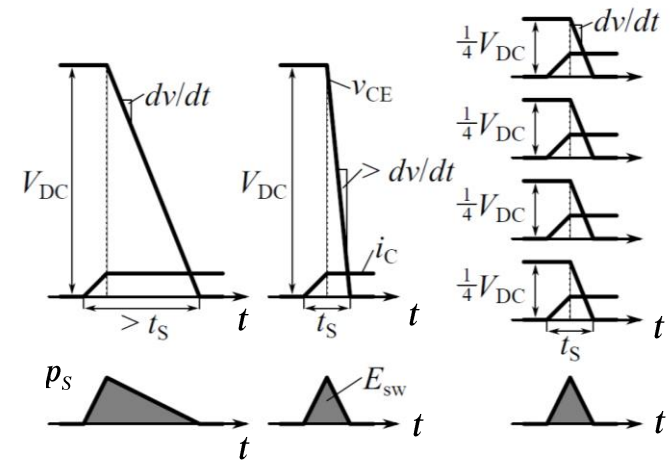
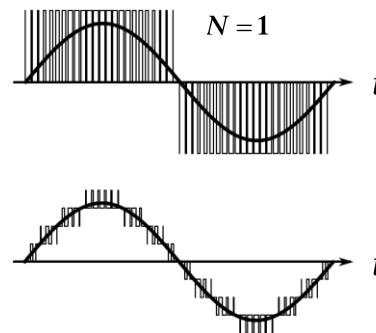
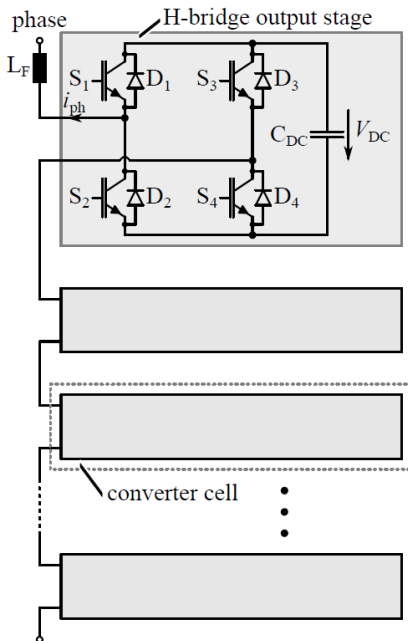
$$(R_{DS,on} \times A)_{eff} \approx \frac{1}{N^{1.5}} (R_{DS,on} \times A)$$



### ■ Excellent Opportunity for Extreme Efficiency Ultra-Compact Converters

## ► Multi-Cell Converters

### ■ Interleaved Series Connection Dramatically Reduces Switching Losses (or Harmonics)



– Scaling of Switching  
Losses for Equal  $\Delta i/I$   
and  $dv/dt$

$$P_{S,N} \approx P_{S,N=1} \cdot \left( \frac{1}{2N^2} \dots \frac{1}{N^3} \right)$$

- Converter Cells Could Operate at VERY Low Switching Frequency (e.g. 5kHz)
- Minimization of Passives (Filter Components)

## ► Multi-Cell Converters – Summary

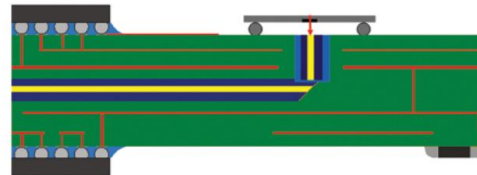
### ■ Advantages

- Switching Frequency Multiplication @ No Loss Increase
- Ripple Reduction @ Input and Output
- Distribution of Losses (Parallel Connect. of Therm. Resistances)
- Larger Surface / Volume Ratio of Indiv. Unit (Easier Cooling)
- Redundancy Possible (High Reliability)
- Deactivation of Units at Part Load (High Part Load Efficiency)
- Solves the Impedance Matching Problem @ High I or U
- Multiplies U, I Capabilities of Single Devices (Very High U, I possible)
- Reduction of Eff. RDS(on) (Shifting Si-Limit for Series Connection)
- Eff. Increase of Switching Speed @ Given  $du/dt$ ,  $di/dt$
- Supports Standardization (Potential Cost Reduction)
- Minimizes Time-to-Market (Allows Platform Solutions)
- Supports PCB Realization even for High Current (Current Partitioning)

### ■ Challenges

- Handling of Control Complexity (Digital Control)
- Overall Complexity Increasing Costs (Economy of Scale?)
- Symmetrization of the Loading of the Individual Units

### ■ Idea for Supporting Technology



PCBs with  
Embedded Optical  
Fibers / Link

... a Highly Powerful Concept with Large Potential (!)

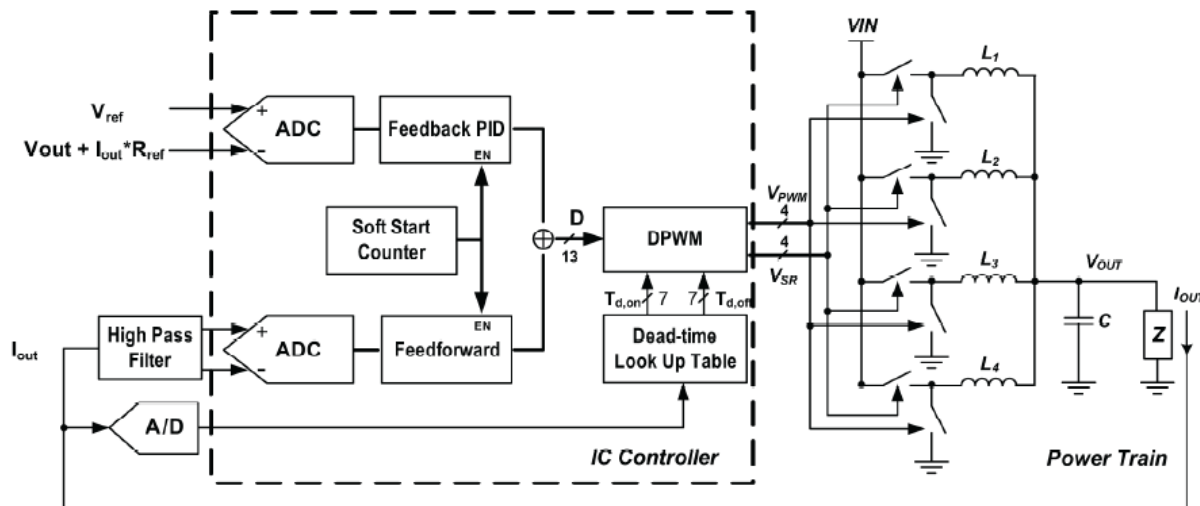
## Examples of Multi-Cell Converters

- VRM
- Ultra-Efficient 1ph. PFC
- Telecom Power Supplies



## ► Voltage Regulator Module

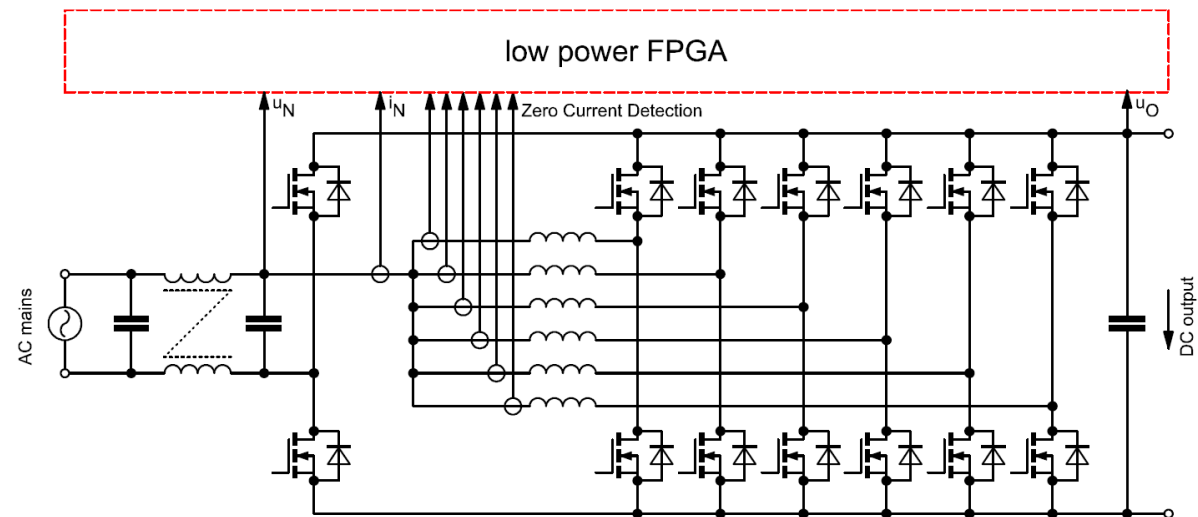
### ■ Multi-Channel / Parallel Interleaving of up to 12 Channels



- **Coupling Inductors (Interphase Inductors) allows Further Reduction of Ind. Comp. Volume**
- **For On-Chip Integration Challenged by Switched Capacitor Converters**

## ► Bidirectional Ultra-Efficient 1- $\Phi$ PFC Mains Interface

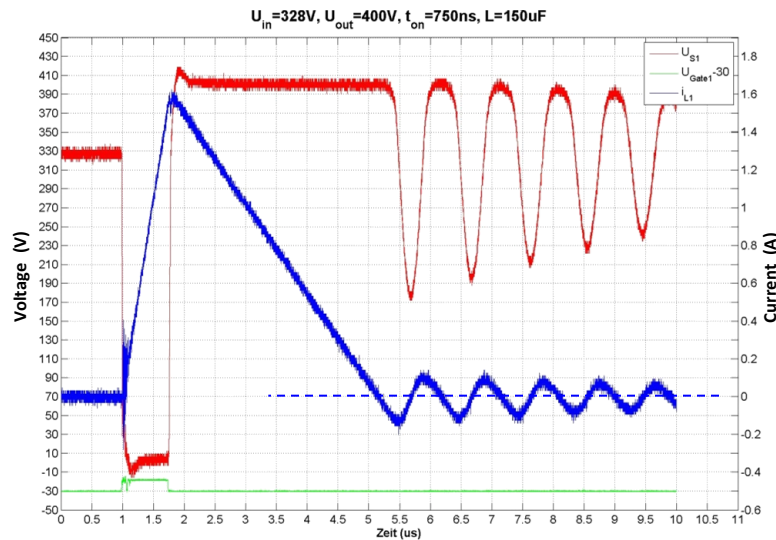
★ 99.36% @ 1.2kW/dm<sup>3</sup>



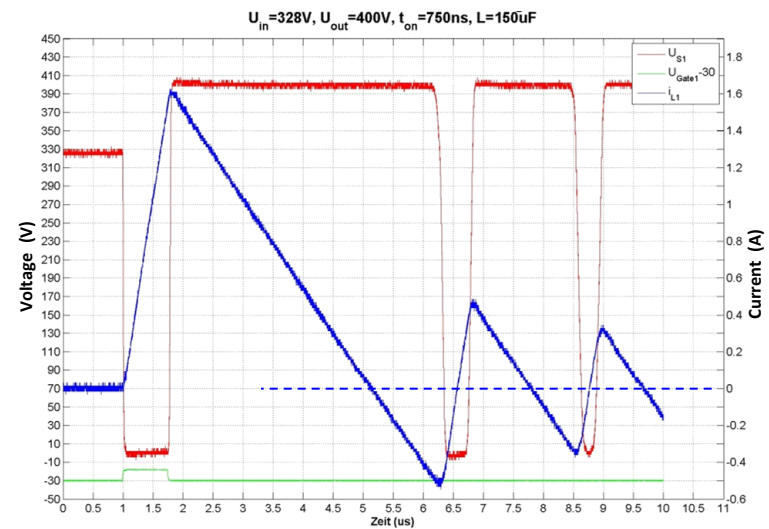
■ Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

## ► Bidirectional Ultra-Efficient 1- $\Phi$ PFC Mains Interface

### ■ AC-DC Rectifier - Single Boost Cell - Measurements



— Hard Turn-On (Partial ZVS)

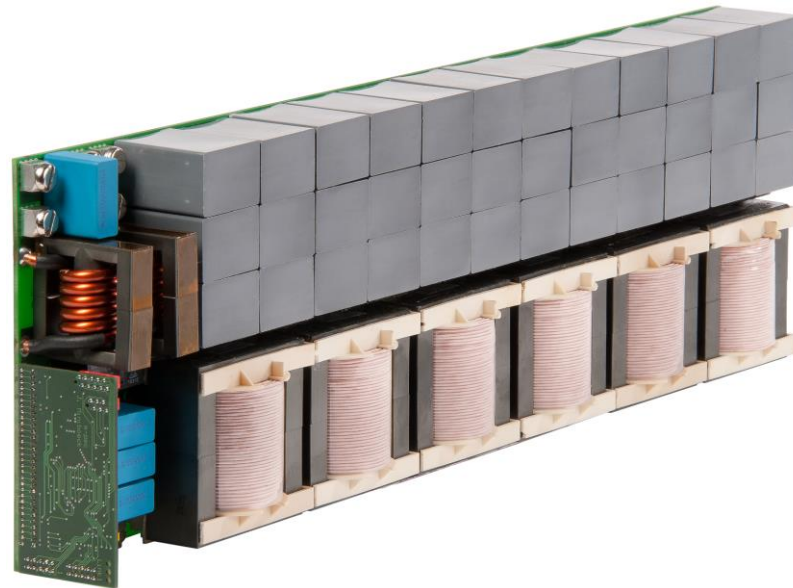


— ZVS Turn-On by Ext. On-Interval of  $S_{11}$  (TCM)

## ► Bidirectional Ultra-Efficient 1- $\Phi$ PFC Mains Interface

★ 99.36% @ 1.2kW/dm<sup>3</sup>

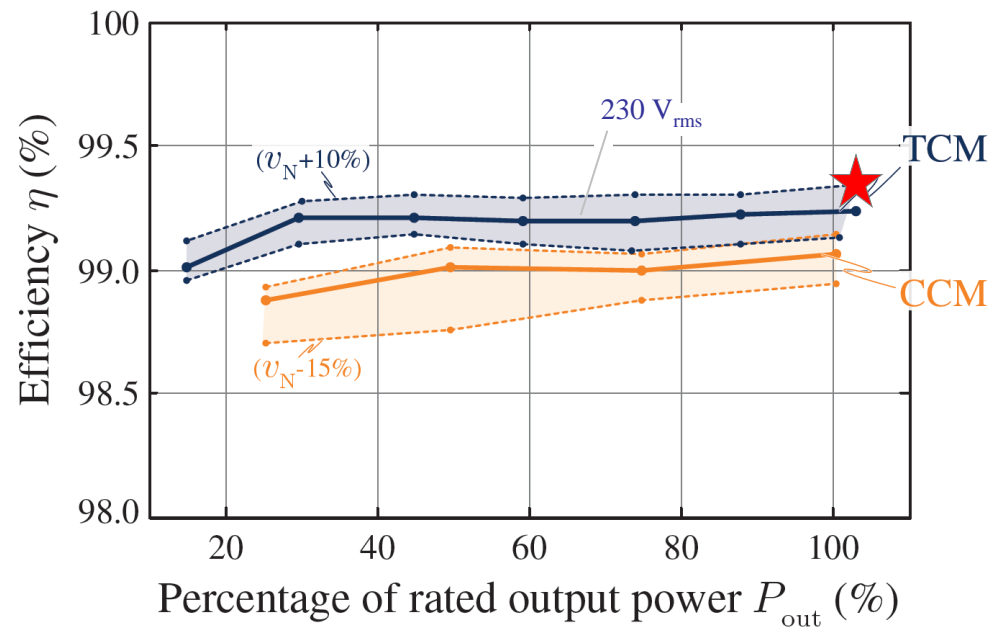
*Hardware Testing  
to be finalized in  
September 2011*



■ Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

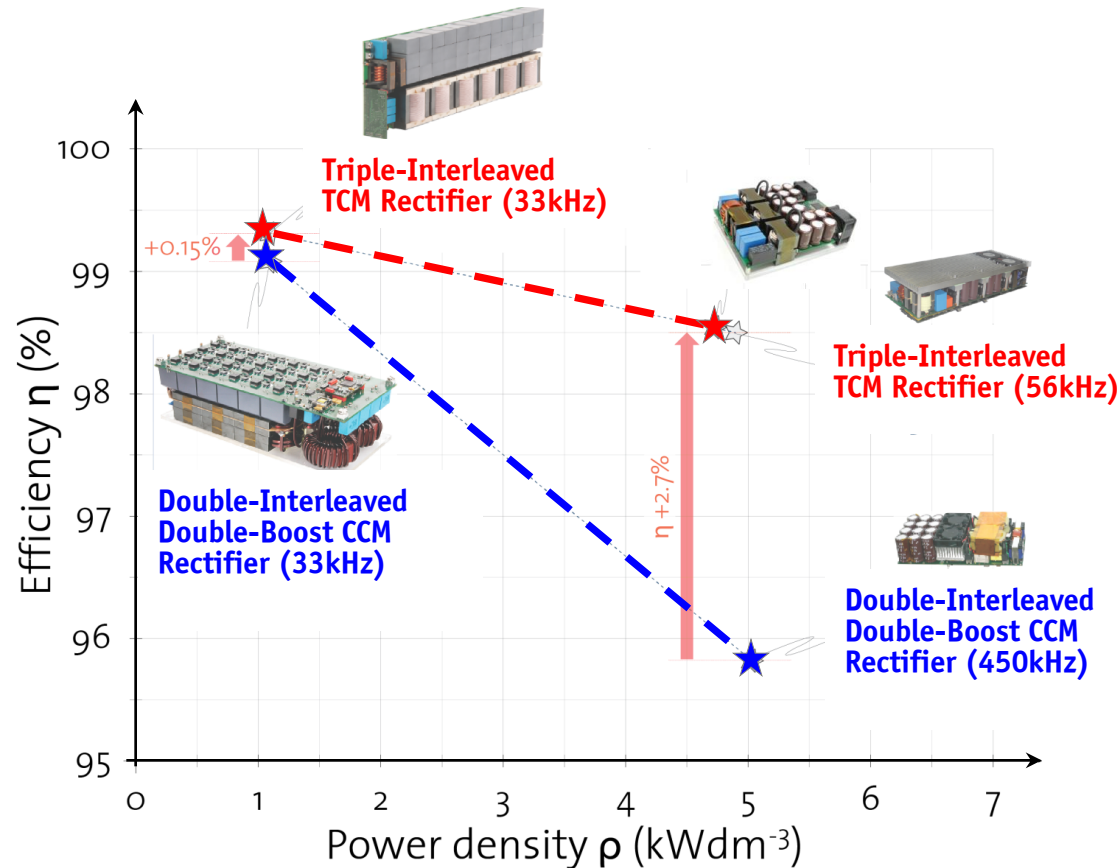
## ► Bidirectional Ultra-Efficient 1- $\Phi$ PFC Mains Interface

★ 99.36% @ 1.2kW/dm<sup>3</sup>



► Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

## ► Converter Performance Evaluation Based on $\eta$ - $\rho$ -Pareto Front



## ► KEYS for Achieving the Performance Improvement

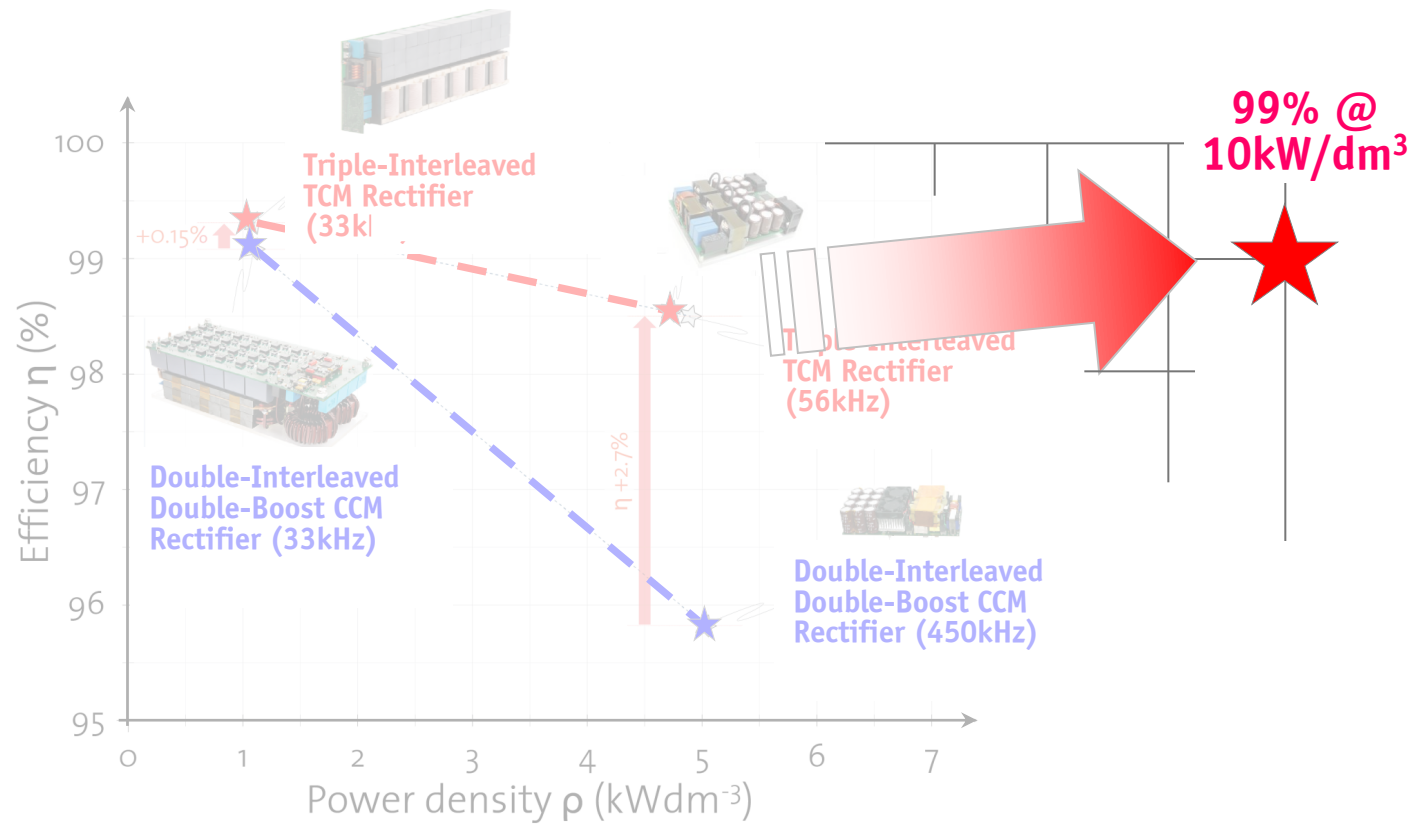
... despite Using “Old”  
Si Technology

- Basic Topology
- ZVS Only Achieved by Modified Operation Mode
- Active ZVS
- Triangular Current Mode (TCM)
- Variable Switching Frequency
- No Diode On-State Voltage Drop
- Continuously Guided  $u$ ,  $i$  Waveforms
- Interleaving
- Utilization of Low Superjunct.  $R_{DS(on)}$
- Utilization of Digital Signal Processing
- Low Complexity
- No Aux. Circuits
- No (Low) Switching Losses
- No Direct Limit of # of Parallel Trans.
- Simple Symm. of Loading of Modules
- Spread & Lower Ampl. EMI Noise
- Synchr. Rectification
- No Free Ringing → Low EMI Filter Vol.
- Low EMI Filter Vol. & Cap. Curr. Stress
- Low Cond. Losses despite TCM
- Low Control Effort despite 6x Interl.



... the Basic Concept is Known since 1989 (!)

## ► Is Another Step of Massive Improvement Possible ?

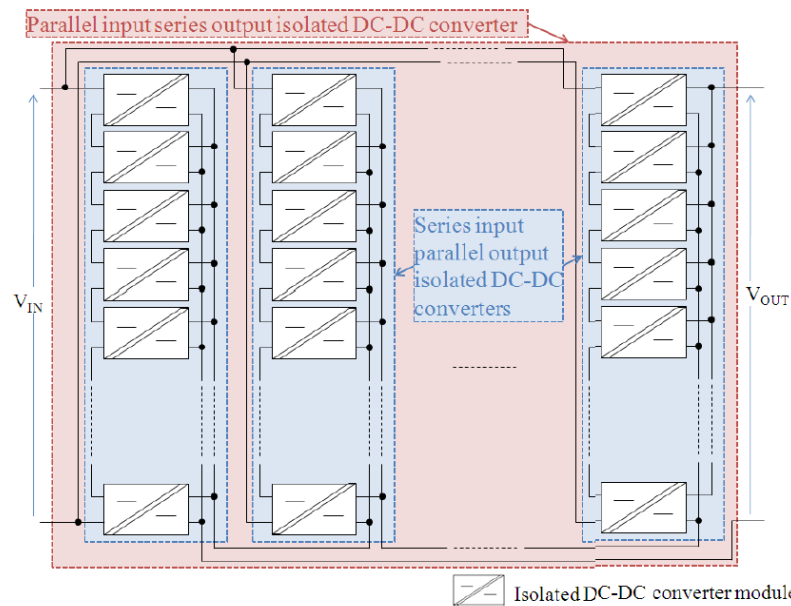




## ► Solution: **ISOP** Multi-Cell Approach (!)

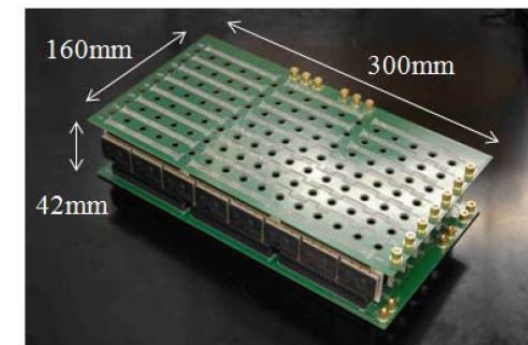
- Isolated 380V/48V Telecom DC-DC Converter
- 8 x 300W 48V/48V VICOR Modules
- 96.5% Efficiency @ 16kW/l Power Density (!)

Hayashi, NTT; 2012



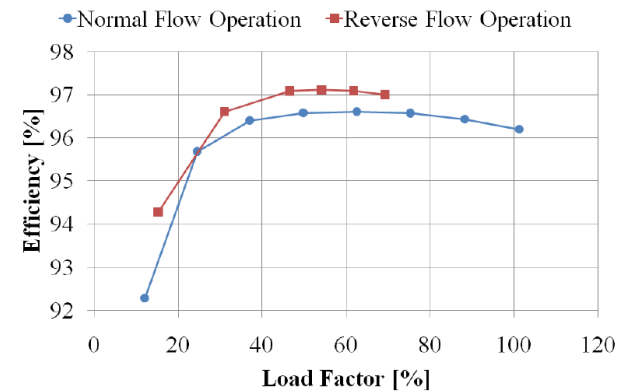
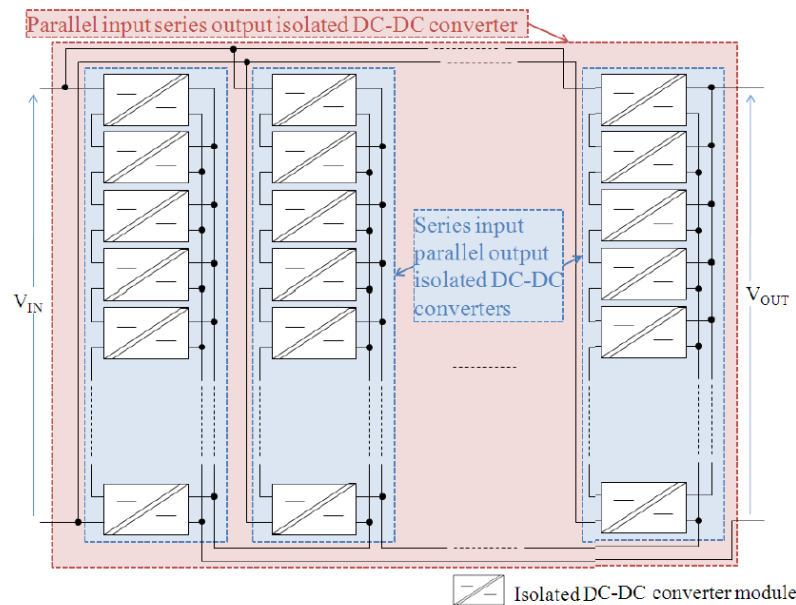
8x8 Modules  
380V/380V

Parameter	Value
Total Output Power	2400W
Rated Input Voltage	384V
Rated Output Voltage	48V
Manufacturer	VICOR
Part Number	V048F480T006
Rated Power	336W
Size (W, D, Ht)	22mm, 32.5mm, 6.73mm
Input Voltage	26V – 55V
Output Voltage	26V – 55V
Efficiency	96.4% (at Full Load)

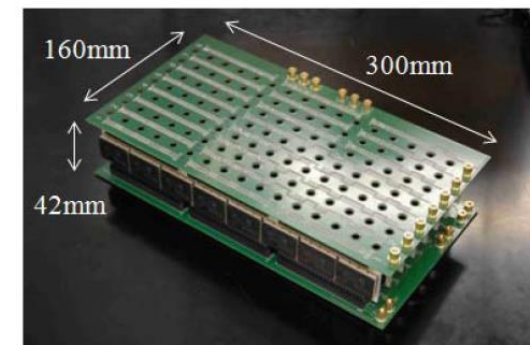


## ► Solution: **ISOP** Multi-Cell Approach (!)

- Isolated 380V/48V Telecom DC-DC Converter
- 8 x 300W 48V/48V VICOR Modules
- 96.5% Efficiency @ 16kW/l Power Density (!)



8 Modules  
380V/380V



## “Killer”- Semiconductor Technologies



**WBG Power Semiconductors**

... Not a Merit of Power Electronics but  
of Power Semiconductor Research

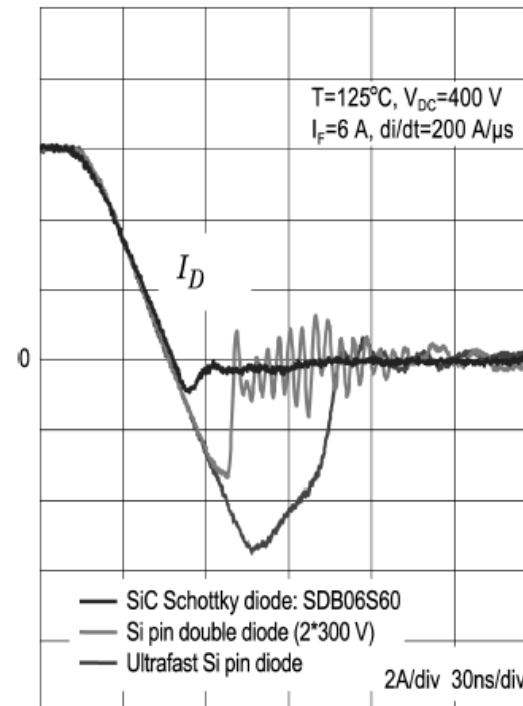


## ► WBG Power Semiconductors

### — Example: SiC Schottky Diode – Zero Recovery Rectifiers

#### ■ General Capabilities

- Higher Switching Frequency
- Higher Operating Temperature
- Higher Blocking Capability



# But ...

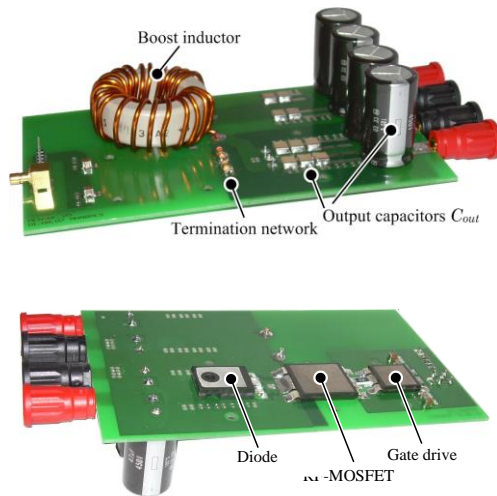
## Today the Capabilities of SiC Cannot be Utilized

- Fast Switching Capability
- High Temp. Capability
- High Blocking Capability



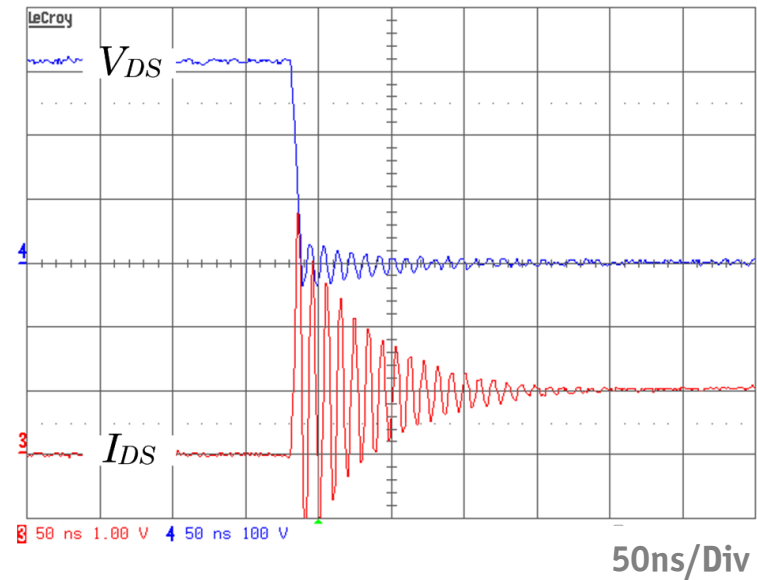
- ▶ Limit by Package (Layout) Parasitics
- ▶ Missing High Temp. Package (Therm. Cycles)
- ▶ Missing High Temp. Passives
- ▶ Multi-Level Topologies !
- ▶ Missing MV / Low Inductance Package

## ► Higher Switching Speed



100V/Div

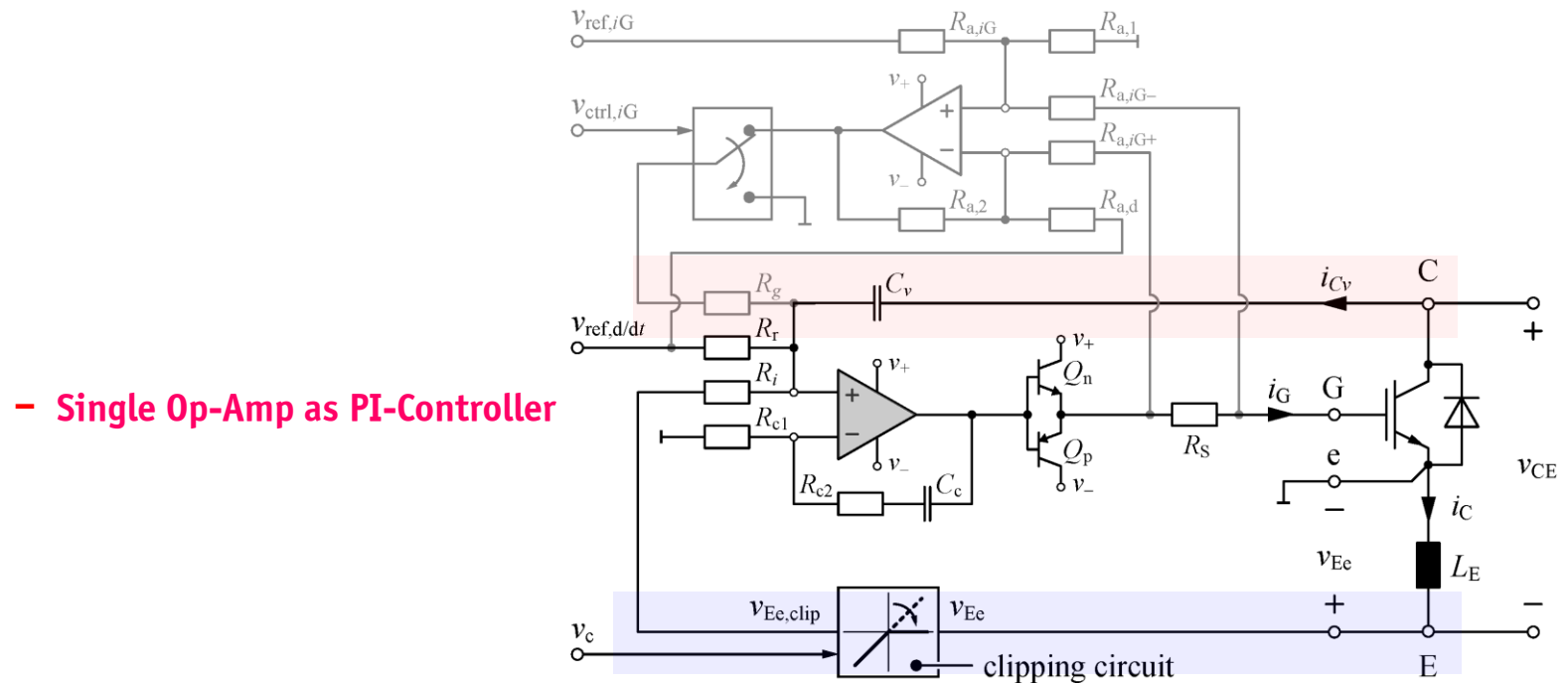
10A/Div



► Missing HF Package

► Missing Integrated Gate Drive (Active Control of Switching Trajectory)

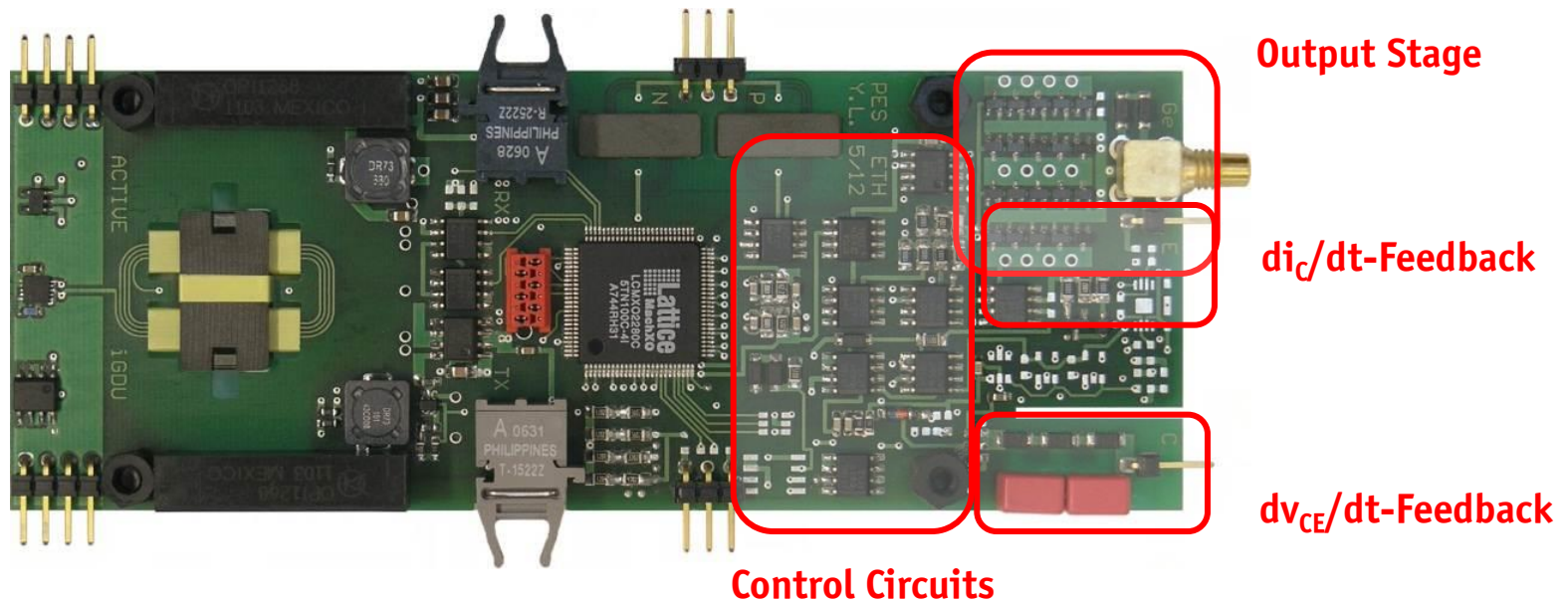
## ► Active Closed Loop Gate Drive



- Continuous (!) Control of the Switching Trajectory incl. Short Circuit
- Options for Monitoring / Reliability Prediction etc.

## ► Hardware Prototype

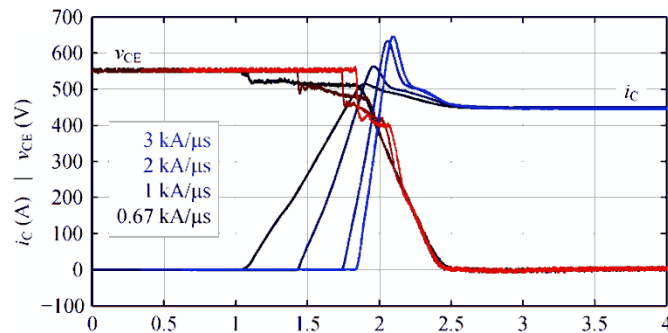
■ **PCB Dimensions** 50 mm x 130 mm (2 in x 5.1 in)



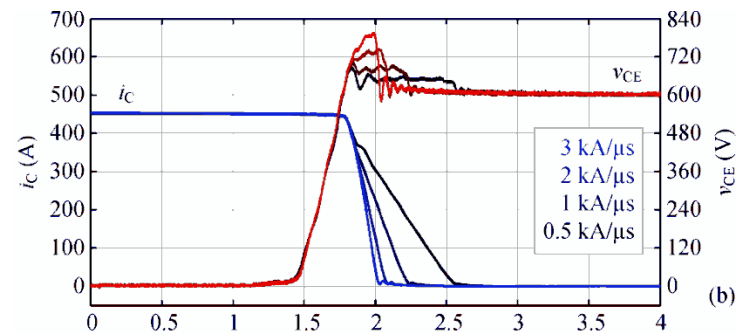


## ► Experimental Results – Individual Variation of References

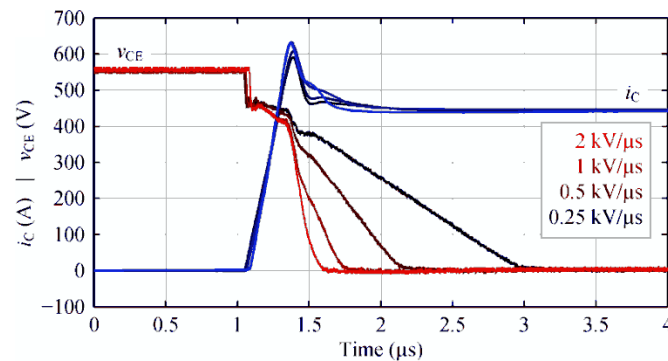
### ■ Turn-On: Variation of $di_c/dt$



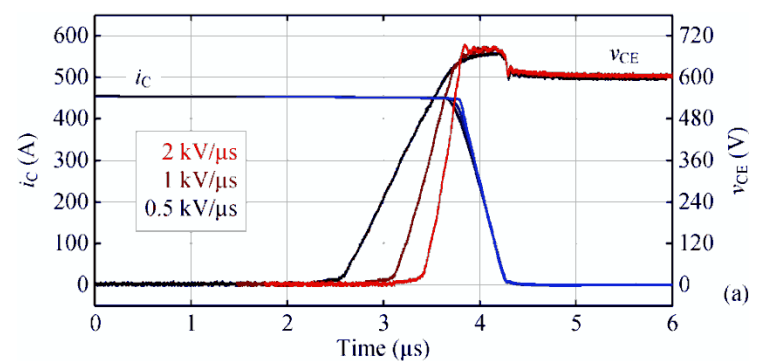
### ■ Turn-Off: Variation of $di_c/dt$



### ■ Turn-On: Variation of $dv_{CE}/dt$



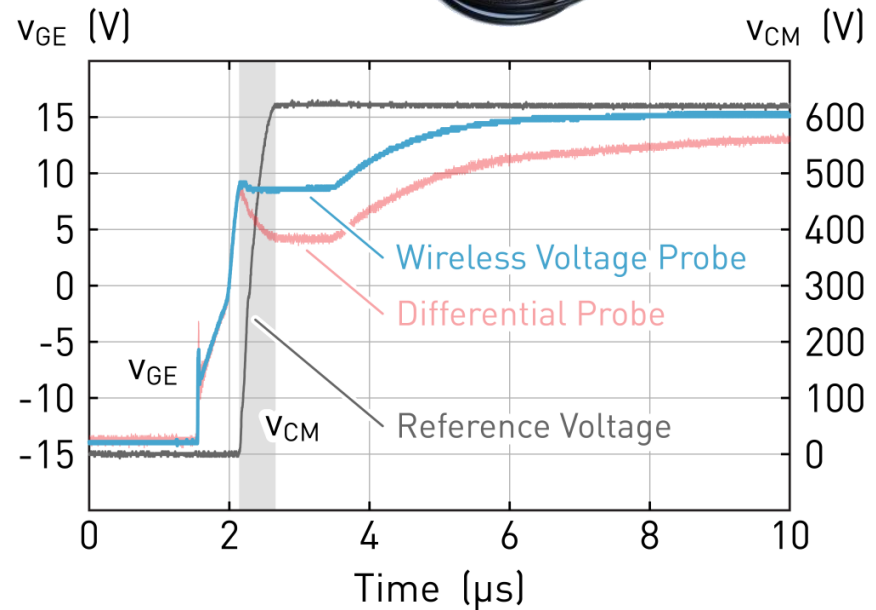
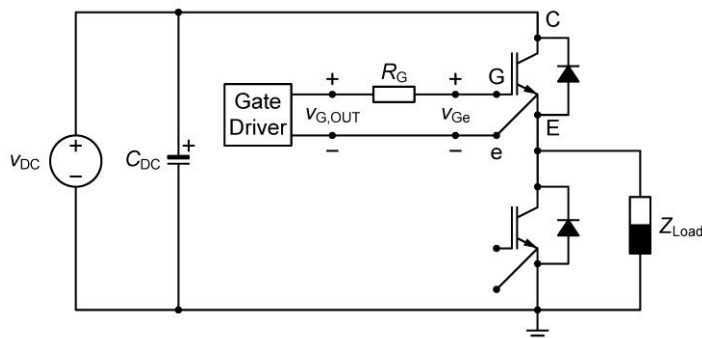
### ■ Turn-Off: Variation of $dv_{CE}/dt$



## ► New Wireless Measurement Technology

- Bandwidth 100 MHz
- Sampling Rate 400 MS/s (8 Bit)
- Bluetooth Communication
- NO  $dv_{CM}/dt$  Limit (!)

anartrionics



## ► GE Planar Power Polymer Packaging (P4™)



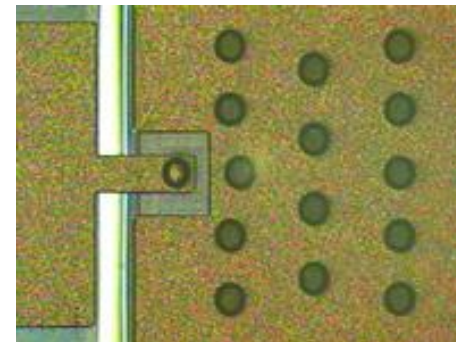
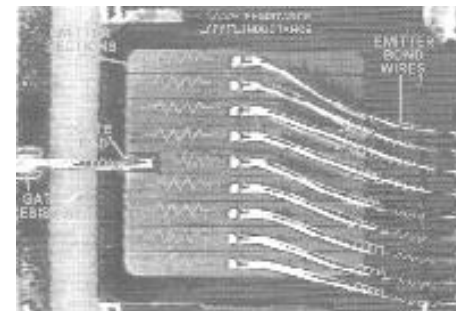
GE Global Research

United States - India - China - Germany

Oriented Toward High Power Devices  
<2400V / 100A...500A  
<200W Device Dissipation

Wire-Bonded Die on Ceramic Substrate  
Replaced with Planar Polymer-Based  
Interconnect Structure

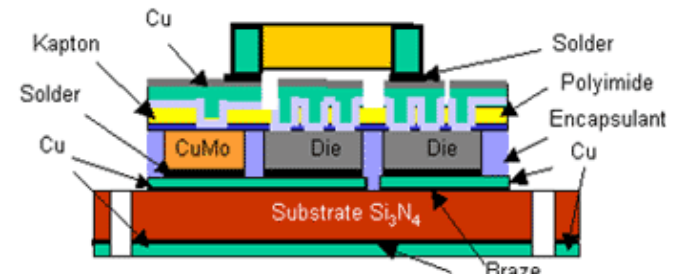
Direct High-Conductivity Cooling Path



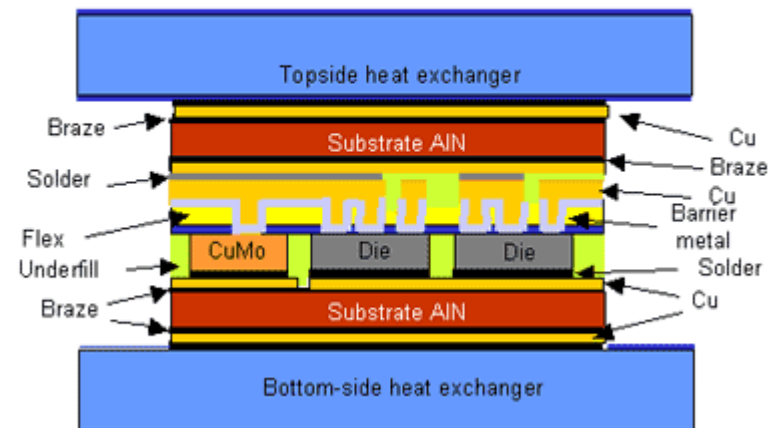
## ► GE Planar Power Polymer Packaging (P4™)

- Reduces Wire Bond Resistance by Factor 100
- Significantly Lower Switching Overvoltages
- Reduced Switching Losses
- No Ringing
- Reduces EMI Radiation
- Enables Topside Cooling
- No Mechanical Stress of Wire Bond Process
- Reduces CTE Wire Bond Stress on Chip Pads

CROSS SECTION OF A POWER OVERLAY MODULE

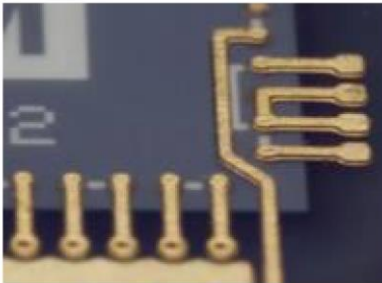


DOUBLE-SIDED COOLING OF A POWER OVERLAY MODULE



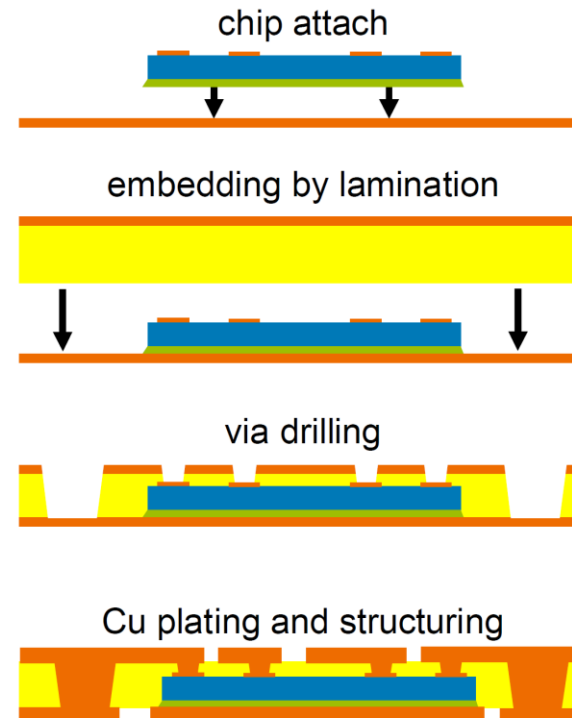
## ► Novel PCB Technologies for High Power Density Systems

### ■ Chip in Polymer Process / Multi-Functional PCB



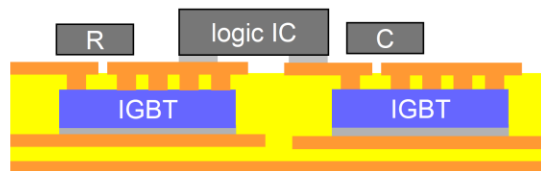
*embedded chip in PCB structure.*

- **Chip Embedding by PCB Technology**
- **Direct Cu Contact to Chip / No Wires or Solder Joints**
- **Thin Planar Packaging enables 3D Stacking**
- **Improved Electrical Performance and Reliability**

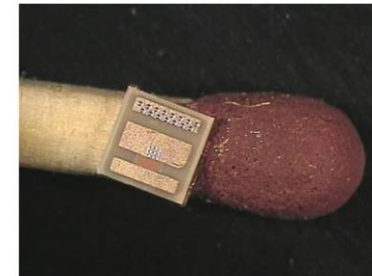


## ► Planar Power Chip Package

### ■ Novel Concepts for Power Packages and Modules



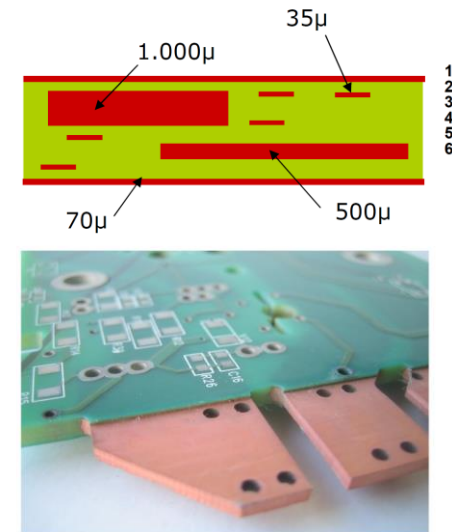
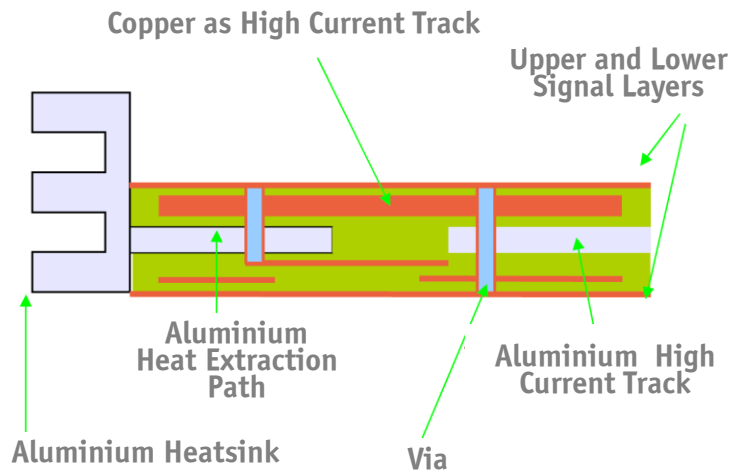
Module with Power and Logic Devices



Single Chip Package for MOSFETs and IGBTs

## ► Multi-Functional PCB

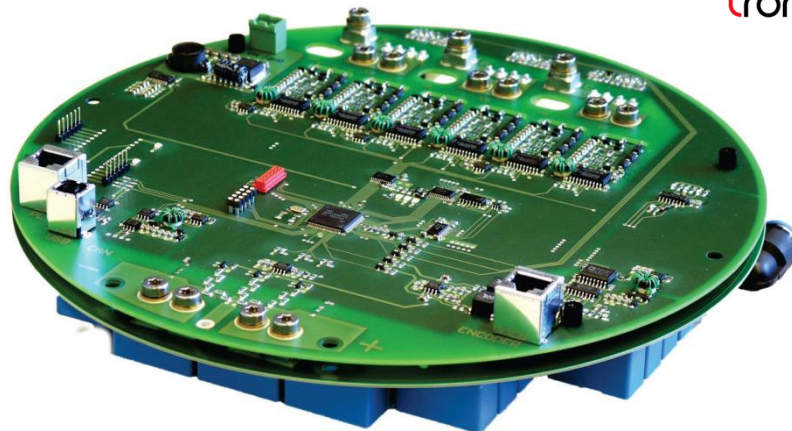
- Multiple Signal and High Current Layers
- Thermal Management



- "Fab-Less" Power Electronics
- Testing is Challenging (Only Voltage Measurement)
- Advanced Simul. Tools of Main Importance (Coupling with Measur.)

## ► 3ph. Inverter in p<sup>2</sup>pack-Technology

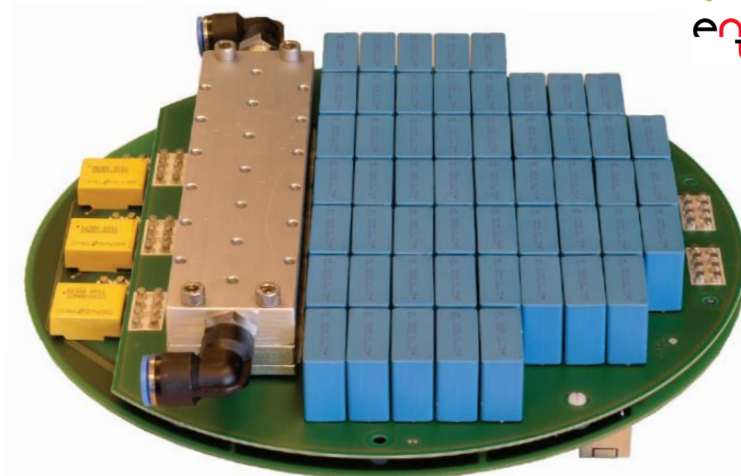
- Rated Power 32kVA
- Input Voltage 700V<sub>DC</sub>
- Output Frequency 0 ... 800Hz
- Switching Frequency 20kHz





## ► 3ph. Inverter in p<sup>2</sup>pack-Technology

- Rated Power 32kVA
- Input Voltage 700V<sub>DC</sub>
- Output Frequency 0 ... 800Hz
- Switching Frequency 20kHz



 SCHWEIZER  
ELECTRONIC  
 ener  
tronics

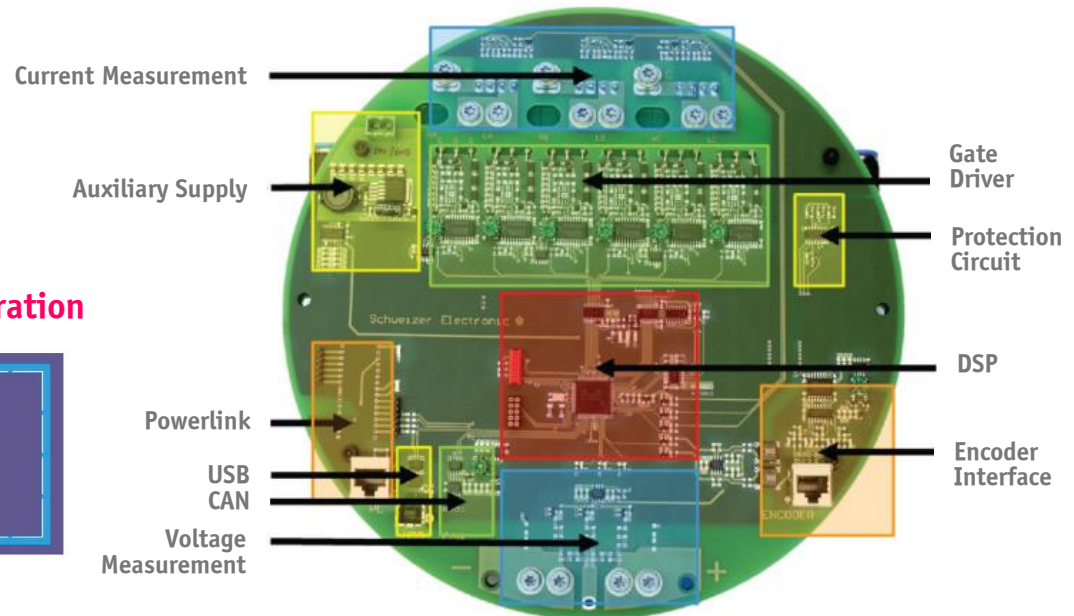
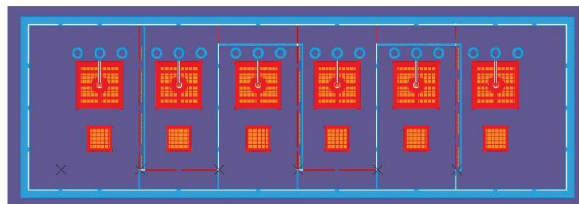


## ► 3ph. Inverter in p<sup>2</sup>pack-Technology

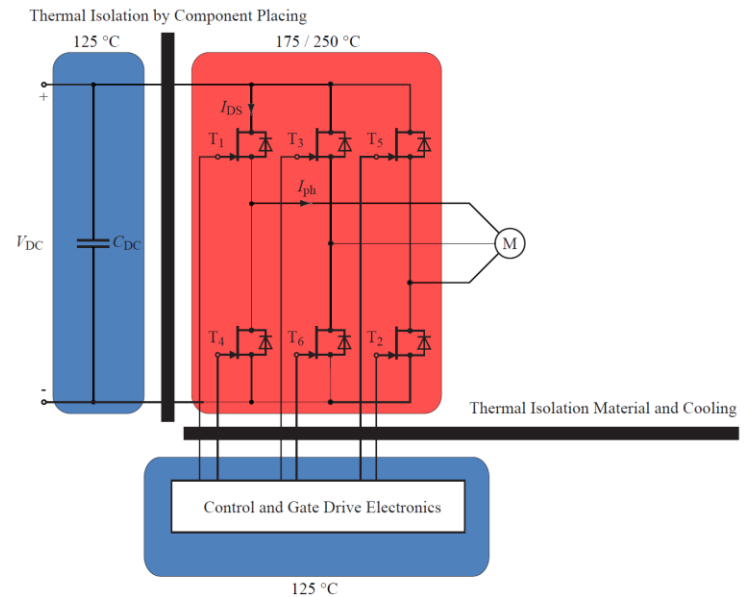
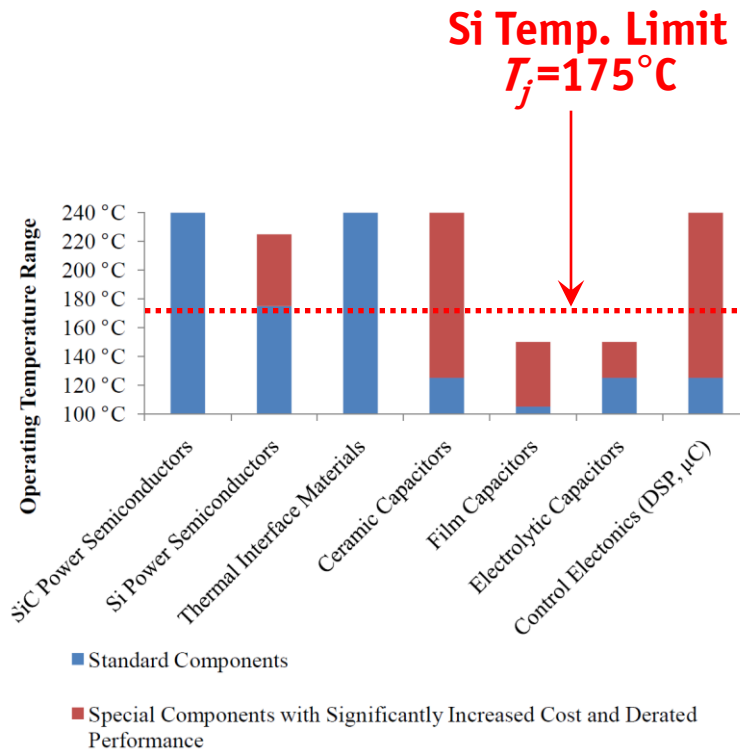
- Rated Power 32kVA
- Input Voltage 700V<sub>DC</sub>
- Output Frequency 0 ... 800Hz
- Switching Frequency 20kHz



### – Power Semiconductor PCB Integration

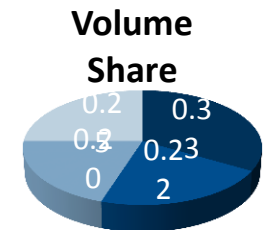
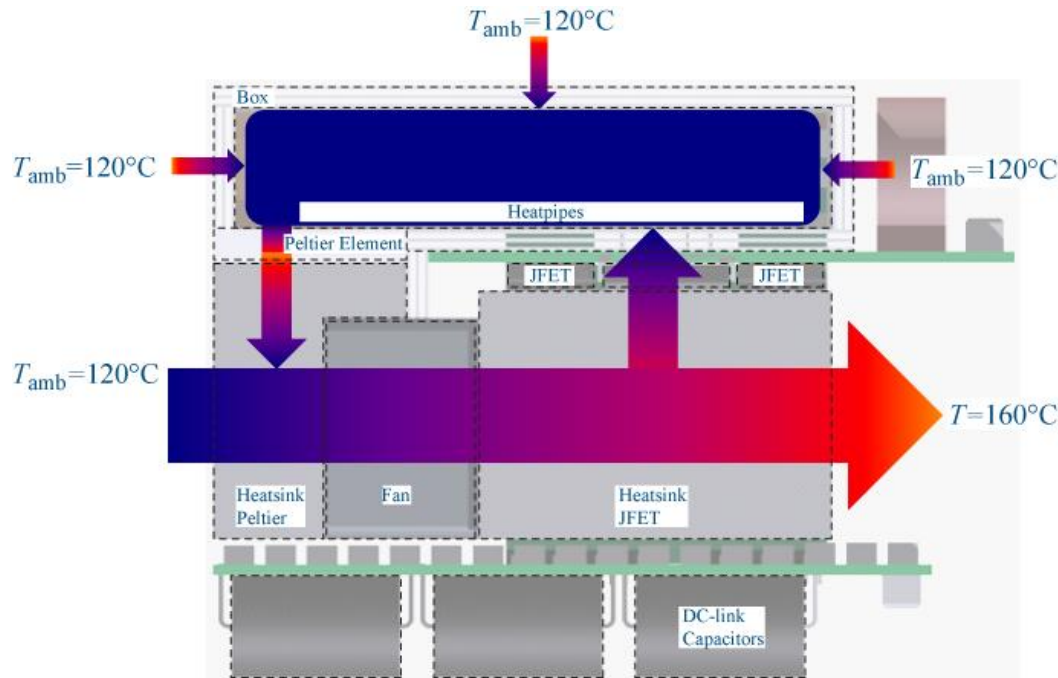


## ► High Temperature (I)



*120°C Ambient Air Cooled  
Automotive Inverter*

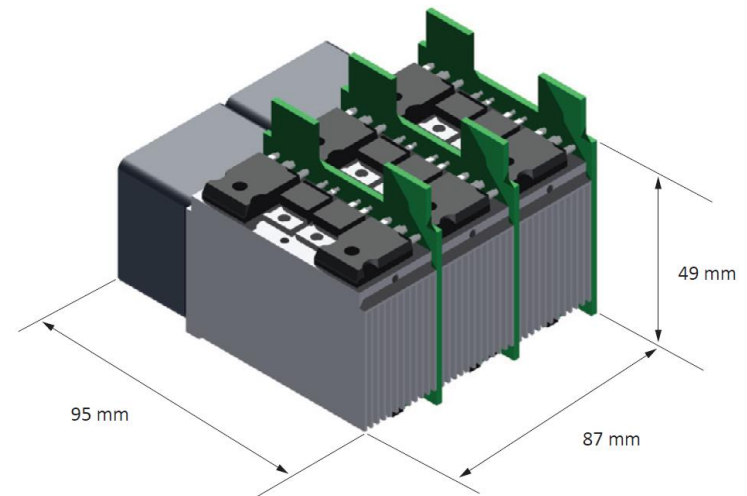
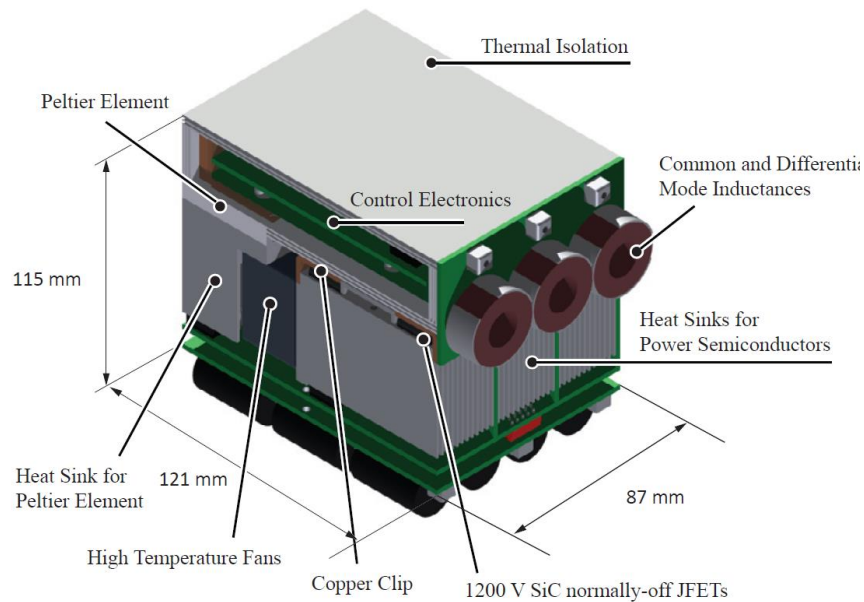
## ► High Temperature (II)



- Power Semiconductors and Cooling
- Signal Electronics

## ■ Thermal Concept of Inverter System

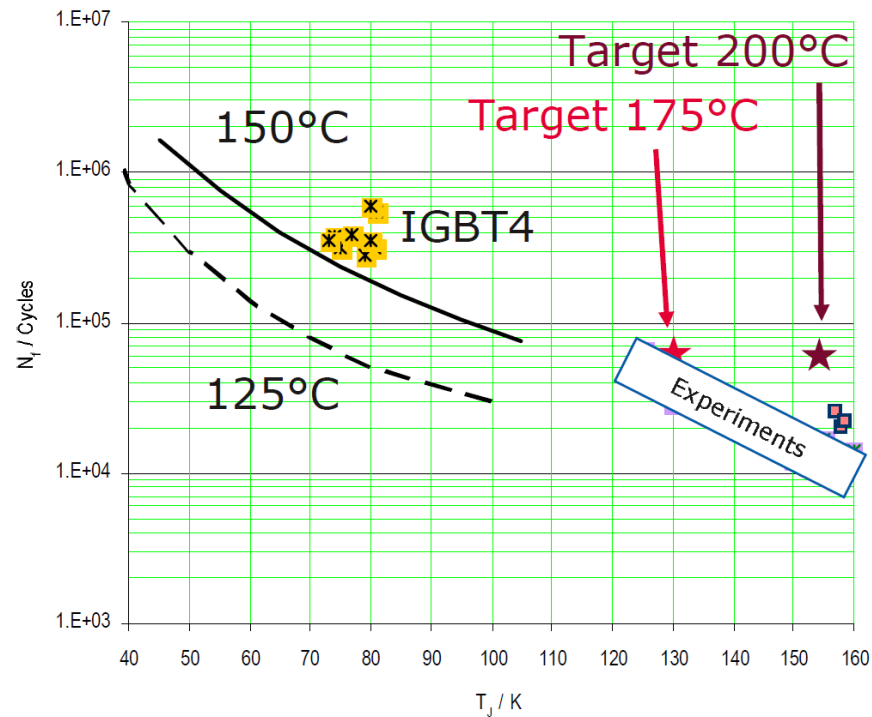
## ► High Temperature (III)



- Missing HT Package (Reliability)
- Missing HT Sensors & Control Electronics & Fans etc.

## ► Power Semiconductors Load Cycling Capability

### ■ New Die Attach Technologies, e.g. Low-Temperature Sinter Technology



Source: Dr. Miller / Infineon

## ► Observation

- SiC ... Not Yet a “Killer” Technology
  - GaN (!) ... Cost Advantage
- Future:  $U > 1.7\text{kV}$   
Only for  $U < 600\text{V}$  in 1<sup>st</sup> Step



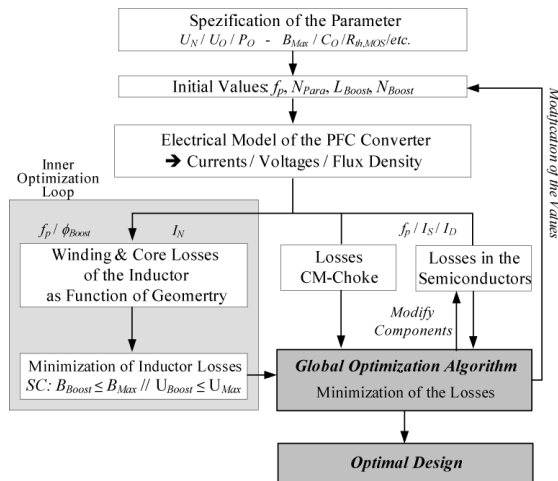
- Do Not Forget the Continuous Improvement of Si Devices (!)
- System Level Adv.e of SiC Still to be Clarified (More Basic Topologies, Smaller Passives)
- SiC for High Efficiency (e.g. for PV or for High Power Density / Low Cooling Effort)

\_\_\_\_\_ **New Simulation Tools**  

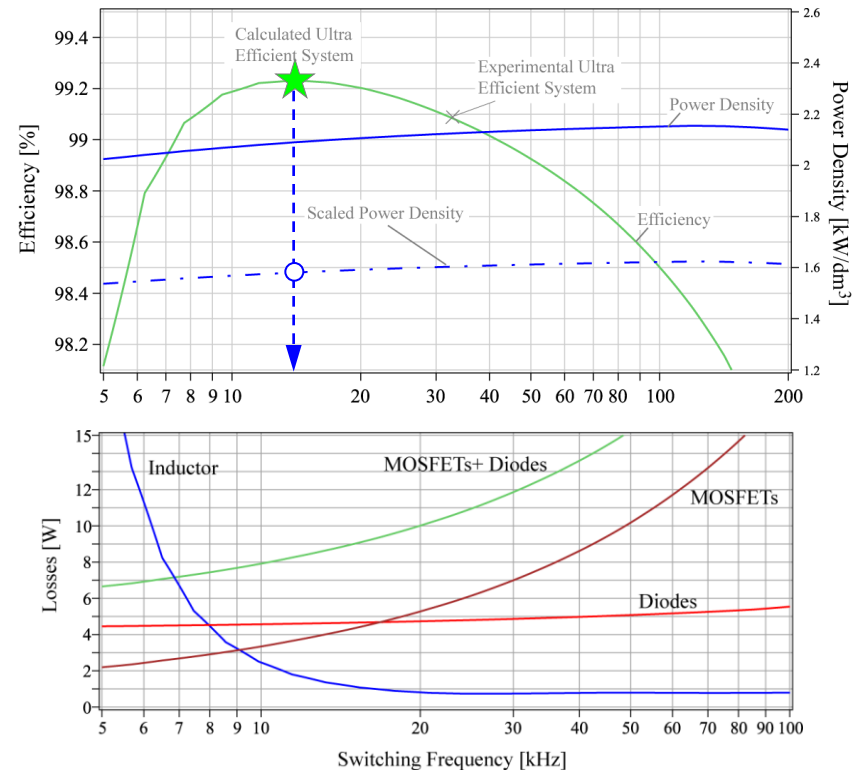


## ► Example: Efficiency Optimization

- Constant Inductor Volume
- Variation of  $f_p$



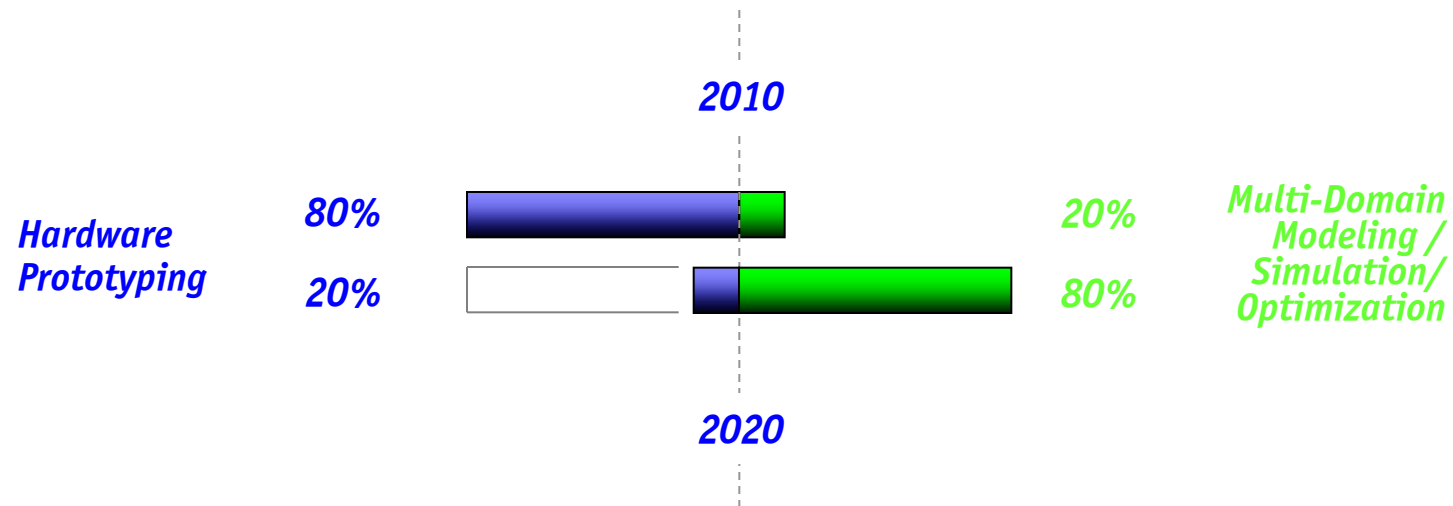
99.2% @ 1.6 kW/dm<sup>3</sup>



- “Flat” Optima for Practical (Robust) Systems → Good Engineering – Similar Result

## ► Future Design Process

### ■ Virtual Prototyping



- Reduces Time-to-Market
- More Application Specific Solutions (PCB, Power Module, and even Chips)
- Only Way to Understand Mutual Dependencies of Performances / Sensitivities
- Simulate What Cannot Any More be Measured (High Integration Level)

## Resulting Research Topics

## ► Potential Research Topics

### — Components — Converters — Systems



- WBG
- Interconnections
- Packaging
- MF Insulation
- Cooling Concepts
- Active Gate Control
- Magn. Flux Meas.
- Acoustic Noise of Mag. Comp.
- Wireless Sensing / Monitoring.
- etc.

- Benchmark SiC / GaN
- High Freq. / High Curr.
- Low Ind. MV Package
- Partial Discharge@ MF
- Airbearing Cooler etc.
- d/dt Feedback and u,i-Limit
- Magnetic Ear
- Influence of DC Magn.
- Wireless Voltage Probe

### - Integration

\* Magnetic

- Inductor/Transformer
- Interph. Transf., Coupl. Ind.
- CM/DM EMI Filter
- RB-, RC-IGBTs

\* Semicond.

\* Power &  
Information

### - Hybridization

\* Act./Passive

- Hybrid Filters / SSTs etc.

- More Oriented to Spec. Application
- Important but **Mostly Incremental**



## ► Potential Research Topics

— Components  
— **Converters**  
— Systems



### - New Topologies & Modularization

- \* MV/MF DC/DC
  - \* MV-Connect.
  - \* Extr. Conv. Ratio
  - \* Extr. Efficiency
  - \* High Curr.
  - \* High Pressure
  - \* Integr. of Funct.
  - \* Fault Tolerance
- Const. V-Transf. Ratio
  - Inp. Series / Outp. Parall.
  - Series Conn. of Switches
  - Aux. Supplies
  - Datacenters / DC Distr.
  - Parallel Operat. of Conv.
  - Subsea Appl.
  - Supply & Filtering etc.

### - Control

- \* Distr. Conv. Syst.
  - \* Parasitic Curr.
  - \* Highly Dyn. Conv.
- Traction/Ship/Aircraft/Subsea
  - Circul. Curr. / CM Curr. etc.
  - High Bandw., incl. Res. Conv.

### - Comp. Evaluation

- \* Multi-Objective
- Cost Models
  - Reliability / Lifetime Models
  - Circ. / Magn. Models
  - Interact. Opt. Tools

■ More Oriented to **Spec. Application**



## ► Potential Research Topics

— Components  
— Converters  
— **Systems**



### Systems incl. Hybrid Systems

- Converter & Load
- Power & Inf.
- Hydraulic/El.
- Wireless Power
- etc.

- Losses Conv. vs. Machine
- Smart Houses
- Smart Batteries etc.
- Hybrid Cranes/Constr. Mach.
- Ind. Power Transfer incl. Inf.

■ Important → **Large Future Potential !**



← **“Optimistic”** View  
Barriers can be Shifted,  
New Converter Technologies etc.

└── **“Pessimistic”** View ──→

## ► “Pessimistic” View → Consider Converters like “ICs”

- If Only Incremental Improvements of Converters Can Be Expected

→ Shift to New Paradigm !



$$p(t) \rightarrow \int_0^t p(t) dt$$

- “Converter” → “Systems” (Microgrid) or “Hybrid Systems” (Autom. / Aircraft)
- “Time” → “Integral over Time”
- “Power” → “Energy”



## ► “Pessimistic” View → Consider Converters like “ICs”

- If Only Incremental Improvements of Converters Can Be Expected

→ Shift to New Paradigm !



$$p(t) \rightarrow \int_0^t p(t) dt$$

- |                       |   |   |
|-----------------------|---|---|
| — Power Conversion    | → | Energy Management / Distribution                                    |
| — Converter Analysis  | → | System Analysis (incl. Interactions Conv. / Conv. or Load or Mains) |
| — Converter Stability | → | System Stability (Autonom. Cntrl of Distributed Converters)         |
| — Cap. Filtering      | → | Energy Storage & Demand Side Management                             |
| — Costs / Efficiency  | → | Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency     |
| — etc.                |   |   |

## ► Example: Smart Grid

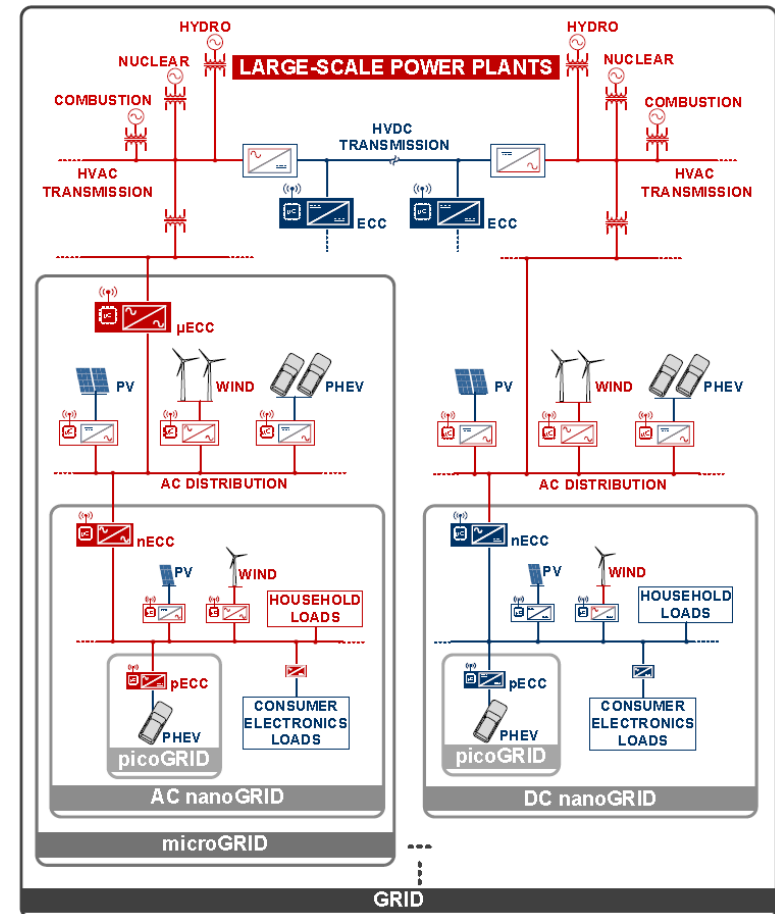
- Borojevic (2010)

### ■ Hierarchically Interconnected Hybrid Mix of AC and DC Sub-Grids

- Distr. Syst. of Contr. Conv. Interfaces
- Source / Load / Power Distrib. Conv.
- Picogrid-Nanogrid-Microgrid-Grid Structure
- Subgrid Seen as Single Electr. Load/Source
- ECCs provide Dyn. Decoupling
- Subgrid Dispatchable by Grid Utility Operator
- Integr. of Ren. Energy Sources

### ■ ECC = Energy Control Center

- Energy Routers
- Continuous Bidir. Power Flow Control
- Enable Hierarchical Distr. Grid Control
- Load / Source / Data Aggregation
- Up- and Downstream Communic.
- Intentional / Unintentional Islanding for Up- or Downstream Protection
- etc.



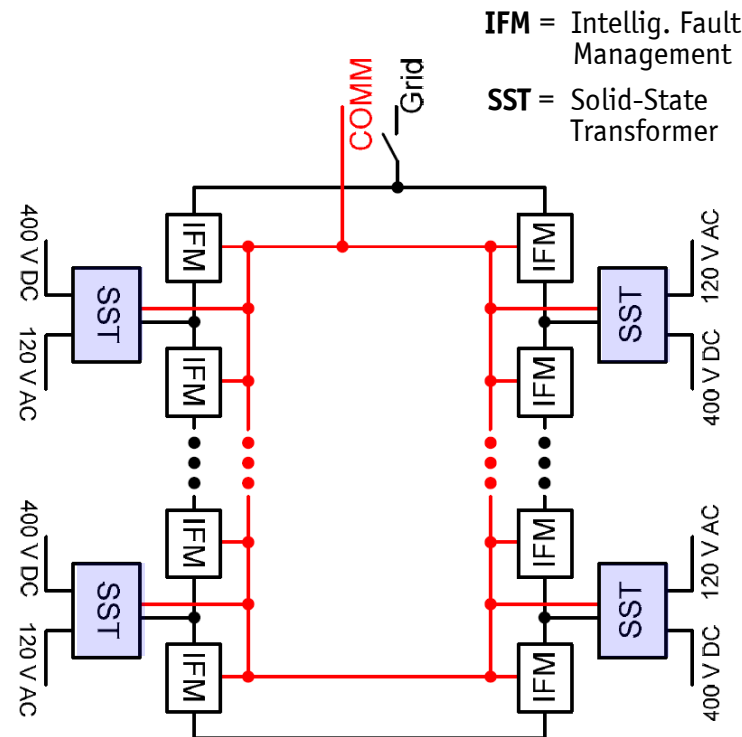
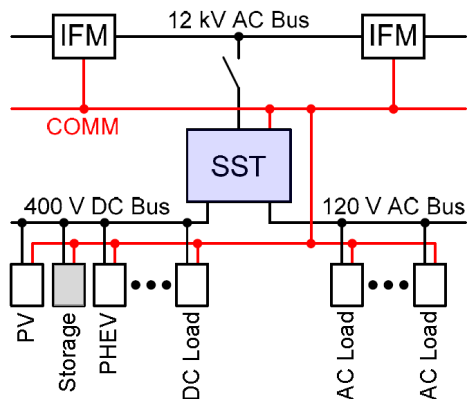
## ► Example: FREEDM Systems

### Future Renewable Electric Energy Delivery & Management Systems

- Huang et al. (2008)

#### ■ “Energy Internet”

- Integr. of DER (Distr. Energy Res.)
- Integr. of DES (Distr. E-Storage) + Intellig. Loads
- Enables Distrib. Intellig. through COMM
- Ensure Stability & Opt. Operation
- AC and DC Distribution

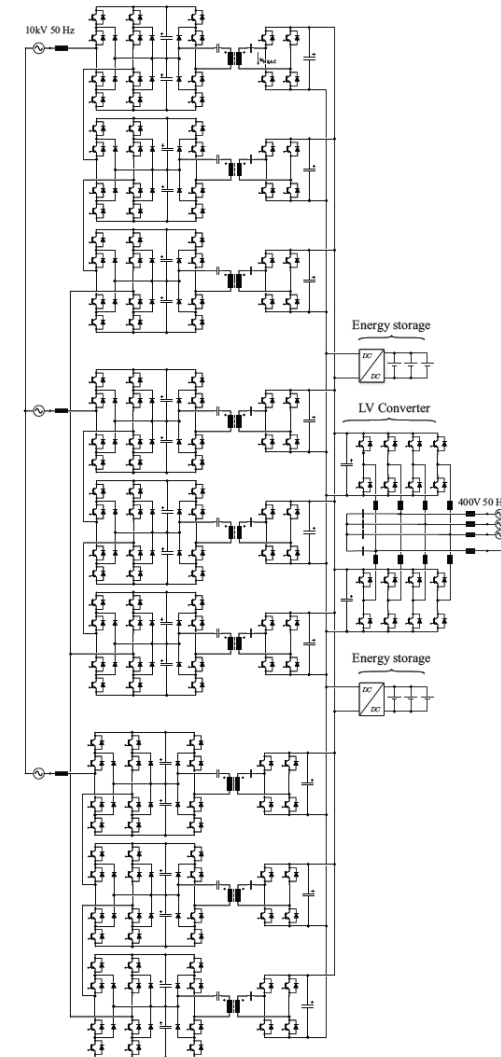
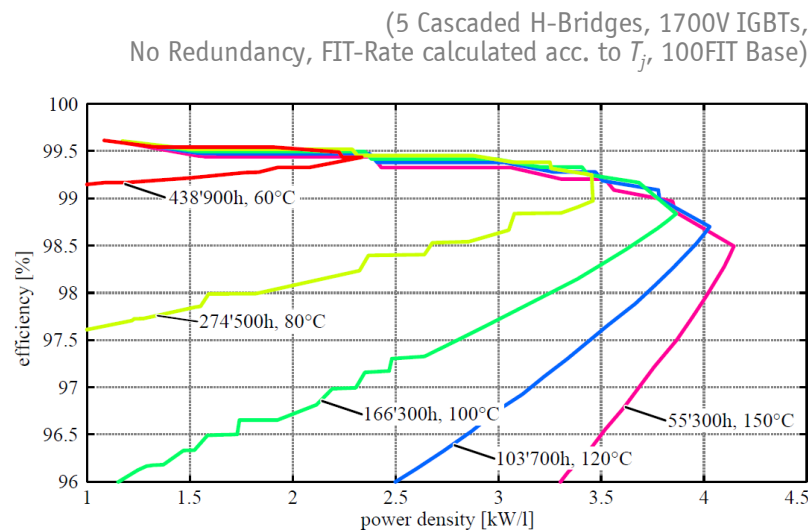


#### ■ Bidirectional Flow of Power & Information / High Bandw. Comm. → Distrib. / Local Autonomous Cntrl

## ► Solid-State Transformer

$$\begin{aligned} S_N &= 630\text{kVA} \\ U_{LV} &= 400\text{ V} \\ U_{MV} &= 10\text{kV} \end{aligned}$$

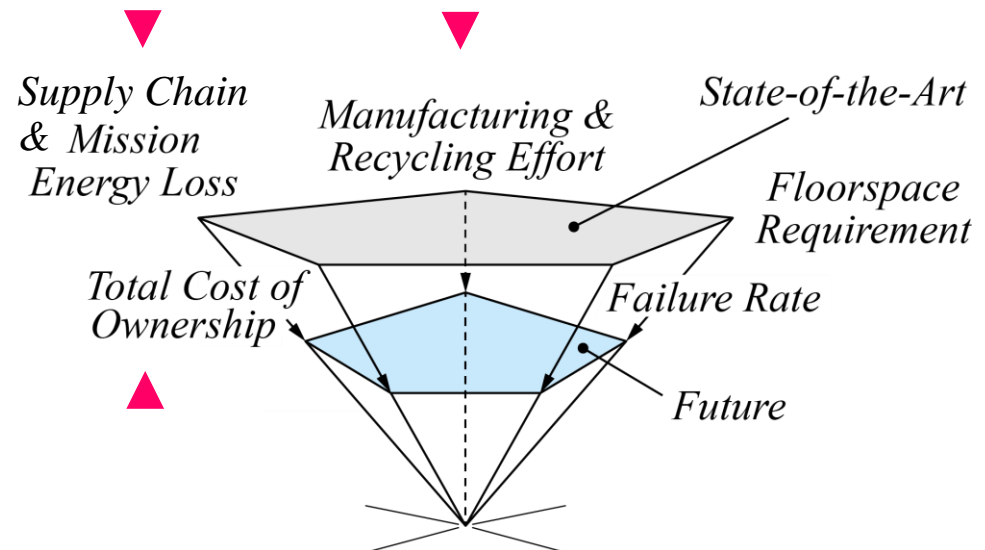
■ Trade-Off → Mean-Time-to-Failure vs. Efficiency / Power Density



## ► Power Electronics **Systems** Performance Figures/Trends

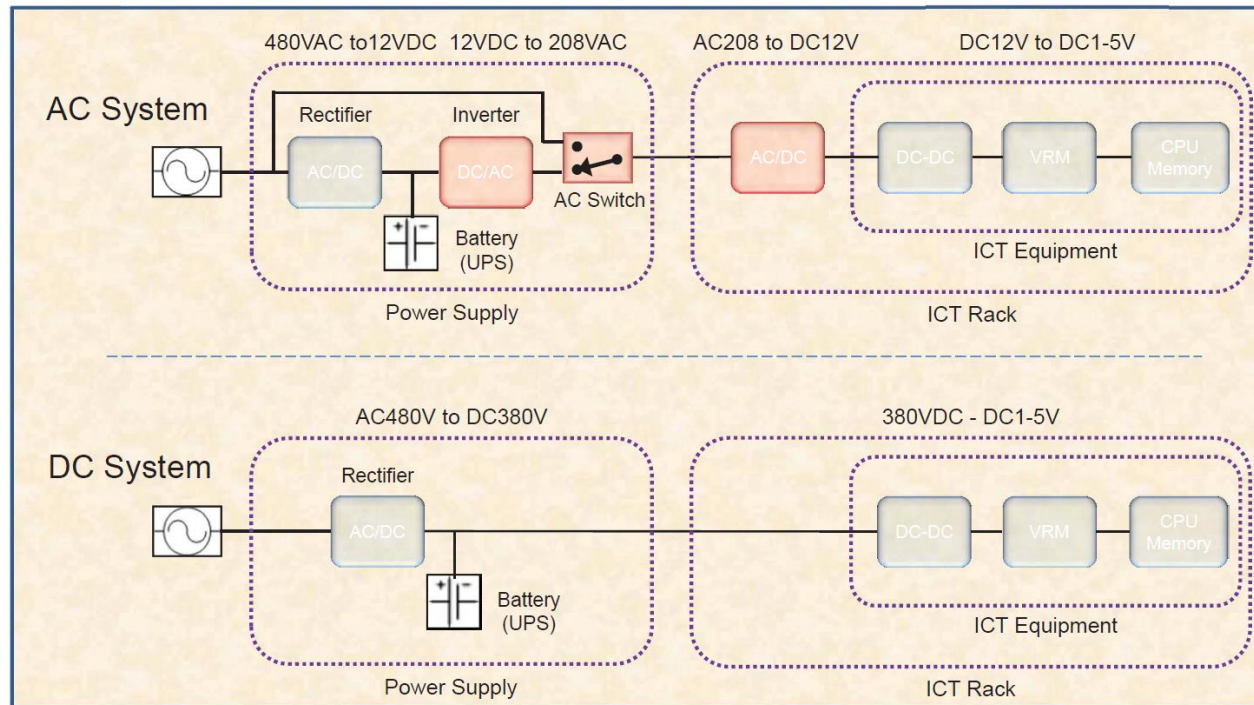
### ■ Complete Set of New Performance Indices

- Power Density [kW/m<sup>2</sup>]
- Environm. Impact [kWs/kW]
- TCO [\$/kW]
- Mission Efficiency [%]
- Failure Rate [h<sup>-1</sup>]



## AC vs DC Power Systems for Data Centers

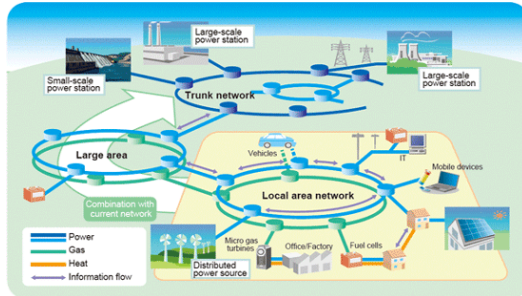
Reduce Loss, Footprint; Improve Reliability, Power Quality



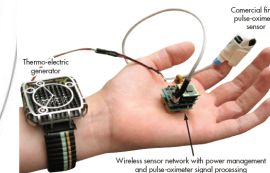
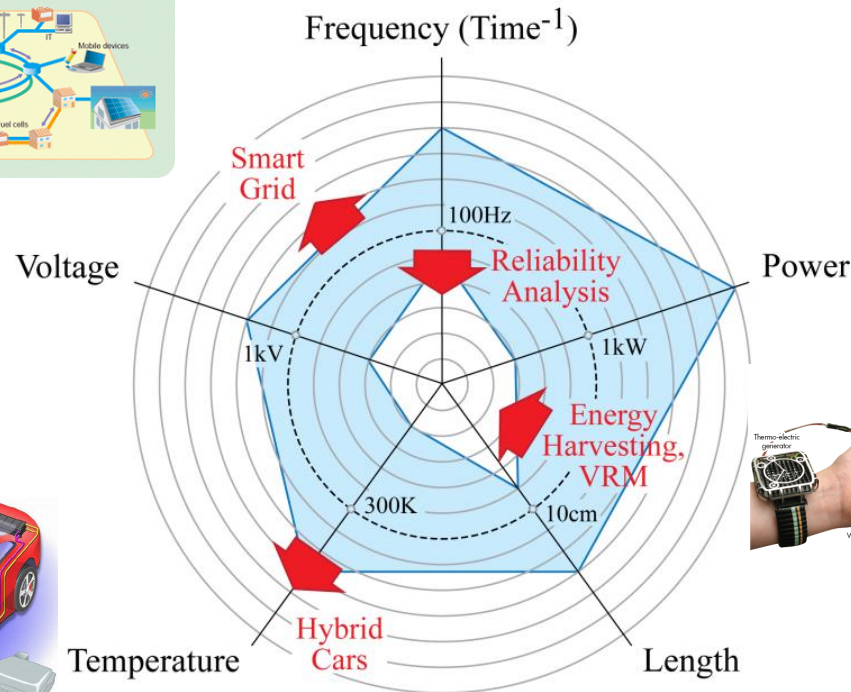
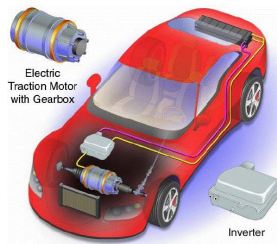
© 2011 EMerge Alliance



## ► Possible Future Extensions of Power Electronics Systems Applications



Source: AIST





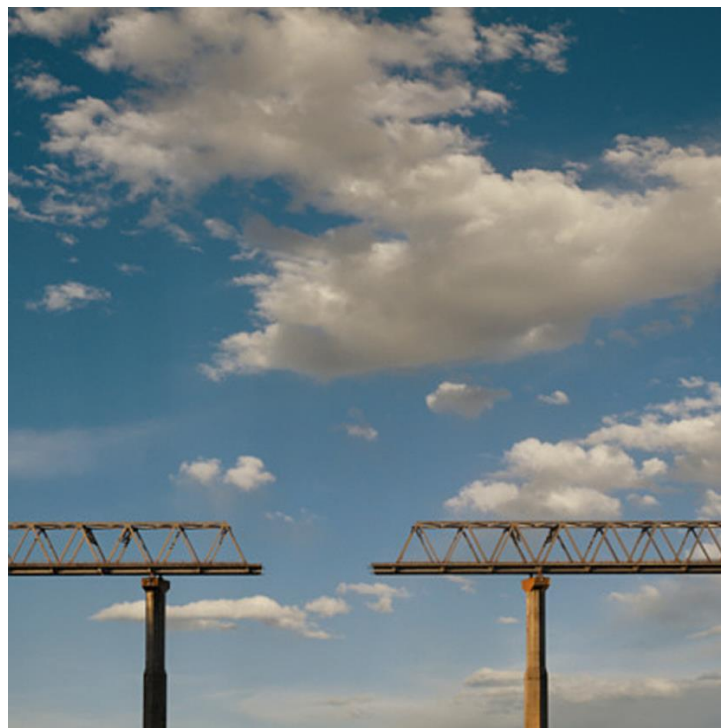
## Remarks on University Research





## ► University Research Orientation

### ■ General Observations



- Gap between Univ. Research and Industry Needs
- In Some Areas Industry Is Leading the Field

## ► University Research Orientation

### ■ Gap between Univ. Research and Industry Needs

#### — Industry Priorities

1. Costs
2. Costs
3. Costs



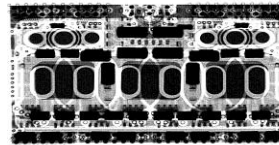
#### — Basic Discrepancy !

Most Important Industry Variable, but  
Unknown Quantity to Universities

- Multiple Objectives ...
- Low Complexity
- Modularity / Scalability
- Robustness
- Ease of Integration into System

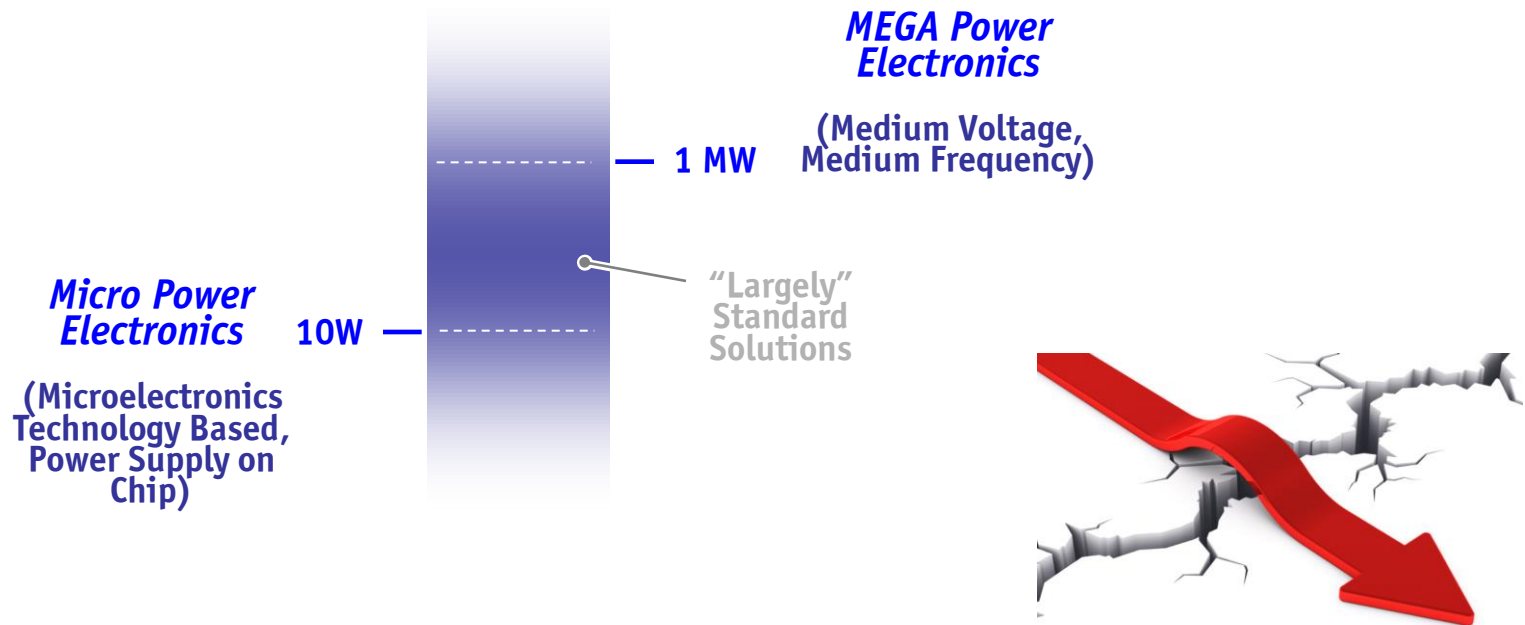
## ► University Research Orientation

- In Some Areas **Industry Is Leading the Field !**



- Industry Low-Power Power Electronics (below 1kW) Heavily Integrated –  
PCB Based Demonstrators Do Not Provide Too Much Information (!)  
Future: “Fab-Less” Research
- Same Situation above 100kW (Costs, Mech. Efforts, Safety Issues with Testing etc.)
- Talk AND Build Megawatt Converters (!)

## ► University Research Orientation



- Establish (Closer) University / Industry (Technology) Partnerships
- Establish Cost Models, Consider Reliability as Performance

## ► University **Education** Orientation

### ■ Need to Insist on High Standards for Education

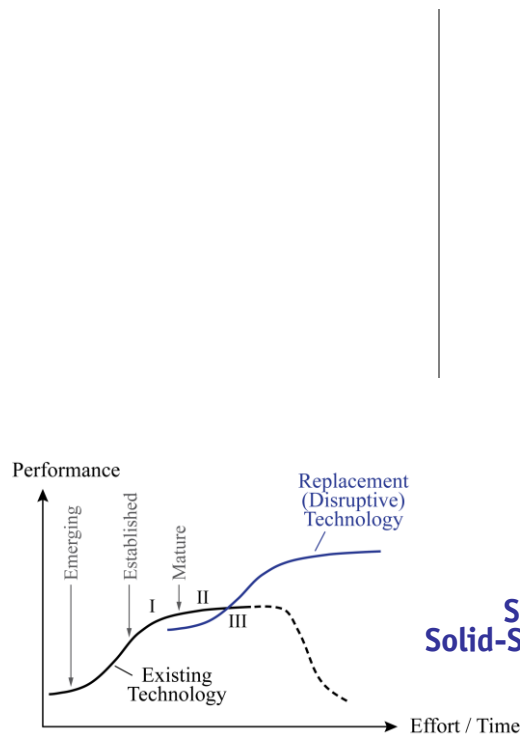
- \* Introduce New Media
- \* Show Latest Stat of the Art (requires New Textbooks)
- \* **Interdisciplinarity**
- \* Introduce New Media (Animation)
- \* Lab Courses!

→ The Only Way to Finally Cross the Borders (Barriers) to  
Neighboring Disciplines !

# Finally, ...

\_\_\_\_\_ **Power Electronics 2.0** \_\_\_\_\_→

## ► Technology S-Curve



...after Switches and Topologies

# “Passives” & EMI

are THE Main Issue of the  
Next Decade

# + Costs + Systems

► Super-Junct. Techn. / WBG  
► Digital Power  
Modeling & Simulation

► Power MOSFETs/IGBTs  
► Microelectronics  
Circuit Topologies  
Modulation Concepts  
Control Concepts

SCRs / Diodes  
Solid-State Devices

Paradigm  
Shift

★  
2014

2025

# Power Electronics 2.0

## New Application Area

- Smart XXX (Integration of Energy/Power & ICT)
- Micro-Power Electronics (VHF, Link to Microelectronics)
- MEGA-Power Electronics (MV, MF)

## Paradigm Shift

- From "Converters" to "Systems"
- From "Inner Function" to "Interaction" Analysis
- From "Power" to "Energy" (incl. Economical Aspects)

## Enablers / Topics

- New (WBG) Power Semiconductors (and Drivers)
- Adv. Digital Signal Processing (on all Levels – Switch to System)
- PEBBs / Cells & Automated (+ Application Specific) Manufacturing
- Multi-Cell Power Conversion
- Multi-Domain Modeling / Multi-Objective Optim. / CAD
- Cybersecurity Strategies



**But,** to get there  
we must ...

## "Bridge the Gaps"

- Univ. / Ind. Technology Partnerships
- Power Electronics + Power Systems
- Vertical Competence Integration (Multi-Domain)
- Comprehensive Virtual Prototyping (Multi-Objective)
- Multi-Disciplinary / Domain Education



# Thank You !

# Questions ?

