



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich



Fraunhofer
IZM



**ECPE Roadmap
2025 Workshop**

Munich, March 26, 2015

Roadmap Power Electronics 2025

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* Fraunhofer IZM, Berlin

** ECPE, Nuremberg



■ Summary of 1st Roadmap Team Meeting

- **Magnetic Components** are the Highest **Cost Factor** in Power Supplies
- **EMI** and Semiconductor Oscillations are **#1 Risk** for **Time to Market**
- **Robustness** is Often More Important than **Reliability**
- **Modularity** Made it **Never Into the Market**
- External Manufacturing Results in Too High Costs
- **Only 6-8 Weeks Development Time** Requires Finished Building Blocks
- Need for Fast Simulation Models
- **Digital Control Issues** (Safety Requirements / **Redundancy**)
- **Efficiency** is also a Political Issue / Depends on **Standardization**
- **Efficiency** is not a **Selling Argument** (only for Last Person in Supply Chain)
- **Ranking: Costs / Reliability / Ease of Manufacturing / Robustness**

Jan. 2014

Sun	Mon	Tue	Wed	Thu	Fri	Sat
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	



Munich

→ **Some Challenges / Limitations Identified**

■ Summary of 2nd Roadmap Meeting

July 2014

Sun	Mon	Tue	Wed	Thu	Fri	Sat
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30	31		



Zurich

... see Summary presented by Th. Harder

■ Summary of 3rd Roadmap Team Meeting

- 2025 Performance Target Values
- Evaluation of Current Research Level Technologies
- Enabling Technologies
- Technology / Research Gaps

Jan. 2015

Sun	Mon	Tue	Wed	Thu	Fri	Sat
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31



Berlin

... see Following Summary



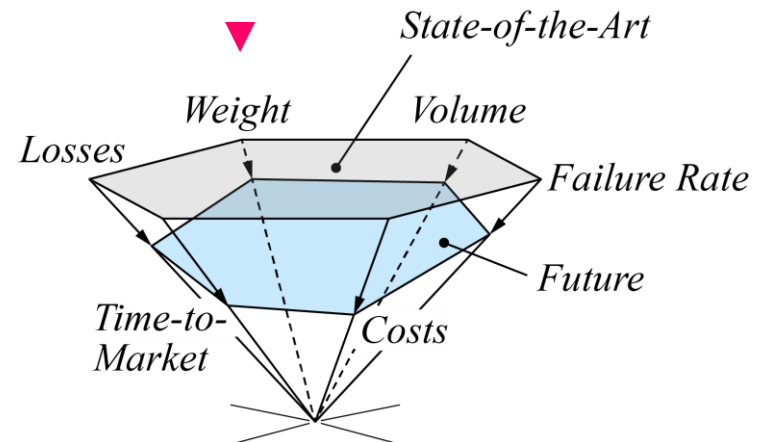
Discussion @ 3rd Meeting →

■ **Key Performance Indices
which Must be Considerably
Improved until 2025**

- Costs
- Power Density
- Efficiency
- Reliability / Robustness
- Time-to-Market

Environmental Impact...

$[\text{kg}_{\text{Fe}} / \text{kW}]$
 $[\text{kg}_{\text{Cu}} / \text{kW}]$
 $[\text{kg}_{\text{Al}} / \text{kW}]$
 $[\text{cm}^2_{\text{Si}} / \text{kW}]$

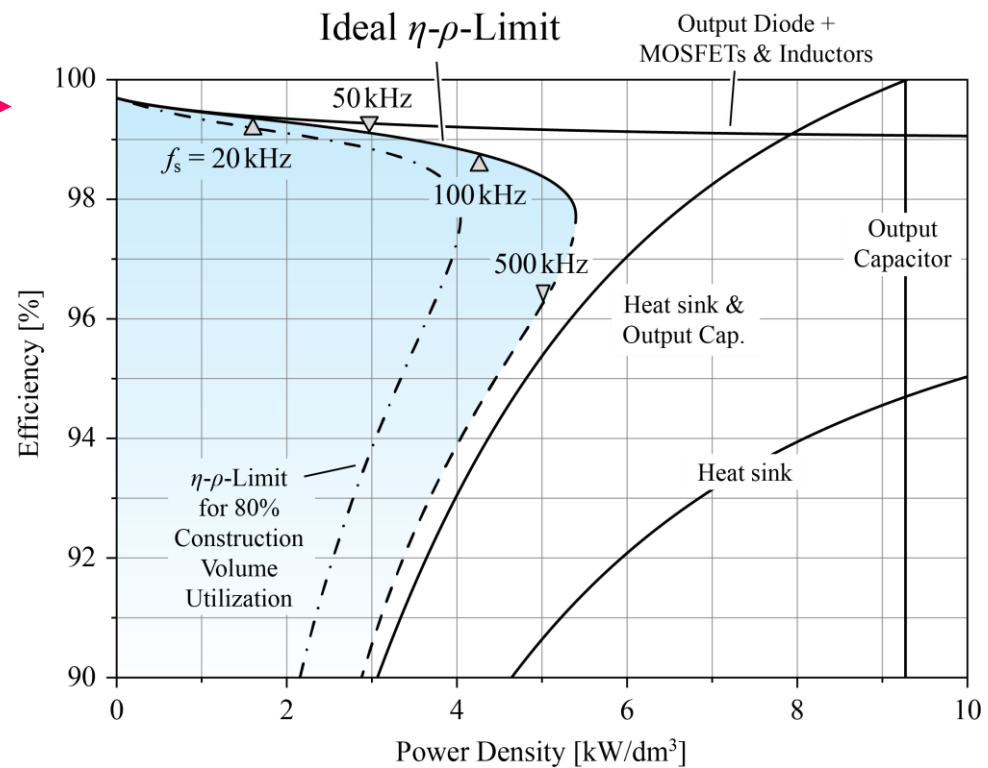


► **Performances are Mutually Coupled**

■ Main Components / Concepts / Processes Determining the Performance Limits

η - ρ -Pareto Limit

- Switching Circuit
- Transformers
- Filter Components
- EMI Filter Components
- Interconnections
- Heatsink
- Sensors
- Control Circuit
- Package
- Manufacturing



■ Roadmap Approach

Step #1

→ Define 2025 Performance Targets

... Considering Past Trend Lines

Step #2

→ Current Research Level Technologies

→ High Switching Frequency

→ High Operating Temperature

... Considered for Each Component in Order to Check for Potential Improvements of a Selected Performance Index

Step #3

→ “Enabling Technologies”

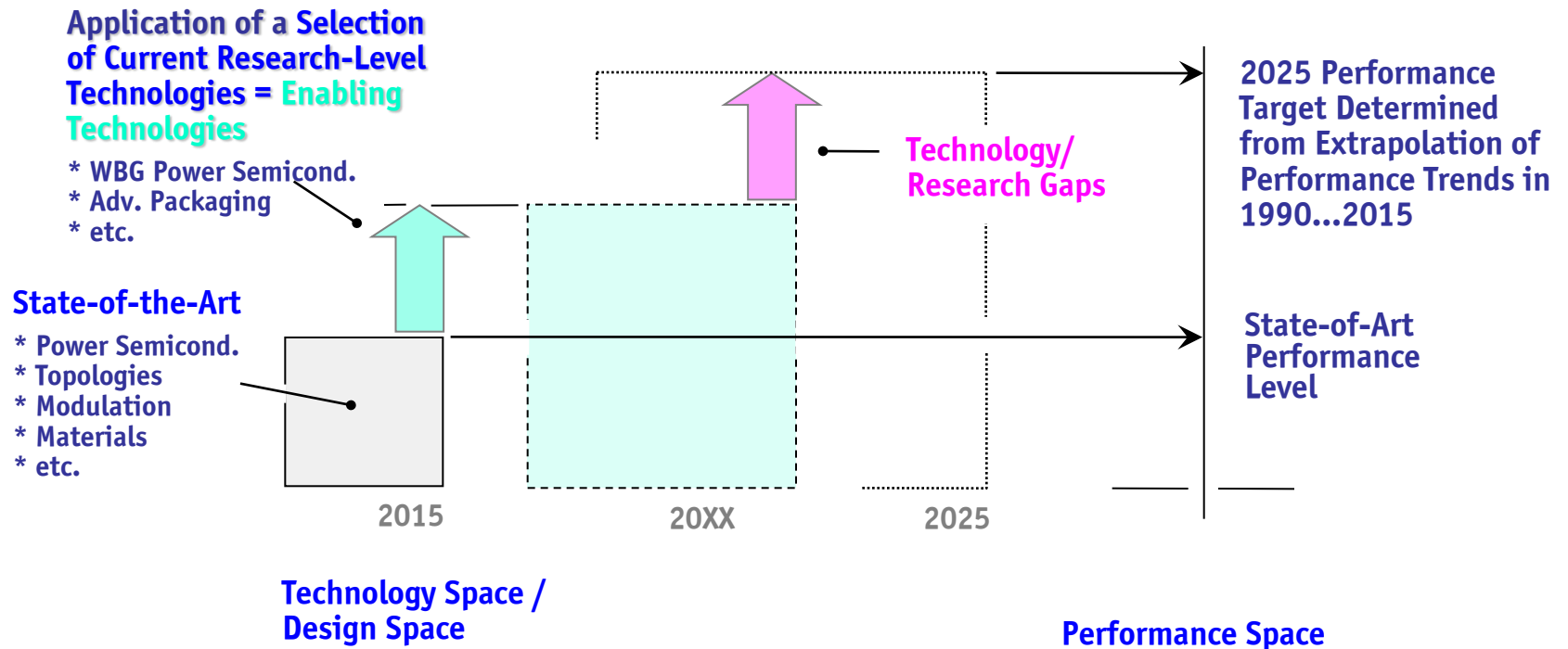
... Selected Subset of “Current Research Level Technologies” which Potentially Enable a Considerable Performance Improvement

Step #4

→ “Technology / Research Gaps”

... Technologies Crucial for Reaching the 2025 Performance Target but Currently Not Considered in Research

Roadmap Approach



■ General Remark

- Pragmatic Approach
- Only Already Known Research Concepts are Considered
- No Speculations on Unknown Disruptive Concepts (e.g. Nanomaterials)
- Identified Barriers are Indicating Future Research Needs
- Trivial Requirements (e.g. Higher Energy Density of Caps) are not Listed

Power Density - Expected Impr. until 2025 – Factor 2 ... 5 (10)

■ Filter Components (→ Minimize Volume)

→ Increase Switching Frequency

Challenges:

- * Higher Switching Losses
- * Higher HF Losses of Passives / Thermal Managmnt
- * Increased EMI Noise (for Hard Switching)

Enablers:

- * Low Switching Loss WBG Semiconductors
- * Adv. Inductor Concepts (e.g. Distributed Gaps)
- * Adv. Packaging – Min. Parasitics (Gate & Power)
- * ZVS / Resonant Converter Concepts
- * High Clock Frequency Digital Control

Barriers:

- * Mag. Materials (Permeability / Losses at HF)
- * Conductor Types / Winding Arrangements
- * Thermal Management
- * Adv. Design Tools (Layout, Magnetics)
- * Adv. Measurem. Tools Integrated with Simulation
- * Engineering Experience

Detour:

- * Interleaving for Frequency Multiplication

Remark:

- * Only Basic Converter Topologies are of Interest

→ „Enablers“ are Taken from the List of „Current Research Technologies“
→ „Barriers“ are Indicating „Technology Gaps“

→ Increase Operating Temp.

Challenges:

- * Reliability of Interconnection Technologies
- * Higher Losses

Enablers:

- * High Temperature Passive Components
- * Interconnection Technologies for Higher Temp.
- * WBG Semiconductors

Barriers:

- * Requirement to Enable all Used Components and Technologies for High Temp.

Remark:

- * Especially Effective for High Temp. Environment

→ Change from CCM to DCM

Challenges:

- * Higher Conduction Losses
- * Higher Filtering Effort

Enablers:

- * Low On-Resistance Power Switches (CoolMOS, WBG)
- * Advanced Digital Control
- * Interleaving for Red. of Filter Effort

Barriers:

- * New Circuit Topologies / Modulation Schemes
- * Magnetic Materials (High Flux Swing, High Frequ.)
- * Conductor Types / Winding Arrangements

Remark:

- * Only Basic Conv. Topologies with Modified Control / Min. Auxiliary Circuits are of Interest

→ etc., etc.

■ EMI Filter (→ Minimize Volume)

→ Increase Switching Frequ. Beyond 500kHz

Challenges:

...

Enablers:

...

Barriers:

...

Remark:

...

→ etc., etc.

■ Heat Sink (→ Minimize Volume)

■ Interconnection / Packaging (→ Minimize Volume)

■ etc.

Efficiency

- Expected Loss Reduction until 2025 – Factor 2 ... 3

■ Evaluation of Contributions to Loss Reduction of the Main Components Employing Current Research Level Technologies

- Switching Circuit and Gate Drive
- Transformers
- Filter Components
- EMI Filter Components
- Heatsink
- Interconnections
- Sensors
- Control Circuit

■ Utilized Current Research Concepts

■ Required Additional New Technologies

- Enabling Technologies
- Technology Gaps

Costs

- Expected Reduction until 2025 – Factor ... 2

- Evaluation of Contributions to Loss Reduction of the Main Components Employing Current Research Level Technologies

- Switching Circuit and Gate Drive
- Transformers
- Filter Components
- EMI Filter Components
- Heatsink
- Interconnections
- Sensors
- Control Circuit

- Utilized Current Research Concepts
- Required Additional New Technologies

- Enabling Technologies
- Technology Gaps

Examples of Enabling Technologies



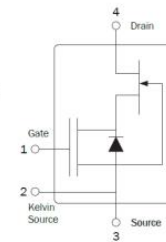
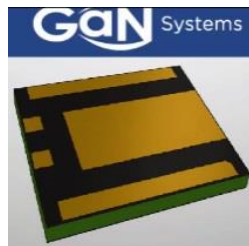
■ Enabling Technologies (1)

→ Wide Bandgap Semiconductors

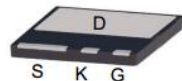
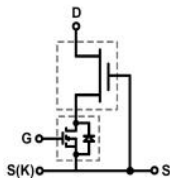
- * Low Switching Losses
- * Low Conduction Losses

→ Next Generation (LV) Si Semiconductors

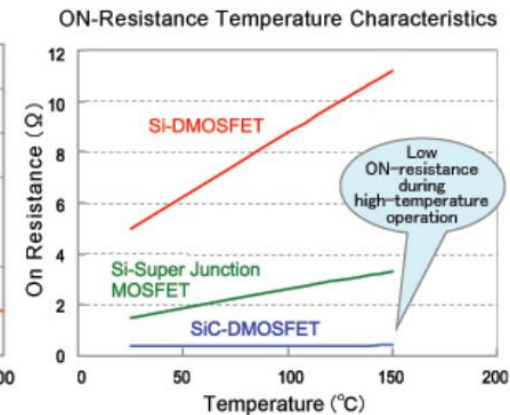
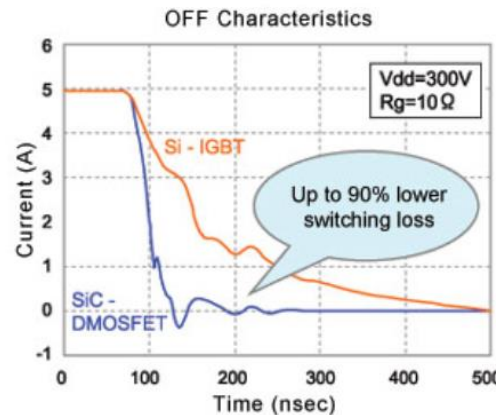
- * Low Conduction Losses



transphorm



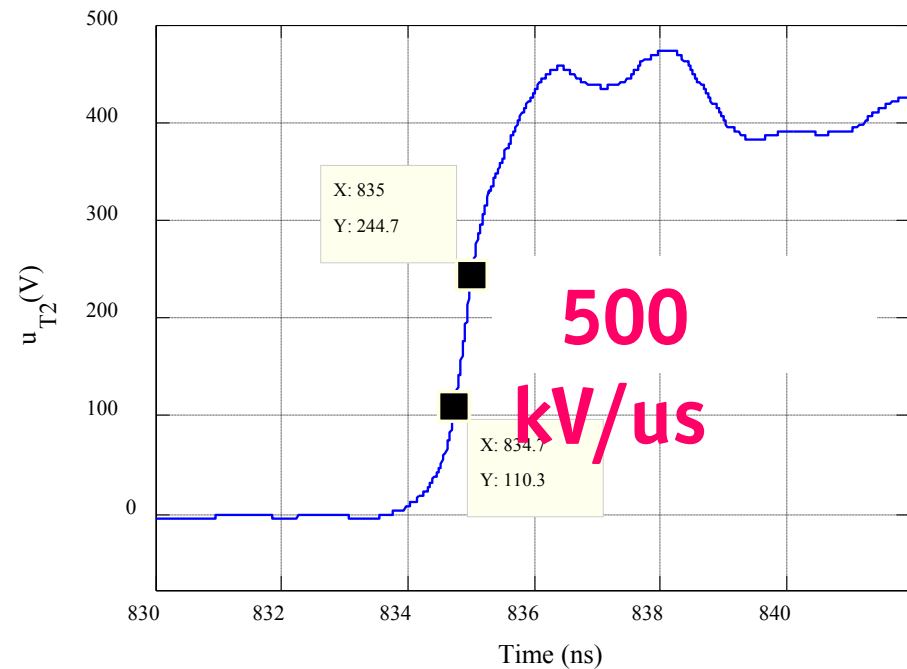
8x8 PQFN Package
(bottom view)



■ Enabling Technologies (2)

- Wide Bandgap Semiconductors
 - * Low Switching Losses
 - * Low Conduction Losses
- Next Generation (LV) Si Semiconductors
 - * Low Conduction Losses

- 600V GaN Switching Behavior
- Main Challenges in Packaging (!)

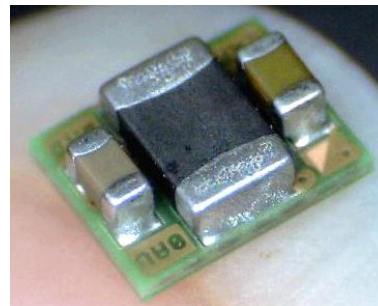


■ Enabling Technologies (3)

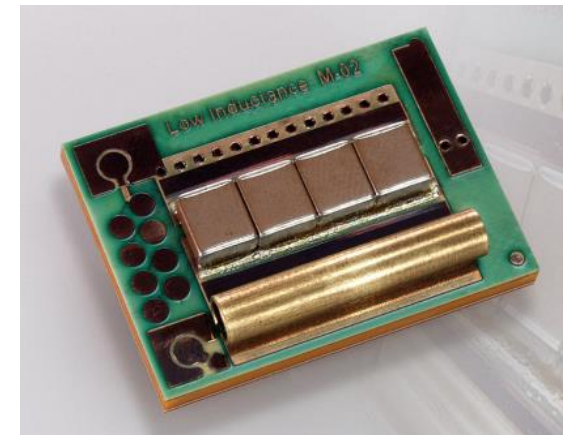
→ Adv. Packaging of Power Semicond (Chip Scale etc.)

- * Low Power Path Parasitics
- * Low Gate Drive Parasitics
- * Low Coupling of Power and Gate Drive Path
- * Low Thermal Resistance
- * 3D Interconnection
- * PCB Embedding (incl. Therm. Management)
- * Minimizing DM and CM EMI (Integr. Switch. Cell)

DC/DC Converter with
Embedded Chip



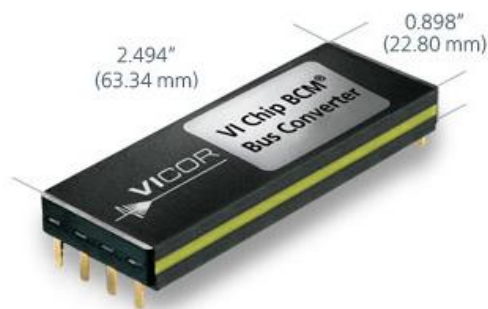
Ultra Low Inductance Package



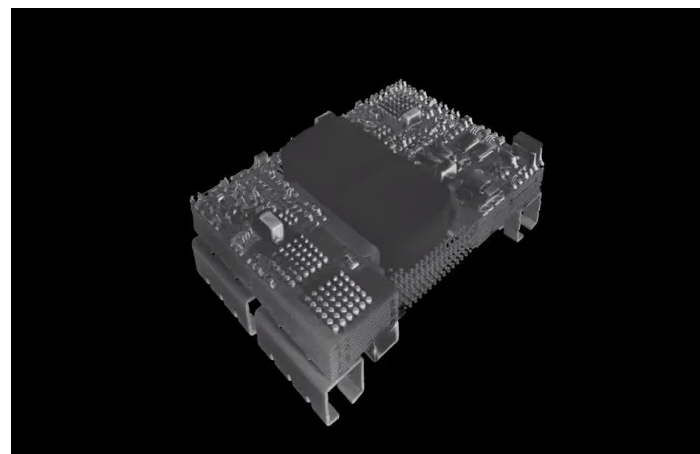
■ Enabling Technologies (4)

→ Heterogeneous Integration

- * Switching Cell in a Package
- * Drivers with Integrated Power Supply
- * DC/DC Converter in a Package



X-Ray Image (Video)



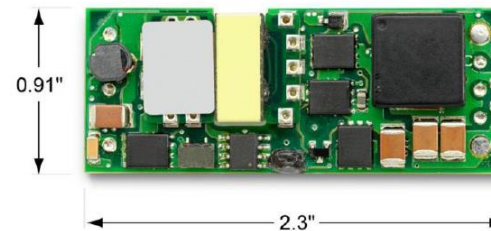
■ Enabling Technologies (5)

→ Heterogeneous Integration

Competitor A

2.1 in² and 34 W/in²

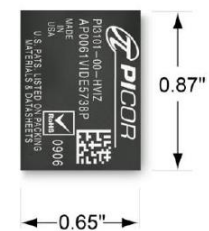
72 Watts



PI3101

0.57 in² and 105 W/in²

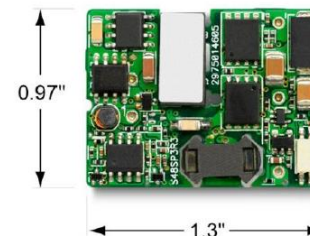
60 Watts



Competitor B

1.26 in² and 26 W/in²

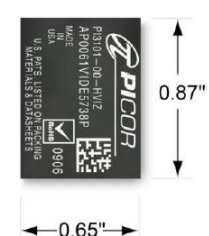
33 Watts



PI3101

0.57 in² and 105 W/in²

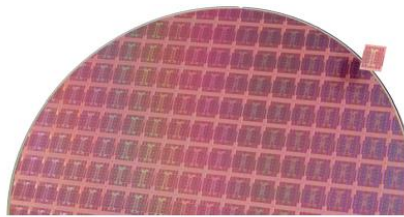
60 Watts



■ System in Package (SiP) Approach

■ Enabling Technologies (6)

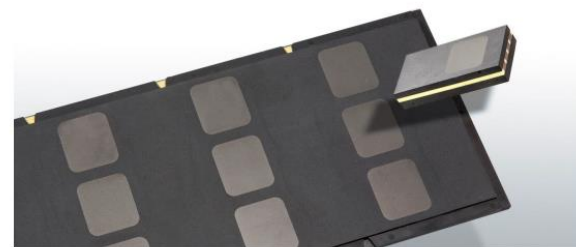
→ Heterogeneous Integration



Information Processors Are Sawn Out of
Scalable Wafers




■ System in Package (SiP) Approach



ChiP Power Components Are Sawn Out of
Scalable Magnetic Panels


■ Enabling Technologies (7)

→ Heterogeneous Integration



12V PowerStage in Embedded Die System-in-Package

Greg J. Miller
Sr. VP – Engineering
Sarda Technologies, Inc.
gmiller@sardatech.com

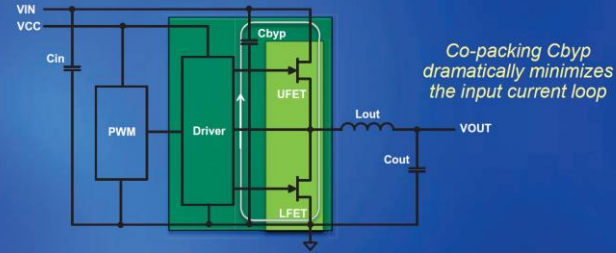


APEC 2015


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Challenges to Higher Density 12Vin POL solutions

- (1) FET Switching Losses → Sarda GaAs FET
- (2) High current inductors are large → Multiphase (lower I/phase)
- (3) Parasitic Impedances → Integrated Power Stage



Co-packing Cbyp dramatically minimizes the input current loop



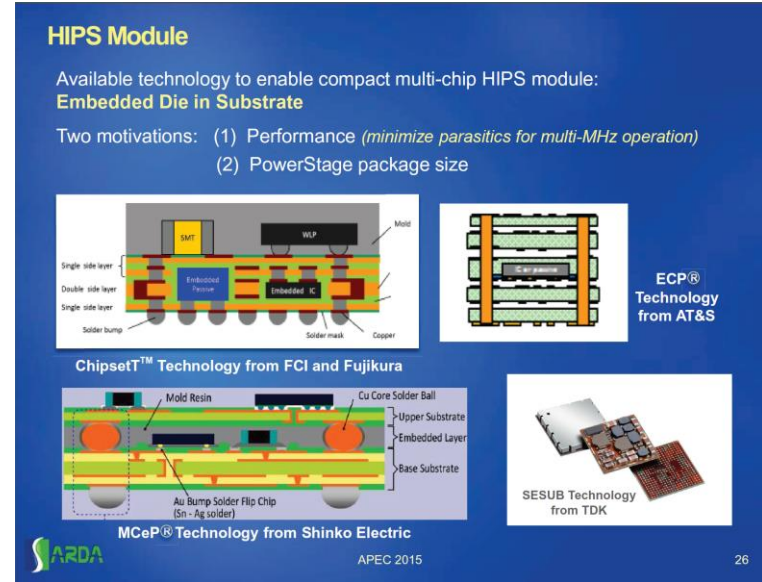
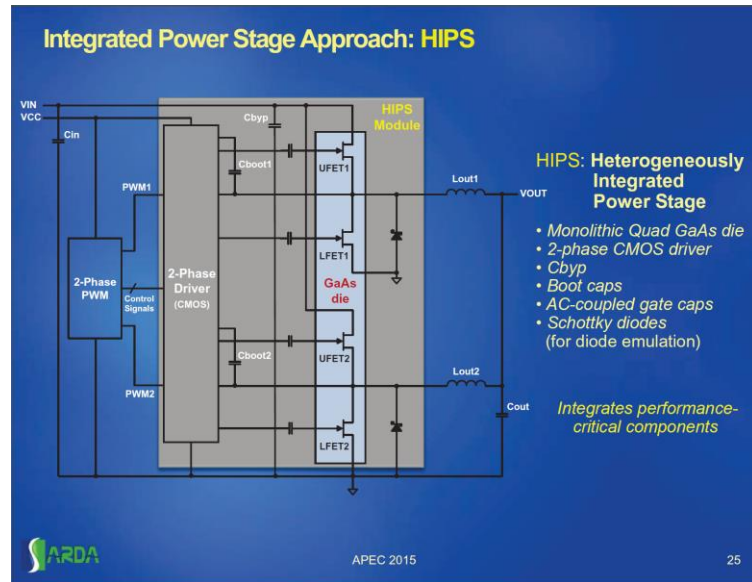
APEC 2015

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► Presented @ APEC 2015

■ Enabling Technologies (8)

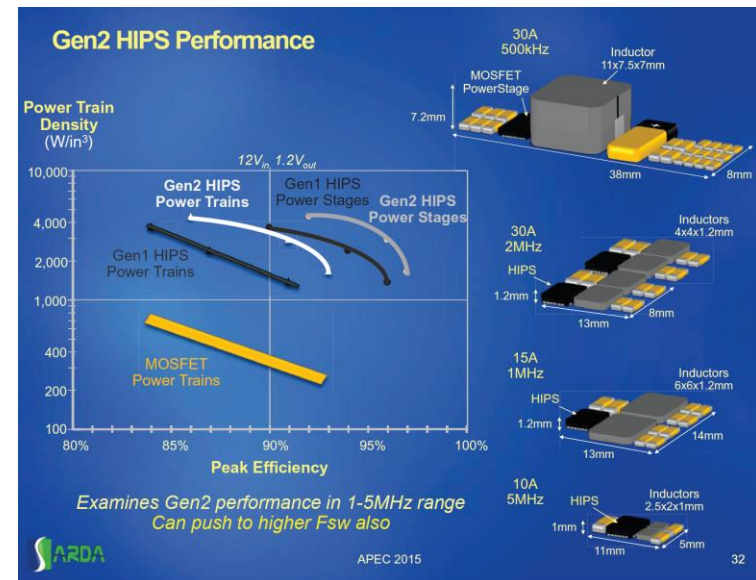
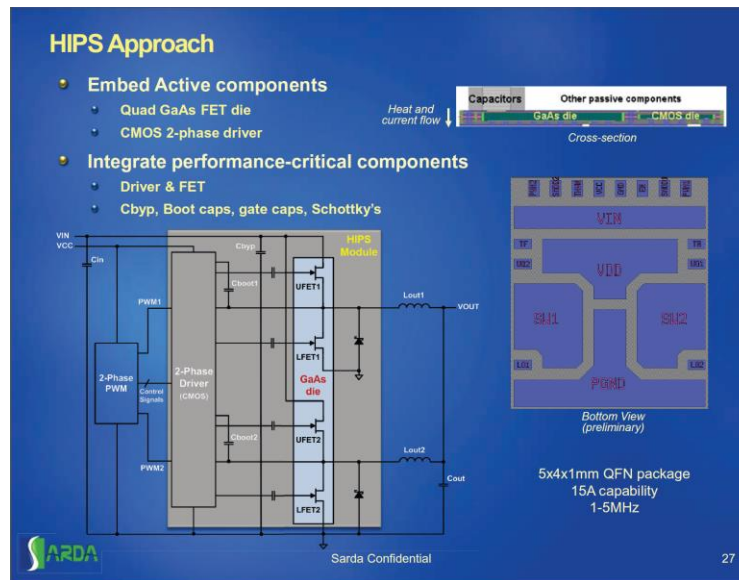
→ Heterogeneous Integration



► Presented @ APEC 2015

■ Enabling Technologies (9)

→ Heterogeneous Integration



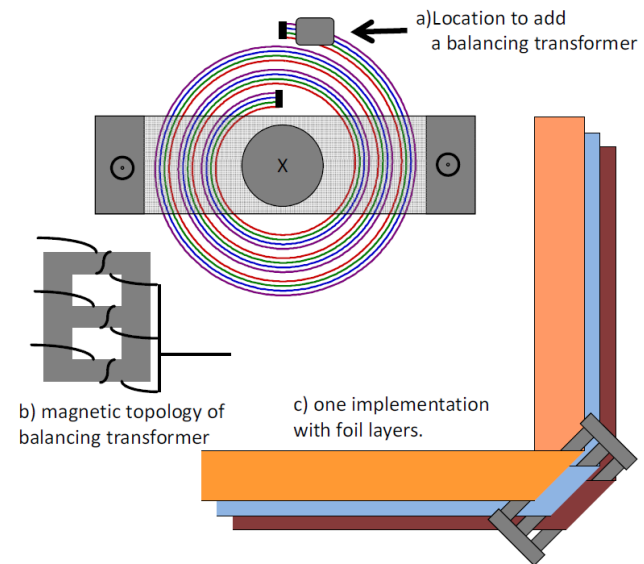
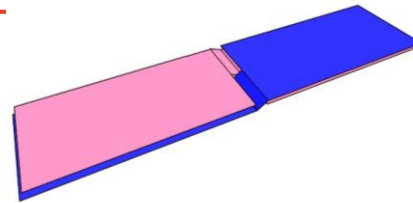
► Presented @ APEC 2015

■ Enabling Technologies (10)

- **Adv. Inductor Concepts**
 - * Magnetic Integration (CM/DM)
 - * Multi-Gapped Magnetic Cores
 - * Constant Flux Density Magnetic Cores
 - * Integrated Cooling
 - * Parasitic Capacitance Cancellation
 - * 3D Interconnection
- **Adv. Capacitor Concepts**
 - * Low Parasitic Ind. 3D Interconnection
 - * Integrated Cooling / High Current Concepts
- **Adv. Component Interconnection Concepts**
 - * Low DC and HF Loss Interconnection
 - * Integrated Concepts (Cooling, Sensing)
- **Adv. Cooling Concepts**
 - * Heat Spreading Concepts
 - * Two-Side Cooling
 - * Two Phase Cooling
 - * Integr. Concepts (El. and Thermal Interconn.)
- **Adv. Low Frequency Energy Buffer Concepts**
 - * Replace Electrolytic Cap. by Conv. And High Δv Cap.

■ Enabling Technologies (11)

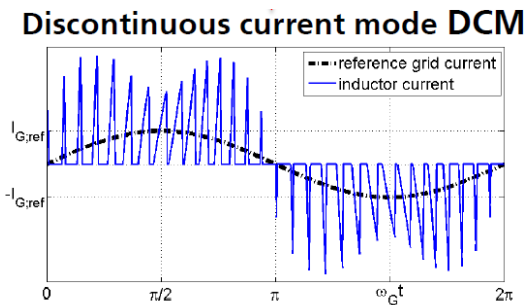
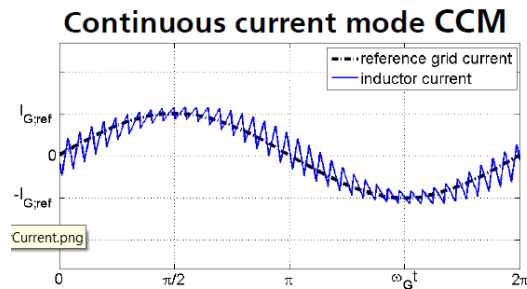
→ Advanced Inductor Concepts



Source: Ch. Sullivan / Dartmouth

- ▶ Layered Foils as Alternative to Litz Wire
- ▶ New Winding Geometries
- ▶ Quasi-Distributed Airgap
- ▶ etc.

■ Enabling Technologies (12)



→ Digital Control (Moores Law)

- * High Calc. Capability / Monitoring / Adv. Control
- * High Clock Rates / High Sampling Frequ.

→ Change from CCM to DCM Operation

- * DCM Inductors Store Less Energy / Lower Vol.
- * Facilitates ZVS / Res. Transition Operation
- * Workaround for Slow Passives Improvement
- * $i=0$ Instead of Cont. Current Sensor

→ Advanced Modulation

- * Noise Shaping Variable Switching Frequency

→ Active ZVS / Resonant Operation

- * Low Switching Losses
- * Low EMI / No Free Ringing

→ Interleaving / Multi-Cell / Multi-Level Converters

- * Increase of Effective Switching Frequency
- * Cancellation (DM-CM Transfer) instead of Filtering

→ Advanced Control

- * Trajectory-Based Control
- * Predictive Control

■ Enabling Technologies (13)

→ Bringing Together Advanced Circuit Concepts / Semiconductors / Packaging



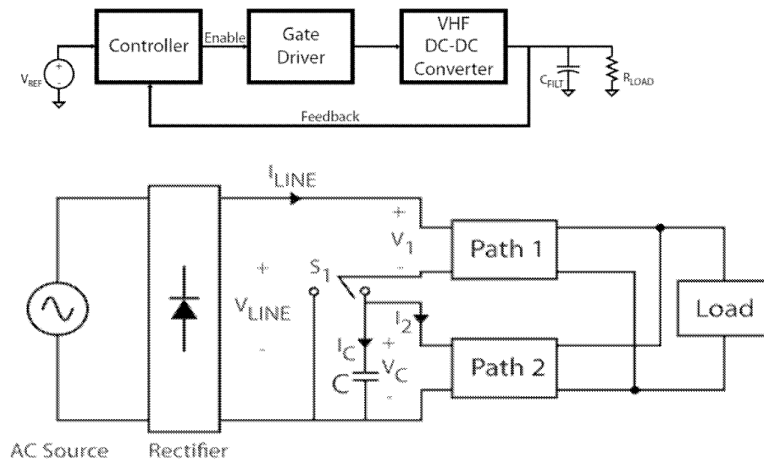
* World Smartest Laptop Charger



* World Smallest Laptop Charger

■ Enabling Technologies (14)

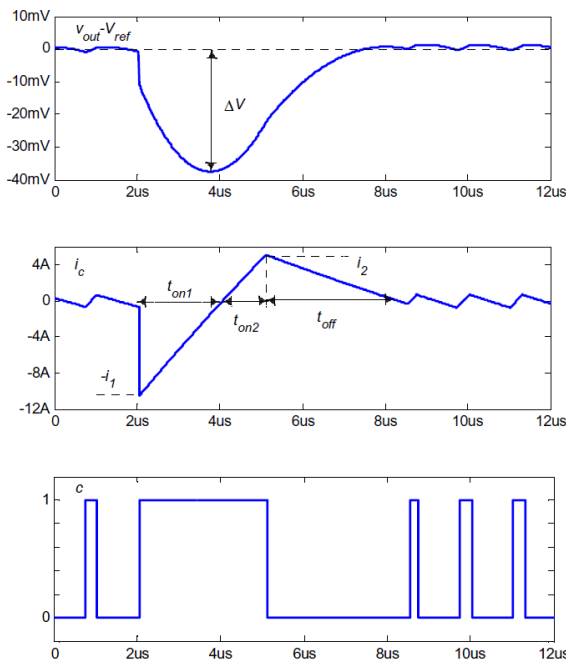
→ Bringing Together Advanced Circuit Concepts / Semiconductors / Packaging



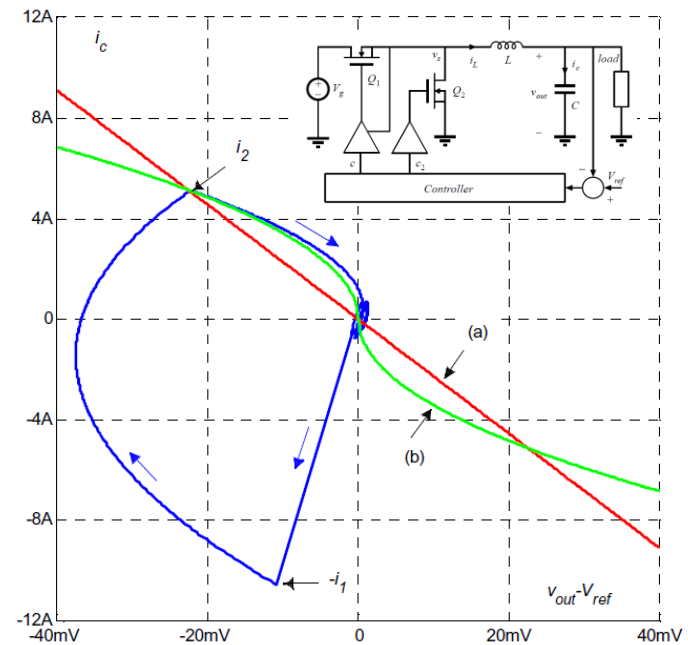
* World Smallest Laptop Charger

■ Enabling Technologies (15)

→ Predictive Control and Optimal Trajectory Control



Source: TI / Yousefzadeh



► Consider Individual Switching Instants vs. Average over Numerous Switching Cycles

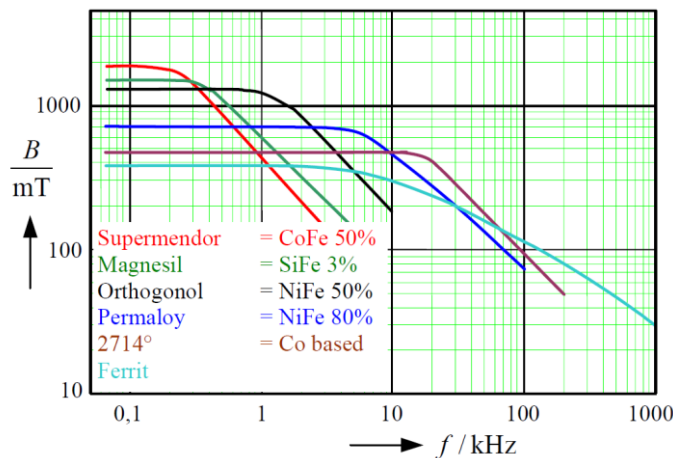
Examples of Technology Barriers



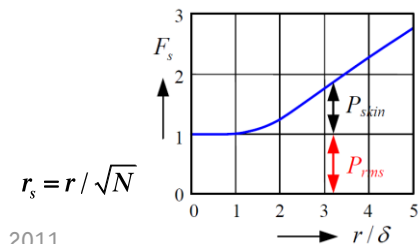
Technology Barriers

► Example: Serious Limitation of Operating Frequency by HF Losses

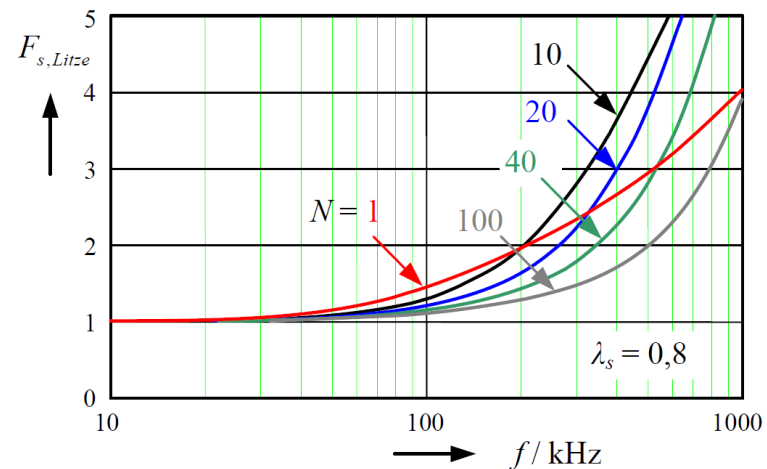
- Core Losses (incr. @ High Freq. & High Operating Temp.)
- Temp. Dependent Lifetime of the Core
- Skin-Effect Losses
- Proximity Effect Losses



■ Adm. Flux Density for given Loss Density



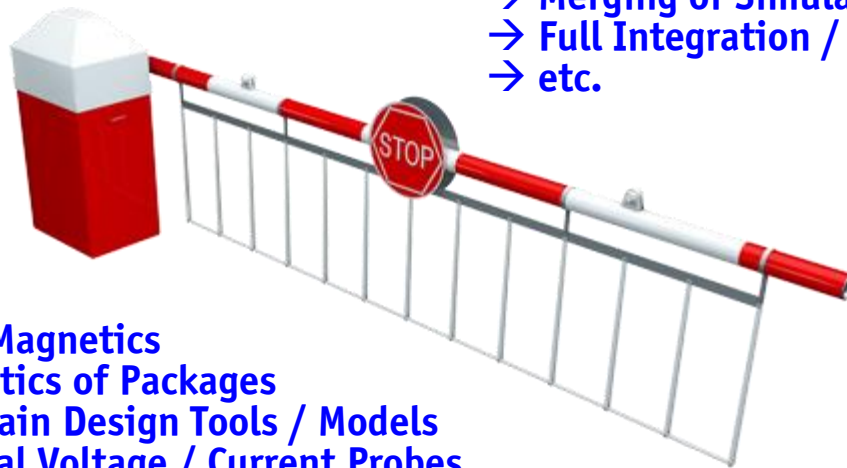
Source: Prof. Albach, 2011



■ Skin-Factor F_s for Litz Wires with N Strands

Technology Barriers

- >50 MHz Switches
- Multi-Domain/Objective Design / Models
- Design for (3D) Manufacturing
- Manufact. of 3D-Integrated Planar Structures
- Built-In Measurement Devices
- Merging of Simulation & Measurement
- Full Integration / Limited Flexibility
- etc.



- < 500 kHz Magnetics
- High Parasitics of Packages
- Single Domain Design Tools / Models
- Conventional Voltage / Current Probes
- Discrete Components / Max. Flexibility
- Technological Limits of Universities
- etc.

► Chicken & Egg Problem of New Technologies / Identification of Killer Applications

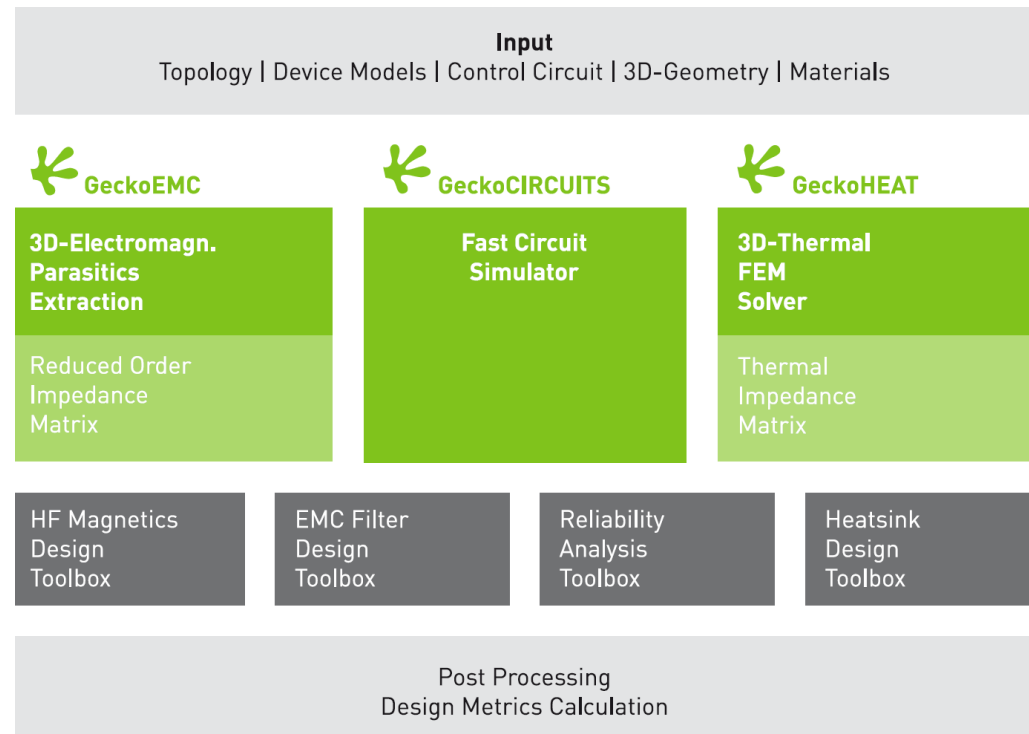
► Example of Advanced Power Electronics Design Platform

Source:



■ Modeling & Design

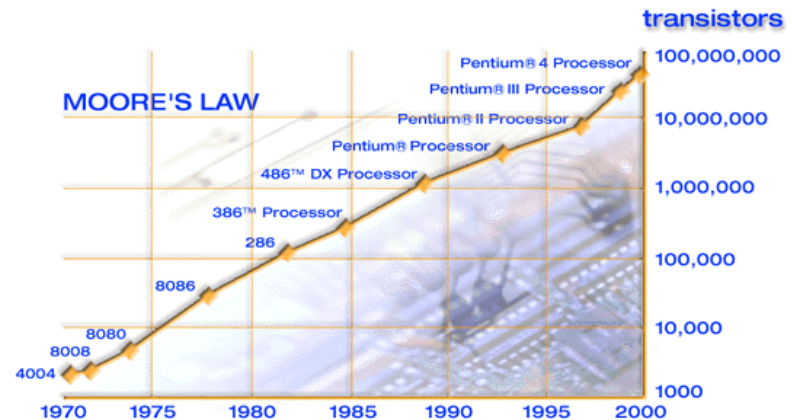
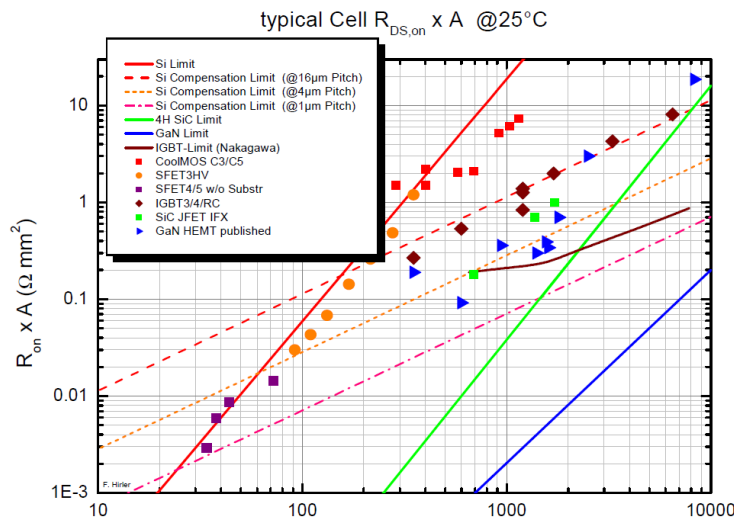
- Circuit Simulation
- Thermal Simulation
- EM Simulation



Summary

Summary (1)

- WBG Semiconductor Technology
- Microelectronics (Moore's Law)
- Adv. Design / Adv. Packaging (Manufacturing) / Adv. Measurement

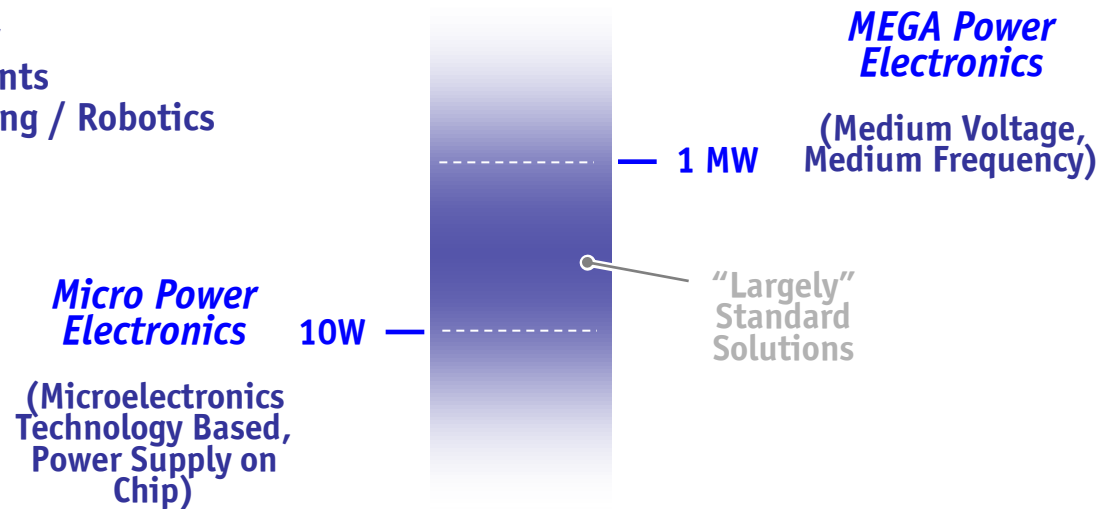


→ Enabling an up to Factor of 10 Performance Improvement

Summary (2)

■ Considerable Future Extension of Power Electronics Application Area

- * Smart Homes / DC Distribution
- * Zero Energy Buildings
- * Wireless Power Transfer
- * Personal Digital Assistants
- * Automated Manufacturing / Robotics
- * EV Charging
- * etc.



- Bridge to Power Systems
- Establish (Closer) University / Industry (Technology) Partnerships
- Establish Cost Models, Consider Reliability as Performance

Thank you!

