Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Power Density vs. Efficiency of Power Electronics

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Outline

- How It All Began
- Recognizing Power Density Barriers
- Multi-Objective Optimization
- Application Examples
- Generalization
- Conclusions

How It All Began…

1. ECPE Demonstrator Program

→ **Max. Power Density**

Demonstrator Program

Development of Ultra Compact Three-Phase Power Supplies

for

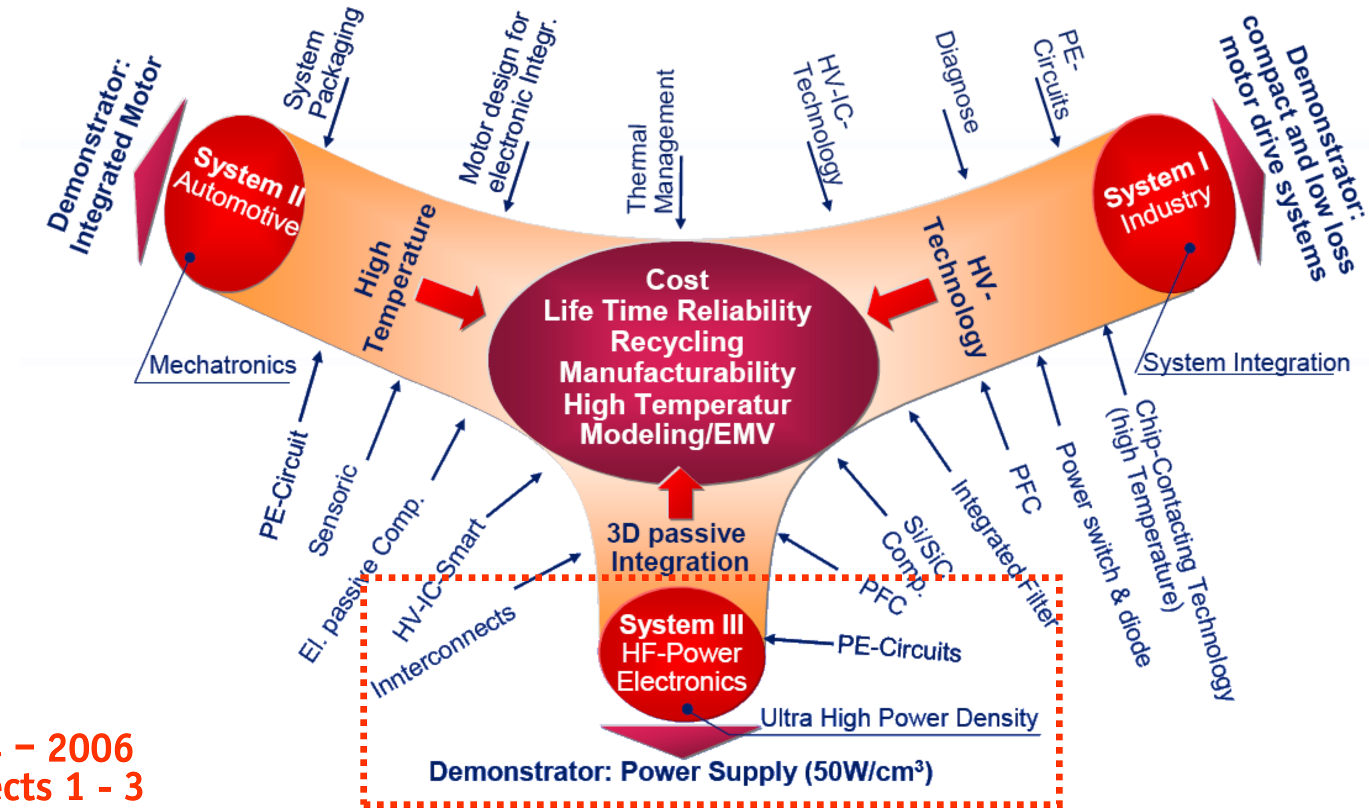
ECPE

by

ETH Zurich
Power Electronic Systems Laboratory
ETH Zentrum, ETL H22
Physikstrasse 3
CH-8044 Zurich

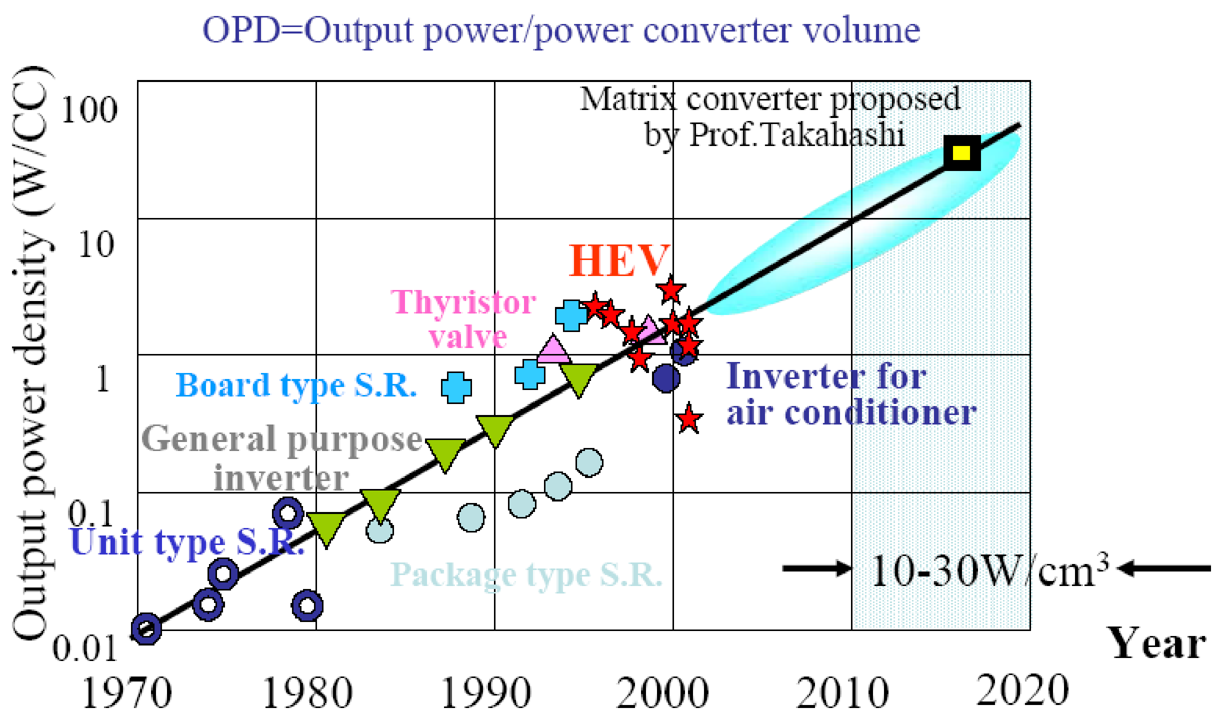
Note: 2004 !

Demonstrator Program



2004 – 2006
Projects 1 - 3

Roadmap of the PERC (Power Electronics Research Center), Japan, coordinated by the National Institute of Advanced Science and Technology



Demonstrator Program
3~ AC/DC Power Supplies

ECPE

Projects 1 - 3

50kW/l !

IPEM
Gate Drive Integration
Current Sensor Integration
Integrated Passives
Planar Interconnections
Novel Semicond. Techn.
Advanced Cooling Concepts

25 GHz.W

20kW/l

System Aspects
Thermal Integration
EMI Filter Integration

10kW/l

System Aspects
Multi-Chip Power Module
Discrete Passive Components

Schedule 09/2004 03/2005 12/2005 12/2006

Basic Project Objective

Development of Ultra Compact Three-Phase AC/DC Utility Interfaces

Application Areas

- Variable Speed AC Drives
- IT Systems
- Process Technology

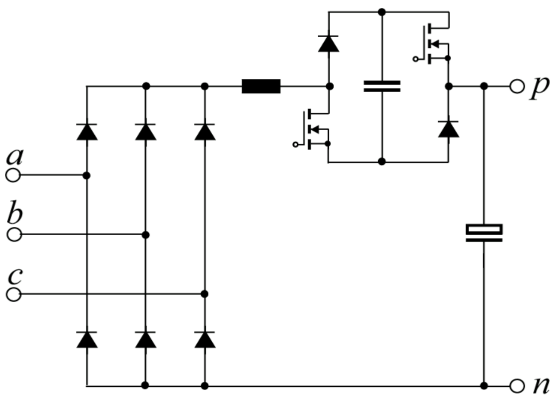
Focus

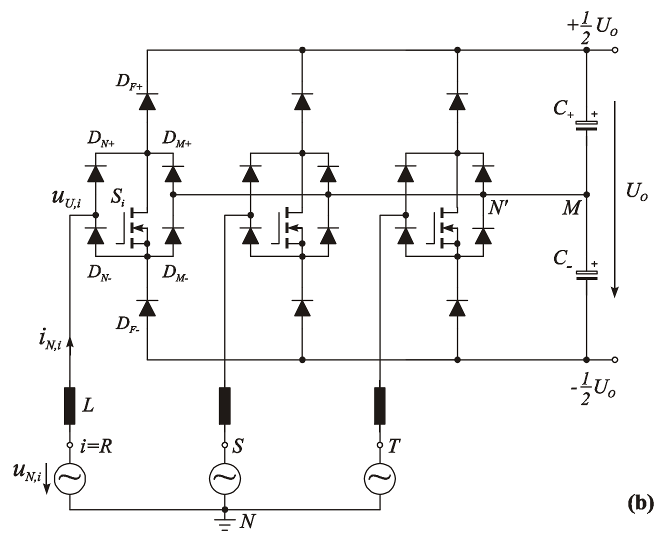
- Application of Advanced Power Semiconductor Technology (SiC)
- Integration, and Advanced Cooling Techniques
- 50kW/l
- Efficiency, Power Density/Size
- Consideration of Reliability, EMI Standards and Costs Reduction

Project 1
Power Supply with 10kW/l Power Density

Tasks / Efforts

- Evaluation of Circuit Topologies
- Electronic Inductor Topology
- Unity Power Factor Three-Phase PMW Rectifier



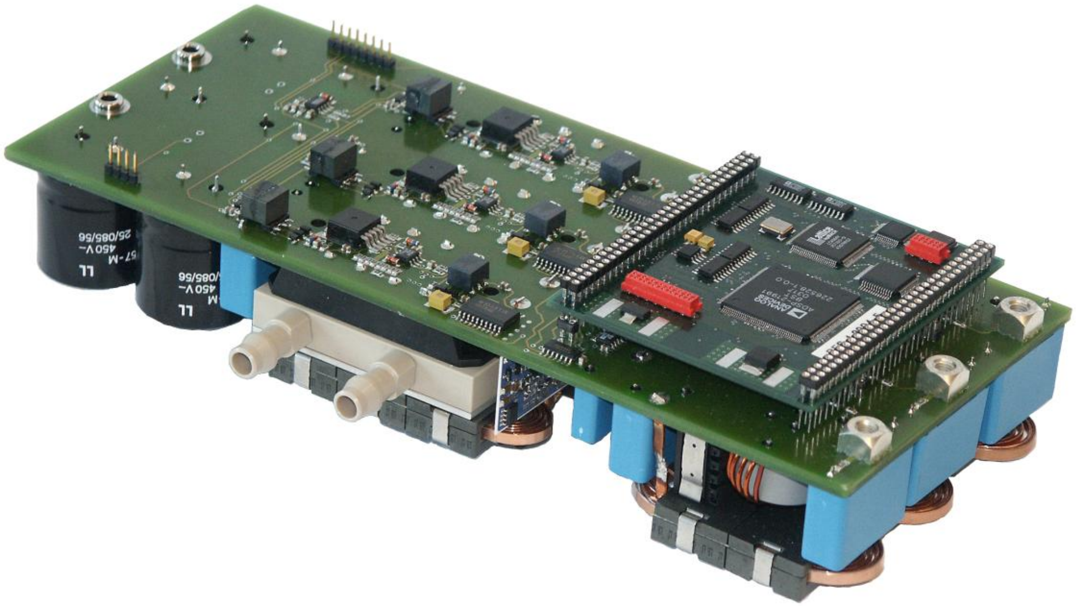


3-Φ Unity Power Factor PMW Rectifier

★ 10 kW/dm³

P_O = 10 kW
U_N = 3-Φ 480V_{AC}
U_{DC} = 800 V_{DC}

f_S = 500 kHz



New Technologies

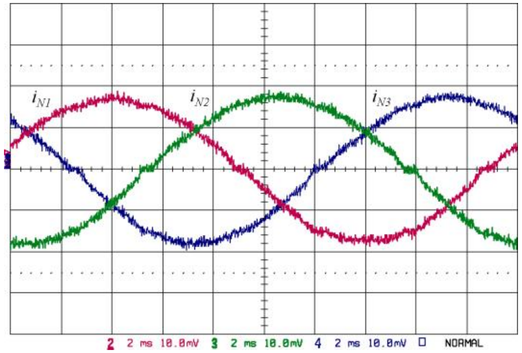
COOLMOS / SiC-Diodes
Micro-Channel Heat Sink
High-Speed DSP-Control
Flat Magnetics
HBW & CMR Current Sensing

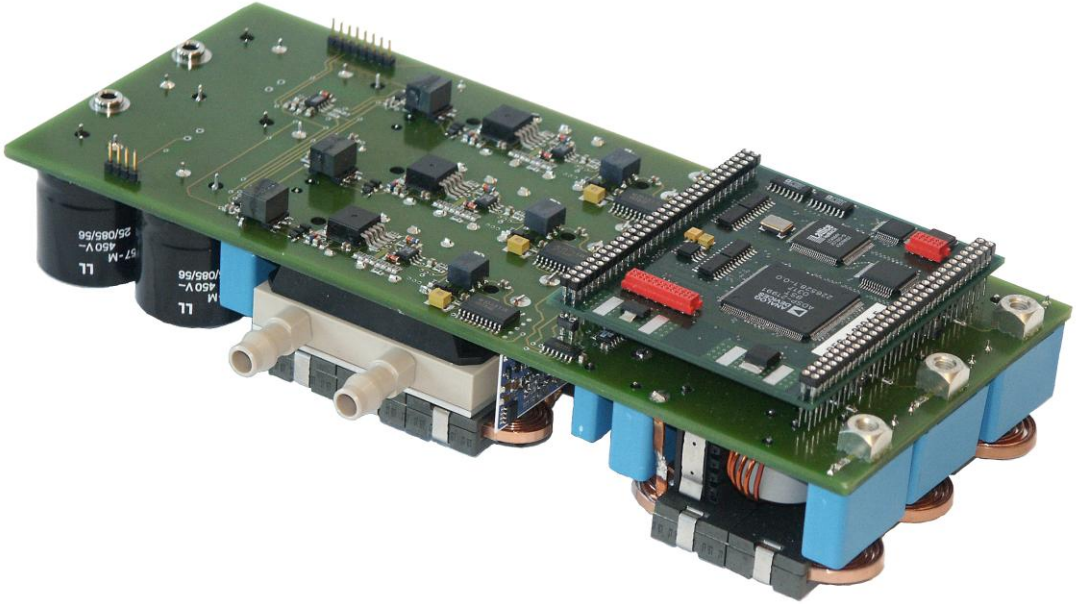
3-Φ Unity Power Factor PMW Rectifier

★ 10 kW/dm³

P_0 = 10 kW
U_N = 3-Φ 480V_{AC}
U_{DC} = 800 V_{DC}

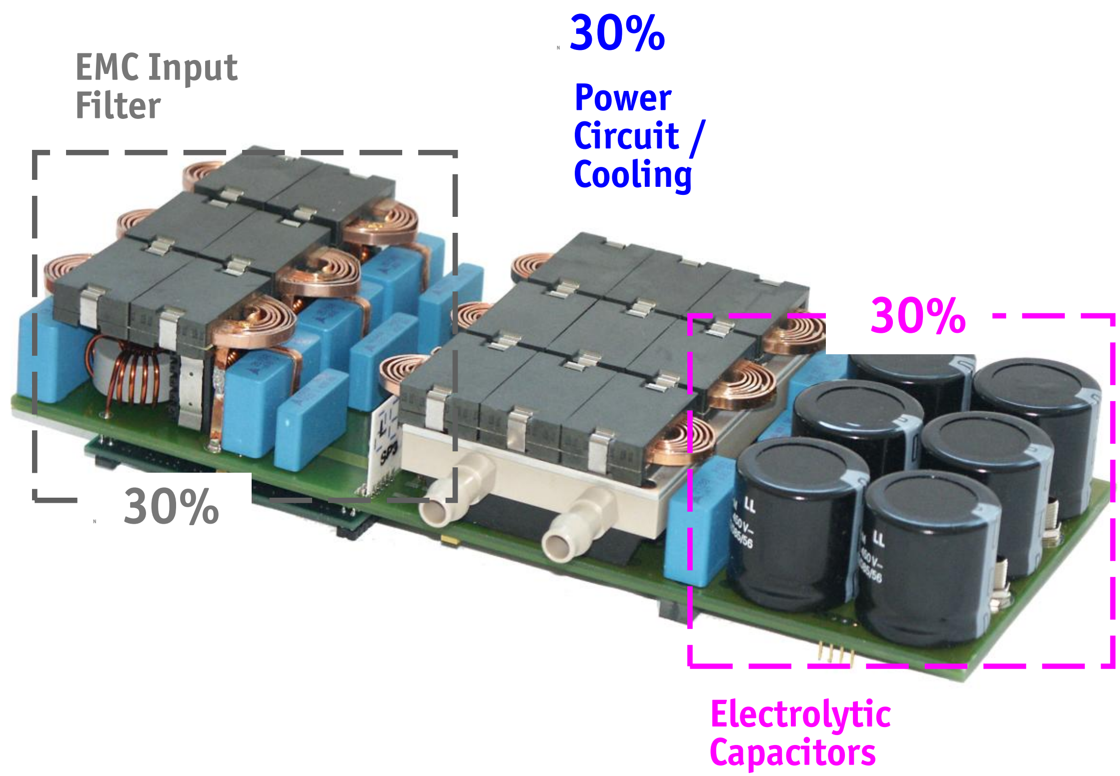
f_S = 500 kHz





Partitioning of the Converter Volume

★ 10 kW/dm³



Main Share of Passive Components

THE INSTITUTE OF ELECTRICAL ENGINEERS OF JAPAN

PCC-Nagoya 2007

April 2-5, 2007

Nagoya Congress Center, Nagoya, Japan

The Fourth Power Conversion Conference

"Red Brick Walls" in Power Electronics

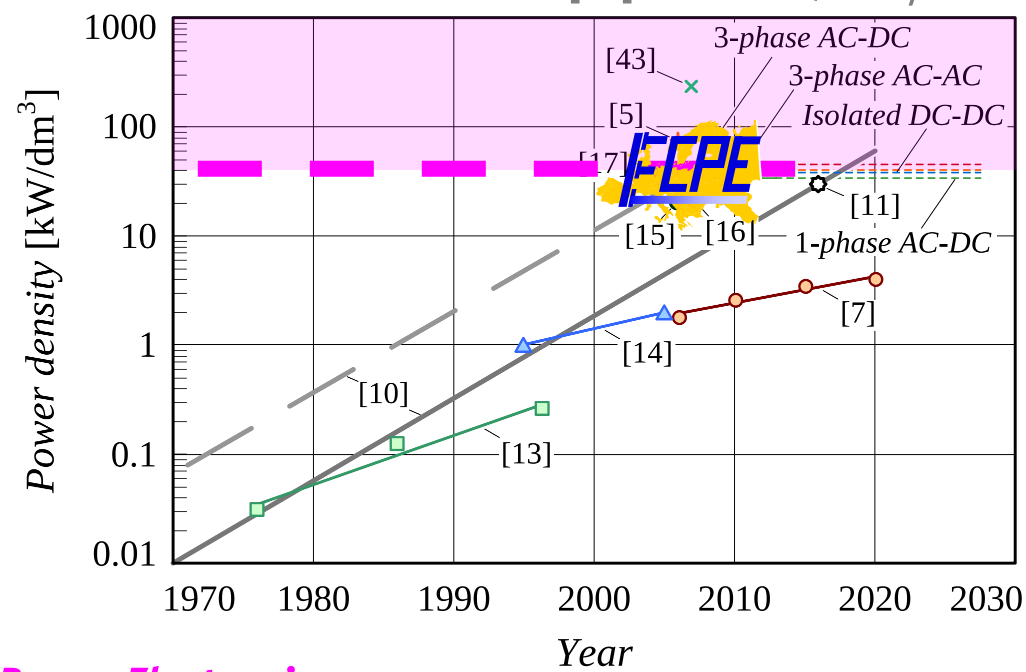
J.W. Kolar, U. Drofenik, J. Biela, M.L. Heldwein, H. Ertl, T. Friedli and S.D. Round

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

Power Density Roadmap

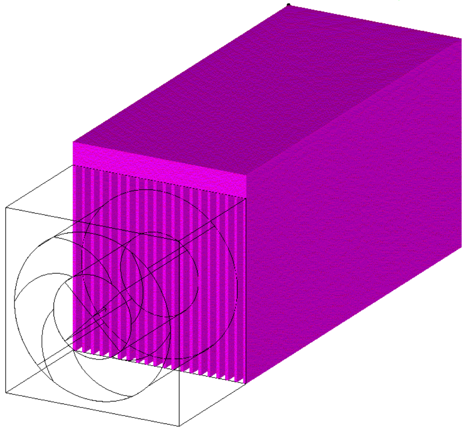
- **Requires Separate Consideration of Basic Converter Types**
  - ** AC/DC*
  - ** DC/DC*
  - ** DC/AC*
  - ** AC/AC*
- **Requires Definition of Cooling Concept**
  - ** Natural Convection*
  - ** Forced Air Cooling*
  - ** Water Cooling*
- **Consider Systems *NOT* Modules**

[10] Dr. Ohashi, 2002/2006



▶ *" Red Brick Walls " in Power Electronics*

Forced Convection Cooling
Power Density Limit



$$P_O = \eta P_i$$

$$\rho_{lim} = \frac{P_O}{Vol_{CS}} = \frac{\eta}{1-\eta} \Delta T_{s-a} CSPI \left[\frac{\mathrm{W}}{\mathrm{dm}^3}\right]$$

$$P_{Loss} = (1-\eta) P_i$$

$$Vol_{CS} = \frac{G_{th}}{CSPI} = \frac{P_{Loss}}{\Delta T_{s-a}} \frac{1}{CSPI}$$

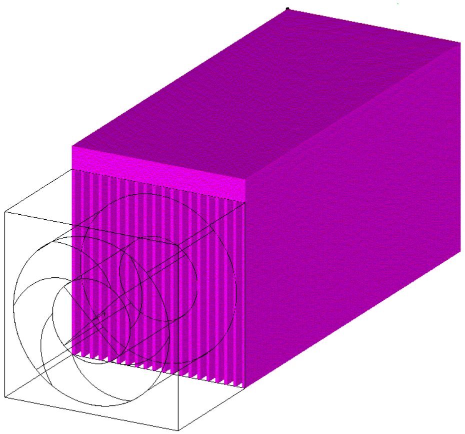
@ η = 97%

- T_s = 90°C
- T_s = 135°C

T_a = 45°C, CSPI = 20 WK^{-1}dm^{-3}

ρ_{lim} = 29 kW/dm^3
ρ_{lim} = 58 kW/dm^3

Forced Convection Cooling
Power Density Limit



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$$P_{Loss} = (1-\eta) P_i$$

@ η = 97%

Coupling of Efficiency & Power Density

- ▶ T_s = 90°C
- ▶ T_s = 135°C

T_a = 45°C, CSPI = 20 WK^{-1}dm^{-3}

ρ_{lim} = 29 kW/dm^3
ρ_{lim} = 58 kW/dm^3

2. ECPE Roadmap Initiative

→ Power Density
→ Efficiency
→ Costs
→ etc.

Registration (Fax Reply)

To: ECPE e.V.
Att.: Ingrid Bollens

Fax: +49 (0)911 / 81 02 88 – 28

Register before **27 August 2007**

Participation fee:

- ☐ **€ 120,-*** for members of the ECPE Network
- ☐ free for invited guests and speakers

The fee includes dinner, lunch, coffee/soft drinks.

With the confirmation of registration you will receive the invoice. (* plus 25 % VAT)
In case of cancellation after 27 August 2007 or non-attendance 50 % of the participation fee are payable.

Sender:

____
title, given name, name

____
company, department

____
full address

____
phone, fax

____
e-mail

____
date, signature

Organisational Information

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90443 Nürnberg, Germany
www.ecpe.org

Contact: Ingrid Bollens, ECPE e.V.
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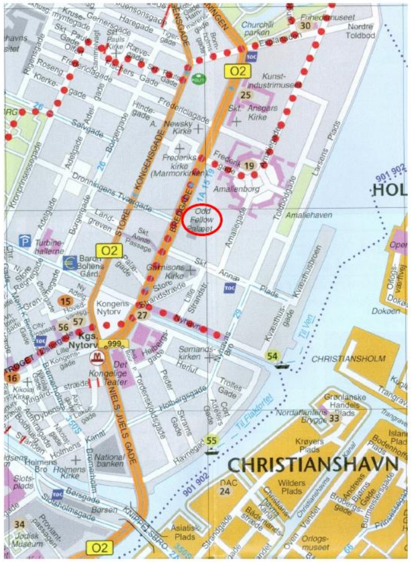
ingrid.bollens@ecpe.org

Venue: Odd Fellow Palais
28, Bredgade
1260 Copenhagen K, Denmark



Further information (hotel list and maps) will be provided in due time.

ECPE European Center for Power Electronics e.V.

ECPE Workshop

Power Electronics Research & Technology Roadmaps

8 September 2007
"Odd Fellow Palais"
Copenhagen, Denmark

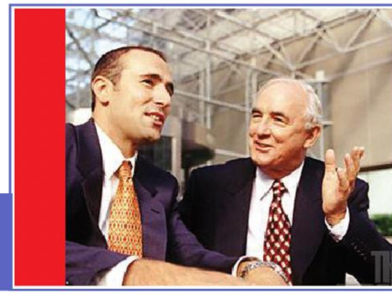
in cooperation with

CPES
Center for Power Electronics Systems (USA)

AIST PERC
Power Electronics Research Center (Japan)

Note: 2007 !

ECPE
Roadmap Methodology



Hansruedi Zeller

For use within the ECPE Roadmap Initiative only!

6 Strategic goals

- Derive Strategic Goals from the Sect. 4, Limiting Challenges and Technology Gaps
- Goals have to be formulated **as a status and not as an activity**!
- Whenever possible, goals should be quantitative
- Present required evolution from today's status to final goal (e.g. today 50%, 2010 80%, 2015 90%, 2020 100% achieved)
- Focus on goals which require breakthroughs, continuous improvement happens automatically.
- At least one goal should refer to the system level (or next higher level in system integration)
- Restrict to approx. 5 goals

Example: Power Supplies (AC/DC, P < 0.5 kW)

1. Ultra high density packaging (hybrid integration, SIP) with 28 W/cinch
2. Fully digital control
3. Fully embedded power + PFC + PWM
4. Efficiency > 90%
5. Cost 50% of 2005 cost.

Power density: 2005 → 6 W/cinch, 2010 → 11 W/cinch, 2015 → 18 W/cinch, 2020 → 28 W/cinch
Control: 2005 → analog, 2010 → secondary control semi analog/digital, 2020 → fully digital
Etc. for the other goals.

List of required breakthroughs: To be made

7 Strategy

- Define a **strategy for each strategic goal**
- Whenever necessary discuss different strategy scenarios
- Decide on best scenario based on SWOT analysis (do a specific SWOT for particular goal if necessary)
- Define metrics to measure success of strategy

3. Efficiency (!) → "THE" New Target

EUROPEAN POWER ELECTRONICS AND DRIVES

ECPE

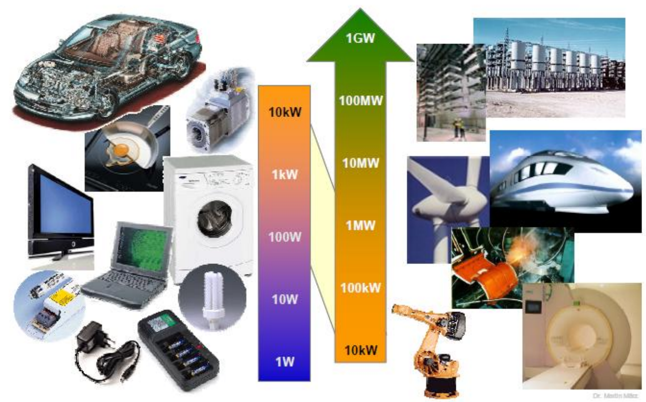
▶ Requirements

(1) Efficiency
(2) Power Density
(3) Costs

Position Paper

on

Energy Efficiency – The Role of Power Electronics



February 2007

ECPE European Center for Power Electronics

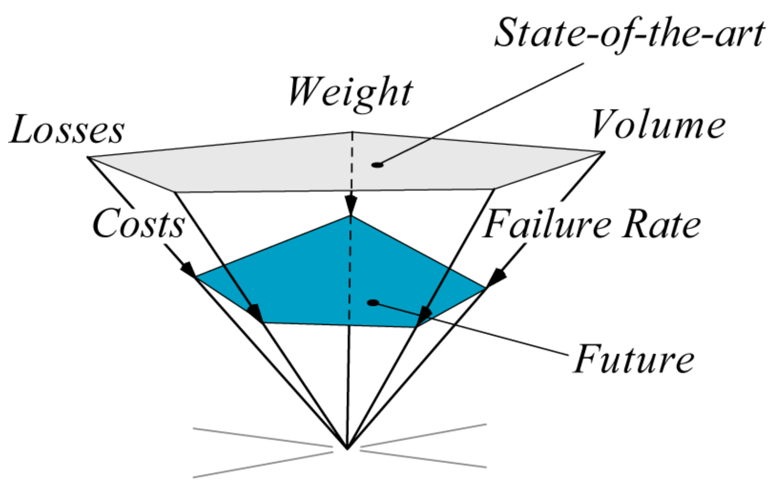
EPE European Power Electronics and Drives

4. Time to Come Up with a Theoretical Foundation

→ Multi-Objective Optimization

Power Electronics
Performance Trends

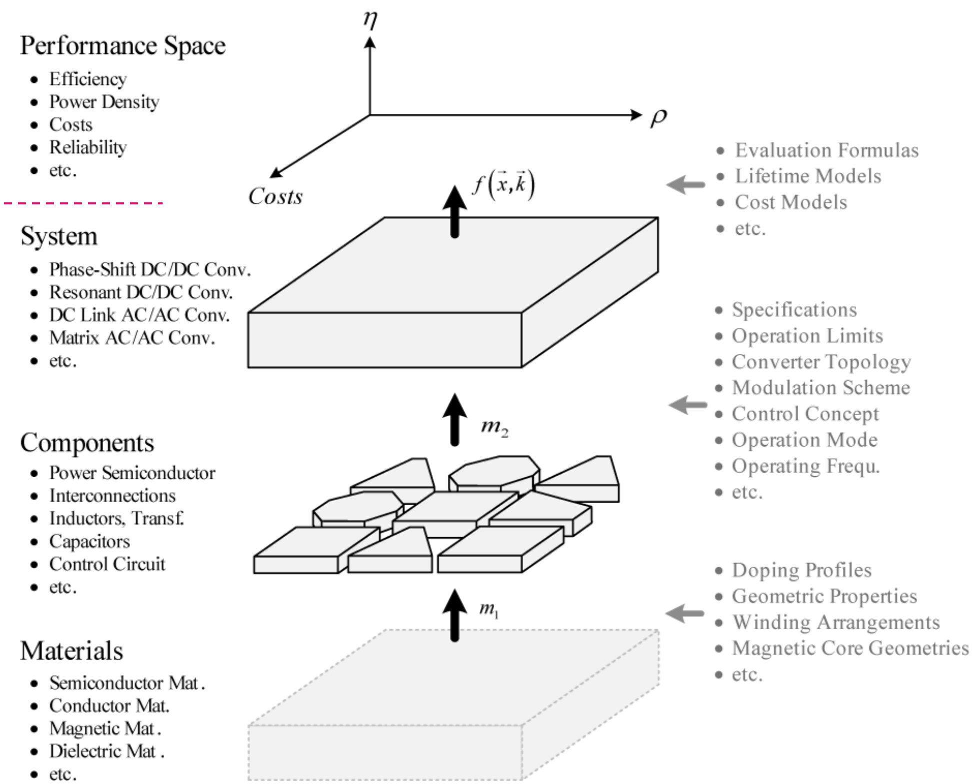
- **Performance Indices**
  - Power Density [kW/dm^3]
  - Power per Unit Weight [kW/kg]
  - Relative Costs [kW/$]
  - Relative Losses [%]
  - Failure Rate [h^{-1}]



Abstraction of Power Converter Design

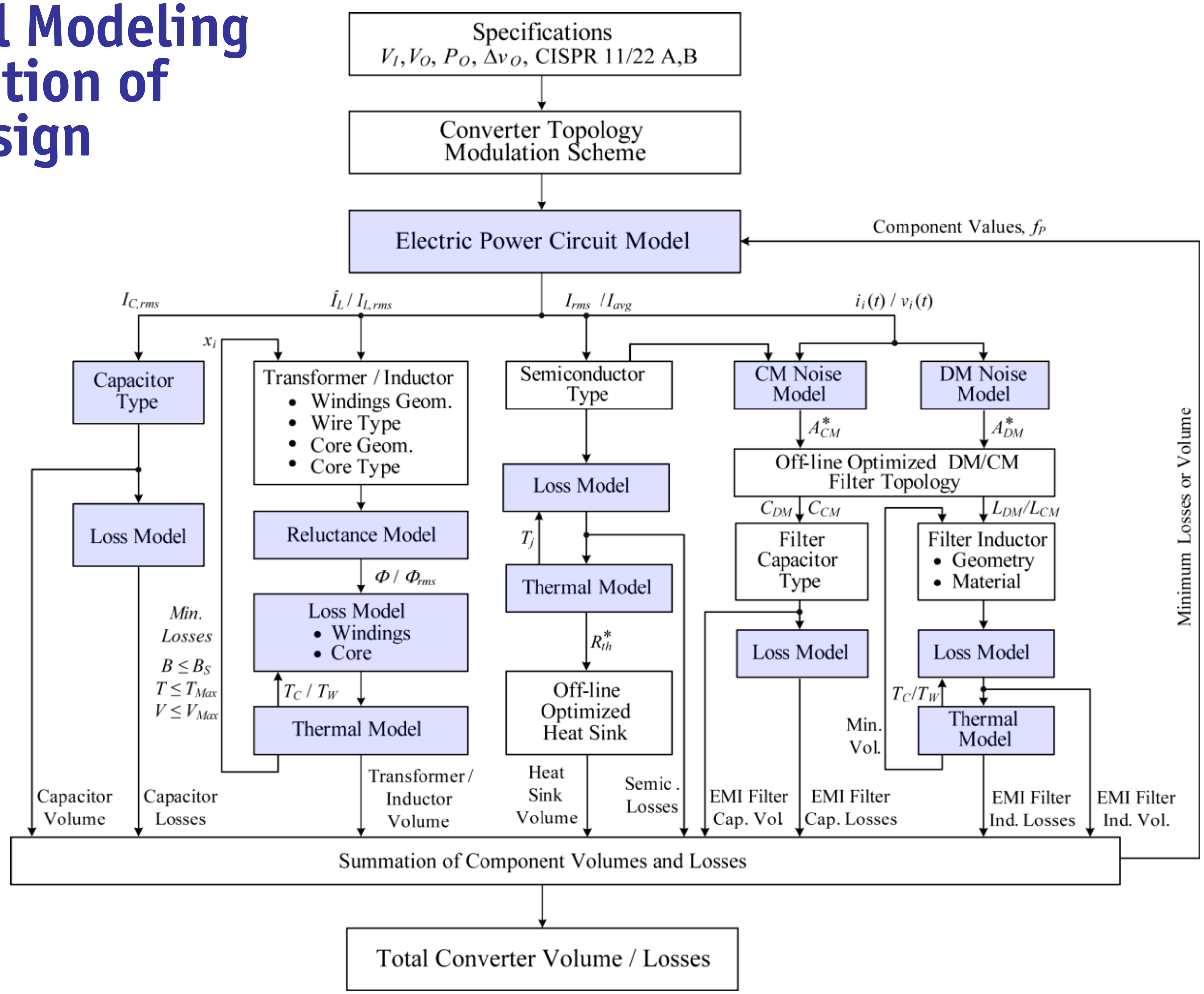
Performance Space

Design Space



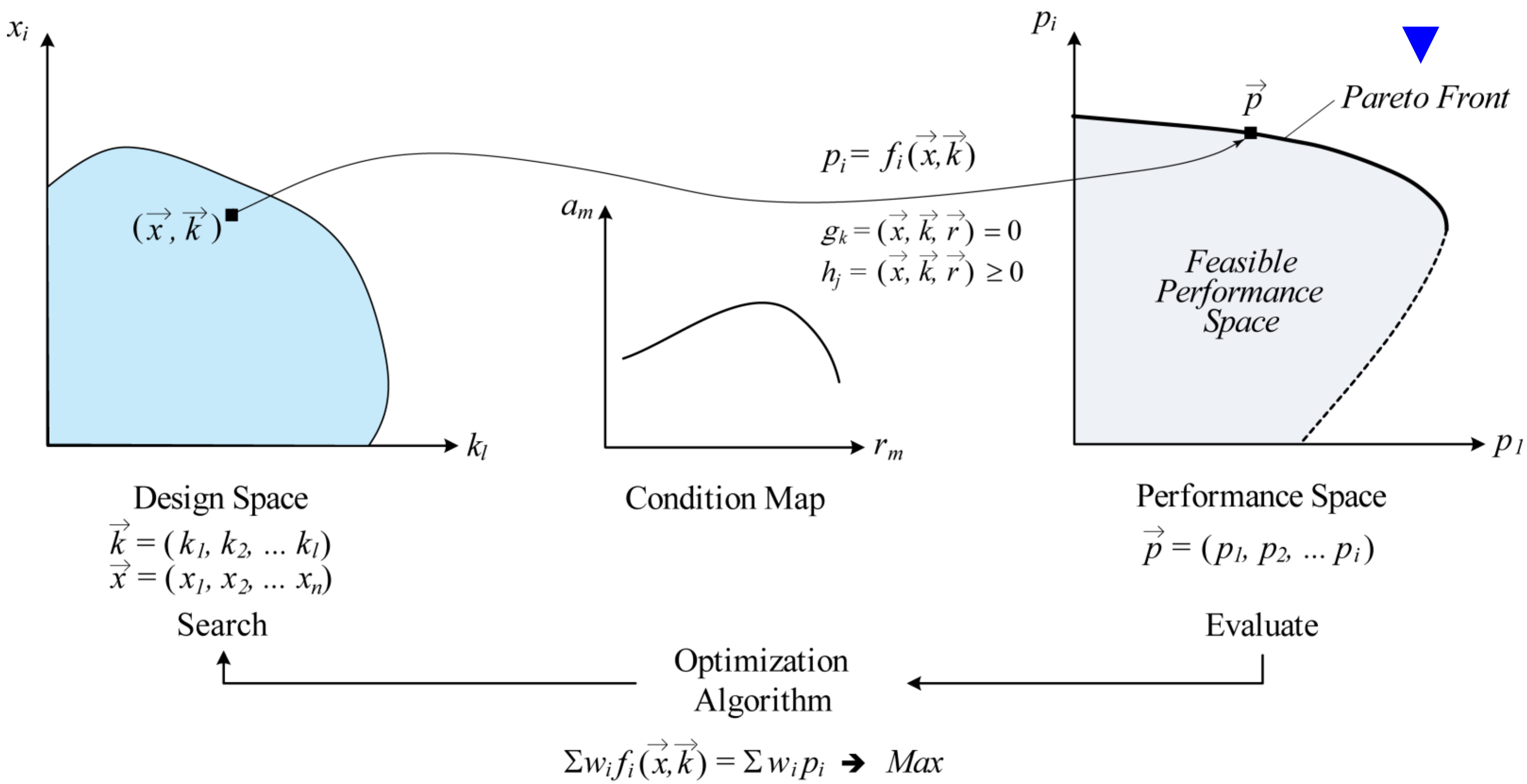
- **Mapping of *Design Space* into System *Performance Space***

Mathematical Modeling and Optimization of Converter Design



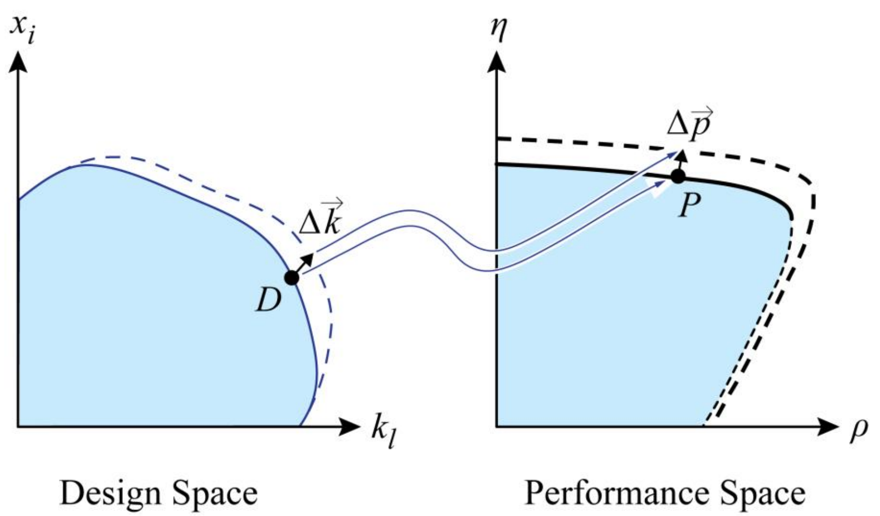
Multi-Objective Converter Design Optimization

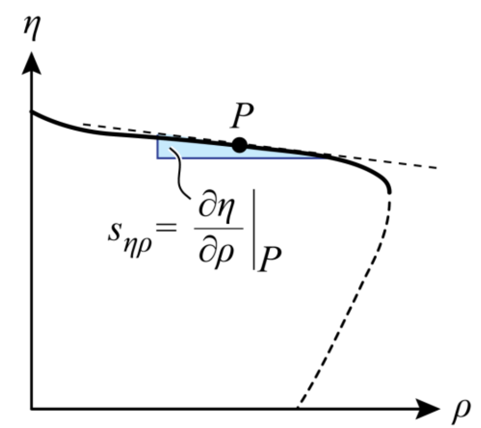
- ***Pareto Front*** **- Limit of Feasible Performance Space**



Technology Sensitivity Analysis Based on η-ρ-Pareto Front

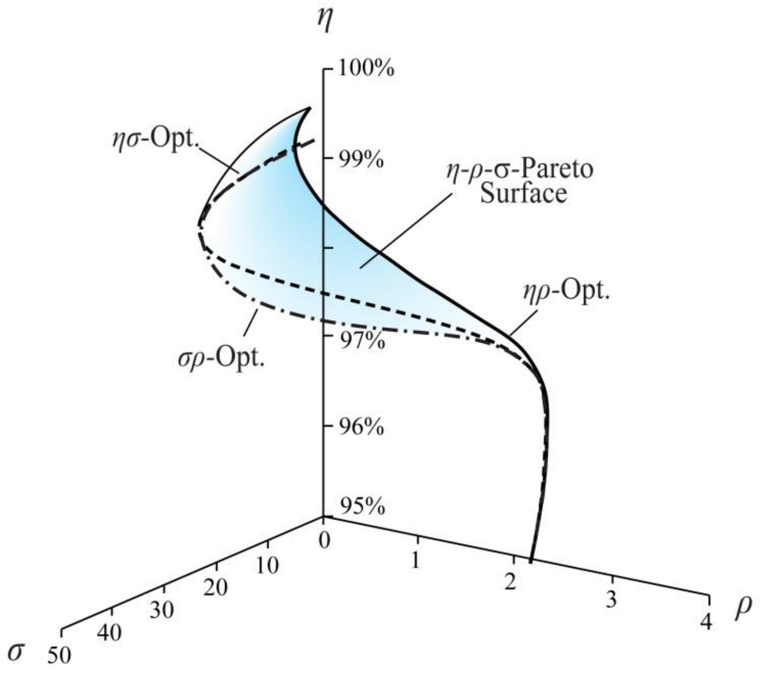
- ▶ Sensitivity to Technology Advancements
- ▶ Trade-off Analysis

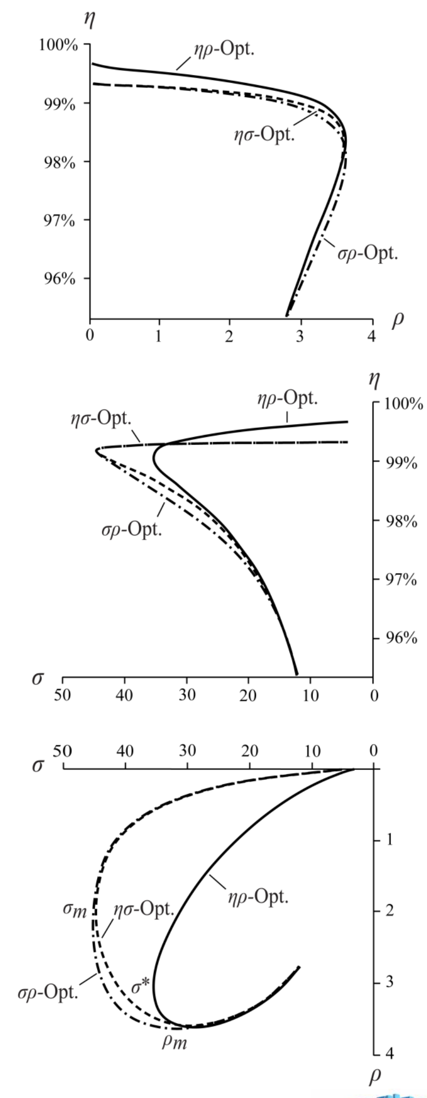




Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

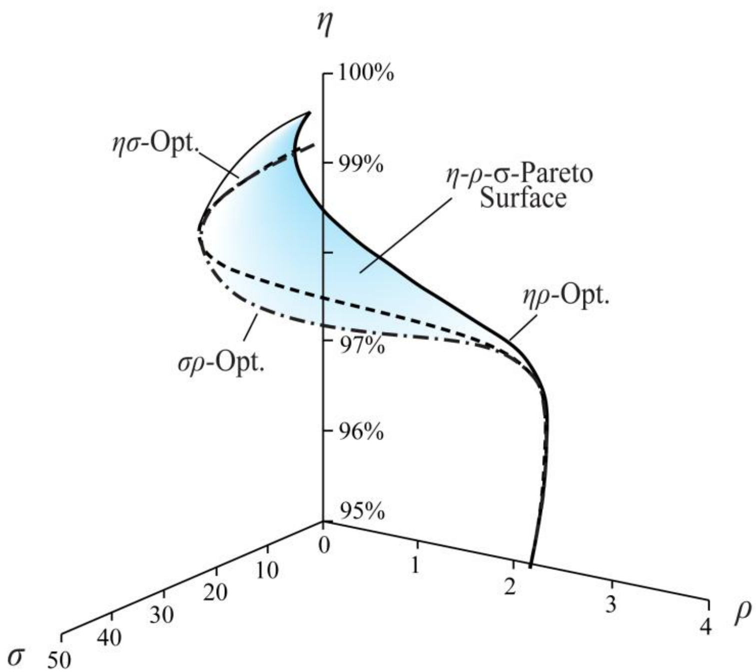
- ► σ: kW/$

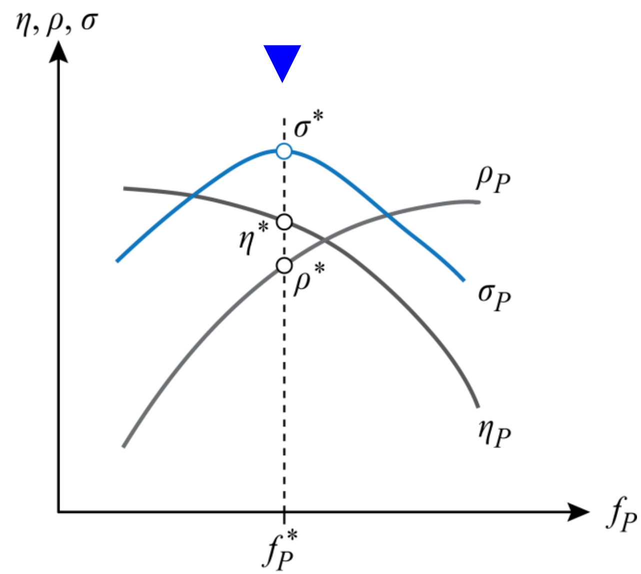




Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

► *´ Technology Node´*





Technology Node: $(\sigma^*, \eta^*, \rho^*, f_P^*)$

Demonstrator Systems

→ 3-ph. VIENNA Rectifier
→ 1-ph. PFC Rectifiers
→ Inductive Charging
→ Power Supply on Chip
→ Airborne Wind Turbine

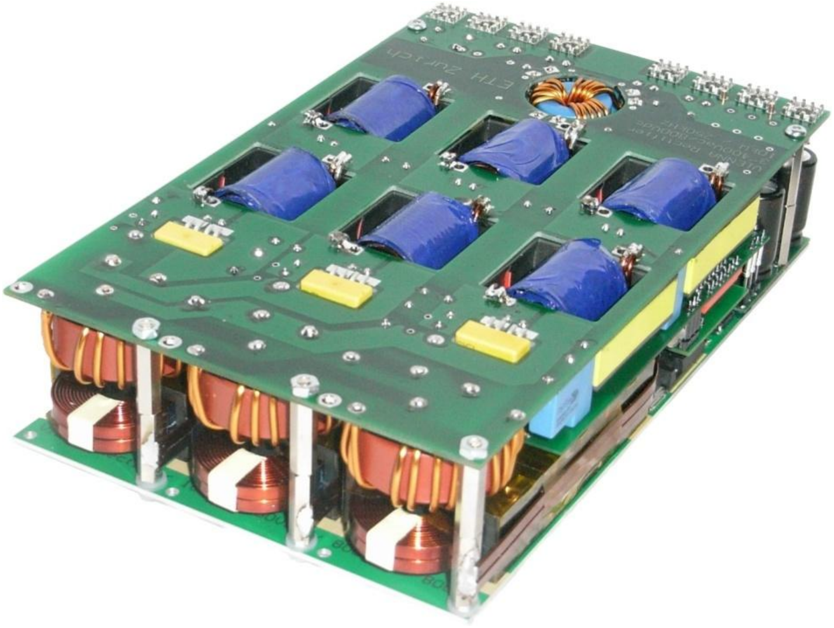
▶ Demonstrator – VR250 (1)

- **Specifications**

  U_{LL} = 3 x 400 V
  f_N = 50 Hz ... 60 Hz or 360 Hz ... 800 Hz
  P_o = 10 kW
  U_o = 2 x 400 V
  f_s = 250 kHz

- **Characteristics**

  η = 96.8 %
  THD_i = 1.6 % @ 800 Hz
  10 kW/dm3
  3.3 kg (≈3 kW/kg)



Dimensions: 195 x 120 x 42.7 mm^3

▶ Demonstrator – VR250 (2)

- **Specifications**

  U_{LL} = 3 x 400 V
  f_N = 50 Hz ... 60 Hz or 360 Hz ... 800 Hz
  P_o = 10 kW
  U_o = 2 x 400 V
  f_s = 250 kHz

- **Characteristics**

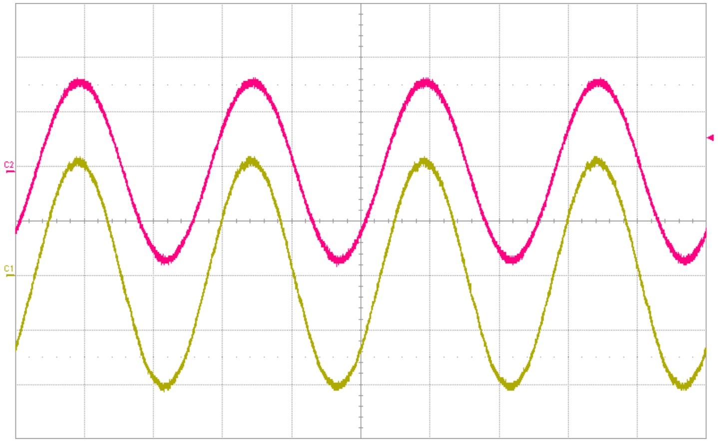
  η = 96.8 %
  THD_i = 1.6 % @ 800 Hz
  10 kW/dm3
  3.3 kg (≈3 kW/kg)

Dimensions: 195 x 120 x 42.7 mm^3

▶ Mains Behavior @ f_N = 400Hz / 800Hz

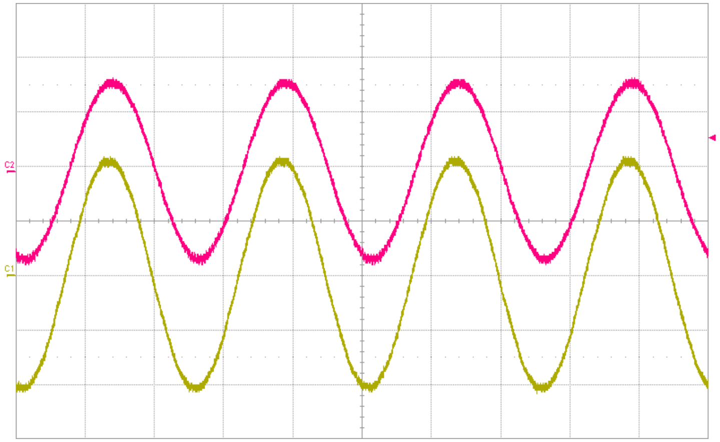
P_0 = 10kW
U_N = 230V
f_N = 400Hz
U_0 = 800V
THD_i = 1.4%

10A/Div
200V/Div
1ms/Div



P_0 = 10kW
U_N = 230V
f_N = 800Hz
U_0 = 800V
THD_i = 1.6%

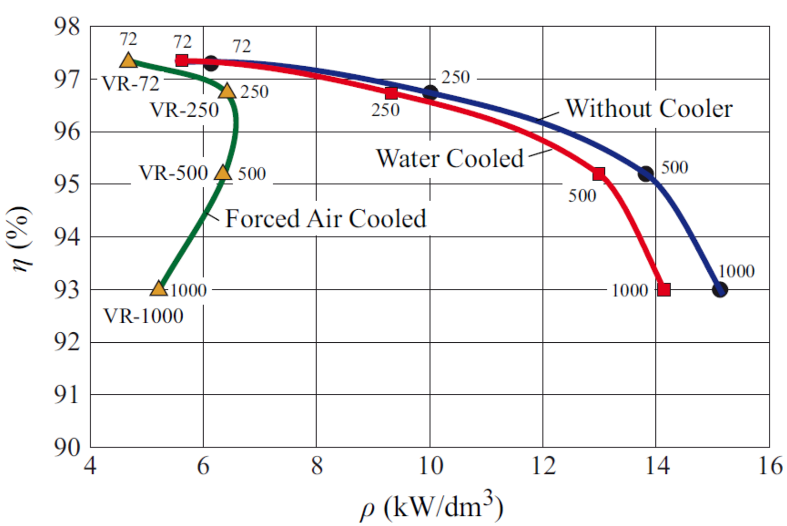
10A/Div
200V/Div
0.5ms/Div



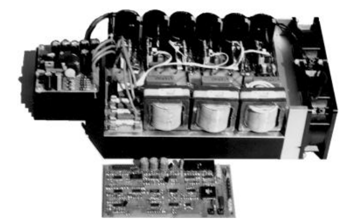
▶ Experimental Analysis

■ Generation 1 – 4 of VIENNA Rectifier Systems

- **Switching Frequency of f_S = 250 kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality THD_i**



f_S = 50 kHz
ρ = 3 kW/dm^3



f_S = 72 kHz
ρ = 4.6 kW/dm^3

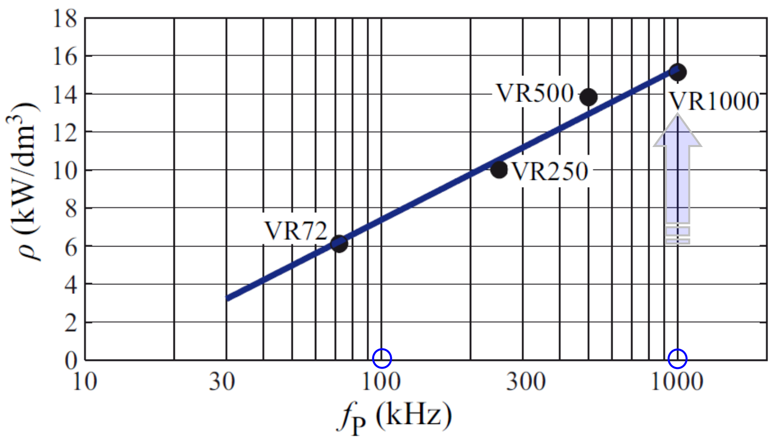
f_s = 250 kHz
ρ = 10 kW/dm^3
(164 W/in^3)
Weight = 3.4 kg

f_S = 1 MHz
ρ = 14.1 kW/dm^3
Weight = 1.1 kg

▶ Experimental Analysis

■ Generation 1 – 4 of VIENNA Rectifier Systems

- Switching Frequency of f_S = 250 kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality THD_i



f_S = 50 kHz
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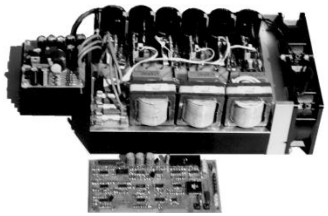

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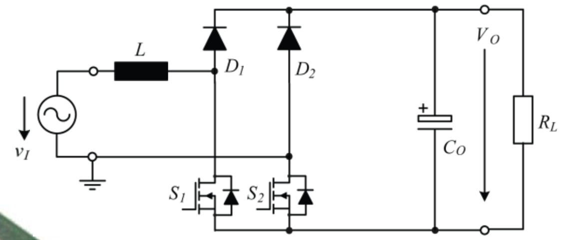
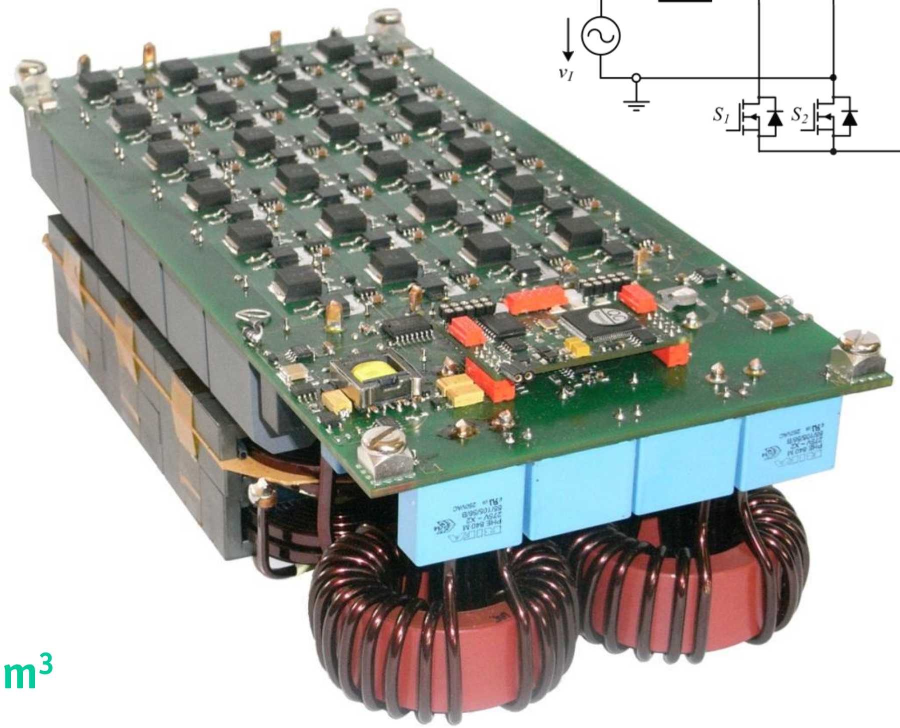
ρ = 10 kW/dm^3
(164 W/in^3)
Weight = 3.4 kg

f_S = 1 MHz
ρ = 14.1 kW/dm^3
Weight = 1.1 kg

1-Φ Boost-Type PFC Rectifier

▶ Si CoolMOS, 99mΩ/600V
▶ SiC Diodes, 10A/600V





P_O=3.2kW
U_N=230V±10%
U_O=365V

f_P=33kHz ±3kHz

Two Interleaved
1.6kW Systems

★ 99.2% @ 1.1kW/dm^3

Ultra-Efficient PFC Rectifier Performance Limits

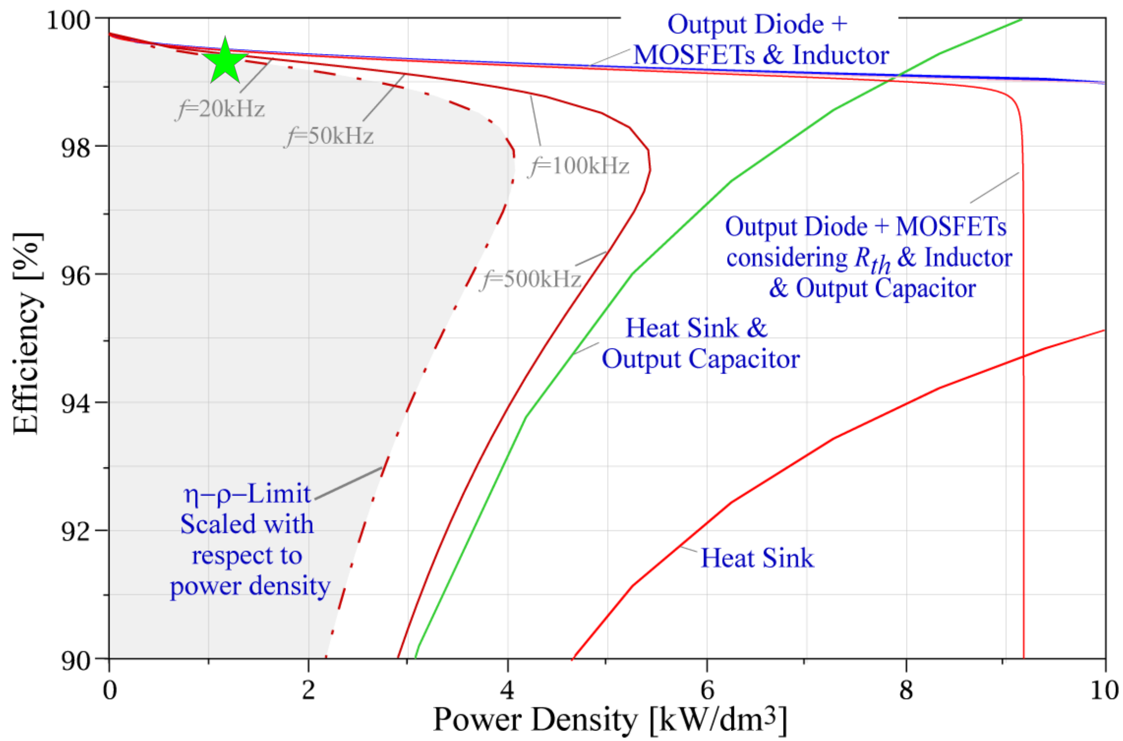
$$(1-\eta) \propto \frac{U_F}{U_O}$$

— Output Diodes
— Power MOSFETs
— Aux. Power

— Inductor
— Output Cap.
— Heatsink

$$\rho_{HS} \propto \frac{\eta}{(1-\eta)}$$

$$(1-\eta) \propto \underbrace{\sqrt{\frac{G^*}{C^*}}}_{FOM_{\eta\rho,1}} \sqrt{\rho_L}$$



Experimental Ultra-Compact
1-Φ PFC Rectifier

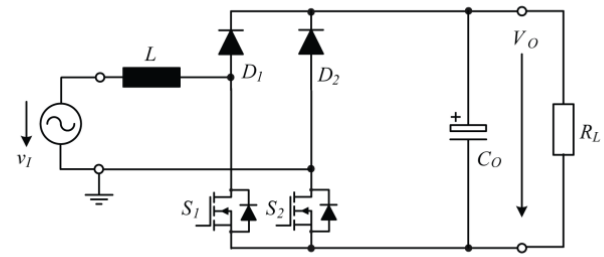
- **Si CoolMOS**
- **SiC Diodes**

P_0=3.2kW
U_N=230V±10%
U_0=400V

f_P=450kHz ±50kHz

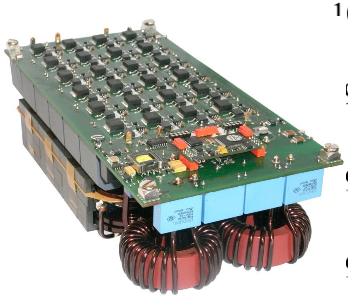
Two Interleaved
1.6kW Systems

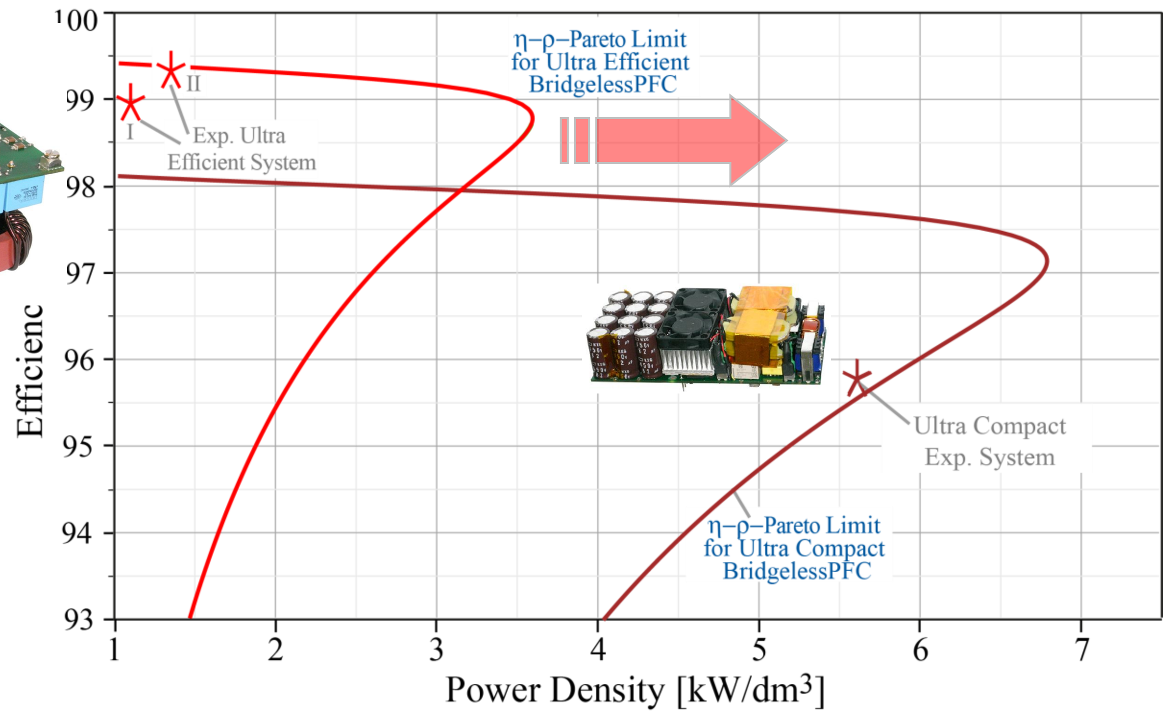
★ **5.5kW/dm³**



Feasible Performance Space

► **Bridgeless PFC Rectifiers @ u_N = 230V**



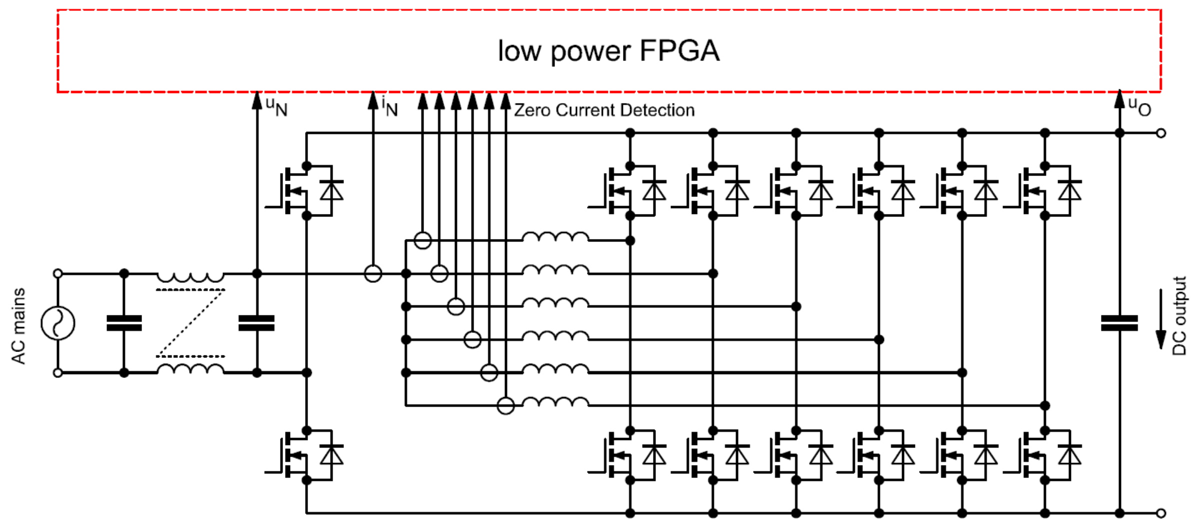


Power Density is Based on Net Volumes ➔ Scaling by 0.6-0.8 Necessary

Bidirectional Ultra-Efficient
1-Φ PFC Mains Interface

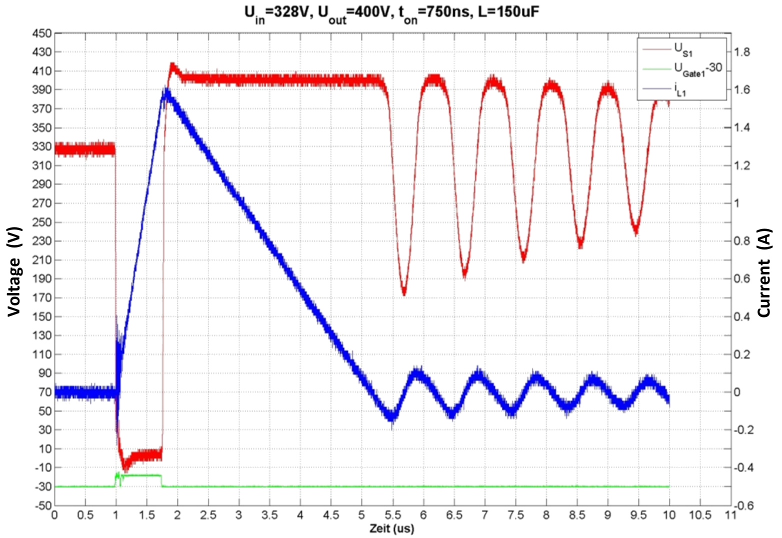
★ **99.36% @ 1.2kW/dm³**

Hardware Testing to be finalized in September 2011

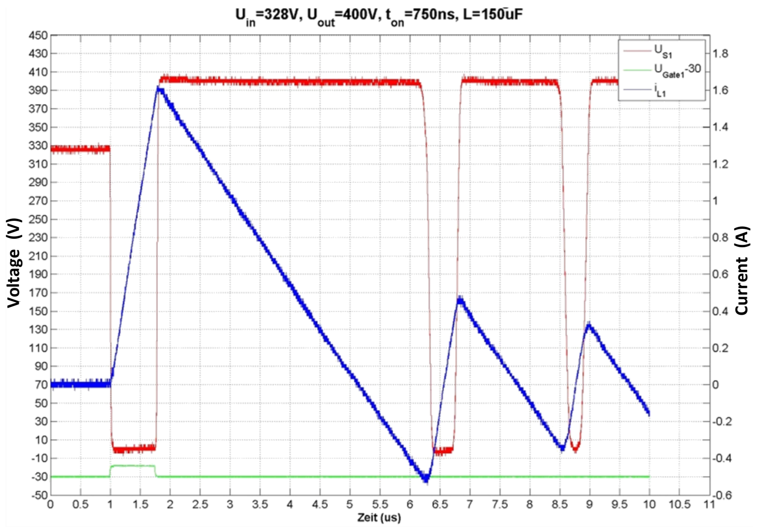


► **Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only**

AC-DC Rectifier - Single Boost Cell - Measurements



No Soft-Switching



Soft-Switching with Extended On-Interval of S_{11}

Bidirectional Ultra-Efficient
1-Φ PFC Mains Interface

★ 99.36% @ 1.2kW/dm³

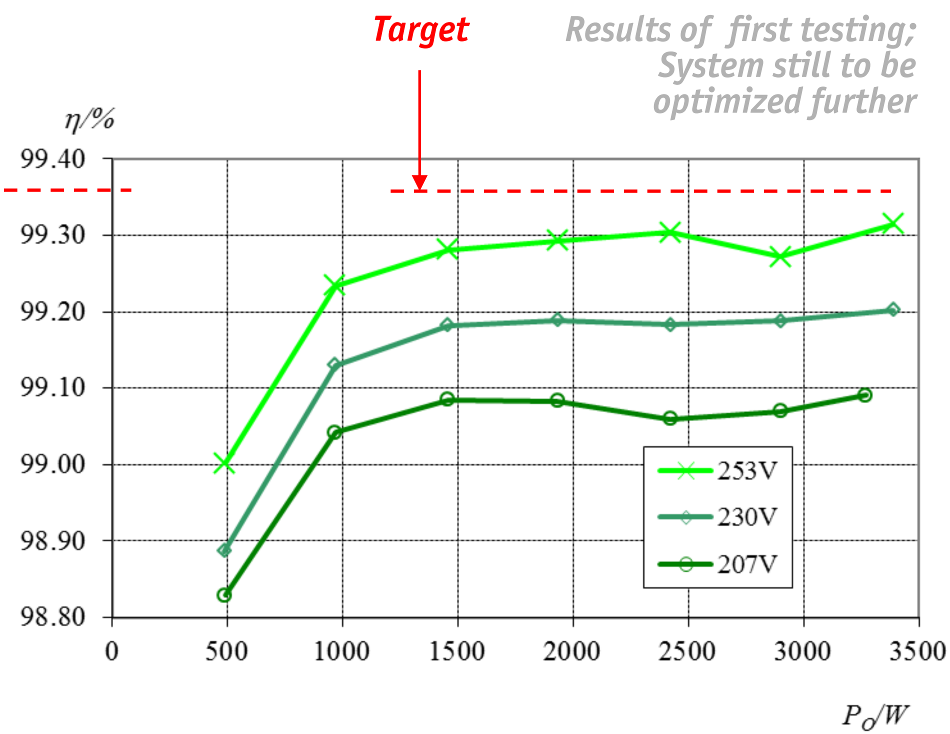
*Hardware Testing
to be finalized in
September 2011*

► Employs <u>NO</u> SiC Power Semiconductors -- Si SJ MOSFETs only

Bidirectional Ultra-Efficient
1-Φ PFC Mains Interface

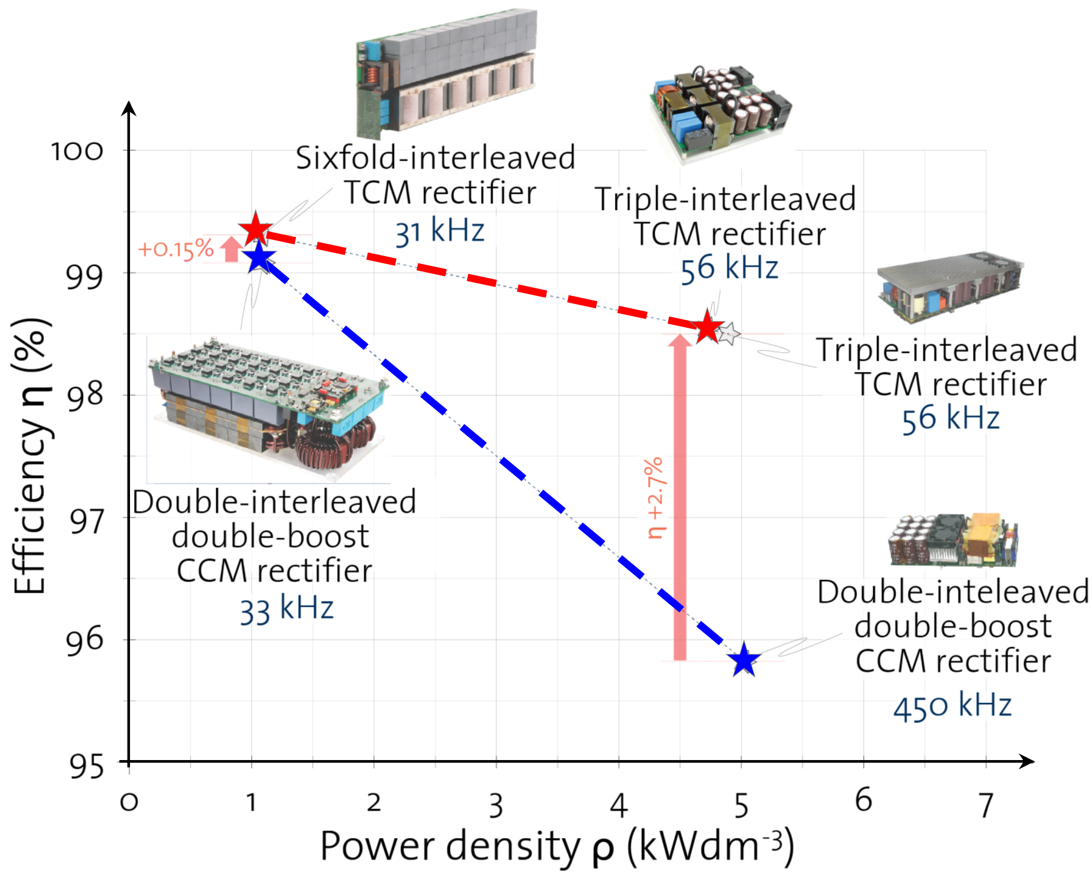
★ **99.36% @ 1.2kW/dm³**

Result of Final Testing



▶ **Employs <u>NO</u> SiC Power Semiconductors -- Si SJ MOSFETs only**

Converter Performance Evaluation Based on η-ρ-Pareto Front



"Out-of-the-Box"
Wind Turbine Concepts

Power Kite & *Ground-Based* EE-Generation
Power Kite & *On-Board* EE-Generation

Revolutionize Wind Power Generation Using Kites / Tethered Airfoils

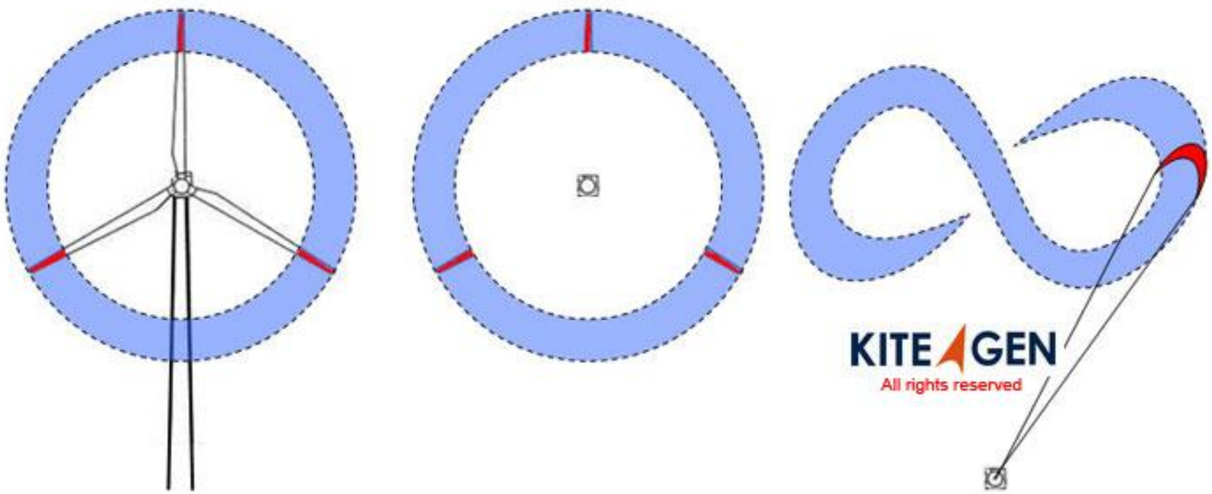
[2] M. Loyd, 1980

- Wing Tips / Highest Speed Regions are the Main Power Generating Parts of a Wind Turbine

Controlled Power Kites for Capturing Wind Power

- ► Replace Blades by Power Kites
- ► Minimum Base Foundation etc. Required
- ► Operative Height Adjustable to Wind Conditions

[2] M. Loyd, 1980



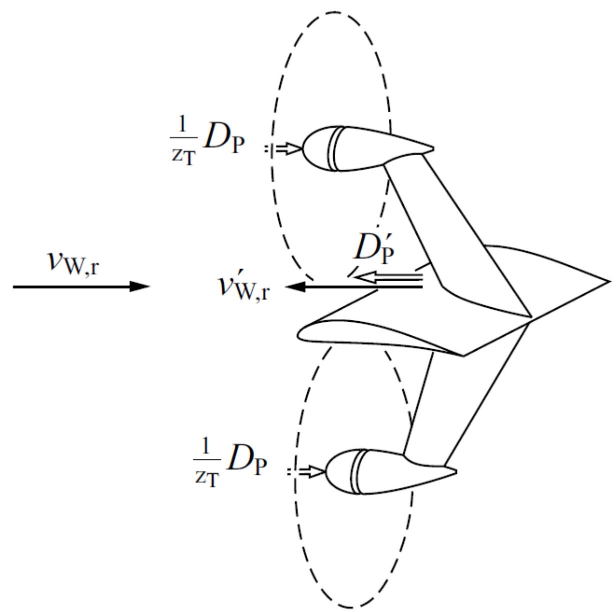
- Wing Tips / Highest Speed Regions are the Main Power Generating Parts of a Wind Turbine

Alternative Concept – Airborne Wind Turbine (AWT)

- ▶ Power Kite Equipped with Turbine / Generator / Power Electronics
- ▶ Power Transmitted to Ground Electrically

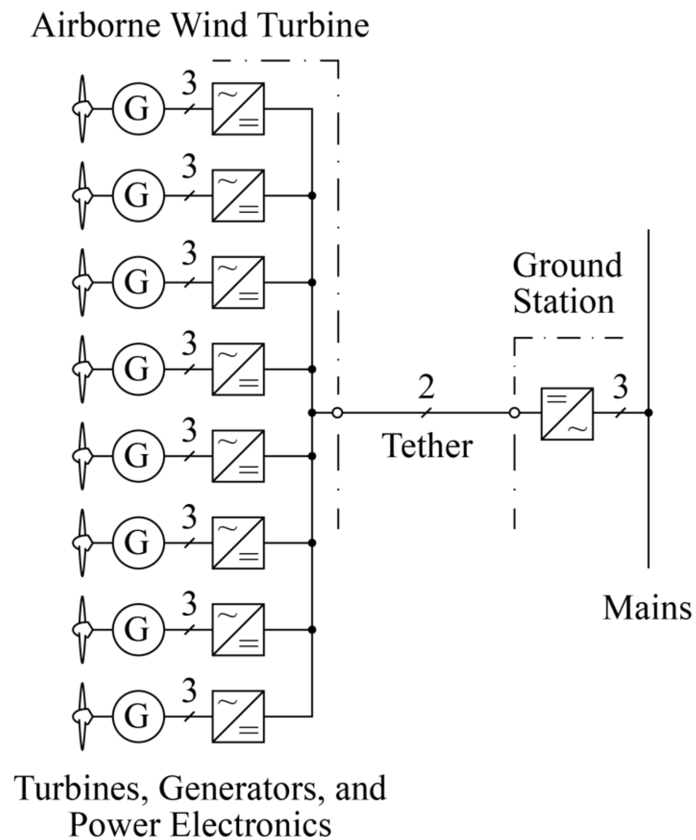
[2] M. Loyd, 1980

Source: JOBY ENERGY



AWT Basic Electrical System Structure

- Rated Power 100kW
- Operating Height 800...1000m
- Ambient Temp. 40°C
- Power Flow Motor & Generator

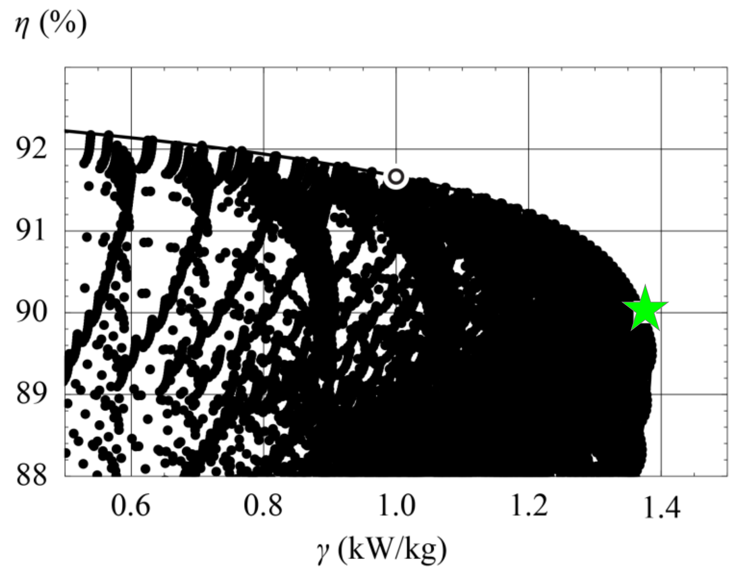


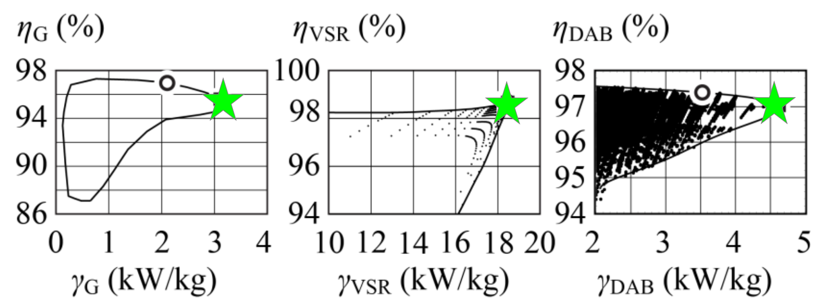
- El. System Target Weight 100kg
- Efficiency (incl. Tether) 90%
- Turbine /Motor 2000/3000rpm

Overall AWT System Performance

EFFICIENCIES AND POWER-TO-WEIGHT RATIOS AT THE 2 DESIGN POINTS MARKED IN FIG. 24(A) (CALCULATED FOR NOMINAL OPERATION).

Total system	Generator, VSR, and DAB converter		
$\gamma = 1.37\,\mathrm{kW/kg}$ $\eta = 90.0\%$	Generator:	$\gamma_{\mathrm{G}} = 3.11\,\mathrm{kW/kg}$,	$\eta_{\mathrm{G}} = 95.4\%$
	VSR:	$\gamma_{\mathrm{VSR}} = 18.3\,\mathrm{kW/kg}$,	$\eta_{\mathrm{VSR}} = 98.6\%$
	DAB:	$\gamma_{\mathrm{DAB}} = 4.60\,\mathrm{kW/kg}$,	$\eta_{\mathrm{DAB}} = 97.1\%$
$\gamma = 1.00\,\mathrm{kW/kg}$ $\eta = 91.7\%$	Generator:	$\gamma_{\mathrm{G}} = 2.14\,\mathrm{kW/kg}$,	$\eta_{\mathrm{G}} = 96.9\%$
	VSR:	$\gamma_{\mathrm{VSR}} = 18.3\,\mathrm{kW/kg}$,	$\eta_{\mathrm{VSR}} = 98.6\%$
	DAB:	$\gamma_{\mathrm{DAB}} = 3.53\,\mathrm{kW/kg}$,	$\eta_{\mathrm{DAB}} = 97.4\%$

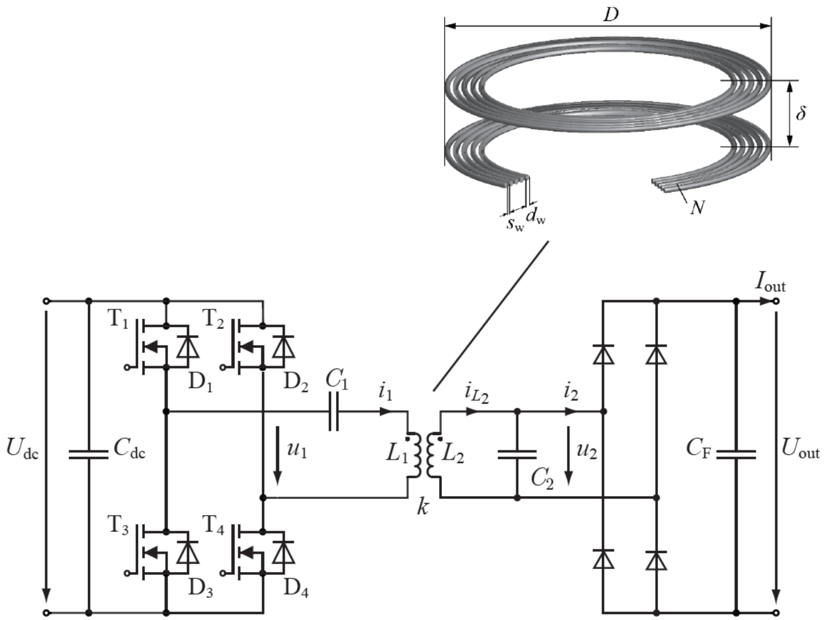


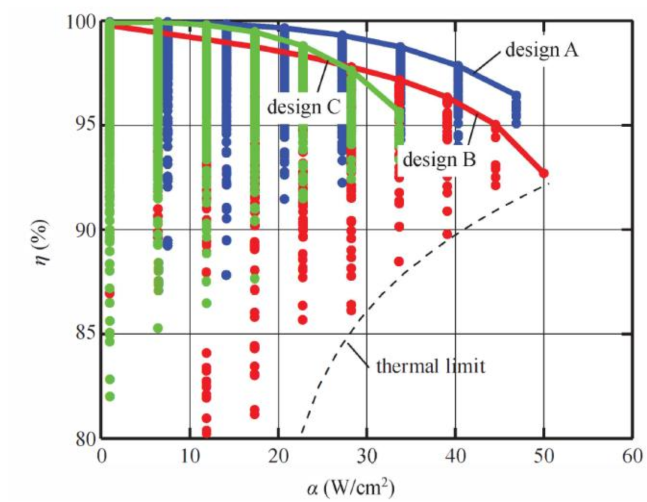


- **Final Step: System Control Consideration**

ηα-Pareto Front for Inductive Charging of EVs

* P_{out} = 0…75kW
* U_{out} = 400…800V
* Air Gap = 100…200mm



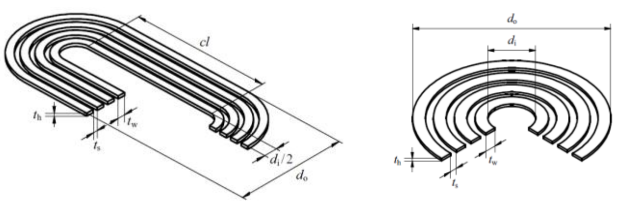


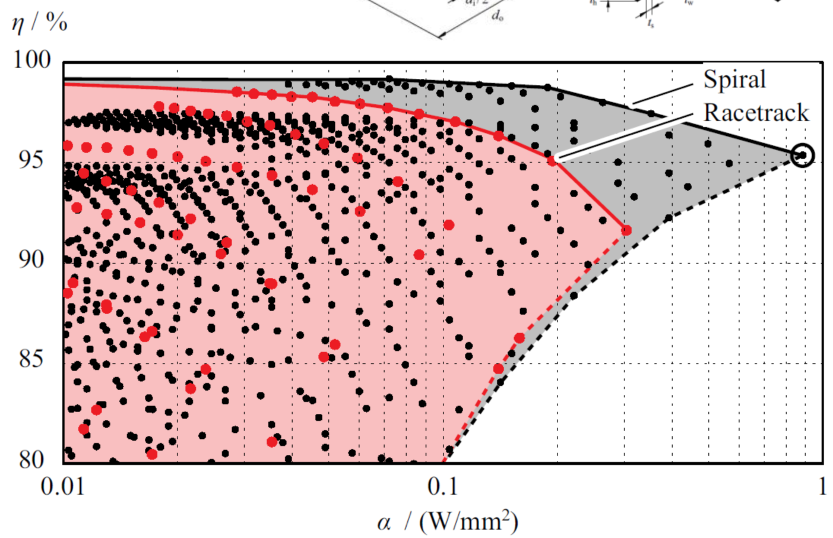
■ **Reduction of Stray Field Results only Possible with Less Efficient Design**

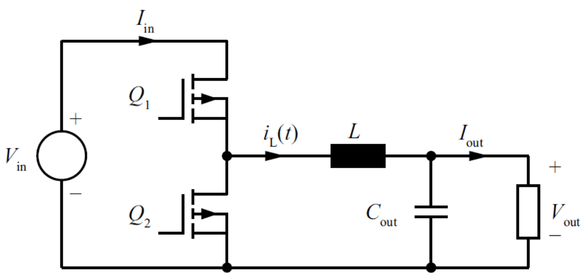
ηα-Pareto Front of Inductor for Power Supply on Chip

* U_{in} = 1.6 V
* U_{out} = 0.8 V
* P_{out} = 1.0 W

- PCB
- On-Top-of-Chip
- On-Chip

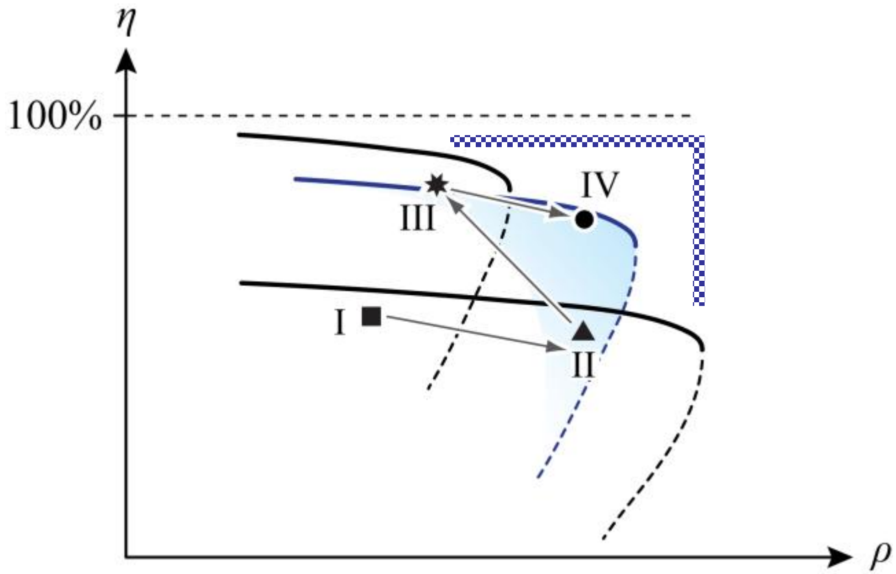






Observation

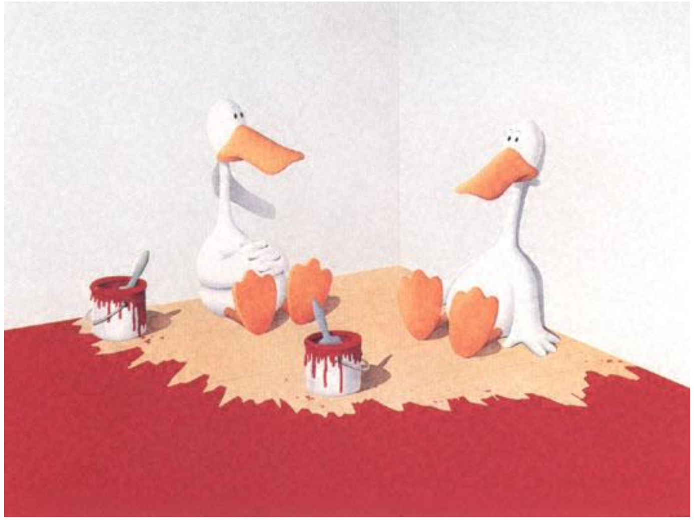
- **Very Limited Room for Further Performance Improvement !**



Observation

► **Very Limited Room for Further Performance Improvement !**

Efficiency



Power Density

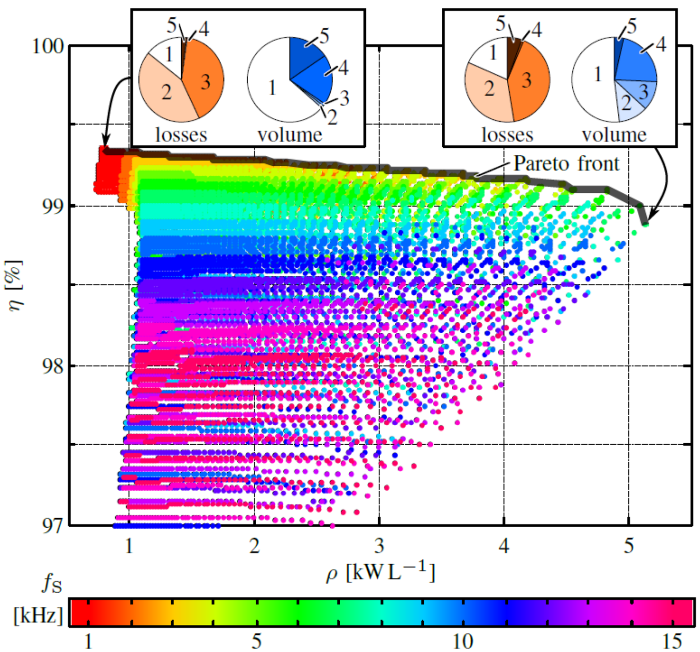
General Trade-Off Analysis

→ Reliability vs. Efficiency
→ Costs vs. Efficiency

Solid-State Transformer

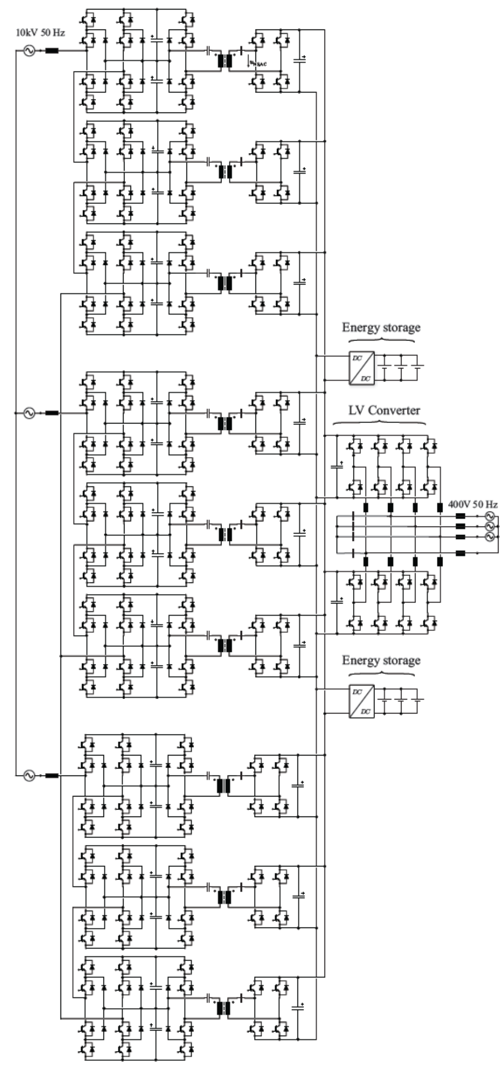
S_N = 630kVA
U_{LV} = 400 V
U_{MV} = 10kV

▶ **Trade-Off → Efficiency / Power Density**



DCM Series
Resonant
DC/DC Converter

(1) Transformer
(2) LV Semiconductors
(3) MV Semiconductors
(4) DC Link
(5) Resonant Capacitors

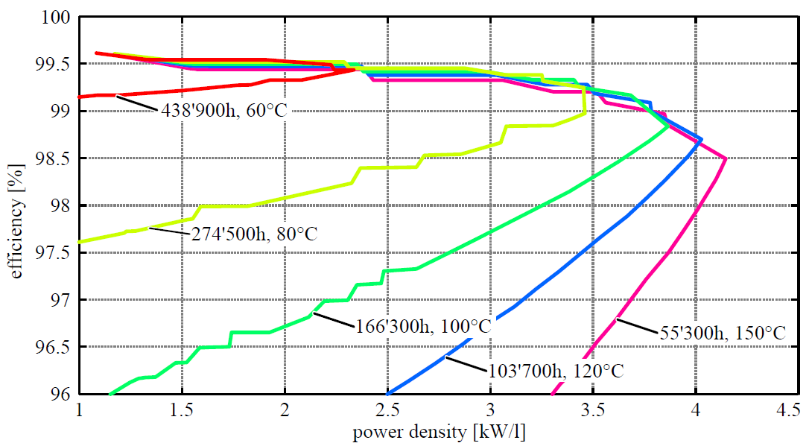


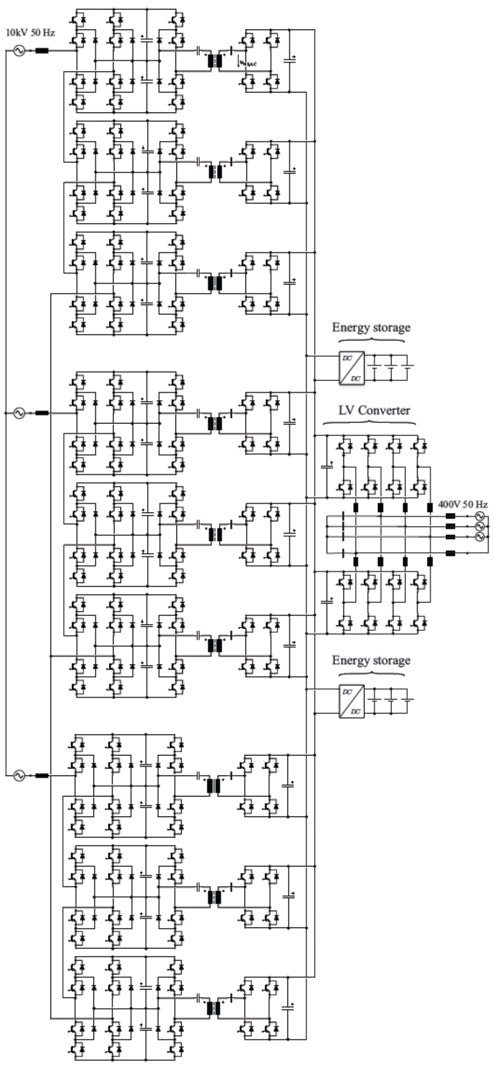
Solid-State Transformer

S_N = 630kVA
U_{LV} = 400 V
U_{MV} = 10kV

▶ Trade-Off → **Mean-Time-to-Failure vs. Efficiency / Power Density**

(5 Cascaded H-Bridges, 1700V IGBTs,
No Redundancy, FIT-Rate calculated acc. to T_j, 100FIT Base)

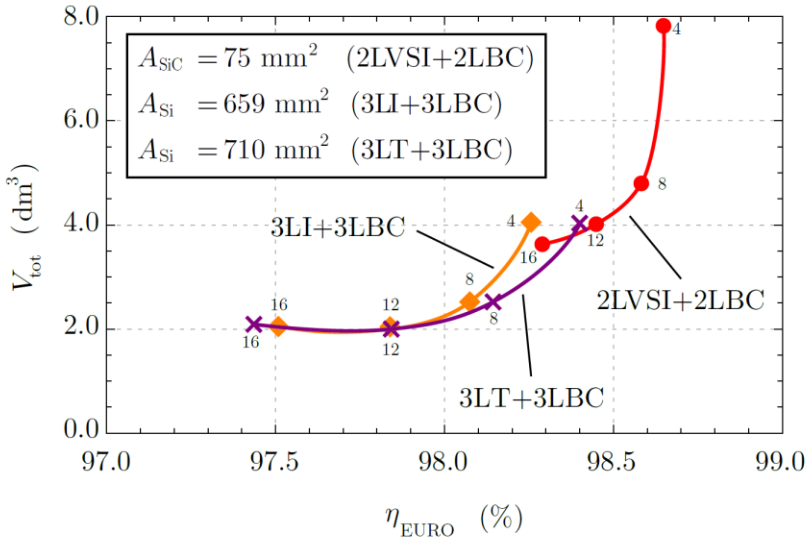


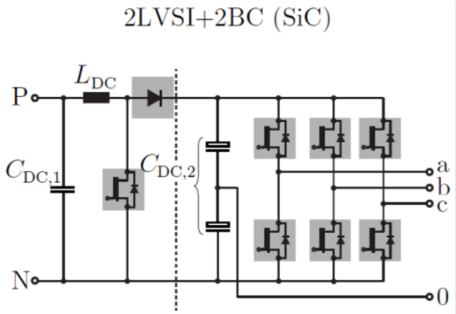


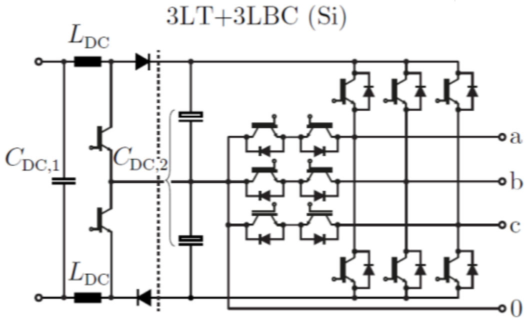
3-ph. PV Inverter Systems → Si vs. SiC

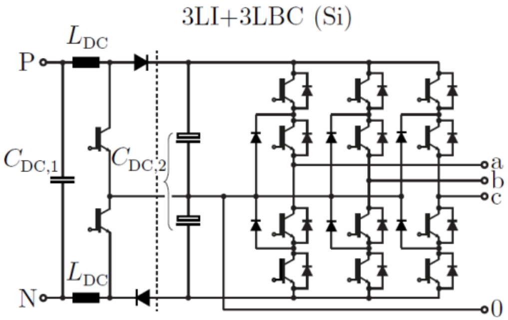
U_N = 400 V
U_{PV} = 450…820V
P = 10kW
f_S = 4…16kHz

► Cost Models → Efficiency / Power Density Analysis Extended to Initial Costs & Operating Revenue Calculation









Conclusions

→ Outlook

Conclusions

- Only the Consideration of the "TECHNOLOGY NODE" – (η,ρ,σ)-Coordinates in the Performance Space Shows the Quality of a Design !

- Don´t be Impressed by 99% Efficiency
- Don´t be Impressed by $100\mathrm{kW/dm^3}$ Power Density
- Don´t be Impressed by 0.05kW/$ Rel. Costs

- Ask in Addition →
  - * Converter Type
  - * Power Range / Operating Range
  - * Type of Cooling
  - * Technologies Used (SiC ?)
  - * etc.

- There is Nothing Magic in Converter Design →
- "Good Engineering & Multi-Objective Optimization"

Thank You !

Questions ?