ETH zürich

European PhD School

General Properties / Scaling Laws & Inherent Limitations of Energy Electronics

J.W. Kolar et al.

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

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J.W. Kolar, F. Krismer, P. Papamanolis

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ETH Zurich

21	Nobel Prizes
509	Professors
5800	T&R Staff
2	Campuses
136	Labs
35%	Int. Students
90	Nationalities
36	Languages
150th	Anniv. in 2005

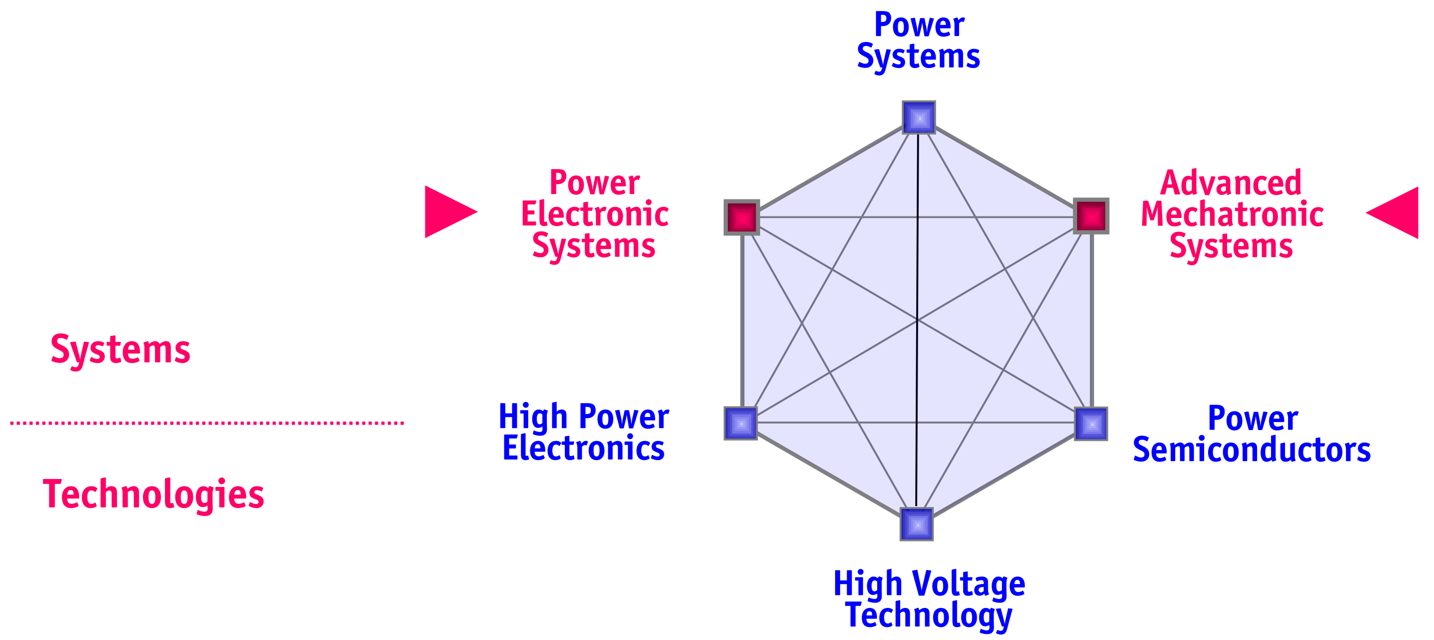
Departments

ARCH	Architecture
BAUG	Civil, Environmental and Geomatics Eng.
BIOL	Biology
BSSE	Biosystems
CHAB	Chemistry and Applied Biosciences
ERDW	Earth Sciences
GESS	Humanities, Social and Political Sciences
HEST	Health Sciences, Technology
INFK	Computer Science
ITET	Information Technology and Electrical Eng.
MATH	Mathematics
MATL	Materials Science
MAVT	Mechanical and Process Engineering
MTEC	Management, Technology and Economy
PHYS	Physics
USYS	Environmental Systems Sciences

Students ETH in total

14’500	B.Sc.+M.Sc.-Students
4’500	Doctoral Students

ITET – Research in E-Energy



- Balance of Fundamental and Application Oriented Research

Power Electronic Systems Laboratory

Industry Relations
R. Coccia / B. Seiler

Johann W. Kolar

Adv. Mechatronic Systems
D. Bortis

AC-DC Converter	AC-AC Converter	DC-DC Converter	DC-AC Converter	Multi-Domain Modeling	Measurement Technology	Advanced Mechatronics	Magnetic Levitation
		F. Krismer	**D. Bortis**	**F. Krismer**		**D. Bortis**	**D. Bortis**
M. Heller D. Menzi D. Neumayr	J. Azurza P. Czyz M. Haider	P. Bezerra T. Guillod G. Knabben J. Schäfer	M. Antivachis J. Böhler M. Guacci	P. Papamanolis	P. Niklaus	E. Hubmann	Th. Holenstein P. Püntener S. Miric

Secretariat
M. Kohn / Y. Schnyder

Administration
P. Maurantonio

Computer Systems
M. Eisenstat

Electronics Laboratory
P. Seitz

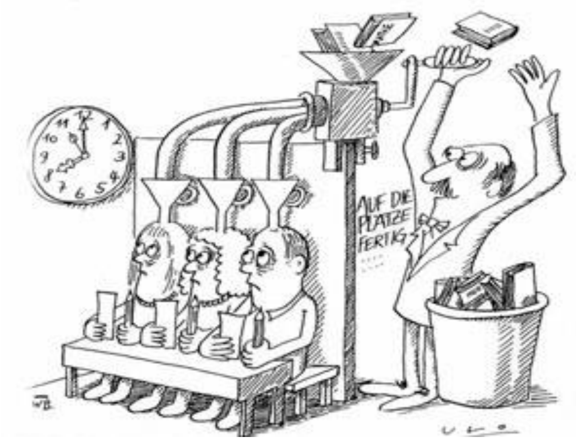
19 Ph.D. Students
2 Sen. Researchers

ECPE Competence Centre

EPSMA

Leading Univ. in Europe

Outline



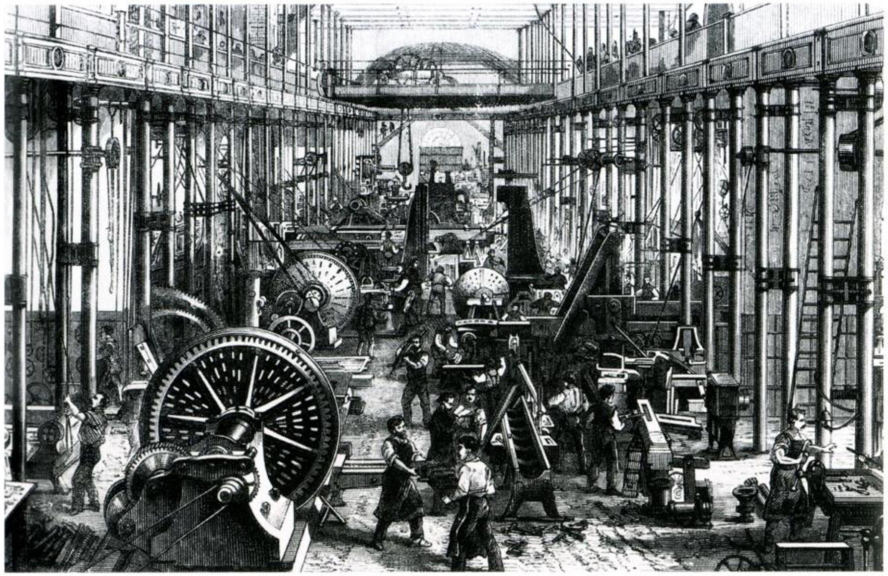
- Introduction
- AC vs. DC
- 1-Φ vs. 3-Φ Power Transmission
- Power Transistors & Packaging
- Efficiency & Multi-Objective Optimization
- Future Technology Development
- Conclusions

Introduction

A Leap Back in Time
to the Beginnings of Electrical Engineering

1^{st} Industrial Revolution → Industry 1.0

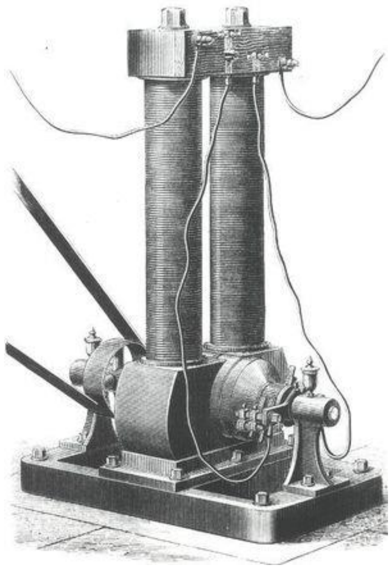
- 1760 → 1840
- Introduced by Numerous Key Inventions
- New Machines Facilitating Adv. Production & Transportation (Locomotives, Ships)
- Coal Fired Steam Engine (J. Watt, 1776) as Main Power Source

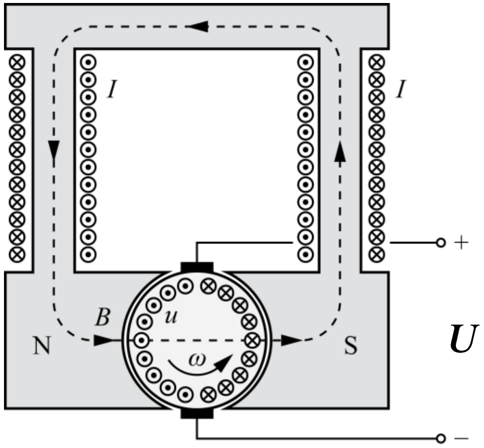


- Immense Growth in Coal Consumption / Massive Air Pollution → UK Public Health Act (1875)

2^{nd} Industrial Revolution → Industry 2.0

- 1840 → 1880
- New Steel Mass Manufacturing Processes (H. Bessemer, 1856)
- Electrical Technology Developed / Main Source of Power & Used in Adv. Production
- First Giant Industrial Corporations (e.g. GE, 1892)





$$U \sim B \cdot l \cdot v = B \cdot l \cdot \omega r$$

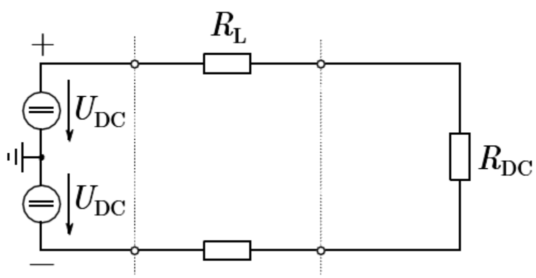
- Steam Turbine Driven DC Generator / Dynamo (*"Long-Legged Mary Ann"*) - *T.A. Edison, 1880*

Voltage Step-Up/Step-Down

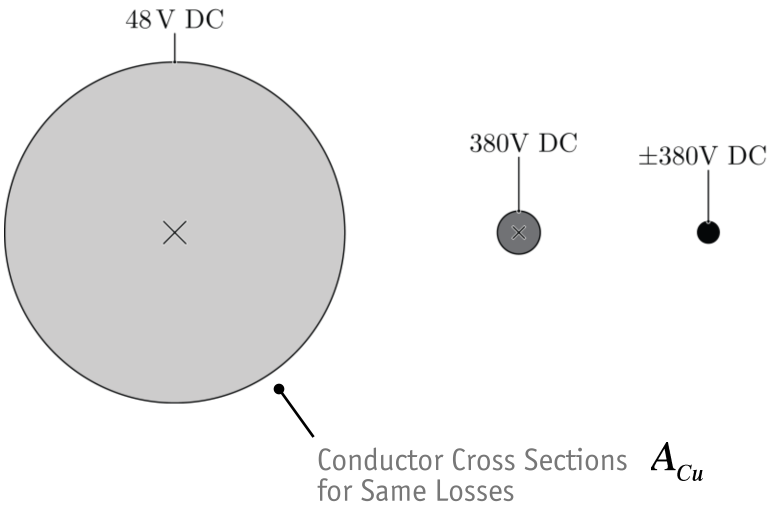
Losses of DC Power Systems

- Increase of Transmission Line Resistance with Transmission Distance l
- Red. of Resistance for Fixed Voltage only Through Larger Conductor Cross Section A_{Cu}

→ *Transmission Losses* $$P_{V,DC} = 2 \cdot \left(\frac{P}{2U_{DC}}\right)^2 \cdot R_L \sim \frac{1}{U_{DC}^2}$$



$$R_L = \frac{l}{\kappa A_{Cu}}$$



- Quadratic (!) Dependency of Losses on Voltage Level
- Allows Massive Reduction of Conductor Cross Section with Increasing Voltage Level

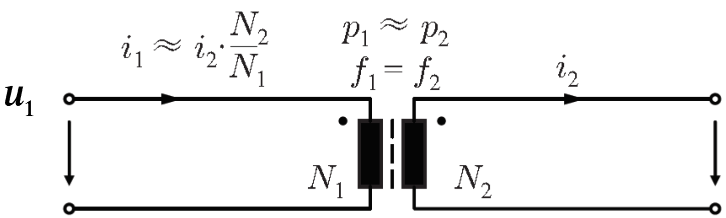
Voltage Step-Up/Down → AC Power System

- Voltage Transformation Based on "Electromagnetic Induction" (M. Faraday, 1831)
- First Transformers Employing Toroidal Cores Starting 1878
- Initially Different Operating Frequencies (e.g. 133Hz)

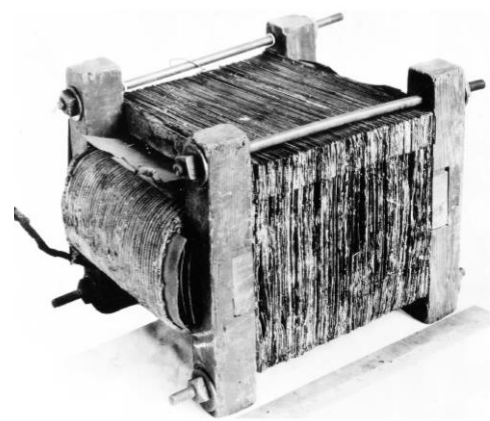
→ *Applied Voltage Determines Rate of Change of Magn. Flux*

$$u_1 = N_1 \cdot \frac{d\Phi}{dt}$$

$$\frac{d\Phi}{dt} \cdot N_2 = u_2$$



$$u_2 = u_1 \cdot \frac{N_2}{N_1}$$



- 1st Transformer Construction Allowing Easy Manufacturing (W. Stanley / G. Westinghouse)
- 2.2kV → 11kV for Long Distance 3-Φ Power Transmission (Niagara Falls → Buffalo, 1896)

Classical Transformer Properties

- Magnetic Core Material — * Silicon Steel
- Winding Material — * Copper or Aluminium
- Insulation/Cooling — * Mineral Oil or Dry-Type
- Operating Frequency — * 50/60Hz (El. Grid, Traction) or 16.7Hz (Traction)

Source: www.faceofmalawi.com

■ Main Advantages

- Inexpensive
- Purely Passive
- Highly Robust / Reliable
- Highly Efficient
- Short Circuit Current Limitation

Scaling of 1-Φ Transformers (1)

■ **Relation of Applied Voltage and Magnetic Flux**

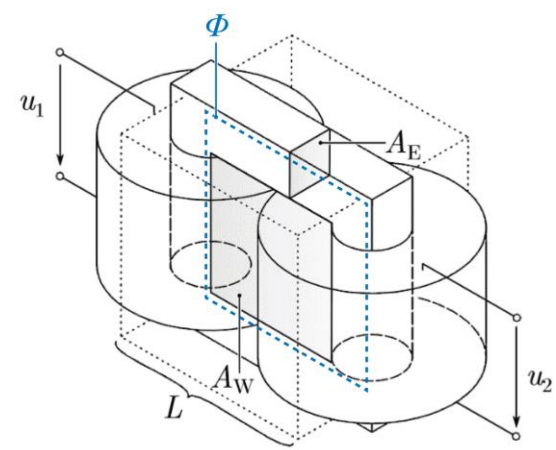
$$u_1 = \sqrt{2}U_1 \sin(\omega t) = N_1 \cdot \frac{d\Phi}{dt} \quad \rightarrow \quad \Phi = -\frac{\sqrt{2}U_1}{\omega N_1}\cos(\omega t) = \hat{B}A_E \cos(\omega t)$$

— **Magnetic Core Cross Section** $$A_E = \frac{1}{\sqrt{2}\pi}\frac{U_1}{\hat{B}_{\max} f}\cdot\frac{1}{N_1}$$

— **Winding Window** $$A_W = 2\frac{I_1}{k_W J_{\mathrm{rms}}}\cdot N_1$$

■ **Area Product** $$A_E A_W = \frac{\sqrt{2}}{\pi}\frac{P_t}{k_W J_{\mathrm{rms}} \hat{B}_{\max} f} \sim L^4 \uparrow$$

P_t .... Rated Power
k_W .... Window Utilization Factor
B_{max}... Flux Density Amplitude
J_{rms}... Winding Current Density
f ..... Frequency



$$I_2 \cdot N_2 \approx I_1 \cdot N_1$$

● **Economic Advantage of Large Systems** → ***"The Bigger the Better"***

Scaling of 1-Φ Transformers (2)

- **Rated Power of Transformers**

$$S_2 = U_2 I_2 = U_1 \tfrac{N_2}{N_1} I_1 \tfrac{N_1}{N_2} = U_1 I_1 = S_1$$

$$S = \frac{1}{2} \sum_i U_i I_i$$

— Area Product

$$A_E A_W = \tfrac{\sqrt{2}}{\pi} \frac{P_t}{k_W J_{\text{rms}} \hat{B}_{\max} f} = \tfrac{\sqrt{2}}{\pi} \frac{S}{k_W J_{\text{rms}} \hat{B}_{\max} f}$$

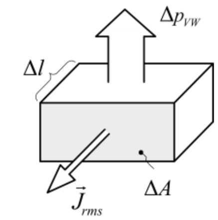
— Scaling of Power $S \sim L^4$

— Scaling of Volume / Mass / Costs $V \sim L^3$ $m \sim L^3$

— Scaling of Core & Wdg Losses $P_{V,W} = p_{VW} V_W \sim L^3$ $P_{V,E} = p_{VE} V_E \sim L^3$

- Economic Advantage of Large Systems → *Lower Relative Costs & Higher Efficiency (!)*

Scaling of 1-Φ Transformers (3)

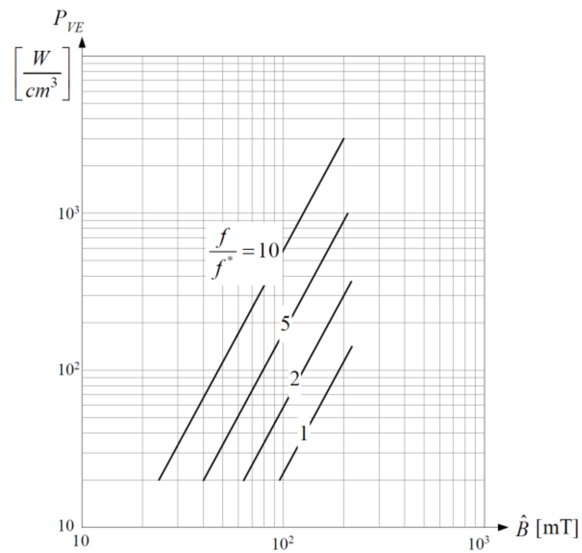


- **Winding Losses**

$$p_{VW} = \frac{\Delta P_{VW}}{\Delta V_W} = \frac{1}{\Delta A \cdot \Delta l}(J_{\mathrm{rms}}\Delta A)^2 \frac{\Delta l}{\kappa \cdot \Delta A} = \frac{J_{\mathrm{rms}}^2}{\kappa}$$

- **Core Losses**

$$p_{VE} = \frac{\Delta P_{VE}}{\Delta V_E} = k\, f^{\alpha}\hat{B}^{\beta} \quad \alpha = 1.2 \ldots 2 \quad \beta = 2.3 \ldots 3$$



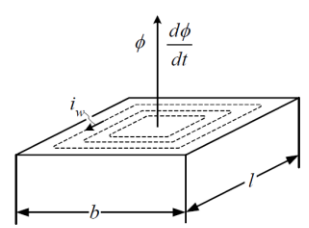
— **Hysteresis Losses (W/cm³)** $\quad p_{VH} = c_H f \hat{B}^2$

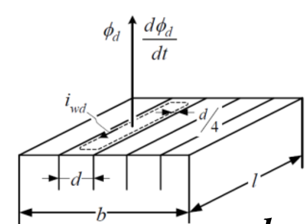
— **Eddy Curr. Losses (W/cm³)**

$$\hat{U} \sim (\tfrac{1}{2}dl) f \hat{B}$$

$$p_{VH} \sim \kappa \frac{b^2}{n^2}(f^2 \hat{B}^2)$$

$$R = \frac{2l}{\kappa(\frac{1}{2}dh)}$$



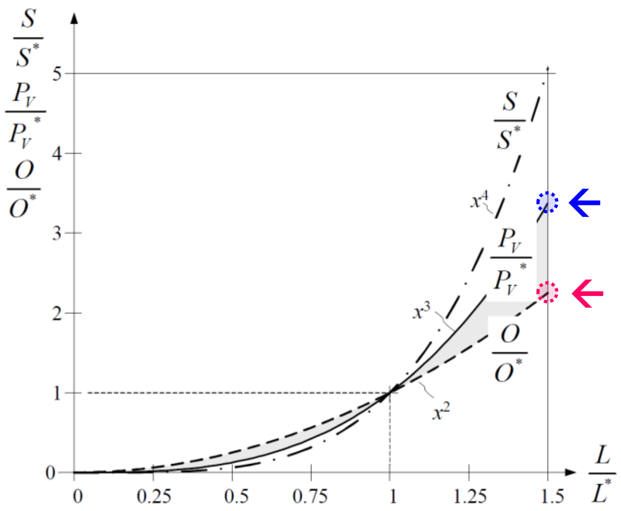


$$n = \frac{b}{d}$$

- **Losses prop. to Volume / Heat Transfer to Ambient prop. to Surface**
- **Requires Adv. Cooling of Higher Power Systems for Avoiding Thermal Limitation**

Scaling of 1-Φ Transformers (4)

- **Thermally Limited Designs** → Allowed Increase of Losses Coupled to Increase of Surface



- Surface Area $O \sim L^2$
- Core Losses $P_{VE} \sim \hat{B}^{\beta} L^3 \sim L^2 \rightarrow \hat{B} \sim L^{-\frac{1}{\beta}}$
- Winding Losses $P_{VW} \sim J_{rms}^2 L^3 \sim L^2 \rightarrow J_{rms} \sim L^{-\frac{1}{2}}$
- Winding Current $I_{rms} \sim L^2 J_{rms} \sim L^{\frac{3}{2}}$

- Scaling for Power Rating

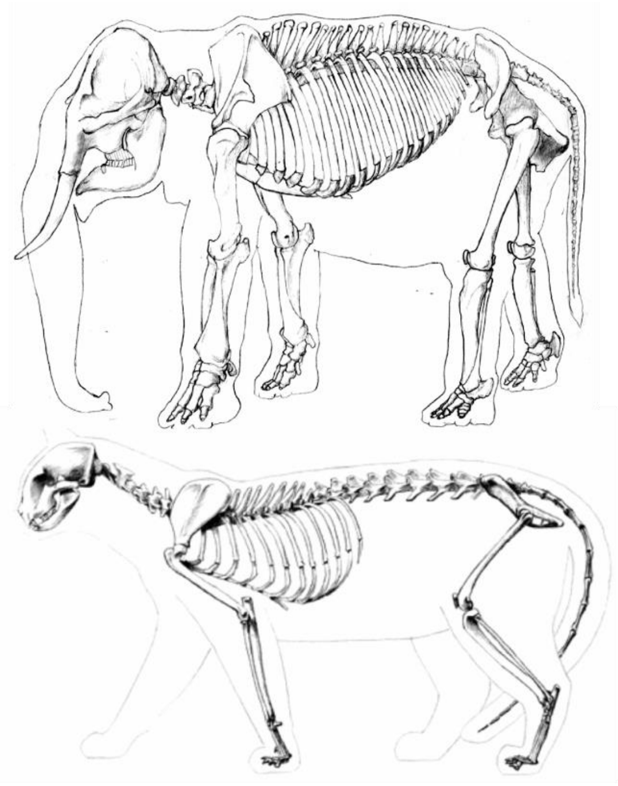
$$S = \frac{1}{2}\sum_i U_i I_i \sim \hat{\Phi} I_{rms} \sim (L^2 \hat{B}_{max}) L^{\frac{3}{2}} \sim L^{3.5} L^{-\frac{1}{\beta}} \sim\simeq L^3$$

- *Volume prop. to Rated Power → Constant Power Density (!)*

Remark — Scaling Applied to Biology

- Comparison of Skeleton / Metabolism etc. of Animals of Different Physical Sizes (e.g. Cat & Elephant)

Source: getdrawings.com/estuary-drawing

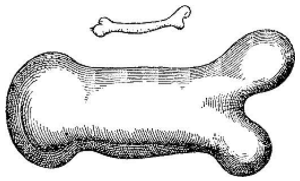


— Mass / Weight of an Animal $m \sim L^3$

— Area-Related Strength of Bones $\sigma\left(\frac{\text{kg}}{\text{cm}^2}\right) \approx \text{const.}$

— Required Diameter of the Bones $\sigma D^2 \sim m \sim L^3$

$$D \sim L^{\frac{3}{2}}$$



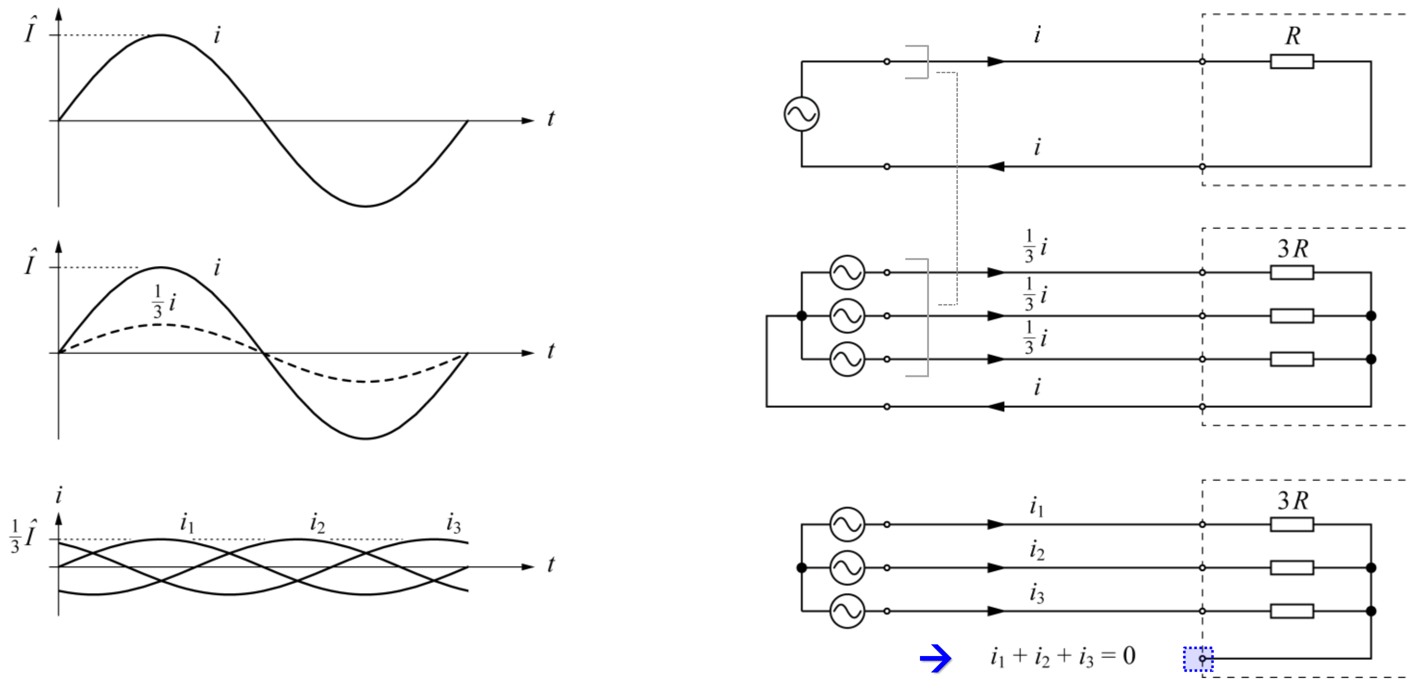
- First Systematic Studies by *Galileo Galilei* (1564-1642)
- Diameter of Bones Disproportional to Length

3-Φ AC Power Transmission

Lower Realization Effort
Constant Instantaneous Power Flow
Generation of Constant Torque

Advantages of 3-Φ Power Transfer (1)

- Comparison for 1-Φ Power Transfer to 3 x 1-Φ System & Direct 3-Φ System



- 3-Φ System → *Reduction of Losses and Conductor Material Effort by Factor of 2 (!)*
- "Interleaving" of the Phases also Employed in Pulse-Width Modulated Converters

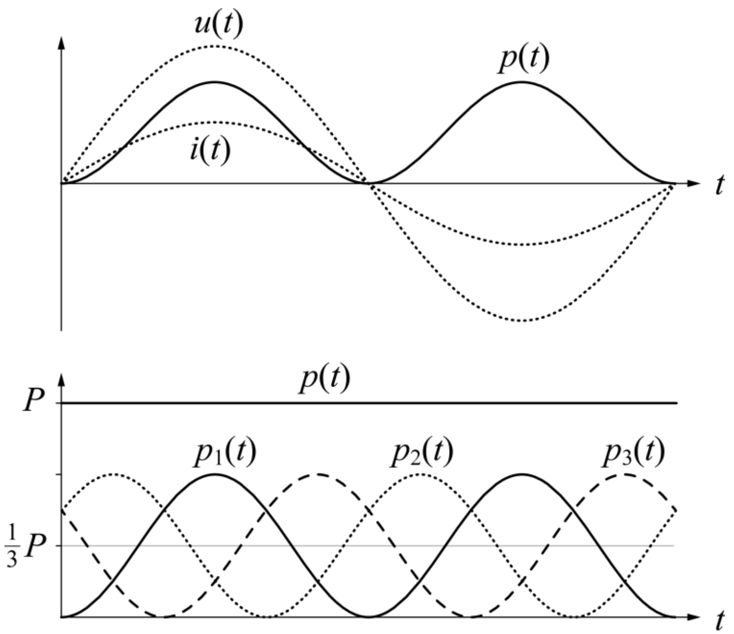
Advantages of 3-Φ Power Transfer (2)

- Comparison of Instantaneous Power Flow of 1-Φ and Direct 3-Φ System

— Voltage & Current Zero Crossings → Power Fluctuation of 1-Φ System with 2x Supply Frequency

$$p(t) = u\,i = UI\left[1 - \cos(2\omega t)\right]$$

$$p(t) = u_1 i_1 + u_2 i_2 + u_3 i_3 = 3UI$$



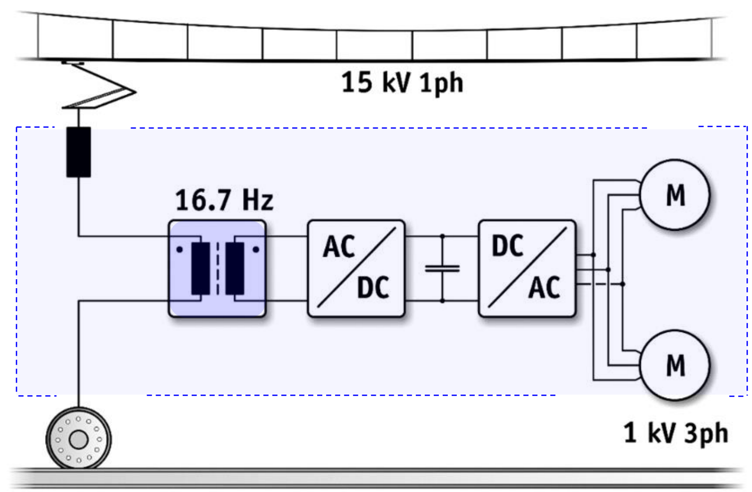
- 3-Φ System → *„Interleaving" of the Phases Results in Const. Instantaneous Overall Power Flow*
- No Storage Required for 3-Φ AC/DC Conversion & Const. Torque Generation of 3-Φ Machines

Remark — Classical Locomotives

- 1-Φ Overhead Line Supply Used for Simplicity / Rail for Current Return
- 16.7Hz Due to Supply Frequ. Related Commutation Problem of Early 1-Φ AC Commutator Motors

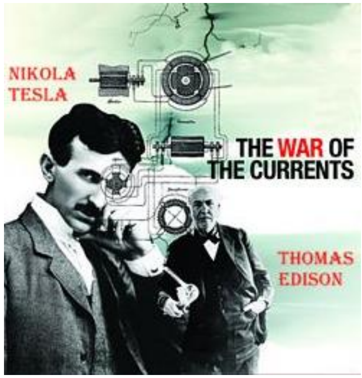
— Catenary Voltage	15kV or 25kV
— Frequency	16.7Hz or 50Hz
— Power Level	1...10MW typ.

Source: www.abb.com



• Transformer	Efficiency	90...95% (due to Restr. Vol., 99% typ. for Distr. Transf.)
	Current Density	6 A/mm^2 (2A/mm^2 typ. Distribution Transformer)
	Power Density	2...4 kg/kVA

AC vs. DC
Power Transmission



Source: www.yacht-chartercroatia.com

T.A. Edison vs. N. Tesla
DC Advantages for Very Long Distance Transmission

Remark

„The War of Currents“

- *DC Current* Favored by Edison (Safety) / *AC Technology* Favored by Westinghouse (Transmission)
- Killing of Elephant "Topsy" (1903) by Electrocution to Demonstrate the Deadly Impact of AC
- AC Dynamo Powered "*Electric Chair*" as Alternative to Hanging → *"Westinghoused"*

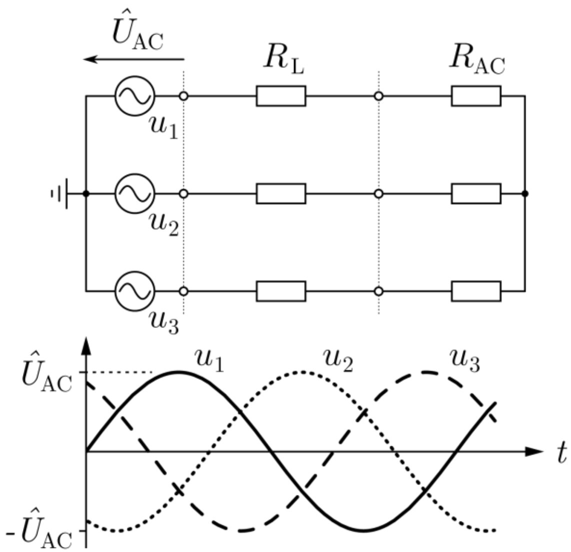
— AC Electric Chair

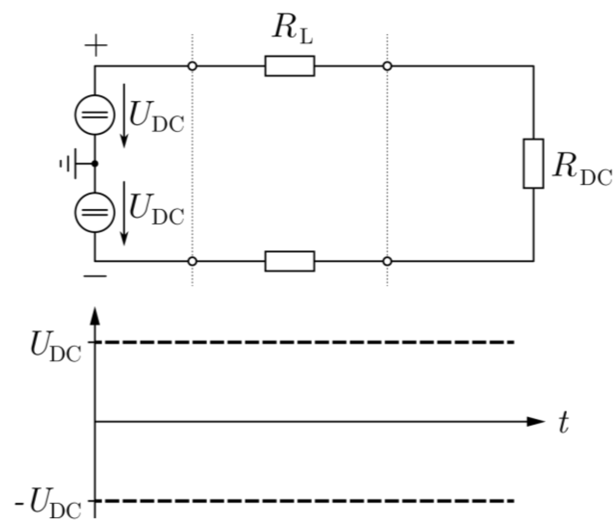
— Documentary Film by *Edison Film Company*

- Finally Breakthrough of AC Technology Due to *Missing DC-Transformer* →*"Edisons´ Missing Link"*

AC vs. DC Power Transmission (1)

- DC Voltage → Max. Utilization of Isol. Voltage → Lower Losses & Less Conductor Material (!)





$$P_{V,AC} = 3 \cdot \left(\frac{\frac{1}{3}P}{U_{AC}}\right)^2 \cdot R_L$$

$$P_{V,DC} = 2 \cdot \left(\frac{P}{2U_{DC}}\right)^2 \cdot R_L$$

$$\frac{P_{V,DC}}{P_{V,AC}} = \frac{3}{2} \cdot \left(\frac{U_{AC}}{U_{DC}}\right)^2 \Big|_{U_{DC}=\hat{U}_{AC}=\sqrt{2}\,U_{AC}} = 0.75$$

- Transformation of DC Voltage Level Requires Power Electronics Interfaces (!)

History and Development of the Electronic Power Converter

E. F. W. ALEXANDERSON
FELLOW AIEE

E. L. PHILLIPI
NONMEMBER AIEE

THE TERM "electronic power converter" needs some definition. The object may be to convert power from direct current to alternating current for d-c power transmission, or to convert power from one frequency into another, or to serve as a commutator for operating an a-c motor at variable speed, or for transforming high-voltage direct current into low-voltage direct current. Other objectives may be mentioned. It is thus evidently not the objective but the means which characterizes the electronic power converter. Other names have been used tentatively but have not been accepted. The emphasis is on electronic means and the term is limited to conversion of power as distinguished from electric energy for purposes of communication. Thus the name is a definition.

Paper 44-143, recommended by the AIEE committee on electronics for presentation at the AIEE summer technical meeting, St. Louis, Mo., June 26–30, 1944. Manuscript submitted April 25, 1944; made available for printing May 18, 1944.

E. F. W. Alexanderson and E. L. Phillipi are with the General Electric Company, Schenectady, N. Y.

1944 !

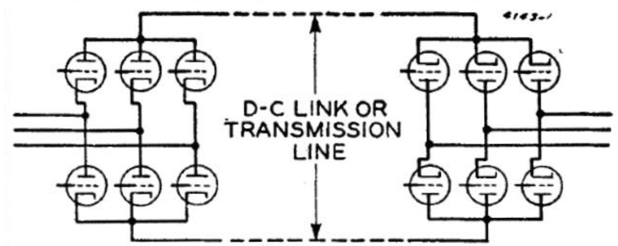


Figure 1. Electronic converter, dual-conversion type

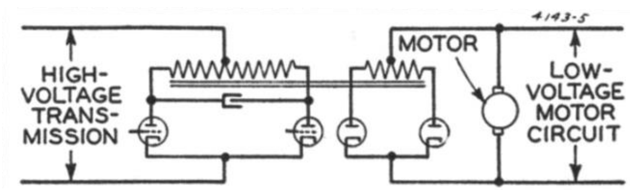
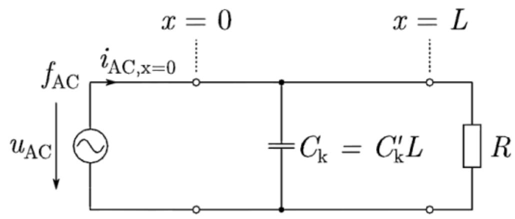
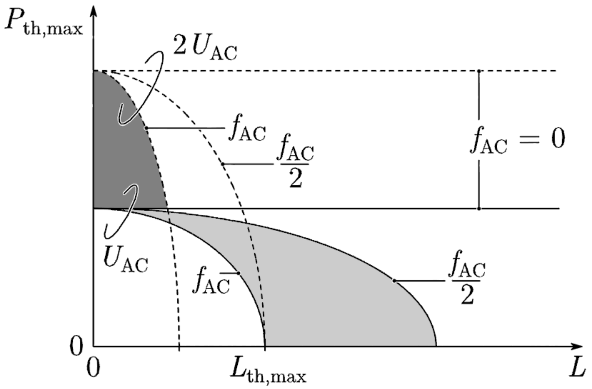


Figure 5 D-c transformer

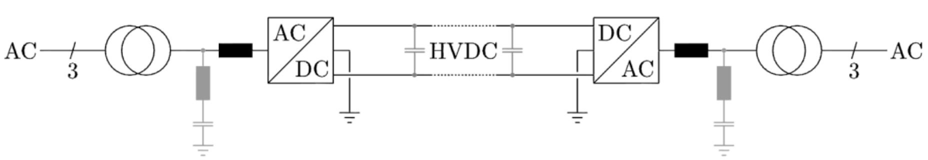
AC vs. DC Power Transmission (2)

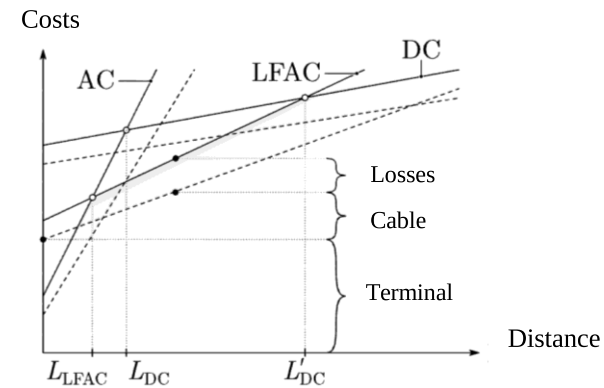
- **AC Cable – Thermal Limit Due to Cap. Current @ x = 0**





- **HVDC Transmission – Advantageous for Long Distances**

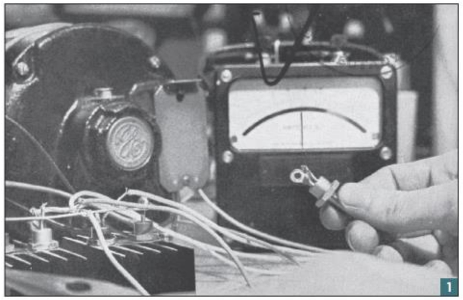




- **Low-Frequency AC (LFAC) as (Purely Passive) Solution for Medium Transmission Distances**

Transition to Modern Power Electronics

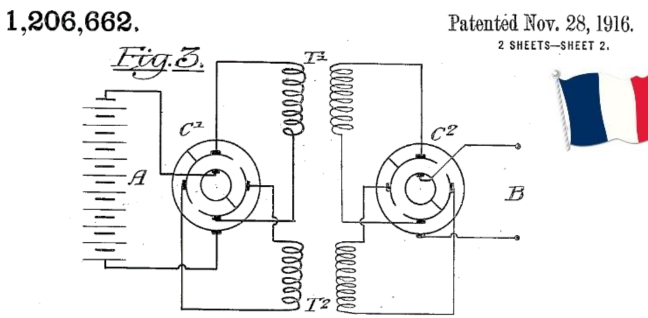
1958

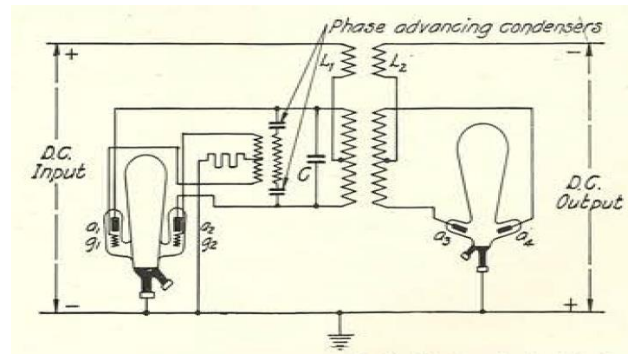


Mercury Arc Valves / Thyratrons →
Power Semiconductors

Electronic Transformer - History

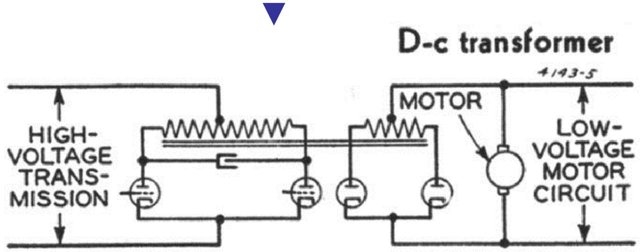
- System Using Mech. Switches *Patented Already in 1913* (!)
- Mechanical Sw. → Tubes → Mercury Arc Valves → Solid State Switches

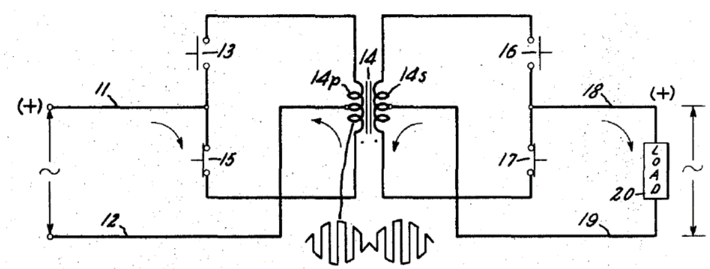




▲
1913 — *P.M.J. Boucherot*
1944 — *E.F.W. Alexanderson et al.*
▼

1928 — *D.C. Prince* ▲
1968 — *W. McMurray* ▼





- "Transformer of Cont. Current" / "DC Transformer" / "Electronic Transformer"

United States Patent Office

3,517,300
Patented June 23, 1970 ← 1970 !

1

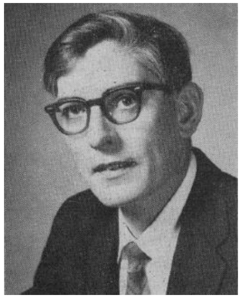
3,517,300
POWER CONVERTER CIRCUITS HAVING A HIGH FREQUENCY LINK

William McMurray, Schenectady, N.Y., assignor to General Electric Company, a corporation of New York

Filed Apr. 16, 1968, Ser. No. 721,817
Int. Cl. H02m 5/16, 5/30
U.S. Cl. 321—60 14 Claims

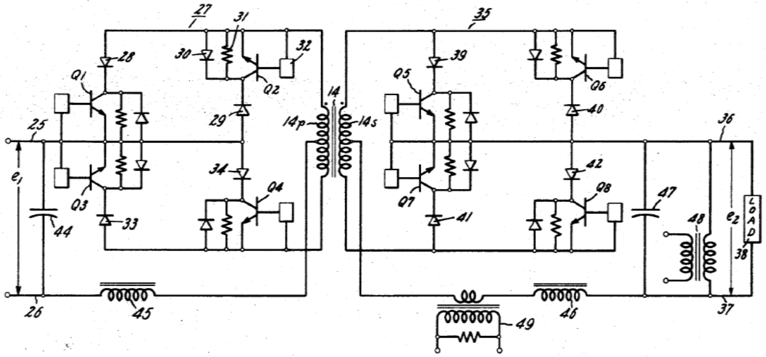
ABSTRACT OF THE DISCLOSURE

Several single phase solid state power converter circuits have a high frequency transformer link whose windings are connected respectively to the load and to a D-C or low frequency A-C source through inverter configuration switching circuits employing inverse-parallel pairs of controlled turn-off switches (such as transistors or gate turn-off SCR's) as the switching devices. Filter means are connected across the input and output terminals. By synchronously rendering conductive one switching device in each of the primary and secondary side circuits, and alternately rendering conductive another device in each switching circuit, the input potential is converted to a high frequency wave, transformed, and reconstructed at the output terminals. Wide range output voltage control is obtained by phase shifting the turn-on of the switching devices on one side with respect to those on the other side by 0° to 180°, and is used to effect current limiting, current interruption, current regulation, and voltage regulation.



Inventor:
William McMurray,
by Donald R. Campbell
His Attorney.

Fig. 3.

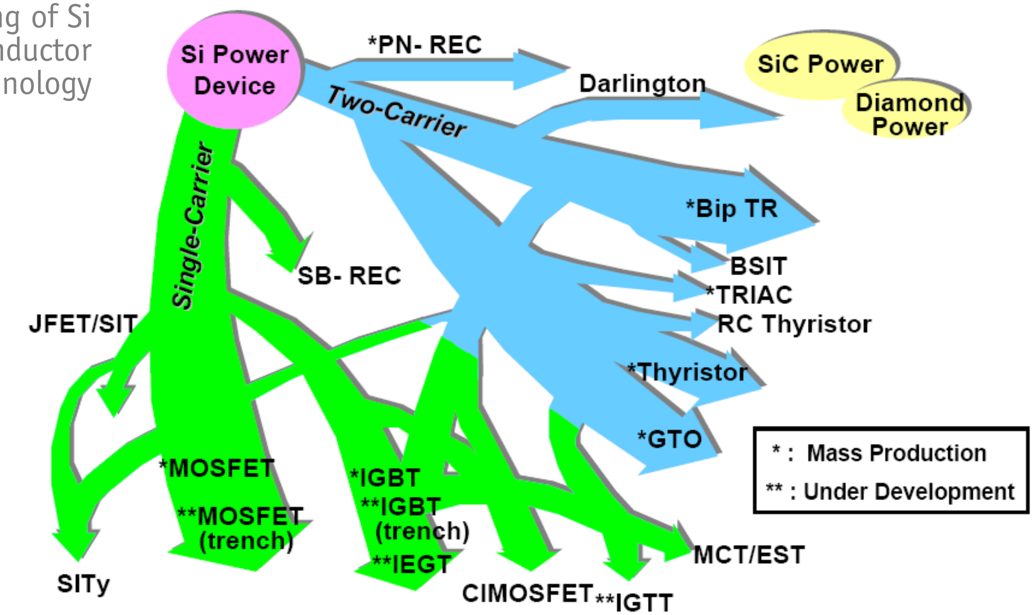


- Transistor/Diode-Based "Electronic Transformer"
- AC or DC Voltage Regulation & Current Regulation/Limitation/Interruption

Power Semiconductor Evolution

- First Commercial Si Thyristor (*Silicon Controlled Rectifier – SCR*) Introduced in 1958 by
- Unipolar and Bipolar Power Semiconductors
- Development Status in 1995 →

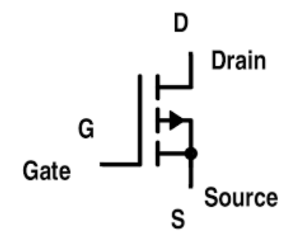
Spreading of Si
Power Semiconductor
Technology



- Si-Thyristor → Si-Bipolar Transistor → Si-Power MOSFET → Si-IGBT → SiC/GaN-Transistor → t.b.c.

Unipolar Si Power Semiconductors (1)

- Power MOSFETs of Higher Blocking Capability → Drift Layer Determines On-State Resistance
- Drift Layer Thickness Dependent on Blocking Capability



— Blocking Voltage $V_B \approx \frac{1}{2} W \cdot E_C \rightarrow \quad W = \frac{2V_B}{E_C}$

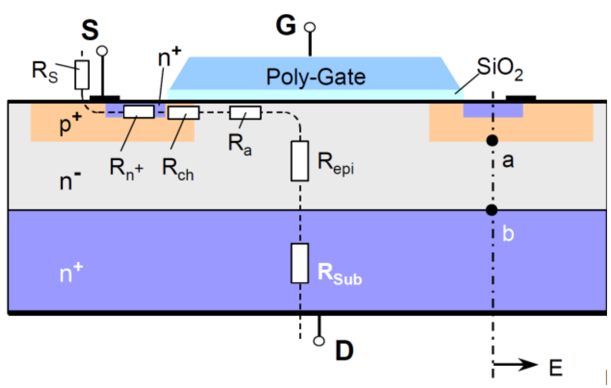
— Relation of Doping and E-Field Gradient $\varepsilon \frac{E_C}{W} = q N_D = \varepsilon \frac{E_C^2}{2V_B}$

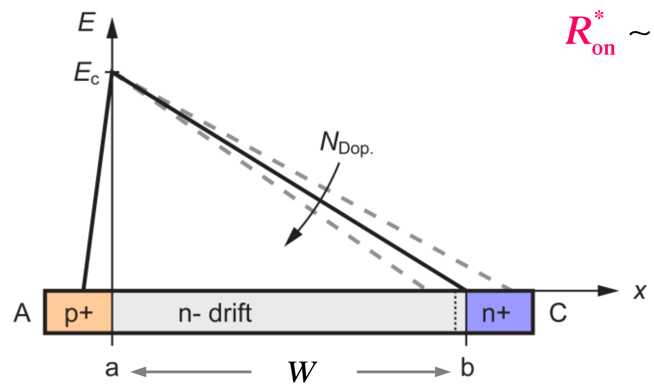
— On-State Resistance $R_{on} = \frac{W}{\kappa A} = \frac{W}{q N_D \mu_n A}$

— Spec. On-Resistance $R_{on}^* = R_{on} A = \frac{W}{q N_D \mu_n}$

— "Silicon Limit" $R_{on}^* = \frac{4V_B^2}{\varepsilon \mu_n E_C^3}$

$R_{on}^* \sim V_B^{2.4...2.6}$

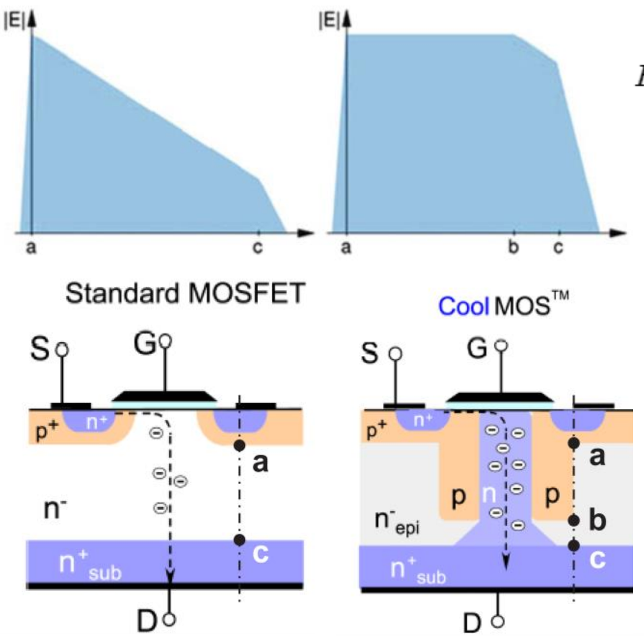


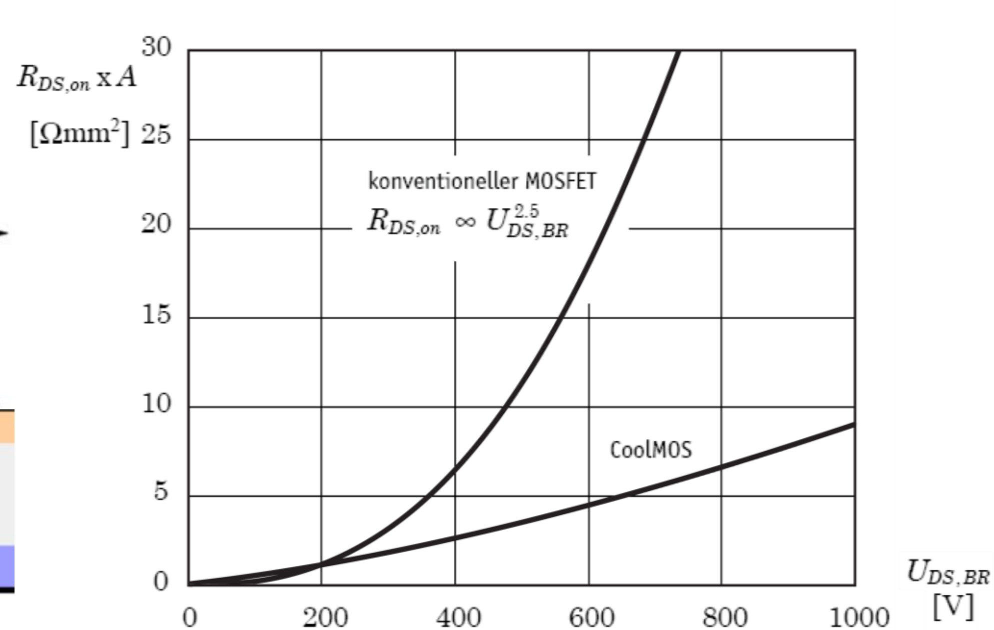


Unipolar Si Power Semiconductors (2)

- **Super-Junction Power MOSFETs (1997) → *Breaking the Silicon Limit* - $R_{DS(on)} \approx U_{DS,BR}^{1.0}$ (!)**
- **Highly-Doped n-Region / p-Columns Compensating the Current Conducting n-Charge**
- **Space Charge Layer along pn-Junction for U_{DS} > 50V / Depleted Voltage Sustaining Drift Zone**

Source: J. Lutz et al.



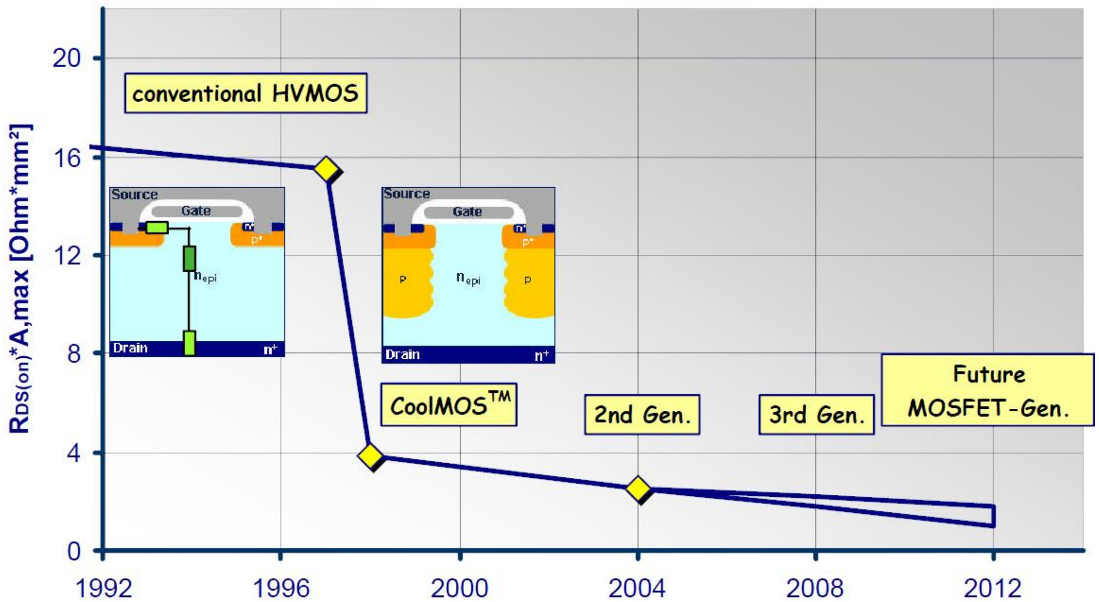


- *Electrical Conductivity Provided by Majority Carriers*

Si - Power MOSFET Development

- **Super-Junction Technology → Disruptive Improvement / Decrease of $R_{DS,(on)}$**

600V MOSFET Technology

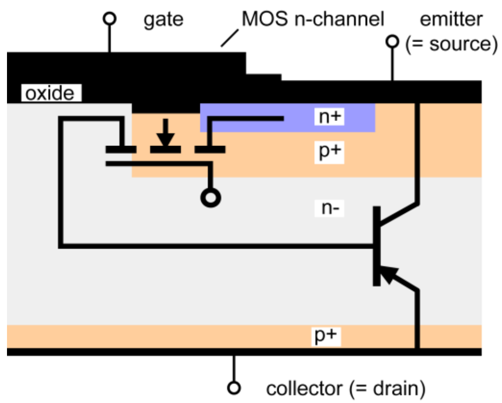


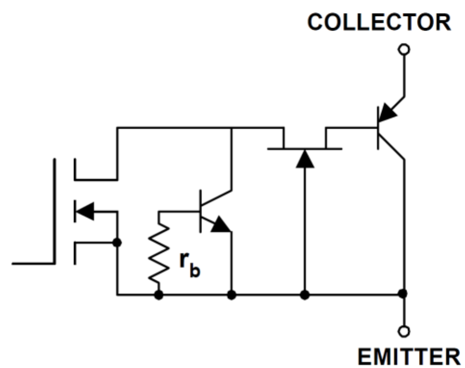
Source: infineon

- *Cont. Further Improvement / Main Challenges also in Low L/Low R_{th} Packaging*

Si - Isolated Gate Bipolar Transistor (IGBT)

- MOSFET Structure Extended with Drain-Side p+ Layer → Minority Carrier Injection into n- Layer
- Conductivity Modulation → Lower On-State Voltage @ High Blocking Voltage Rating
- Lifetime of Min. Carriers → Stored in pnp-BJT Base & Resulting in "Tail Current"/Sw. Losses



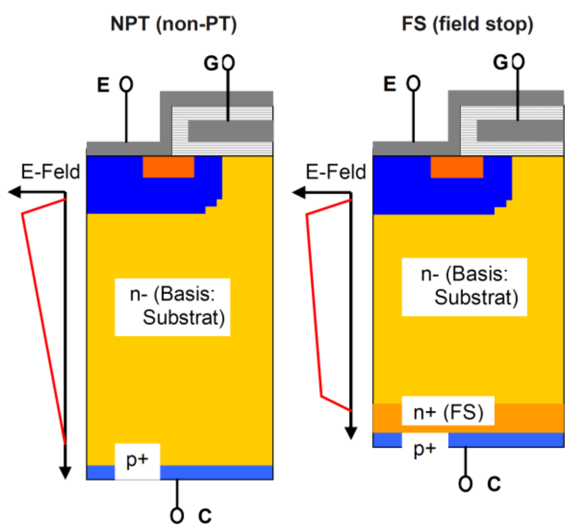


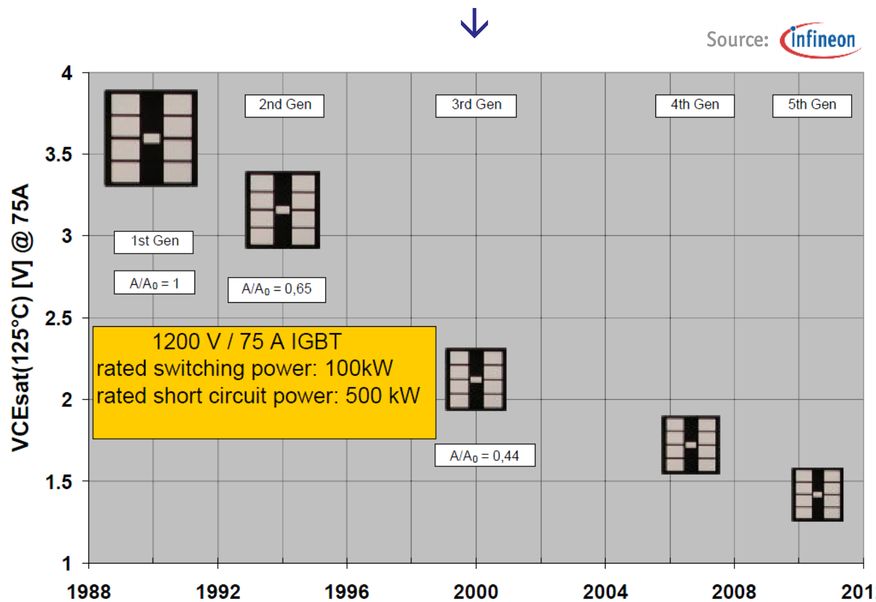
Source: IRF

- *IGBT: pnp-Bipolar Junct. Transistor Driven by n-Channel MOSFET in Pseudo-Darlington Structure*

Si - IGBT Development (1)

- 1988 Punch-Through (PT) → High Costs & Neg. Temp. Coefficient (TK)
- 1990 Non-Punch Through (NPT) → Rel. High On-State Voltage, pos. TK
- 2000 Field Stop (FS) Layer → Low Losses (Tail Current), pos. TK

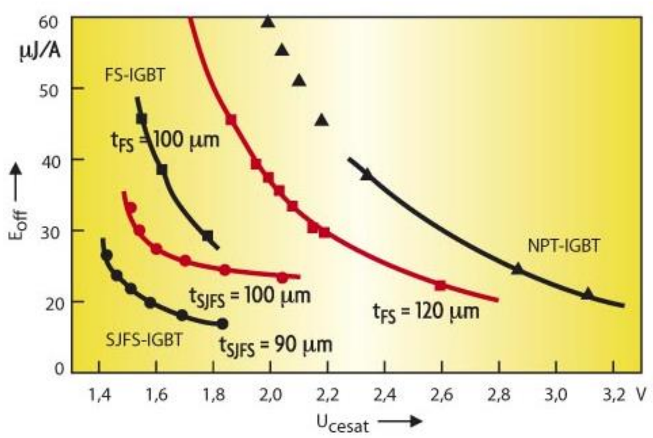


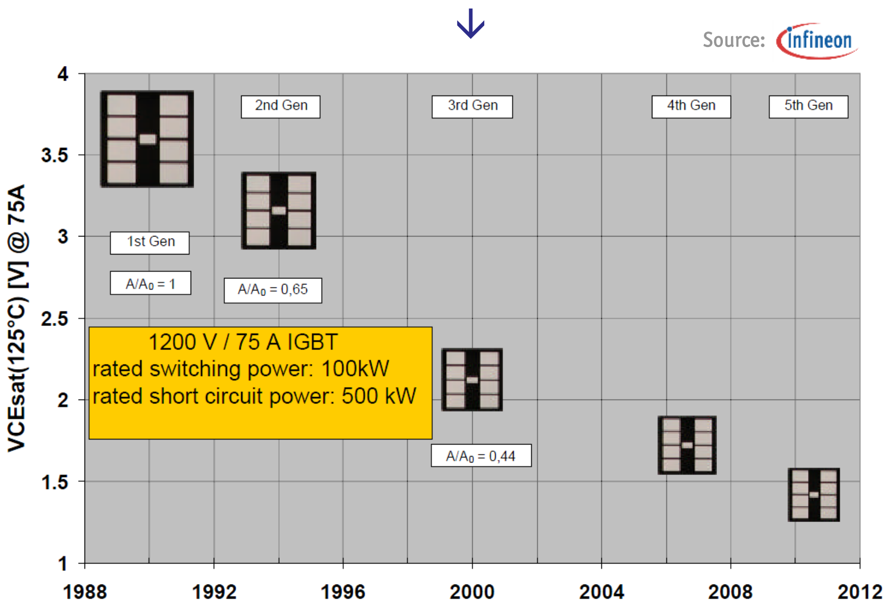


- *Reverse Conducting (RC) IGBT Monolithically Integr. Free-Wheeling Diode (Spec. Anode Structure)*

Si - IGBT Development (2)

- Field Stop (FS) Layer → Thinner Wafers & Improved Sw. Performance Comp. to NPT Structure
- FS Layer & Trench Gate → Improved Saturation Voltage $V_{CE,sat}$ & Turn-Off Energy E_{off}





- *Reverse Conducting (RC) IGBT Monolithically Integr. Free-Wheeling Diode (Spec. Anode Structure)*

Modern Switch-Mode Power Conversion

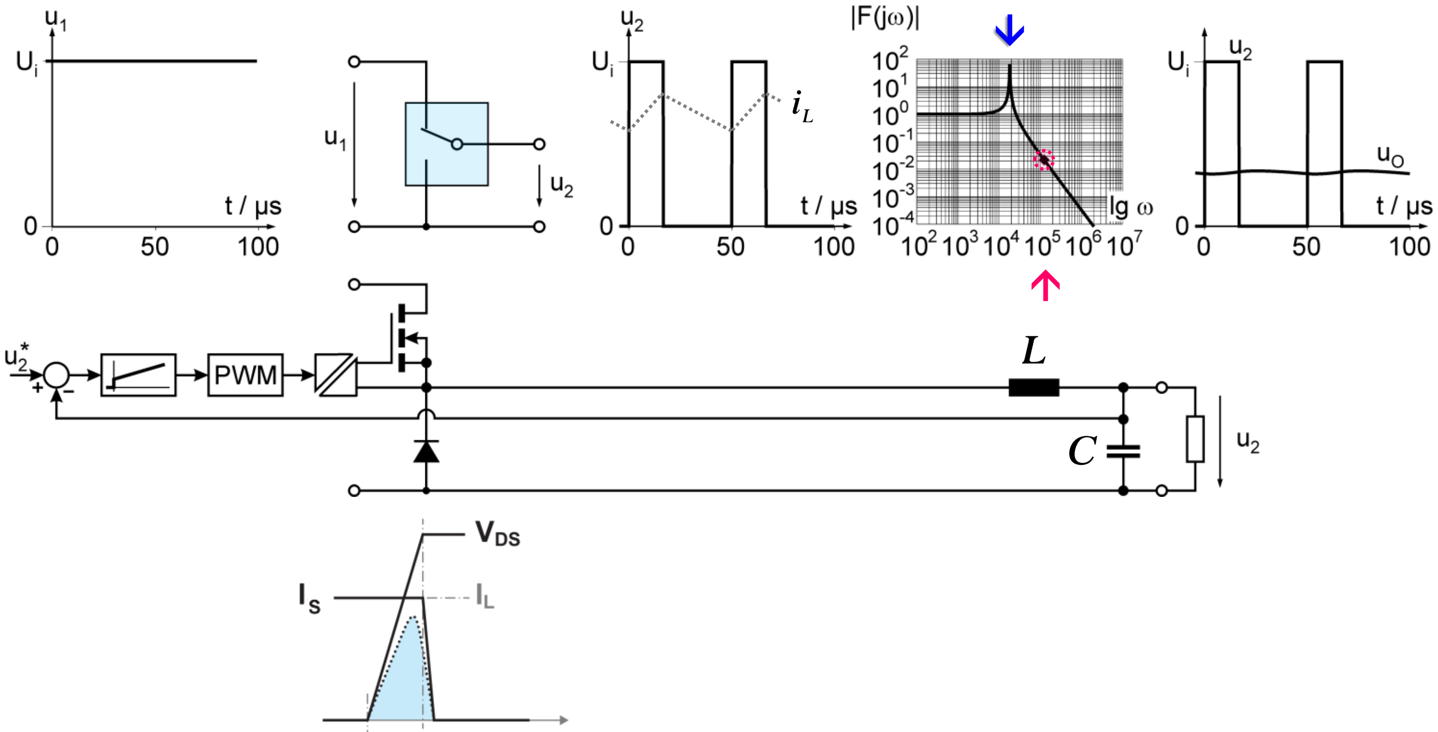
Pulse-Width Modulation
Time/Frequency Domain & Filtering
Parallel & Series Interleaving

Source: www.gograph.com

Pulse Width Modulated Converters

■ Basic Concept

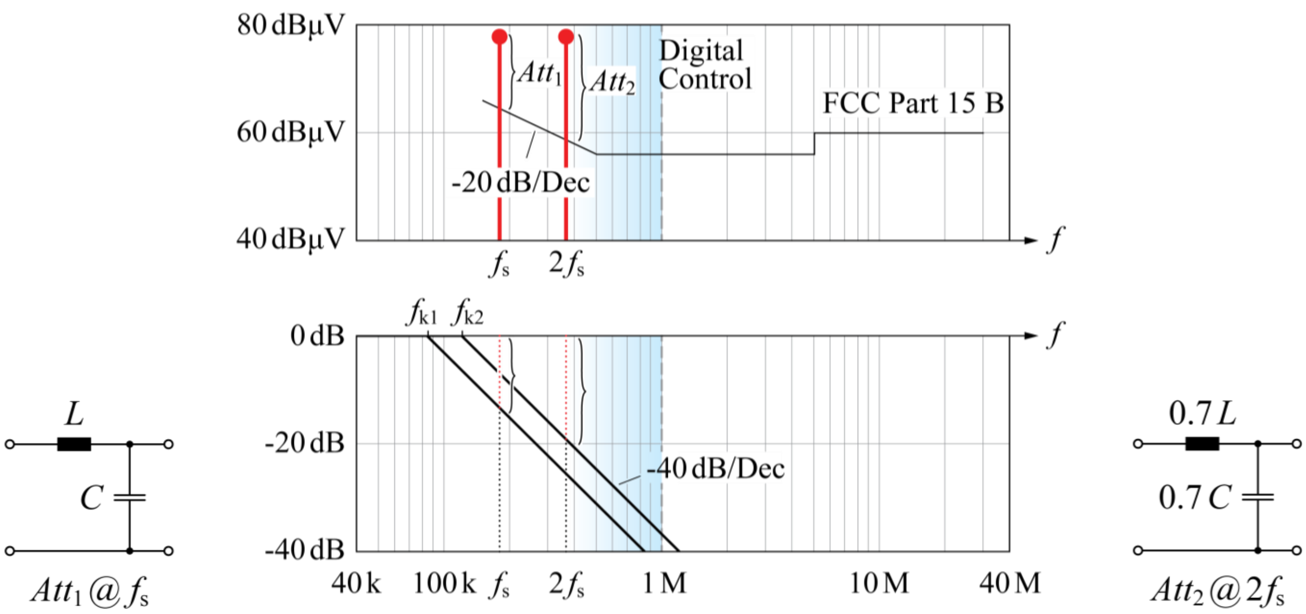
$$\omega_K = \frac{1}{\sqrt{LC}}$$



- Switch-Mode Voltage Formation and Subsequent Filtering
- *Higher Sw. Frequency → Smaller Filter Components* (Limited by Sw. Losses, Signal Processing etc.)

Increasing Switching Frequency

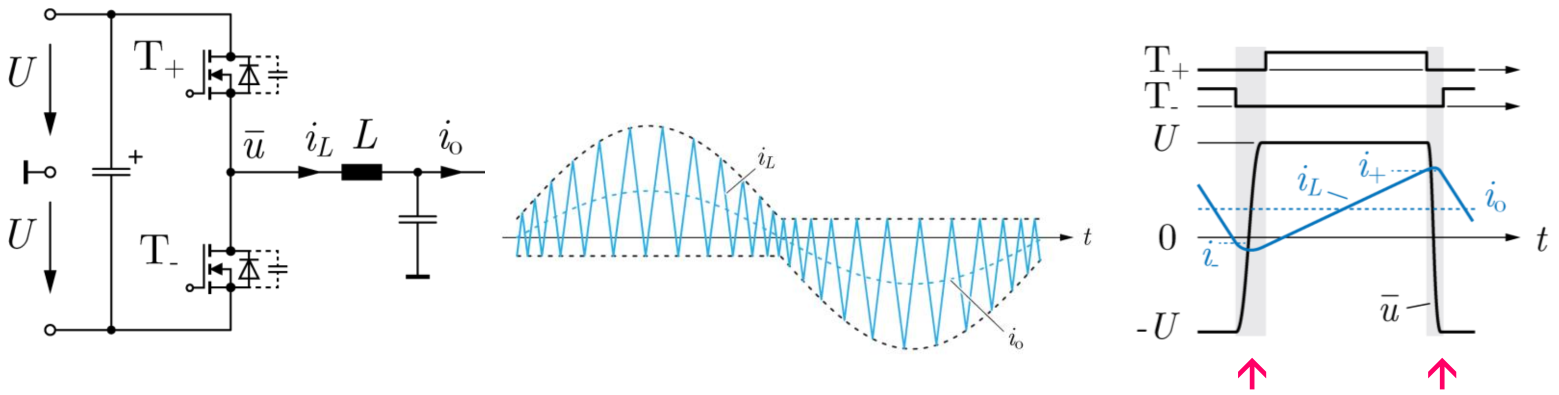
- *Reduction of EMI Filter Volume for Increasing Sw. Frequency*



- **Sw. Frequ. Limit** **Due to Sw. Losses (Heatsink Vol.), Inductor Losses, Signal Processing Delays etc.**

Soft-Switching Operation

- Low Inductance / Triang. Curr. Mode → *Zero Voltage Turn-Off AND Zero Voltage Turn-On (ZVS)*
- Increase of Conduction Losses Especially @ Low Load / Residual ZVS Losses of Si-Devices



- Requires Certain Voltage Headroom for Avoiding Very Low Sw. Frequencies
- *Wide Variation of Sw. Frequ.* → Spreading of EMI Noise & Red. Filter Effort / Fast Sign. Processing

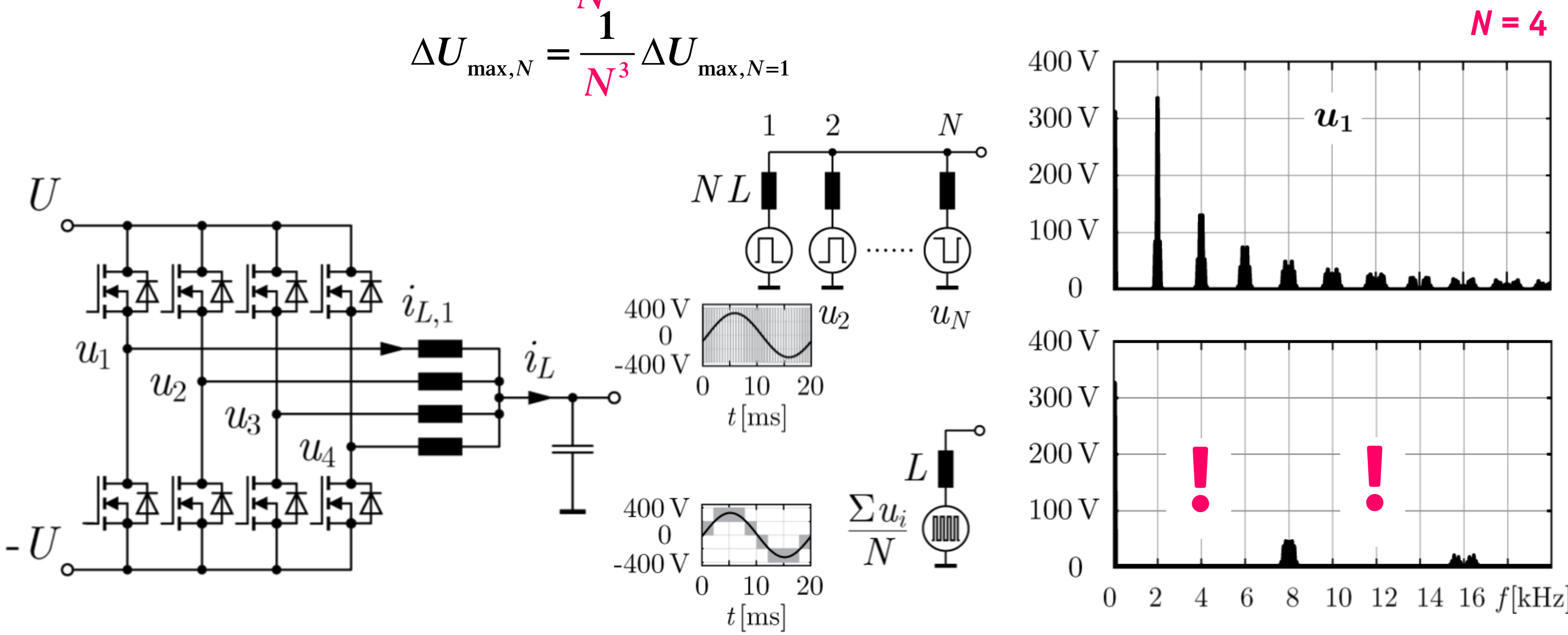
Parallel Interleaving (1)

- Multiplies Sw. Frequ. / Reduced Ripple @ Same (!) Switching Losses & Incr. Control Dynamics

$$f_{S,\mathrm{eff}} = N \cdot f_S$$

$$\Delta I_{\max,N} = \frac{1}{N^2} \Delta I_{\max,N=1}$$

$$\Delta U_{\max,N} = \frac{1}{N^3} \Delta U_{\max,N=1}$$



- Control Implementation Benefits from Improving Digital IC Technology
- Redundancy → Allows Large Number of Units without Impairing Reliability

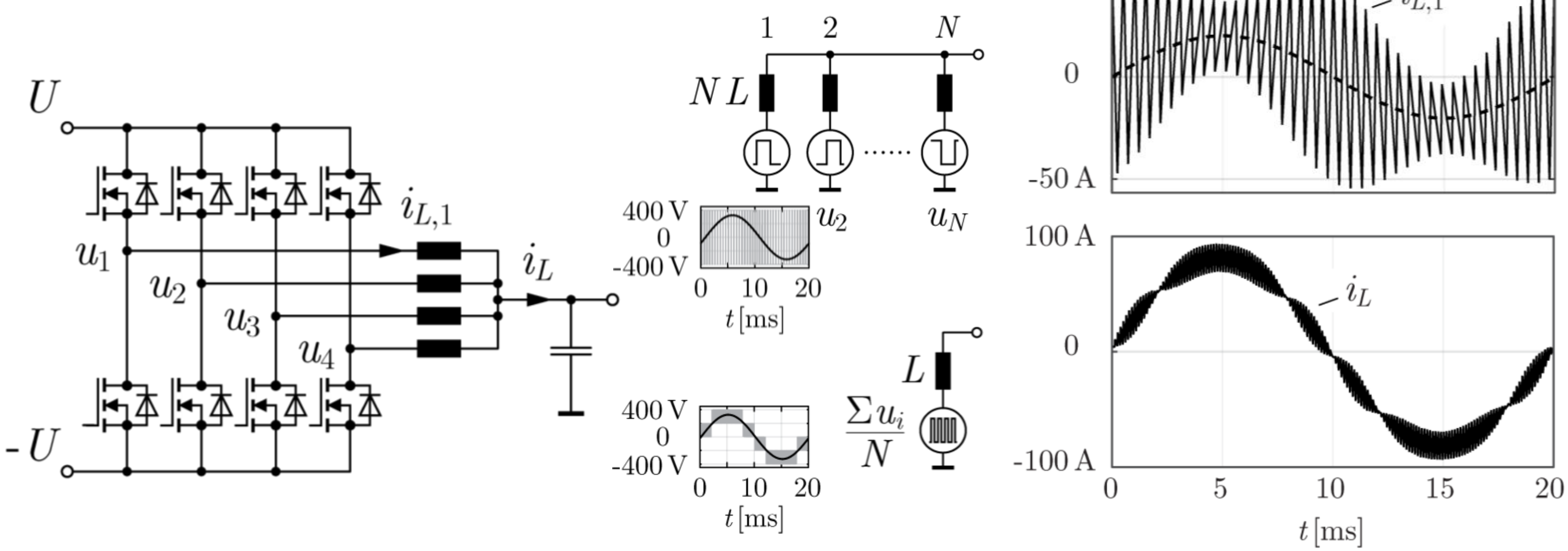
Parallel Interleaving (2)

- Multiplies Sw. Frequ. / Reduced Ripple @ Same (!) Switching Losses & Incr. Control Dynamics

$$f_{S,\text{eff}} = N \cdot f_S \qquad \Delta I_{\max,N} = \frac{1}{N^2} \Delta I_{\max,N=1}$$

$$\Delta U_{\max,N} = \frac{1}{N^3} \Delta U_{\max,N=1}$$

N = 4



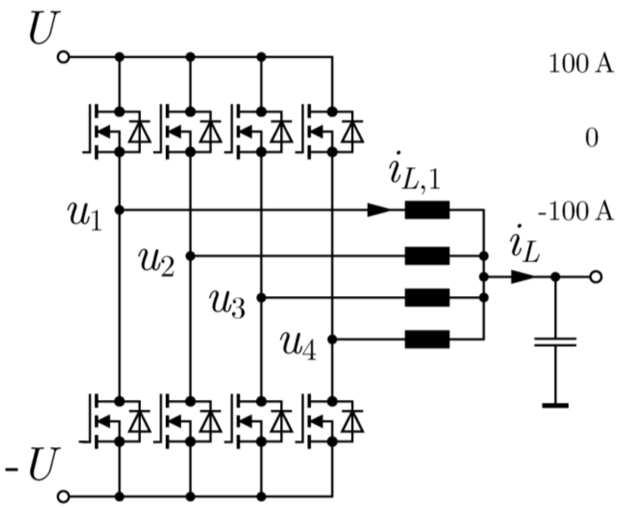
- Control Implementation Benefits from Improving Digital IC Technology
- Redundancy → Allows Large Number of Units without Impairing Reliability

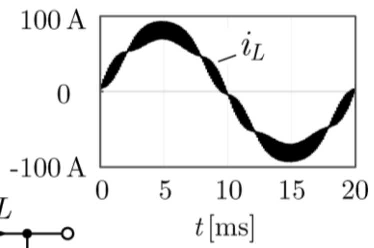
Parallel Interleaving (3)

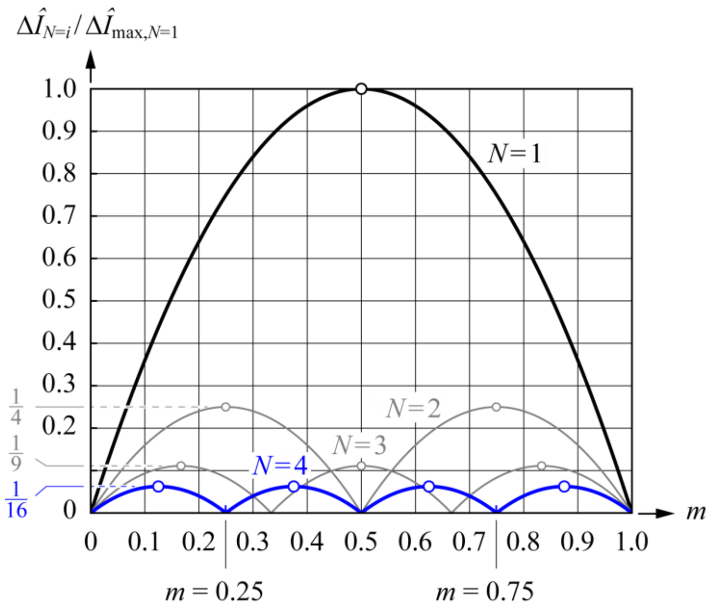
- **Output Current Ripple Cancellation**

$$\Delta\hat{I}_{\max,N=1}=\frac{U}{4f_sL} \rightarrow \Delta\hat{I}_{\max,N=4}=\frac{1}{16}\Delta\hat{I}_{\max,N=1}$$

Multiplication of Switching Frequency @ Same Switching Losses





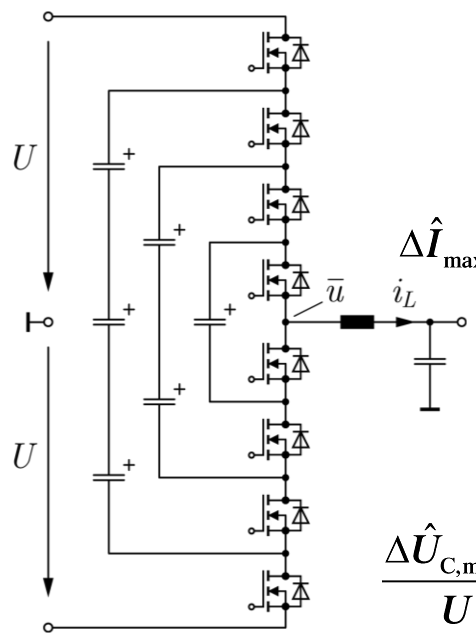


- *Massive Reduction of Filter Capacitance $C \rightarrow C/64$ – OR – Inductance $L \rightarrow L/16$*

Series Interleaving (1)

- Example of Flying Capacitor Converter

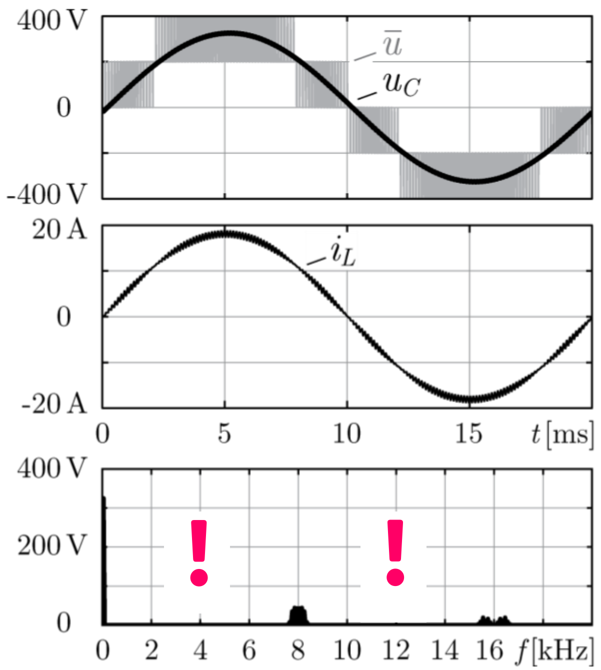
— *Breaks the Frequency Barrier*
— *Breaks the Silicon Limit 1+1=2 NOT 2^2=4 (!)*
— *Breaks Cost Barrier - Standardization*
— *Extends LV Technology to HV*



$$\Delta \hat{I}_{\max,N} = \frac{1}{N^2} \Delta \hat{I}_{\max,N=1}$$

$$\Delta \hat{I}_{\max,N=1} = \frac{U}{8 f_s L}$$

$$\frac{\Delta \hat{U}_{C,\max,N}}{U} = \frac{\pi^2}{32} \left(\frac{f_O}{f_S}\right)^2 \frac{1}{N^3}$$



- $x^{2.5}$ Dependency of $R_{DS,(on)}$ on Blocking Voltage → Adv. of Series Connection of LV MOSFETs

Series Interleaving (2)

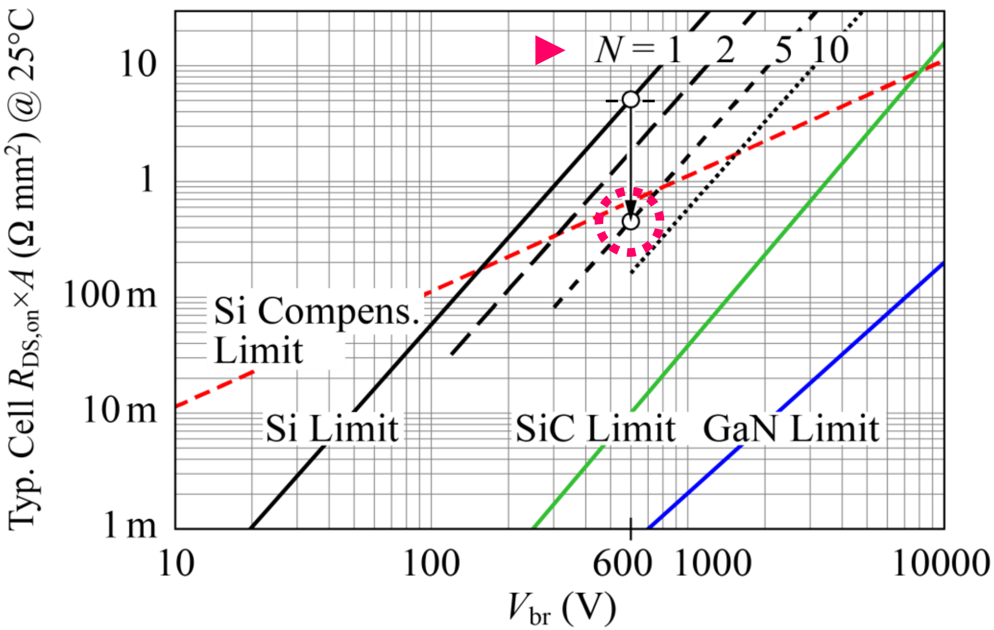
- *Series Connection of LV MOSFETs (or LV Cells) Effectively* ***BREAKS the Si-Limit*** (!)

Assumption:

Chip Area of each LV Chip Equal to the Chip Area of the HV Chip

- **Scaling of Specific On-State Resistance**

$$(R_{\mathrm{DS,on}} \times A)_{\mathrm{eff}} \approx \frac{1}{N^{1.5}} (R_{\mathrm{DS,on}} \times A)$$

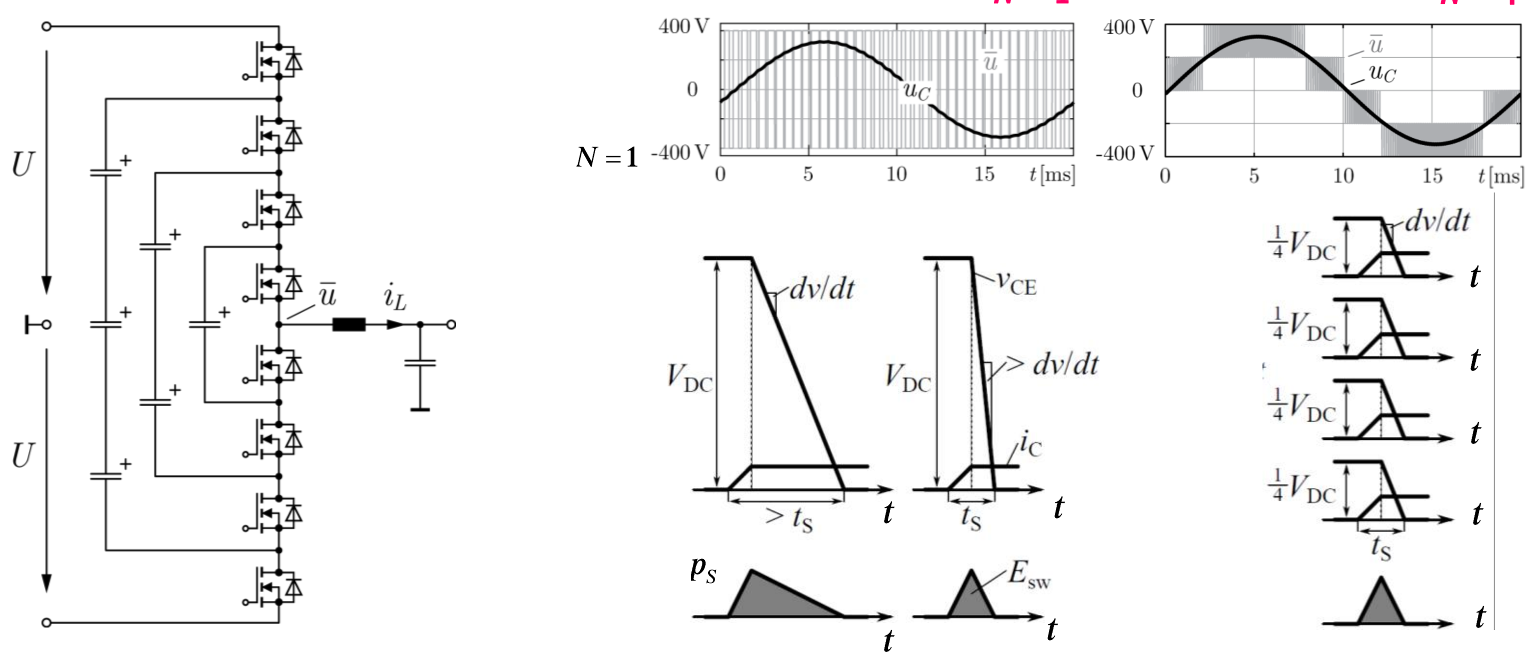


- **Excellent Concept for Building Extreme Efficiency Ultra-Compact Converters**

Series Interleaving (3)

- **Dramatically Reduced Switching Losses (or Harmonics) for Equal $\Delta i/I$ and dv/dt**

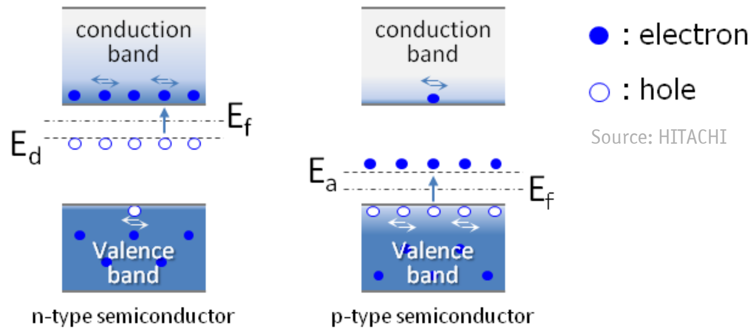
$$P_{S,N} \approx P_{S,N=1}\left(\frac{1}{2N^2} \dots \frac{1}{N^3}\right)$$



- Transistors Could Operate @ VERY Low Sw. Frequency (e.g. 20kHz) → Low Sw. Losses / High Eff.
- Alternative Operation with High Effective Sw. Frequency → Minimization of Filter Components

Components & Packaging

Wide Bandgap Semiconductors Packaging



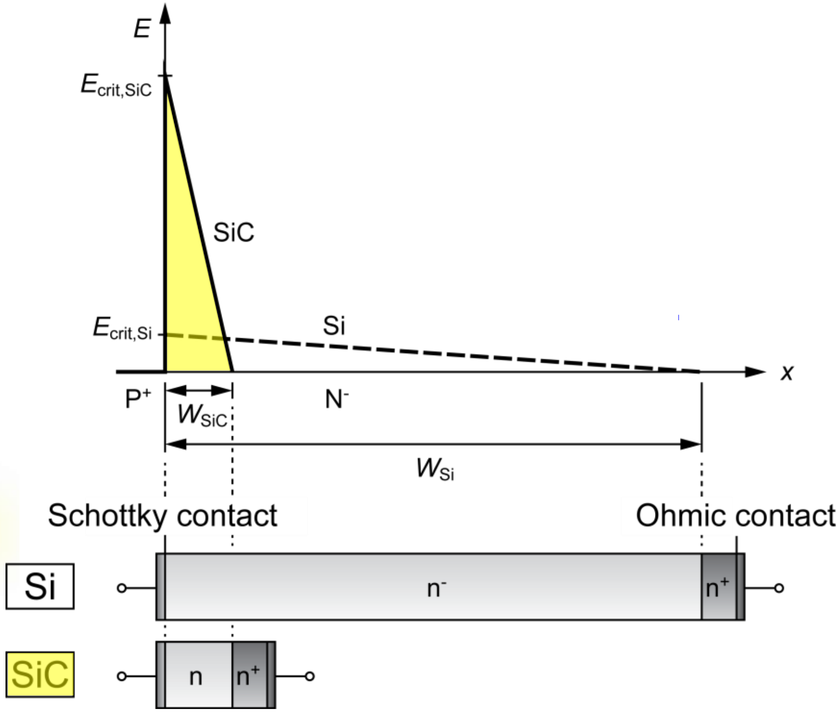
Source: HITACHI

SiC Power Semiconductors

- **Wide Band Gap / High $T_{j,max}$**
- ***High Critical E-Field of SiC → Thinner Drift Layer***

at 300 K	Si	GaAs	4H/6H-SiC	GaN
E_g (eV)	1.12	1.4	3.0-3.2	3.4
E_c (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm²/Vs)	1350	8500	100-1000	1000
ε_r	11.9	13	10	9.5
v_{sat} (cm/s)	1×10^7	1×10^7	2×10^7	3×10^7
λ (W/cmK)	1.5	0.5	3 - 5	1.3

© 2000 Carl-Mikael Zetterling



$$R_{on}^* = \frac{4V_B^2}{\varepsilon \mu_n E_C^3} \leftarrow$$

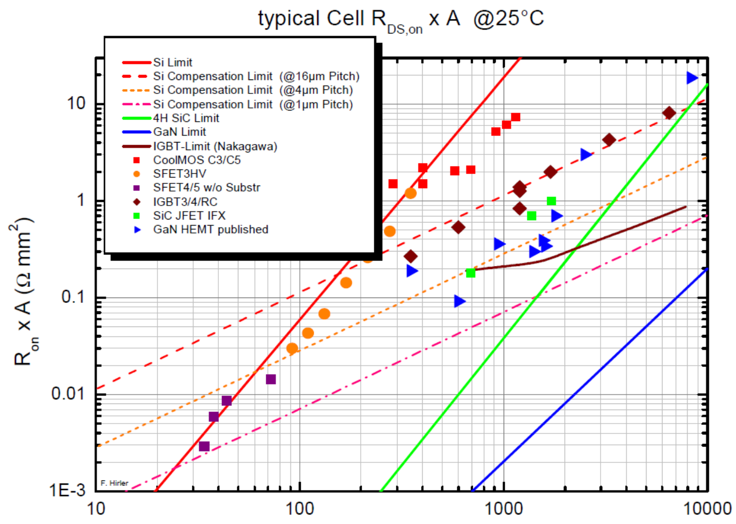
For 1kV:	Si	SiC
W (μm)	100	10
N_D (cm⁻³)	10^{14}	10^{16}

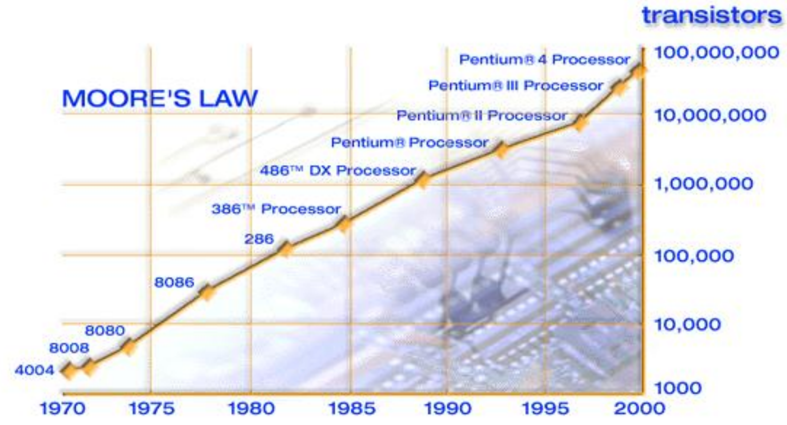
$$R_{on,SiC}^* \approx \frac{1}{300} R_{on,Si}^*$$

- *Massive Reduction of Relative On-Resistance (!) → High Blocking Voltage Unipolar Devices*

SiC & Digital Control → Technology Push

- WBG Semiconductor Technology → Higher Efficiency, Lower Complexity
- Digital Signal Processing → Fully Digital Control / Computing Power / Flexibility





→ + Advanced Packaging (!)

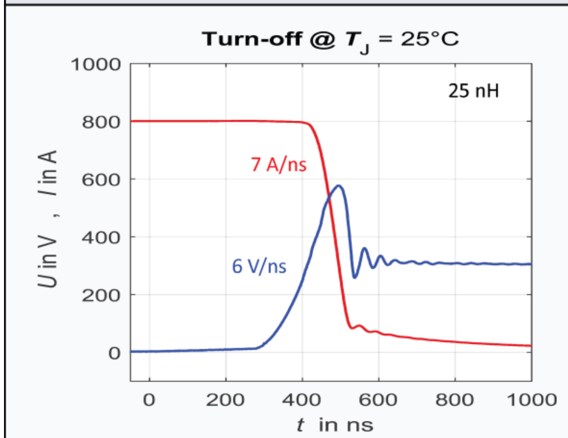
→ Moore's Law

SiC-MOSFETs vs. Si-IGBTs

- *Si-IGBT* → *Blocking Voltages up to 6.5kV / Rel. Low Switching Speed*
- *SiC-MOSFETs* → *Blocking Voltages up to 15kV (1st Samples) / Factor 10…100 Higher Sw. Speed*

Source: M. Bakran / ECPE 2019

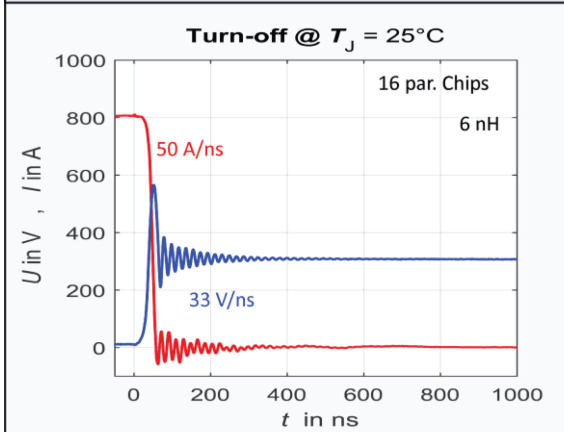
Si-IGBT / Hybrid-Pack 2



E_{off} = 45900 µJ

-> 8 kV/µs at 400V

SiC-MOSFET / (scaled for low inductance)



E_{off} = 4672 µJ

-> 44 kV/µs at 400 V

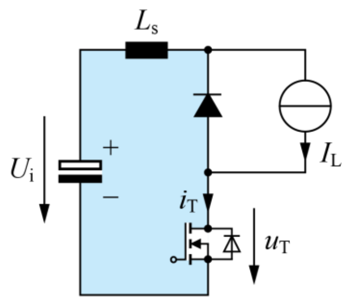
- *Extremely High di/dt & dv/dt* → *Challenges in Packaging / Motor Isolation Stress / EMI etc.*

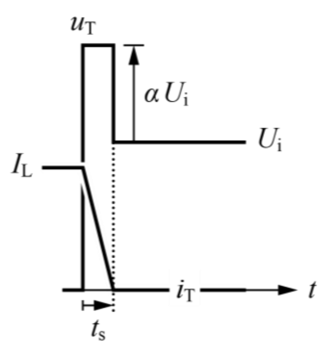
Effect of Commutation Loop Inductance

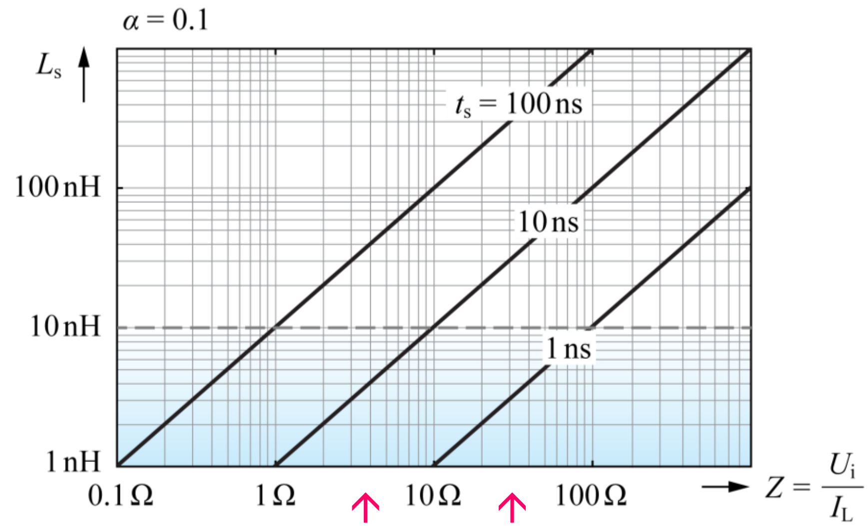
- Allowed L_s Directly Related to Switching Time t_s →

$$L_s \leq \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \frac{U_i}{I_L}$$

Z







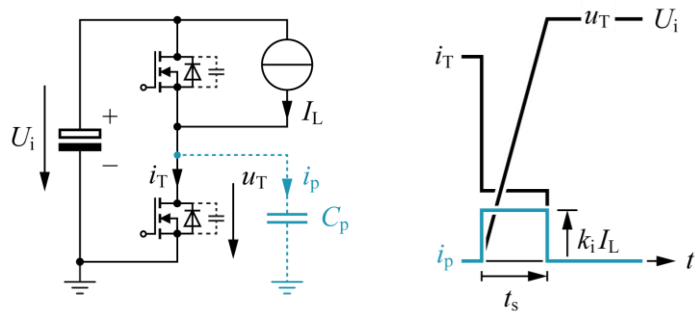
- *Parallel Interleaving Allows to Split-Up Large Currents → Increase of Z / Allows Faster Switching*

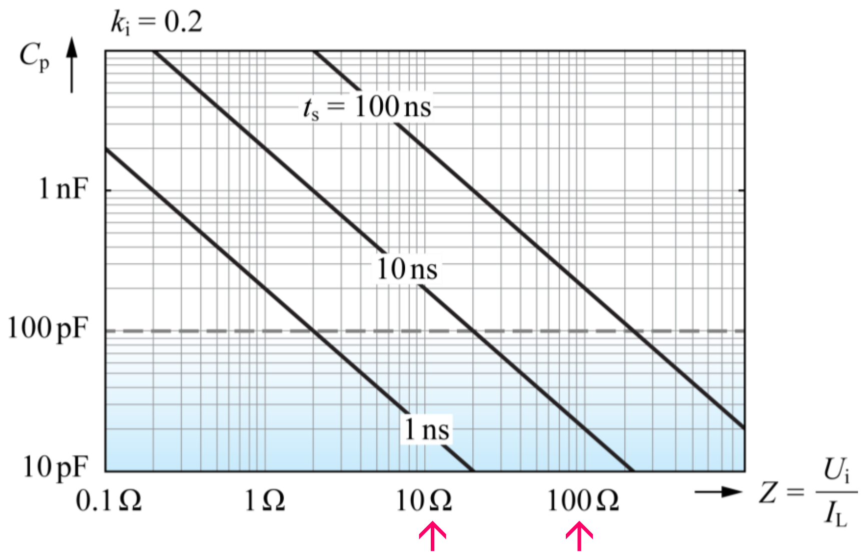
Effect of Switch-Node Capacitance

- Allowed C_p Directly Related to Switching Time t_s →

$$C_p \leq \frac{\alpha I_i}{\frac{U_i}{t_s}} = \alpha t_s \left(\frac{U_i}{I_i}\right)^{-1}$$

Z

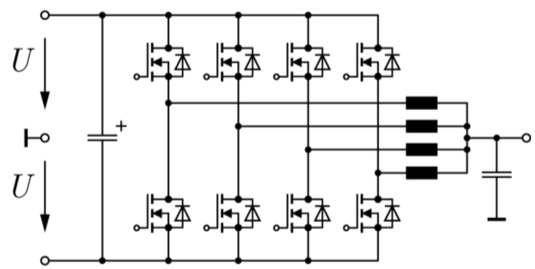


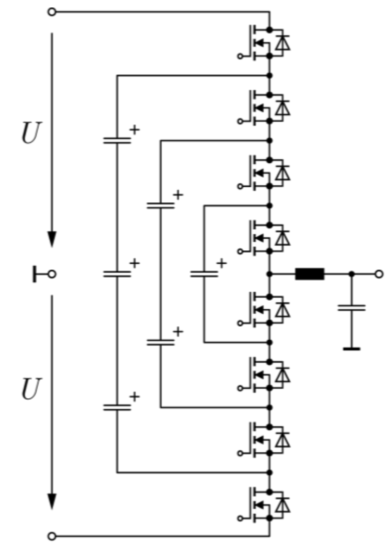


- *Series Interleaving for Split-Up of Large Voltages → Decrease of Z / Allows Faster Switching*

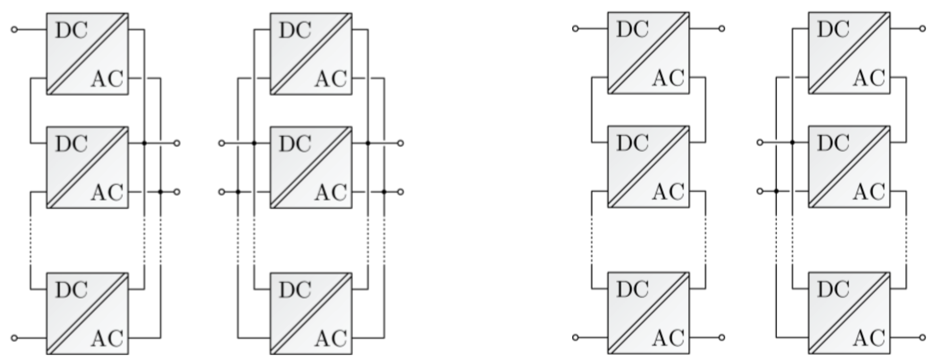
Impedance Matching

- Direct Parallel/Series Connection of Switches/Bridge-Legs
- ISOP / IPOP / ISOS / IPOS Conn. of Isol. Conv. Modules
- Also Allows Heat Spreading & Economy of Scale





- *Parallel Interleaving / Split-Up of Large Currents → Increase of Z / Allows Faster Switching*
- *Series Interleaving / Split-Up of Large Voltages → Decrease of Z / Allows Faster Switching*

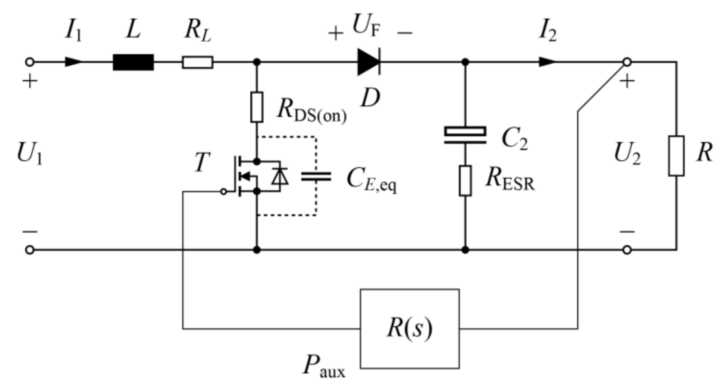


Efficiency Analysis

Loss Components
Efficiency Maximum

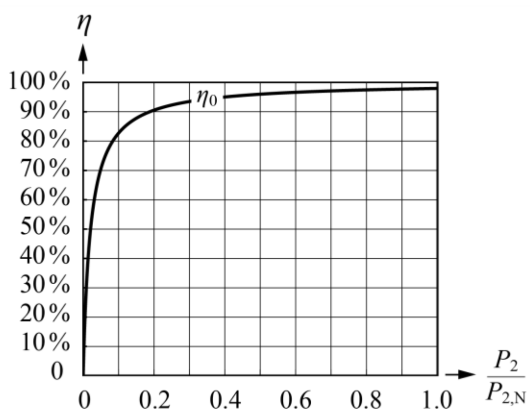
Source: www.clipground,com

Influence of Loss Components on Efficiency Characteristic

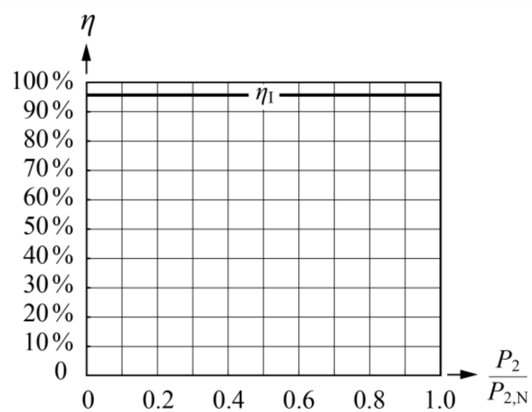


$$\eta = \frac{P_2}{P_1} = \frac{1}{1+\frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}$$

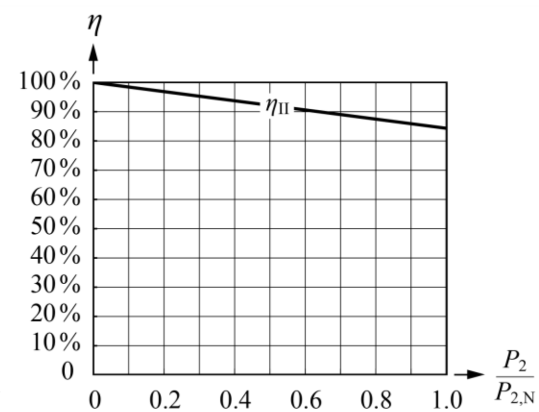
$$P_V = P_{V,O} + P_{V,I} + P_{V,II} = k_O + k_I P_2 + k_{II} P_2^2$$



... $C_{E,eq}$ MOSFET Losses
Auxiliary

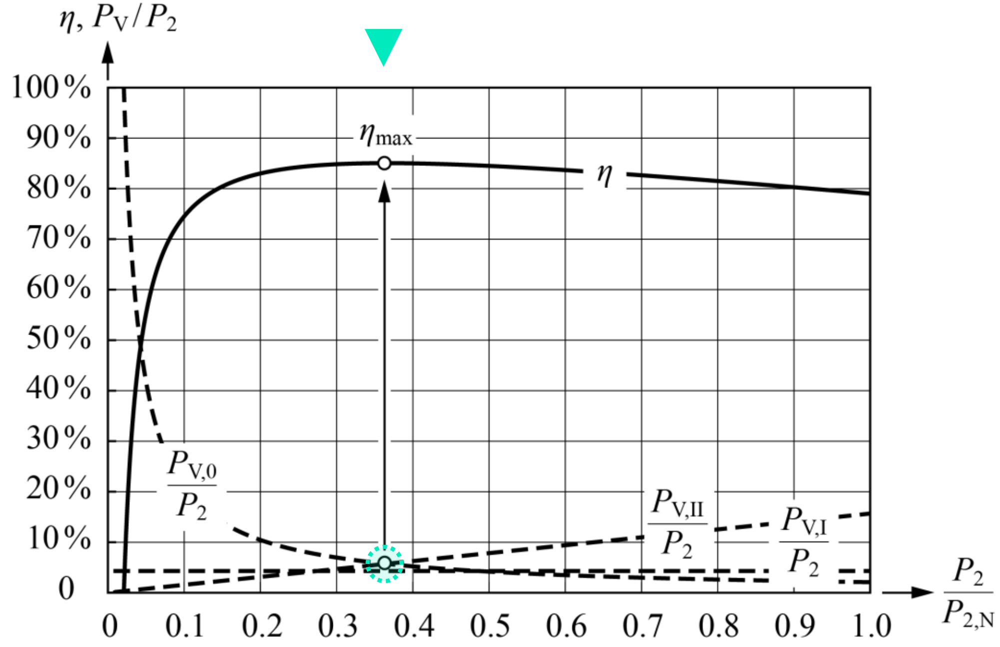


... Diodes



... $R_{DS(on)}$ MOSFET
Inductor Winding

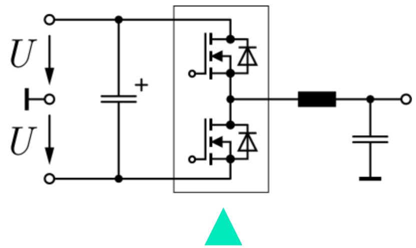
Efficiency Maximum

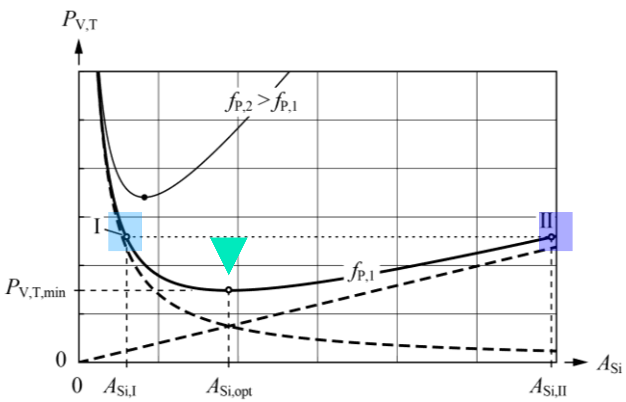


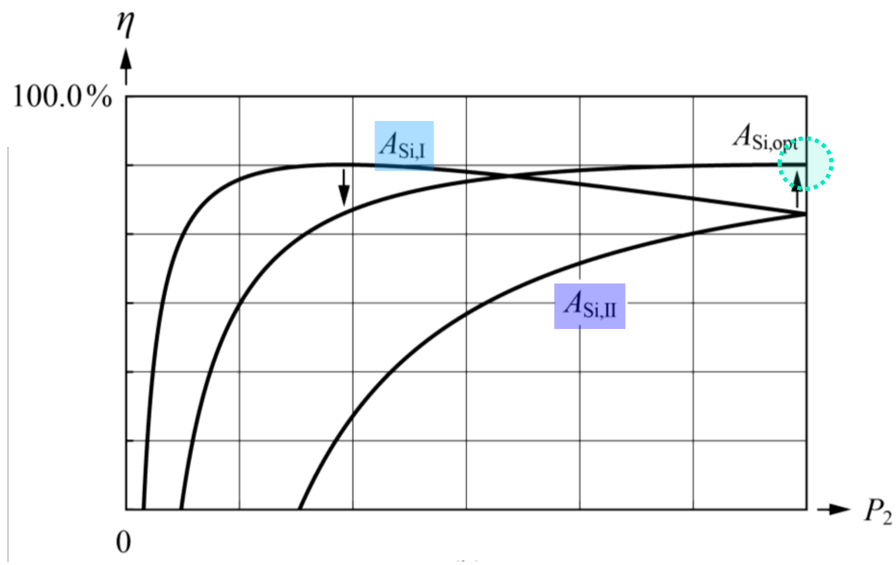
@ Maximum Efficiency: $P_{V,II} = P_{V,0}$ → Equal Const. & Quadratic Losses

Influence of Chip Area on Efficiency

- Larger Chip Area → Lower On-Resistance / Cond. Losses **BUT** Higher Cap. Sw. Losses
- *Optimal / Minimum Total Losses for Opt. Chip Area* (Dependent on Sw. Frequency)



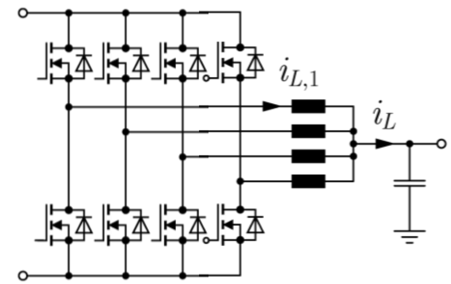




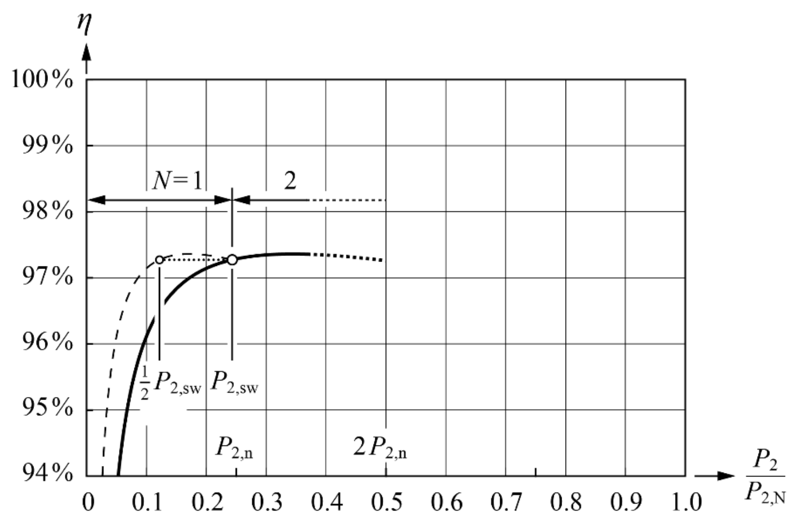
- **Part Load Efficiency Benefits from** $A_{Si} < A_{Si,opt}$

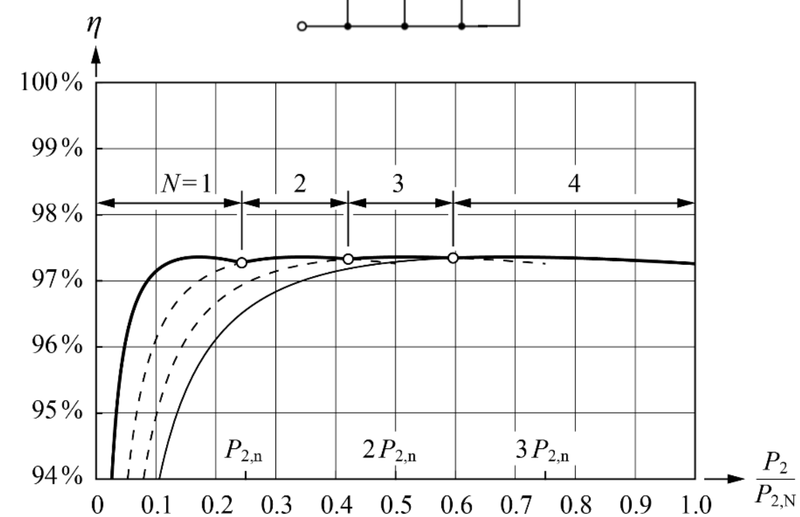
Parallel Operation of Sub-Systems

- **Efficiency Optimal Phase-Shedding**
- **Maximization of Part-Load Efficiency**



$$\eta\left\{\frac{1}{N}P_{2,sw}\right\}=\eta\left\{\frac{1}{N+1}P_{2,sw}\right\}$$





- **Features Phase-Shedding – Equiv. to Adjust. Si-Area!** → **Part Load Efficiency**
- **Features Cancellation of Harmonics** → **Power Density & Efficiency**

Heat Sink Properties

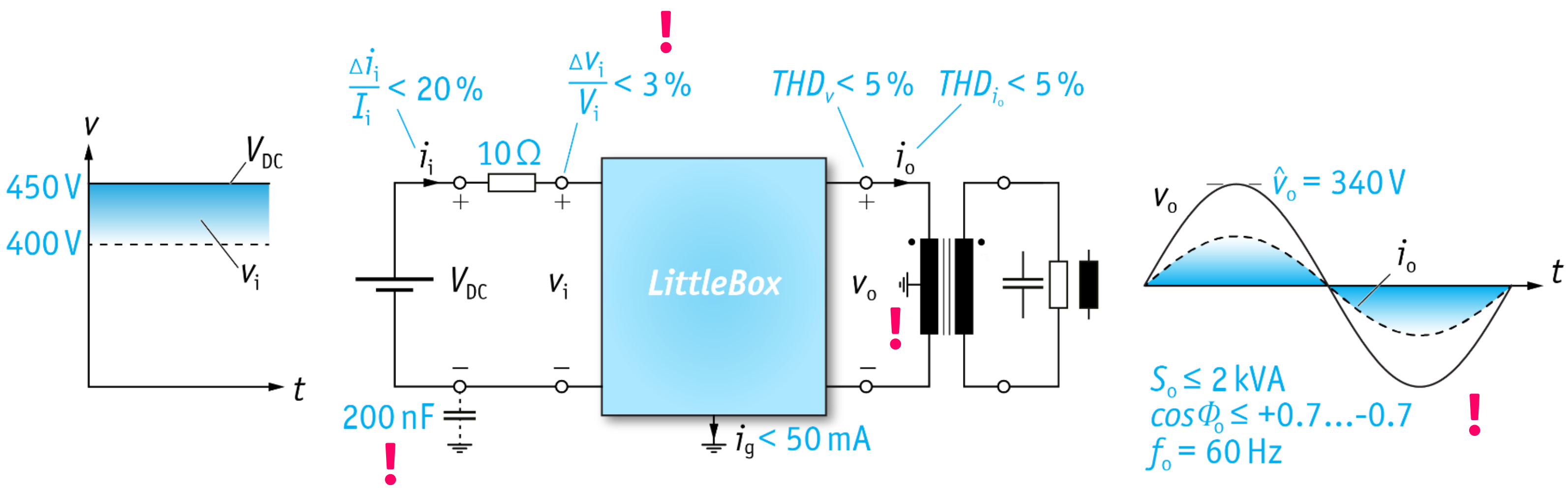
Loss-Determined
Power Density Limit

Source: www.seton.com

LiTTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



- Push the Forefront of New Technologies in R&D of High Power Density Inverters

The Grand Prize

- Highest Power Density (> 50W/in^3)
- Highest Level of Innovation

$1,000,000

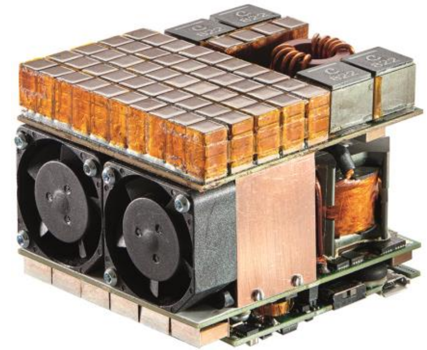
- Timeline
  - Challenge Announced in Summer 2014
  - 2000+ Teams Registered Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - 18 Finalists (3 No-Shows)

Power Density Limit Due to Cooling

- **Max. Possible Power Density Def. by Heatsink Volume**

$$\rho_{max} = \frac{P_O}{Vol_{HS}}$$

★ Google
Little-Box 2.0
240 W/in^3



- **Cooling System Performance Index (CSPI)**
  - **Highest Performance Fan**
  - **Fin Thickness / Channel Width Optimization**
  - **Maximum Thermal Conductance / Volume**

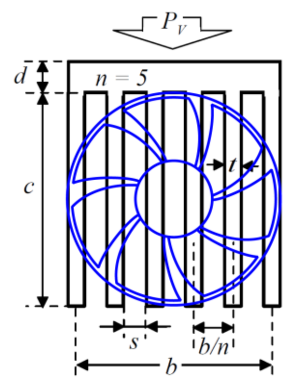
$$CSPI = \frac{G_{th}}{Vol_{HS}} \rightarrow \text{Max}$$

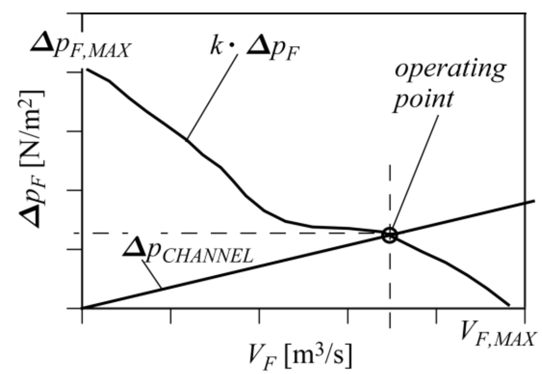
$$Vol_{HS} = \frac{G_{th}}{CSPI} = \frac{\frac{P_{loss}}{\Delta T_{s-a}}\left[\frac{\text{W}}{\text{K}}\right]}{CSPI}$$

- **Eff.-Dependent Power Density Limit**

$$P_{loss} = (1-\eta)P_i = \frac{(1-\eta)}{\eta}P_O$$

$$\rho_{max} = \frac{\eta}{(1-\eta)}\Delta T_{s-a} CSPI\left[\frac{\text{W}}{\text{dm}^3}\right]$$



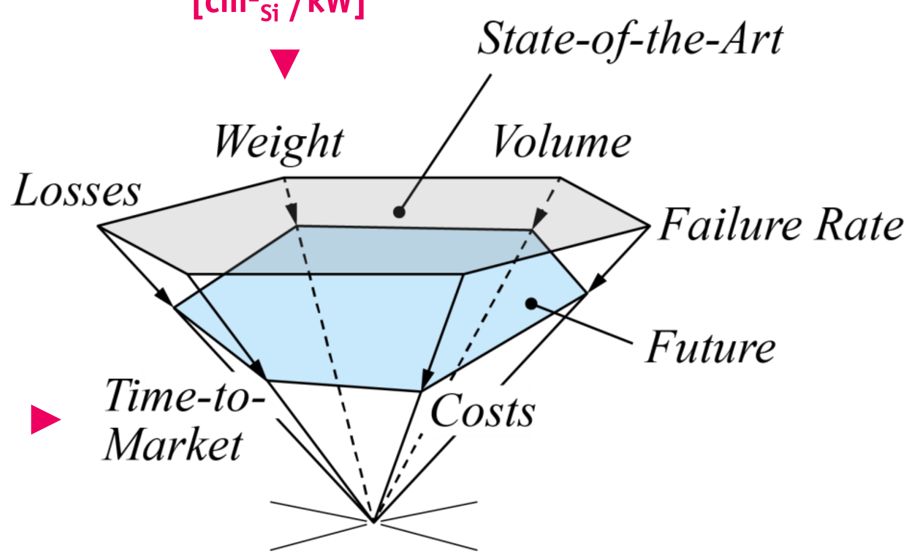


Multi-Objective Optimization

Abstraction of Converter Design
Design Space / Performance Space
Pareto Front
Sensitivities / Trade-Offs

Required Performance Improvement

Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

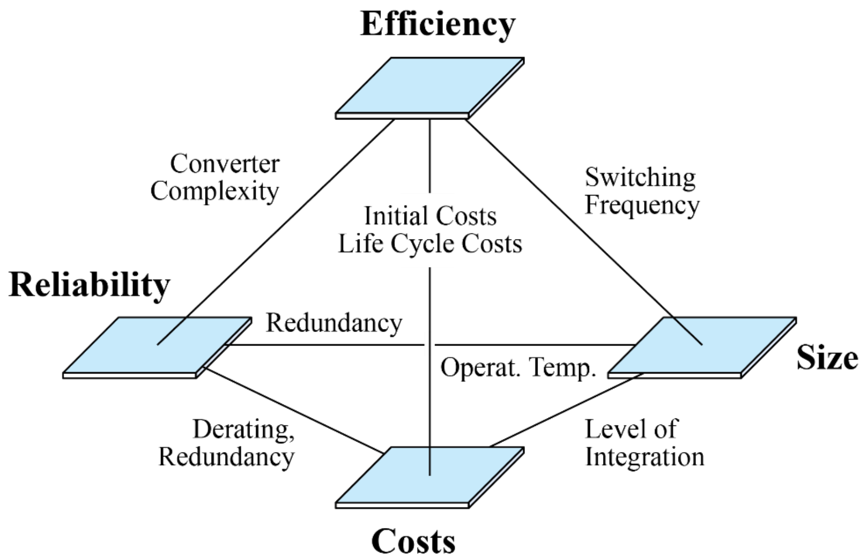


- **Performance Indices**

  - Power Density [kW/dm³]
  - Power per Unit Weight [kW/kg]
  - Relative Costs [kW/$]
  - Relative Losses [%]
  - Failure Rate [h^{-1}]

Multi-Objective Design Challenge (1)

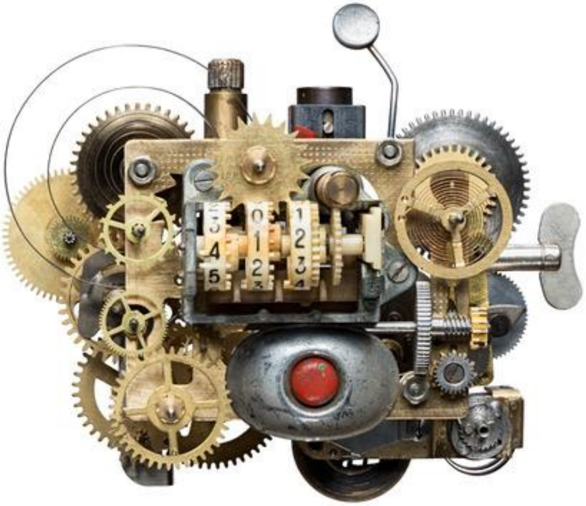
- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices → Trade-Offs



- Large Number of Degrees of Freedom / Multi-Dimensional Design Space
- Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

Multi-Objective Design Challenge (2)

- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices → Trade-Offs

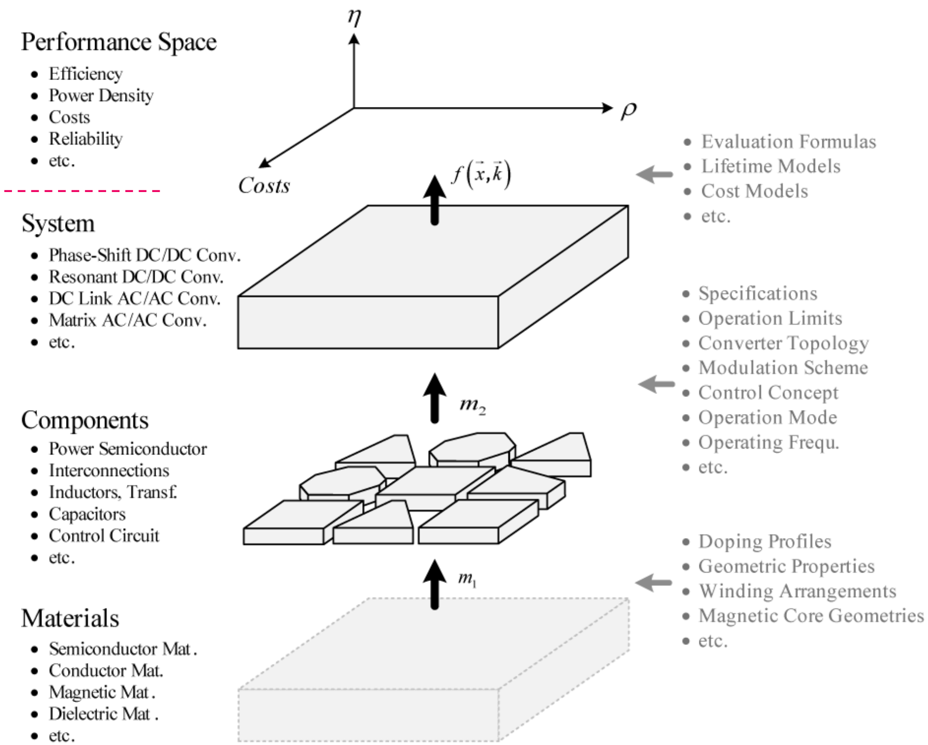


- Large Number of Degrees of Freedom / Multi-Dimensional Design Space
- Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

Abstraction of Power Converter Design

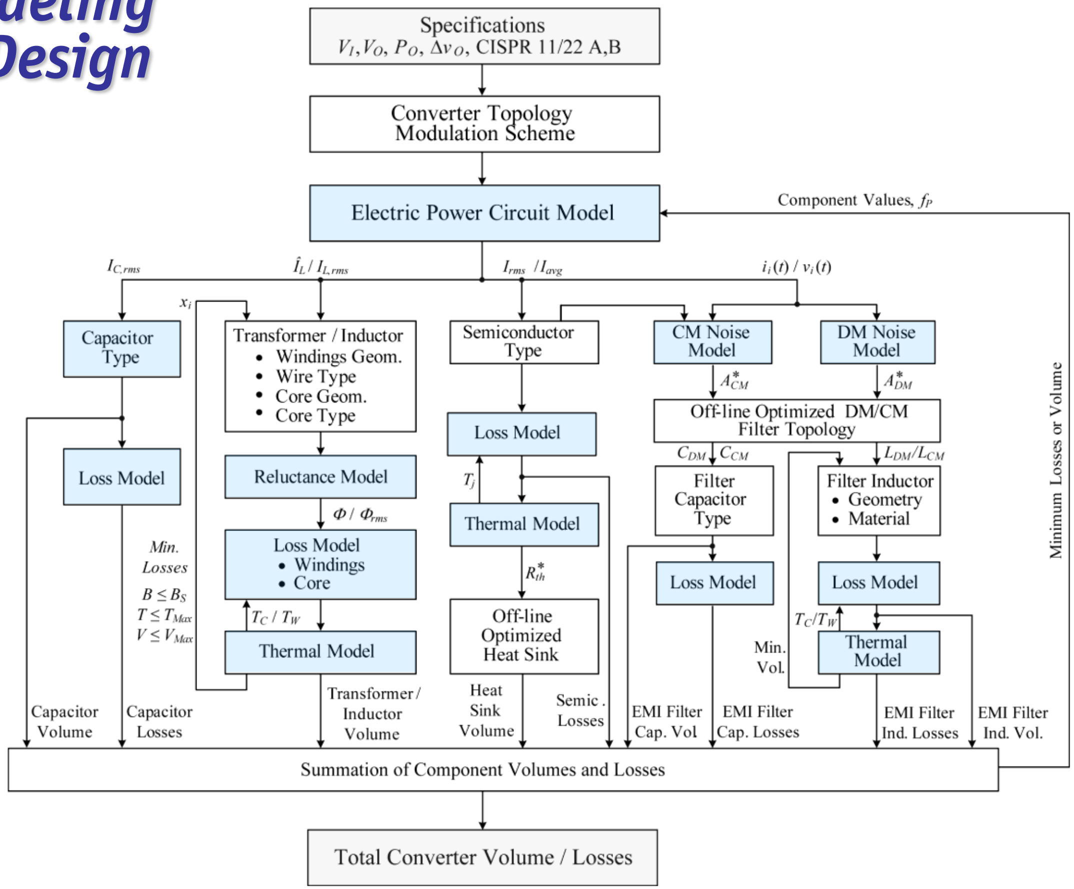
Performance Space

Design Space



- *Mapping* **of "*Design Space*" into System "*Performance Space*"**

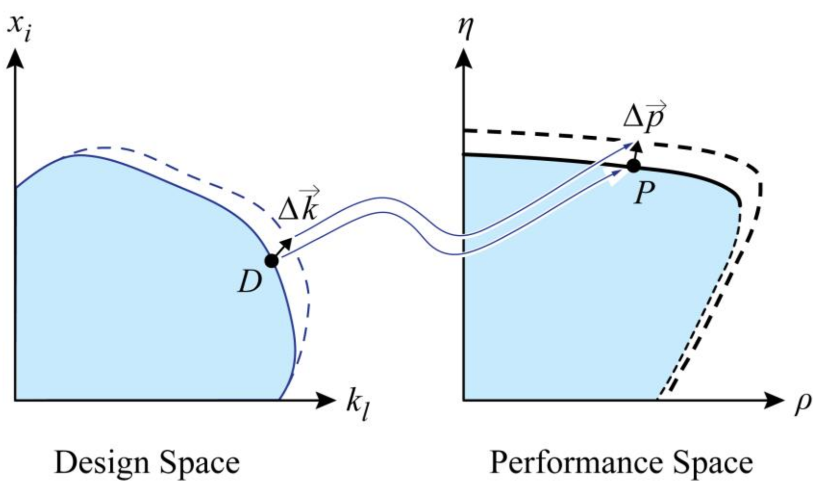
Mathematical Modeling of the Converter Design

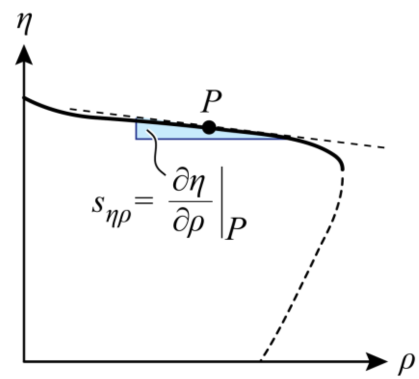


- **Multi-Objective Optimization** – ***Guarantees Best Utilization of All Degrees of Freedom*** **(!)**

Multi-Objective Optimization (1)

- Ensures Optimal Mapping of the "Design Space" into the "Performance Space"
- Identifies Absolute Performance Limits → Pareto Front / Surface



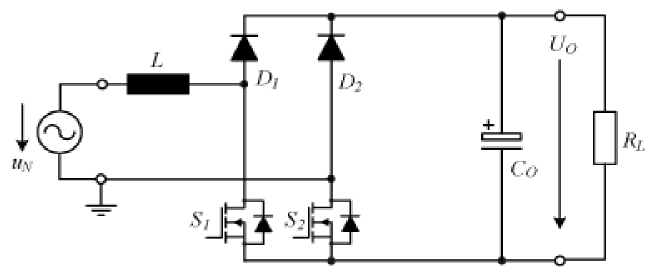


- Clarifies Sensitivity $\Delta\vec{p} / \Delta\vec{k}$ to Improvements of Technologies
- Trade-off Analysis

Determination of the η-ρ-Pareto Front (a)

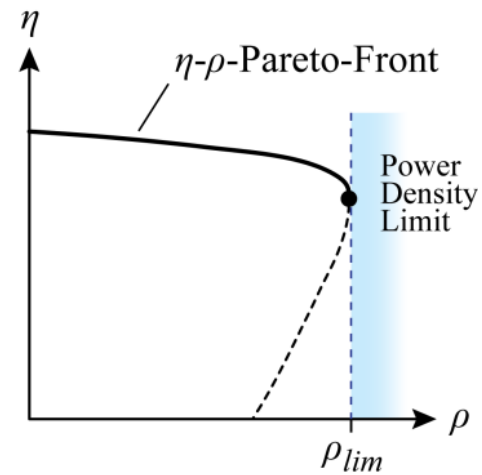
- **Comp.-Level Degrees of Freedom of the Design**

— Core Geometry / Material
— Single / Multiple Airgaps
— Solid / Litz Wire, Foils
— Winding Topology
— Natural / Forced Conv. Cooling
— Hard-/Soft-Switching
— Si / SiC
— etc.
— etc.
— etc.



- **System-Level Degrees of Freedom**

— Circuit Topology
— Modulation Scheme
— Switching Frequ.
— etc.
— etc.



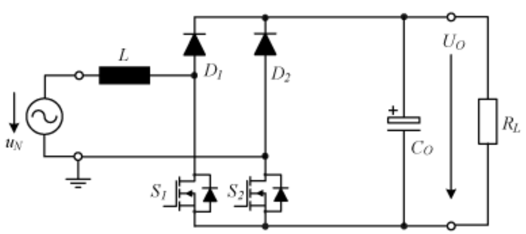
- **Only η-ρ-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)**

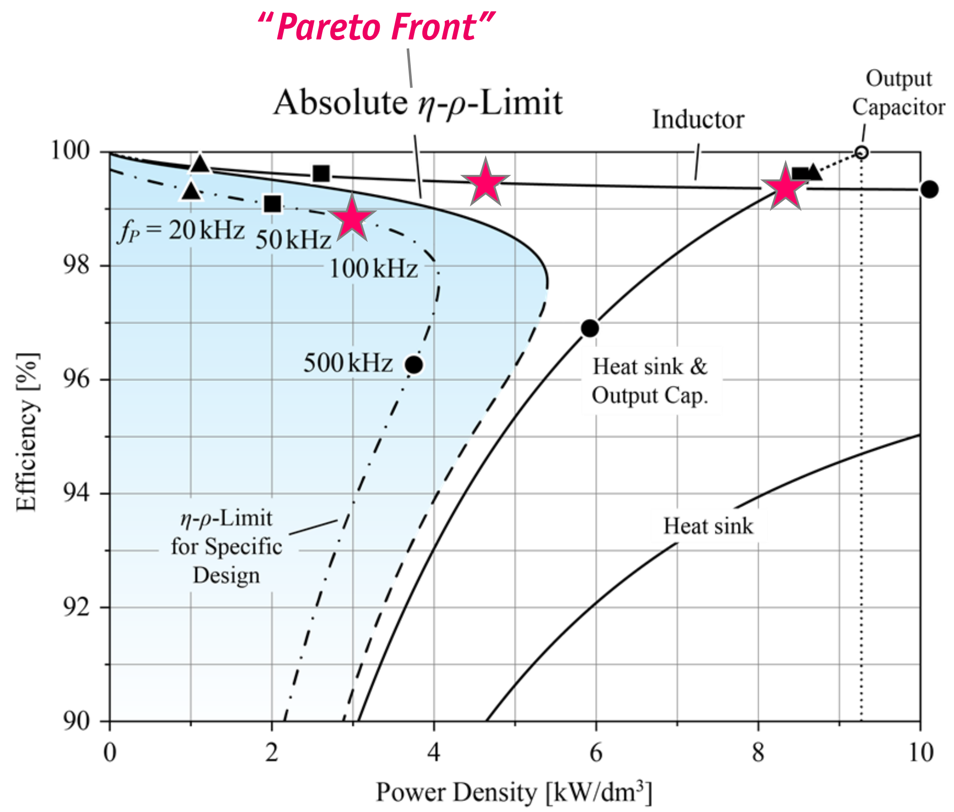
Determination of the η-ρ-Pareto Front (b)

- Example: Consider Only f_P as Design Parameter

- Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute η-ρ-Performance Limit

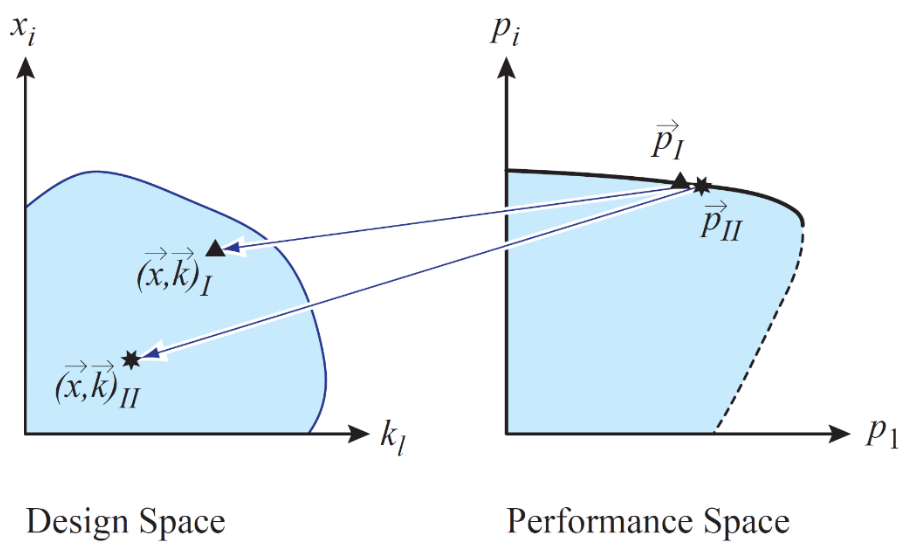
★ f_P =100kHz





Multi-Objective Optimization (2)

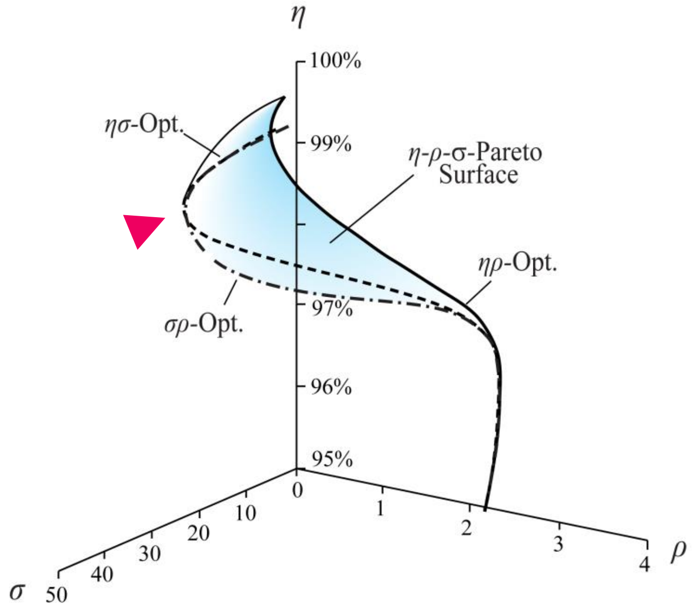
- Design Space Diversity
- Equal Performance for Largely Different Sets of Design Parameters

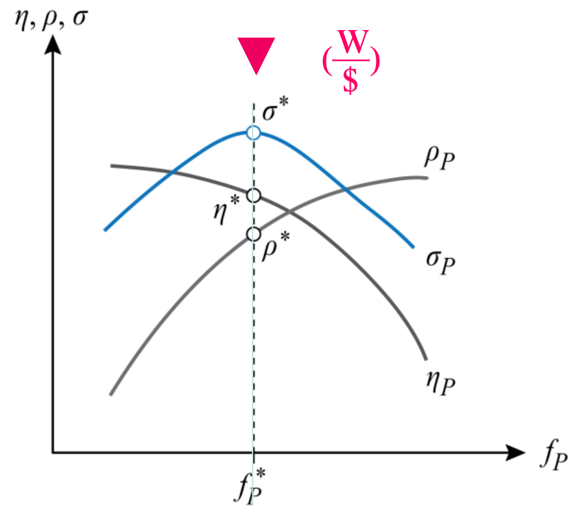


- E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)
- Allows Optimization for Further Performance Index (e.g. Costs)

Converter η-ρ-σ-Pareto Surface (1)

- Pareto Front / Surface Used for Performance Evaluation
- Definition of a Power Electronics *"Technology Node"* → ($\eta^*, \rho^*, \sigma^*, f_P^*$)
- Maximum σ [kW/$], Related Efficiency & Power Density

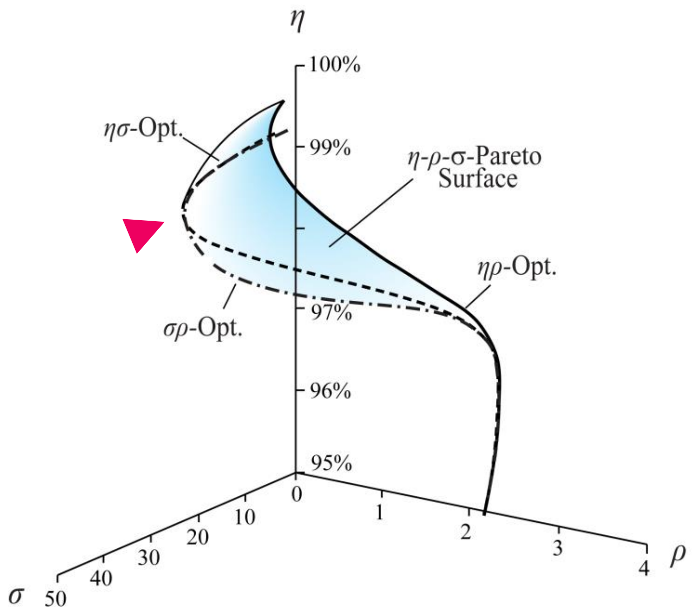


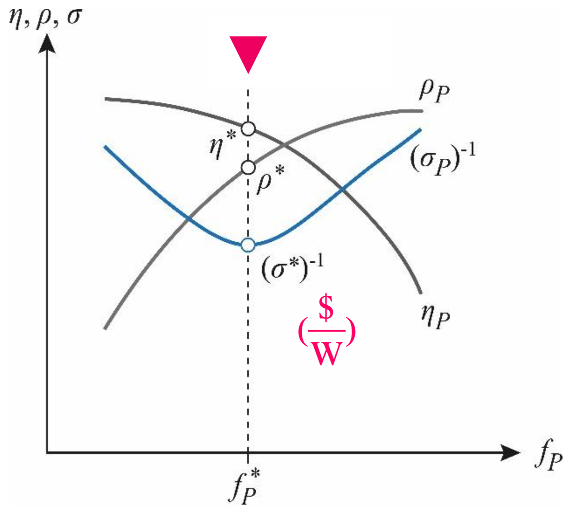


- Specifying Only a Single Performance Index is of No Value (!)
- Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)

Converter η-ρ-σ-Pareto Surface (2)

- Pareto Front / Surface Used for Performance Evaluation
- Definition of a Power Electronics *"Technology Node"* → ($\eta^*, \rho^*, \sigma^*, f_P^*$)
- Maximum σ [kW/$], Related Efficiency & Power Density



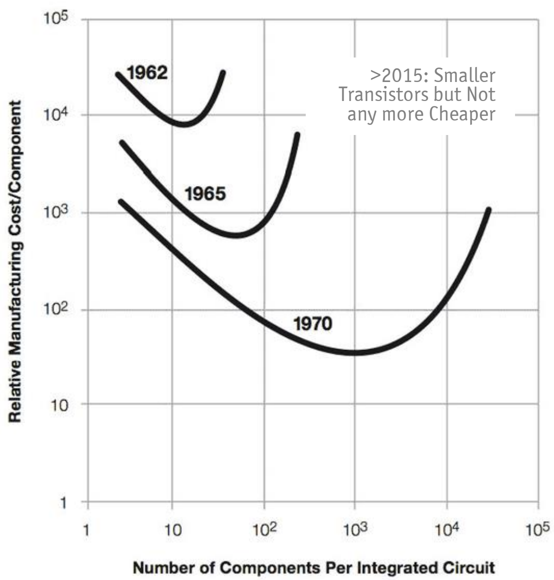


- Specifying Only a Single Performance Index is of No Value (!)
- Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)

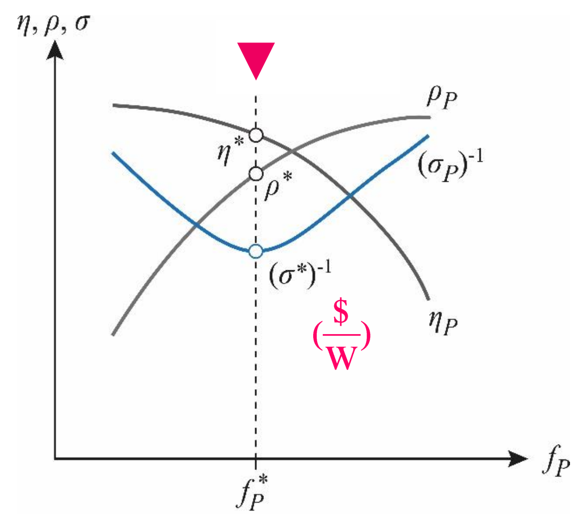
Remark — Comparison to "Moore´s Law"

- "Moore´s Law" Defines Consecutive Techn. Nodes Based on Min. Costs per Integr. Circuit (!)
- *Number of Transistors* (Density @ Minimum Costs) *Doubles Every 2 Years*

Economy of Scale → ← Lower Yield



Gordon Moore: The Future of Integrated Electronics, 1965 (Consideration of Three Consecutive Technology Nodes)



- Definition of "$\eta^*, \rho^*, \sigma^*, f_P^*$–Node" Must Consider Conv. Type / Operating Range etc. (!)

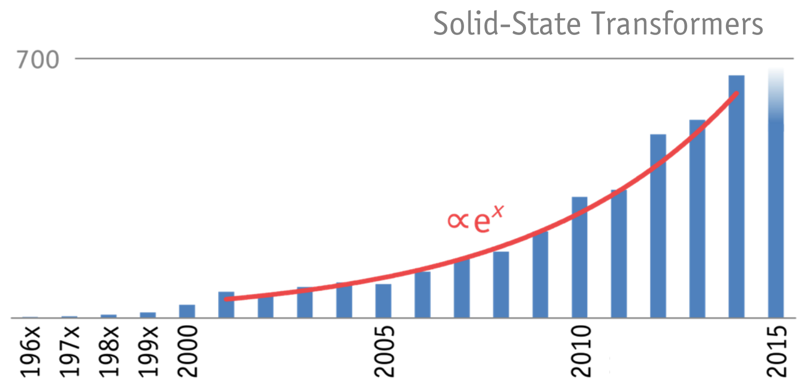
Technology Development Characteristics

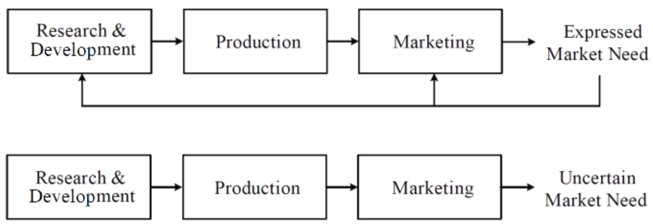
Hype Cycle
S-Curve / Disruption
Learning Curve

Source: www.clipart-library.com

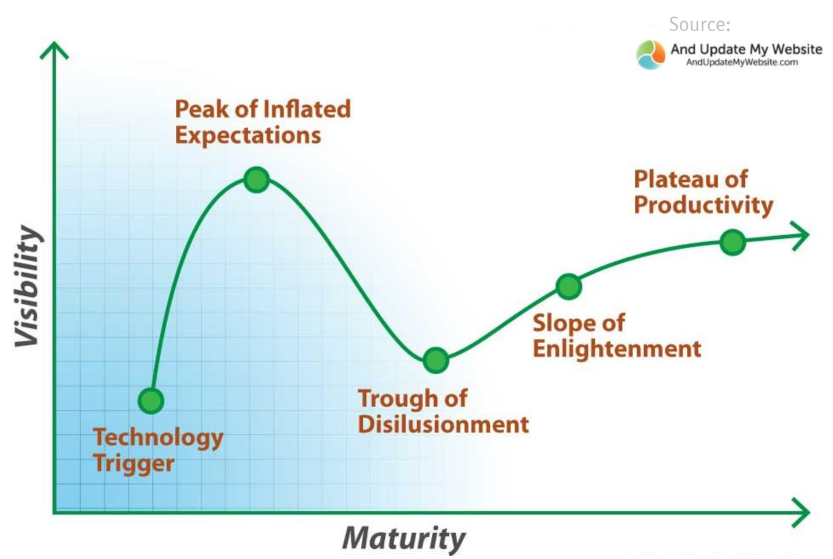
Hype-Cycle of Technologies

- Innovations are Driven by "Demand Pull" and "Technology Push"
- New Technologies are "Enablers" → Technology Roadmaps
- Initially Overexpected Importance of New Technologies Due to Exp. Increasing # of Publications (Positive Feedback) etc.



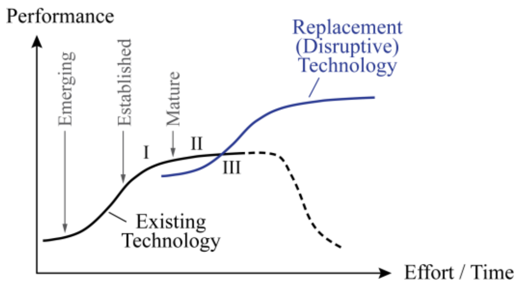


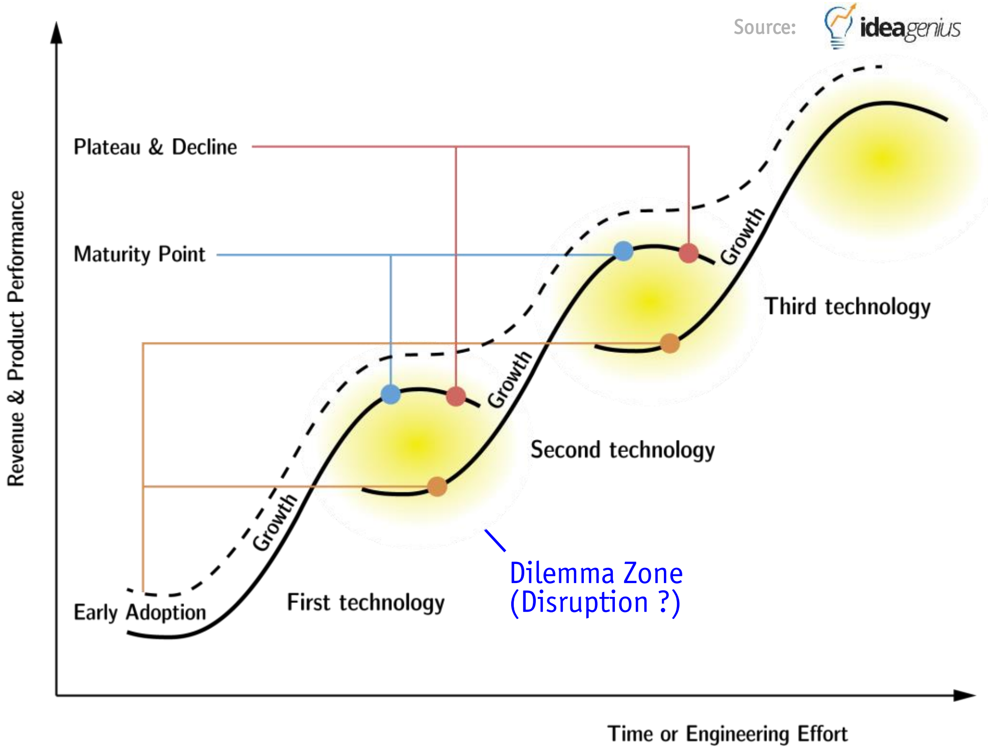
- *New Technology → ? of "Killer" Application*



S-Curve Pattern of Innovation

- Technologies Show Predictable Cycle of Adoption / Growth / Maturity (S-Curve)
- Breakthrough Inventions → More Ideal Way of Delivering an Existing Function

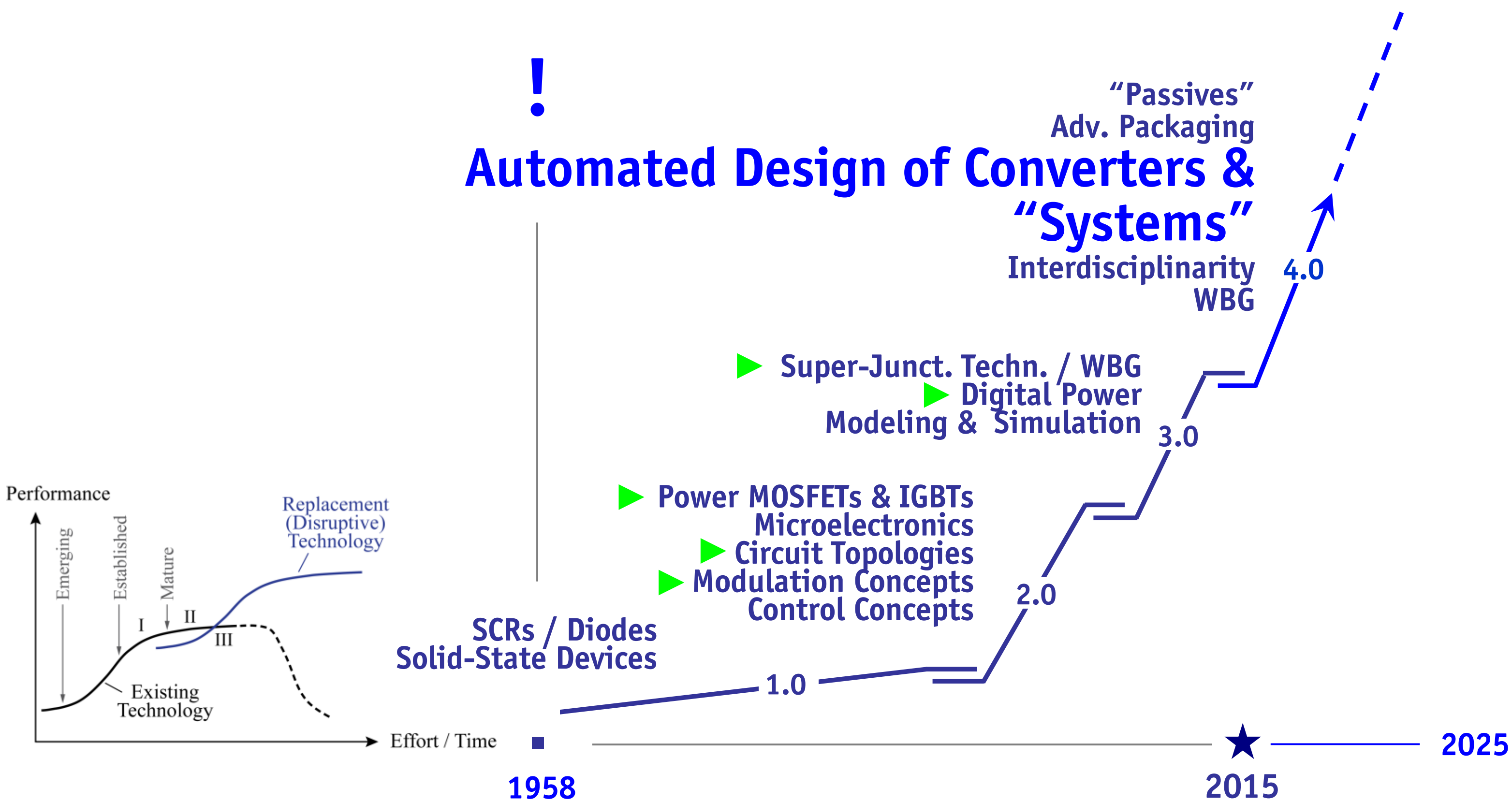




- *Evolution of Systems Driven by S-Curves of All Core Technologies*

S-Curve of Power Electronics

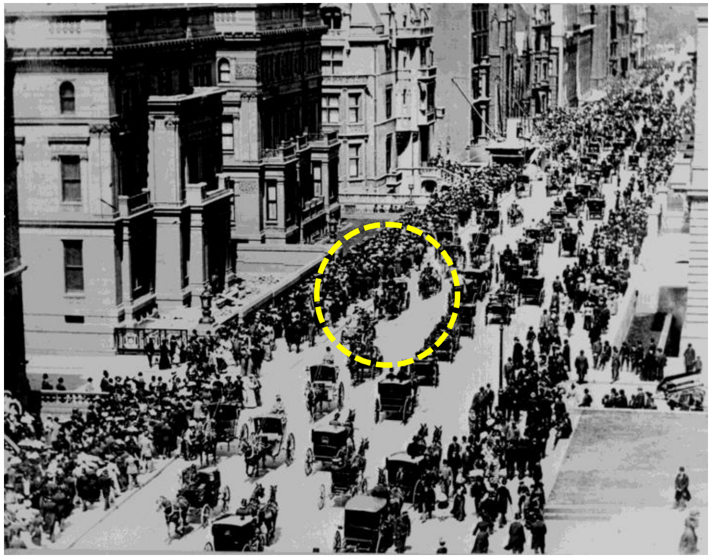
- Power Electronics 1.0 → 4.0



Disruptive Innovations

- Example — Rapid Change of Transportation Enabled by New Technology (ICE) & Business Model
  Tony Seba: "All New Vehicles, Globally, will be Electric by 2030"

— NY City, 5th Av., Easter Parade → Year 1900: One Motor Cycle / Year 1913: One Horse & Carriage (!)

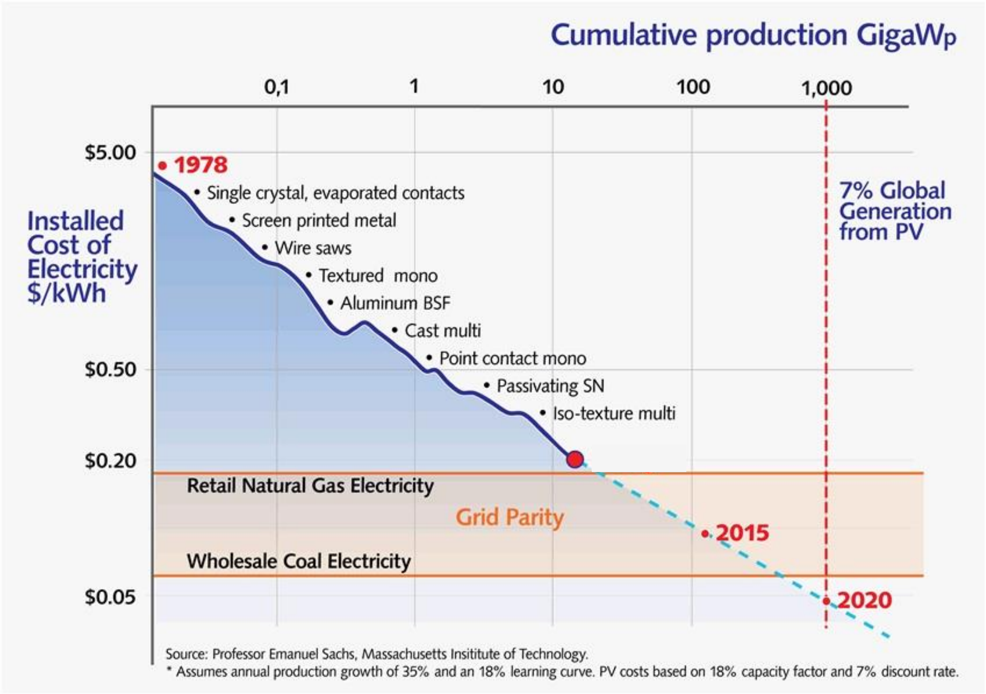


Source: Tony Seba

- Further Examples - Digital / Analogue Photography, VHS Cassette Tape System / DVD etc.
- *The Stone Age Didn´t End for the Lack of Stone (Disrupted by Bronze Tools)*

Learning Curve of Technologies

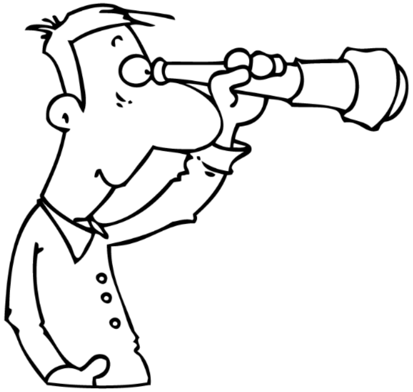
- *Analysis of the Performance Improvement as Function of Accumulated Experience*
- *Learning Rate → Improvement / Cost Reduction for Each Doubling of Cumulative Installed Capacity*



- *Typ. Learning Rate of 15...25% → Dramatic Cost Reduction over Longer Timespan*
- **Used for Prediction of Future Costs of a Technology (e.g. PV "Grid Parity") → Long Term Strategies**

Future Applications

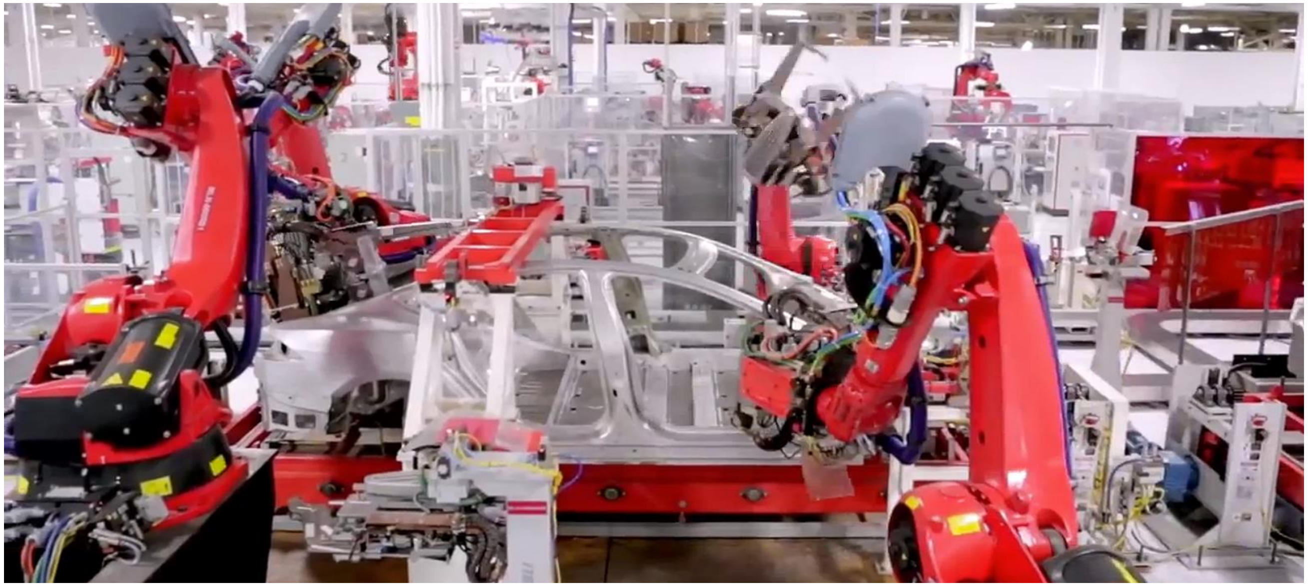
Driven by MEGATRENDS



Industry Automation / Robotics

- All Kinds of Automated Assembling
- Material Machining / Processing – Drilling, Milling, etc.
- Pumps / Fans / Compressors
- etc., etc.

Source: TESLA MOTORS



- *60% of El. Energy Used in Industry Consumed by VSDs*

Deep Green / Zero CARBON Datacenters

- Ranging from Medium Voltage to Power-Supplies-on-Chip
- Short Power Supply Innovation Cycles
- Modularity / Scalability

— Higher Availability
— Higher Efficiency
— Higher Power Density
— Lower Costs

Server-Farms
up to 450 MW
99.9999%/<30s/a
$1.0 Mio./Shutdown

Since 2006
Running Costs >
Initial Costs

33 Watts

→

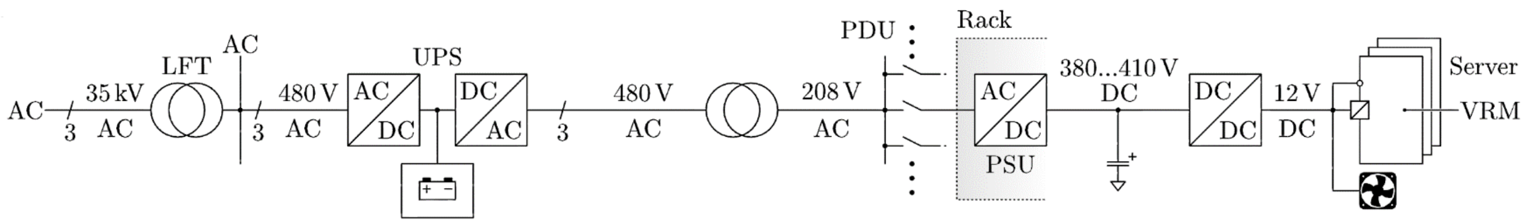
60 Watts

Source: REUTERS/Sigtryggur Ari

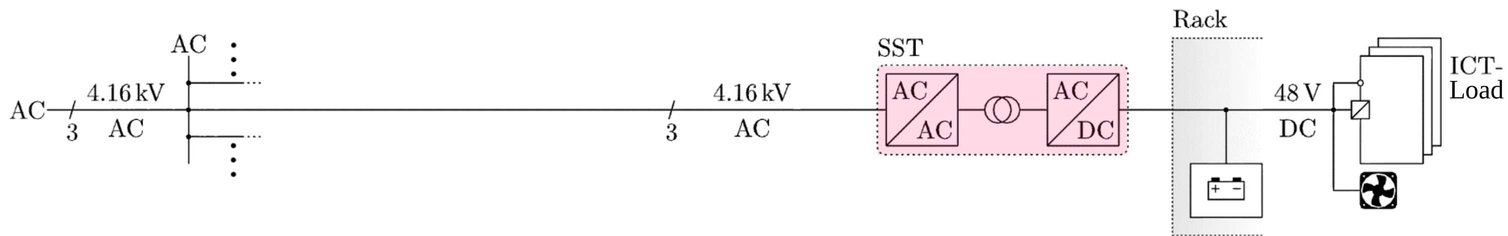
→ Future Modular Power Distribution

- Direct MV-Supply of Individual Racks Using Solid-State Transformer → 5…7% Red. in Losses
- Improves Reliability & Power Quality / Smaller Footprint

— Conventional



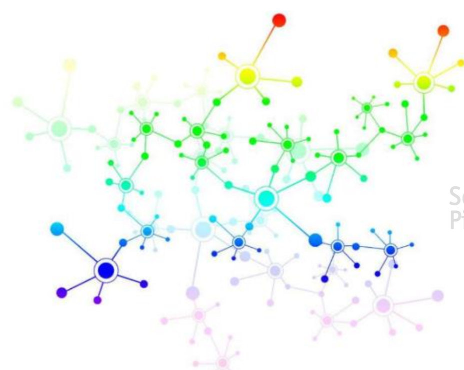
— Direct 3-Φ 6.6kV AC → 48V DC Conversion / Unidirectional SST



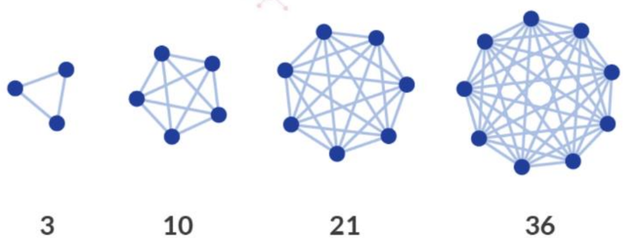
- MV → 48V → 1.2V - Only 2 Conversion Stages from MV to CPU-Level (!)

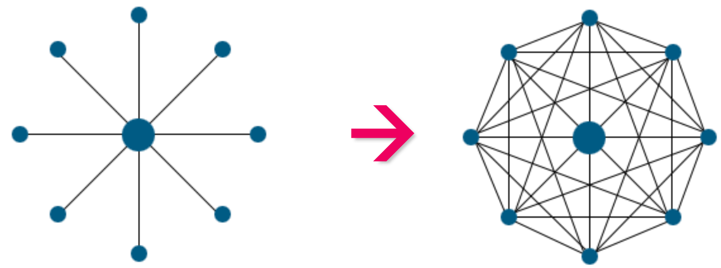
Digitalization Driver

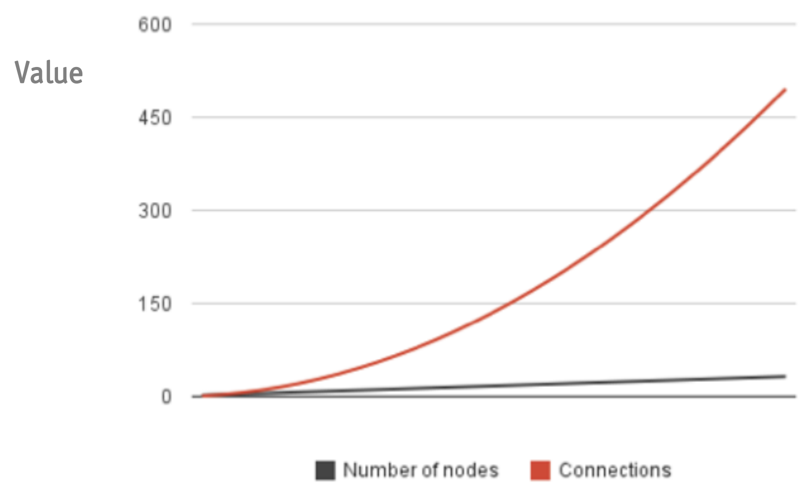
- **Metcalfe's Law**
  - Moving from Hub-Based Concept to Community Concept Increases Potential Network Value Exponentially (~n(n-1) or ~n log(n))



Source: Pixabay

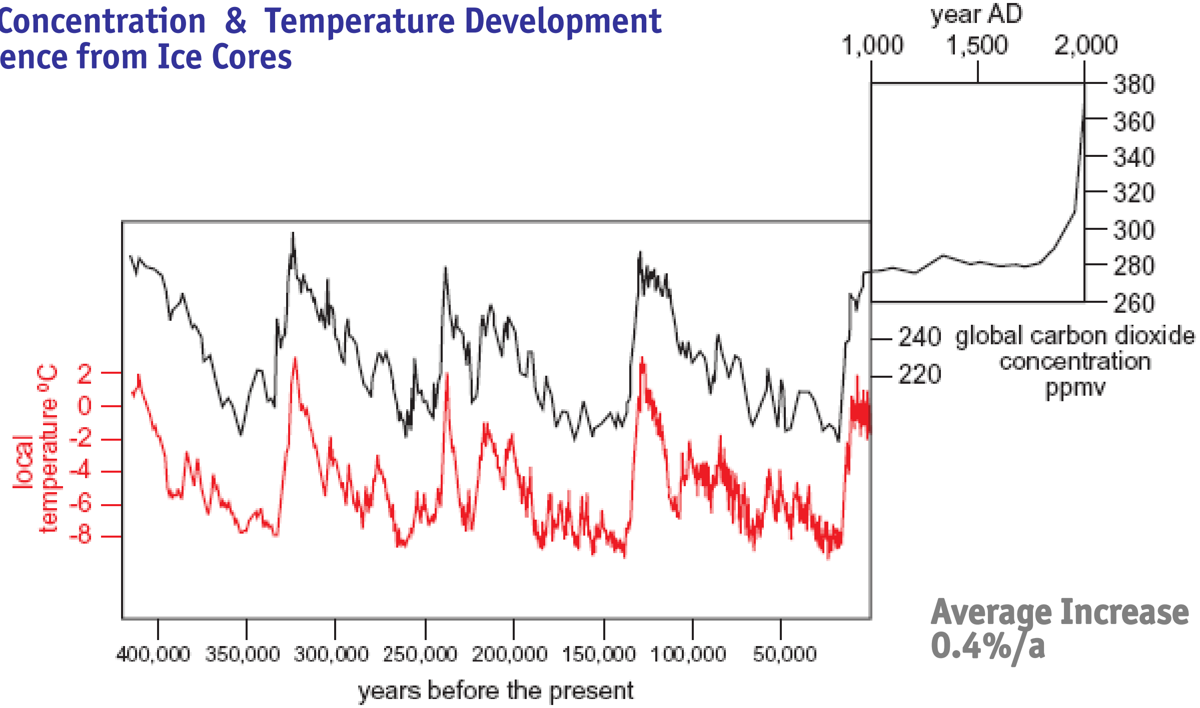






Climate Change

- CO_2 Concentration & Temperature Development
- Evidence from Ice Cores



Average Increase 0.4%/a

- Reduce CO_2 Emissions *Intensity* (CO_2/GDP) to Stabilize Atmospheric CO_2 Concentration
- 1/3 in 2050 → less than 1/10 in 2100 (AIST, Japan @ IEA Workshop 2007)

Climate Change

- CO_2 Concentration & Temperature Development
- Evidence from Ice Cores

Source: H. Nilsson
Chairman IEA DSM Program
FourFact AB

- Reduce CO_2 Emissions *Intensity* (CO_2/GDP) to Stabilize Atmospheric CO_2 Concentration
- 1/3 in 2050 → less than 1/10 in 2100 (AIST, Japan @ IEA Workshop 2007)

→ *Off-Shore Wind Farms*

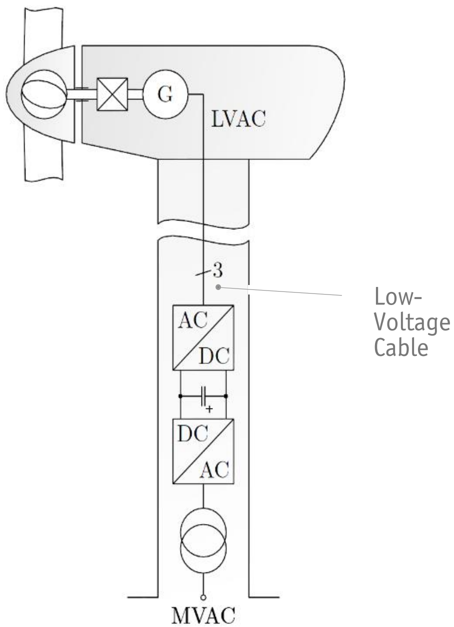
■ **Medium-Voltage (DC) Power Collection and Transmission**

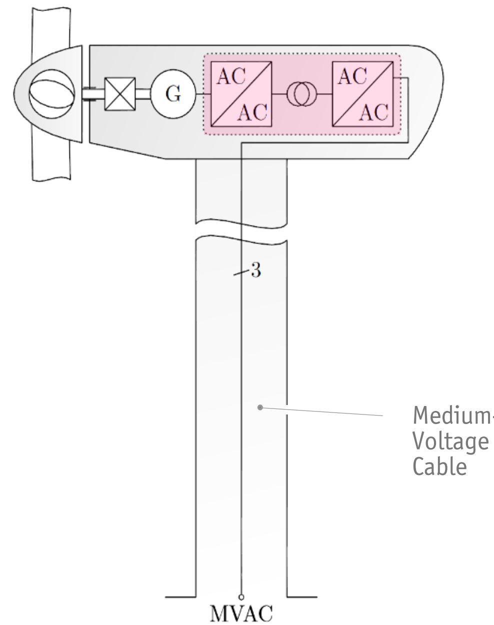
Source: M. Prahm / Flickr

- **Off-Shore Wind Farm**

→ Wind Turbine Electrical System

— Current 690V Electrical System → Significant Cabling Weight/Costs & Space Requirement
— Future Local Medium-Frequency Conv. to Medium-Voltage AC or DC

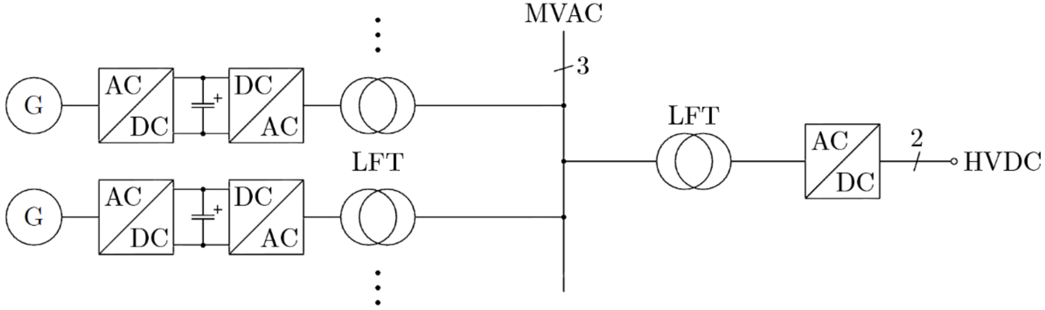




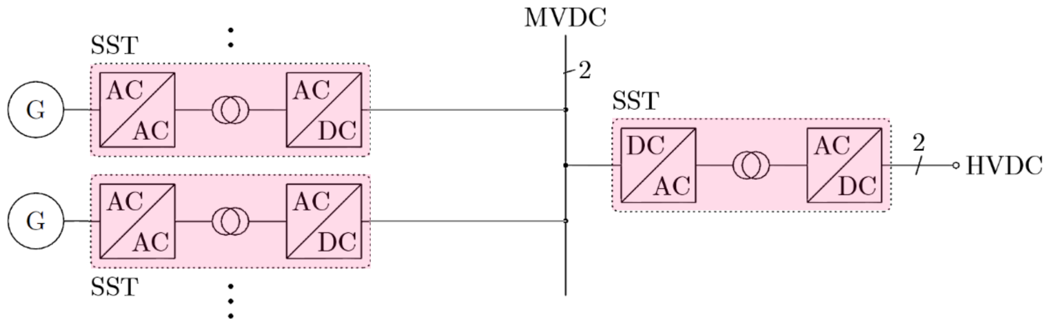
► On-Shore Wind Power System

► Future Off-Shore System

→ Off-Shore Collector-Grid Concepts



- Conventional AC Collector-Grid



- DC/DC-Interface of Wind Turbine DC Link to MVDC Collector Grid → Lower Losses (1%) & Volume
- DC/DC-Interface of MVDC Grid to HVDC Transmission → Lower Losses (1%) & Volume

→ *Utility-Scale Solar Power Plants*

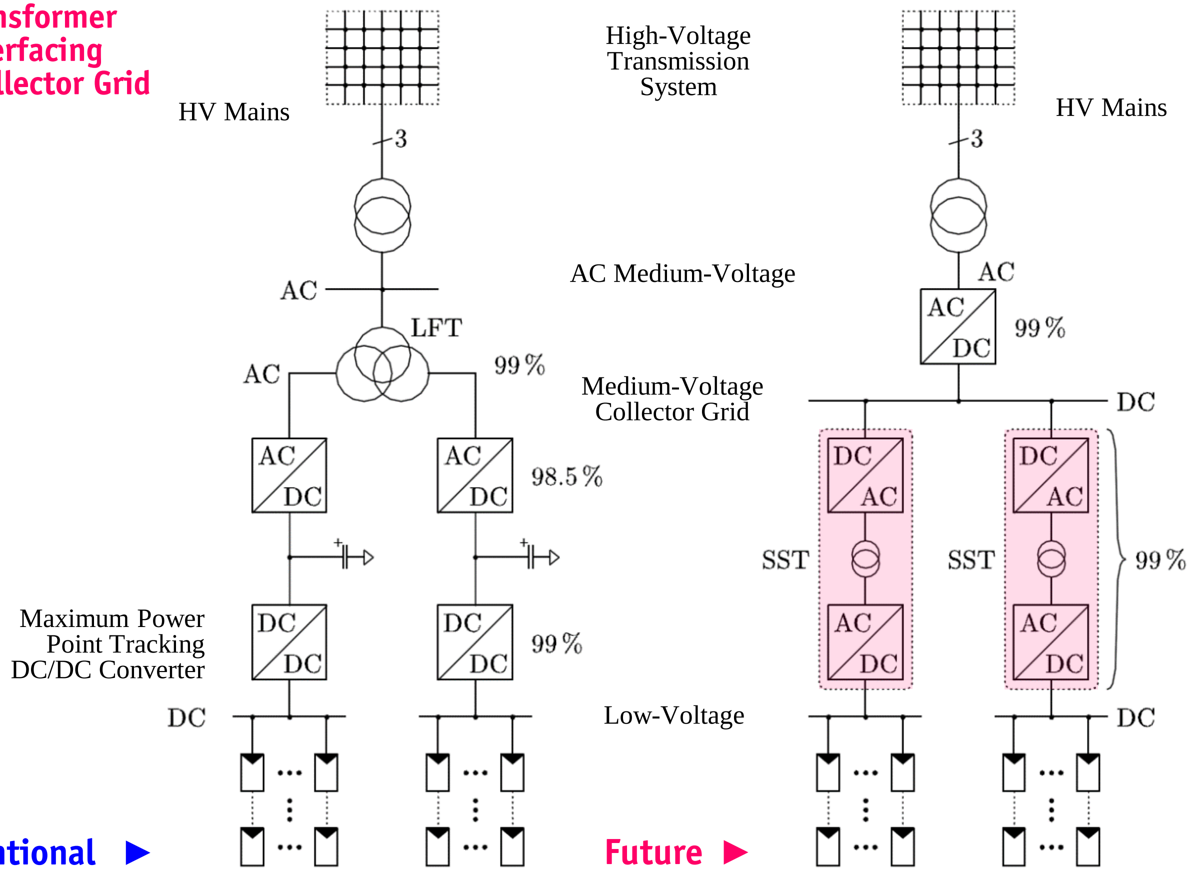
■ Medium-Voltage (DC) Power Collection and Transmission

Source: REUTERS/Stringer

- **Globally Installed PV Capacity Forecasted to 2.7 Terawatt by 2030 (IEA)**

→ Future DC Collector Grid

- **DC/DC Solid-State Transformer for MPPT & Direct Interfacing of PV Strings to MV Collector Grid**
- **1.5% Efficiency Gain Compared to Conv. AC Technology**

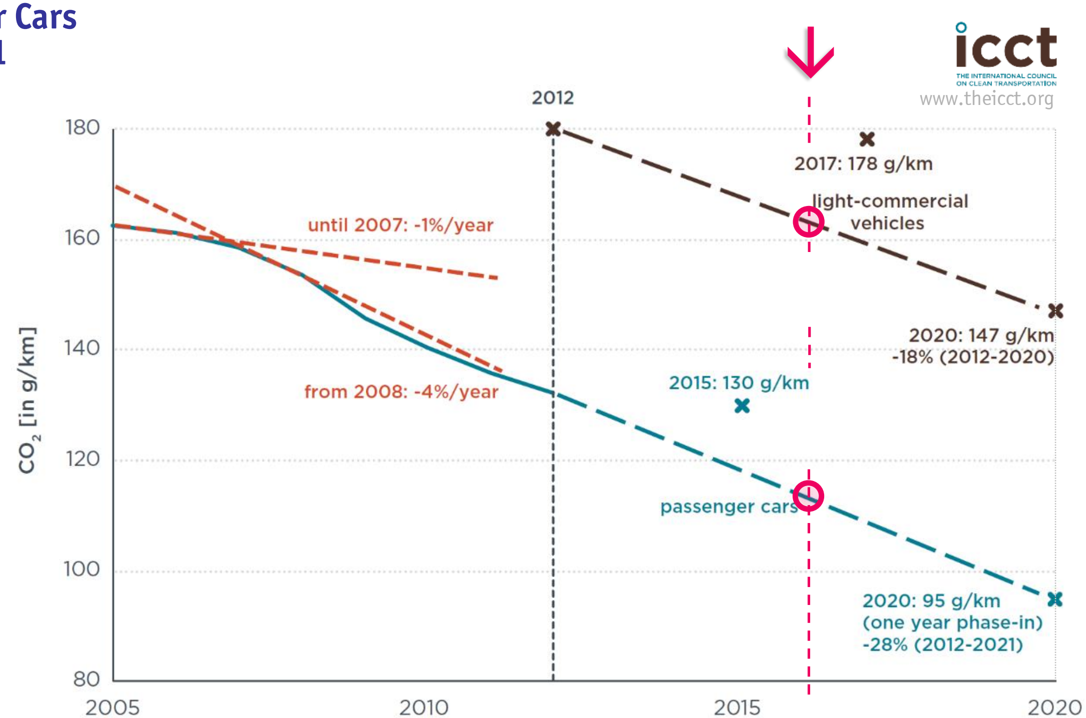


Conventional ▶ **Future ▶**

Sustainable Mobility

- **EU Mandatory 2020 CO_2 Emission Targets for New Cars**

— 147g CO_2/km for Light-Commercial Vehicles
— 95g CO_2/km for Passenger Cars
— 100% Compliance in 2021



- **Hybrid Vehicles**
- **Electric Vehicles**

→ Ultra-Fast / High-Power EV Charging

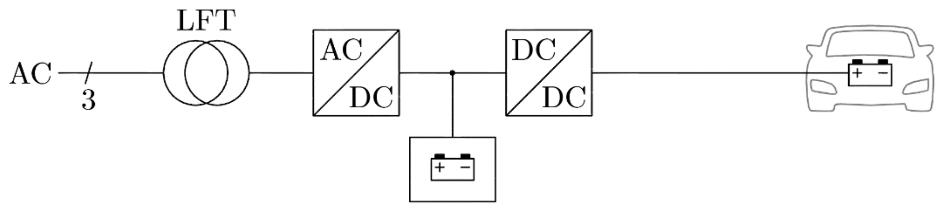
- Medium Voltage Connected Modular Charging Systems
- Very Wide Output Voltage Range (200…800V)

Source: Porsche Mission-E Project

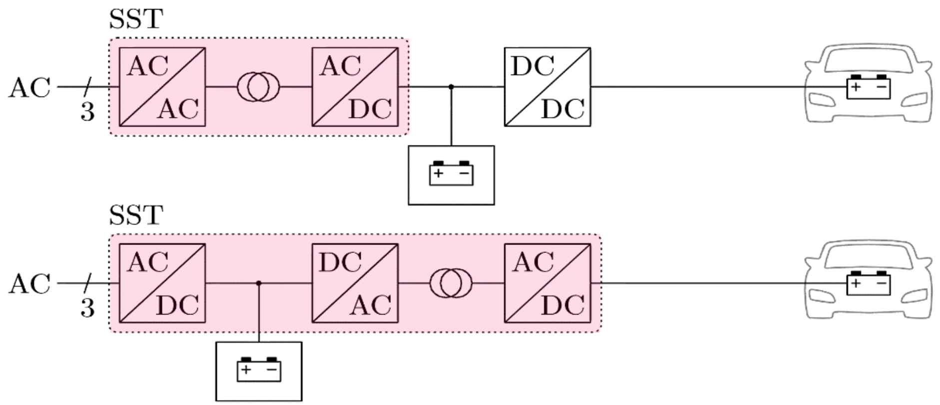
- E.g., Porsche *FlexBox* incl. Cooling
- Local Battery Buffer (140kWh)
- 320kW → 400km Range in 20min

→ *Bidirectional MV Interface*

- **Conventional**



- ***Future Solid-State Transformer (SST)-Based Concept***



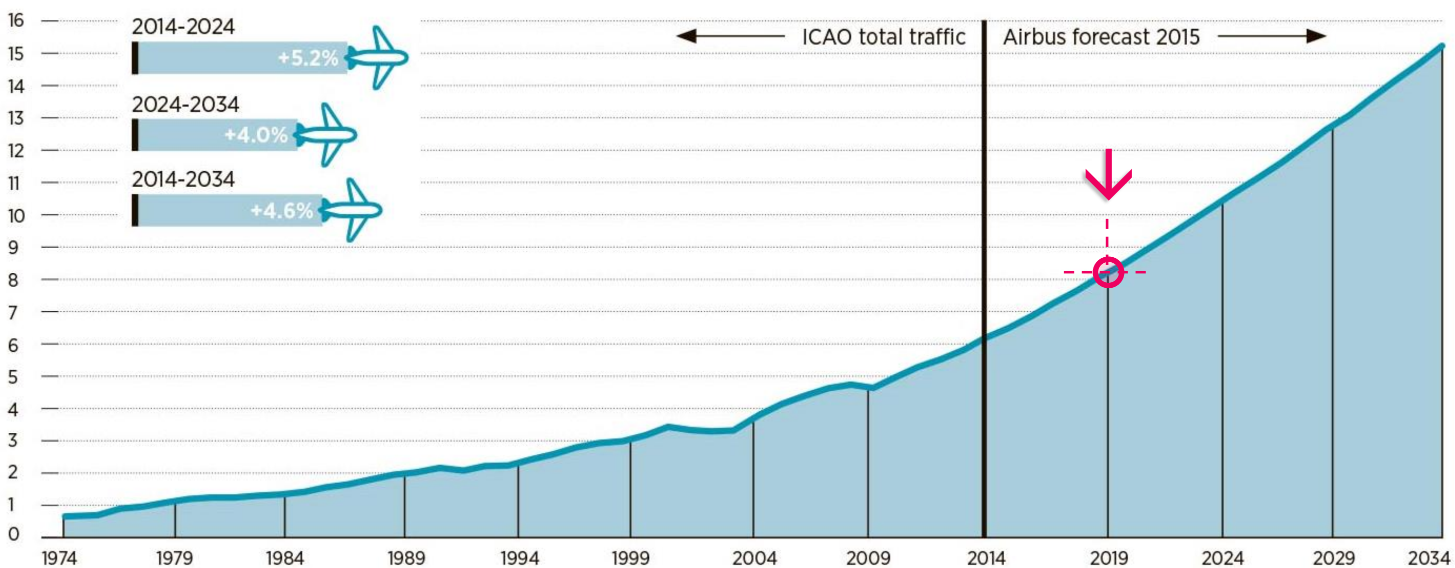
- **On-Site Power / Energy Buffer → „Energy-Hub“**
- **Power / Energy Management → Peak Load Shaving & Grid Support / Stabilization**

Sustainable Air Transportation

- **Massive Steady Increase of Global Air Traffic Over the Next Decades**
  - Need for 70´000 New Airliners over the Next 20 Years (Boeing & Airbus)
  - Stringent *Flightpath 2050 Goals* of ACARE → Reduction of CO_2/NO_x/Noise Emissions

GLOBAL AIR TRAFFIC (TRILLION REVENUE PASSENGER KILOMETRES)

Traffic is expected to double in the next 15 years



Source: International Civil Aviation Organization (ICAO)/Airbus 2015

→ Futuristic Mobility Concepts (1)

- Distributed Propulsion Aircraft
- Cut Emissions Until 2050
  - CO_2 by 75%,
  - NO_x by 90%,
  - Noise Level by 65%

Source: EADS

Future Hybrid
Distributed Propulsion Aircraft

- Eff. Optim. Gas Turbine
- 1000Wh/kg Batteries
- Distrib. Fans (E-Thrust)
- Supercond. Motors
- Med. Volt. Power Distrib.

→ Futuristic Mobility Concepts (2)

- Distributed Propulsion Aircraft
- Cut Emissions Until 2050
  - — CO_2 by 75%,
  - — NO_x by 90%,
  - — Noise Level by 65%

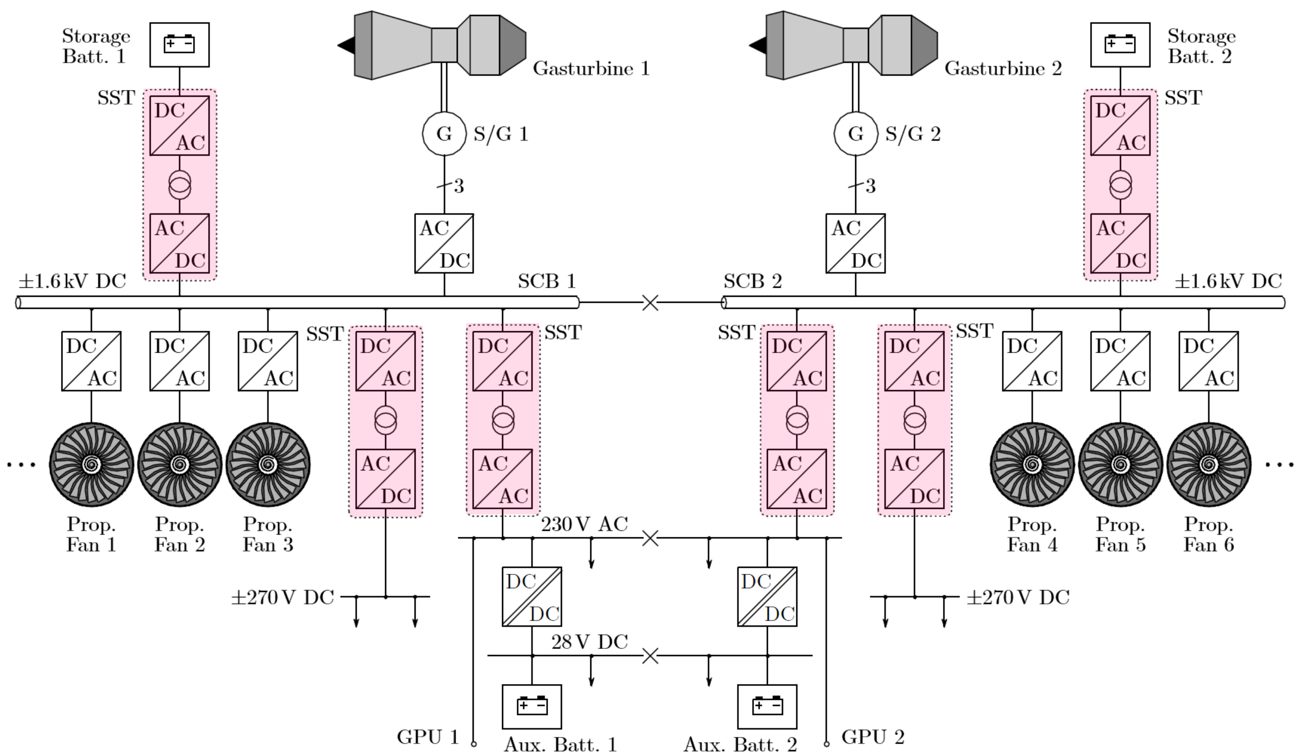
Source: NASA

NASA N3-X Vehicle Concept

- Wing-Tip Mounted Eff. Optimized Gas Turbines & Distributed E-Fans ("E-Thrust")
- MV or Superconducting Power Distribution Integr. 1000Wh/kg Batteries (EADS-Concept)

Future Aircraft Electric Power System

▶ MV or Superconducting Power Distribution Integr. 1000Wh/kg Batteries (EADS-Concept)

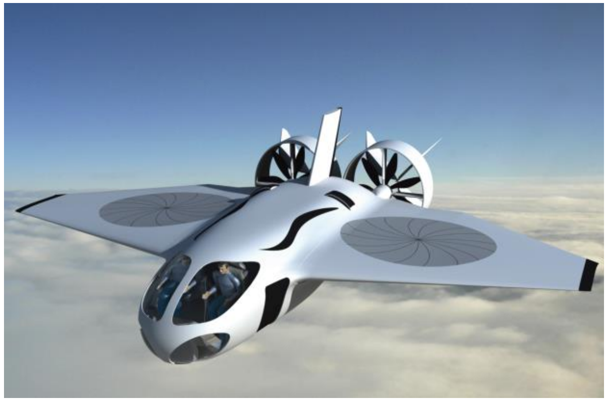


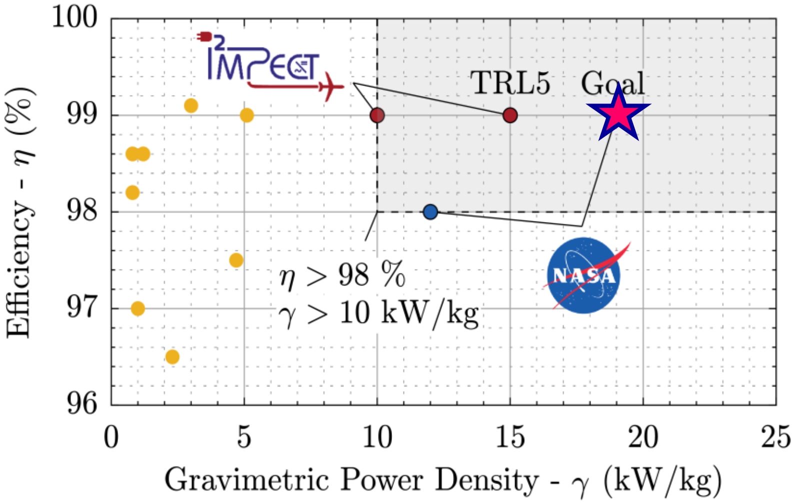
- Generators — 2 x 40.2MW (NASA)
- E-Fans — 14 x 5.7 MW (1.3m Diameter)

→ Future Technology Requirements

- *Red. Inverter Volume / Weight* → *Matching of Low High-Speed Motor Volume*
- *Lower Cooling Requirement* → *Low Inverter Losses & HF Motor Losses*
- *High Speed Machines* → *High Output Frequency Range*

Source: Georgia Tech



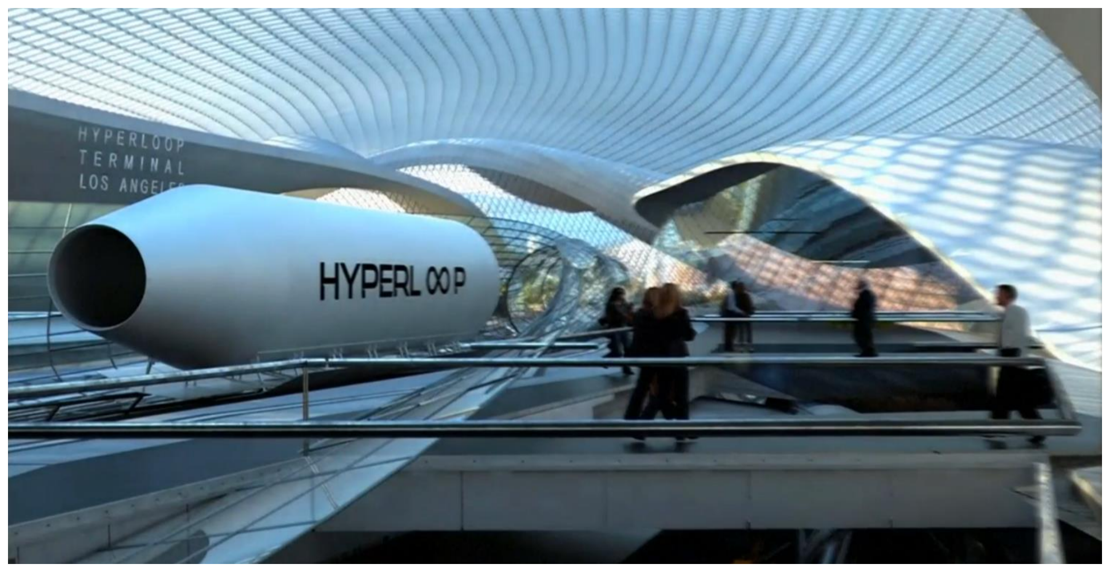


→ *Main "Enablers" — SiC/GaN Power Semiconductors & Adv. Inverter Topologies*

→ *Futuristic Ground-Based Mobility*

- Hyperloop
- San Francisco → Los Angeles in 35min

HYPERLOOP
POD COMPETITION
www.spacex.com/hyperloop



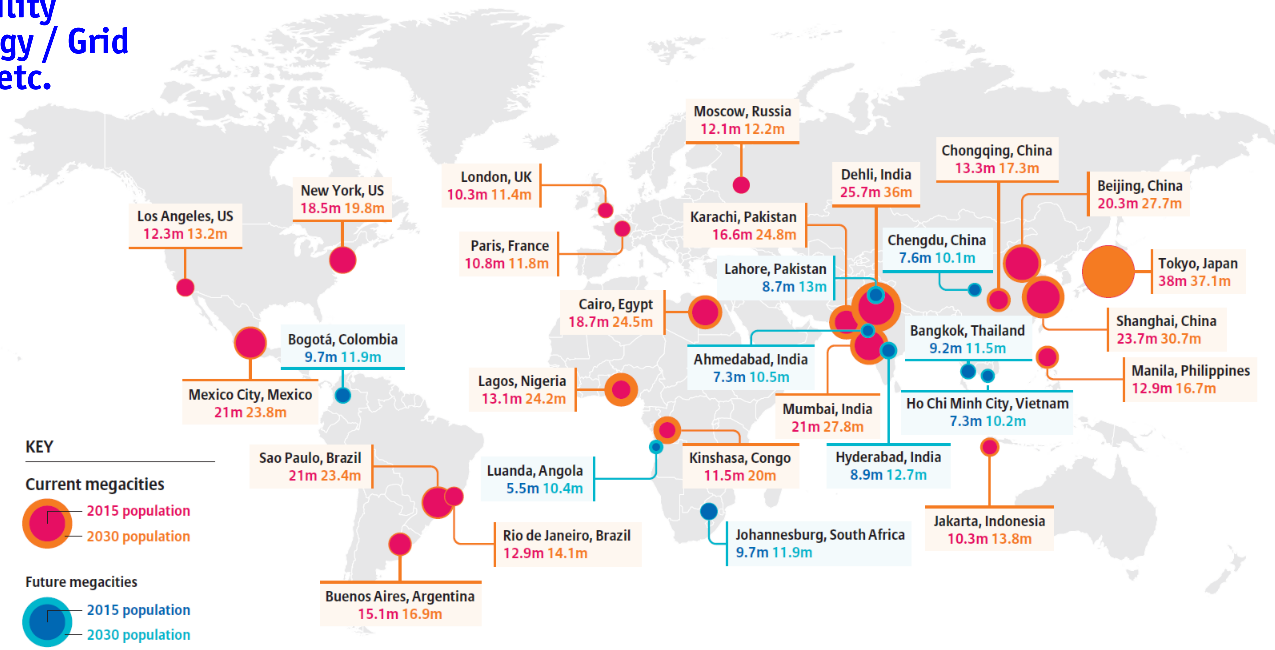
- Low Pressure Tube
- Magnetic Levitation
- Linear Ind. Motor
- Air Compressor in Nose

Urbanization

- 60% of World Population Exp. to Live in Urban Cities by 2025
- 30 MEGA Cities Globally by 2023

— Smart Buildings
— Smart Mobility
— Smart Energy / Grid
— Smart ICT, etc.

Source: World Urbanization Prospects: The 2014 Revision



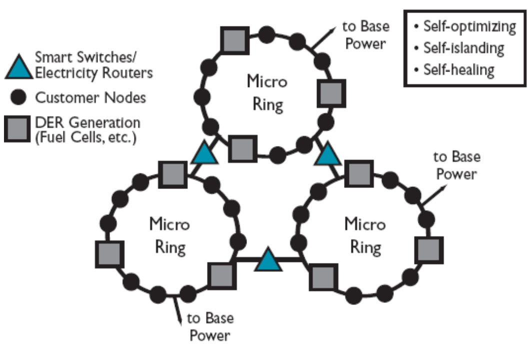
- *Selected Current & Future MEGA Cities 2015 → 2030*

→ Smart Cities / Grids / Buildings (1)

- *Masdar = “Source”*
- — Fully Sustainable Energy Generation
  - * Zero CO_2
  - * Zero Waste
- — EV Transport / IPT Charging
- — to be finished 2025

Masdar CITY
www.masdar.ae

Source: EPRI ELECTRIC POWER RESEARCH INSTITUTE

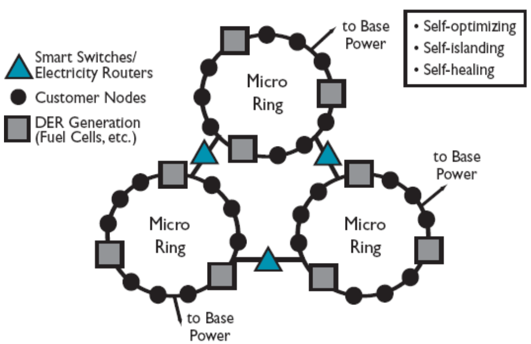


→ Smart Cities / Grids / Buildings (2)

- *Masdar = "Source"*
- — Fully Sustainable Energy Generation
  - * Zero CO_2
  - * Zero Waste
- — EV Transport / IPT Charging
- — to be finished 2025

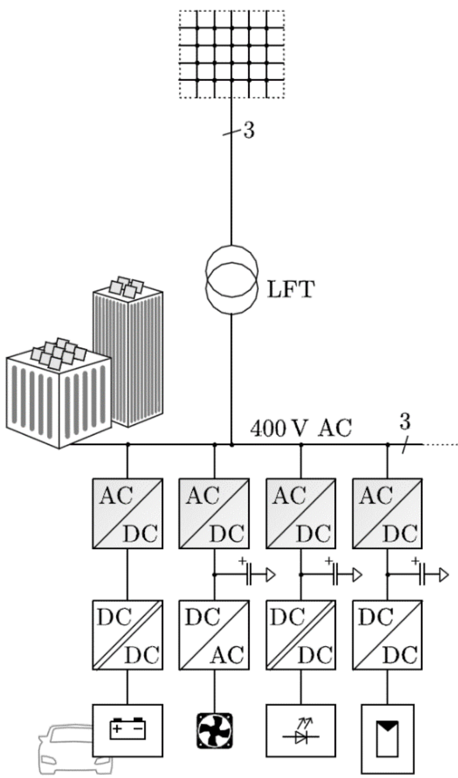
Masdar CITY
www.masdar.ae

Source: EPRI ELECTRIC POWER RESEARCH INSTITUTE

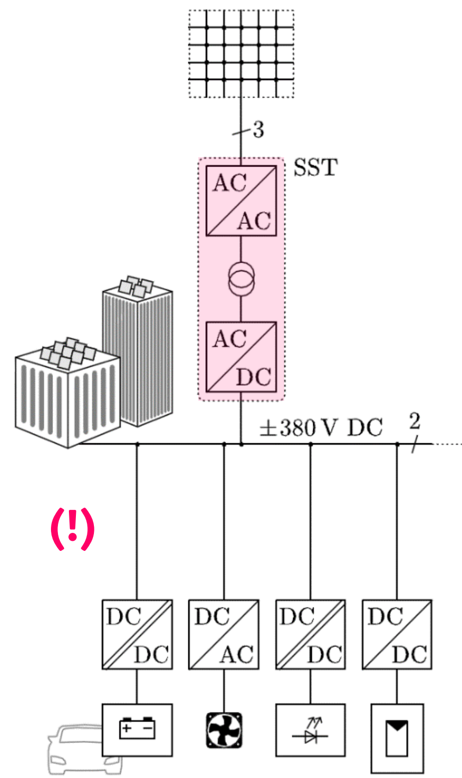


→ DC Microgrids

- **Local DC Microgrid** **Integrating Loads/Ren. Sources/Storage**
- **No Low-Voltage AC/DC Conversion → Higher Efficiency & Lower Realization Effort**



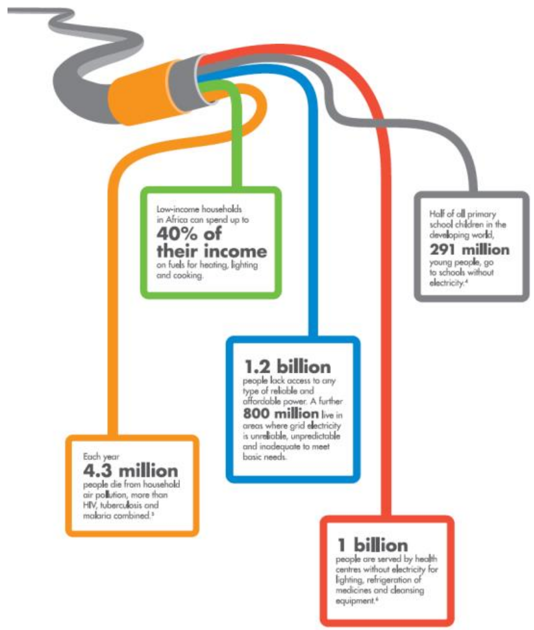
— **Conventional**

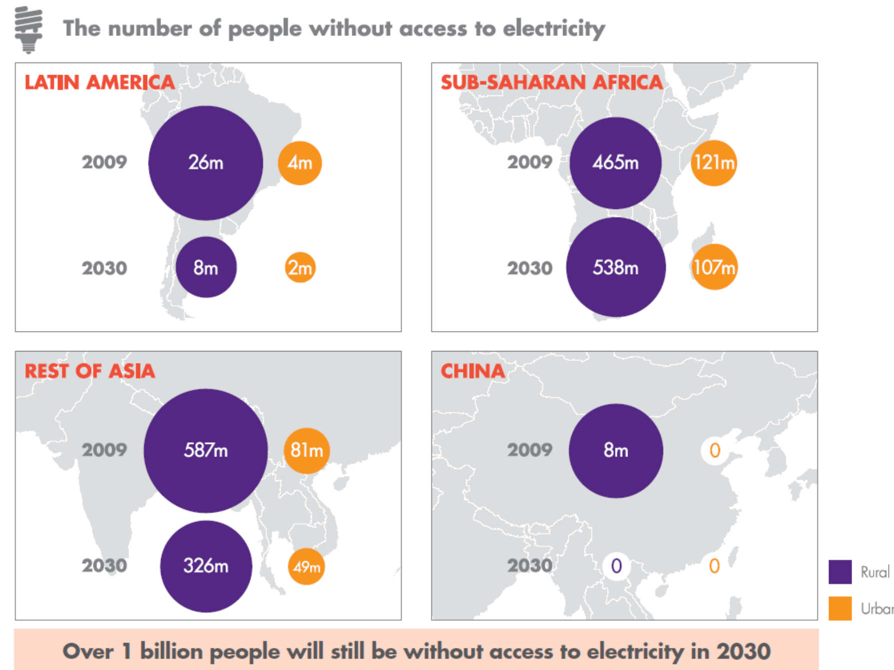


— ***Future SST-Based Concept***

Alleviate Poverty

- 2 Billion "Bottom-of-the-Pyramid People" are Lacking Access to Clean Energy
- Rural Electrification in the Developing World





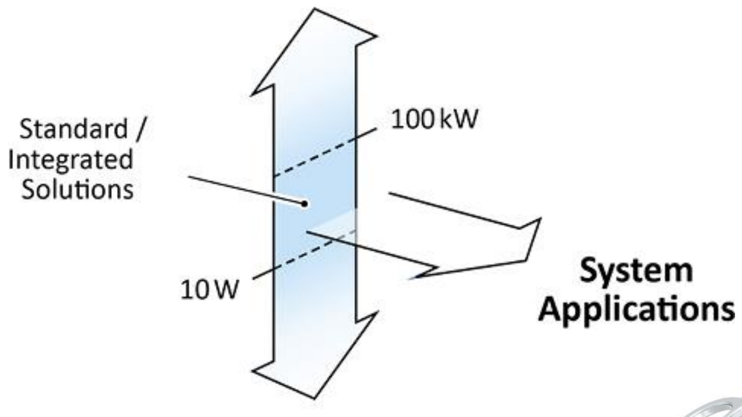
Source: IEA, Dalberg Analysis, IFC

- Urgent Need for Village-Scale Solar DC Microgrids etc.
- 2 US$ for 2 LED Lights + Mobile-Phone Charging / Household / Month (!)

Future Development

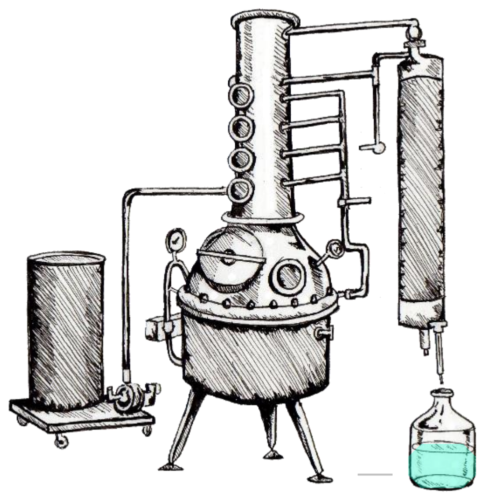
- Commoditization / Standardization
- Extreme Cost Pressure (!)

"There is Plenty of Room at the Top" → *Medium Voltage/Frequency Solid-State Transformers*



Power-Supplies on Chip ← **"There is Plenty of Room at the Bottom"**

- Key Importance of Technology Partnerships of Academia & Industry



Source: whiskeybehavior.info

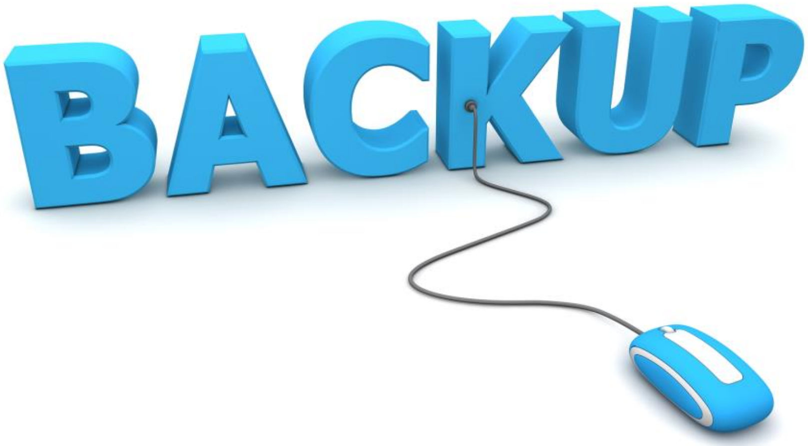
Conclusion

Conclusion

Source: www.insites-consulting.com

→ ***Power Electronics is a Key and Enabling Technology for all Kinds of Electric Energy Utilization !***

Thank you!

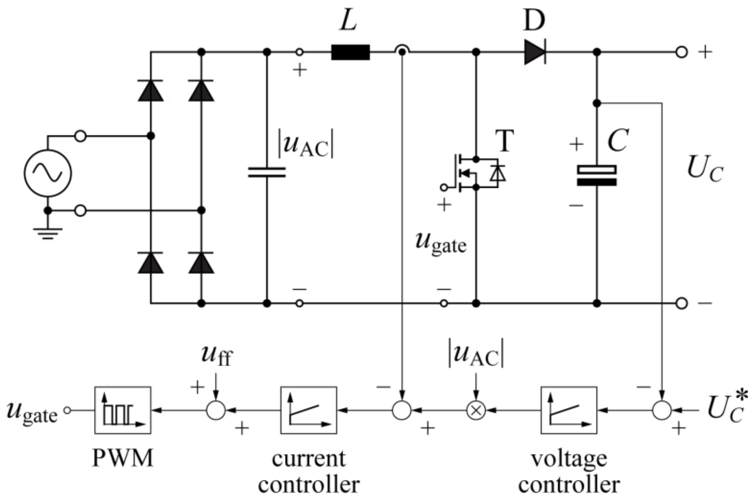

BACKUP

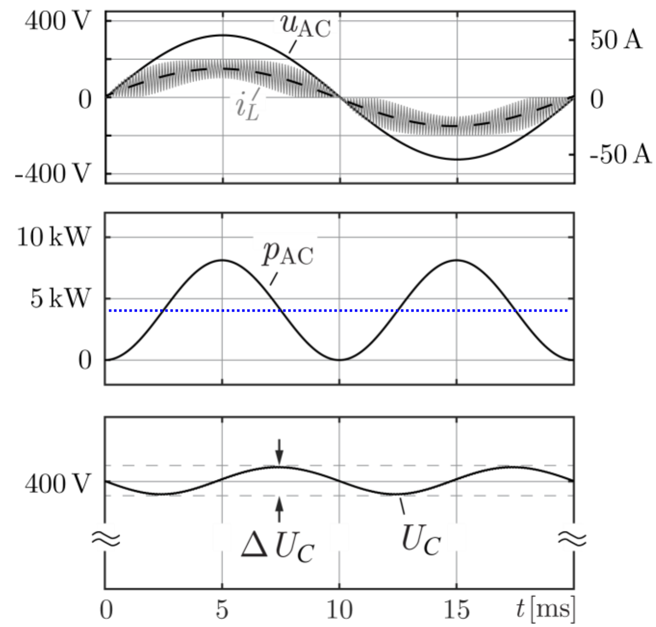
1-Φ AC/DC Conversion

DC-Side Energy Storage Requirement

1-Φ AC/DC Conversion

■ Example of Boost-Type PFC Rectifier

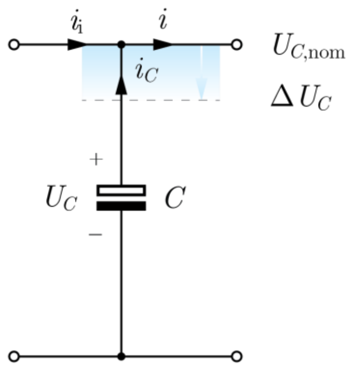


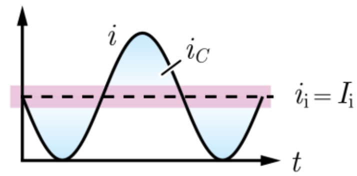


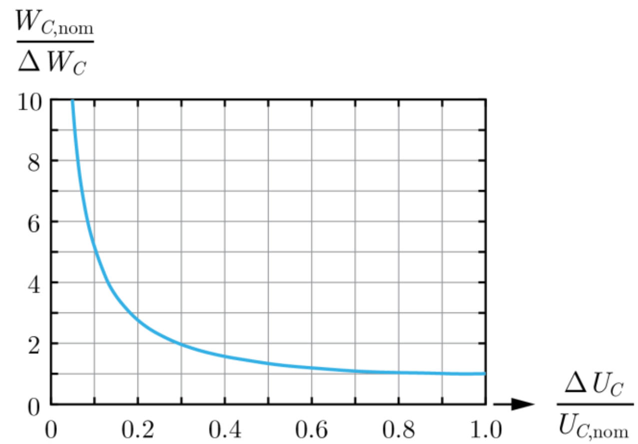
- **Input Voltage & Current / Power Flow / DC Output Voltage Fluctuation**

Passive Power Pulsation Buffer

■ Electrolytic Capacitor





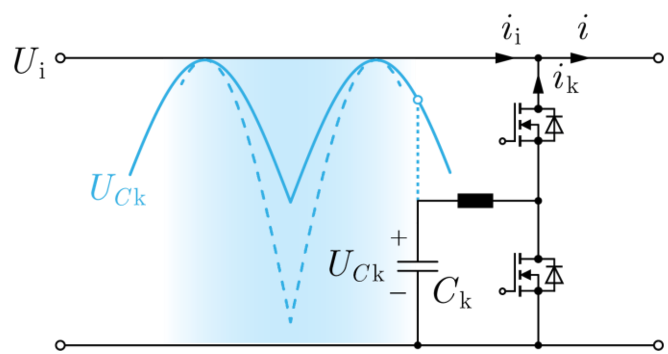


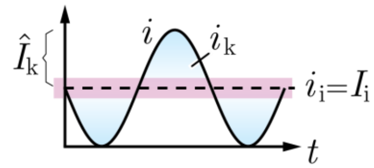
Example
S_0 = 2.0 kVA
$\cos \Phi_0$ = 0.7
$U_{C,nom}$ = 400 V
$\Delta U_C/U_{C,nom}$=3 %

- C > 1.3mF / 100 cm³ → 1/3 of the Total Converter Volume (!)

Active Power Pulsation Buffer

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck-Type (Lower Voltage Levels) or Boost-Type DC/DC Interface Converter



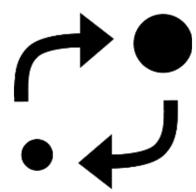


CeraLink™
TDK

108 x 1.2µF /400 V
$C_k \approx 140\mu F$
$V_{Ck} = 23.7 cm^3$

- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

Scaling of Electric Machines



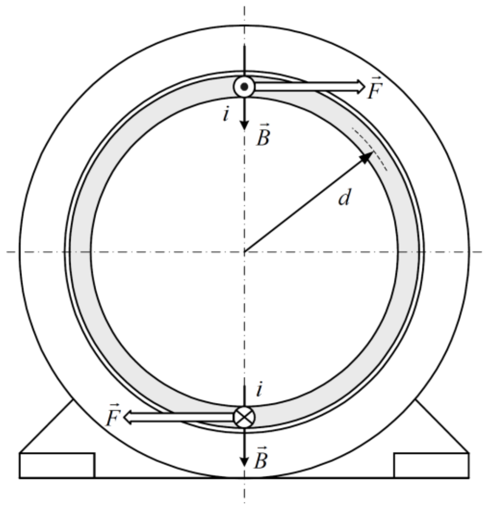
Source: www.freevector.co

Scaling of Electric Machines (1)

- Generated Force Dependent on Magnetic Field and Current
- Current Def. by "*Current Loading*" (A/cm) or *Current Density* (A/cm²) or *Cooling* (W/cm²)
- Magnetic Field Strength Limited by Saturation

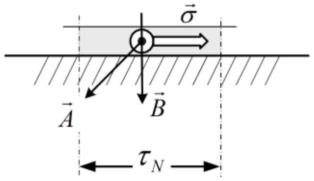
→ Assumption: A = const.

$$F = I \cdot l \cdot B = A\tau_N \cdot l \cdot B$$



→ Rotor Surface Area Related Force (N/cm²)

$$\sigma = \frac{F}{\tau_N \cdot l} = A \cdot B$$



→ Torque

$$T = \frac{d}{2}(d\pi \cdot l)\sigma \sim 2A \cdot B(\frac{d^2\pi}{4} \cdot l) \sim L^3$$

- Const. Current Density
- Const. Loss / Surface

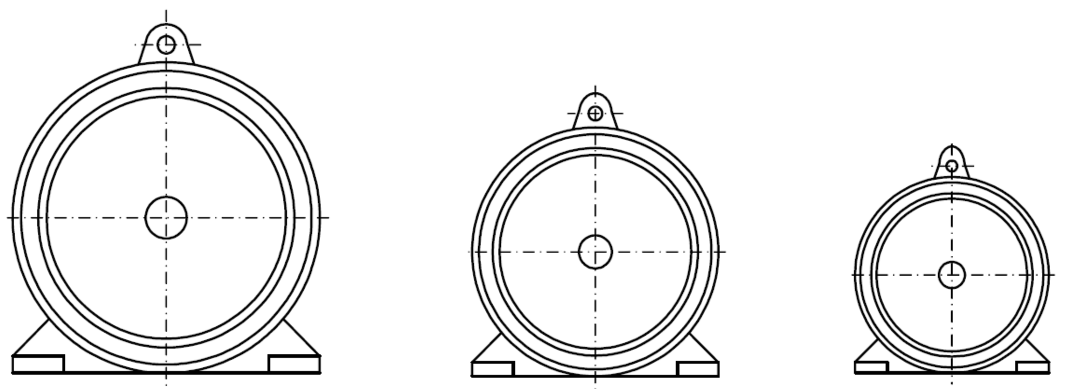
$$T \sim L^4$$
$$T \sim L^{3.5}$$

Scaling of Electric Machines (2)

- Dependency of Motor / Generator Size on Output Power
- Overall Size Drops with Increasing Motor Speed

→ Power $P = T \cdot \omega = T \cdot 2\pi n$

→ Volume $L^3 \sim T \sim \dfrac{P}{2\pi n}$ ↑



$P = P^*$, $n = n^*$, $T = T^*$

$P = P^*$, $n = 2n^*$, $T = \frac{1}{2}T^*$

$P = P^*$, $n = 4n^*$, $T = \frac{1}{4}T^*$

- Gearbox Required for Low Speed of Turbine / Load → Adds Volume and Losses