ETH zürich

Power Electronics Workshop 2016

Multi-Objective Optimization of Power Electronics Converter Systems

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Outline

- Introduction
- *Multi-Objective Optimization Approach*
- *Optimization Application Examples*
- Summary

Acknowledgement

D. Bortis
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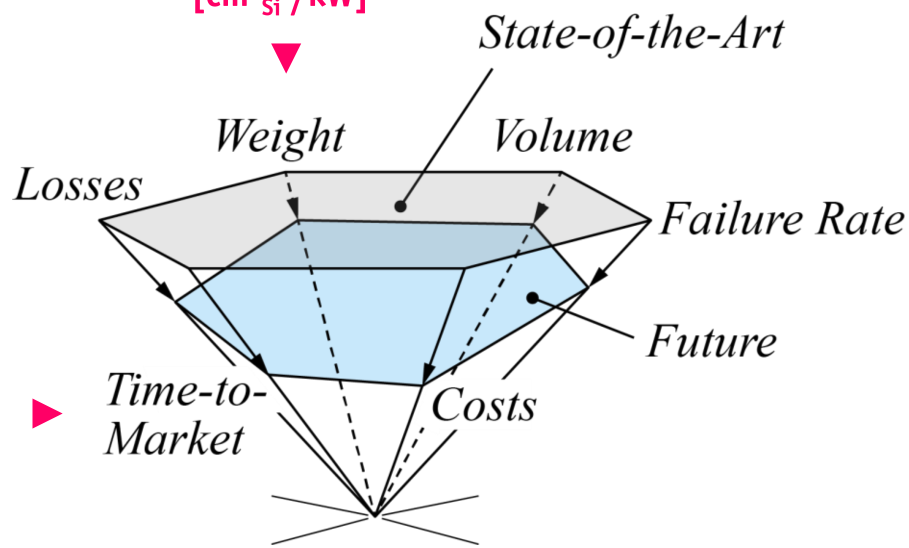
R. Burkart
F. Krismer

Introduction

Power Electronics Performance Trends
Power Converter Design Challenge

Power Electronics Converters Performance Trends

Environmental Impact... $[kg_{Fe}\ /kW]$
$[kg_{Cu}\ /kW]$
$[kg_{Al}\ /kW]$
$[cm^2_{Si}\ /kW]$

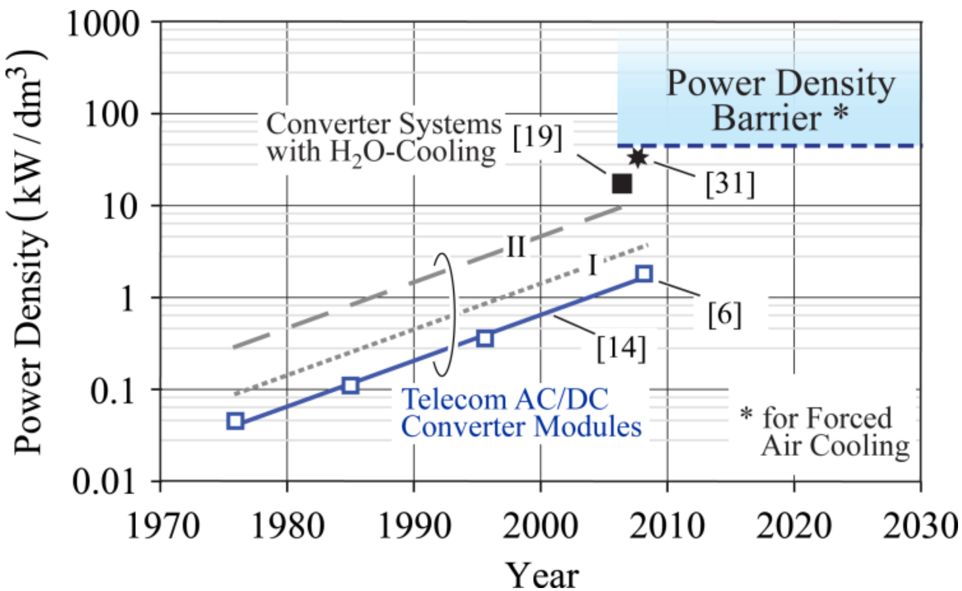


Performance Indices

- Power Density [kW/dm³]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h⁻¹]

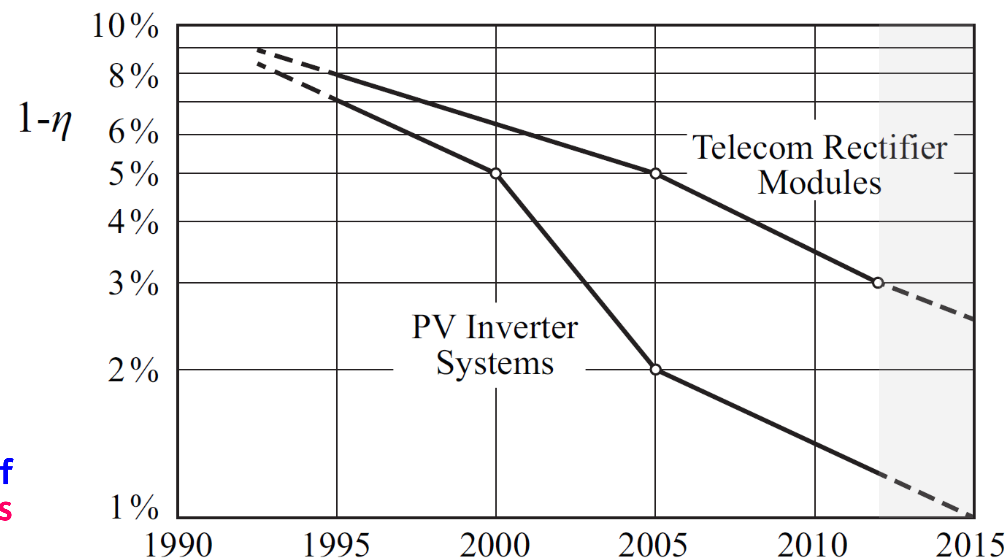
▶ Performance Improvements (1)

- **Power Density**
  - **Telecom Power Supply Modules:** Typ. Factor 2 over 10 Years



▶ Performance Improvements (2)

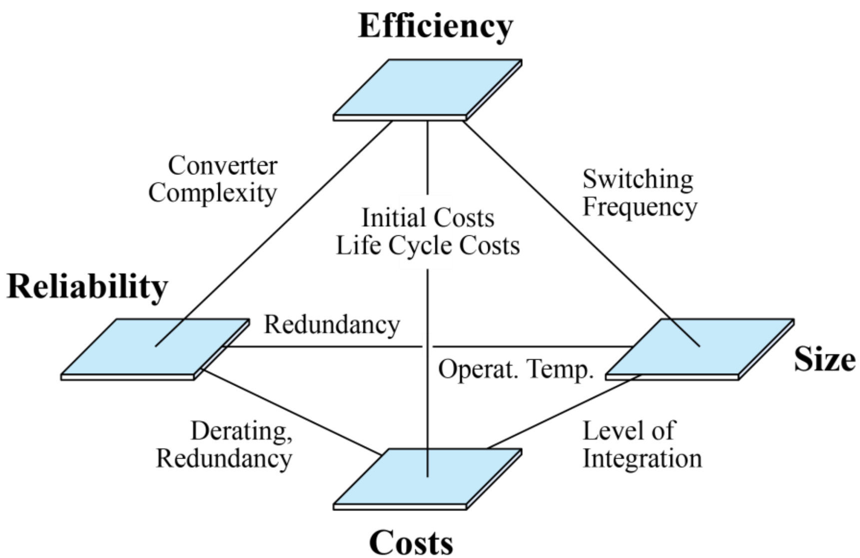
Inefficiency (Losses)...



- **Efficiency**
  - PV Inverters: Typ. Loss Red. of Typ. Factor 2 over 5...10 Years

▶ Multi-Objective Design Challenge (1)

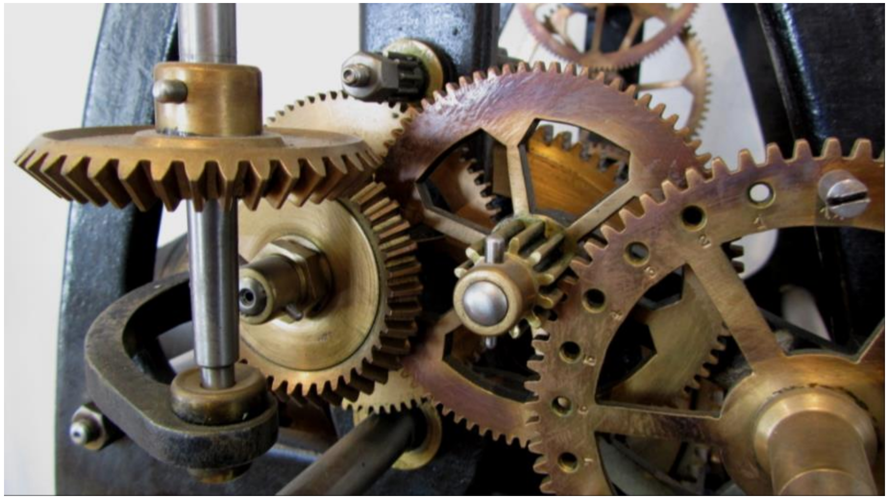
- Performances are Approaching Physical Limits (e.g. Efficiency)
- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices - Trade-Offs



→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

▶ Multi-Objective Design Challenge (2)

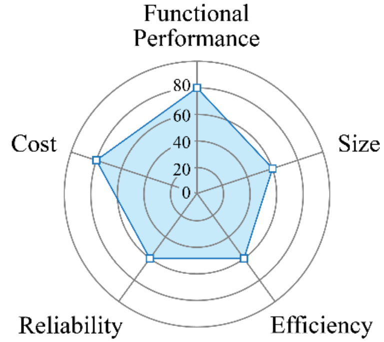
- Performances are Approaching Physical Limits (e.g. Efficiency)
- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices - Trade-Offs



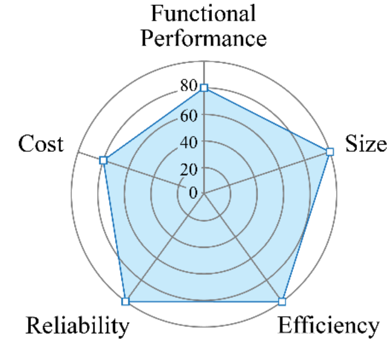
→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

Multi-Objective Design Challenge (3)

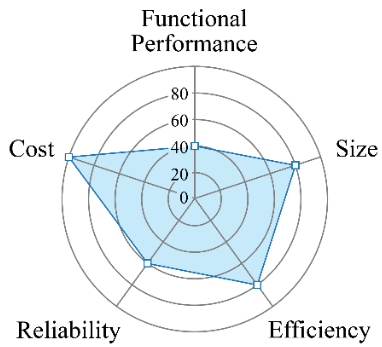
- Specific Performance Profiles / Trade-Offs Dependent on Application



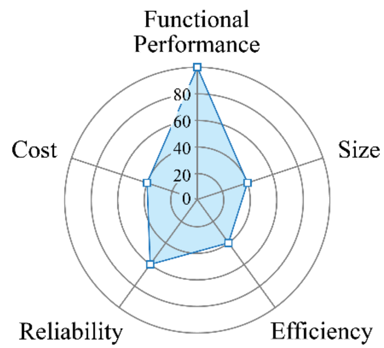
Industry Applications



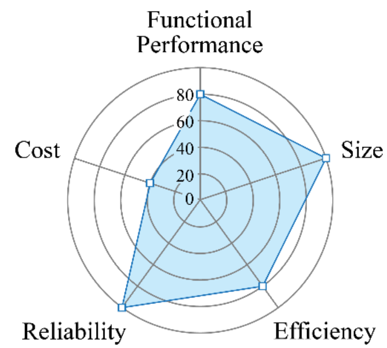
Information & Communication Industry



Domestic Applications



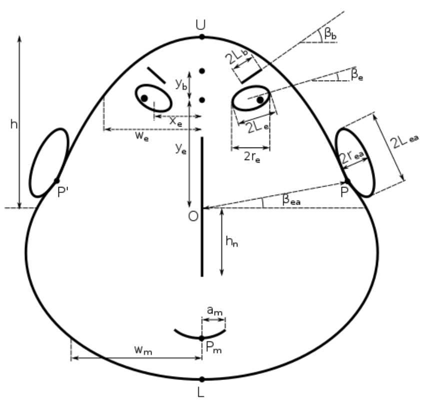
Laboratory Applications

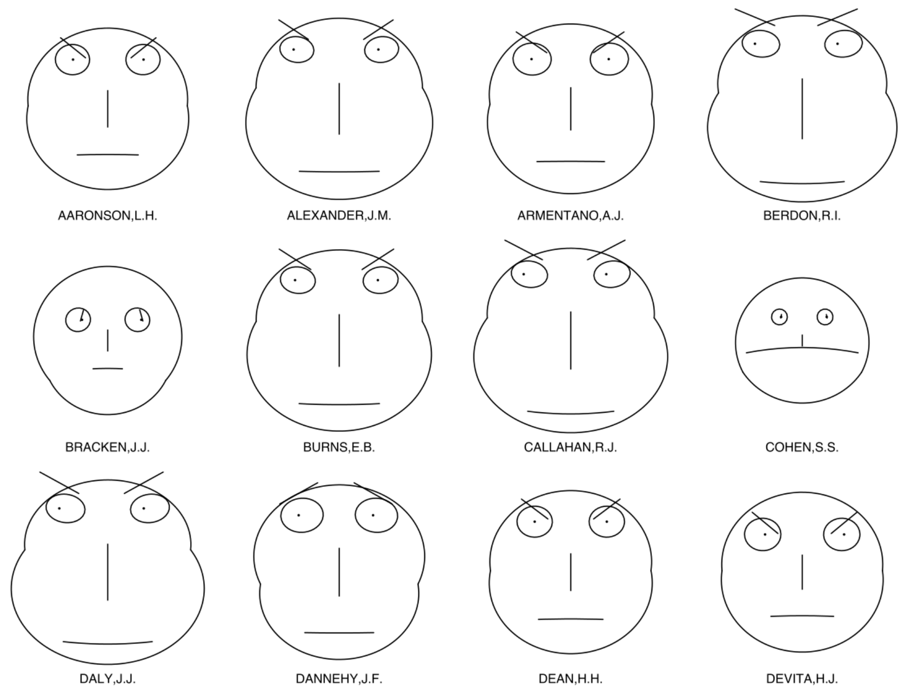


Aerospace Applications

▶ Visualization of Multiple Performances

- Spider Charts, etc.
- Chernoff-Faces ;-)





→ H. Chernoff / Stanford: "The Use of Faces to Represent Points in K-Dimensional Space Graphically"

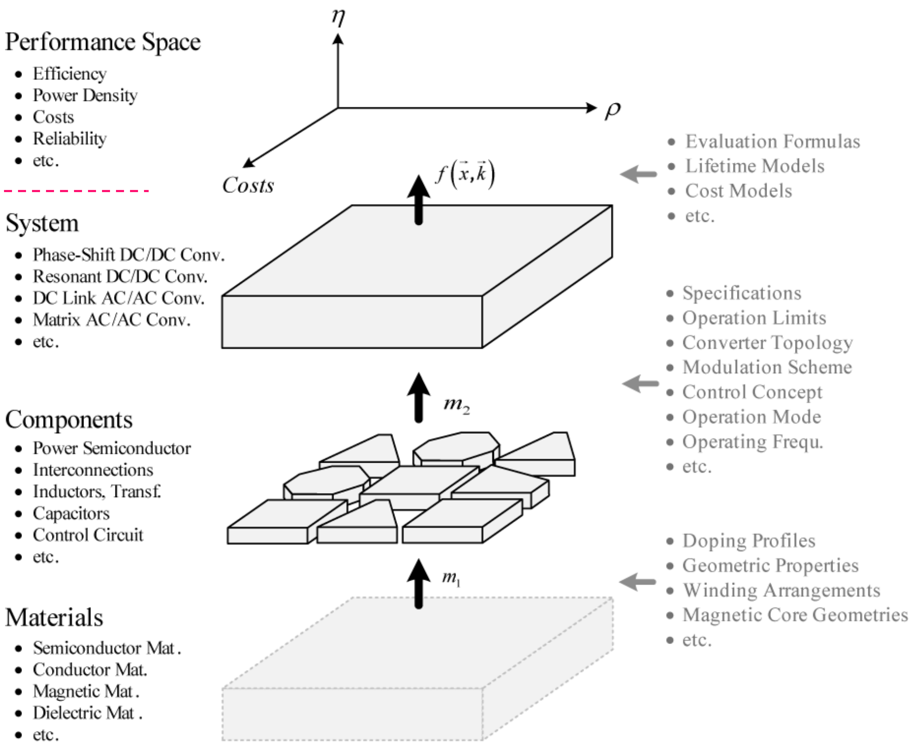
Multi-Objective Optimization

Abstraction of Converter Design
Design Space / Performance Space
Pareto Front
Sensitivities / Trade-Offs

▶ Abstraction of Power Converter Design

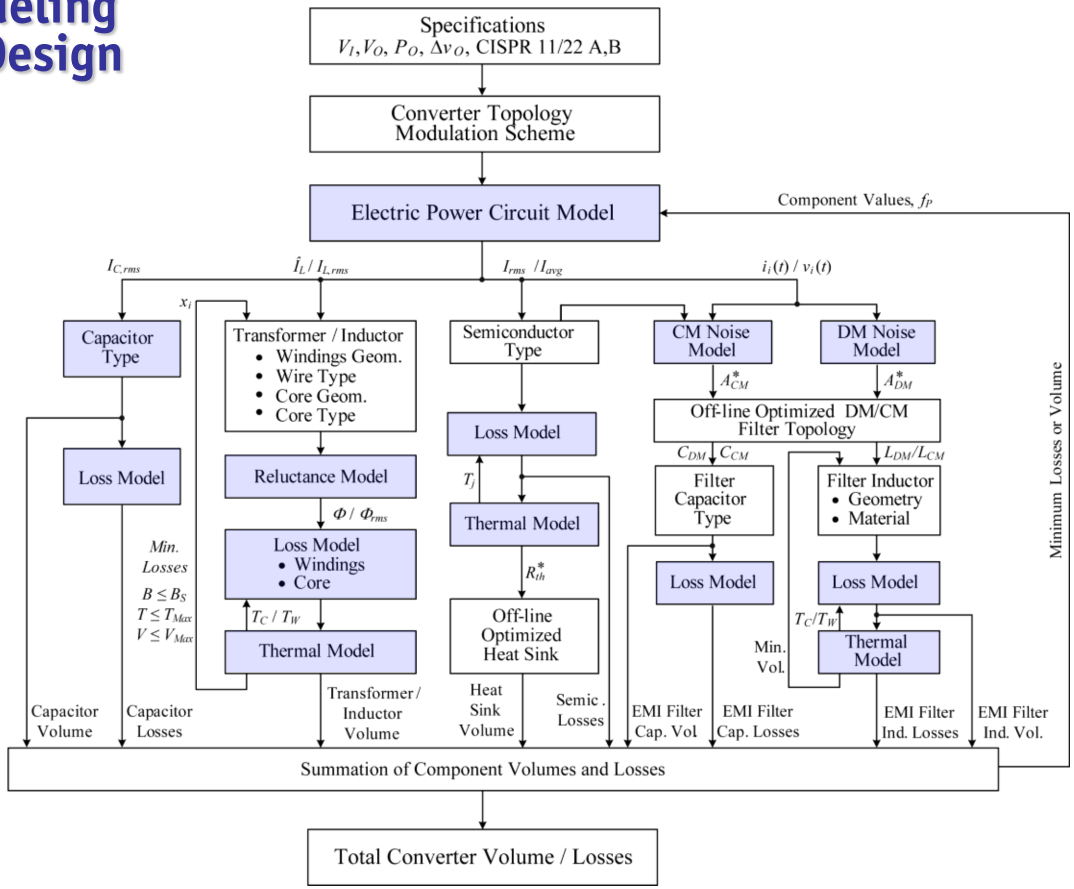
Performance Space

Design Space



→ *Mapping* of "*Design Space*" into System "*Performance Space*"

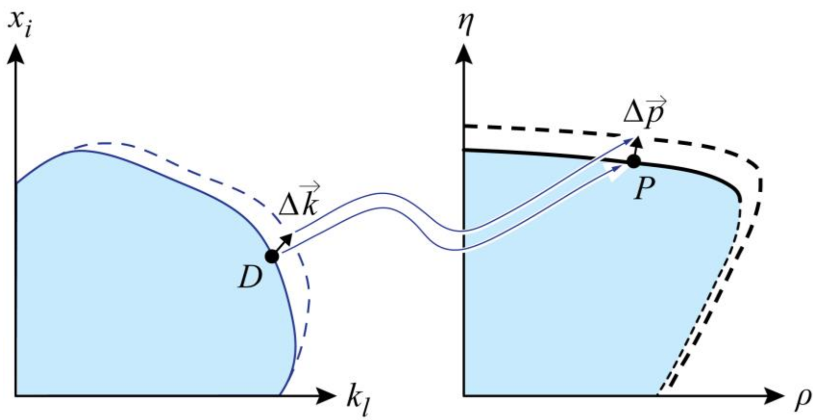
▶ Mathematical Modeling of the Converter Design



→ **Multi-Objective Optimization – Best Utilization of All Degrees of Freedom**

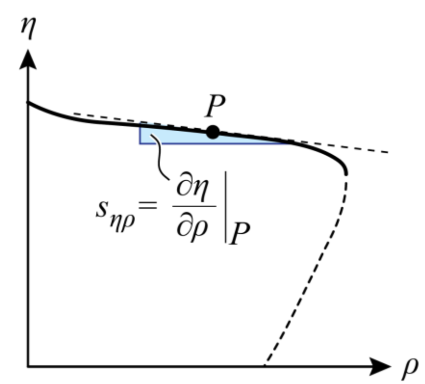
▶ Multi-Objective Optimization (1)

- Ensures Optimal Mapping of the "Design Space" into the "Performance Space"
- Identifies Absolute Performance Limits → Pareto Front / Surface



Design Space

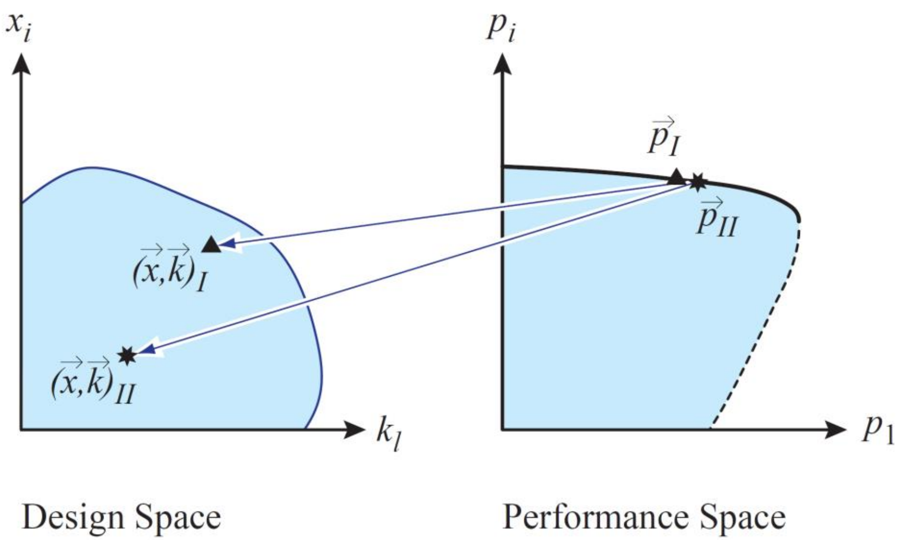
Performance Space



→ Clarifies Sensitivity $\Delta\vec{p}\,/\,\Delta\vec{k}$ to Improvements of Technologies
→ Trade-off Analysis

▶ Multi-Objective Optimization (2)

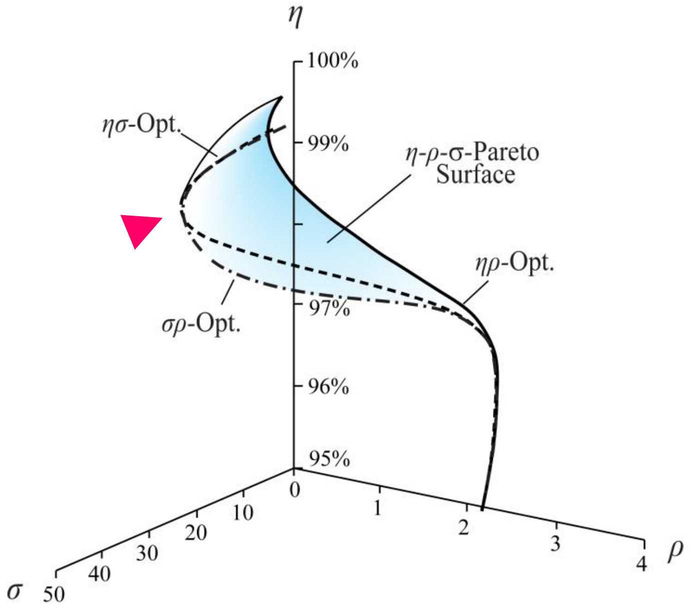
- Design Space Diversity
- Equal Performance for Largely Different Sets of Design Parameters

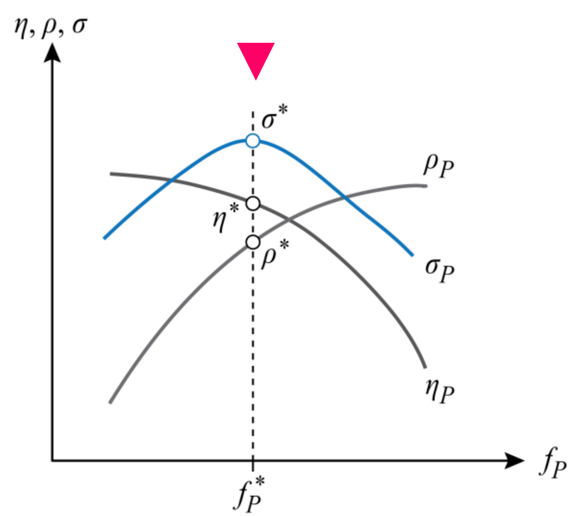


→ E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)
→ Allows Optimization for Further Performance Index (e.g. Costs)

► Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- Definition of a Power Electronics *"Technology Node"* → (η^*,ρ^*,σ^*,f_P^*)
- Maximum σ [kW/$], Related Efficiency & Power Density





→ Specifying Only a Single Performance Index is of No Value (!)
→ Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)

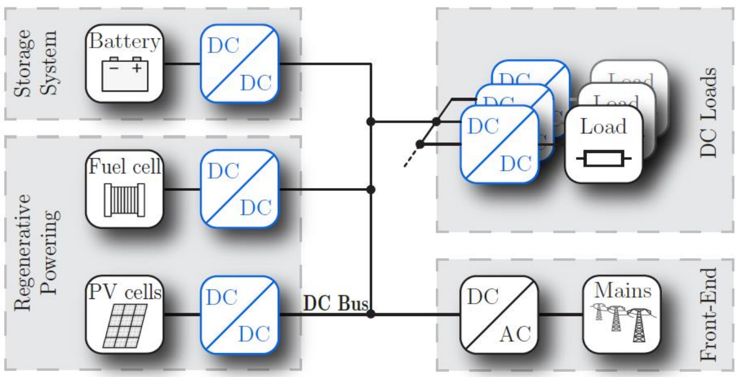
Multi-Objective Optimization Application Examples

Comparative Converter Evaluation
Impact of Technology Progress
Design Space Diversity

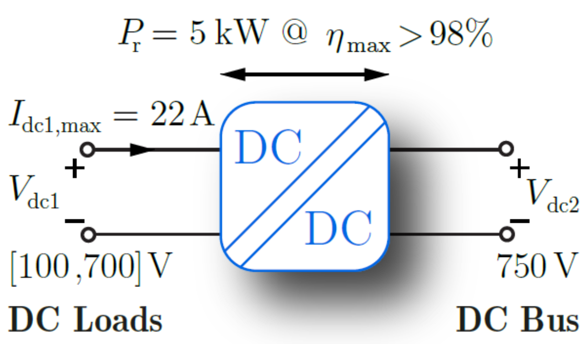
Comparative
Converter Evaluation →

Wide Input Voltage Range Isolated DC/DC Converter

Structure of "Smart Home" DC Microgrid



Universal DC/DC Converter

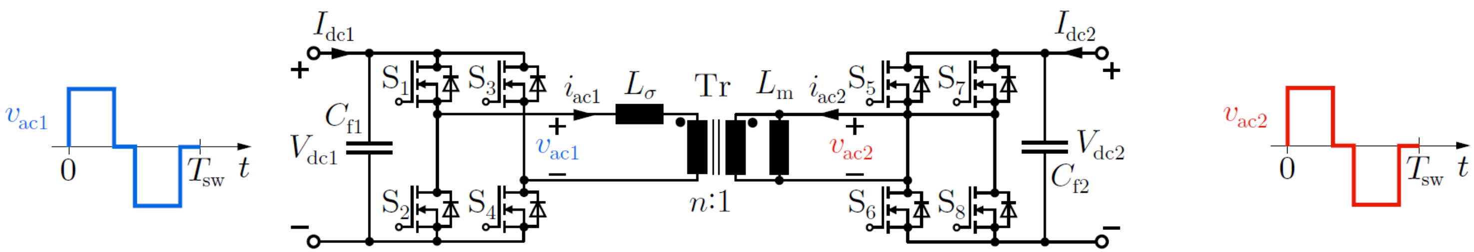


- **Universal Isolated DC/DC Converter**
  - Bidirectional Power Flow
  - Galvanic Isolation
  - Wide Voltage Range
  - High Partial Load Efficiency

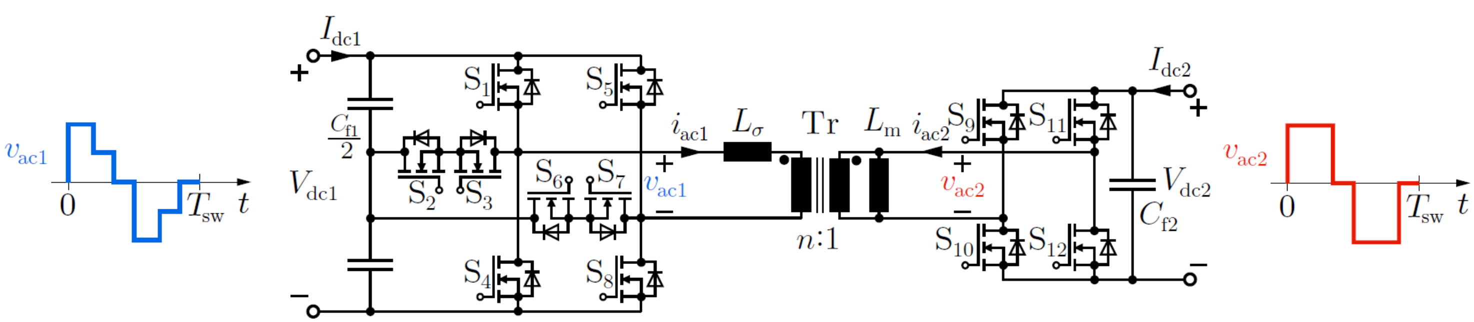
- **Advantages**
  - Reduced System Complexity
  - Lower Overall Development Costs
  - Economies of Scale

Comparative Evaluation of Converter Topologies

- Conv. 3-Level Dual Active Bridge (3L-DAB)

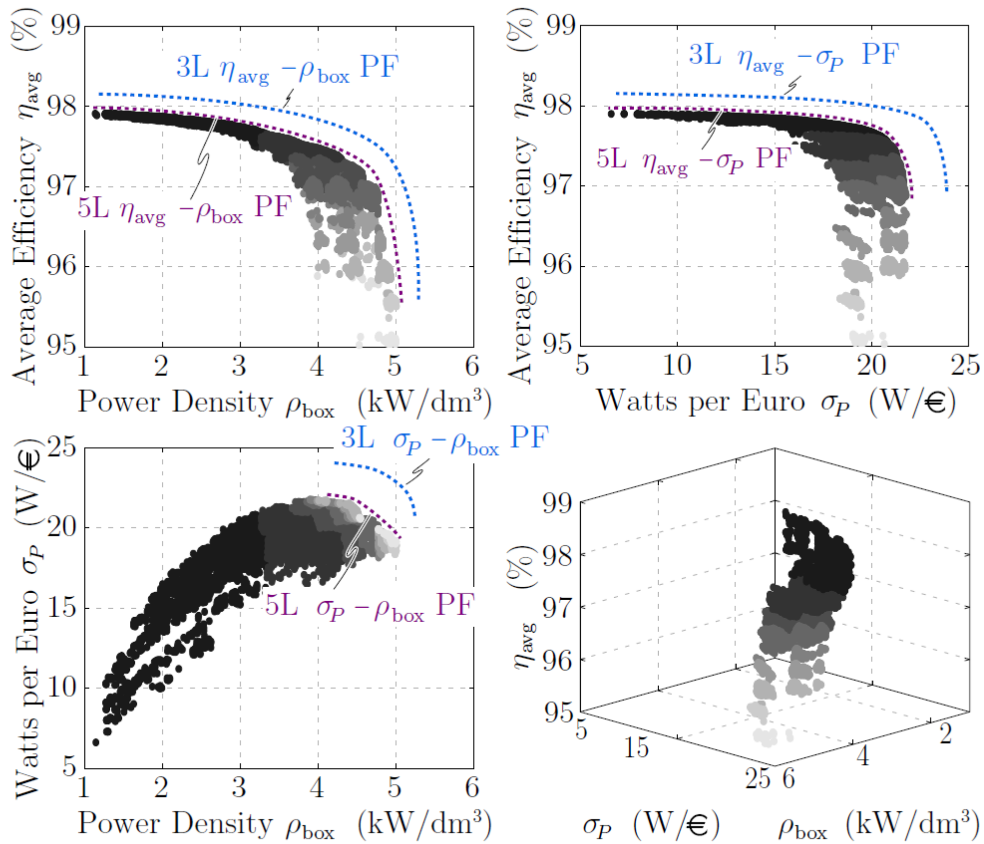


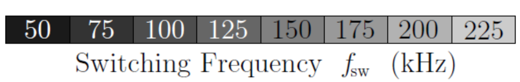
- Advanced 5-Level Dual Active Bridge (5L-DAB)



▶ Optimization Results - Pareto Surfaces

- 3-Level Dual Active Bridge
- 5-Level Dual Active Bridge



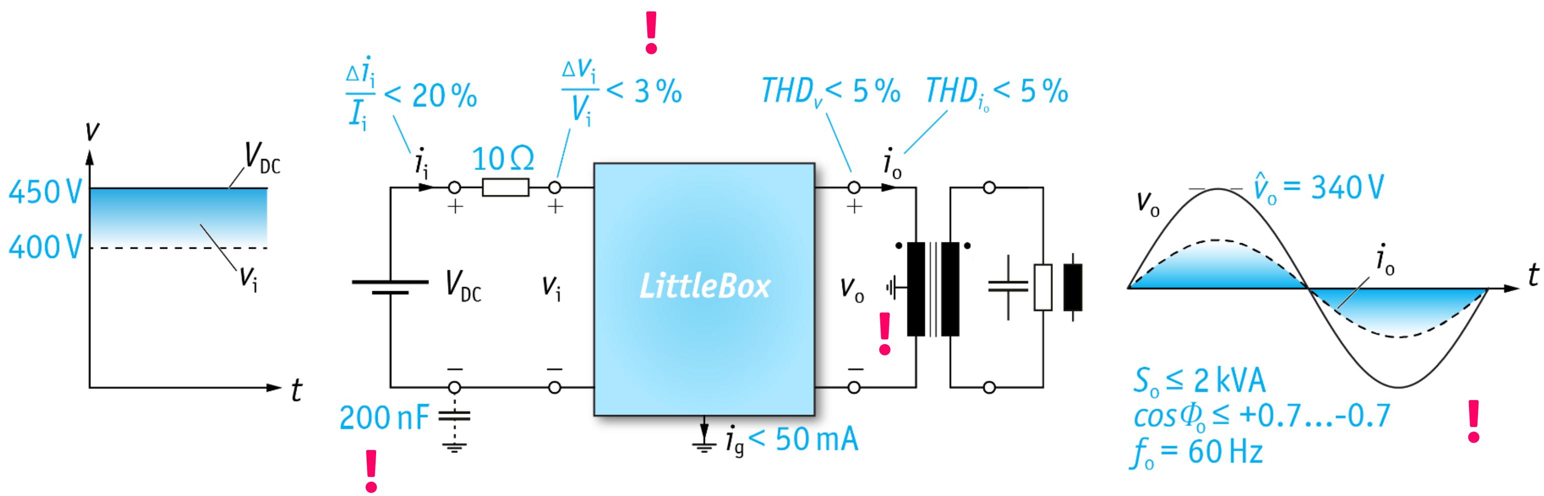


Impact of Technology Progress
& Design Space Diversity →

LiTTLE BOX CHALLENGE

Google | IEEE

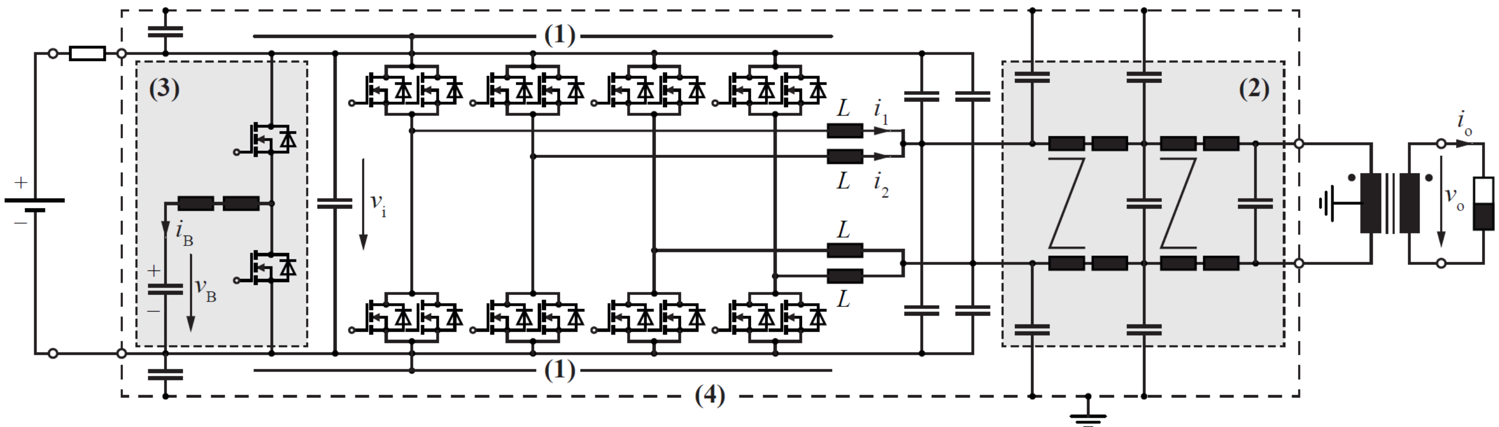
- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



→ Push the Forefront of New Technologies in R&D of High Power Density Inverters

Selected Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

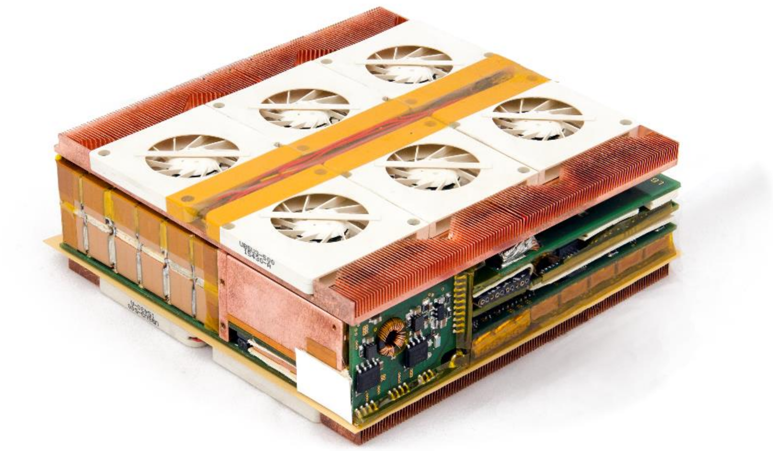


→ ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
→ Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

Little-Box 1.0 Prototype

- **Performance**
  - 8.2 kW/dm^3
  - 96,3% Efficiency @ 2kW
  - T_c=58°C @ 2kW

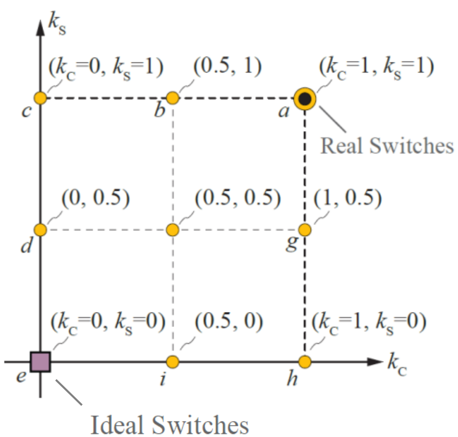
- **Design Details**
  - 600V IFX Normally-Off GaN GIT
  - Antiparallel SiC Schottky Diodes
  - Multi-Airgap Ind. w. Multi-Layer Foil Wdg
  - Triangular Curr. Mode ZVS Operation
  - CeraLink Power Pulsation Buffer

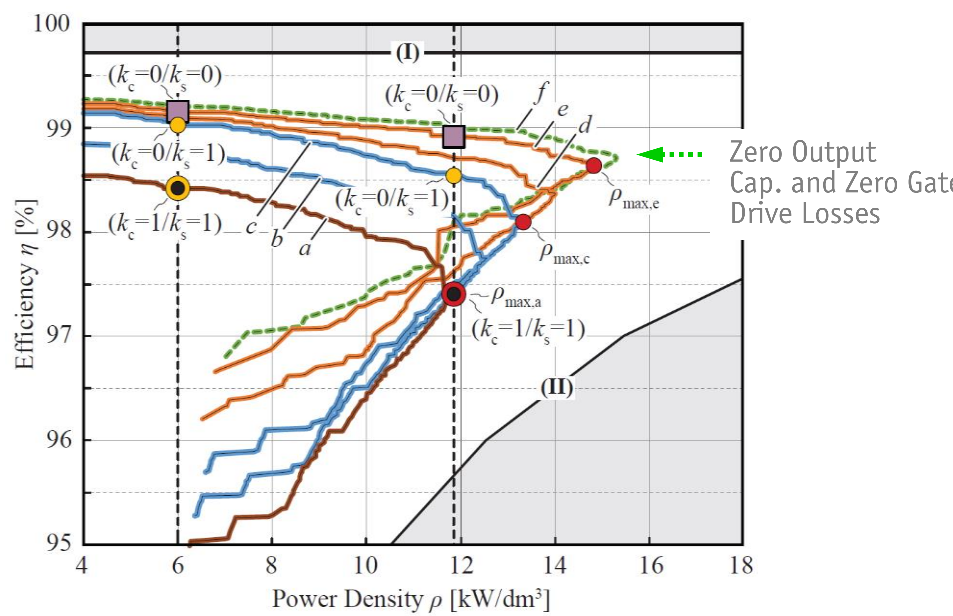


→ Analysis of Potential Performance Improvement for *Ideal Switches*

Little Box 1.0 @ Ideal Switches (TCM)

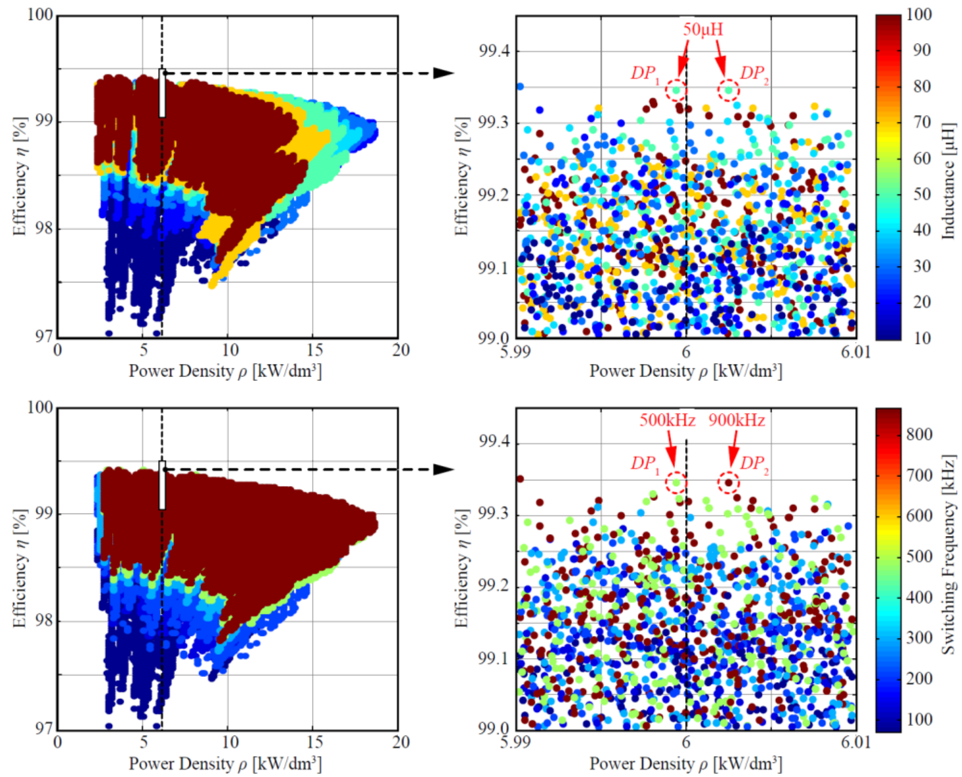
- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: k_C= 0 (Zero Cond. Losses); k_S= 0 (Zero Sw. Losses)





→ Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density
→ *The Ideal Switch is NOT Enough* (!)

Little Box 1.0 @ Ideal Switches (PWM)



ρ = 6kW/dm^3
η ≈ 99.35%

L = 50uH
f_S = 500kHz or 900kHz

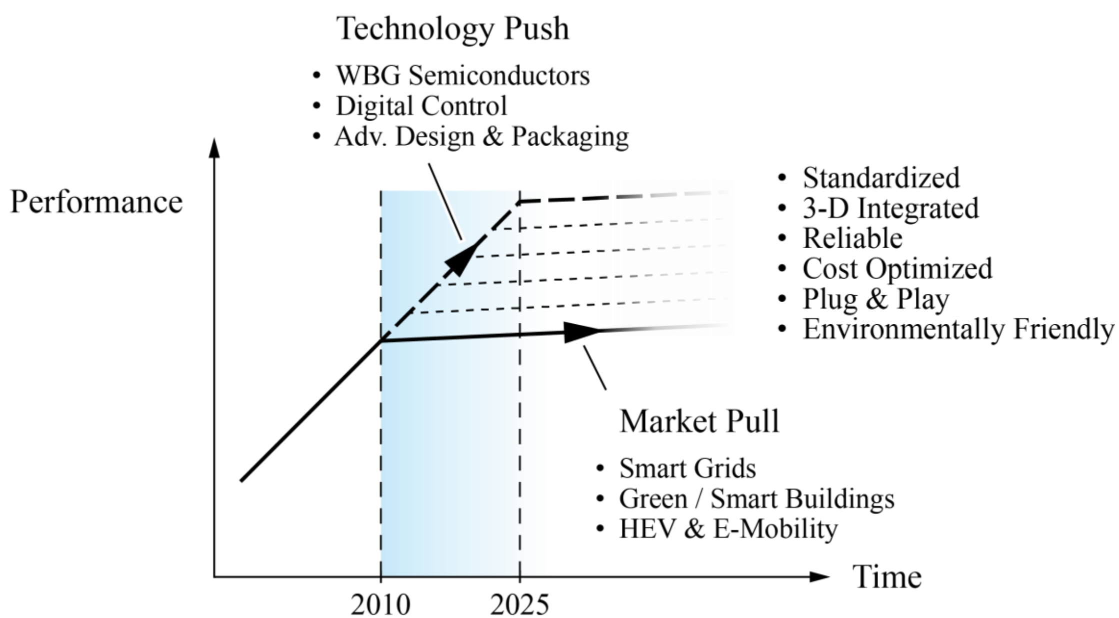
- L & f_S are Independent Degrees of Freedom
- Large Design Space Diversity (Mutual Compensation of HF and LF Loss Contributions)

Summary

Future Developments/Design Process
Future Research Topics
Power Electronics 2.0
Appendix

▶ Future Developments

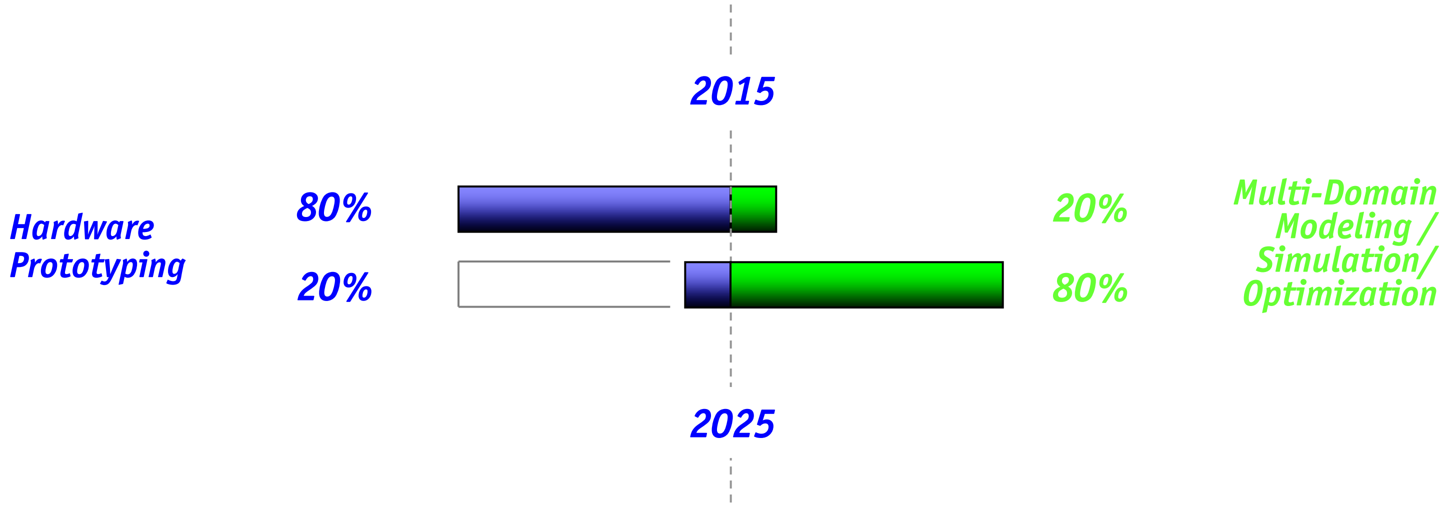
- Megatrends – Renewable Energy / Energy Saving / E-Mobility / “SMART” XXX
- Power Electronics will Massively Spread in Applications



→ More Application Specific Solutions
→ Mature Technology – Cost Optimization @ Given Performance Level
→ Design / Optimize / Verify (in Simulation) - Cheaper / Faster / Better

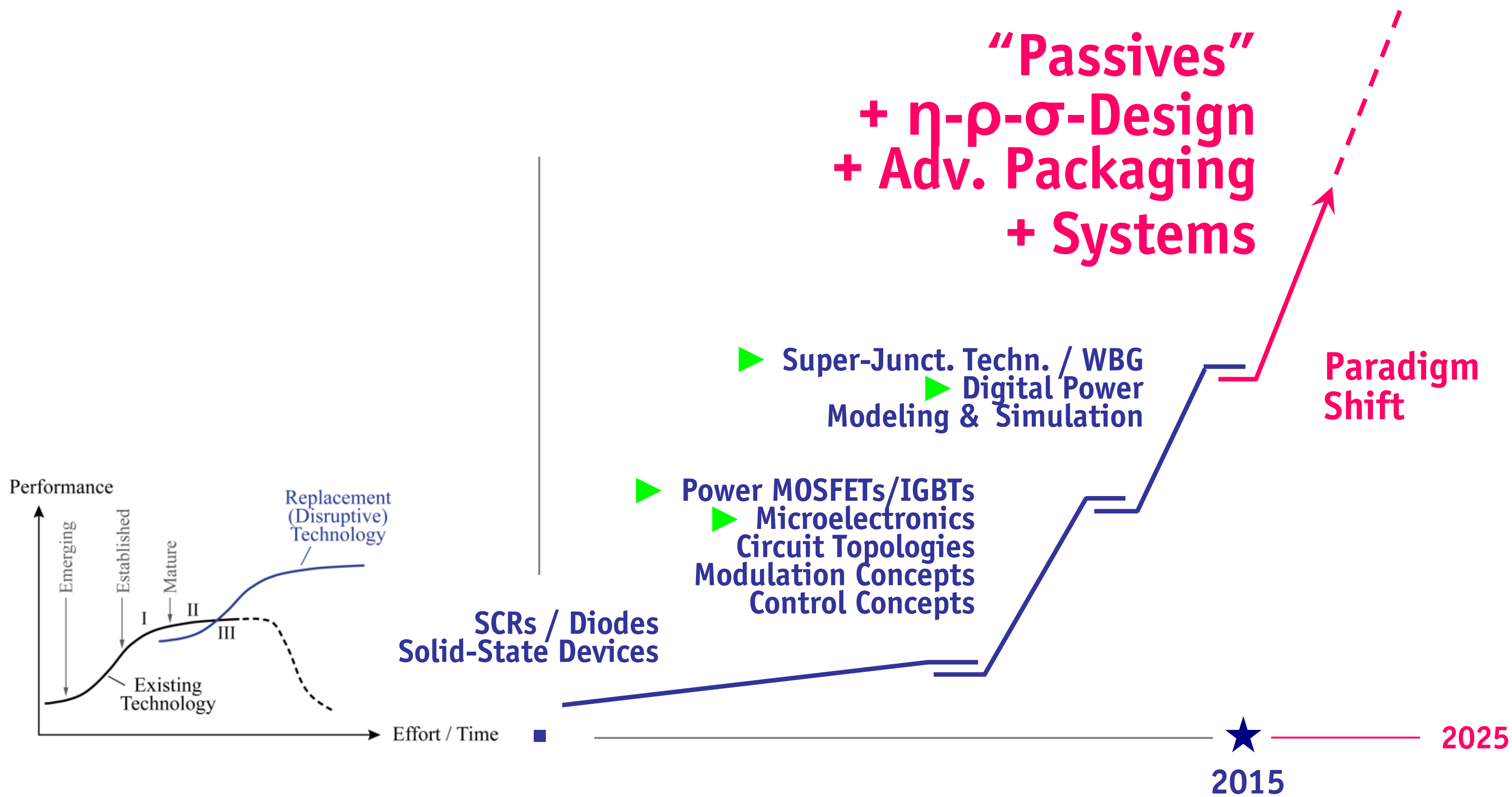
▶ Future Design Process

- Main Challenges: Modeling (EMI, etc.) & Implementation in Industry



→ Reduces Time-to-Market - Cheaper / Faster / Better
→ Allows to Understand Mutual Dependencies of Performances / Sensitivities (!)
→ Simulate What Cannot Any More be Measured (High Integration Level)

▶ Power Electronics Technology S-Curve



▶ Summary

- **Advantages**
  - Design / Optimize / Verify - All in Simulation
  - Provide a *Fully Virtual Design* for *Fully Automated Manufacturing*
  - Reduce Design Period from Weeks to Hours (Factor >100)
  - Directly Build Systems from Optimiz. Results (3D Printing etc.)
  - Pre-Analyze Improvement by New Technologies ("Research Efficiency")
  - Optimize over Extreme Span (Semicond. Doping to Conv. Mission Profile)
  - Free Adjustment of Optimization Criteria (Design on Demand)
- **Research Topics**
  - Reduced Order Models / Model Accuracy
  - Opt. Combination of Analytical & FEM Models
  - Partitioning of Optimiz. (Local/Global Variables & Optimiz. etc.)
  - Selection of Abstraction Level / Timescale /
  - Translation of Geometries into Model Parameters (e.g. EMI)
  - Consideration of Geometric Limitations (Design for Manufact.)
  - New Models for Highly Integr. Converters (Strong EM & Therm. Coupl.)
  - Convergence of Simulations & Measurements (Autom. Param. Adj.)
  - Visualization of Optim. Results / Interfaces (Programming & Results)
- **Challenges**
  - Introduction in Industry (and Academia ;-))
  - Company-Wide Updates / Maintenance
  - Integration in "Virtual Prototyping" Environment
- **Limitations**
  - Simulation Extends the Knowledge Space ... **But,...** Cannot Create Fundamentally New Concepts (!)

***Future
Paradigm
Shift***

▶ Power Electronics 2.0

- Design Considering Converters as "Integrated Circuits" (PEBBs)
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

- "Converter" → "Systems" (Microgrid) or "Hybrid Systems" (Automation / Aircraft)
- "Time" → "Integral over Time"
- "Power" → "Energy"

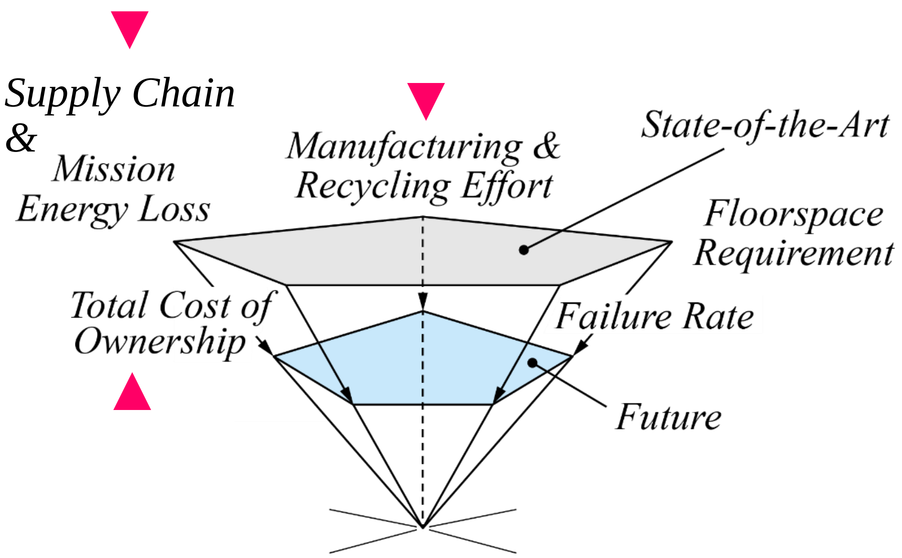
$$p(t) \quad \rightarrow \quad \int_0^t p(t)\,\mathrm{d}t$$

- Power Conversion → Energy Management / Distribution
- Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
- Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
- Cap. Filtering → Energy Storage & Demand Side Management
- Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
- etc.

► New Power Electronics Systems Performance Figures/Trends

■ Complete Set of New Performance Indices

— Power Density [kW/m²]
— Environm. Impact [kWs/kW]
— TCO [$/kW]
— Mission Efficiency [%]
— Failure Rate [h^{-1}]



Thank You !

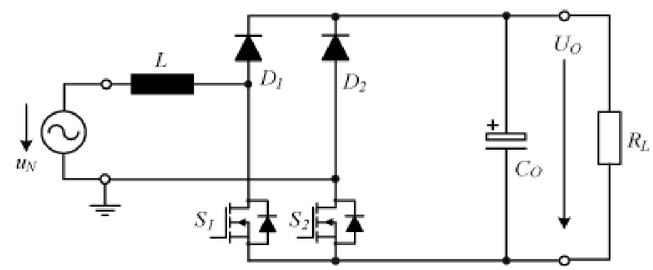
Appendix #1

Determination of the η-ρ-Pareto Front →

► Determination of the η-ρ-Pareto Front (1)

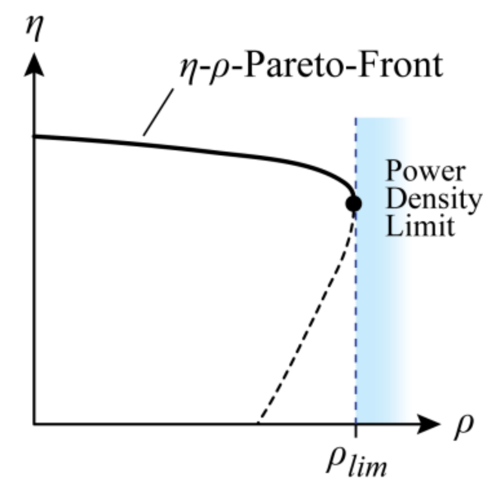
■ Comp.-Level Degrees of Freedom of the Design

— Core Geometry / Material
— Single / Multiple Airgaps
— Solid / Litz Wire, Foils
— Winding Topology
— Natural / Forced Conv. Cooling
— Hard-/Soft-Switching
— Si / SiC
— etc.
— etc.
— etc.



■ System-Level Degrees of Freedom

— Circuit Topology
— Modulation Scheme
— etc.
— etc.
— etc.

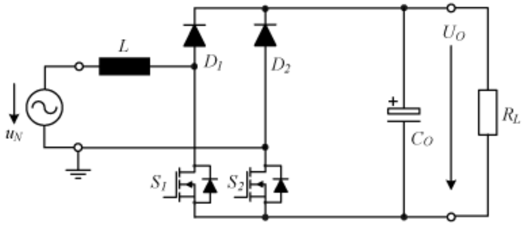


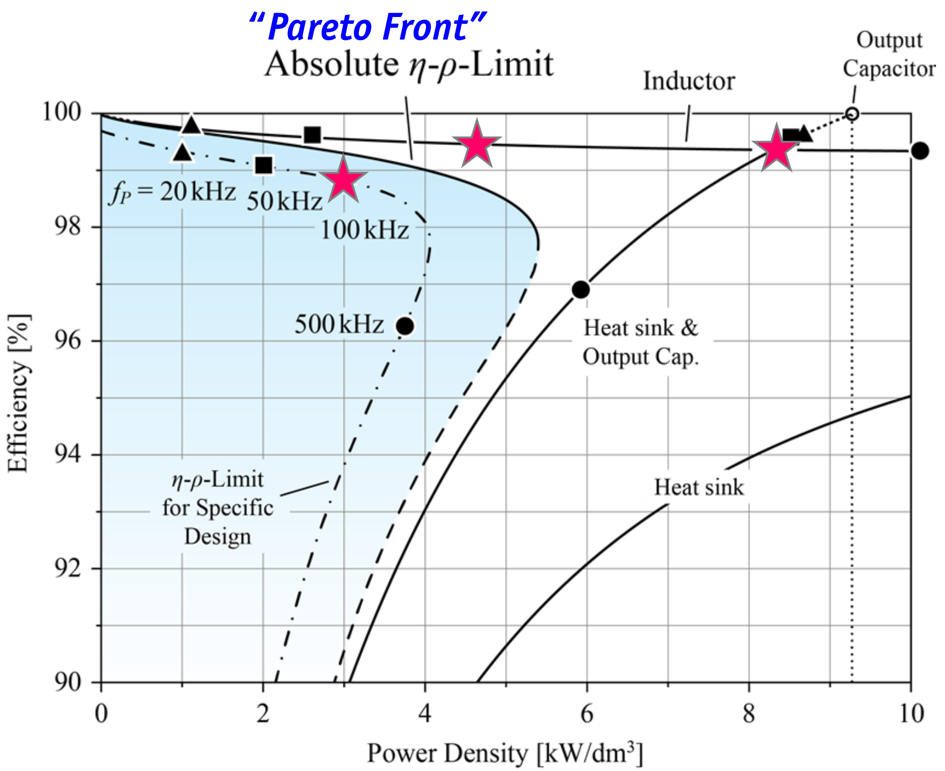
■ Only η-ρ-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)

► Determination of the η-ρ-Pareto Front (1)

- Specific Design → Only f_P as Variable Design Parameter
- Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute η-ρ-Performance Limit

★ f_P =100kHz





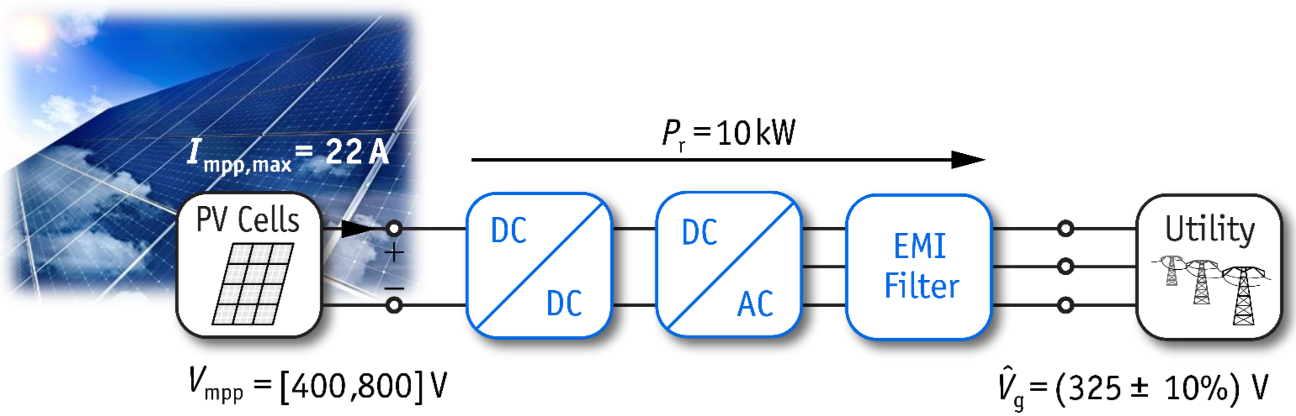
Appendix #2

**Performance & Life-Cycle-
Costs of SiC vs. Si** →

► Multi-Objective η-ρ-σ-Comparison of *Si vs. SiC*

■ Three-Phase PV Inverter System

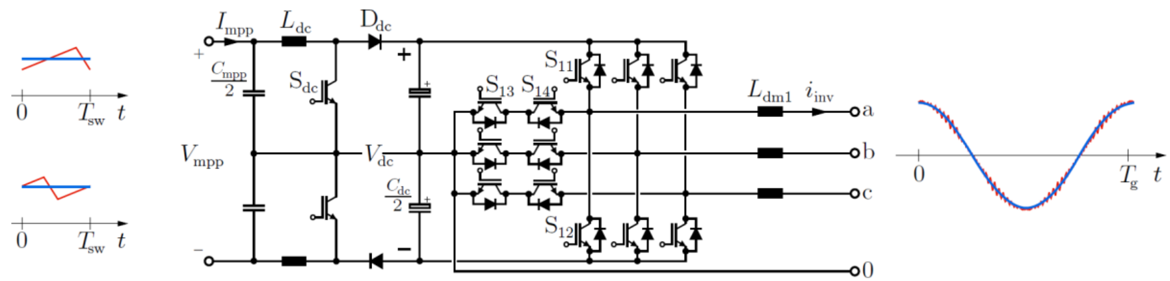
— Single-Input/Single-MPP-Tracker Multi-String PV Converter
— DC/DC Boost Converter for Wide MPP Voltage Range
— Output EMI Filter
— Typical Residential Application



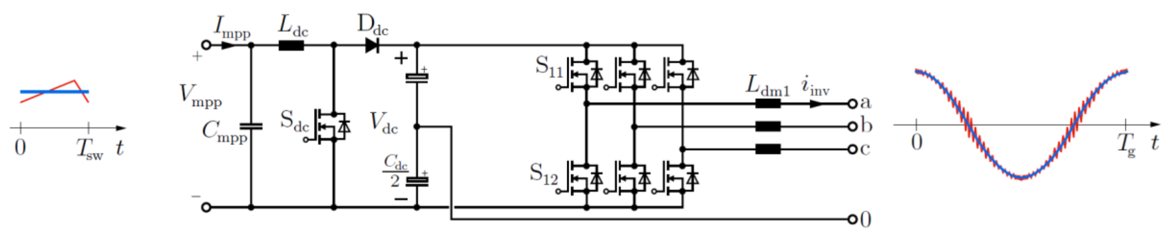
→ Exploit Excellent Hard- AND Soft-Switching Capabilities of SiC
→ Find Useful Switching Frequency and Current Ripple Ranges
→ Find Appropriate Core Material

▶ Topologies - Converter Stages

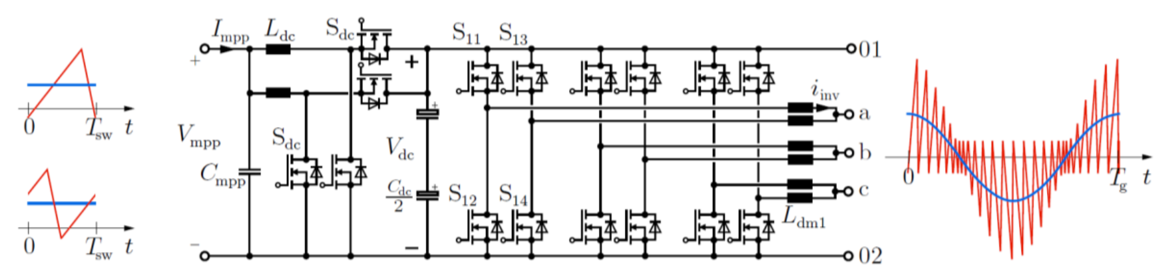
- **Si IGBT 2L-PWM Inverter**



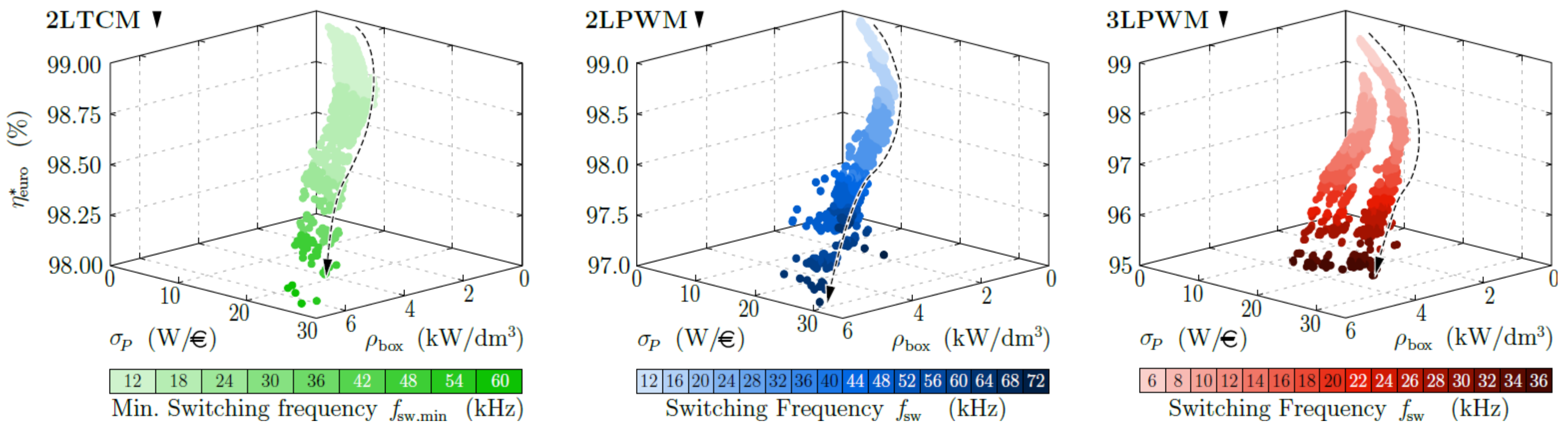
- **SiC MOSFET 2L-PWM Inverter**



- **SiC MOSFET Interleaved 2L-TCM Inverter**



▶ Optimization Results - Pareto Surfaces



- No Pareto-Optimal Designs for $f_{sw,min}$ > 60 kHz
- No METGLAS Amorphous Iron Designs

- Pareto-Optimal Designs for Entire Considered f_{sw} Range
- No METGLAS Amorphous Iron Designs

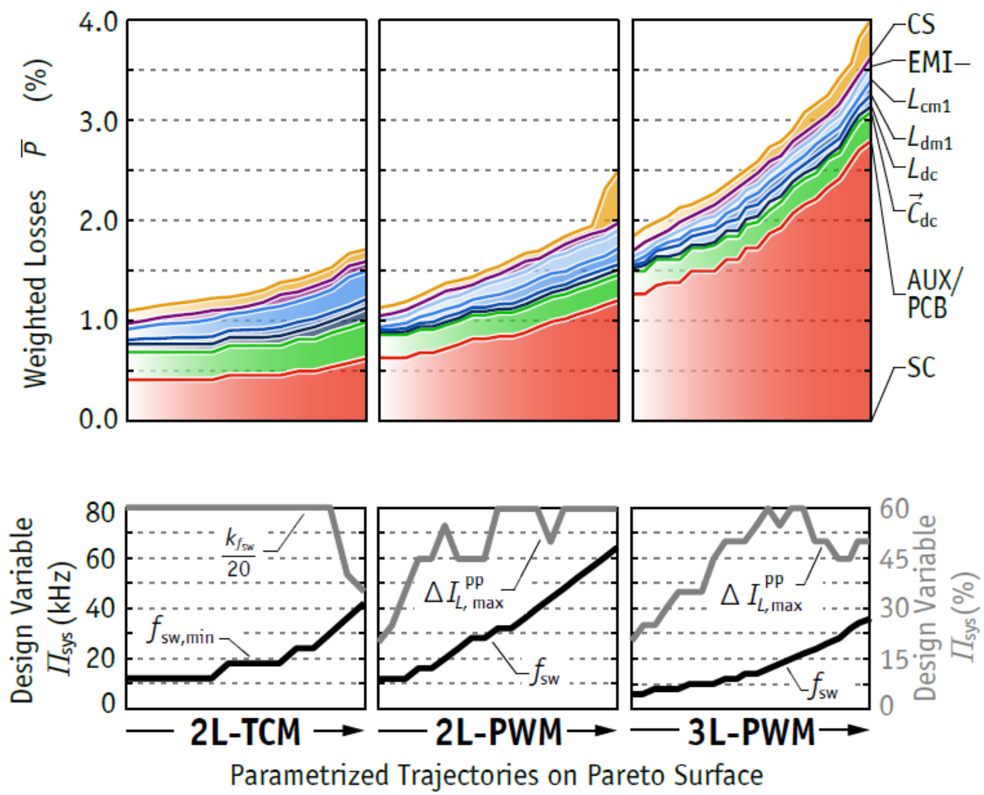
- Pareto-Optimal Designs for Entire Considered f_{sw} Range
- METGLAS Amorphous Iron and Ferrite Designs

▶ Optimization Results – Investigations Along Pareto Surfaces

■ **Comparison of the Inverter Concepts**

	η	ρ	σ
• 2L-TCM	🙂	🙂	☹
• 2L-PWM	😐	😐	🙂
• 3L-PWM	☹	☹	🙂

→ **Semiconductor Losses Clearly Dominating (35…70%)**



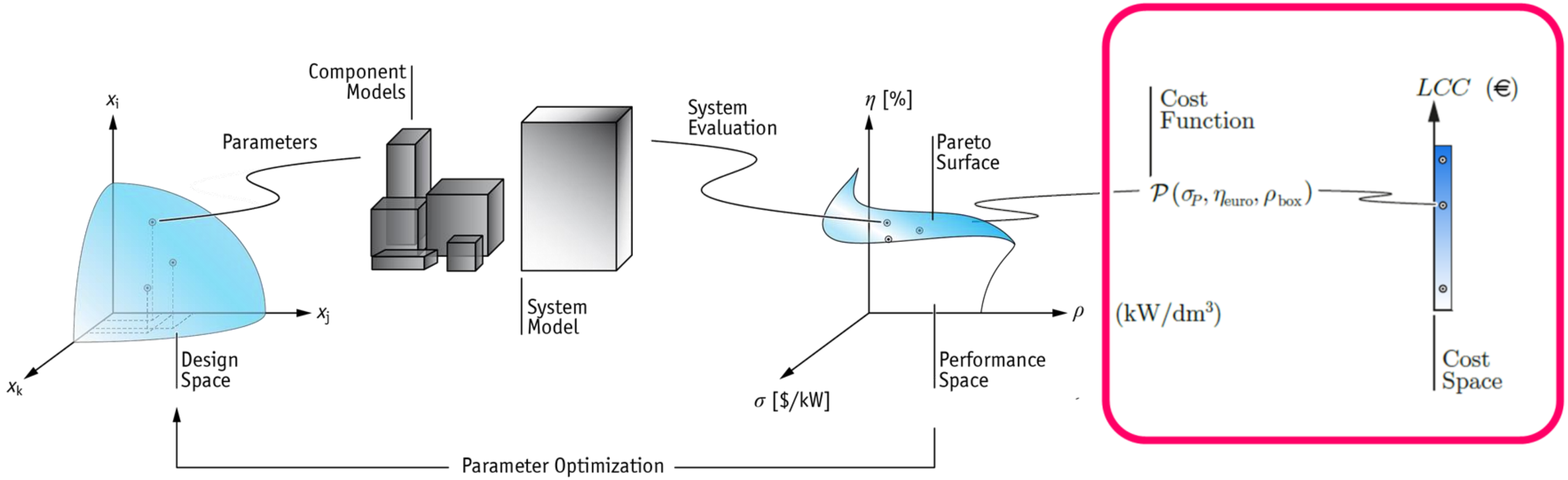
▶ Extension to *Life-Cycle Cost (LCC) Analysis*

- **Performance Space Analysis**

— 3 Performance Measures: η, ρ, σ
— Reveals Absolute Performance Limits / Trade-Offs Between Performances

- **LCC Analysis**

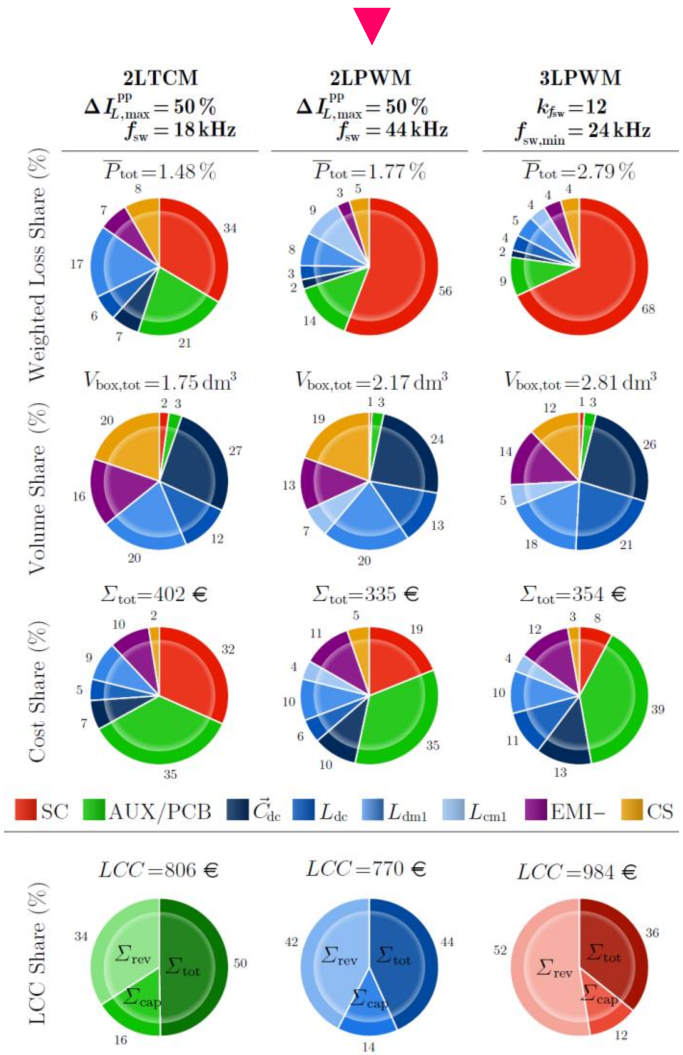
— Post-Processing of Pareto-Optimal Designs
— Determination of Min.-LCC Design
— Arbitrary Cost Function Possible



→ Which is the Best Solution Weighting η, ρ, σ, e.g. in Form of Life-Cycle Costs (LCC)?
→ How Much Better is the Best Design?
→ Optimal Switching Frequency?

▶ Post-Processing

■ LCC – Analysis



■ **Best System - 2L-PWM SiC Converter @ 44kHz & 50% Ripple**

— 22% Lower LCC than 3L-PWM
— 5% Lower LCC than 2L-TCM
— Simplest Design
— Probably Highest Reliability
— Lower Vol. (Housing) Not Yet Considered!

→ Application of SiC Justified on "System Level"

- **End**