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DAPE
Design Automation for Power Electronics

IEEE Design Automation for Power Electronics Workshop

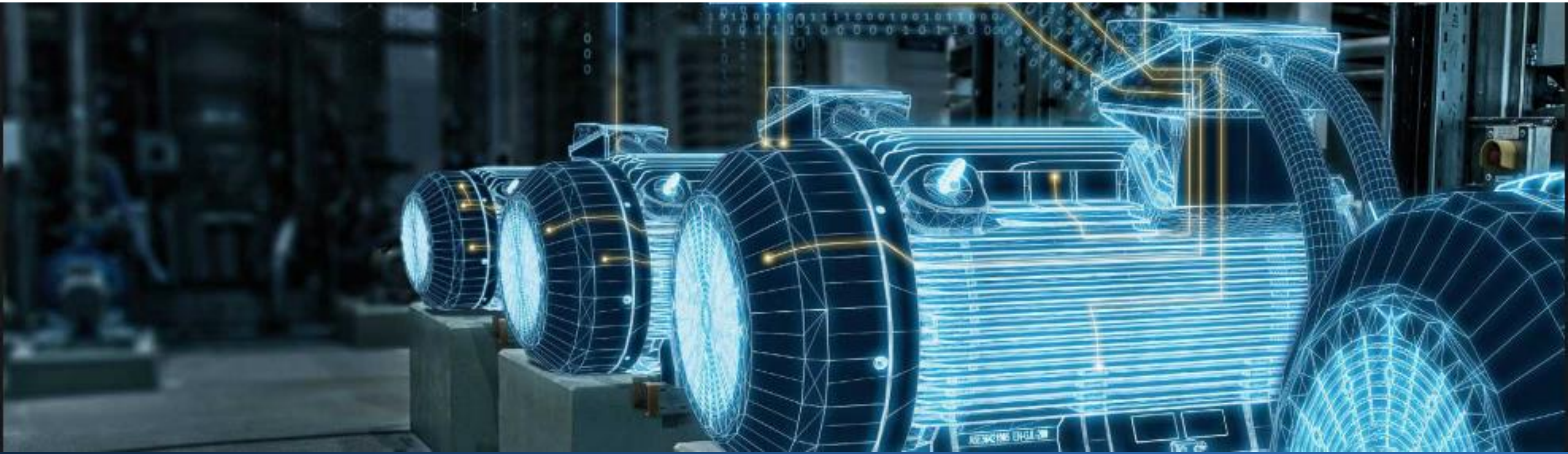
Power Electronics Design 4.0

Johann W. Kolar

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

Sept. 22, 2018

Source: SIEMENS



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Source: SIEMENS

Outline

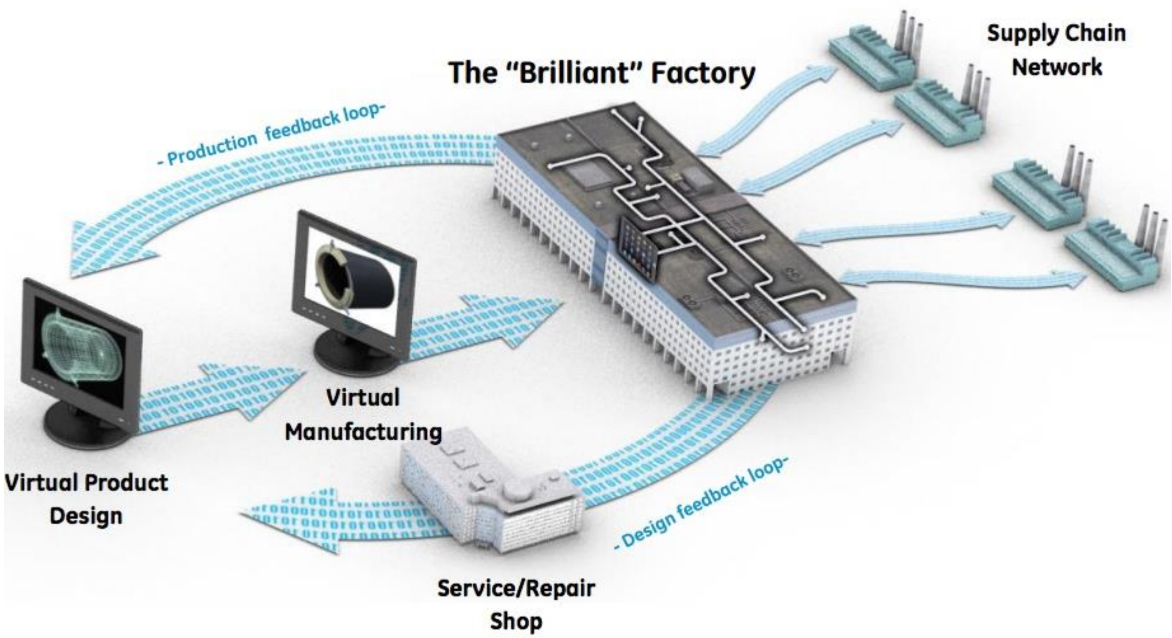
- *Digital Transformation*
- *Power Electronics Performance Trends*
- *Model-Based Design/Evaluation/Operation*
- *Conclusions*

Digitization
Digitalization
Digital Transformation

Digital Thread
Digital Twins
"Virtual Environment"
Power Electronics 4.0

Digital Transformation (1)

- **Digitization** → Convert Information Written on Paper into Digital Format
- **Digitalization** → Compiled Digitized Information Introduced in Standard Processes

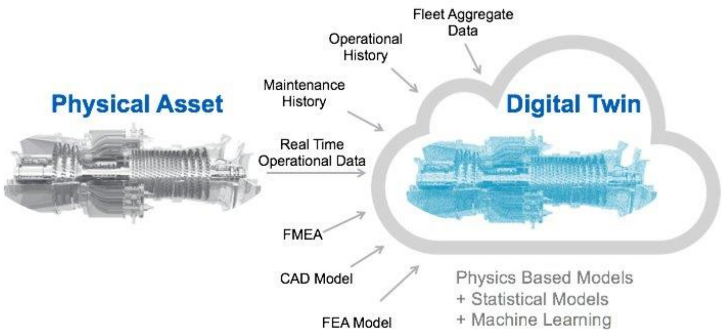


Source: GE

▶ **Digital Transformation** → Digitized Data & Digitalized Applications Used for "Virtualization"

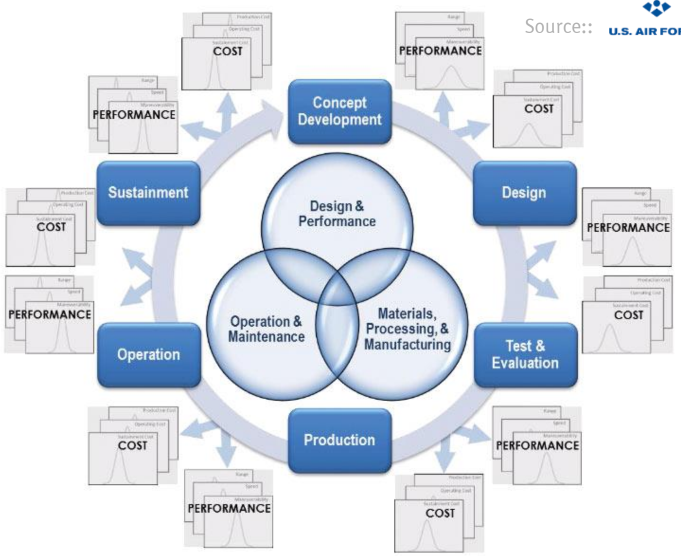
Digital Transformation (2)

- **Digital Thread** → **Cont. Bidir. Data Path** Linking Simulation Model/Manufacturing/Testing etc.
  → Originally Developed by Lockheed Martin for 3D-CAD Data → CNC Machines
- **Digital Twin** → **Phys.-Based Dig. Mirror Image** of Planned & Manufact. Product **w. Bidir. Data Link**
  → Holds Data from Design, Prototype, Finished Product, Operation etc.
  → Real-Time Assessment of System´s Curr. & Future Abilities



Source: www.railwayage.com

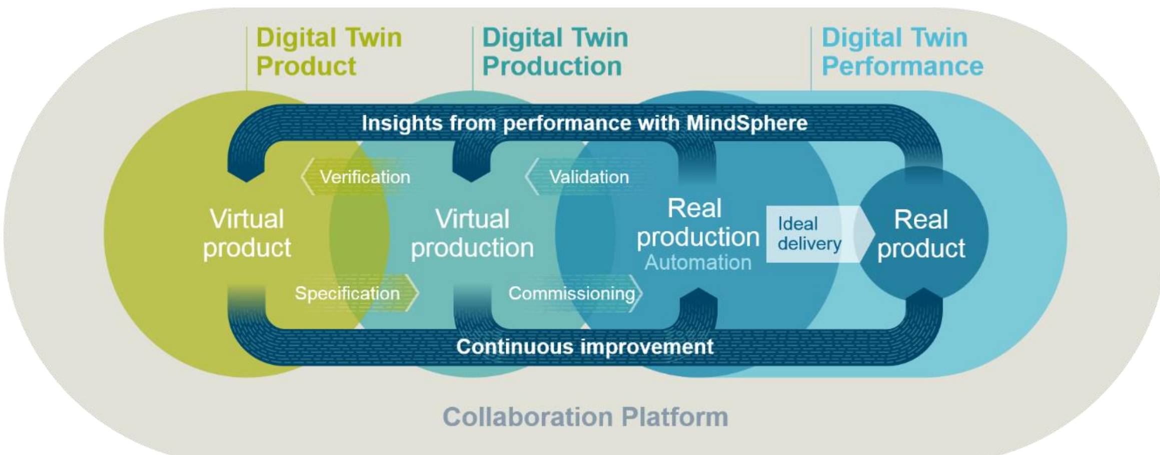
Source:: U.S. AIR FORCE



▶ "End-to-End Model-Based" → Specific./Design/Manufact./Test/Operation/Monitoring/ Recycling
▶ Targeting *Zero Distance* of Digital (Virtual) Representation and Physical Realization

Digital Transformation (3)

- *Digital Thread / Digital Twin* → "Weaving" Real/Physical & Virtual World Together
- *"Digital Birth Certificate"* → Each Part/Machine to Keep Track Through Whole Lifetime
- Fully Digital Product Lifecycle → "Digital Tapestry" (Lockheed Martin)

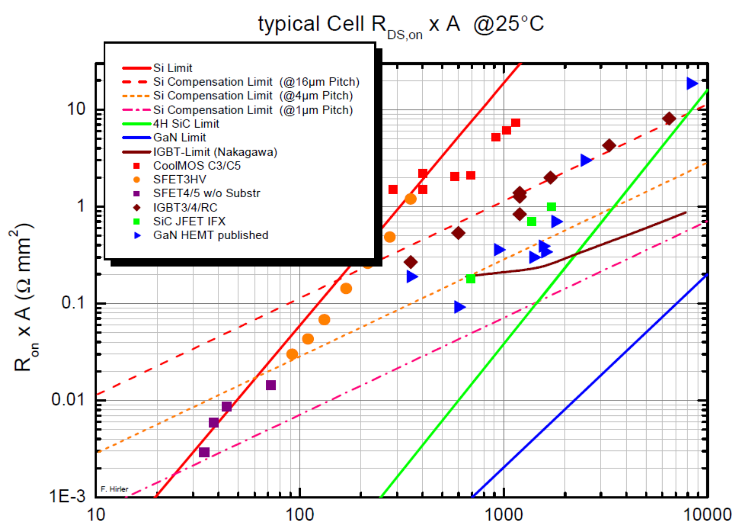


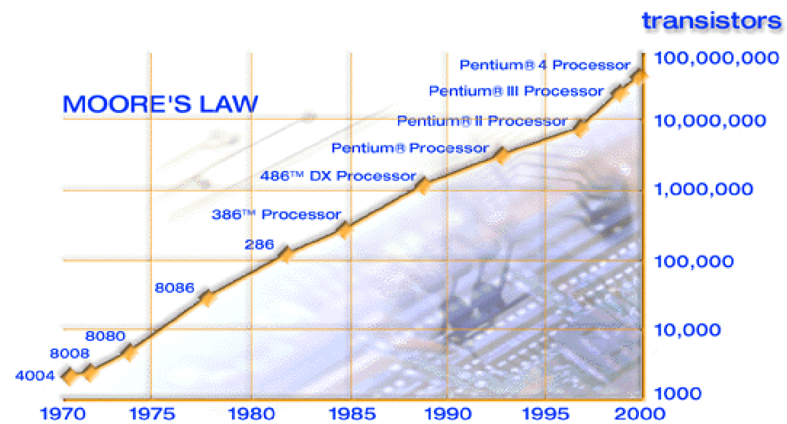
Source: SIEMENS

- *Future Power Electronics Models/Design* → To be Embedded in this Virtual Environment!
- Smart Components Integr. Sensors Connect to Dig. Twin → Design Improv. / Prev. Maintenance etc.

Power Electronics – *Technology Push*

- WBG Semiconductor Technology → Higher Efficiency, Lower Complexity
- Microelectronics → More Computing Power



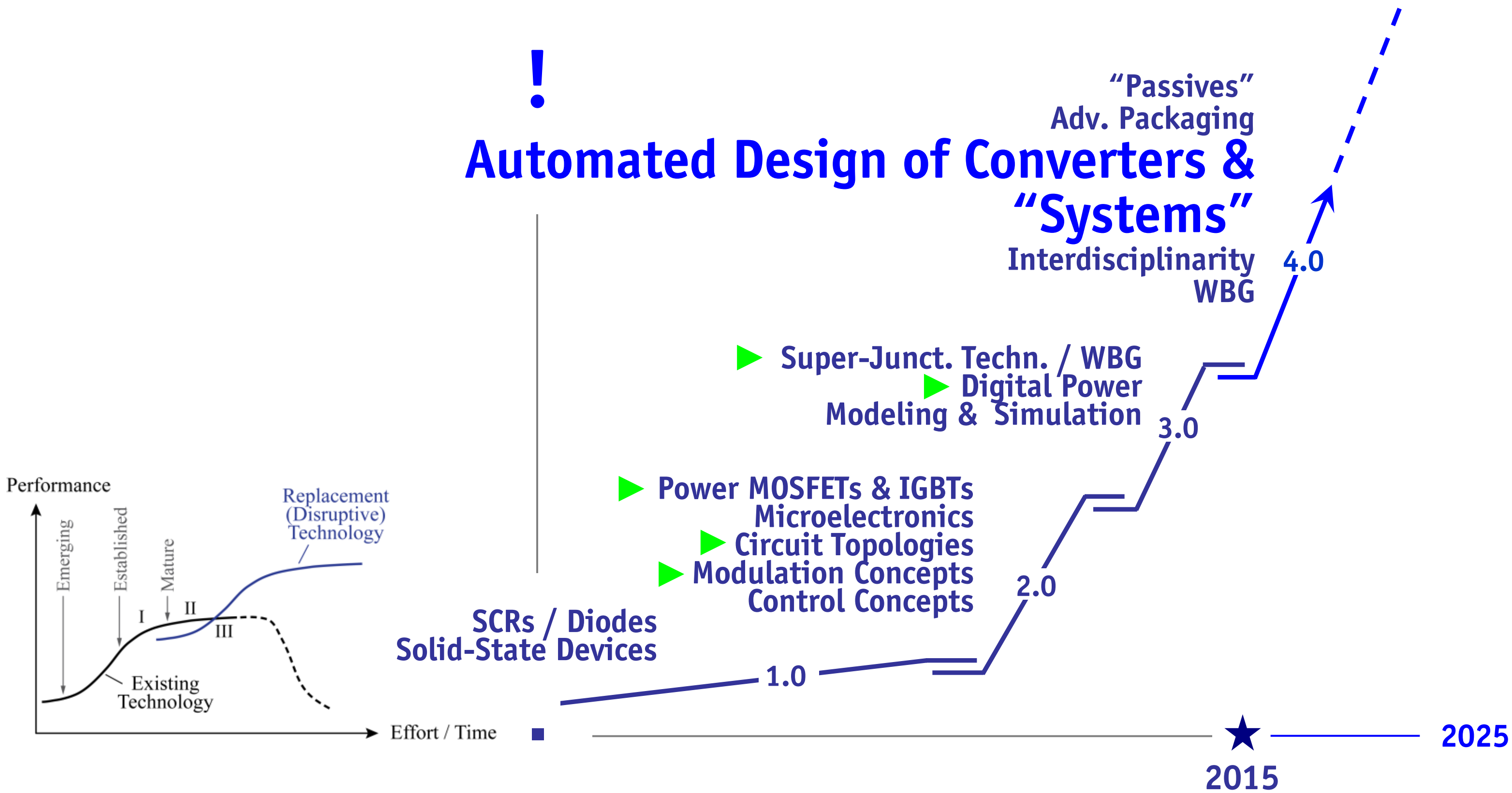


→ + Advanced Packaging (!)

→ Moore's Law

Power Electronics Technology S-Curve

- Power Electronics 4.0

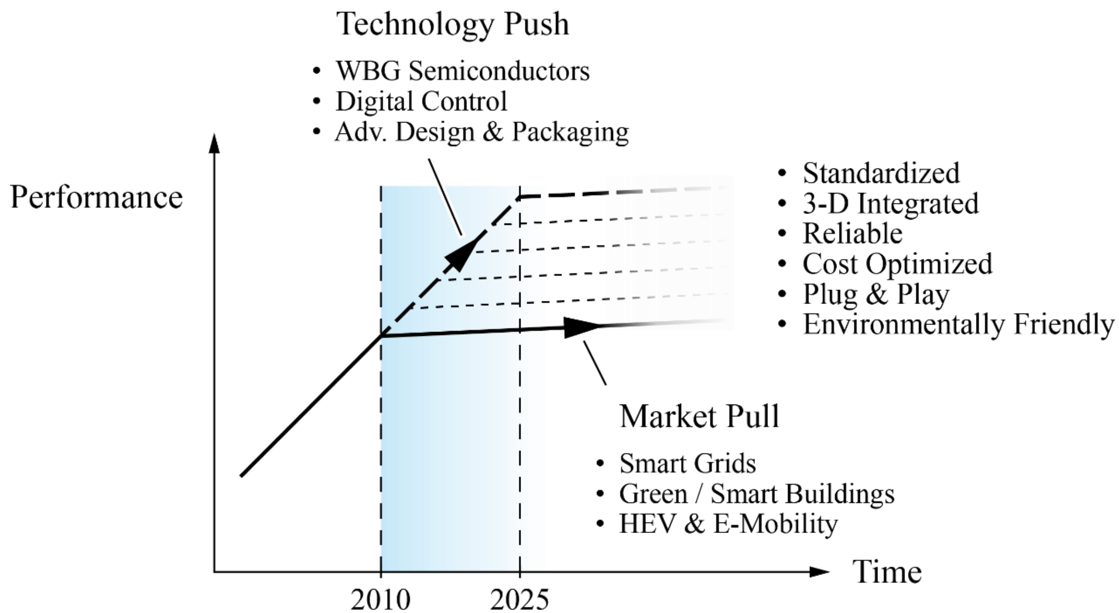


Power Electronics Design

Requirements
Design Challenges
Design Abstraction
Multi-Obj. Optimiz. (State-of-the-Art)
Results

Future Development (1)

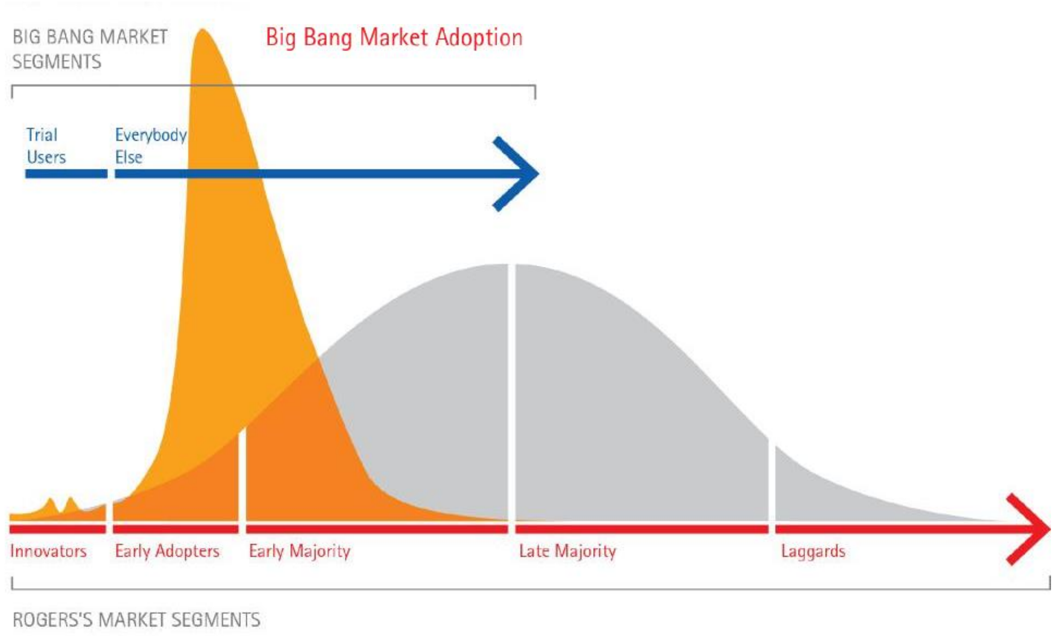
- Megatrends – Renewable Energy / Energy Saving / E-Mobility / "SMART XXX"
- Power Electronics will Massively Spread in Applications



→ More Application Specific Solutions
→ Cost Optimization @ Given Performance Level for Standard Solutions
→ More Specific Requirements – High Peak/Avg. Ratio, Wide Volt. Range etc.
→ Design / Optimize / Verify (All in Simulation) - Faster / Cheaper / Better

Future "Big-Bang" Disruptions

- "Catastrophic" Success of Disruptive New (Digital) Technologies
- No Bell-Curve Technology Adoption / Technology S-Curve
- "Shark Fin"-Model



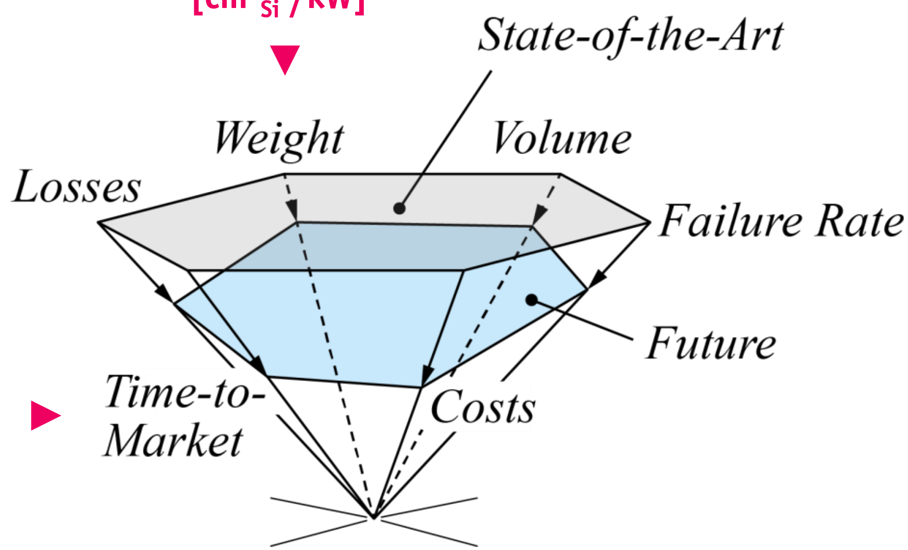
Source: www.verschuerent.wordpress.com
February 2015

See also:
Big Bang Disruption – Strategy in the Age of Devastating Innovation, L. Downes and P. Nunes

► Consequence: Market Immediately & Be Ready to Scale Up — and Exit — Swiftly (!)

Required Power Electronics Performance Improvements

Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

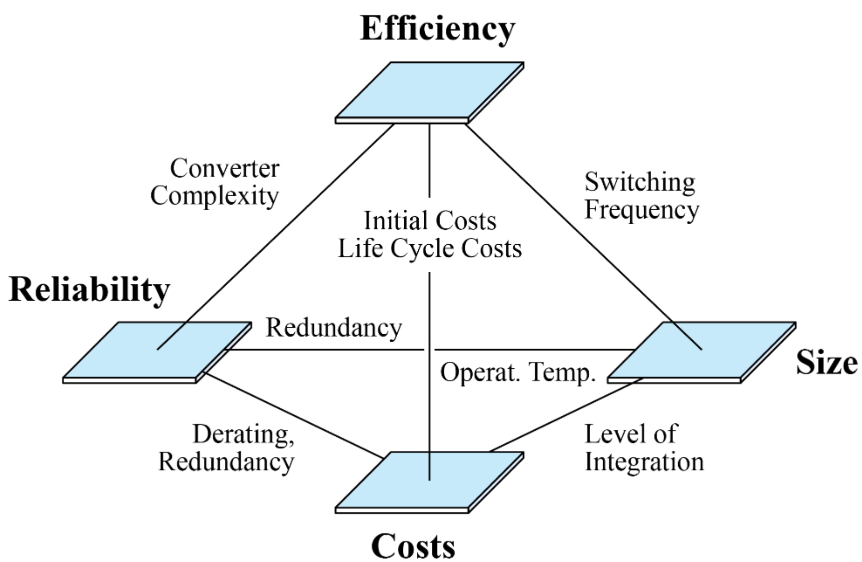


- **Performance Indices**

  - Power Density [kW/dm^3]
  - Power per Unit Weight [kW/kg]
  - Relative Costs [kW/$]
  - Relative Losses [%]
  - Failure Rate [h^{-1}]

Multi-Objective Design Challenge (1)

- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices → Trade-Offs



▶ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
▶ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

Multi-Objective Design Challenge (1)

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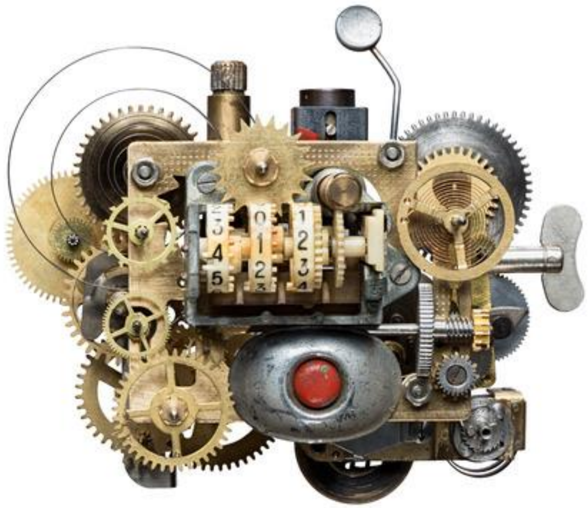
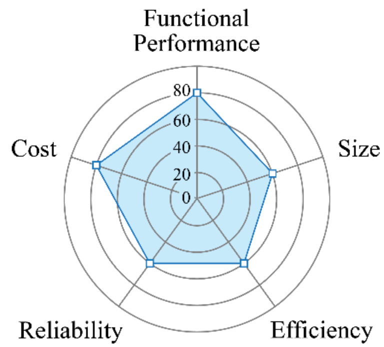


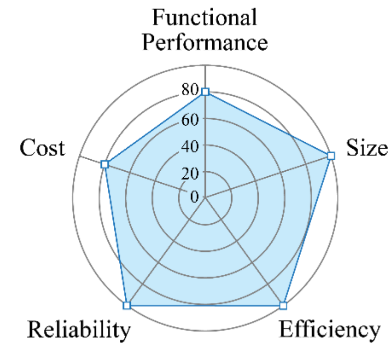
► Large Number of Degrees of Freedom / Multi-Dimensional Design Space
► Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

Multi-Objective Design Challenge (2)

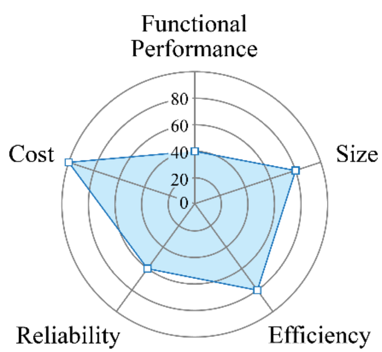
- Specific Performance Profiles / Trade-Offs Dependent on Application



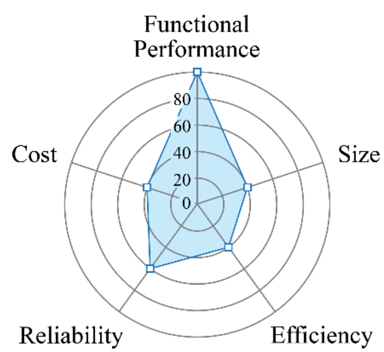
Industry Applications



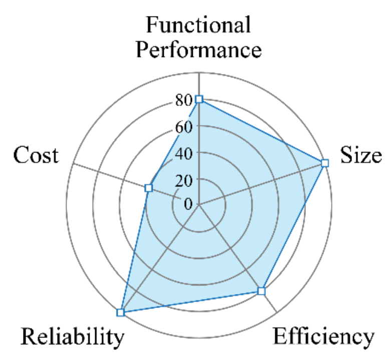
Information & Communication Industry



Domestic Applications



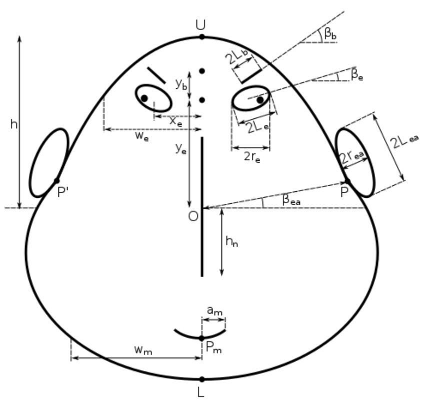
Laboratory Applications

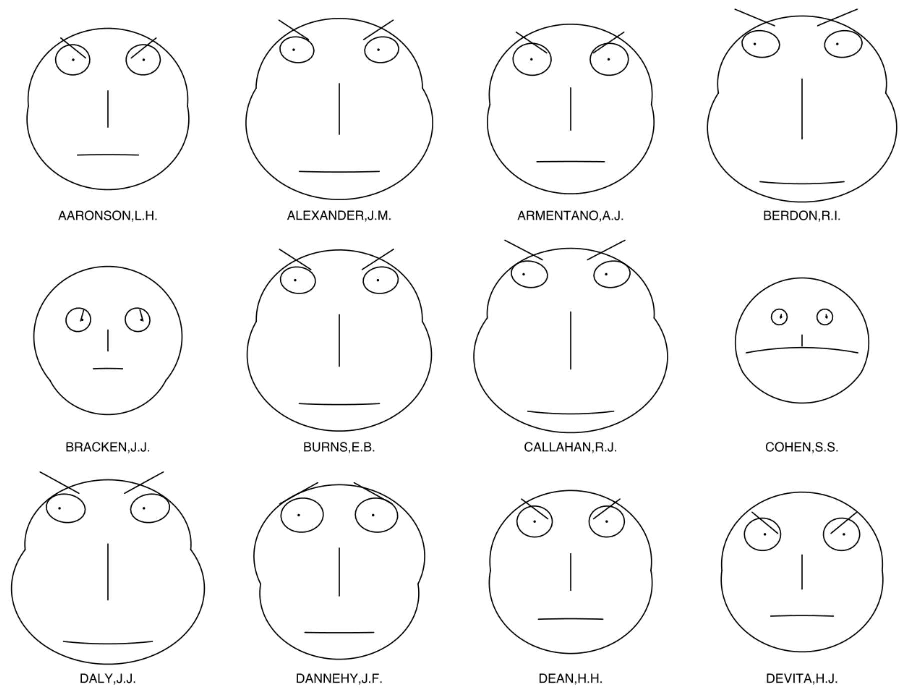


Aerospace Applications

Remark: Visualization of Multiple Performances ;-)

- Spider Charts, etc.
- Chernoff-Faces





► H. Chernoff (Stanford): "The Use of Faces to Represent Points in K-Dimensional Space Graphically"

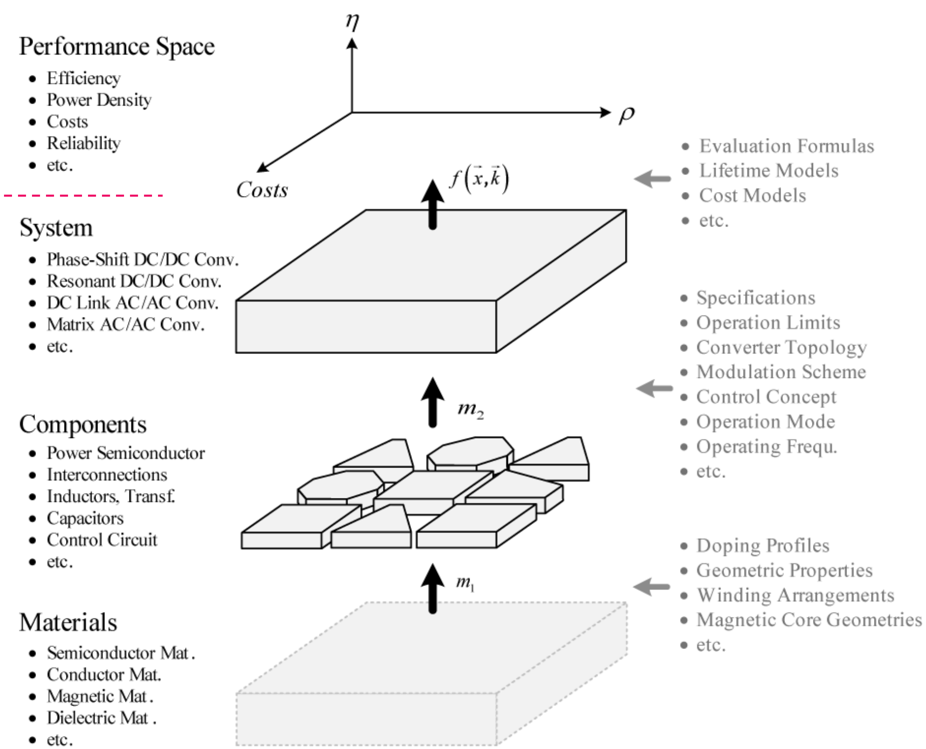
Multi-Objective Optimization

Abstraction of Converter Design
Design Space / Performance Space
Pareto Front
Sensitivities / Trade-Offs

Abstraction of Power Converter Design

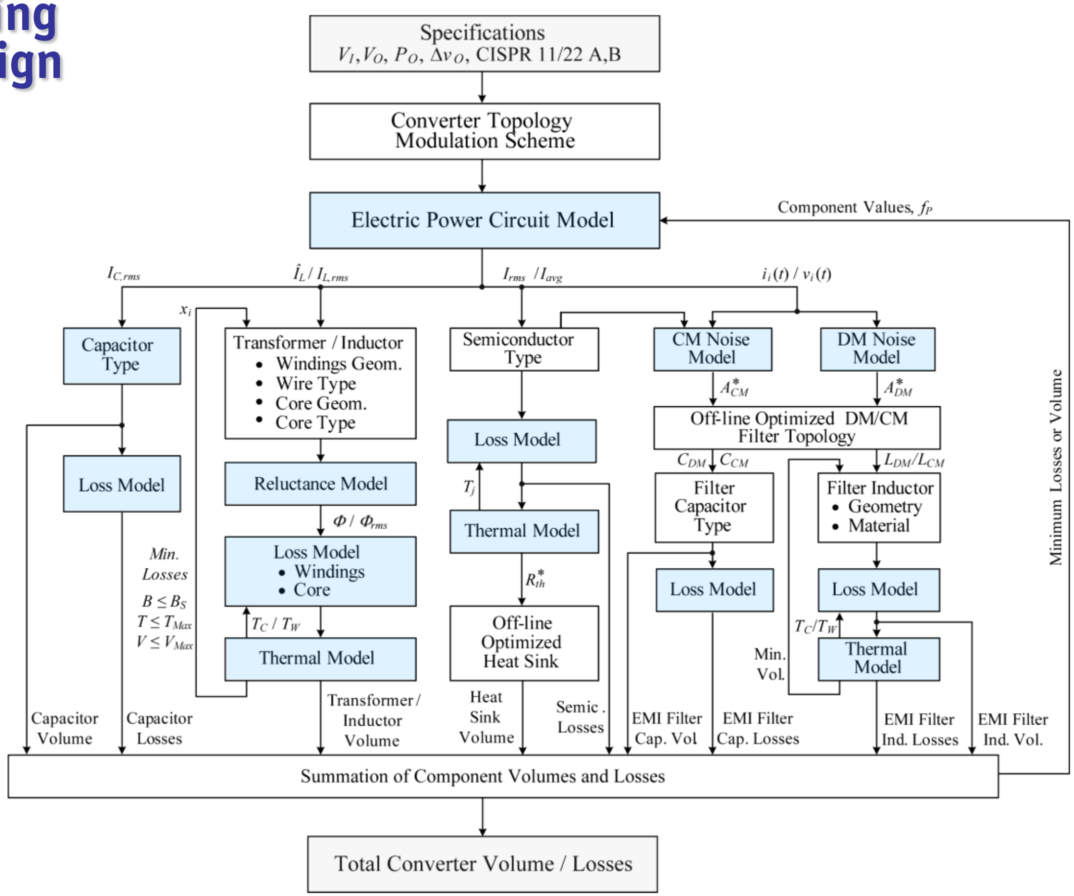
Performance Space

Design Space



► *Mapping* of "*Design Space*" into System "*Performance Space*"

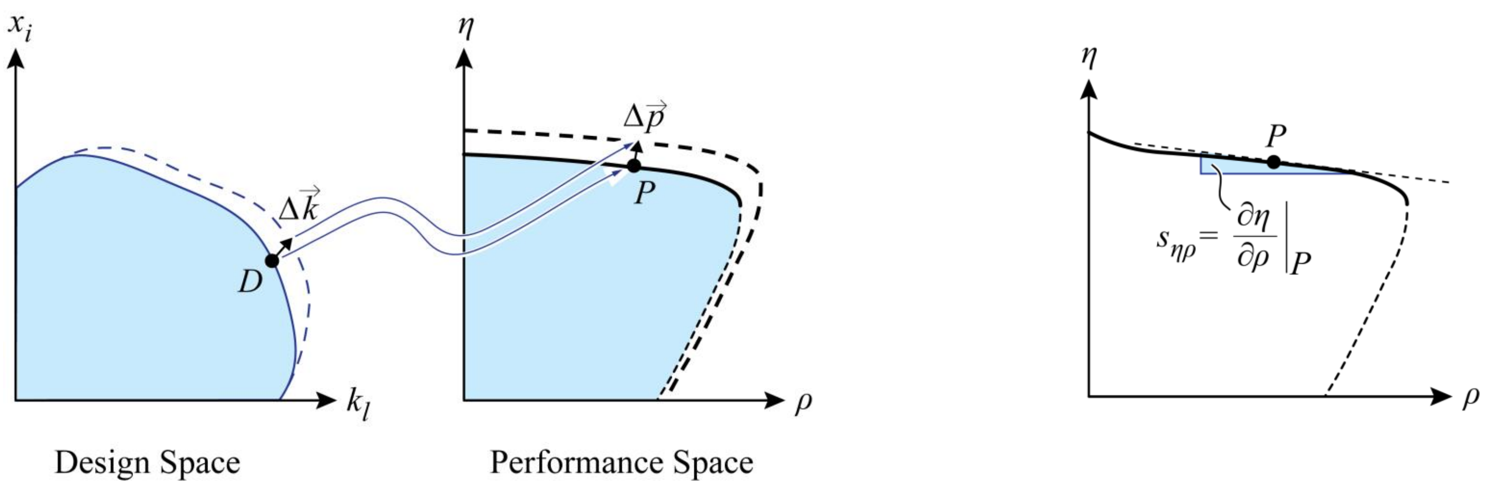
Mathematical Modeling of the Converter Design



► **Multi-Objective Optimization – *Guarantees Best Utilization of All Degrees of Freedom* (!)**

Multi-Objective Optimization (1)

- Ensures Optimal Mapping of the "Design Space" into the "Performance Space"
- Identifies Absolute Performance Limits → Pareto Front / Surface

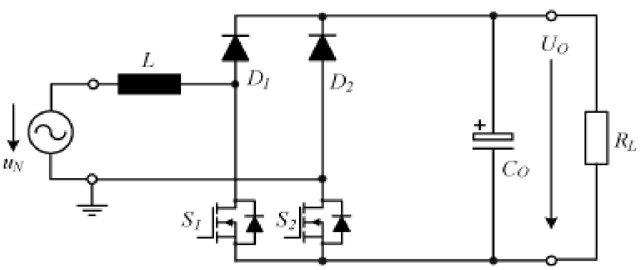


- ► Clarifies Sensitivity $\Delta\vec{p} \,/\, \Delta\vec{k}$ to Improvements of Technologies
- ► Trade-off Analysis

Determination of the η-ρ-Pareto Front (a)

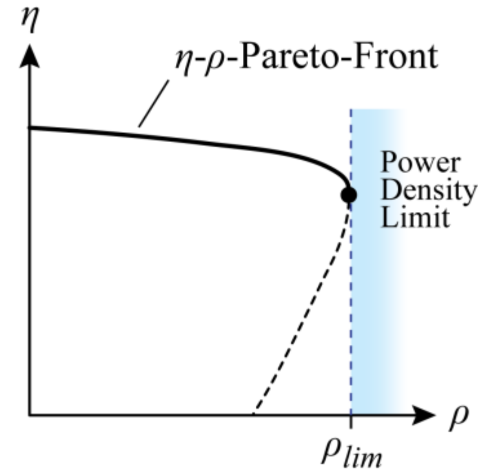
- **Comp.-Level Degrees of Freedom of the Design**

— Core Geometry / Material
— Single / Multiple Airgaps
— Solid / Litz Wire, Foils
— Winding Topology
— Natural / Forced Conv. Cooling
— Hard-/Soft-Switching
— Si / SiC
— etc.
— etc.
— etc.



- **System-Level Degrees of Freedom**

— Circuit Topology
— Modulation Scheme
— Switching Frequ.
— etc.
— etc.

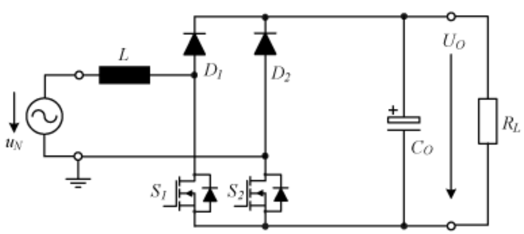


- **Only η-ρ-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)**

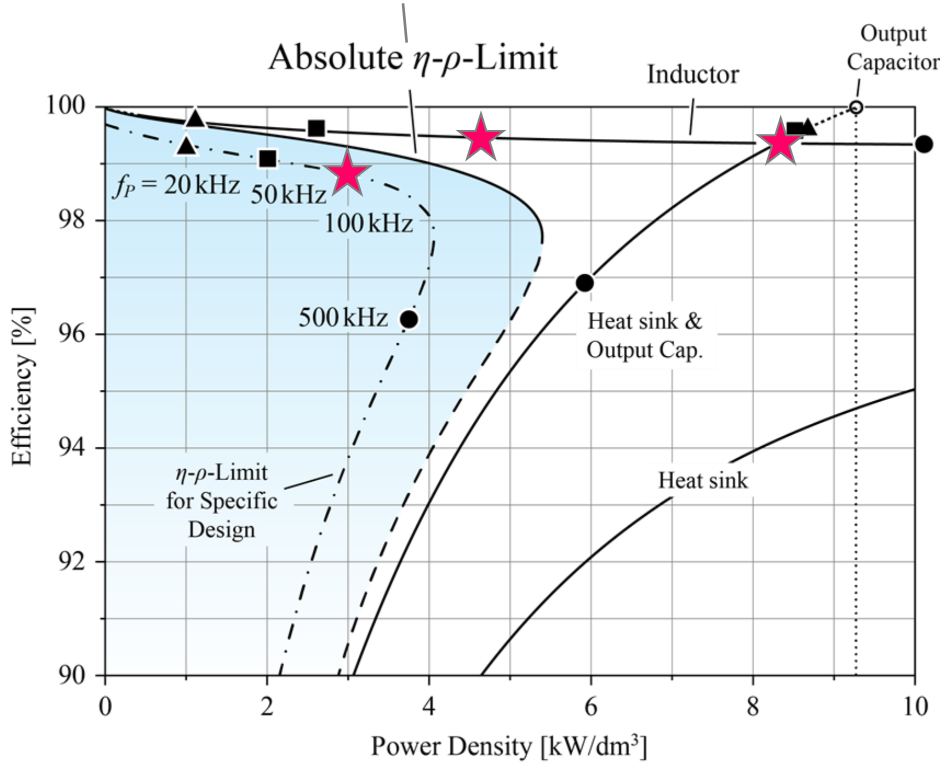
Determination of the η-ρ-Pareto Front (b)

- Example: Consider Only f_P as Design Parameter
- Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute η-ρ-Performance Limit

★ f_P =100kHz

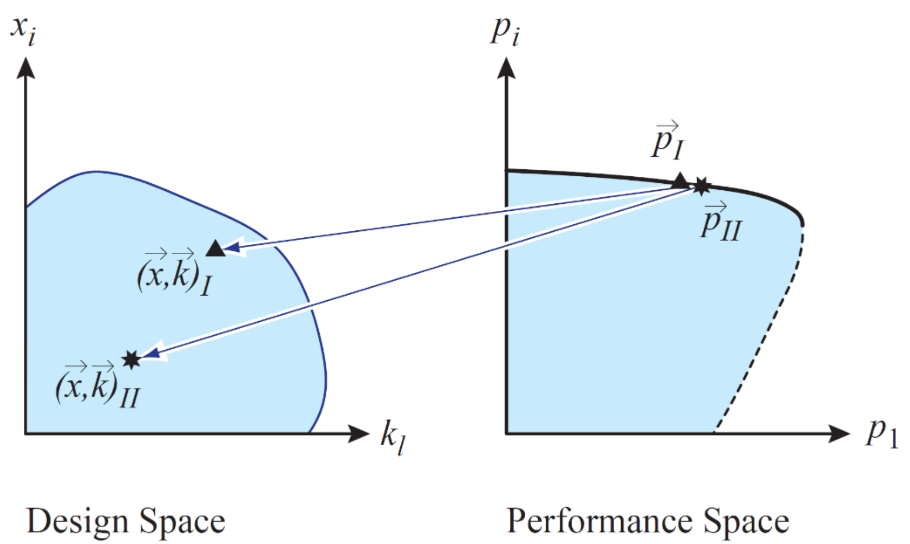


"Pareto Front"



Multi-Objective Optimization (2)

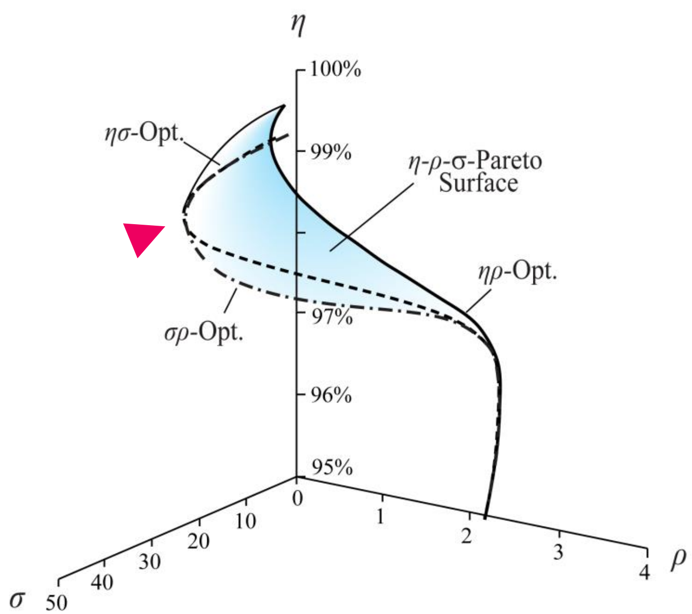
- Design Space Diversity
- Equal Performance for Largely Different Sets of Design Parameters

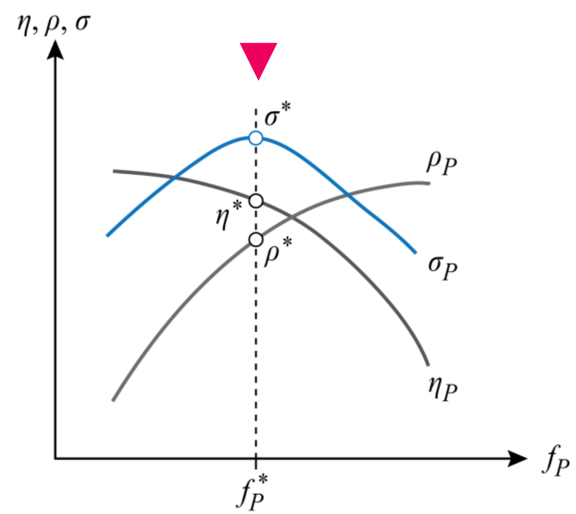


- ► E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)
- ► Allows Optimization for Further Performance Index (e.g. Costs)

Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- Definition of a Power Electronics *"Technology Node"* → ($\eta^*,\rho^*,\sigma^*,f_P^*$)
- Maximum σ [kW/$], Related Efficiency & Power Density





- ► Specifying Only a Single Performance Index is of No Value (!)
- ► Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)

Converter Performance Evaluation Based on *η-ρ-σ*-Pareto Surface

- Definition of a Power Electronics *"Technology Node"* → $(\eta^*,\rho^*,\sigma^*,f_P^*)$
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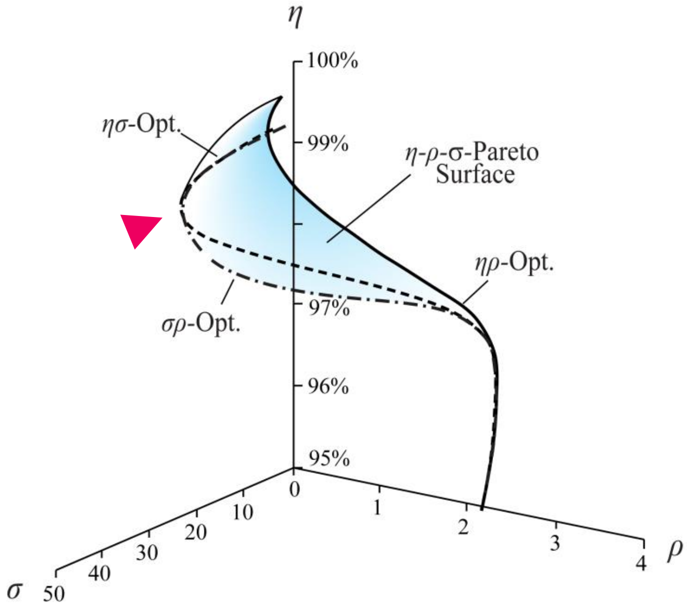

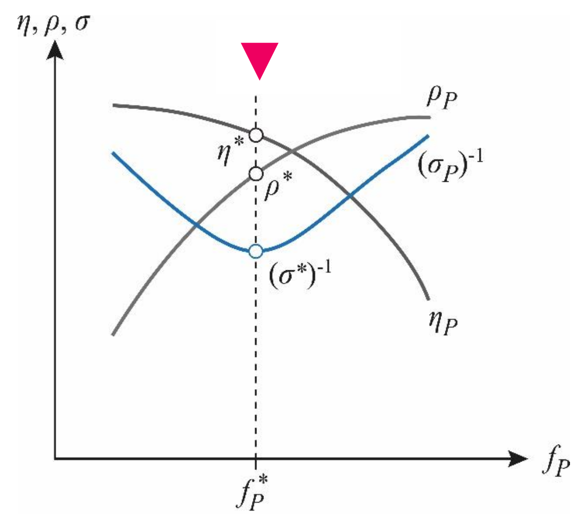

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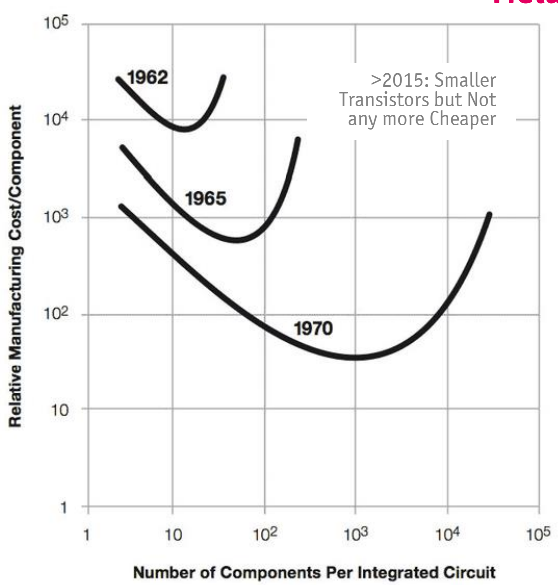
- Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)

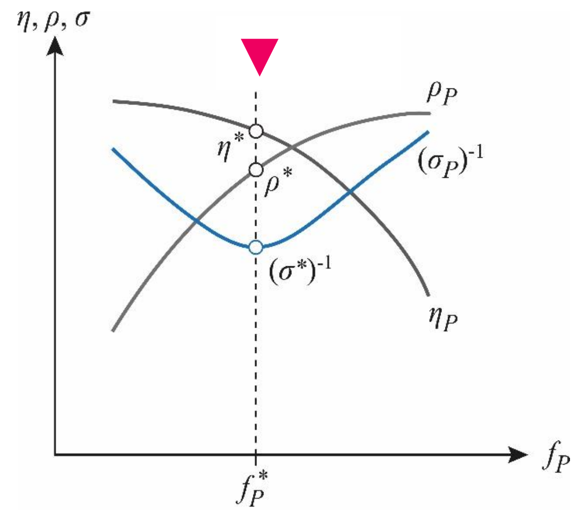
Remark: Comparison to "Moores Law"

- "Moores Law" Defines Consecutive Techn. Nodes Based on Min. Costs per Integr. Circuit (!)
- Complexity for Min. Comp. Costs Increases approx. by Factor of 2 / Year

Economy of Scale → ← Lower Yield



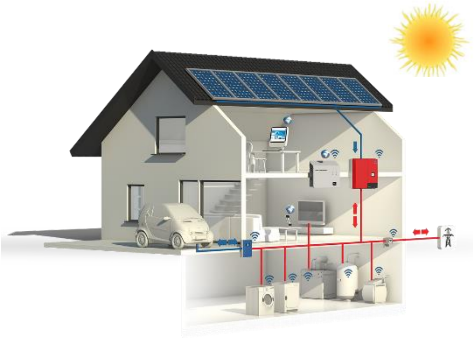
Gordon Moore: The Future of Integrated Electronics, 1965 (Consideration of Three Consecutive Technology Nodes)



▶ Definition of "$\eta^*, \rho^*, \sigma^*, f_P^*$–Node" Must Consider Conv. Type / Operating Range etc. (!)

Example

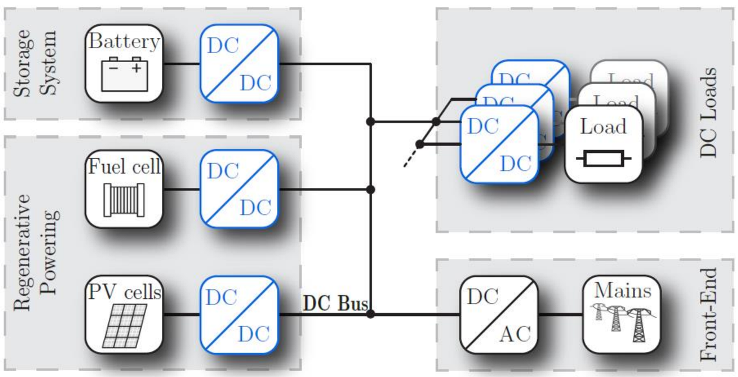
Two-Level vs. Three-Level Dual Active Bridge



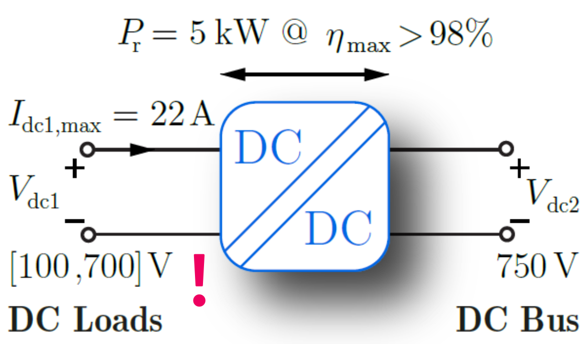
Source: SMA

Wide Input Voltage Range Isolated DC/DC Converter

Structure of "Smart Home" DC Microgrid



Universal DC/DC Converter

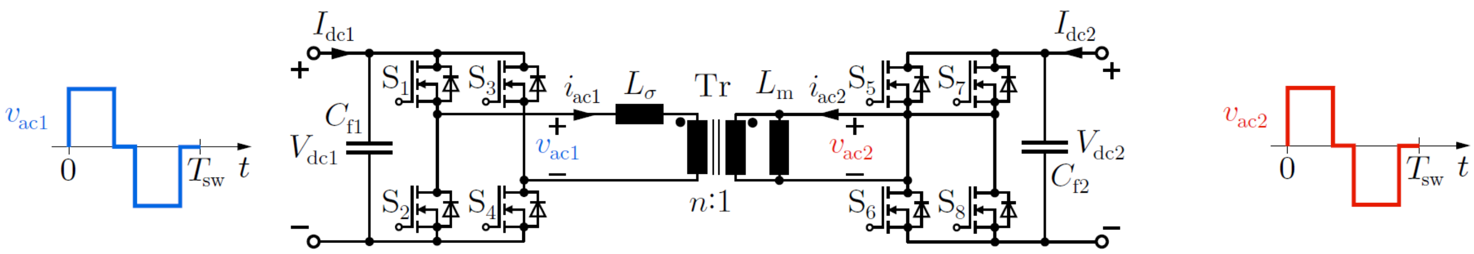


- Universal Isolated DC/DC Converter
  - Bidirectional Power Flow
  - Galvanic Isolation
  - Wide Voltage Range
  - High Partial Load Efficiency

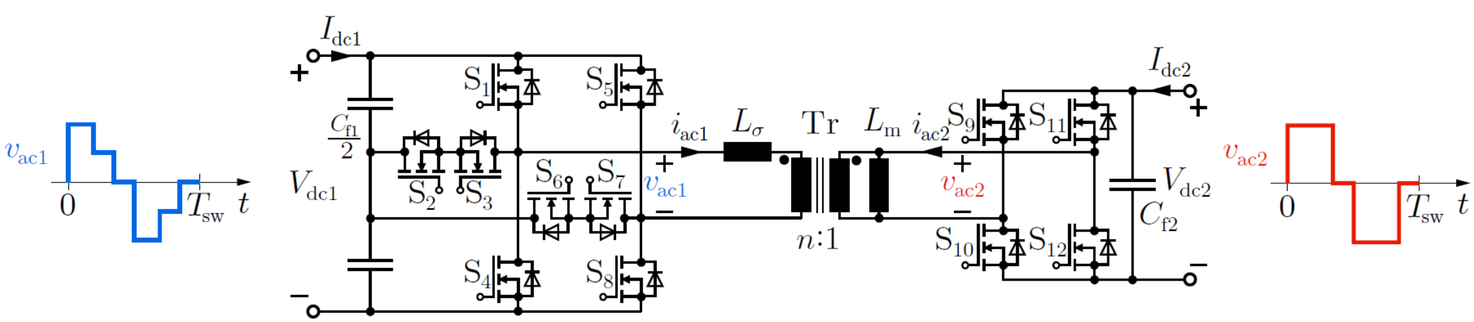
- Advantages
  - Reduced System Complexity
  - Lower Overall Development Costs
  - Economy of Scale

Comparative Evaluation of Converter Topologies

- Conv. 3-Level Dual Active Bridge (3L-DAB)

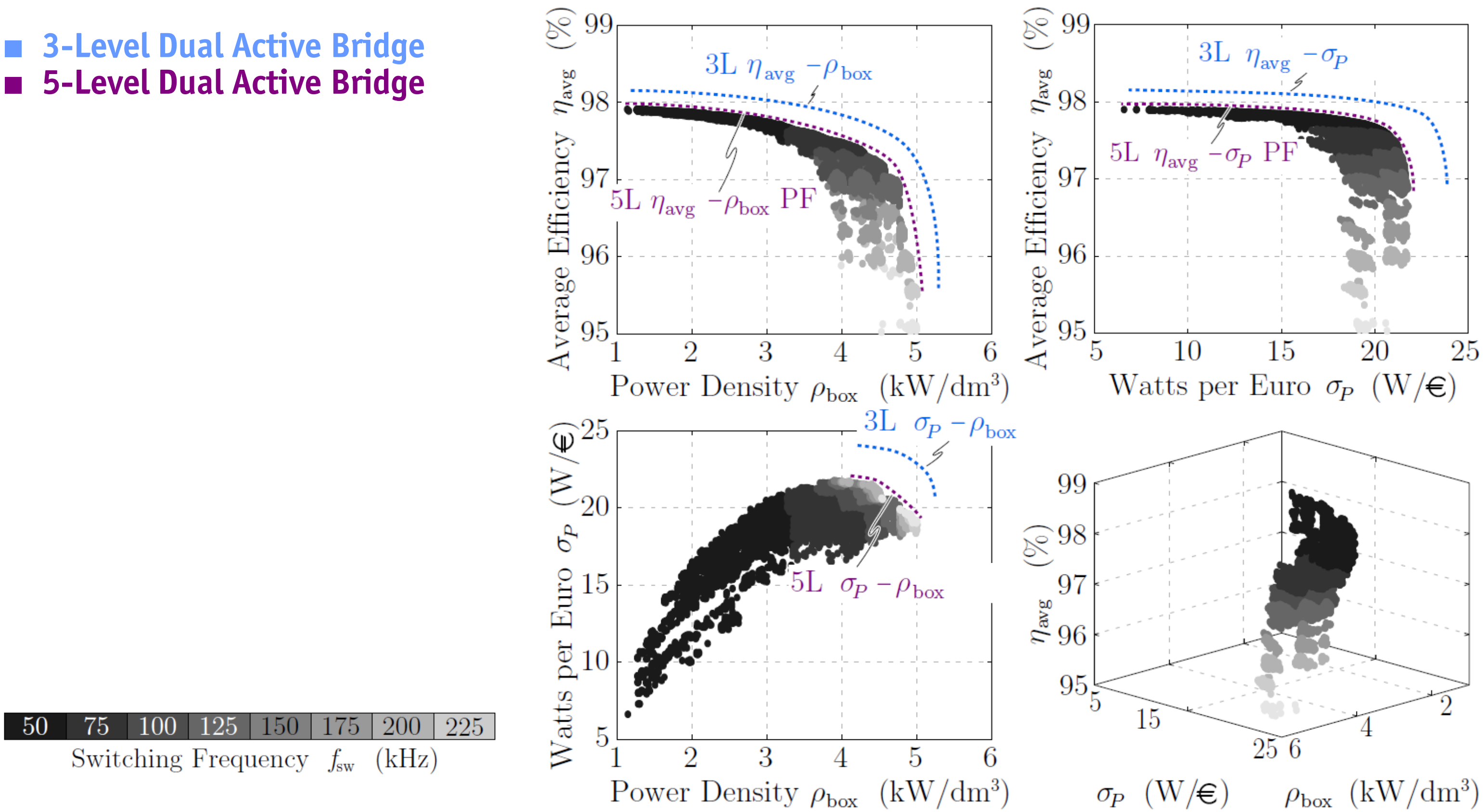


- Advanced 5-Level Dual Active Bridge (5L-DAB)



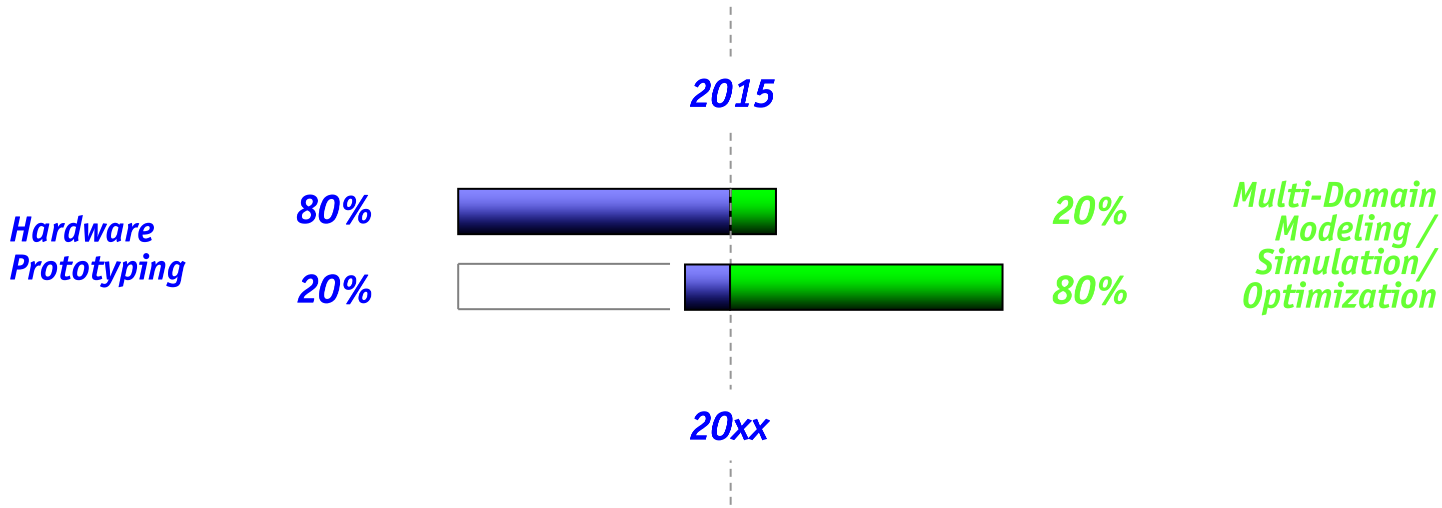
Optimization Results - Pareto Surfaces

- 3-Level Dual Active Bridge
- 5-Level Dual Active Bridge



Multi-Objective Optimization

- Offers Incredible Design Insight – Quantifies Trade-Offs / Technology Sensitivities (!)
- Extends Theory of Components – "Theory of Systems"
- Reduces Time-to-Market – Cuts Design Time from Weeks to Hours



- ▶ Increasingly Used in Industry (BOSCH, Infineon, etc.)
- ▶ Could be Extended to Platform Solutions (Def. as Side Conditions) & Systems & Life Cycle Analysis

Power Electronics Design & Testing 4.0

Assisted
Augmented
Autonomous

Roadmap to Power Electronics Design 4.0

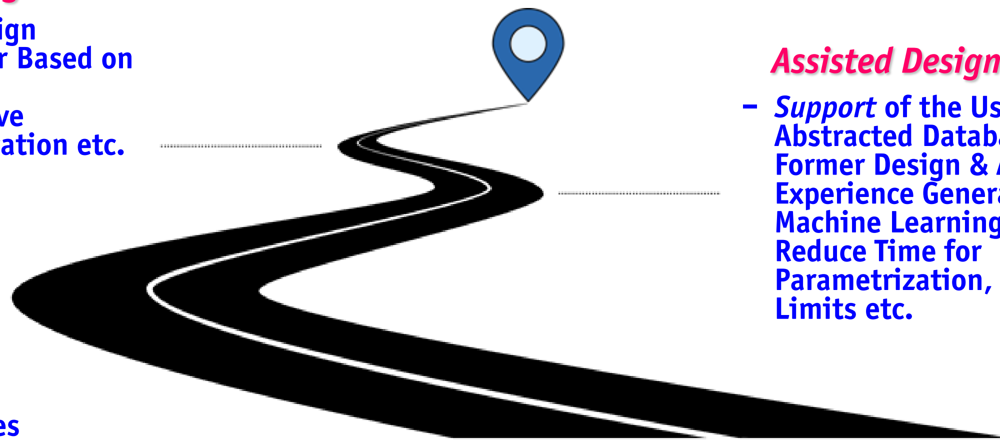
- **End-to-End Horizon** of Modeling & Simulation (Specification → Recycling)

Autonomous Design → Design 4.0

– *Independent* Generation of Full Designs & Graphical Representation of Performances/ Sensitivities/Diversities for Final (Expert) User Judgement etc.

Augmented Design

– *Suggestion* of Design Details to the User Based on Previous Designs, incl. Comprehensive Performance Indication etc. in Graphical Form



Assisted Design

– *Support* of the User with Abstracted Database of Former Design & Appl. Experience Generated by Machine Learning in Order to Reduce Time for Parametrization, Def. of Limits etc.

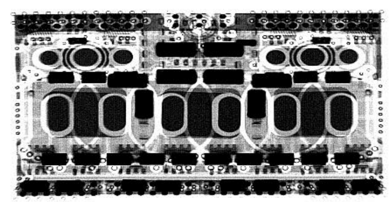
State-of-the-Art

– Models and Simulation/ Optimization Structure Defined by the User
– Limited Interactive Features
– Fragmented / High License Costs

► **Multi-Obj. Design for Cost / Volume Target / Manufacturing / Testing / Reliability / Recycling**
► **The Only Way to Survive** in a World of Exponentially Increasing Knowledge Bases / # of Papers (!)

Remark – *Future Experimental Analysis*

- No Access to Inner Details / Only Terminal Waveforms Available for Measurement (!)



- Convergence of *Measurement* & *Simulation* → *Augmented Reality Oscilloscope*
- *Measured* Signals & *Simulated* Inner Voltages/Currents/Temp. Displayed Simultaneously
- Automatic Tuning of Simulation Parameter Models for Best Fit of Simulated/Measured Waveforms

Source:
www.roadtrafficsigns.com

Conclusions

→

"Energy" Electronics

- Design Considering Converters as "Integrated Circuits" (PEBBs)
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

— "Converter" → "Systems" (Microgrid) or "Hybrid Systems" (Automation / Aircraft)
— "Time" → "Integral over Time"
— "Power" → "Energy"

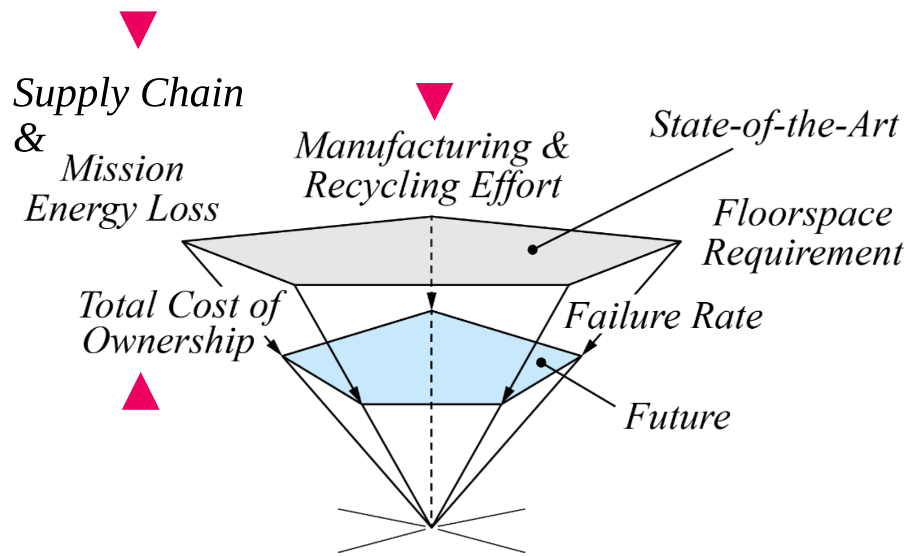
$$p(t) \rightarrow \int_0^t p(t)\,\mathrm{d}t$$

— Power Conversion → Energy Management / Distribution
— Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
— Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
— Cap. Filtering → Energy Storage & Demand Side Management
— Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
— etc.

New Power Electronics Systems Performance Figures/Trends

- Complete Set of New Performance Indices

— Power Density [kW/m²]
— Environm. Impact [kWs/kW]
— TCO [$/kW]
— Mission Efficiency [%]
— Failure Rate [h^{-1}]



► Conclusions

- **Challenges in *Modeling & Simulation***

– Improvement & Comb. of Analytic, Equiv. Circuit, FEM, Hybrid Red. Order Models
– Models in Certain Areas Largely Missing (Costs, EMI, Reliability, Manufacturability, etc.)
– Strategies for Hierarchical Structuring of Modeling (Doping Profile → Mission Profile)
– Strategies for Comput. Efficient Design Space Exploration & Multi-Obj. Simulation
– Sensitivity of Performance Prediction to Model Inaccuracies Largely Unknown
– Design Space Diversity and Performance Sensitivities Not Utilized

- **Challenges of *Company-Wide Introduction***

– No Readily Available Software
– Company-Wide Model Updates & Software Updates
– Complete Restructuring of Engineering Departments
– License Costs
– etc.

... but, ***"The Train Has Left the Station"* (!)**

■ End

Thank You !