ETH zürich

Applied Innovative Power Electronics

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Power Electronic Systems Laboratory
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Outline

- 1-Φ Multi-Cell Telecom Rectifier
- Google Little Box 2.0
- 3-Φ SiC vs. Si PV Inverter
- 3-Φ Buck-Type PFC Rectifier
- Outlook

1-Φ Multi-Cell Telecom Rectifier

Multi-Objective Optimization
Hardware Demonstrator
4D-Modulation
Cap. Coupling
Swiss SST

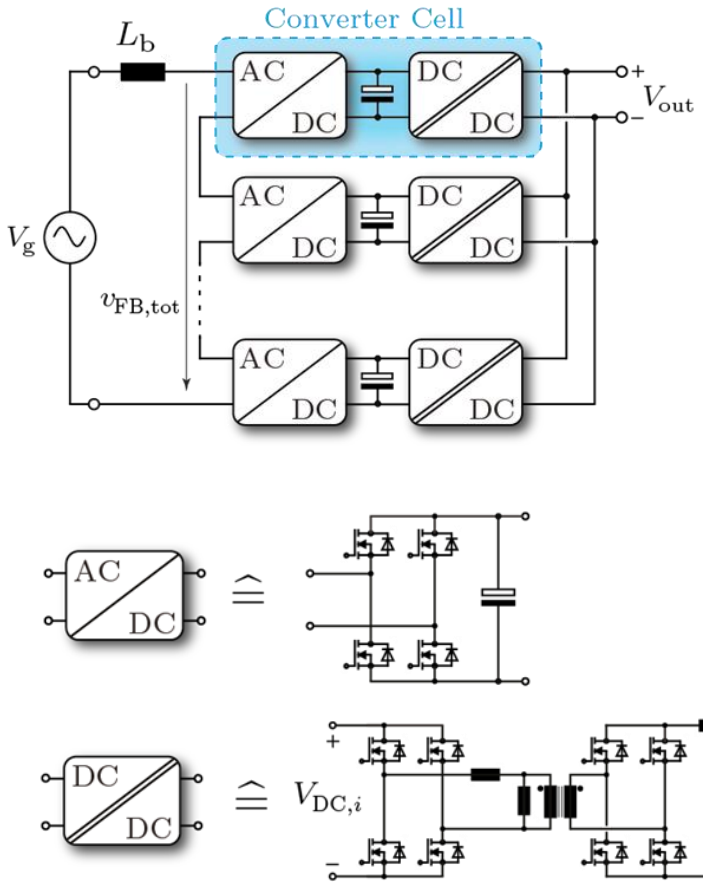
▶ 1-Φ Multi-Cell Telecom Rectifier

- Input-Series Output Parallel Arrangement
- Interleaving on Input and Output Side
- Realization Based on LV MOSFETs

V_{in} = 230V ± 10%
V_{out} = 48V
P_{out} = 3.3kW
T_{hold} = 10ms

- Full-Bridge AC/DC Converter
- Phase-Shift Full Bridge DC/DC Stage

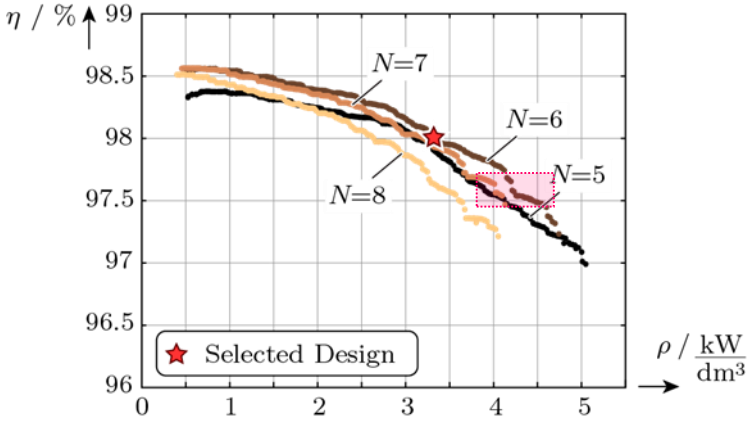
→ Multi-Objective Optimization

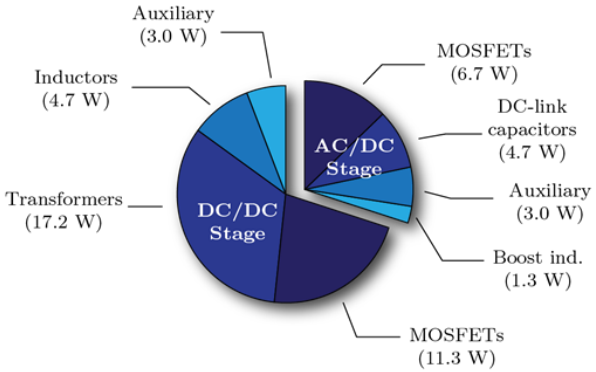


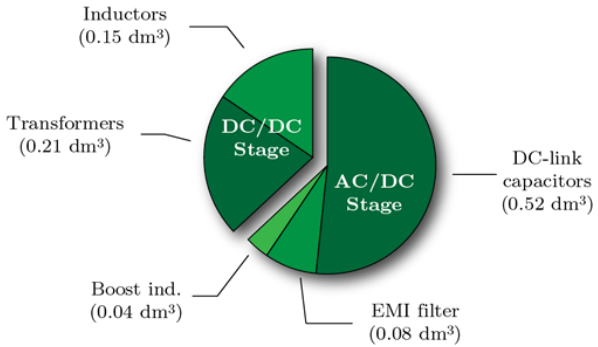
▶ Results of ηρ-Pareto Optimization

- All Degrees of Freedom Considered
- 80% Part Load Optimization

- *N*=6 Converter Cells (550W each)
- 100V Si MOSFETs / 4mΩ
- AC/DC Cells: 20kHz (120kHz eff.)
- DC/DC Cells: 80kHz



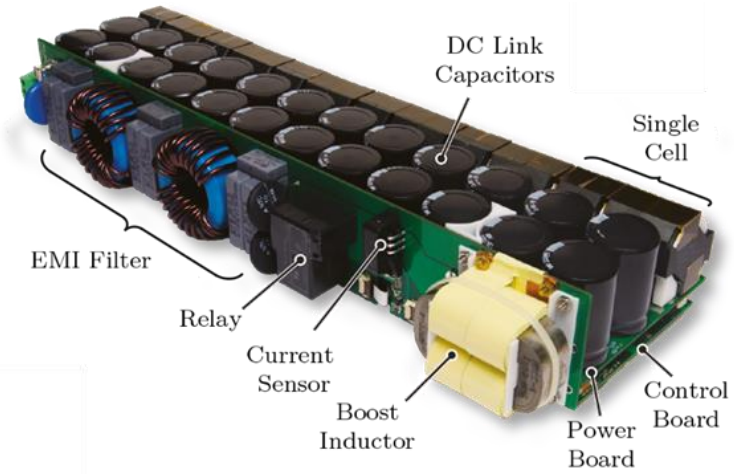


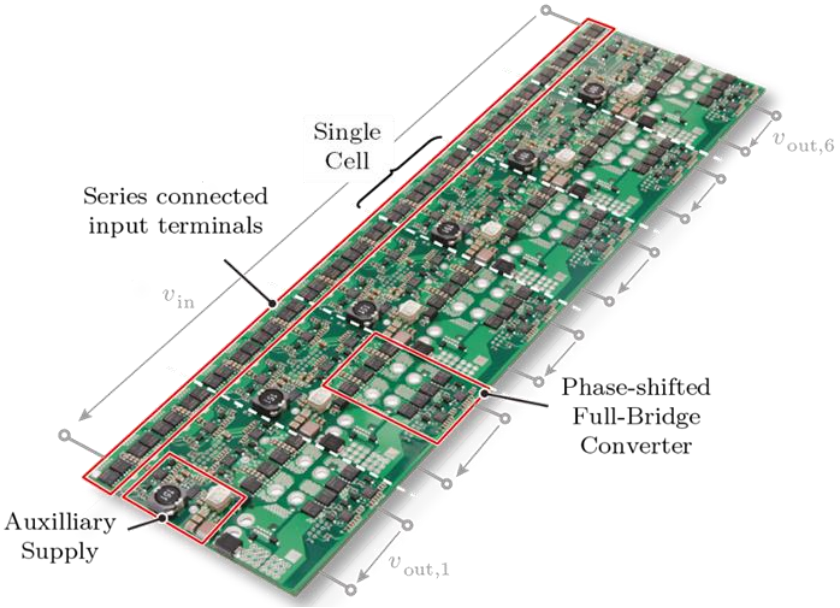


→ Volume & Loss Distribution

▶ Hardware Demonstrator

- Dimensions: 31cm x 11cm x 4.8cm = 1.6dm^3
- 2.1 kW/dm^3



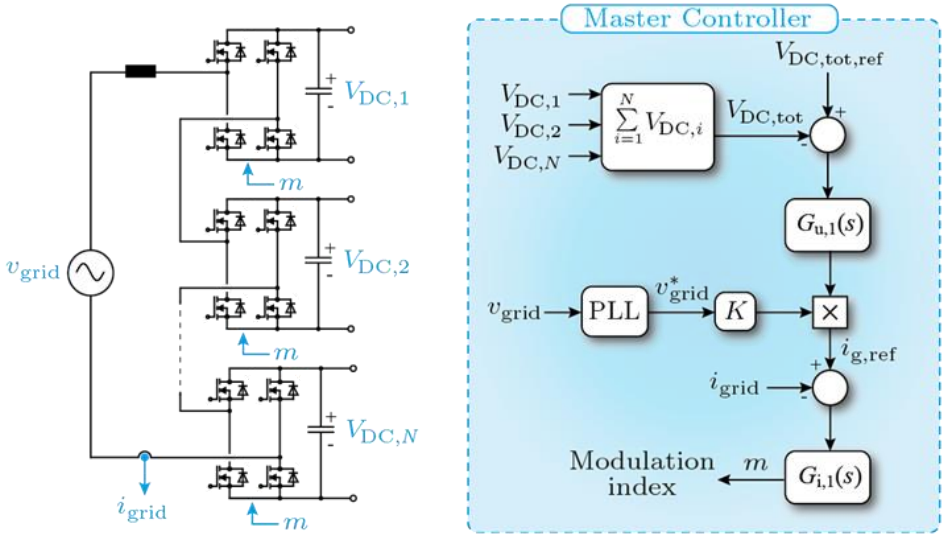


→ Full-System and Power Board

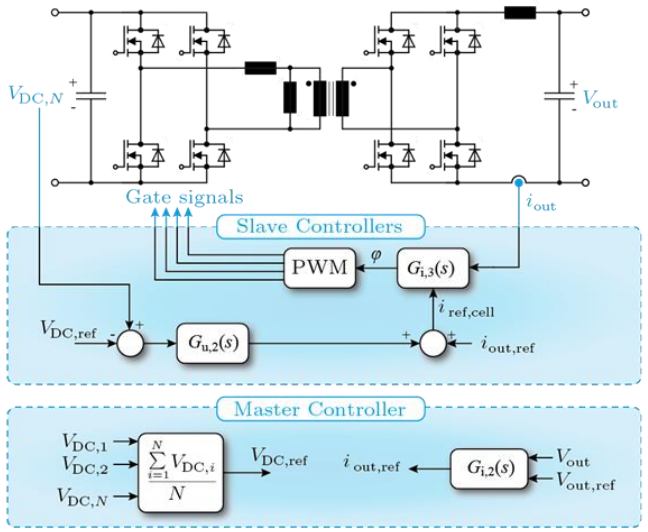
▶ Control Concept

■ Master / Slave Control

- AC/DC Stages



- DC/DC Stages

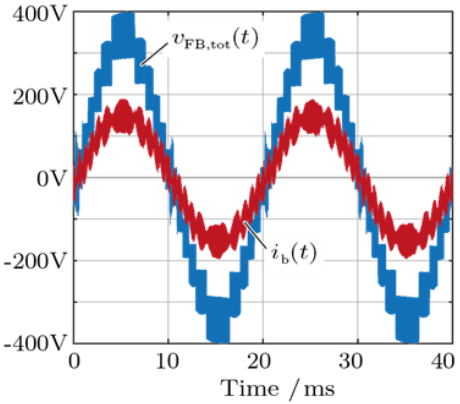


→ Control of DC Link Voltages Trough DC/DC Converter Stages

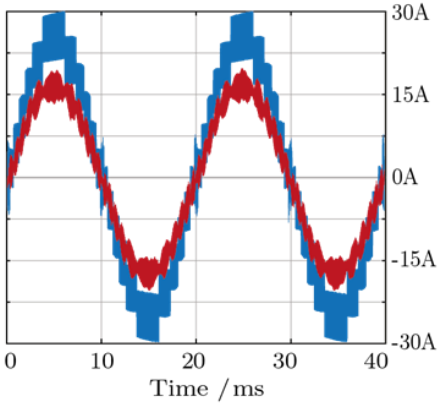
Measurement Results

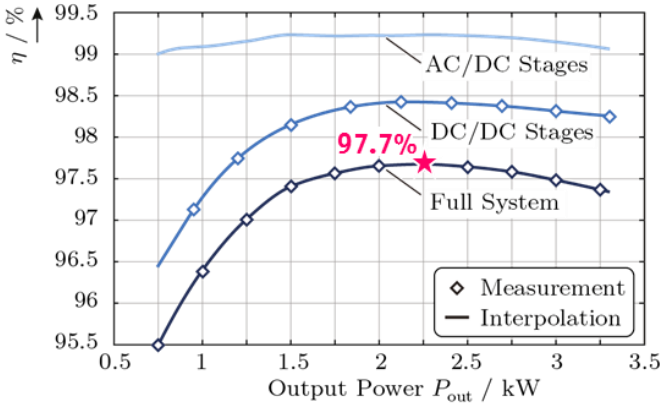
- Closed-Loop Operation
- Measurements @ V_{in}=230V, V_{out}=48V

P_{out}=1.5kW



P_{out}=2.5kW

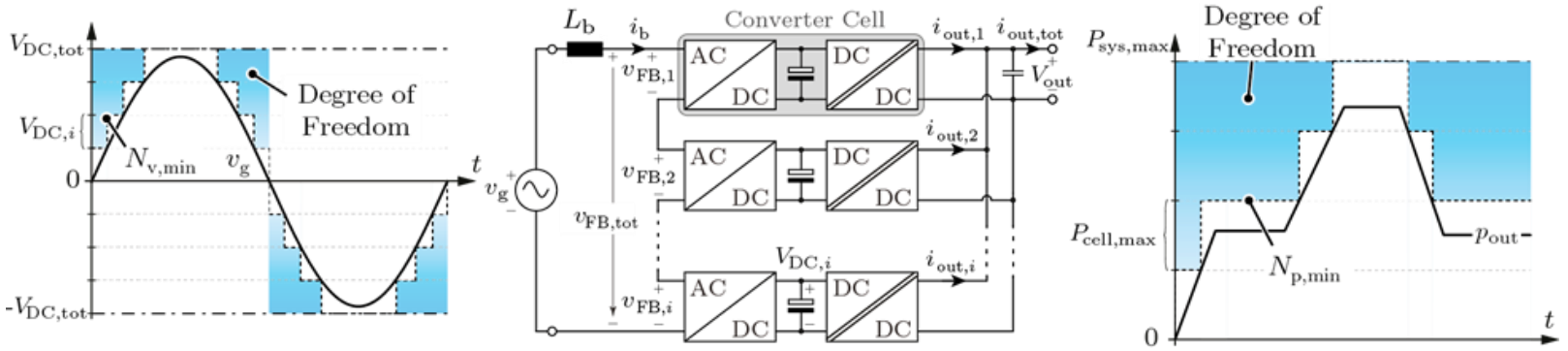




→ Peak Efficiency of 97.7%
→ Diff. to Calculation due to PCB Losses etc.

▶ 4D-Interleaving Operation (1)

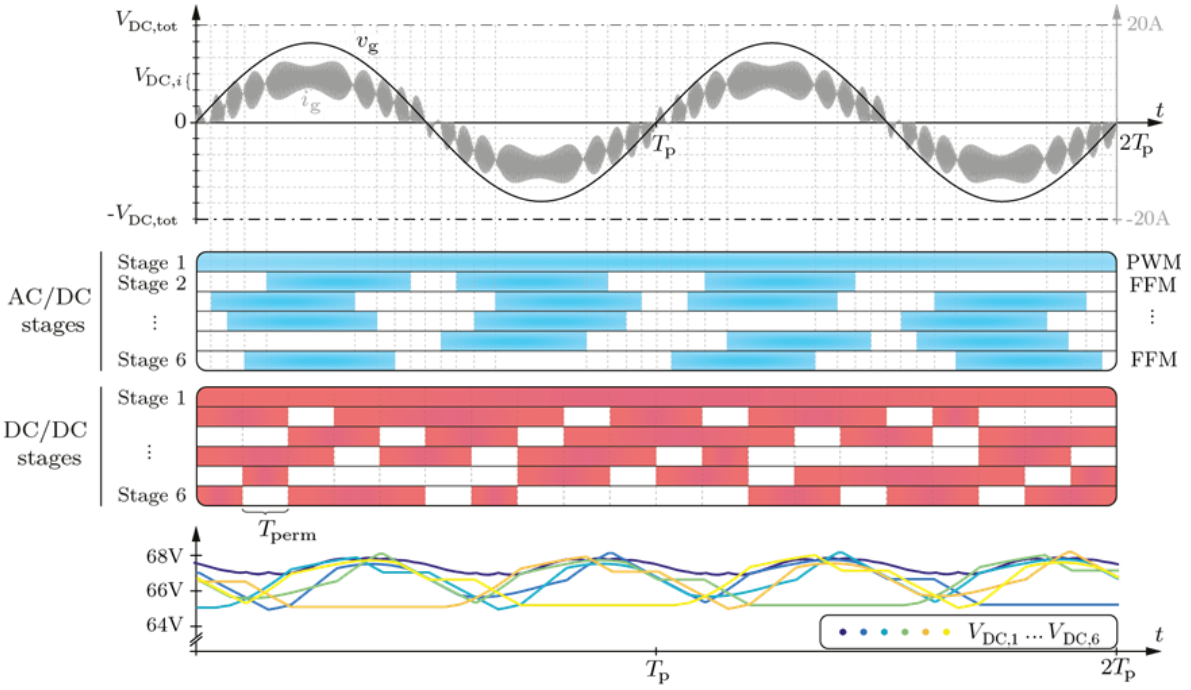
- **Utilizing All Degrees of Freedom of the ISOP Multi-Cell Converter Concept**



→ **Sinusoidal Mains Voltage – Intervals with Low Modulation Index / Low Power**
→ **Power Decoupling of Input and Output due to DC Link Caps.**

▶ 4D-Interleaving Operation (2)

- **Utilizing All Degrees of Freedom of the ISOP Multi-Cell Converter Concept**

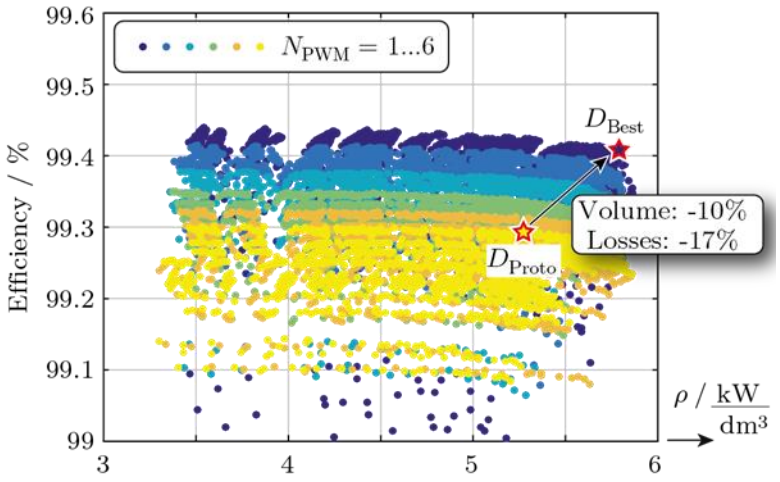


→ **Permutation of AC/DC and DC/DC Stages for Average Power Balancing**

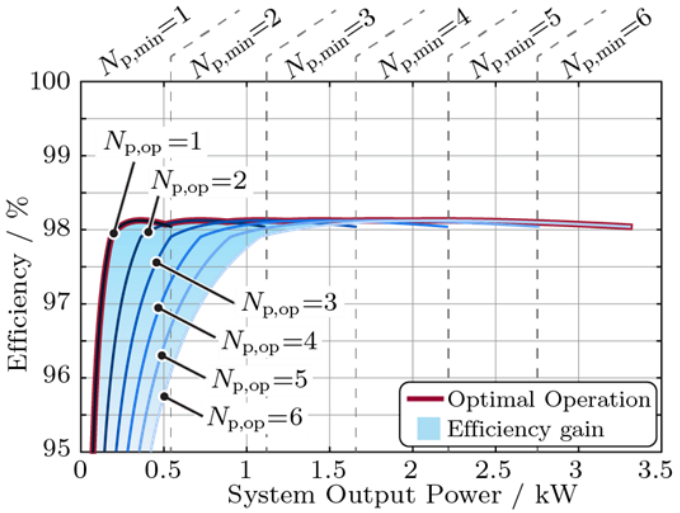
▶ 4D-Interleaving – Performance Improvement

- Performance Improvements w. 4D-Interleaving

AC/DC Stages



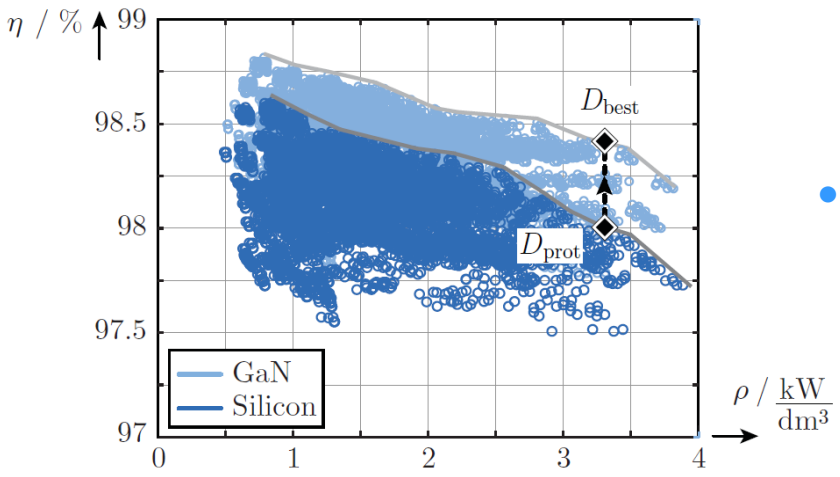
DC/DC Stages



→ Optimal Operation of AC/DC Converter w. Single PWM Cell, i.e. 5 Mains-Frequency Sw. Cells
→ Flat DC/DC Converter Efficiency Characteristic

▶ GaN vs. Si Power Semiconductor Technology

■ **Multi-Objective Optimization**



→ **Further Efficiency Improvement**
→ **Higher Power Density by 3D-Integration**

● **Si MOSFETs**

AC/DC Rectifier	
Switching frequency	$f_{sw,cell} = 20\,kHz$
Boost inductance	AMCC-4, 2605SA1, 25 µH, 7 turns
MOSFETs	2x BSC040N10NS5G, 100 V, 4.0 mΩ
DC-link cap.	4x Panasonic ECO-S1KA222CA, alum. elect., 80 V, 2.2 mF
EMI filter	3 stages, 2x common mode chokes (EPCOS R40 cores T38, 10 turns), 3x680 nF
DC/DC Converter	
Switching frequency	$f_{sw} = 80\,kHz$
Transformer	turns ratio 9:9, RM14, N97, EPCOS litz wire (420x71 µm)
Inductance	RM14LP, N97, EPCOS, 25 µH
Prim. MOSFETs	BSC040N10NS5G, 100 V, 4.0 mΩ
Sec. MOSFETs	BSC040N10NS5G, 100 V, 4.0 mΩ

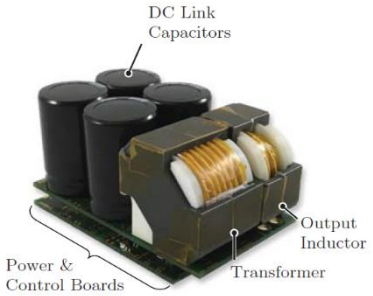
● **GaN**

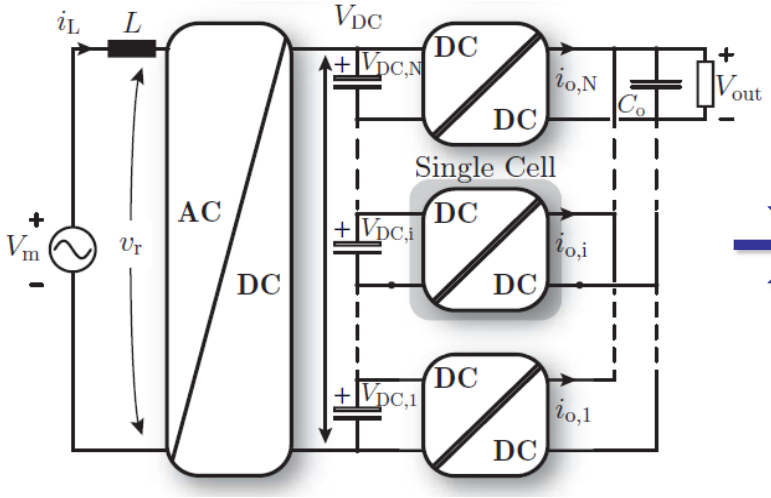
AC/DC Rectifier	
Switching frequency	$f_{sw,cell} = 20\,kHz$
Boost inductance	AMCC-4, 2605SA1, 25 µH, 7 turns
MOSFETs	3x EPC2022, 100 V, 3.2 mΩ
DC-link cap.	4x Panasonic ECO-S1KA222CA, alum. elect., 80 V, 2.2 mF
EMI filter	3 stages, 2x common mode chokes (EPCOS R40 cores T38, 10 turns), 3x680 nF
DC/DC Converter	
Switching frequency	$f_{sw} = 140\,kHz$
Transformer	turns ratio 7:7, RM14, N97, EPCOS litz wire (420x71 µm)
Inductance	RM14LP, N97, EPCOS, 12 µH
Prim. MOSFETs	EPC2022, 100 V, 3.2 mΩ
Sec. MOSFETs	2xEPC2022, 100 V, 3.2 mΩ

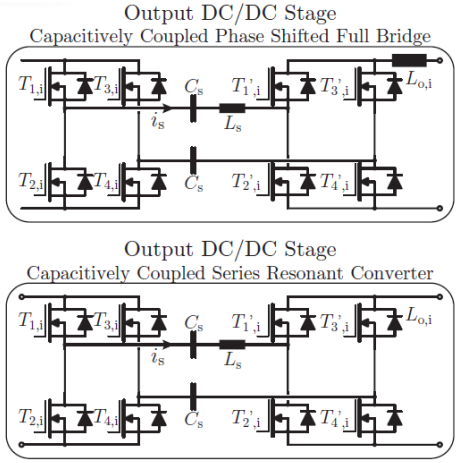
▶ Remark #1: Capacitive Coupling ISOP DC/DC Converter

- Phase-Shift or Resonant Operation
- Cap. Coupled "Sine Amplitude Converter"

- Conventional Transformer-Coupled DC/DC Converter Cell





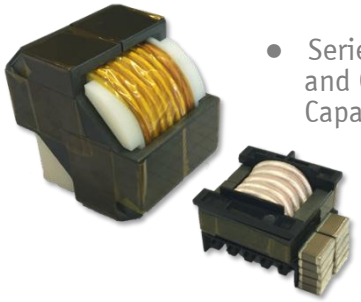


→ Substantial Saving of Losses / Volume

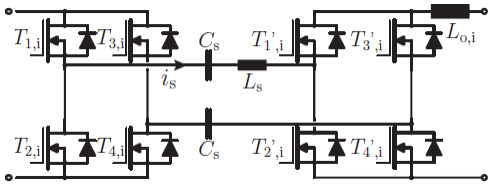
▶ Remark #1: Capacitive Coupling ISOP DC/DC Converter

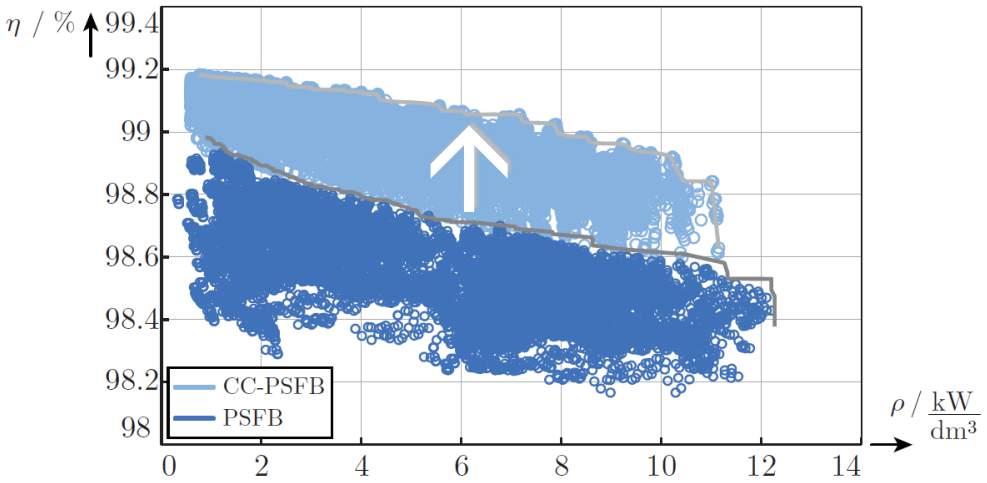
■ Multi-Objective Optimization of Cap. Coupled Phase-Shift Full-Bridge

- Transformer



- Series Ind. and Coupling Capacitors

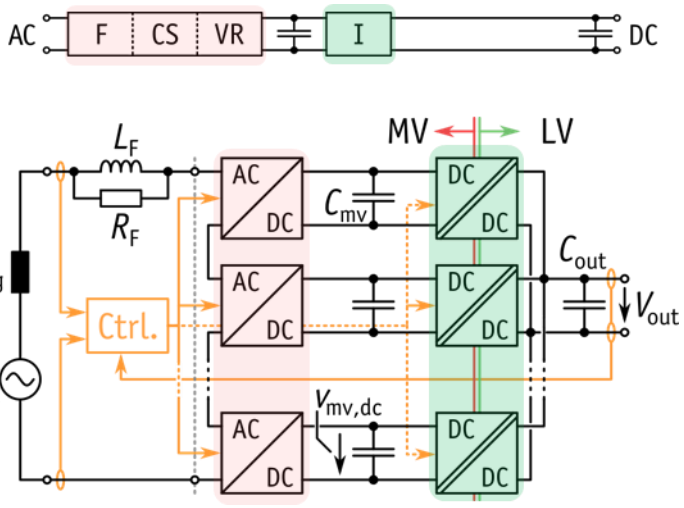




→ - 80% Volume and Substantial Saving of Losses

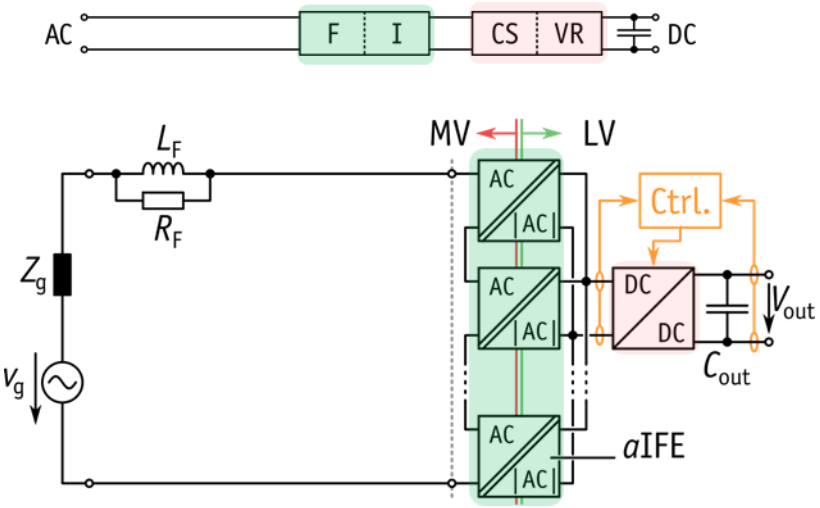
▶ Remark #2: Isolated Front-End vs. Isolated Back-End

■ Isolated DC/DC Back End



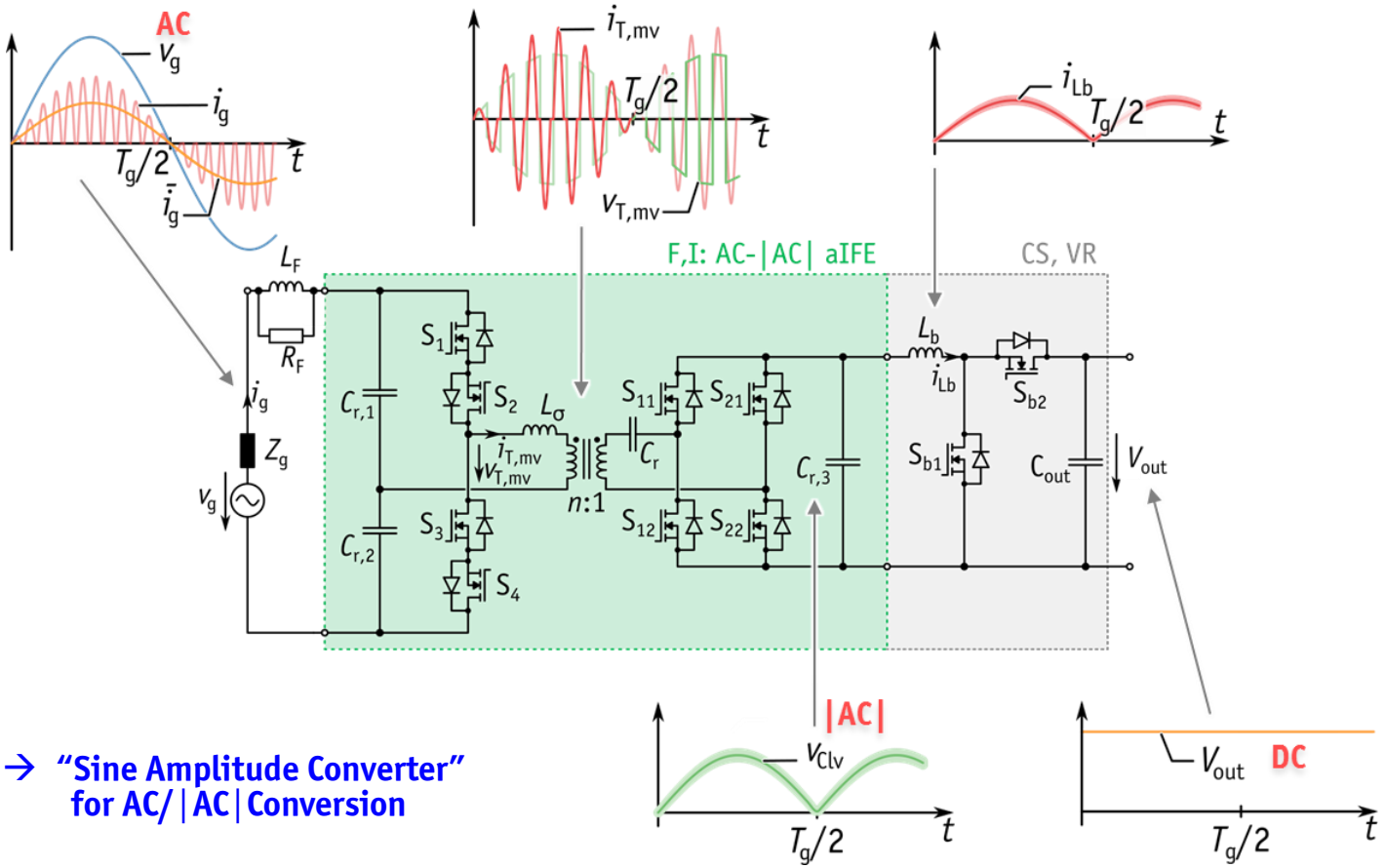
- Conventional ISOP Topology
- Direct Input Current Control
- Indir. or Direct Output Voltage Control
- Controlled or Sine Ampl. Isol. Stage
- Distributed DC Link Capacitors
- High Complexity

■ Isolated AC/ | AC | Front End



- Swiss SST (S3T)
- Indirect Input Current Control
- Direct Output Voltage Control
- Sine Amplitude Isolation Stage
- Single Storage Capacitor
- Low Complexity

▶ Remark #2: Isolated Front-End vs. Isolated Back-End



→ "Sine Amplitude Converter" for AC/|AC| Conversion

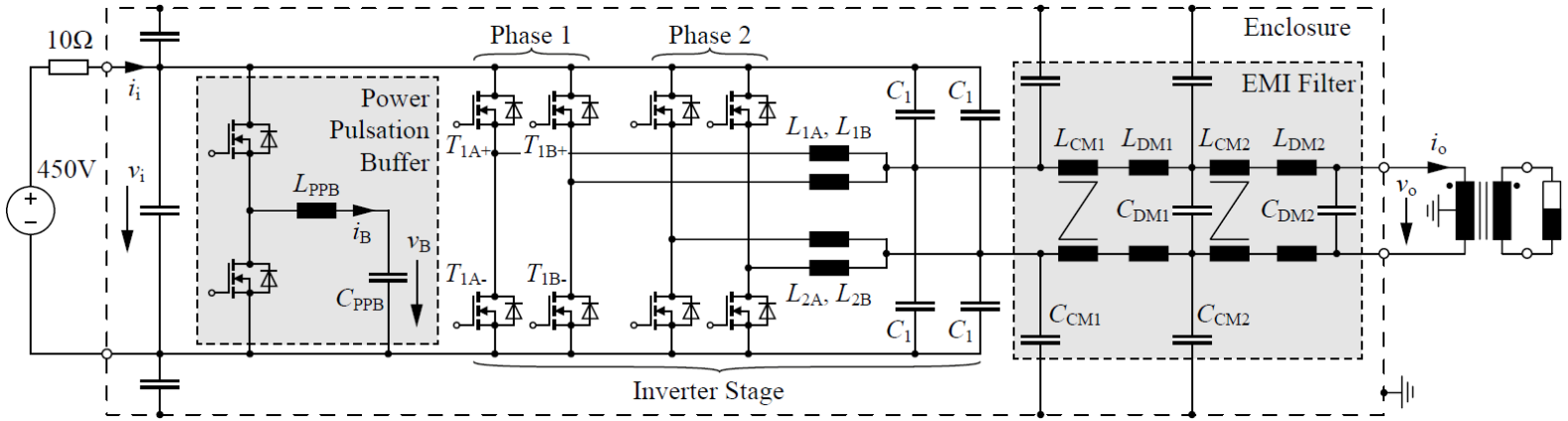
Google

Little Box 2.0

Full-Bridge DC/AC Converter
DC/⎪AC⎪- Converter + Unfolder
“The Ideal Switch is Not Enough” (!)

LiTTLE BOX CHALLENGE Little Box 1.0 Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

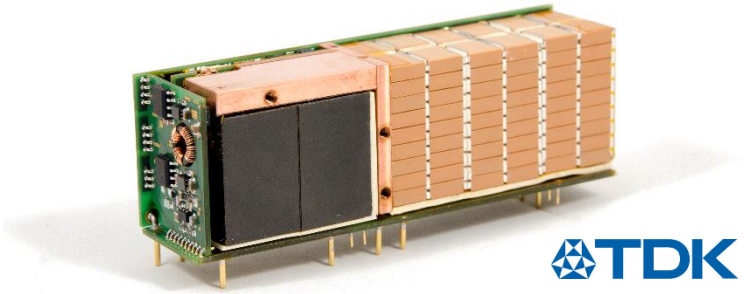


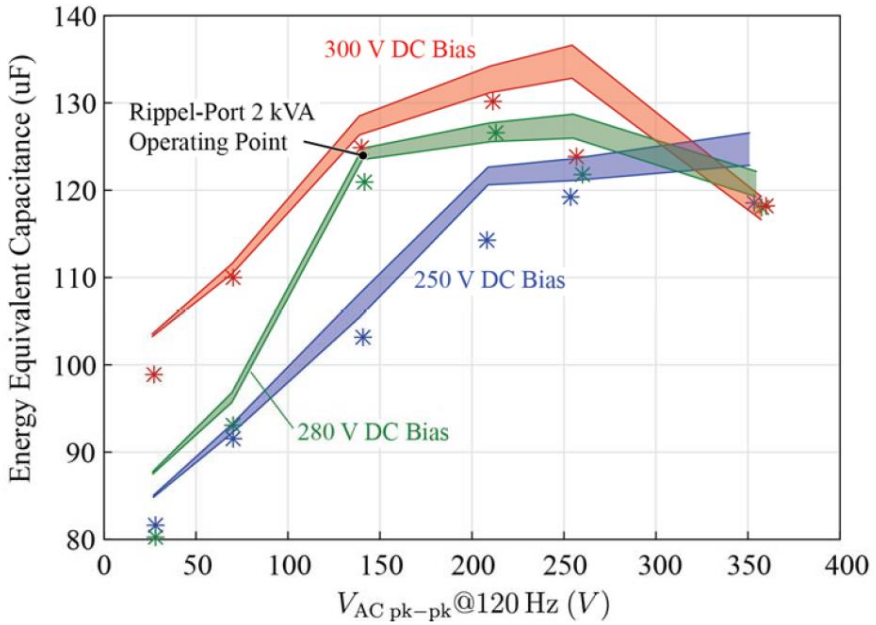
- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

Little Box 1.0 Power Pulsation Buffer

- High Energy Density 2nd Gen. 400V_{DC} CeraLink Capacitors Utilized as Energy Storage
- Highly Non-Linear Behavior → Opt. DC Bias Voltage of 280VDC
- Cap. Losses of 16W @ 2kVA Output Power

- 108 x 1.2µF /400 V
- 23.7cm³ Capacitor Volume





- Effective Large Signal Capacitance of C ≈140µF

Little-Box 1.0 Prototype (1)

- **DC-Side Power Pulsation Buffer**

- 8.2 kW/dm^3
- 8.9cm x 8.8cm x 3.1cm
- **96,3% Efficiency @ 2kW**
- **T_c=58°C @ 2kW**

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD+N_U$= 2.6%
- $THD+N_I$= 1.9%

- **Compliant to All *Original* Specifications (!)**

- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

Little-Box 1.0 Prototype (2)

- **DC-Side Power Pulsation Buffer**

- 8.2 kW/dm^3
- 8.9cm x 8.8cm x 3.1cm
- **96,3% Efficiency @ 2kW**
- **T_c=58°C @ 2kW**

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD+N_U$= 2.6%
- $THD+N_I$= 1.9%

★ **135 W/in^3**

■ **Compliant to All *Original* Specifications (!)**

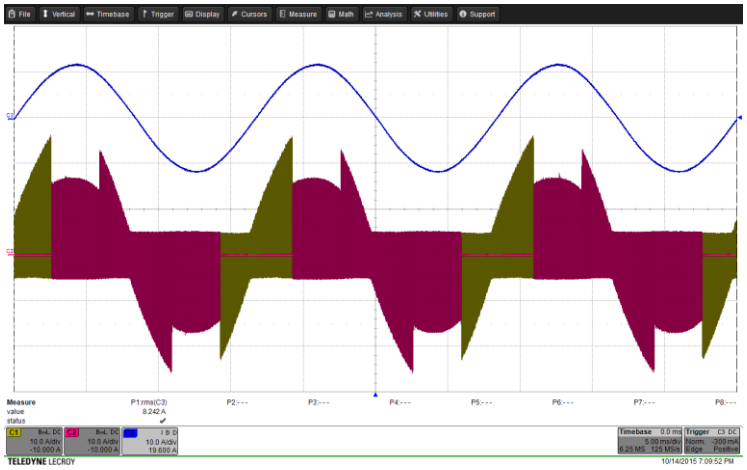
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

Little-Box 1.0 Measurement Results

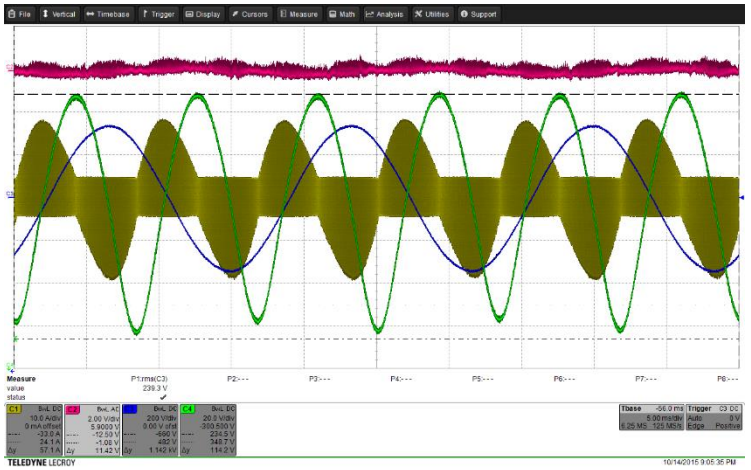
- DC-Side Power Pulsation Buffer

- Ohmic Load / 2kW

Output Current
Inductor Current Bridge Leg 1-1
Inductor Current Bridge Leg 1-2



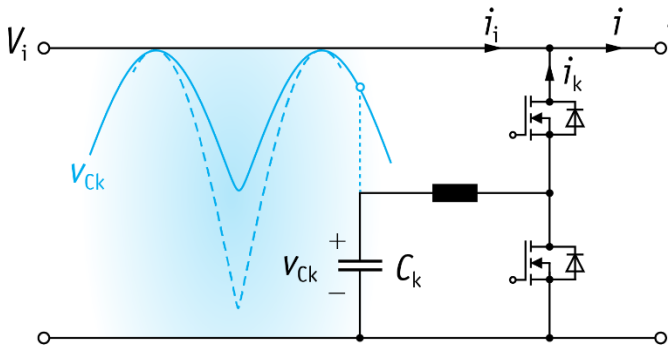
DC Link Voltage (AC-Coupl., 2V/Div.)
Buffer Cap. Voltage
Buffer Cap. Current
Output Voltage

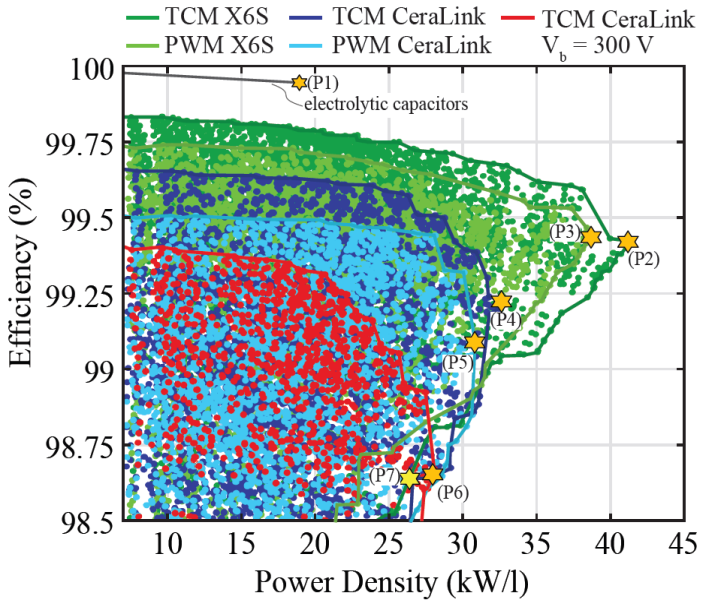


- Compliant to All *Original* Specifications (!)

Little Box 1.0 → X6S Power Pulsation Buffer (1)

- X6S Capacitor Technology Allows Considerable Loss Reduction vs. CeraLink (P2 vs. P7)
- Lower Losses / Lower Heatsink Volume → Higher Power Density

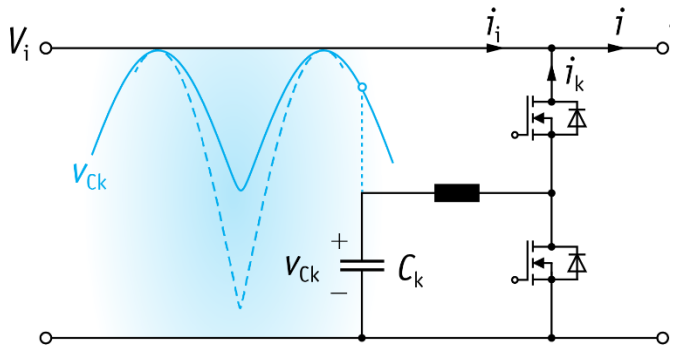


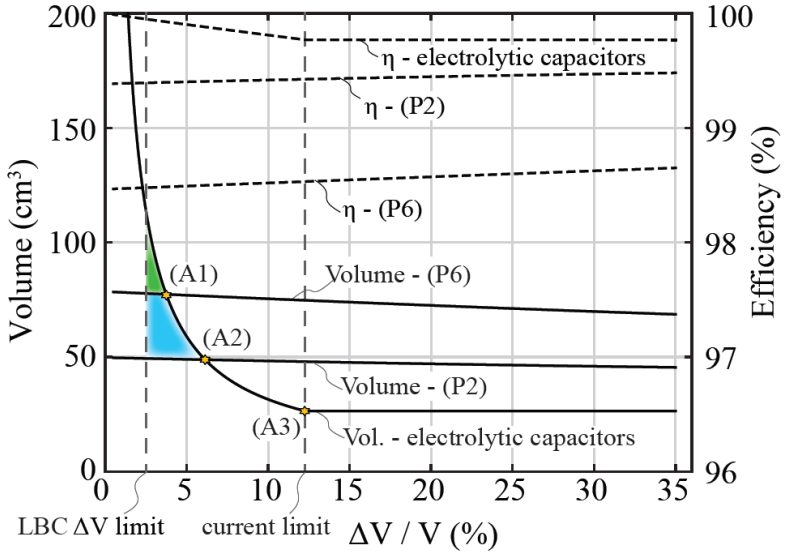


- Lower Volume Comp. to Electrolytic Cap. only for ΔV/V < 5% / No Efficiency Benefit

Little Box 1.0 → X6S Power Pulsation Buffer (2)

- X6S Capacitor Technology Allows Considerable Loss Reduction vs. CeraLink (P2 vs. P7)
- Lower Losses / Lower Heatsink Volume → Higher Power Density

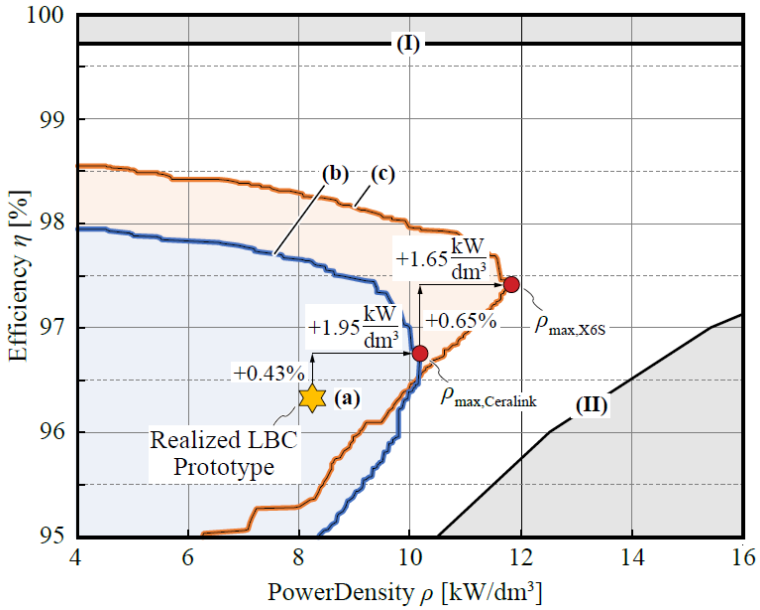




- Lower Volume Comp. to Electrolytic Cap. only for ΔV/V < 5% / No Efficiency Benefit

Little Box 1.0 → X6S Power Pulsation Buffer (3)

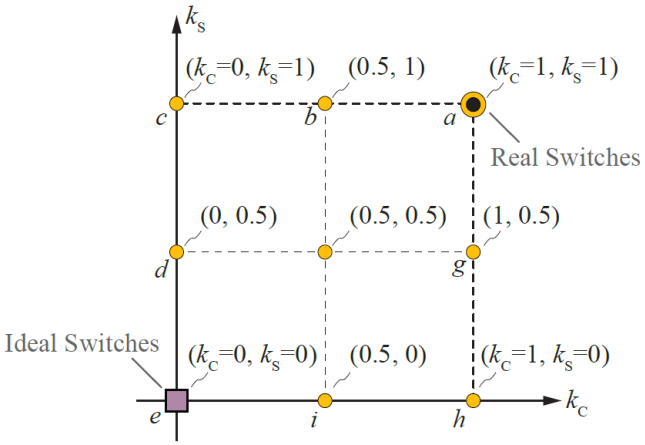
- Multi-Objective Optimization of Little-Box 1.0 (incl. CeraLink → X6S)
- Absolute Performance Limits (I) - DSP/FPGA Power Consumption
  (II) - Heatsink Volume @ (1-η)

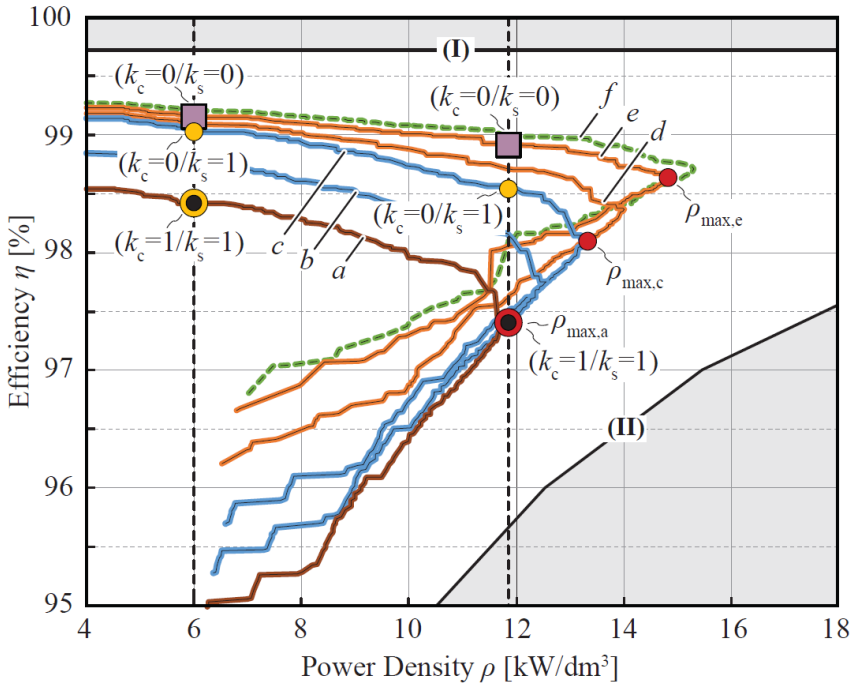


- Further Performance Improvement for Triangular Current Mode (TCM) → PWM

Little Box 1.0 @ Ideal Switches

- Multi-Objective Optimization of Little-Box 1.0 (Example: TCM, X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors

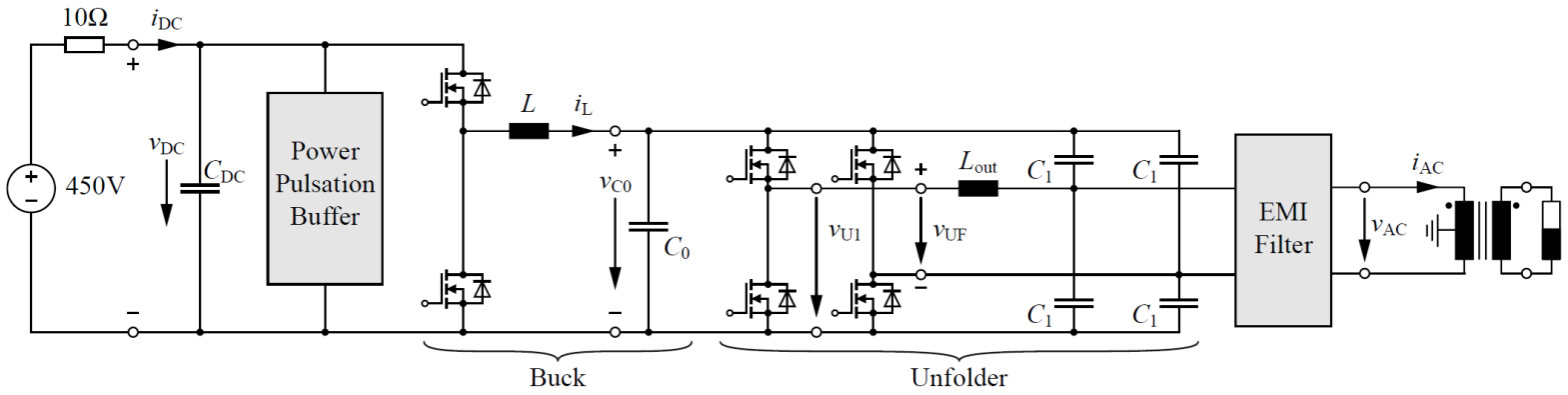




- The Ideal Switch is NOT Enough (!) → High Frequency Magnetics etc.

Little Box 2.0 – New Converter Topology

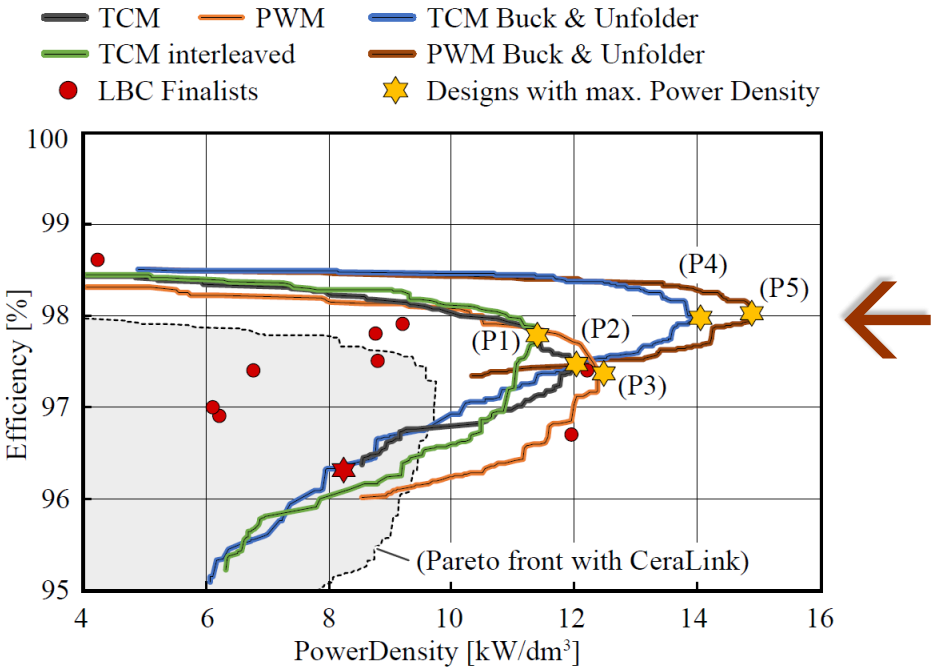
- Novel Converter Topology - DC/ | AC | - Buck Converter + Unfolder
- Temporary PWM of Unfolder for Ensuring Continuous Current Control
- TCM or PWM of Buck-Converter



- Full Optimization of All Converter Options / Idealization of the Switches

Little Box 2.0 – Multi-Objective Optimization

- Novel Converter Topology - DC/ | AC | - Buck Converter + Unfolder
- Temporary PWM of Unfolder for Ensuring Continuous Current Control
- TCM or PWM of Buck-Converter



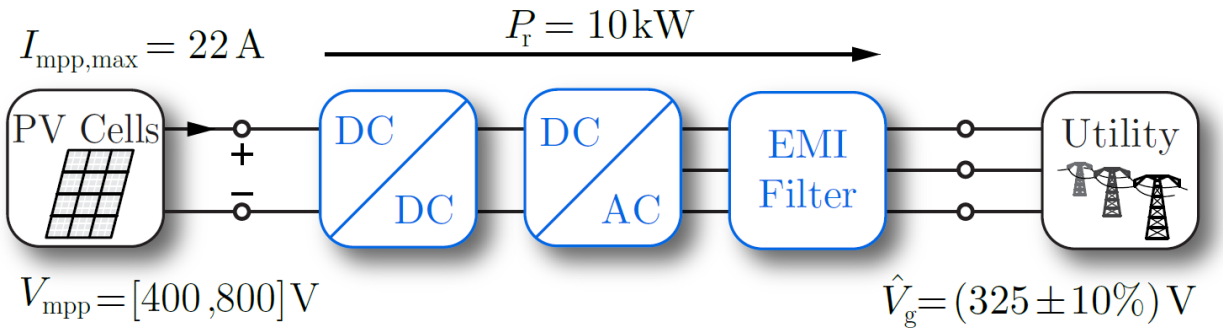
- Full Optimization Allows Power Density of ≈250W/in³ @ 98% Efficiency

3-Φ SiC vs. Si PV Inverter

Multi-Objective Optimization
Flying Capacitor Conv. Concept

Analysis of 3-Φ Si vs. SiC PV Inverter

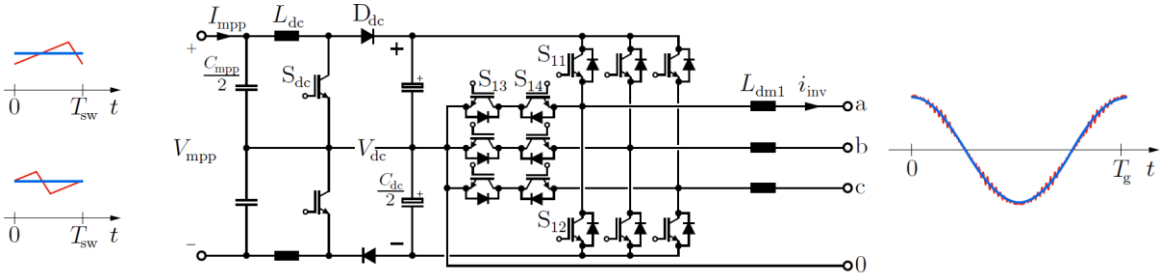
- Single-Input/Single-MPP-Tracker Multi-String PV Converter
- DC/DC Boost Converter for Wide MPP Voltage Range
- Output EMI Filter
- Typical Residential Application



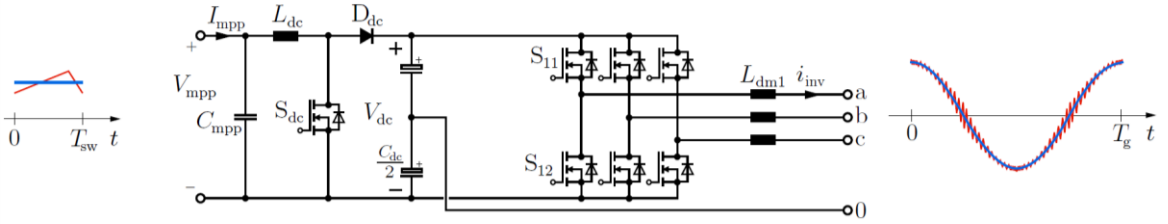
- Systematic Multi-Objective η-ρ-σ-Comparison of Si vs. SiC
- Exploit Excellent Hard- *AND* Soft-Switching Capabilities of SiC
- Find Useful Switching Frequency and Current Ripple Ranges
- Find Appropriate Core Material

Topologies - Converter Stages

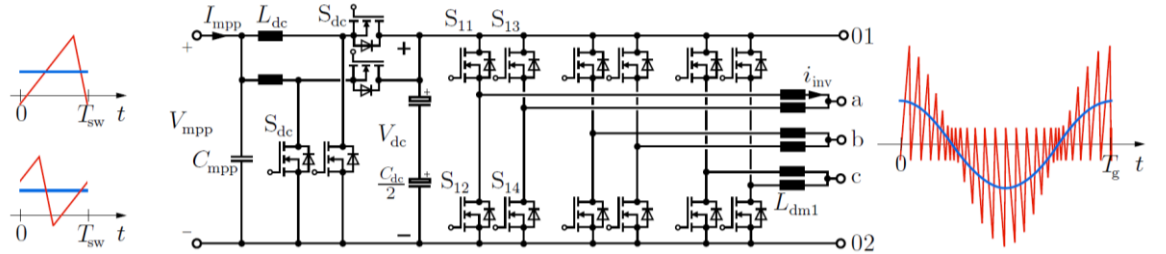
- **All-Si IGBT 3-Level PWM Inverter (3L-PWM)**



- **All-SiC MOSFET 2-Level PWM Inverter (2L-PWM)**

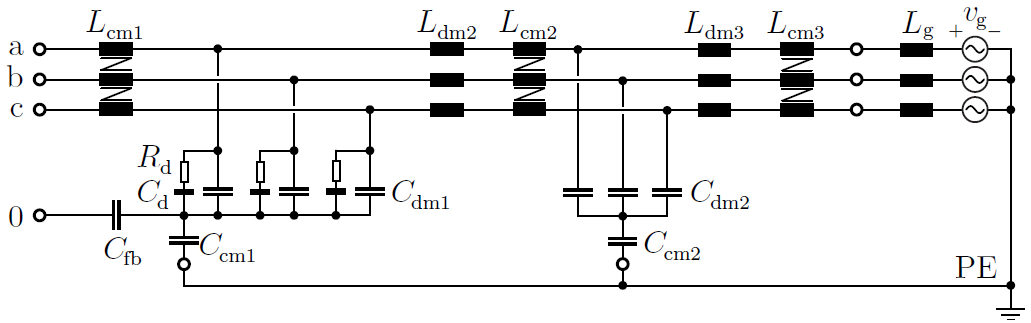


- **All-SiC MOSFET 2-Level Double-Interleaved TCM-Inverter (2L-TCM)**

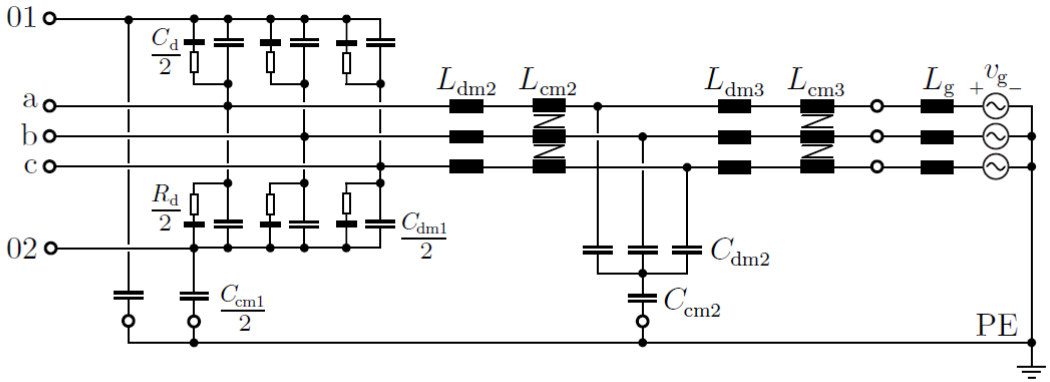


Topologies - Filter Stages

- 2-Stage DM & CM Filter for 2L-PWM and 3L-PWM



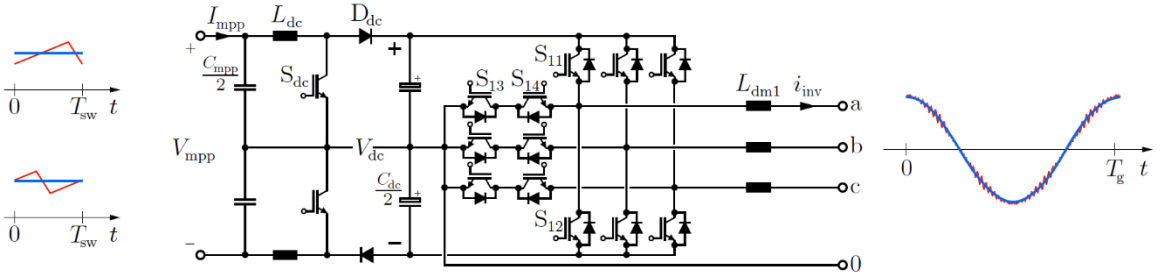
- 2-Stage DM & CM Filter for 2L-TCM
- TCM Inductor Acting as DM & CM Inductance



Modulation Schemes - PWM Converters

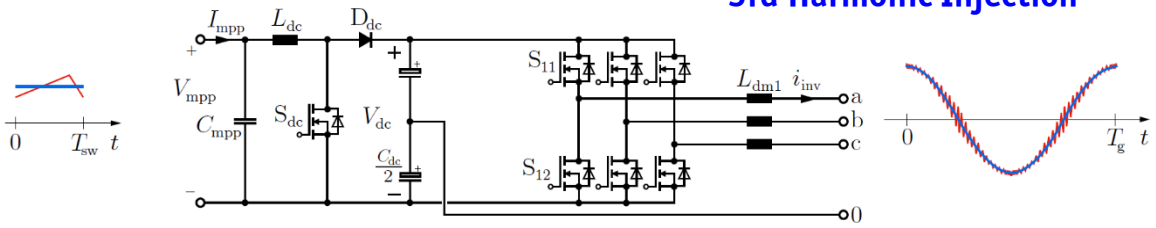
Three-Level PWM Inverter (3L-PMW)

- Symmetric Boost Converter
- Interleaved Operation
- Part. Compensation of LF DC-Link Midpoint Variation
- 3-Level T-Type Converter
- 3-Level PWM Modulation
- 3rd Harmonic Injection



Two-Level PWM Inverter (2L-PMW)

- Standard DC/DC Booster
- Standard Modulation
- 2-Level Converter
- 2-Level PWM Modulation
- 3rd Harmonic Injection

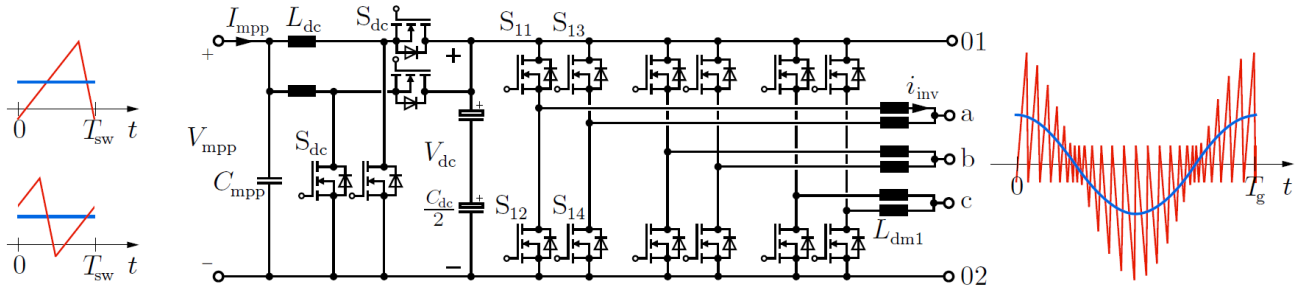


Modulation Schemes - TCM Converter

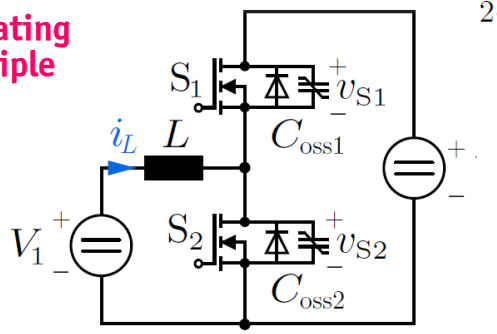
Two-Level TCM Inverter (2L-TCM)

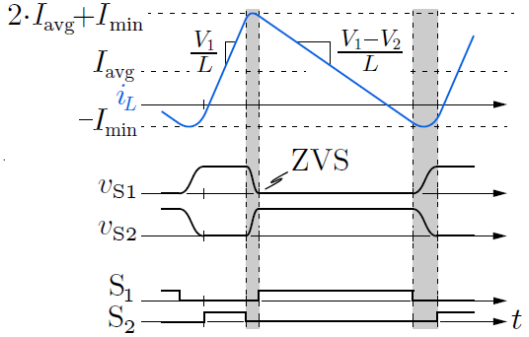
- 2-Level/Double Interleaved Booster
- Interleaved TCM Operation
- Turn-Off of Branch in Partial Load

- 2-Level/Double Interleaved
- Interleaved TCM Operation
- Turn-Off of Branch in Partial Load



TCM Operating Principle

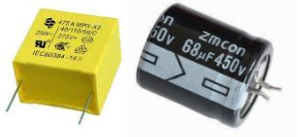




- ZVS for All Sw. Transitions
- Variable f_{sw}

- I_{min} to Limit f_{sw}
- Losses Due to I_{min} @ Low Loads

Components and Materials

	3L-PWM ▼	2L-PWM ▼	2L-TCM ▼
Power Semiconductors	 — 6 x Infineon Si IGBT H3 25 A 1200 V / PiN Diode — 6 x Infineon Si IGBT T&F 30 A 600 V / PiN Diode — 2 x Infineon Si IGBT T&F 30 A 600 V — Infineon Si PiN Diode 45 A 600 V	— 7 x CREE SiC MOSFET 80 mΩ 1200 V — 1 x CREE SiC Schottky Diode 20 A 1200 V	— 16 x CREE SiC MOSFET 80 mΩ 1200 V
Cooling System	 — Optimized Al Heat Sinks — Range of Sanyo Low Power Long Life DC Fans		
Main Induct.	 — METGLAS 2605SA1 Amorphous Iron C Cores — Solid Round Wire	*Or*	— EPCOS N87 Ferrite E Cores — Litz Wire With Range of Strand Diameters
DC Caps	 — EPCOS MKP DC Film Capacitors 575V and 1100 V for MPP Cap. — EPCOS Long Life Al Electrolytic Capacitors 500 V for DC-Link Cap.		
Filter	 — EPCOS X2 (DM/CM) and Y2 (CM) EMI Capacitors — Magnetics KoolMu Gapless Powder Cores / Solid Round Wire (DM) — VAC Vitroperm 250F/500F Nanocrystalline Toroid Cores / Solid Round Wire (CM)		

Global Optimization Routine

Independent Design Variables

- **3L-PWM**

$$\vec{\Pi}_{\text{sys}}^{\text{3LPWM}} : f_{\text{sw}} \in [6, 36]\,\text{kHz}, \quad \Delta I_{L,\text{max}}^{\text{pp}} \in [5, 60]\,\%$$

- **2L-PWM**

$$\vec{\Pi}_{\text{sys}}^{\text{2LPWM}} : f_{\text{sw}} \in [12, 72]\,\text{kHz}, \; \Delta I_{L,\text{max}}^{\text{pp}} \in [5, 60]\,\%$$

- **2L-TCM**

$$\vec{\Pi}_{\text{sys}}^{\text{2LTCM}} : f_{\text{sw,min}} \in [12, 84]\,\text{kHz}, \quad k_{f_{\text{sw}}} \in [4, 12]$$

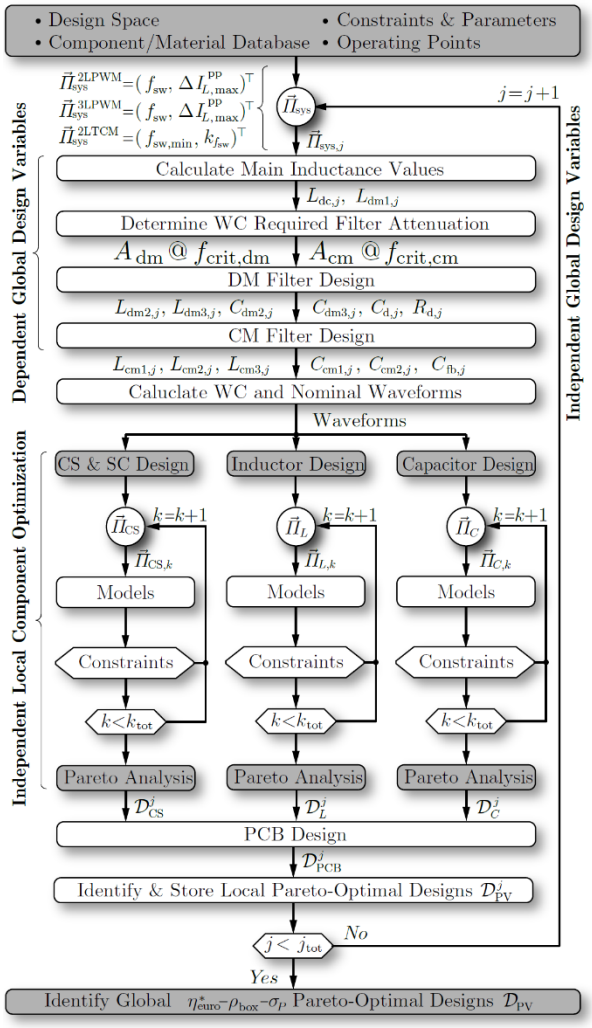
Dependent Design Variables

- **Main Inductances Function of f_{sw} and $\Delta I_{L,max}^{pp}$**
- **Filter Components Based on CISPR Class B**

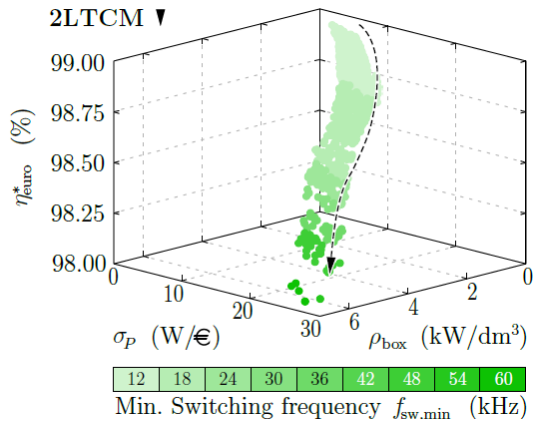
European Efficiency

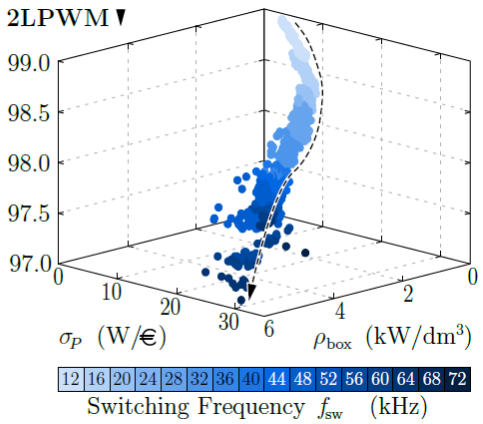
$$\eta_{\text{euro}} = 0.05 \cdot \eta_{0.03 \cdot P_r} + 0.1 \cdot \eta_{0.1 \cdot P_r} + 0.2 \cdot \eta_{0.2 \cdot P_r} + 0.3 \cdot \eta_{0.3 \cdot P_r} + 0.5 \cdot \eta_{0.5 \cdot P_r} + 1 \cdot \eta_{1.0 \cdot P_r}$$

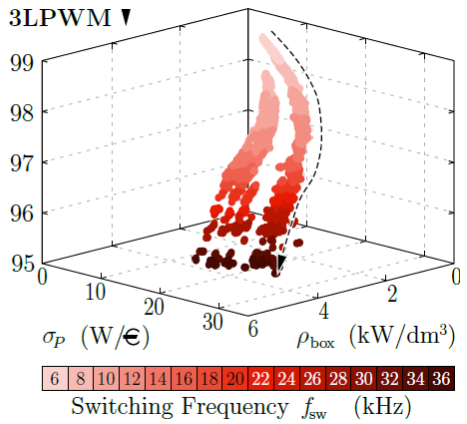
- **Add. Weighted for {525, 575, 625} V MPP Voltage**



Optimization Results - Pareto Surfaces (1)







- No Pareto-Optimal Designs for $f_{\text{sw,min}}$> 60 kHz
- No METGLAS Amorphous Iron Designs

- Pareto-Optimal Designs for Entire Considered f_{sw} Range
- No METGLAS Amorphous Iron Designs

- Pareto-Optimal Designs for Entire Considered f_{sw} Range
- METGLAS Amorphous Iron and Ferrite Designs

Optimization Results - Pareto Surfaces (2)

3L-PWM Core Material

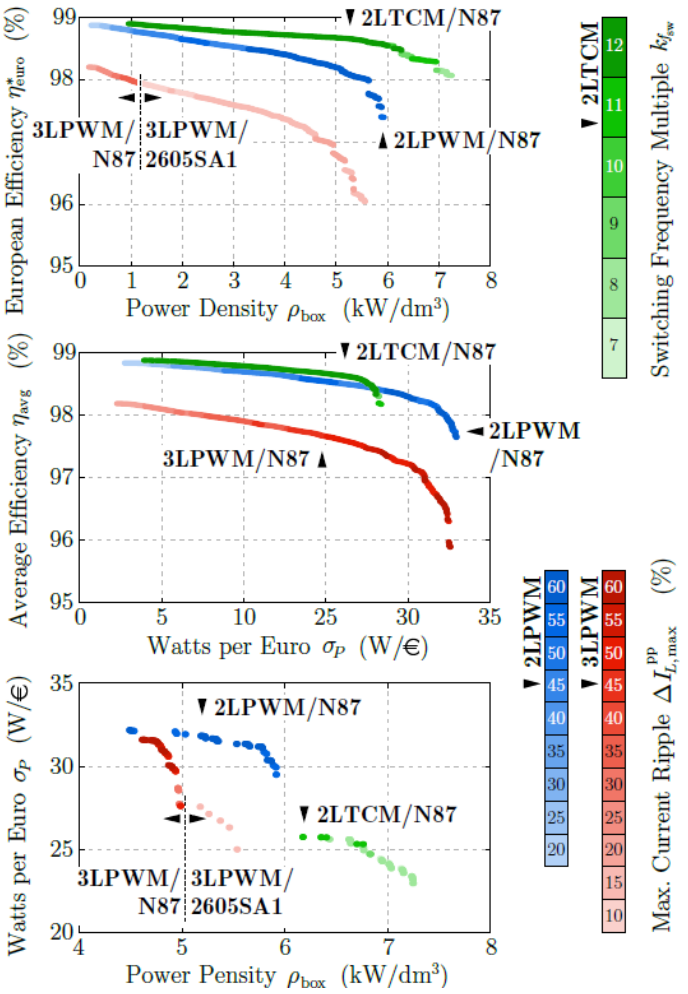
- Compact Designs with Amorphous Core Material @ Low Ripples
- Cheap Designs with Ferrite @ High Ripples Despite Larger Volume

2L-TCM Core Material

- Only Ferrite for 2L-TCM Due Large HF Excitations
- Expected Result

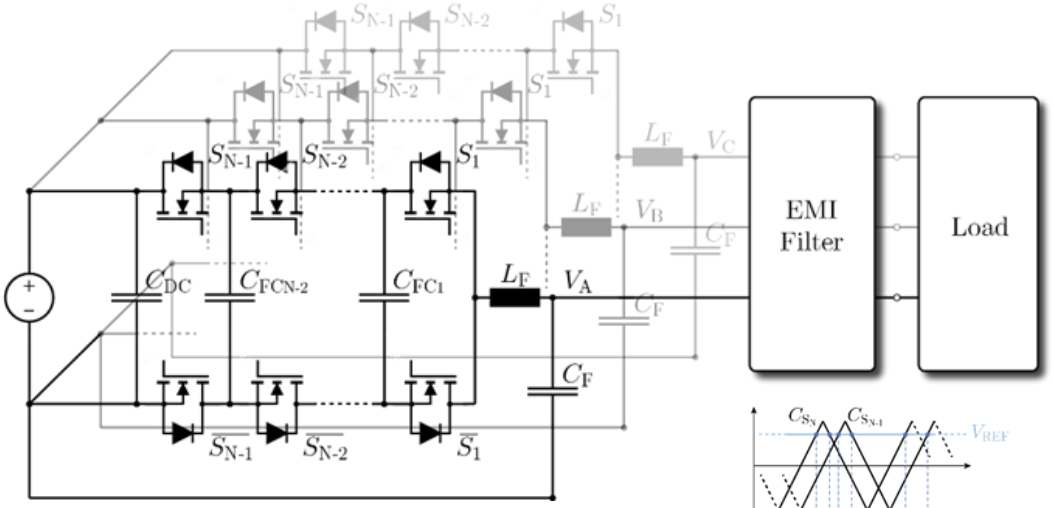
2L-PWM Core Material

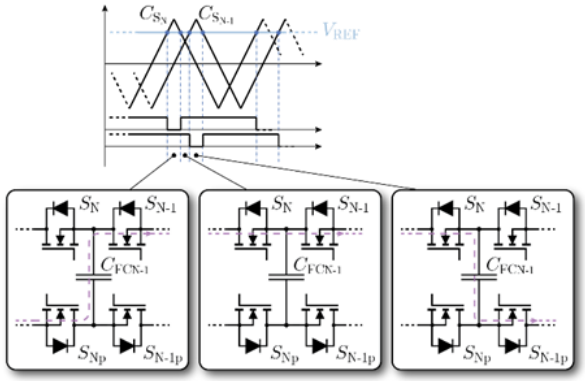
- Ferrite @ High Ripples Cheaper *AND* Smaller - Unexpected Result (!)
- Amorphous Core Material too High Losses Already @ Low Ripples, High Flux Density Not Exploited



Increasing the # of Levels - Flying Capacitor Converter (FCC)

- Each Cell Consists of 2 Switches / 1 Capacitor
- Phase-Modular Topology Supports DC/AC and AC/AC Conversion
- Standard Phase-Shift PWM



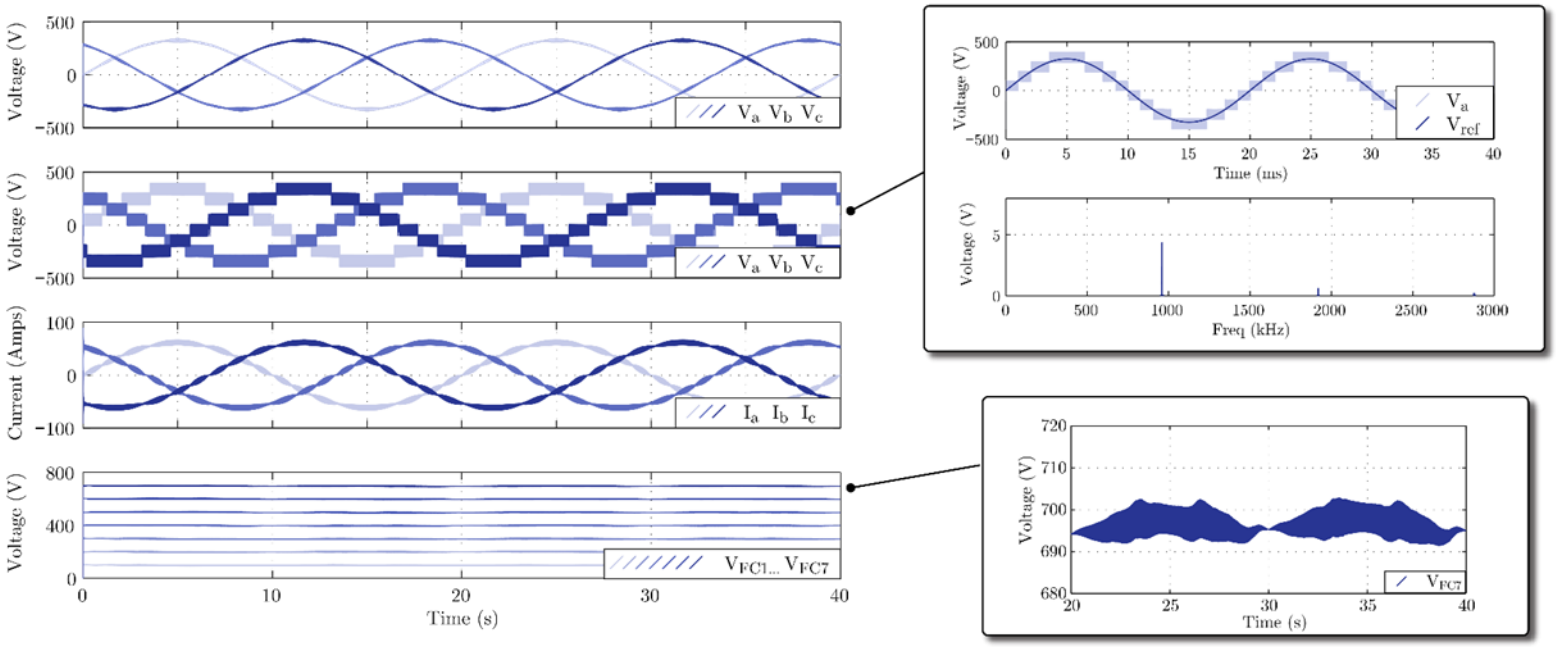


- Natural Capacitor Voltage Balancing
- No 50Hz Cap. Voltage Ripple

▶ Flying Capacitor Converter – Simulation Results (1)

- Example of N=9-Level FCC
- Switch Blocking Voltage: U_{Sw}= $U_{DC}/(N-1)$ → 100V @ 800V DC Link
- Effective Output Frequency $f_{Sw,eff}$= $f_{Sw}(N-1)$ → 960kHz @ 120kHz/Switch
- Standard Phase-Shift PWM

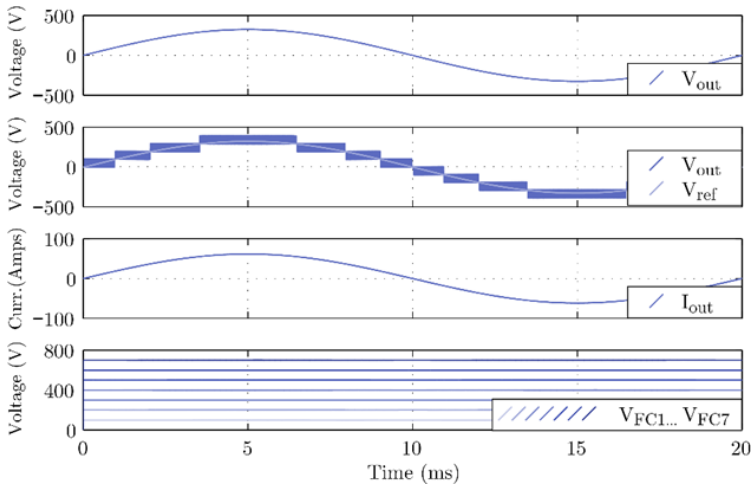
→ P=30kW C_{FC}= 10uF LC-Filter: 3uH / 1uF



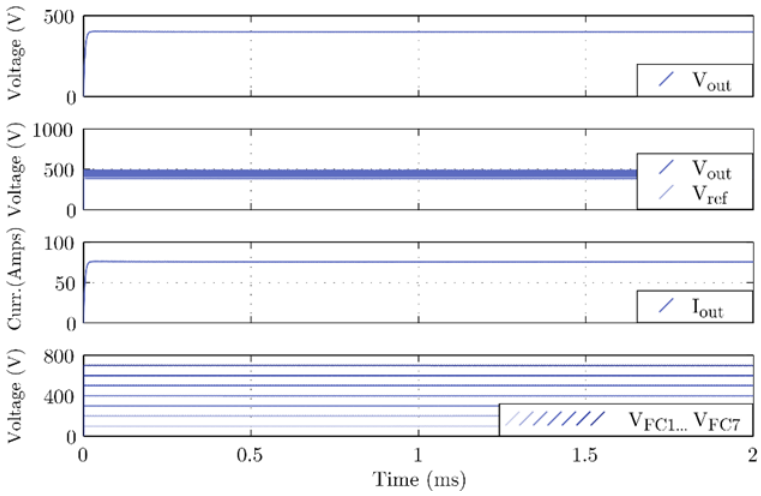
▶ Flying Capacitor Converter – Simulation Results (2)

- Concept Applicable for DC/AC and DC/DC Operation
- Design of Flying Capacitors only for Sw.-Frequency Components

→ AC/DC Operation ($800V_{DC}/400V_{AC}$)



→ DC/DC Operation ($800V_{DC}/400V_{DC}$)

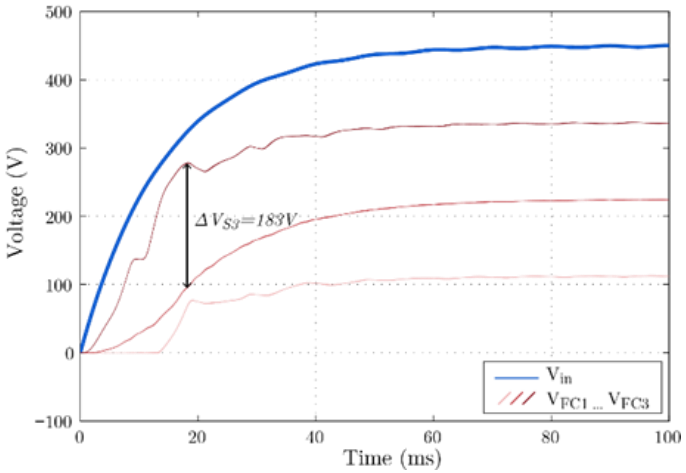


- Natural Flying Cap. Voltage Balancing Independent of Current Direction

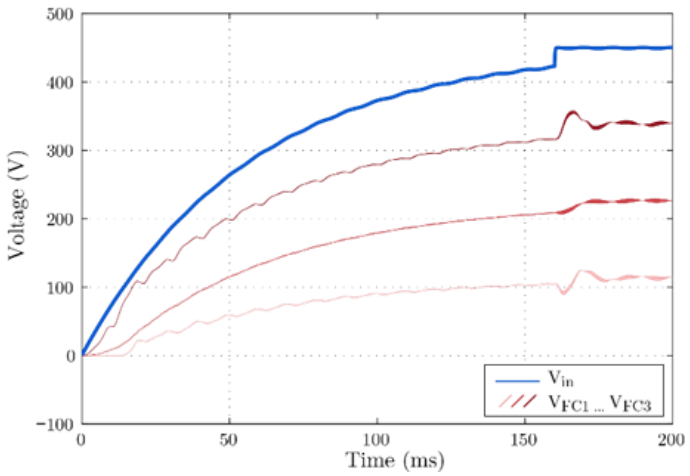
Flying Capacitor Converter – Simulation Results (3)

- **Design Issues:** Start-Up / Shut-Down / No-Load / Standby (DC Energized, No U_{out})
- **E.g. Startup:** U_{DC} Pre-Charging Time Constant $\tau_{DC} = R_{DC}C_{DC} > 2\,\tau_{FC}$

→ Pre-Charging w. Small τ_{DC}



→ Pre-Charging w. Sufficient τ_{DC}



→ Example of Startup of 5-Level FCC (U_{DC}=450V, U_{CF}≈ 110V)

3-Φ Buck-Type PFC Rectifier

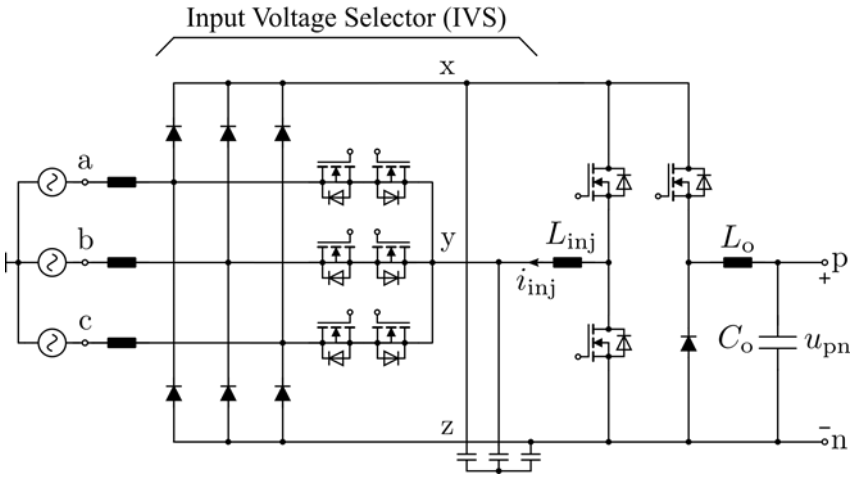
Integr. Active Filter Rectifier Concept
High Efficiency Demonstrator

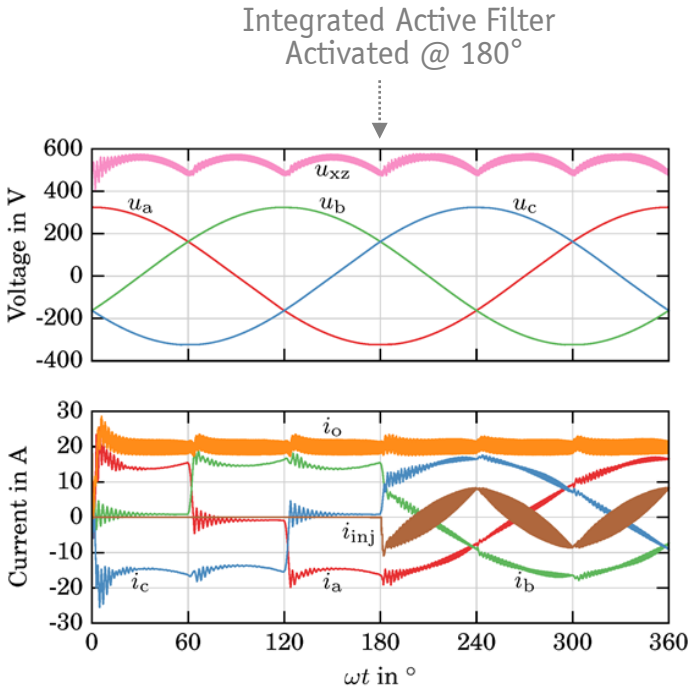
▶ 3-Φ Integrated Active Filter (IAF) Rectifier

- Injection of 3rd Harmonic Ensures Sinusoidal Input
- Six-Pulse Output of Uncontrolled Rectifier Stage
- Buck-Type Output Stage Generates DC Output from Six-Pulse Rectifier Output
- Three Devices in the Main Conduction Path

- Specifications

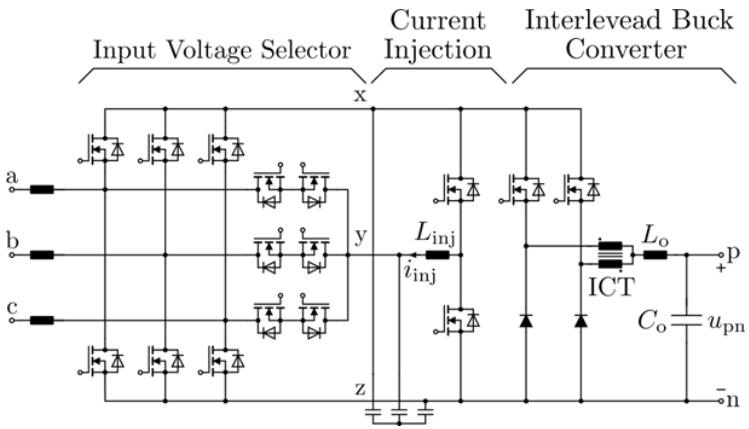
$V_{in} = 400V_{ac}$
$V_{out} = 400V_{dc}$
$P_{out} = 8kW$
$f_S = 27kHz$

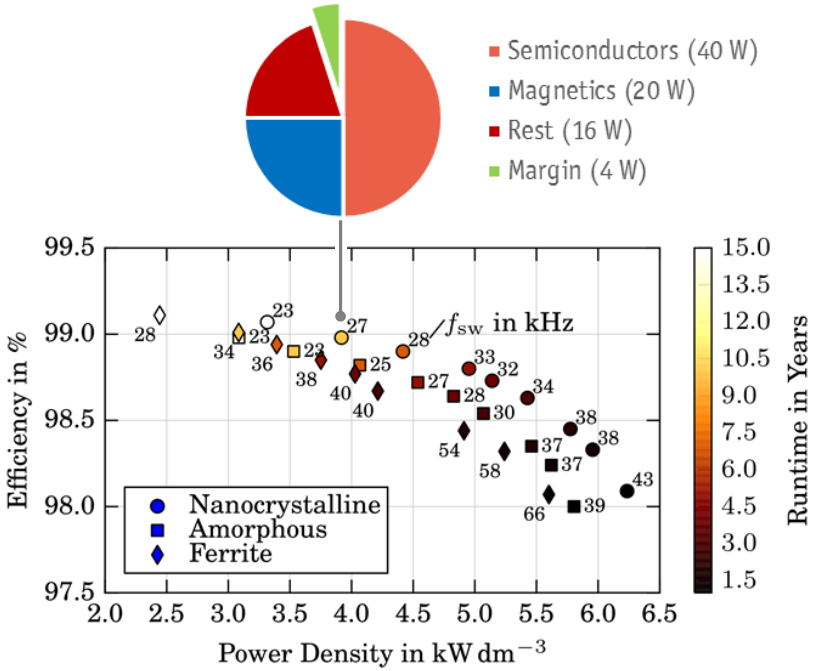




▶ 3-Φ IAF Rectifier Optimization

- Multi-Objective Optimization - Max. Efficiency / Max. Power Density / Min. Life Cycle Costs
- Life Cycle Costs: (i) Initial Costs & (ii) Electricity Costs of Converter Losses

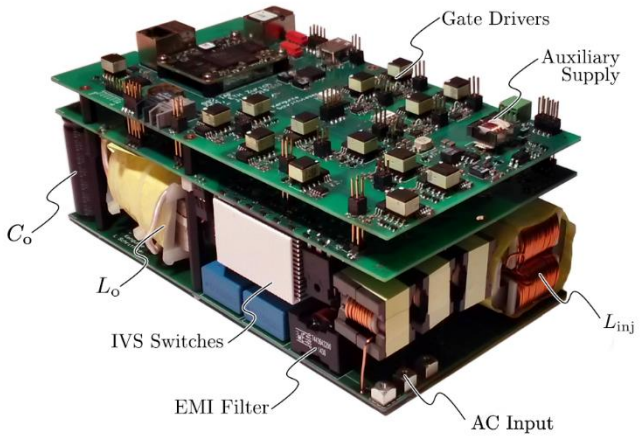




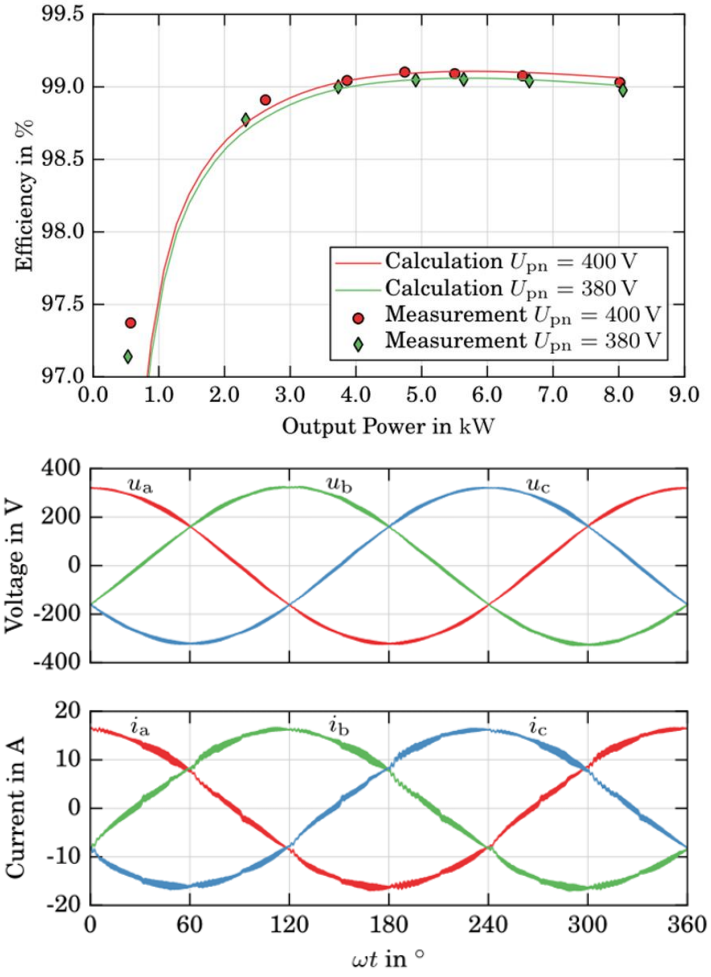
→ 10 Years of 24x7 Operation Demands η≈99% for Min. LCC

▶ 3-Φ IAF Rectifier Demonstrator

- Efficiency η> 99% @ 60% Rated Load
- Mains Current THD≈ 2% @ Rated Load
- Power Density ρ≈ 4kW/dm³



→ SiC Power MOSFETs & Diodes



Conclusions →

▶ Outlook

■ Research Targets @ ETH Zurich

- 1-Φ 250W/in³ @ 98% PFC Rectifier Module (EV Charger etc.)
- 1-Φ 99+% PFC Rectifier (Telecom etc.)
- 3-Φ Non-Isolated Very High Bandwidth AC Source
- 3-Φ Non-Isolated Ultra-Compact Inverter
- 3-Φ 99% Isolated Two-Stage (!) AC/DC Converter
- Bidirectional Extr. Eff. Resonant Multi-Port DC/DC Converters
- Design Space Diversity of Multi-Objective Optimization
- Little Box 3.0 / HF Magnetics (10MHz)
- Cellular Scalable Converter Topologies
- etc.

Thank You!

Questions