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Power Electronic Systems Laboratory

High Power Density On-Chip Switched Capacitor Converters for Microprocessor Power Delivery

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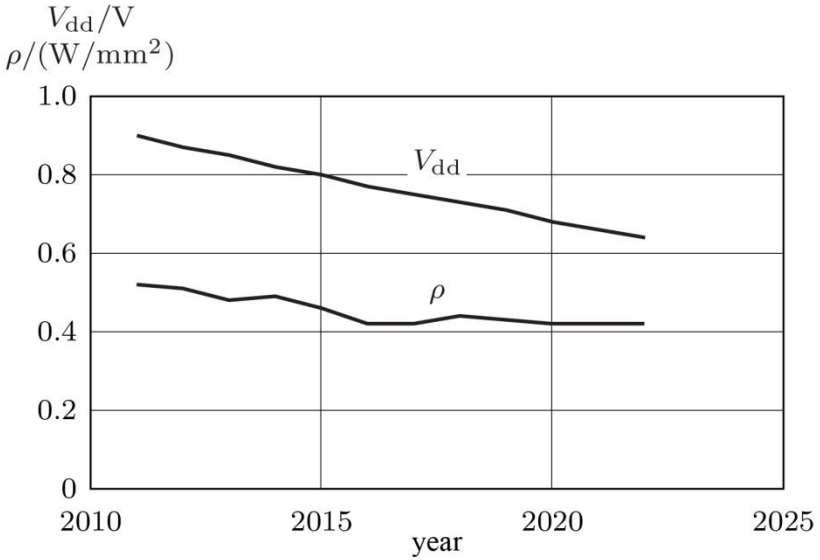
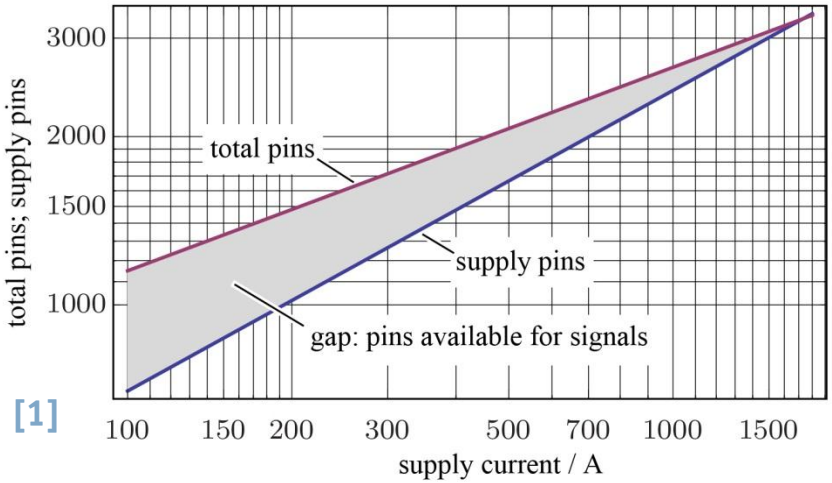
Trends in next generation microprocessors

- ITRS 2011 predicts:
  - Decreasing supply voltage
  - Close-to-constant power density
  - Increasing supply current



- Future projections
  - Higher supply current
  - Fewer signal pins

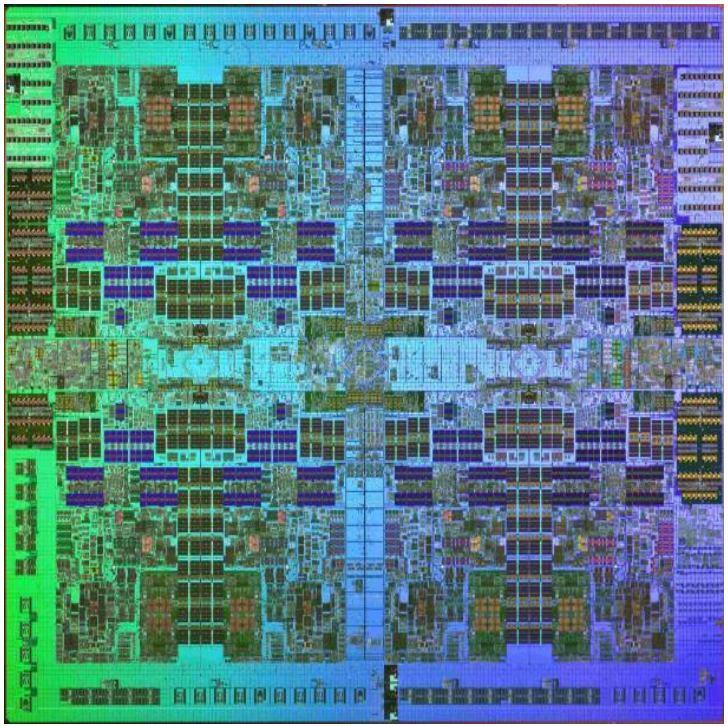


[1]

[1] Stanley-Marbell - ISLPED 2011 - Pinned to the walls — Impact of packaging and application properties on the memory and power walls

Motivation

- Increasing supply currents cause:
  - More power pins required
  - IR drops
  - Power supply instability $L\frac{\partial i(t)}{\partial t}$
- On-chip power conversion enables:
  - Higher input voltage – lower input current
  - Final power conversion on-chip
  - High granularity power distribution
  - Per-core regulation
  - Ultra-fast transient response (DVFS)
  - 3D chip integration and More-than-Moore
- On-chip microprocessor power supply requirements
  - Same microprocessor technology
  - High efficiency
  - High power density

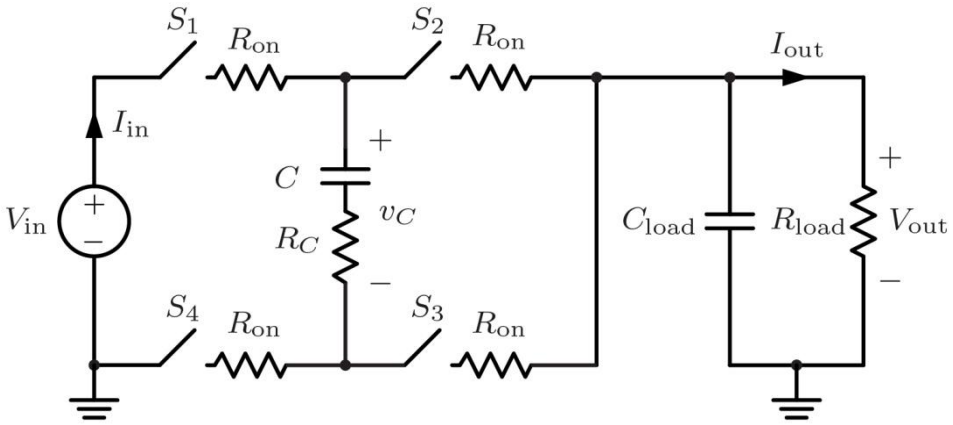


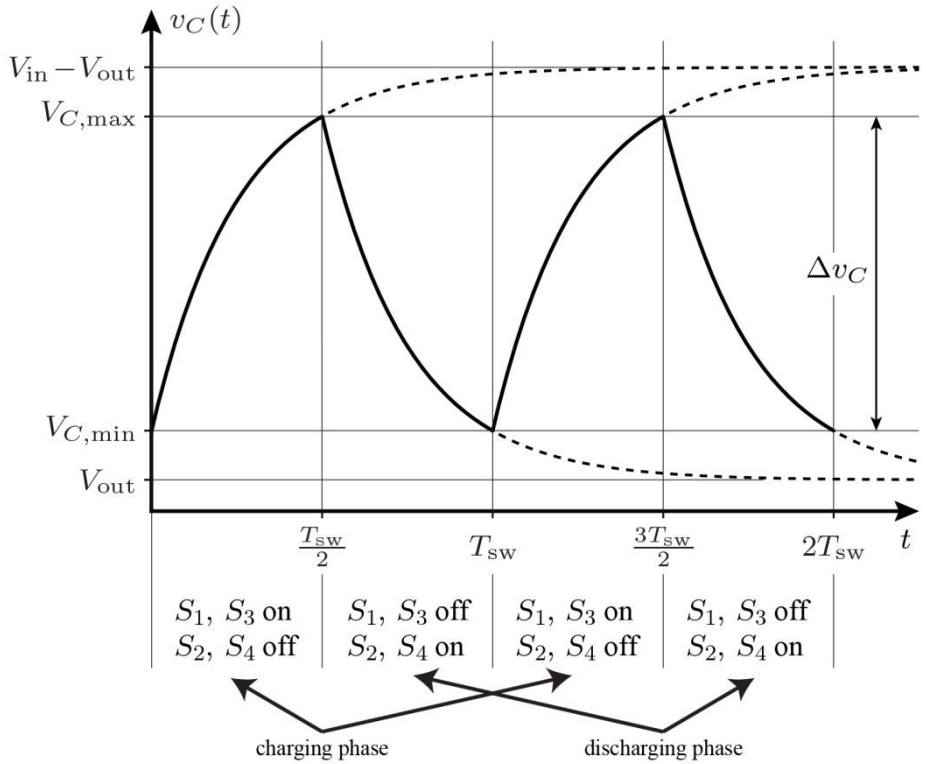
IBM power 7 CPU [online]

Outline

- Switched capacitor converter 2:1 power stage analysis
  - Analytical analysis
  - Simple design procedure
- Implementation in 32 nm SOI CMOS
  - Deep trench capacitor
  - Complete transistor level circuit diagram
  - Simple charge recycling
- Measurement results
- Conclusion and outlook

2:1 switched capacitor converter power stage model and analysis





Primary design equation:

$$I_{out} = Q_{tot} f_{sw} = 2C\left(V_{in} - 2V_{out}\right) k f_{sw}$$

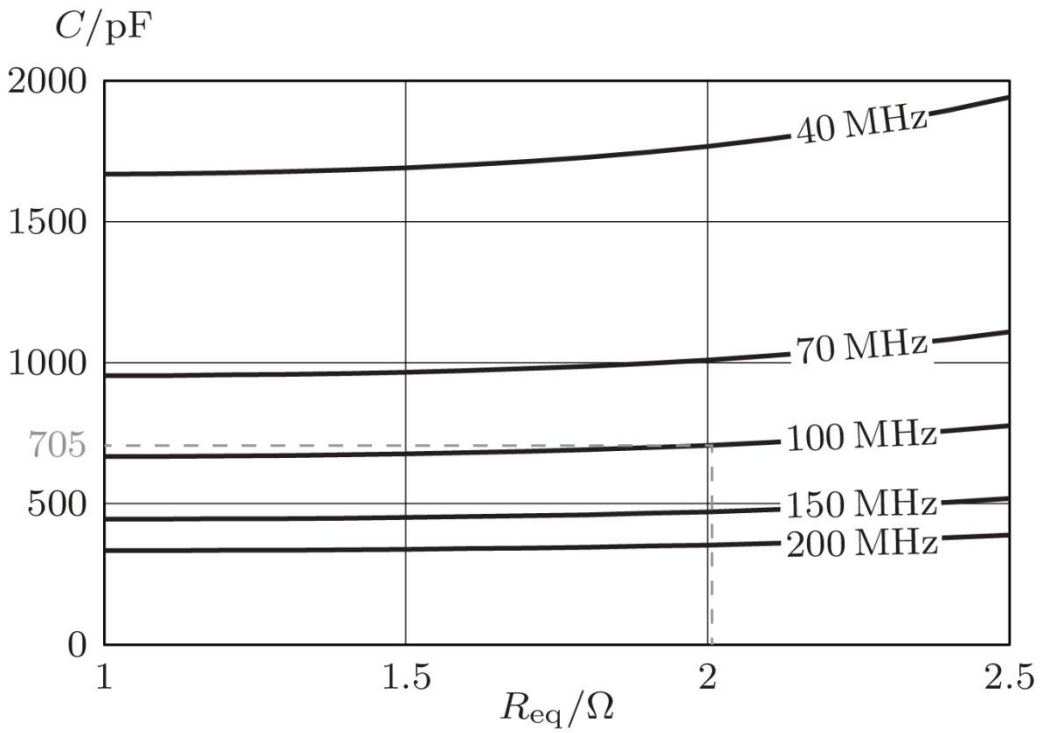
$$k = \frac{1-e^{-1/(2 f_{sw} R_{eq} C)}}{1+e^{-1/(2 f_{sw} R_{eq} C)}}$$

Switched capacitor converter design procedure

- Define power specification
  - $V_{\text{in}} = 1.8\ \text{V}$, $V_{\text{out}} = 825\ \text{mV}$, $I_{\text{out}} = 20\ \text{mA}$
- Select f_{sw}
  - Large influence on C
  - $f_{\text{sw}} = 100\ \text{MHz}$
- Select R_{eq}
  - Small influence on C
  - $R_{\text{eq}} = 2R_{\text{on}} + R_C + R_{\text{wiring}}$
  - $R_{\text{eq}} = 2\ \Omega$
- Determine C
  - $C = 705\ \text{pF}$
- Efficiency (conduction losses)
  - $\eta = \frac{2V_{\text{out}}}{V_{\text{in}}} = 91.7\%$

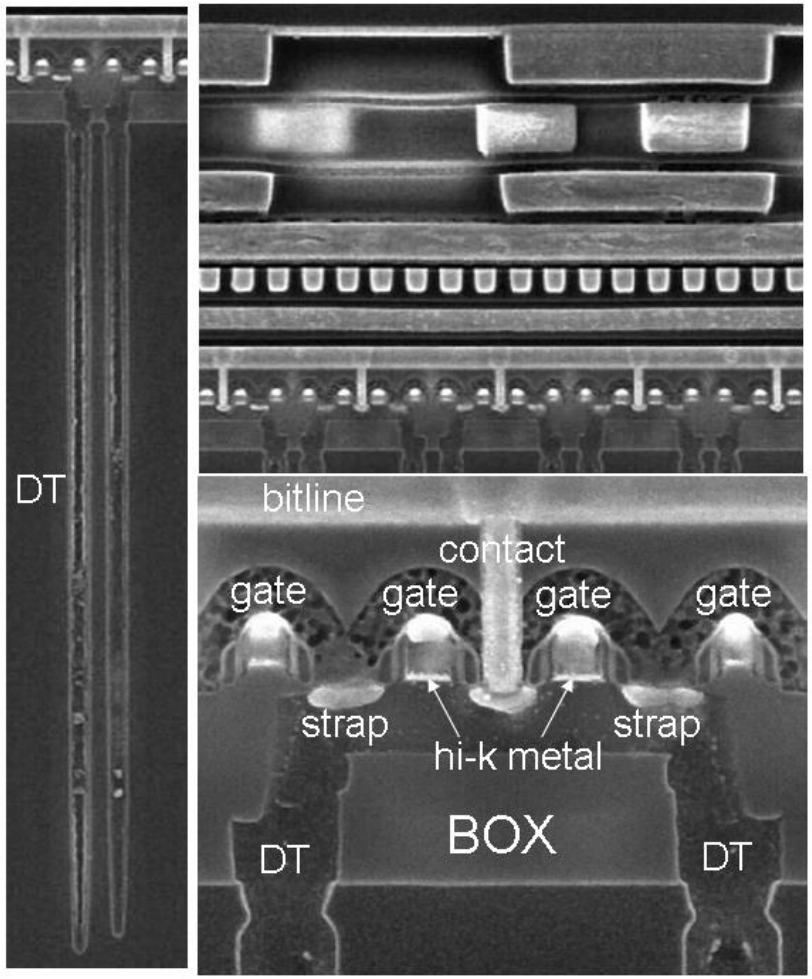
$$I_{\text{out}} = Q_{\text{tot}} f_{\text{sw}} = 2C\,(V_{\text{in}} - 2V_{\text{out}})\,k f_{\text{sw}}$$

$$k = \frac{1-e^{-1/(2f_{\text{sw}}R_{\text{eq}}C)}}{1+e^{-1/(2f_{\text{sw}}R_{\text{eq}}C)}}$$



Implementation of a 2:1 switched capacitor converter

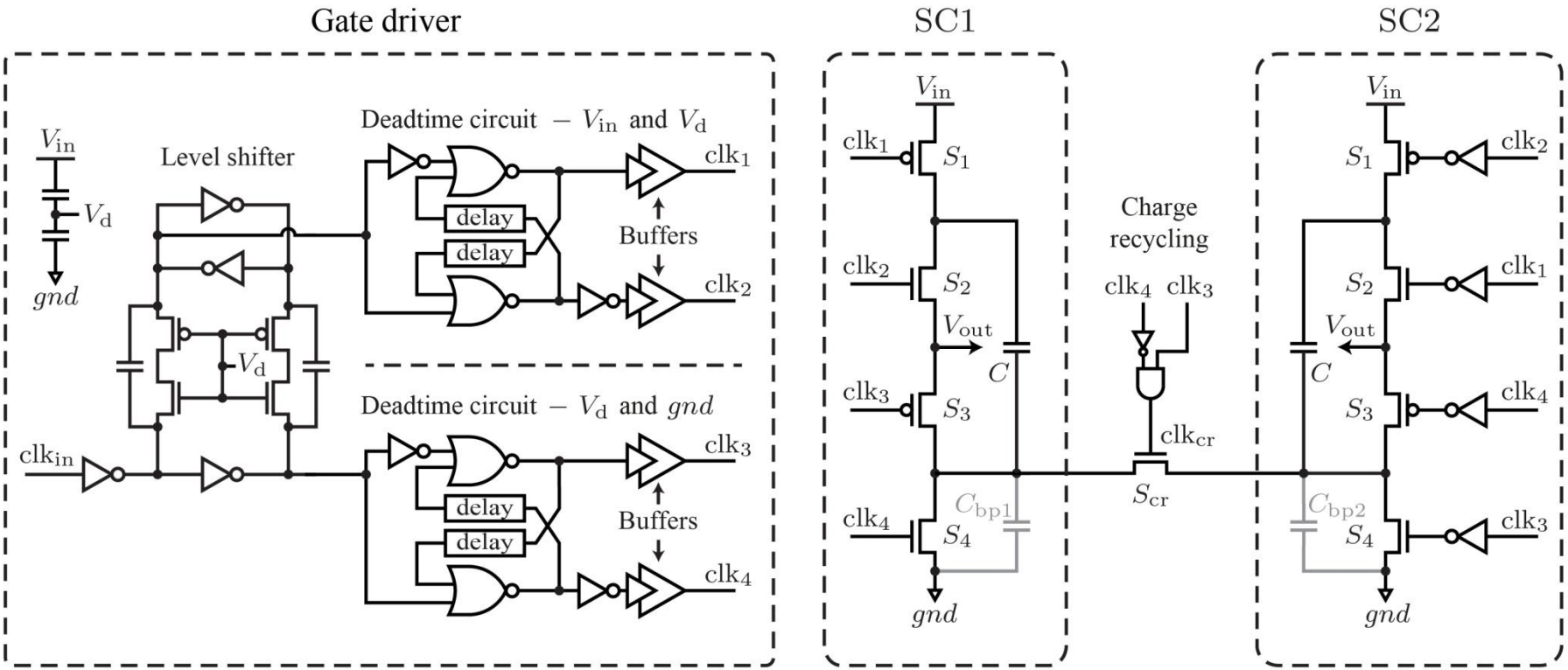
- 32 nm SOI CMOS technology
- Deep trench capacitors
  - High capacitance density
  - Low $\alpha = C_{\mathrm{bp}}/C$
- Fast transistors
  - Good R_{on} and Q_{g} figure-of-merit



Deep trench capacitor in 32nm SOI [2]

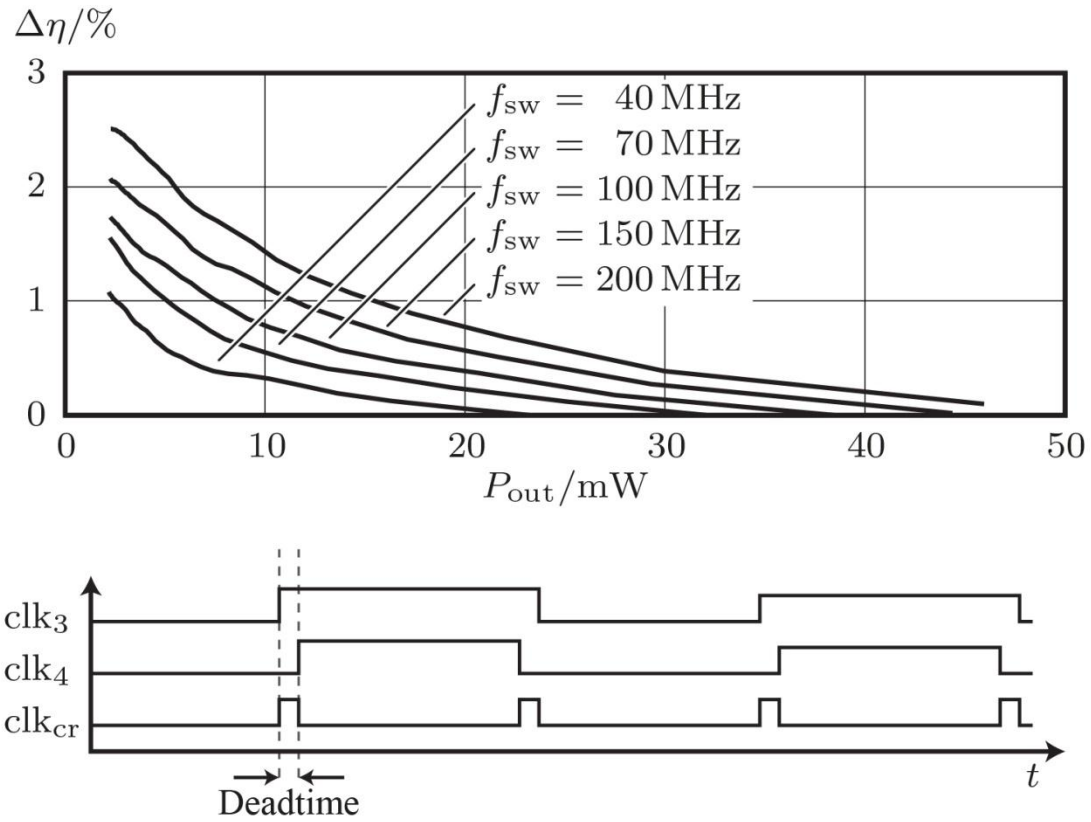
[2] Wang – EIDM 2009 – Scaling deep trench based eDRAM on SOI to 32nm and beyond

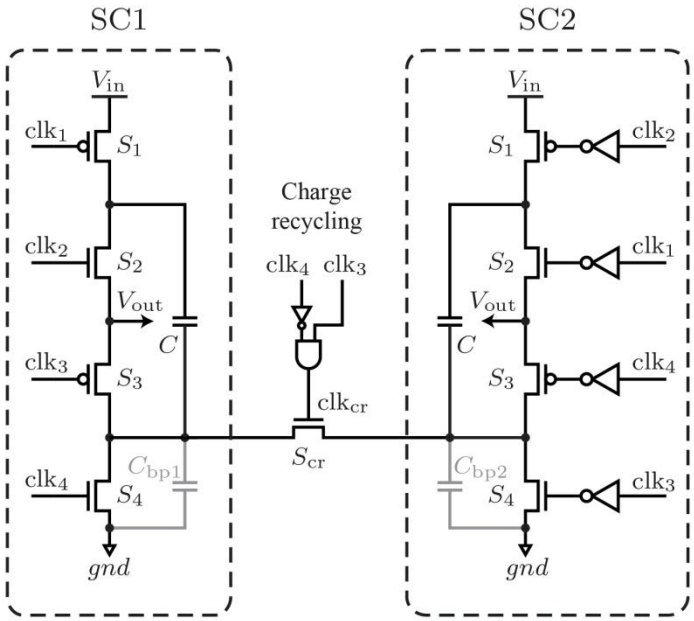
Complete circuit schematic



- Split switched capacitor (SC) converter power stage
  - Charge recycling circuit
- Stacked voltage domain gate driver
  - Ensures no over-voltage of all transistors

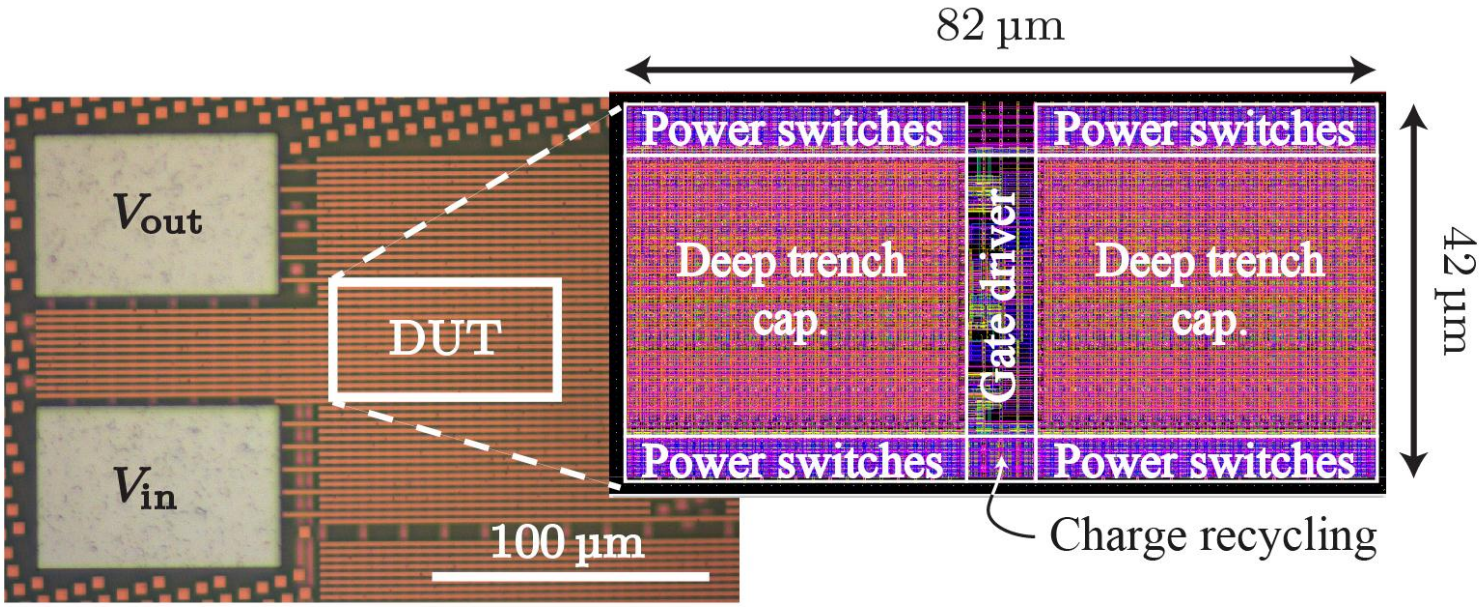
Charge recycling





- Reducing parasitic bottom plate capacitor losses

Implementation of a 2:1 on-chip switched capacitor converter in 32 nm SOI CMOS

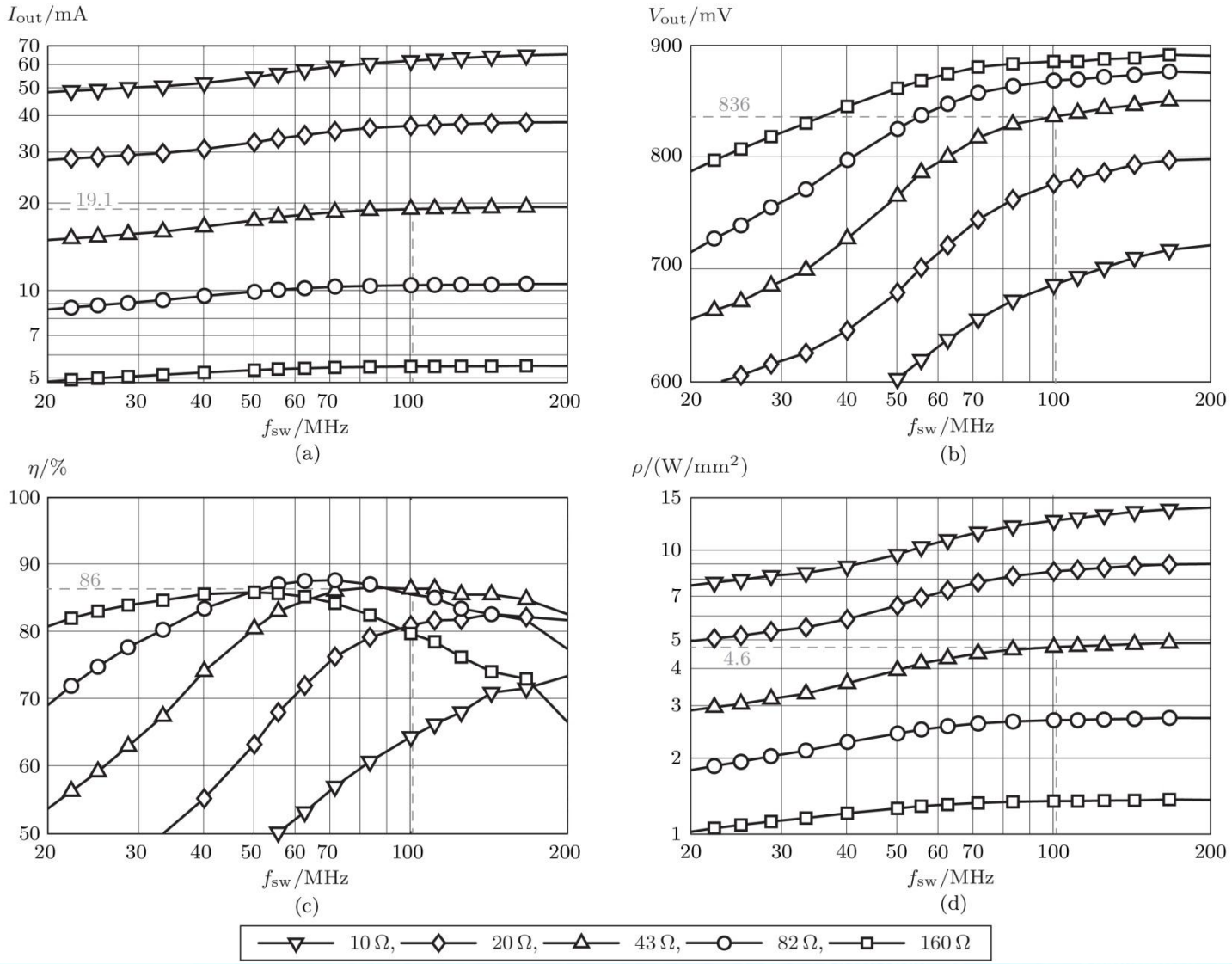


- Symmetrical layout style
  - Compatible with interleaving
  - Compatible with parallelling
- Estimated parameters
  - $C_{tot} \approx 690$ pF
  - $R_{eq,tot} \approx 2\ \Omega$

Measurement results

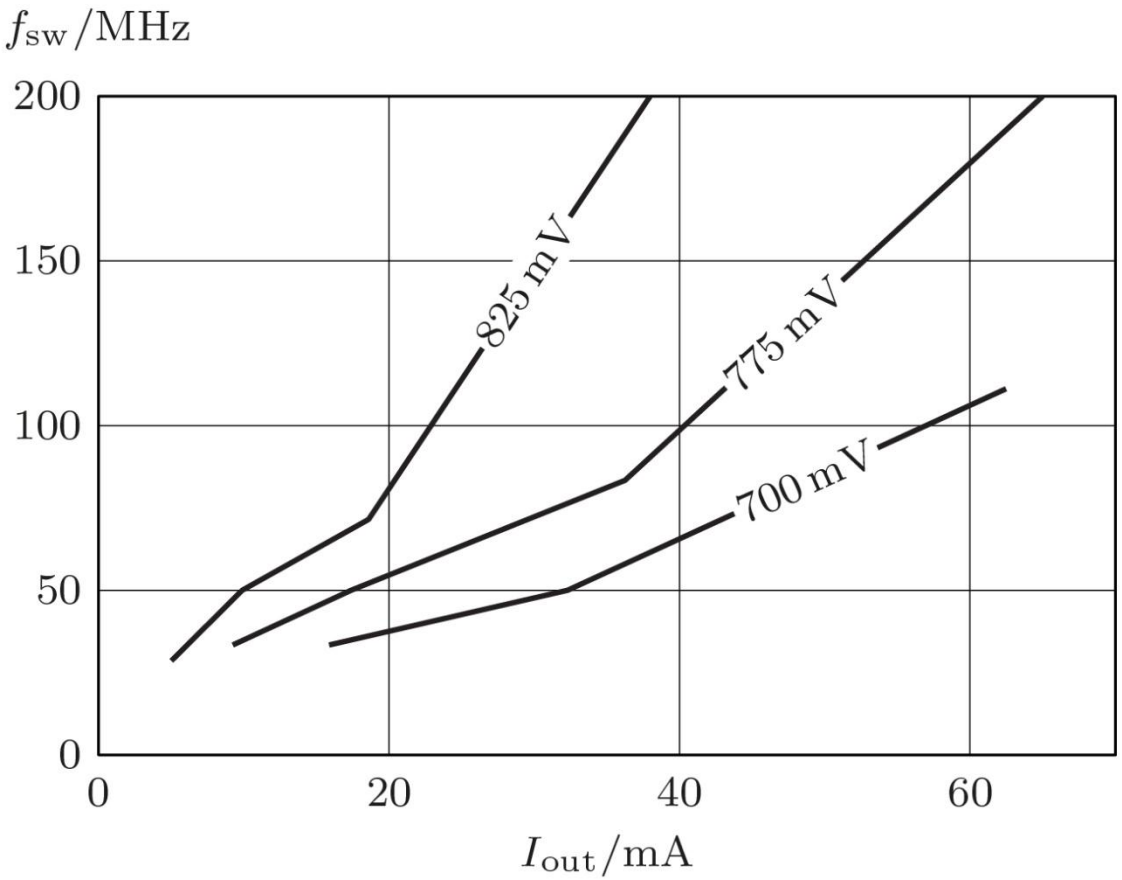
- Nominal operation
  - 1.8 V input voltage
  - 43 Ω off-chip load resistor
  - 100 MHz switching frequency
  - 33 nF off-chip output decoupling capacitor
- Measured performance at nominal operation
  - 836 mV output voltage
  - 19.1 mA output current
  - 16 mW output power
  - 0.00344 mm^2 converter area (including gate driver and charge recycling)
  - 4.6 W/mm^2 power density
  - 86% peak efficiency

Measurement results II



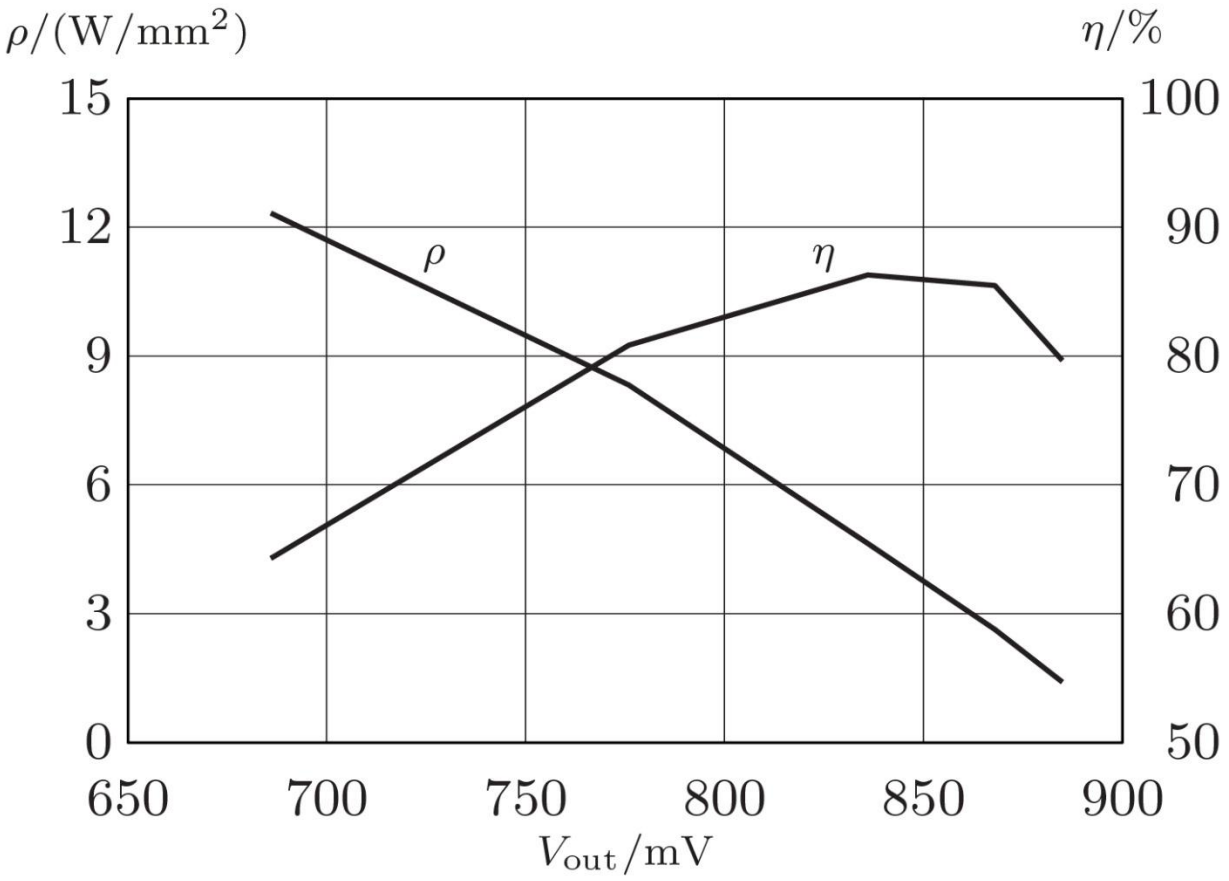
Measurements III

- Output voltage and current regulation capability
  - Frequency control



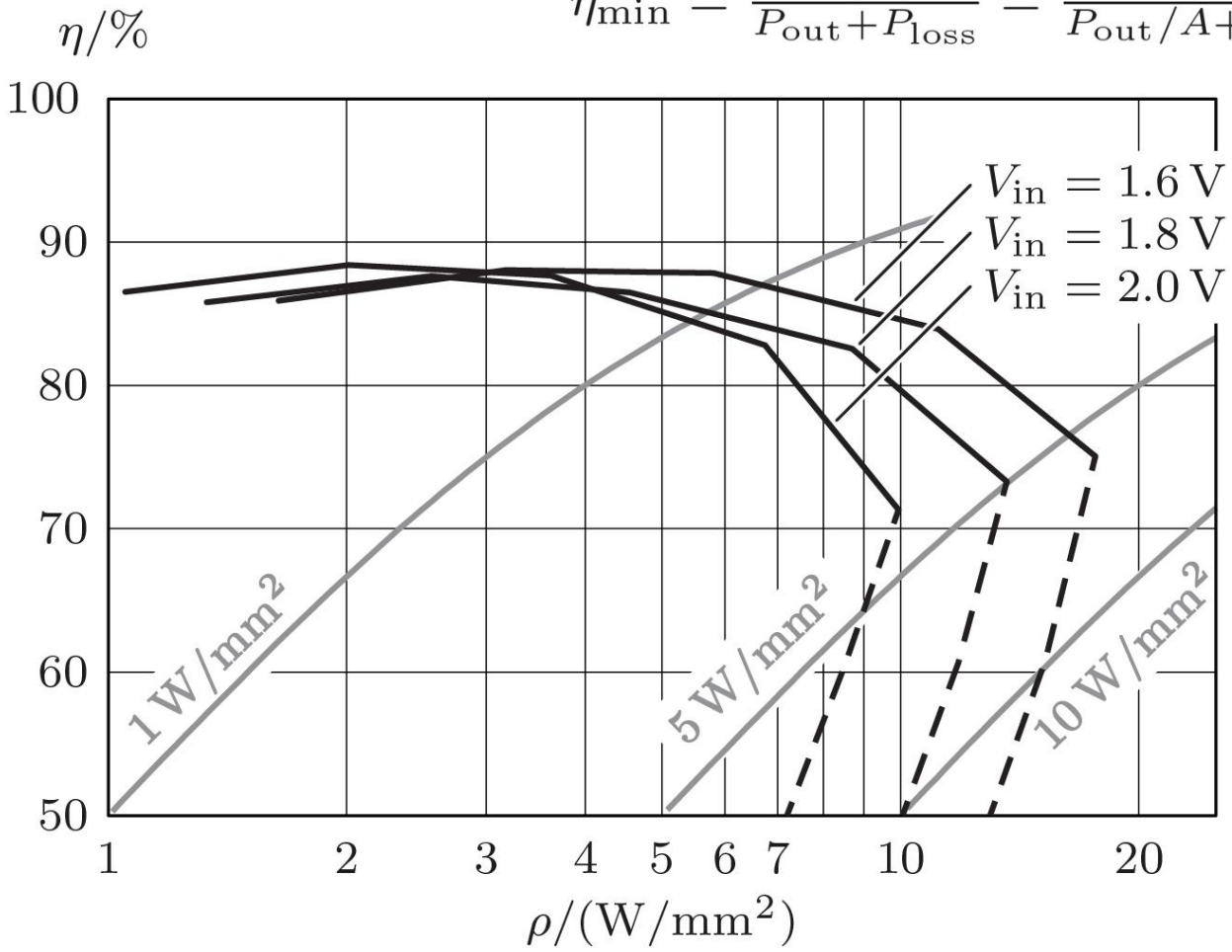
Measurements IV

- Trade-off between power density and efficiency over output voltage



Cooling requirements

$$\eta_{\min} = \frac{P_{\text{out}}}{P_{\text{out}}+P_{\text{loss}}} = \frac{P_{\text{out}}/A}{P_{\text{out}}/A+P_{\text{loss}}/A} = \frac{\rho}{\rho+\rho_{\text{cool}}}$$



7 W/mm² cooling power densities can be achieved [3]

[3] Escher, W – Experimental investigations of an ultrathin manifold microchannel heat sink for liquid cooled chips, J. Heat Transfer Aug. 2010

Conclusion and outlook

- High power density and efficiency achieved with on-chip switched capacitor converter
- Deep trench capacitors and fast transistors in the 32 nm SOI CMOS technology
- Simple charge recycling circuit to reduce the parasitic bottom plate capacitor losses
- Measurement results of a 2:1 conversion ratio on-chip switched capacitor converter
  - 4.6 W/mm^2 power density
  - 86% efficiency
- Outlook
  - Interleaving
  - Improved voltage and current regulation capability
  - Digital controller
  - Fast transient response times for DVFS
- Upcoming publication
  - Andersen, T. M. et al. - A 4.6W/mm^2 86% efficiency on-chip switched capacitor converter in 32nm SOI CMOS, APEC 2013, publication pending

Questions?