98.5% / 1.5kW/dm³ Multi-Cell Telecom Rectifier Module (230VAC/48VDC) – Breaking the Pareto Limit of Conventional Converter Approaches

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▶ Motivation

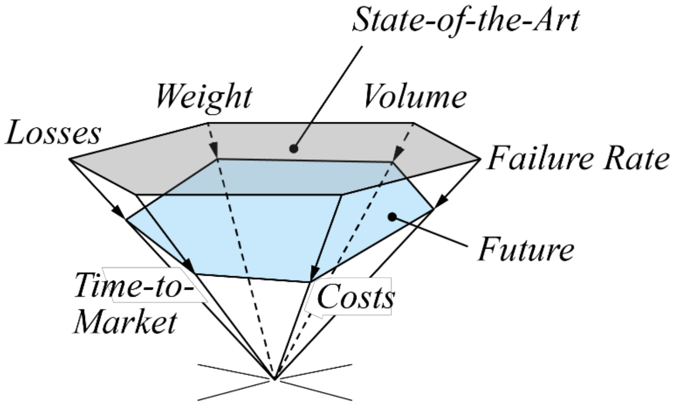
Leverage advantages of the multi-cell approach

- ▶ higher effective switching frequency due to phase shift
- ▶ lower filtering effort due to the cancellation of harmonics
- ▶ use of low-rated semiconductor devices
- ▶ improved thermal behavior due to a better surface-to-volume ratio

in order to shift the performance indices of power electronic converters to new levels.

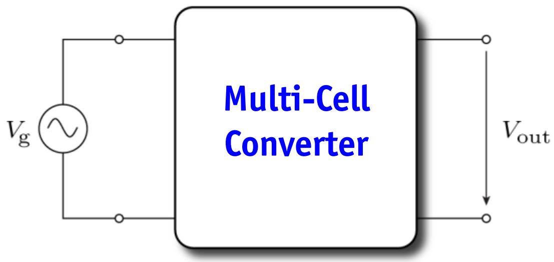
Performance indices

- Power Density [kW/dm³]
- Relative Losses [%]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Failure Rate [h⁻¹]
- Time-to-Market [months]



▶ Target Application

- **Telecom Rectifier Module**
  24/7 Always ON operation ▶ driver for high efficiency



- **Specifications:**

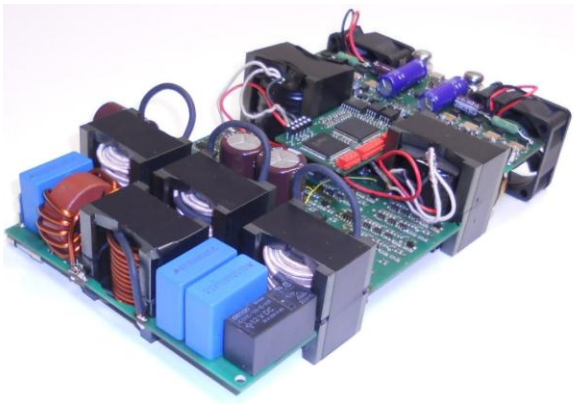
Input voltage:	230 V_{RMS} (180 V_{RMS} – 270 V_{RMS}) / 50 Hz
Nominal output voltage:	48 V DC
Output voltage range:	40-60 V DC
Rated power:	3.3 kW
Target efficiency:	98.5%
Target power density:	3 kW/L
Hold-up time:	10 ms at rated power
Switching frequency:	≥18 kHz (per module)
EMI standards:	CISPR Class A and Class B

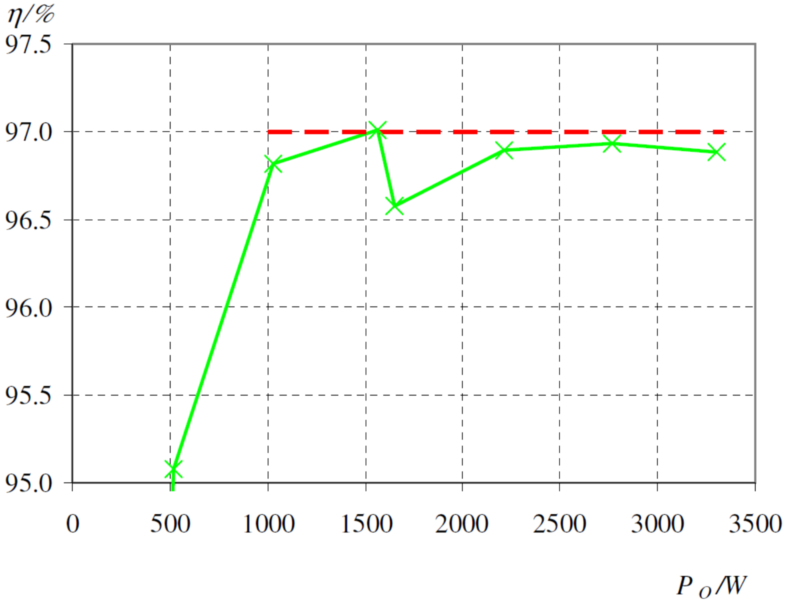
- **Output characteristics: Voltage source and current source**

▶ Benchmark: "Conventional" 3.3kW Telecom Rectifier Module

- ▶ 3x Interleaved TCM PFC Rectifier Stages
- ▶ 2x Interleaved Full-Bridge Phase-Shift DC/DC Conv. / Full-Bridge Synchr. Rectifier

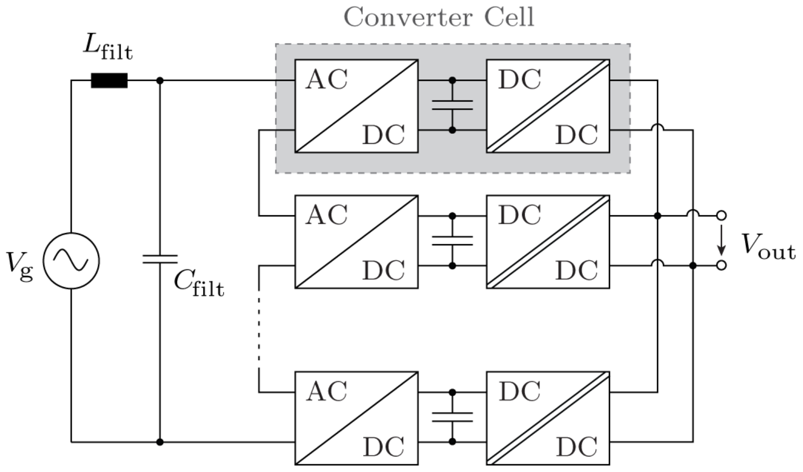
★ 97% @ 3.3kW/dm^3



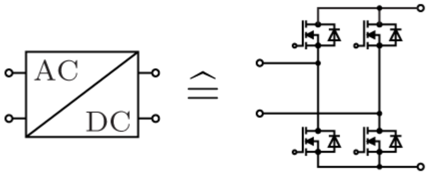


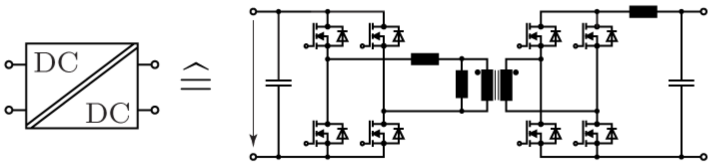
▶ Multi-Cell Telecom Rectifier

- Multiple converter cells connected in Input Series Output Parallel (ISOP) connection
  - ▶ Natural step down ratio of $1/N_{cell}$



- Each converter cell consisting of a
  - Full bridge rectification ▶ Totem Pole
  - Isolated DC-DC converter ▶ Phase Shift Full Bridge w/ sync. rect.





▶ Degrees of Freedom in Multi-Cell Converters Optimizations

- Converter realization possibilities

Converter cell combination [ISOP, ISOS, IPOP, IPOS]

↓

Converter cell topologies

↓

Number of converter cells [3…10]

↓

Voltage drop of DC-link during hold-up time [10%…40%]

AC/DC stage

Switching frequency
Input current ripple
Boost inductor realization
MOSFET chip size and junc. temp.
DC link capacitor realization
Input filter design

DC/DC stage

Switching frequency
Transformer realization
MOSFET chip size and junc. temp.
Output current ripple
Output inductor realization

▶ Calculation of losses and volumes for all (!) design combinations

▶ Optimization Setup and Converter Modelling

Analytic modelling of losses and volumes necessary for optimization

MOSFETs

- Conduction losses ▶ RMS current values
  ▶ $R_{DS,on}(T_j, A_{Chip})$
- Switching losses ▶ U_{Sw}, I_{Sw}, f_{Sw}
  ▶ $C_{OSS}(A_{Chip}), Q_{rr}(A_{Chip}), C_{GD}(A_{Chip})$
- Heat sink volume ▶ $R_{Th,JC}(A_{Chip})$, CSPI

} Find optimal A_{Chip}

Inductive components

- Core losses ▶ iGSE (improved generalized Steinmetz equation)
- Winding losses ▶ DC and AC losses (skin & proximity effect)

Electrolyte DC-link capacitors

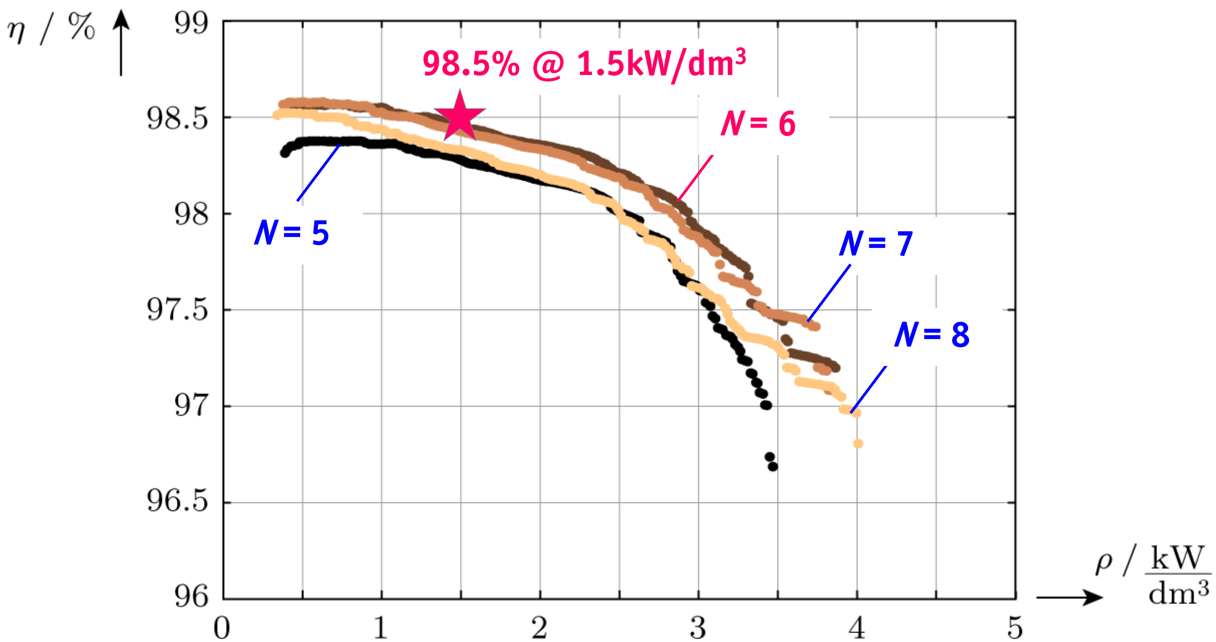
- ESR and leak. curr. losses ▶ RMS current @ 100Hz & f_{sw}

Input filter ▶ Volume

Auxiliary losses ▶ Central controller and aux. electronics per module

▶ Full System Optimization Results

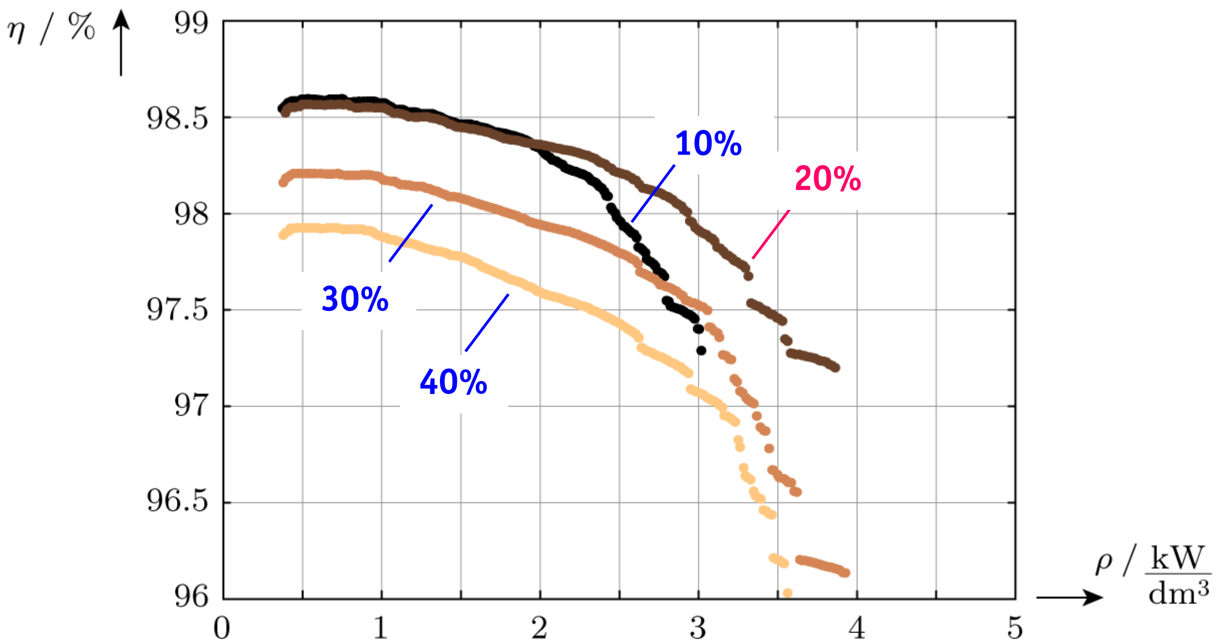
- Pareto optimal results for full load operation.
- Determination of the optimal number of converter cells.
- Voltage drop of the DC-link voltage during hold-up time 20%.



▶ Choose $N = 6$ due to lower communication and hardware realization efforts.

▶ Full System Optimization Results

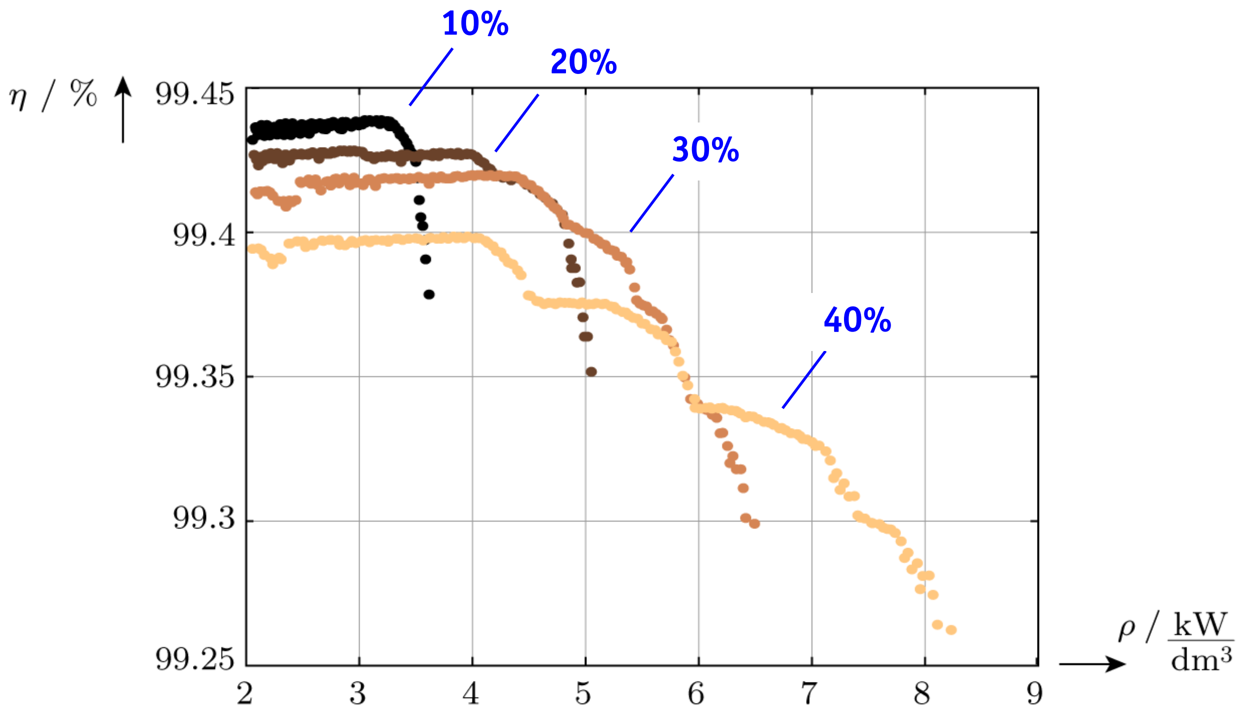
- Determination of Pareto optimal voltage drop of the DC-link voltage during 10 ms hold-up time
- Number of converter cells *N* = 6



▶ Which trade-offs lead to 20% voltage drop of the DC-link during the hold-up time as best value?

▶ Optimization Results: AC/DC Rectifier Stage

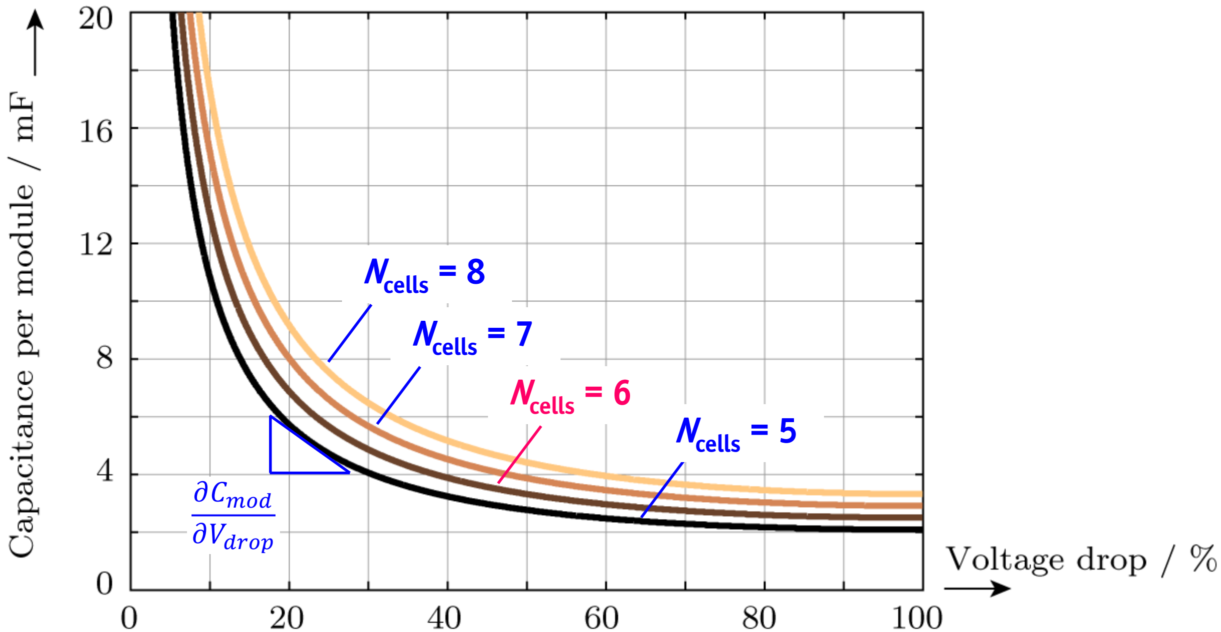
- Pareto-optimal results for the PFC stage for different permissible DC-link voltage drops
- Number of cells $N = 6$



▶ Main influence on efficiency/power-density by DC-link electrolyte capacitors.

▶ Optimization Results: AC/DC Rectifier Stage

- Required capacitance per module for different number of cells N_{cells} vs. the voltage drop during the hold-up time.



▶ A voltage drop of 20% … 30% is a reasonable choice with respect to the required capacitance.
▶ Larger voltage drop → lower capacitance (and volume) → larger ESR (and losses)

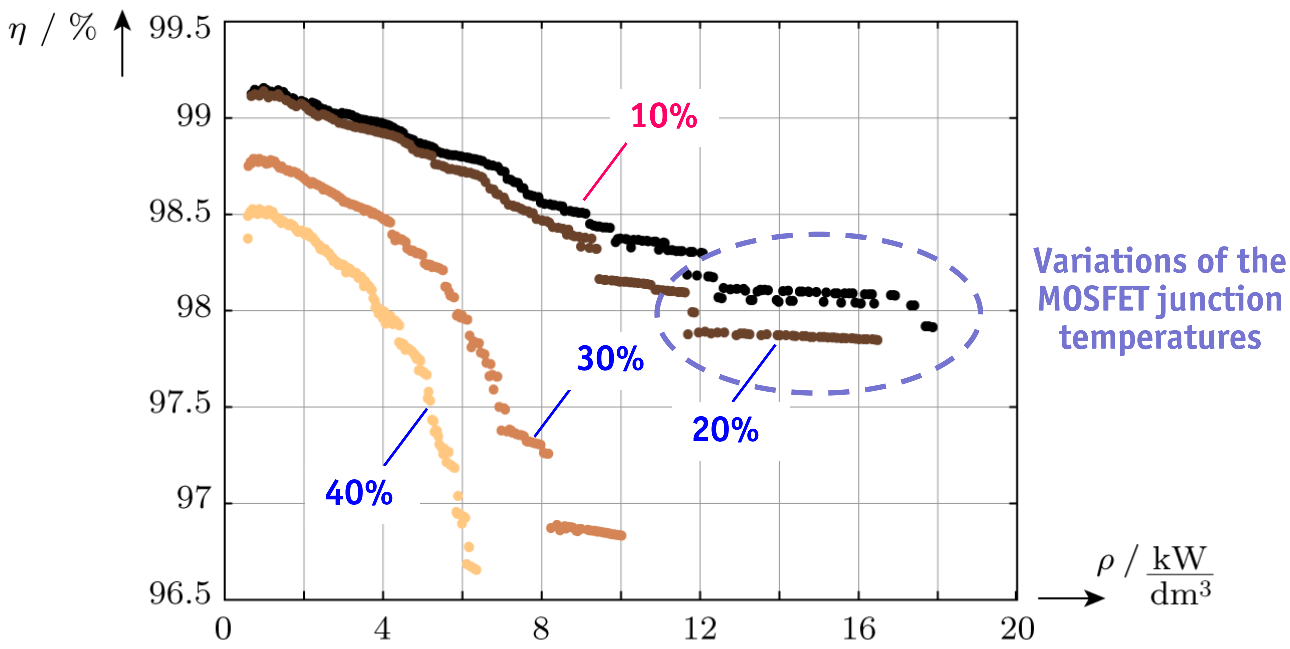
► Summary of Results for the AC/DC Rectifier Stage

A larger voltage drop leads to

- ► larger capacitor losses due to a larger ESR.
- ► a smaller capacitor volume since less capacitance is needed.
- ► no change in MOSFET losses.
- ► no change in inductor losses.

▶ Optimization Results: DC/DC Converter Stage

- Pareto-optimal results of the Phase-Shift Full Bridge converter stage.
- Number of converter cells $N = 6$.



▶ The performance improves with lower permissible voltage drop values during the hold-up time.

► Summary of Results for the DC/DC Converter Stage

A larger voltage drop leads to

- a larger output inductance and thus either higher losses or a larger volume.
- higher transformer losses since a lower duty cycle and a larger turns ratio are required (→ less winding area per turn and higher RMS currents).
- larger RMS current values in the primary full-bridge MOSFETs.
- larger reverse recovery losses due to a higher blocking voltage.

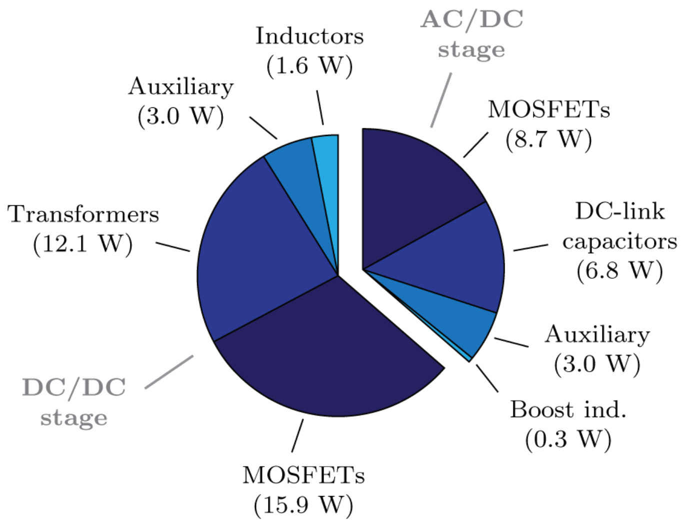
Final System

Parameters of the final system

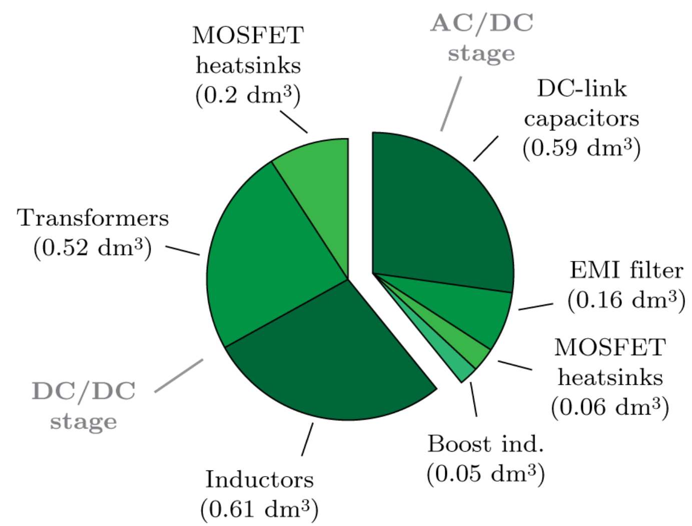
- Efficiency: 98.5% @ $P_{load} = 0.8\ P_{rated}$
- Power density: 1.5 kW/L
- $N_{cells} = 6$
- Voltage drop during hold-up time: 20 %
- AC/DC rectifier stages
  - Sw. freq.: 18 kHz (per cell)
  - Boost inductor: 8 µH, 2x E 34/14/9, Metglas
  - DC-bus capacitors: 4x 2.2 mF
  - Total DC link voltage: 400V
  - MOSFETs: BSC046N10NS3 / Infineon @ $T_j = 75°C$
- Isolated DC/DC converters
  - Sw. freq.: 100 kHz
  - Transformer: 2x E 47/20/16, N87
  - Inductor: 41 µH, E 47/20/16, N87
  - MOSFETs: BSC046N10NS3 / Infineon @ $T_j = 60°C$

▶ Final System

- **Loss distribution (at full load operation)**



- **Volume distribution**



	Losses	Volumes
AC/DC stage	18.8 W	0.86 dm^3
DC/DC stage	32.6 W	1.33 dm^3
Total	**51.4 W**	**2.19 dm^3**

▶ Conclusions and Outlook

- The benefits of the ISOP multi-cell converter approach allow to achieve efficiencies beyond the barriers of state-of-the-art systems.

- A comprehensive system optimization yields
  - an optimum number of converter cells
  - an optimum permissible voltage drop in the DC-link
  - an efficiency/power-density Pareto front for the entire system for all possible combinations of AC-DC rectifier and DC-DC converter stages.
  - A design with an efficiency of 98.5% at a power density of 1.5 kW/dm^3

- Future work
  - Experimental verification of optimization results

► Thank you very much for your attention!

Please feel free to ask questions