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Power Electronic Systems Laboratory

Closed-Loop di/dt and dv/dt IGBT Gate Drive Concepts

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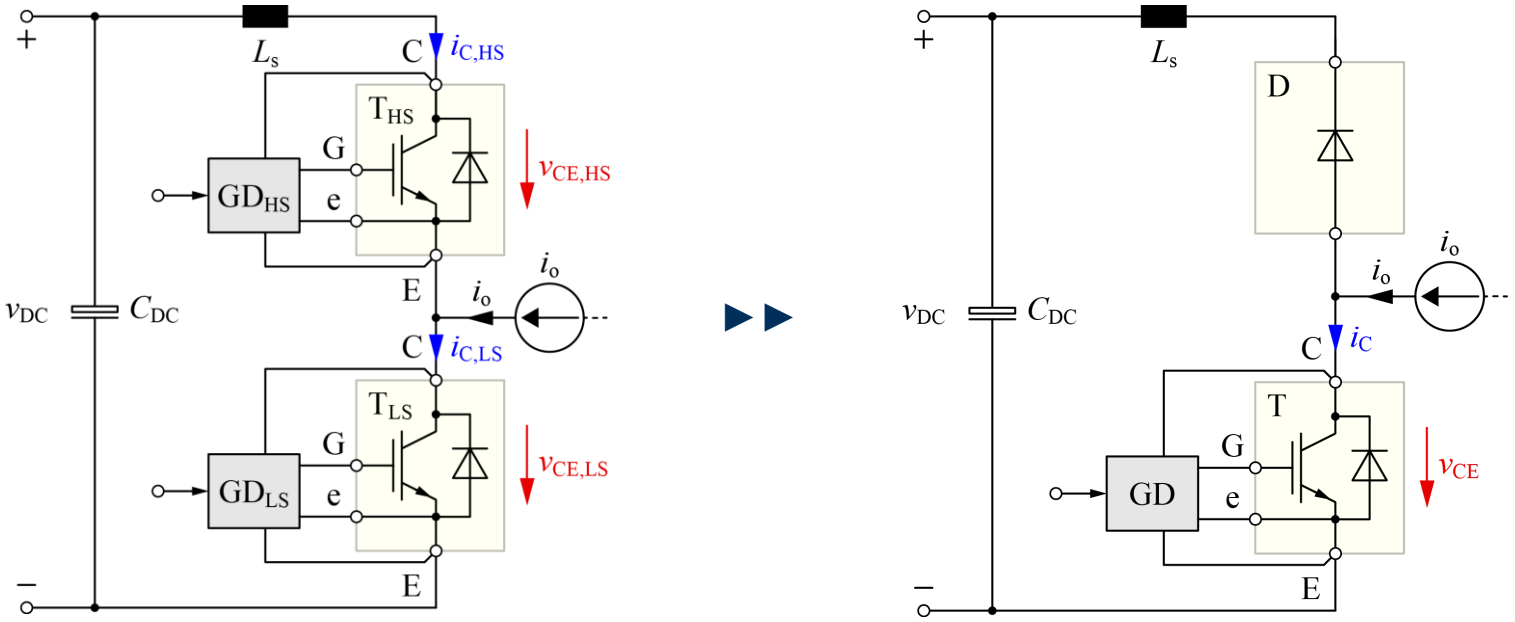
Outline

- Switching Trajectory Trade-Off / Challenges
- State-of-the-Art IGBT Switching Trajectory Control
- New Closed-Loop di/dt and dv/dt IGBT Gate Drive
- Future Trends

Clamped Inductive Load (Hard) Switching

▶ Equivalent circuit for switching trajectories



- **Main goals:** lowest delay times / switching losses / EMI & SOA operation at all operating points (load current levels, junction temperatures, ...)

Trade-Off / Main Goals

- Low Switching Delay Times
- Low Switching Losses
- Low EMI
- SOA Operation

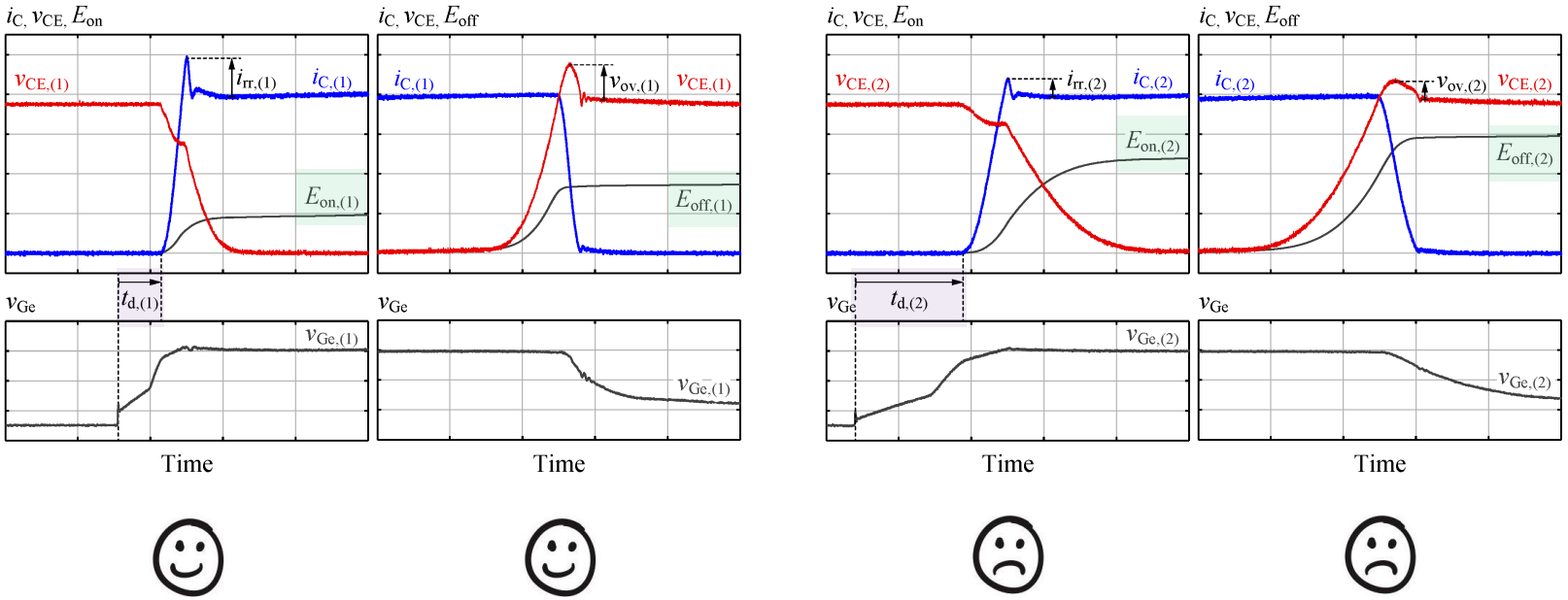
Switching Delay Times / Switching Losses

▶ Fast switching (small gate resistor)

- High di/dt and dv/dt values
- Low switching delay times t_d
- Low switching losses $E_{on/off}$

▶ Slow switching (large gate resistor)

- Low di/dt and dv/dt values
- High switching delay times t_d
- High switching losses $E_{on/off}$

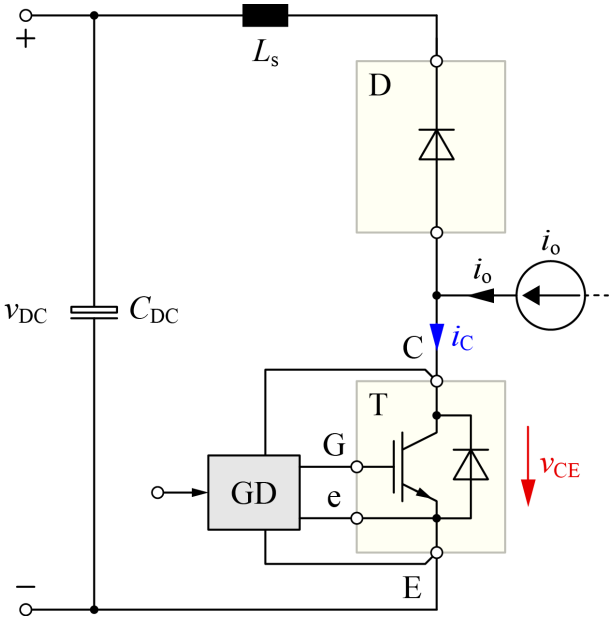


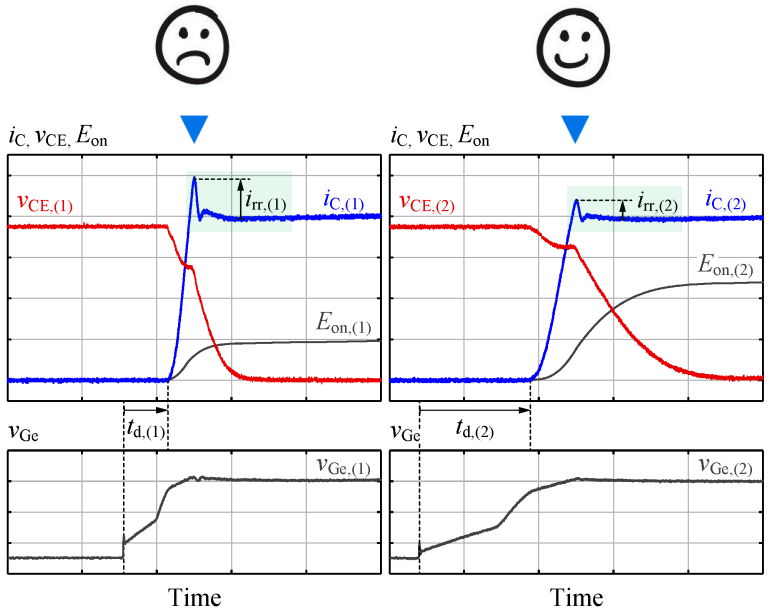
Turn-On – Diode Peak Reverse Recovery Current i_{rr}

▶ Turn-on: freewheeling diode commutation

- di_C/dt affects diode peak reverse recovery current i_{rr}
- di_D/dt affects diode switching overvoltage
- SOA operation must be guaranteed

$$i_{rr} \approx \sqrt{Q_{rr} \frac{di_C}{dt}}$$

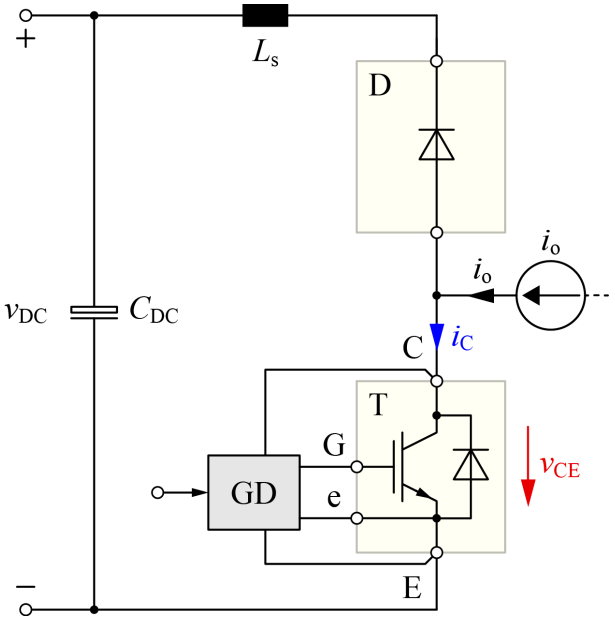


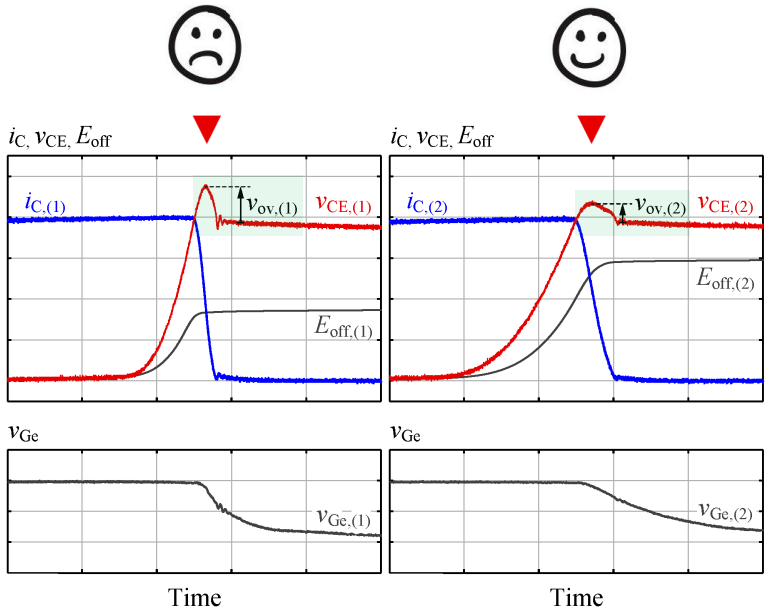


Turn-Off – Overvoltage v_{ov}

- **Turn-off: transistor switching overvoltage due to stray inductance L_s**
  - di_C/dt affects transient overvoltage v_{ov}
  - SOA operation must be guaranteed

$$v_{ov} = -L_s \frac{di_C}{dt}$$

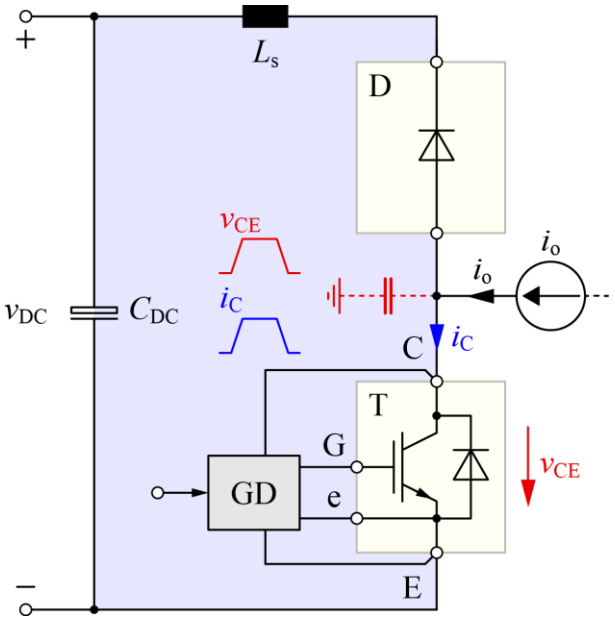


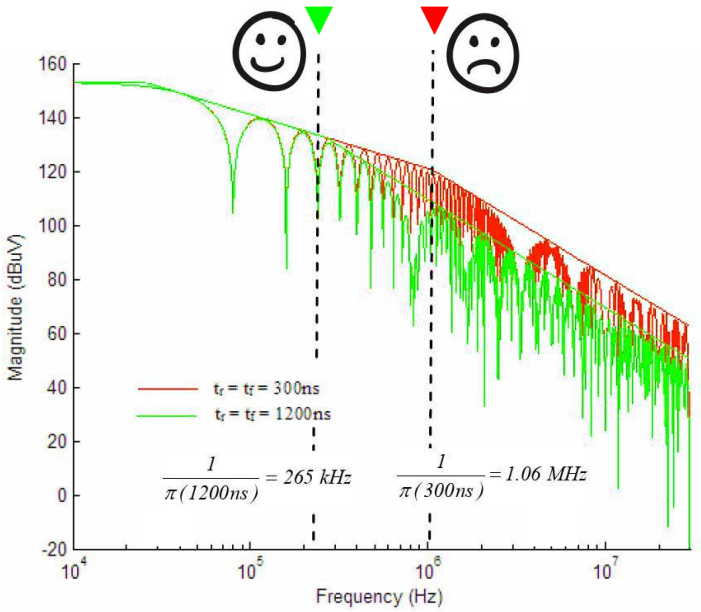


Electromagnetic Compatibility (EMC)

- **Restriction of di/dt and dv/dt**
  - Limits HF emissions / filtering effort
  - Increases switching losses

- **Conducted CM EMI dependent on dv_{CE}/dt**
- **Radiated EMI dependent on di_C/dt**
  - Direct impact on 2nd corner frequency





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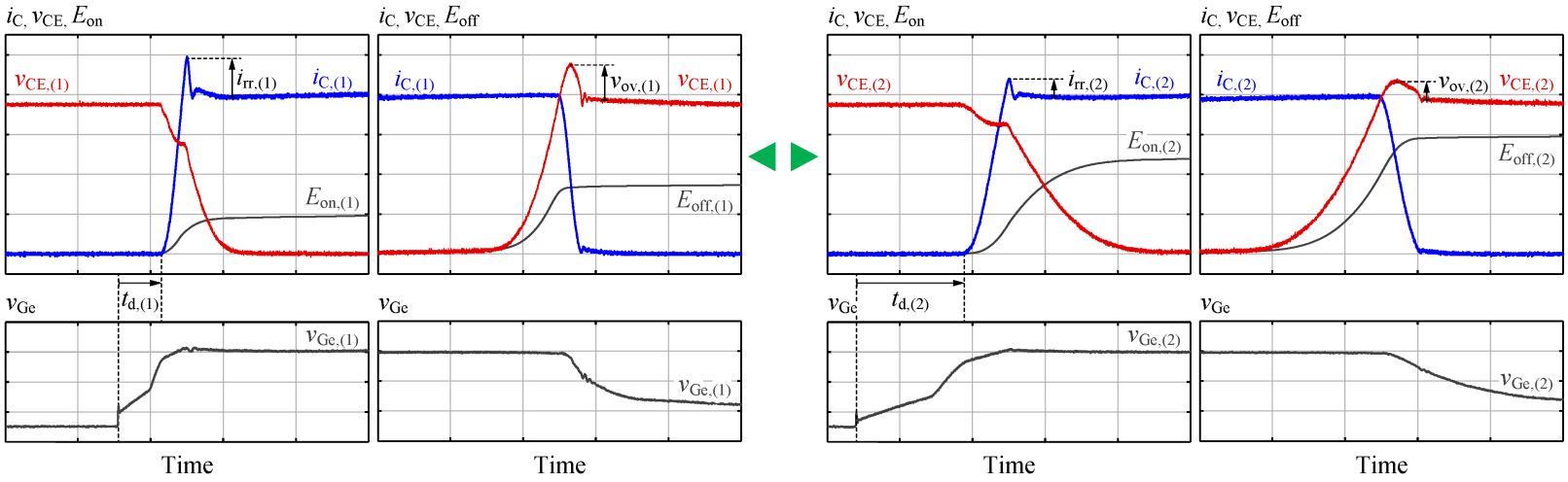
Switching Trajectory Trade-Off / Summary

▶ Fast switching (small gate resistor)

- Low switching delay times t_d
- Low switching losses $E_{on/off}$

▶ Slow switching (large gate resistor)

- Low peak reverse recovery current i_{rr}
- Low turn-off overvoltage v_{ov}
- Low EMI



▶ Optimal switching trajectories

- Independent control of di/dt and dv/dt individually for turn-on and turn-off !

Challenges of Switching Trajectory Shaping

- Non-Linearities
- Temperature Dependencies
- Operating Point Dependencies
- Intrinsic Effects

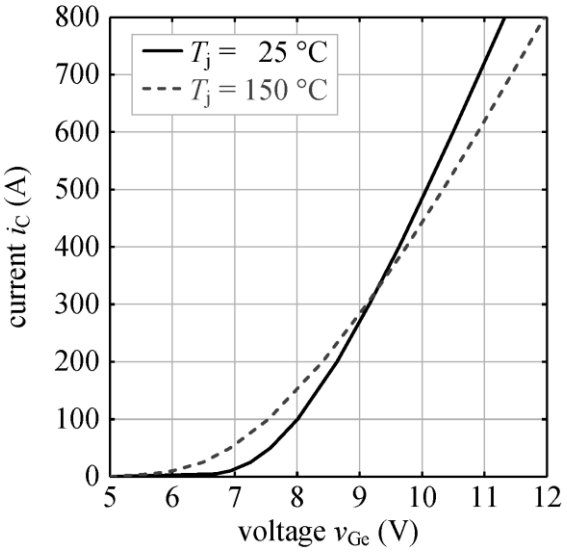
Challenges of IGBT Switching Trajectory Shaping (1)

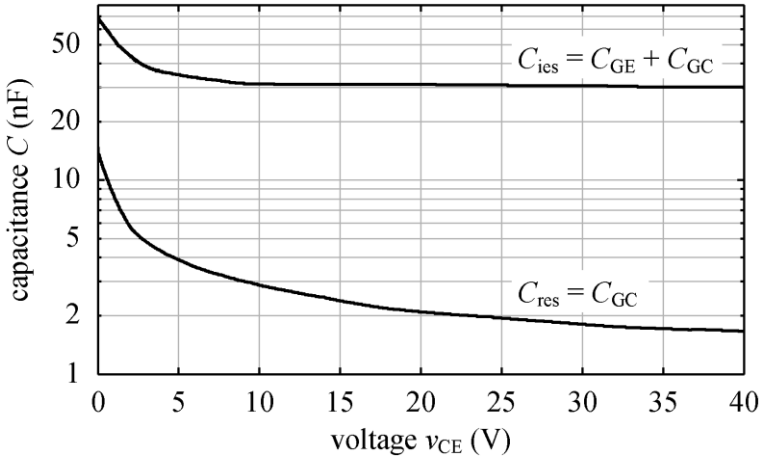
▶ Basic IGBT behavior

- Non-Linearities
- Temperature Dependencies
- Operating Point Dependencies

▶ Current / voltage time derivatives:

- $\frac{\mathrm{d}i_C}{\mathrm{d}t} = \frac{i_G}{C_{GE}}\left(g_m + v_{Ge}\frac{\mathrm{d}g_m}{\mathrm{d}v_{Ge}}\right)$
- $\frac{\mathrm{d}v_{CE}}{\mathrm{d}t} = -\frac{i_G}{C_{GC}}$



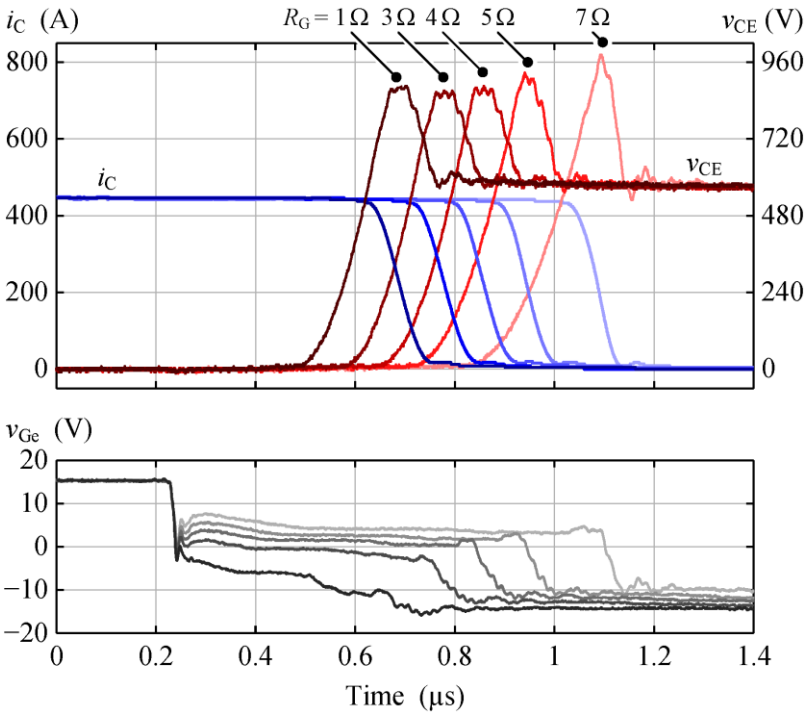


Challenges of IGBT Switching Trajectory Shaping (2)

► Intrinsic IGBT effects

- **Turn-off with slightly larger gate resistor**
  - Lower dv_{CE}/dt
  - Longer lasting voltage slope
  - More stored charge is extracted
  - Desaturation of the device
  - **Faster current slope (higher overvoltage) for Trench-Fieldstop IGBTs !**

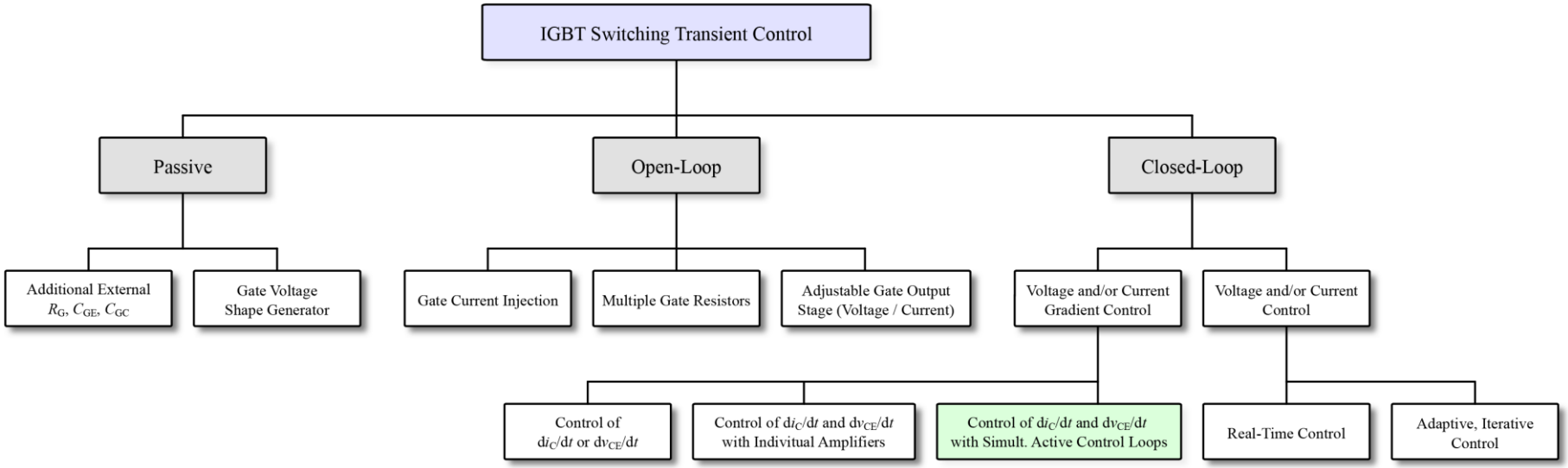
- **Lowest delay times / switching losses / EMI and SOA operation at all operating points only for Active Gate Drive !**



State-of-the-Art IGBT Trajectory Control

- Passive Gate Drive
- Open-Loop Gate Drive
- Closed-Loop Gate Drive

Classification of Gate Drive Circuits



► **Proposed Gate Drive**

Passive Gate Drive

▶ Adjustments

- External gate resistor R_G
- Added Miller capacitance C_{GC}
- Added gate capacitance C_{Ge}

▶ Advantages

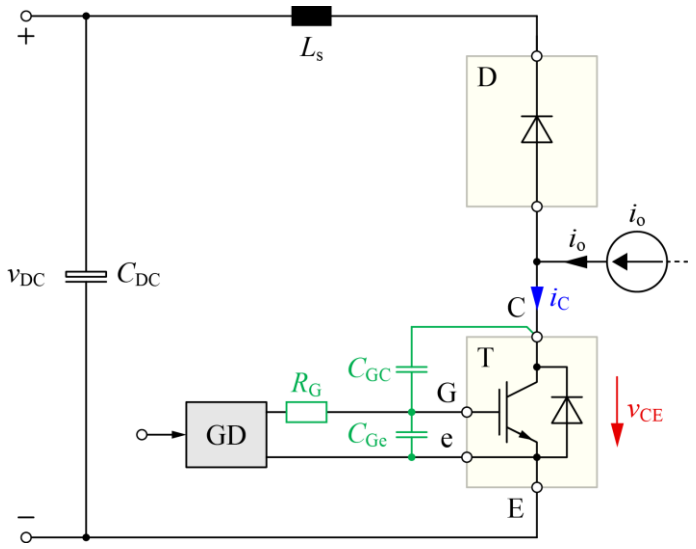
- Low complexity
- Inexpensive

▶ Disadvantages

- No compensation of parameter variations
- Higher switching losses
- Large driving losses

▶ Current / voltage time derivatives:

- $\frac{\mathrm{d}i_C}{\mathrm{d}t} = \frac{i_G}{C_{GE,tot}}\left(g_m + v_{Ge}\frac{\mathrm{d}g_m}{\mathrm{d}v_{Ge}}\right)$
- $\frac{\mathrm{d}v_{CE}}{\mathrm{d}t} = -\frac{i_G}{C_{GC,tot}}$



Open-Loop Gate Drive

- Switchable multiple gate resistors
- Gate voltage / current profile
- Gate current injection

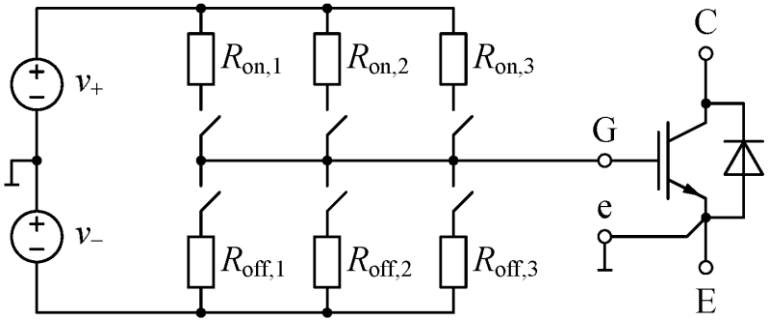
  – Fixed profile
  – Event feedback
  – Operating point feedback

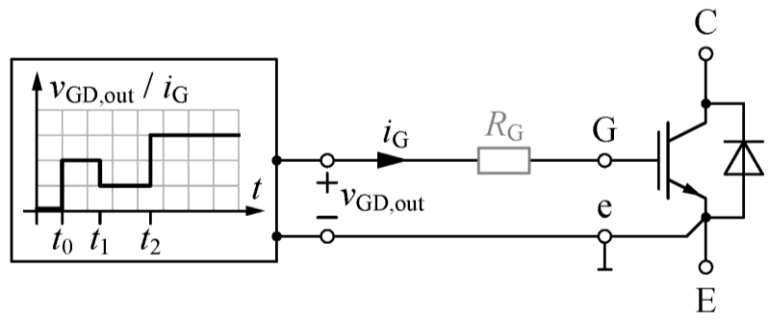
- Advantages

  – Low complexity

- Disadvantages

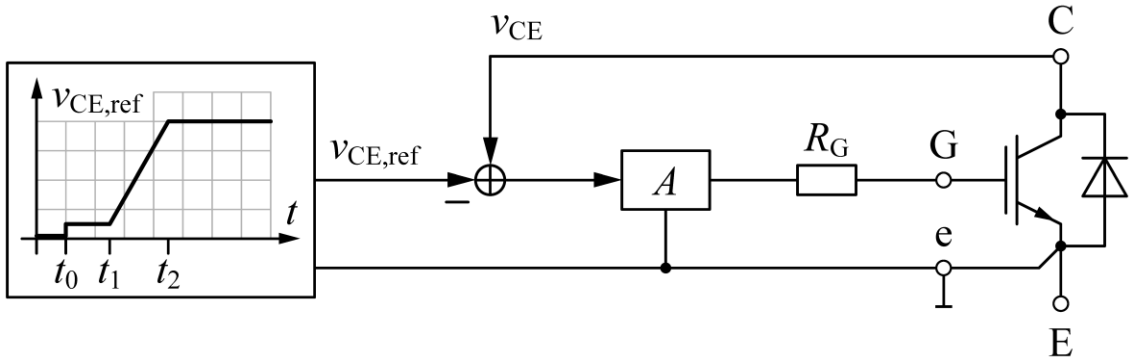
  – No compensation of non-linearities
  – Compromise in order to never exceed max. di_C/dt or dv_{CE}/dt for varied T_j, i_o, v_{DC}





Closed-Loop Gate Drive – Analog

- v_{CE} and/or i_C reference profile
- Feedback(s) to analog control loop
  - v_{CE} measurement by voltage divider
  - i_C measurement by current sensor



- Advantages
  - Direct control of v_{CE} (and i_C)
  - Compensation of non-linearities

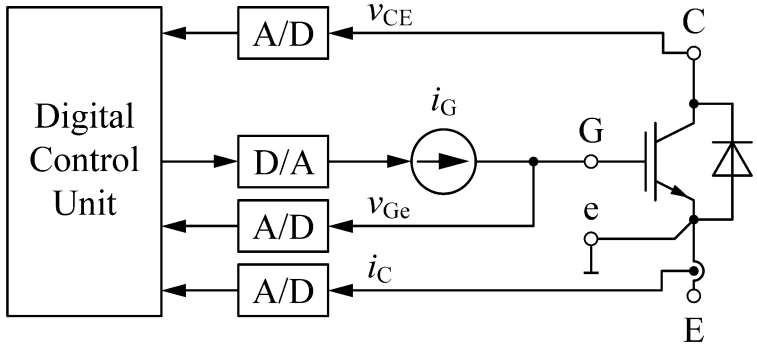
- Disadvantages
  - Bandwidth limit / losses of current sensors
  - Complex generation of reference signal if v_{CE} and i_C control are required

Closed-Loop Gate Drive – Digital

- Measurement and A/D-conversion of v_{CE}, i_C, v_{Ge}
- i_C and v_{CE} control via gate current
- Digital control unit (FPGA)

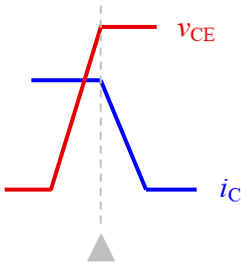
- Advantages
  - High flexibility due to digital control unit, e.g. reference profiles or transition from i_C to v_{CE} control
  - Compensation of non-linearities

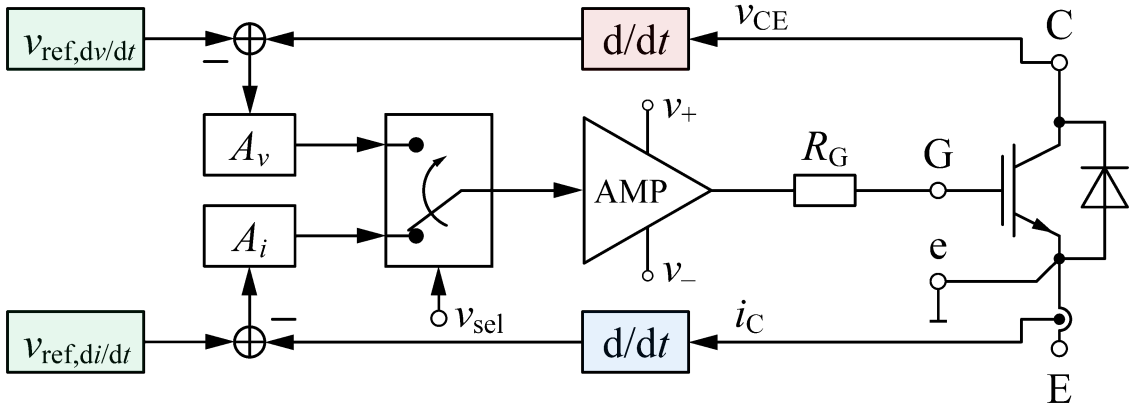
- Disadvantages
  - Large delays of A/D and D/A conversions
  - Expensive
  - Real-time control not feasible for switching times faster than 2 µs
  - Alternative: adaptive / learning control



Closed-Loop Gate Drive – Voltage/Current Slopes

- dv_{CE}/dt control and/or di_C/dt control





- Advantages
  - Constant reference values
  - Passive measurement circuits
  - Compensation of non-linearities and parameter variations

- Disadvantages
  - Active switchover between the two control loops
  - Transition point for switchover from di_C/dt control to dv_{CE}/dt control must be detected accurately

Proposed Closed-Loop Gate Drive

- **Basic Idea / Principle of Operation**
- Experimental Results
- Stability Analysis

Clamped Inductive Load Switching - Review

Assumption

- Load current i_o = const. in the switching interval for inductive load switching

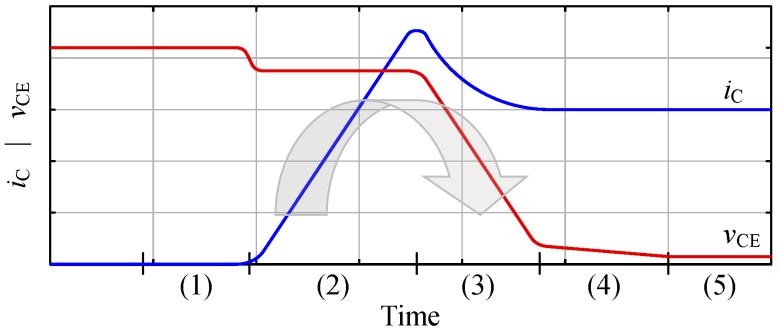
Observation

- dv_{CE}/dt = 0 during current slope
- di_C/dt = 0 during voltage slope

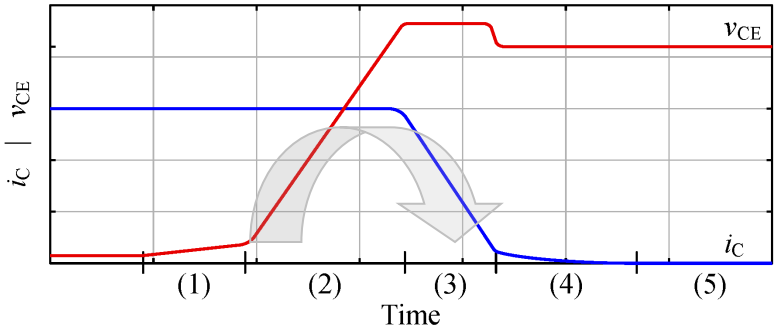
Basic idea

- For di_C/dt control and dv_{CE}/dt control both feedback loops can be active simultaneously
- No need for active switchover between the two control loops

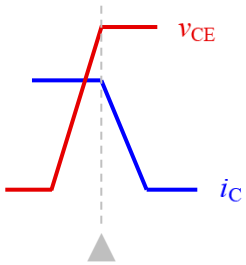
Turn-on

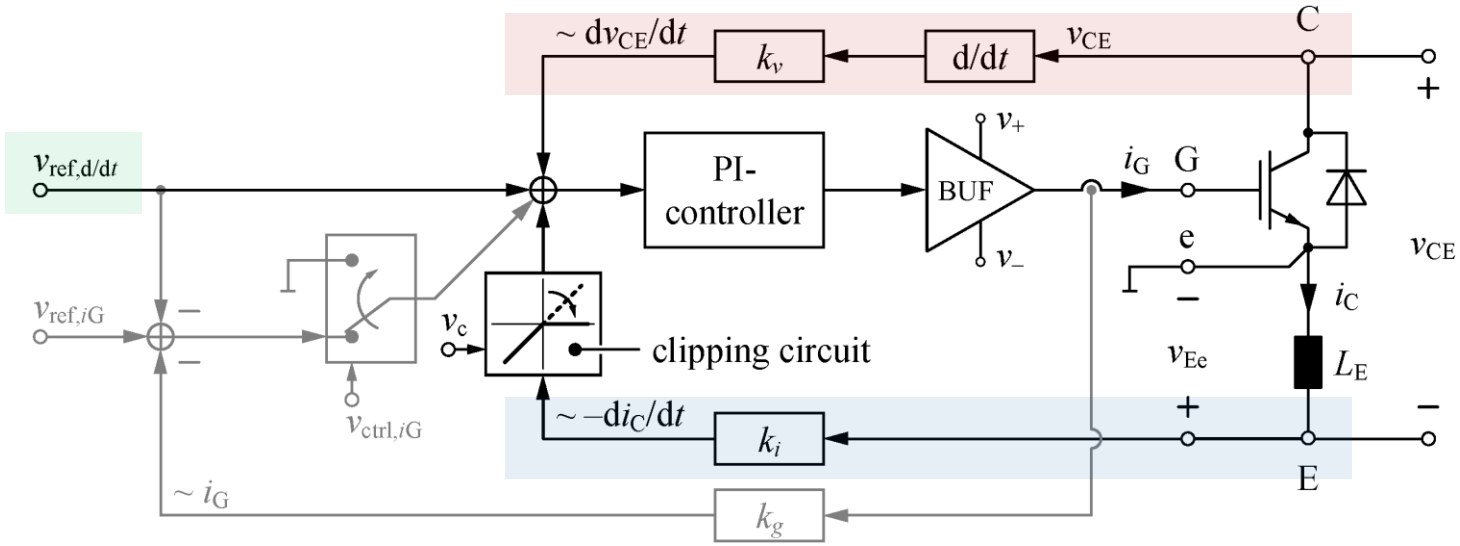


Turn-off



Block Diagram





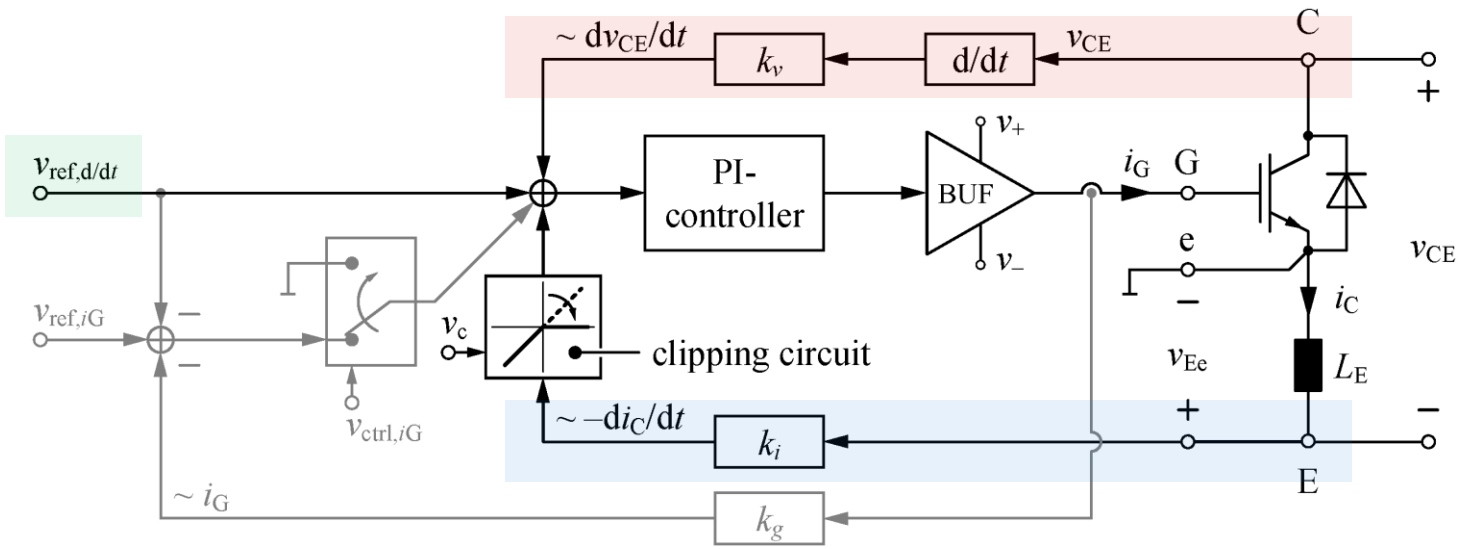
▶ Main control loop

- Combined di_C/dt and dv_{CE}/dt feedbacks
- Individual feedback gains (k_i, k_v)
- Common control reference signal $v_{ref,d/dt}$

▶ Additional control loop

- Gate current control during turn-on/off delay
- Minimizes turn-on/off delay times
- If activated, d/dt-control reference is set to zero

Control Reference / Set-Points



▶ Current slope

$$\left(\frac{di_C}{dt}\right)_{ref} = \frac{v_{ref,d/dt}}{k_i \cdot L_E}$$

▶ Voltage slope

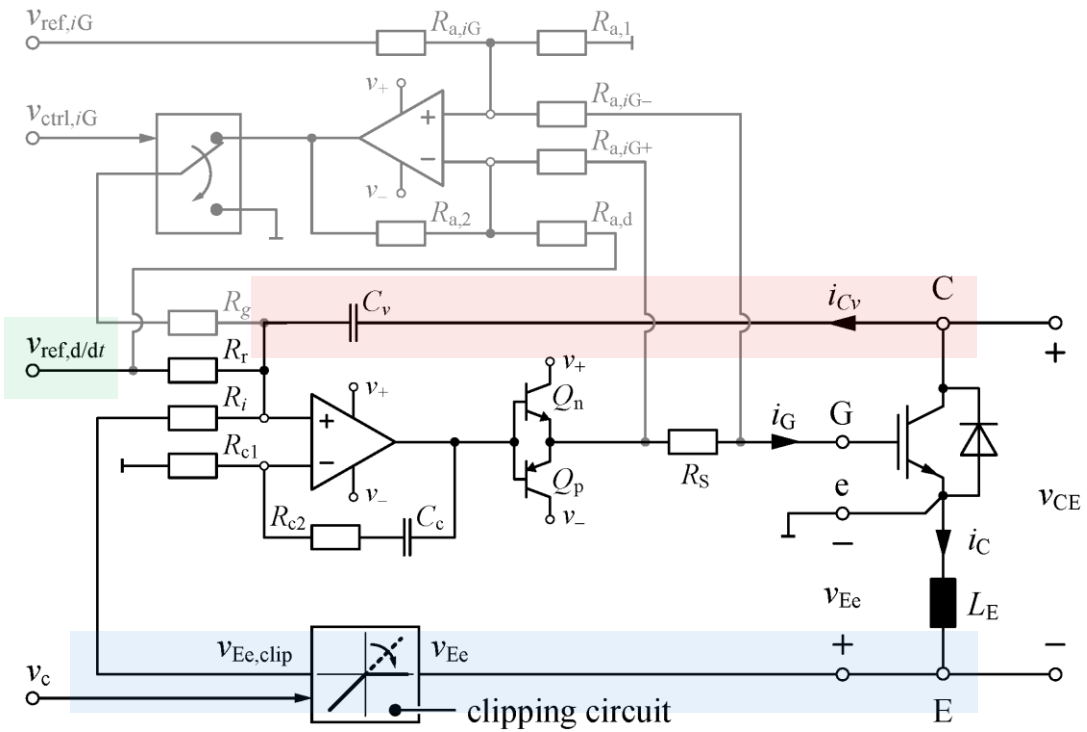
$$\left(\frac{dv_{CE}}{dt}\right)_{ref} = -\frac{v_{ref,d/dt}}{k_v}$$

▶ Reference signal $v_{ref,d/dt}$

- Turn-on: positive (+di_C/dt, -dv_{CE}/dt)
- Turn-off: negative (+dv_{CE}/dt, -di_C/dt)

Circuit Diagram

- **Passive measurements**
  - dv_{CE}/dt: C_v in voltage path (CR high-pass filter)
  - di_C/dt: L_E in current path (bond wire inductance)
  - i_G: R_s in gate path (shunt)
- **Error signal**
  - Passive resistor network
- **Control amplifier**
  - Single fast op-amp wired as a PI-controller



di/dt Clipping Circuit

Exception / Issue

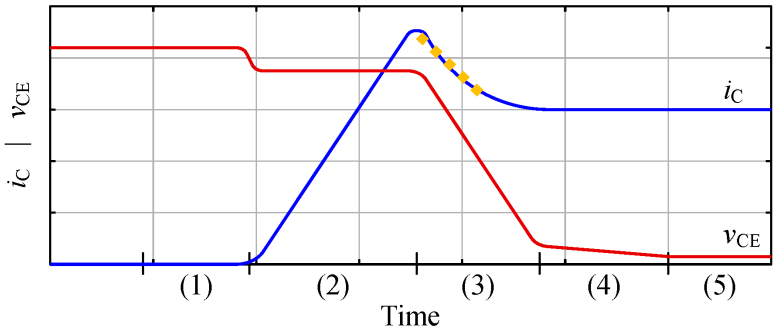
- di/dt is not zero at turn-on after diode reverse recovery current peak
- Influence on dv/dt control

Solution: clipping circuit

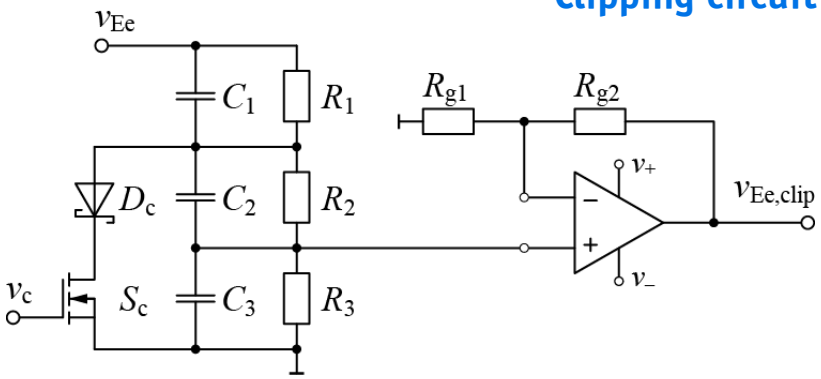
- S_c closed during turn-on transients
- S_c open at turn-off

- Neg. di/dt values (pos. voltages of v_{Ee}) at turn-on are limited to volt. prop. to v_{Dc}
- Pos. di/dt values are not affected

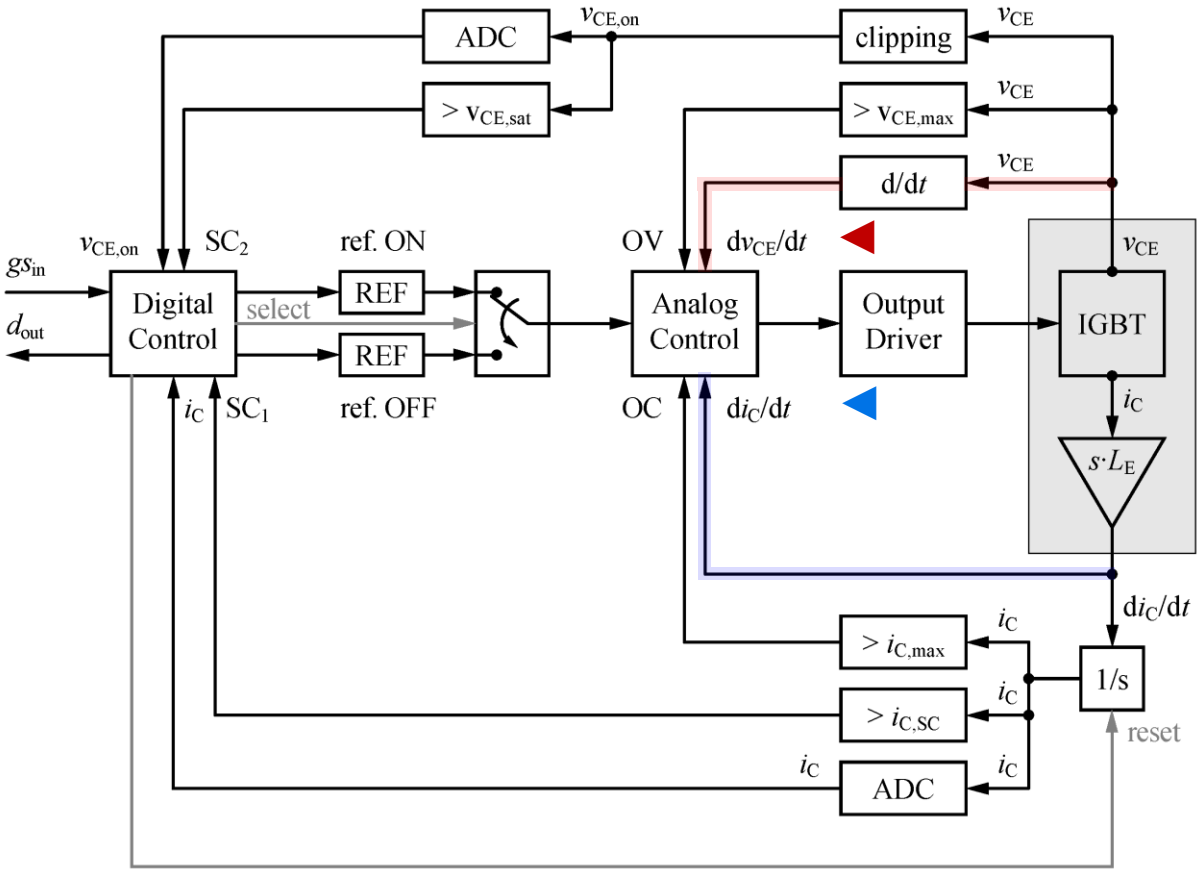
Turn-on



Clipping circuit



Closed-Loop Gate Drive – Block Diagram

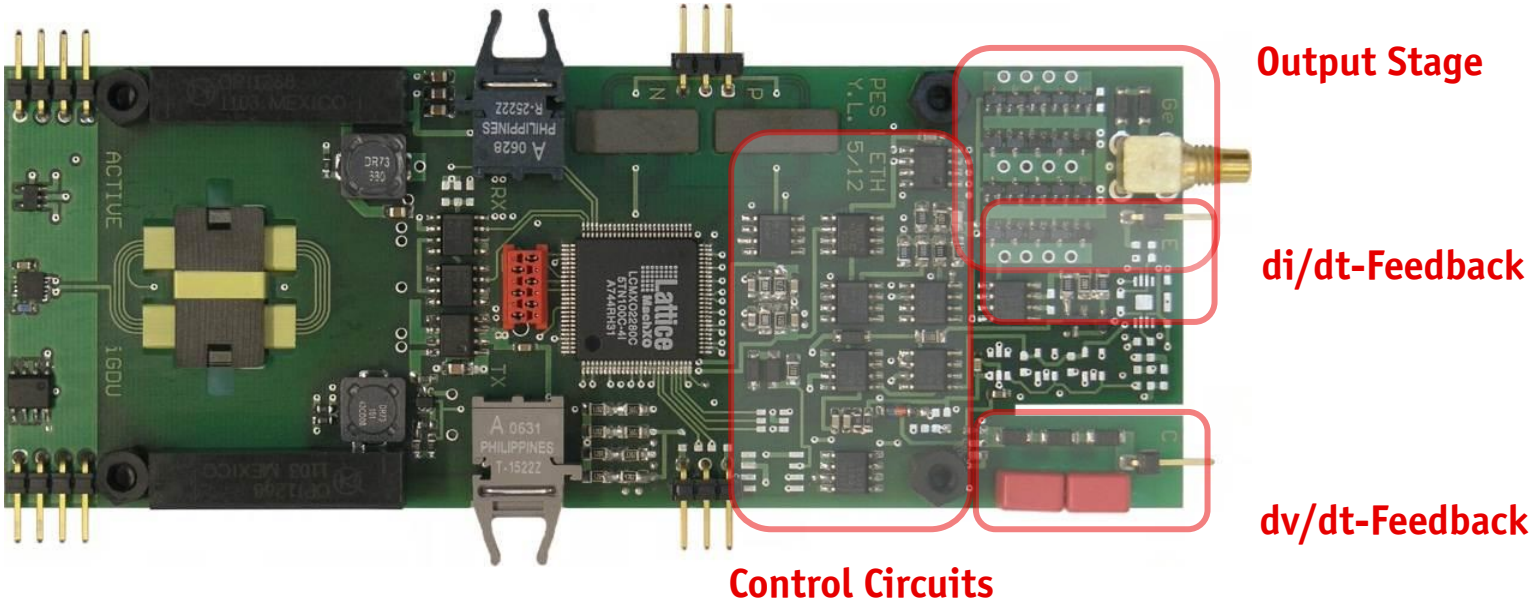


Proposed Closed-Loop Gate Drive

- Basic Idea / Principle of Operation
- **Experimental Results**
- Stability Analysis

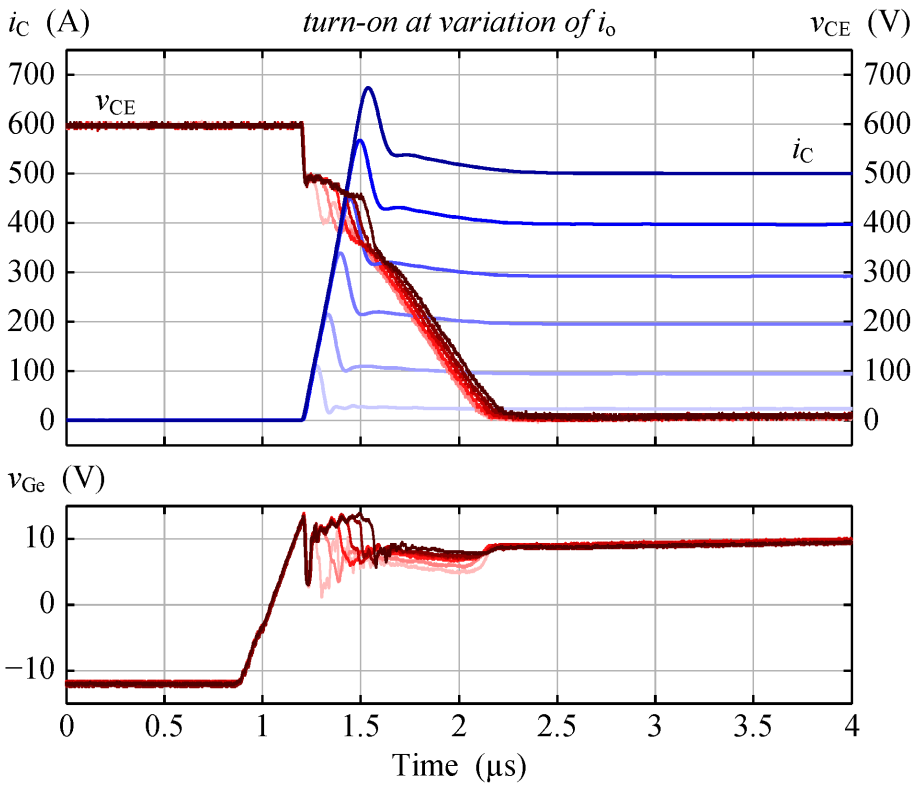
Closed-Loop Gate Drive - Hardware

- **PCB Dimensions: 5 cm x 13 cm**



Experimental Results – Turn-On Transients

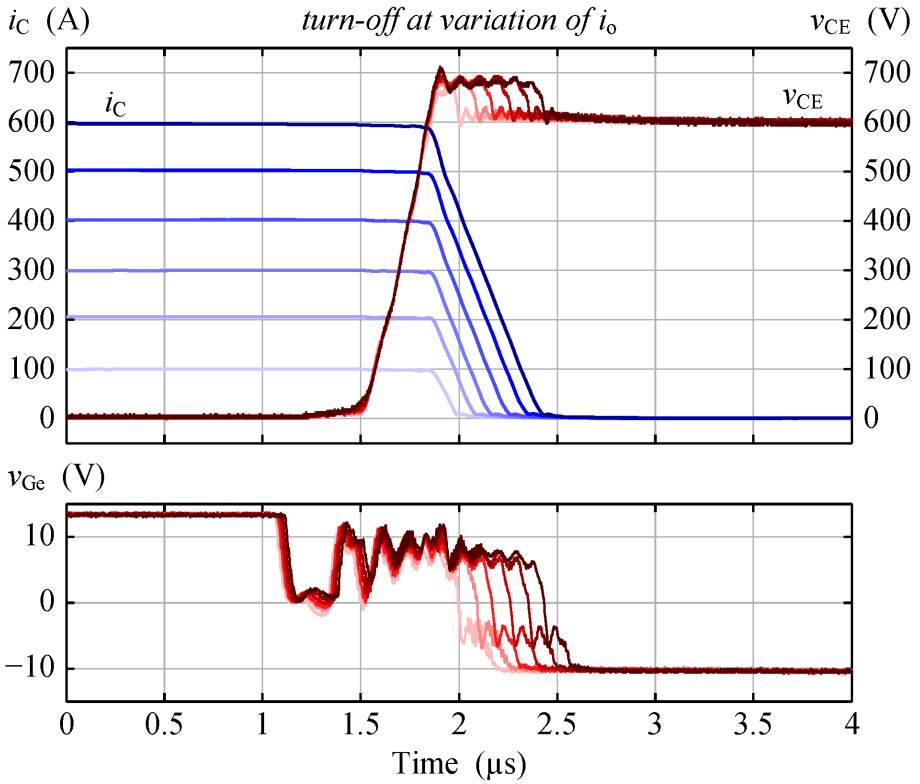
- **Variation of load current**
  - di/dt = 2 kA/µs
  - dv/dt = -0.5 kV/µs
- **Outcome**
  - **Independent control of current and voltage slope!**
  - Natural transition from di/dt to dv/dt control
  - Low overshoot in dv/dt after transition
  - No load current dependency at i_C and v_{CE}, but on v_{Ge} (higher v_{Ge} at higher current)



Experimental Results – Turn-Off Transients

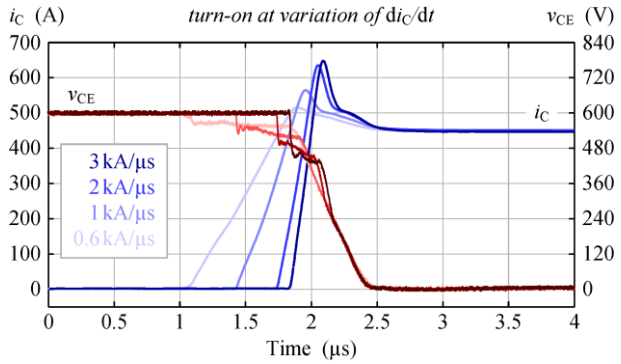
- **Variation of load current**
  - di/dt = -1 kA/µs
  - dv/dt = 2 kV/µs

- **Outcome**
  - **Independent control of current and voltage slope!**
  - Natural transition from dv/dt to di/dt control
  - Low overshoot in di/dt after transition
  - No load current dependency at i_C and v_{CE}, but on v_{Ge} (higher v_{Ge} at higher current)

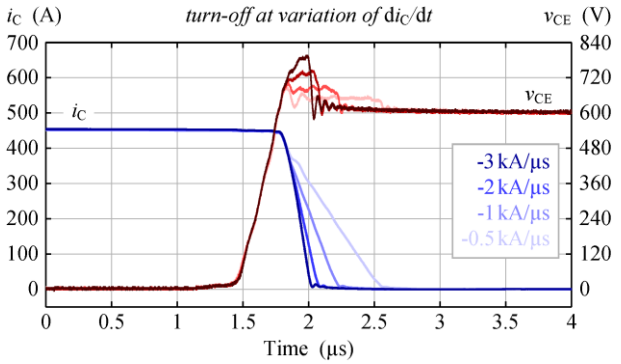


Experimental Results – Individual Variation of References

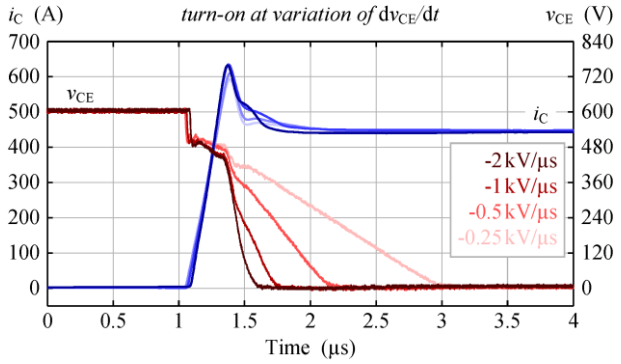
▶ Turn-On: Variation of di/dt



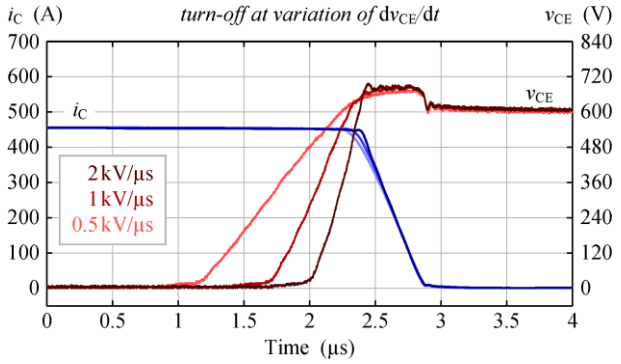
▶ Turn-Off: Variation of di/dt



▶ Turn-On: Variation of dv/dt

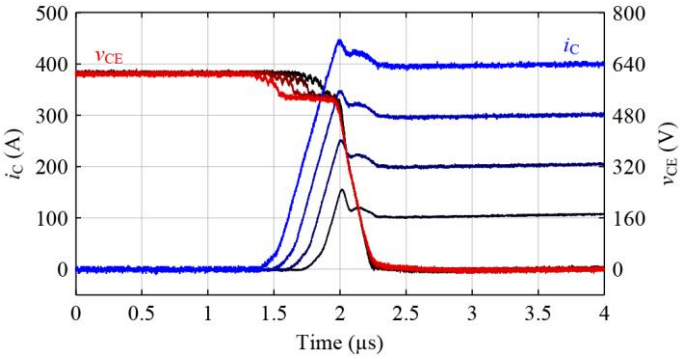


▶ Turn-Off: Variation of dv/dt

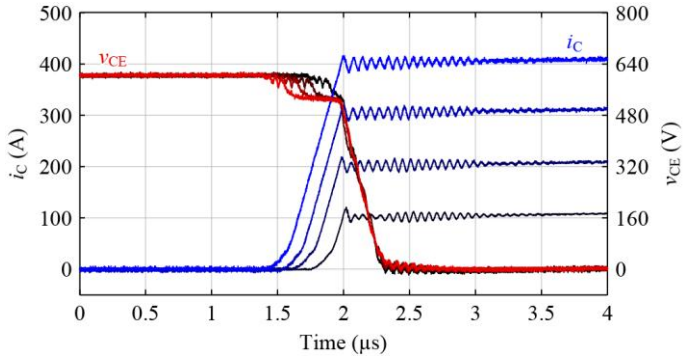


Experimental Results – Si vs. SiC Diode @ Turn-On

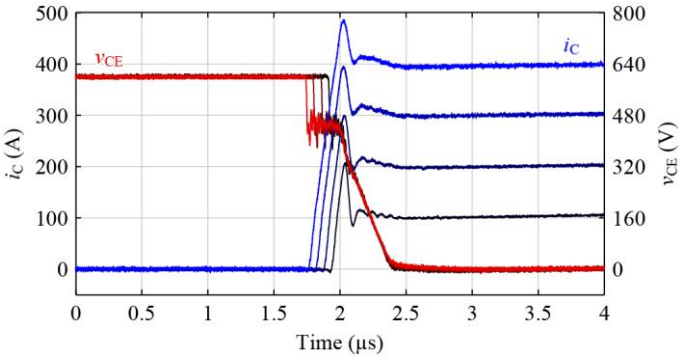
- Si: 1 kA/µs, -2 kV/µs



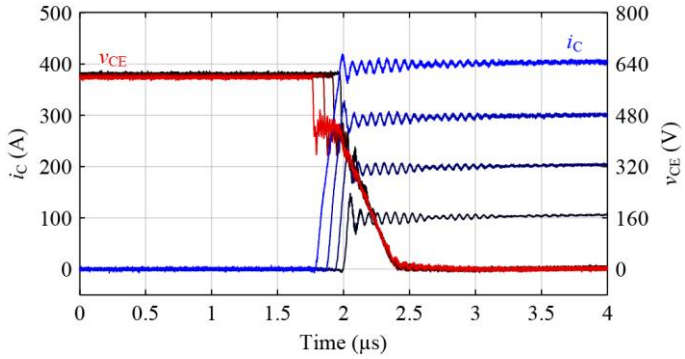
- SiC: 1 kA/µs, -2 kV/µs



- Si: 2 kA/µs, -1 kV/µs

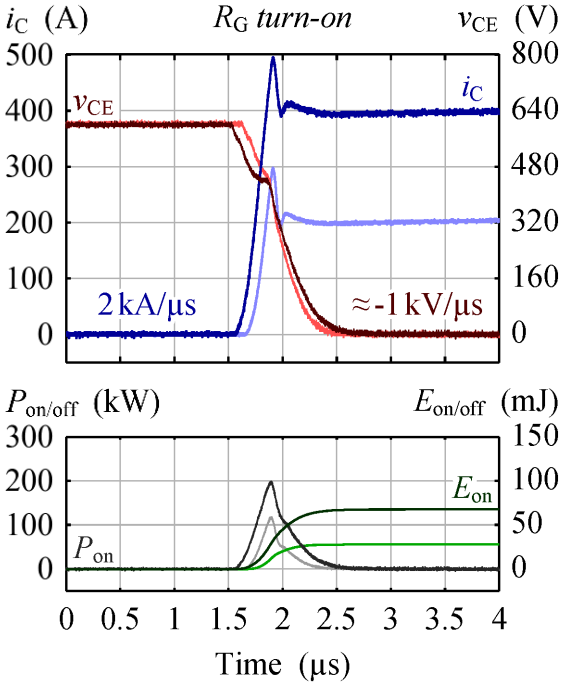


- SiC: 2 kA/µs, -1 kV/µs

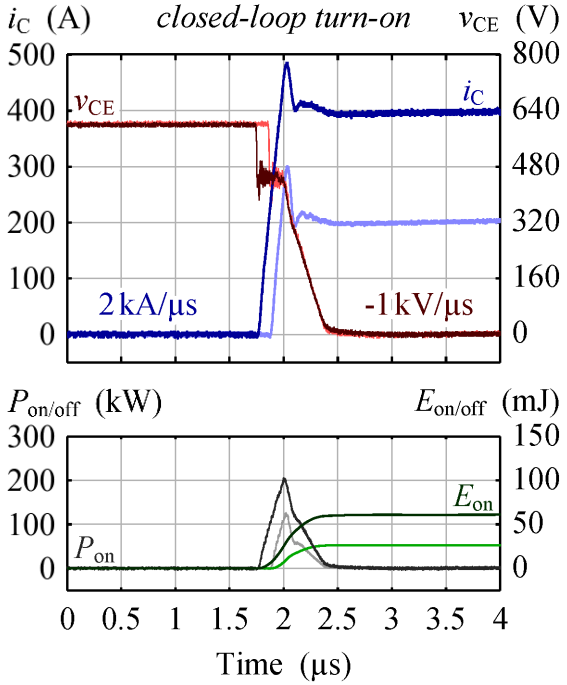


Experimental Results – R_G vs. Closed-Loop @ Turn-On (1)

- R_G: 2 kA/µs @ 400A



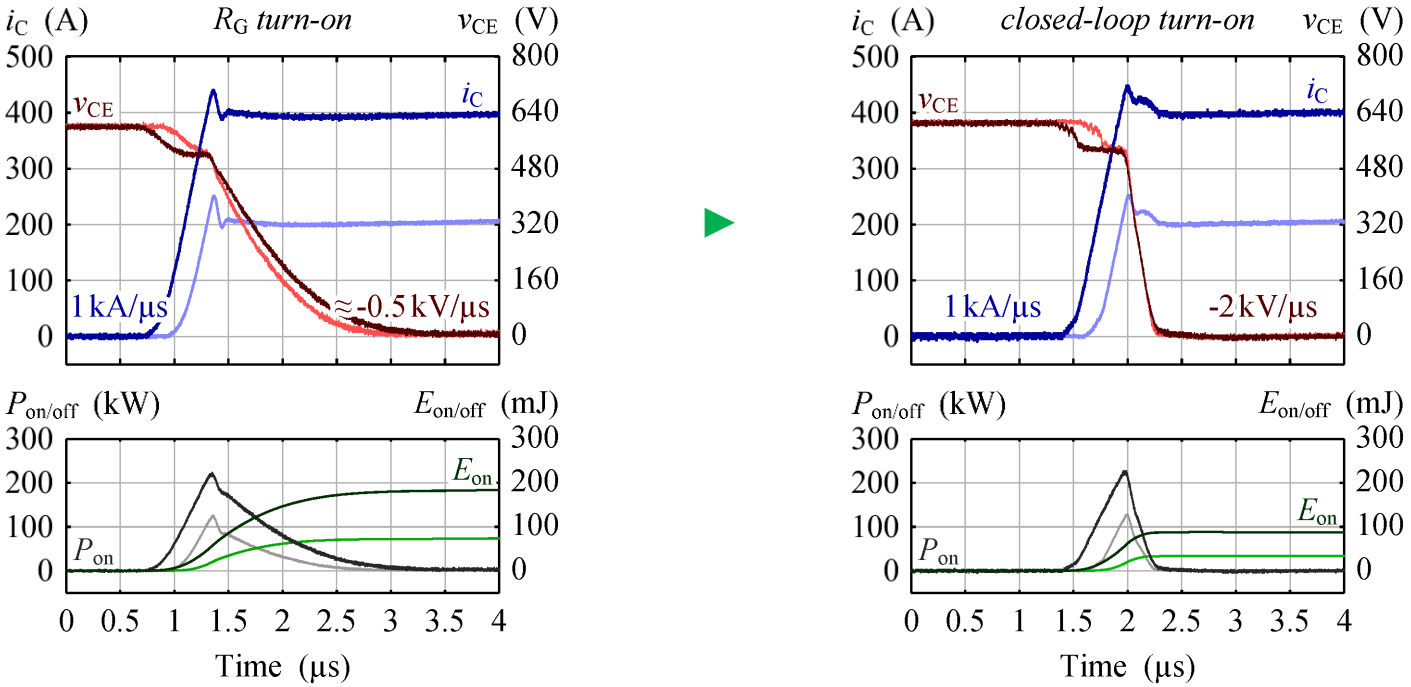
- Closed-Loop: 2 kA/µs, -1 kV/µs



- No influence on dv/dt with R_G (selected to achieve 2 kA/µs @ 400A)
- Similar switching losses since di/dt and dv/dt are similar in both cases

Experimental Results – R_G vs. Closed-Loop @ Turn-On (2)

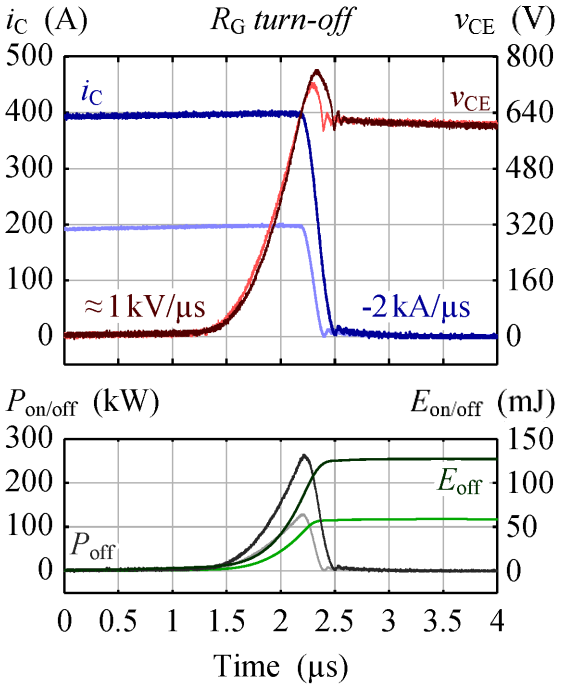
- R_G: 1 kA/µs @ 400A
- Closed-Loop: 1 kA/µs, -2 kV/µs



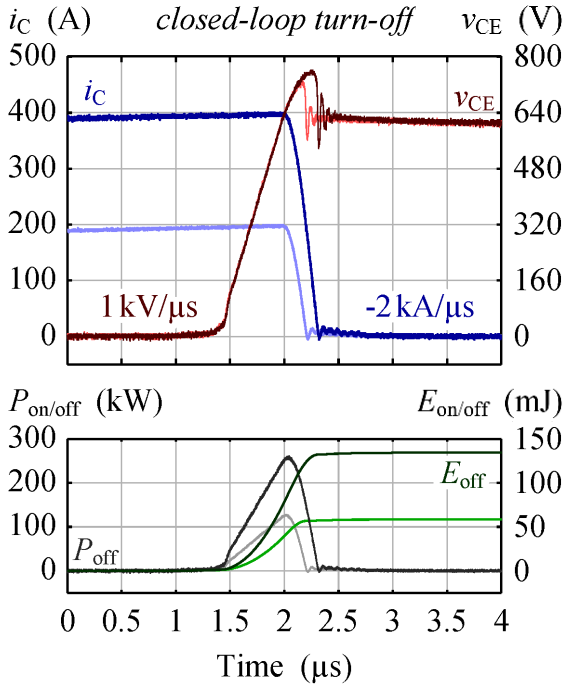
- No influence on dv/dt with R_G (selected to achieve 1 kA/µs @ 400A)
- ≈ 50 % of switching losses with closed-loop control compared to R_G !

Experimental Results – R_G vs. Closed-Loop @ Turn-Off (1)

- R_G: -2 kA/µs @ 400A



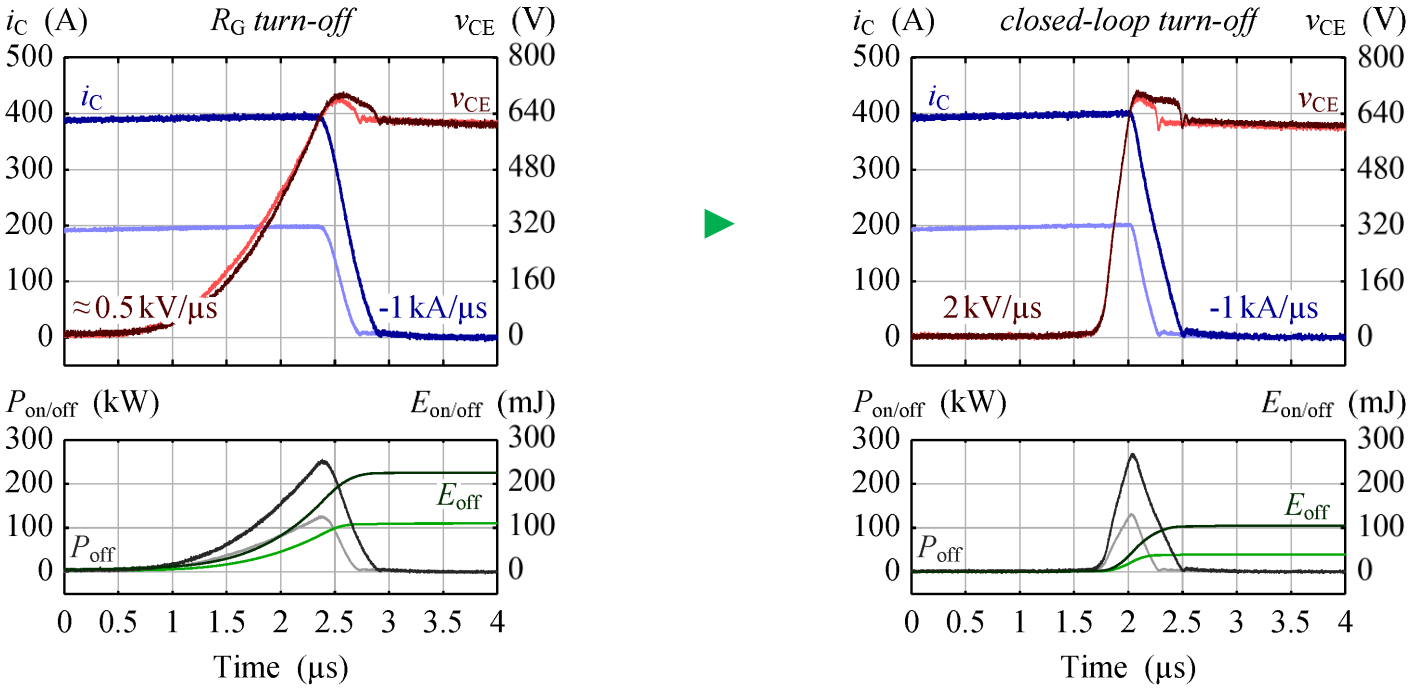
- Closed-Loop: 1 kV/µs, -2 kV/µs



- No influence on dv/dt with R_G (selected to achieve -2 kA/µs @ 400A)
- Similar switching losses since di/dt and dv/dt are similar in both cases

Experimental Results – R_G vs. Closed-Loop @ Turn-Off (2)

- R_G: -1 kA/µs @ 400A
- Closed-Loop: 2 kV/µs, -1 kA/µs



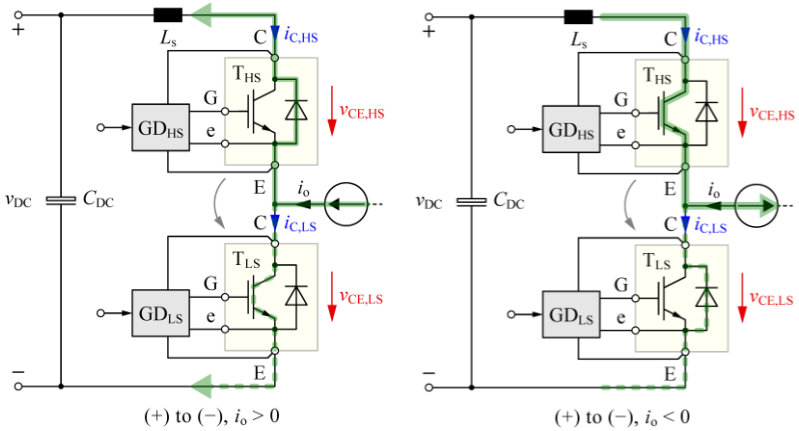
- No influence on dv/dt with R_G (selected to achieve -1 kA/µs @ 400A)
- ≈ 50 % of switching losses with closed-loop control compared to R_G !

Considerations for Bridge Leg Configurations

▶ Main goals

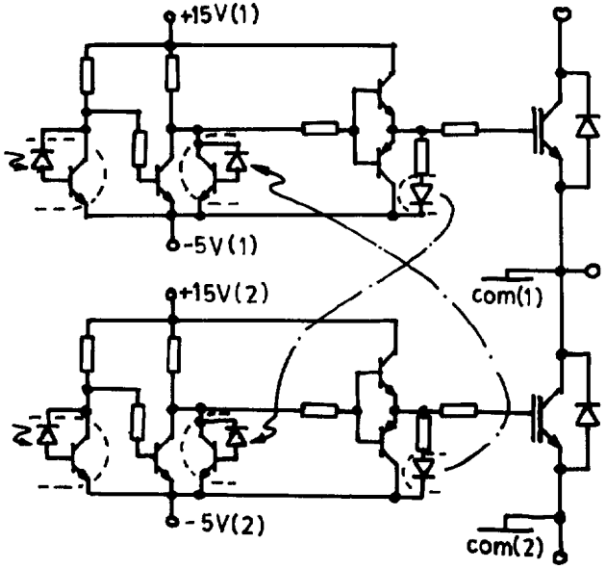
- Minimal interlock delay time
- No distortion of the output voltage (volt-seconds according to gate signal)

- Transition depends on load current direction
  - Need for additional supperordinate control



▶ Solution for conventional gate drives

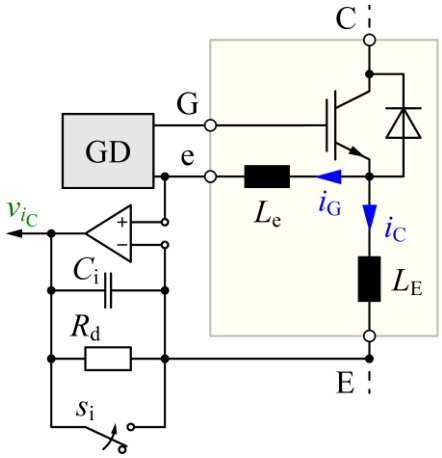
- Modifications of closed-loop di/dt and dv/dt gate drive are needed: [46]



Short Circuit – Types and Detection

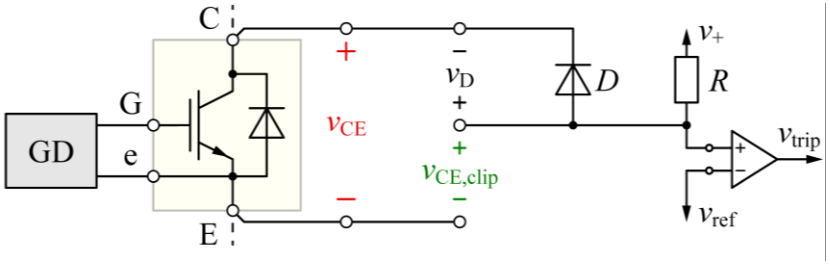
▶ Hard Switching Failure

- IGBT turns-on to an already existing short circuit at the load terminals
- Detection by means of current i_C measurement (active integration of voltage across bond wire inductance or Rogowski coil voltage)
  - $i_C > i_{C,max}$



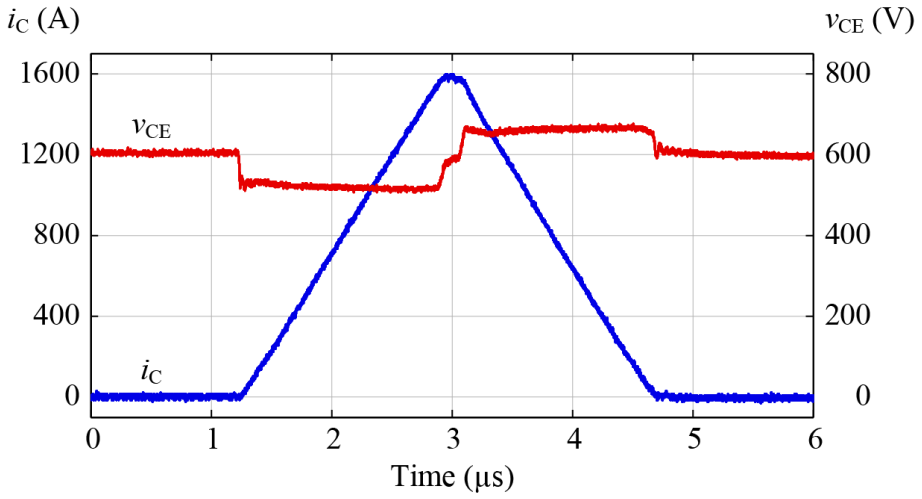
▶ Failure Under Load

- IGBT is conducting current when the short circuit occurs at the load terminals
- Detection by means of desaturation detection ($v_{CE} > v_{CE,max}$) with voltage limiting circuit
  - On-state: $v_{CE,clip} = V_{CE} + V_D$
  - Off-state: $v_{CE,clip} = v_+$



Experimental Results – Hard Switching Failure

- **Turn-on into short circuit of opposite IGBT module ($v_{GE,opp}$ = 15 V)**
  - Turn-on current slope actively controlled to di/dt = 1 kA/µs
  - Short circuit detected and turned-off with di/dt = -1 kA/µs
  - Defined turn-off di/dt
  - Constant turn-off overvoltage
  - SOA operation ensured



Proposed Closed-Loop Gate Drive

- Basic Idea / Principle of Operation
- Experimental Results
- **Stability Analysis**

Control-Oriented Modelling: Gate Drive

▶ Transfer functions

- **Op-amp: lim. gain-bandwidth product**

$$G_{\mathrm{OP}} = \frac{A_{\mathrm{DC,OP}}}{s\frac{A_{\mathrm{DC,OP}}}{2\pi f_{\mathrm{T,OP}}}+1}$$

- ***PI*-controller**

$$G_{PI} = \frac{G_{\mathrm{OP}}(sP+I)}{s(G_{\mathrm{OP}}+P)+I}$$

- **Output amplifier**

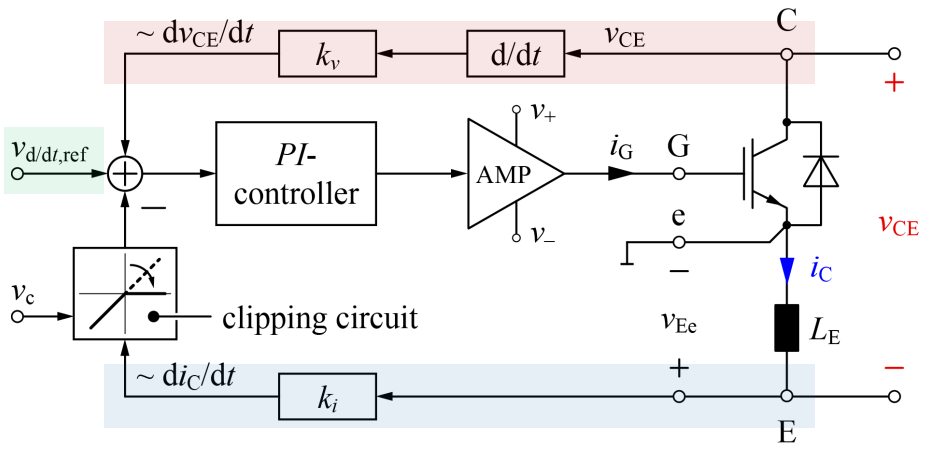
$$G_{\mathrm{AMP}} = \frac{1}{s\frac{1}{2\pi f_{\mathrm{c,AMP}}}+1}$$

- **$\mathrm{dv_{CE}/dt}$ measurement**

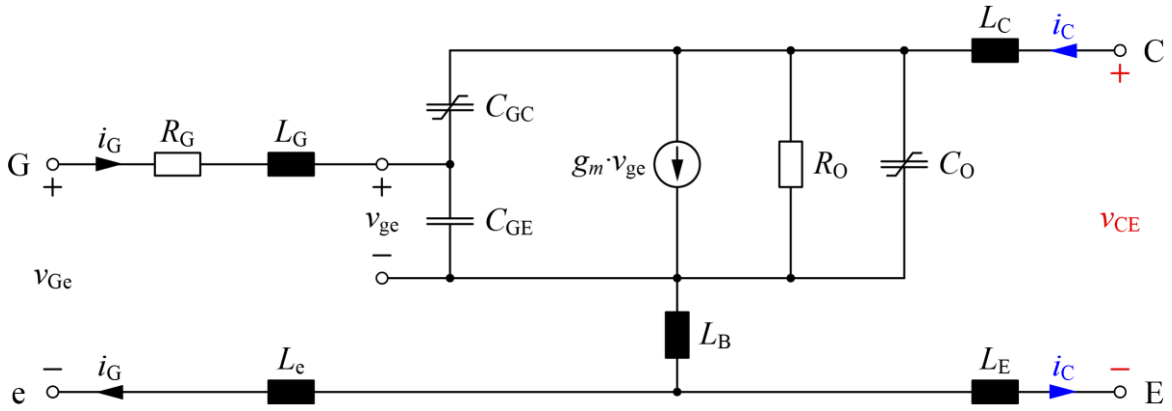
$$H_{V,\mathrm{HP}} = \tau_V \frac{s}{s\tau_V+1}$$

- **$\mathrm{di_C/dt}$ measurement**

$$H_{I,\mathrm{HP}} = \tau_I s$$



Control-Oriented Modeling: IGBT (small-signal)



▶ Key features

- Considering parasitic inductances of the bond wires and the electrical terminals
- Valid in the active region
  - i_C: voltage controlled current source
  - v_{CE}: feedback via Miller-capacitance

▶ General limits

- Valid at selected (i.e. worst case) operating point
- Not considering dynamic device behavior (e.g. dependency on stored charge)

▶ Needed transfer functions

- v_{Ge} (input) to v_{CE} (output)
- v_{Ge} (input) to i_C (output)

IGBT (small-signal) Transfer Functions

▶ Voltage slope TF (assuming $di_C/dt = 0$)

$$G_V = \frac{V_{\mathrm{CE}}}{V_{\mathrm{Ge}}} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$\begin{aligned}
a_0 &= -g_m R_{\mathrm{O}} \\
a_1 &= R_{\mathrm{O}} C_{\mathrm{GC}} \\
a_2 &= L_{\mathrm{B}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
a_3 &= L_{\mathrm{B}} R_{\mathrm{O}} C_{\mathrm{t}} \\
b_0 &= 1 \\
b_1 &= R_{\mathrm{O}}(C_{\mathrm{GC}} + C_{\mathrm{O}}) + R_{\mathrm{G}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
b_2 &= R_{\mathrm{O}} R_{\mathrm{G}} C_{\mathrm{t}} + (L_{\mathrm{Ge}} + L_{\mathrm{B}})(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
b_3 &= R_{\mathrm{O}} C_{\mathrm{t}}(L_{\mathrm{Ge}} + L_{\mathrm{B}}) \\
C_{\mathrm{t}} &= C_{\mathrm{GE}} C_{\mathrm{GC}} + C_{\mathrm{GE}} C_{\mathrm{O}} + C_{\mathrm{GC}} C_{\mathrm{O}},
\end{aligned}$$

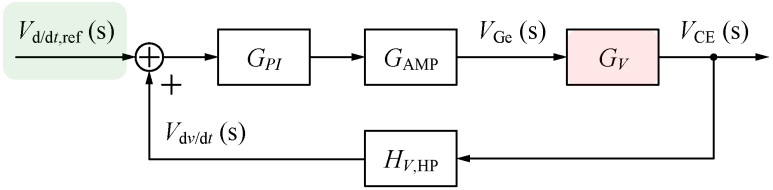
▶ Current slope TF (assuming $dv_{CE}/dt = 0$)

$$G_I = \frac{I_{\mathrm{C}}}{V_{\mathrm{Ge}}} = \frac{c_3 s^3 + c_2 s^2 + c_1 s + c_0}{d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0}$$

$$\begin{aligned}
c_0 &= g_m R_{\mathrm{O}} \\
c_1 &= -R_{\mathrm{O}} C_{\mathrm{GC}} \\
c_2 &= -L_{\mathrm{B}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
c_3 &= -L_{\mathrm{B}} R_{\mathrm{O}} C_{\mathrm{t}} \\
d_0 &= R_{\mathrm{O}} \\
d_1 &= L_{\mathrm{CE}} + L_{\mathrm{B}}(1 + g_m R_{\mathrm{O}}) + R_{\mathrm{G}} R_{\mathrm{O}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}) \\
d_2 &= R_{\mathrm{G}}(L_{\mathrm{CE}} + L_{\mathrm{B}})(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
&\quad + R_{\mathrm{O}}(C_{\mathrm{GE}}(L_{\mathrm{B}} + L_{\mathrm{Ge}}) + C_{\mathrm{GC}}(L_{\mathrm{CE}} + L_{\mathrm{Ge}}) \\
&\quad + C_{\mathrm{CE}}(L_{\mathrm{CE}} + L_{\mathrm{B}})) \\
d_3 &= R_{\mathrm{G}} R_{\mathrm{O}} C_{\mathrm{t}}(L_{\mathrm{CE}} + L_{\mathrm{B}}) \\
&\quad + L_{\mathrm{t}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
d_4 &= L_{\mathrm{t}} R_{\mathrm{O}} C_{\mathrm{t}} \\
C_{\mathrm{t}} &= C_{\mathrm{GE}} C_{\mathrm{GC}} + C_{\mathrm{GE}} C_{\mathrm{O}} + C_{\mathrm{GC}} C_{\mathrm{O}} \\
L_{\mathrm{t}} &= L_{\mathrm{CE}} L_{\mathrm{Ge}} + L_{\mathrm{CE}} L_{\mathrm{B}} + L_{\mathrm{Ge}} L_{\mathrm{B}},
\end{aligned}$$

Block Diagrams and Closed-Loop Transfer Functions

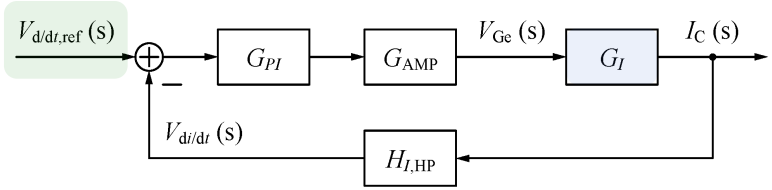
▶ Voltage slope



$$G_{V,\mathrm{OL}} = \frac{V_{\mathrm{d}v/\mathrm{d}t}}{V_{\mathrm{d}/\mathrm{d}t,\mathrm{ref}}} = G_{PI} G_{\mathrm{AMP}} G_V H_{V,\mathrm{HP}}$$

$$G_{V,\mathrm{CL}} = \frac{G_{V,\mathrm{OL}}}{1 - G_{V,\mathrm{OL}}}$$

▶ Current slope



$$G_{I,\mathrm{OL}} = \frac{V_{\mathrm{d}i/\mathrm{d}t}}{V_{\mathrm{d}/\mathrm{d}t,\mathrm{ref}}} = G_{PI} G_{\mathrm{AMP}} G_I H_{I,\mathrm{HP}}$$

$$G_{I,\mathrm{CL}} = \frac{G_{I,\mathrm{OL}}}{1 + G_{I,\mathrm{OL}}}$$

▶ Control performance

– **Strong dependency on IGBT module (G_V, G_I) parasitics !**

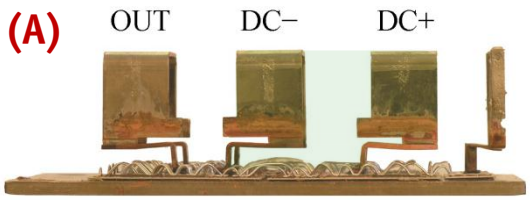
IGBT Modules – Internal Construction

▶ Parasitic inductances

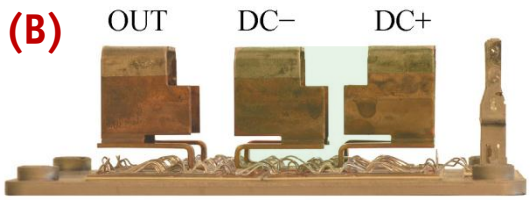
- Present in power and gate wiring
- Different for different modules (A, B, C); 1.2 kV, 400-450 A
- Affect the stability / control performance of the closed-loop control

▶ Power Terminals

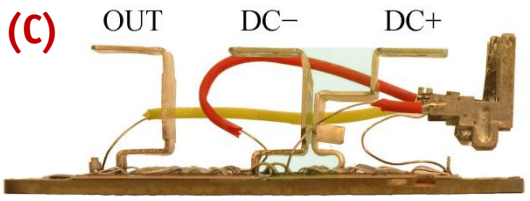
- $L_{DC+/DC-}$ = 20.9 ... 27.8 nH



$L_{DC+/DC-}$ = 27.8 nH



$L_{DC+/DC-}$ = 23.2 nH



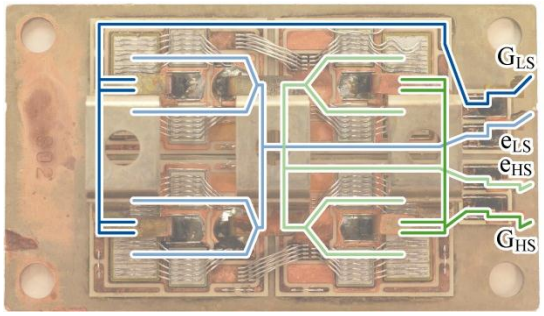
$L_{DC+/DC-}$ = 20.9 nH

IGBT Modules – Internal Construction

▶ Gate Wiring

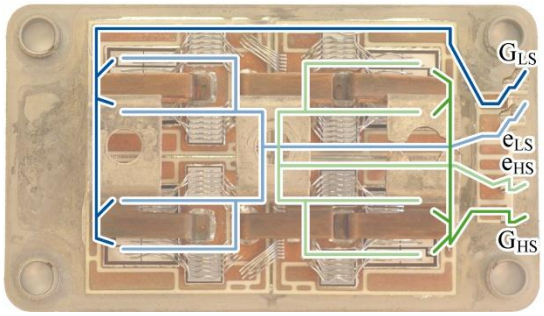
– $L_{Ge,LS/HS}$ = 54.2 ... 121.3 nH

(A)



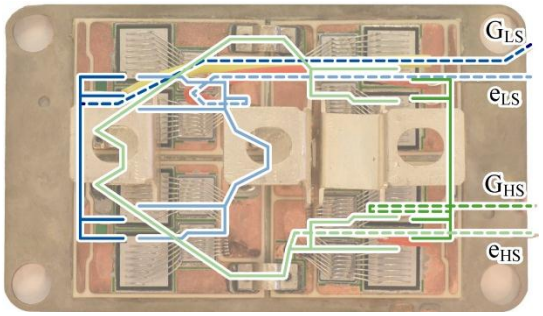
$L_{Ge,LS}$ = 104.6 nH
$L_{Ge,HS}$ = 54.2 nH

(B)



$L_{Ge,LS}$ = 94.8 nH
$L_{Ge,HS}$ = 30 nH*

(C)

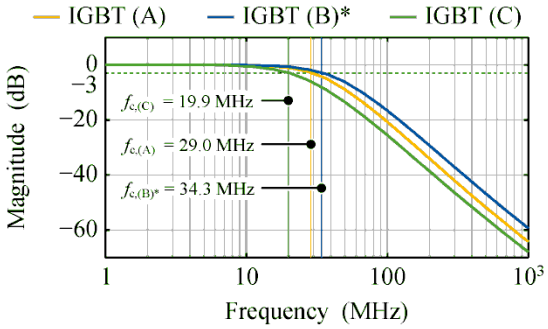


$L_{Ge,HS}$ = 121.3 nH
$L_{Ge,HS}$ = 83.5 nH

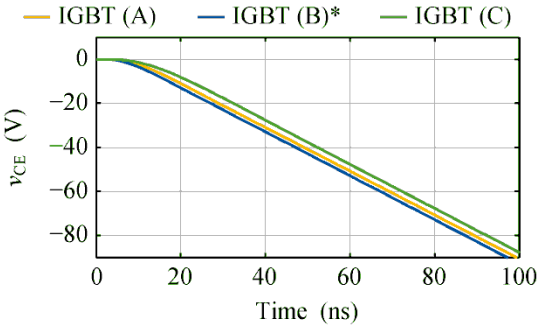
* Using a low-inductive coaxial connection to the foot ends of the gate driving terminals reduces the gate inductance by 26 nH, i.e. from 56 nH to 30 nH.

Closed-Loop Transfer Functions – Voltage Slope

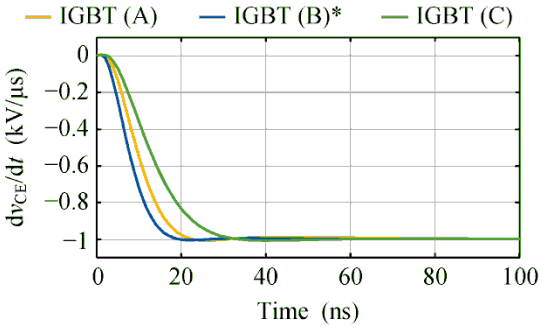
Bode diagram



v_{CE} step response



dv_{CE}/dt step response

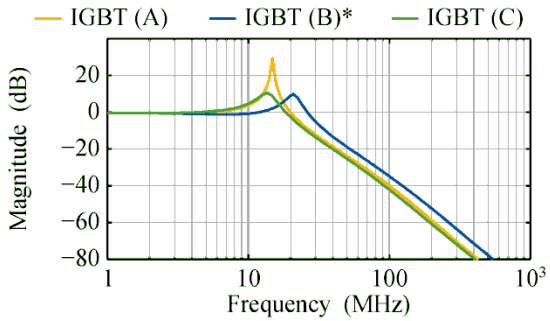


- **High gate loop inductance is unfavorable**
  - **High *P*- and *I* values of the controller needed**
  - **Lower control bandwidth f_c (limited gain-bandwidth product of op-amp)**
  - **Practical implementation: limited output voltage of op-amp and amplifier (+/- 15 V)**

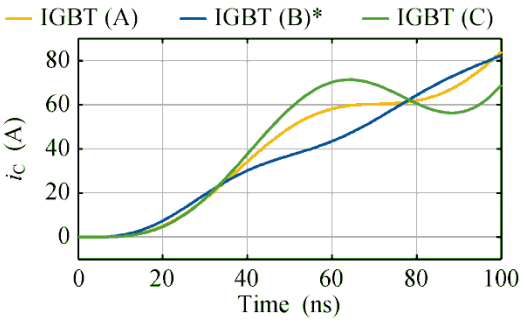
	P	I
IGBT (A)	3.75	$12.9 \cdot 10^7$
IGBT (B)*	1.34	$8.57 \cdot 10^7$
IGBT (C)	5.93	$14.5 \cdot 10^7$

Closed-Loop Transfer Functions – Current Slope (1)

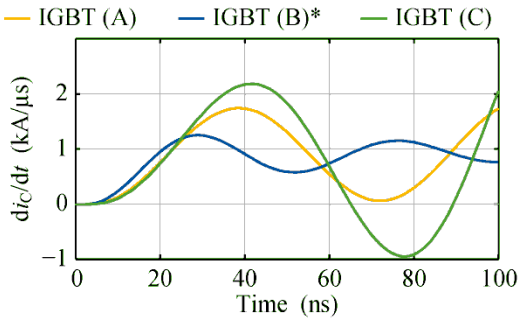
Bode diagram



i_C step response



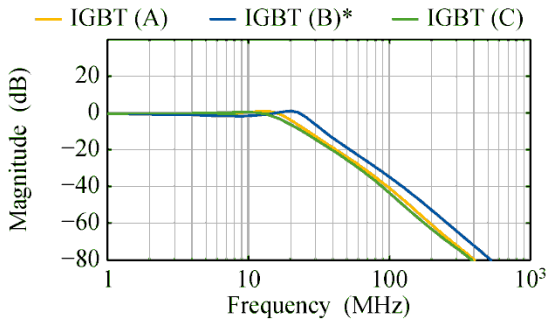
di_C/dt step response



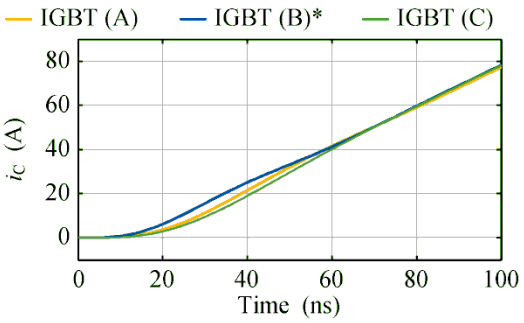
- **Unsatisfying performance !**
  - Only one *PI*-controller (here adjusted for the voltage slope), but two different control loops
  - Solution 1: adjustment of controller for the more sensitive loop, i.e. the current loop in this case
  - Solution 2: adding gate- or Miller capacitance as low-pass filters to the corresponding control loop (gate: di_C/dt; Miller: dv_{CE}/dt)

Closed-Loop Transfer Functions – Current Slope (2)

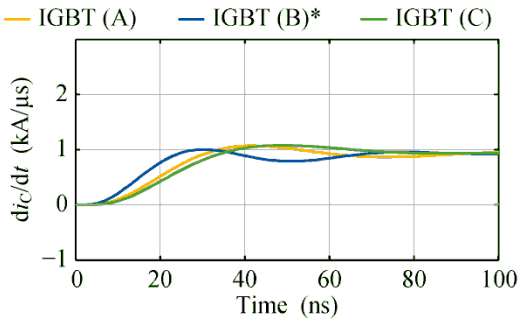
Bode diagram



i_C step response

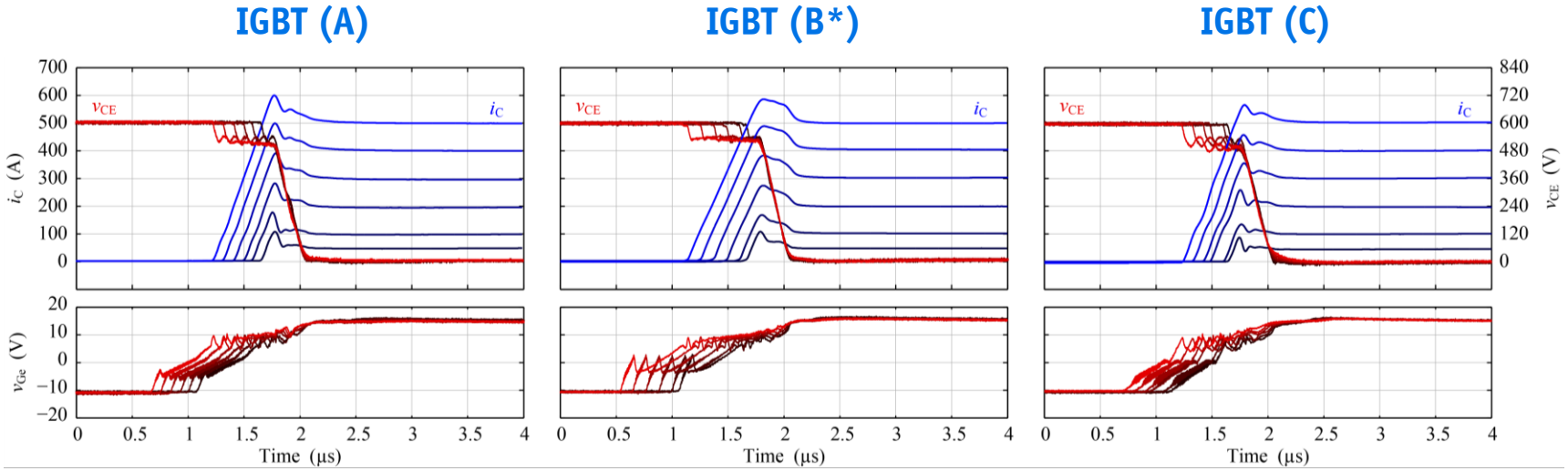


di_C/dt step response



- **Optimal performance for voltage and current control !**
  - Same *P*- and *I*-parameters as before, but with additional gate capacitance
  - Additional degree of freedom for individual control loop optimization
  - Disadvantages
    - Additional gate driving losses
    - Difficulty of inserting a capacitor close to the IGBT chip

IGBT Module Comparison at Closed-Loop Switching

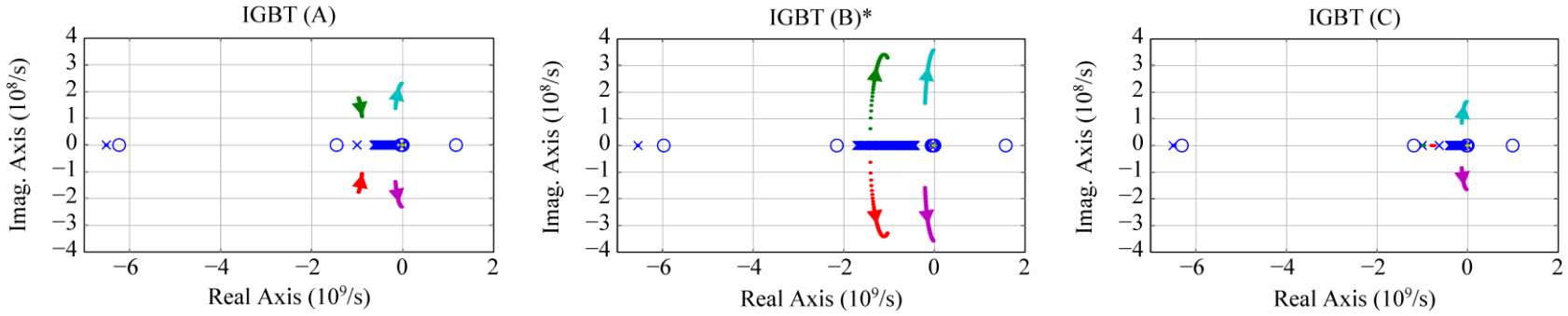


- Similar switching performance for different IGBT modules
- Lowest gate loop inductance –> Highest control bandwidth
  - Most accurately controlled voltage and current slopes
  - Most stable control performance
  - Here: no additional gate capacitance was used to optimize the current control loop

Stability Analysis for Parameter Variations (1)

▶ Sensitivity to the *PI*-controller gain

– Increasing of *P* up to 4-times nominal value



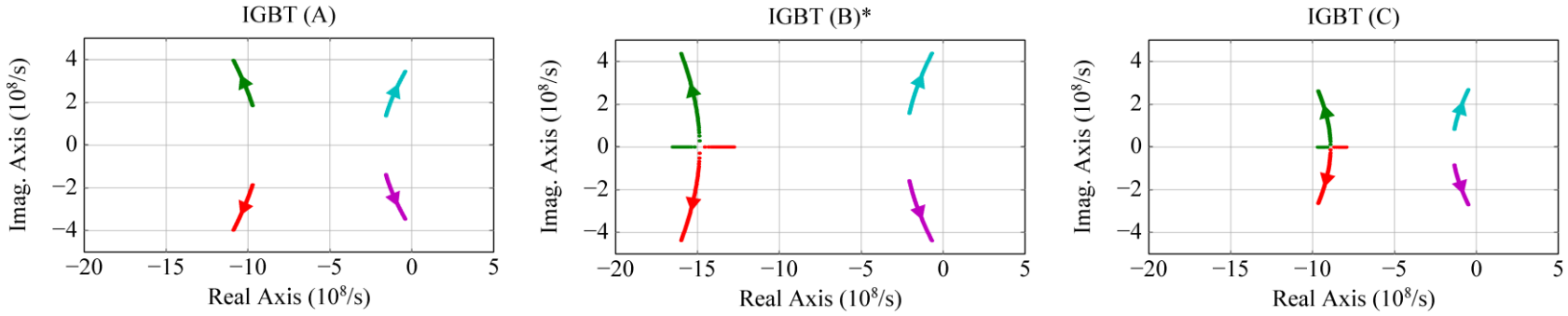
▪ Not critical

– Pivotal poles are shifted towards the right s-half plane
– *P* is properly adjusted initially
– *P* is kept constant
– Factor 4 is far away from tolerances

Stability Analysis for Parameter Variations (2)

▶ Sensitivity to the Miller capacitance

– **Decreasing of C_{GC} down to 0.25-times nominal value**



▪ Worst case assumption of C_{GC} (for high values of v_{CE})

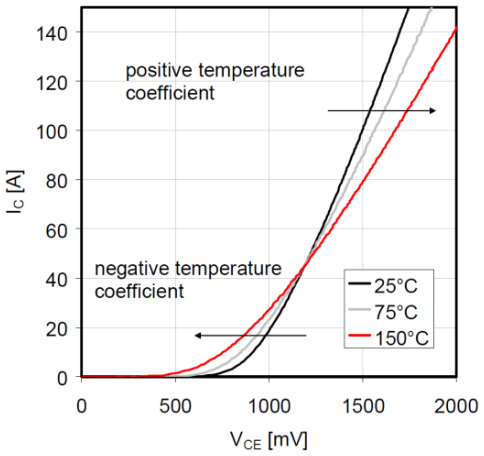
– **Pivotal poles are shifted towards the right s-half plane**
– **System is still stable**
– **Value of C_{GC} can be extracted from datasheet, thus no stability issues are expected**

Future Trends

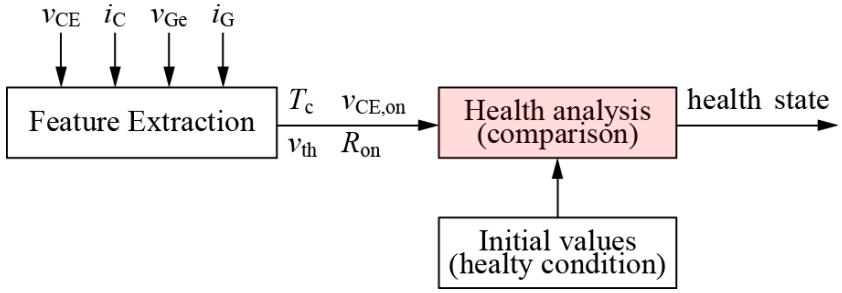
- IGBT Protection
- IGBT Monitoring / Online Measurement

IGBT Protection

- **Overcurrent: i_C at turn-on**
  - Active integration of Rogowski coil voltage or voltage across main/aux. Emitter terminals
- **Desaturation: $v_{CE,sat}$**
  - Accurate measurement of v_{CE} in on-state with clipping circuit
- **Overtemperature: T_j**
  - Estimation based on on-state characteristics



- **Health analysis for protection**



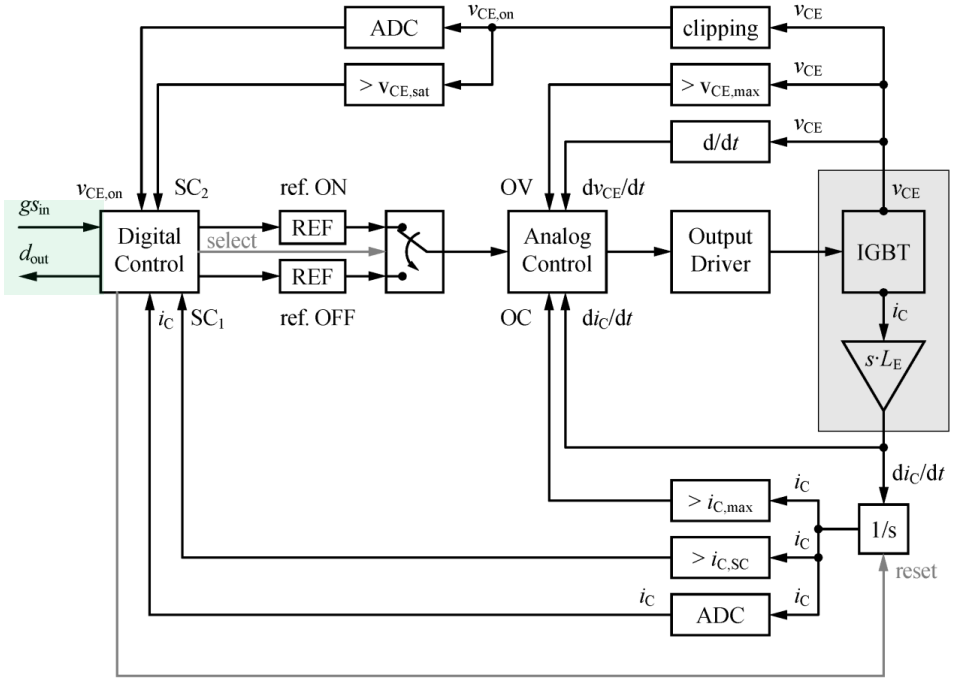
IGBT Monitoring / Online Measurement

▶ Feedback to main controller: d_{out}

- Switched current i_C
- On-state voltage $v_{CE,on}$
- Estimated junction temperature T_j
- Health state

▶ Superordinate control by main controller

- Converter control at max. output power, i.e. at max. junction temperature instead of max. rated power, with T_j feedback



Summary

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- **Closed-loop di/dt and dv/dt gate drive**
  - ensures a defined and safe switching behavior
  - enables a desired trade-off between switching losses and EMI

- **Minimize**
  - Switching losses
  - Delay times

- **Compensate**
  - Junction temperature
  - Load current level

- **Limit**
  - Turn-off overvoltage
  - Turn-on reverse recovery current

- **Ensure**
  - SOA operation
  - EMI specifications

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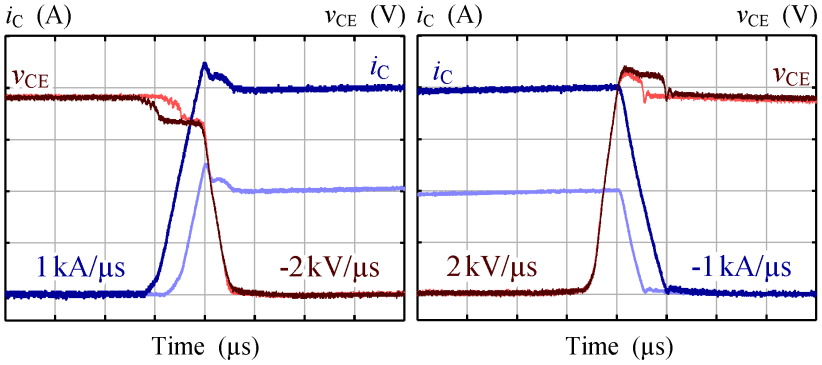

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Questions ?