Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Power Electronic Systems Laboratory

Nordic Power Converters
Powering a brighter future™

Multi-objective Optimization of Fully Integrated Voltage Regulators:

Switched Capacitor and Inductor-Based Converters

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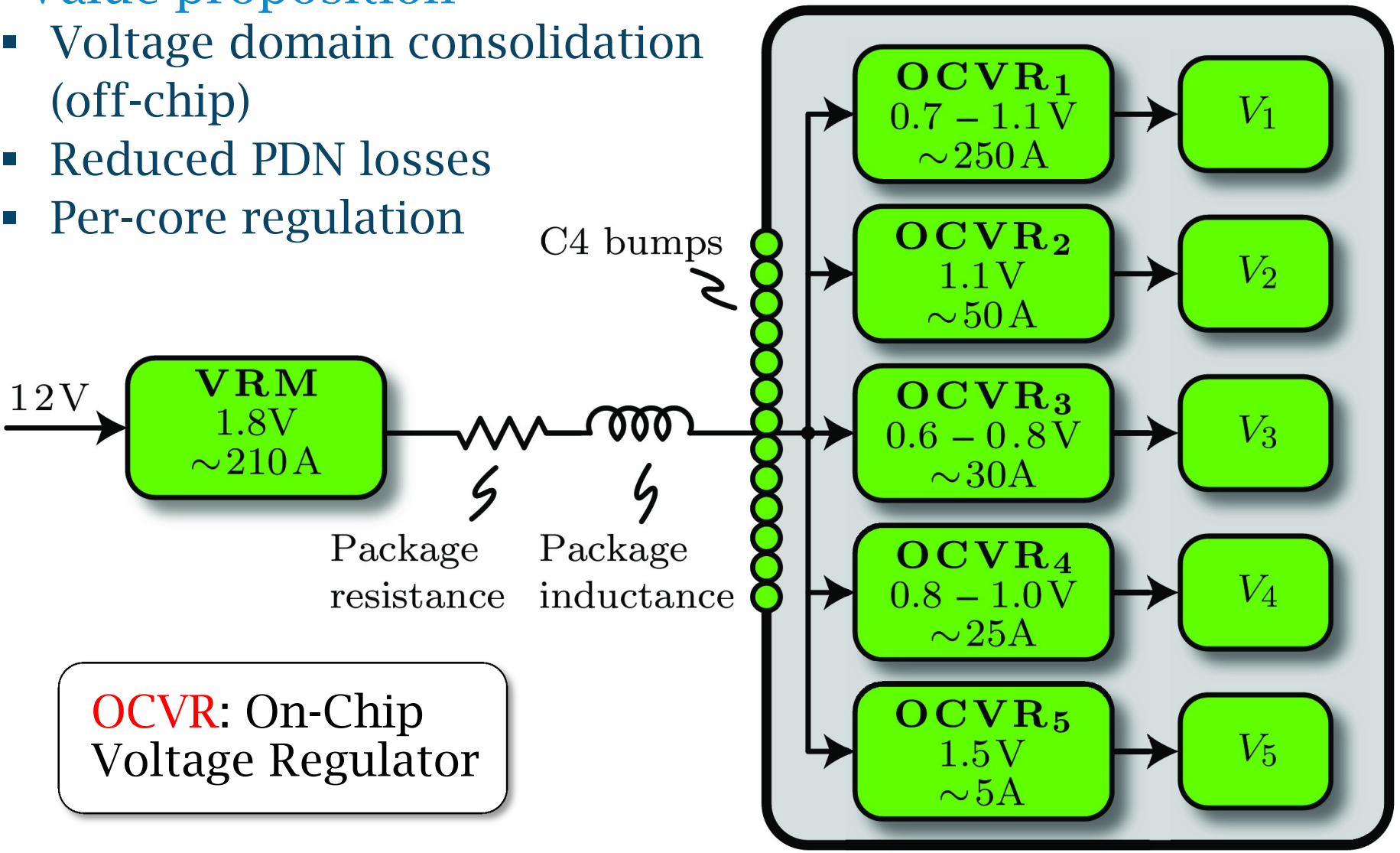
Arvind Sridhar, Thomas Brunschwiler, Thomas Toifl

Granular Microprocessor Power Delivery

- Value proposition
  - Voltage domain consolidation (off-chip)
  - Reduced PDN losses
  - Per-core regulation



OCVR: On-Chip Voltage Regulator

– How to Design an On-Chip Voltage Regulator that…

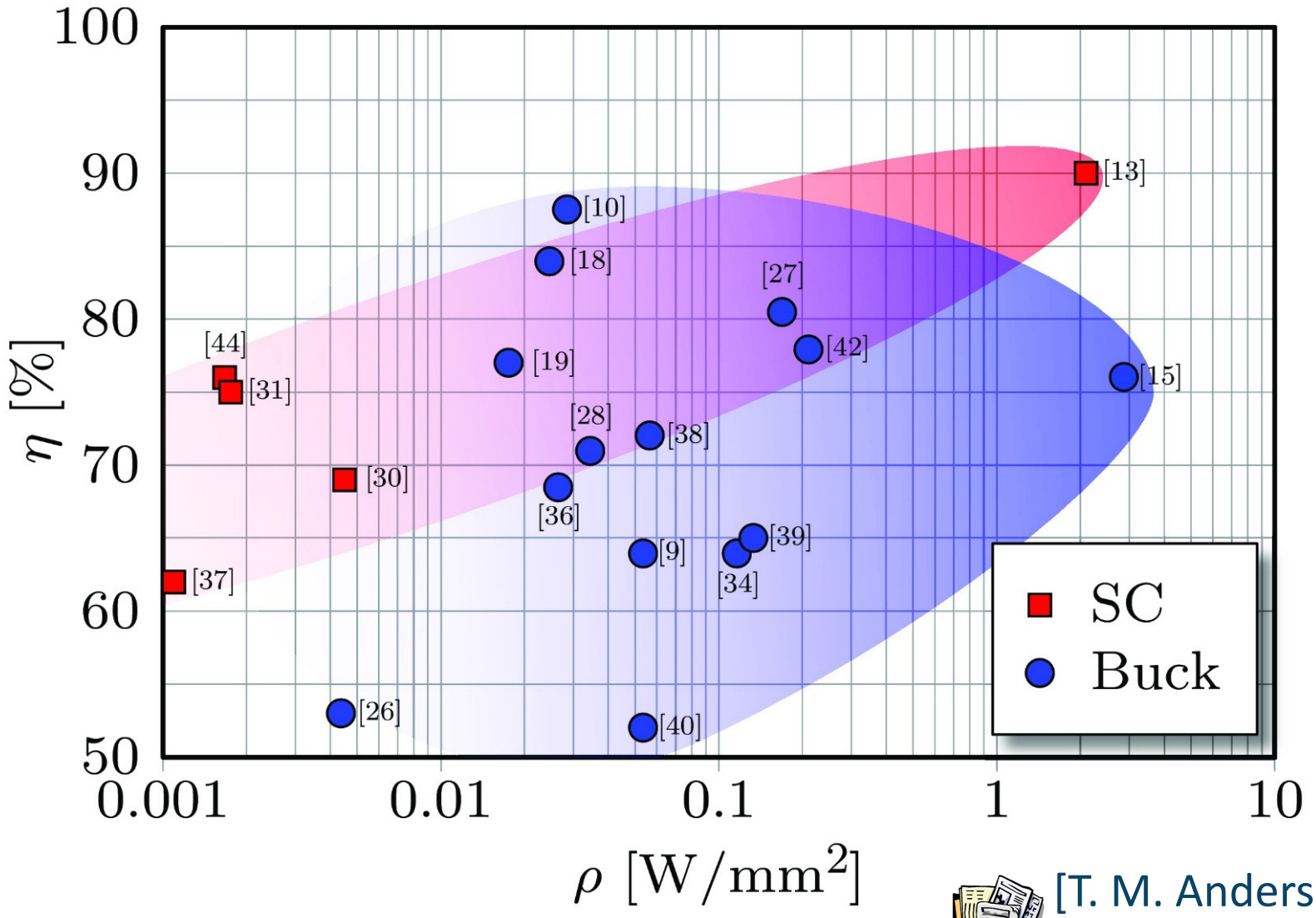
- Achieves high efficiency?
  > 85%
- Achieves high power density?
  > 1 W/mm^2
- Achieves fast transient response?
  < 1 ns
- Achieves high output power?
  > 1 W

Simultaneously!

Outline

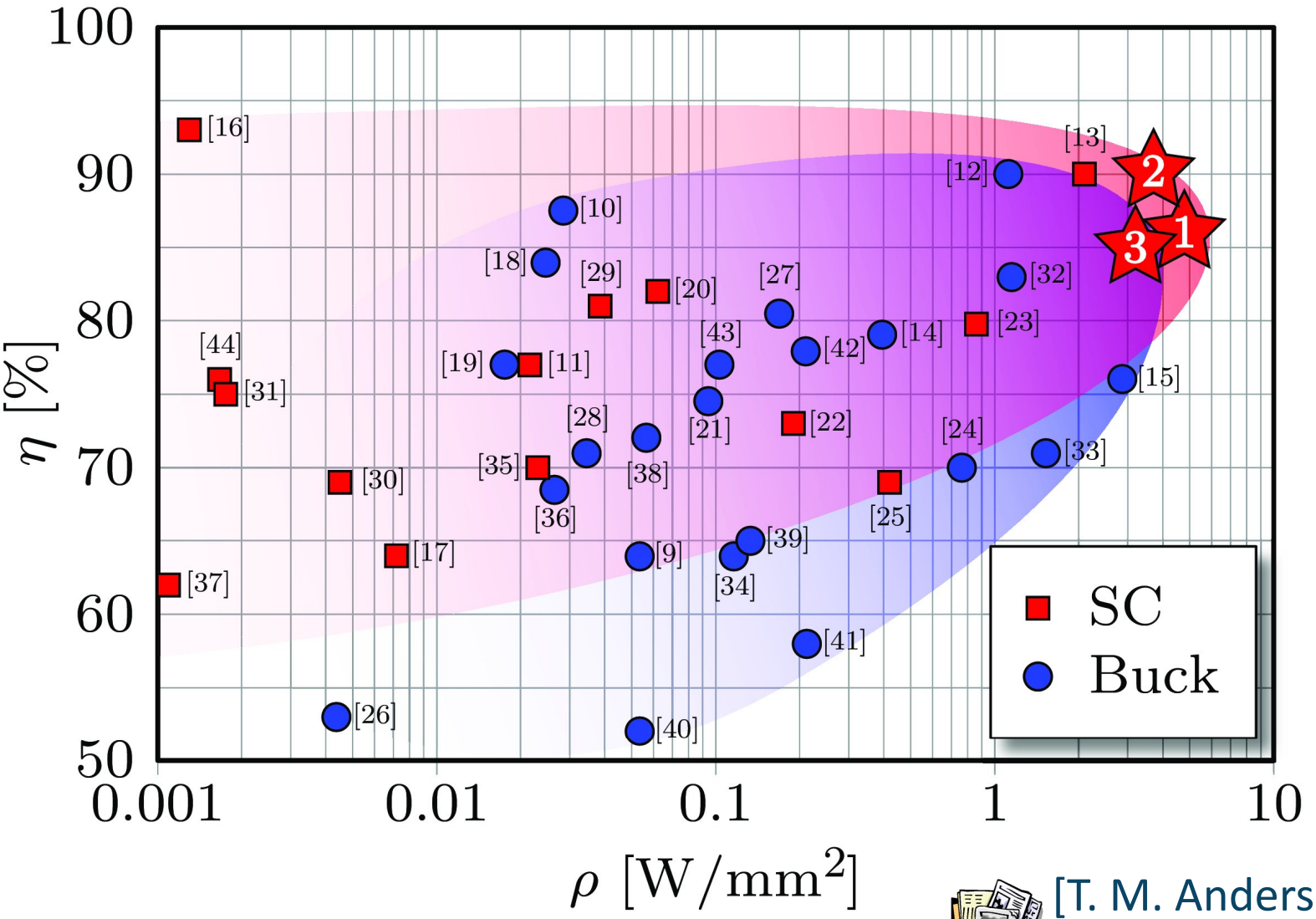
- State of the art on FIVRs
- Switched capacitor converters
  - Components' technologies
  - State space model framework
  - 2:1 SC converter design
  - Hardware results
- Inductor-based converters
  - Considered converter topology
  - PMIC components' models
  - Optimization procedure
  - Optimization results
- Summary and conclusion

State of the Art 2010



[T. M. Andersen, PhD thesis]

State of the Art 2015



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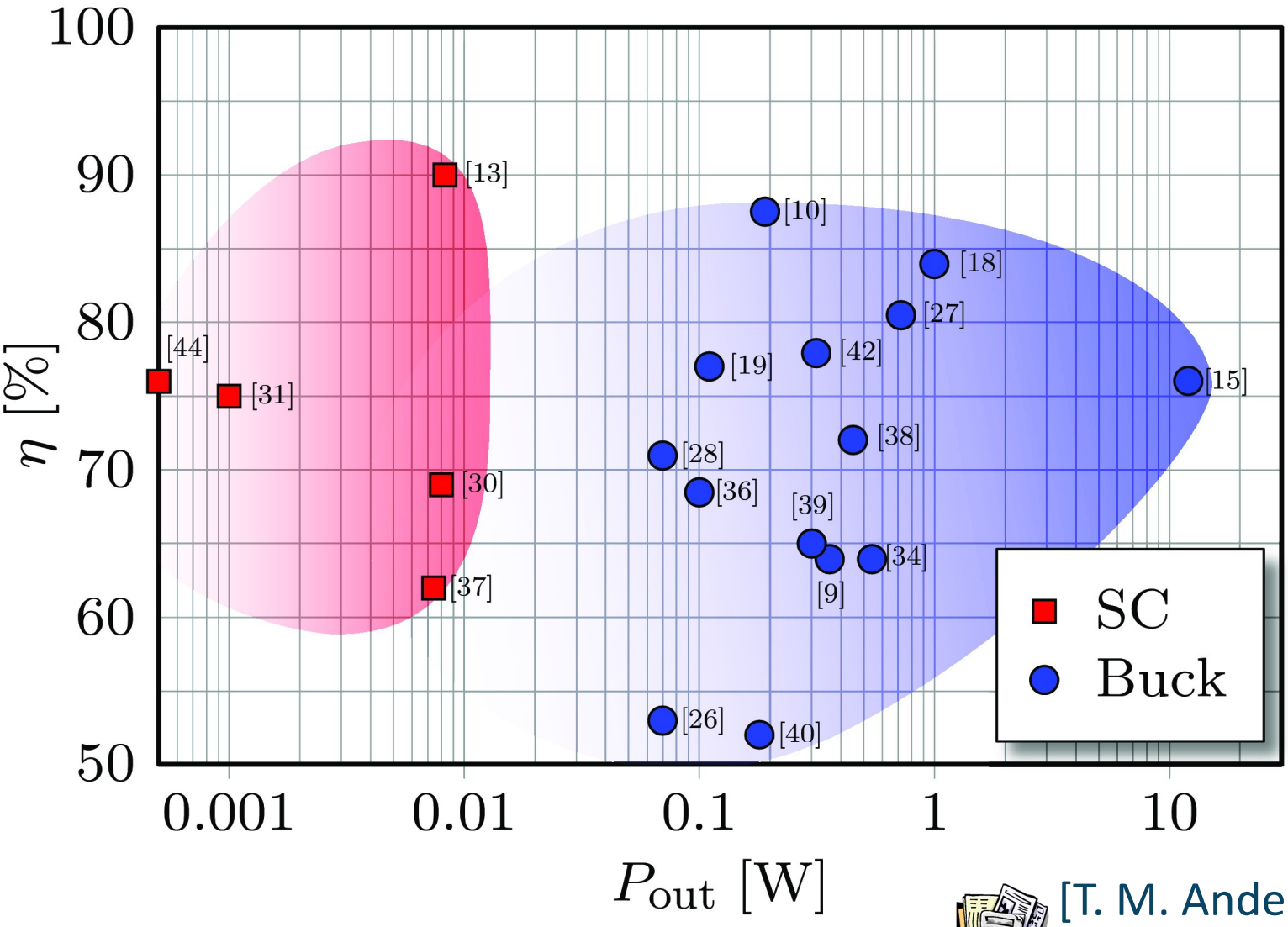
State of the Art 2010



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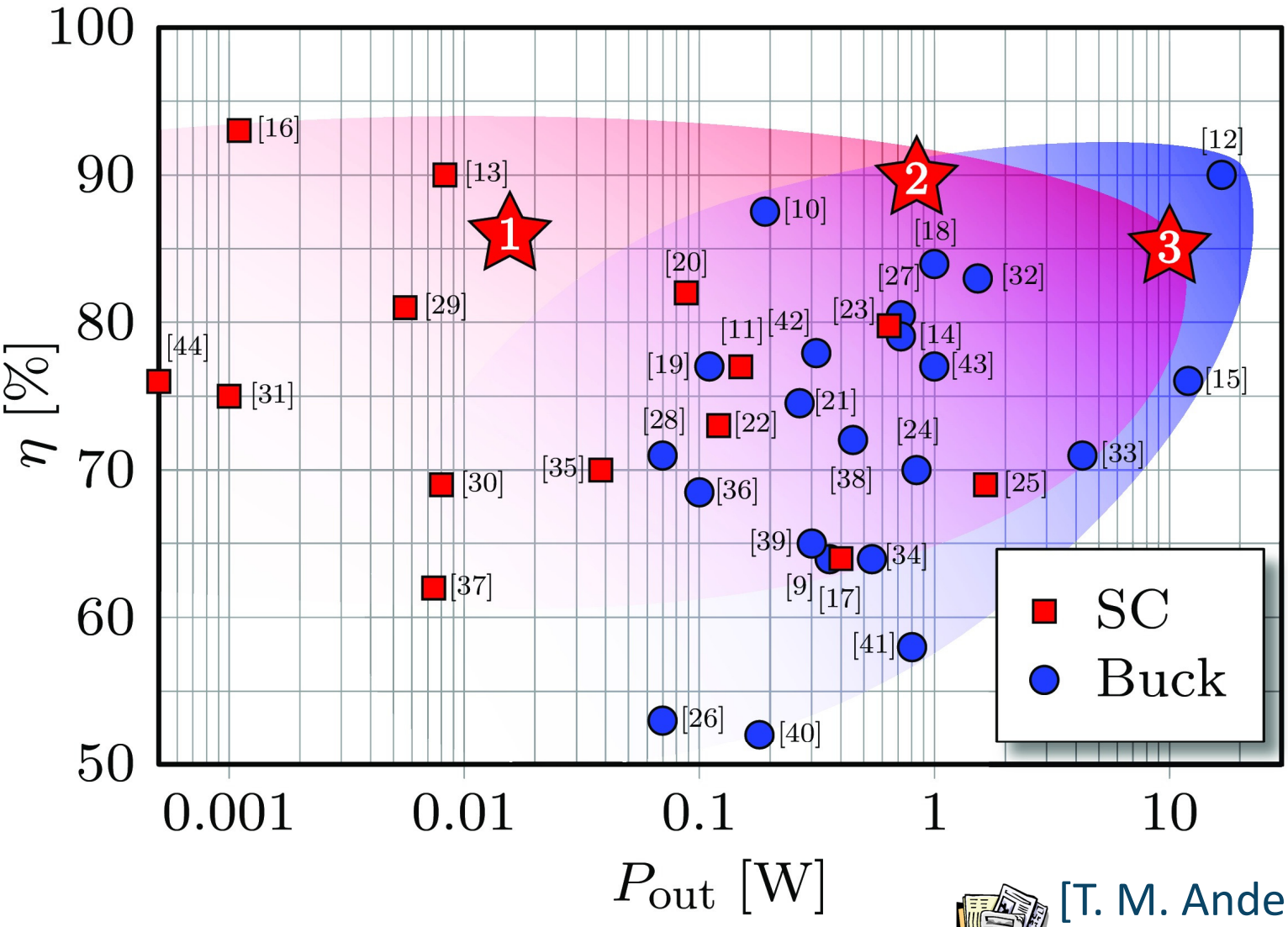
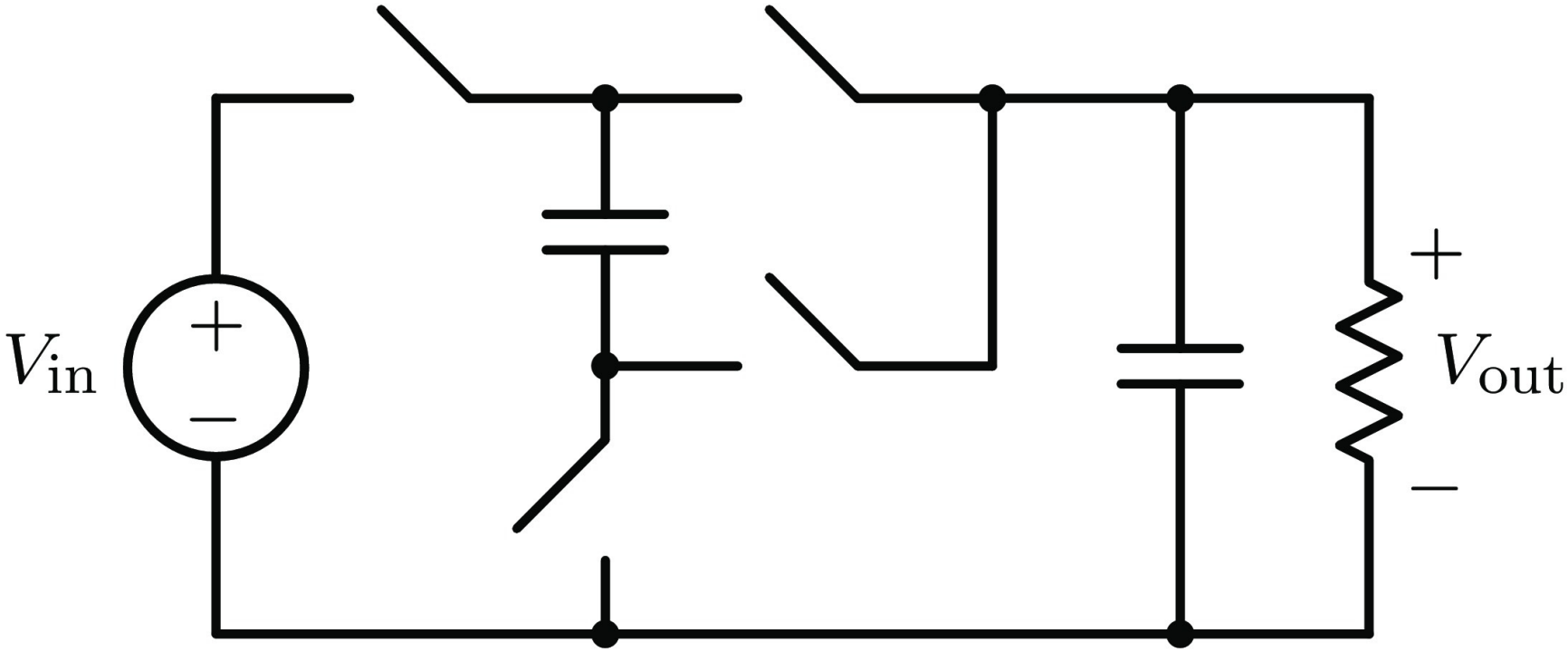
State of the Art 2015



[T. M. Andersen, PhD thesis]

On-Chip Switched Capacitor Converters

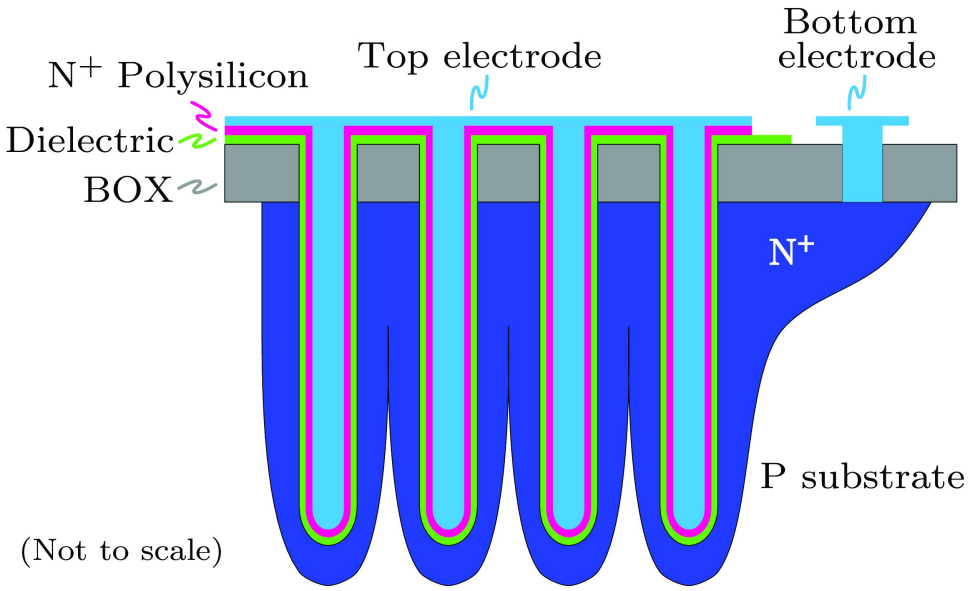


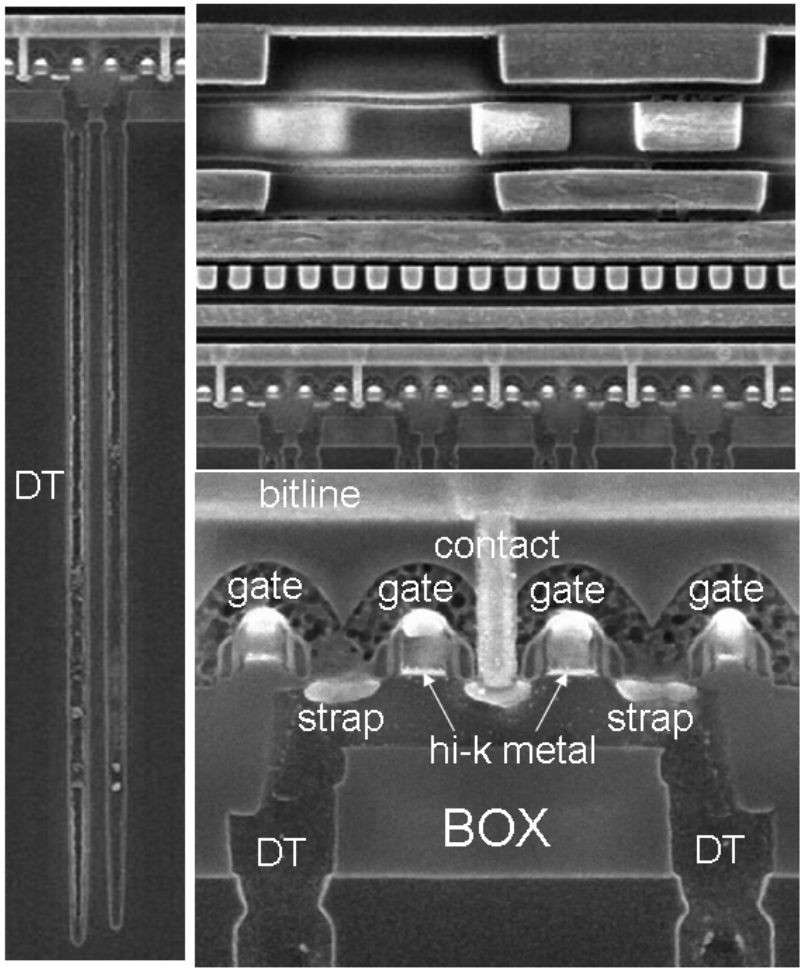
- 2:1 Switched capacitor topology

32 nm SOI CMOS Semiconductor Technology

Deep Trench Capacitor

- High capacitance density
- Low bottom plate losses



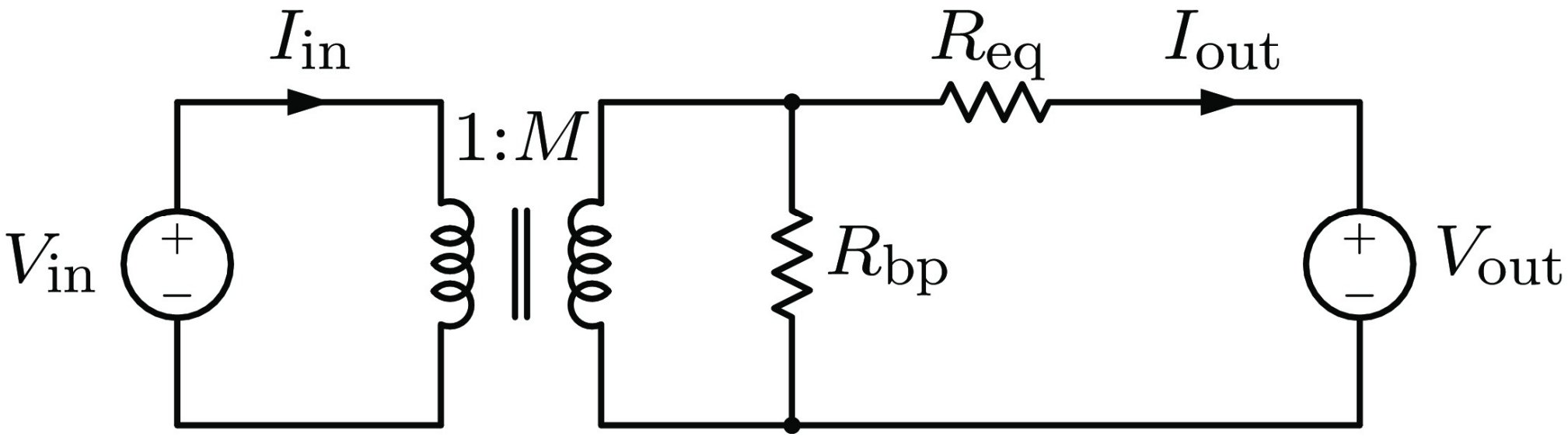


Thin-Oxide Transistors

- Good R_{on} and Q_g FOM
- 1.2V allowable blocking voltage

Wang et al., EIDM 2009

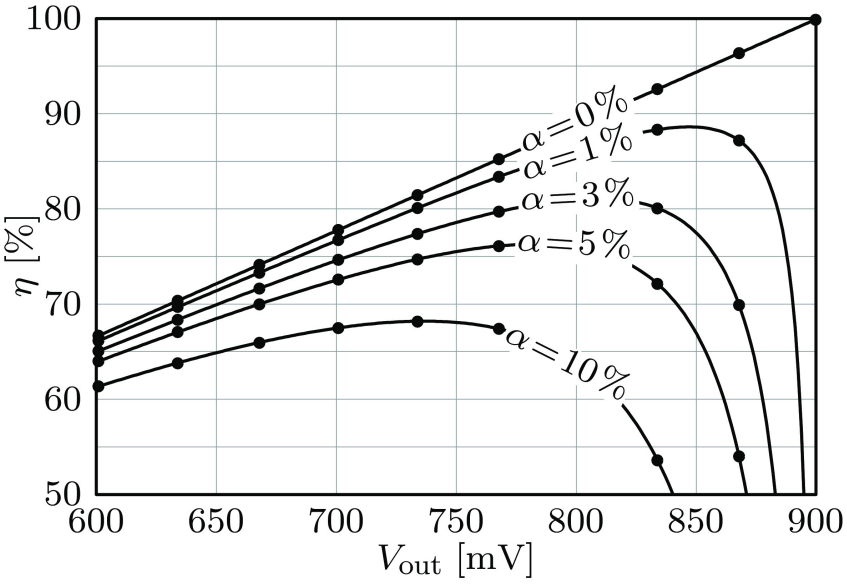
SC Equivalent Model

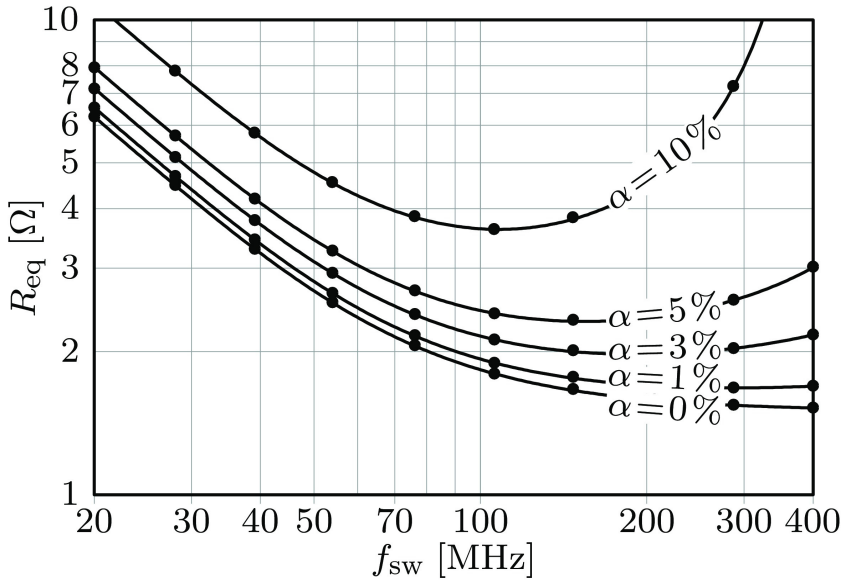


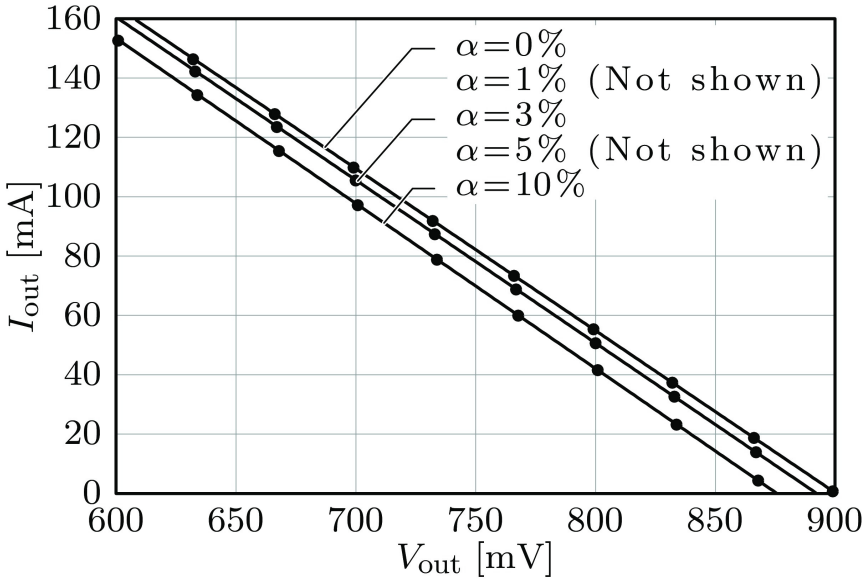
- State Space Model Framework
  - Include parasitic bottom plate capacitance modeled by R_{bp}
  - No approximation in R_{eq}

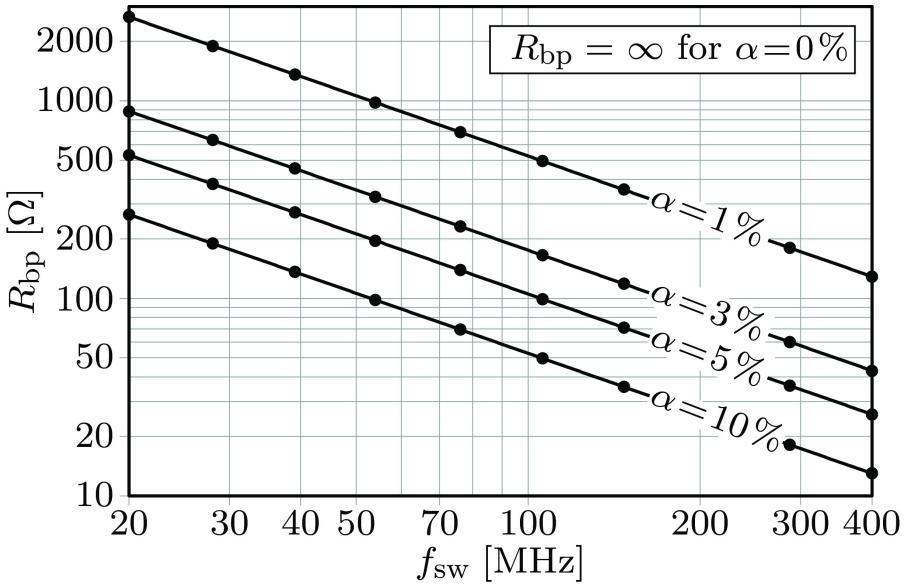
$$R_{\text{eq}} = \frac{MV_{\text{in}} - V_{\text{out}}}{I_{\text{out}}} = \frac{\frac{1}{2}V_{\text{in}} - V_{\text{out}}}{\left(2q_C - q_{C\text{bp}}\right) f_{\text{sw}}} \qquad R_{\text{bp}} = \frac{MV_{\text{in}}}{\frac{1}{M}I_{\text{in}} - I_{\text{out}}} = \frac{\frac{1}{2}V_{\text{in}}}{q_{C\text{bp}} f_{\text{sw}}},$$

Model Verification, $\alpha = \frac{C_{bp}}{C}$

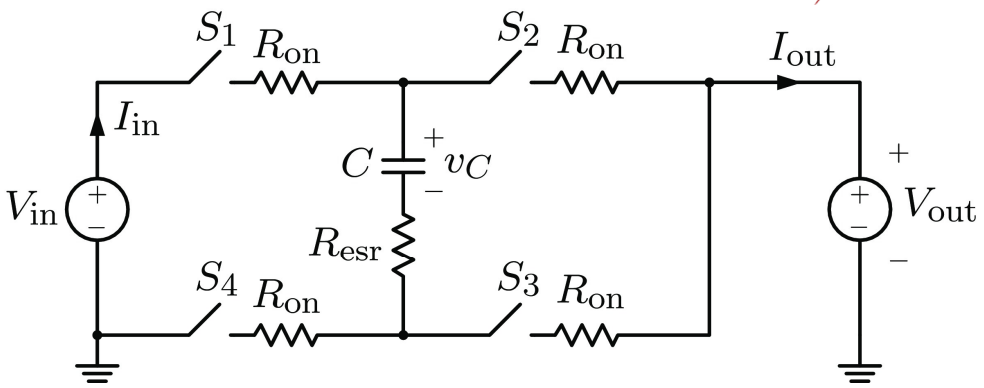


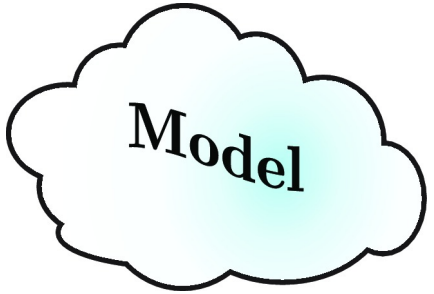






2:1 SC Converter Design

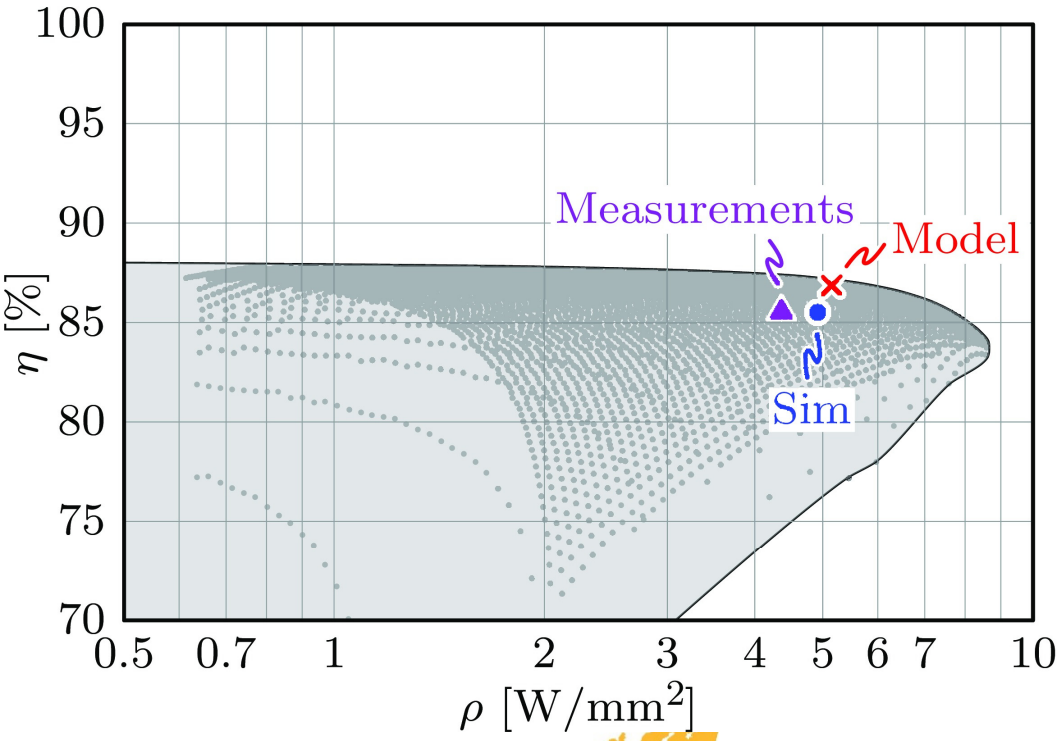




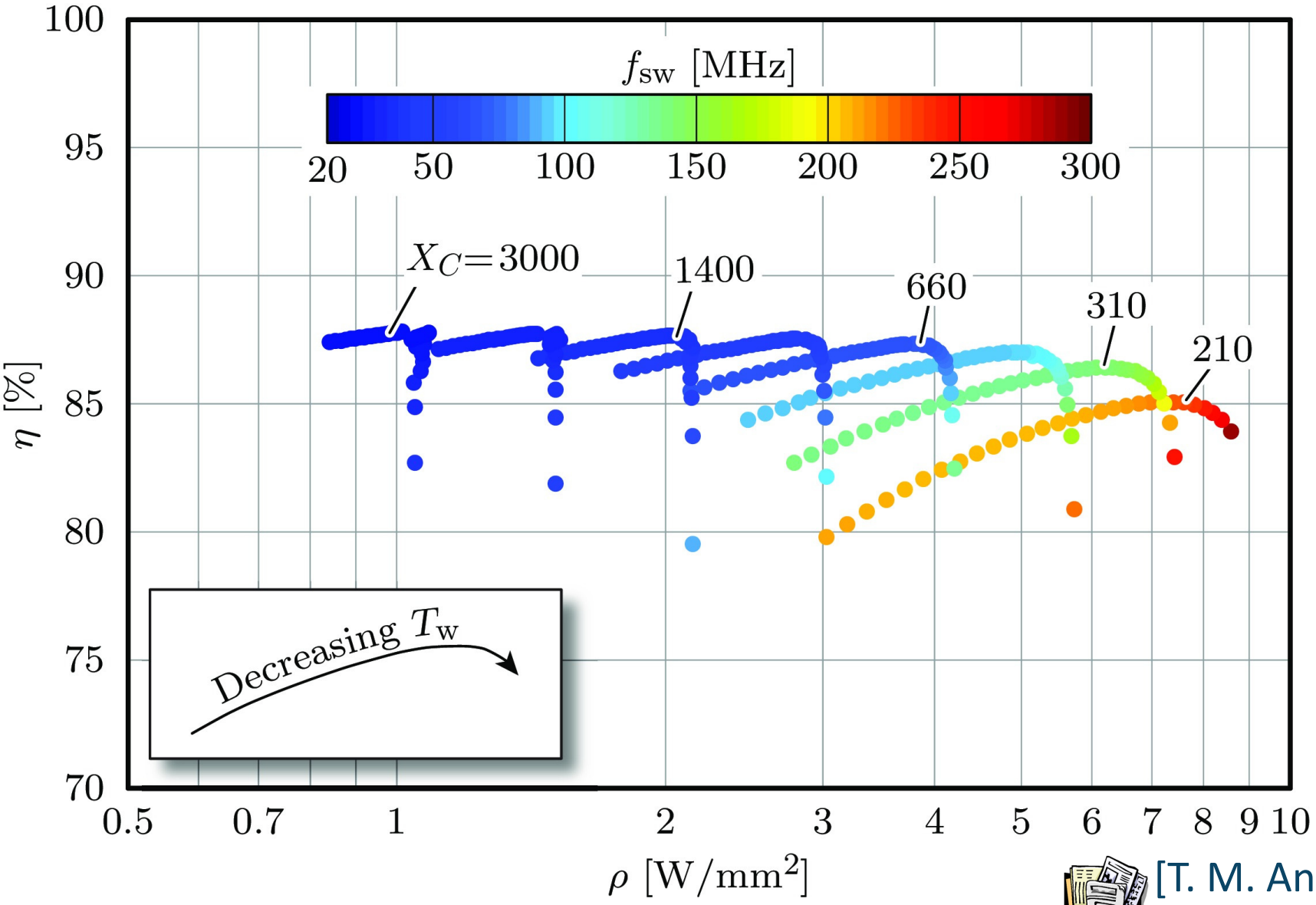
[T. M. Andersen, PhD thesis]

Pareto Optimization

- Specifications
  - $V_{in} = 1.8\,V$
  - $V_{out} = 830\,mV$
  - $I_{out} = 20\,mA$
- Design Space
  - Transistor width
  - Capacitance
  - Switching frequency

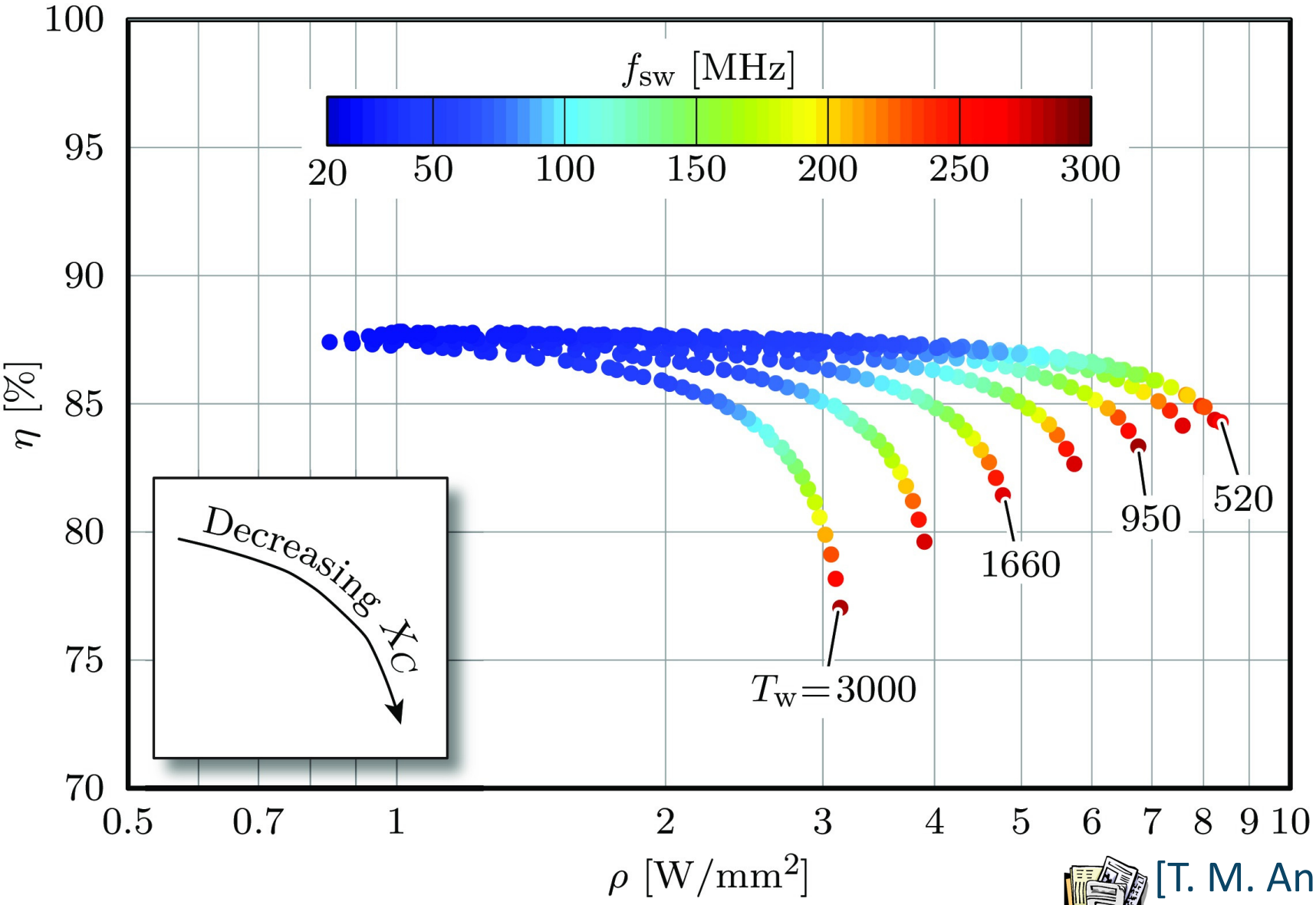


SC Pareto Front Investigation I



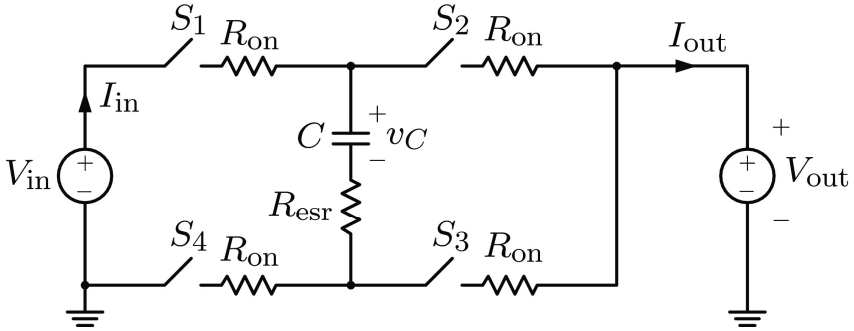
[T. M. Andersen, PhD thesis]

SC Pareto Front Investigation II

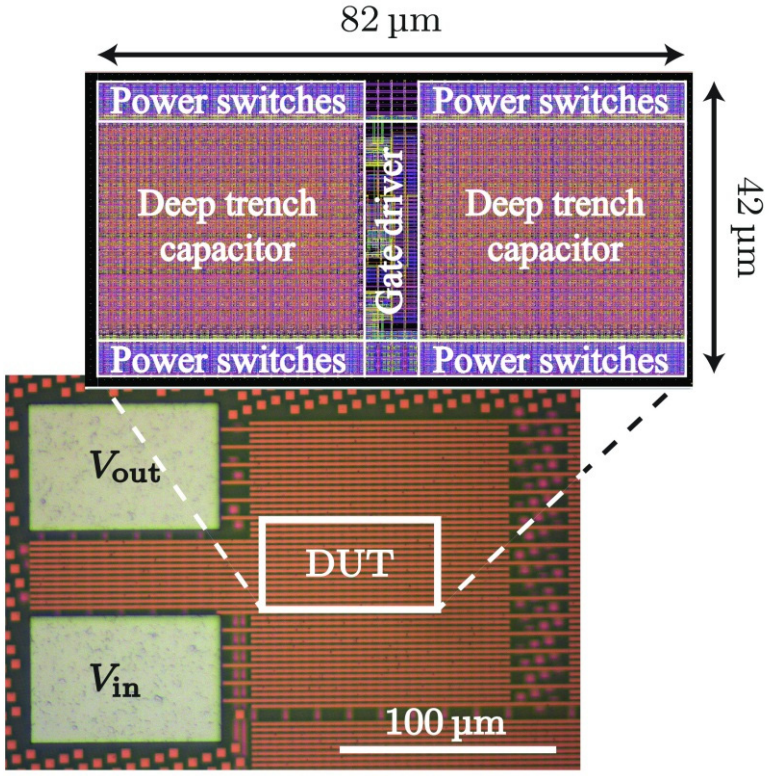


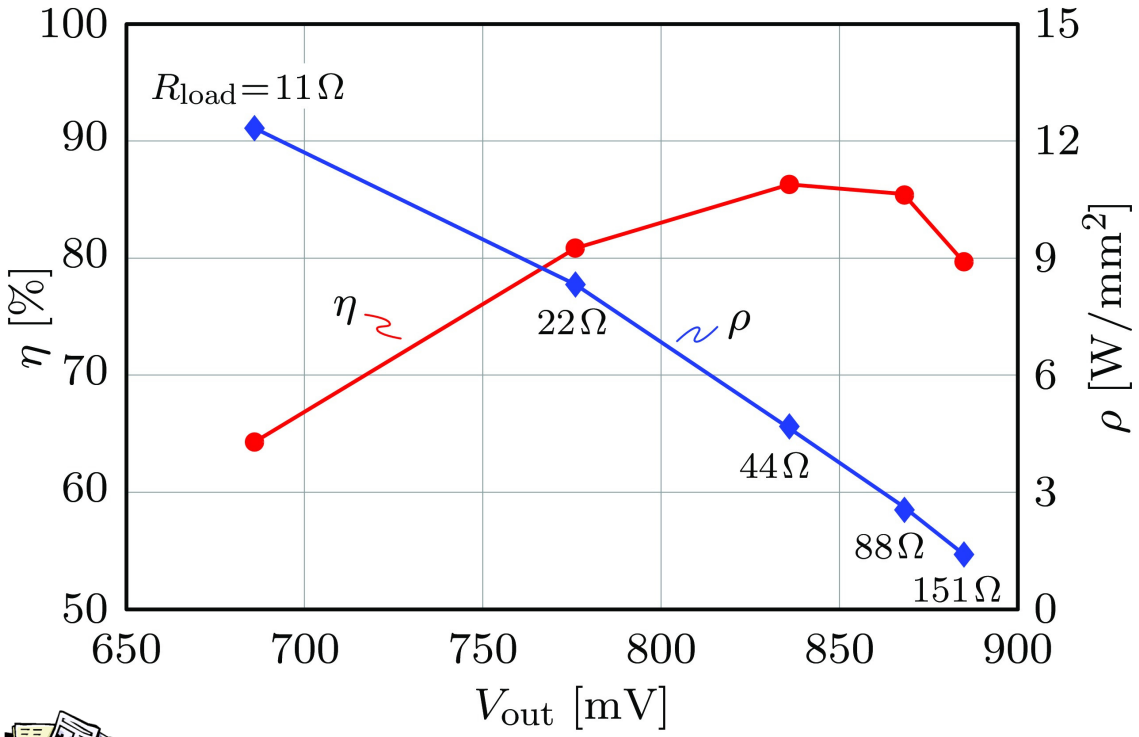
[T. M. Andersen, PhD thesis]

First chip – 2:1 SC Converter

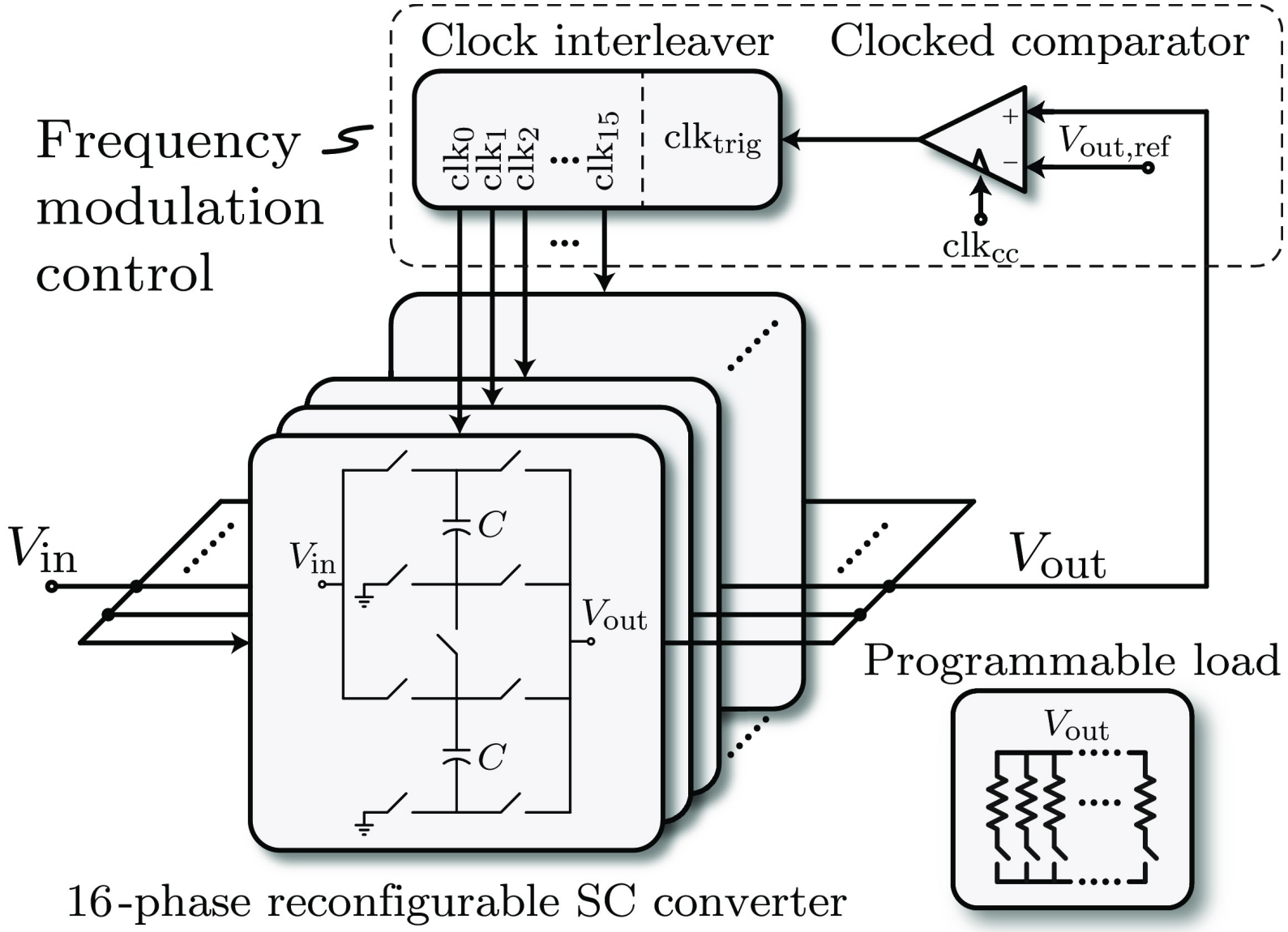


- A "learning vehicle"
  - 32 nm SOI CMOS
  - 86% efficiency
  - 4.6 W/mm² power density
    (= 4600 kW/liter for 1 mm height)
  - 100 MHz switching frequency

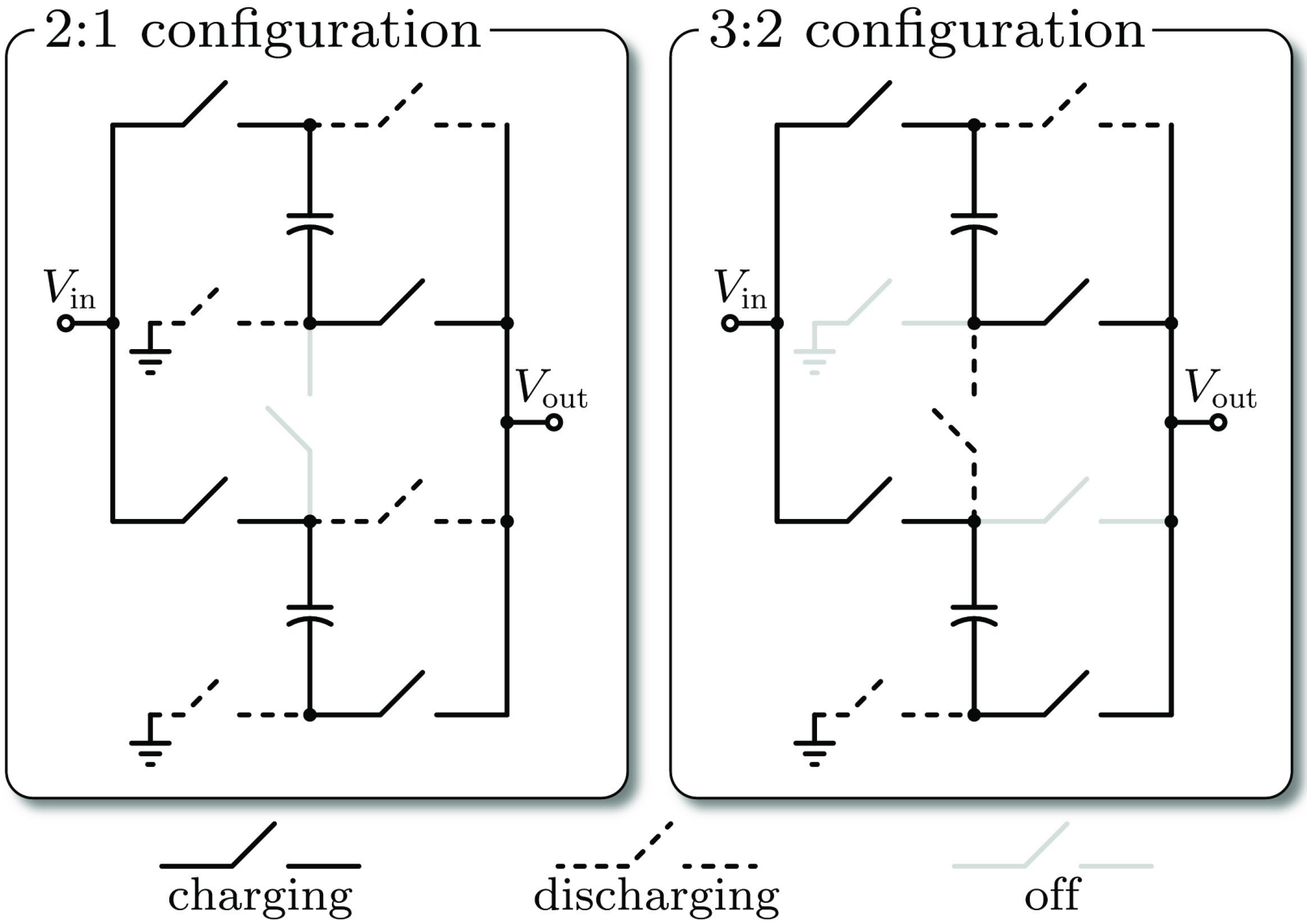




Second Chip: Overview

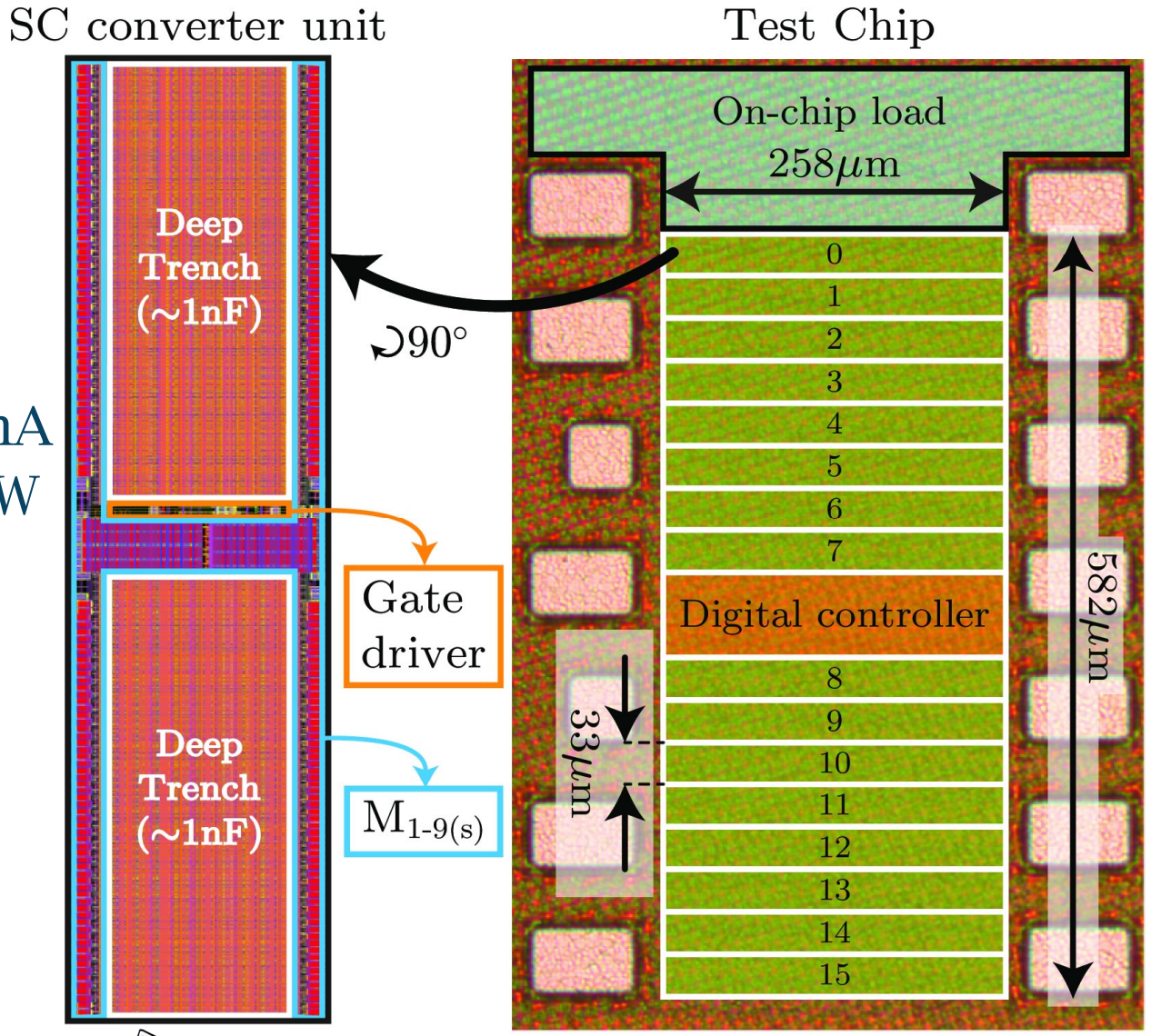


Reconfigurable SC Converter

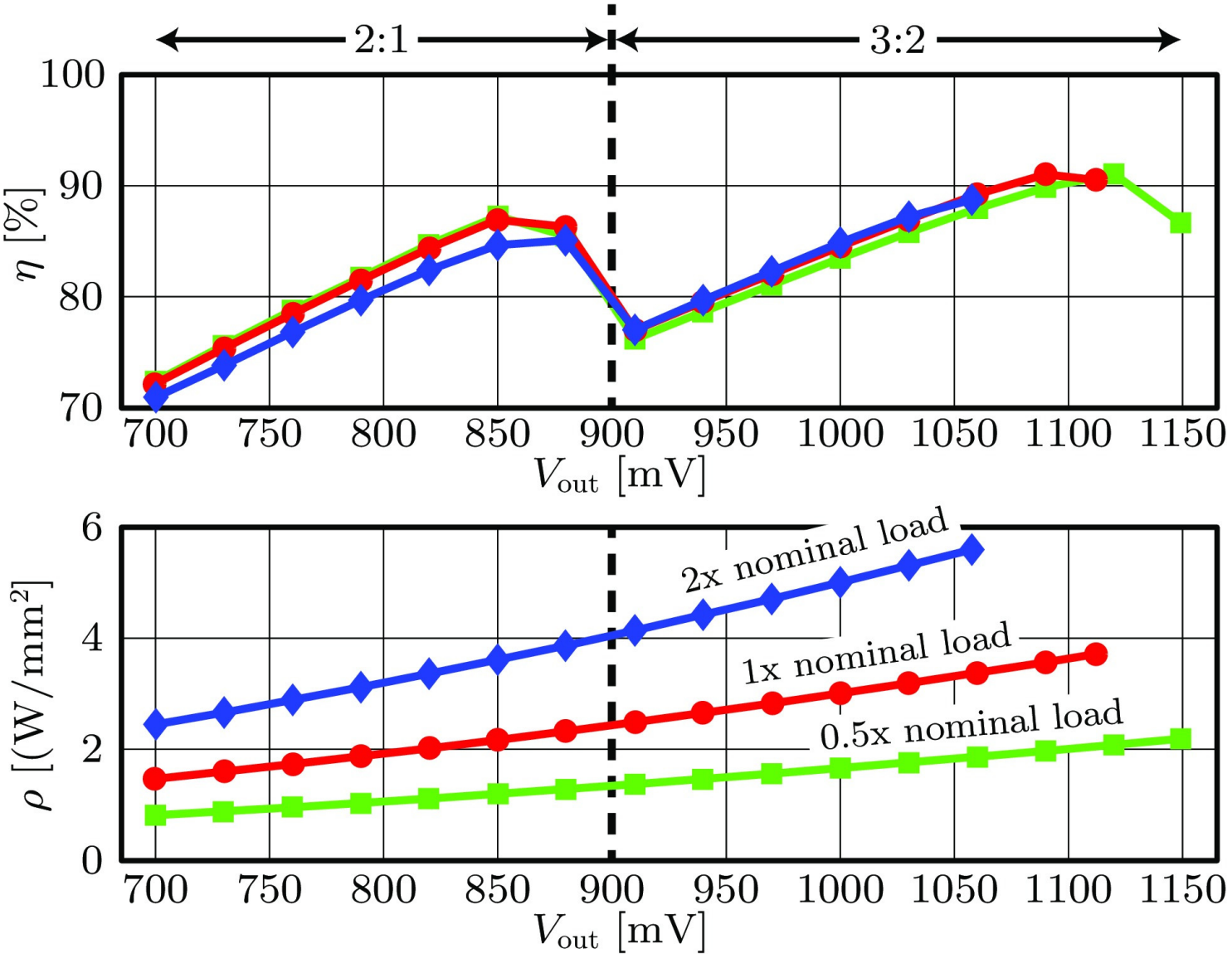


Implementation in 32nm SOI CMOS

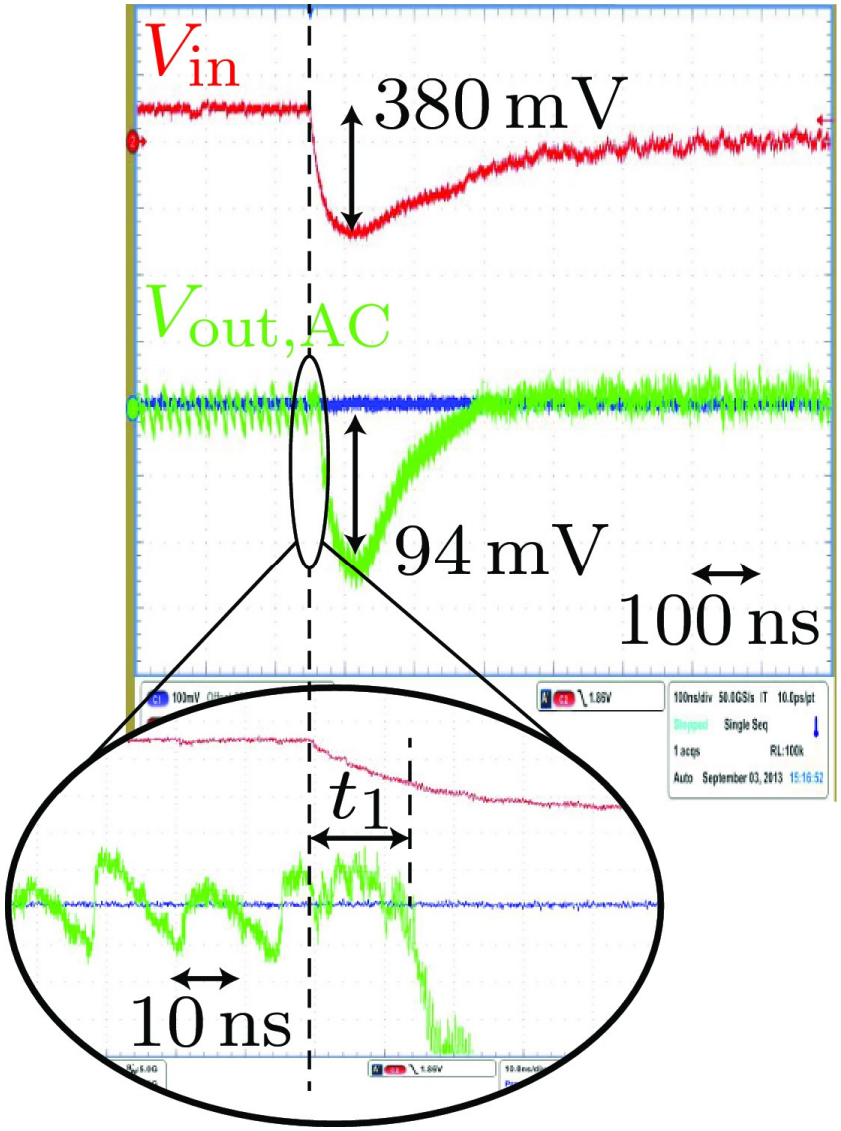
- Specifications
  - V_{in} = 1.8 V
  - V_{out} = 0.7 V - 1.1 V
  - I_{out} = 0 m A - 770 mA
  - P_{out} = 0 mW- 840 mW
  - C_{out} = 0 nF
  - # = 16
  - f_{trig} = 4 GHz
  - $f_{sw,max}$ = 125 MHz
  - Area = 0.15 mm²



Measured Efficiency and Power Density

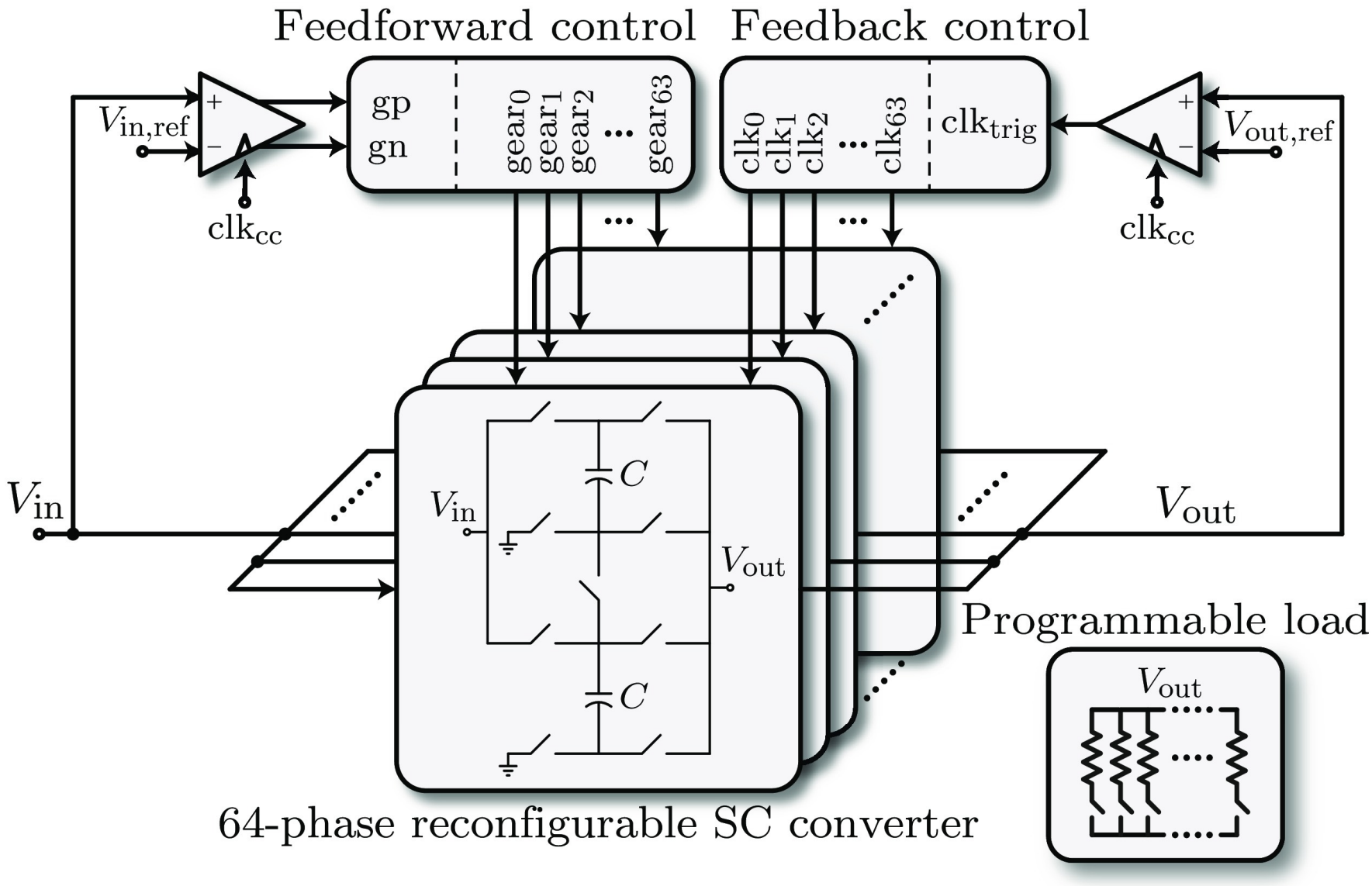


Measured Transient Response

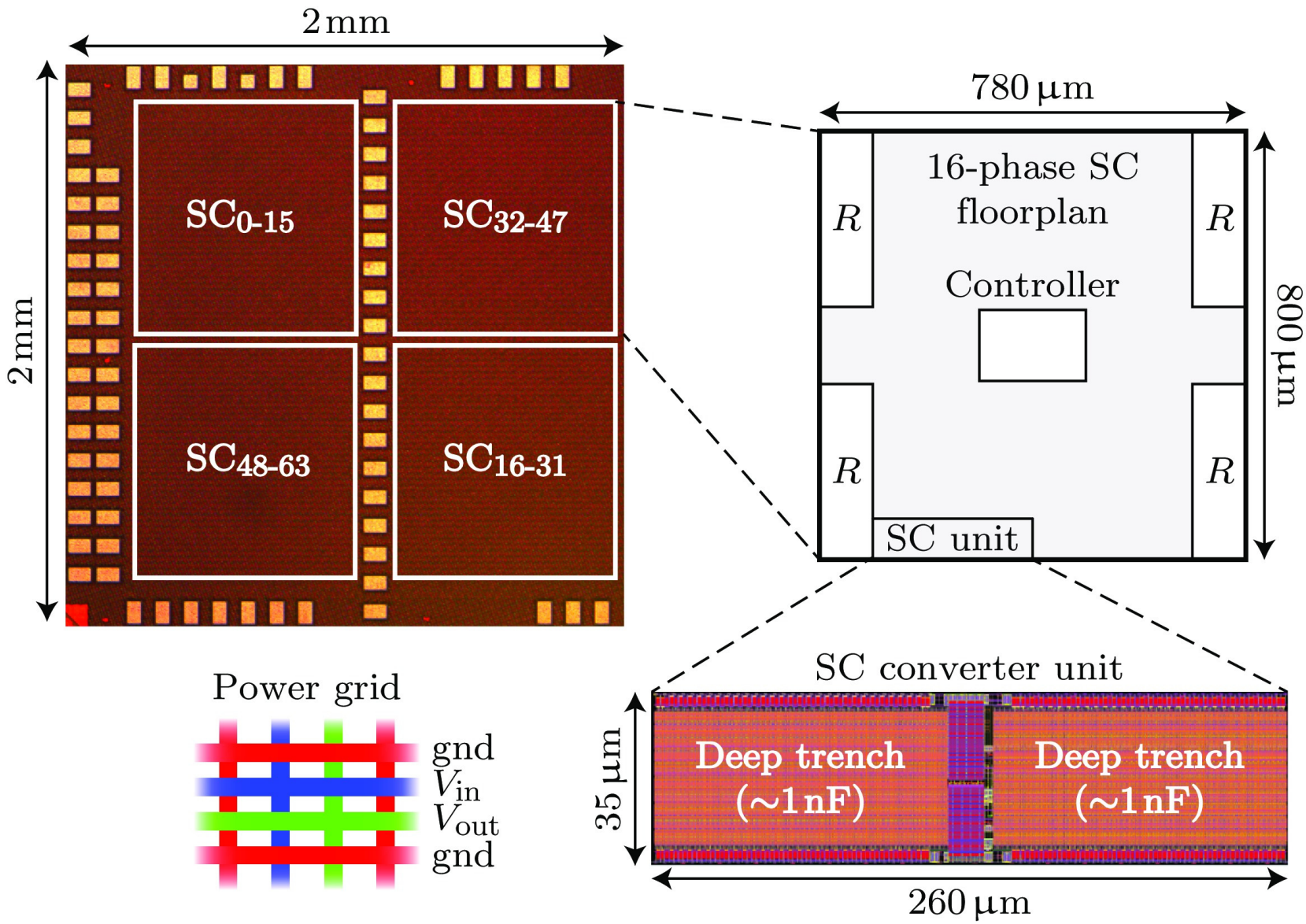


V_{in} collapse is causing the output voltage droop

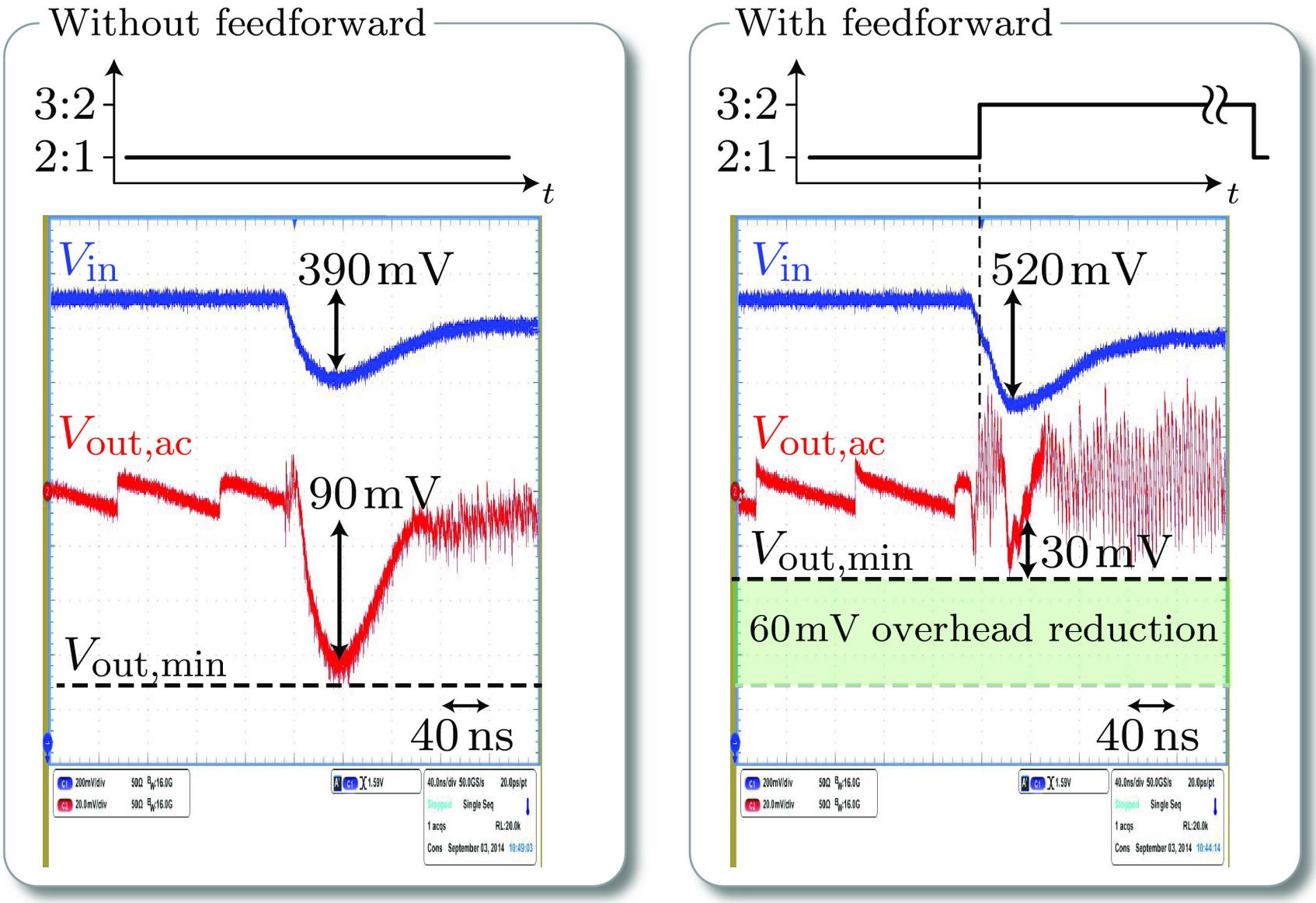
Third Chip: Overview



Implementation in 32nm SOI CMOS

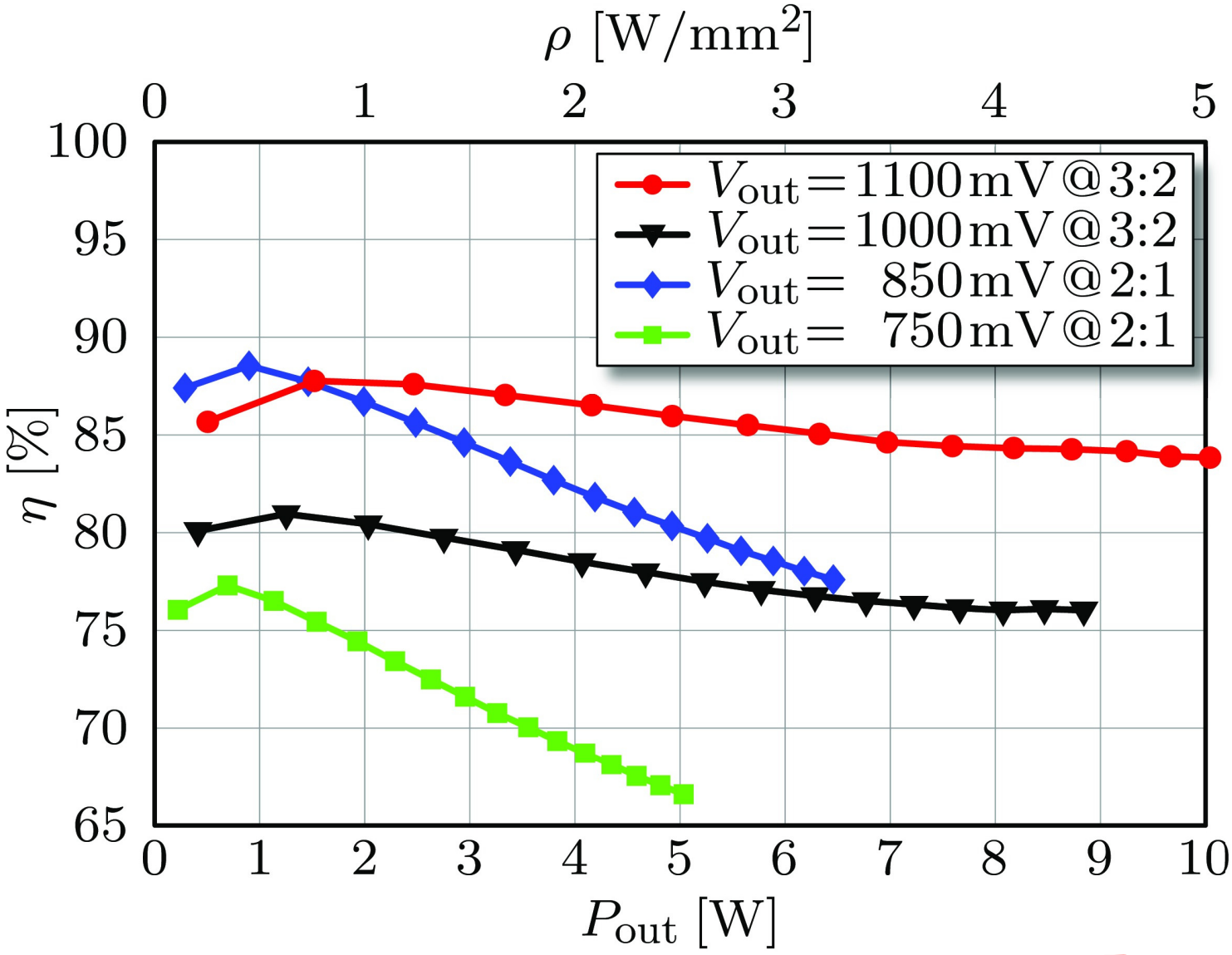


New Transient Responses



Overhead reduction → Significant system energy savings

Efficiency over Output Power



$P_{out,max} = 10W$

How did we Do?

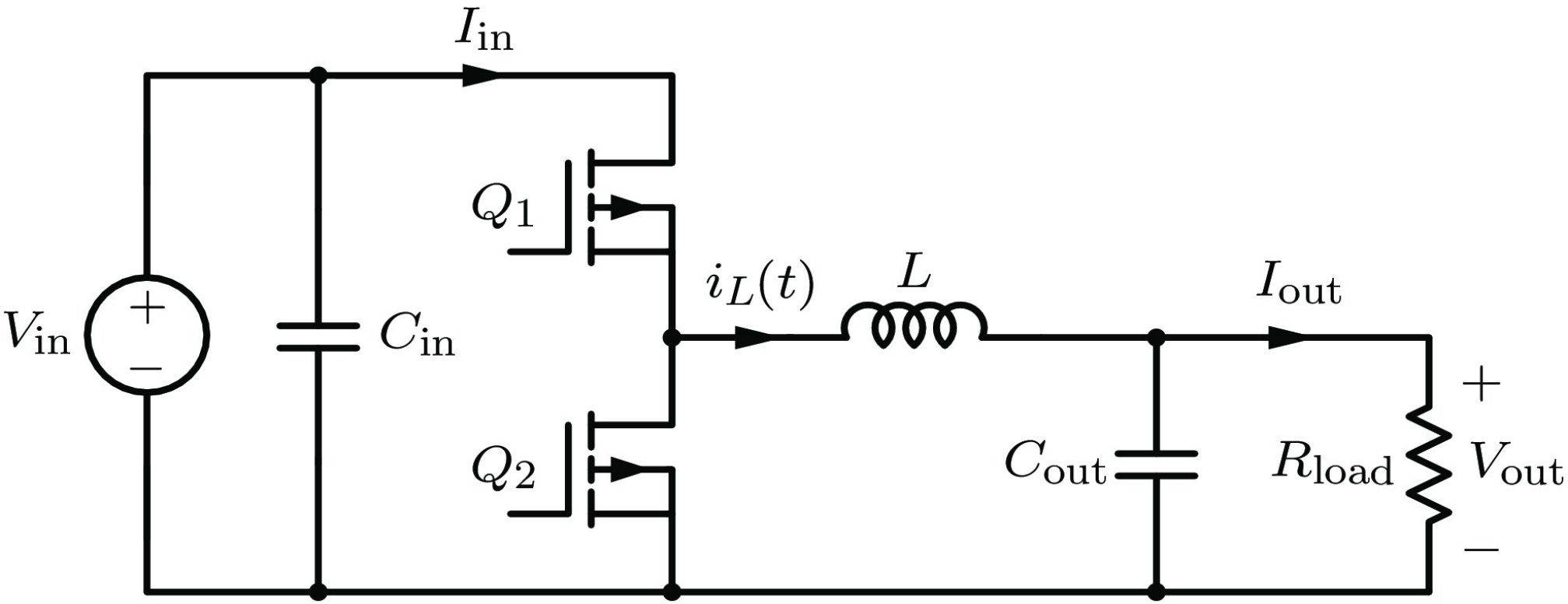
- Achieve high efficiency?
  > 85% → 85% – 88%

- Achieve high power density?
  > 1 W/mm² → Up to 5 W/mm²

- Achieve fast transient response?
  < 1 ns → < 1 ns with reduced overhead

- Achieve high output power
  > 1 W → Up to 10 W

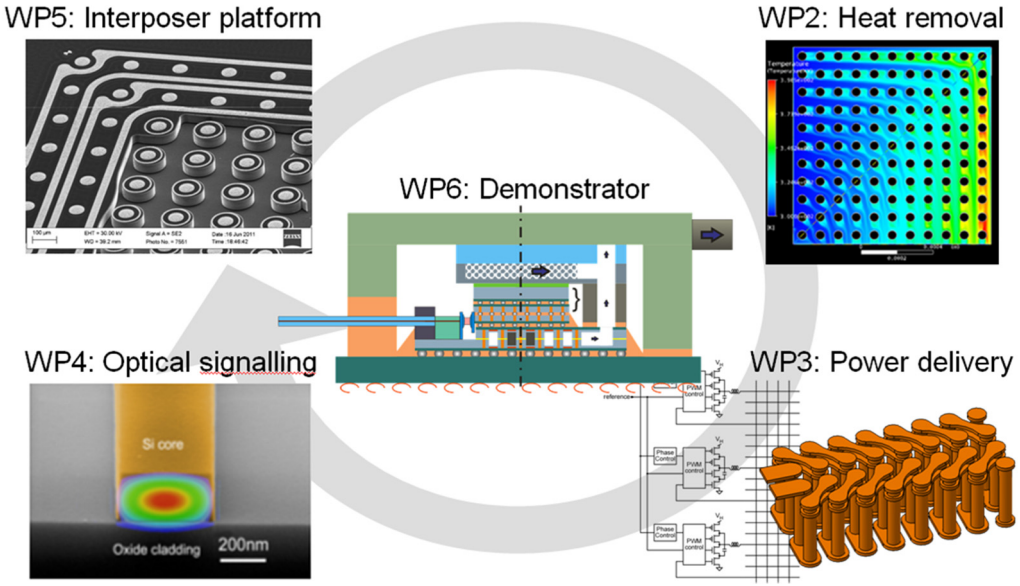
On-Chip Inductor-Based Converters



- Conventional buck converter

- Modular interposer architecture providing scalable heat removal, power delivery and communication

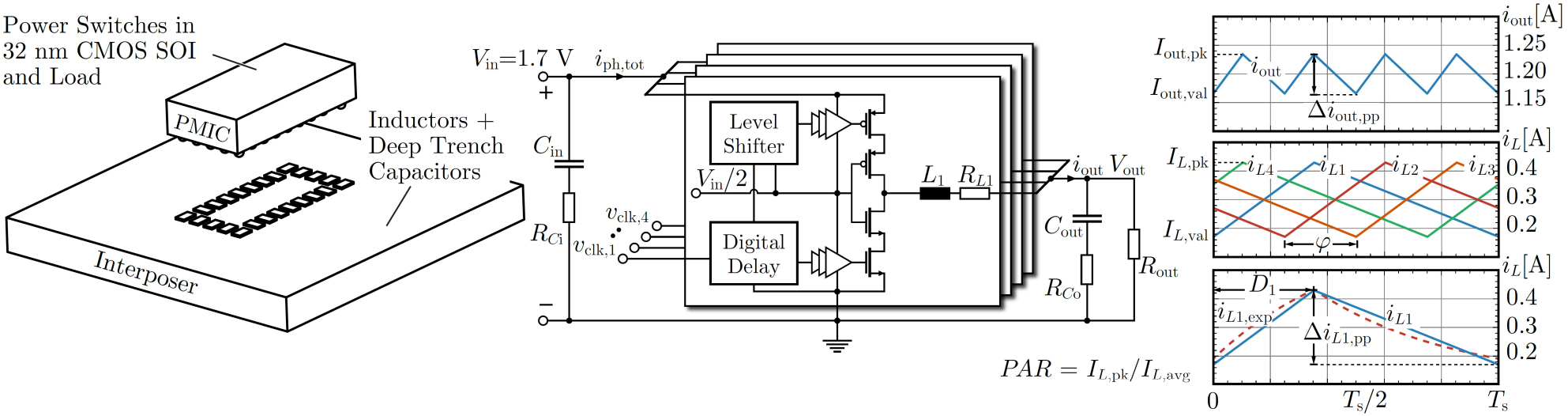
- WP3: Power delivery
  - Active die:
    - Power switches assembled in submicron technologies (32 nm)
  - Passive silicon interposer:
    - 3D TSV inductors (toroidal and helical structures)
    - High density deep-trench capacitors



- Acknowledgements:

Tyndall National Institute
ipdia
Fraunhofer IZM
optocap

Considered Converter



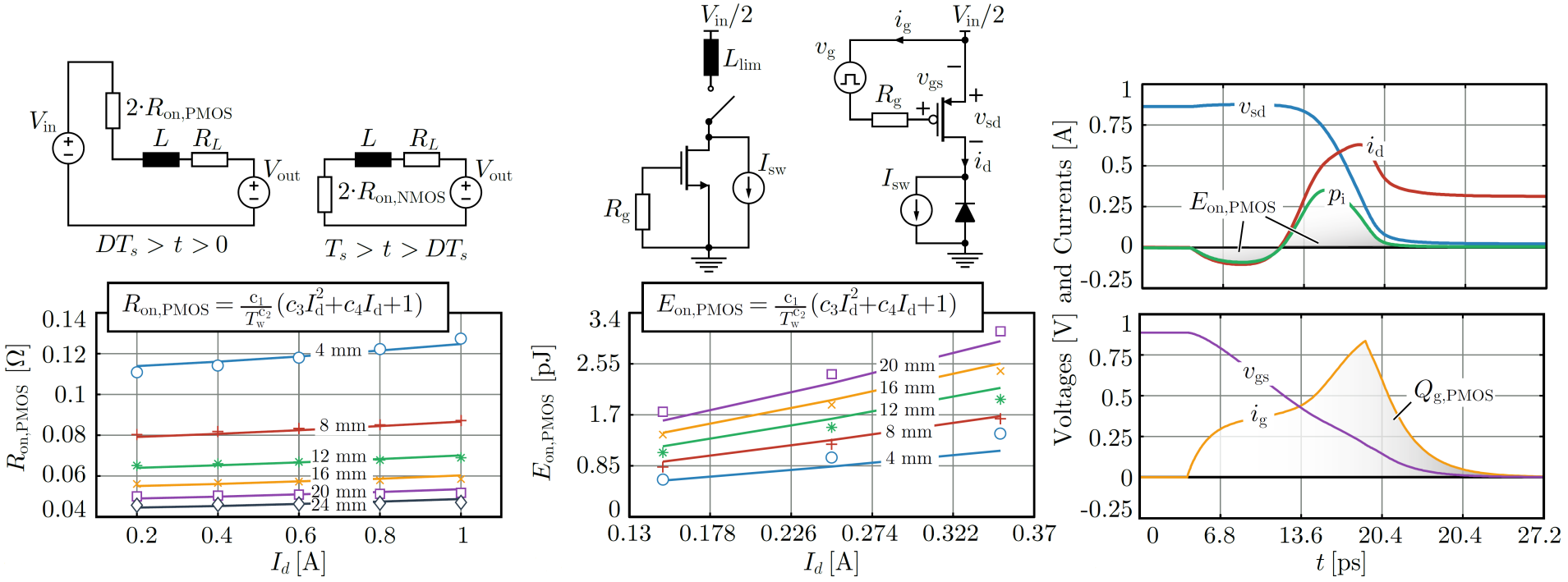
- 2.5D integration
  - Passives in a silicon interposer
- Stacked transistors
  - Support the relatively high input voltage
- Four-phase buck converter
  - For current ripple reduction

Specifications:

- V_{in} = 1.7 V
- V_{out} = 850 mV
- I_{out} = 1.18 A
- P_{out} = 1 W
- $\Delta V_{out,max}$ = 0.5% · V_{out}
- Phases = 4

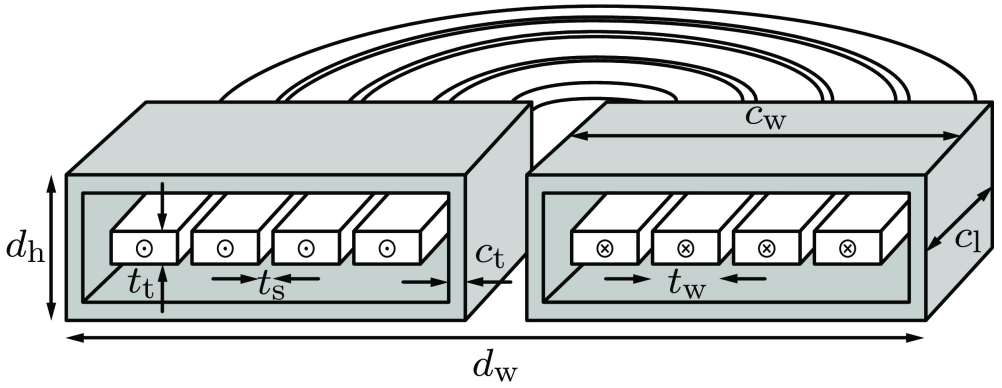
Components' Models: PMIC

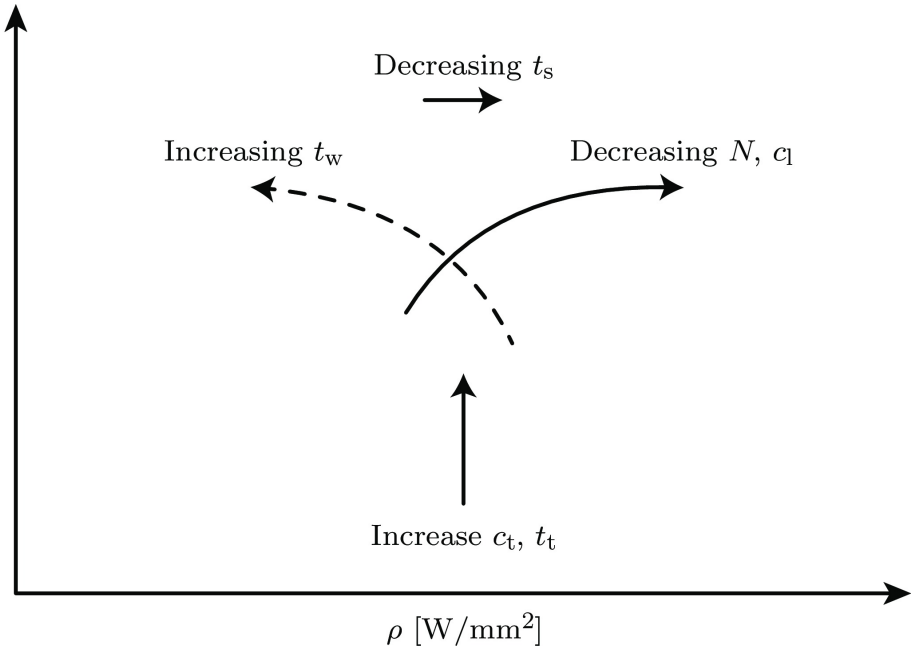
- Power Switches
  - Models extracted from cadence simulations for 32 nm CMOS SOI power switches
    - Transistor's on-state resistance
    - NMOS and PMOS gate charges
    - NMOS body diode reverse recovery charge
    - PMOS turn-on energy losses



Components' Models: Interposer

- Racetrack Inductors with Core Material
  - Thin-film with magnetic material: $Ni_{45}Fe_{55}$

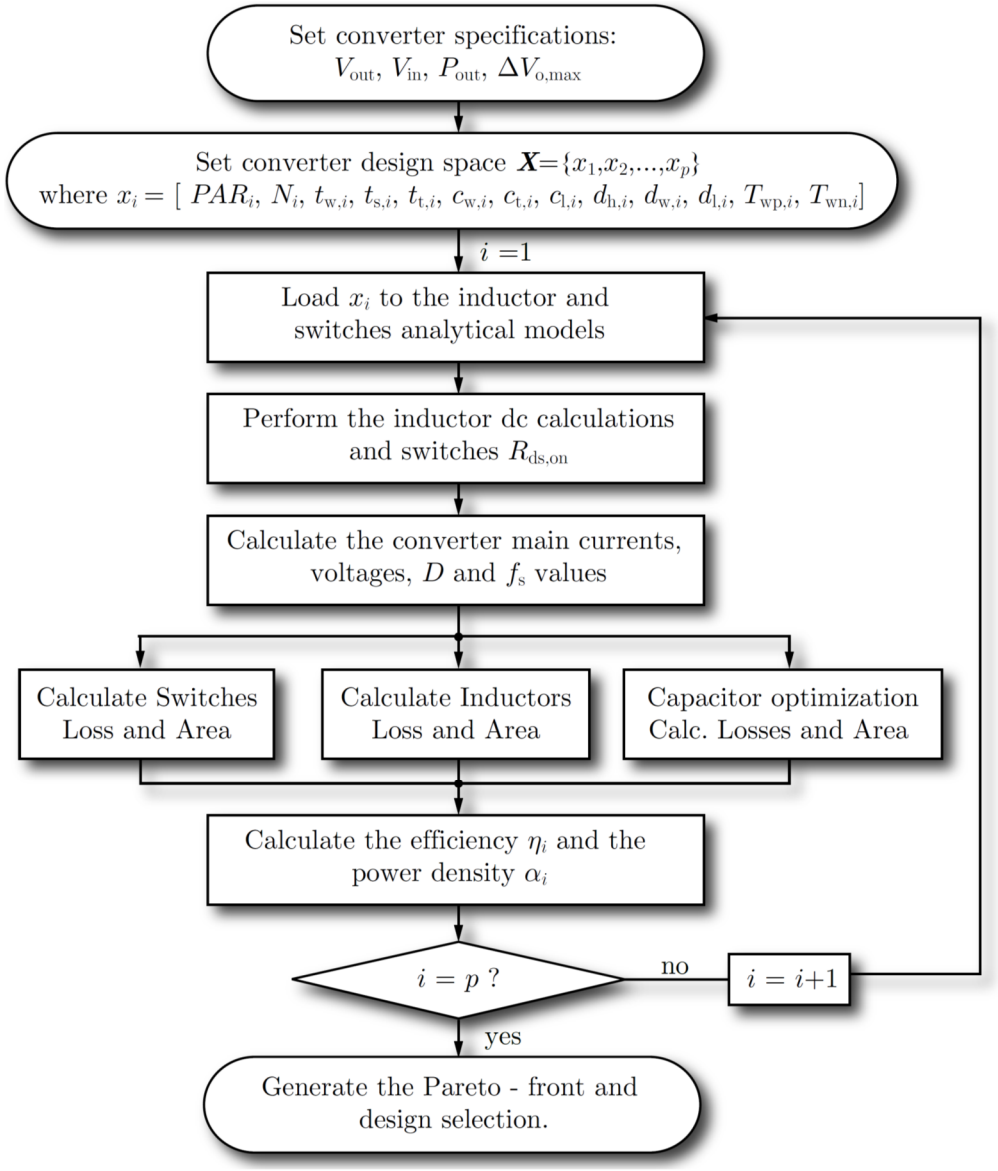




  - Loss model
    - Dc and ac copper losses
    - Eddy current and hysteresis core losses

- Output Capacitor
  - ESR vs. capacitance extracted from experimental data provided by IPDiA.

Optimization Procedure

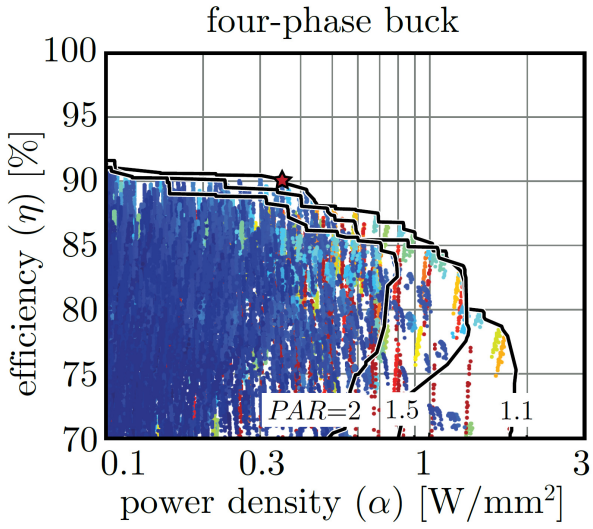


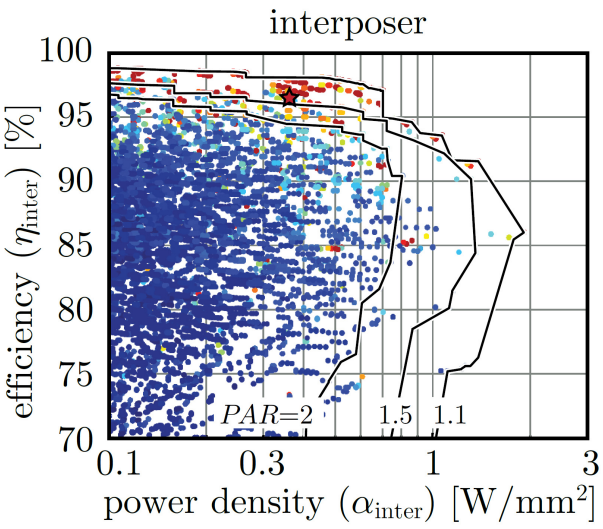
Design Space

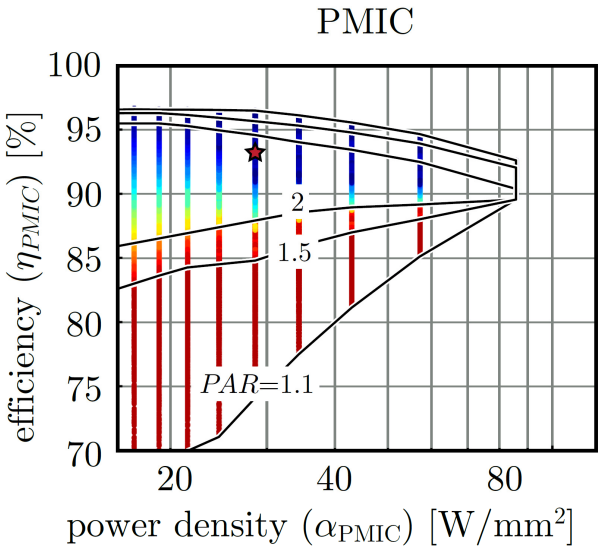
Symbol	Description	Value
PAR	Peak to average ratio	1.1, 1.5, 2
N	Number of turns	1… 8
t_w	Winding width	10… 1400 µm
t_t	Winding thickness	10… 50 µm
t_s	Winding spacing	10… 50 µm
c_t	Core thickness	1...12 µm
c_l	Core length	1... 10 mm
T_{wp}	PMOS transistor width	4… 20 mm
T_{wn}	NMOS transistor width	4… 20 mm

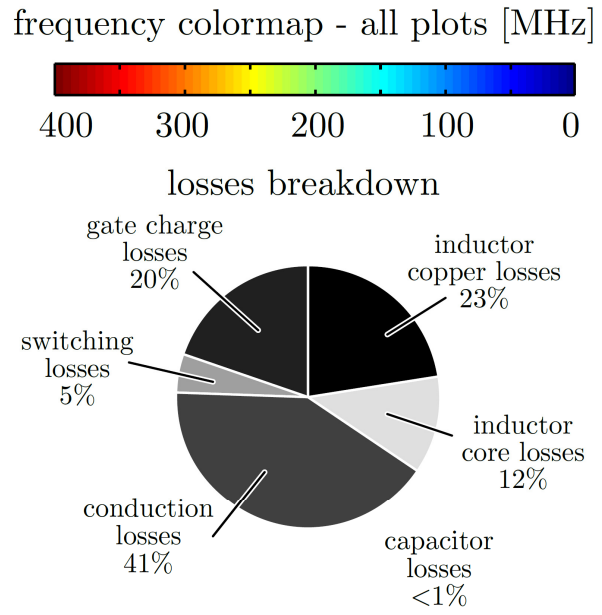
- Capacitor optimized for minimum area possible and still provide $\Delta V_{out} < \Delta V_{out,max}$
- Designs featuring $B > B_{sat}$ and PMIC loss density > 10W/mm^2 are excluded from the results

Optimization Procedure: Results









Selected Design

- f_s = 115 MHz
- L = 62 nH
- PAR = 1.1
- D = 0.52
- C_{out} = 10.3 nF
- η = 90.1%
- α = 0.351 W/mm^2
- α_{PMIC} = 28.4 W/mm^2
- α_{inter} = 0.355 W/mm^2
- T_{wp} = 12 mm
- T_{wn} = 12 mm

Summary and Conclusion

- Switched Capacitor Converters
  - Deep trench capacitors available in the 32 nm SOI CMOS or in silicon interposers are a game changer with respect to SC converters efficiency and power density.
  - The developed state-space model framework, including the bottom plate capacitor, is suitable for a Pareto optimization analysis.
  - Reconfigurable SC converter power stages efficiently widen the supported output voltage range for a fixed input supply.
  - The 10W implemented SC converter demonstrates the feasibility of the SC topology for high-power applications.
  - Experimental Achievements:
    - Efficiency: 85% – 88%
    - Chip Power Density: up to 5W/mm2
    - Output power: up to 10W
    - Fast transient response: 1ns with reduced overhead
- Inductor-Based Converters
  - For the considered topology, specifications, and components $\eta > 90\%$ and $\alpha > 1$ W/mm^2 are achievable, but not simultaneously .
  - Future analysis will investigate the converter optimization also with air-core inductors and with new TSV inductors.
  - Switching losses models will be improved to consider the ZVS switching event of the half-bridge (PMOS+NMOS).

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