ETH zürich

12 / 2020

Research Vectors in Power Electronic & Mechatronic Systems @ ETH Zurich

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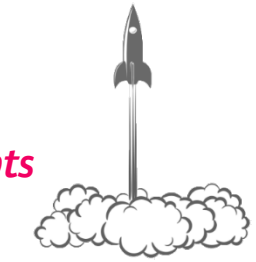
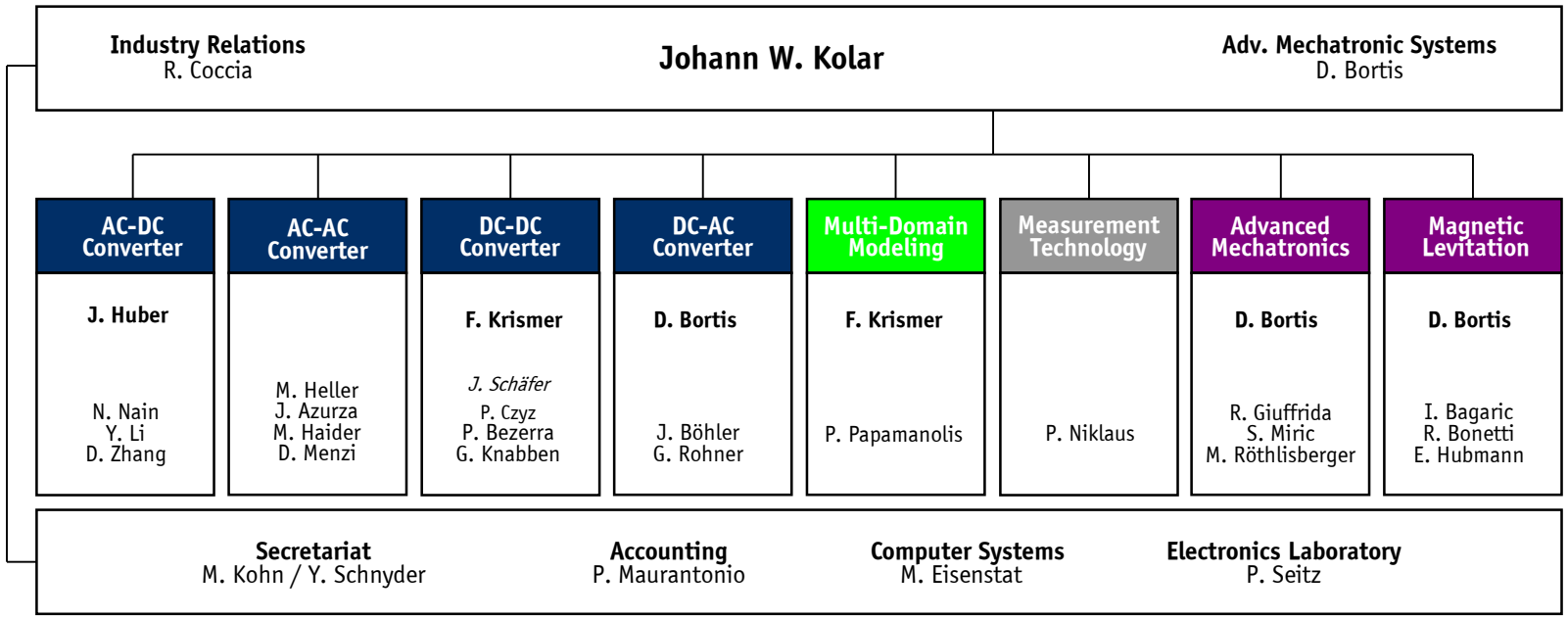
Outline

- *Introduction*
- *Performance Trends*
- *10x –Technologies / Concepts*
- *Research Results*
- *Conclusions*



Power Electronic Systems Laboratory



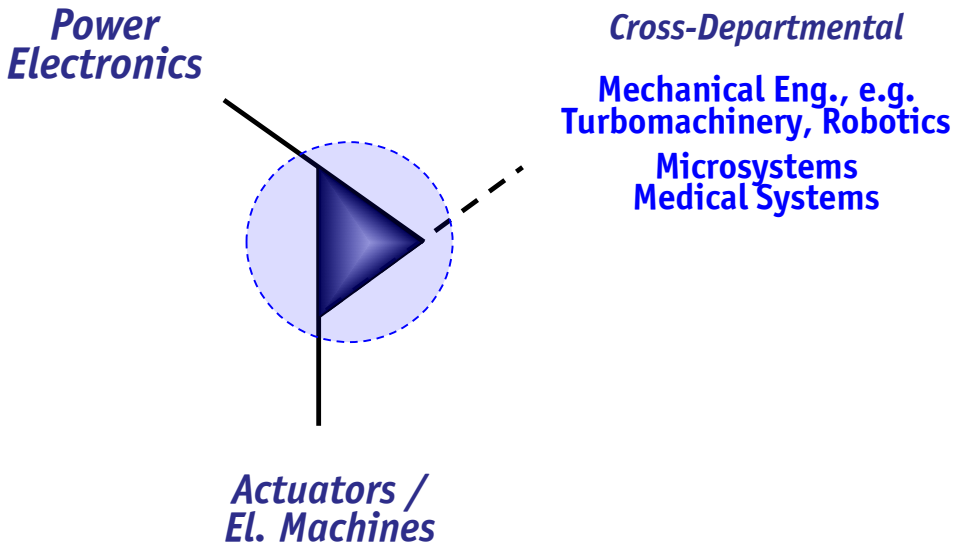
20 Ph.D. Students
1 PostDoc
3 Research Fellows

ECPE Competence Centre

EPSMA

Leading Univ. in Europe

Research Scope



- *Explore the Limits / Create New Concepts / Push the Envelope*
- *Maximize Technology Utilization*
- *Enable New Applications*

Dr. Dominik Bortis

Advanced Mechatronics

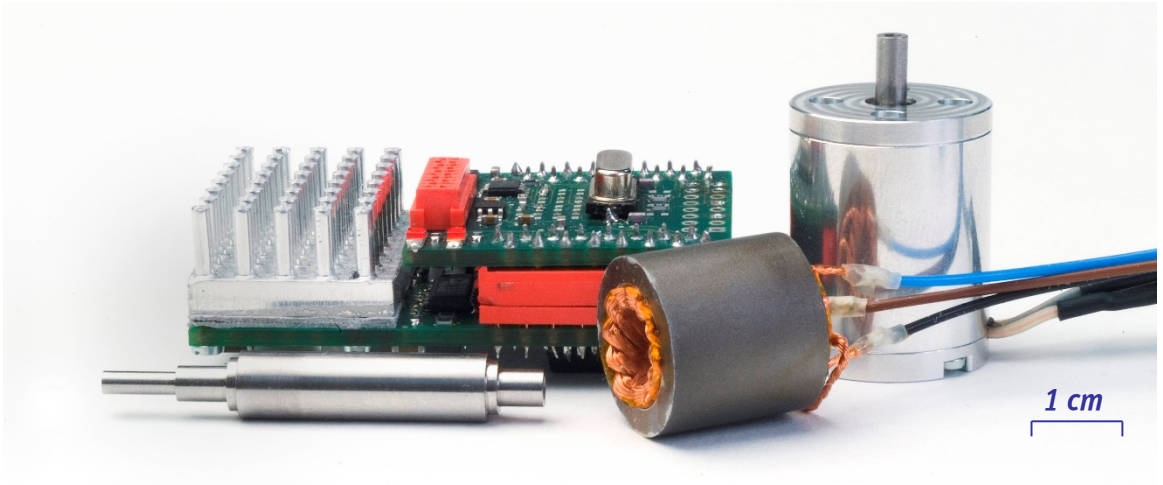
Selected Research Results

Ultra-High Speed Drive Systems

New Record !

100W @ 1‘000‘000 rpm

- µm-Scale PCB Drilling
- Dental Technology
- Laser Measurement Technology
- Turbo-Compressor Systems
- Air-to-Power
- Artificial Muscles
- Mega Gravity Science

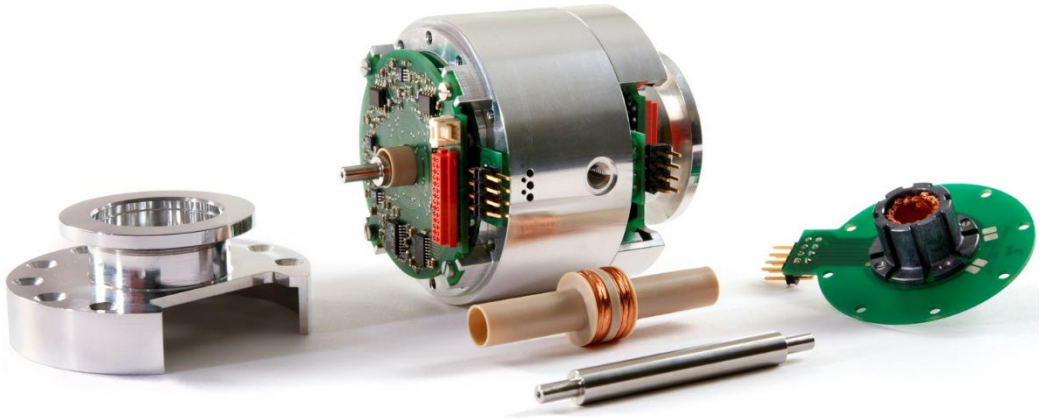


Magnetically Levitated UHS Drive Systems

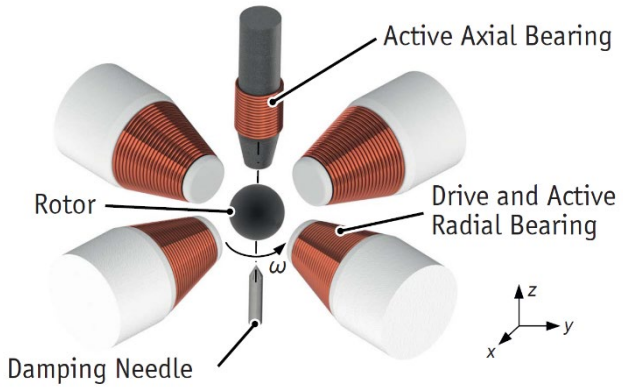
- Laser Measurement Technology
- Active Damping of Air Bearings
- Satellite Attitude Control

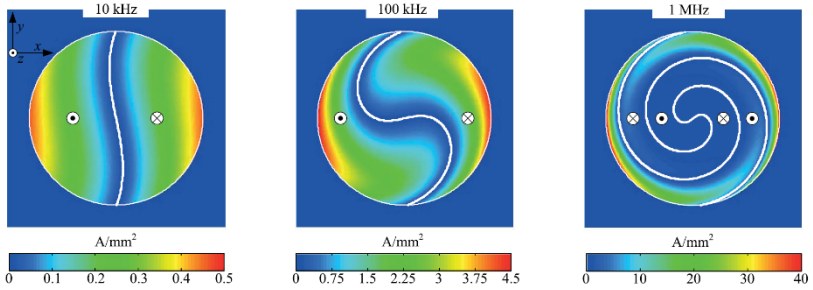
New Record !

500'000 rpm



Highest Rotational Speeds



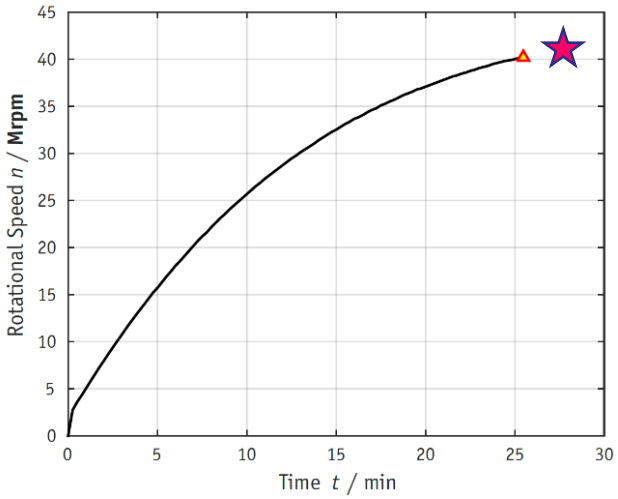


- *Highest Rotational Speed Ever Achieved*
- *Sub-Millimeter Rotors*
- *Magnetic Levitation in Vacuum*
- *Mega Gravity Science (10^8g)*
- *Materials Research*

World Record !

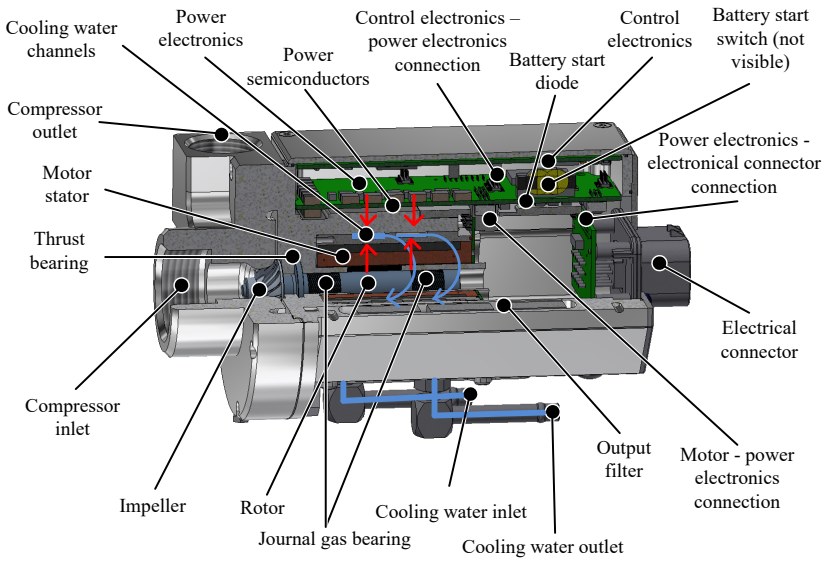
40'260'000 rpm

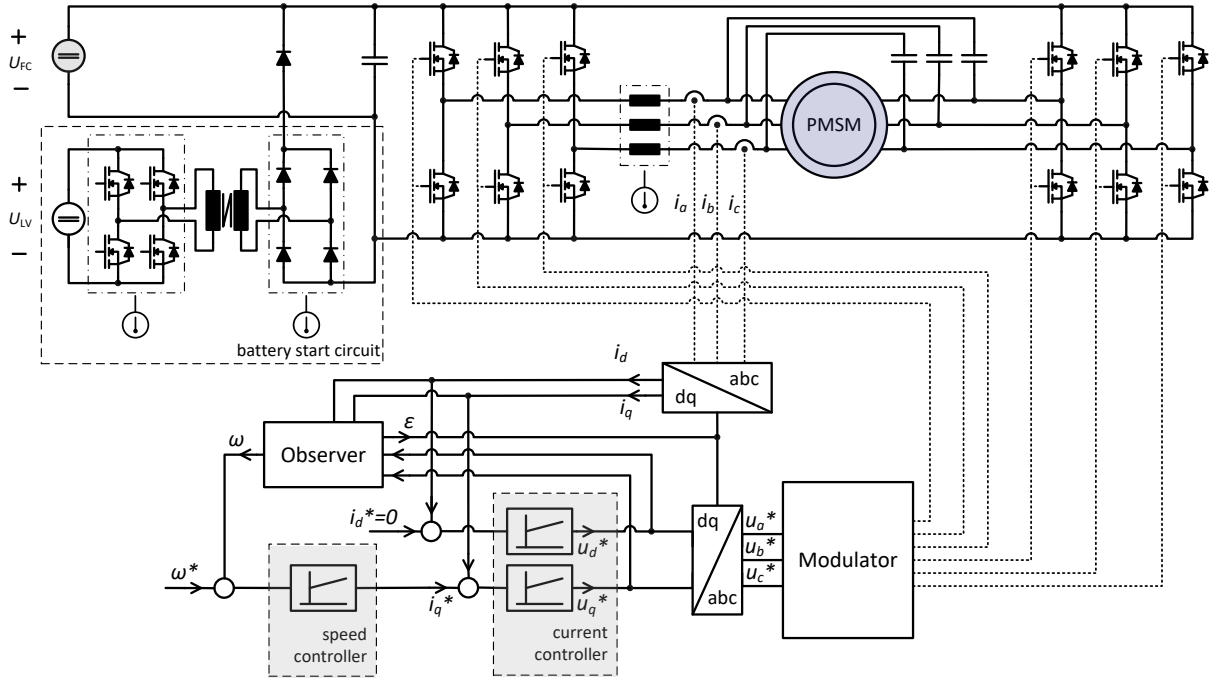
Circumferential Speed > 3000 km/h



Turbo Compressor-Integrated GaN-Inverter

- *E-Mobility 5...15kW Fuel Cell Pressurized Air Supply*
- *1kW Rated Power, f_{sw}=300kHz | n= 280'000rpm / f_{out}= 4.6kHz*
- *Low EMI / Low Cabling Effort*



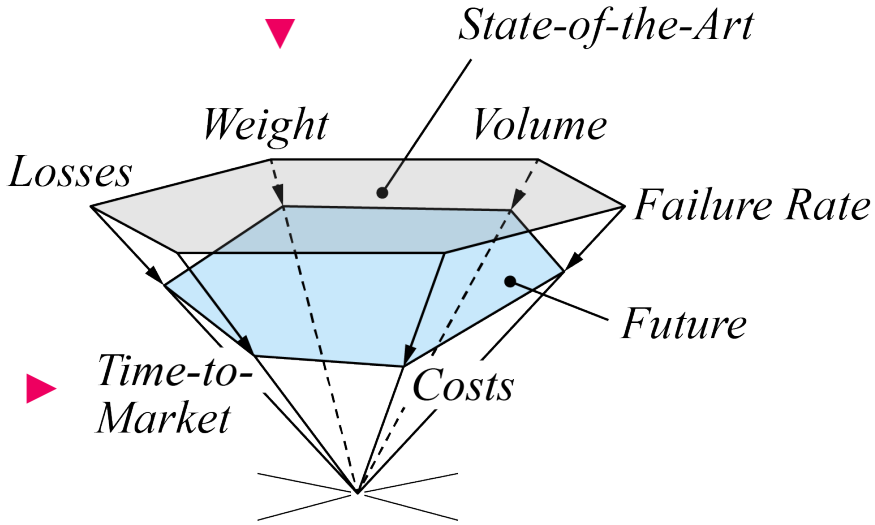


- *Integration → 2x System Power Density | 97% → 98.5% Inverter Efficiency*

Power Electronics
Research Topics / Results

Required Performance Improvements

Environmental Impact... **[kg_{Fe} /kW]**
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

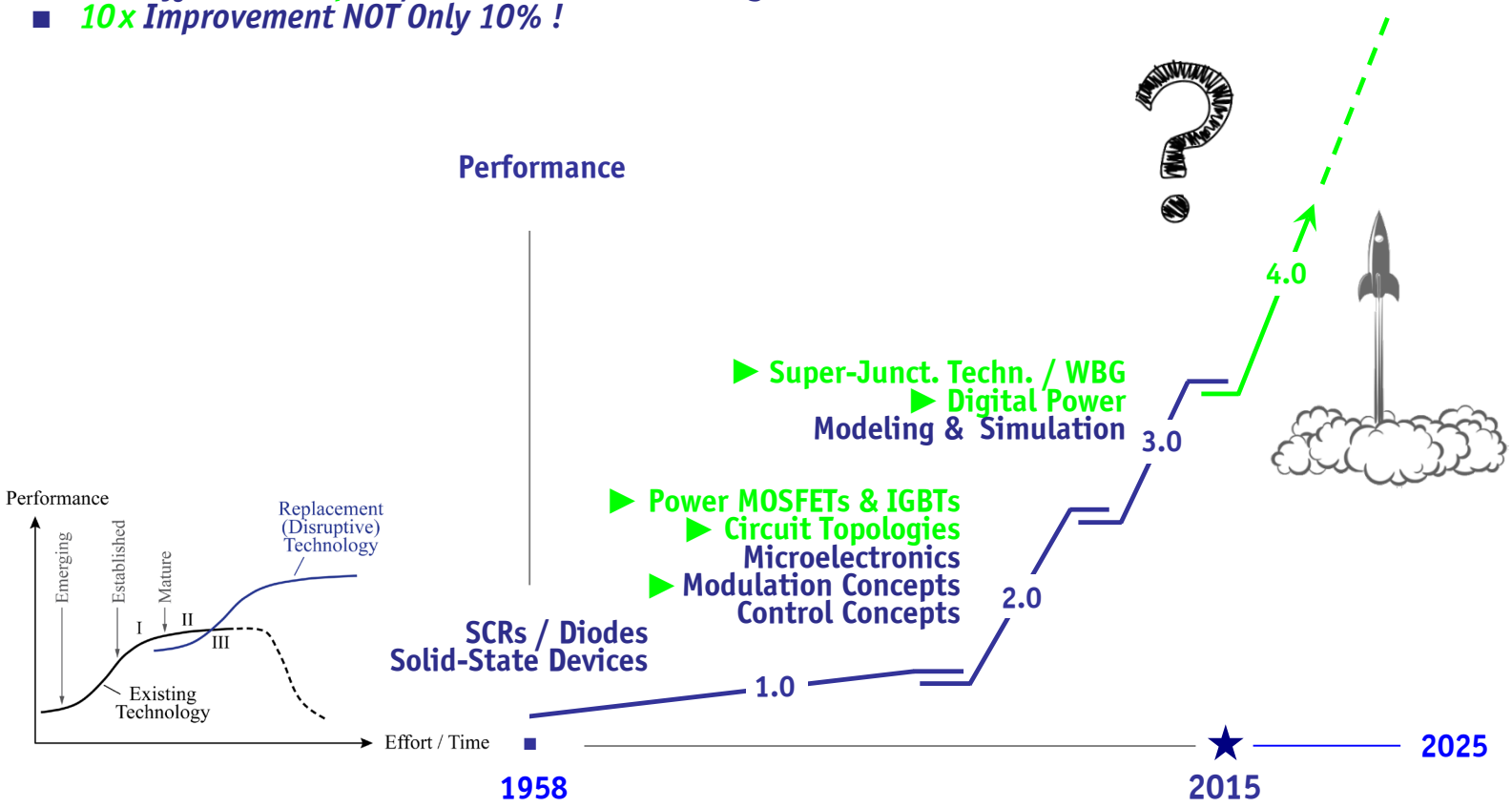


- Power Density [kW/dm^3]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]

- ***Connected Intelligent Power Electronic Systems → Power Electronics 4.0***

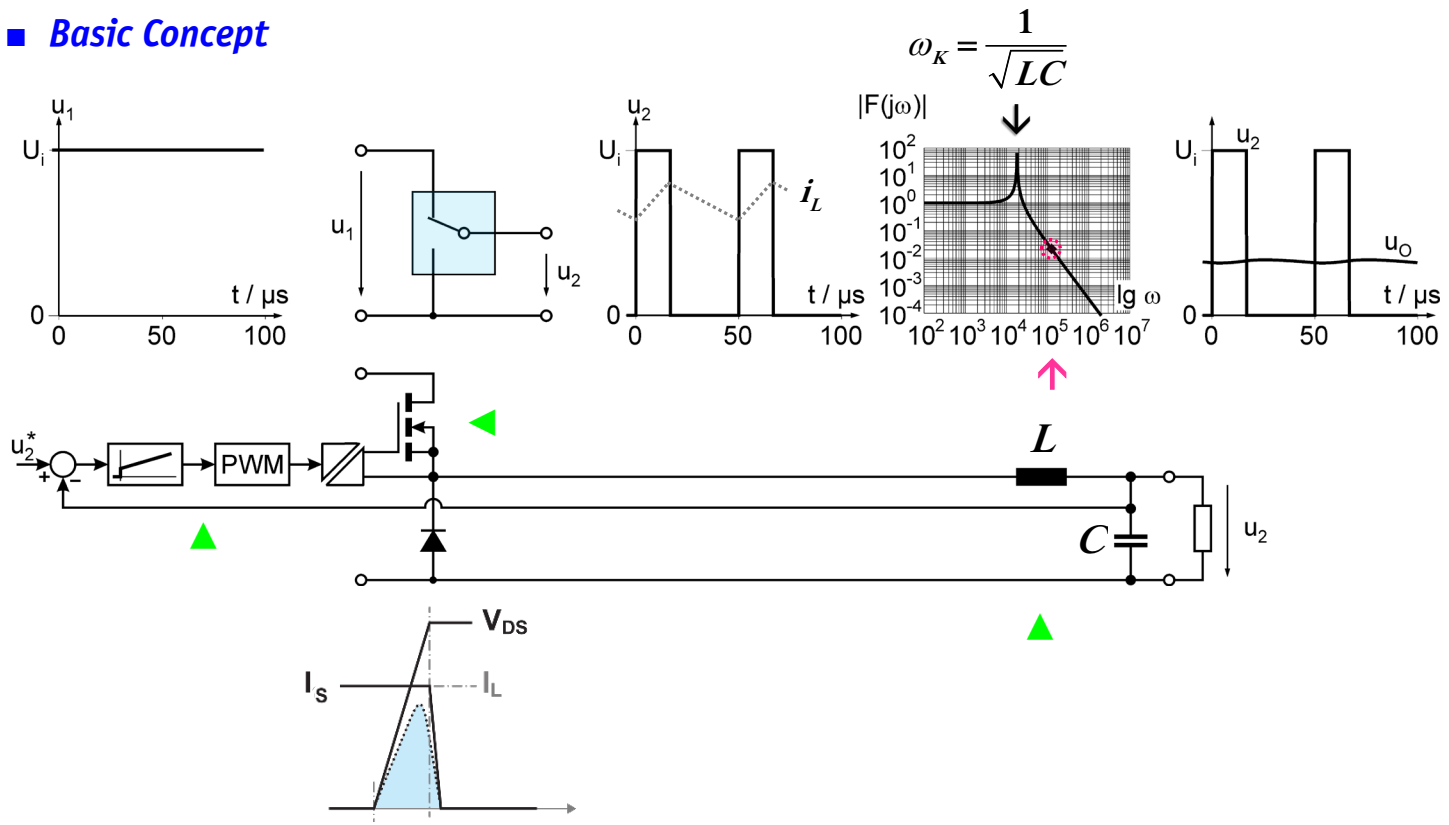
S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*



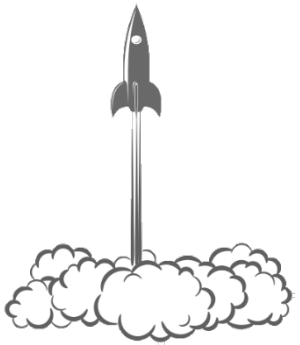
Pulse-Width-Modulated Converters

- *Basic Concept*



- Switch-Mode Voltage Formation and Subsequent Filtering
- *Higher Sw. Frequency → Smaller Filter Components (Limited by Sw. Losses, Signal Processing etc.)*

X-Technology #1



Wide Bandgap Power Semiconductors

Low $R_{DS(on)}$ High-Voltage Devices

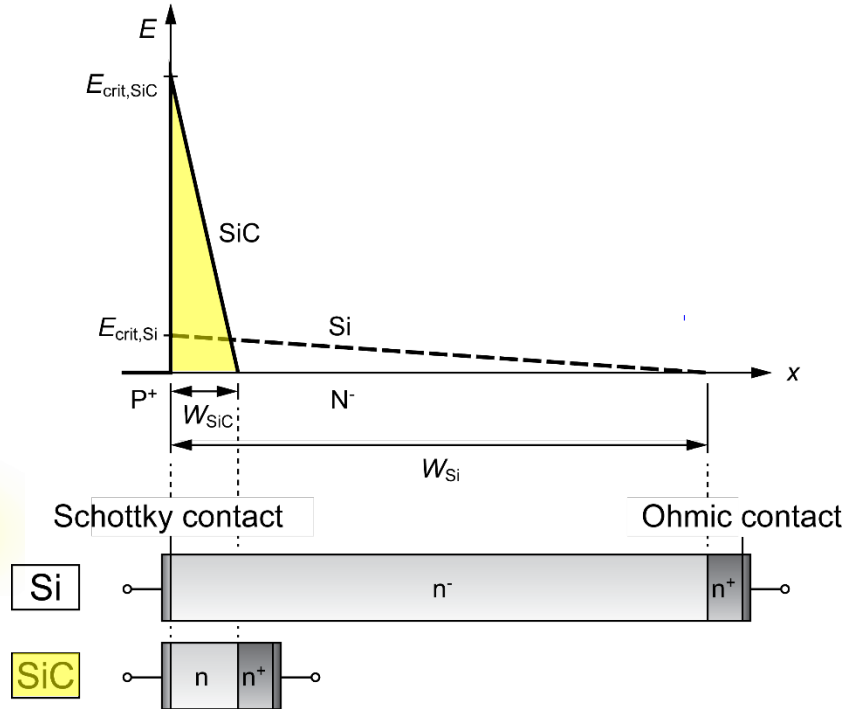
- *Higher Critical E-Field of SiC → Thinner Drift Layer*
- *Higher Maximum Junction Temperature $T_{j,max}$*

at 300 K	Si	GaAs	4H/6H-SiC	GaN
Eg (eV)	1.12	1.4	3.0-3.2	3.4
Ec (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm^2/Vs)	1350	8500	100-1000	1000
ε_r	11.9	13	10	9.5
Vsat (cm/s)	$1x10^7$	$1x10^7$	$2x10^7$	$3x10^7$
λ (W/cmK)	1.5	0.5	3 - 5	1.3

$$R_{on}^{*} = \frac{4 V_B^2}{\varepsilon \mu_n E_C^3} \leftarrow$$

For 1kV:	Si	SiC
W (μm)	100	10
N_D (cm^{-3})	10^{14}	10^{16}

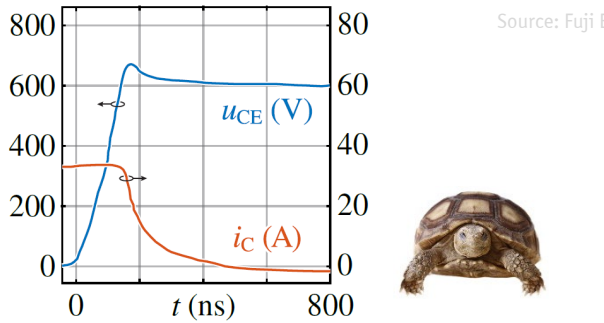
$$R_{on,SiC}^{*} \approx \frac{1}{300} R_{on,Si}^{*}$$



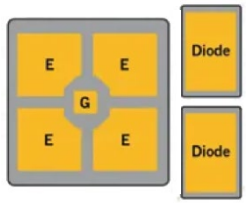
- *Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices*

Si vs. SiC Switching Behavior

- *Si-IGBT → Const. On-State Voltage Drop / Rel. Low Switching Speed,*
- *SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed*

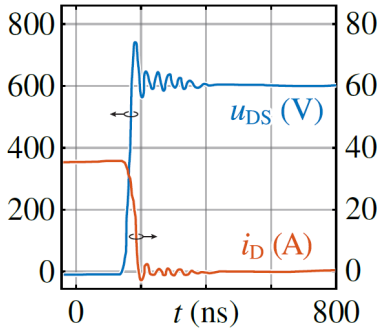


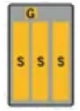
Source: Fuji Electric



1200V 100A
Die Size: 98.8mm² + 39.4mm²

Source: Infineon



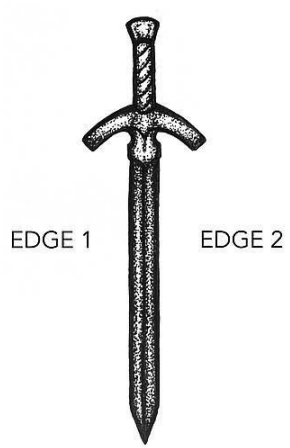


1200V 100A
Die Size: 25.6mm²

Source: Cree

- *Extremely High di/dt & dv/dt → Challenges in Packaging / EMI / Motor Insulation*

Challenges

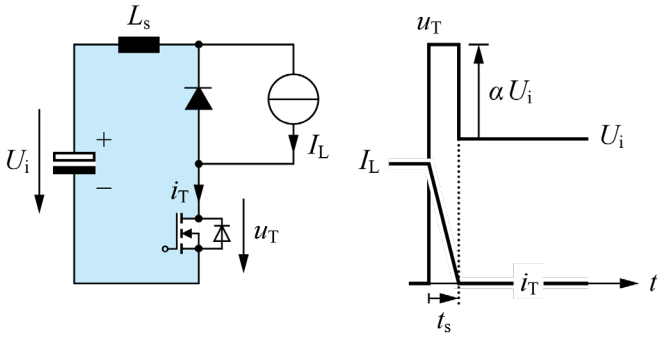


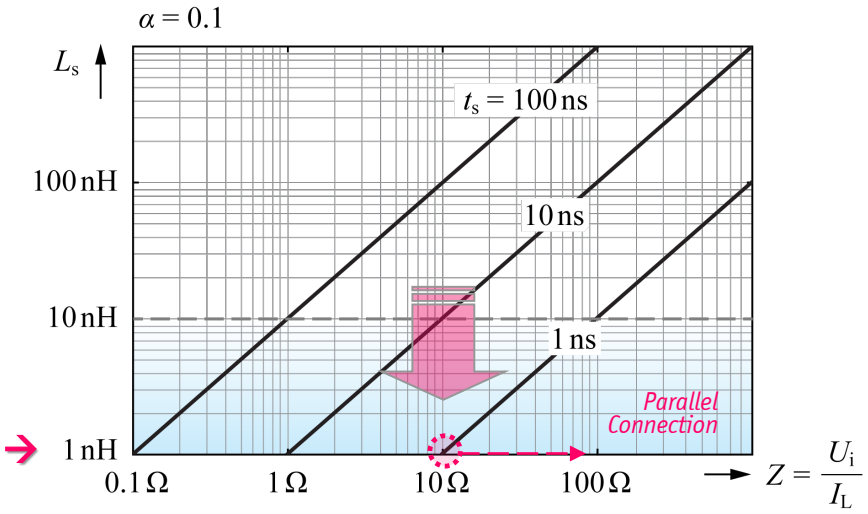
Circuit Parasitics

- *Extremely High di/dt*
- *Commutation Loop Inductance L_S*
- Allowed L_s Directly Related to Switching Time t_s →

$$L\frac{di}{dt} = u$$

$$L_s \le \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \underbrace{\frac{U_i}{I_L}}_{Z}$$



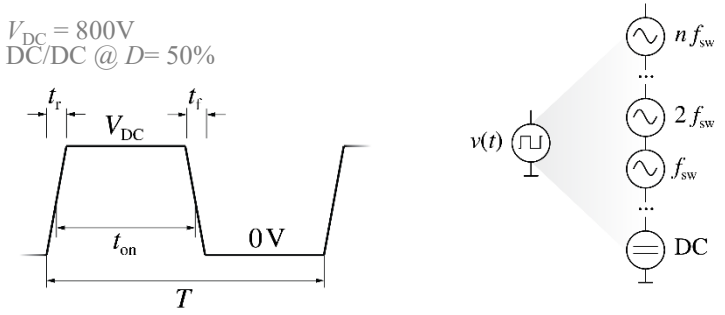


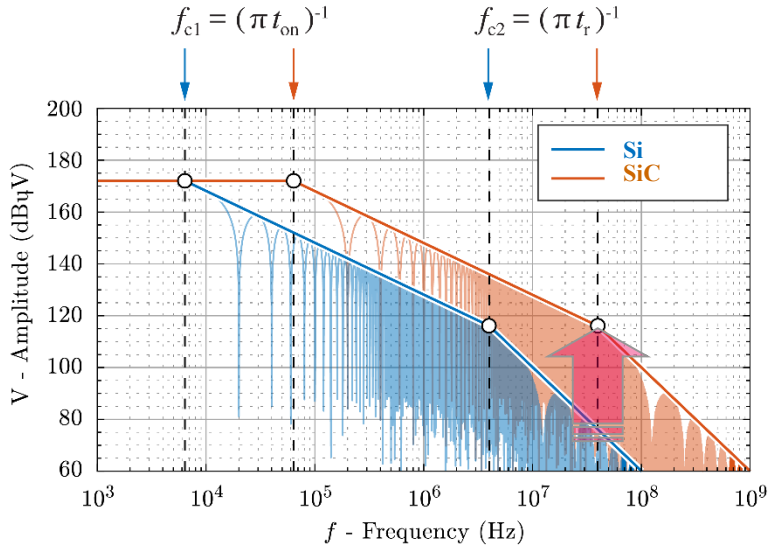
- *Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents*

Si vs. SiC EMI Emissions

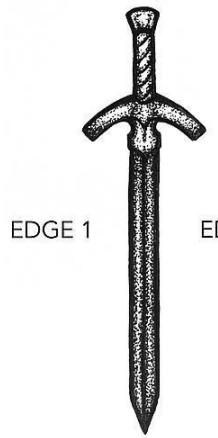
- Higher dv/dt → Factor 10
- Higher Switching Frequencies → Factor 10
- EMI Envelope Shifted to Higher Frequencies

f_S= 10kHz & 5 kV/us for (Si IGBT)
f_S= 100kHz & 50 kV/us for (SiC MOSFET)





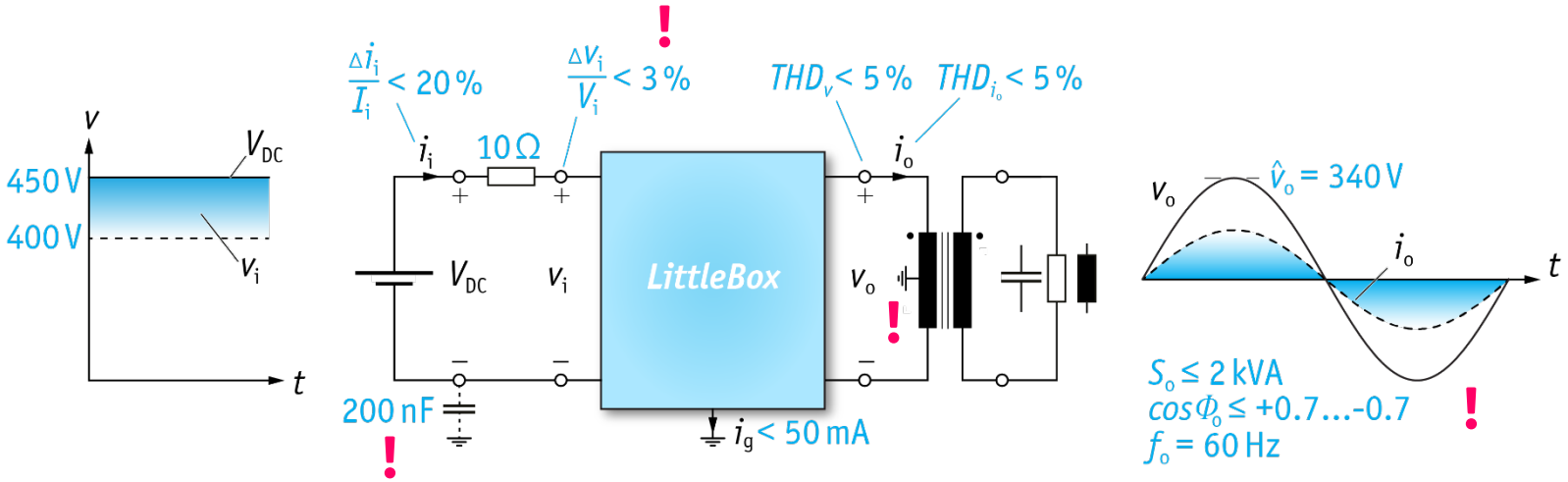
- Higher Influence of Filter Component Parasitics & Couplings → Advanced Design



LiTTLE BOX CHALLENGE

Google | IEEE

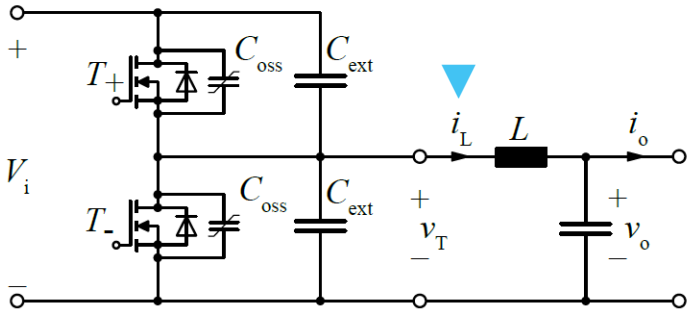
- *Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World*
- *Power Density > 50W/in³ (3kW/dm³)*
- *Efficiency > 95%*
- *Case Temp. < 60°C*
- *EMI FCC Part 15 B*

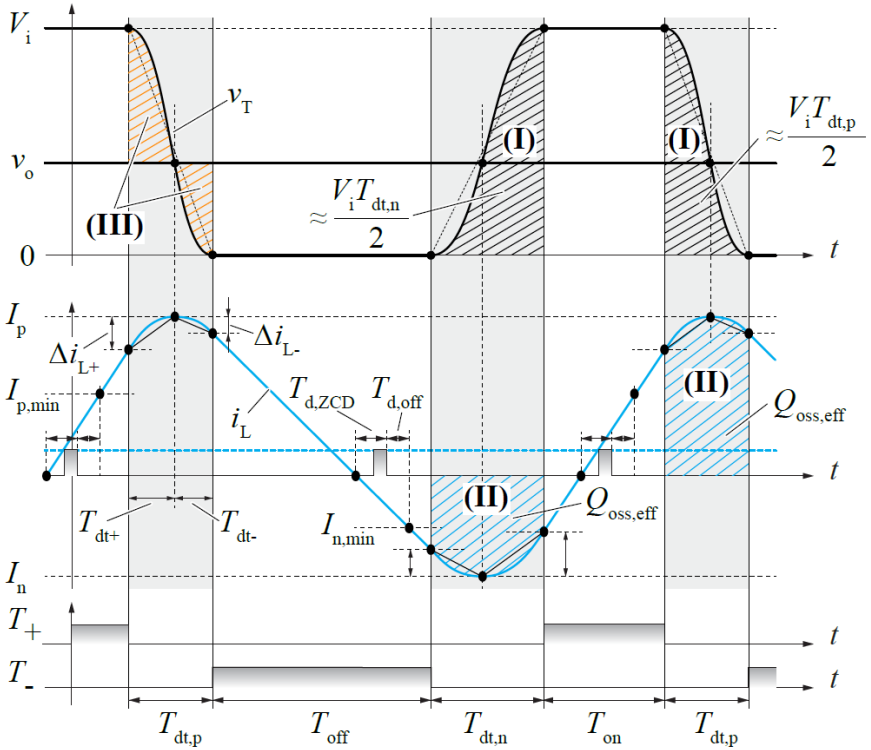


- *Push the Forefront of New Technologies (!)*

ZVS/TCM & Full Digital Control @ f_S > 1MHz

- ZVS Dead Times & Gate Drive Time Delays
- i = 0 Detection Time Delay
- Control of Interleaving

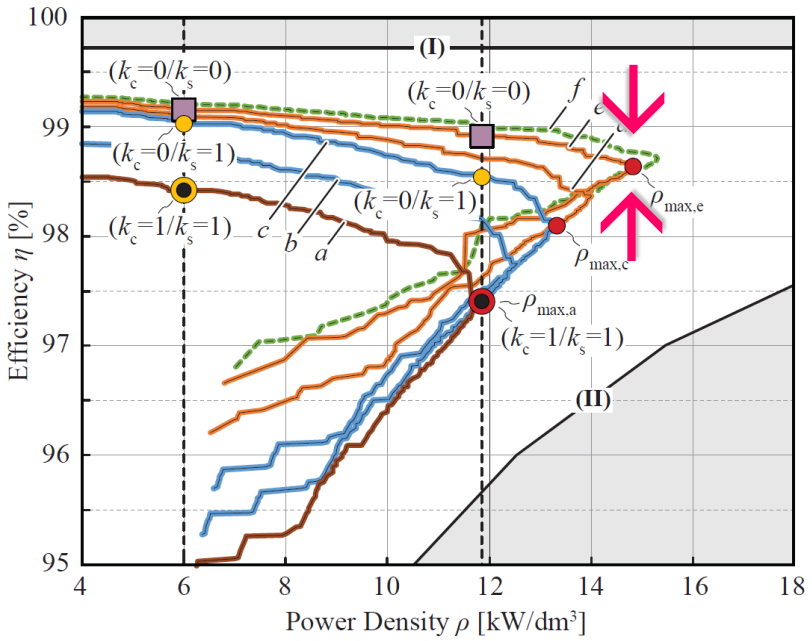




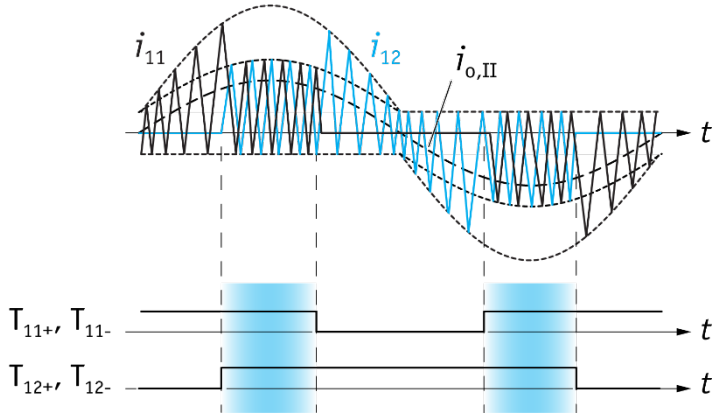
- Novel 4D-Interleaving ZVS / TCM Concept
- Novel High-Speed / Isolated i = 0 Detection Concept

Multi-Objective Optimization

- *Multi-Objective Optimization of Little-Box 1.0 & 2.0*
- *Step-by-Step Idealization of the Power Transistors*
- *Ideal Switches: k_c= 0 (Zero Cond. Losses); k_s= 0 (Zero Sw. Losses)*



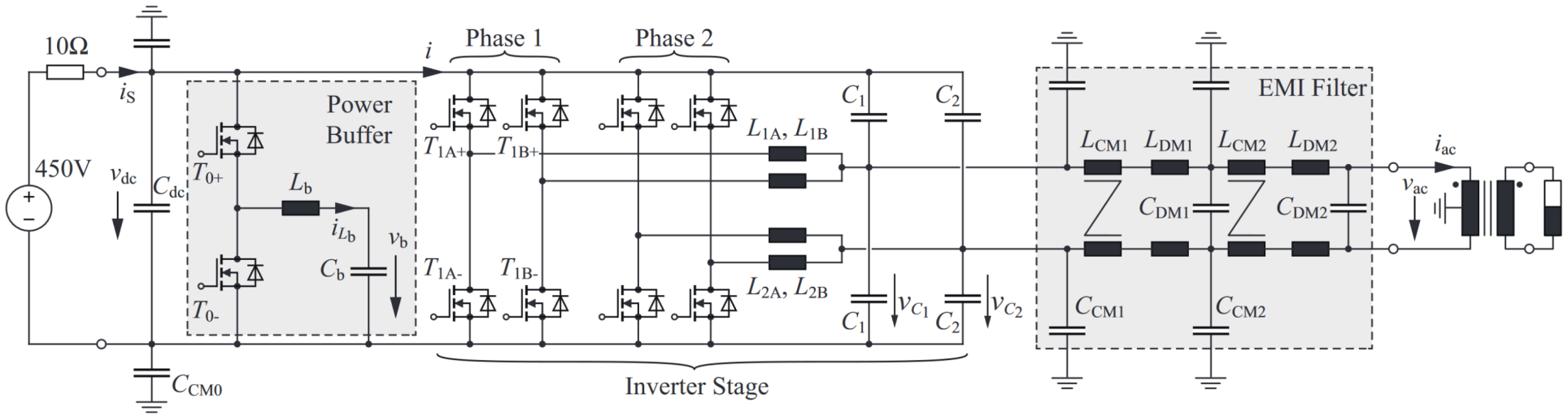
- 4D-Interleaving Considered for TCM



- *ρ= 250W/in³ (15kW/dm³) @ η= 98% Efficiency Achievable for Full Optimization*

Little-Box 1.0 Topology

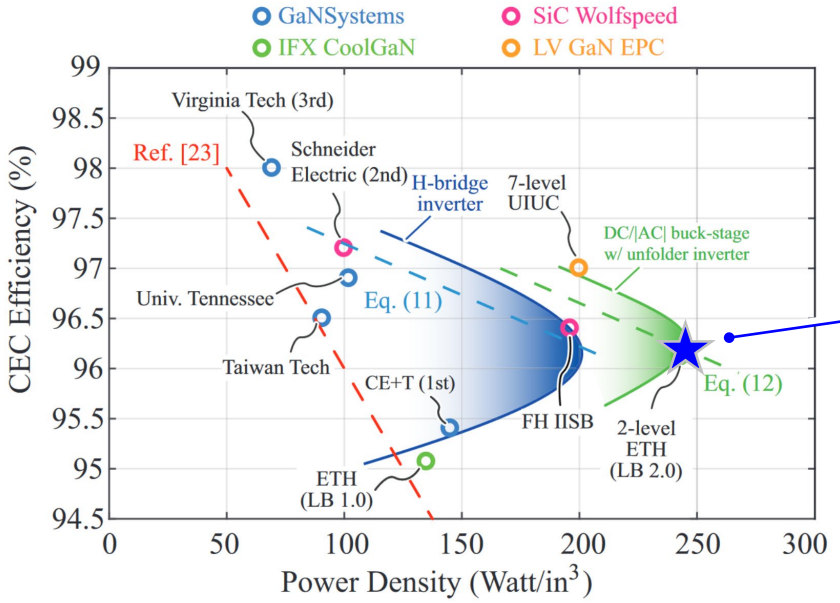
- *Active DC-Side Buck-Type Power Pulsation Buffer*
- *Interleaving of 2 Bridge-Legs per Phase*
- *2-Stage EMI AC Output Filter*



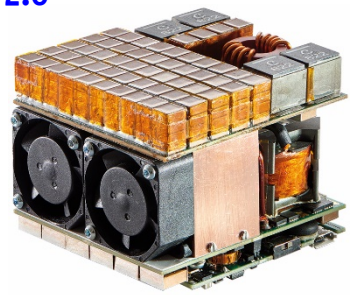
- *ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)*

Performance Comparison of the Finalists

- *SiC or GaN / Sw. Frequencies up to 1MHz*
- *ZVS / ZVS-TCM / Hard Switching Approaches*
- *Two-Level and Multi-Level Bridge-Legs*
- *Parallel or Series Active Power Buffers*

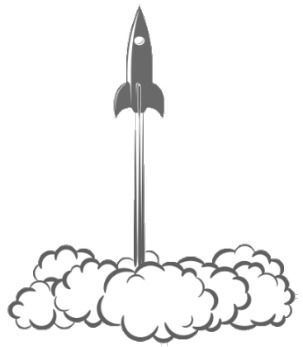


ETH zürich
Little-Box 2.0
240 W/in³
97.4%



- *2 Categories of Solutions Dependent on CM Requirements*

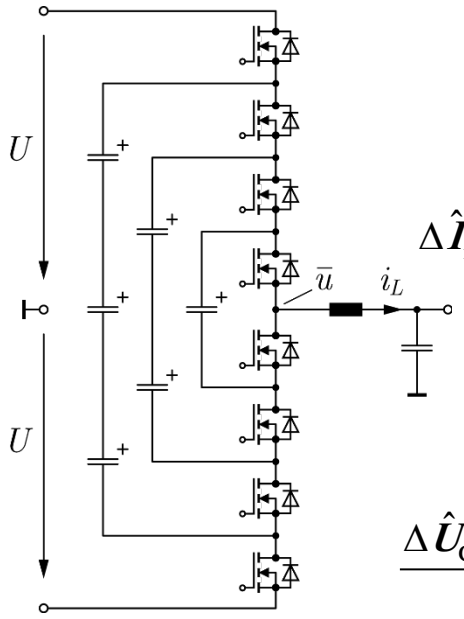
X-Technology #2



Multi-Level / Cell Converters & Modularity

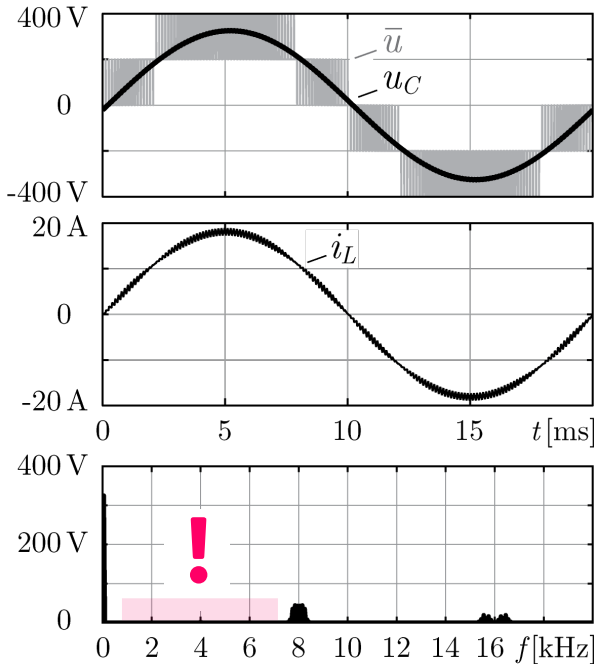
Multi-Level Bridge-Leg Concepts / Scaling

- *Reduced Ripple @ Same (!) Switching Losses*
- *Lower Overall On-Resistance @ Given Blocking Voltage → 1+1=2 NOT $2^2 = 4$ (!)*
- *Application of LV Technology to HV*



$$\Delta\hat{I}_{\max,N} = \frac{1}{N^2}\Delta\hat{I}_{\max,N=1} \quad \Big/ \quad \frac{U}{8 f_s L}$$

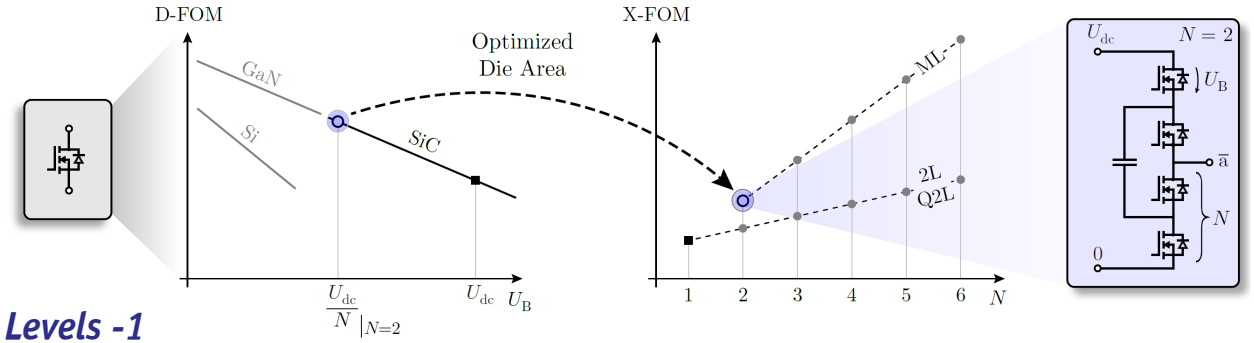
$$\frac{\Delta\hat{U}_{C,\max,N}}{U} = \frac{\pi^2}{32}\left(\frac{f_o}{f_s}\right)^2 \frac{1}{N^3}$$



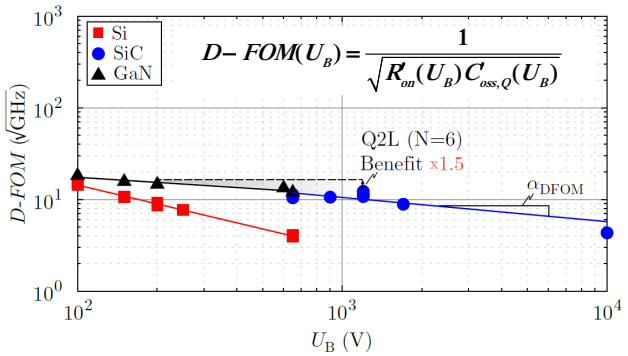
- *Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy*

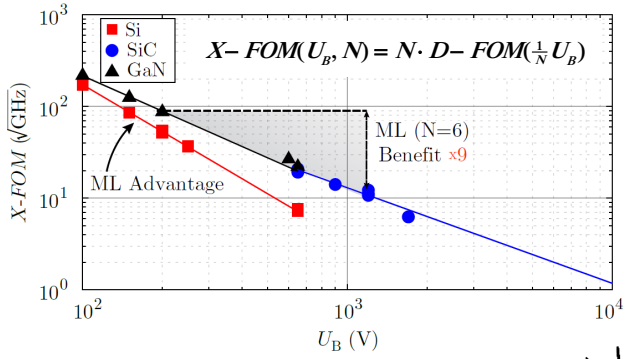
X-FOM of Multi-Level Bridge-Legs

- *Quantifies Bridge-Leg Performance of N-Level FC Converters*
- *Identifies Max. Achievable Efficiency & Loss Opt. Chip Area @ Given Sw. Frequ.*



N= # of Levels -1

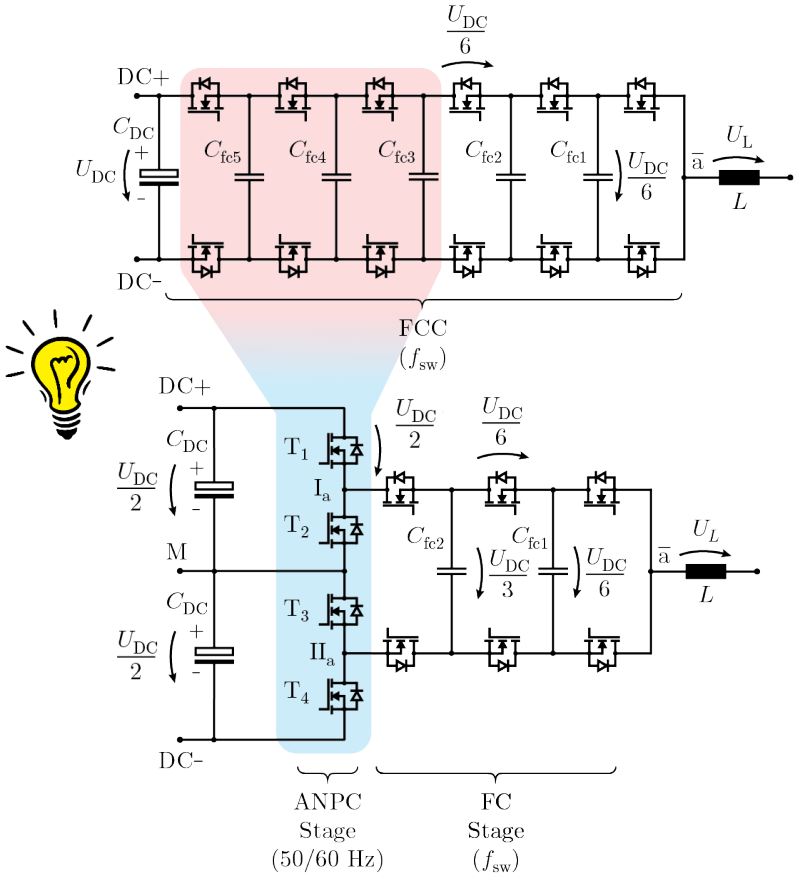


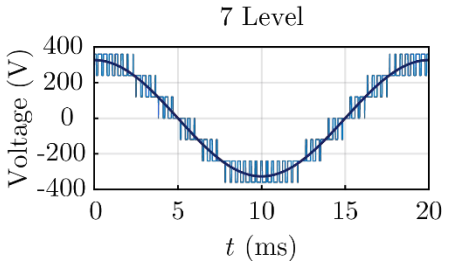


- *Compared to 2-Level Benchmark @ Same Filter Ind. Volt-Seconds* → $P_{semi,min,ML} \approx 1/N^{1.2} P_{semi,min,2L}$, $A_{chip,ML} \approx N^{1.2} A_{chip,2L}$

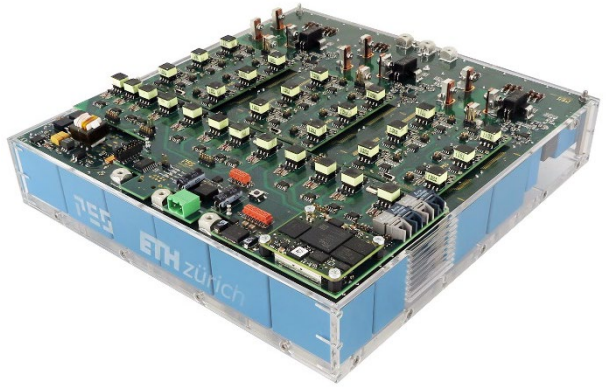
3-Φ Hybrid Multi-Level Inverter Demonstrator

- Realization of a 99%++ Efficient 10kW 3-Φ $400V_{rms,ll}$ Inverter System
- 7-Level Hybrid Active NPC Topology / LV Si-Technology





99.35%
2.6kW/kg
56 W/in³

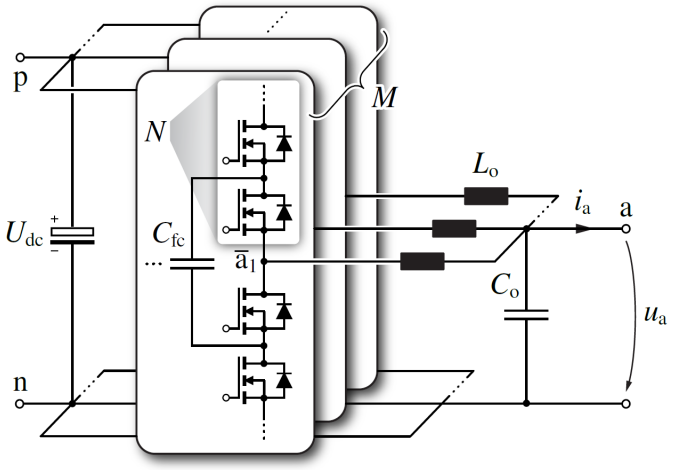


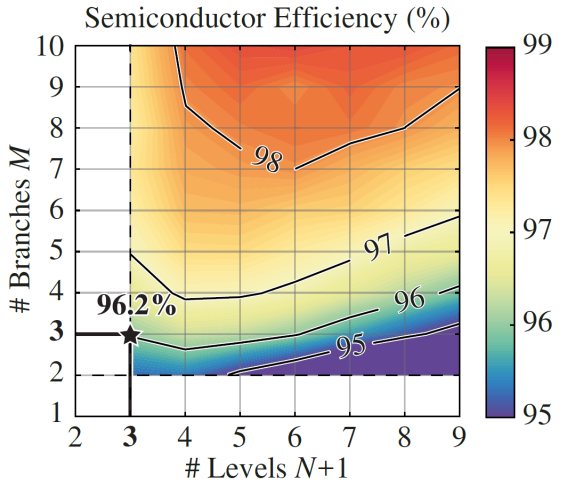
- 200V Si → 200V GaN Technology Results in 99.5% Efficiency

4.8MHz GaN Half-Bridge Phase Module

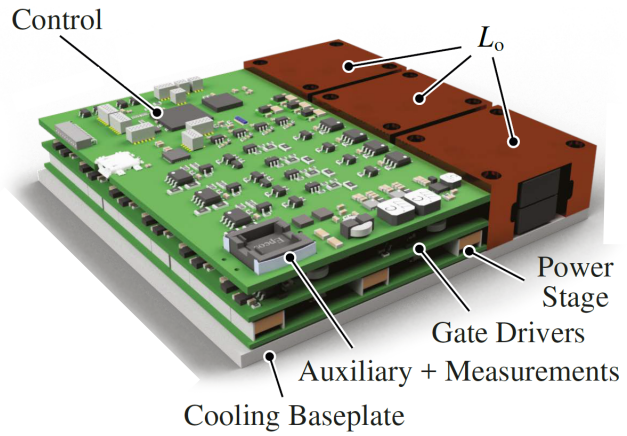
- *Combination of Series & Parallel Interleaving*

— *600V GaN Power Semiconductors, f_{sw}= 800kHz*
— *Volume of ≈180cm³ (incl. Control etc.)*
— *H_2O Cooling Through Baseplate*





≈ *820 W/in³*

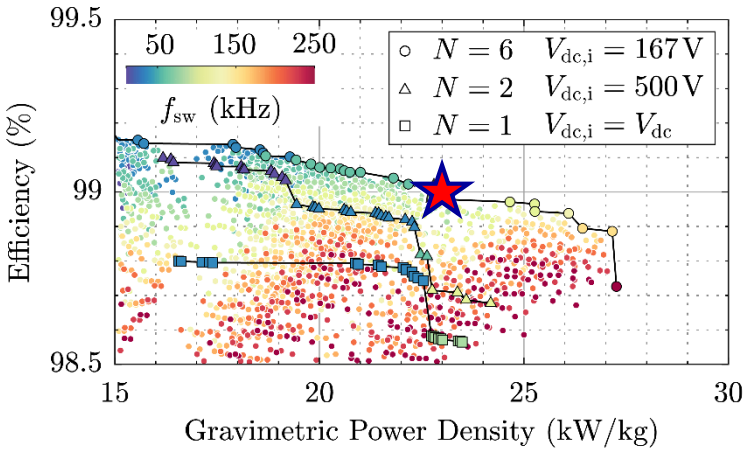


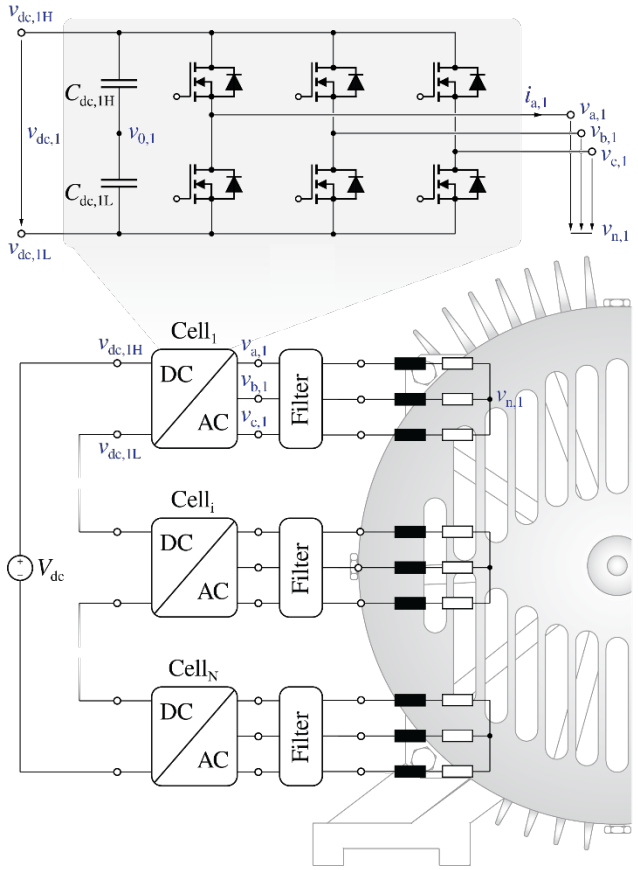
- *Operation @ f_{out}=100kHz / $f_{S,eff}$= 4.8MHz, 10kW, U_{dc}=800V*

Motor-Integrated Modular Inverter

- *Fault-Tolerant VSD*
- *Low-Voltage Inverter Modules*
- *Very-High Efficiency / Power Density*
- *Automated Manufacturing*

- *Rated Power* *45kW / f_{out} = 2kHz*
- *DC-Link Voltage* *1 kV*

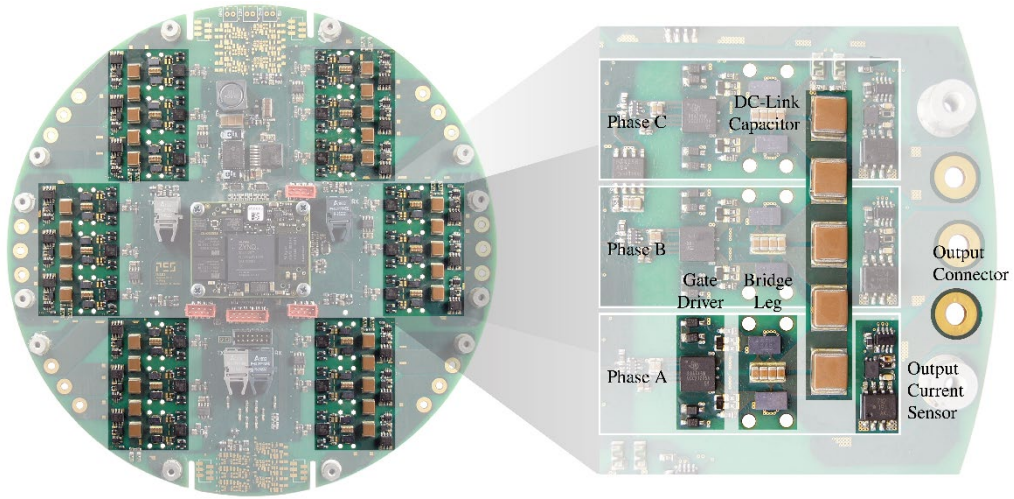


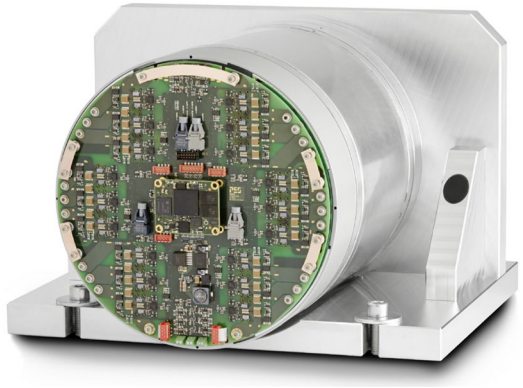


- *Smart Motor / Plug & Play* | *Connected / Intelligent VSD 4.0*

Motor-Integrated Inverter Demonstrator

- Rated Power 9kW @ 3700rpm
- DC-Link Voltage 650V...720V
- 3-Φ Power Cells 5+1
- Outer Diameter 220mm

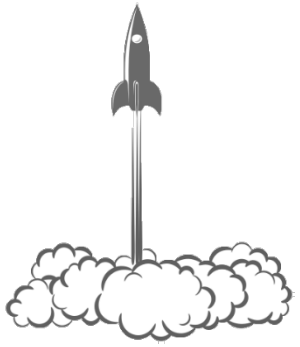




- Axial Stator Mount
- 200V GaN e-FETs
- Low-Capacitance DC-Links
- 45mm x 58mm / Cell

- Main Challenge — Thermal Coupling/Decoupling of Motor & Inverter

X-Technology #3

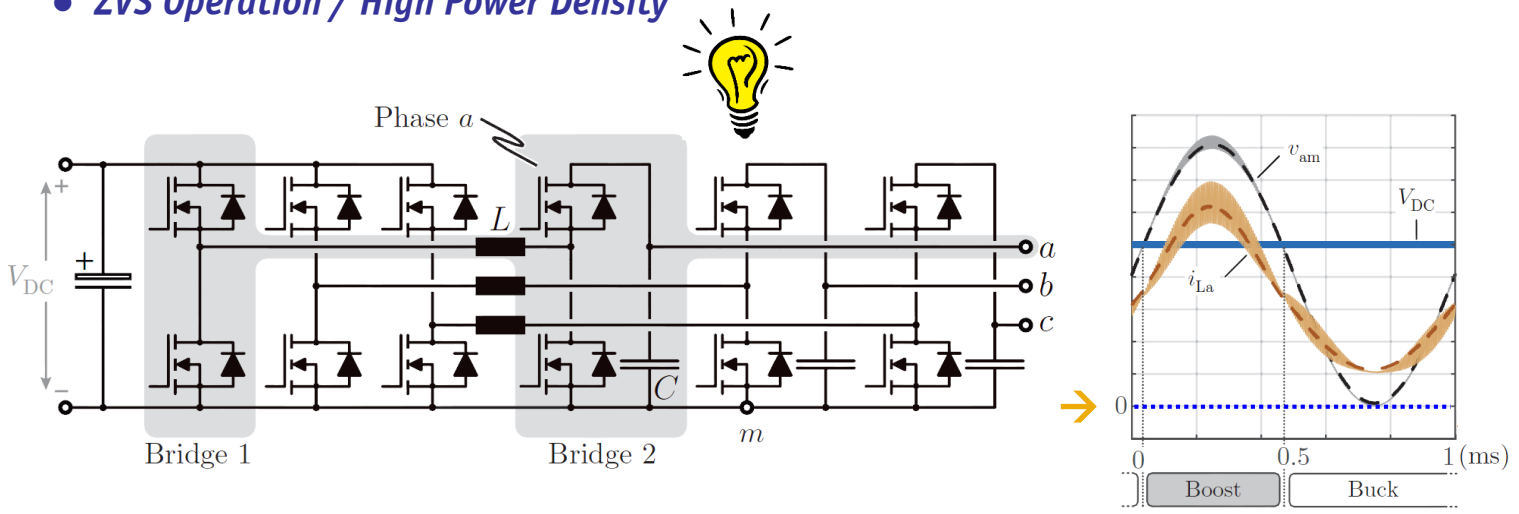


Functional Integration & Synergetic Association

Lighthouse Project

- *3-Φ Continuous Voltage Output*
- *Buck+Boost Operation*
- *Standard Bridge-Legs / Building Blocks*
- *ZVS Operation / High Power Density*

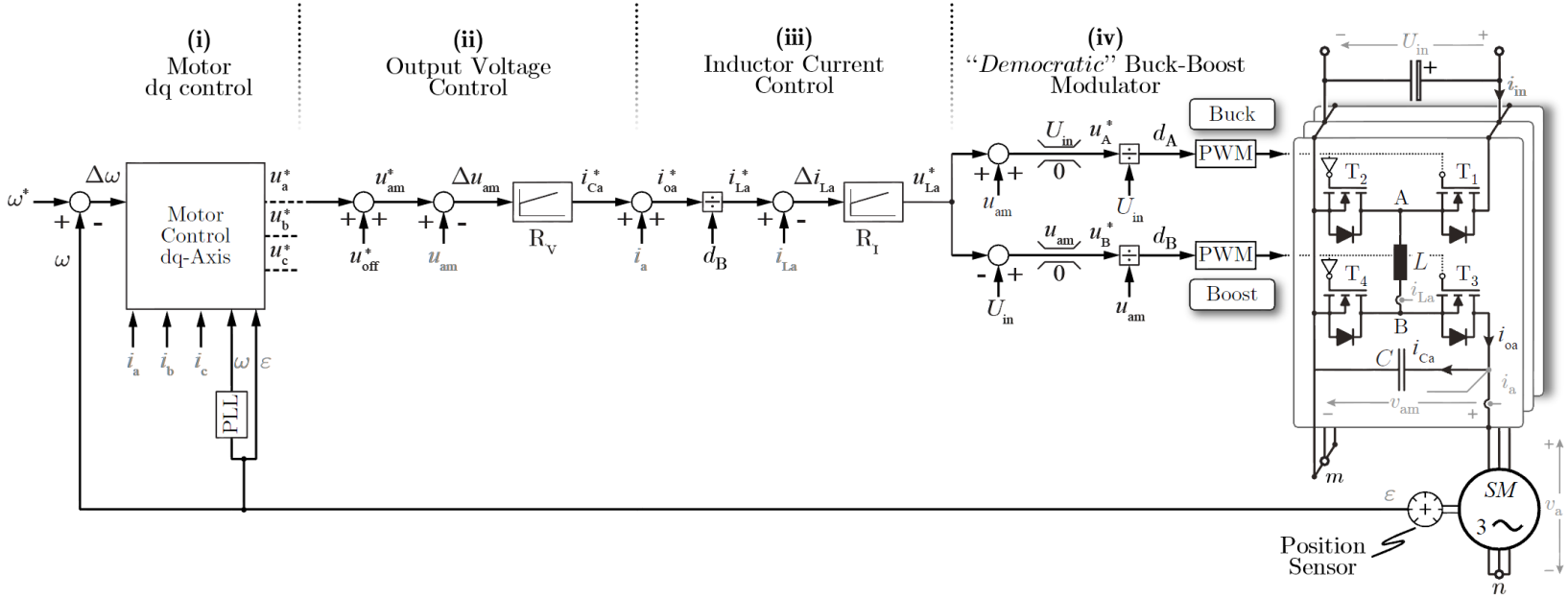
- *Low EMI / No Shielded Cables / No Motor Insul. Stress*
- *Very Wide Input Voltage / Speed Range*
- *1.2kV SiC MOSFETs*



- *Project Scope → Hardware Demonstrator / Exp. Analysis / Comparative Evaluation*

Control Structure

- *Motor Speed Control*

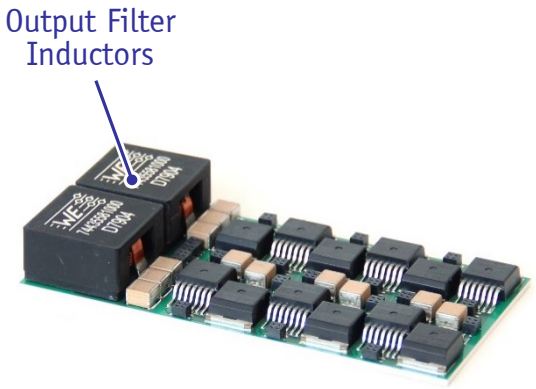


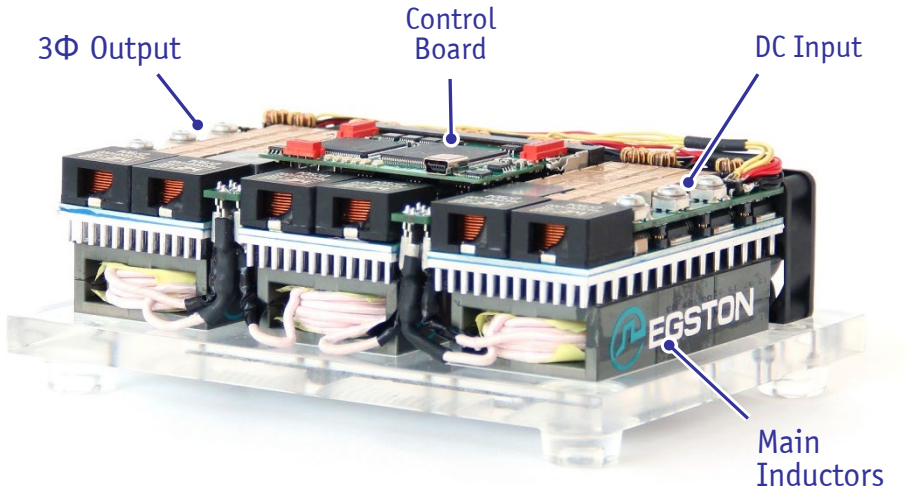
- *Cascaded Current / Voltage / Current Control Loops*
- *Seamless Transition between Boost- & Buck-Mode → "Democratic" Control*

3-Φ Modular Buck-Boost Inverter Prototype

- DC Voltage Range 400...750V_{DC}
- Output Voltage 0...230V_{rms} (Phase)
- Output Frequency 0...500Hz
- Sw. Frequency 100kHz
- 3x SiC (75mΩ)/1200V per Switch

★ ≈ 15 kW/dm³

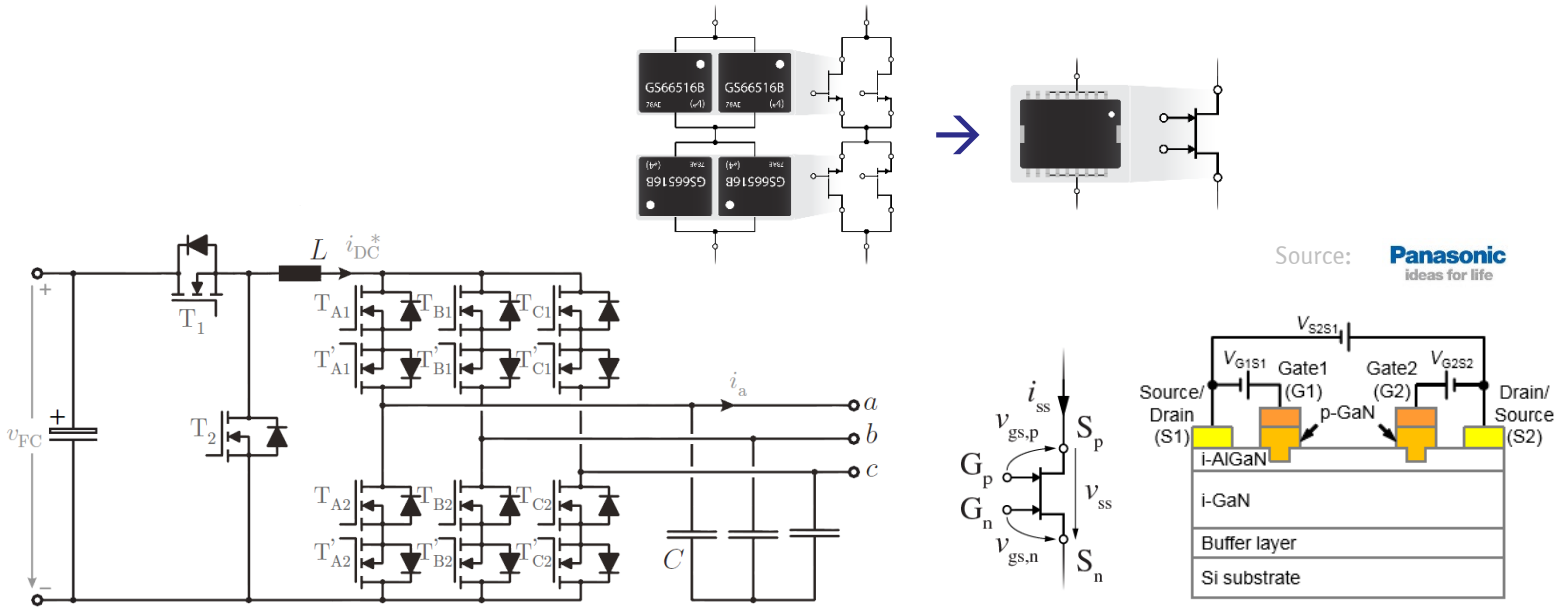




- Dimensions → 160 x 110 x 42 mm³ (245W/in³)
- IMS Carrying Buck/Boost-Stage Transistors & Comm. Caps & 2nd Filter Ind.

3-Φ Modular → 3-Φ Integrated Buck-Boost CSI

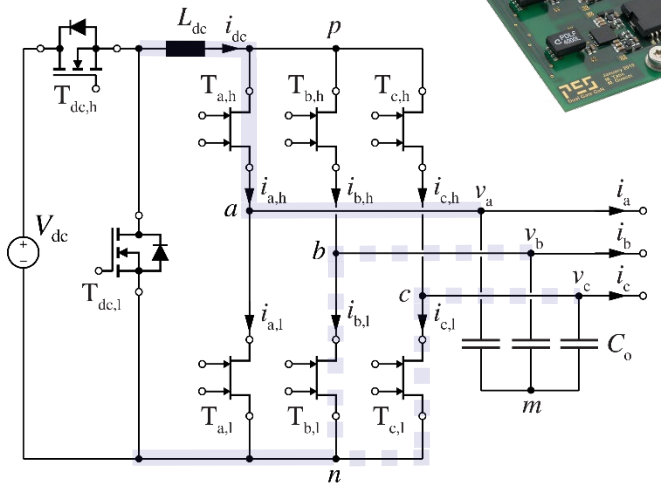
- *Bidirectional/Bipolar Switches → Positive DC-Side Voltage for Both Directions of Power Flow*

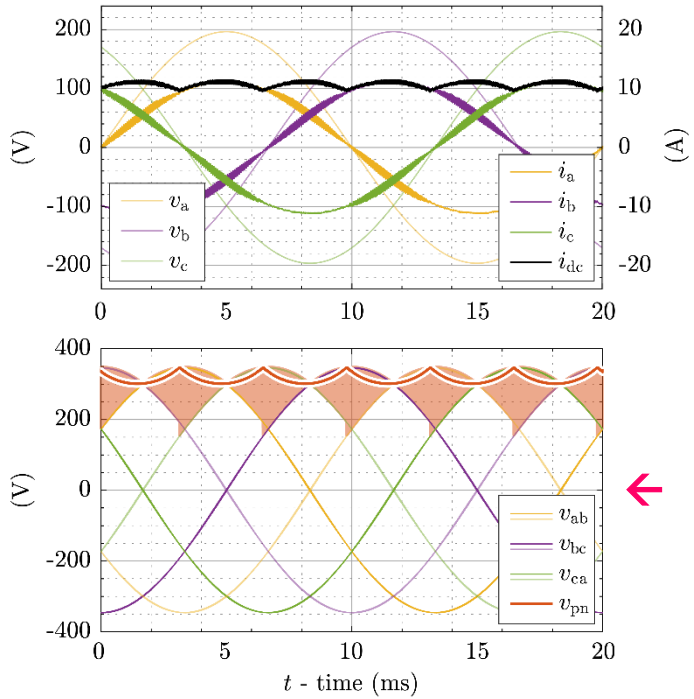


- *Monolithic Bidir. GaN Switches → Factor 4 Reduction of Chip Area Comp. to Discrete Realization*

3-Φ-Integrated Buck-Boost CSI

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase*

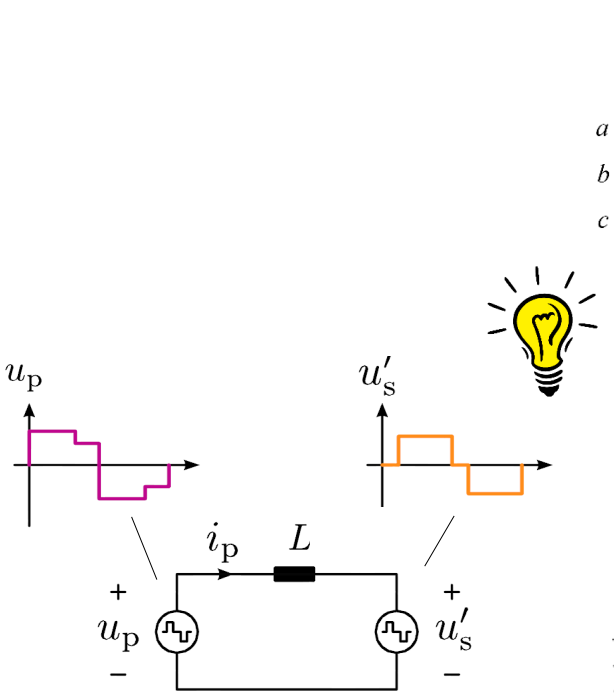




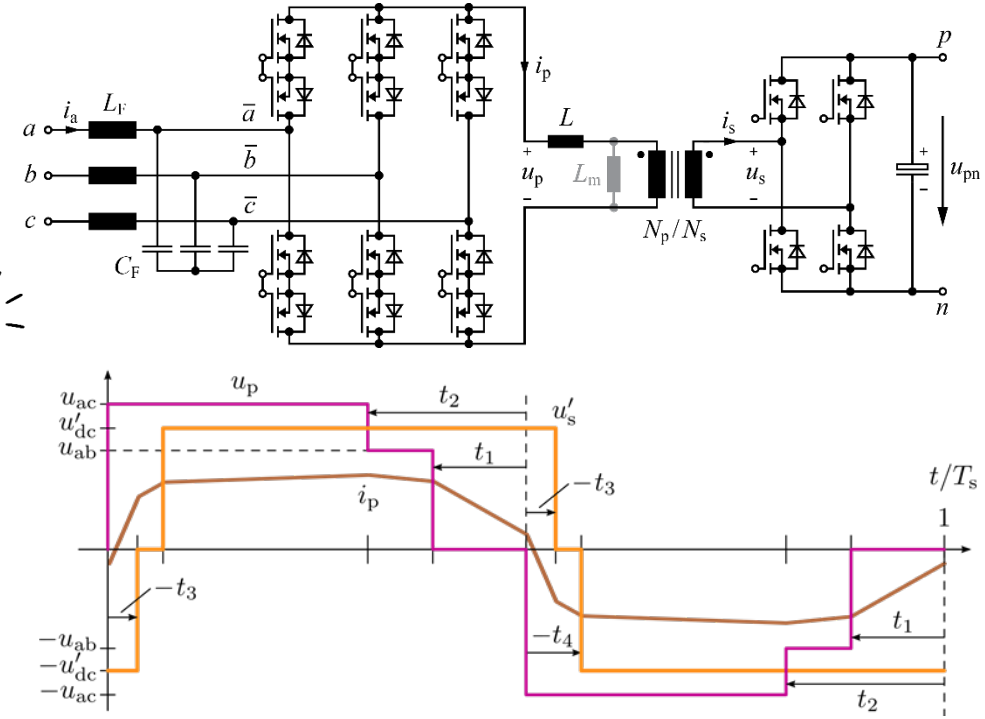
- *Switching of Only 2 of 3 Phase Legs → Reduction of Sw. Losses by ≈ 86% (!)*

Isolated 3-Φ Matrix-Type *PFC Rectifier*

- *Based on Dual Active Bridge* (DAB) Concept
- *Optimal Modulation* ($t_1 \ldots t_4$) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation



► Equivalent Circuit

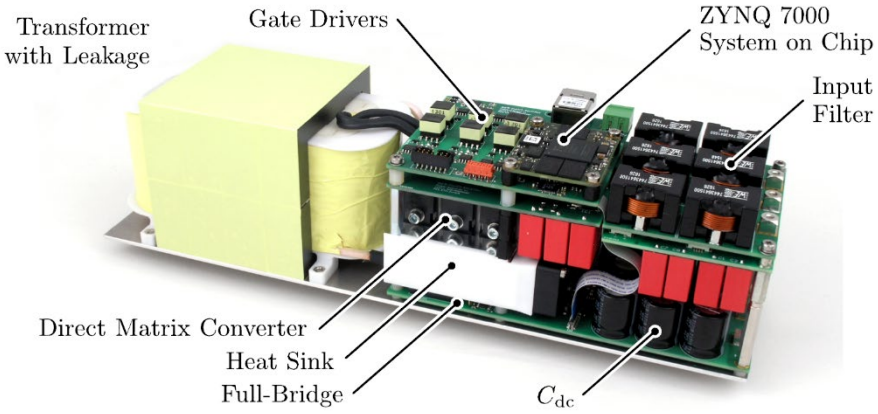


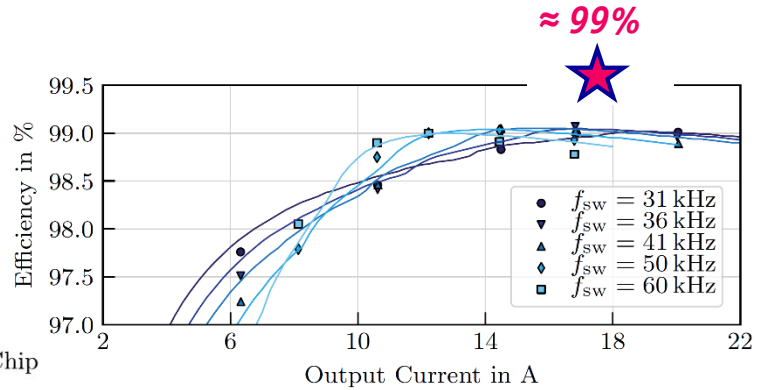
► Transformer Voltages / Currents

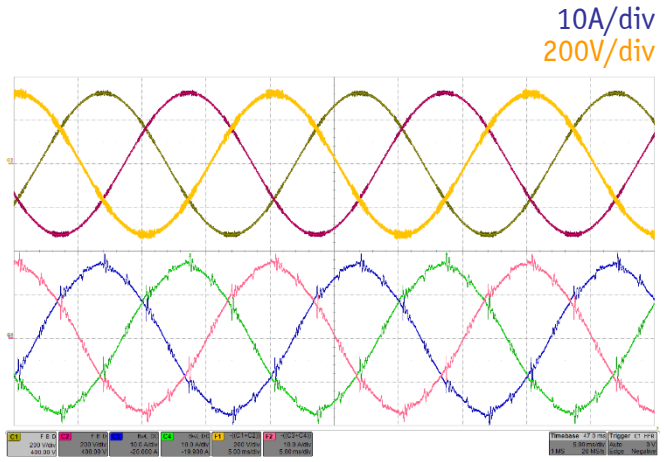
Isolated 3-Φ Matrix-Type *PFC Rectifier*

- Efficiency η = 98.9% @ 60% Rated Load (ZVS)
- Mains Current $THD_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4 kW/dm^3$

P_0= 8 kW
U_N= 400V_{AC} → U_0= 400V_{DC}
f_S = 36kHz



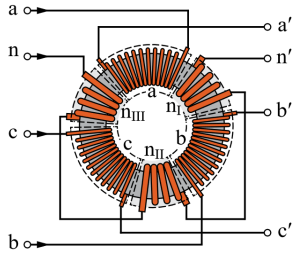


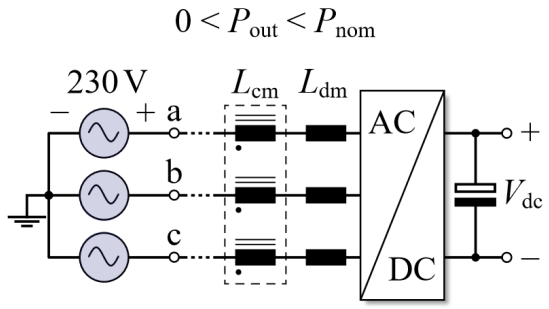


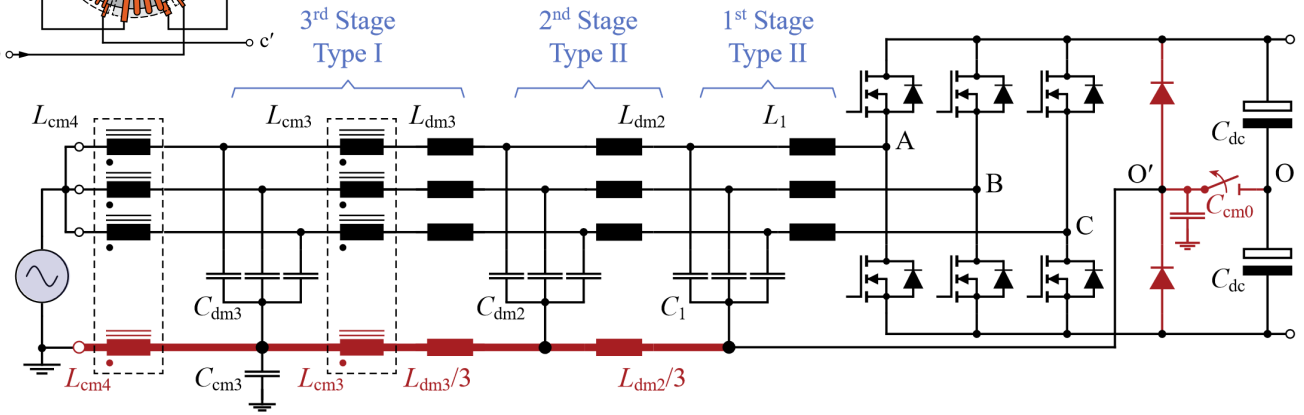
- 900V / 10mΩ SiC Power MOSFETs
- Opt. Modulation Based on 3D Look-Up Table

3-Φ / 1-Φ Full-Power PFC Rectifier

- 4-Wdg. CM Filter Inductors & Add. Diode Bridge-Leg
- Interleaving of Bridge-Legs in 1-Φ Operation
- Application as EU/USA EV-Charger Front-End



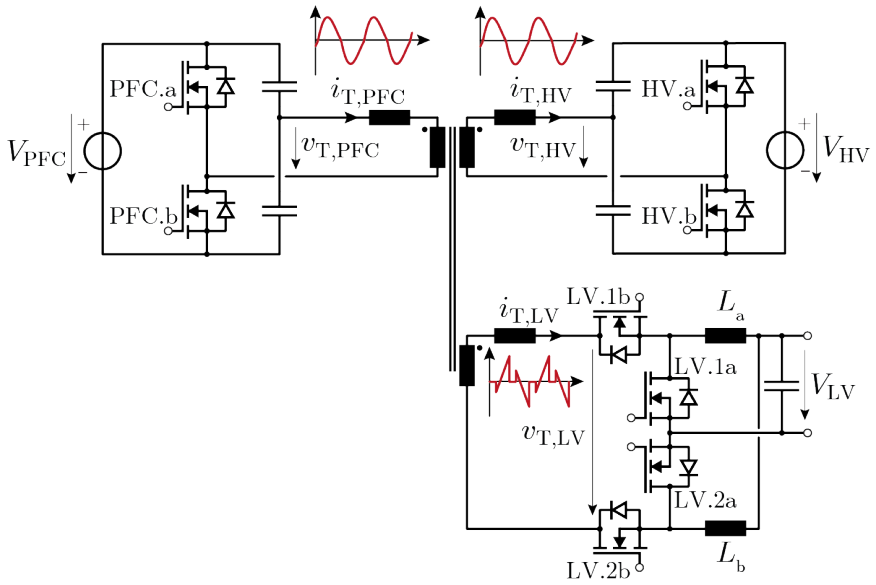


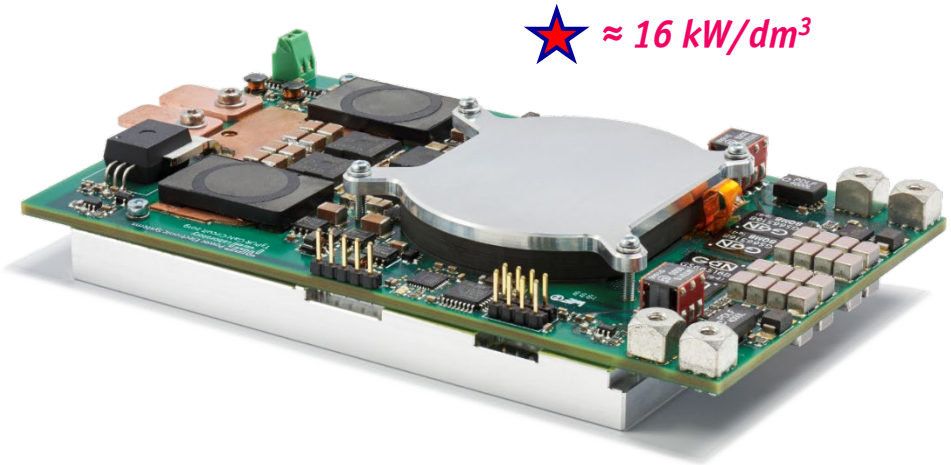


- 22kW / U_{DC}=750V / U_{AC}= 3-Φ 400V OR 1-Φ 240V | 98.4 % Efficiency | 6.8 kW/dm³ Power Density

3-Port Resonant GaN DC/DC Converter

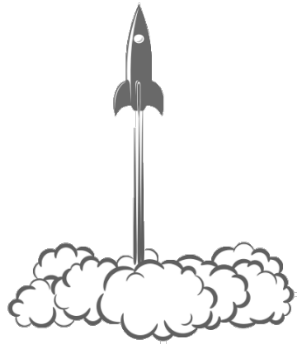
- *Single Transformer & Decoupled Power Flow Control*
- *Charge Mode PFC → HV (250...500V) SRC DCX / Const. f_{sw}, Min. Series Inductance / ZVS*
- *Drive Mode HV → LV (10.5...15V) 2 Interleaved Buck-Converters / Var. f_{sw} / ZVS*
- *P = 3.6kW*





- *Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode*

X-Technology #4

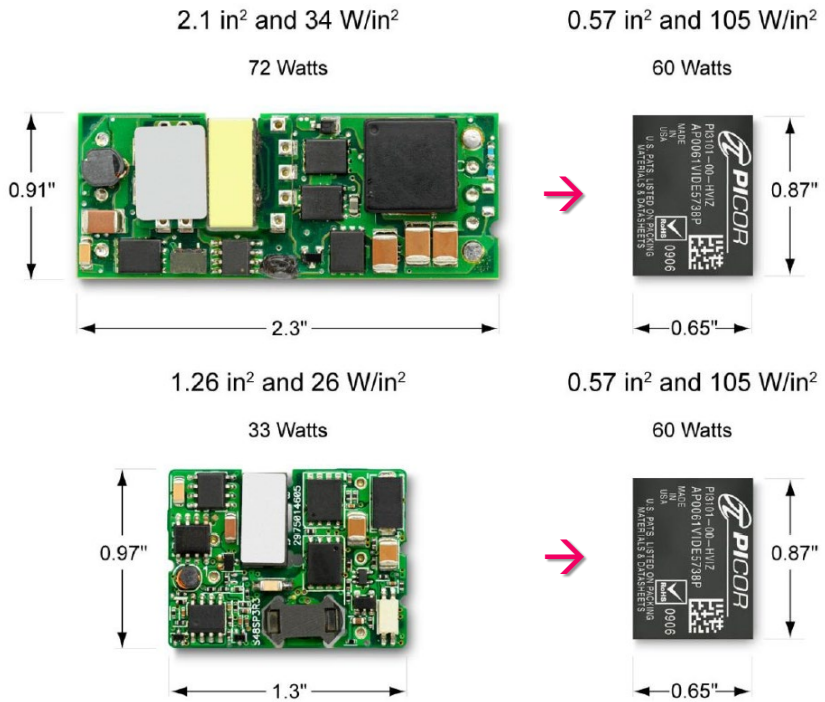


3D-Packaging
Automated Manufacturing

3D-Packaging / Heterogeneous Integration

- *System in Package (SiP) Approach*
- *Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management*
- *Very High Power Density (No Bond Wires / Solder / Thermal Paste)*
- *Automated Manufacturing*

Source: VICOR



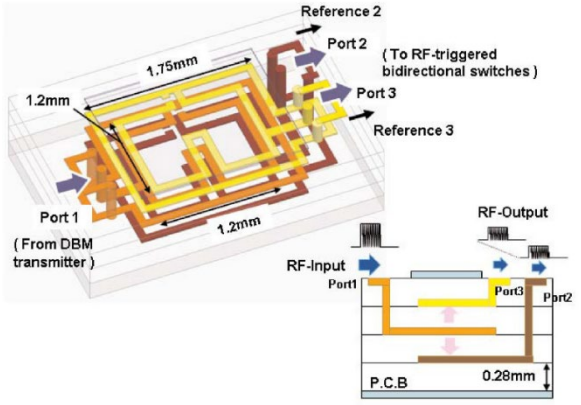
- *Future Application Up to 100kW (!)*
- *New Design Tools & Measurement Systems (!)*
- *University / Industry Technology Partnership (!)*

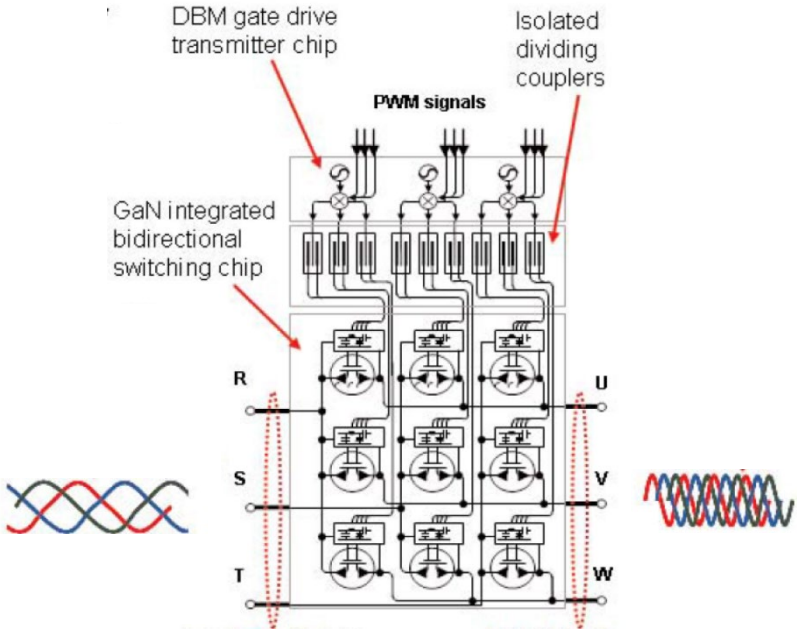
Monolithic 3D-Integration

Source: Panasonic ISSCC 2014

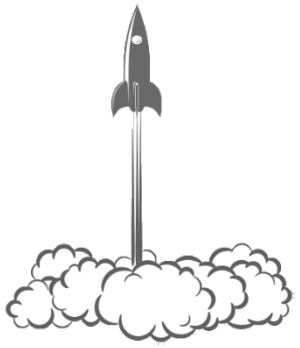
- *GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology*
  - *9 Dual-Gate GaN AC-Switches*
  - *DBM Gate Drive Transmitter Chip & Isolating Couplers*
  - *Ultra Compact → 25 x 18 mm² (600V, 10A – 5kW Motor)*

5.0GHz Isolated (5kVDC) Dividing Coupler





X-Technology #5

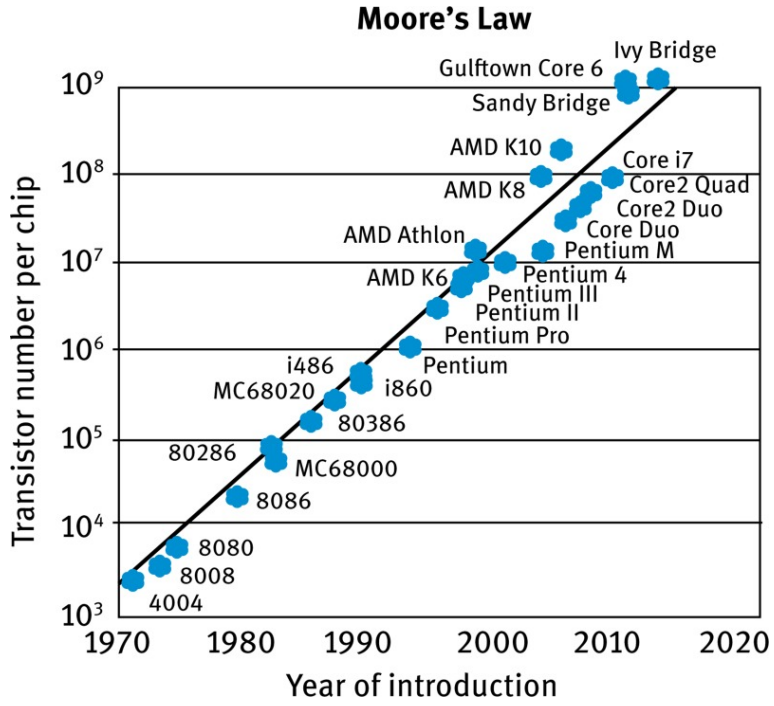


Automated Design
Digital Twin / Industry 4.0

Digital Signal & Data Processing

- *Exponentially Improving uC / Storage Technology (!)*

— *Extreme Levels of Density / Processing Speed*
— *Software Defined Functions / Flexibility*
— *Cont. Relative Cost Reduction*



Source: Ostendorf & König /DeGruyter

- *Fully Digital Control of Complex Systems*
- *Massive Computational Power → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)*

Automated Design Roadmap

- *End-to-End Horizon of Modeling & Simulation*
- *Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling*

Autonomous Design → Design 4.0

– *Independent* Generation of Full Designs for Final Expert Judgement

Augmented Design

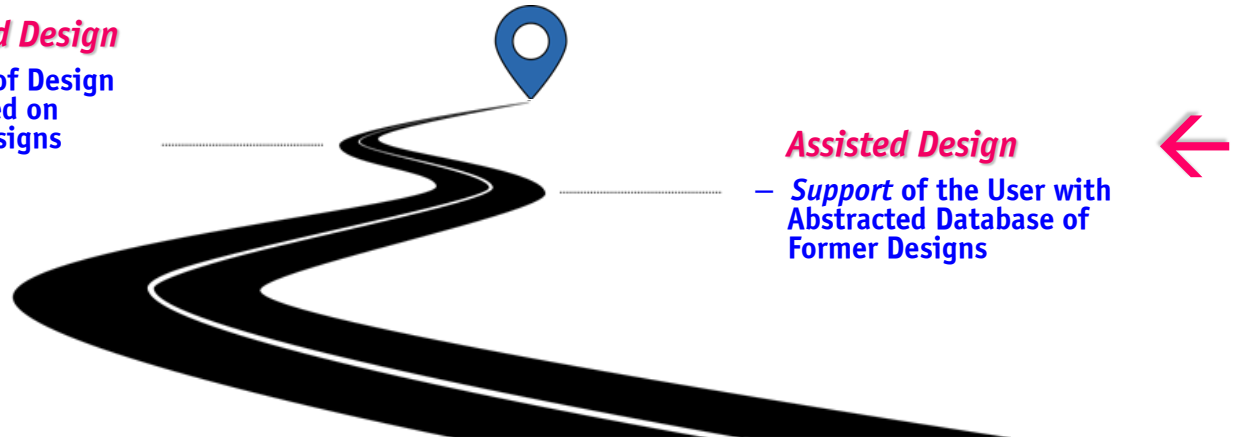
– *Suggestion* of Design Details Based on Previous Designs

Assisted Design

– *Support* of the User with Abstracted Database of Former Designs

State-of-the-Art

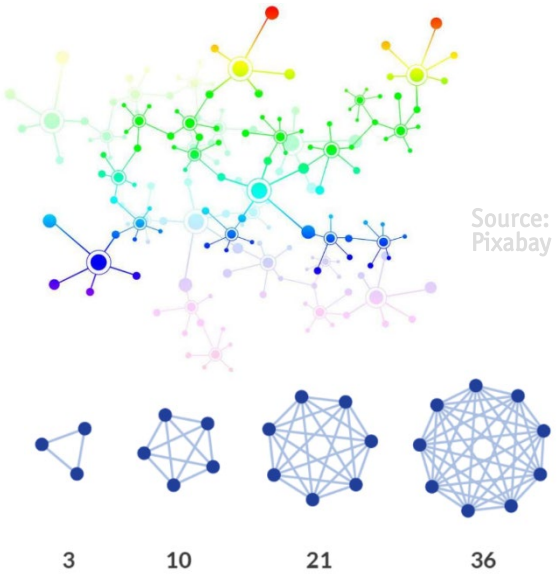
– *User Defined* Models and Simulation / Fragmented

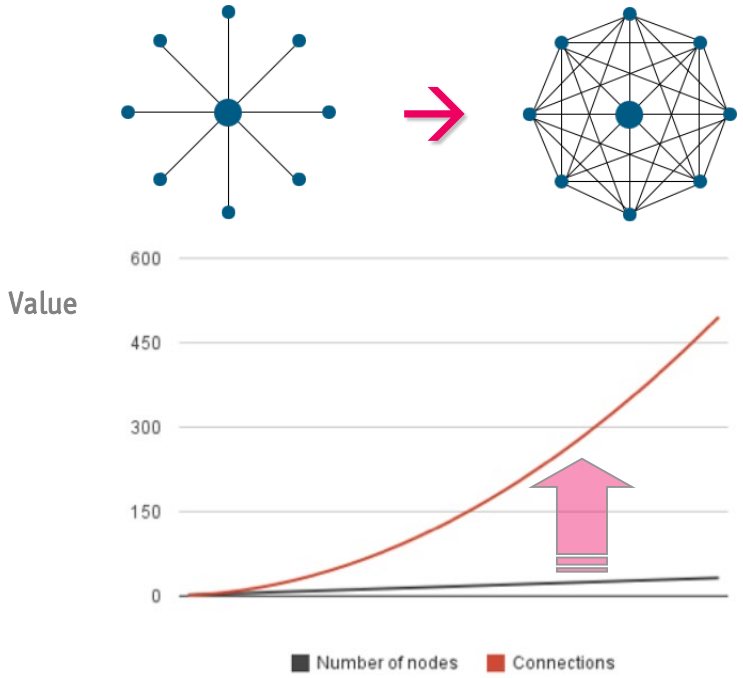


- *AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)*

Scaling Law – Power Electronics 4.0

- **Metcalfe's Law**
  - *Moving from Hub-Based Concept to Community Concept Increases Value Exponentially (~n(n-1) or ~n log(n))*



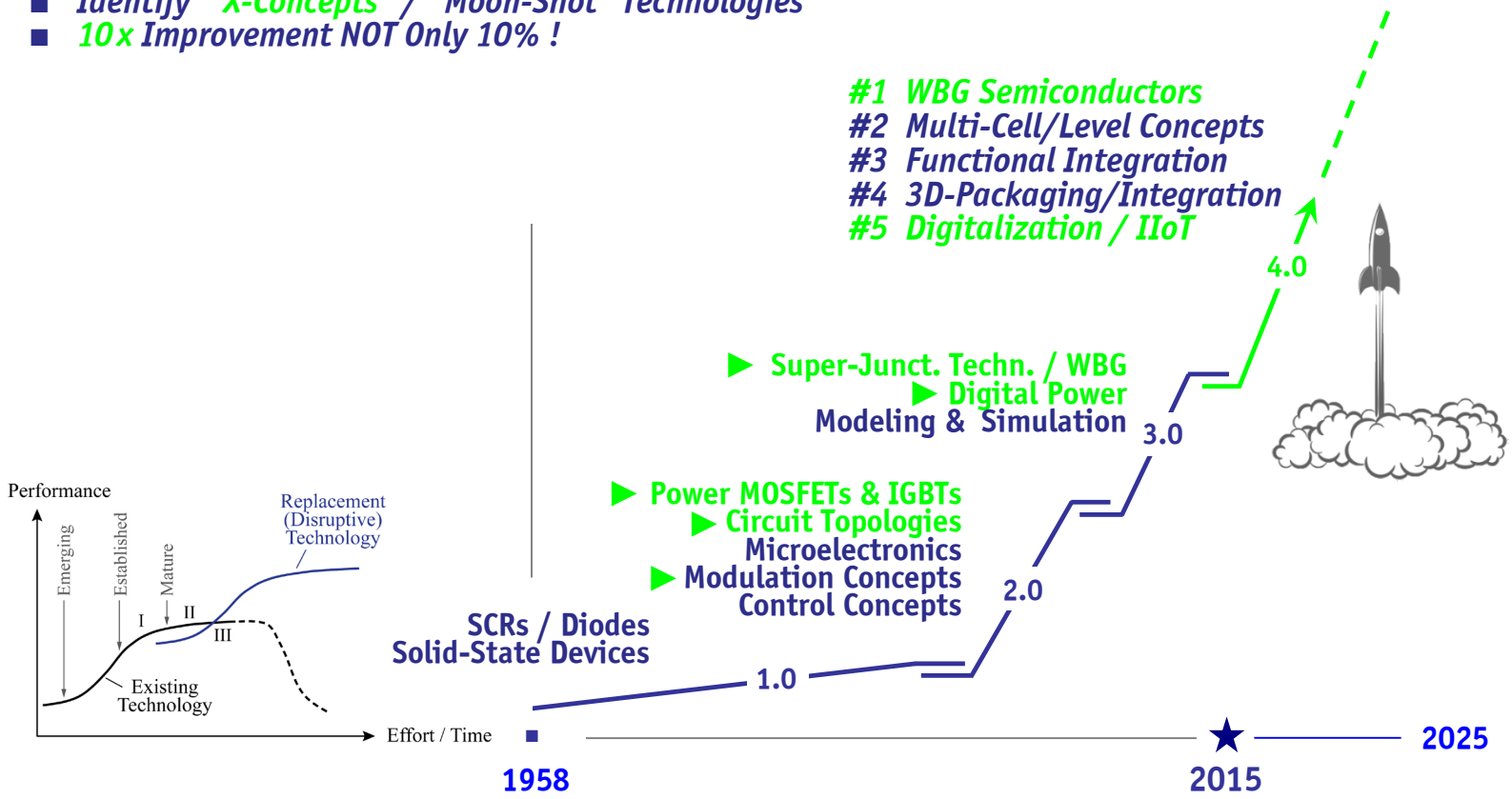


- *Automated Design / Digital Control / Digital Twin*

Conclusion

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*



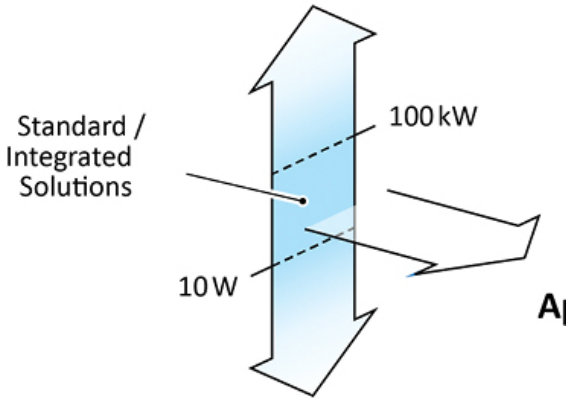
Thank you!


BACKUP

Future Development

- Commoditization / Standardization
- Extreme Cost Pressure (!)

"There is Plenty of Room at the Top" → *Medium Voltage/Frequency Solid-State Transformers*



System Applications

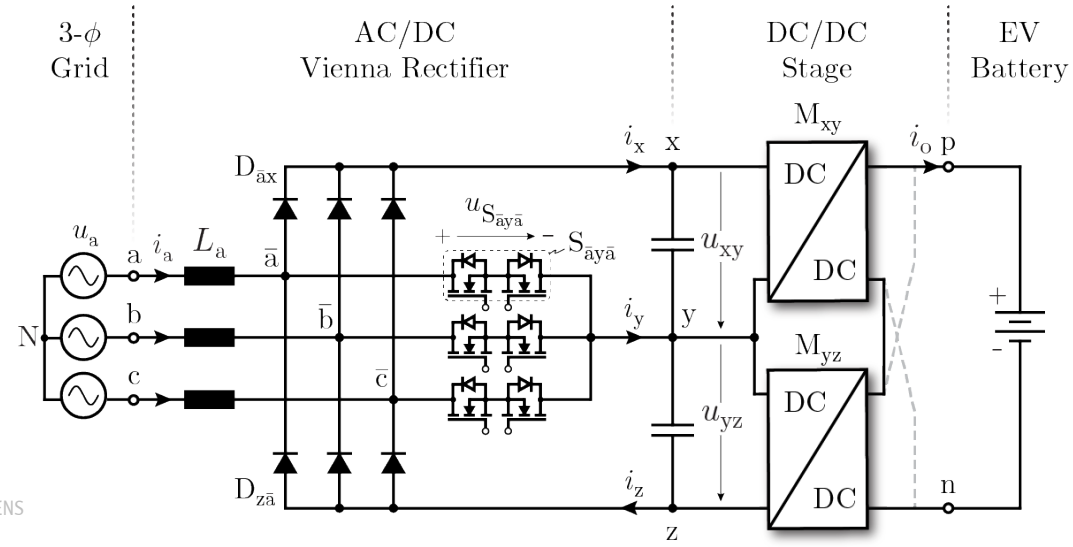
Power-Supplies on Chip ← **"There is Plenty of Room at the Bottom"**

- Key Importance of Technology Partnerships of Academia & Industry

Selected EV Charger Topology

- Isolated Controlled Output Voltage
- Buck-Boost Functionality & Sinusoidal Input Current
- *Applicability of 600V GaN Semiconductor Technology*
- *High Power Density / Low Costs*

Source: SIEMENS

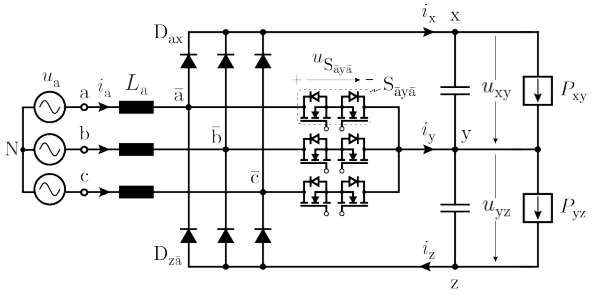


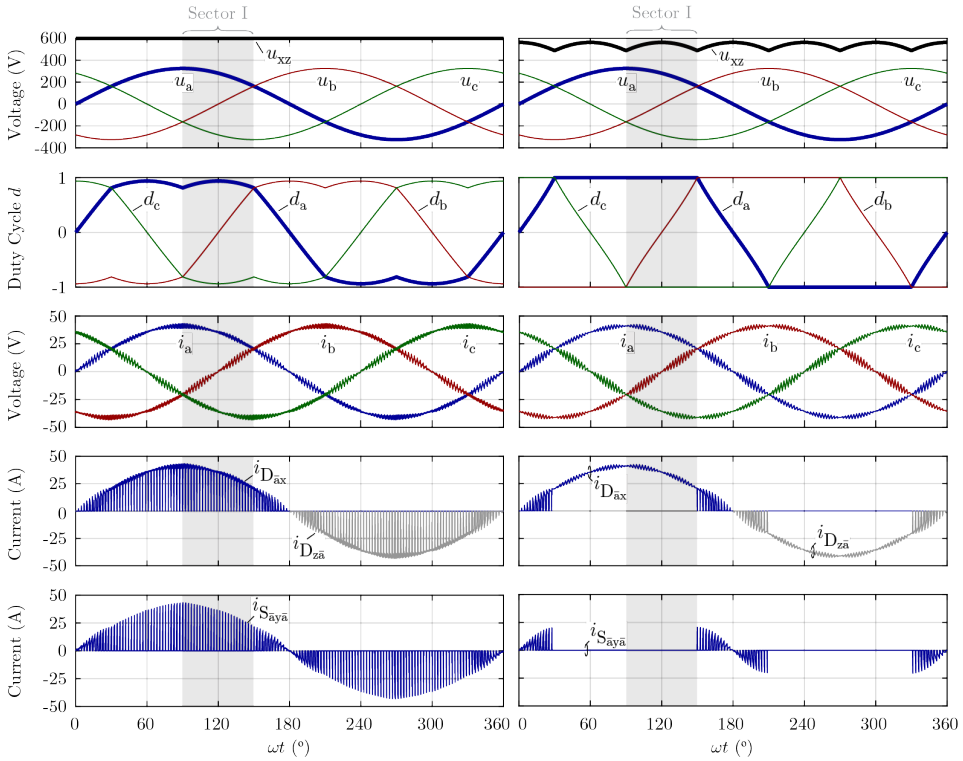
→ *Conventional / Independent OR* "Synergetic Control" *of Input & Output Stage*

Conventional vs. "Synergetic" Control

- *1/3-Modulation → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM*

- *Conduction Losses ≈ -80%*
- *Switching Losses ≈ -70%*





→ *Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses*

Wireless Power Transfer

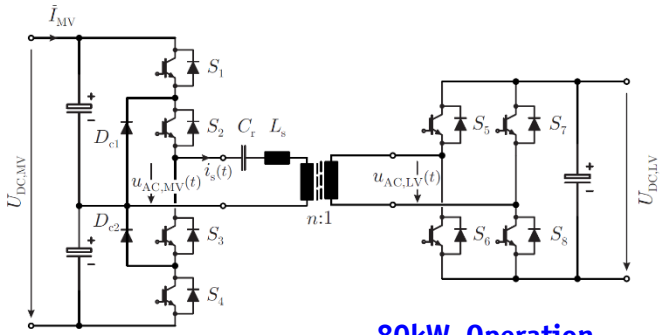
- **All-SiC Power Electronics**
  - Rated Power 50kW
  - Battery Voltage 600...800V
  - Power Density 9.5kW/dm^3
  - Sw. Frequency 50kHz/85kHz

- **Inductive Power Transfer Coils**
  - Air Gap 150...220mm
  - Power Density 1.6kW/dm^2
  - Frequency 85kHz

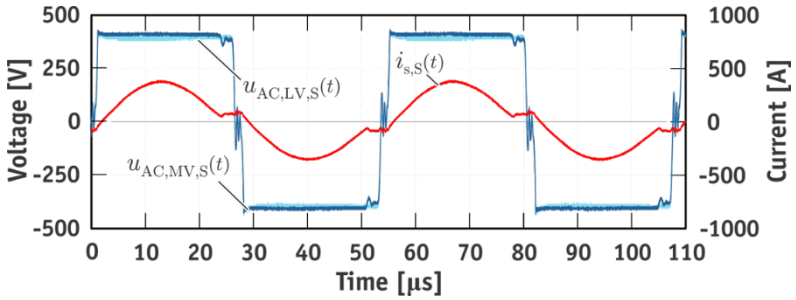
★ η_{DCDC} = 95.8% @ 50kW / ICNIRP @ 800mm

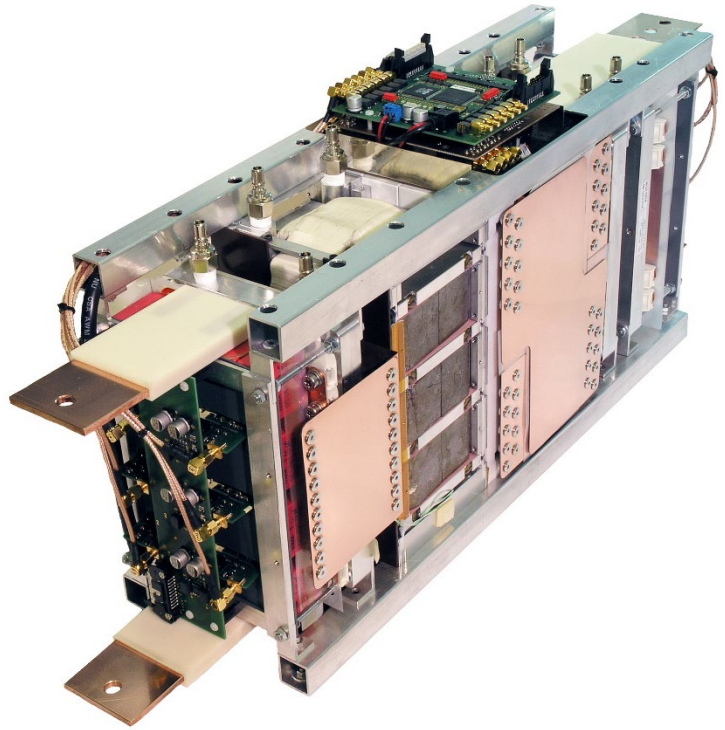
166kW / 20kHz DC-Transformer

- Half-Cycle DCM Series Resonant DC-DC Converter
- Medium-Voltage Side 2kV
- Low-Voltage Side 400V



80kW Operation





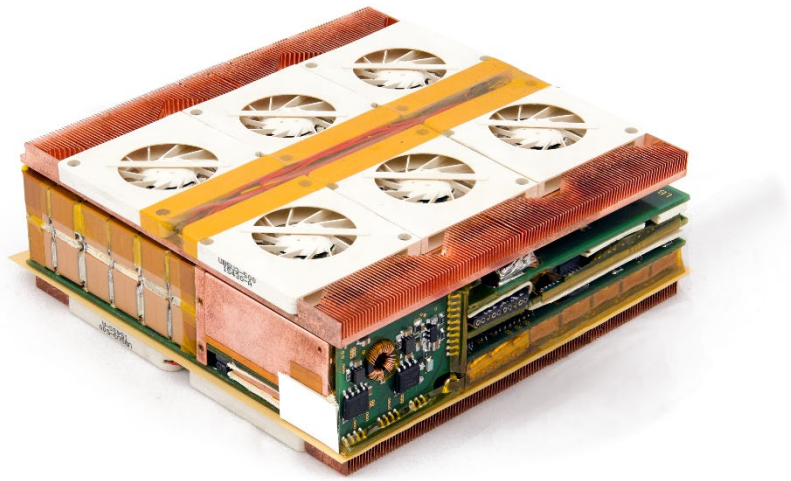
Little-Box 1.0 Prototype

- *DC-Side Power Pulsation Buffer*

- 8.2 kW/dm^3
- 8.9cm x 8.8cm x 3.1cm
- **96,3% Efficiency @ 2kW**
- **T_c=58°C @ 2kW**

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

★ **135 W/in^3**



- *Compliant to All Original Specifications (!)*

- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

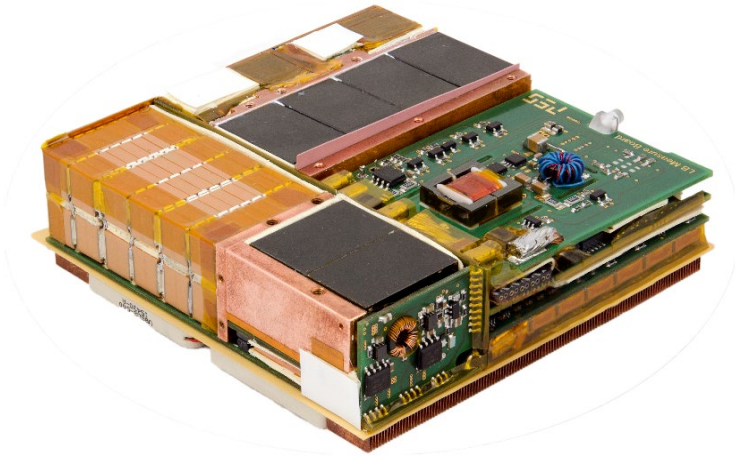
Little-Box 1.0 Prototype

- *DC-Side Power Pulsation Buffer*

- 8.2 kW/dm^3
- 8.9cm x 8.8cm x 3.1cm
- **96,3% Efficiency @ 2kW**
- **T_c=58°C @ 2kW**

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

★ **135 W/in^3**



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