



Future SiC/GaN Variable Speed Drive Inverter Topologies

"How to Handle a Double-Edged Sword"

Dominik Bortis, et al.



Swiss Federal Institute of Technology (ETH) Zurich Power Electronic Systems Laboratory www.pes.ee.ethz.ch

2nd Wagner Automotive Symposium — Inverter Trends & Technology, November 7th, 2019







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ETH Zurich

Nobel Prizes 21 509 Professors 5800 T&R Staff 2 Camp 136 Labs Campuses 35% Int. Students Nationalities 90 36 Languages



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CHAB	Chemistry and Applied Biosciences
ERDW	Earth Sciences
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HEST	Health Sciences, Technology
INFK	Computer Science
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Outline

► Introduction

- SiC/GaN Application Challenges
 VSI with Output Filters
 Boost-Buck VSI

- Buck-Boost CSI
- Q3L & Modular Inverters
- **Conclusions**

J. Azurza T. Guillod F. Krismer D. Menzi J. Miniböck P. Niklaus P. Papamanolis D. Zhang

Acknowledgement:



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3-Ф Variable Speed Drive Inverter Systems

State-of-the-Art Future Requirements



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VSD State-of-the-Art

- Mains Interface / 3-Ф PWM Inverter / Motor All Separated
 - → Large Installation Space
 / \$\$\$
 → Complicated / Expert Installation
 / \$\$\$

Conducted EMI / Radiated EMI / Bearing Currents / Reflections on Long Motor Cables

- → Shielded Motor Cables / \$\$\$
- \rightarrow Inverter Output Filters (Add. Vol.) / \$\$\$



• High Performance @ High Level of Complexity / High Costs (!)



Future Requirements (1)

- "Non-Expert" Install. / Low-Cost Motors → "Sinus-Inverter" OR Integrated Inv. Wide Applicability / Wide Voltage & Speed Range → Matching of Supply & Motor Voltage
- High Availability



Single-Stage Energy Conversion \rightarrow No Add. Converter for Voltage Adaption



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Future Requirements (2)

- *Red. Inverter Volume / Weight*
- Lower Cooling Requirement High Speed Machines

- → Matching of Low High-Speed Motor Volume
 → Low Inverter Losses & Low HF Motor Losses
- \rightarrow High Output Frequency Range



→ Main "Enablers" — SiC/GaN Power Semiconductors & Adv. Inverter Topologies









Idea: F.C. Lee

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Carlen.



EDGE 2
● Challenges → Packaging / Thermal Management / Gate Drive / PCB Layout



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Si vs. SiC

Extremely High dv/dt (Si-IGBT: dv/dt = 2...6kV/us vs. SiC-MOSFETs: dv/dt = 20...60kV/us)

Very Low Switching Losses
 High Switching Frequencies

SiC-MOSFET / (scaled for low inductance) Si-IGBT / Hybrid-Pack 2 **Turn-off @** *T*₁ = 25°C **Turn-off @** *T*_1 = 25°C 1000 1000 16 par. Chips 25 nH 800 800 6 nH 50 A/ns / in A / in A 7 A/ns 600 600 V in V 400 >400 U II 6 V/ns \sim 200 200 33 V/ns Ο 0 0 200 400 600 800 1000 200 400 600 800 1000 0 t in ns t in ns $E_{\rm off} = 4672 \ \mu J$ -> 8 kV/µs at 400V -> 44 kV/µs at 400 V $E_{\rm off} = 45900 \ \mu J$

Source: M. Bakran / ECPE 2019

EDGE 2

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EDGE 1

Challenges→Motor Insul. Stress (Volt. Peaks → Insul. Breakdown → Partial Discharge)→Reflections(Impedance Mismatch of long Cable & Motor)→Bearing Currents(Motor Shaft Volt. → Elect. Discharge in Bearing)→EMI(Conducted & Radiated)

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Inverter Output Filters

Full-Sinewave Filtering





— Full-Sinewave Filtering — YASKAWA

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► 3-Φ 650V GaN Inverter System (1)

Source: YASKAWA

Transphorm 650V GaN HEMT/30V Si-MOSFET Cascode Switching Devices

• Measurement of Sw. Properties \rightarrow Turn-On/Off 10A/400V



- Factor 10 Lower On/Off Delay & Sw. Times Comp. to IGBTs
- Extremely Low Sw. Losses
- Sinewave LC Output Filter
- → Inverter Sw. Frequency f_s = 100kHz → Corner Frequency f_c = 34kHz (f_s = 100kHz)



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► 3-Φ 650V GaN Inverter System (2)

Source: YASKAWA

Comparison of GaN Inverter with LC-Filter to Si-IGBT System (No Filter, f_s=15kHz)
 Measurement of Inverter Stage & Overall Drive Losses @ 60Hz



 \rightarrow 2% Higher Efficiency of GaN System Despite LC-Filter (Saving in Motor Losses) !



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► 3-Φ 650V GaN Inverter System (3)

Source: YASKAWA

Sigma-7F Servo Drive — Integration of Inverter (TO-220 GaN) Into Motor Housing
 Distributed DC-Link System ("Converter" generates DC)
 0.1 - 0.4kW / 270...324V Nominal DC Link Voltage





Buck-Boost Inverter

VSI & DC/DC Front-End — Phase-Modular Buck-Boost Inverter CSI & DC/DC Front-End



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Boost Converter DC-Link Voltage Adaption

- Inverter-Integr. DC/DC Boost Conv. → Higher DC-Link Voltage / Lower Motor Current
- Access to Motor Star Point & Specific Motor Design Required
- No Add. Components



Explicit Front-End DC/DC Boost Stage



 \rightarrow Analyze Coupling of the Control of Both Converter Stages \rightarrow "Synergetic Control"



"Synergetic Control" of Boost-Buck Inverter (1)

- DC/DC Boost Converter Used for 6-Pulse Shaping of DC-Link Voltage 2 (!) Inverter Phases Clamped (1/3 PWM) → Low Switching Losses / High Efficiency Conv. PWM Inverter / Clamped Boost-Stage Operation @ Low Speed



• Preferable for Low-Dynamics Drive Systems



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"Synergetic Control" of Boost-Buck Inverter (2)

Control Structure and Simulation Results



• Seamless Transition — Clamped Boost-Stage \rightarrow Temporary \rightarrow Full Boost-Stage Operation



"Synergetic Control" of Boost-Buck Inverter (3)

Experimental Verification



 \rightarrow Comparison to Conv. U_{DC}=const. Operation (PWM of 2/3 Phases or 3/3 Phases)



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"Synergetic Control" of Boost-Buck Inverter (4)

- **Experimental Verification**
- Const. DC-Link Voltage & PWM of 3/3 Phases or 2/3 Phases Synergetic Control = PWM of 1/3 Phases \rightarrow Substantial Loss Saving (!)



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Phase-Modular Topologies

Boost-Buck Modules Buck-Boost Modules



Phase-Modular Boost-Buck / Buck-Boost Inverter

- Realization of 3- Φ Inverter Using 3 DC/DC Converter (Phase) Modules S. Cuk/1982 Wide Voltage Conv. Range \rightarrow Battery or Fuel-Cell Supply & Adaption to Motor Voltage Continuous Output Voltage \rightarrow Explicit or Integrated LC Output Filter



 \rightarrow Preference for Low Number of Ind. Components \rightarrow Buck-Boost Concept – "Y-Inverter"



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- 3-Ф Continuous Output / Low EMI !
- Buck-Boost Operation / Wide Input &/or Output Range Industrial Drive
 Standard Bridge Legs / Building Blocks 1.2kV SiC MOSFE
 High Power Density

- No Shielded Cables / No Insul. Stress

- 1.2kV SiC MOSFETs
- Phase a $V_{\rm DC}$ $V_{\rm DC}$ **-0** C mBridge 1 Bridge 2 0.5 $1 \,(\mathrm{ms})$ Boost Buck

Project Scope \rightarrow Hardware Demonstrator / Exp. Analysis / Comparative Evaluation



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► Y-Inverter (1)

• Operating Behavior



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► Y-Inverter (2)

• Control Structure



■ *"Democratic Control"* → Seamless Transition Between Buck & Boost Operation



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► Y-Inverter Prototype

- DC Voltage Range 400...750V_{DC}
- Max. Input Current ± 15A
- 0...230V_{rms} (Phase) 0...500Hz • Output Voltage
- Output Frequency
- Sw. Frequency 100kHz
- $3x \operatorname{SiC} (75 \mathrm{m}\Omega) / 1200 \mathrm{V}$ per Switch
- IMS Carrying Buck/Boost-Stage Semicond. & Comm. Caps & 2nd Filter Ind.



Dimensions \rightarrow 160 x 110 x 42 mm³ (15kW/dm³, 245W/in³)





Dynamic Behavior V-f Control and Load-Step



Experimental Results - Conducted EMI

• Measurements of the Cond. EMI Noise on the AC-Side (QP, with AC-LISN)

Experimental Results - Radiated EMI

- Measurement Setup
 Alternative Measurement Principle
- Y-Inverter Placed in Metallic Enclosure
 Measurement Setup
 Alternative Measurement Principle
 → Emulate Housing, but UNshielded Cables (!)
 → According IEC 61800-3
 → Conducted CM-Current Instead of Radiation

 \rightarrow Already Noticeable Noise Floor

 \rightarrow HF-Emissions Well Below Equivalent EMI-Limit \rightarrow Verification Using Antenna

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Efficiency Measurements

• Dependency on Input Voltage & Output Power Level

 U_{DC} = 400V / 600V U_{AC} = 230V_{rms} (Motor Phase-Voltage) f_{S} = 100kHz

→ Multi-Level Bridge-Leg Structure for Increase of Power Density @ Same Efficiency

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Current Source Inverter (CSI) Topologies

Phase Modular Concept → Y-Inverter (Buck-Stage / Current Link / Boost-Stage)
 3-Φ Integrated Concept → Buck-Stage & Current DC Link Inverter

→ Low Number of Ind. Components & Utilization of Bidir. GaN Semicond. Technology

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► 3-Φ Integrated Buck-Boost CSI (1)

- Basic Topology Proposed in 1984 (Ph.D. Thesis of K.D.T. Ngo/CPES) Monolithic Bidirectional 650V GaN e-FETs

→ Factor 4 Improvement in Chip Area Comp. to Discrete Realization \rightarrow Also Beneficial for Matrix Converter Topologies or Back-to-Back Configurations

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► 3-Φ Integrated Buck-Boost CSI (2)

- Monolithic Bidir. GaN Switches Featuring 2 Gates / Full Controllability
- Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control

• Conventional Control of Inverter Stage \rightarrow Switching of All 3 Phase Legs (3/3)

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► 3-Φ Integrated Buck-Boost CSI (3)

- Monolithic Bidir. GaN Switches Featuring 2 Gates / Full Controllability
- Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control

• Conventional Control of Inverter Stage \rightarrow Rel. High CSI-Stage Sw. Losses

► 3-Φ Integrated Buck-Boost CSI (4)

- "Synergetic" Control of Buck-Stage & CSI Stage 6-Pulse-Shaping of DC Current by Buck Stage \rightarrow Allows Clamping of a CSI-Phase

• Switching of Only 2 of 3 Phase Legs \rightarrow Significant Red. of Sw. Losses (\approx -86% for R-Load)

► 3-Φ Integrated Buck-Boost CSI (5)

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• Switching of Only 2 of 3 Phase Legs \rightarrow Significant Red. of Sw. Losses (\approx -86% for R-Load)

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Further Concepts

Quasi-2-Level FC Inverter —— Integrated Filter Power Module ———

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► Quasi-2L & Quasi-3L Inverters (1)

- Operation of N-Level Topology in 2-Level or 3-Level Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

- Reduced Average $dv/dt \rightarrow$ Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
 Low Voltage/Low R_{DS(on)}/Low \$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

► Quasi-2L & Quasi-3L Inverters (2)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

- Reduced Average $dv/dt \rightarrow$ Lower EMI / Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
 Low Voltage/R_{DS(on)}/\$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

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- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

Operation @ 3.2kW

- *Conv. Output Voltage*
- Sw. Stage Output Voltage
 Flying Cap. (FC) Voltage
 Q-FC Voltage (Uncntrl.)

- Output Current - Conv. Side Current
- Reduced Average $dv/dt \rightarrow$ Lower EMI / Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
 Low Voltage/R_{DS(on)}/\$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

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► Integrated Filter GaN Half-Bridge Module (1)

- Minimization of Filter Volume by Series & Parallel Interleaving & Extreme Sw. Frequency
- Selection of M=3 / N=3 Considering Efficiency / Filter Volume Trade-Off
- 650V GaN E-HEMT Technology
- U_{DC} =800V, P=10kW, $\Delta u_{out,pp}$ = 1%, $f_{S,eff}$ = 4.8MHz

• Design for Max. Output Frequency of $f_{out} = 100 \text{kHz}$ (!) @ Full-Scale Voltage Swing

► Integrated Filter GaN Half-Bridge Module (2)

- 10kW Demonstrator System
- 650V GaN Power Semiconductors
- Volume of ≈180cm³ (incl. Control etc.)
- $-H_2$ O Cooling Through Baseplate

Operation @ f_{out}=100kHz (f_{S,eff}= 4.8MHz)
95% calc. Efficiency

Motor-Integrated Modular Inverter

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Motor-Integrated Modular Inverter

- Machine/Inverter Fault-Tolerant VSD
- Motor-Integr. Low-Voltage Inverter Modules
- Very-High Power Density / Efficiency
 Supply of 3-Φ Winding Sets / Low C Buffer Cap.
- Rated Power $45kW / f_{out} = 2kHz$ DC-Link Voltage 1 kV

 \rightarrow Evaluate Machine Concept (PMSM vs. SRM etc.) / Wdg Topologies / Filter Requ. / etc.

 $v_{\rm dc,1H}$

 $v_{dc,1}$

 $v_{dc,1L}$

 $C_{\rm dc,1H}$

 $v_{0.1}$

Cell

H C

(a)

Filter

Filter

Filter

(b)

Motor-Integrated Inverter Demonstrator

- Rated Power 9kW @ 3700rpm DC-Link Voltage 650V...720V 3-Φ Power Cells 5+1
- Outer Diameter 220mm

- Axial Stator Mount
- 200V GaN e-FETs
- Low-Capacitance DC-Links 45mm x 58mm / Cell ____

 \rightarrow Main Challenge — Thermal Coupling/Decoupling of Motor & Inverter

—— Conclusions ——

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Conclusions

- Future Need for Single-Edged "SWISS Knife"-Type Systems feat. Multiple Tools
- Wide Input / Output Voltage Range
- Continuous / Sinusoidal Output Voltage
- Electromagnetically "Quiet" No Shielded Cables
- On-Line Monitoring / Industry 4.0
- "Plug & Play" / Non-Expert Installation
- SMART Motors
- Enabling Technologies
- SiC / GaN
- Adv. (Multi-Level) Topologies incl. PFC Rectifier
- "Synergetic" Control
- Monolithic Bidirectional GaN
- Intelligent Power Modules
- Integration of Switch / Gate Drive / Sensing / Monitoring
- Adv. Modeling / Simulation / Optimization

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System Level \rightarrow Integration of Storage, Distributed DC Bus Systems, etc.

Biography of the Presenter bortis@lem.ee.ethz.ch

Dominik Bortis received the M.Sc. and Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects.

Since January 2016 he is heading the research group Advanced Mechatronic Systems at PES, which concentrates on ultrahigh speed motors, magnetic bearings and bearingless drives, new linear-rotary actuator and machine concepts with integrated power electronics. Targeted applications include e.g. highly dynamic and precise positioning systems, medical and pharmaceutical systems, and future mobility concepts. Dr. Bortis has published 90+ scientific papers in international journals and conference proceedings. He has filed 32 patents and has received 6 IEEE Conference Prize Paper Awards.

