ETH zürich

ECPE

Expert Discussion on
"Design Automation and Next Generation
Measurement Technologies in Power Electronics"

Power Electronics Design 4.0

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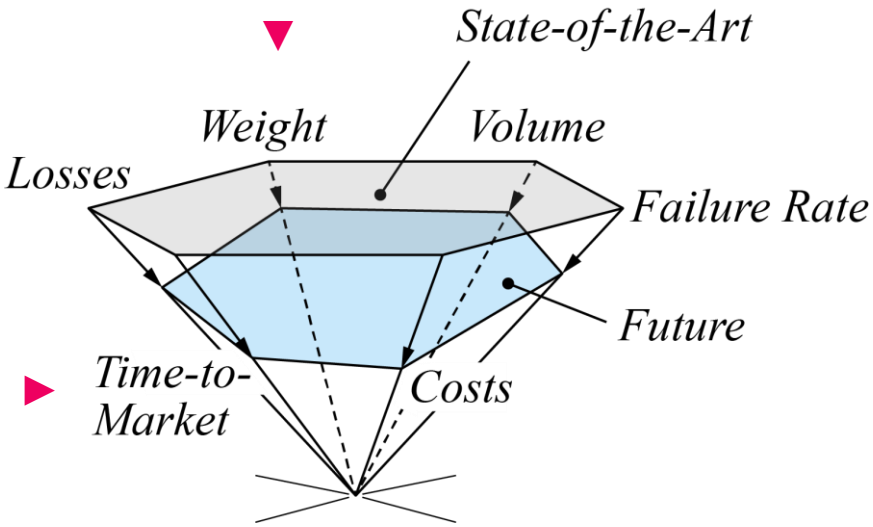
Outline

- *Power Electronics Performance Trends*
- *X-Concepts /"Moon-Shot" Technologies*
- *Power Electronics Design 4.0*

Acknowledgement: J. Azurza
T. Guillod
F. Krismer

Required Performance Improvements

Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

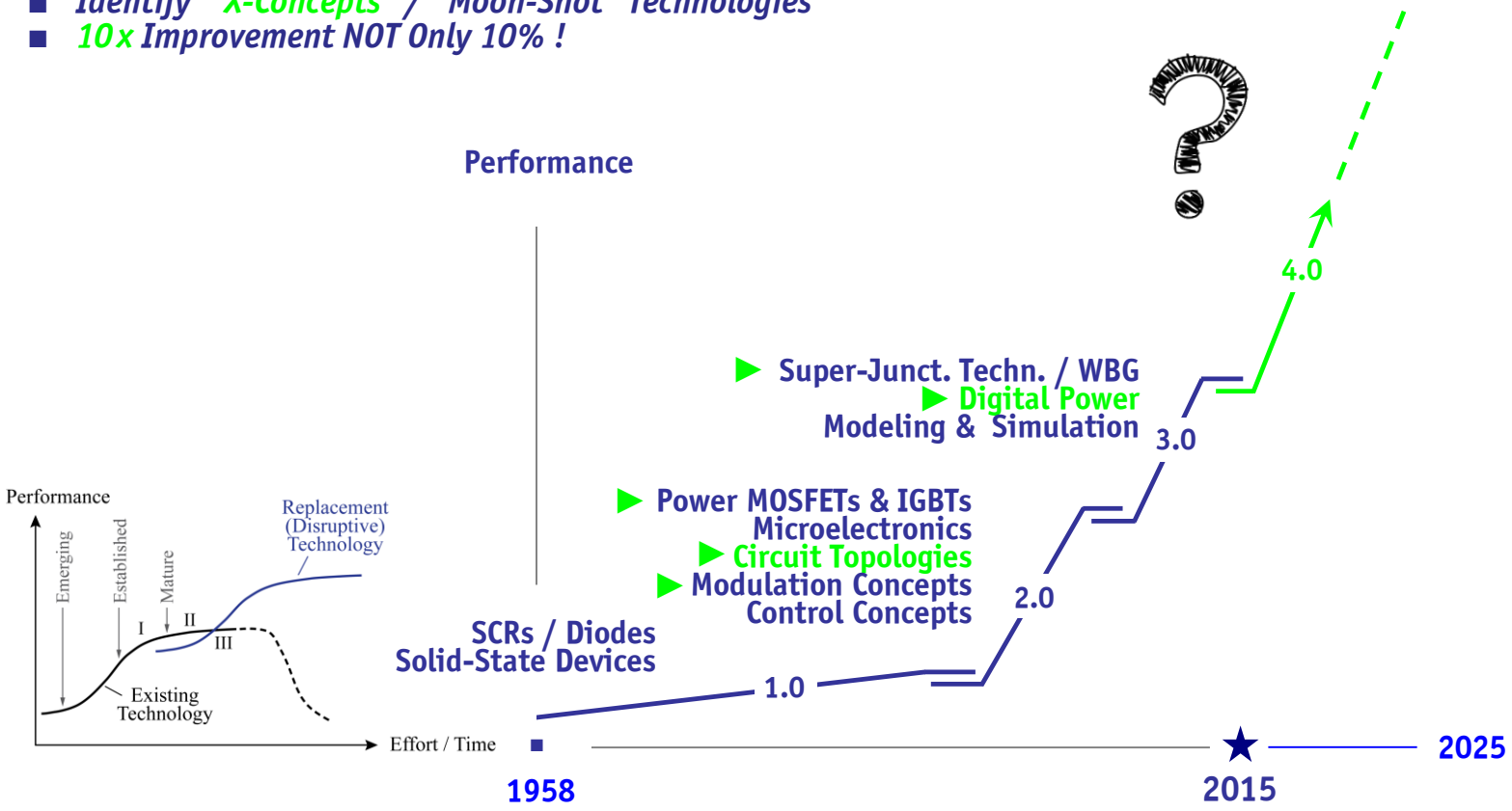


- Power Density [kW/dm^3]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]

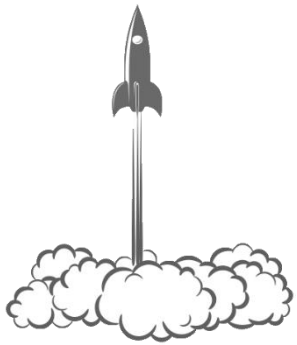
■ *Future → Cost / Cost / Cost & Robustness & Availability & Recyclability*

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*



X-Technology #1



Wide Bandgap Power Semiconductors

Low $R_{DS(on)}$ High-Voltage Devices 1/2

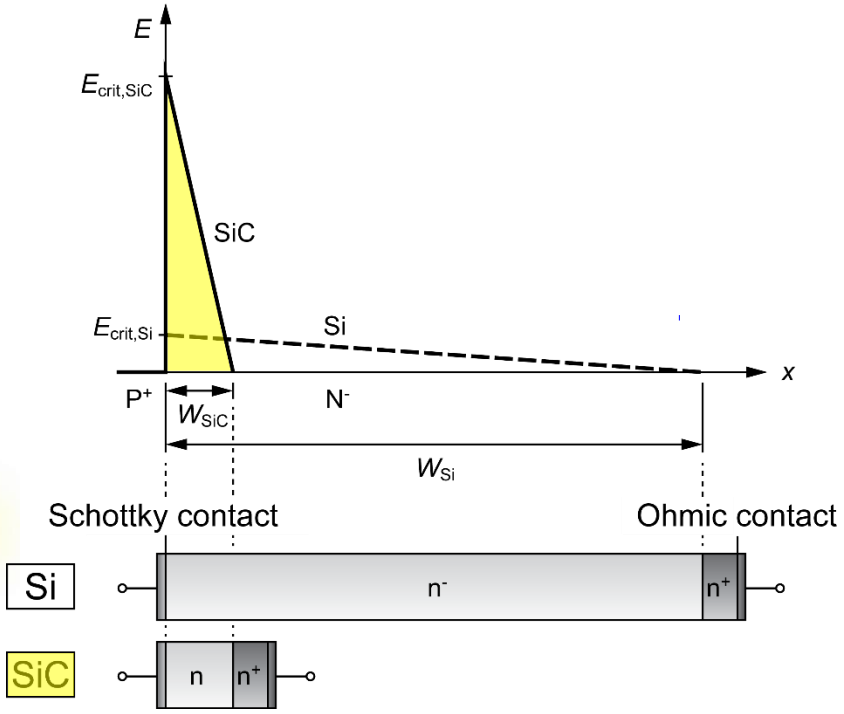
- *High Critical E-Field of SiC → Thinner Drift Layer*
- *High Maximum Junction Temperature $T_{j,max}$*

at 300 K	Si	GaAs	4H/6H-SiC	GaN
Eg (eV)	1.12	1.4	3.0-3.2	3.4
Ec (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm²/Vs)	1350	8500	100-1000	1000
ε_r	11.9	13	10	9.5
vsat (cm/s)	$1x10^7$	$1x10^7$	$2x10^7$	$3x10^7$
λ (W/cmK)	1.5	0.5	3 - 5	1.3

$$R_{on}^{*} = \frac{4V_B^2}{\varepsilon \mu_n E_C^3} \leftarrow$$

For 1kV:	Si	SiC
W (µm)	100	10
N_D (cm⁻³)	10^{14}	10^{16}

$$R_{on,SiC}^{*} \approx \frac{1}{300} R_{on,Si}^{*}$$

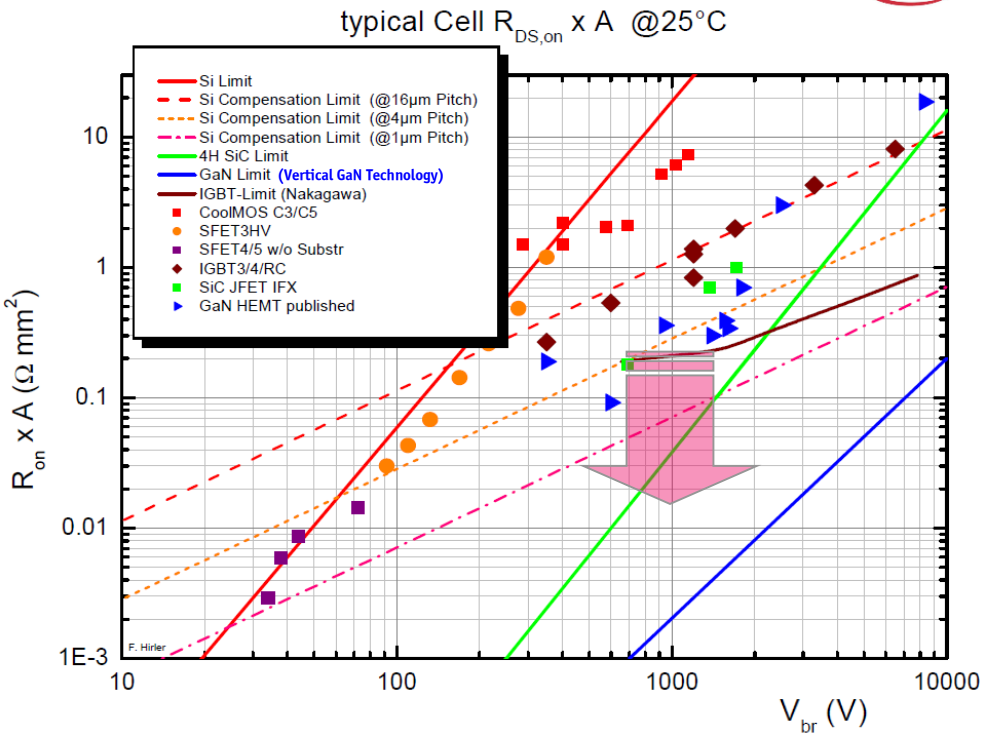


- *Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices*

Low $R_{DS(on)}$ High-Voltage Devices 2/2

- *SiC / GaN (Monolithic AC-Switch & Integration)*
- *Low Circuit Complexity*
- *High Efficiency*

Source: Infineon



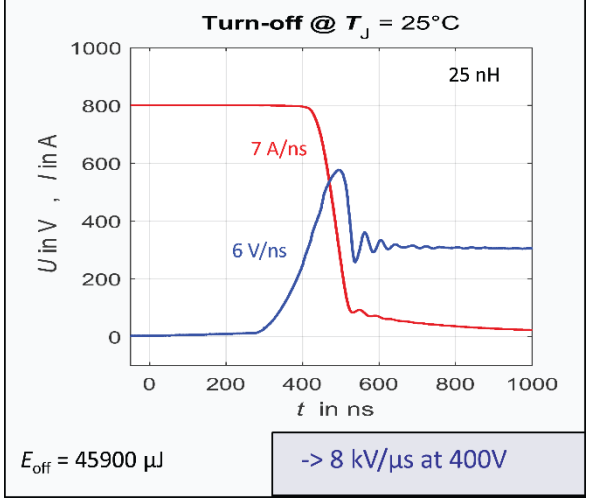
- *High Heat Conductivity & Excellent Switching Performance*

Low Switching Losses

- *Si-IGBT → Up to 6.5kV / Rel. Low Switching Speed*
- *SiC-MOSFETs → Up to 15kV (1st Samples) / Factor 10...100 Higher Sw. Speed*

Source: M. Bakran / ECPE 2019

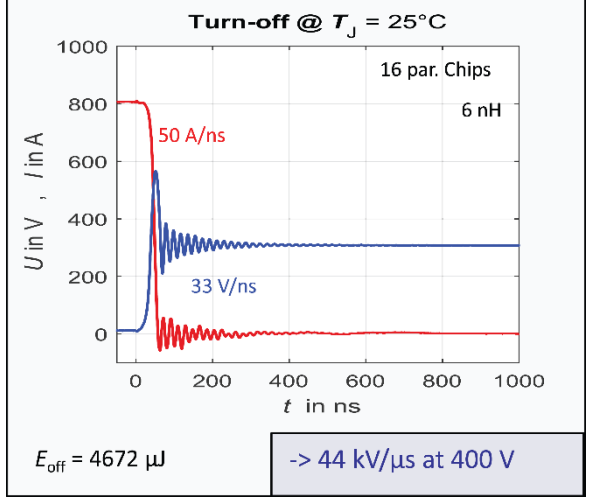
Si-IGBT / Hybrid-Pack 2



E_{off} = 45900 µJ

-> 8 kV/µs at 400V

SiC-MOSFET / (scaled for low inductance)

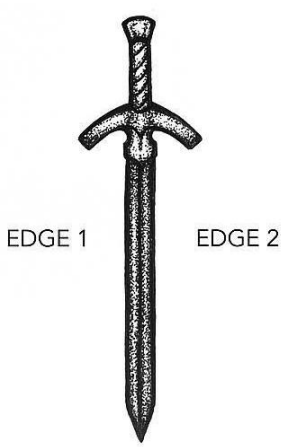


E_{off} = 4672 µJ

-> 44 kV/µs at 400 V

- *Extremely High di/dt & dv/dt → Challenges in Packaging / EMI*

Challenges



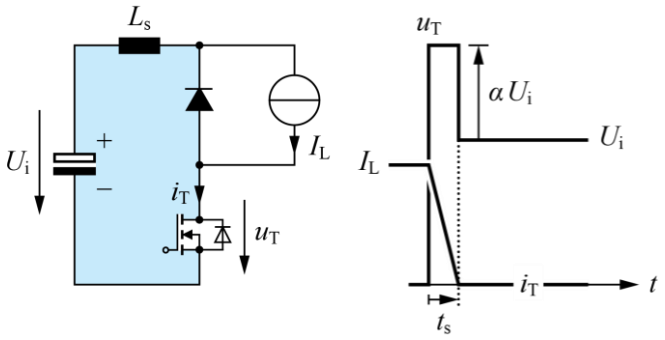
Idea: F.C. Lee

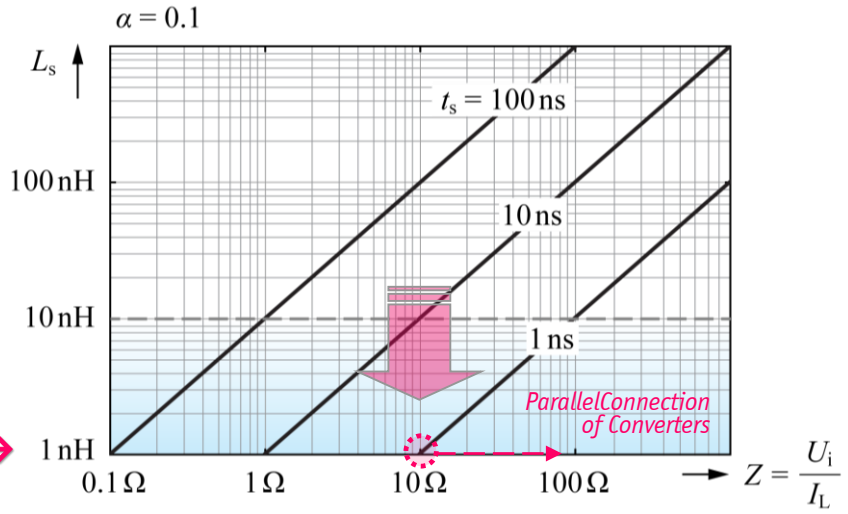
Circuit Parasitics

$$L\frac{di}{dt} = u$$

- *Extremely High di/dt*
- *Commutation Loop Inductance L_S*
- Allowed L_s Directly Related to Switching Time t_s →

$$L_s \le \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \frac{U_i}{I_L} \qquad z$$





- *Advanced Packaging / Design & Parallel Interleaving for Partitioning of Large Currents*

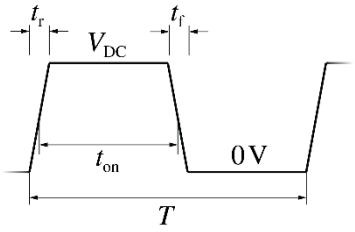
EMI Emissions

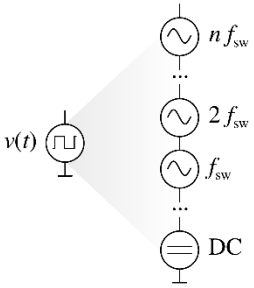
- Higher dv/dt → Factor 10
- Higher Switching Frequencies → Factor 10
- EMI Envelope Shifted to Higher Frequencies

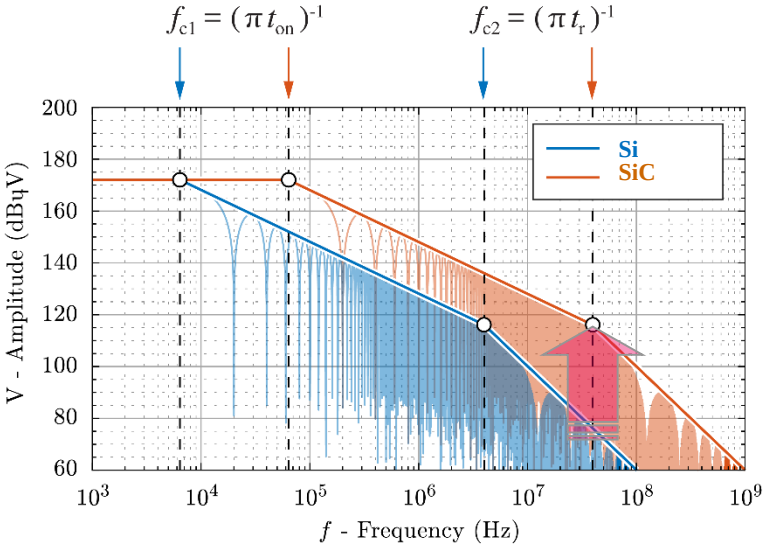
Idea: M. Schutten

f_S= 10kHz & 5 kV/us for (Si IGBT)
f_S= 100kHz & 50 kV/us for (SiC MOSFET)

V_{DC} = 800V
DC/DC @ D= 50%

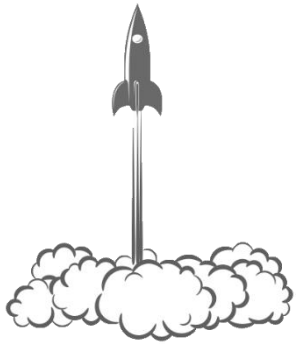






- Influence of Filter Component Parasitics and Couplings → Advanced Packaging / Design

X-Technology #2

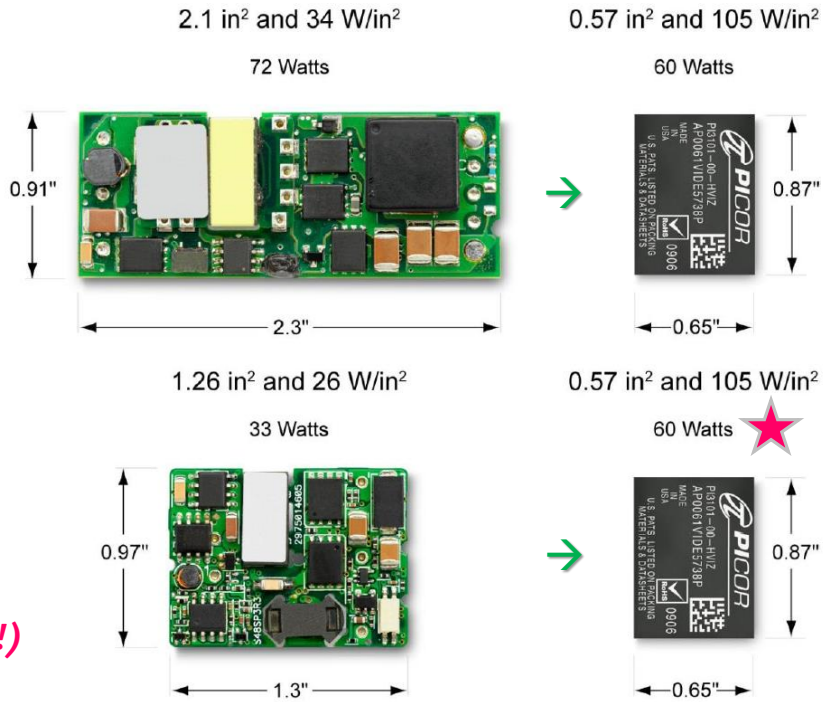


3D-Packaging
Automated Manufacturing

3D-Packaging / Heterogeneous Integration

- *System in Package (SiP) Approach*
- *Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management*
- *Very High Power Density (No Bond Wires / Solder / Thermal Paste)*
- *Automated Manufacturing*

Source: VICOR



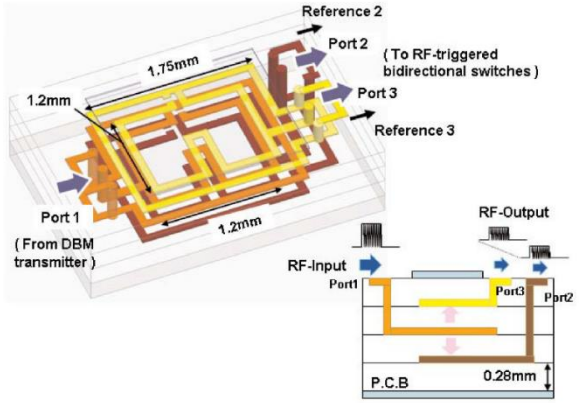
- *Future Application Up to 100kW (!)*
- *New Design Tools & Measurement Systems (!)*

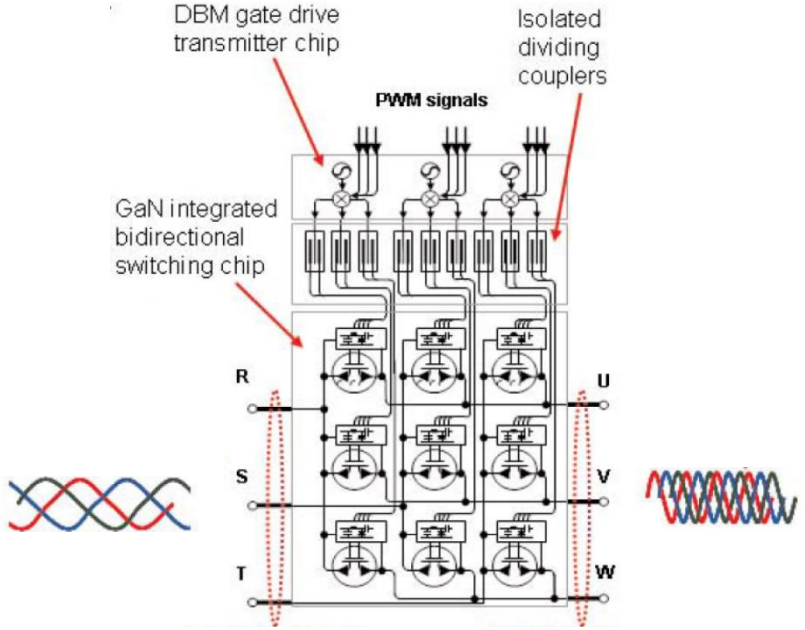
Monolithic 3D-Integration

Source: Panasonic ISSCC 2014

- GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology
  - 9 Dual-Gate GaN AC-Switches
  - DBM Gate Drive Transmitter Chip & Isolating Couplers
  - Ultra Compact → 25 x 18 mm² (600V, 10A – 5kW Motor)

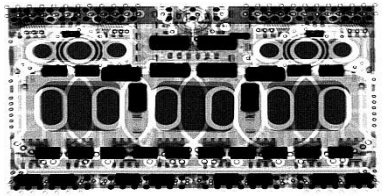
5.0GHz Isolated (5kVDC) Dividing Coupler





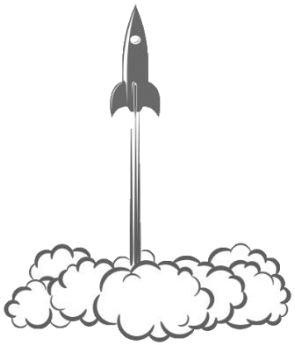
Remark – *Future Experimental Analysis*

- No Access to Inner Details / Only Terminal Waveforms Available for Measurement (!)



- *Convergence of Design / Simulation & Measurement Tools → Augmented Reality Oscilloscope*
- *Measured* Signals & *Simulated* Inner Voltages/Currents/Temp. Displayed Simultaneously
- Automatic Tuning of Simulation Parameter Models for Best Fit of Simulated/Measured Waveforms

X-Technology #3

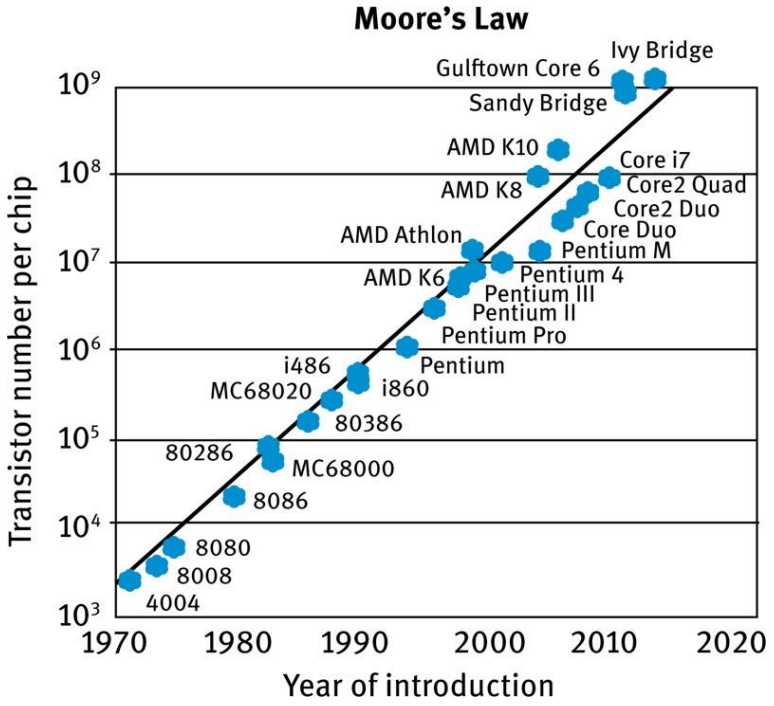


Digital Control / IIoT
Computer Based Design

Digital Integrated Circuits

- *Exponentially Improving uC / Storage Technology (!)*

— *Extreme Levels of Density / Processing Speed*
— *Software Defined Functions / Flexibility*
— *Cont. Relative Cost Reduction*



Source: Ostendorf & König /DeGruyter

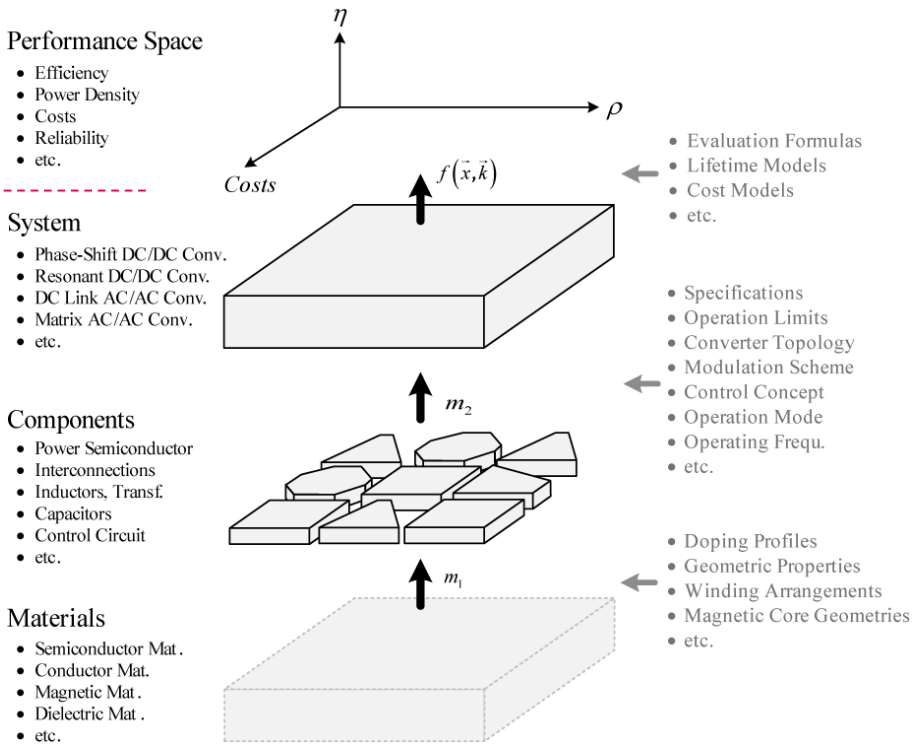
- *Fully Digital Control of Complex Systems (Capability of Managing Complexity)*
- *Massive Comput. Power & Cloud → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)*

Automated Design

Automated Design 1/4

Performance Space

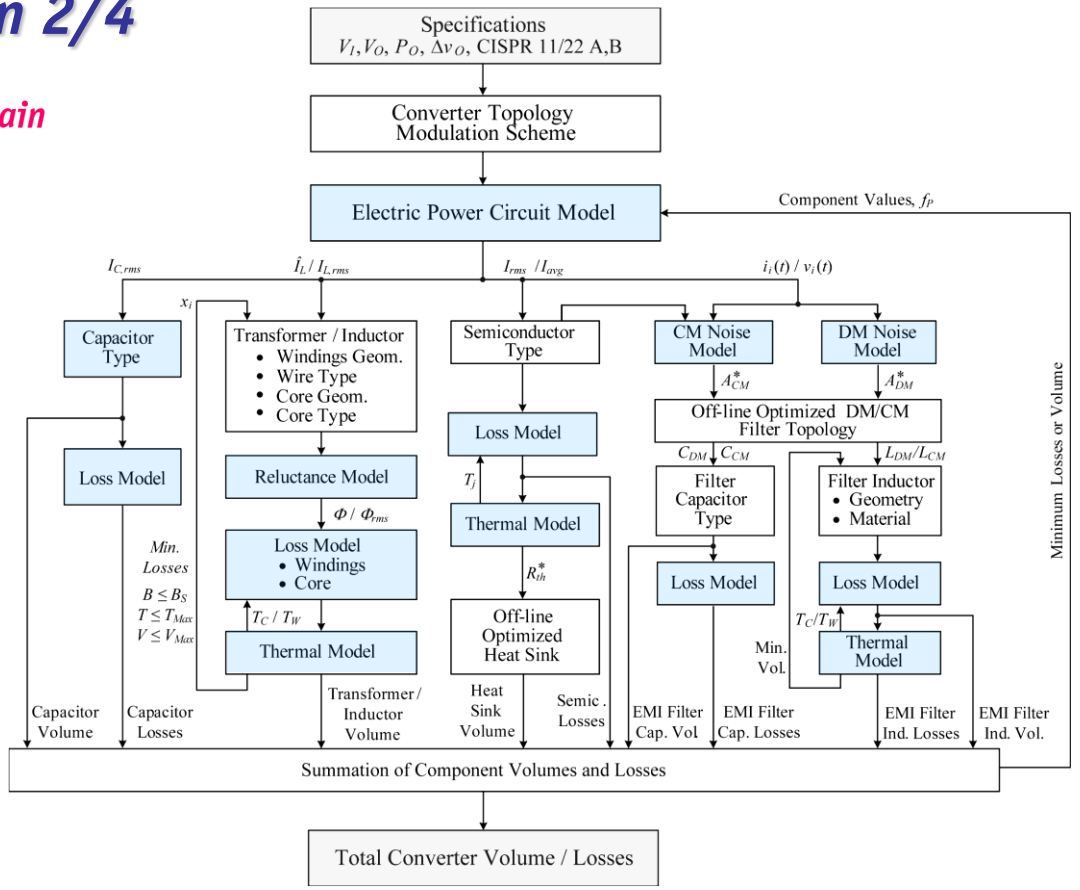
Design Space



- *Mathematical Description of the Mapping "Technologies" → "System Performance"*

Automated Design 2/4

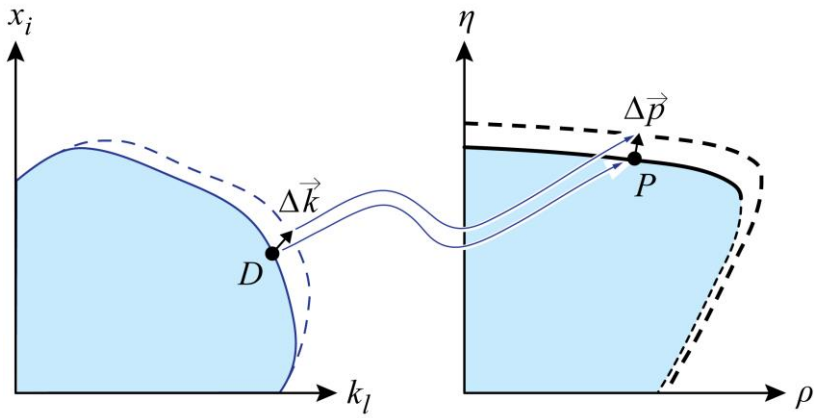
- *Mathematical Models of Main Converter Components & Interactions*



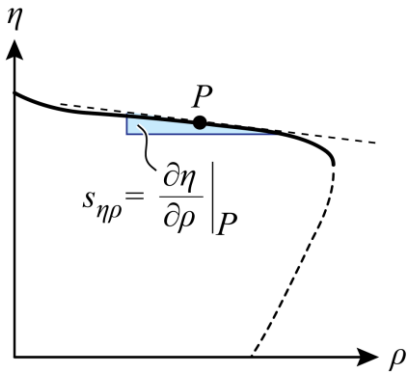
- **Multi-Objective Optimization** – *Guarantees Best Utilization of All Degrees of Freedom* (!)

Automated Design 3/4

- *Based on Mathematical Model of the Technology Mapping*
- *Multi-Objective Optimization → Best Utilization of the "Design Space"*
- *Identifies Absolute Performance Limits → Pareto Front / Surface*



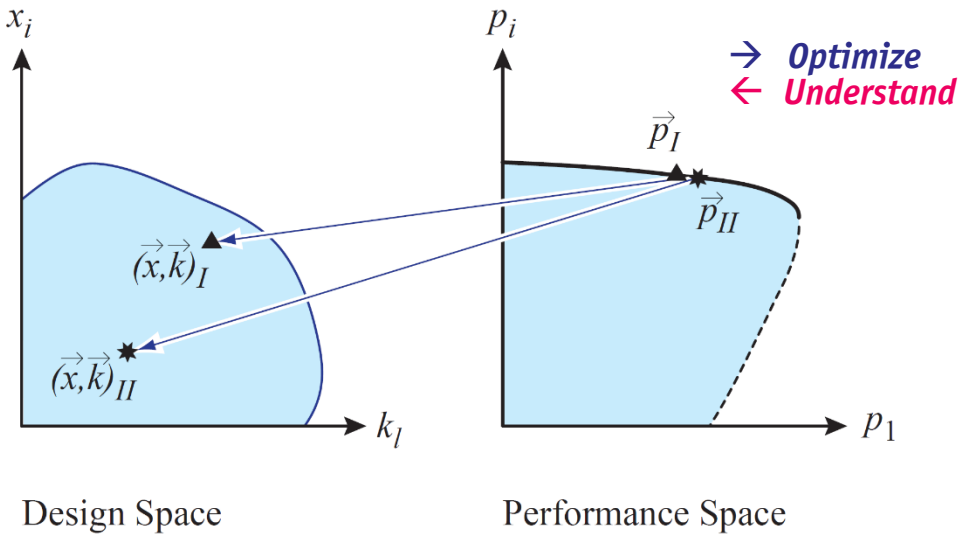
Design Space Performance Space



- *Clarifies Sensitivity $\Delta\vec{p}$ / $\Delta\vec{k}$ to Improvements of Technologies & Power Density Limit*
- *Trade-Off Analysis*

Automated Design 4/4

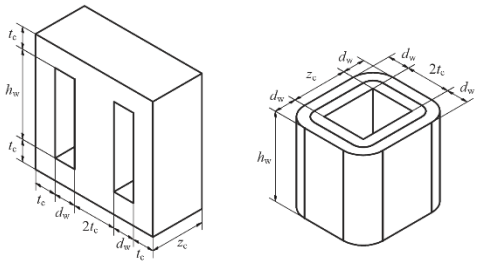
- *Design Space Diversity*
- *Equal Performance for Largely Different Sets of Design Parameters (!)*



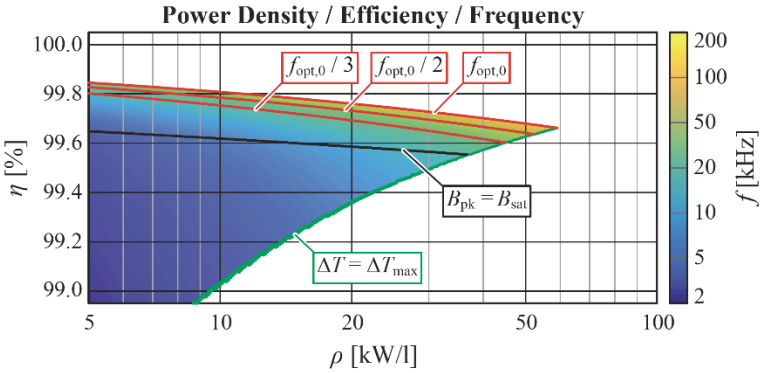
- *E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)*
- *Allows Optimization for Further Performance Index (e.g. Costs)*

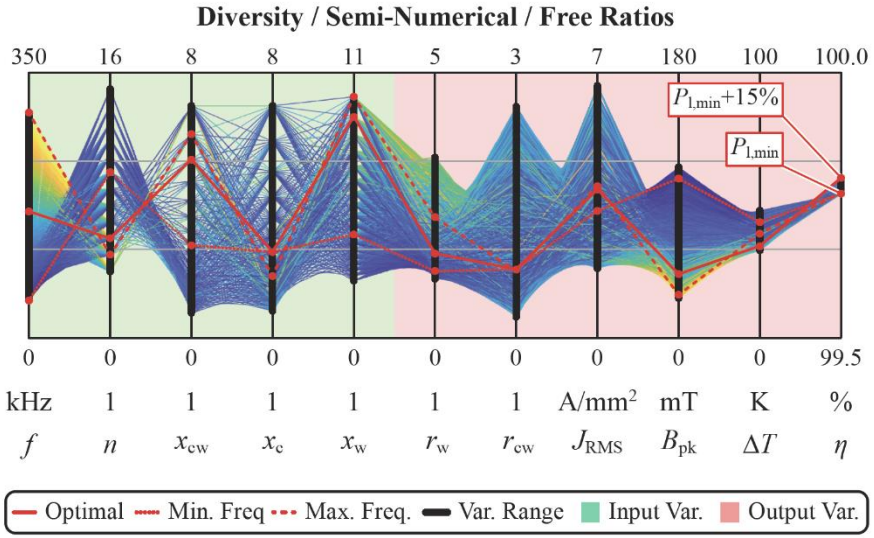
Design Space Diversity - Example

- *Design of a Medium-Frequency Transformer*
- *Wdg./Core Loss Ratio, Geometry, n etc. as Design Parameters*
- *Power Level & Power Density = const.*



Source: T. Guillod / ETH



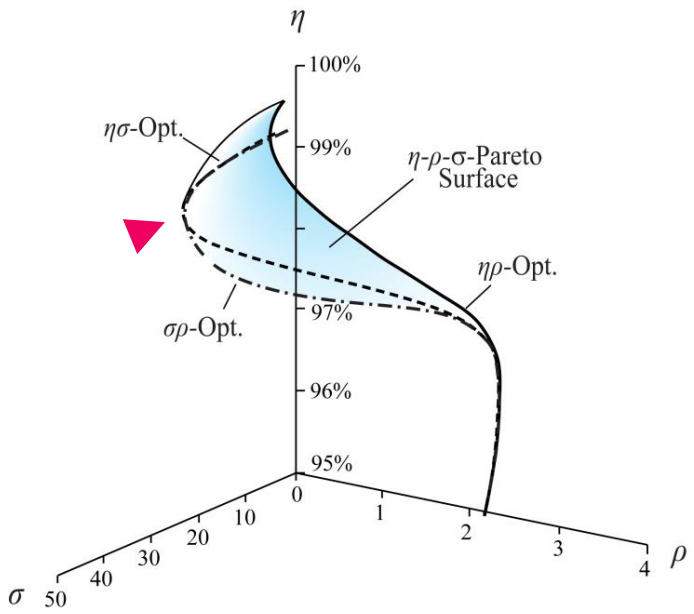


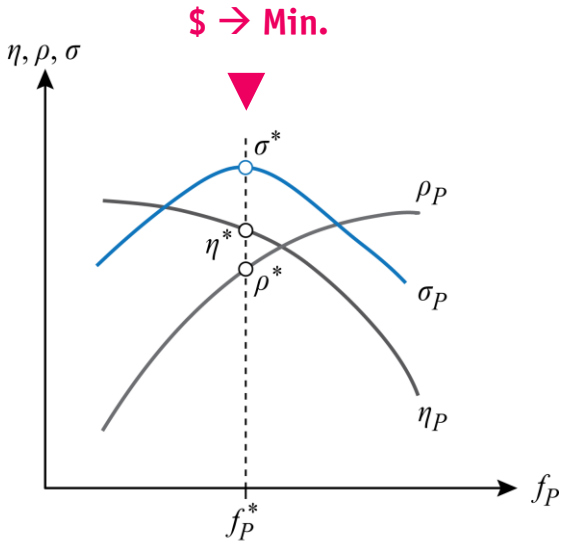
$$x_{cw} = A_c / A_w, \quad x_c = z_c / 2\,t_c, \quad x_w = h_w / d_w$$

- *Mutual Compensation Core & Winding Losses Changes*
- *Limit on Part Load Efficiency / Costs / Fixed Geometry → Restricts Diversity*

Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- *Definition of a Power Electronics "Technology Node" → (η^*,ρ^*,σ^*,f_P^*)*
- *Maximum σ [kW/$], Related Efficiency & Power Density*





- *Specifying Only a Single Performance Index is of No Value (!)*
- *Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)*

Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- *Definition of a Power Electronics "Technology Node" → (η^*,ρ^*,σ^*,f_P^*)*
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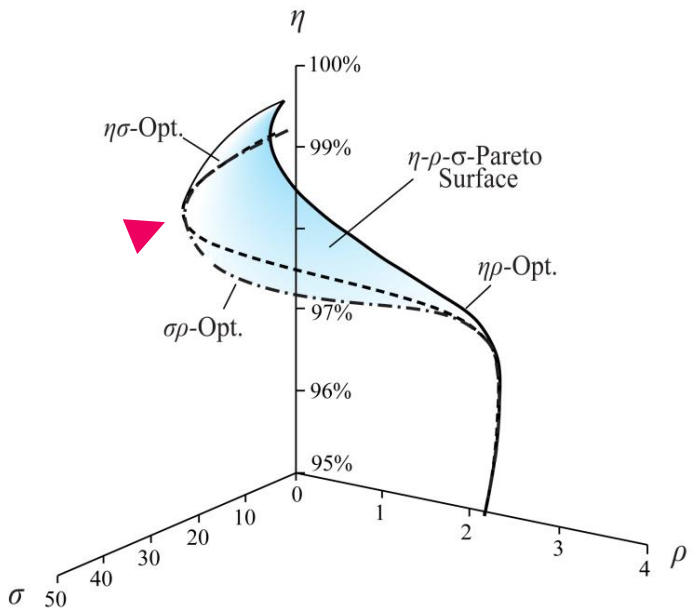

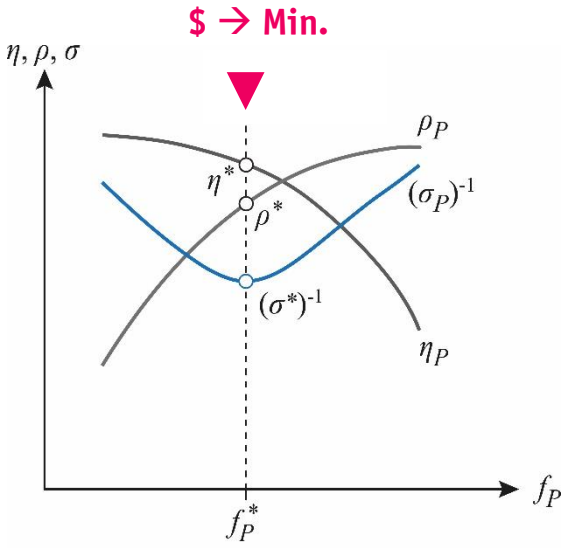

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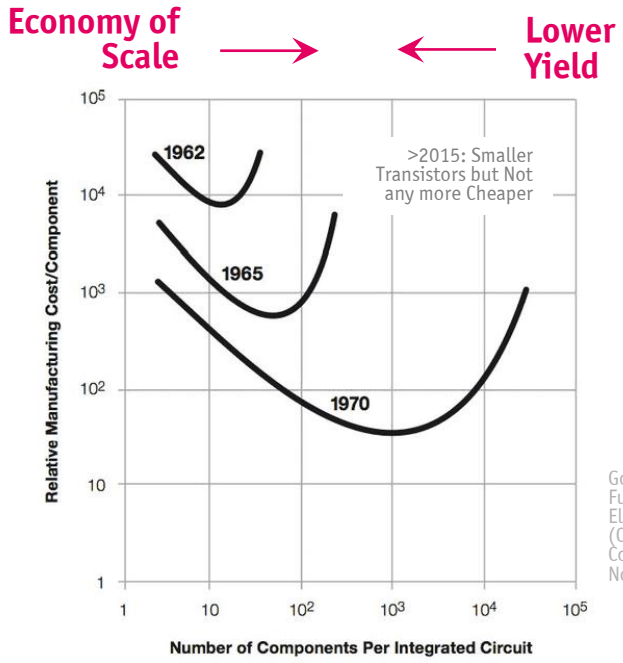
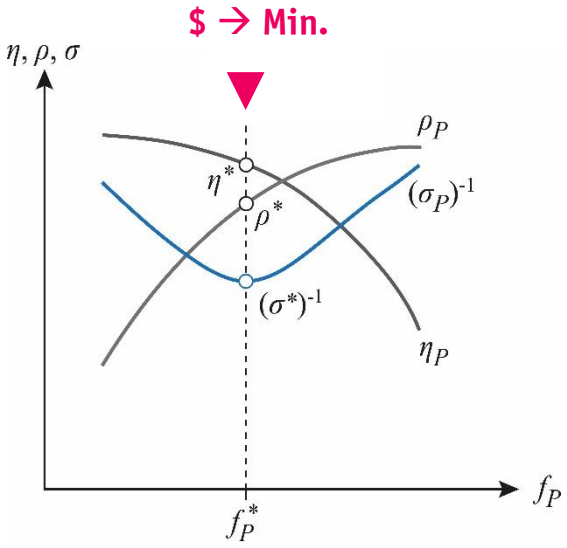
Comparison to "Moores Law"

- *"Moores Law" Defines Consecutive Techn. Nodes Based on Min. Costs per Integr. Circuit (!)*
- *Complexity for Min. Comp. Costs Increases approx. by Factor of 2 / Year*



Gordon Moore: The Future of Integrated Electronics, 1965 (Consideration of Three Consecutive Technology Nodes)

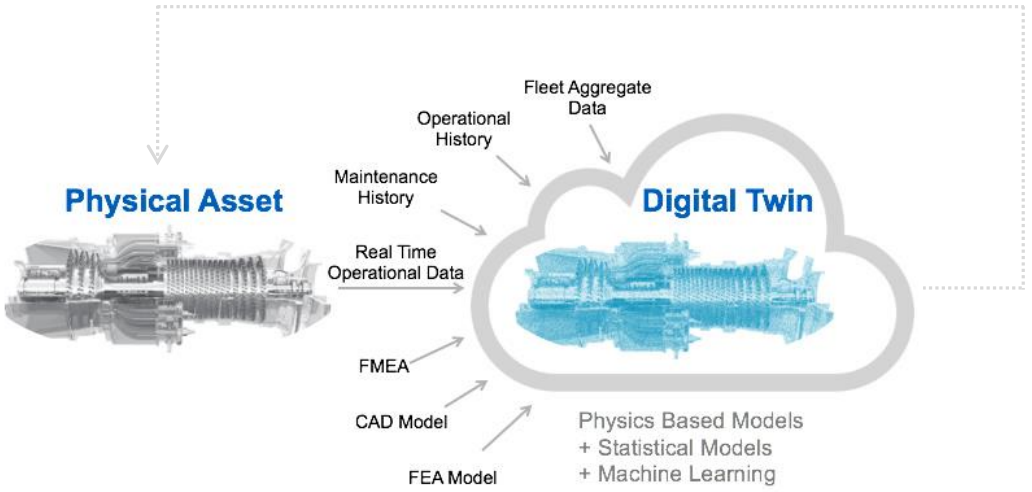


- *Definition of "η*,ρ*,σ*,f_P*–Node" Must Consider Conv. Type / Operating Range etc. (!)*

Digital Twin / Industry 4.0

IIoT in Power Electronics

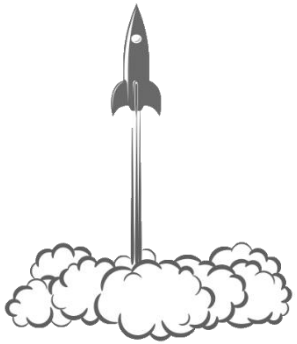
- *Digital Twin → Physics-Based Digital Mirror Image*
- *Digital Thread → "Weaving" Real/Physical & Virtual World Together*



Source: www.railwayage.com

- *Requires Proper Interfaces for Models & Automated Design*
- *Model of System´s Past/Current/Future State → Design Corrections / Prev. Maintenance etc.*

X-Technology #4



Interleaving & Modularity

History and Development of the Electronic Power Converter

E. F. W. ALEXANDERSON
FELLOW AIEE

E. L. PHILLIPI
NONMEMBER AIEE

THE TERM "electronic power converter" needs some definition. The object may be to convert power from direct current to alternating current for d-c power transmission, or to convert power from one frequency into another, or to serve as a commutator for operating an a-c motor at variable speed, or for transforming high-voltage direct current into low-voltage direct current. Other objectives may be mentioned. It is thus evidently not the objective but the means which characterizes the electronic power converter. Other names have been used tentatively but have not been accepted. The emphasis is on electronic means and the term is limited to conversion of power as distinguished from electric energy for purposes of communication. Thus the name is a definition.

Paper 44-143, recommended by the AIEE committee on electronics for presentation at the AIEE summer technical meeting, St. Louis, Mo., June 26–30, 1944. Manuscript submitted April 25, 1944; made available for printing May 18, 1944.

E. F. W. ALEXANDERSON and E. L. PHILLIPI are with the General Electric Company, Schenectady, N. Y.

1944 !

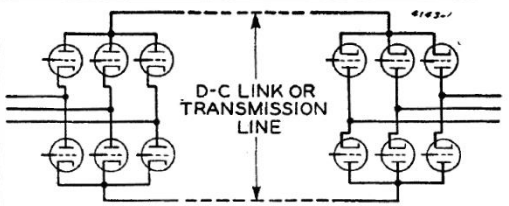


Figure 1. Electronic converter, dual-conversion type

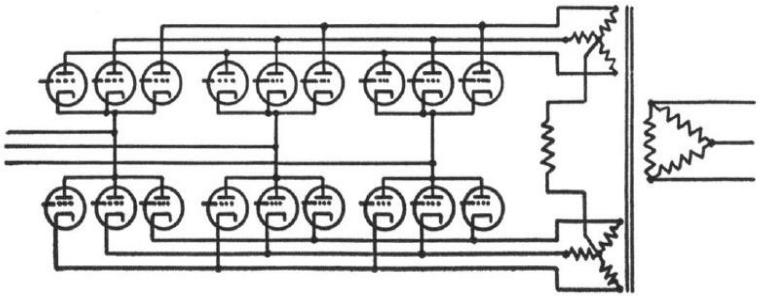
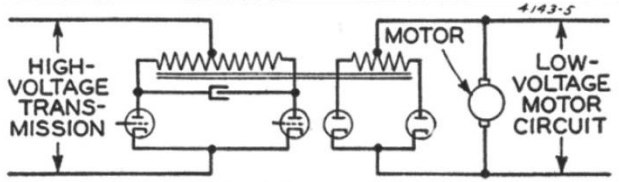


Figure 4 (left). Single-conversion-type frequency changer

Figure 5 (below). D-c transformer



- *Basic Topologies Known > 30...40 Years*
- *Min. Complexity Circuits Used in Industry*
- *Optimization of Modulation / Control "Completed"*
- *Several Solutions of Equal Performance*

SCC ... Switched Capacitor Converters

... "Refinements" & Interleaving & Hybrid SCCs & Comparative Evaluation (!)

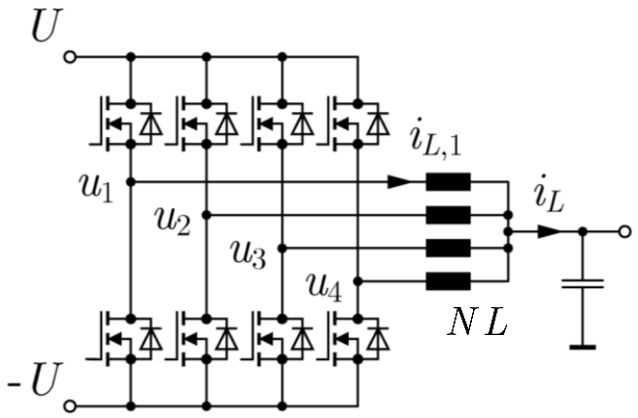
Parallel Interleaving 1/2

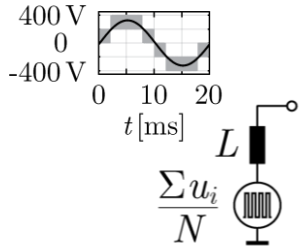
- *Loss-Neutral Multiplication of Switching Frequency*
- *Reduced Ripple @ Same (!) Switching Losses*

$$f_{S,\mathrm{eff}} = N \cdot f_S$$

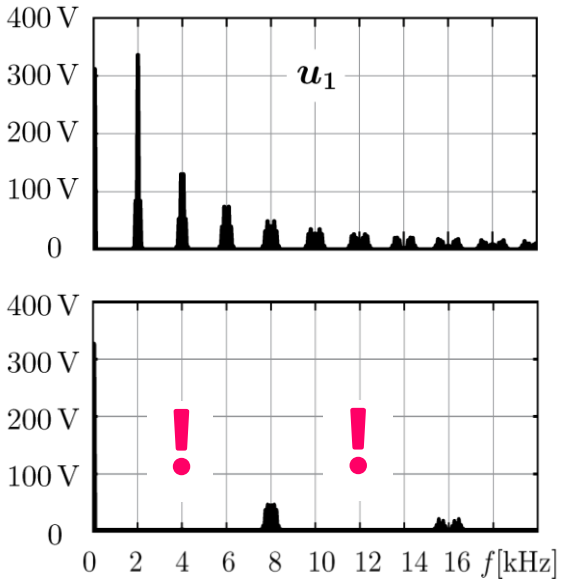
$$\Delta I_{\max,N} = \frac{1}{N^2} \Delta I_{\max,N=1}$$

$$\Delta U_{\max,N} = \frac{1}{N^3} \Delta U_{\max,N=1}$$





N = 4



- *Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy*

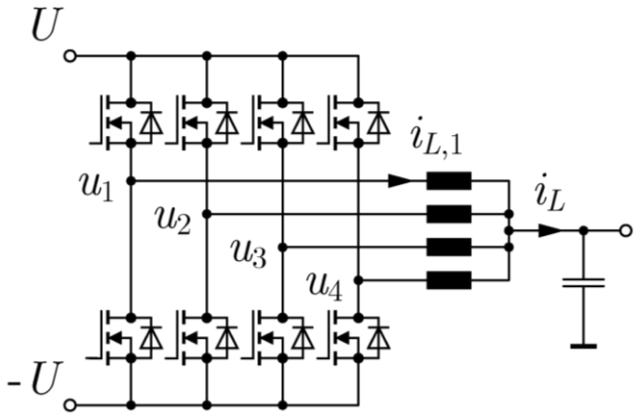
Parallel Interleaving 2/2

- *Loss-Neutral Multiplication of Switching Frequency*
- *Reduced Ripple @ Same (!) Switching Losses*

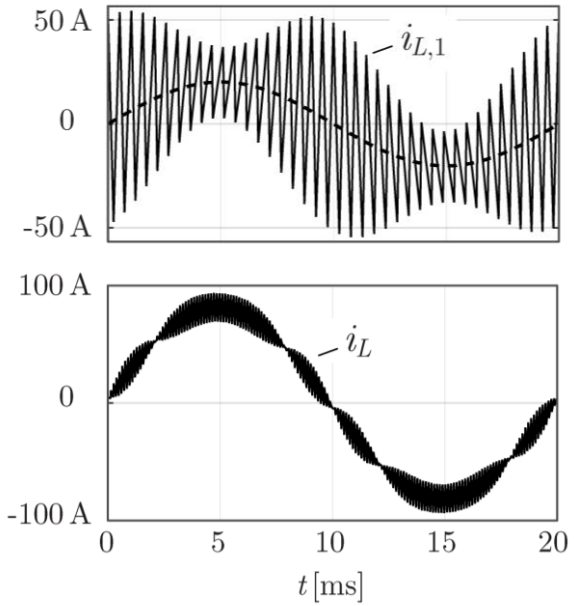
$$f_{S,\mathrm{eff}} = N \cdot f_S$$

$$\Delta I_{\max,N} = \frac{1}{N^2} \Delta I_{\max,N=1}$$

$$\Delta U_{\max,N} = \frac{1}{N^3} \Delta U_{\max,N=1}$$



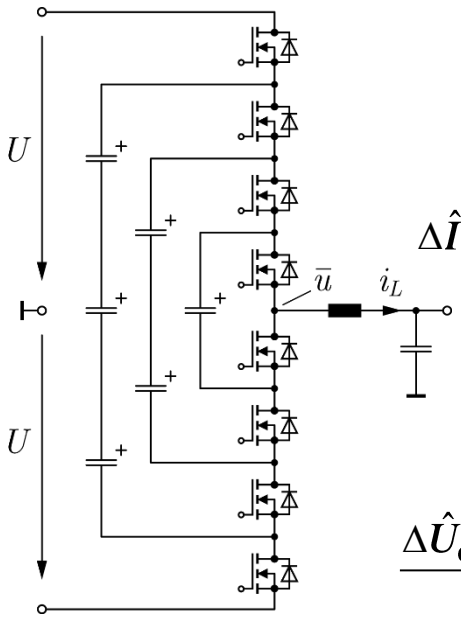
N = 4



- *Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy*

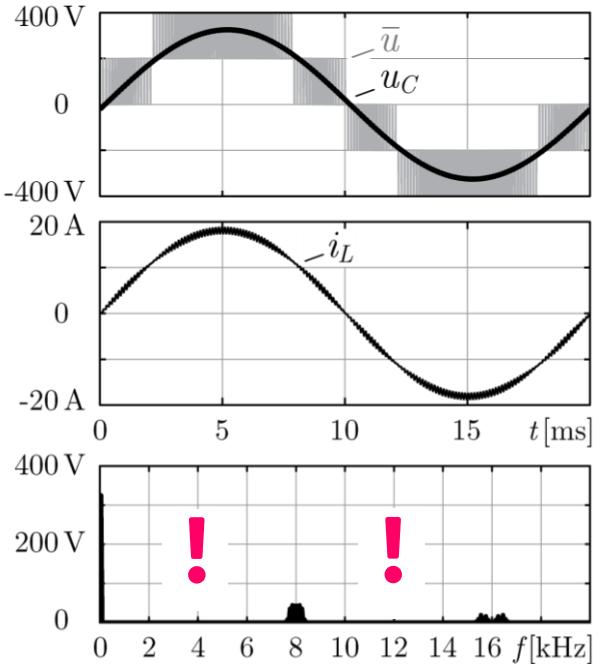
Series Interleaving 1/2

- *Reduced Ripple @ Same (!) Switching Losses*
- *Lower On-Resistance @ Given Blocking Voltage → 1+1=2 NOT $2^2 = 4$ (!)*
- *Extends LV Technology to HV*



$$\Delta\hat{I}_{\max,N} = \frac{1}{N^2}\Delta\hat{I}_{\max,N=1} \quad \Big/ \quad \frac{U}{8 f_s L}$$

$$\frac{\Delta\hat{U}_{C,\max,N}}{U} = \frac{\pi^2}{32}\left(\frac{f_O}{f_S}\right)^2 \frac{1}{N^3}$$

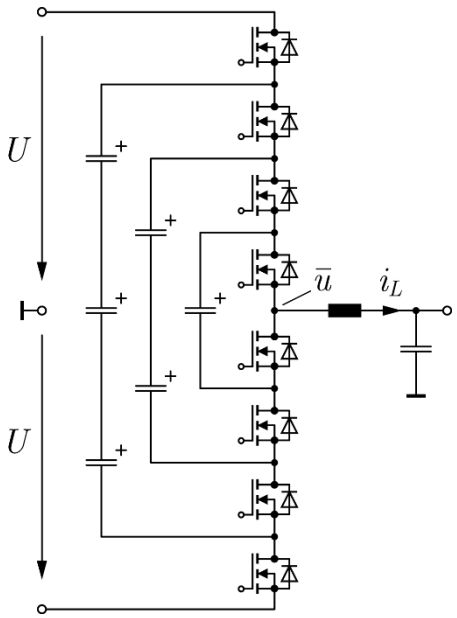


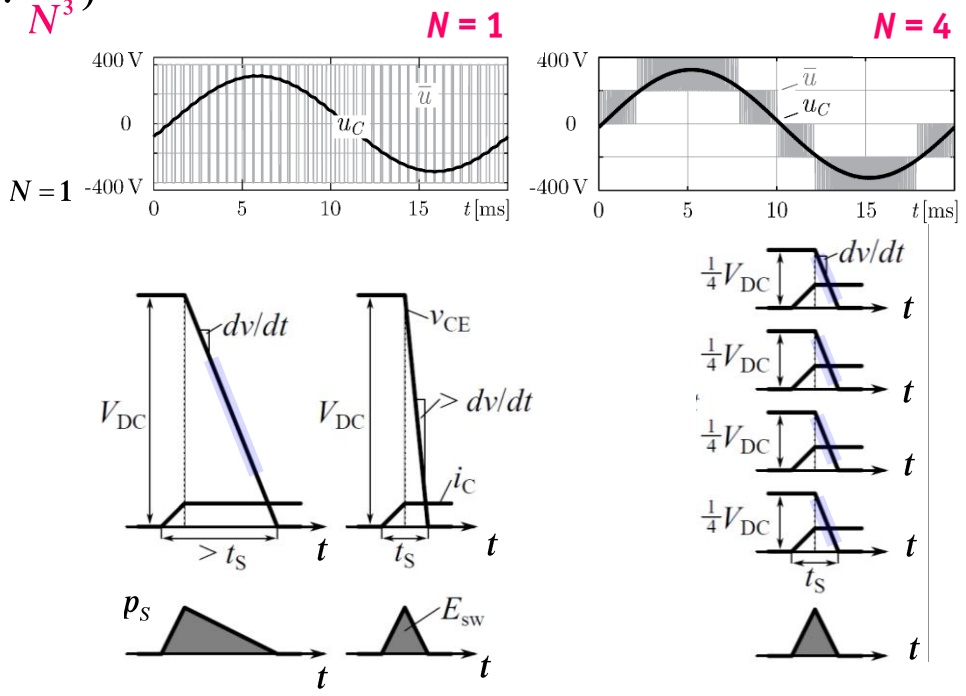
- *Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy*

Series Interleaving 2/2

- *Dramatically Reduced Switching Losses (or Harmonics) for Same* di/dt *and* dv/dt

$$P_{S,N} \approx P_{S,N=1}\left(\frac{1}{2N^2} \cdots \frac{1}{N^3}\right)$$

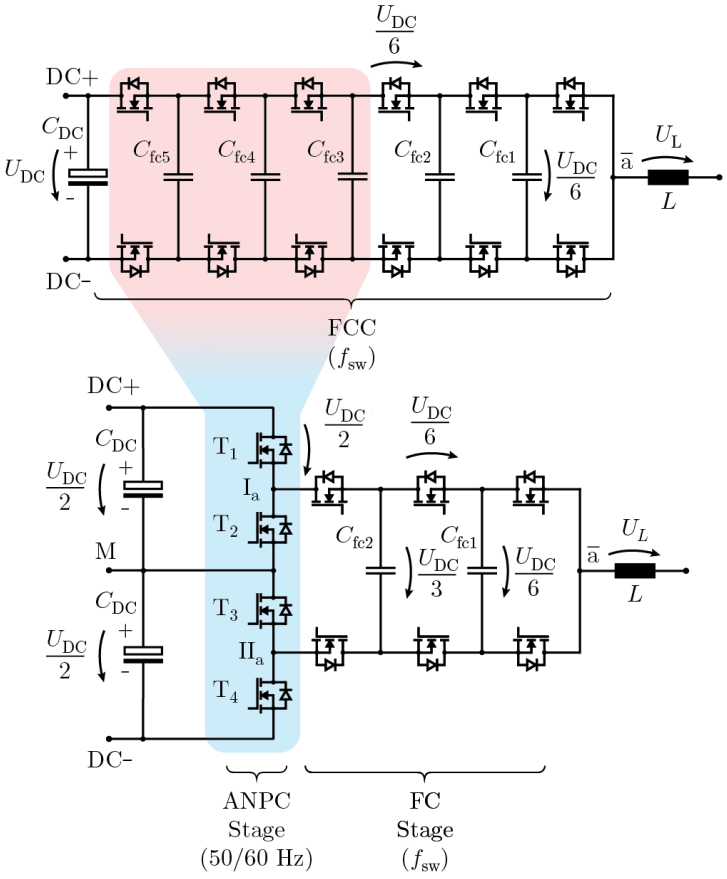


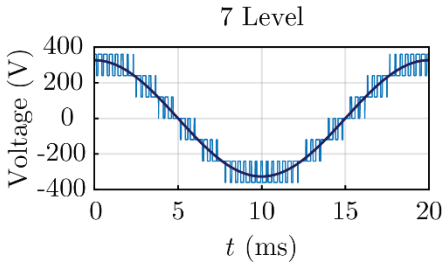


- *High Efficiency @ High Effective Switching Frequency → High Power Density*

Series Interleaving – Example

- *Realization of a 99%++ Efficient 10kW 3-Φ 400V$_{rms,ll}$ Inverter System*
- *7-Level Hybrid Active NPC Topology / LV Si-Technology*



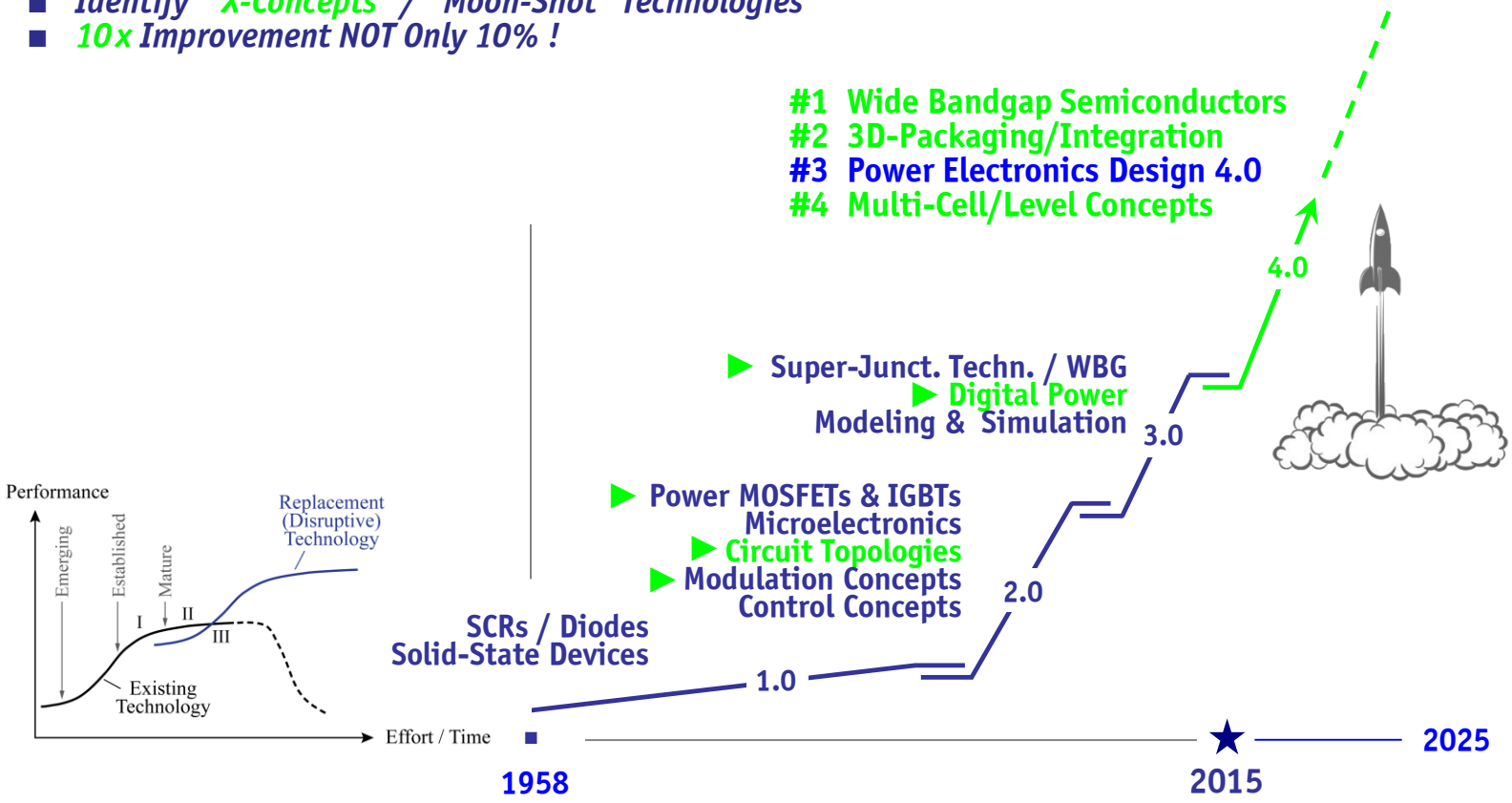


99.35%
2.6kW/kg
56 W/in^3


FUTURE

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*



Automated Design Roadmap

- *End-to-End Horizon of Modeling & Simulation*
- *Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling*

Autonomous Design → Design 4.0
– *Independent* Generation of Full Designs for Final Expert Judgement

Augmented Design
– *Suggestion* of Design Details Based on Previous Designs

Assisted Design
– *Support* of the User with Abstracted Database of Former Designs

State-of-the-Art
– *User Defined* Models and Simulation / Fragmented

- *AI-Based "Summaries" → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)*

Conclusions

- **Challenges in *Modeling & Simulation***

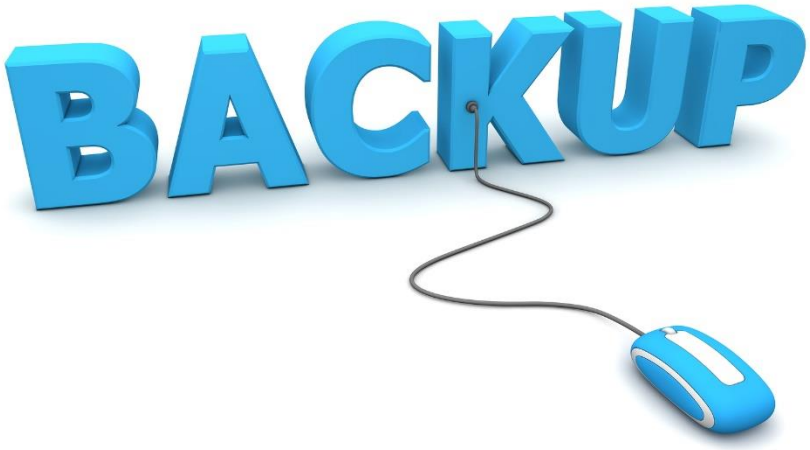
- *Improvement & Combination of Analytic, Equiv. Circuit, FEM, Hybrid Red. Order Models*
- *Models in Certain Areas Largely Missing (Costs, EMI, Reliability, Manufacturability, etc.)*
- *Strategies for Hierarchical Structuring of Modeling (Doping Profile → Mission Profile)*
- *Strategies for Comput. Efficient Design Space Exploration & Multi-Obj. Simulation*
- *Sensitivity of Performance Prediction to Model Inaccuracies Largely Unknown*
- *Design Space Diversity and Performance Sensitivities Not Utilized*
- *AI Not Yet Utilized*

- **Challenges of *Company-Wide Introduction***

- *No Readily Available Software*
- *Company-Wide Model Updates & Software Updates*
- *Complete Restructuring of Engineering Departments*
- *License Costs*
- *etc.*

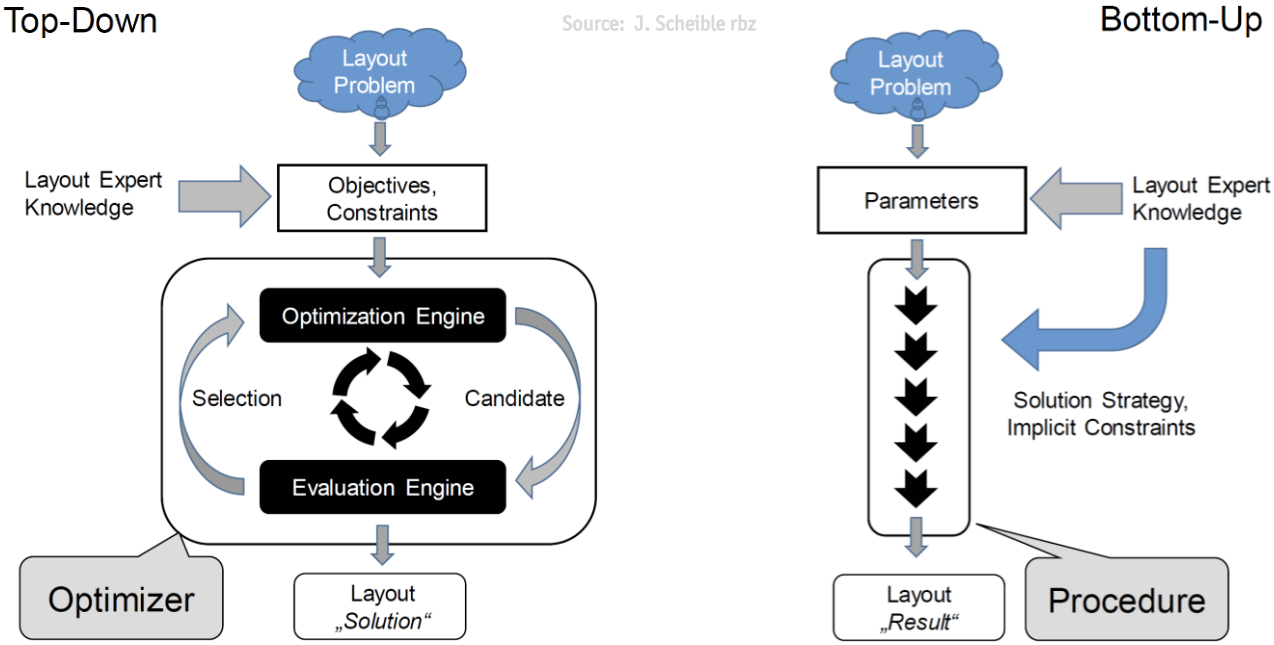
… "The Train Has Just Left the Station" (!)

Thank you!


BACKUP

Manual Design Automation Strategies

- *Example of Analog Integrated Circuit Design Automation*
- *"Top-Down" Optimization (Repetitive Refinement) vs. "Bottom-Up" Procedures*



- *Top-Down → Limited to Aspects Described in the Models / All Parasitics Must be Modelled !*
- *Bottom-Up → Manual Design Process Translated into Executable Script Steered by an Expert*

Power Electronics → Energy Electronics

Source:
www.roadtrafficsigns.com

"Energy" Electronics

- Design Considering Converters as "Integrated Circuits" (PEBBs)
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

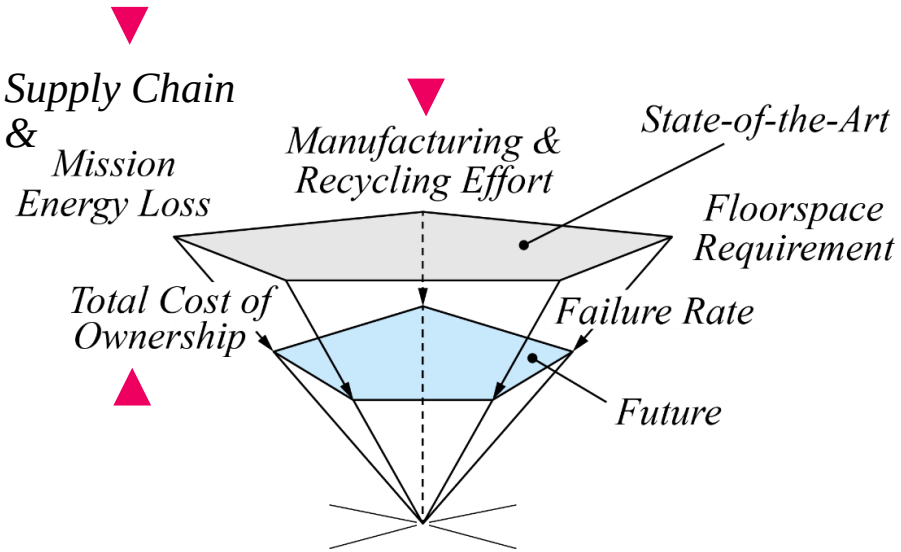
- "Converter" → "Systems" (Microgrid) or "Hybrid Systems" (Automation / Aircraft)
- "Time" → "Integral over Time"
- "Power" → "Energy"

$$p(t) \rightarrow \int_0^t p(t)\,\mathrm{d}t$$

- Power Conversion → Energy Management / Distribution
- Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
- Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
- Cap. Filtering → Energy Storage & Demand Side Management
- Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
- etc.

New Power Electronics Systems Performance Figures/Trends

- Complete Set of New Performance Indices
  - Power Density [kW/m²]
  - Environm. Impact [kWs/kW]
  - TCO [$/kW]
  - Mission Efficiency [%]
  - Failure Rate [h⁻¹]



End