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Power Electronic Systems Laboratory

Evaluation of a Hybrid Multi-Level Flying-Capacitor Bridge-Leg Topology for Beyond 99% Power Conversion Efficiency

Jon Azurza et al.

Swiss Federal Institute of Technology (ETH) Zurich

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J. Azurza, M. Guacci, D. Neumayr, J. W. Kolar
Swiss Federal Institute of Technology (ETH) Zurich
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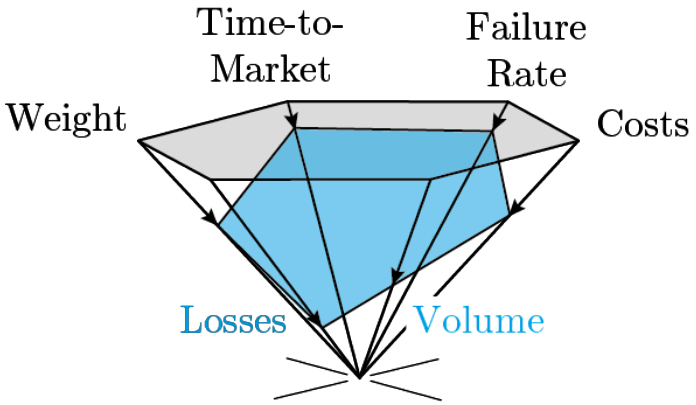
In collaboration with:

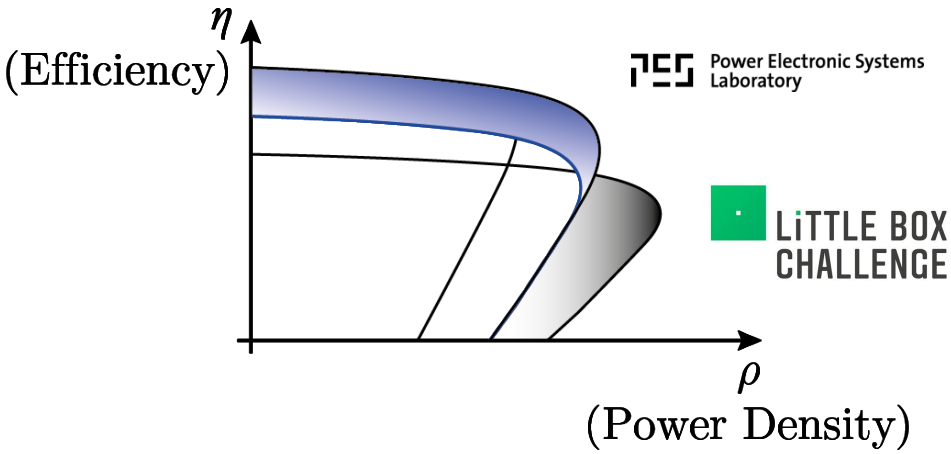
Infineon

Feb. 20th, 2019

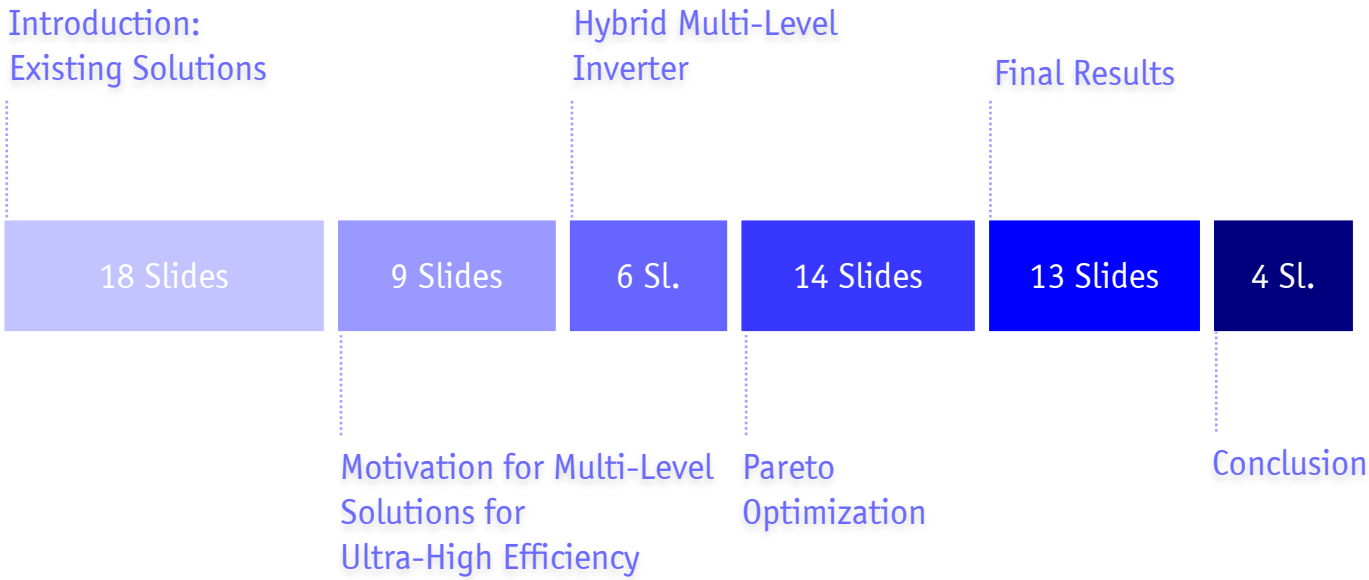
Acknowledgements: K. L. Pally

▶Towards Ultra-High Efficiency





Agenda


Introduction: Existing Solutions
Hybrid Multi-Level Inverter
Final Results
18 Slides
9 Slides
6 Sl.
14 Slides
13 Slides
4 Sl.
Motivation for Multi-Level Solutions for Ultra-High Efficiency
Pareto Optimization
Conclusion

Pushing the Barriers: Existing Solutions

- *Ultra-High Efficiency*
- *Ultra-High Power Density*

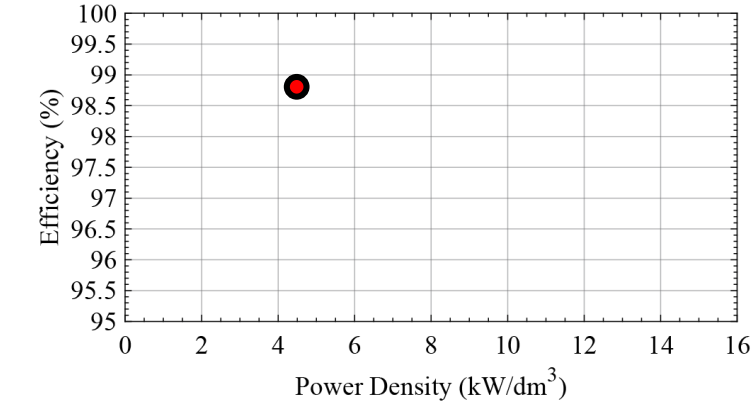
▶Ultra-High Efficiency (1)

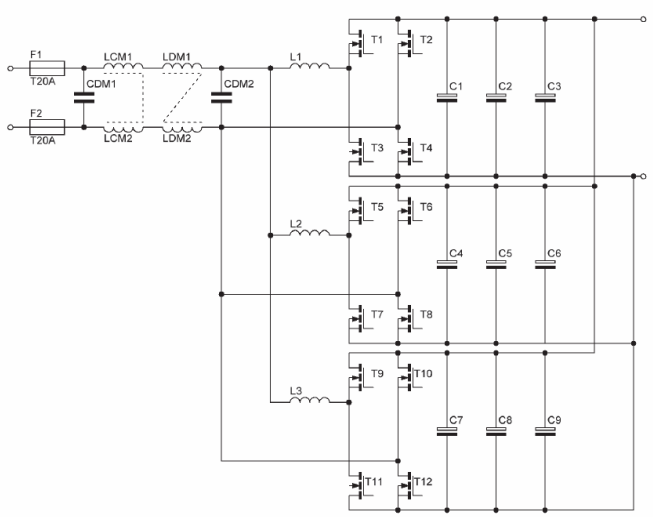
➢ Boost-Type TCM PFC Rectifier – ETH Zurich

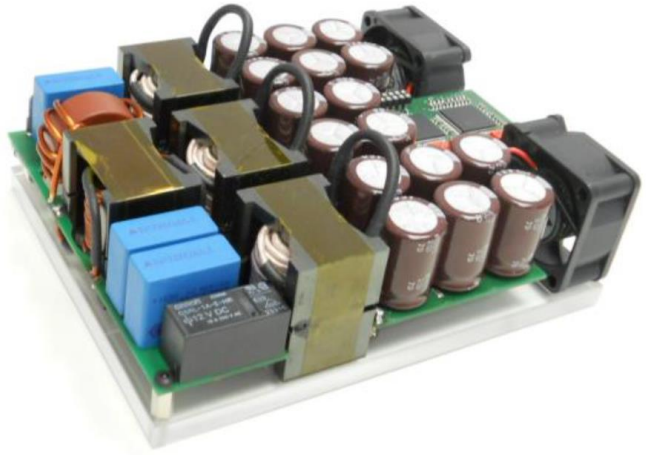
- Input Voltage: 184...264V_{AC}
- Output Voltage: 400 V_{DC}
- Rated Power: 3.3 kW

■ Triple-Interleaved Topology

- 4.5kW/dm³ (73.8W/in³)
- 15.0cm x 12.0cm x 4.0cm
- 98.8% Peak Efficiency





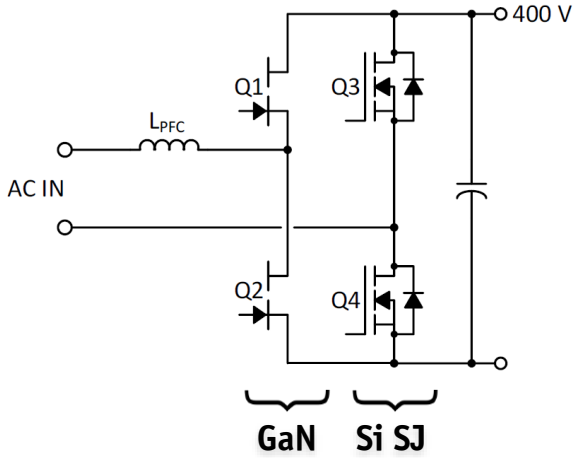


▶ Ultra-High Efficiency (2)

➢ Infineon PFC Rectifier Evaluation Board

- Input Voltage: $85...265V_{AC}$
- Output Voltage: $400\ V_{DC}$
- Rated Power: 2.5 kW

- CoolGaN™ → 70mΩ / 600V (GaN HEMTs)
- CoolMOS™ C7 → 33mΩ / 650V (Silicon SJ technology)
- CCM (Hard-Switching) → @ 65kHz
- Totem-Pole Full-Bridge Topology
- Fulfills EMI CISPR Class B



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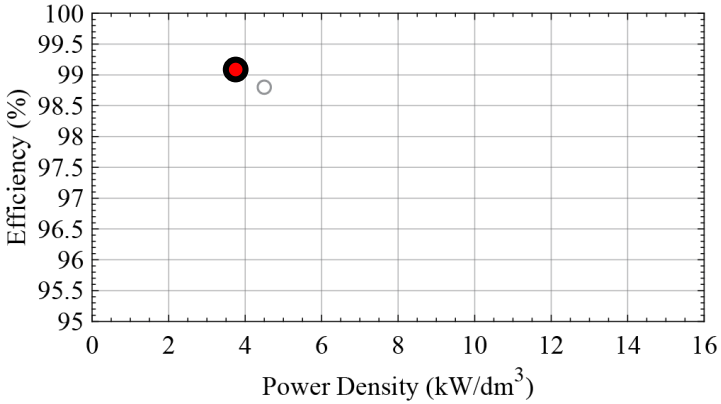
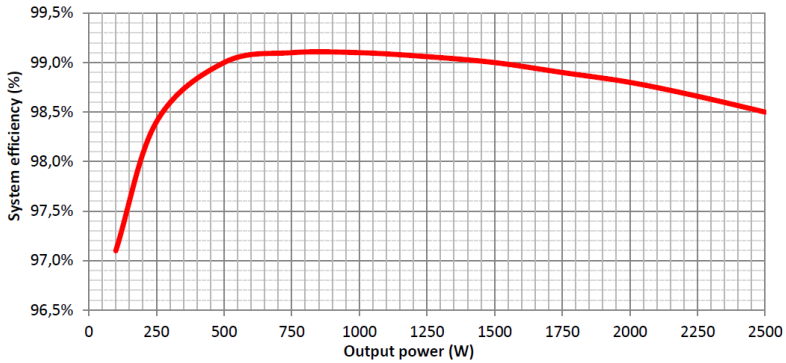


- 3.76kW/dm³ (61.7W/in³)
- 22.0cm x 7.2cm x 4.2cm
- f_S = 65kHz (PWM → Soft + Hard Switching)
- 99.1% Peak Efficiency



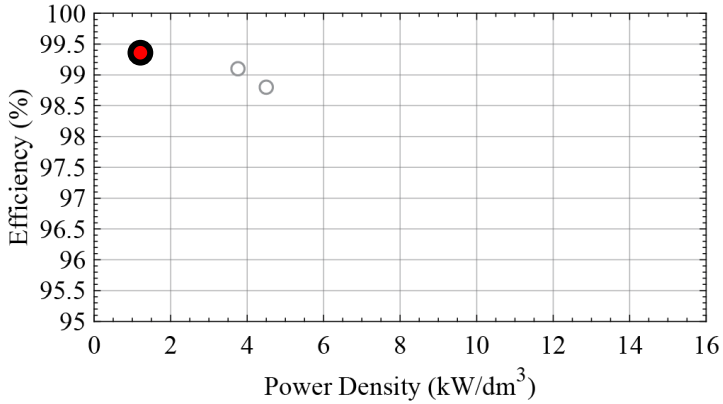
▶Ultra-High Efficiency (3)

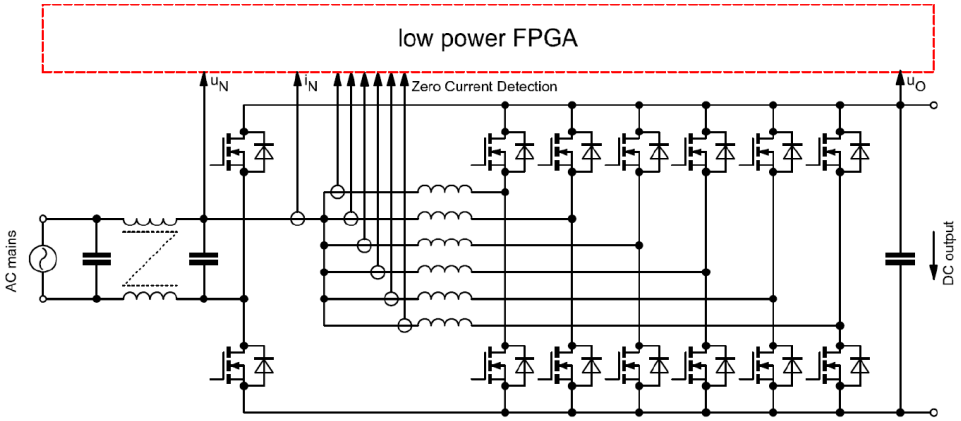
➢ Interleaved TCM PFC Rectifier – ETH Zurich

- Output Voltage: 400 V_{DC}
- Rated Power: 3.3 kW

- ZVS in All Bridges
- Large effective f_s for Filter
- High Partial Load Efficiency (>99% for P>500W)
- Fulfills EMI CISPR Class B
- Only Si SJ MOSFETs → No SiC devices

- 1.20kW/dm³ (19.7W/in³)
- f_s max. 100kHz
- 99.36% Peak Efficiency





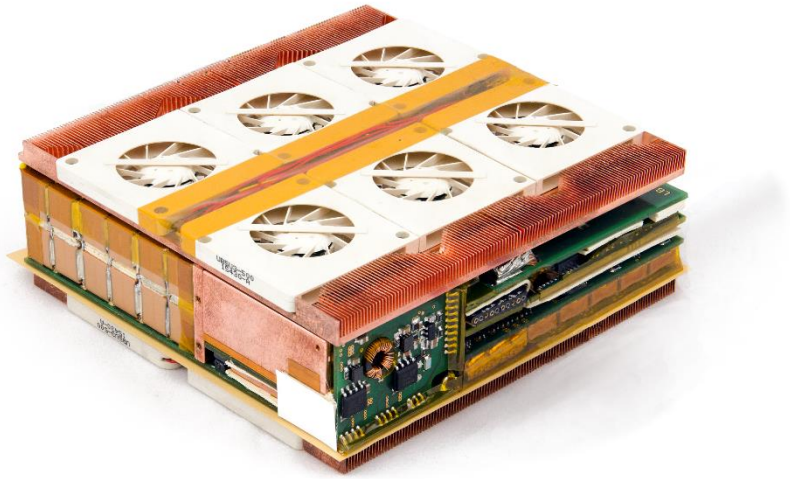
▶ Ultra-High Power Density (1)

➢ GLBC: ETH Zurich (1.0)

LITTLE BOX CHALLENGE

- System Employing Active CeraLink™ 1-Φ Power Pulsation Buffer
- Interleaving of 2 Bridge Legs per Phase

- 8.2kW/dm³ (135W/in³)
- 8.9cm x 8.8cm x 3.1cm
- f_S = 250kHz ... 1MHz
- 96,3% Peak Efficiency @ 2kW
- T_c=58 °C @ 2kW



■ Compliant to All "Original" Specifications (!)

- i_{gnd} < 5mA (!)
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

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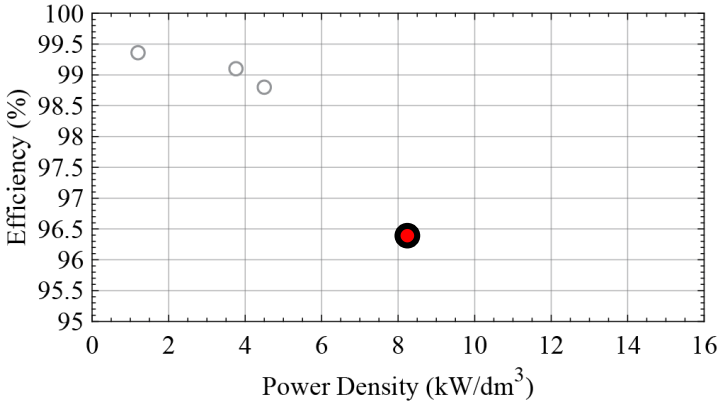

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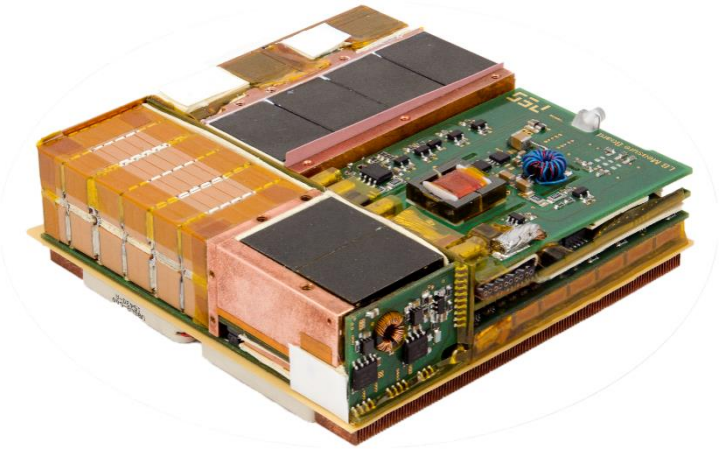

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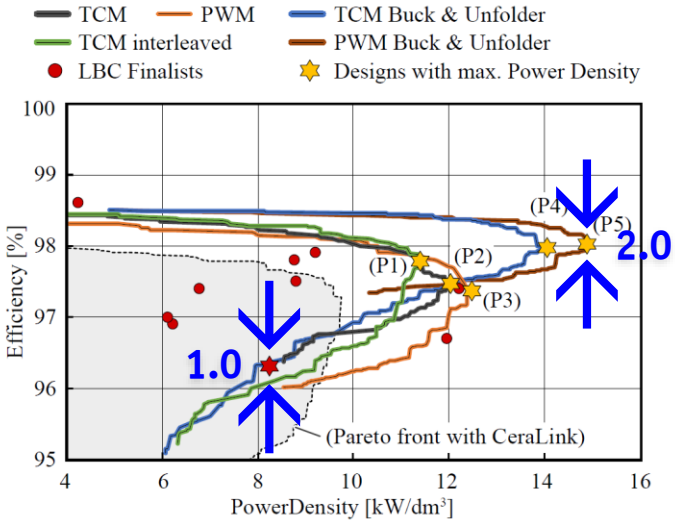
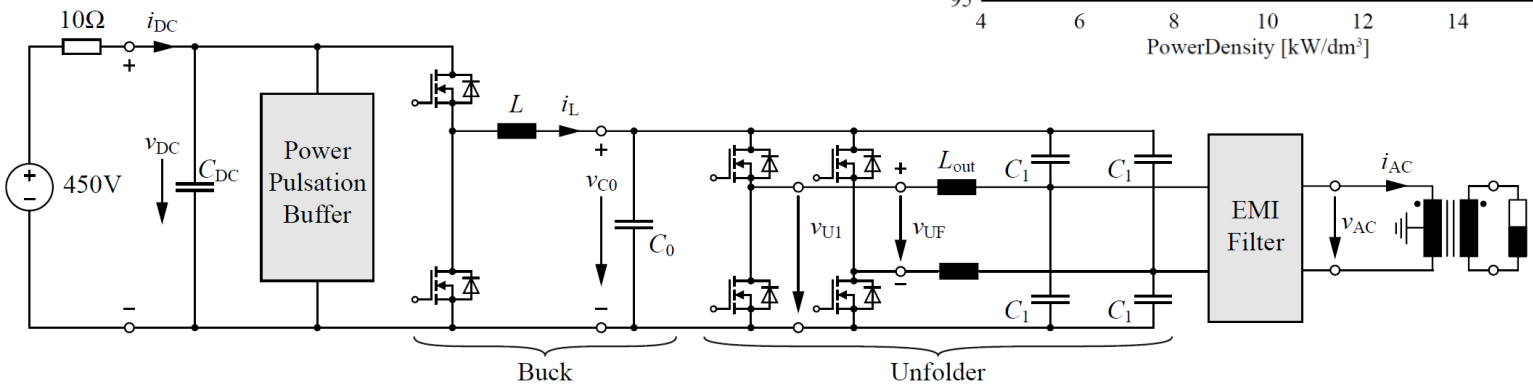
▶ Ultra-High Power Density (2)

➢ GLBC: ETH Zurich (2.0)

- Alternative Converter Topology: DC/|AC| - Buck Converter + Unfolder
- 60Hz – Unfolder
- TCM or PWM of DC/|AC| - Buck Converter
- X6S capacitors instead of Ceralink™

- DC/|AC| + Unfolder → Best Performance
- 2 Switching Bridge Legs → Larger Volume & Losses
- Interleaving → Not advantageous



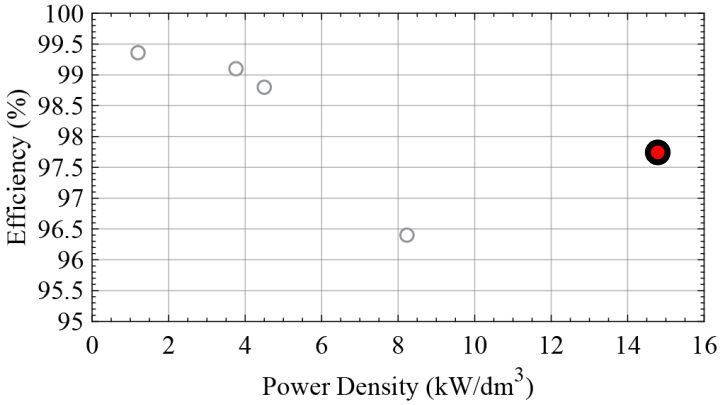


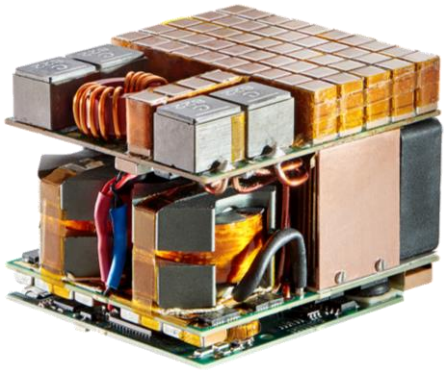
▶Ultra-High Power Density (2)

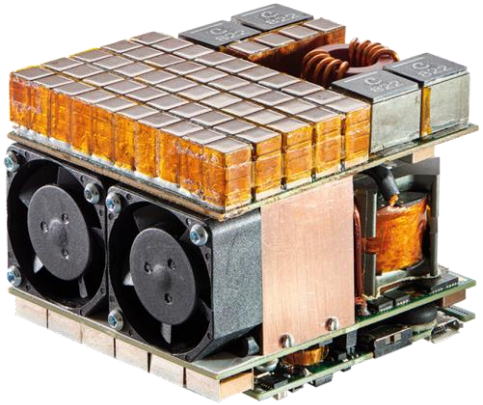
➢ GLBC: ETH Zurich (2.0)

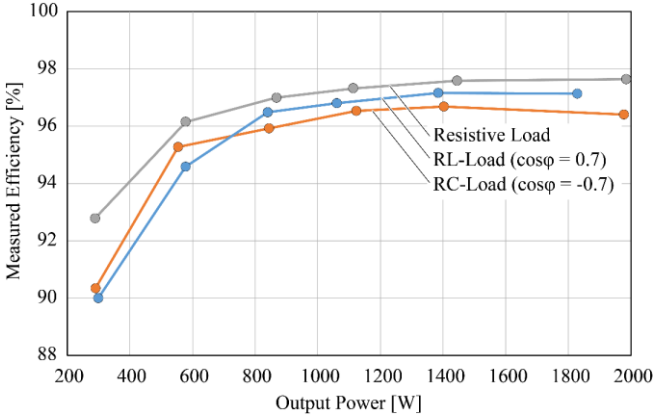
- Performance of First DC/|AC| + Unfolder Prototype
- PWM Operation
- Without Power Pulsation Buffer

- 14.8kW/dm³ (243W/in³)
- 6.0cm x 5.0cm x 4.5cm
- f_S = 250kHz
- 97.8% Peak Efficiency @ 2kW







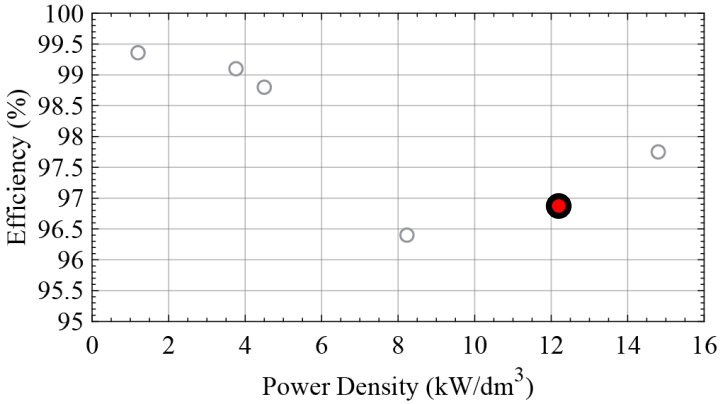


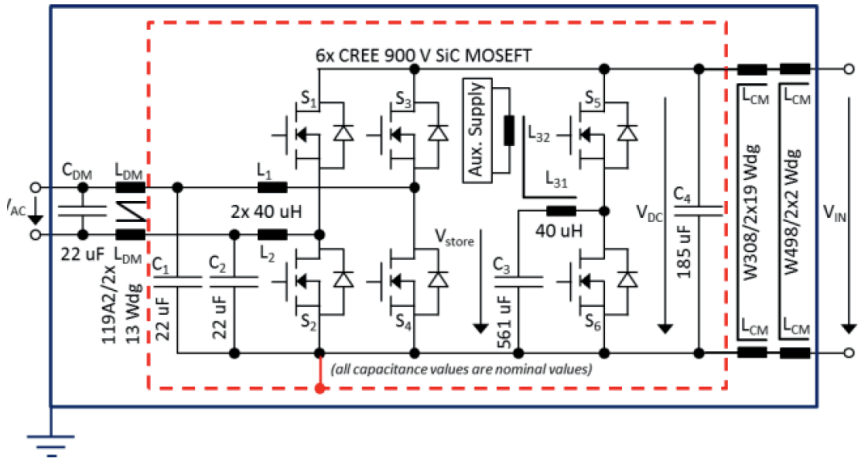
▶Ultra-High Power Density (3)

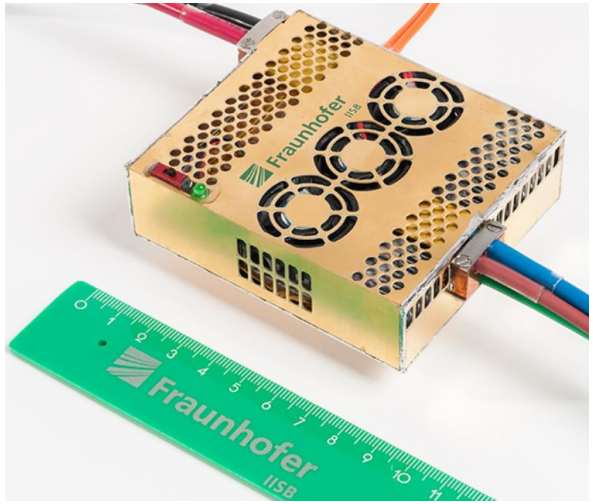
➢ GLBC: Fraunhofer IISB

- Very Well Engineered:
  - 3D Printed Heatsinks w/ Integrated Fans
  - 1 PCB Board
- Multi-Airgap Inductors
- 900 V SiC with PWM (Soft + Hard Switching)
- Buck-Type DC-side Power Pulsation Buffer

- 12.2kW/dm³ (201W/in³)
- f_s = 140kHz
- 96.9% Peak Efficiency



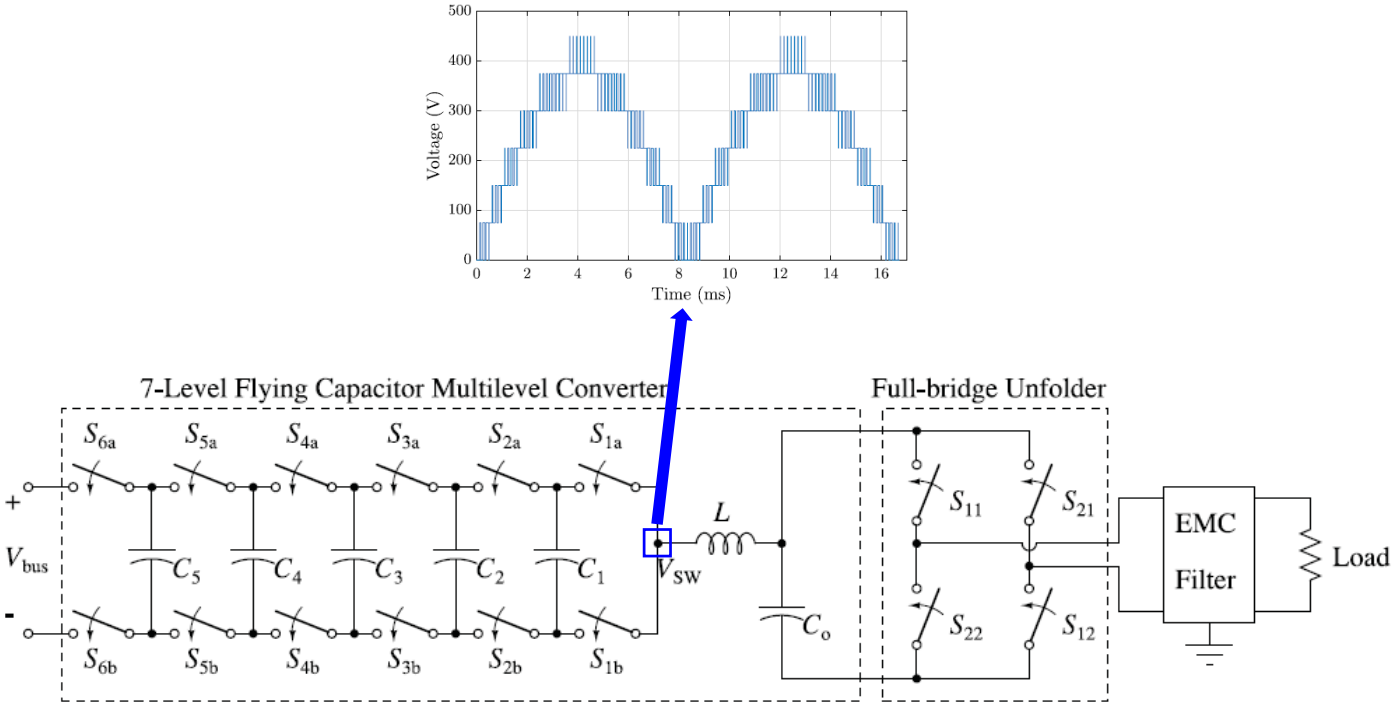




▶Ultra-High Power Density (4)

➢ GLBC: UIUC (Prof. Pilawa)

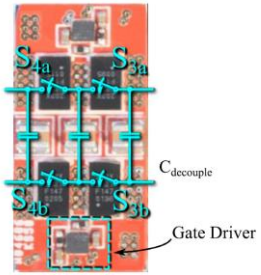
- Multi-Level Topology: Flying Capacitor Converter (FCC)
- Seven-Level Output Voltage: Smaller Output Filter
- Low-Voltage (150V) GaN Switches (EPC 2033)
- 60Hz-Unfolder
- Full-Bridge Active Power Buffer

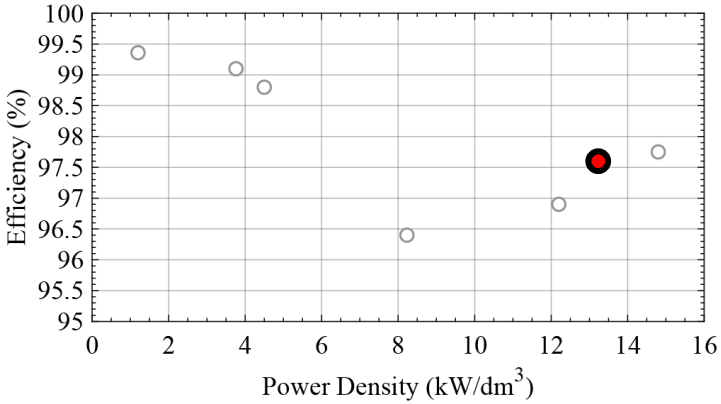


▶ Ultra-High Power Density (4)

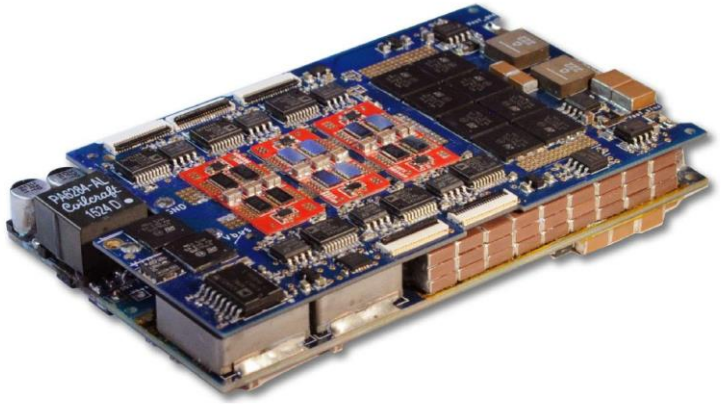
➢ GLBC: UIUC (Prof. Pilawa)

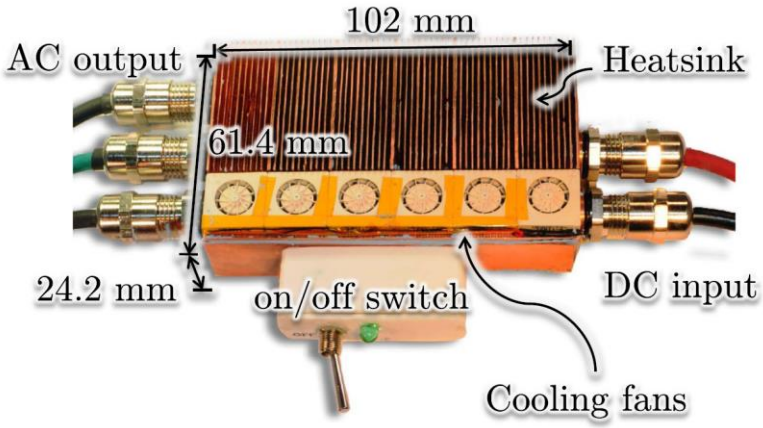
- Careful Design of Switching Cells →
  - Modularity
  - Reduced Parasitic Inductance
  - Reduced Switching Overvoltage





- 13.2kW/dm³ (216W/in³)
- 10.2cm x 6.1cm x 2.4cm
- f_S = 120kHz (effective 720kHz)
- 97.6% Peak Efficiency

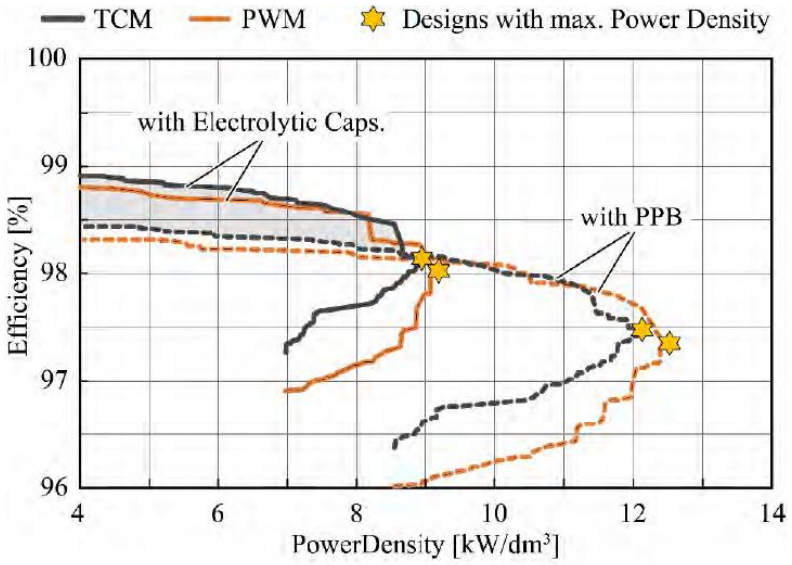




▶Performance Drivers for High Efficiency

1. Power Pulsation Buffer (PPB)

- Analysis for Google Little Box Challenge ($\Delta V/V < 3\%$)
- Efficiency Benefit of PPB→ For High Power Density ($\rho > 9kW/dm^3$)



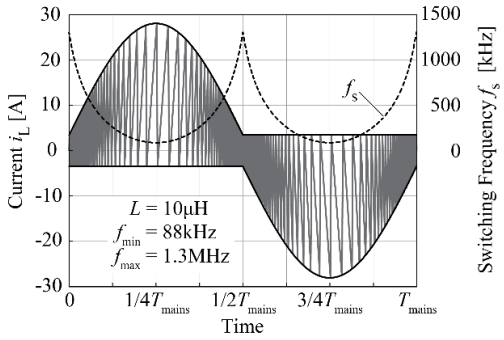
- Electrolytics Favorable for High Efficiency @ Moderate Power Density ($\Delta\eta$= +0.5%)
- Electrolytics Show Lower Vol. & Lower Losses if Large $\Delta V/V$ is accepted

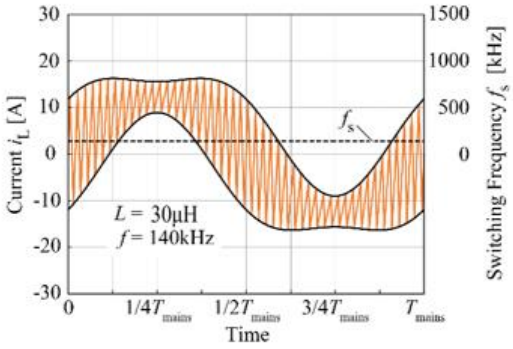
▶ Performance Drivers for High Efficiency

2. TCM vs. CCM

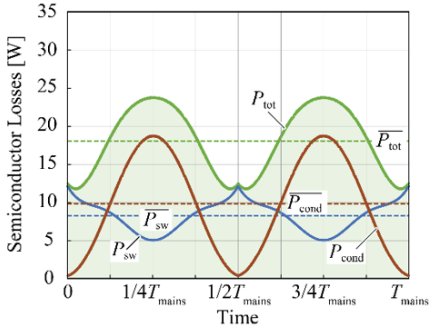
- **TCM:**
  + Low (Soft) Switching Losses
  - Larger RMS Currents in Inductor and Switches

- **CCM (PWM):**
  + Lower RMS Currents in Inductor and Switches
  - High (Hard) Switching Losses

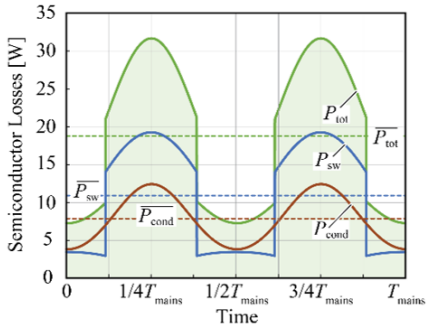




- **Not a clear winner** → Case Dependent and Has To Be Optimized
- Optimization for GaN GIT & No Interleaving → Optimal Inductors: L_{TCM} = 10µH and L_{CCM} = 30µH

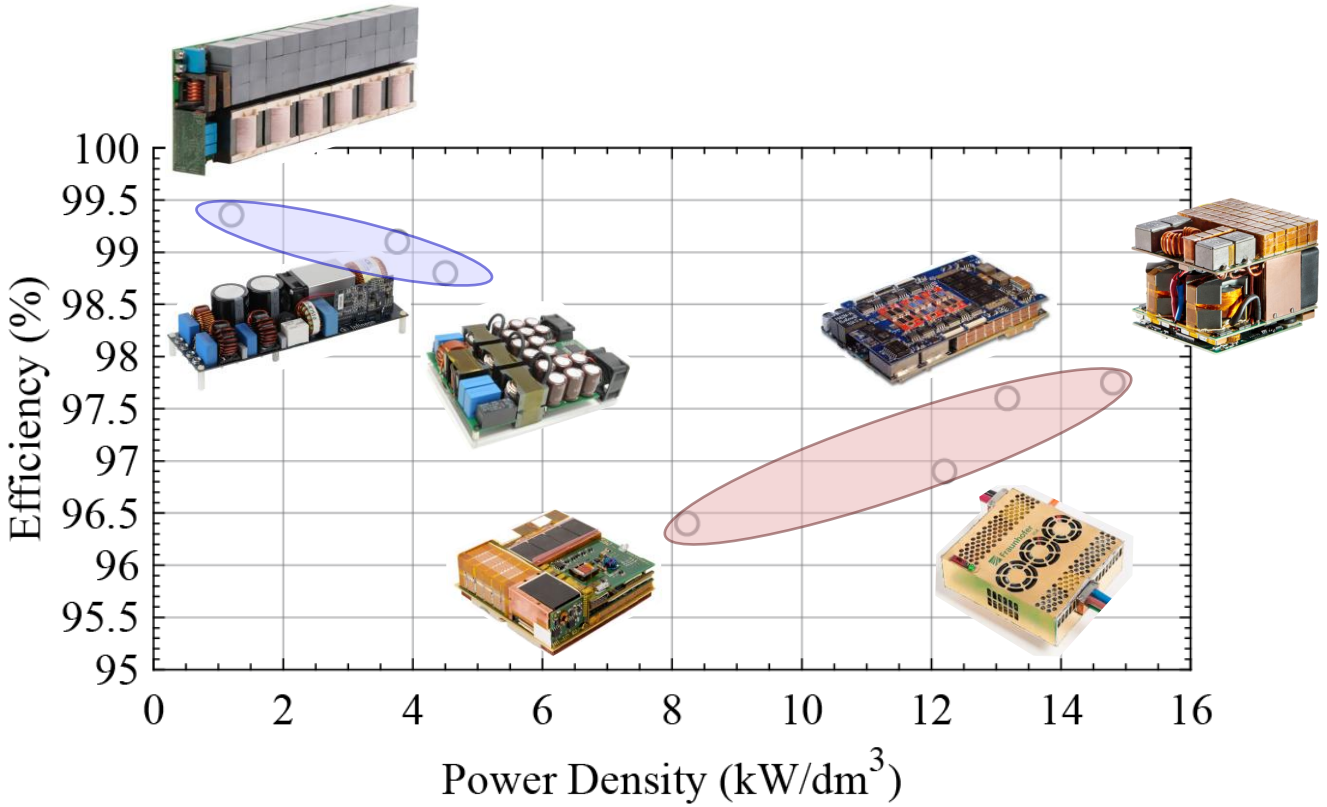


ρ = **11.9 kW/dm³**
η = **97.4%**



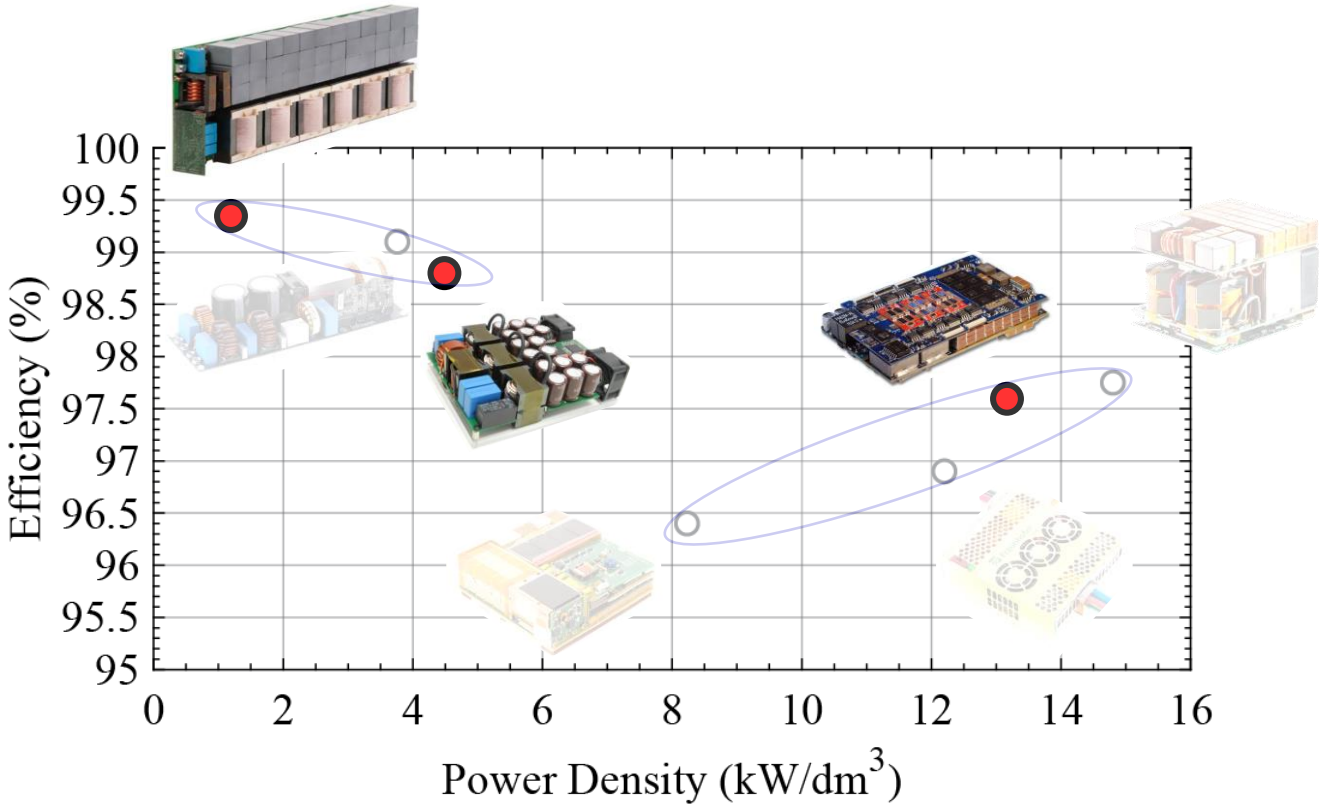
ρ = **12.5 kW/dm³**
η = **97.4%**

▶ Performance Drivers for High Efficiency



▶ Performance Drivers for High Efficiency

3. Low Switching Frequency... But High Effective Switching Frequency



▶ Performance Drivers for High Efficiency

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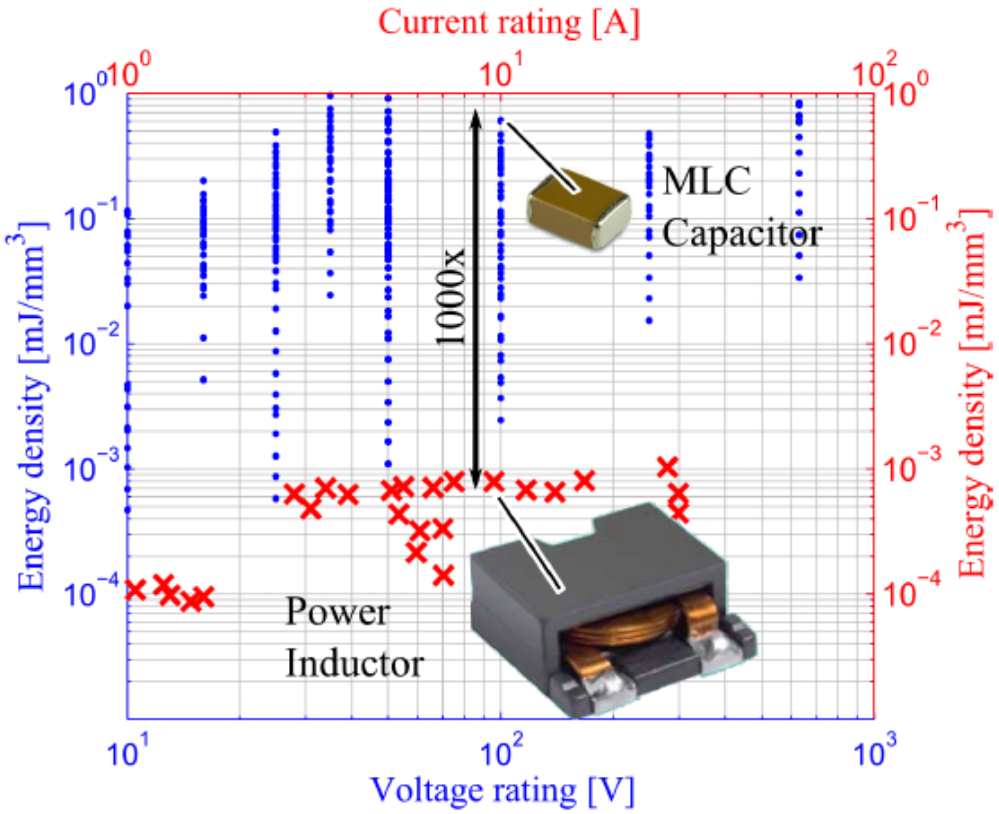

Source: Pilawa

▶ Performance Drivers for High Efficiency

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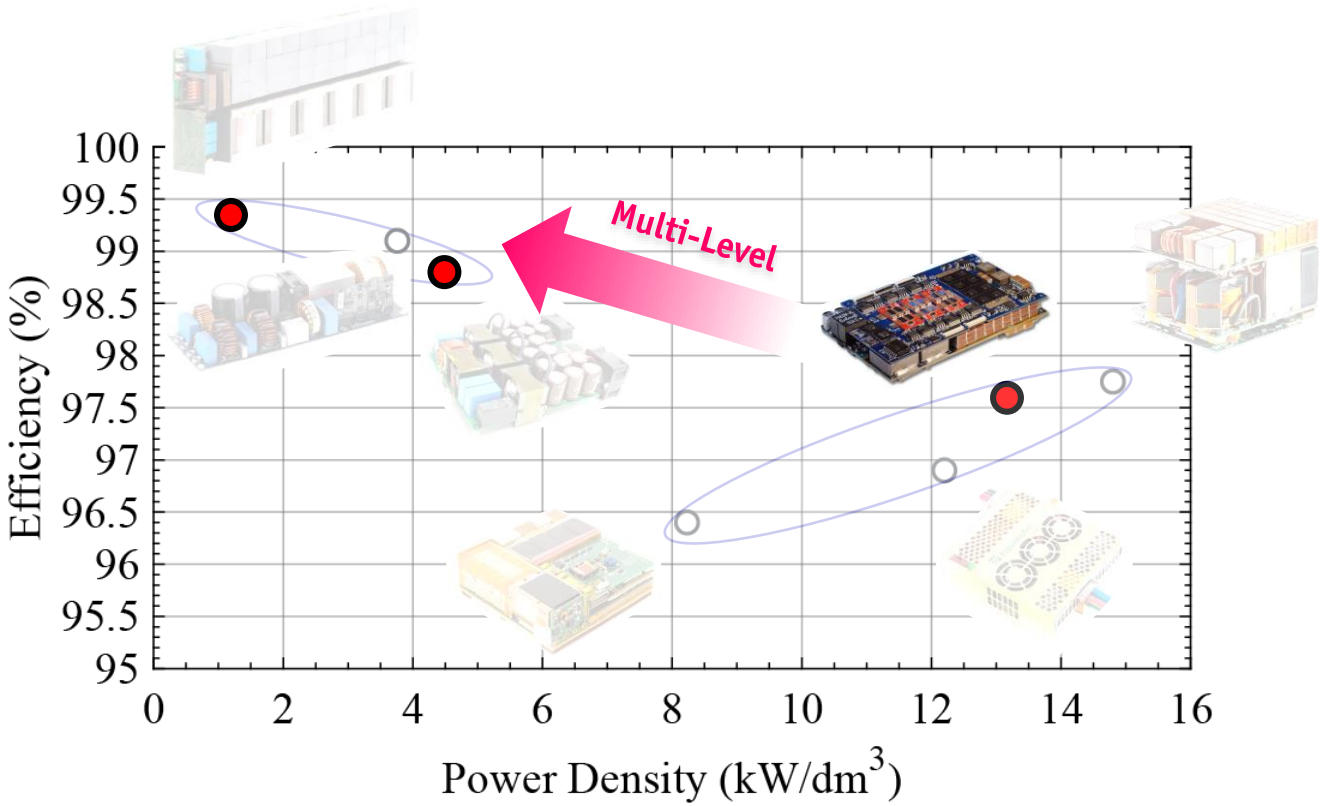


Multi-Level Solutions
Ultra-High Efficiency

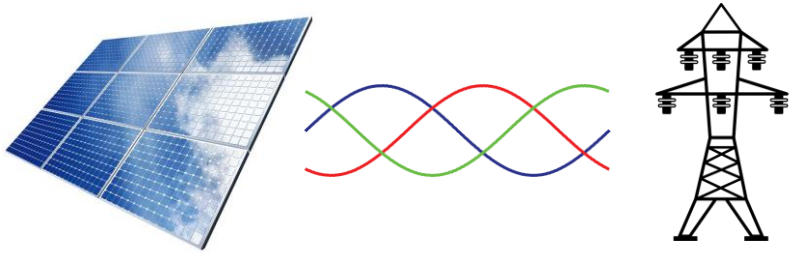
- *Specifications*
- *Motivation for Multi-Level*
- *Bridge Leg Comparison*

▶Specifications

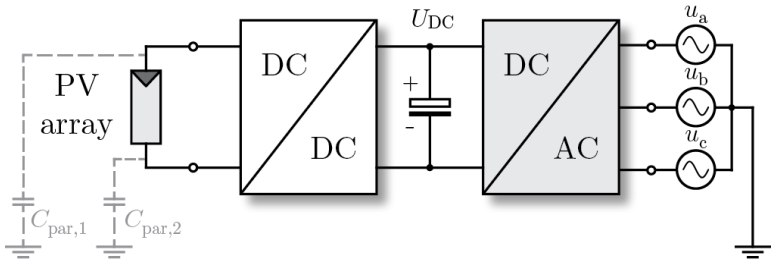
Nom. Power	10 kW
Max. Power	12.5 kW
$V_{DC,nominal}$	720 V (max. 800V)
$V_{AC,nominal,RMS}$	230 V
Operation Mode	DC/AC (bidirectional)
EMI Filtering	Class A
# Phases	3

Target

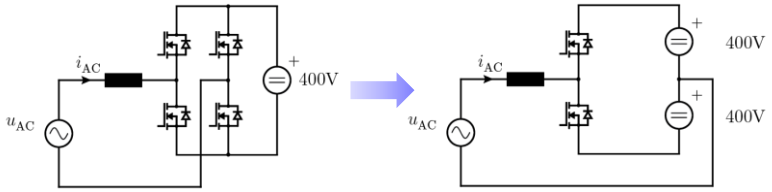
99.5 %
Efficiency



- **Questions to be answered:**
  - Can 99.5 % peak efficiency be reached?
  - At what price (volume, weight and cost)?



▶ DC-Link Voltage: 400V...800V



■ What is the Challenge from $400V_{DC}$ to $800\ V_{DC}$?

→ For the same AC-side power:

➢ Semiconductor **Switching** Losses

- Switched Currents Don't Change → Determined by AC Current
- Switched Voltage Changes → Determined by DC Voltage

Increase in Losses

➢ Semiconductor **Conduction** Losses

- RMS Current in Half-Bridge Doesn't Change → Determined by AC side
- Semicond. On-State Resistance Changes → Blocking Voltage Dependent

Increase in Losses

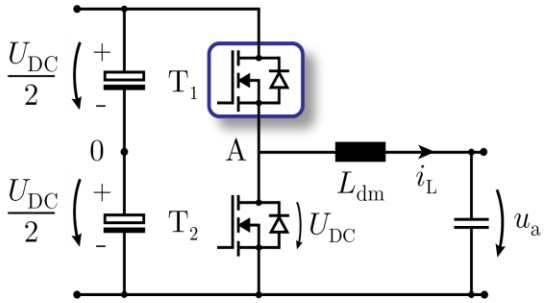
➢ Capacitor Voltage Rating – Series Connection

- Volume Quadratic With # of Series Connected Capacitors for Same C
- Passive (Resistive) Voltage Balancing

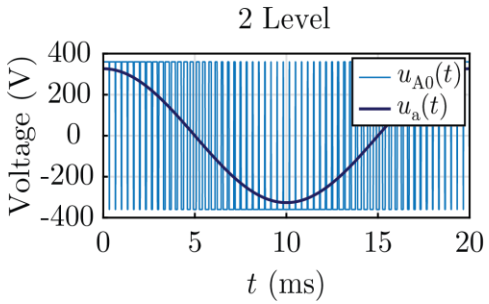
Increase in Volume & Losses

▶ Motivation for Multi-Level Topologies

■ Analyze best strategy to achieve target 99.5% efficiency

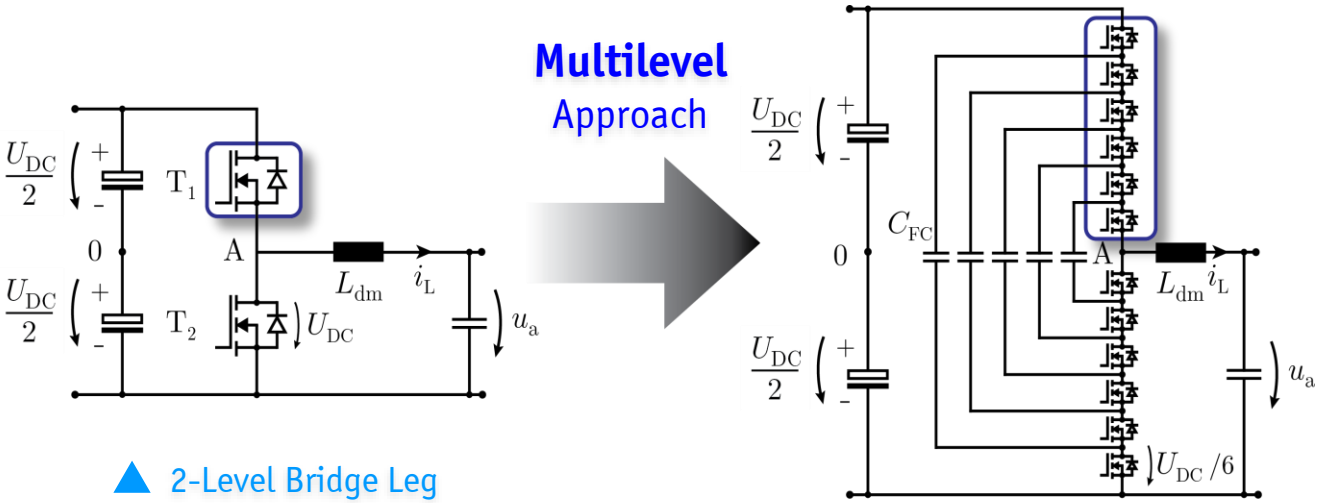


▲ 2-Level Bridge Leg



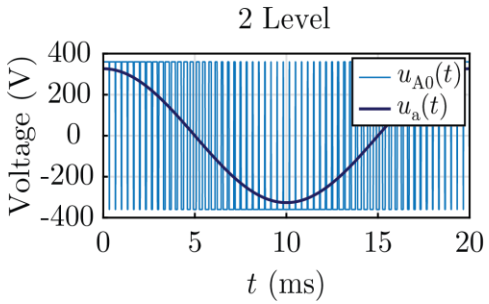
▶ Motivation for Multi-Level Topologies

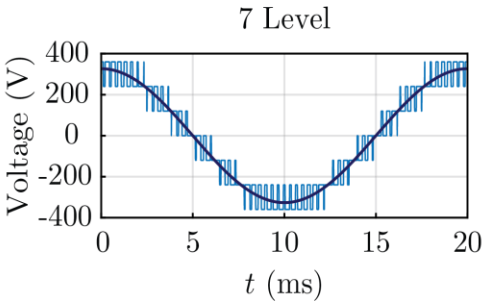
■ Analyze best strategy to achieve target 99.5% efficiency



▲ 2-Level Bridge Leg

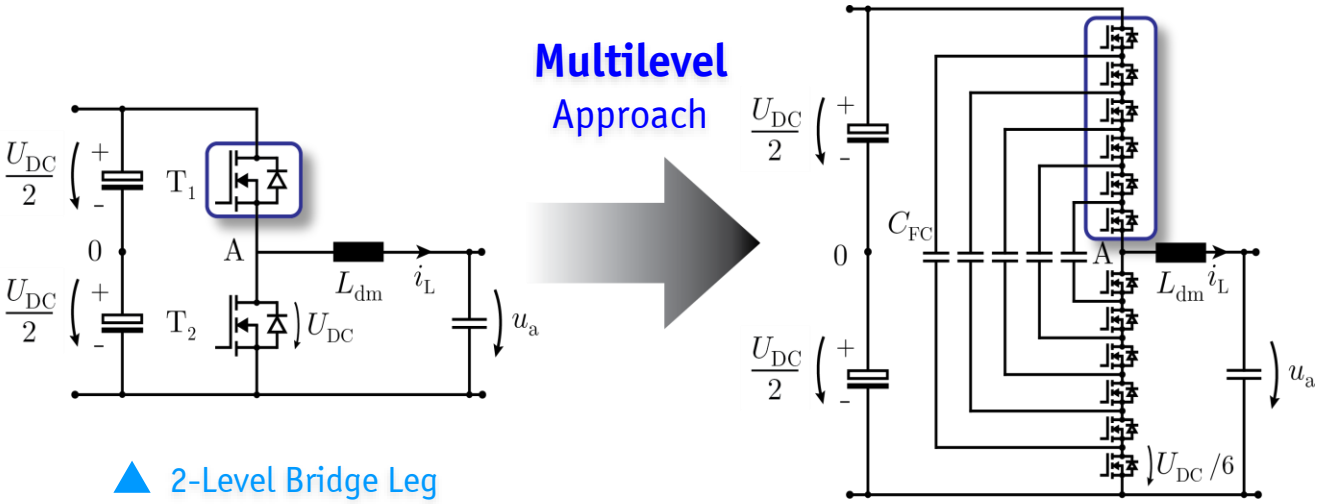
▲ 7-Level FC Bridge Leg





▶ Motivation for Multi-Level Topologies

■ Analyze best strategy to achieve target 99.5% efficiency



▲ 2-Level Bridge Leg

▲ 7-Level FC Bridge Leg

■ Three main advantages

1. More output voltage levels
2. Higher effective frequency

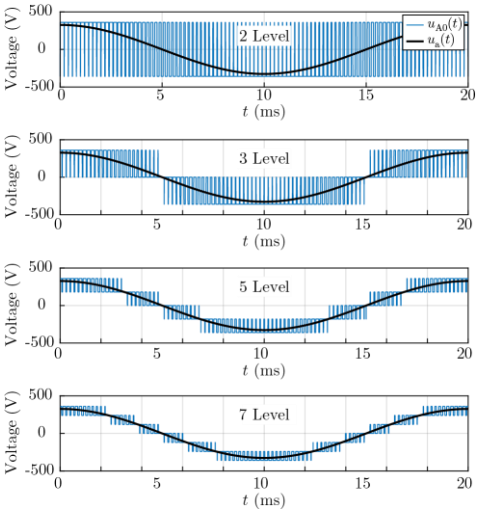
} Smaller magnetics

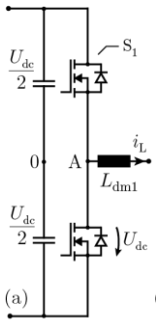
3. Better switch utilization (LV switches outperform HV switches)

$$\Delta i_L \propto \frac{1}{N_{lev}^2} \cdot \frac{1}{L}$$

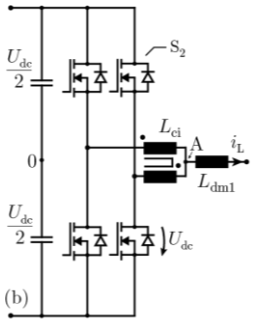
▶ Bridge Leg Analysis – 99.5% Efficiency Target

- **Optimum Number of Levels?**
- **Compared topologies:**
  - 2 Level
  - 2 Level-Interleaved (3 Level)
  - 3 Level T-type
  - 3, 5 and 7 Level Flying Cap. Converter (FCC)
  - 5 and 7 Level Hybrid Active NPC (HANPC)

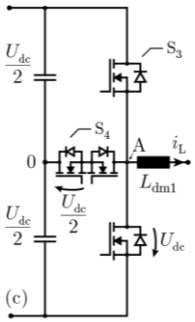




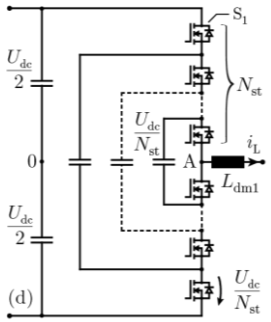
▲ 2-L



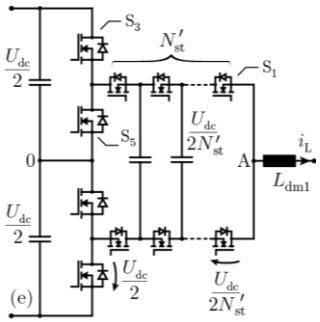
▲ 2-L **Interleaved**



▲ 3-L **T-type**



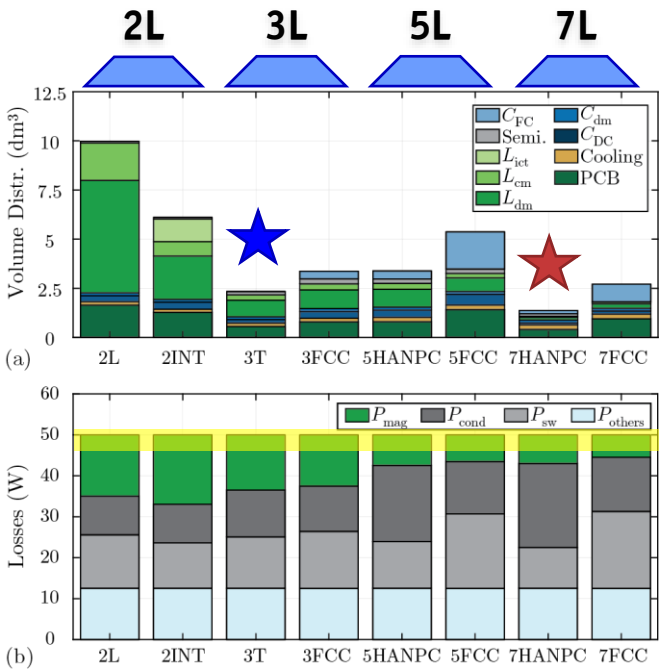
▲ (N_{st}+1) Level **FCC**



▲ (2N'$_{st}$+1) Level **HANPC**

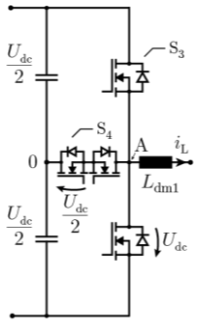
▶ Result of the Bridge Leg Analysis – 99.5% Efficiency Target

- **Aim:** topologies with highest power density (lowest volume).

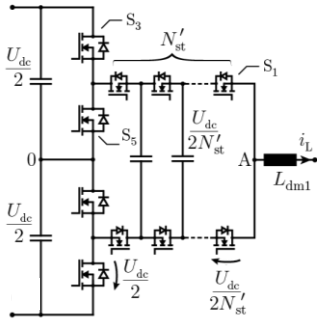


Volume

Losses @ 10 kW



▲ 3-L **T-type**



▲ 7-Level **HANPC**

- **Conclusions:**
  - ✓ **3L T-type**: Good **trade-off** between **magnetics** and **semiconductors**. No capacitors.
  - ✓ **7L HANPC**: Good **trade-off** between **capacitors** and **semiconductors**. Small magnetics.

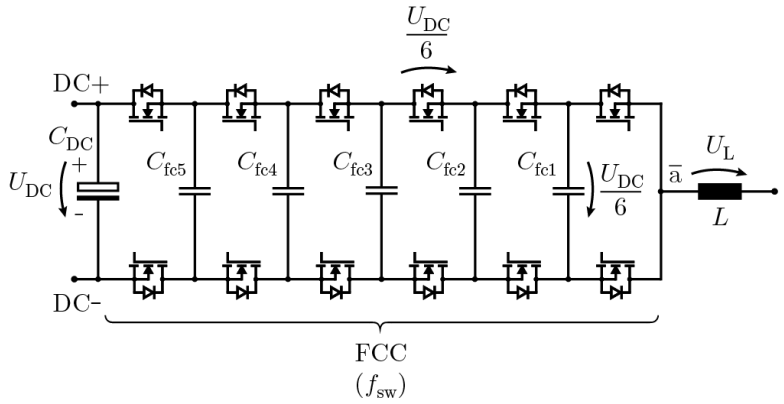
▶ Hardware prototypes

3-Level T-type	7-Level HANPC converter
	
2.35 kW/dm³ (39.3 W/in³)	3.34 kW/dm³ (55.9 W/in³)
1.06 kW/kg (11.8 kg)	2.63 kW/kg (4.8 kg)
- % (measured) 99.5 % (expected)	99.35 % (measured) 99.37 % (expected)

7-Level HANPC Inverter Topology

▶ HANPC topology: derivation

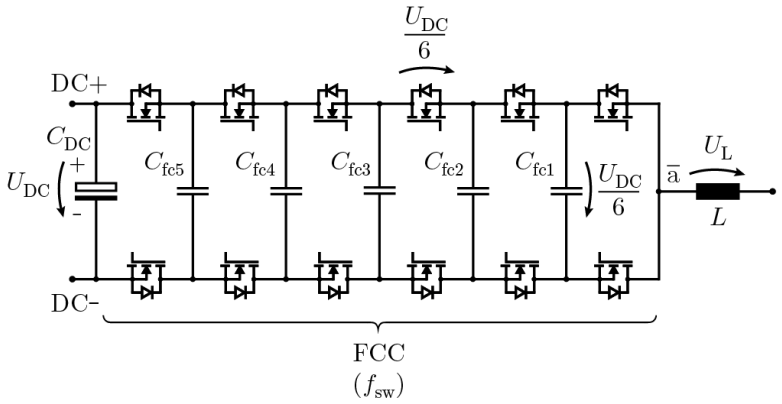
- The **HANPC** topology can be **derived from** the Flying Capacitor Converter (**FCC**)



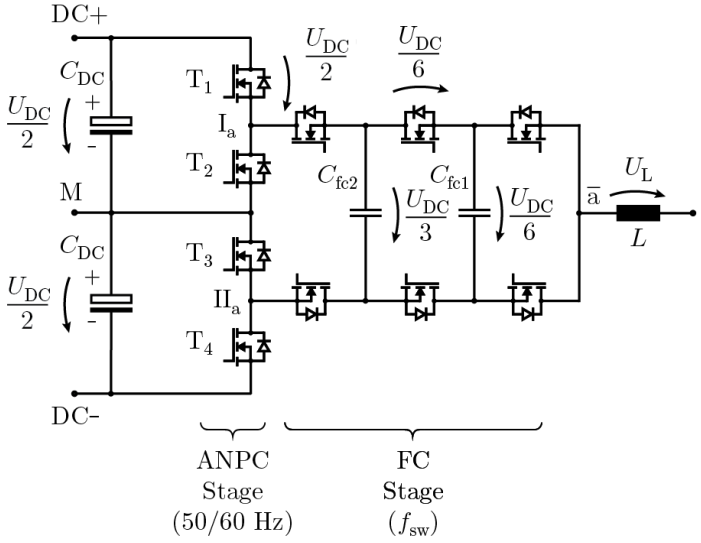
◀ 7-L FCC

▶ HANPC topology: derivation

- The **HANPC** topology can be **derived from** the Flying Capacitor Converter (**FCC**)



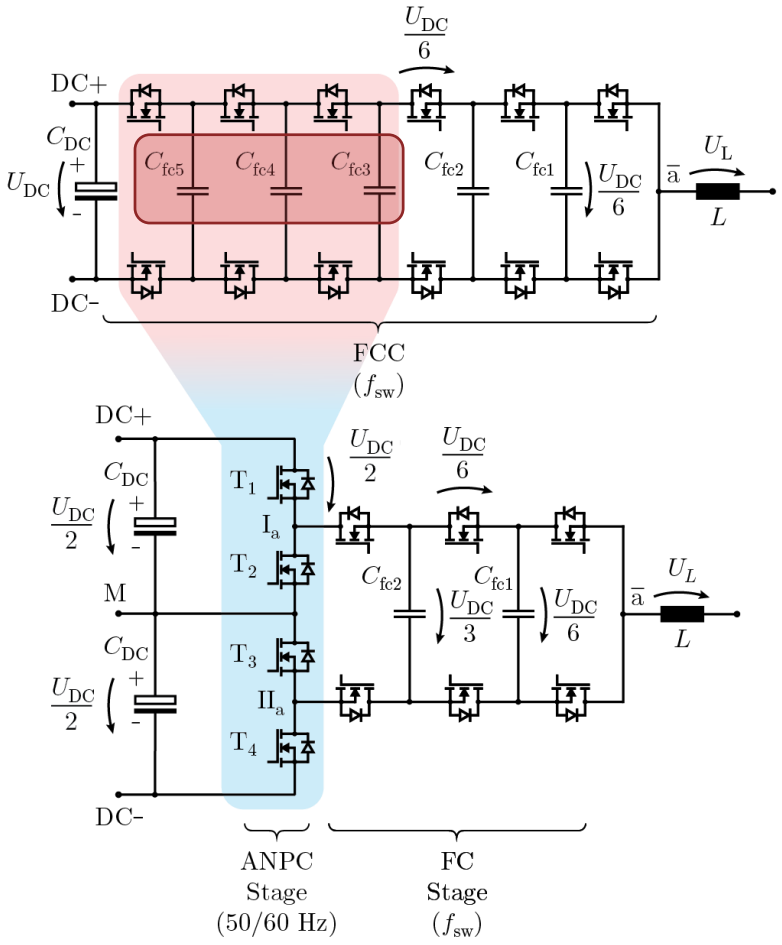
◀ 7-L FCC



◀ 7-L HANPC inverter

▶ HANPC topology: derivation

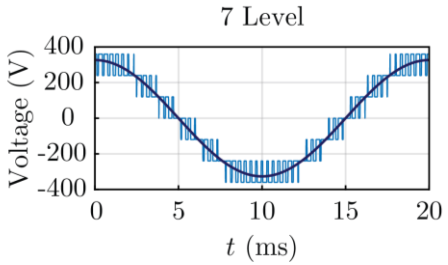
■ The **HANPC** topology can be **derived from** the Flying Capacitor Converter (**FCC**)



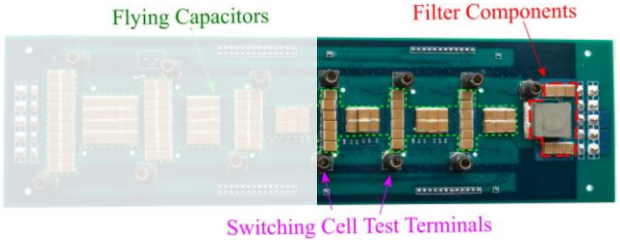
◀ 7-L FCC

◀ 7-L HANPC inverter

✔ 7- Level Output



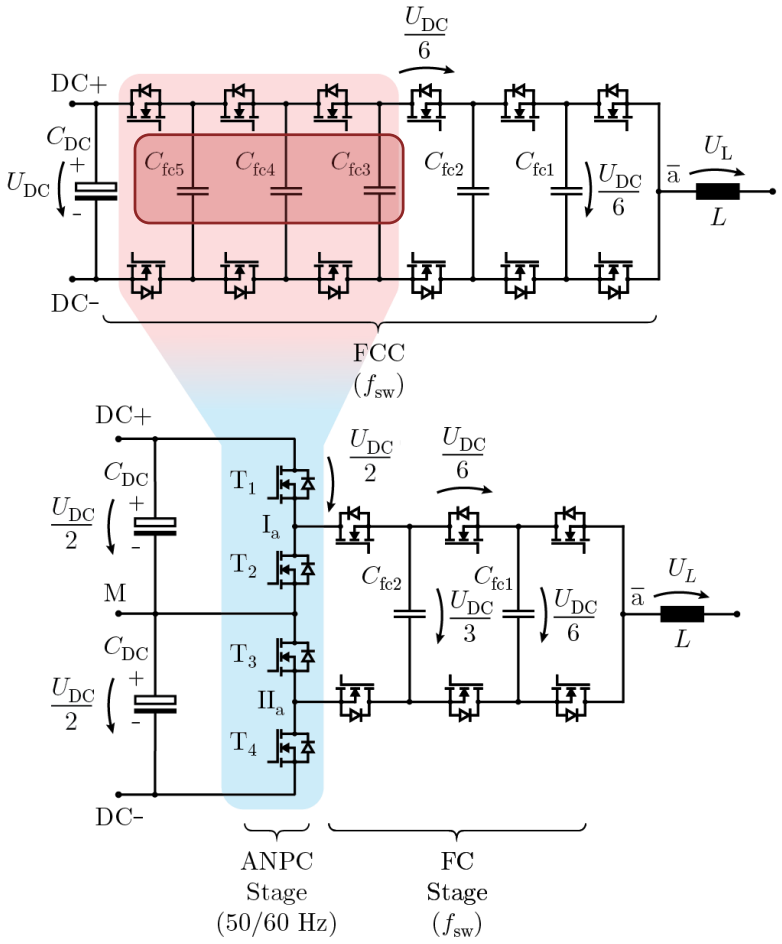
✔ Less than **half** the capacitors (large volume savings)



▲ 13-Level FCC (Source: Pilawa et al.)

▶ HANPC topology: derivation

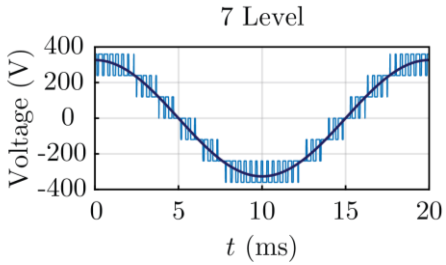
- The **HANPC** topology can be **derived from** the Flying Capacitor Converter (**FCC**)



◀ 7-L FCC

◀ 7-L HANPC inverter

✔ 7- Level Output



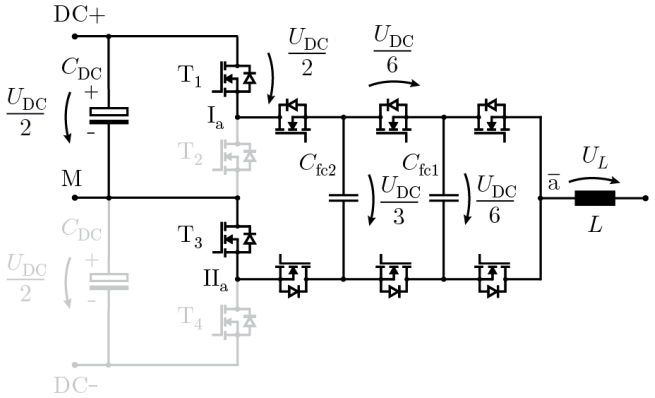
✔ Less than **half** the capacitors (large volume savings)

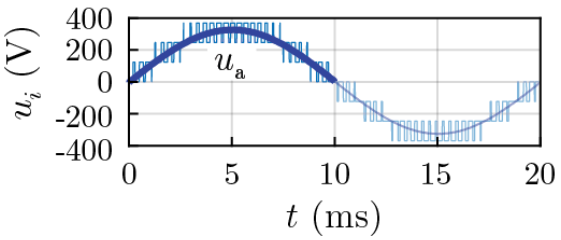
✔ Same requirement for EMI filter

▶ HANPC topology

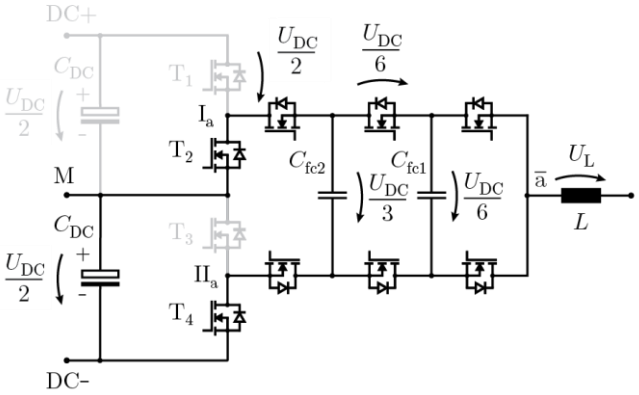
- ANPC stage clamps the FC stage to the high-side and low-side DC-link on 50 Hz basis

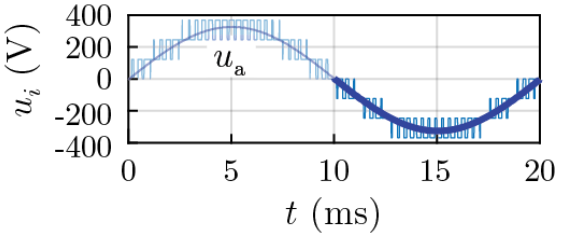
U > 0





U < 0





7-Level HANPC

Pareto Optimization

▶Switching Loss Data

■ **Accurate and Reliable Switching Data is Necessary**

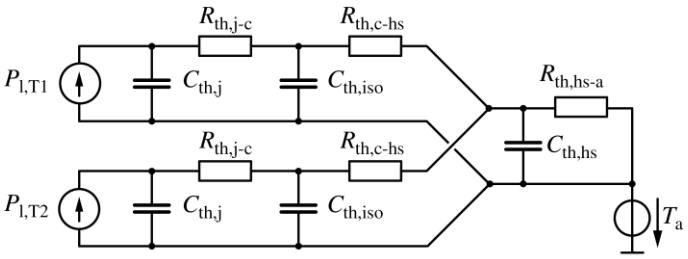
- Specially when Switches Account for 60..70% of Total Losses
- LV semiconductor datasheets provide no data

➢ **Switching losses have to be measured**

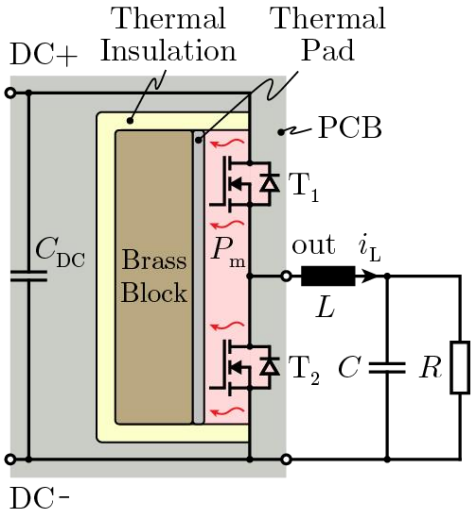
▶Switching Loss Measurement Method

➢ Half-Bridge "In-The-Box"

- Brass Block as Heat-Sink
- Measure Elapsed Time to Heat-Up Block ΔT



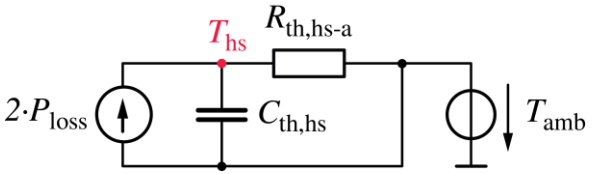
▲ Thermal Circuit



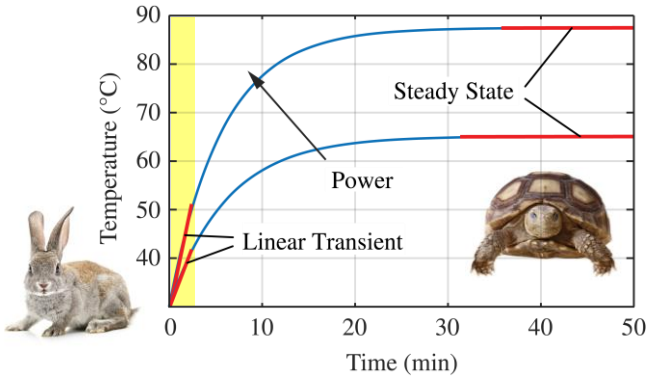
▶Switching Loss Measurement Method

➢ Half-Bridge "In-The-Box"

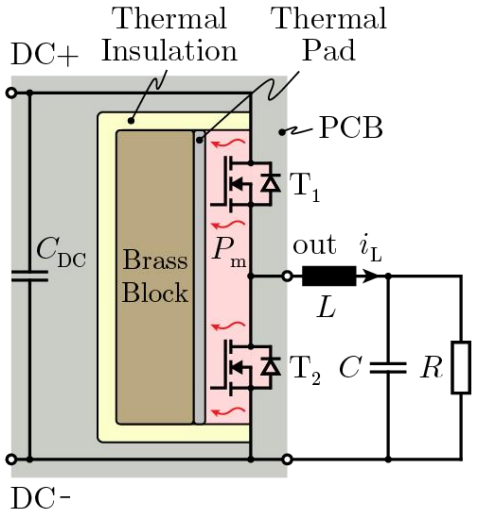
- **Brass Block as Heat-Sink**
- **Measure Elapsed Time to Heat-Up Block ΔT**



▲ Simplified Thermal Circuit



R-C Characteristic



▶Switching Loss Measurement Method

➢ Half-Bridge "In-The-Box"

- Brass Block as Heat-Sink
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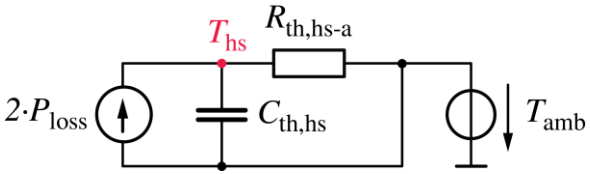
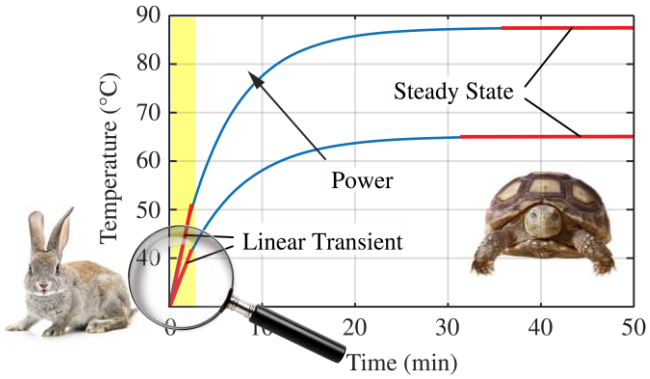
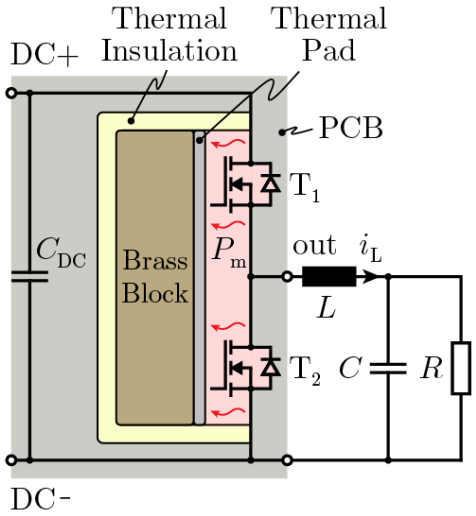
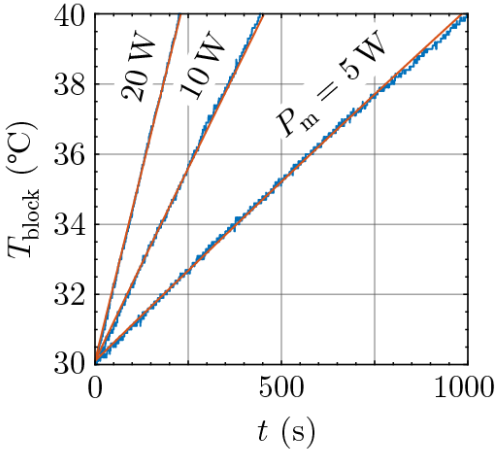


▲ Simplified Thermal Circuit



R-C Characteristic

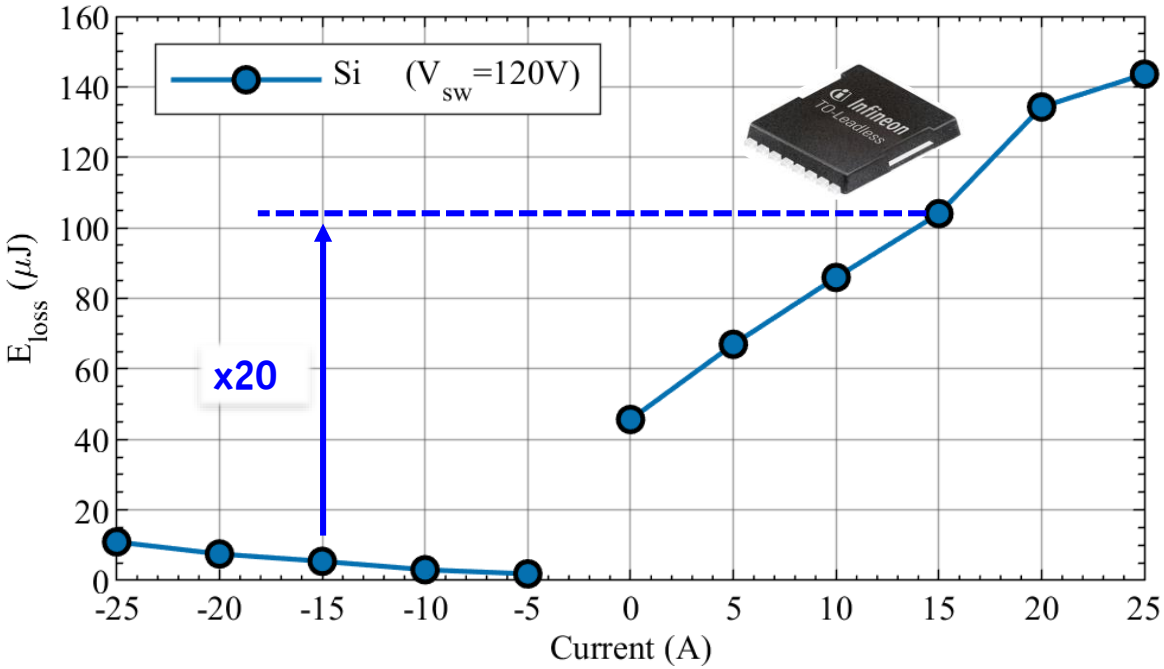




▶Switching Loss Measurement Results

■ Obtained Data is Used in Optimization

Silicon FD
200V 11.1mΩ
(*Infineon*)

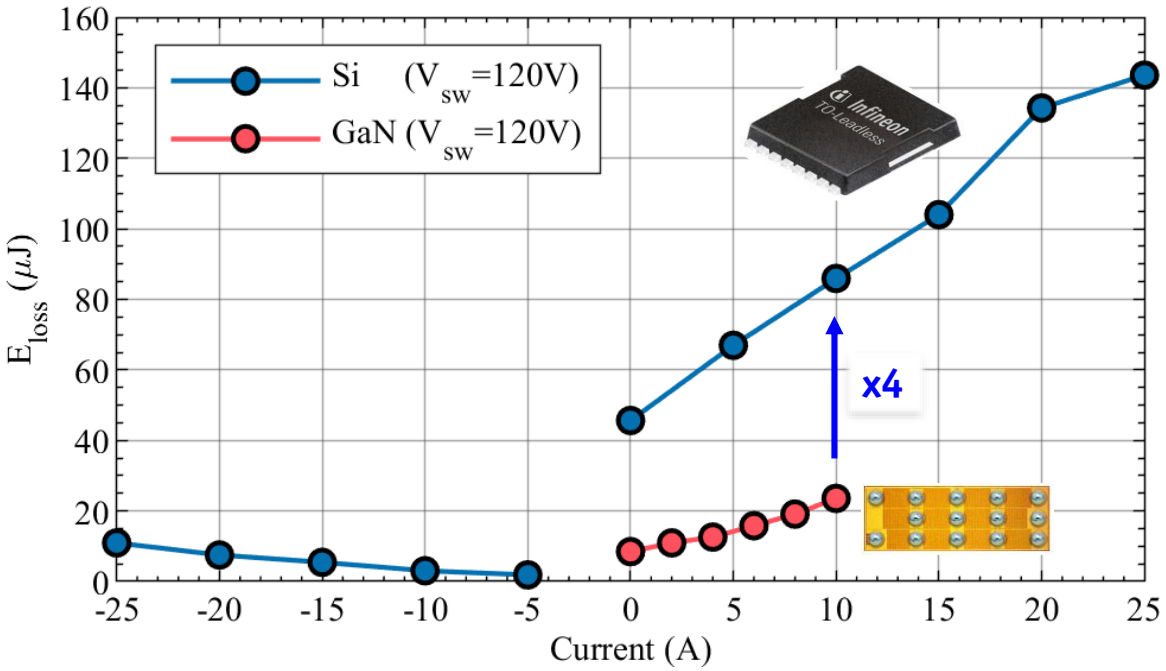


Turn-Off **Turn-On**

(Soft-Switched) **(Hard-Switched)**

▶Switching Loss Measurement Results

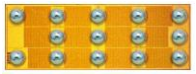
■ Obtained Data is Used in Optimization



Turn-Off (Soft-Switched)

Turn-On (Hard-Switched)

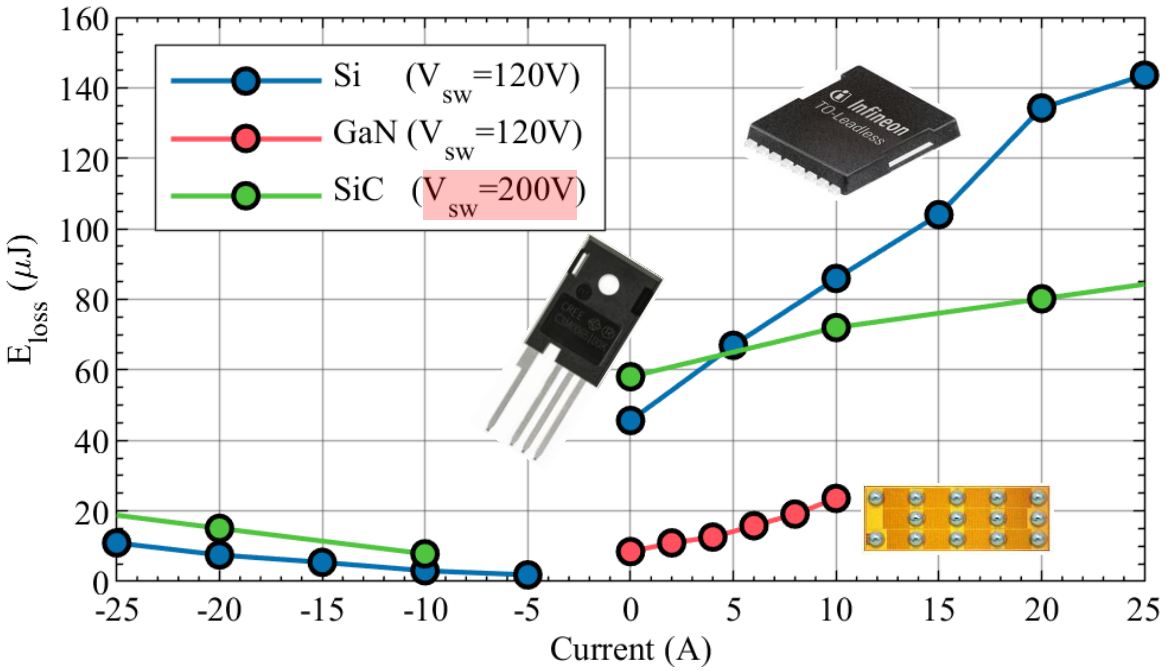
Silicon FD
200V 11.1mΩ
(*Infineon*)



GaN
200V 10mΩ
(*EPC 2047*)

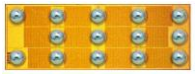
▶Switching Loss Measurement Results

■ Obtained Data is Used in Optimization



Turn-Off (Soft-Switched) **Turn-On** (Hard-Switched)

Silicon FD
200V 11.1mΩ
(*Infineon*)



GaN
200V 10mΩ
(*EPC 2047*)

SiC
900V 10mΩ
(*Wolfspeed*)

▶ Flying Capacitors

■ Dimensioning Criteria:

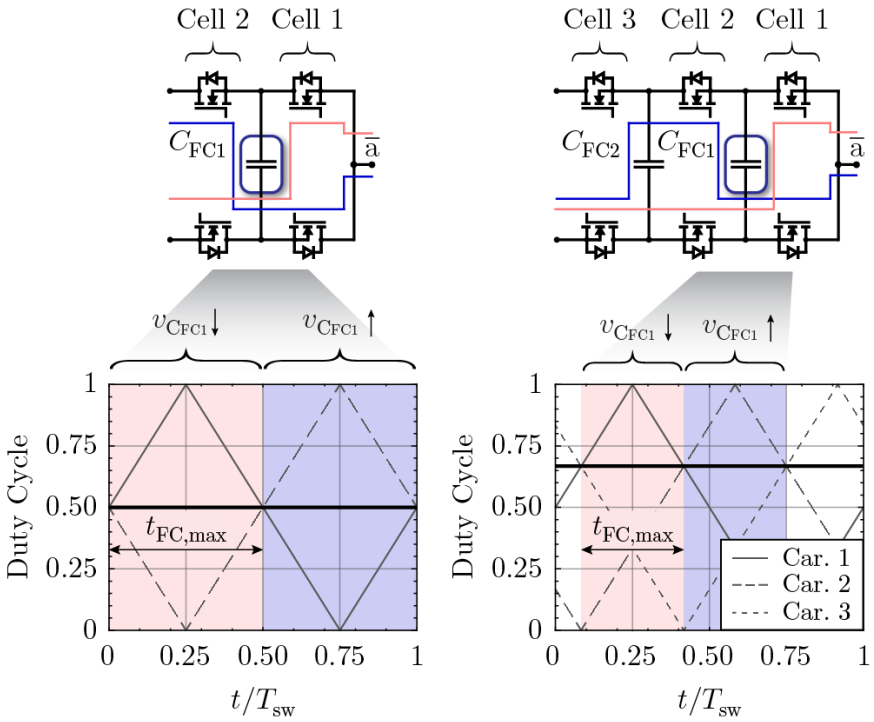
$$C_{\mathrm{FC,min}} = \frac{I_{\mathrm{ac,pk}}}{N_{\mathrm{FCcell}} f_{\mathrm{sw}} \Delta U_{\mathrm{FC,max}}}$$

■ Max. Voltage Ripple:

- $\Delta U_{\mathrm{FC,max}} = 5\mathrm{V}$ (arbitrary)

■ Switching Freq.:

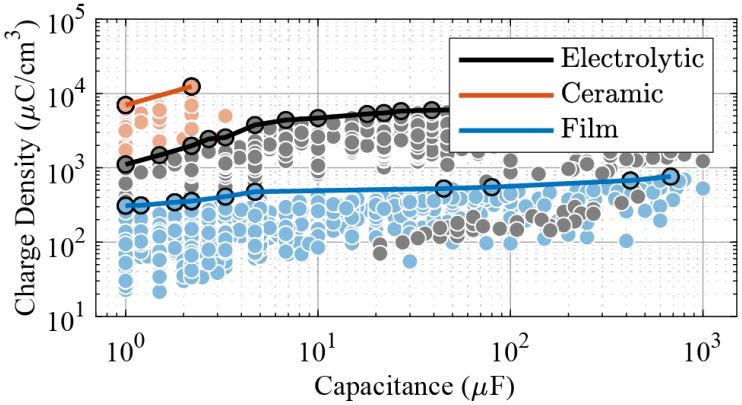
- Highly Affects Cap. Requirement
- Key Volume Contribution



$$t_{\mathrm{FC,max}} = \frac{1}{N_{\mathrm{FCcell}} f_{\mathrm{sw}}}$$

▶ Flying Capacitors: Capacitor Type Selection

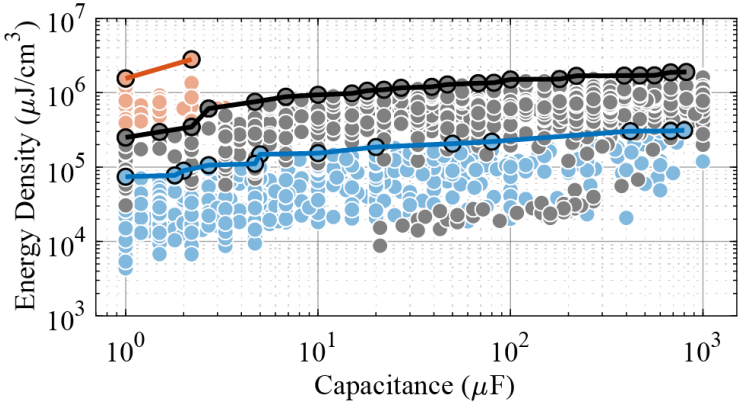
■ Charge Density:



$$Q = C \cdot V$$

Electrolytic **Film** **Ceramic**

■ Energy Density:

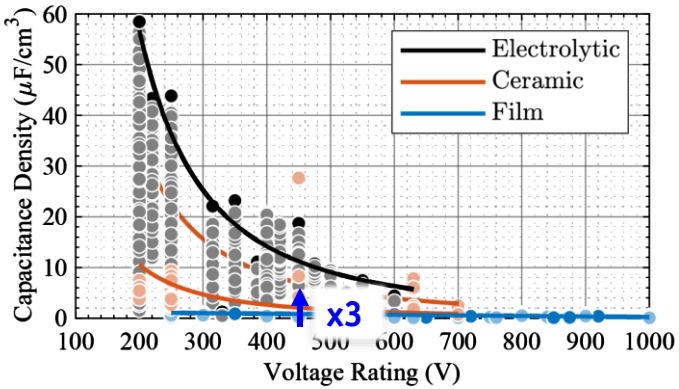


$$E = \frac{1}{2} \cdot C \cdot V^2$$

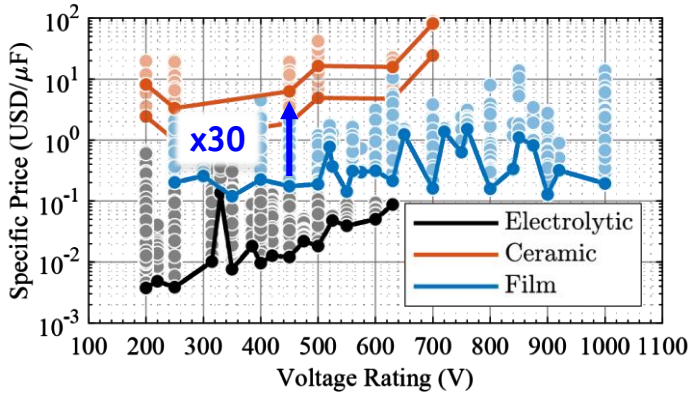
▶ Flying Capacitors: Capacitor Type Selection

➢ Key Factors:

■ Capacitance Density:



■ Price/Capacitance Ratio:



➢ Key Technical Factor for Choosing Capacitor, Not Charge or Energy Density

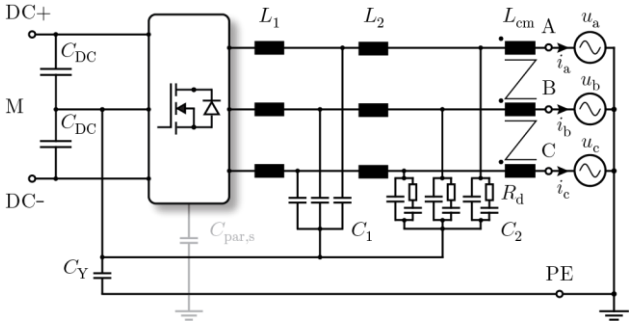
- Electrolytic Seem the Best… But
  - Losses
  - Current Rating
  - Reliability/Lifetime…
- Ceramic are a Good Alternative for High Switching Frequencies
  - Capacitance Derating (30% assumed)
  - Price
  - Stacking of Ceramic Capacitors
  - Losses (problem for LF AC)
- Film are a Good Alternative for Low Switching Frequencies
  - Bulky

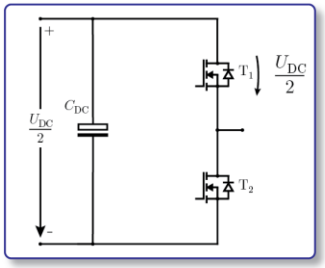
▶ Optimization: Considerations

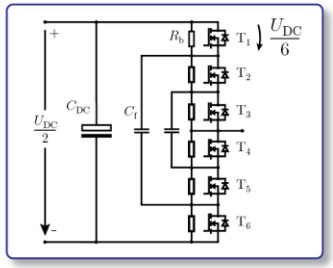
- **Semiconductors**
  - **ANPC Stage** (50/60 Hz): Silicon
  - **FC Stage** (f_{sw}): 3 x Silicon + GaN
- **Magnetics**
  - **Nanocrystalline** Cores
  - **Helical** Windings

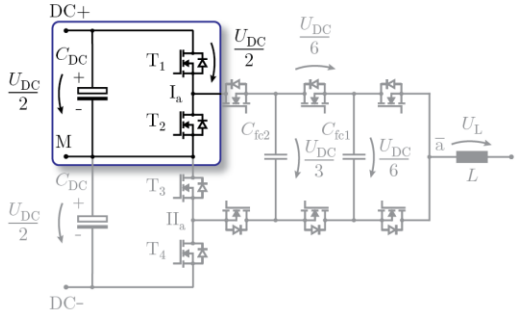
- **EMI Filter**
  - **L-C structure** (Simultaneous DM+CM Attenuation)
- **Topology variation**
  - **Low-Voltage Switch** Configuration for **ANPC Stage**: Same Voltage Level Switches in all Converter

▼ Final EMI Filter Stage





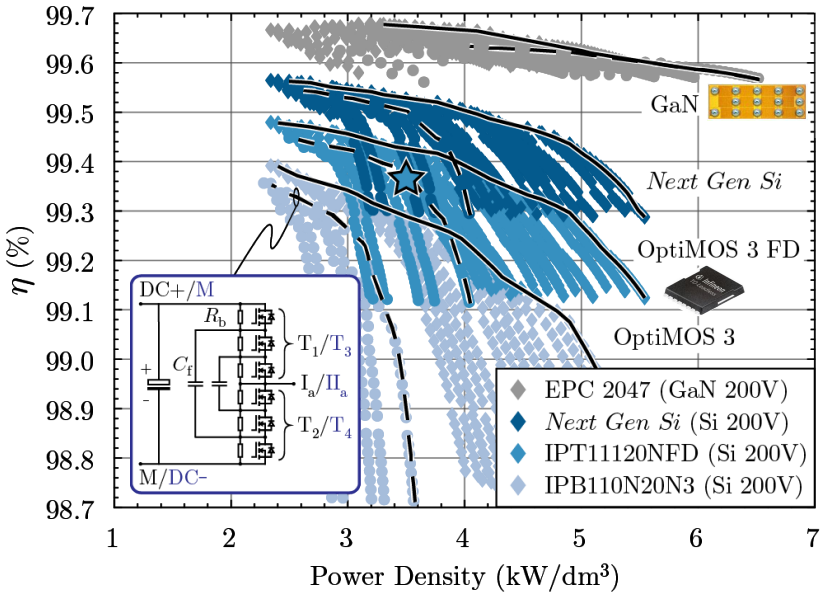




▲ "Low-Voltage Switch" Bridge Leg Concept for ANPC Stage

Low-Voltage Switch

▶Optimization: Results



GaN

Silicon

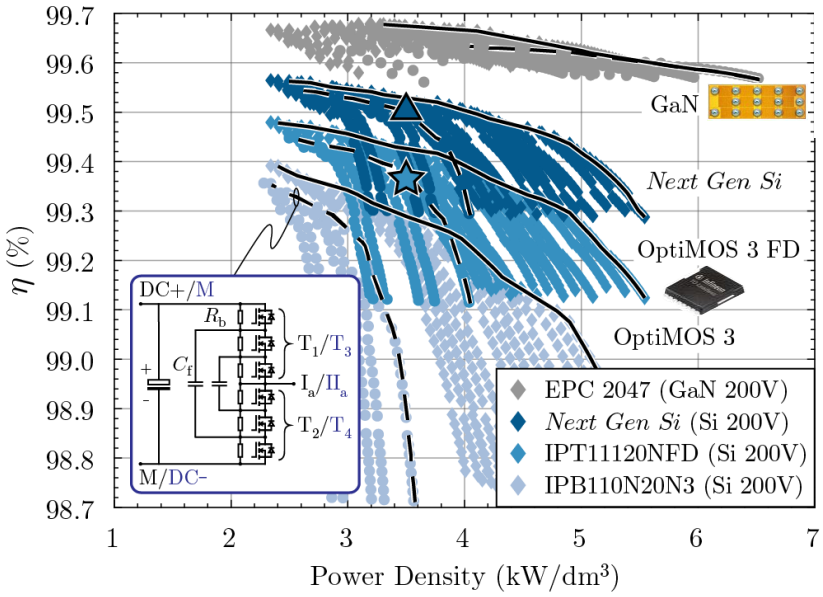
Built Design

▲ Pareto Front Optimization Results (η @ 10 kW)

Built Design

Switches	**ANPC Stage:** 4 x CoolMOS CFD7 31mΩ (*Infineon*) **FCC Stage:** 2 x OptiMOS 3 FD 11.1mΩ (*Infineon*)
f_{sw}	16 kHz

▶Optimization: Results



GaN

Silicon

★ **Built Design**

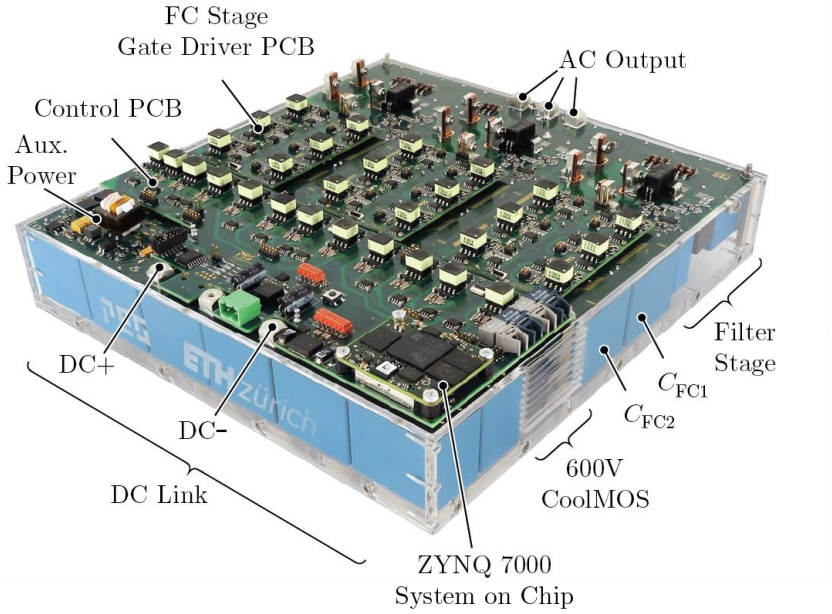
▲ **Current Hardware with *Next* Silicon Semiconductors (*Infineon*)**

▲ Pareto Front Optimization Results (η @ 10 kW)

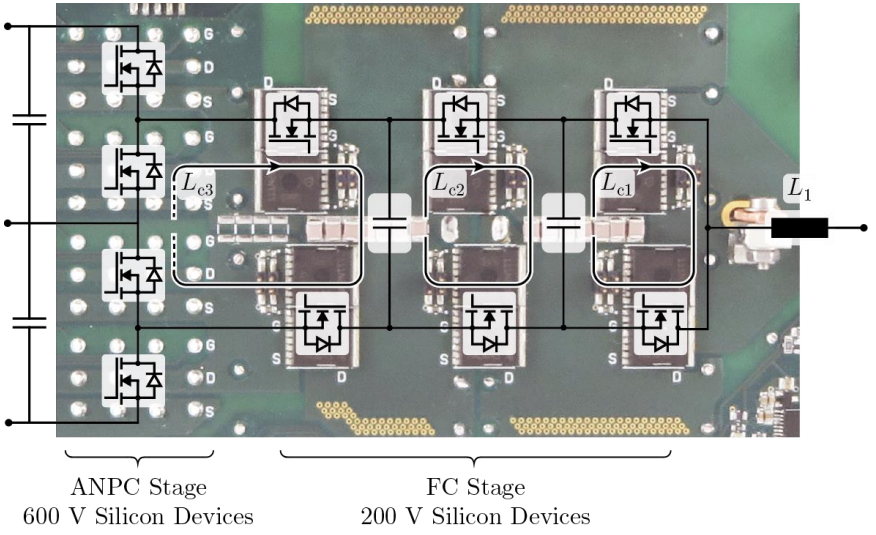
Switches	**ANPC Stage:** 4 x CoolMOS CFD7 31mΩ (*Infineon*) **FCC Stage:** 2 x Next Gen. Silicon (*Infineon*) ▲
f_{sw}	16 kHz

99.35 % Ultra-Efficient 7-Level HANPC Measurements

▶Commutation Path



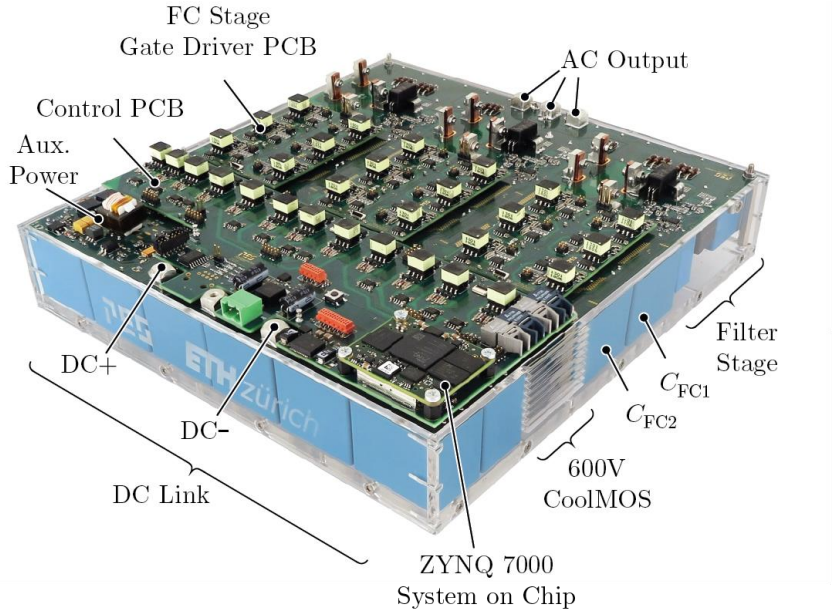
▲ 7L-HANPC Hardware Prototype



▲ Semiconductor Layout on the Power PCB

▶ Final Results

★ **3.34 kW/dm³** (55.9 W/in³)



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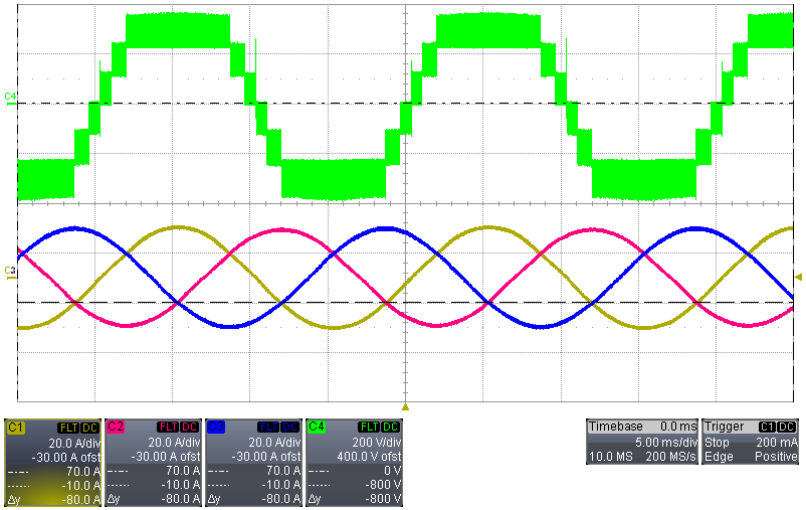
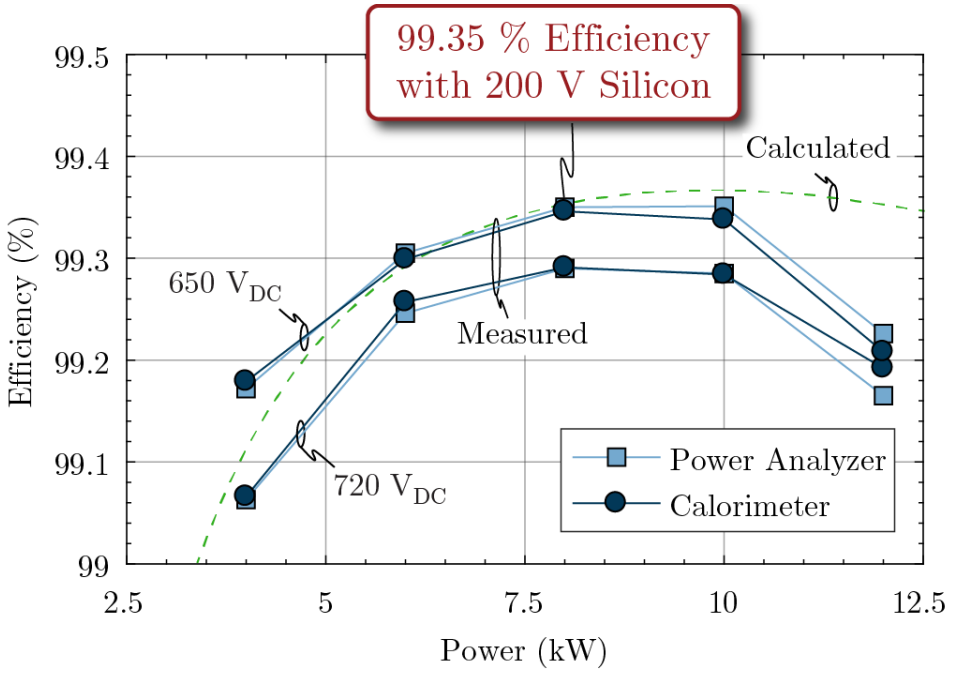
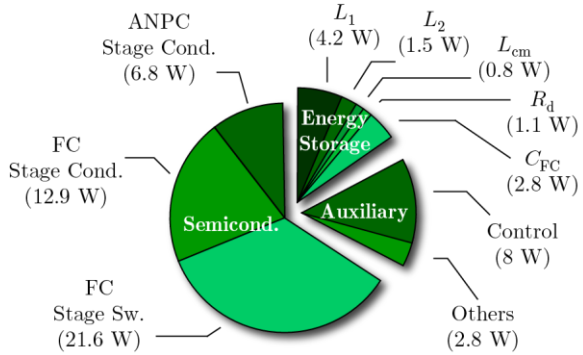


▲ 7-Level Output Voltage and Phase Currents @ 10 kW

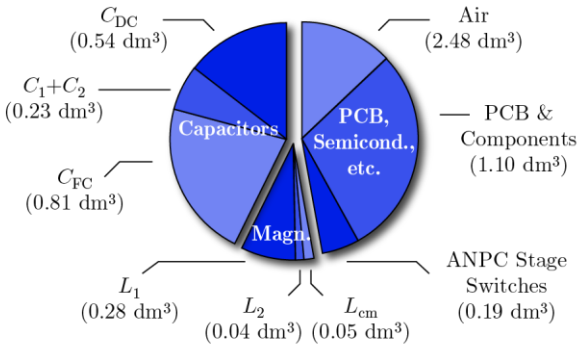
4.8 kg (2.63 kW/kg)

▶Final Results – Efficiency Measurements





◀ Loss Distr. @ 10kW

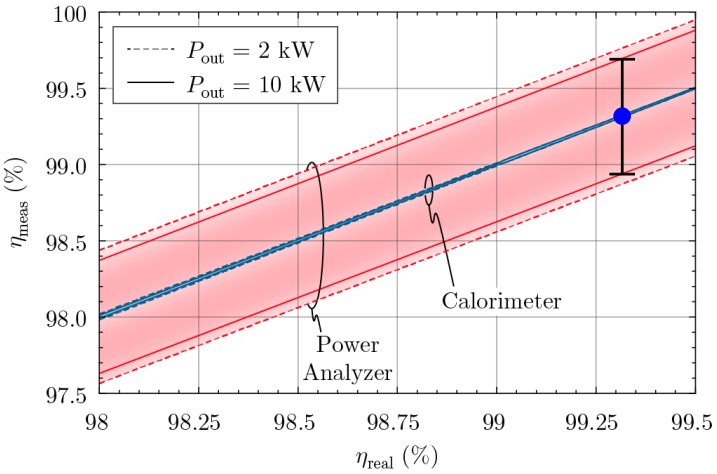


◀ Volume Distr.

▲ Measured Efficiency in Steady-State @ V_{DC} = 720V and V_{DC} = 650V

▶ Electric vs. Calorimetric Efficiency Measurements

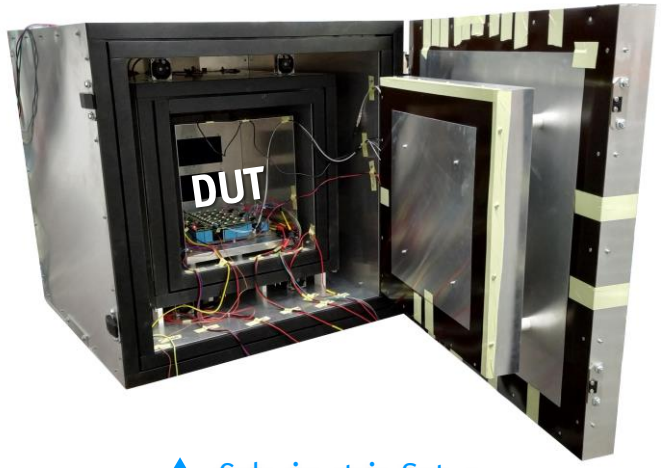
■ Large Uncertainty in Loss Determination with Electric Efficiency Measurement



99.73%
....
99.35% **(±0.38%)**
....
98.97%

▲ Error Bars for Electric & Calorimetric Eff. Meas. Methods

▲ Yokogawa WT3000 Precision Power Analyzer

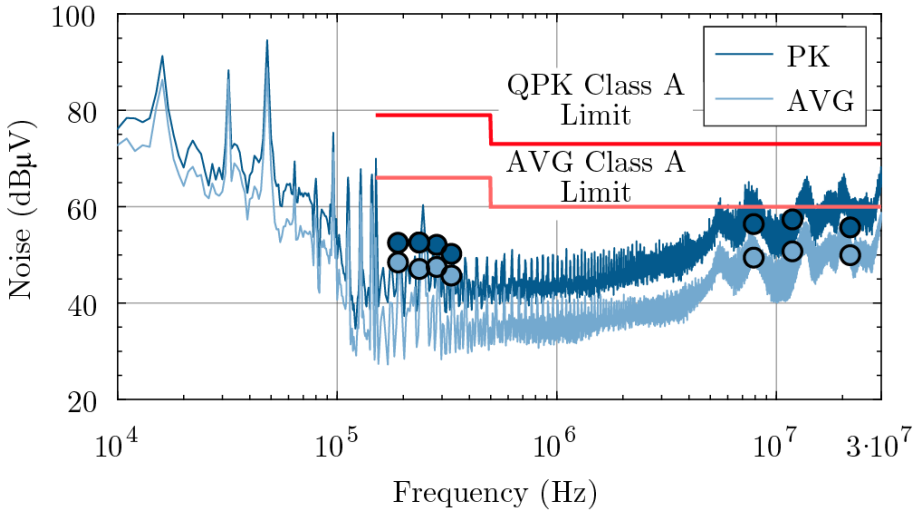


▲ Calorimetric Setup

➢ In This Case, Both Efficiency Measurement Methods Match, But Uncertainty is Too Large

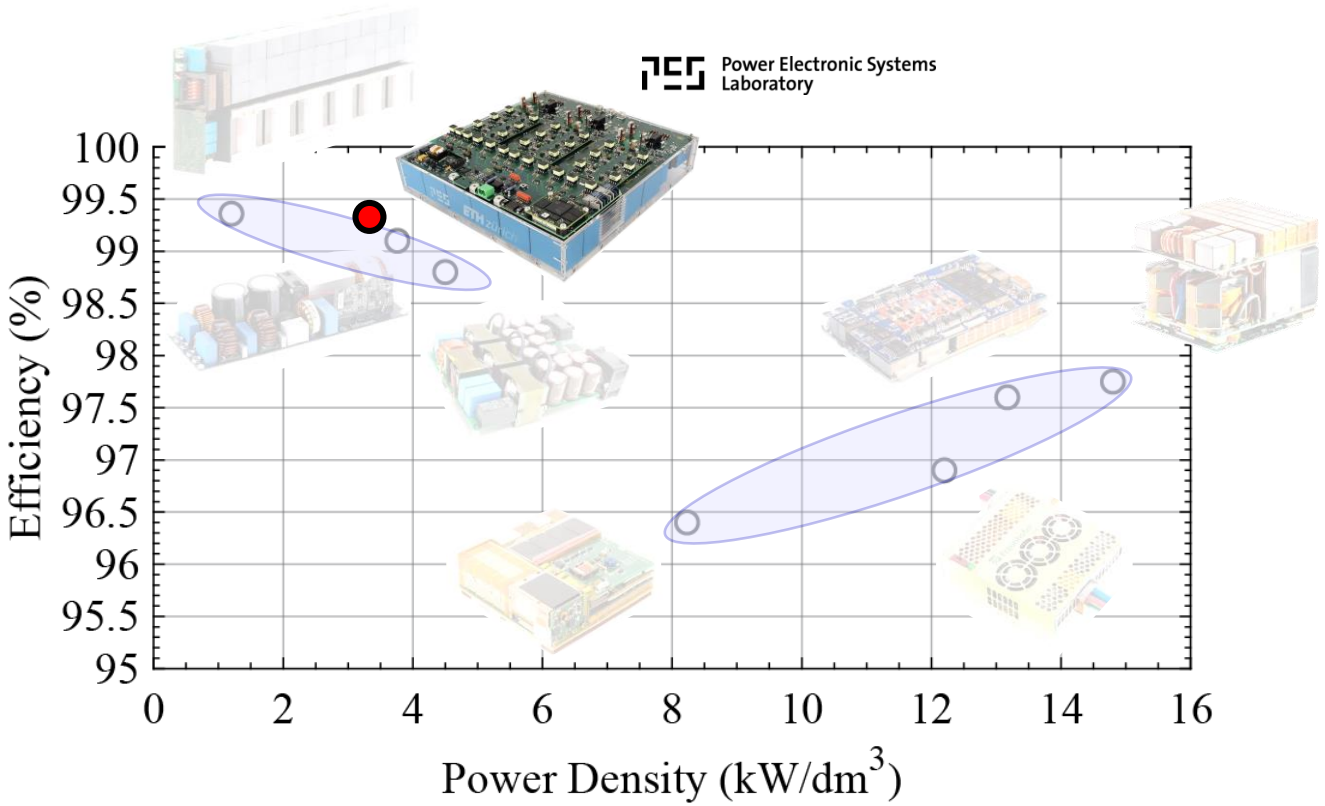
▶ Final Results – EMI Measurements

■ Hardware Passes EMI CISPR Class A Requirements



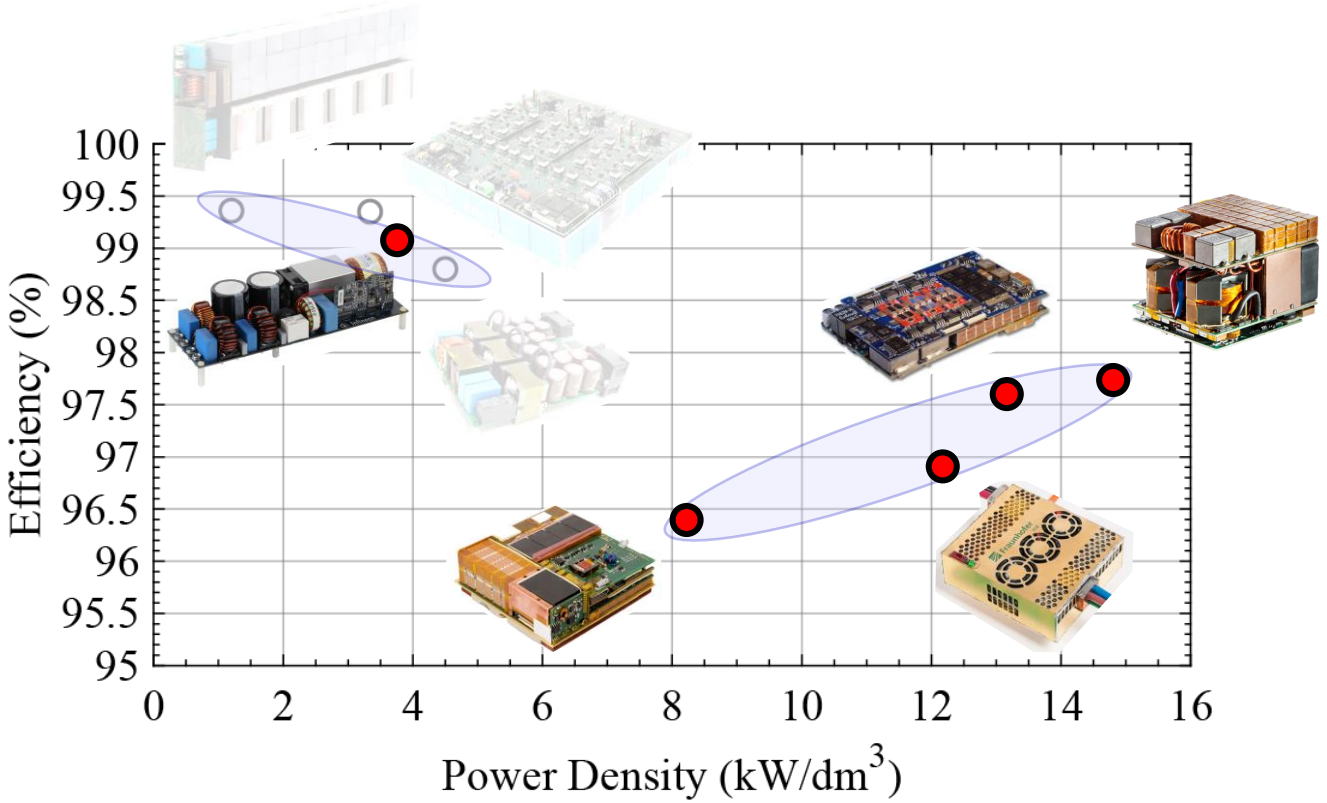
▲ Measured EMI Spectrum with the Quasi-Peak (QPK) and Average (AVG) Test Receivers.

▶ Multi-Level Approach for High-Efficiency



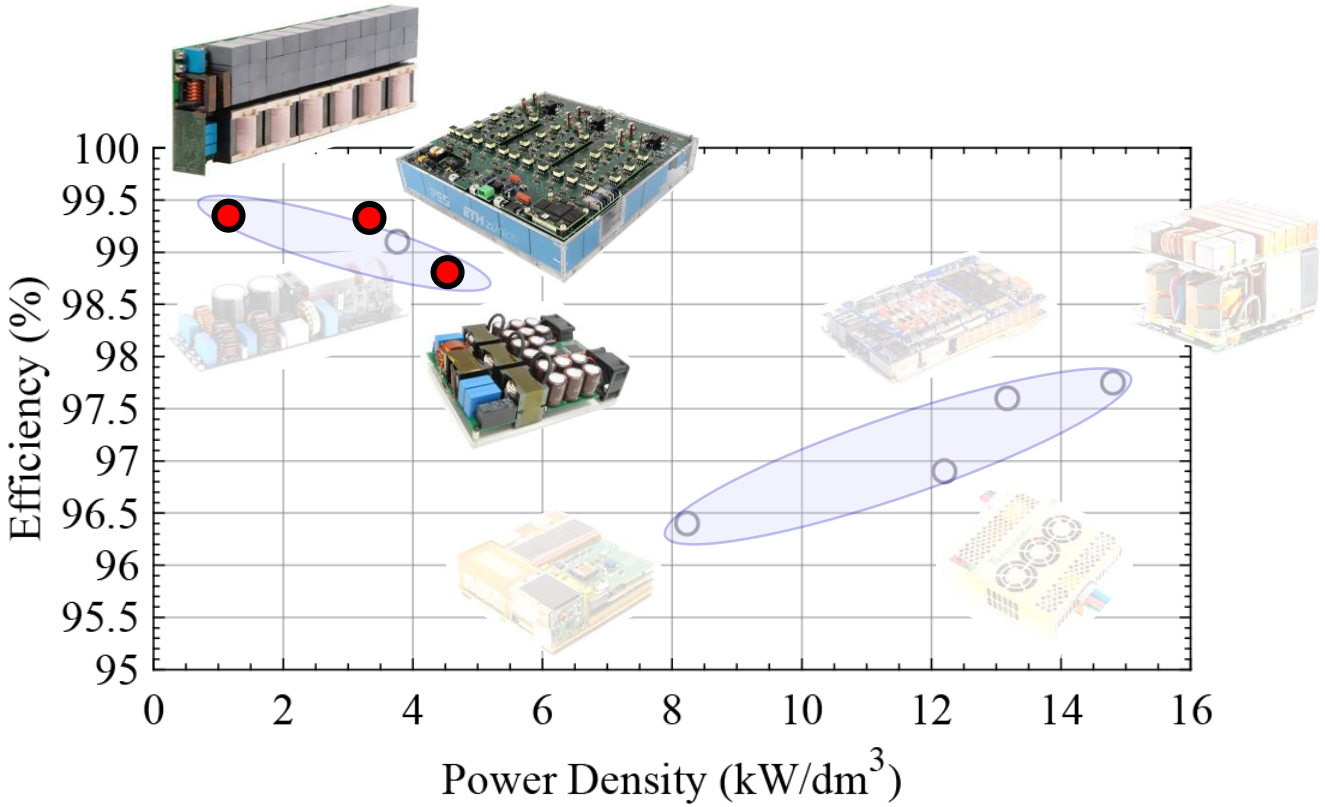
▶ Multi-Level Approach for High-Efficiency

➢ Wide Band-Gap (WBG) Technology



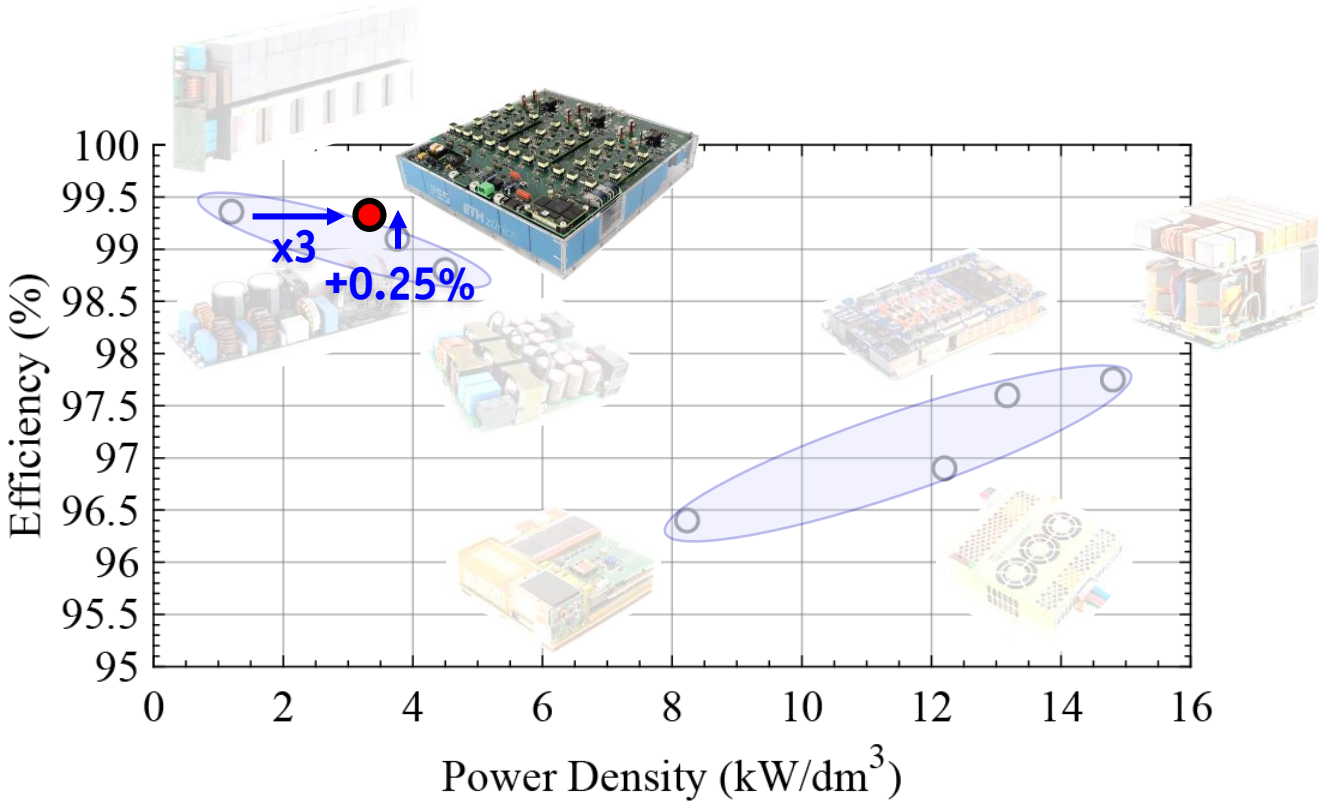
▶ Multi-Level Approach for High-Efficiency

➢ Silicon Technology



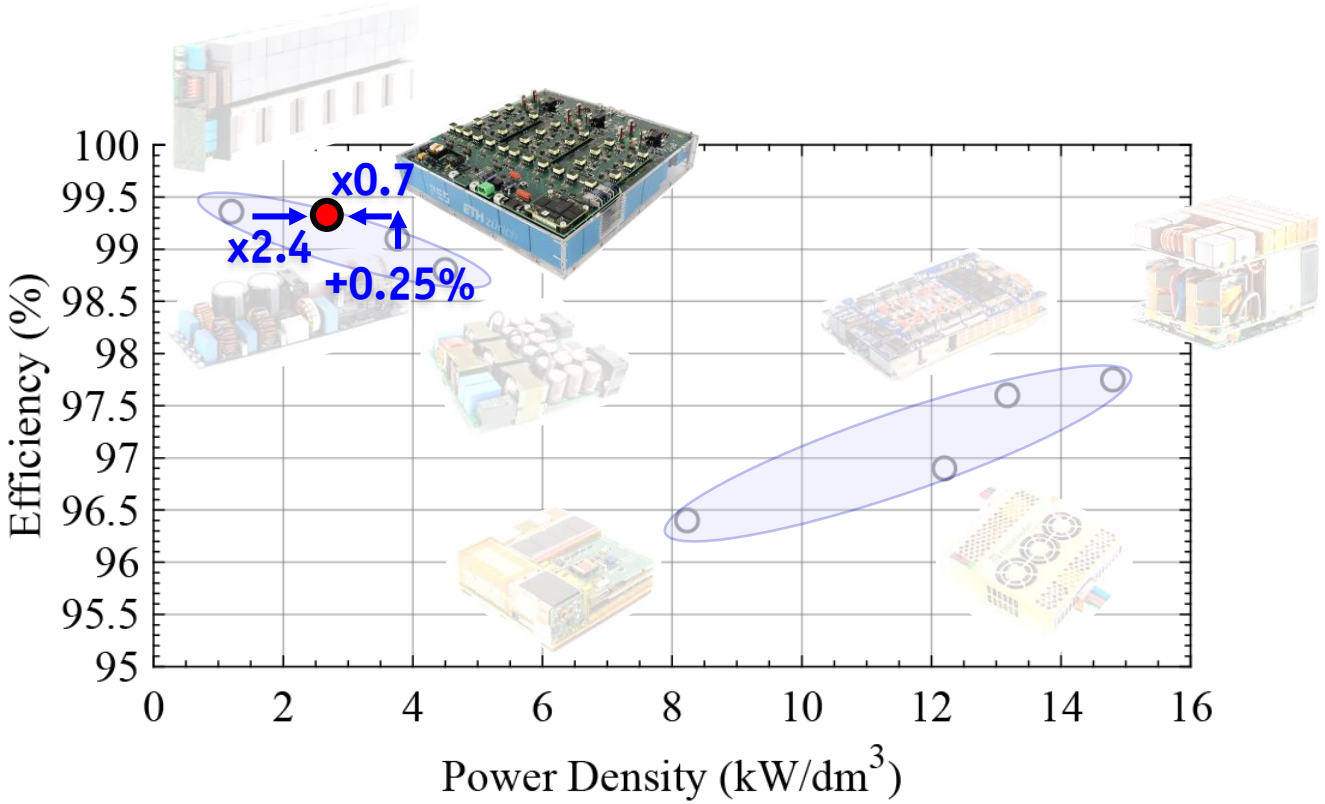
▶ Multi-Level Approach for High-Efficiency

➢ System Comparison



▶ Multi-Level Approach for High-Efficiency

➢ System Comparison → 25% Volume Addition for DC-Link 100Hz Power Buffering



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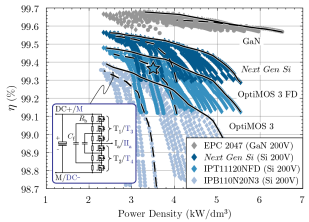

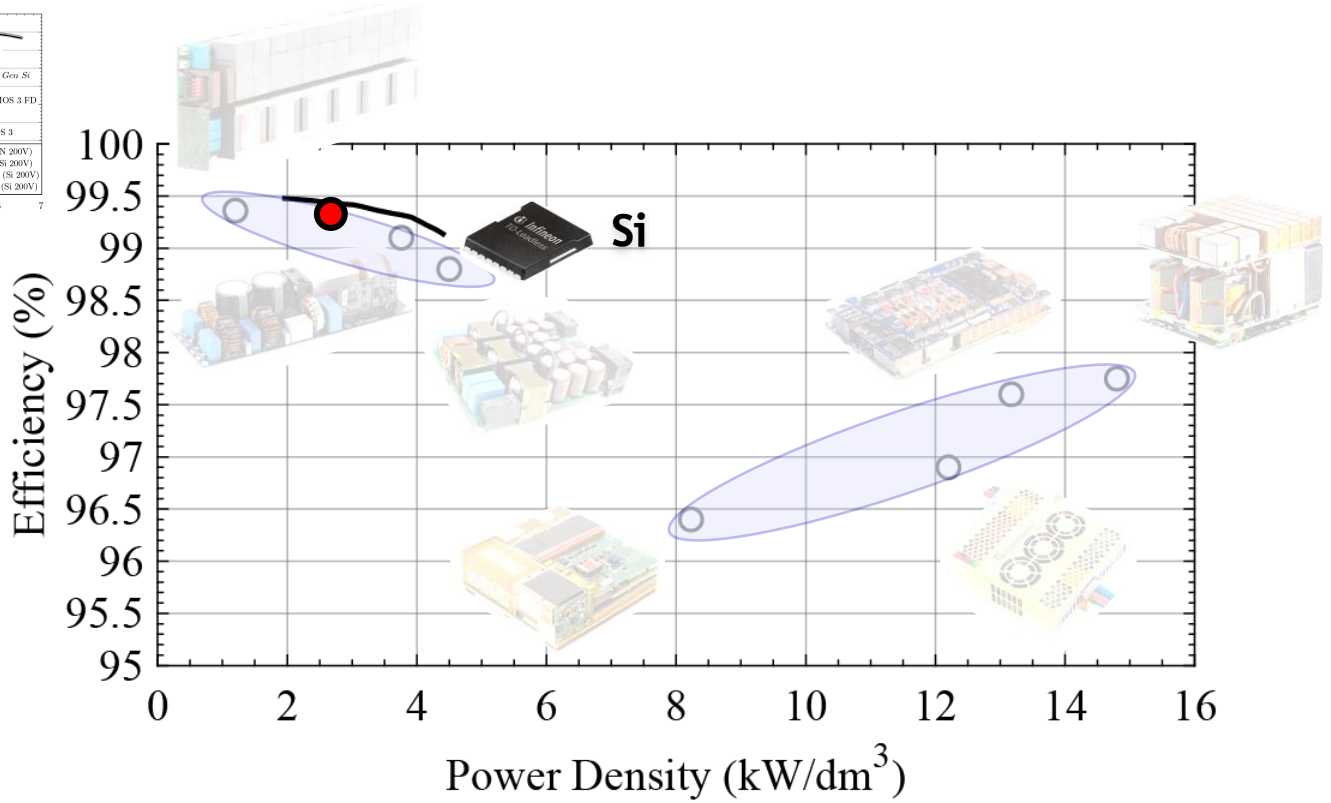

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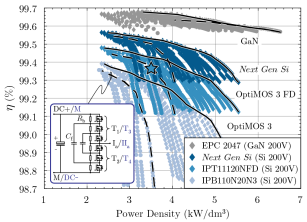
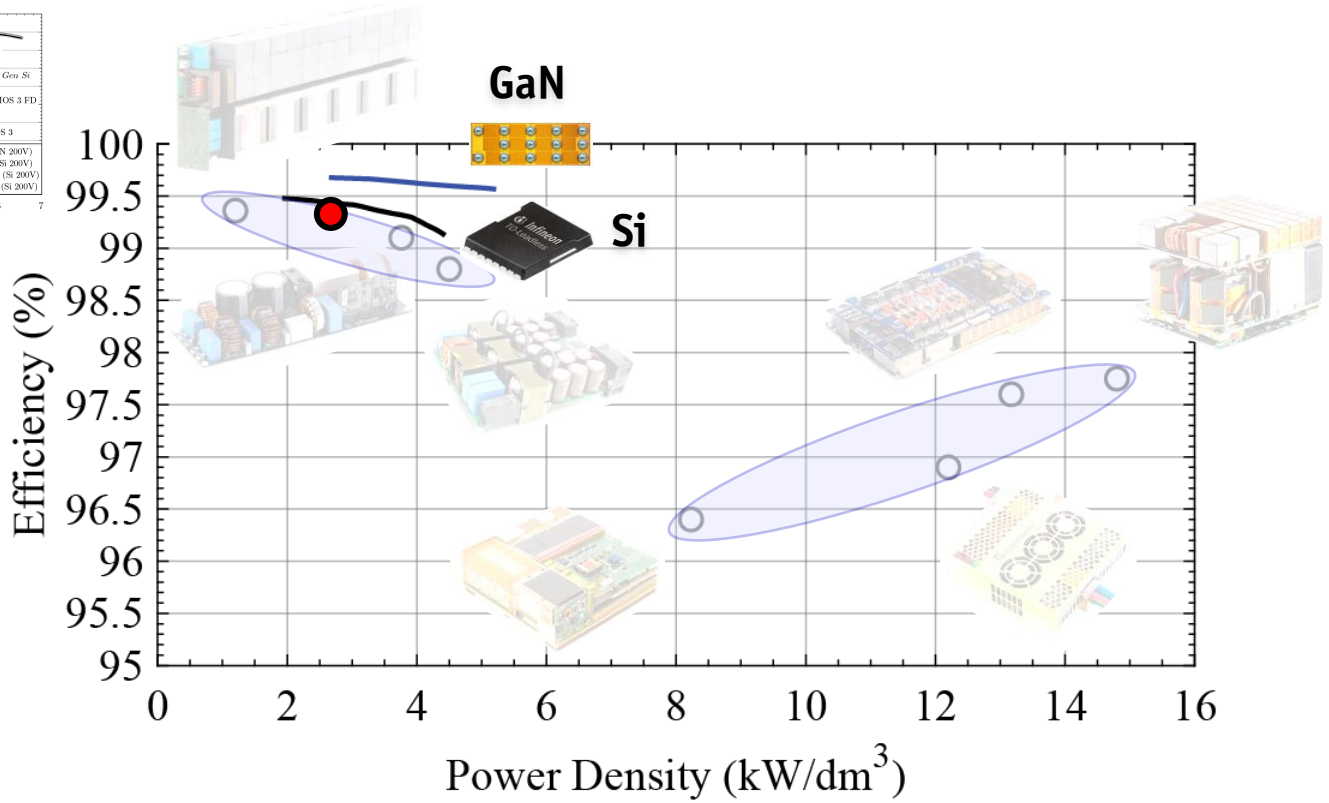




Conclusion: Road towards the Future

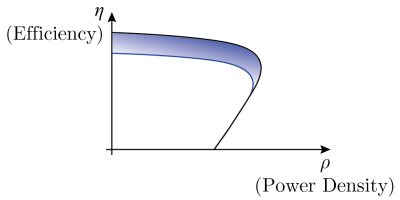
▶ Conclusion

- Multi-Level Converters are Adequate for Ultra-High Efficiency Applications

- Efficiency Barriers Pushed
  - 99.35% Peak Efficiency
  - European Weighted Efficiency ≈ 99.10%
  - California Energy Commission (CEC) Weighted Efficiency ≈ 99.20%

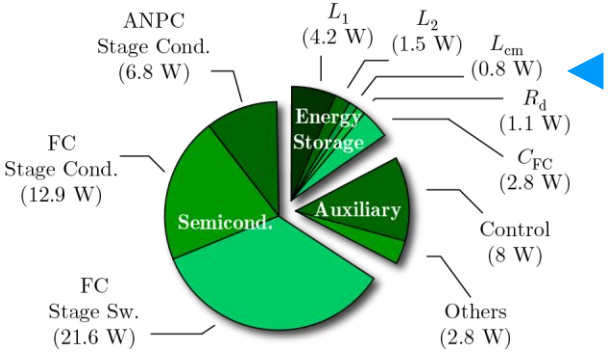
- Ultra-High Efficiency is Achievable with Off-The-Shelf Silicon Semiconductors
- 99.5% Efficiency can be Reached with Next-Generation Silicon Devices
- 99.5+% Efficiency can be Reached with Commercial GaN Devices

▶ Performance Limits & Future Requirements

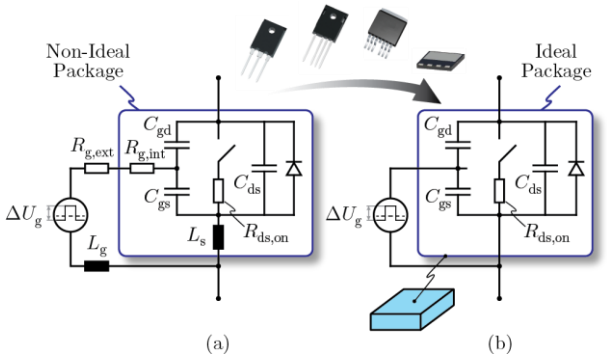


➢ Losses:

- **Semiconductors**
  - 66% of the Losses
  - WBG: Better on Paper… But in Reality?
  - Advanced Packaging → "Ideal Switch"
- **Control**
  - Low Power µC and/or FPGA/CPLD
- **Every Watt Counts…**

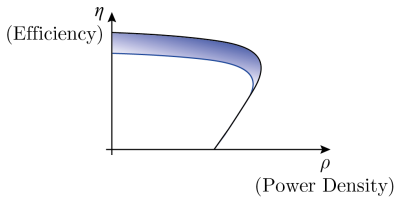


◀ Loss Distr. @ 10kW



▲ Transition Towards Ideal Gate Driver and Package

▶ Performance Limits & Future Requirements



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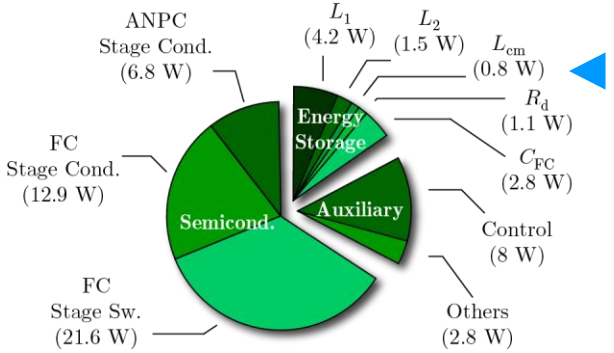
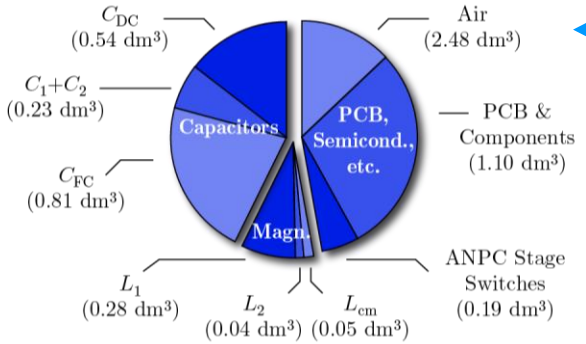


◀ Loss Distr. @ 10kW

➢ Volume:

- Capacitors
  - Determine the Volume for Low Sw. Freq. Converters
  - -0.2% in Efficiency → +50% Power Density
- High Efficiency → No Heat-Sink
- Building Blocks: Standardized and Low Cost



◀ Volume Distr.

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Jon Azurza Anderson (SM´16) received his B.Sc. degree in Industrial Technology Engineering from TECNUN School of Engineering of the University of Navarra in 2014, and his M.Sc. degree in Electrical Engineering from ETH Zurich (with distinction) in 2016, specializing in energy and power electronics. In 2013 and 2014 he worked for Fraunhofer IIS in Nuremberg, Germany, developing software in the RFID & Radio Systems group. In November 2016 he joined the Power Electronics Systems Laboratory (PES) as a scientific assistant, where in February 2017 he began his Ph.D. studies, focusing on ultra-high efficiency three-phase multi-level PWM converters.

Mattia Guacci (SM'16) studied Electronic Engineering at the University of Udine, Italy where in July 2013 and in October 2015 he received his B.Sc. summa cum laude and his M.Sc. Summa cum laude, respectively. In 2014 he was with Metasystems SpA in Reggio nell'Emilia, Italy working on on-board battery chargers for electric vehicles. In November 2015 he joined the Power Electronic Systems Laboratory (PES) at ETH Zurich as a scientific assistant investigating innovative inverter topologies. In September 2016 he started his Ph.D. at PES focusing on advanced power electronics concepts for future aircraft and electric vehicle applications.

Dominik Neumayr (SM'10) started his academic education at the University of Applied Sciences (FH) for Automation Engineering in Wels and received the Dipl.-Ing. (FH) degree in 2008. He was with the Center for Advanced Power Systems (CAPS) in Tallahassee/Florida working on Power/Controller Hardware-in-the-Loop simulations and control systems design for AC/DC/AC PEBB based converter systems from ABB. He continued his academic education at the Swiss Federal Institute of Technology in Zurich (ETH Zurich) and received the M.Sc. degrees in electrical engineering and information technology in 2015. Since spring 2015 he is a PhD student at the Power Electronic Systems (PES) Laboratory, ETH Zurich. His current research focuses on ultra-high power density converter systems.

Johann W. Kolar (F´10) received his Ph.D. degree (summa cum laude) from the Vienna University of Technology, Austria. He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised 70+ Ph.D. students. He has published 880+ scientific papers in international journals and conference proceedings, 4 book chapters, and has filed 190+ patents. He has received 26 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE William E. Newell Power Electronics Award, and the 2016 IEEE PEMC Council Award. He has initiated and/or is the founder of 4 ETH Spin-off companies.

Thank You

Feb. 20th, 2019