

General Perspectives for Power Electronics....

Johann W. Kolar et al.

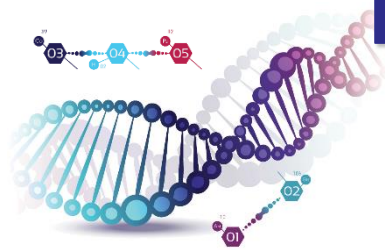


Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

Dec. 2, 2021



The DNA of Future High-Performance Power Electronic Systems



Source: hathornconsultinggroup.com

Johann W. Kolar & Jonas E. Huber

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

Dec. 2, 2021



Outline

- ▶ *Introduction*
- ▶ *X-Technologies*
- ▶ *X-Concepts / «Genes»*
- ▶ *Conclusions*



Source: hathornconsultinggroup.com

Acknowledgement

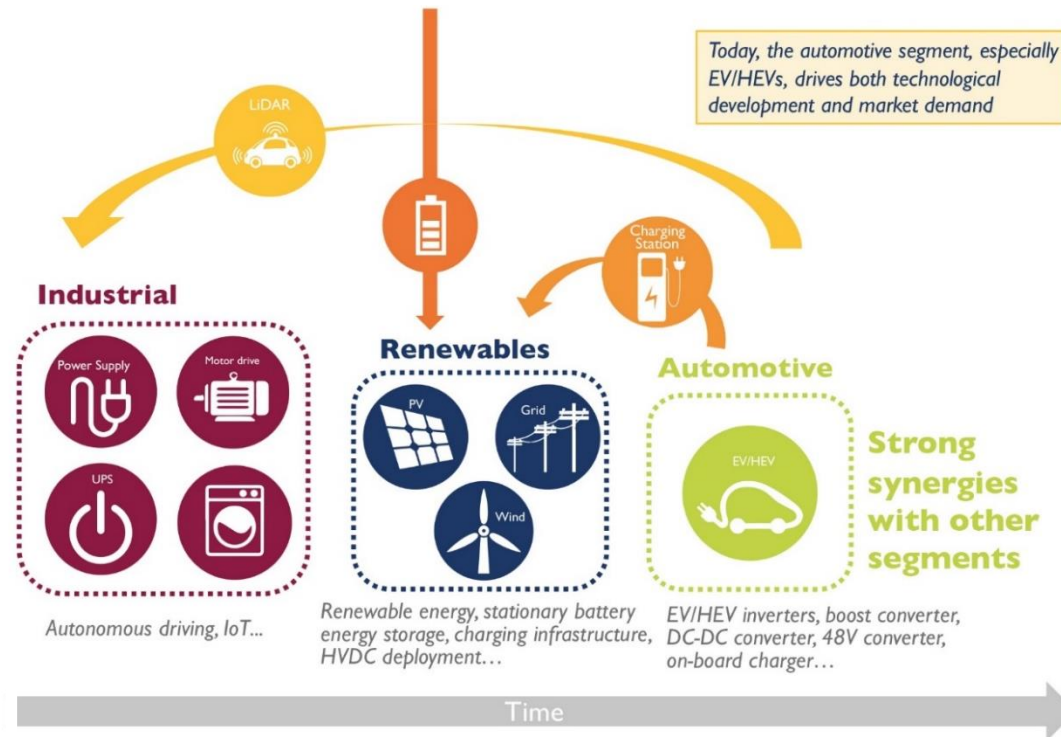
M. Antivachis
J. Azurza
D. Bortis
M. Guacci
T. Guillod
M. Haider
G. Knabben
F. Krismer
D. Menzi
S. Miric
J. Miniböck
N. Nain
J. Schäfer
L. Schrittwieser
F. Vollmaier
St. Waffler
D. Zhang

Power Electronics

*Driving Applications
General Perspective
Performance Indicators / Trends
Technology S-Curve*

Driving Applications

- Global MEGA-Trends → Industry Automation | Renewable Energy | Sustainable Mobility | Urbanization etc.



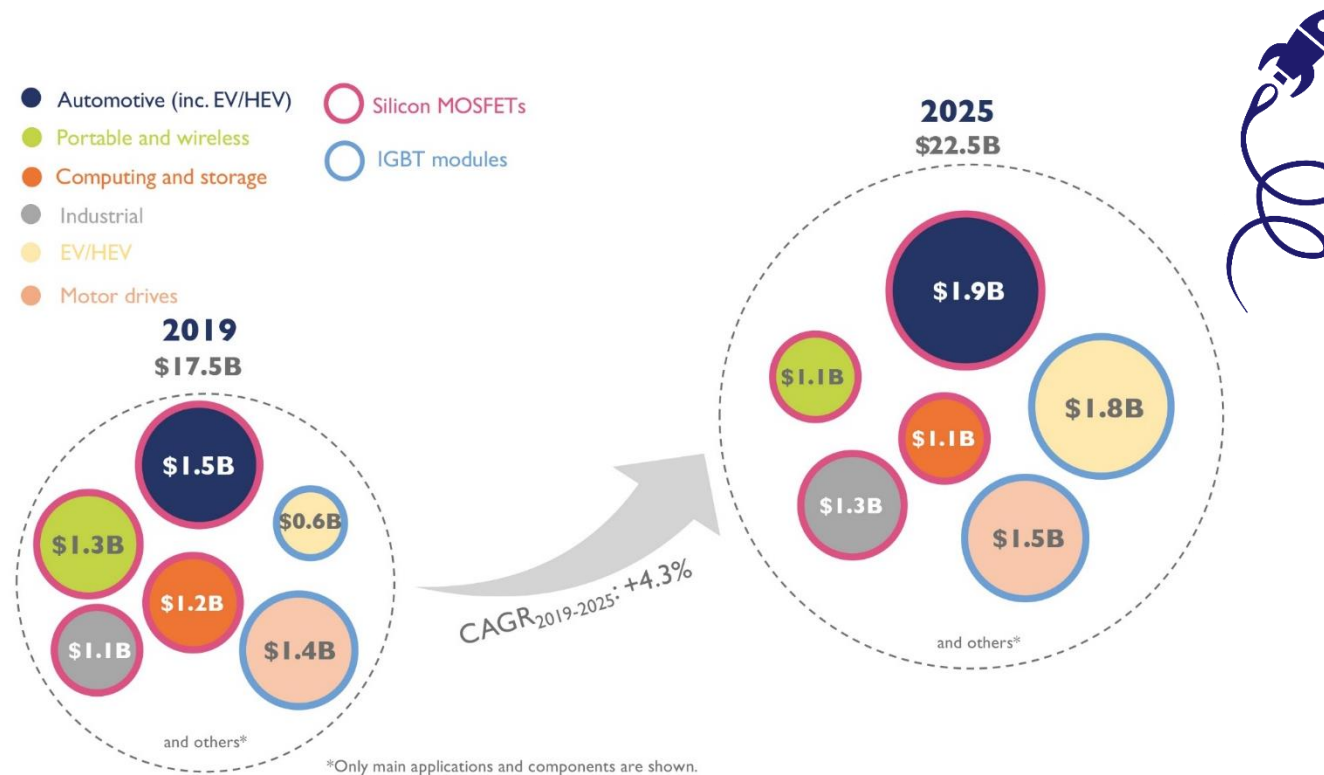
Source: Status of Power Electronics Industry 2019 Report



- Clean Energy Transition → “All-Electric” Society
- UN Sustainable Development Agenda → There can be No “Plan B”, because there is No “Planet B” (Ban Ki-moon)

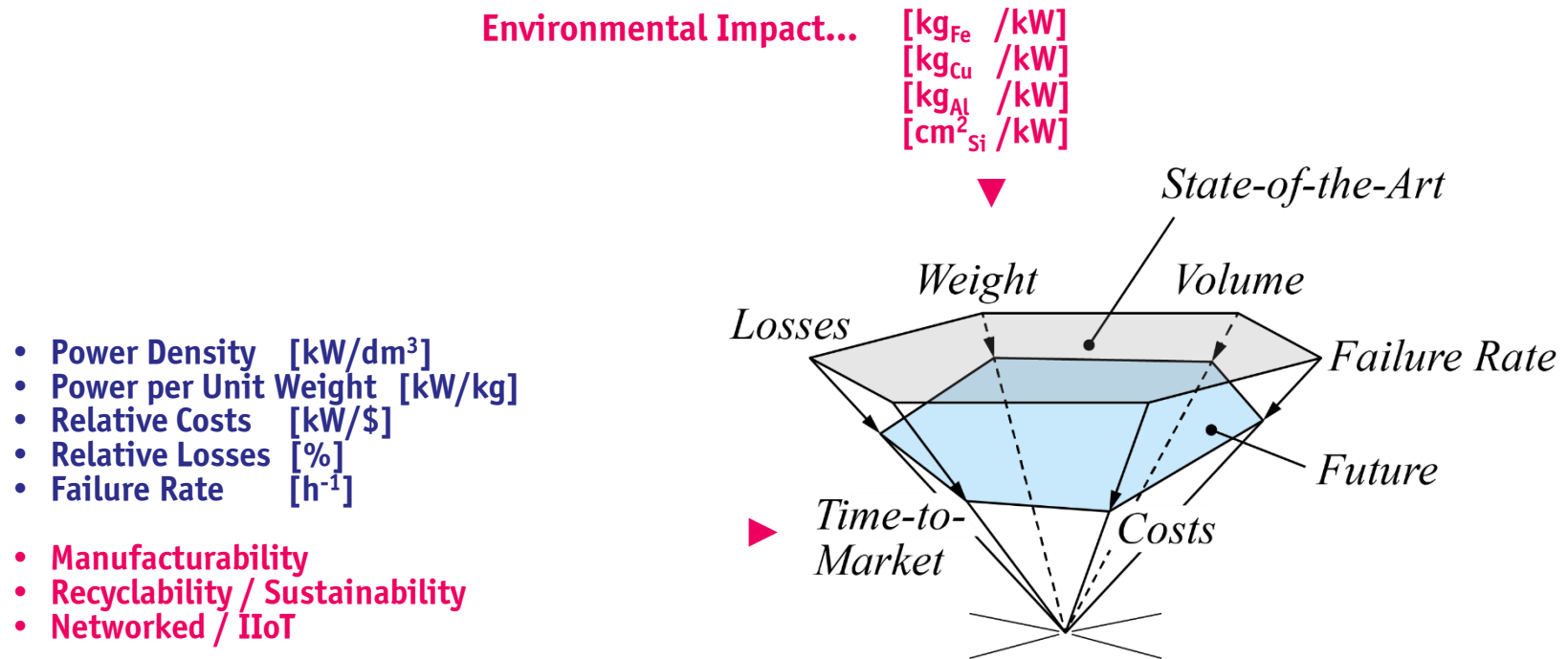
General Perspective

- **Power Electronics is Key to Clean Energy Utilization | Automation | etc.** → “All-Electric Society”
- **2019 — 2015 Power Electronics Market Evolution & Main Segments**



- **Source – Status of the Power Electronics Industry 2020 Report**

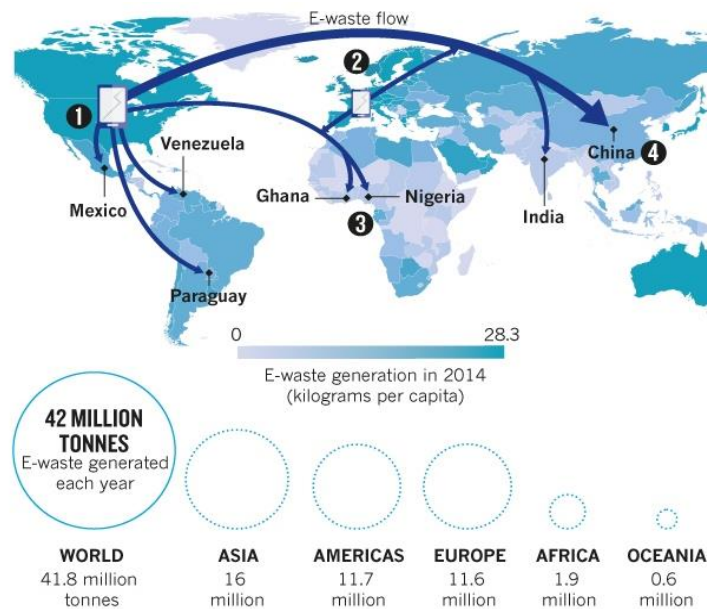
Performance Indicators / Trends



Remark Increasing E-Waste Problem

- 53'000'000 Tons of Electronic Waste Produced Worldwide in 2019 → 74'000'000 Tons in 2030
- Large Proportion Ends up in **Africa & China** → Melting of PCBS & Cables etc. / Hazardous Substances
- **Increasingly Complex Constructions** → No Repair or Recycling

Source:
Green IT
Solution



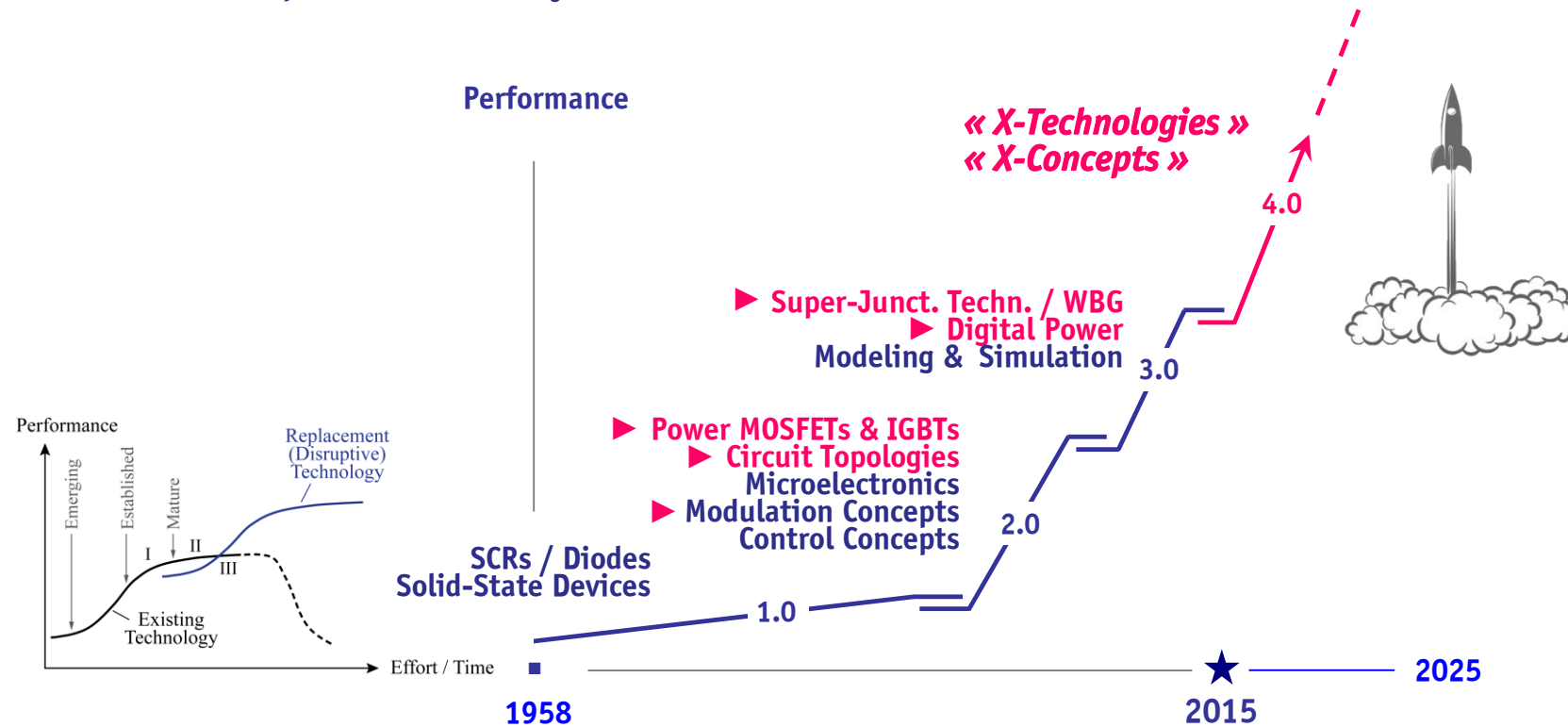
Source: nature



- Growing Global E-Waste Streams → Increasing Attention of the Public / Upcoming Regulations

S-Curve of Power Electronics

- « X-Technologies » / “Moon-Shot” Technologies
- « X-Concepts » → Full Utilization of Basic Scaling Laws & « X-Technologies »
- Power Electronics 1.0 → Power Electronics 4.0
- 2...5...10x Improvement NOT Only 10% !



X-Technologies

***SiC | GaN
3D-Packaging & Integration
Digital Signal Processing
Energy Storage***

X-Technology  *SiC | GaN*

Low $R_{DS(on)}$ High-Voltage Devices

- Higher Critical E-Field of SiC → Thinner Drift Layer
- Higher Maximum Junction Temperature $T_{j,max}$

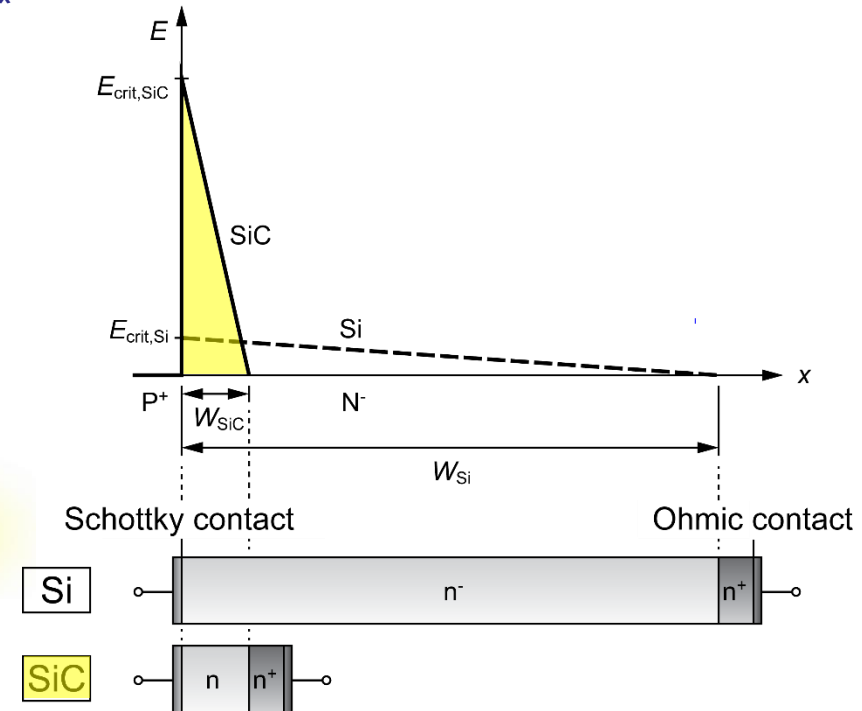
at 300 K	Si	GaAs	4H/6H-SiC	GaN
E_g (eV)	1.12	1.4	3.0-3.2	3.4
E_c (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm ² /Vs)	1350	8500	100-1000	1000
ϵ_r	11.9	13	10	9.5
V_{sat} (cm/s)	1×10^7	1×10^7	2×10^7	3×10^7
λ (W/cmK)	1.5	0.5	3 - 5	1.3

© 2000 Carl-Mikael Zetterling

$$R_{on}^* = \frac{4V_B^2}{\epsilon\mu_n E_C^3} \leftarrow \text{For 1kV:}$$

	Si	SiC
W (μm)	100	10
N_D (cm ⁻³)	10^{14}	10^{16}

$$R_{on,SiC}^* \approx \frac{1}{300} R_{on,Si}^*$$



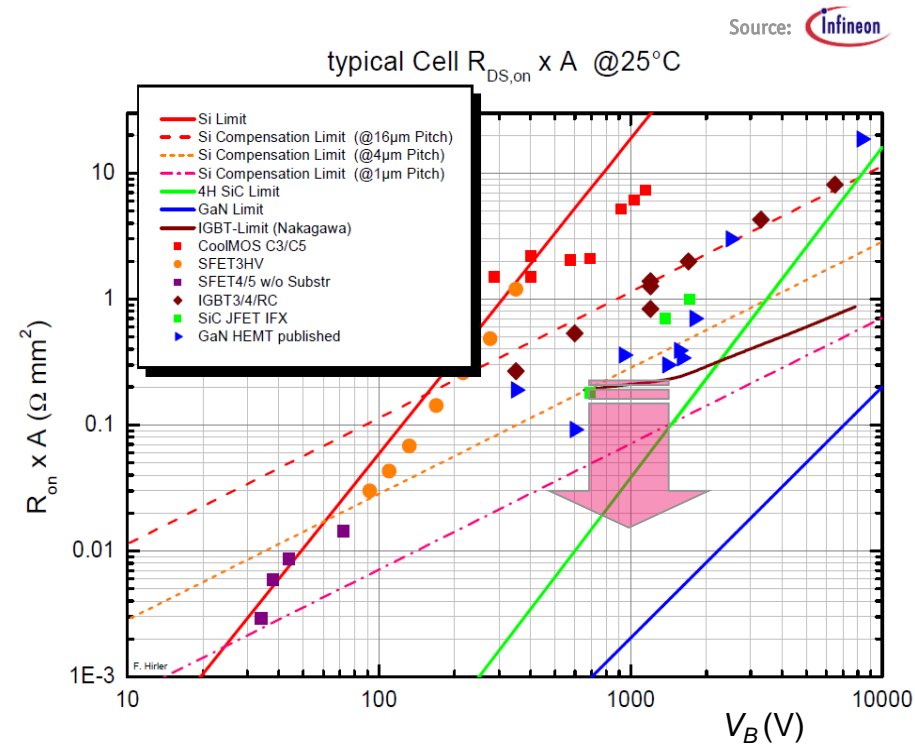
- Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices

Low $R_{DS(on)}^*$ High-Voltage Devices

- *SiC MOSFETs / GaN HEMTs (Monolithic AC-Switch)*
- *Low Conduction Losses & ZVS*
- *High Efficiency*

$$R_{on}^* = \frac{4V_B^2}{\epsilon\mu_n E_C^3} \leftarrow$$

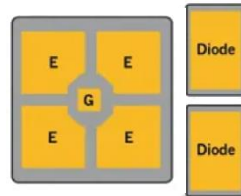
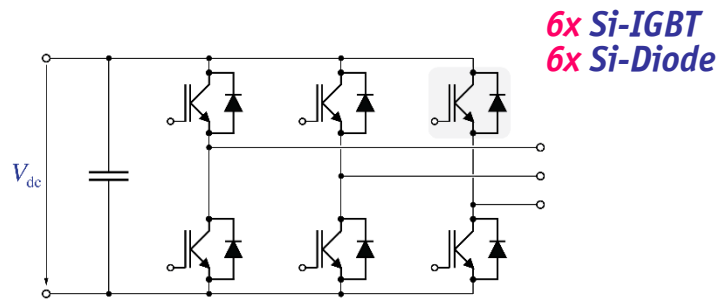
$$R_{on,SiC}^* \approx \frac{1}{300} R_{on,Si}^*$$



- *High-Voltage Unipolar (!) Devices → Excellent Switching Performance*

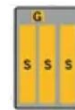
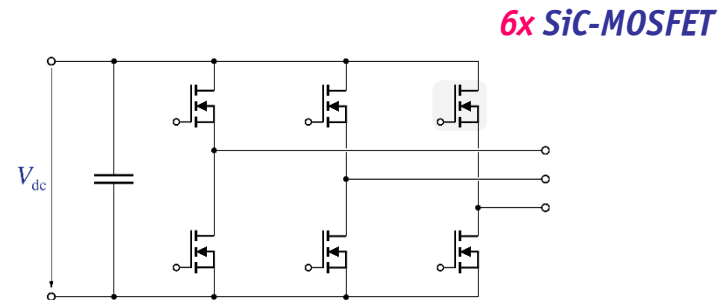
Si vs. SiC

- **Si-IGBT / Diode** → **Const. On-State Voltage, Turn-Off Tail Current & Diode Reverse Recovery Current**
- **SiC-MOSFET** → **Massive Loss Reduction @ Part Load BUT Higher R_{th}**



1200 V 100 A
Die Size: 98.8 mm² + 39.4 mm²

Source:
ATZ elektronik
2018



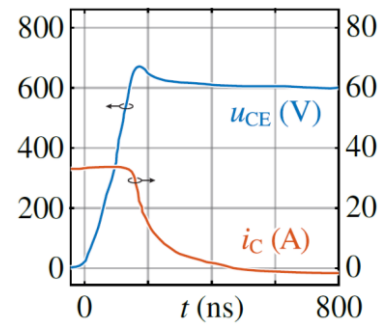
1200 V 100 A
Die Size: 25.6 mm²

Source: Cree

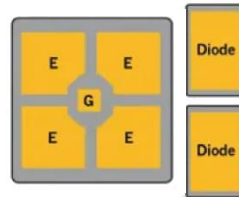
- **Space Saving of >30% on Module Level (!)**

Si vs. SiC Switching Behavior

- **Si-IGBT** → *Const. On-State Voltage Drop / Rel. Low Switching Speed,*
- **SiC-MOSFETs** → *Resistive On-State Behavior / Factor 10 Higher Sw. Speed*

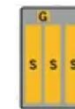
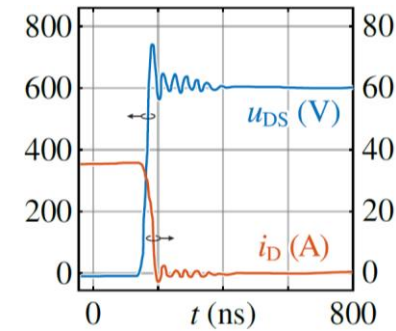


Source: Fuji Electric



1200V 100A
Die Size: $98.8\text{mm}^2 + 39.4\text{mm}^2$

Source: Infineon



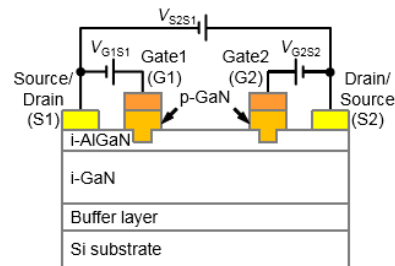
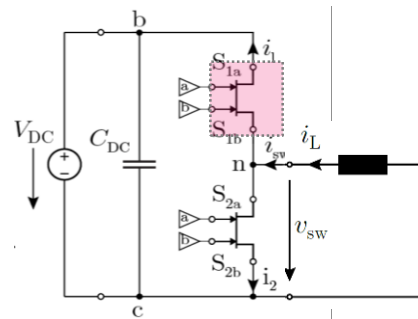
1200V 100A
Die Size: 25.6mm^2

Source: Cree

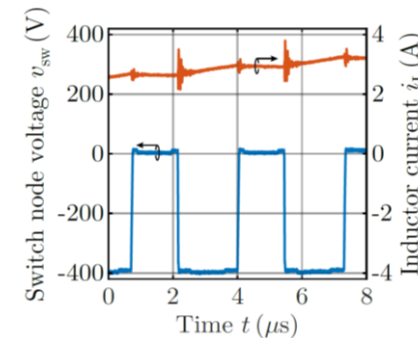
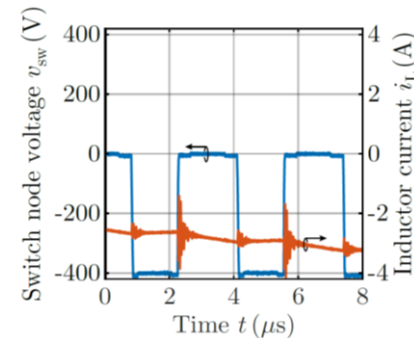
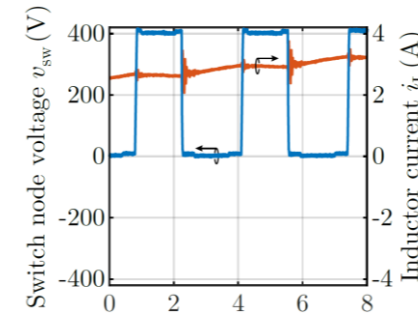
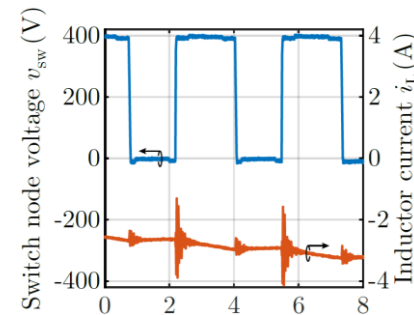
- **Extremely High di/dt & dv/dt** → *Challenges in Packaging / EMI*

Monolithic 600V GaN Bidirectional/Bipolar Switch

- **POWER AMERICA Program** — Based on Infineon's CoolGaN™ HEMT Technology 
- **Dual-Gate Device / Controllability of Both Current Directions**
- **Bipolar Voltage Blocking Capability | Normally-On or -Off**



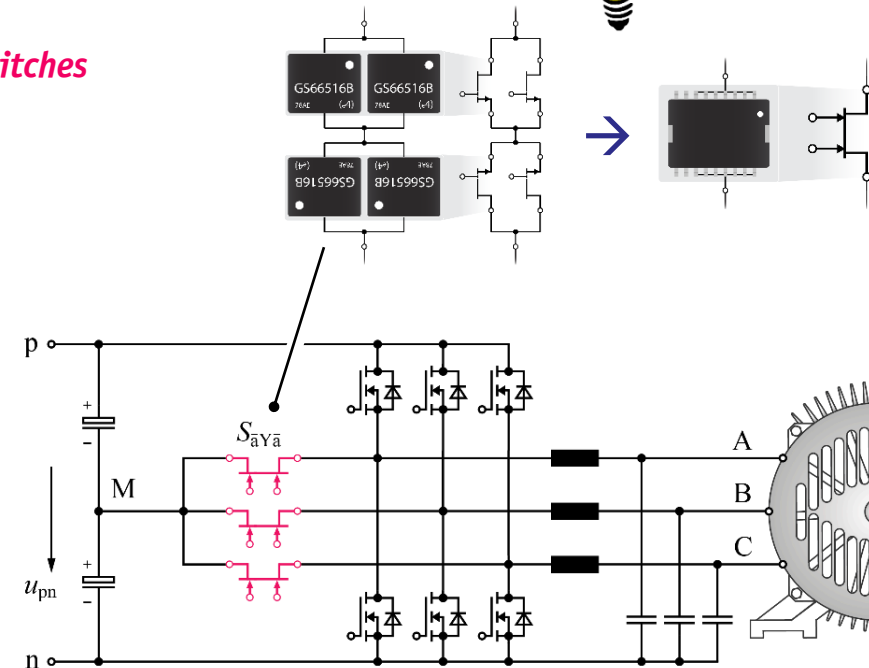
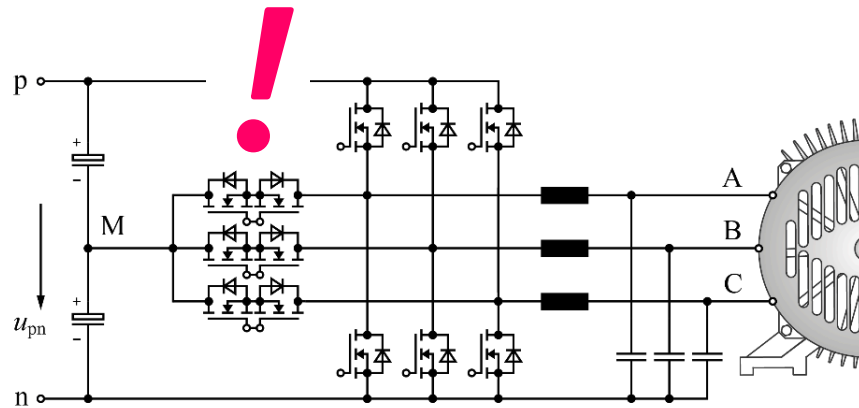
Source: **Panasonic**
ideas for life



- **Analysis of 4-Quadrant Operation of $R_{DS(on)} = 140\text{m}\Omega$ | 600V Sample @ $\pm 400\text{V}$**

Example of 3-Level T-Type Inverter

- Utilization of 600V **Monolithic Bidirectional GaN Switches**
- 2-Gate Structure Provides Full Controllability



- **Factor 4 (!) Reduction of Chip Area vs. Discrete Realization**

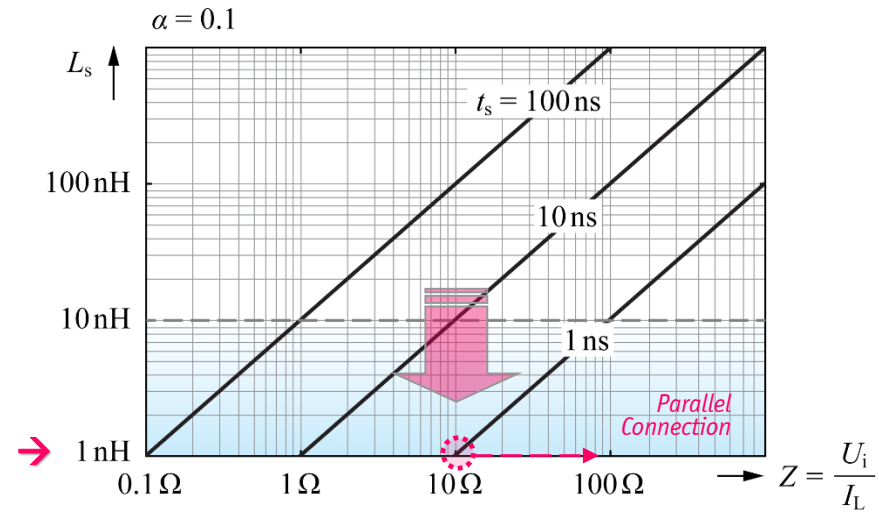
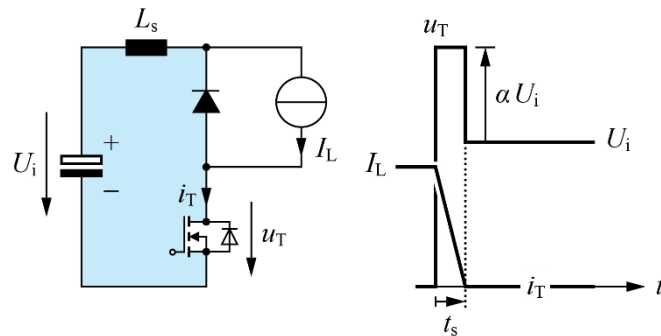


Circuit Parasitics

- Extremely High di/dt
- Commutation Loop Inductance L_s
- Allowed L_s Directly Related to Switching Time t_s →

$$L \frac{di}{dt} = u$$

$$L_s \leq \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \frac{U_i}{I_L}$$

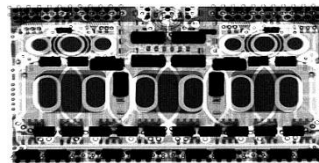
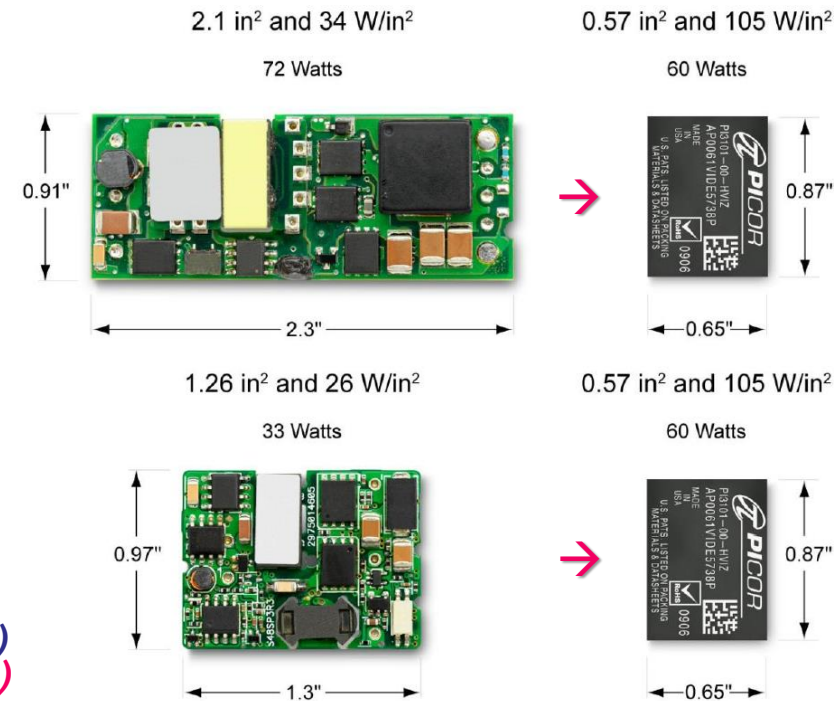


- Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents (Z-Matching)

3D-Packaging / Heterogeneous Integration

- **System in Package (SiP) Approach**
- **Minim. of Parasitic Inductances** / EMI Shielding / Integr. Thermal Management
- **Very High Power Density** (No Bond Wires / Solder / Thermal Paste)
- **PCBs Embedded Optic Fibres**
- **Automated Manufacturing**
- **Recycling (?)**

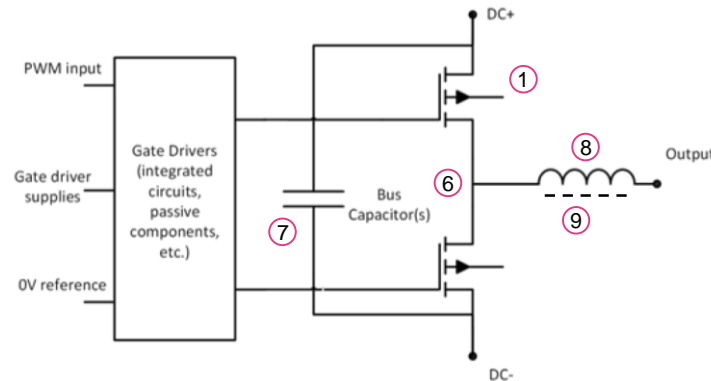
Source: 



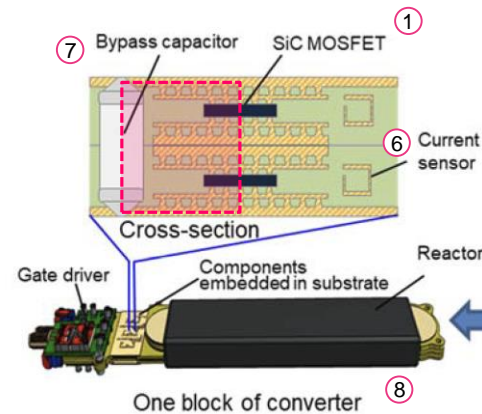
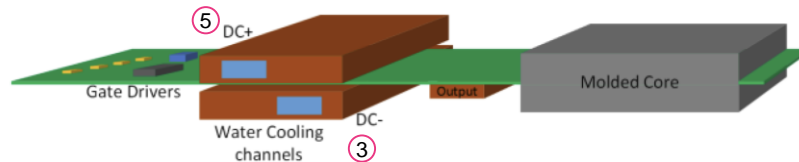
- **Future Application Up to 100kW (!)**
- **New Design Tools & Measurement Systems (!)**
- **University / Industry Technology Partnership (!)**

High-Power PCB-Embedding Technology

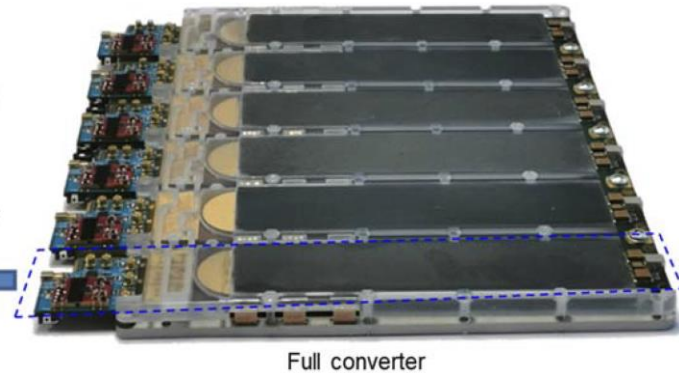
- **PCB Integr. of SiC Chips / Passives / Sensors etc.** → **PCB Design Software / Custom Design / Low \$\$\$**
- **3D-Vertical Multilayer Structure** → **Ultra-Low Comm. & Gate Loop Ind. < 1nH / Low Sw. Losses & EMI**
- **Multi-Functional Use of Busbars** → **DC Supply & 2-Side Liquid Cooling of SiC Chips**
- **Results in Flat Structures (!)**



400um & 35um Cu Layers



Source: **mitsubishi electric** St. Mollov et al., 2019
Changes for the Better

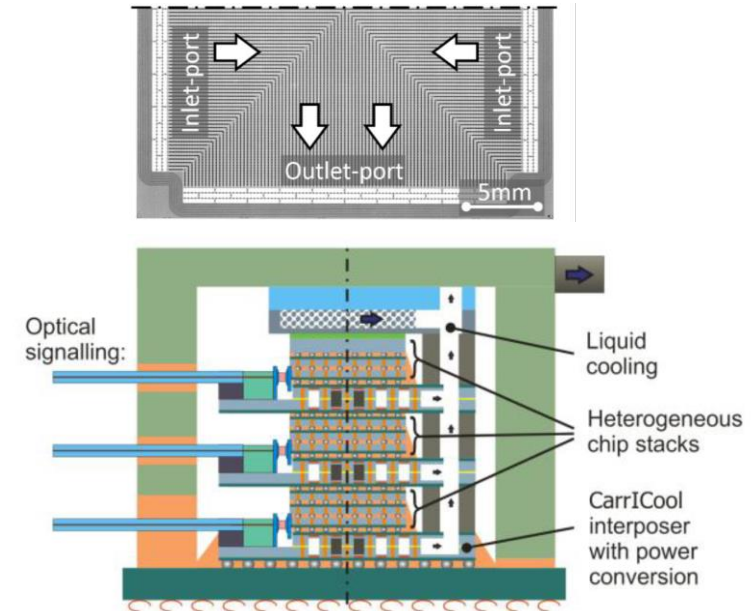
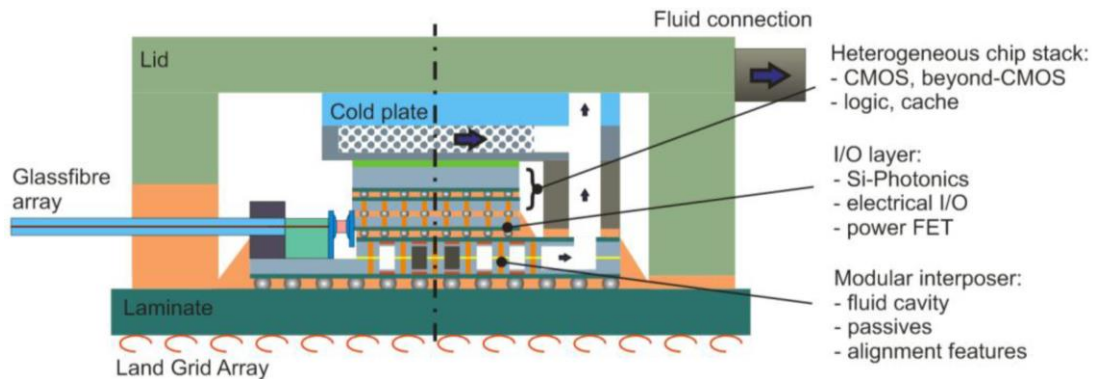


- **800V DC-Link Bidirectional 100kW SiC DC/DC-Converter (24 x 18 x 1.7cm)**

★ **≈ 136 kW/dm³**

Remark Future uP Chip-Stack Packaging

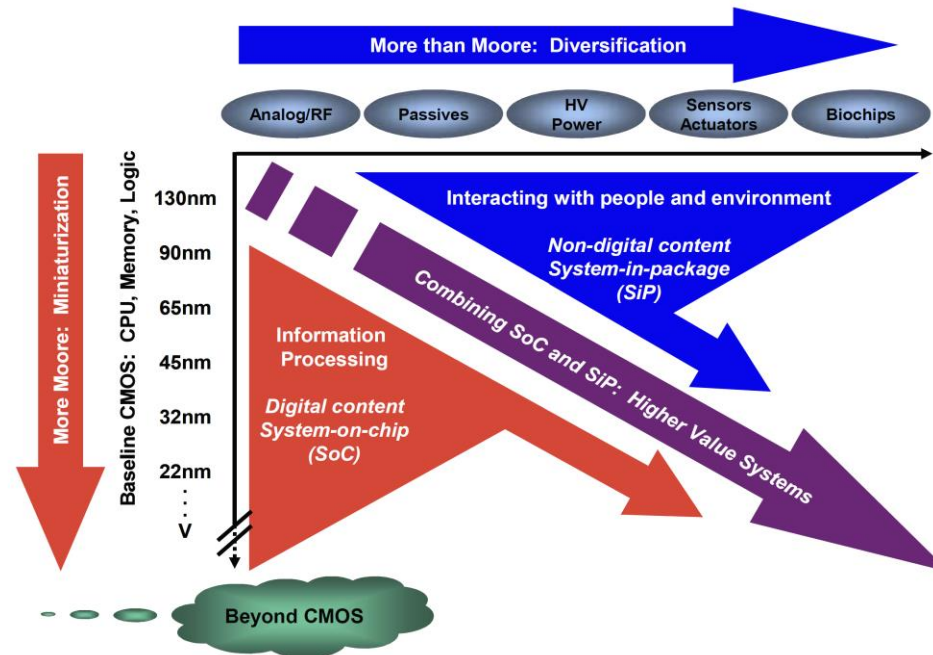
- Slowing Transistor Node Scaling → Vertical & Heterogeneous Integr. of ICs for Performance Gains
- Extreme 3D-Integrated Cube-Sized Compute Nodes
- *Dual Side & Interlayer Microchannel Cooling*



- Interposer Supporting *Optical Signaling* / *Volumetric Heat Removal* / *Power Conversion*

Remark “More Moore” & “More-than-Moore”

- CMOS-Based Digital Domain for Memory & uP → Technology Driven Miniaturization / “Moore’s Law”
- Applications → Multi-Funct. Heterogeneous Analog & Mixed-Signal Systems → “More-than-Moore”
- Dual Trend → Int. Roadmap for Devices and Systems (ITRS → IRDS, since 2005)



- Development of Generic Appl.-Specific Technology Modules / Technology Platforms
- Close Analogy to WBG Power Semiconductors & Full Converter Systems

X-Technology



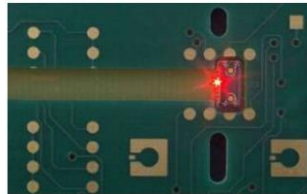
*Digital Signal /
Data Processing*

Digital Signal & Data Processing

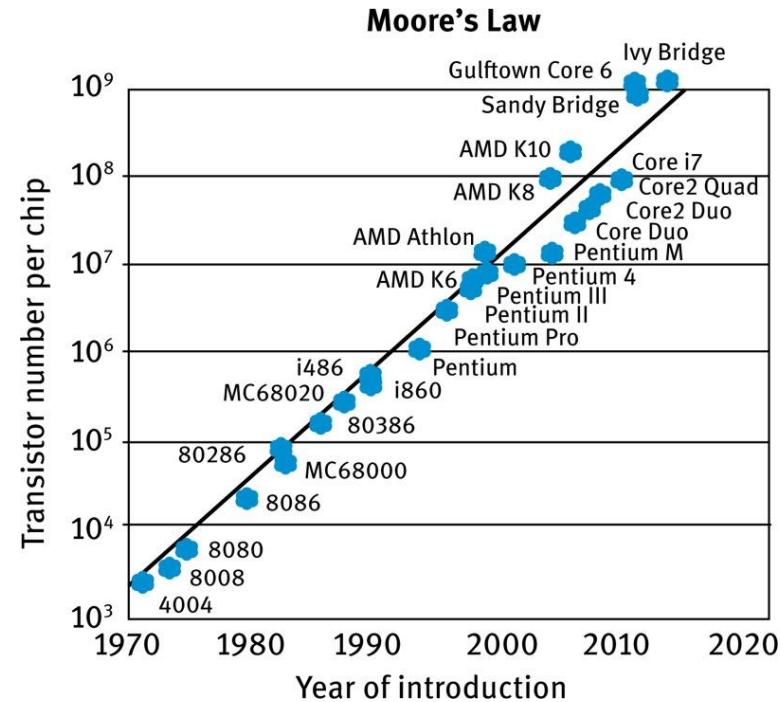
■ Exponentially Improving μC / Storage Technology (!)

- Extreme Levels of Density / Processing Speed
- Software Defined Functions / Flexibility
- Continuous Relative Cost Reduction

Source: vario-optics.ch/
Electro-Optical PCBs

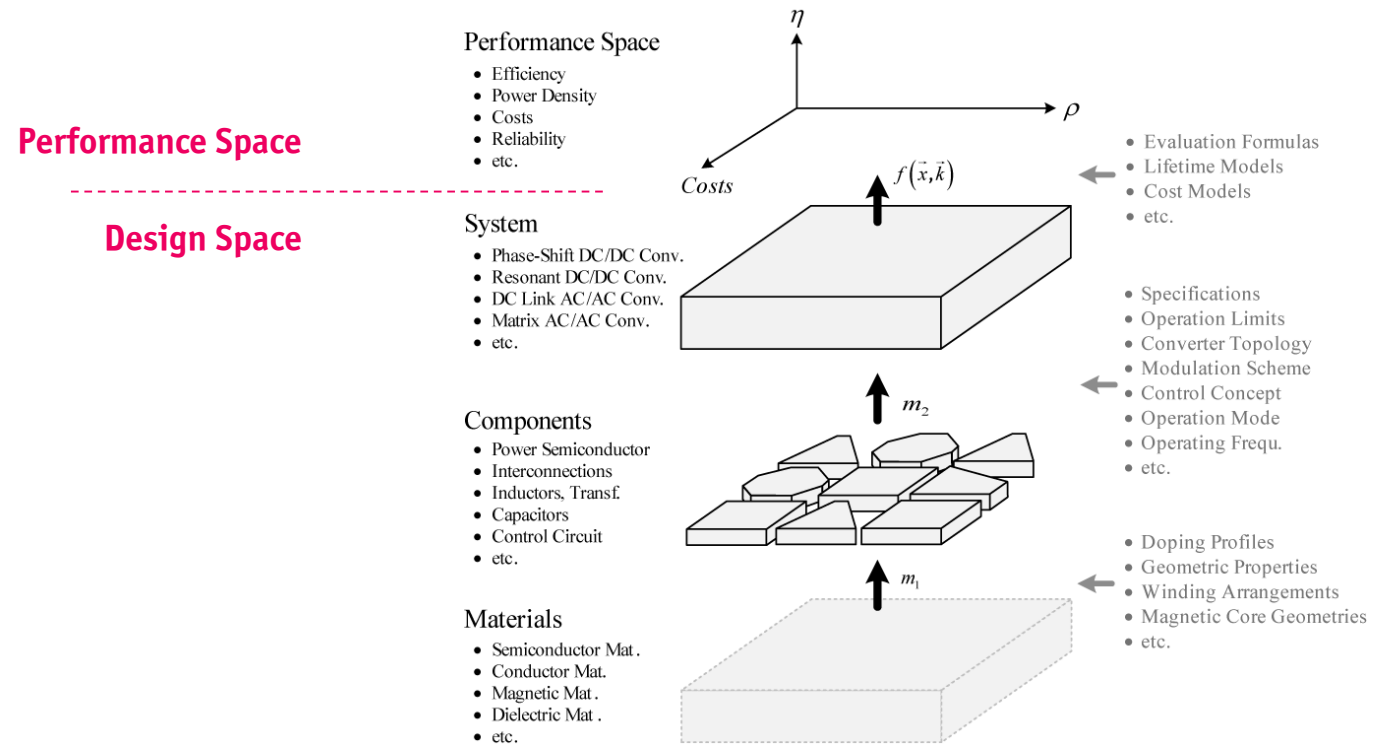


Source: Ostendorf & König / DeGruyter



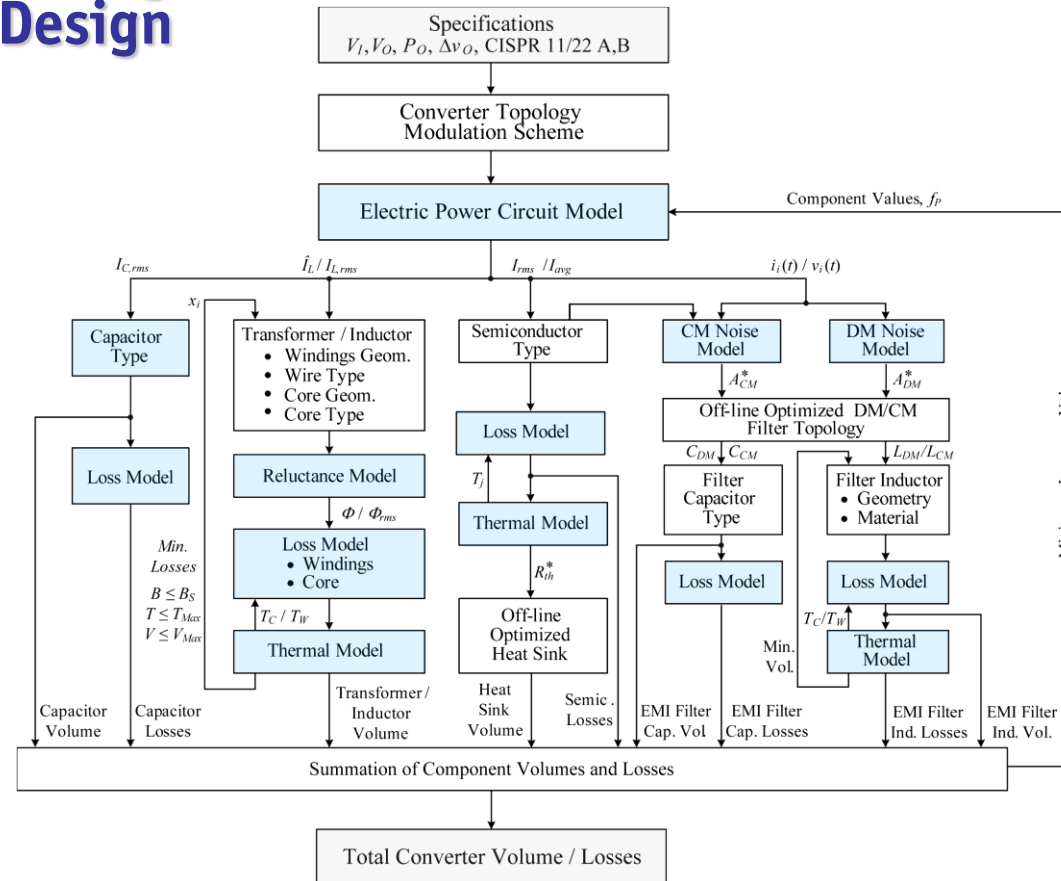
- Distributed Intelligence
- Fully Digital Control of Complex Systems – Electrical/Optical/Wireless Signal Transfer
- Massive Comp. Power → Fully Automated AI-Supported Design / Digital Twins / Industrial IoT (IIoT)

Abstraction of Power Converter Design



- Mapping of **Design Space** into Converter **" η - ρ - σ -Performance Space"**
- **Design Space** — Set of Selected Design- & Operating Parameters, Materials, Components, Topology, etc.

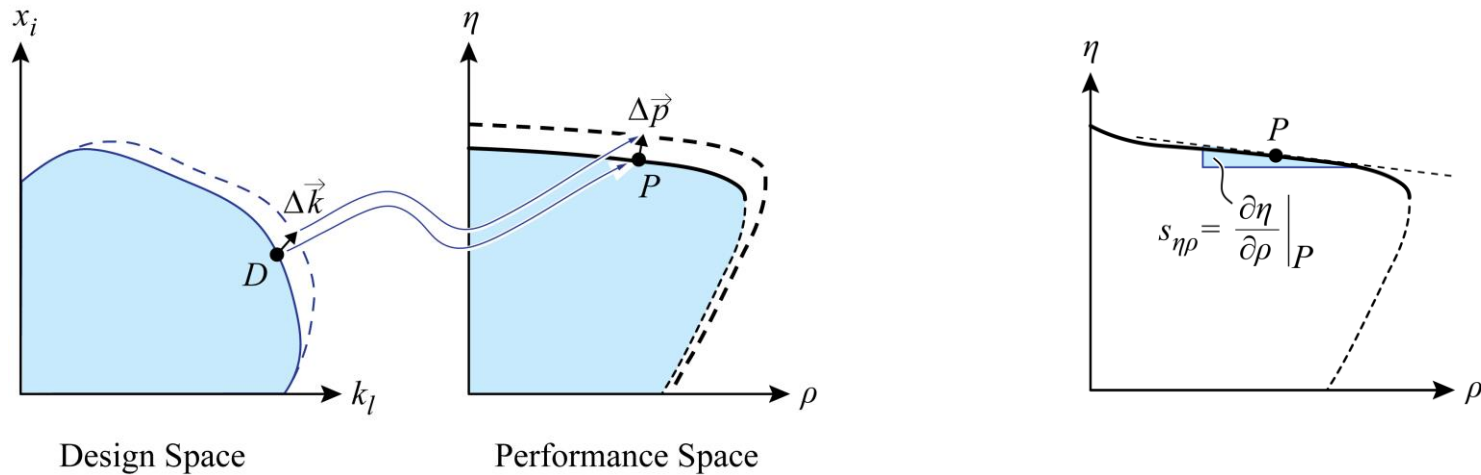
Mathematical Modeling of the Converter Design



- *Best Utilization of All Degrees of Freedom* → *Multi-Objective Optimization*

Multi-Objective Optimization

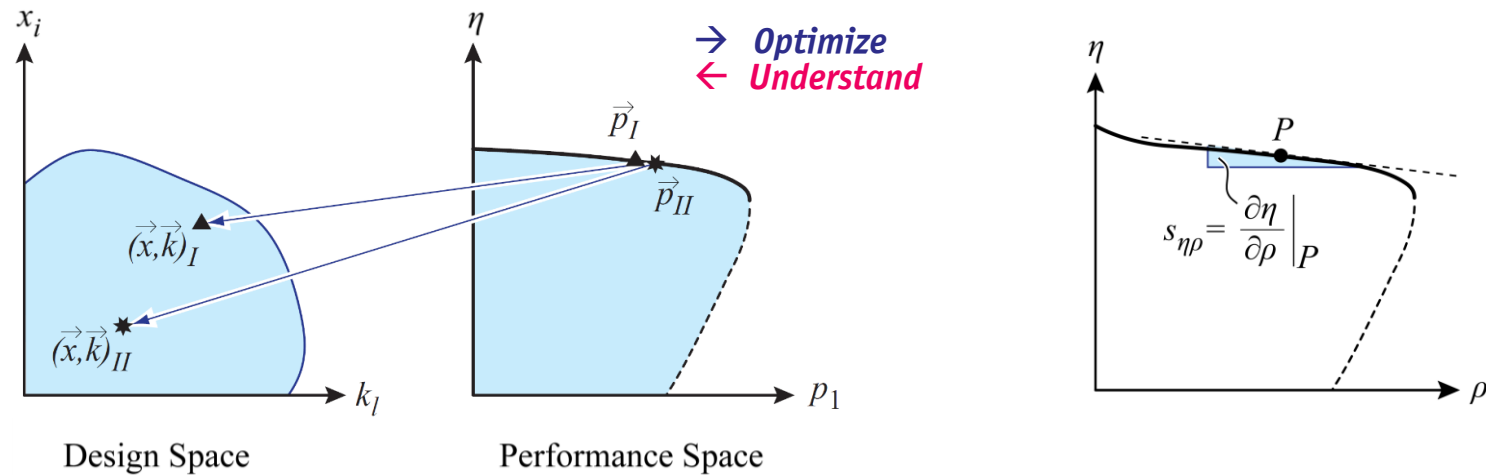
- Based on Mathematical Model of the Technology Mapping
- Multi-Objective Optimization → Best Utilization of the "Design Space"
- Identifies Absolute Performance Limits → Pareto Front / Surface



- Clarifies Sensitivity $\Delta \vec{p} / \Delta \vec{k}$ to Improvements of Technologies
- Trade-Off Analysis

Design Space Diversity

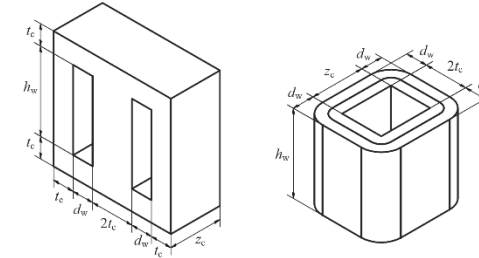
- **Equal Performance \vec{p}_i for Largely Different Sets $(\vec{x}, \vec{k})_i$ of Design Parameters**
- **E.g. Mutual Compensation of Volume or Loss Contributions (e.g. Cond. & Sw. Losses)**



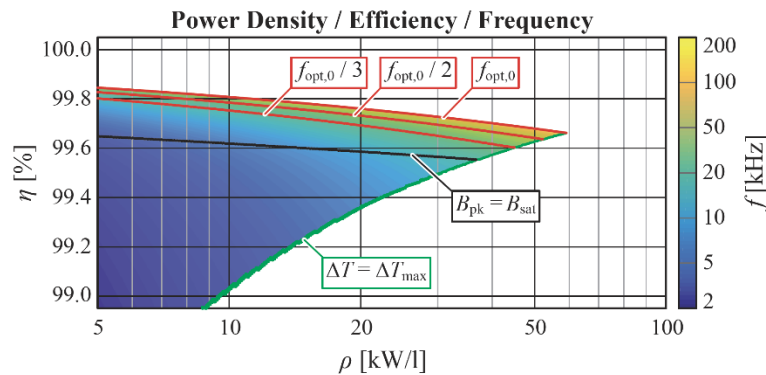
- **Allows Consideration of Additional Performance Targets (e.g. Costs)**

Design Space Diversity — Example

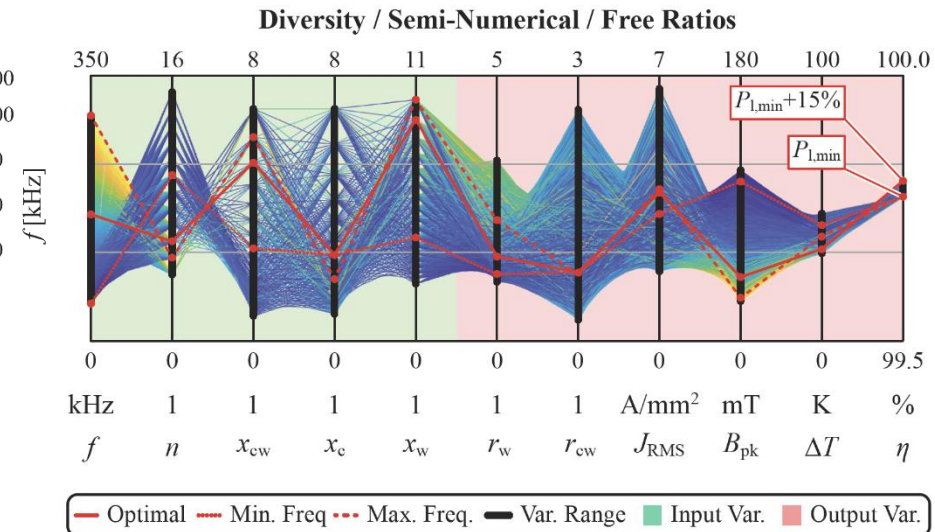
- *Design of a Medium-Frequency Transformer*
- *Power Level & Power Density = const.*
- *Wdg./Core Loss Ratio, Geometry, n etc. as Design Parameters*



Source: T. Guillod / ETH



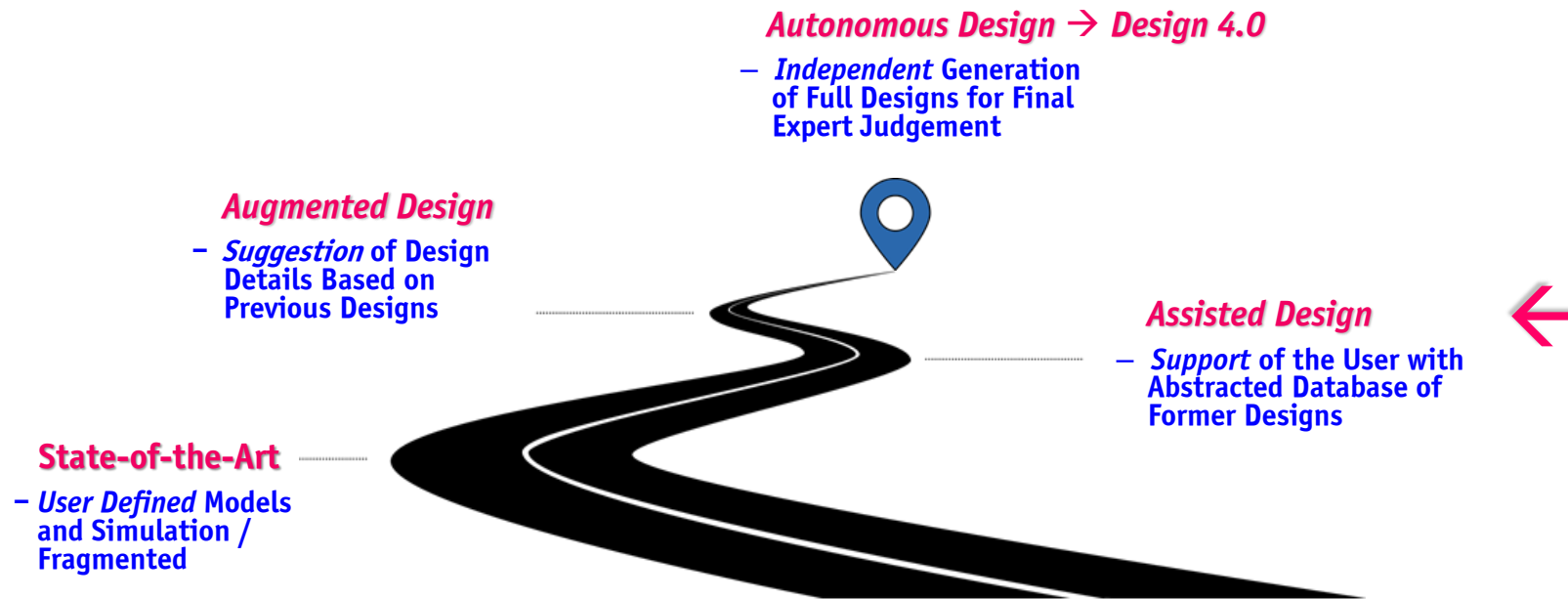
$$x_{cw} = A_c / A_w, \quad x_c = z_c / 2 t_c, \quad x_w = h_w / d_w$$



- *Mutual Compensation Core & Winding Losses Changes*
- *Limits on Part Load Efficiency / Costs / Fixed Geometry → Restricted Diversity*

Design Automation Roadmap

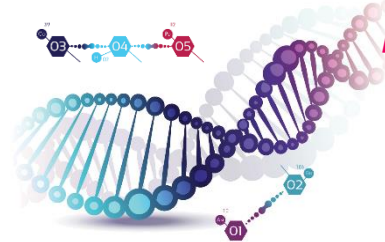
- *End-to-End Horizon* — *Cradle-to-Grave/Cradle* — *Modeling & Simulation*
- *Design for Cost / Volume / Efficiency* / *Manufacturing* / *Testing* / *Reliability* / *Recycling*



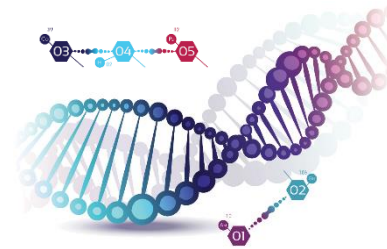
- *AI-Based Summaries* → *No Other Way to Survive* in a World of Exp. Increasing # of Publications (!)

X-Concepts

***Modularization
Functional Integration
Synergetic Association
Hybridization
Decentralization***



X-Concept



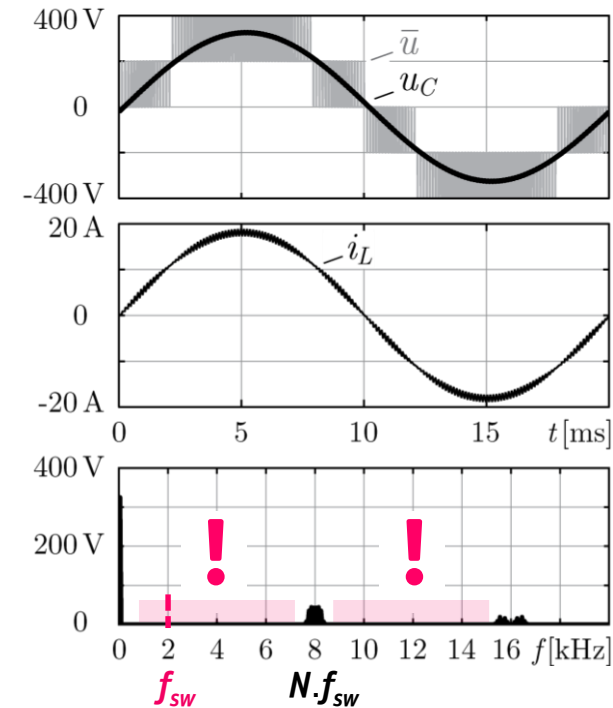
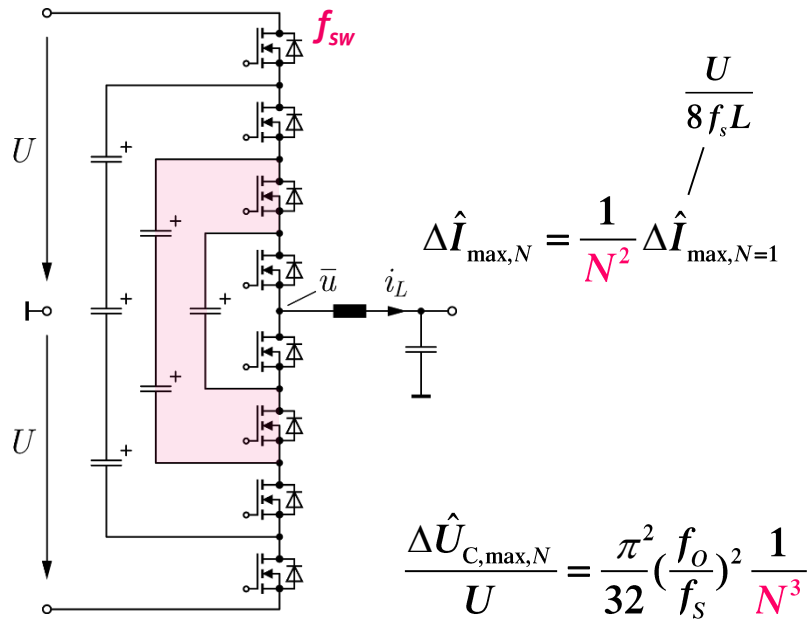
Modularization

Scaling of Multi-Cell/Level Concepts

- **Reduced Ripple @ Same (!) Switching Losses**
- **Lower Overall On-Resistance @ Given Blocking Voltage**
- **Application of LV Technology to HV**



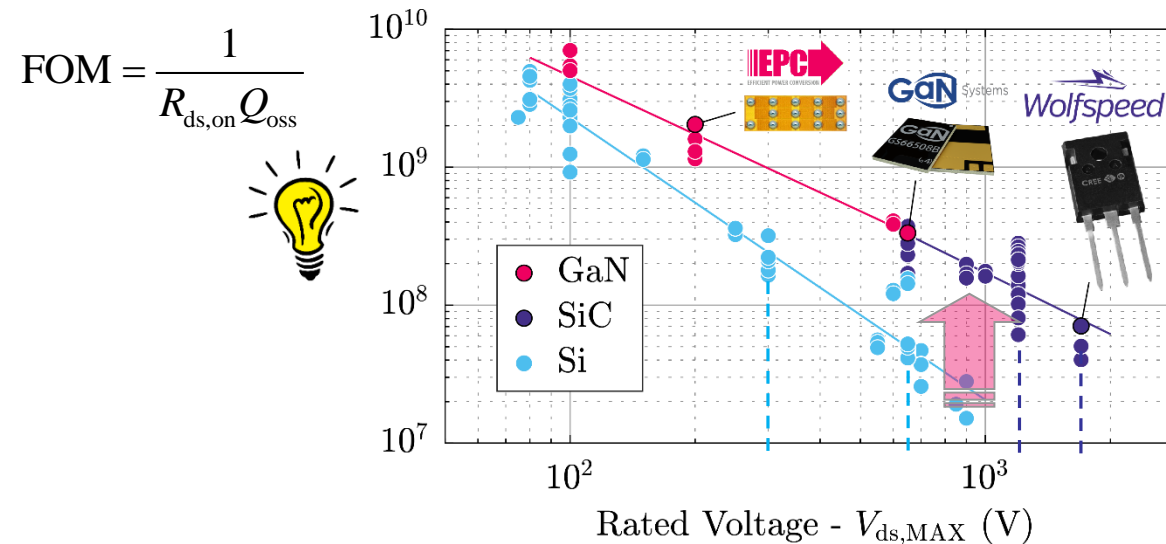
Source: R. Pilawa
Integrated Dual-Sided
Half-Bridge Flying
Capacitor Converter
Switching Cell



- **Scalability / Manufacturability / Standardization / Redundancy**

SiC/GaN Figure-of-Merit

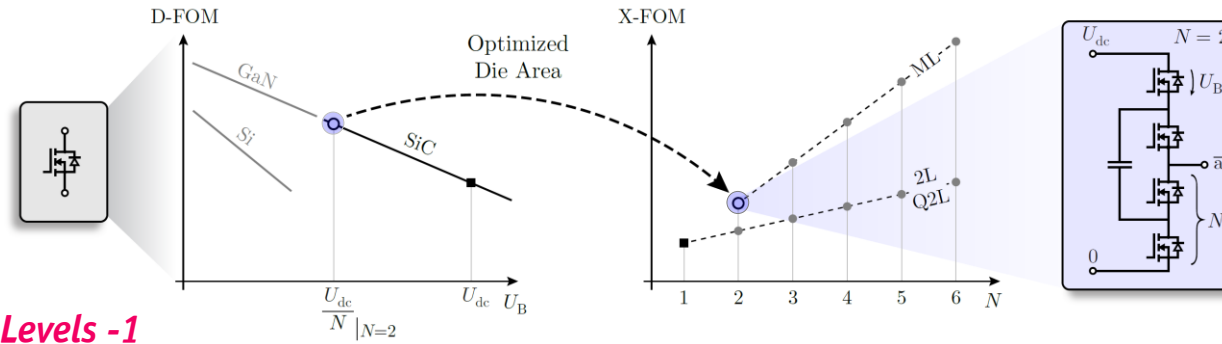
- *Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties*
- *FOM Determines Max. Achievable Efficiency @ Given Sw. Frequ.*



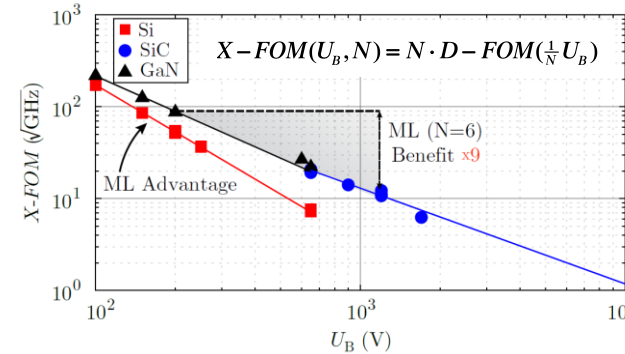
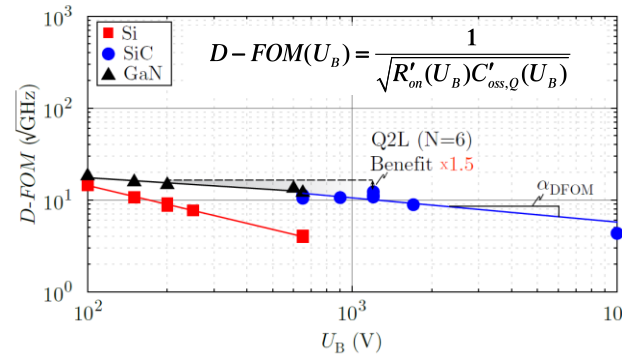
- *Advantage of Multi-Level over 2-Level Converter Topologies*

X-FOM of ML-Bridge-Legs

- Quantifies Bridge-Leg Performance of N-Level FC Converters
- Determines Max. Achievable Efficiency & Loss Opt. Chip Area @ Given Sw. Frequ.



$N = \# \text{ of Levels} - 1$



- Compared to 2-Level Benchmark @ Same Filter Ind. Volt-Seconds

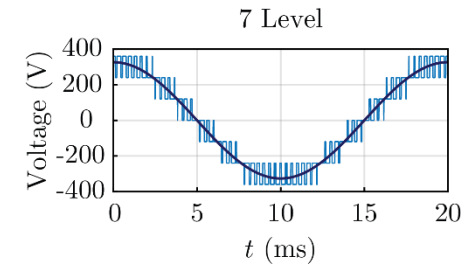
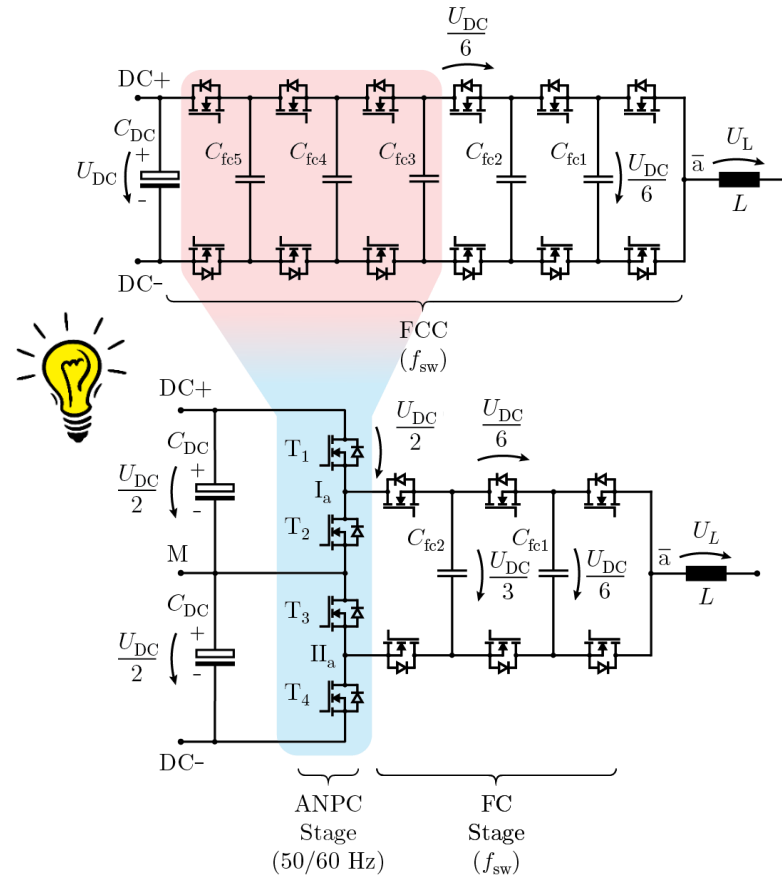


$$\begin{aligned} P_{\text{semi,min,ML}} &\approx \frac{1}{N^{1.2}} P_{\text{semi,min,2L}} \\ A_{\text{chip,ML}} &\approx N^{1.2} A_{\text{chip,2L}} \end{aligned}$$



3-Φ Hybrid Multi-Level Inverter

- Realization of a **99%++ Efficient 10kW 3-Φ 400V_{rms,LL} Inverter System**
- **7-Level Hybrid Active NPC Topology / LV Si-Technology**



★ **99.35%**
2.6kW/kg
56 W/in³



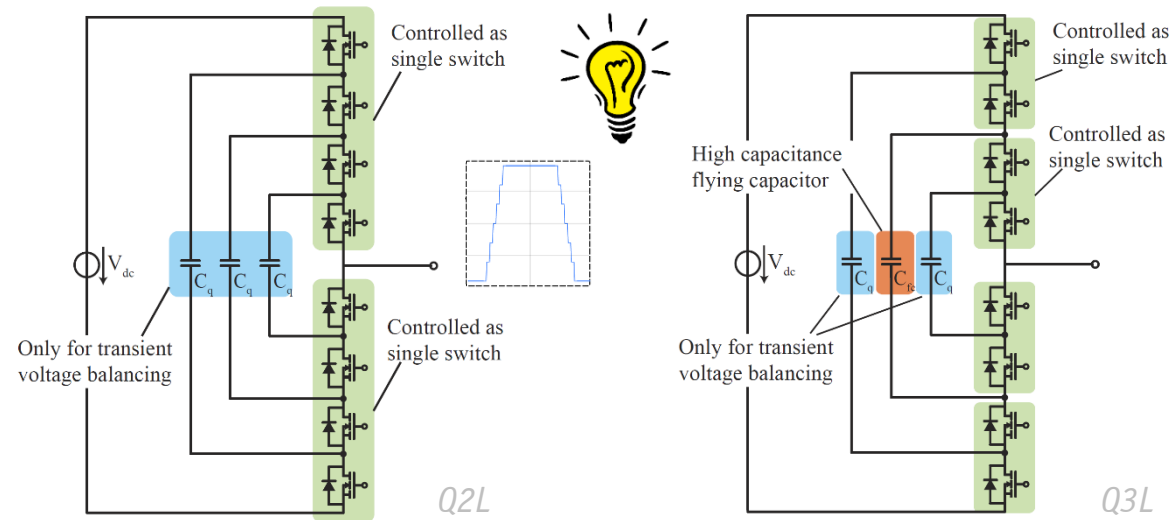
- **200V Si → 200V GaN Technology Results in 99.5% Efficiency**

Quasi-2L & Quasi-3L Inverters

- **Operation of N-Level Topology in 2-Level or 3-Level Mode**
- **Intermediate Voltage Levels Only Used During Sw. Transients**

Source: M. Schweizer

ABB



- **Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors**
- **Low Voltage/Low $R_{DS(on)}$ /Low \$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages**

Quasi-2L & Quasi-3L Inverters

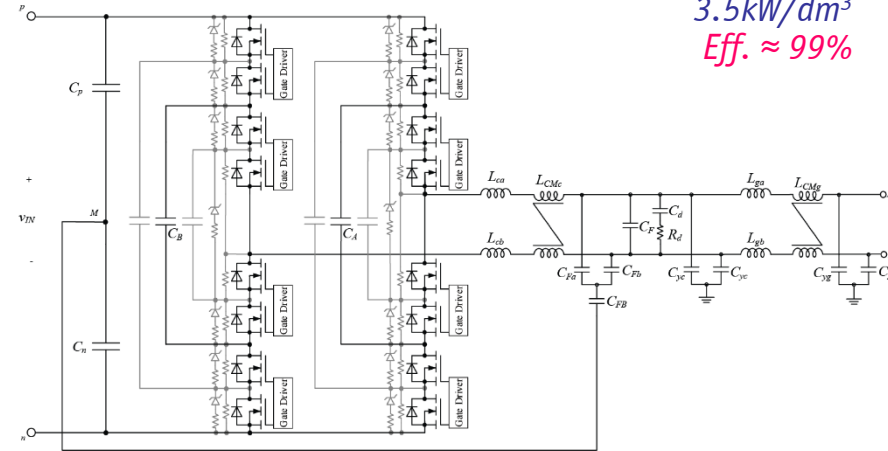
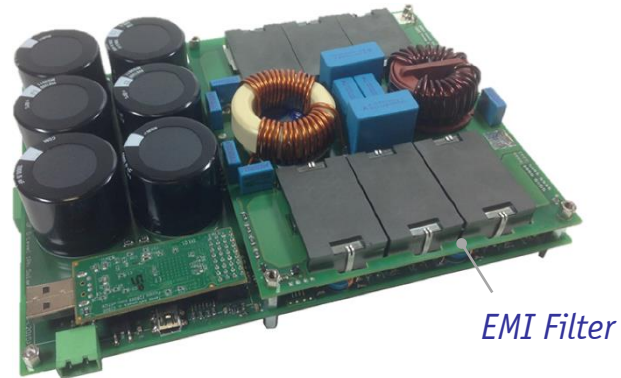
- *Operation of 5L Bridge-Leg Topology in Quasi-3L Mode*
- *Intermediate Voltage Levels Only Used During Sw. Transients*
- *Applicability to All Types of Multi-Level Converters*

Source: M. Schweizer

ABID

3.3kW @ 230V_{rms}/50Hz
Equiv. $f_s = 48\text{kHz}$

3.5kW/dm³
Eff. \approx 99%



- Reduced Average $dv/dt \rightarrow$ **Lower EMI**
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- **Low Voltage/Low $R_{DS(on)}$ /Low \$ MOSFETs \rightarrow High Efficiency / No Heatsinks / SMD Packages**

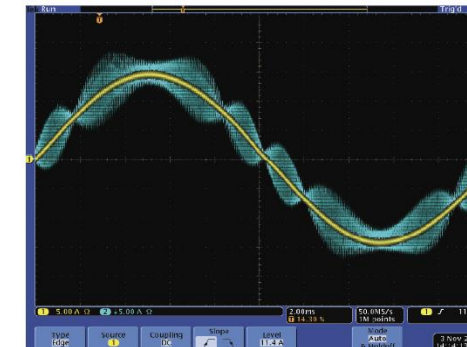
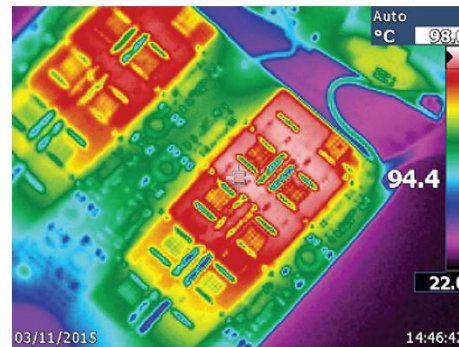
Quasi-2L & Quasi-3L Inverters

Source: M. Schweizer



- Operation of 5L Bridge-Leg Topology in *Quasi-3L Mode*
- *Intermediate Voltage Levels Only Used During Sw. Transients*
- Applicability to All Types of Multi-Level Converters

Operation @ 3.2kW



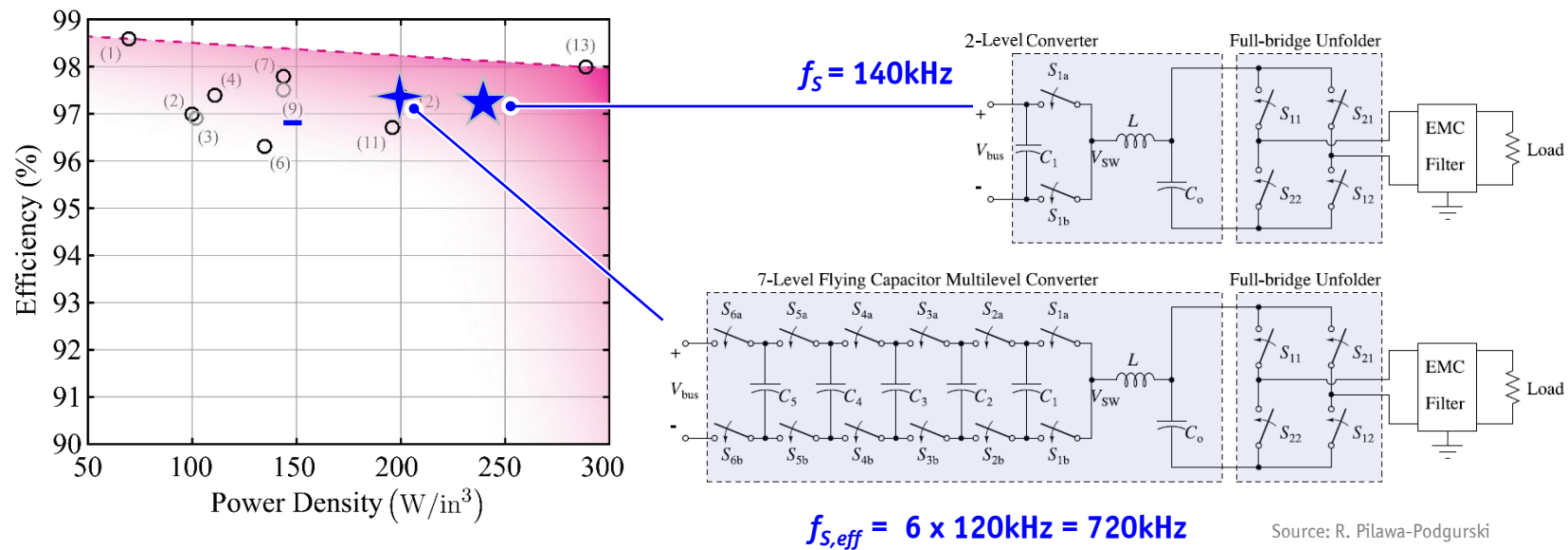
— Conv. Output Voltage
— Sw. Stage Output Voltage
— Flying Cap. (FC) Voltage
— Q-FC Voltage (Uncntrl.)

— Output Current
— Conv. Side Current

- Reduced Average $dv/dt \rightarrow$ **Lower EMI**
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$ /Low \$ MOSFETs \rightarrow High Efficiency / No Heatsinks / SMD Packages

Remark 2-Level vs. Multi-Level Inverter

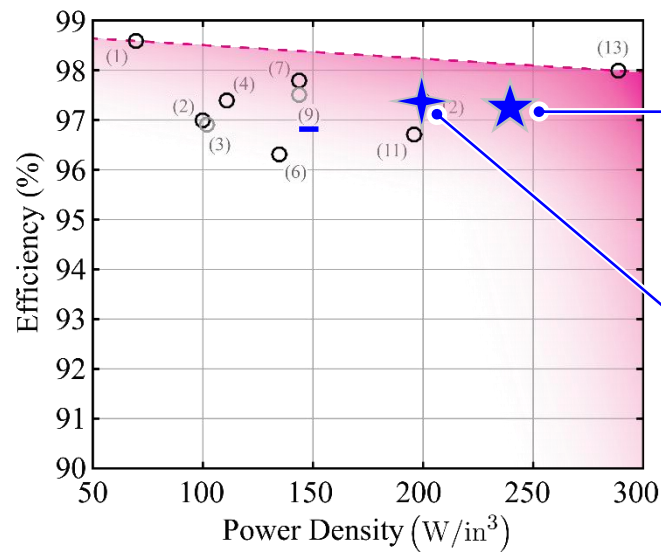
- Example of Google Little Box Challenge
- Target: 2kW 1- Φ Solar Inverter with Worldwide Highest Power Density
- Comparative Analysis of Approaches of the Finalists



- 3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)

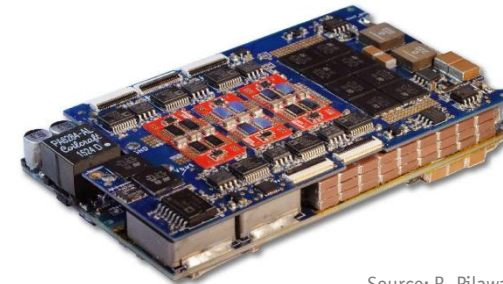
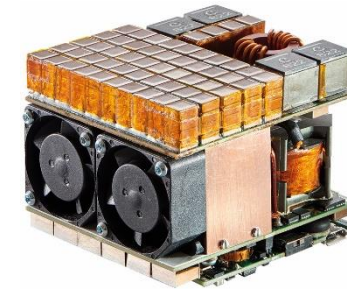
Remark 2-Level vs. Multi-Level Inverter

- **Example of Google Little Box Challenge**
- **Target: 2kW 1- Φ Solar Inverter with Worldwide Highest Power Density**
- **Comparative Analysis of Approaches of the Finalists**



ETH zürich
Little-Box 2.0
240 W/in^3
97.4%

ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN
215 W/in^3
97.6%



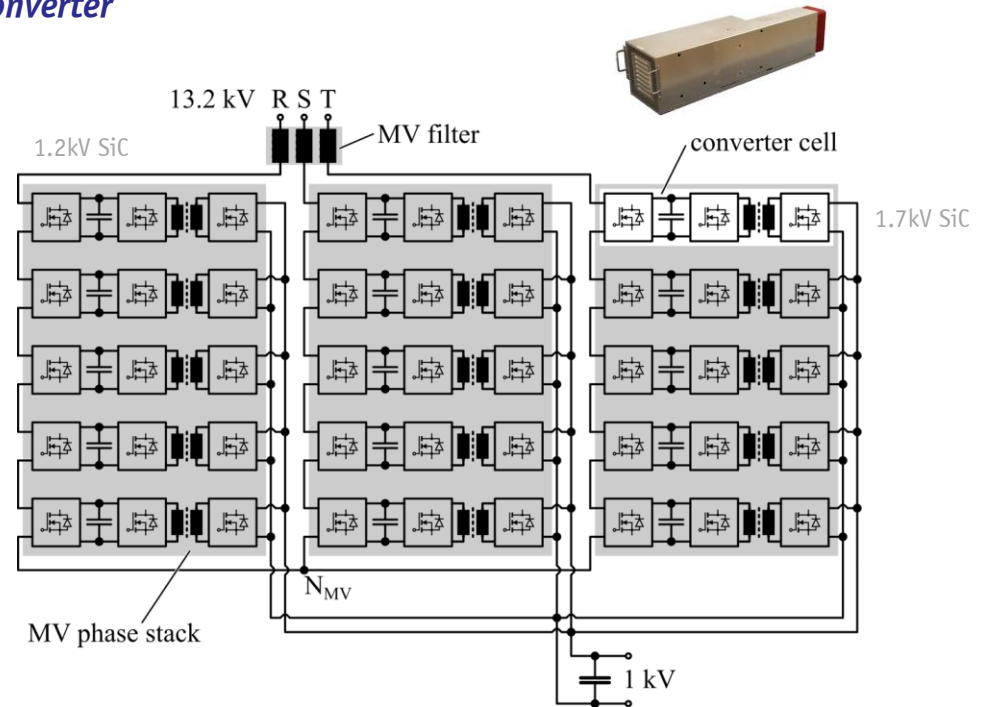
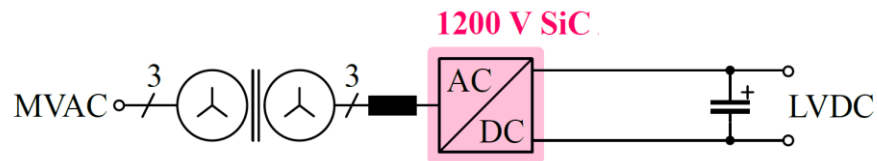
Source: R. Pilawa-Podgurski

- **3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)**

Remark

2-Level vs. Multi-Level Inverter

- **400kW Extreme Fast EV Charger** | **3- Φ 13.2kV AC \rightarrow 1kV DC**
- **Input Series Output Parallel (ISOP) Solid-State Transformer**
- **Alternative Low-Frequency Transformer & AC/DC Converter**

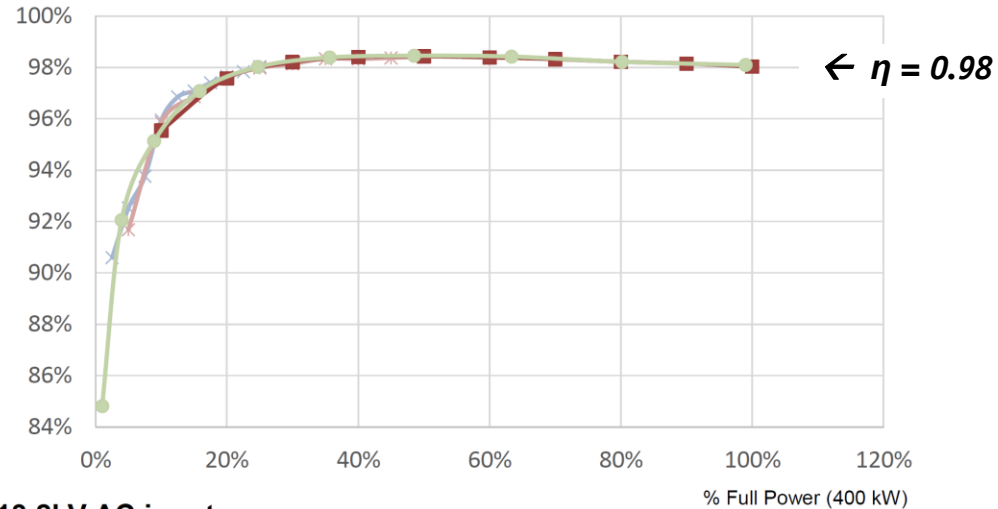


- **1.2kV SiC MOSFETs Utilized in Both Systems**
- **3 x 9 = 27 AC/DC—DC/DC Cells / 3-Level PFC Input Stage & Full-Bridge DC/DC Output Stage**

Remark

2-Level vs. Multi-Level Inverter

- **400kW Extreme Fast EV Charger** | **3- Φ 13.2kV AC \rightarrow 1kV DC**
- **Input Series Output Parallel (ISOP) Solid-State Transformer**



13.2kV AC input

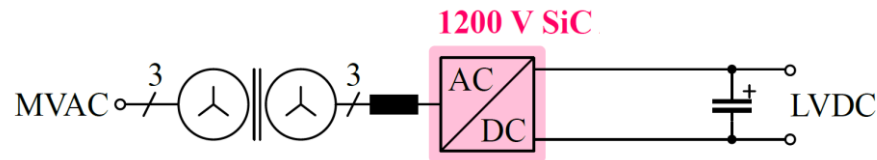
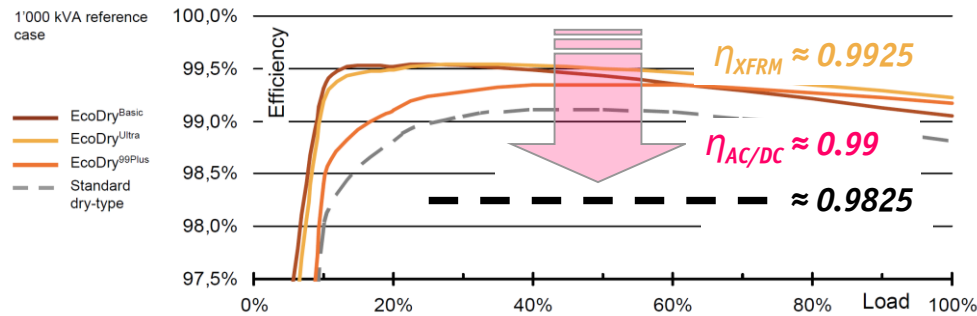


AC Input Cabinet | Converter Cabinets | Control Cabinet

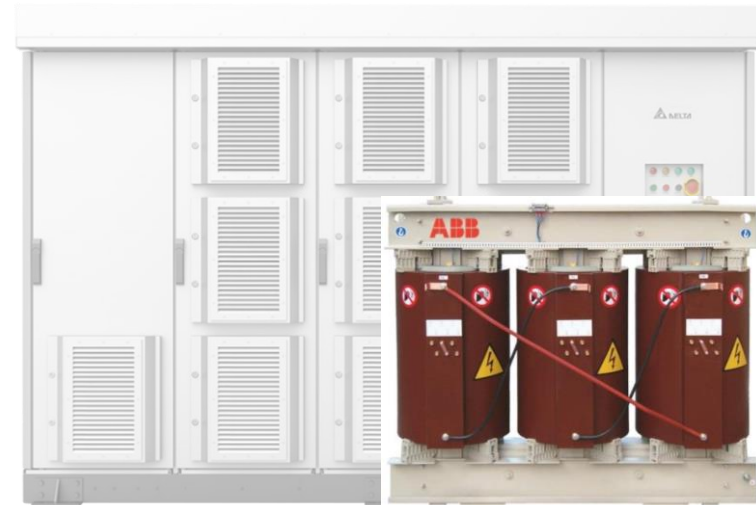
- **Forced Air Cooling**
- **3 x 9 = 27 AC/DC—DC/DC Cells**
- **98+ % Efficiency** | **3000kgs Weight** | **3100 x 1300 x 2100 mm Outer Dimensions**

Remark 2-Level vs. Multi-Level Inverter

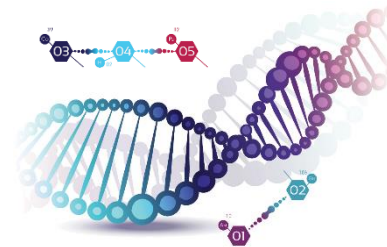
- **400kVA EcoDry™ High-Efficiency Transformer & AC/DC Converter**
- **Vacuum Cast Coils** → No Fire Hazard
- **Amorphous Metal Core** → Low No-Load Losses
- **High Overvoltage / Overload Capability**



- **400kVA** → 1400 x 750 x 1500 mm Outer Dimensions
- Utilizing SST SiC MOSFETs in AC/DC Stage → 99++ % Efficiency
- Higher Efficiency / Power Density / Robustness of LFT-Based Concept (!)



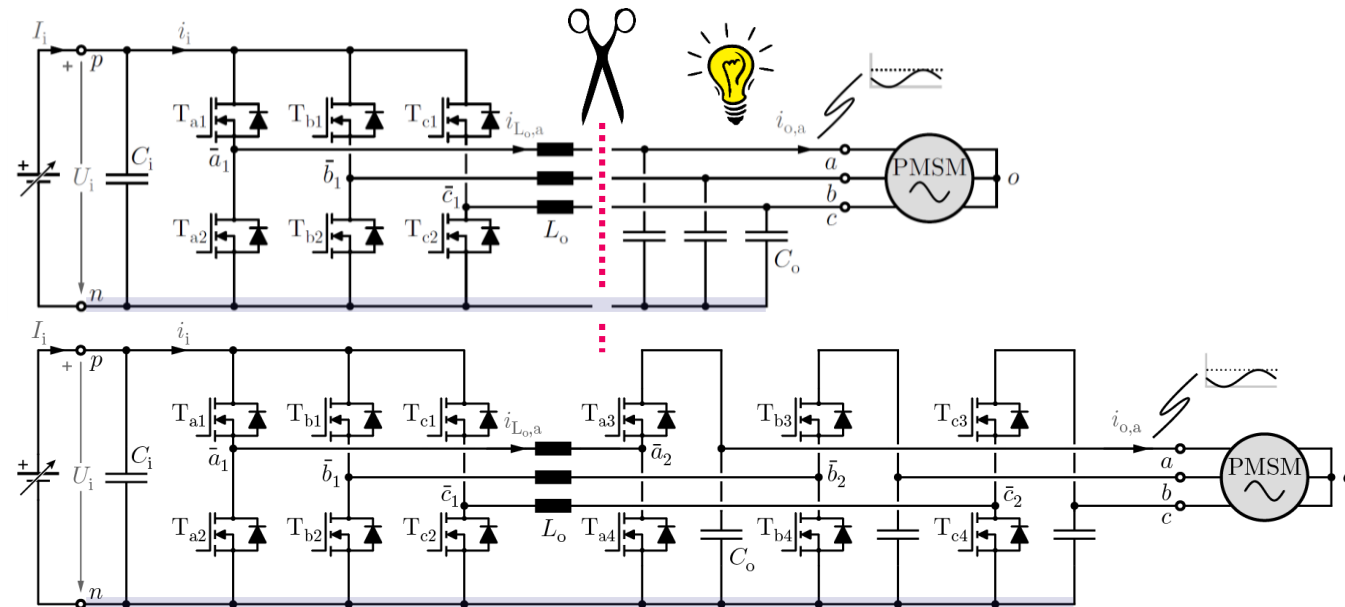
X-Concept



*Functional
Integration*

Buck-Boost 3- Φ Variable Speed Drive Inverter

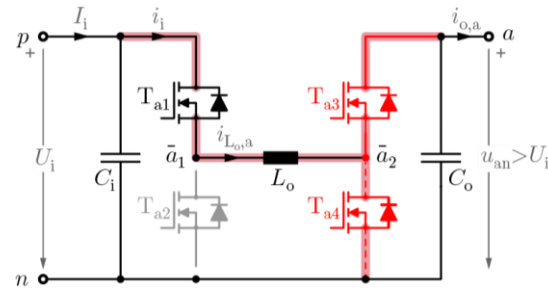
- Generation of **AC-Voltages** Using **Unipolar Bridge-Legs**
- Utilize **Filter Inductor** for Boost Operation \rightarrow **Functional Integration**



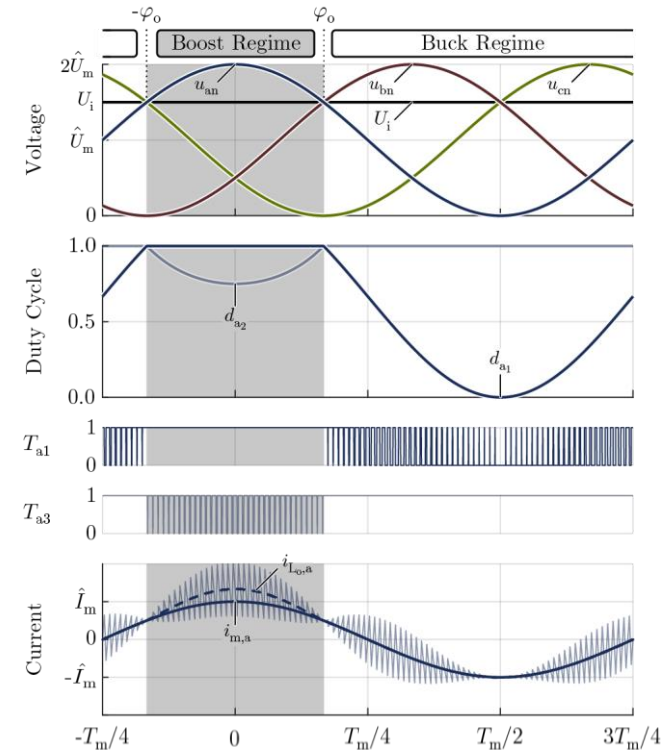
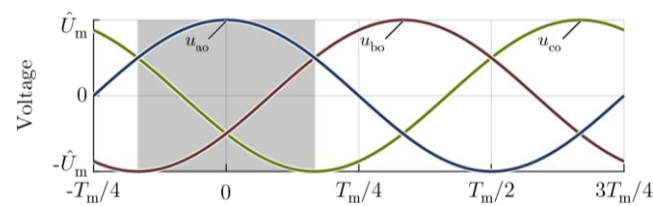
- **Switch-Mode Operation of Buck OR Boost Stage** \rightarrow **Single-Stage Energy Conversion (!)**
- **3- Φ Continuous Sinusoidal Output / Low EMI** \rightarrow **No Shielded Cables / No Motor Insul. Stress**

Boost-Operation $u_{an} > U_i$

■ Phase-Module



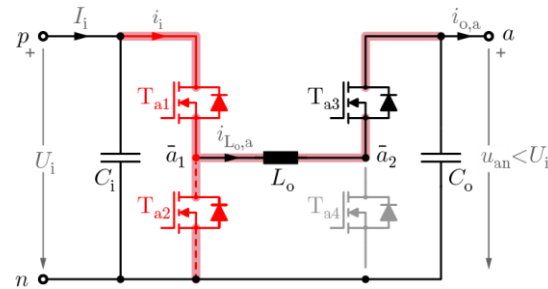
■ Motor Phase Voltages



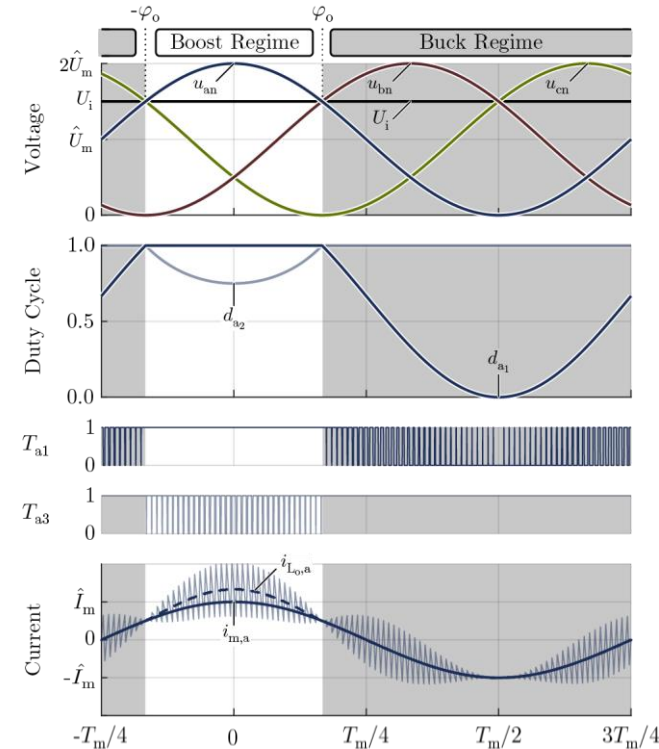
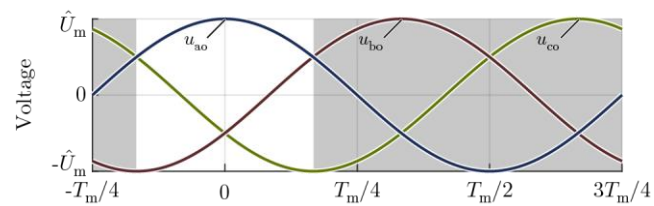
- **Current-Source-Type Operation**
- **Clamping of Buck-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion**

Buck-Operation $u_{an} < U_i$

■ Phase-Module



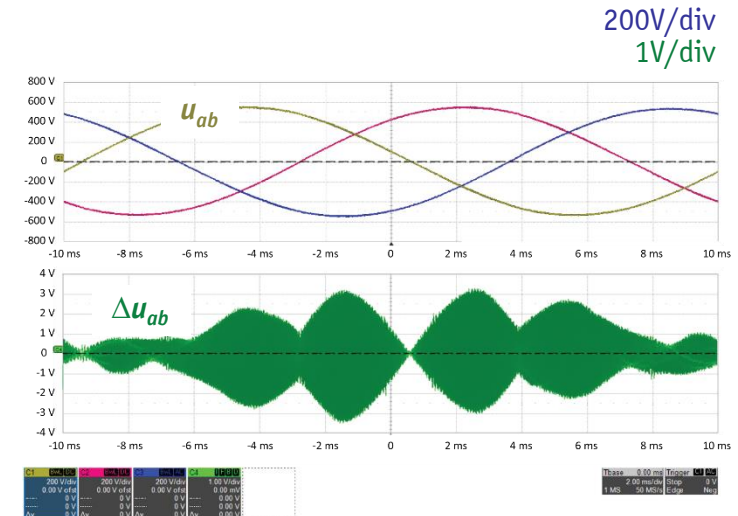
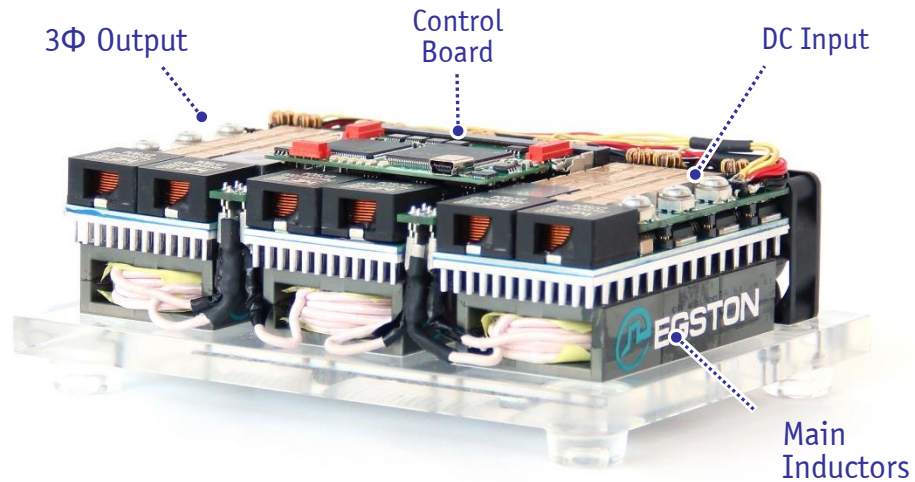
■ Motor Phase Voltages



- **Voltage-Source-Type Operation**
- **Clamping of Boost-Bridge High-Side Switch** → **Quasi Single-Stage Energy Conversion**

SiC 3- Φ Buck-Boost Inverter Demonstrator

- DC Voltage Range $400 \dots 750 V_{DC}$
- Max. Input Current $\pm 15 A$
- Output Voltage $0 \dots 230 V_{rms}$ (Phase)
- Output Frequency $0 \dots 500 Hz$
- Sw. Frequency $100 kHz$



■ **Dimensions** $\rightarrow 160 \times 110 \times 42 \text{ mm}^3$

★ $\approx 245 \text{ W/in}^3$

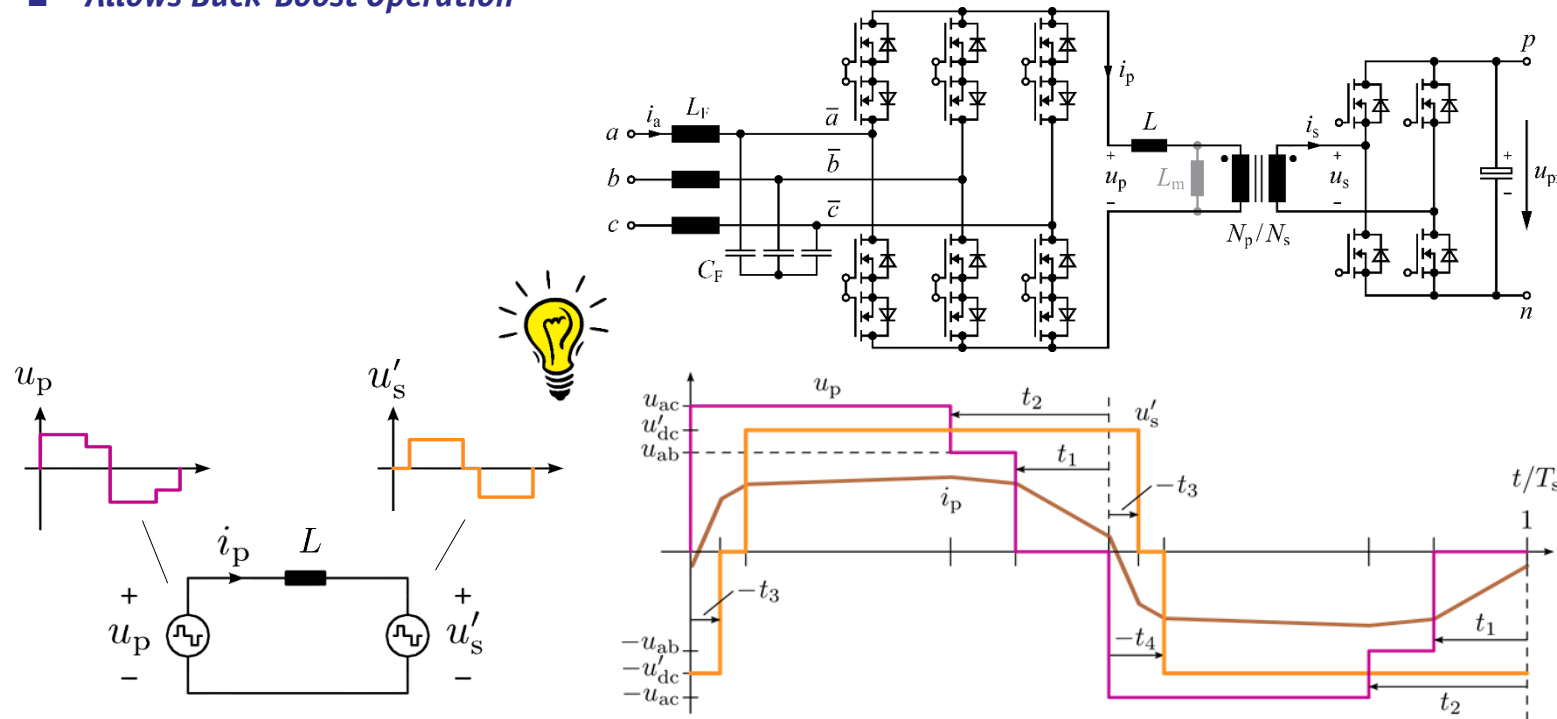


Lighthouse
Project



Isolated Matrix-Type 3- Φ PFC Rectifier

- Based on Dual Active Bridge (DAB) Concept
- Integration of 3- Φ PFC Rectifier & DC/DC Converter Stage
- Opt. Modulation ($t_1 \dots t_4$) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation



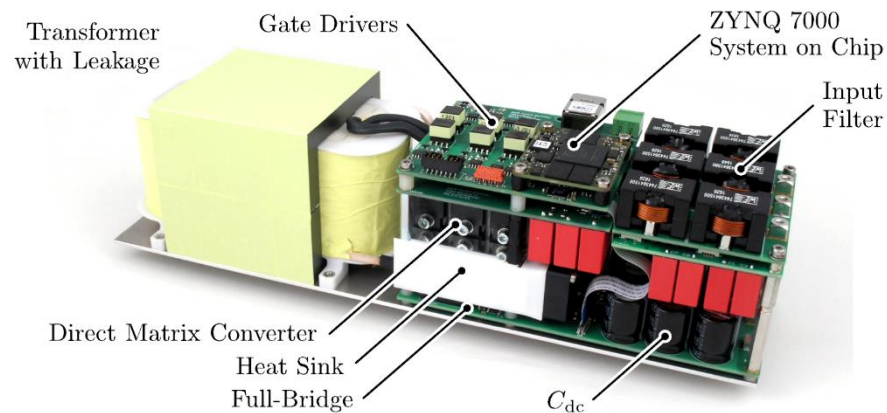
• Equivalent Circuit

• Transformer Voltages / Currents

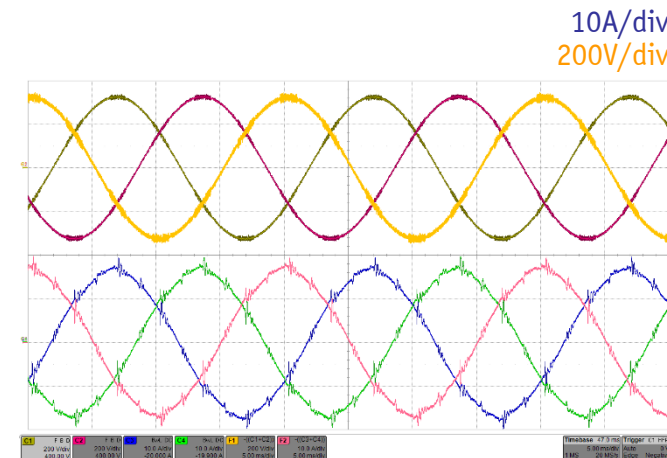
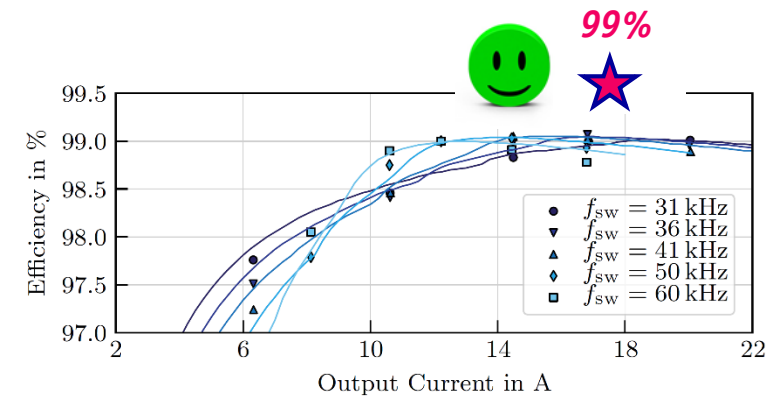
Isolated Matrix-Type 3-Φ PFC Rectifier

- Efficiency $\eta = 99\%$ @ 60% Rated Load (ZVS)
- Mains Current $THD_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4\text{kW}/\text{dm}^3$

$$\begin{aligned} P_o &= 8 \text{ kW} \\ U_N &= 400\text{V}_{\text{AC}} \rightarrow U_o = 400\text{V}_{\text{DC}} \\ f_s &= 36\text{kHz} \end{aligned}$$

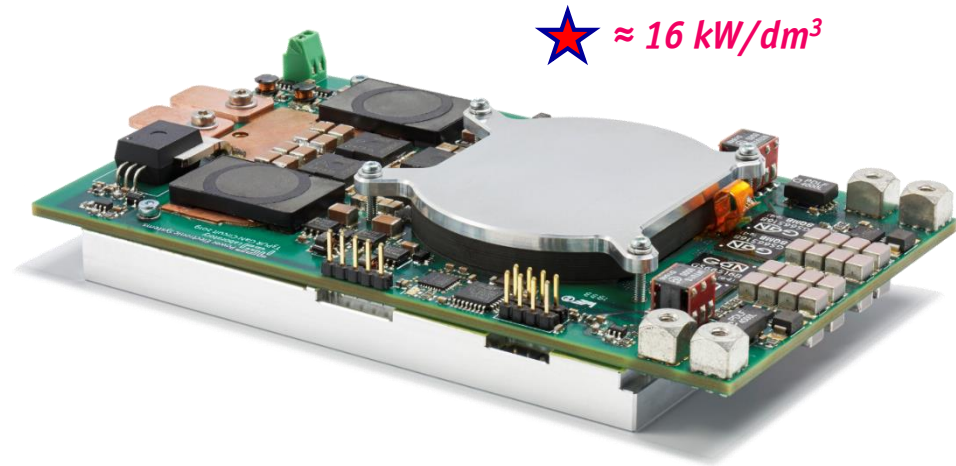
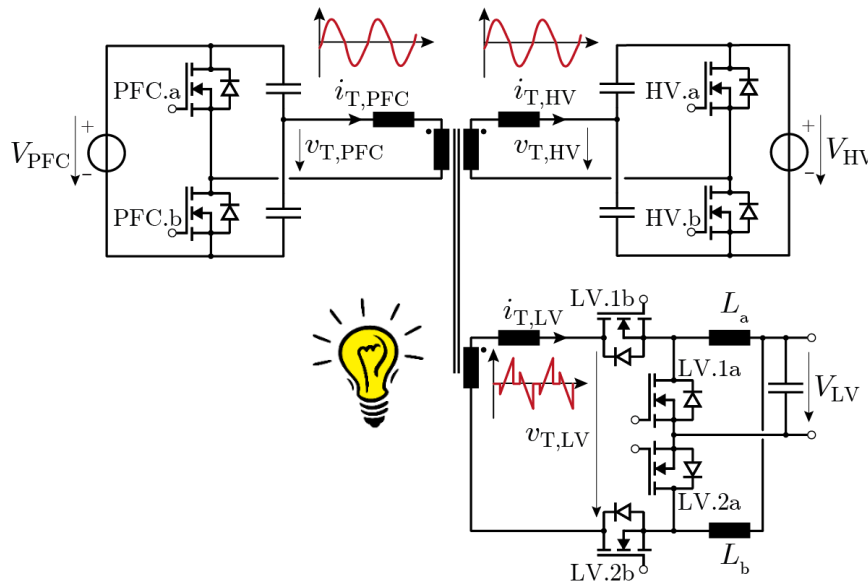


- 900V / 10mΩ SiC Power MOSFETs
- Opt. Modulation Based on 3D Look-Up Table



3-Port Resonant GaN DC/DC Converter

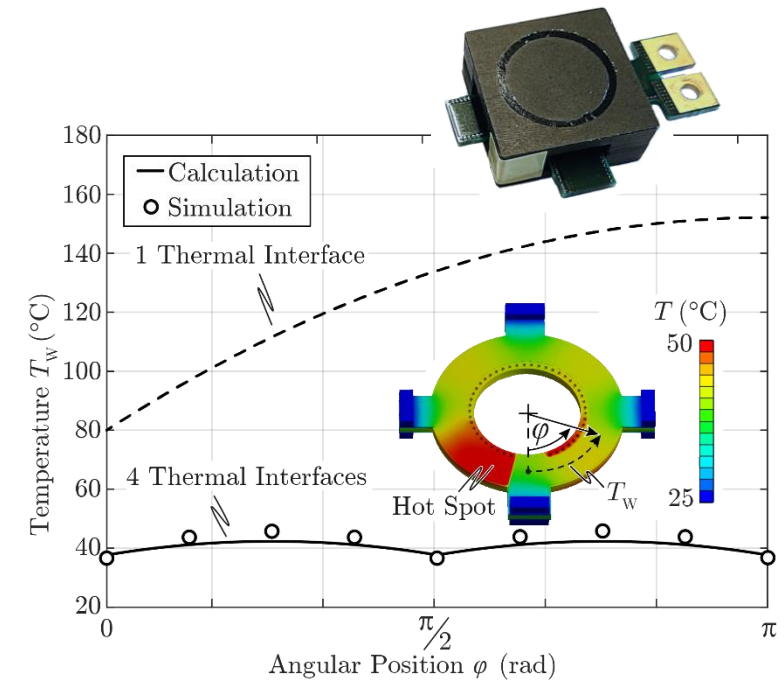
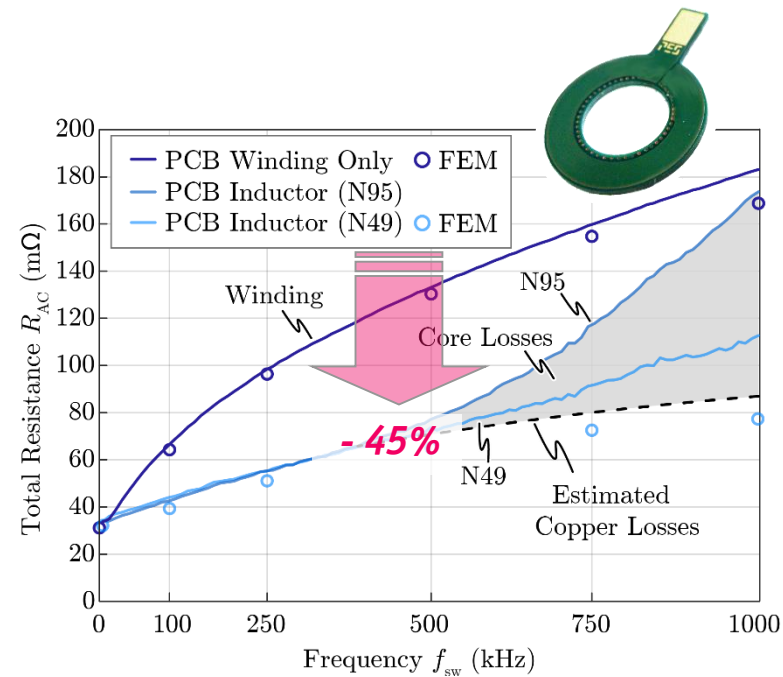
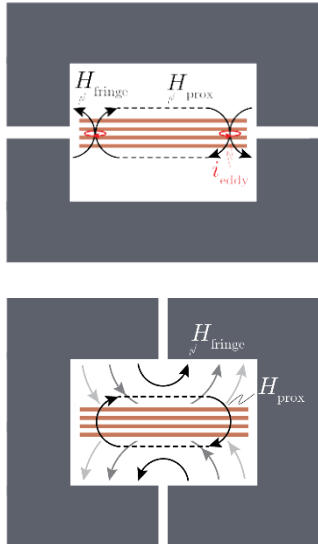
- **Single Transformer & Decoupled Power Flow Control**
- **Charge Mode PFC** \rightarrow HV (250...500V) SRC DCX / **Const. f_{sw}** , Min. Series Inductance / ZVS
- **Drive Mode** HV \rightarrow LV (10.5...15V) 2 Interleaved Buck-Converters / **Var. f_{sw}** / ZVS
- **$P = 3.6\text{kW}$**



- **Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode**
- **PCB-Based Windings / No Litz Wire Windings \rightarrow Fully Automated Manufacturing**

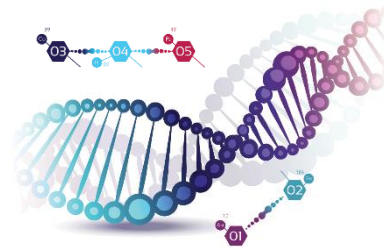
Low-Loss PCB-Winding Inductor

- *Conv. PCB Windings & Airgaps* → *Skin / Proximity / Fringing Field* ⊥ *to PCB* → *Current Displacement*
- *Arrangement of Airgaps for Mutual Field Compensation*
- *Thermal Interfaces for Efficient Cooling*



- *Optimal Positions & Wdg Distance of Airgaps for Multi-Airgap / Multi-Layer Inductors*
- *Factor of 3 Red. of Skin & Prox. Losses*

X-Concept



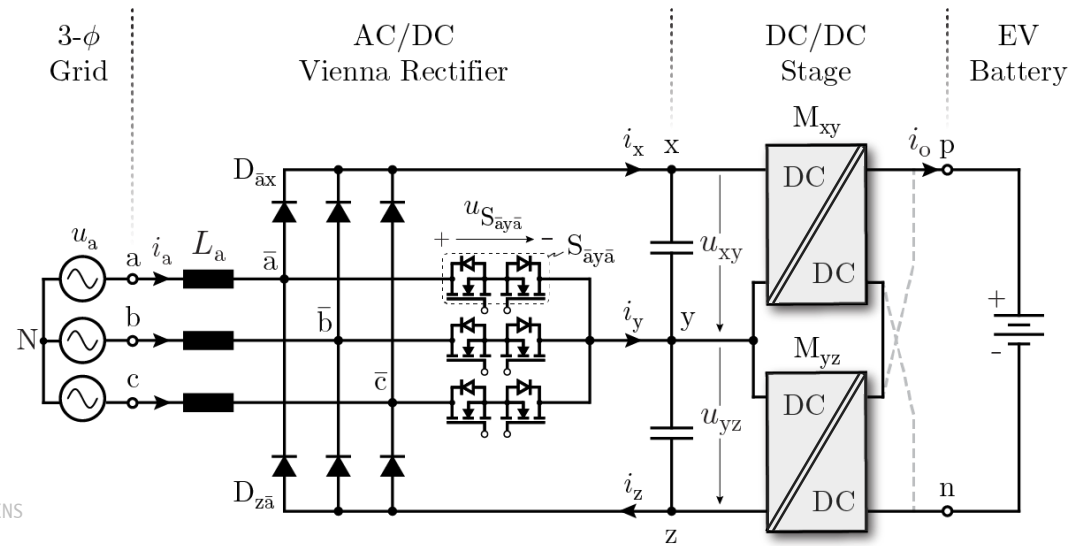
*Synergetic
Association*

3- Φ EV-Charger Topology

- **Isolated** Controlled Output Voltage
- **Buck-Boost** Functionality & Sinusoidal Input Current
- Applicability of **600V GaN Semiconductor Technology**
- **High Power Density / Low Costs**



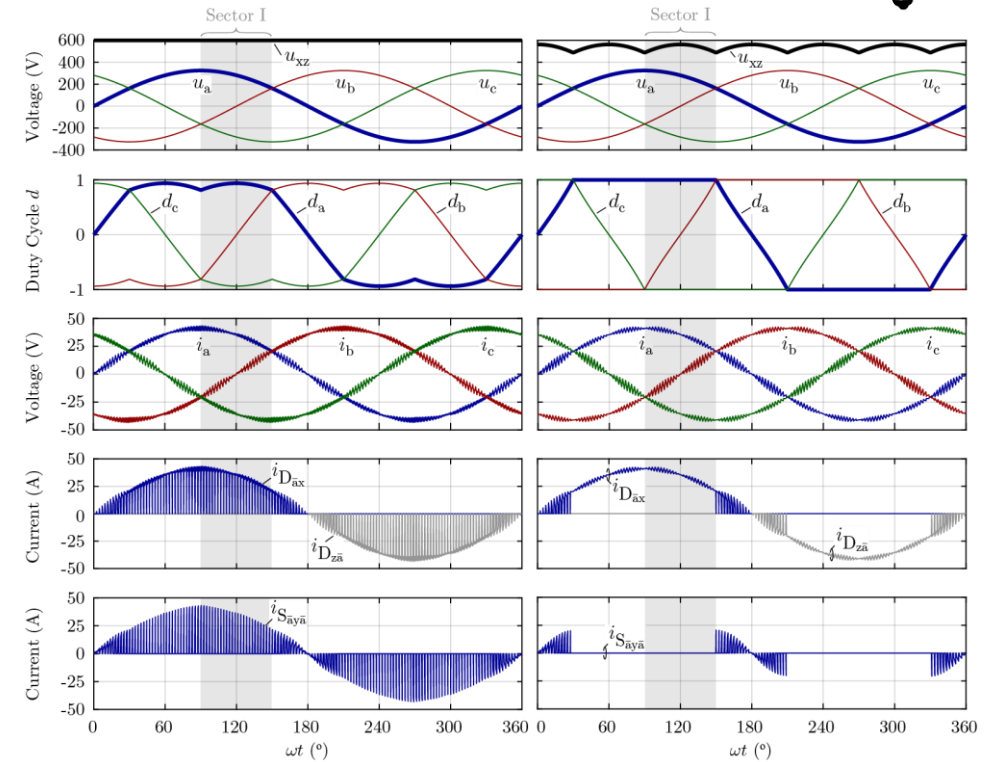
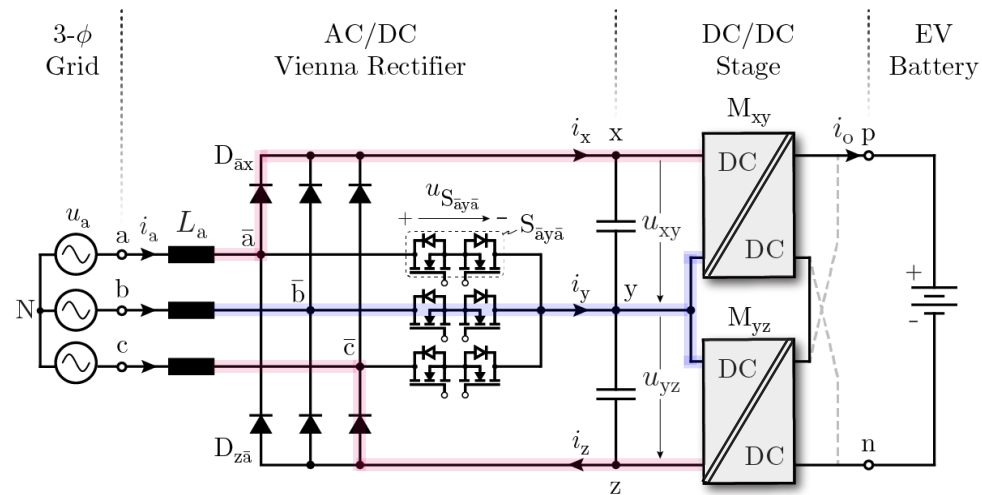
Source: SIEMENS



→ Conventional / Independent OR "Synergetic Control" of Input & Output Stage

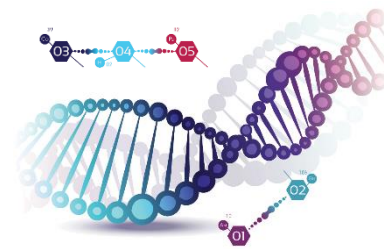
Synergetic Association

- **1/3-Modulation** → **Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM**
- **Conduction Losses of the Switches $\approx -80\%$**
- **Switching Losses $\approx -70\%$**



- **Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses**

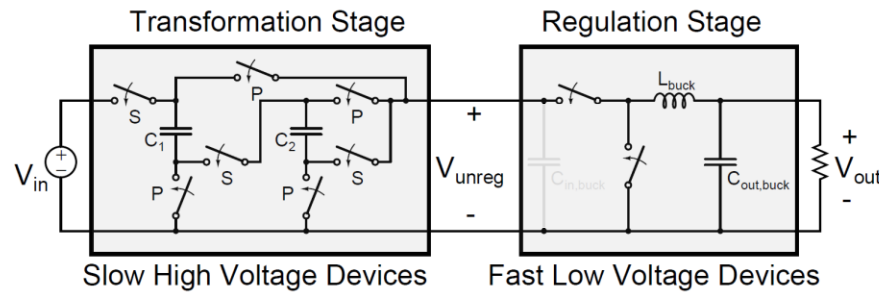
X-Concept



Hybridization

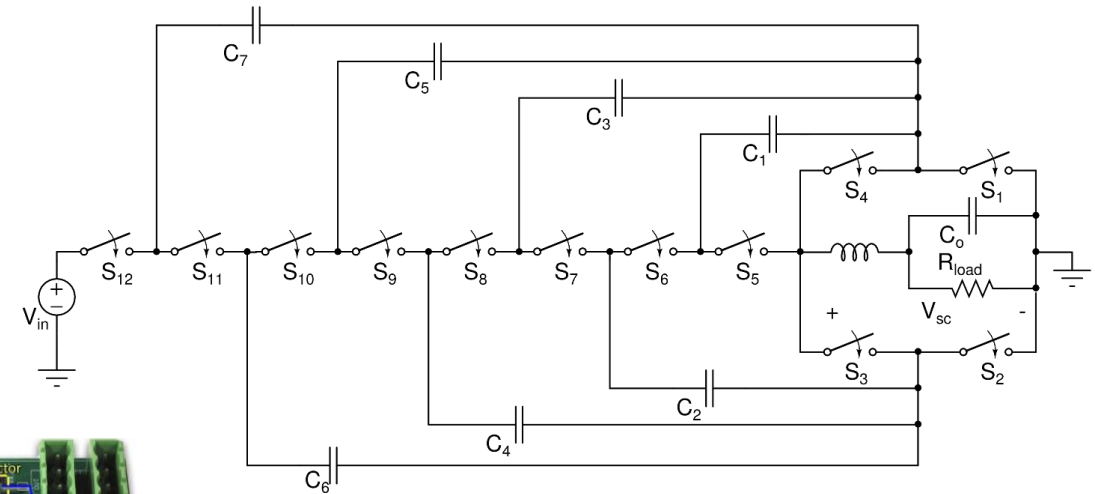
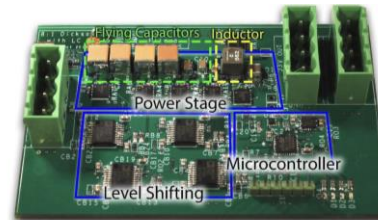
Hybrid Switched-Capacitor Converters (SCC)

- **High Step-Down Ratio SCC / Voltage Adaption & High-Frequency Magnetic-Based Post-Regulation**
- **Current-Impressing Converter/Load → “Soft-Charging” / No Charging Curr. Spikes / High Efficiency**
- **High Energy Density of Caps. vs. Inductors → High Power Density / Suitable for Integration**



★ $\approx 16 \text{ kW/dm}^3$

$U_{in} = 200\text{V}$
 $U_{out} = 25\text{V}$
 $I_{out} = 3\text{A}$
 $f_{Sw} = 250\text{kHz}$
 $\eta_{max} = 95.5\%$

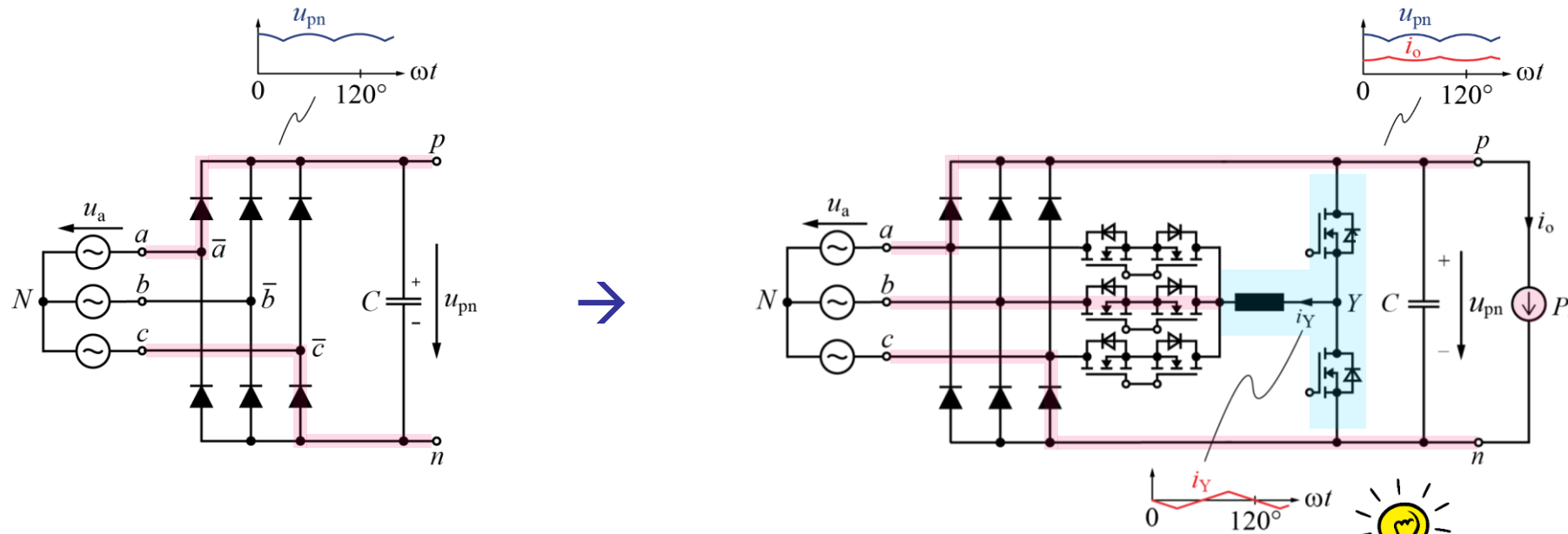


Source: Y. Lei &
R. Pilawa-Podgurski, 2015

- **8-to-1 Dickson Soft-Charging SCC**
- **12 GaN Switches (40V & 100V) / 7 Flying Caps. (0.22uF & 2.2uF, 50|100|250V), 3.3uH**

Hybrid Integrated Active Filter (IAF) PFC Rectifier

- **Hybrid Combination** of Mains- and Forced-Commutated Converter
- **3rd Harmonic Current Injection** into Phase with Lowest Voltage
- **Phase Selector AC Switches** Operated @ Mains Frequency — **3- Φ Unfolder**



- **Non-Sinusoidal Mains Current**

- **P_o = const. Required**
- **Sinusoidal Mains Current**
- **NO (!) DC Voltage Control**

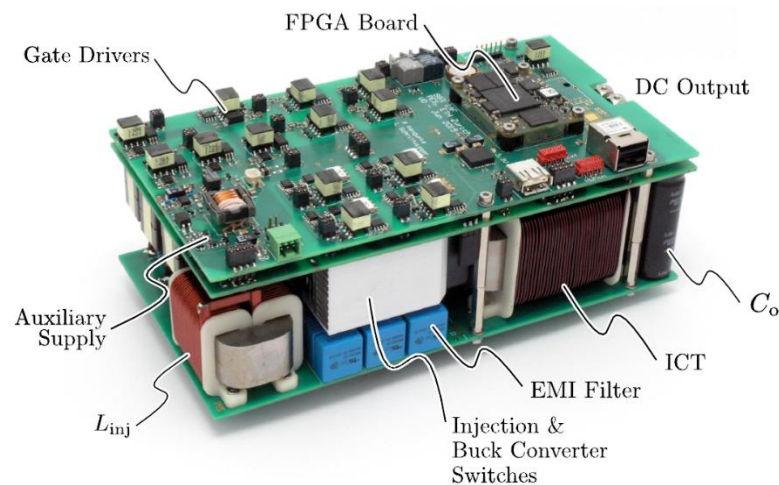
IAF PFC Rectifier & Buck Converter Demonstrator

- Efficiency $\eta > 99.1\%$ @ 60% Rated Load
- Mains Current $THD_I \approx 2\%$ @ Rated Load
- Power Density $\rho \approx 4\text{kW}/\text{dm}^3$

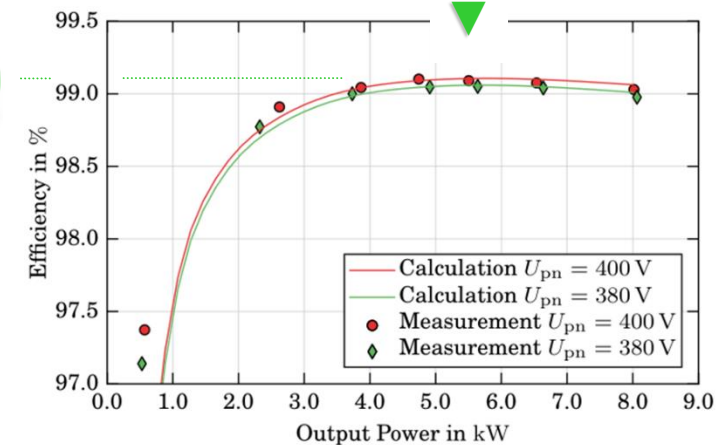
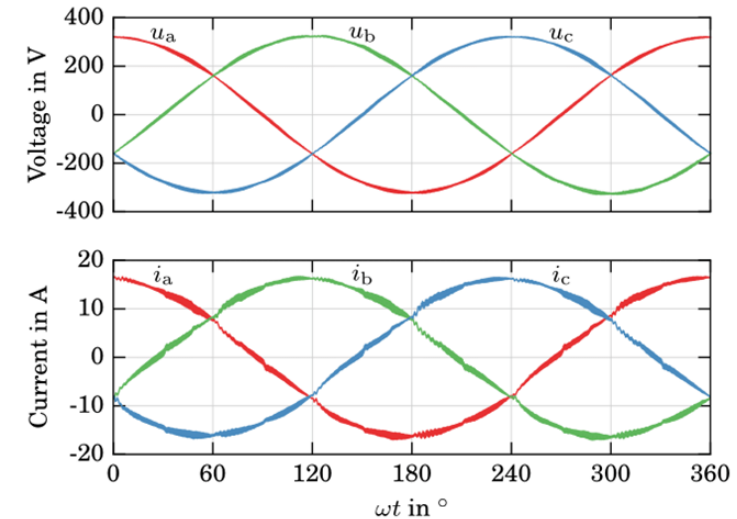
$$P_o = 8\text{ kW}$$

$$U_N = 400\text{V}_{AC} \rightarrow U_o = 400\text{V}_{DC}$$

$$f_s = 27\text{kHz}$$

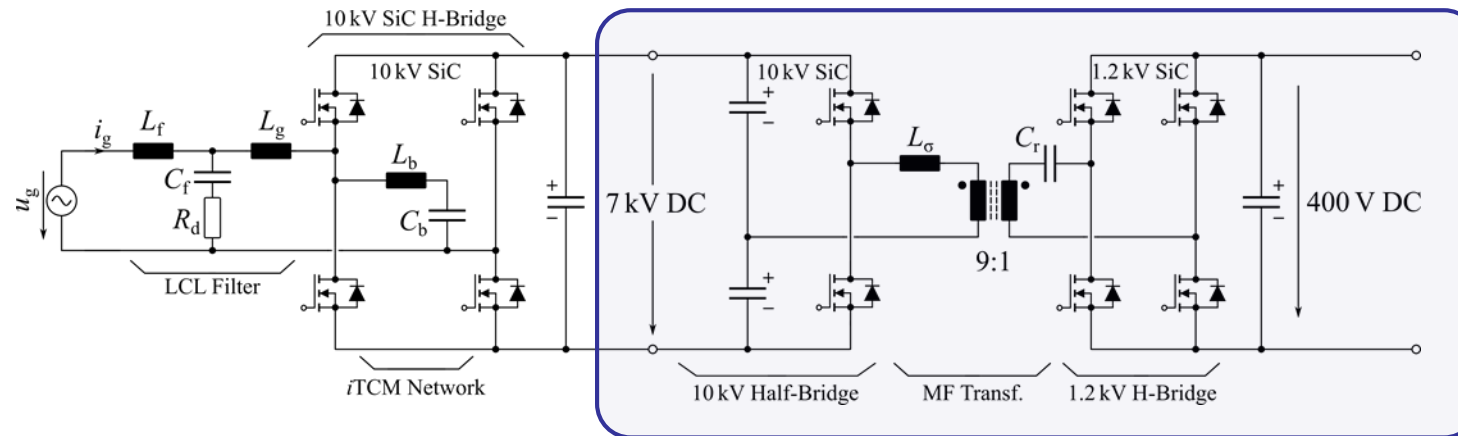


- SiC Power MOSFETs & Diodes
- 2 Interleaved Buck Output Stages
- Controlled Output Voltage



Hybrid 1- Φ AC/DC—DC/DC Solid-State Transformer

- Bidirectional 3.8 kV_{rms} 1- Φ AC \rightarrow 400V DC @ 25 kW Power Conversion
- Based on 10 kV SiC MOSFETs
- Full Soft-Switching

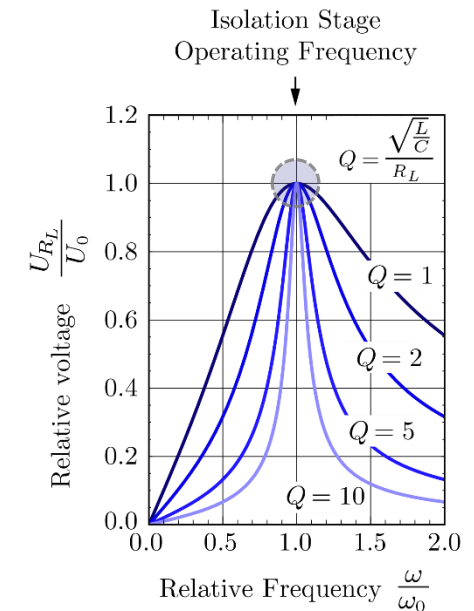


★ 3.3 kW/dm³

★ 3.8 kW/dm³

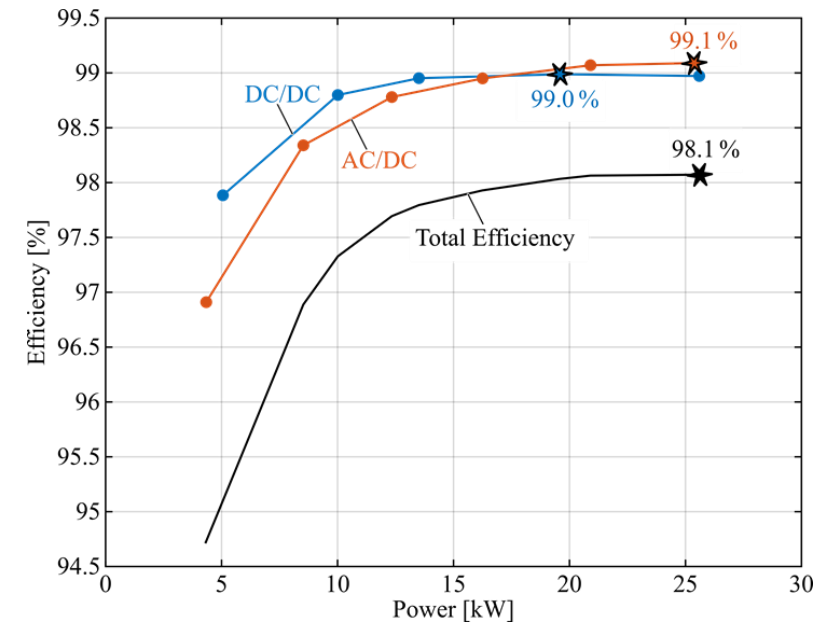
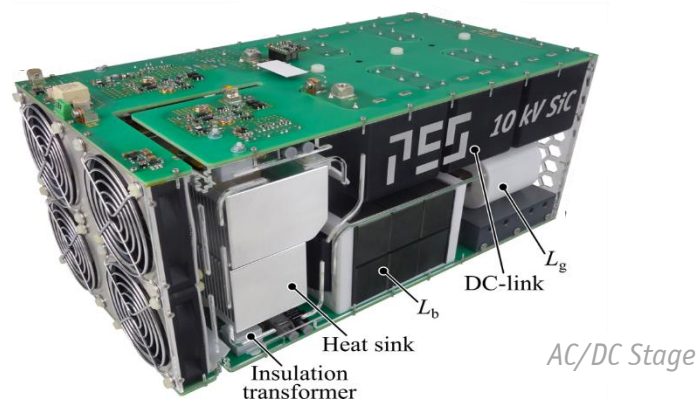
• 35...75 kHz iTCM Input Stage

• 48 kHz «DC-Transformer» Output Stage



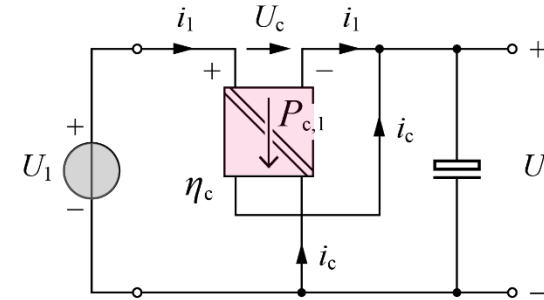
Overall Performance AC/DC — DC/DC

- Full Soft-Switching
- 98.1% Overall Efficiency @ 25 kW
- 1.8 kW/dm³ (30 W/in³)



- Significantly Simpler System Structure Compared to Multi-Module (ISOP) SST Approach

Partial/Differential Power Processing



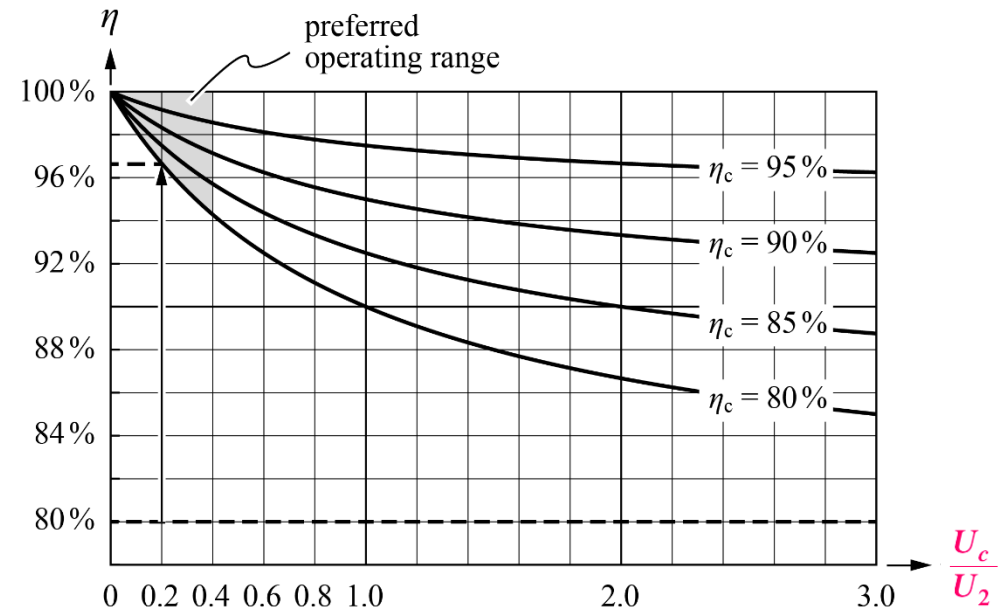
$$U_2 = U_1 - U_c$$

■ Reduced Converter Rating

$$p_c = \frac{P_{c,1}}{P_1} = \frac{\frac{U_c}{U_2}}{1 + \frac{U_c}{U_2}}$$

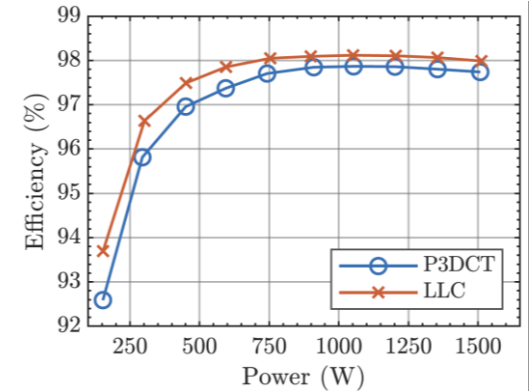
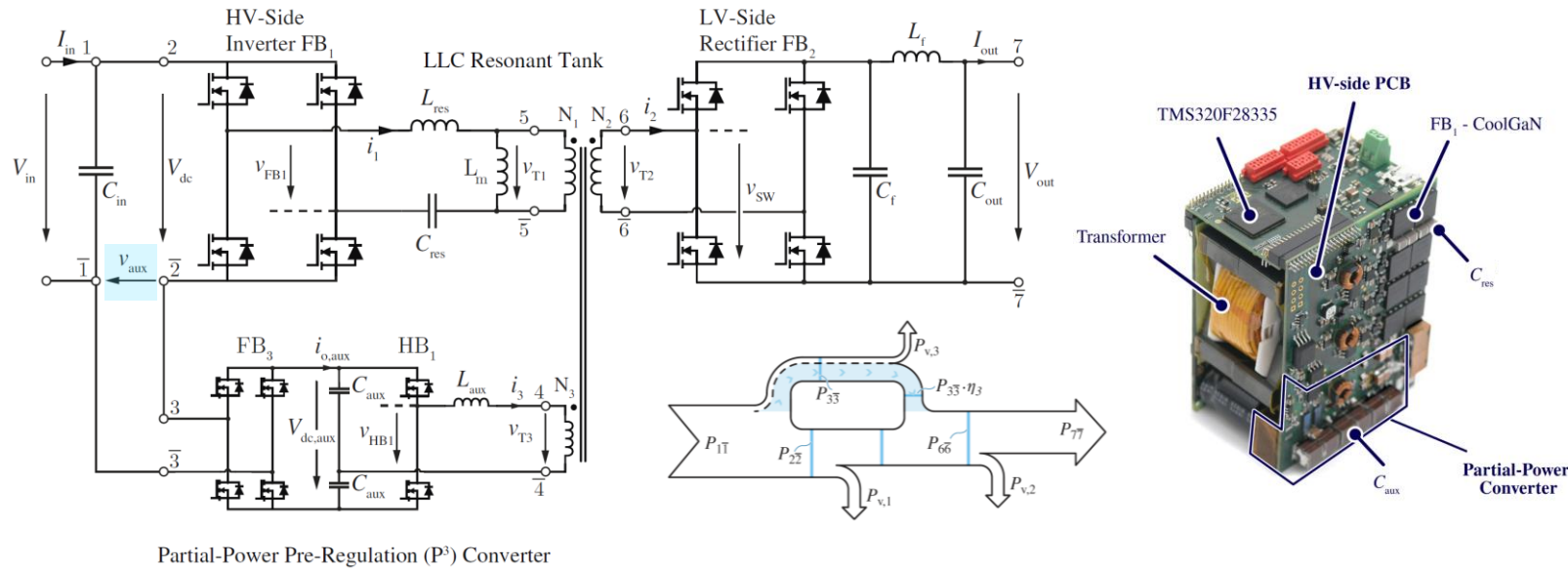
■ Low Influence of Converter Efficiency on Overall Efficiency

$$\eta = \frac{P_2}{P_1} = \frac{(1 + \frac{U_c}{U_2} \eta_c)}{(1 + \frac{U_c}{U_2})}$$



Partial-Power Pre-Regulated LLC DC-Transformer

- **Aux. Converter Stage for $\pm 10\%$ V_{in} Compensation** | $V_{in} = 340V \dots 420V$
- **Const. Voltage Transfer Ratio / High Efficiency LLC «DC/DC Transformer»** @ Const. Frequency | $f_{sw} = 100kHz$
- **Const. Output Voltage** | $V_{out} = 48V$

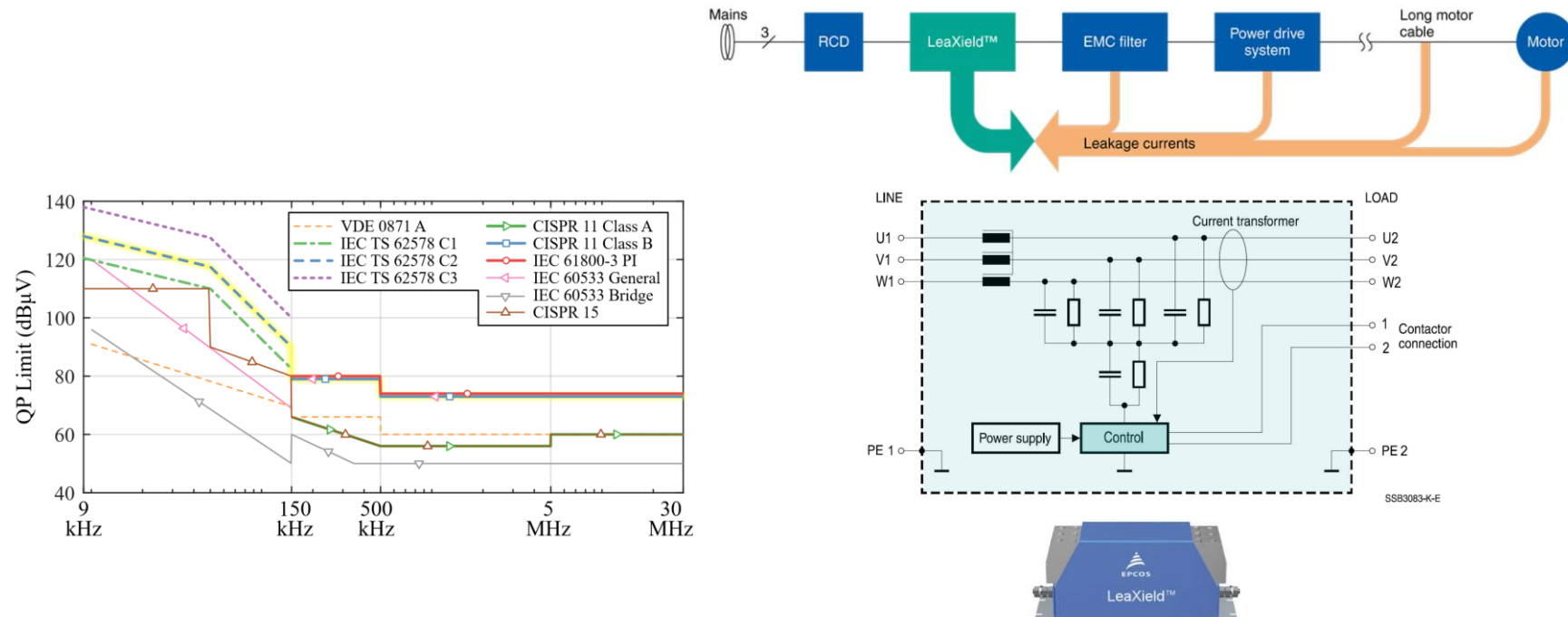


★ $\approx 140 W/in^3$

- **Rectangular Aux. Voltage Added or Subtracted ($f_{aux} = 600kHz$) from V_{in}**
- **Marginal Impact of Control on Overall Power Density & Efficiency**

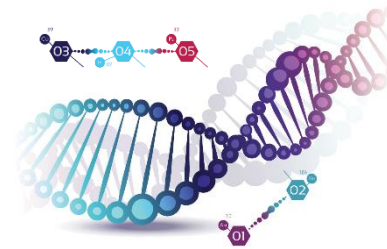
Hybrid EMI-Filter / Leakage Current Reduction

- **Future Extension of EMI Limits — 9kHz ...150kHz** | IEC TS 62578 Tech Spec. for Active Infeed Conv. Applications
- **Earth Leakage Current “Compensation”**
- **Conducted CM EMI-Filter**



- **Prevents Unintentional Residual Current Device (RCD) Tripping w/o Isolation Transformer**
- **Attenuation of Cond. EMI Emissions in Wide Frequency Range 30/40/15dB @ 4/10/150kHz**

X-Concept

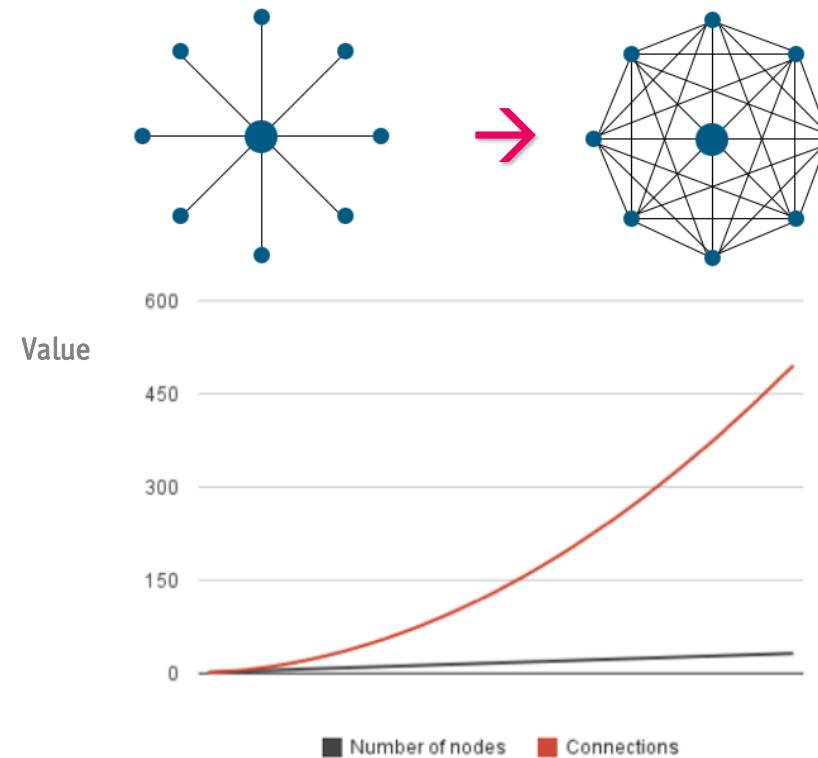
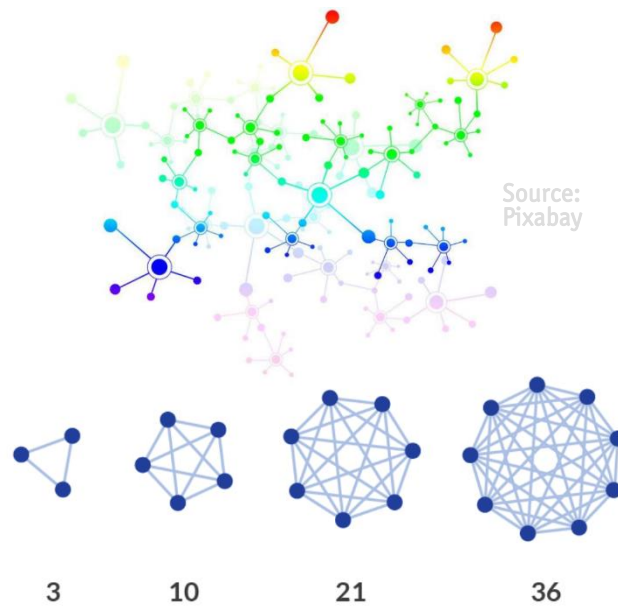


Decentralization

Networking Scaling

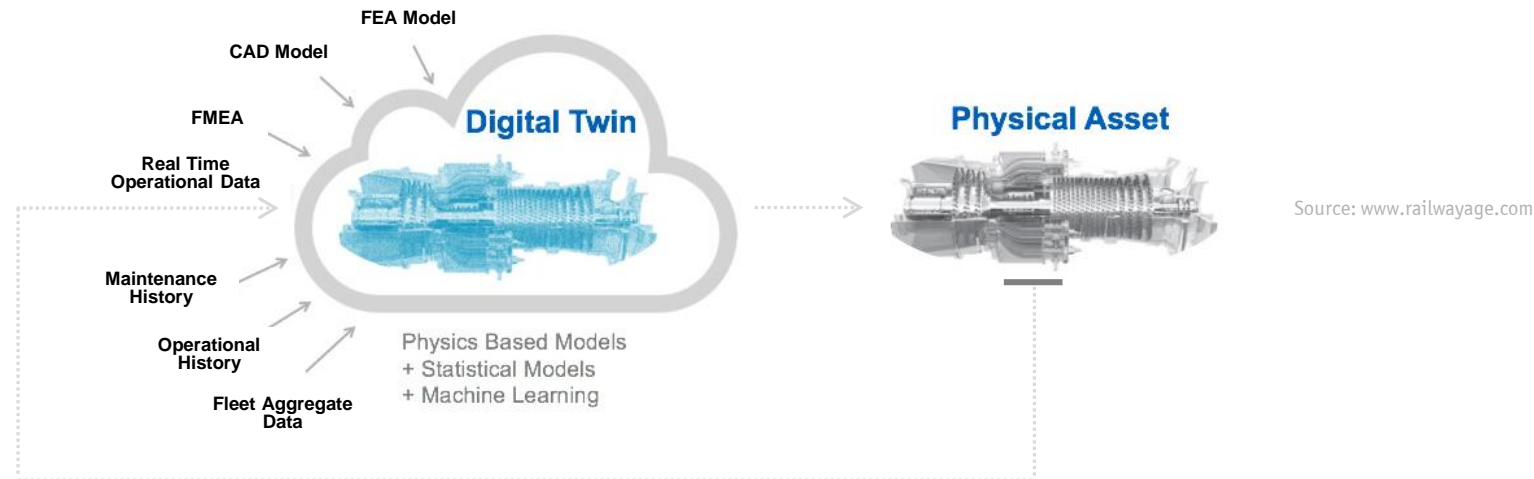
■ Metcalfe's Law

- Moving from Hub-Based Concept to Community Concept Increases Potential Network Value
Over-Proportional $\rightarrow \sim n(n-1)$ or $\sim n \log(n)$



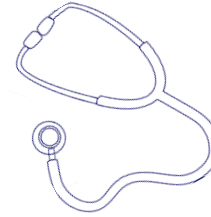
IIoT in Power Electronics

- **Digital Twin** → **Physics-Based “Digital Mirror Image”**
- **Digital Thread** → **“Weaving” Real/Physical & Virtual World Together**

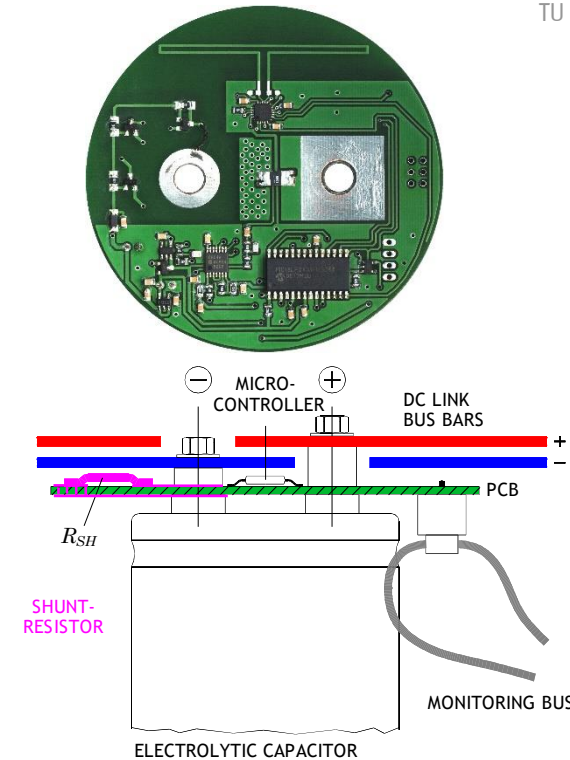
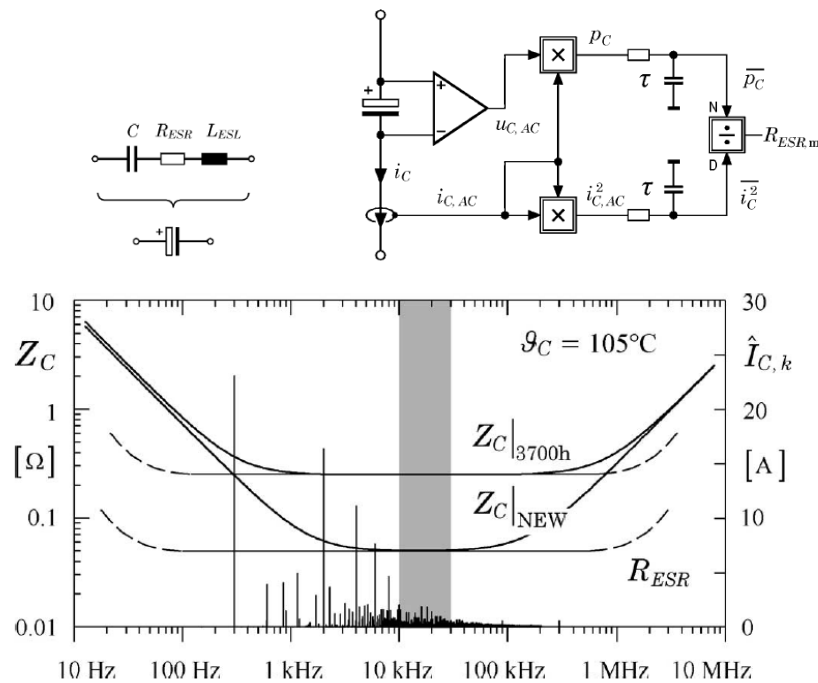


- **Requires Proper Interfaces for Models & Automated Design**
- **Model of System's Past/Current/Future State → Design Corrections / Predictive Maintenance etc.**

IIoT Starts with Sensors (!)



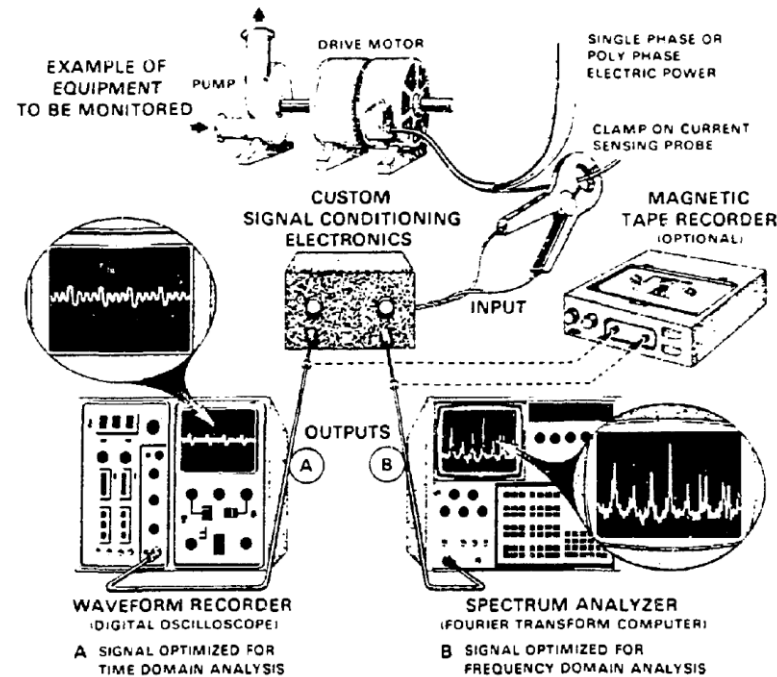
- **Condition Monitoring of DC Link Capacitors**
- **On-Line Measurement of the ESR in "Frequency Window" (Temp. Compensated)**
- **Data Transfer by Optical Fibre or Near-Field RF-Link**



- **Possible Integration into Capacitor Housing or PCB**
- **Additionally features Series Connect. Voltage Balancing**

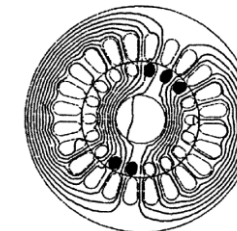
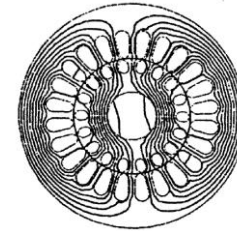
Motor Condition Monitoring / Fault Detection

- Utilize the “Motor as Transducer” for Determining Aging / Service Wear of Motor / Mechanical Load
- Non-Intrusive Detection of Mechanical or Electrical - Bearings or Stator & Rotor - Abnormalities
- Motor Current Signature Analysis (MCSA) in Time & Frequency Domain

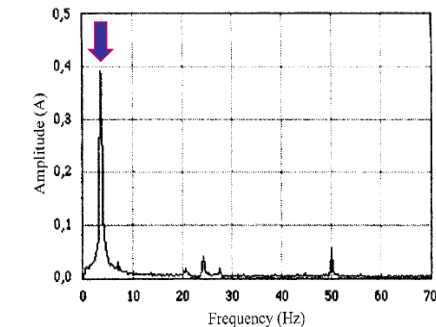
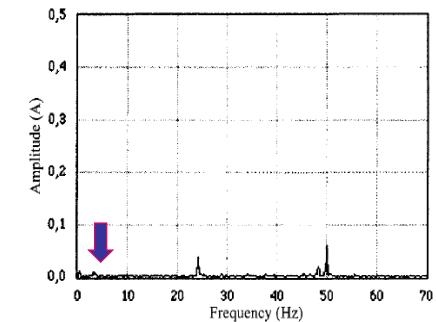


Source: ORNL, Kryter et al., 1989

Source: R. Fiser et al, 1997

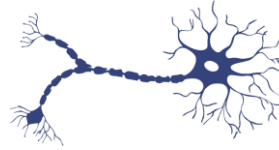


Source: S. Cruz et al, 1998



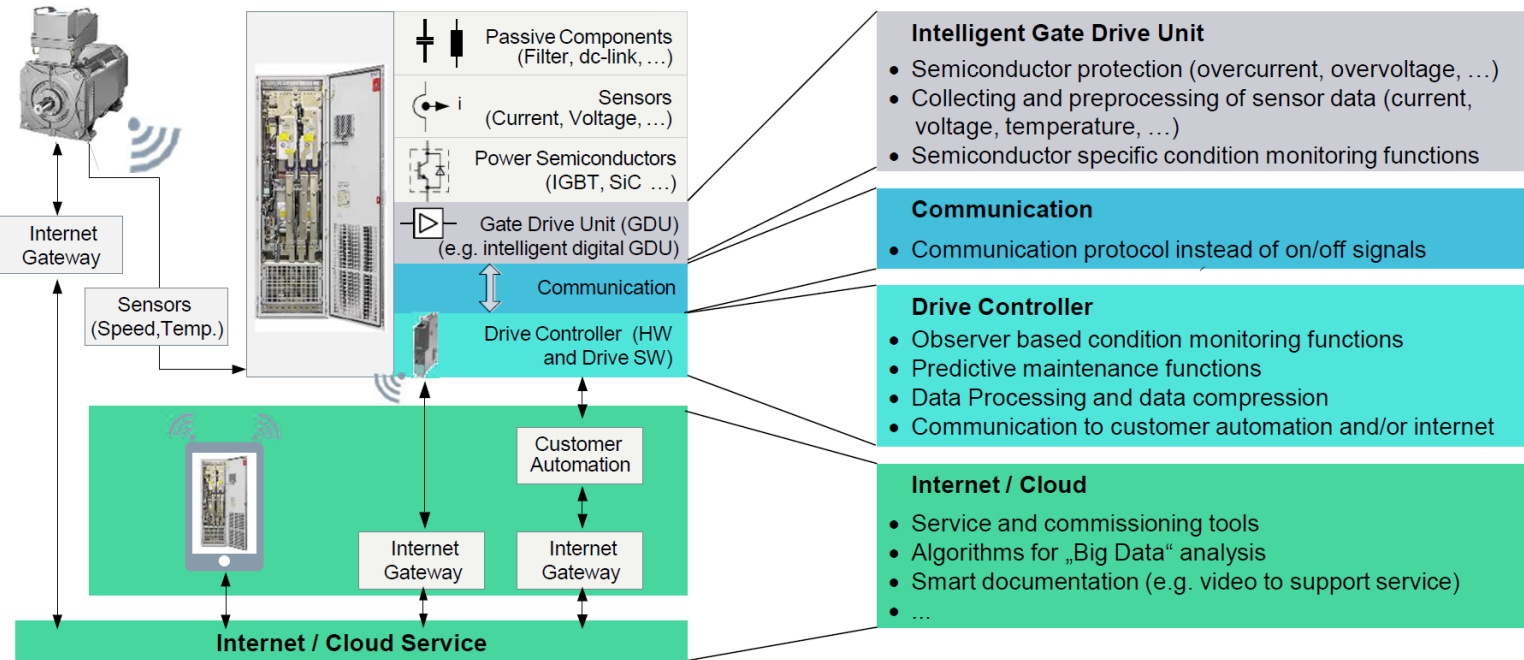
- ORNL (1989) — MCSA Condition Monitoring of Motor-Valves in Nuclear Power Plant Safety Systems
- ANNs Discussed for Diagnostics since 25+ Years — Improvements w/ Computing Power of Modern Inverters

Smart Inverter Concept



■ Utilize High Computing Power and Network Effects in the Cloud

Source: R. Sommer
SIEMENS

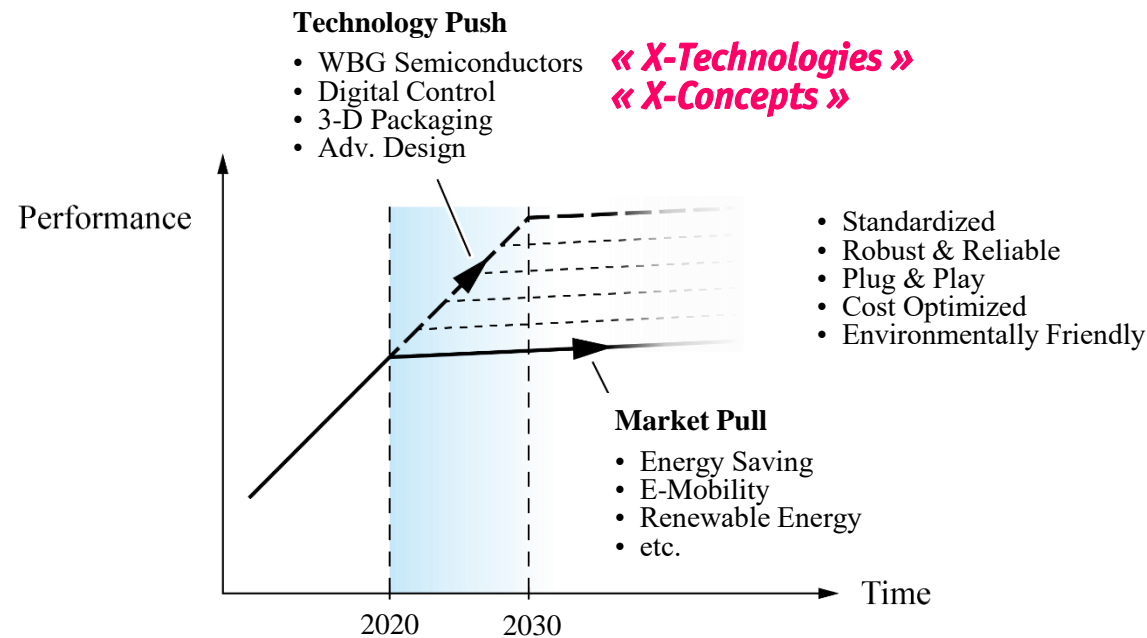


- *On-Line Protection / Monitoring / Optimization on Component | Converter | Drive | Application Level*

— Conclusion —

Future Development / Trends

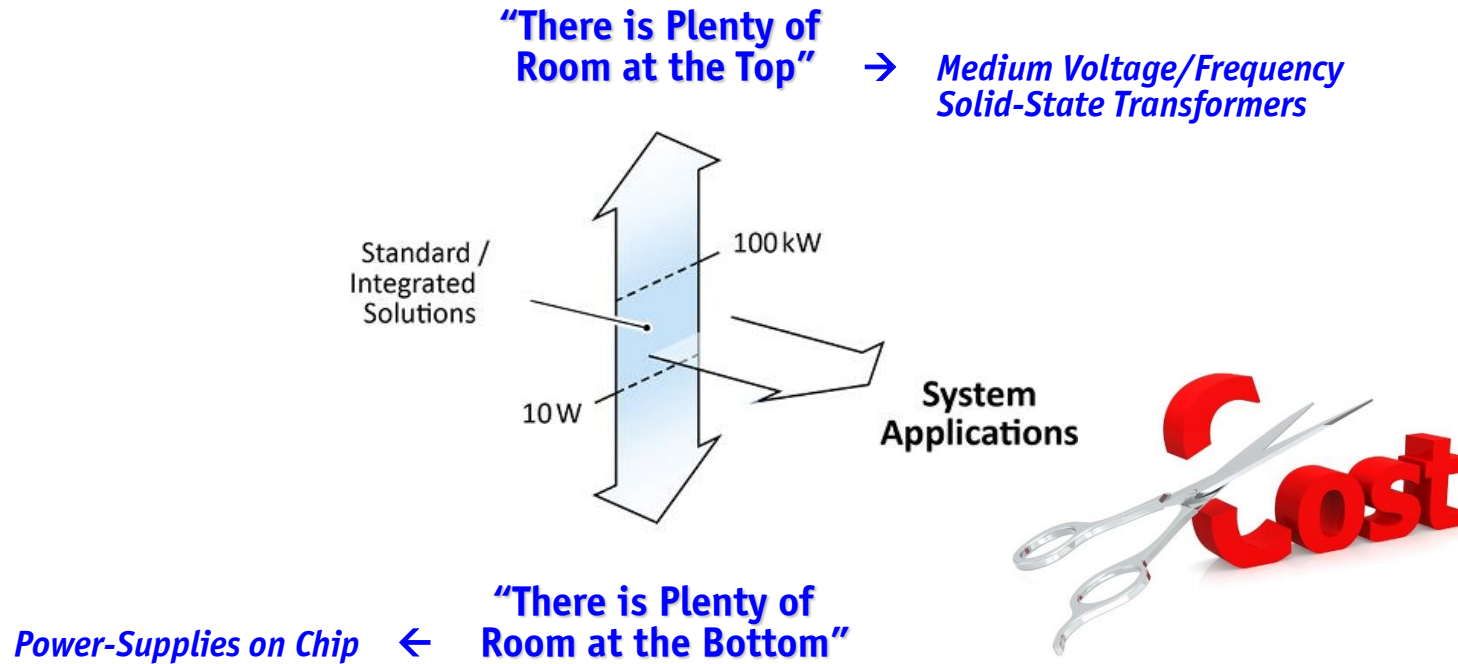
- **MEGA-Trends** — Renewable Energy / Energy Saving / E-Mobility / “SMART XXX”
- **Power Electronics will Massively Spread in Highly Diverse Applications**



- **More Application Specific Solutions**
- **More Specific Requirements** – High Peak/Avg. Ratio, Wide Volt. Range etc.
- **Cost Optimization @ Given Performance Level for Standard Solutions**
- **Design / Optimize / Verify (All in Simulation) — Faster / Cheaper / Better**

Future Application Areas

- *WBG Driven Extension to Medium Voltage | Extension to Micro-Power Electronics*
- *Extreme Cost Pressure for Standardized Solutions (!)*

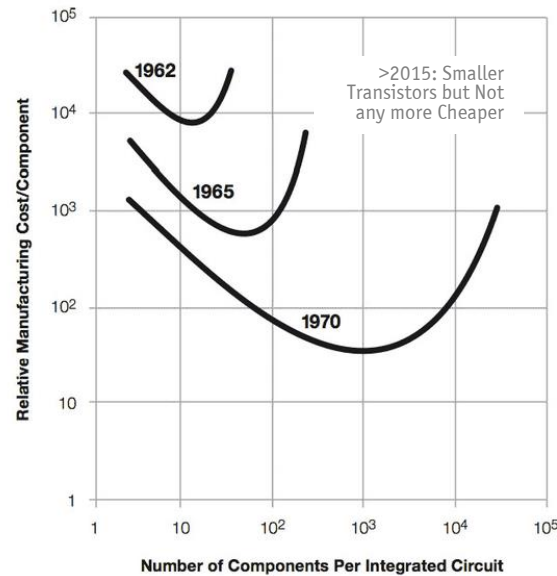


- *“There's Plenty of Room at the Bottom”, Lecture by R. Feynman @ Caltech, 1959*
- *Key Importance of Technology Partnerships of Academia & Industry*

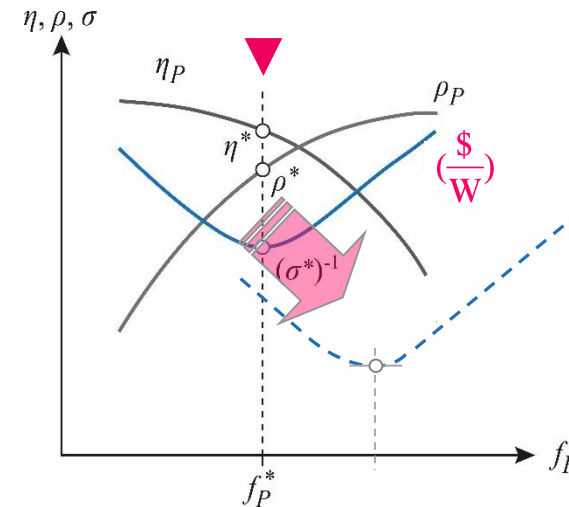
“Moore’s Law” of Power Electronics

- **“Moore’s Law”** Defines Consecutive Technology Nodes Based on Min. Costs per Integr. Circuit (!)
- Complexity @ Min. Comp. Costs Increases approx. by Factor of 2 / Year

Economy of Scale → ← Lower Yield



Gordon Moore: The Future of Integrated Electronics, 1965 (Consideration of Three Consecutive Technology Nodes)



- Potential Power Density Improvement — Factor 2... 5 Until 2030
- Definition of “ $\eta^*, \rho^*, \sigma^*, f_P^*$ – Technology Node” Must Consider Conv. Type / Operating Range etc. (!)

Source:
www.roadtrafficsigns.com



Power Electronics → “Energy” Electronics



- *Design Considering Converters as Standardized “Integrated Circuits” (PEBBs)*
- *Extend Analysis to Converter Clusters / Power Supply Chains / etc.*

- “Converter” → “Systems” (Microgrid) or “Hybrid Systems” (Automation / Aircraft)
- “Time” → “Integral over Time”
- “Power” → “Energy”

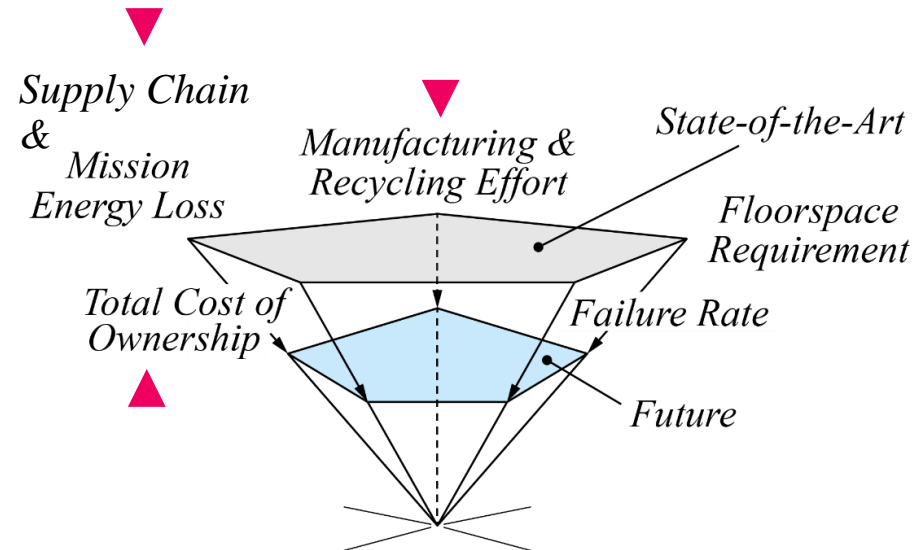
$$p(t) \rightarrow \int_0^t p(t) dt$$

- *Power Conversion* → *Energy Management / Distribution*
- *Converter Analysis* → *System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)*
- *Converter Stability* → *System Stability (Autonom. Cntrl of Distributed Converters)*
- *Cap. Filtering* → *Energy Storage & Demand Side Management*
- *Costs / Efficiency* → *Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency*
- *etc.*

Energy Electronics Systems Performance Figures/Trends

■ Complete Set of New Performance Indices

— Power Density	$[\text{kW}/\text{m}^2]$
— Energy Density	$[\text{kWh}/\text{m}^3]$
— Environmental Impact	$[\text{kWs}/\text{kW}]$
— TCO	$[\$/\text{kW}]$
— Mission Efficiency	$[\%]$
— Failure Rate	$[\text{h}^{-1}]$



Thank you!

