ETH zürich

Power Electronic Systems Laboratory

Motor-Integrated Power Factor Corrected Single-to-Three-Phase AC/AC Converter Concepts

Michael Haider, Dominik Bortis, Johann W. Kolar

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

March 4, 2022

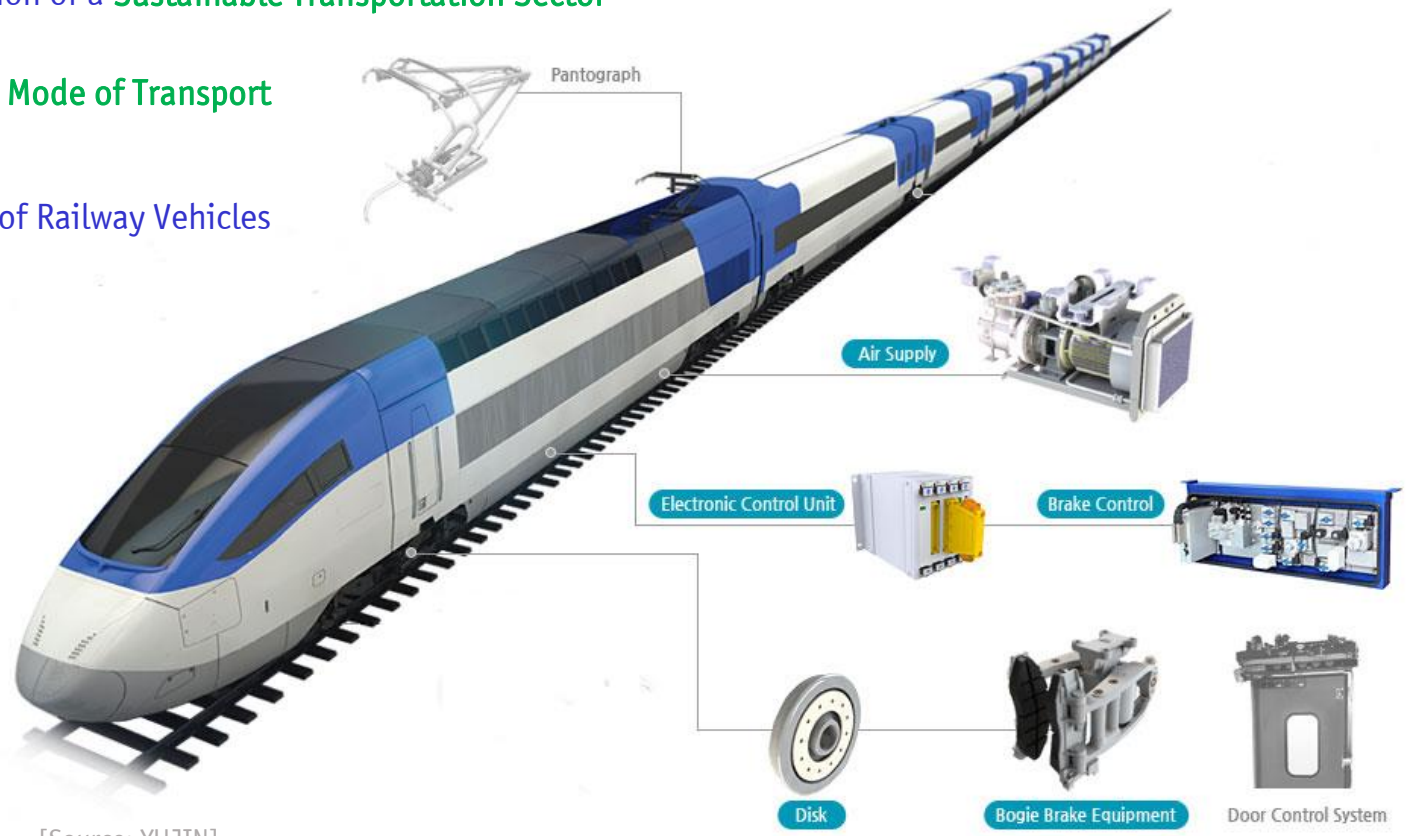
Motivation

- **Reduction of Global Carbon Emissions Required**
- **Transportation Sector Responsible for 14 %** of CO_2 Emissions
- Transportation in **Europe** Approx. **25 %** of All Emissions
- Transportation in **US** Approx. **29 %** of All Emissions

→ **Goal:** Decarbonization and Implementation of a **Sustainable Transportation Sector**

- **Railway Systems: Greenest and Cleanest Mode of Transport**
  - Performance Improvements Demanded
- Focus on **Pressurized Air Supply System** of Railway Vehicles
  - **Air Brake System**
  - Door Control System
  - Pantograph Lifting
- **General Requirements**
  - **Compactness**
  - High Efficiency
  - Reliability
  - Redundancy

→ **Unique Operating Conditions**

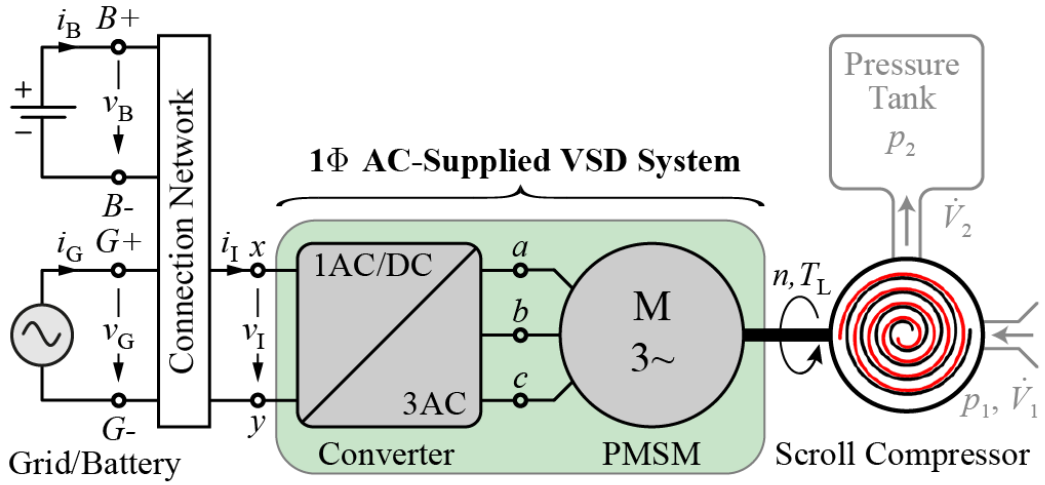


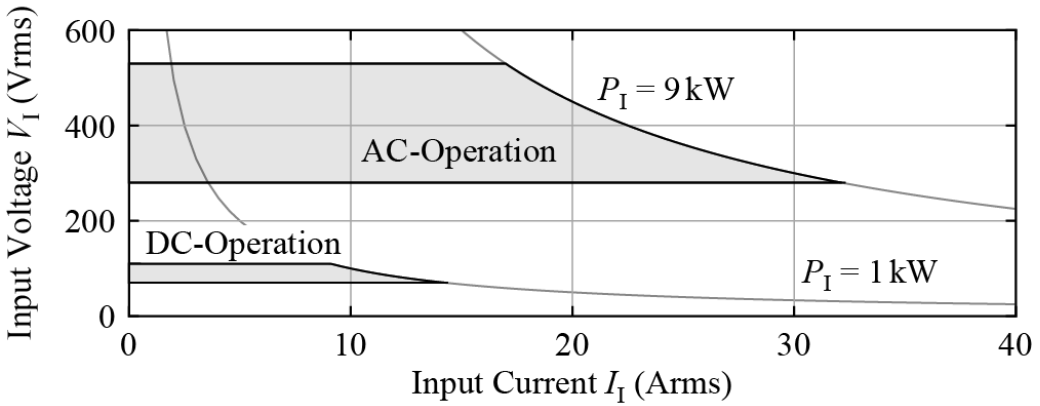
[Source: YUJIN]

Application

- **Oil-Free Scroll Compressor** — 7.5 kW @ 3700 rpm
  - Charge Pressure Tank
- **Variable Speed Operation**
  - Maximum System Performance
- **AC-Operation (Grid)** — 280...530 Vrms
  - Nominal Voltage — 400 Vrms @ 50 Hz
  - Tertiary Traction Transformer Winding
  - Ensure Unity Power Factor Operation
- **DC-Operation (Battery)** — 70....110 Vdc
  - On-Board Battery
  - Startup and Grid Interruption
- **1Φ AC/DC-to-3Φ AC Converter System**
  - **Wide-Input Voltage Range**
  - **Survive Grid Disturbances and Interruptions**

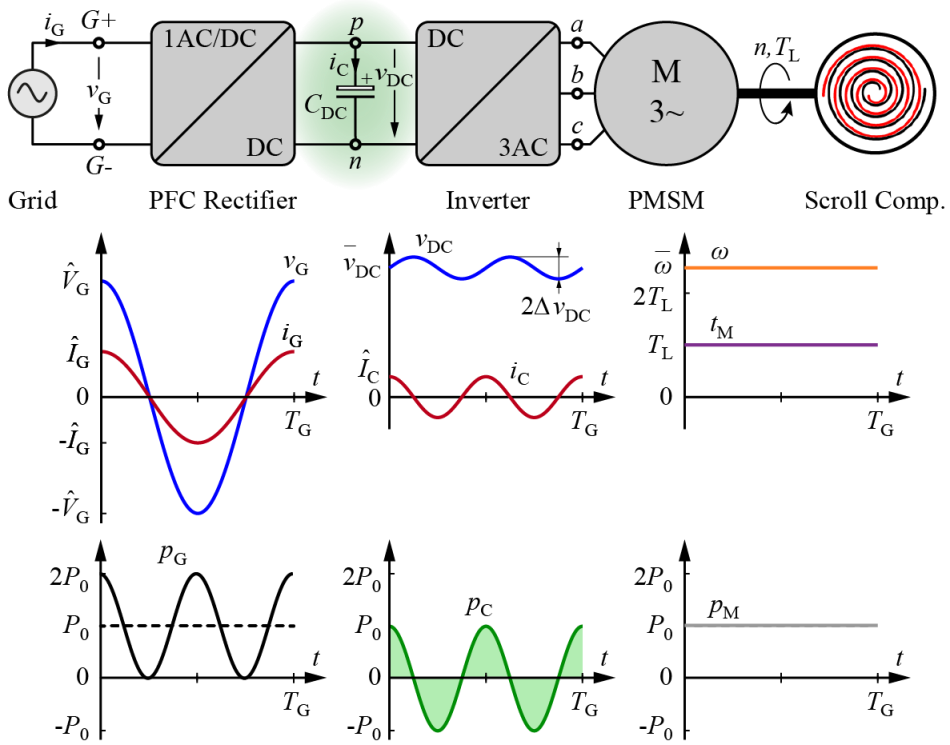
→ **Ultra Compact 1Φ AC-Supplied VSD System**





Challenge

- State-of-the-Art
  - Electrical Energy Storage C_{DC} $\Delta v_{DC} = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{v}_{DC}\, C_{DC}}$

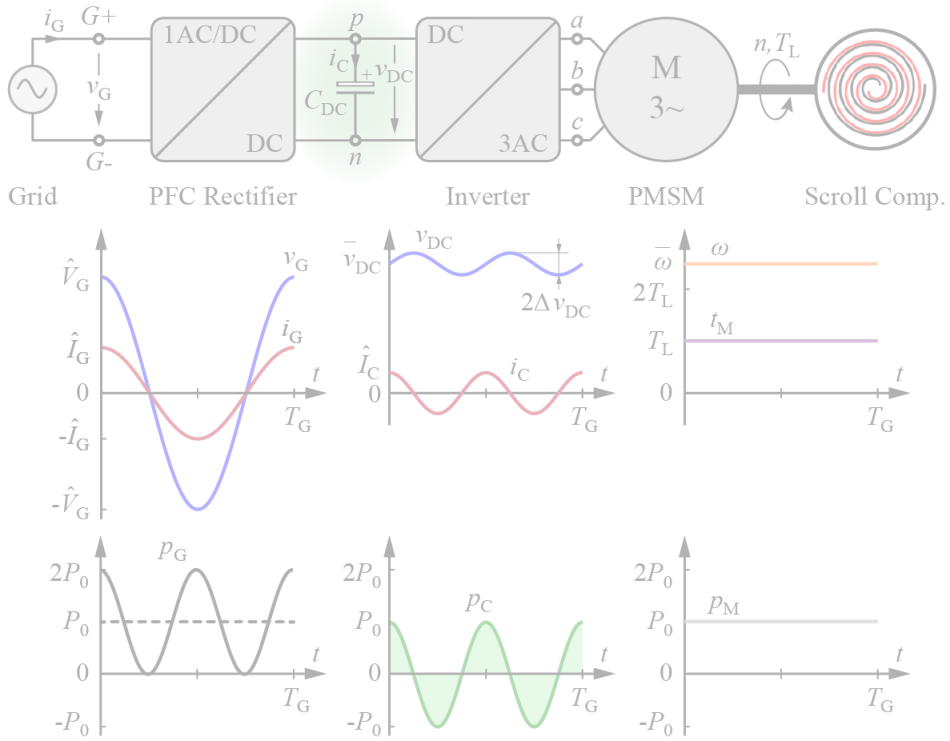


- Avoid Electrolytic Capacitors (1 ltr.) → Increased Lifetime

Motor-Integrated Power Pulsation Buffer (MPPB)

State-of-the-Art

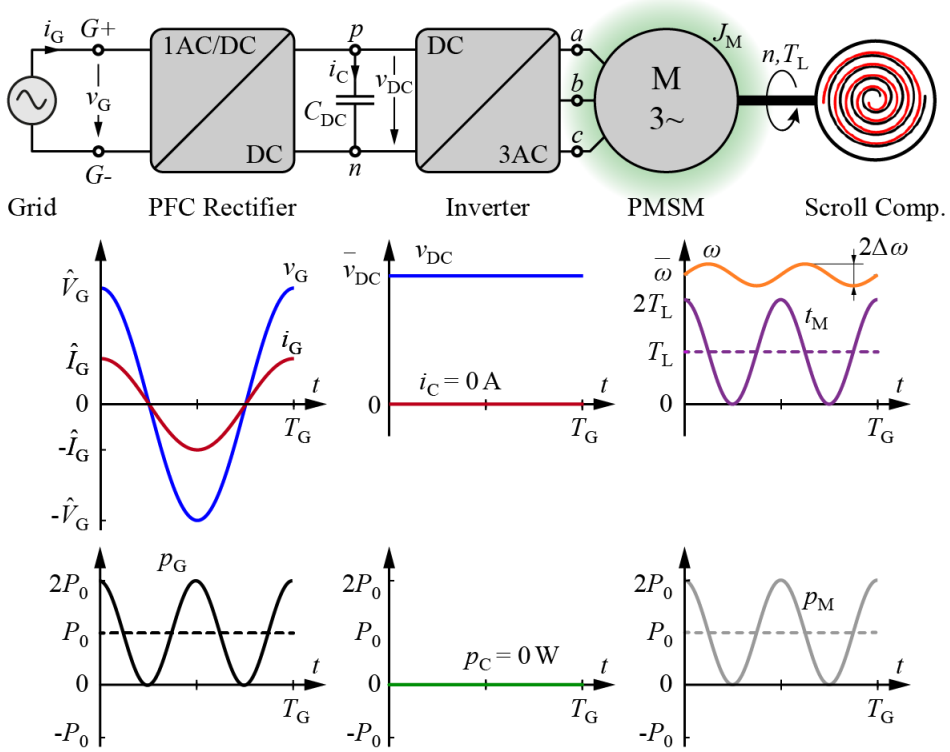
- Electrical Energy Storage C_{DC} $\quad \Delta v_{DC} = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{v}_{DC}\, C_{DC}}$



- Avoid Electrolytic Capacitors (1 ltr.) → Increased Lifetime

Proposed MPPB Concept

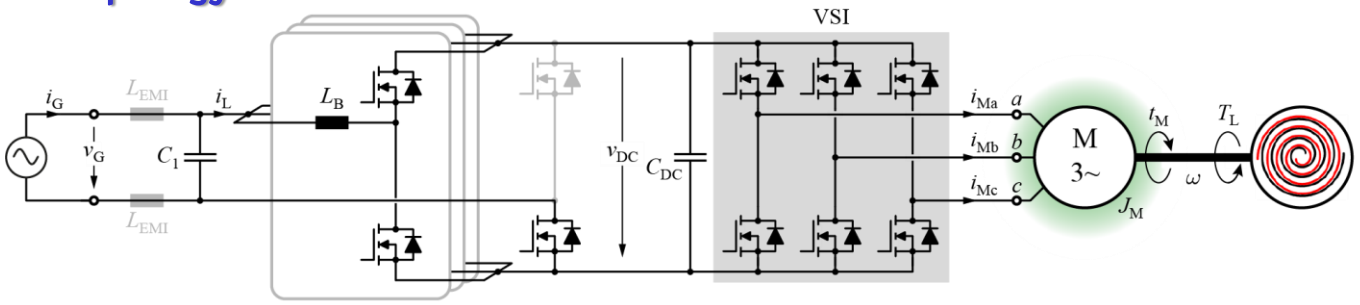
- Mechanical Energy Storage J_M $\quad \Delta\omega = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{\omega}\, J_M}$



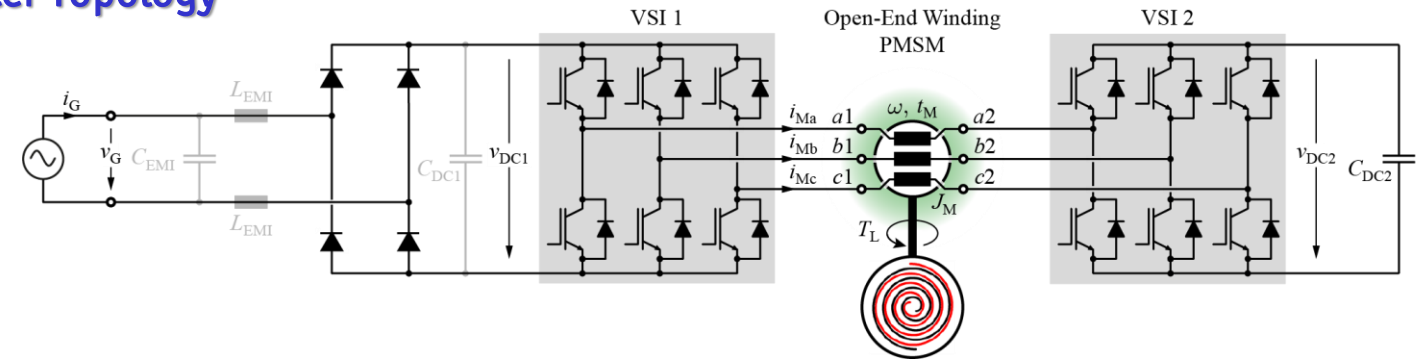
→ Electrolytic-Less 1Φ AC-Supplied VSD System

Focus of the Talk

Part I: Single-Inverter Topology

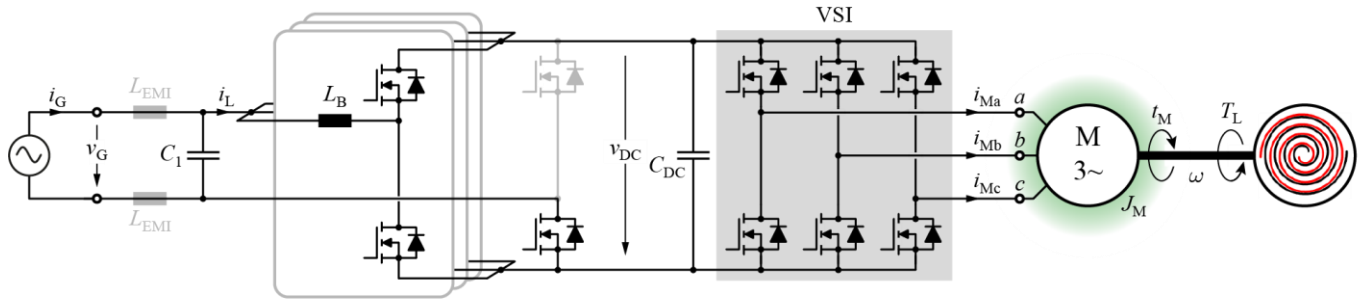


Part II: Dual-Inverter Topology



Part III: dv/dt-Limited PWM-Based VSD Systems

Part I
Single-Inverter (SI) Topology



SI – Topology

- **Two-Stage Implementation**

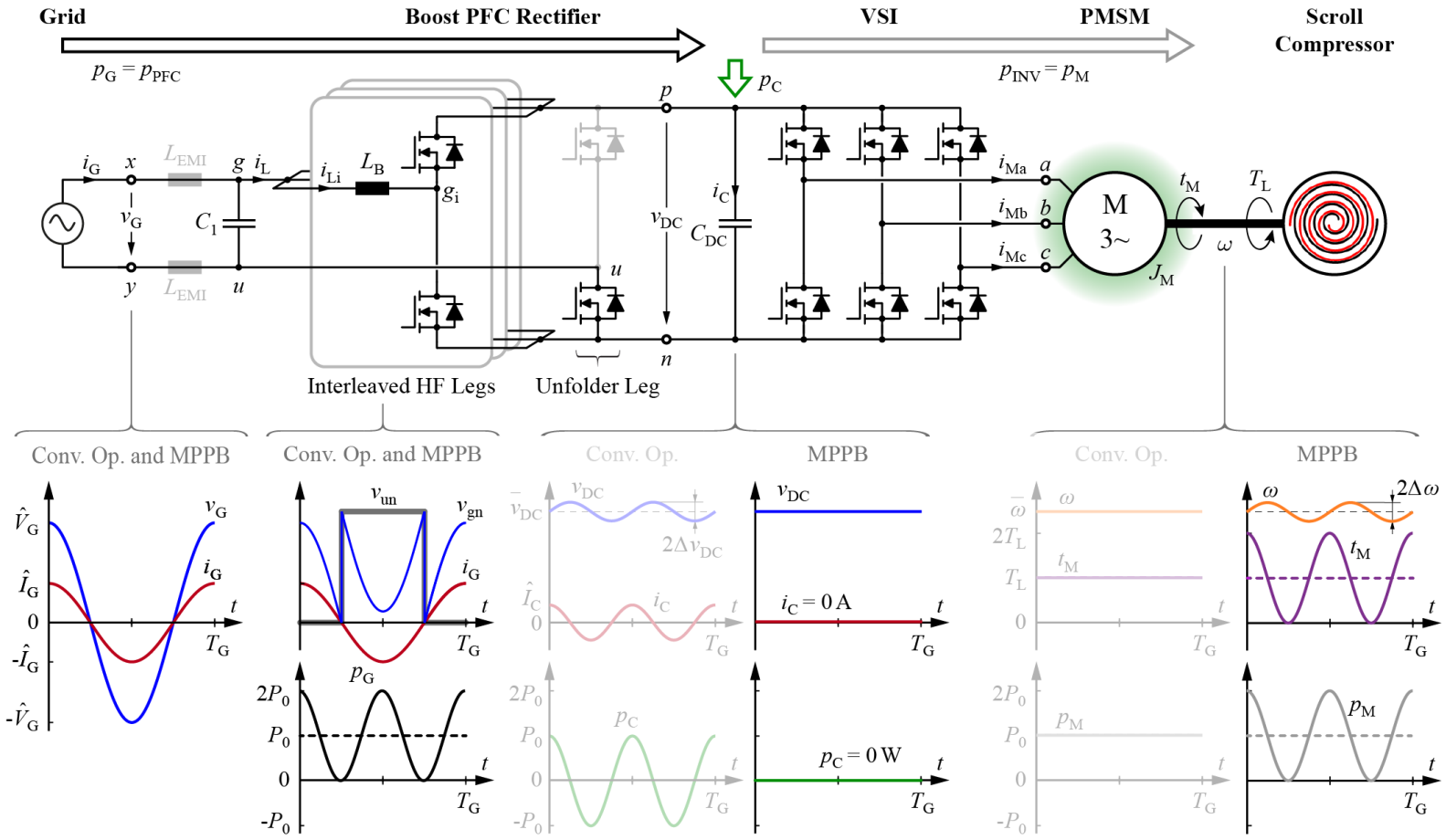
- **I. PFC Rectifier**
  - Boost-Type
  - Totem-Pole with Unfolder Leg
  - Three Interleaved HF Legs

- **Intermediate DC-Link**
  - Electrolytic-Less
  - Nominal: 650 Vdc
  - Maximum: 800 Vdc

→ 1.2 kV SiC MOSFETs

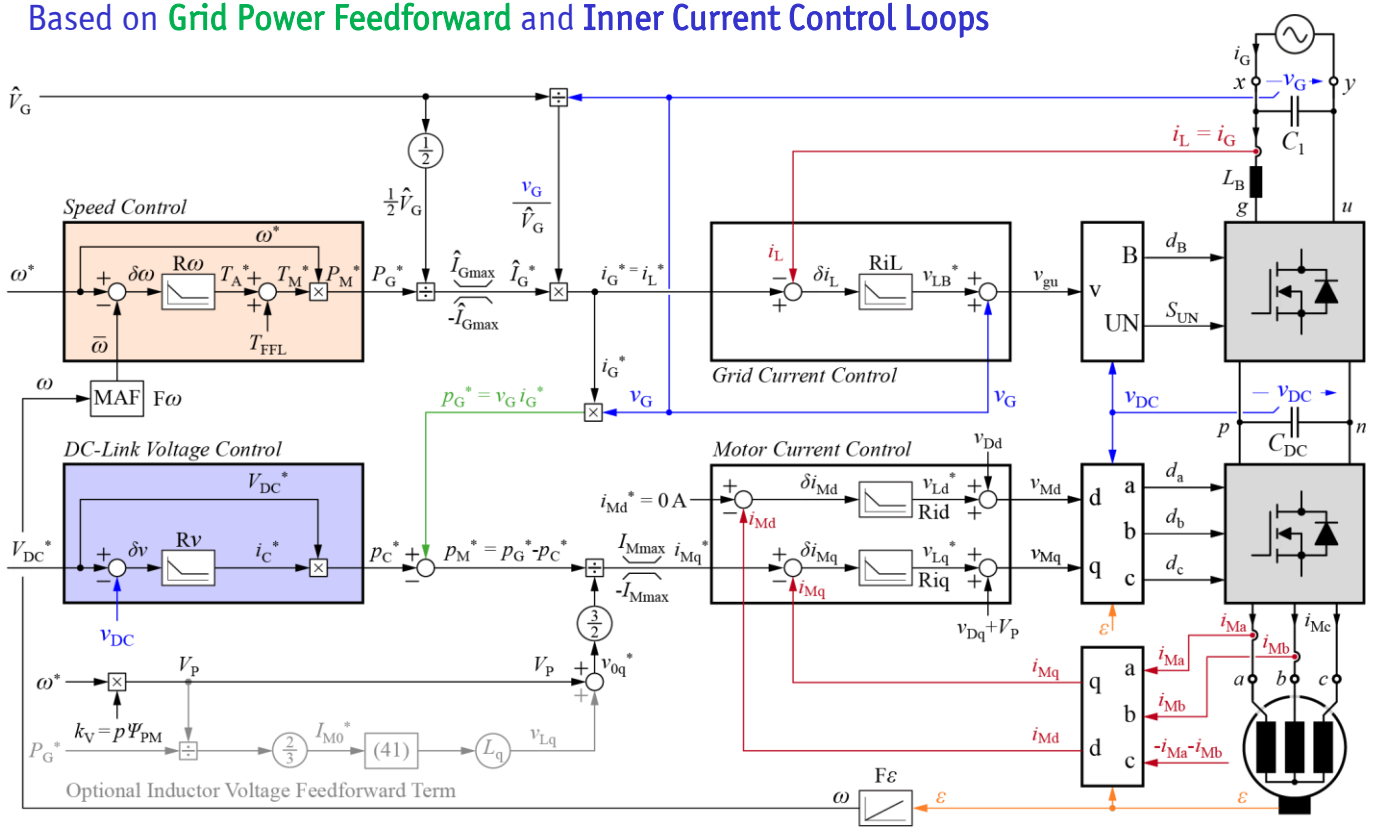
- **II. Three-Phase Inverter**
  - Two-Level
  - Voltage Source Inverter (VSI)

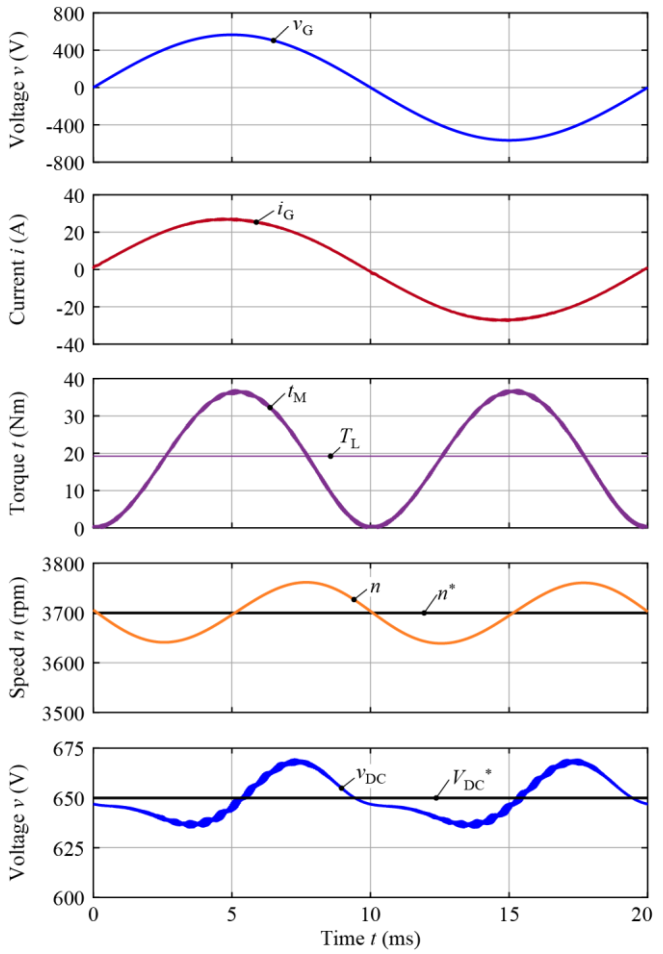
→ How to Control?



SI – Control

- **Control Objectives: PFC Operation, DC-Link Voltage and Average Speed Control**
- Implemented in Cascaded Fashion
- Based on **Grid Power Feedforward** and **Inner Current Control Loops**





→ Verified by Circuit Simulation for C_{DC} = 60 µF - only 8 µF/kW

→ Voltage / Speed Ripple 34 V_{pkpk} / 120 rpm_{pkpk}

Performance Analysis

Source: Siemens

SI – Comparative Phase Current Analysis

■ Conventional System ($i_{Md} = 0$ A)

- Torque-Generating Current

$$i_{Mq} = I_{M0} = \frac{2P_0}{3V_P} \sim T_L$$

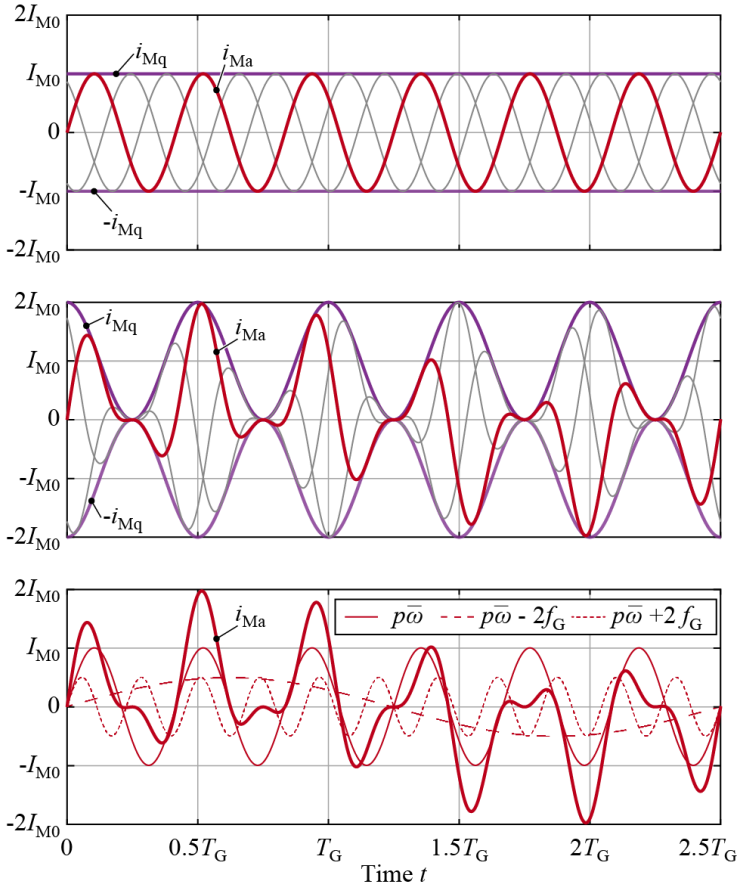
■ Electrolytic-Less MPPB ($i_{Md} = 0$ A)

- Torque-Generating Current

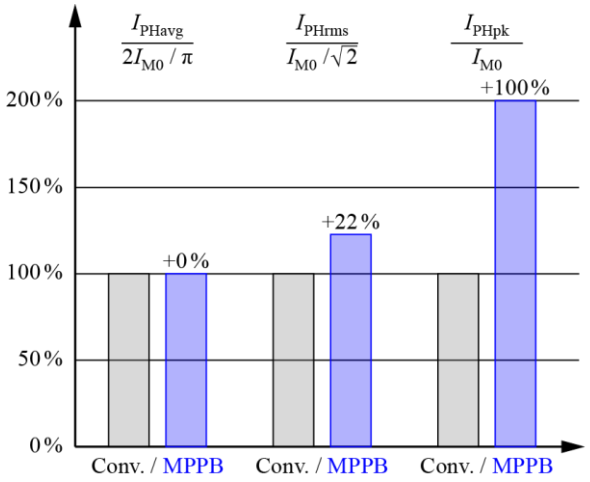
$$i_{Mq} = I_{M0}\,[1 + \cos(4\pi f_G\, t)] \sim t_M$$

■ dq-Transformation with $\varepsilon = p\bar{\omega}\, t$

$$\begin{bmatrix} i_{Ma} \\ i_{Mb} \\ i_{Mc} \end{bmatrix} = \begin{bmatrix} \cos(\varepsilon) & \sin(\varepsilon) \\ \cos(\varepsilon - 2\pi/3) & \sin(\varepsilon - 2\pi/3) \\ \cos(\varepsilon + 2\pi/3) & \sin(\varepsilon + 2\pi/3) \end{bmatrix} \cdot \begin{bmatrix} i_{Md} \\ i_{Mq} \end{bmatrix}$$



■ Comparison



Source: Siemens

■ Superposition: $i_{Ma} = -I_{M0}\left[\sin(p\bar{\omega}\, t) + \frac{1}{2}\sin(p\bar{\omega}\, t + 4\pi f_G\, t) + \frac{1}{2}\sin(p\bar{\omega}\, t - 4\pi f_G\, t)\right]$

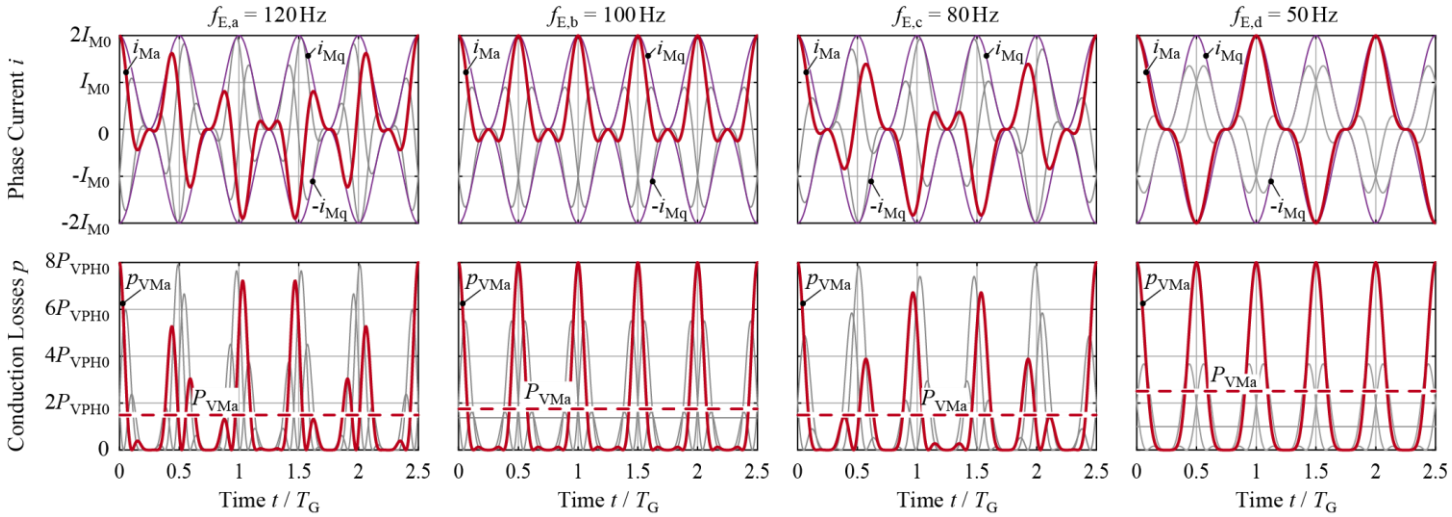
→ Harmonic Components @ $p\bar{\omega}$, $p\bar{\omega} + 4\pi f_G$ and $p\bar{\omega} - 4\pi f_G$

SI – Phase Conduction Losses

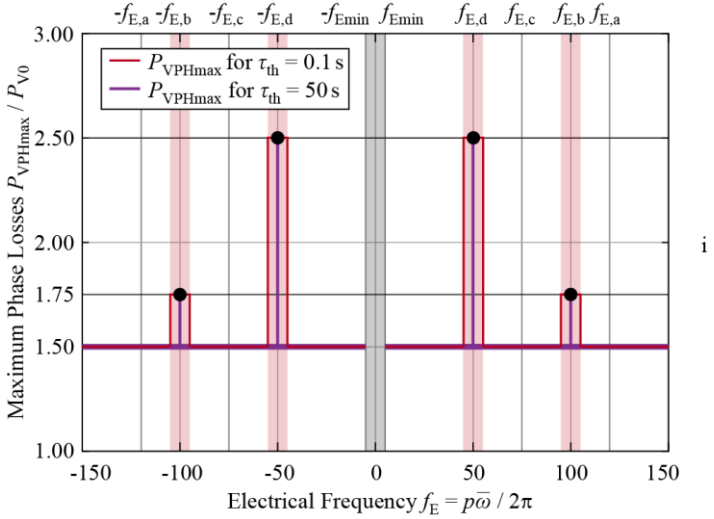
- Harmonic Components: $p\bar{\omega}$, $p\bar{\omega} + 4\pi f_G$ and $p\bar{\omega} - 4\pi f_G$

- **Standing Waves** for $p\bar{\omega} = 4\pi f_G$ (100 Hz) and $p\bar{\omega} = 2\pi f_G$ (50 Hz)
- Similar to Startup

- Asymmetric Phase Stresses



→ Restricted Frequency Ranges



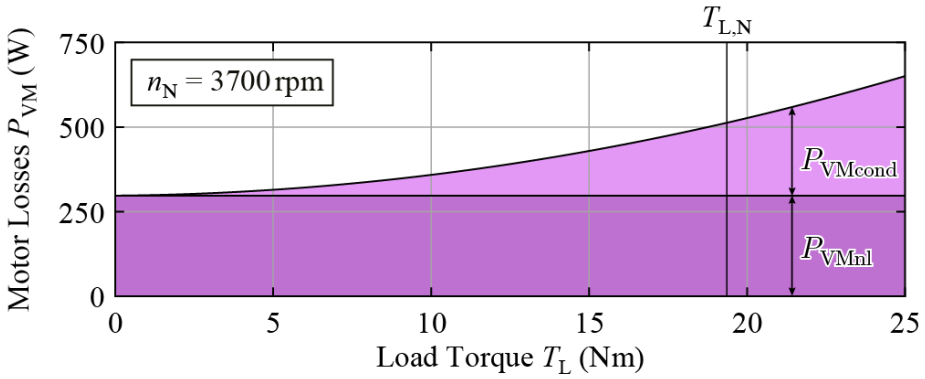
- Total Conduction Losses Remain

→ **Degree of Freedom:** Number of Pole Pairs p

SI – Performance Analysis: Motor and Inverter

M. Motor

- Conventional System $P_{VM0} = P_{VMnl} + \frac{3}{2} R_s I_{M0}^2$
- Electrolytic-Less MPPB $P_{VM} = P_{VMnl} + \frac{9}{4} R_s I_{M0}^2$
- Relative Loss Increase +25 %



I. IGBT Inverter

$$P_{VI} = 3V_f I_{PHavg} + 3f_{Isw} k_1 I_{PHavg}$$

- No Additional Losses - High Total Losses

II. MOSFET Inverter with dv/dt-Limitation (Miller Capacitor)

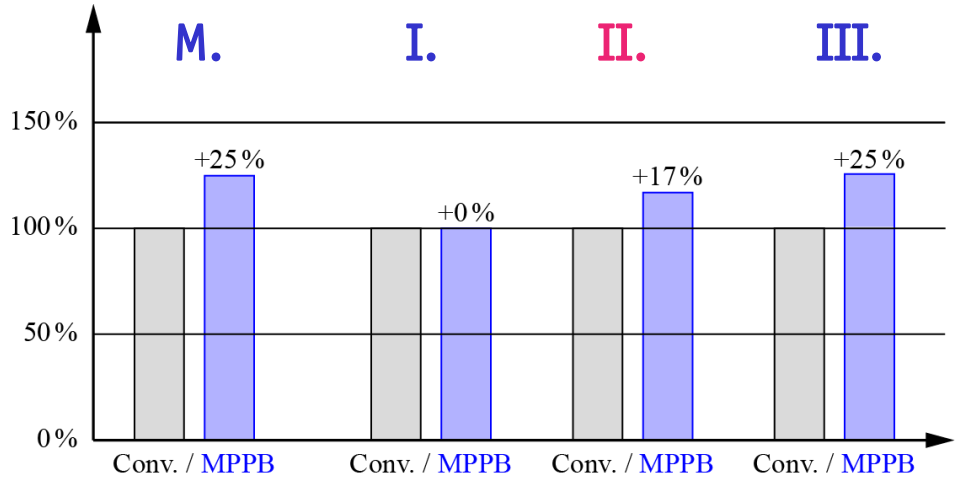
$$P_{VI} = 3R_{on} I_{PHrms}^2 + 3f_{Isw}(k_0 + k_1 I_{PHavg})$$

- Relative Loss Increase + 17 %

III. MOSFET Inverter with LC-Output-Filter

$$P_{VI} = 3R_{on} I_{PHrms}^2 + 3f_{Isw}(k_0 + k_1 I_{PHavg} + k_2 I_{PHrms}^2)$$

- Relative Loss Increase + 25 %
- Peak Phase Current + 100 %

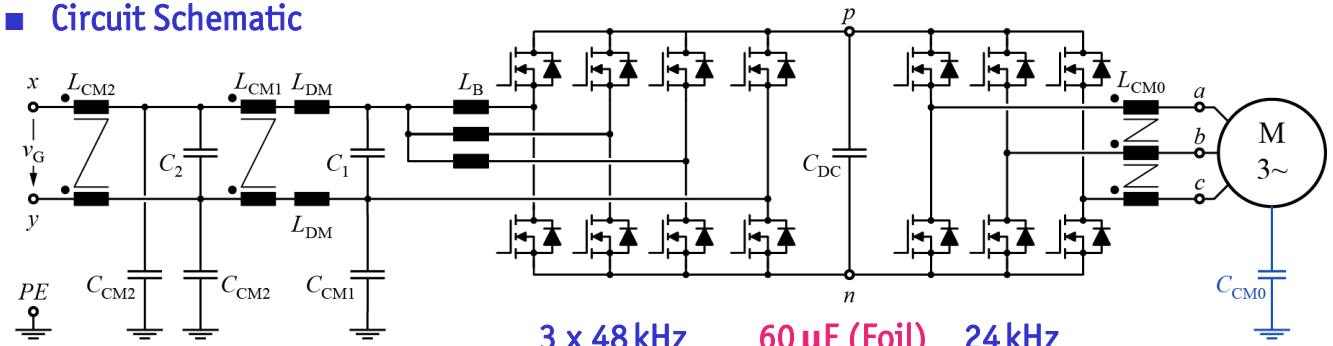


→ Implement and Verify Hardware Demonstrator

Implementation and Verification

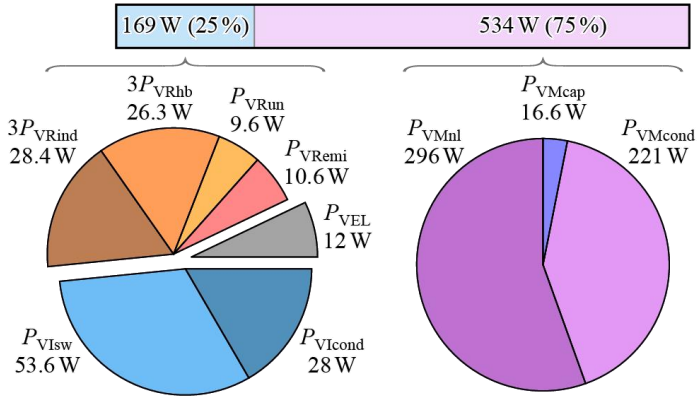
SI – Implementation

Circuit Schematic

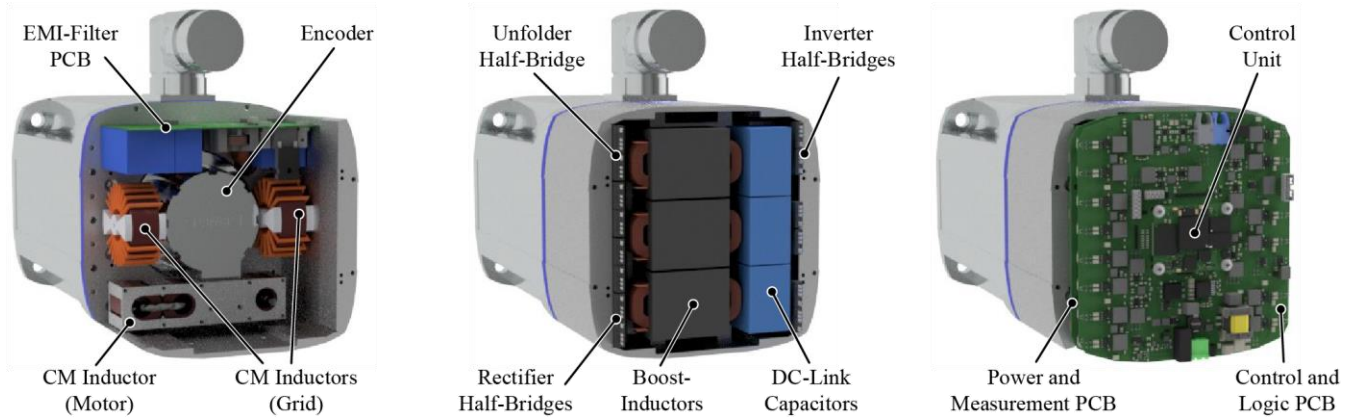


3 x 48 kHz 60 µF (Foil) 24 kHz

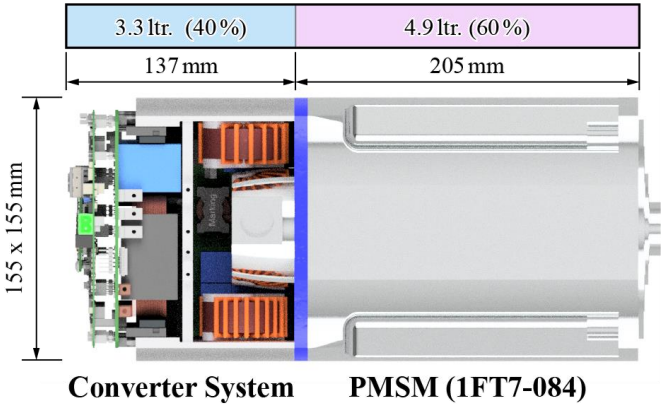
Losses: 703 W (91.4 %)



Motor Integration in Three Layers



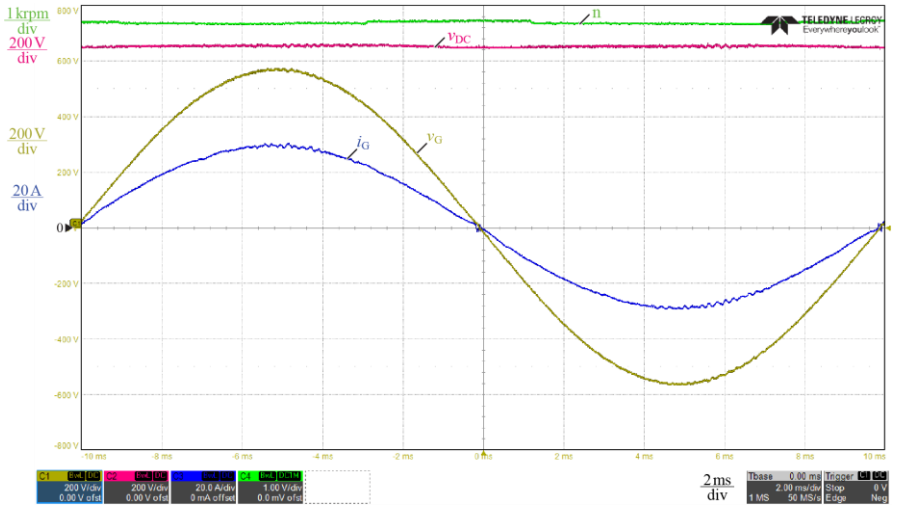
Volume: 8.2 ltr. (0.91 kW/ltr.)

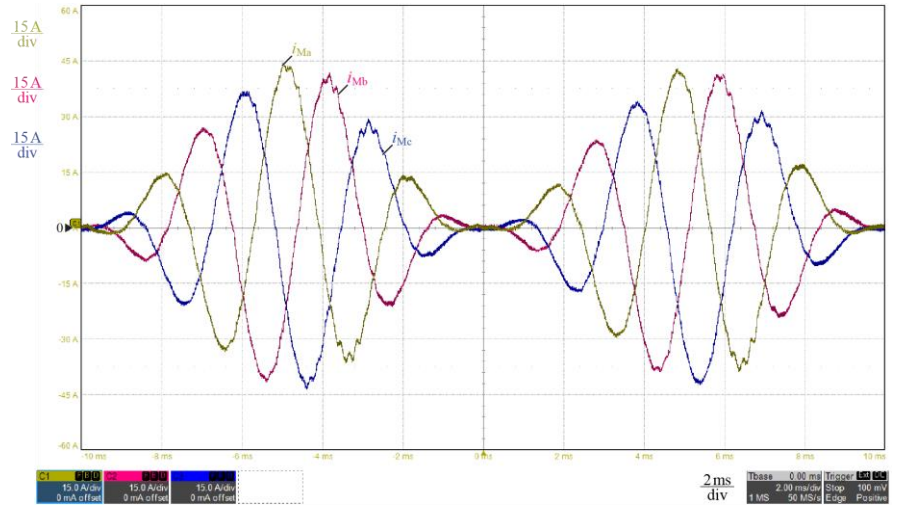


→ Drive System Performance: 0.91 kW/ltr. and 91.4 % @ 7.5 kW - IES2 Compliant

SI – Hardware Demonstrator

- Motor-Integrated Electrolytic-Less 1Φ AC-Supplied VSD System
- Time-Domain Waveforms at Nominal Operating Point
- Verification on Motor Test Bench (Specifically Developed)





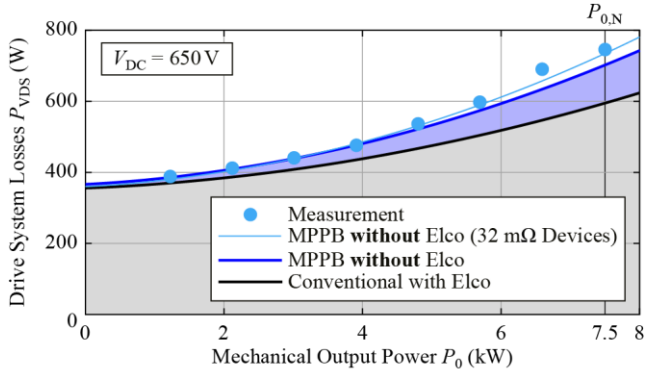
→ Demonstrator Matches Expected System Behavior

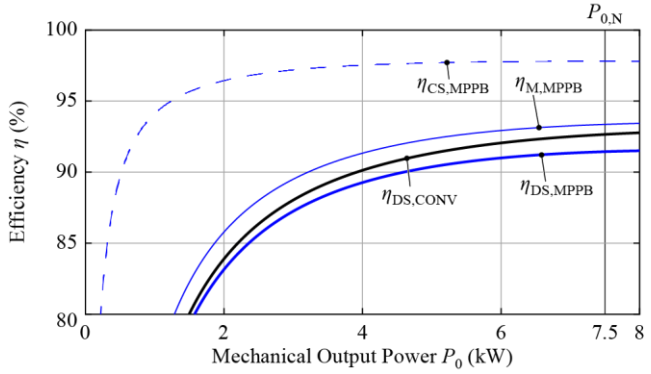
→ Verify Design Models

SI – Design Models

Loss Model

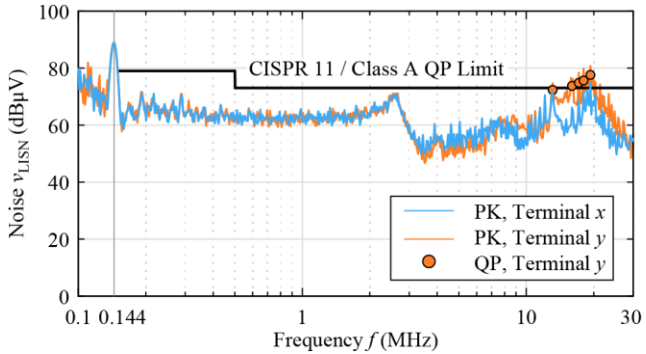
- Conventional System 600 W (92.6 %)
- Electrolytic-Less MPPB 703 W (91.4 %)
- Drive System Efficiency >90 % for P_0 > 5 kW

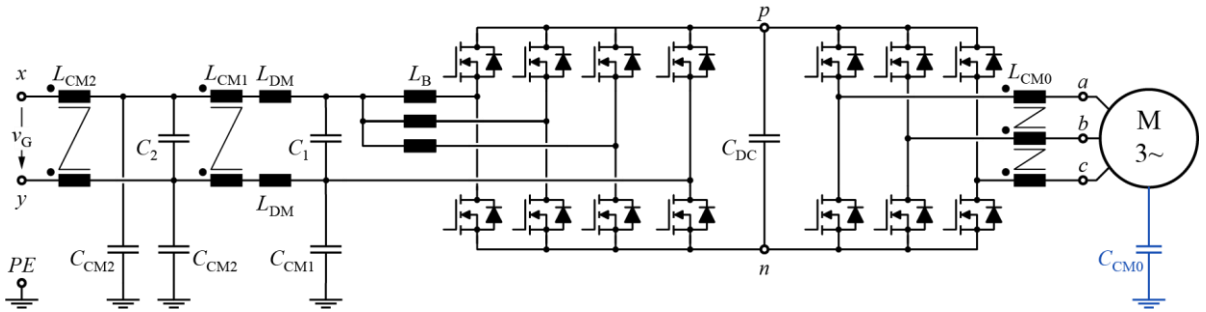




EMI-Model

- CISPR 11 / **Class A**
- DM-Noise: PFC Rectifier @ 288 kHz
- CM-Noise: Inverter @ 168 kHz

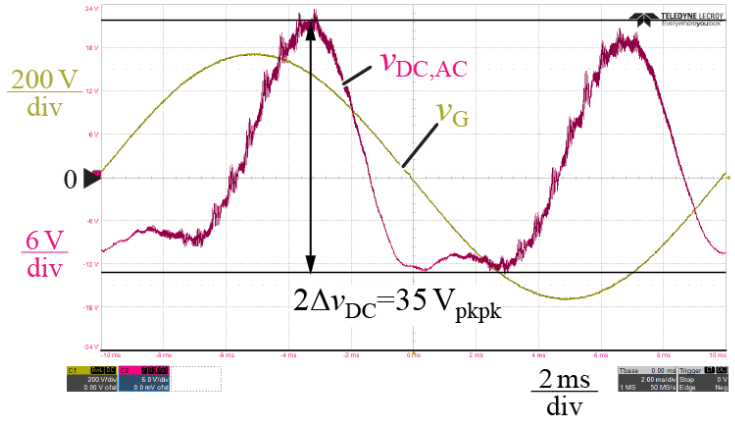




→ In-Depth Model Verification - 103 W of Additional Losses to Eliminate 1 ltr. of Electrolytic Capacitors

SI – DC-Link Voltage Ripple

- **LF DC-Link Voltage Fluctuations: 35 V**
  - Caused by Disturbances

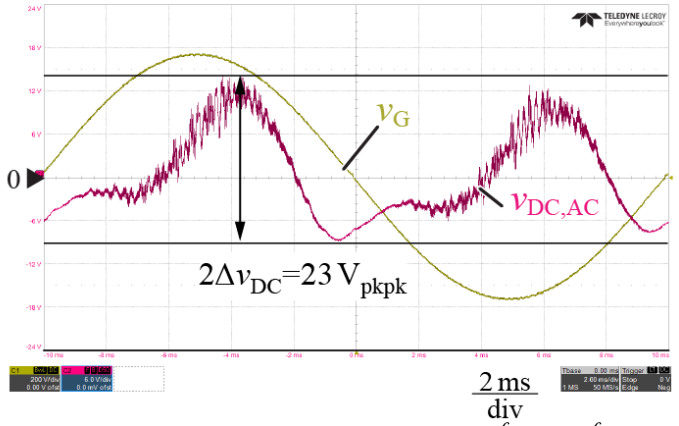


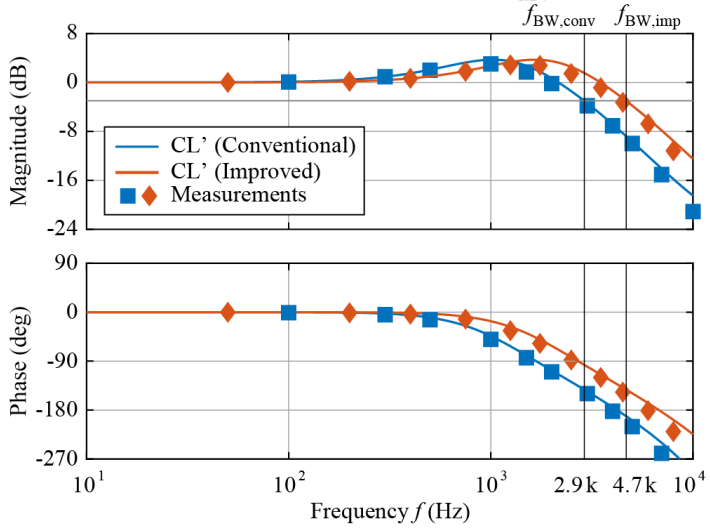
  - DC-Link Voltage Ripple matches Simulation
  - Increase C_{DC} = 60 µF
  - Increase f_{sw} = 24 kHz

→ **Efficiency, Power Density or Cost Penalty**

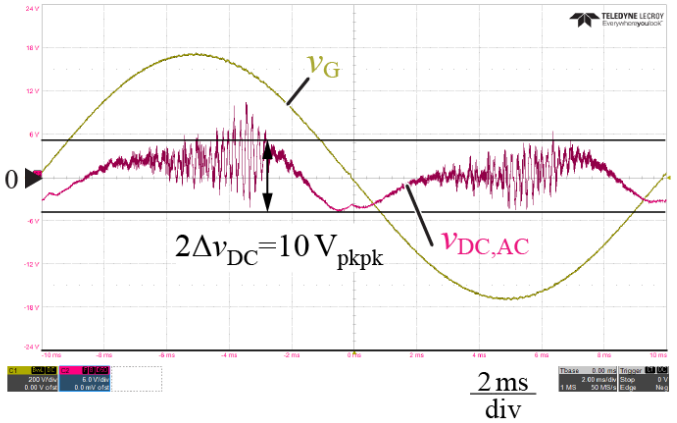
→ **Analyze Grid Interruption Sustainability**

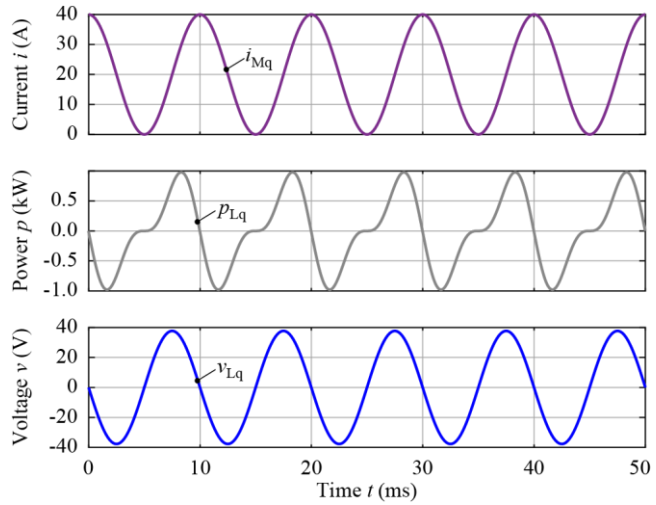
- **Delay Time Reduction: 23 V**
  - Improve Controller Bandwidth





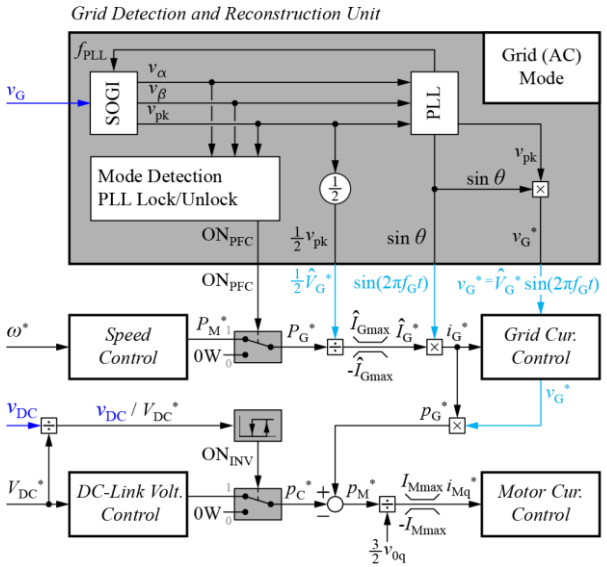
- **Feedforward Term: 10 V**
  - Counteract Motor Magnetization Power



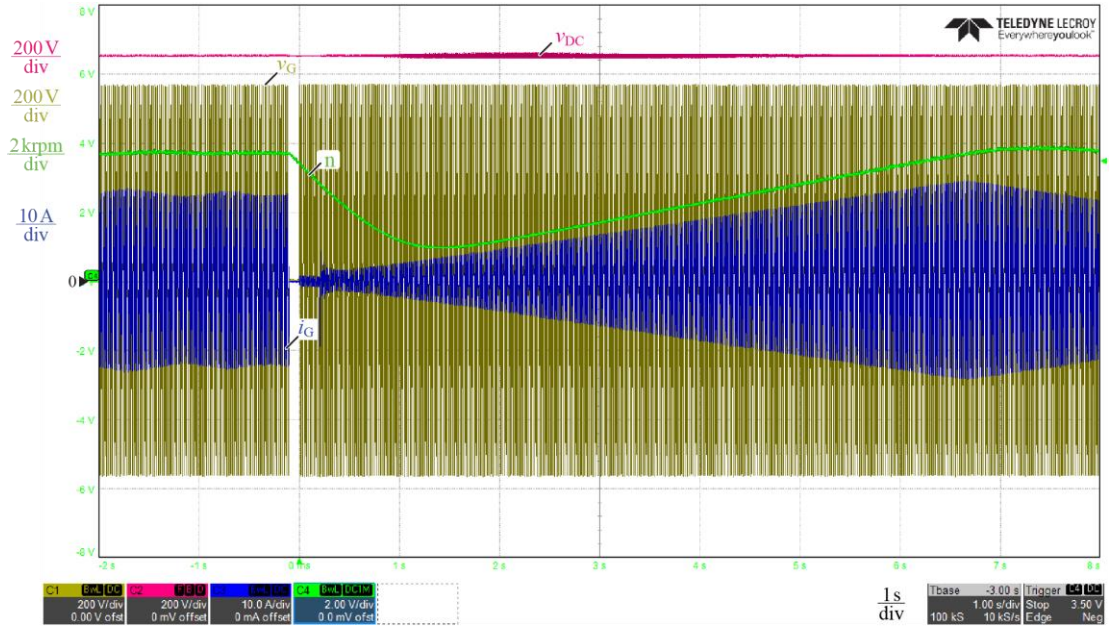


SI – Short-Term Grid Interruption

- Objective: Ridethrough keeps System Operational
- State-of-the-Art: Covered by DC-Link Energy Storage
- MPPB Concept: Lacks any Electrical Energy Storage
  - PFC Rectifier in Idle
  - Inverter Controls DC-Link Voltage (Recuperation)



- Verification: 100 ms Grid Interruption @ 4.3 kW
  - Load Torque «Discharges» Kinetic Energy Storage
  - Ramp-Up after PLL Synchronization

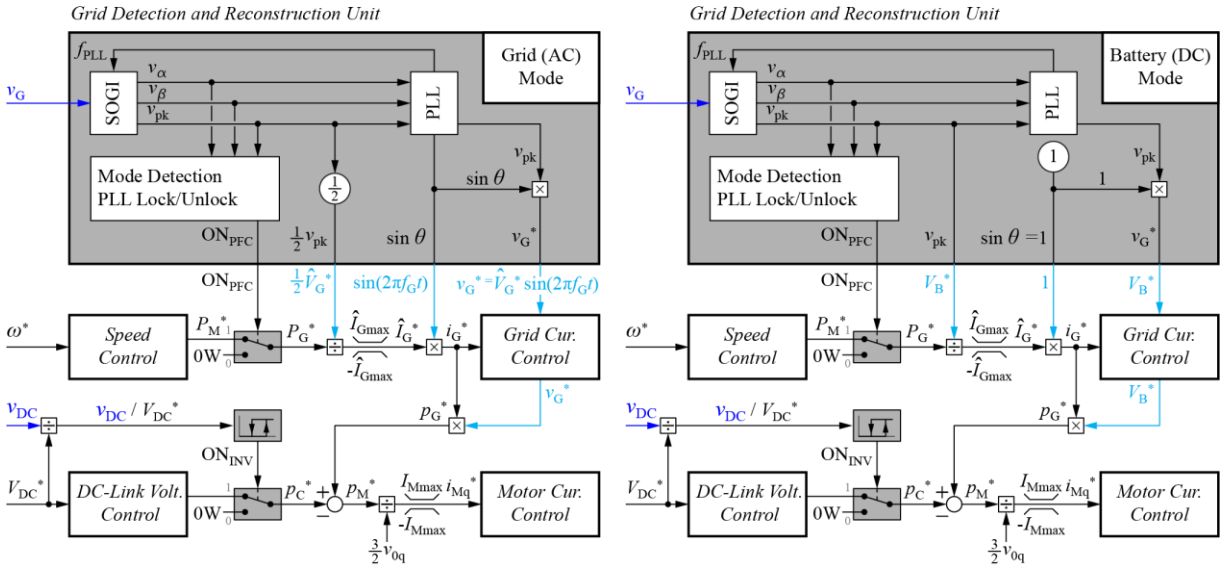


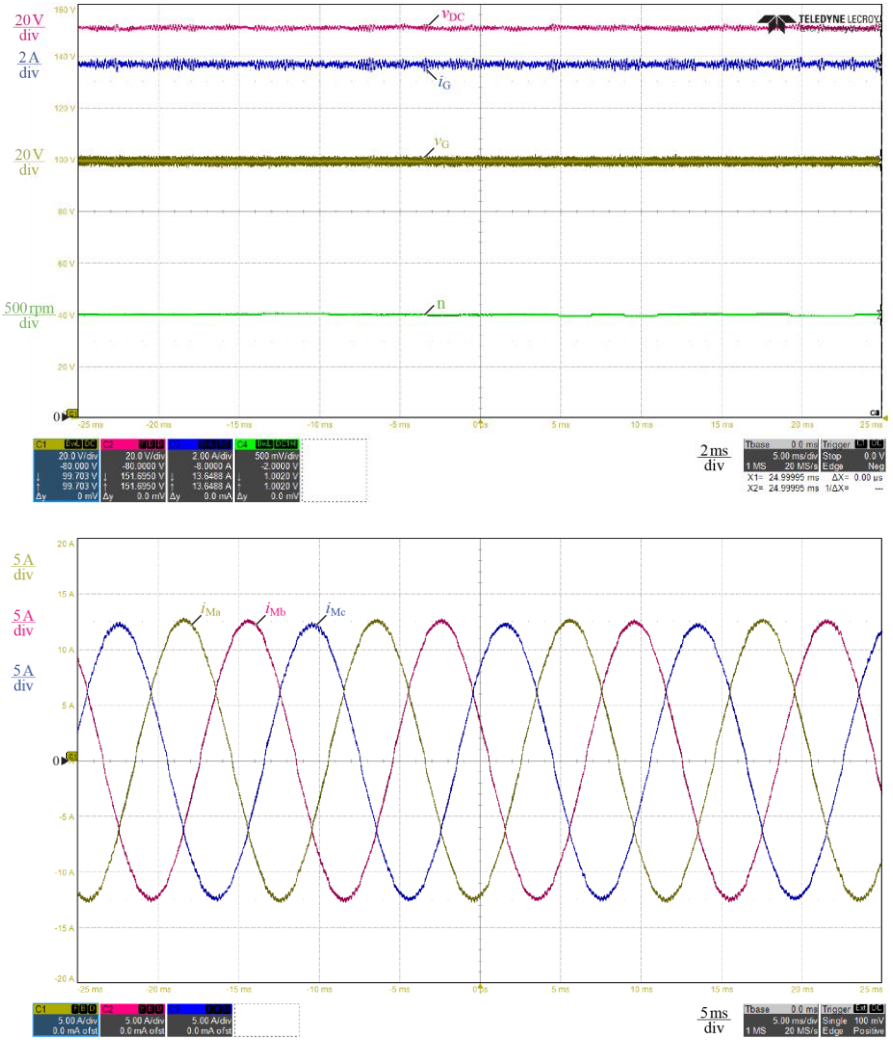
→ Not Suitable for Extended Grid Interruptions

SI – Long-Term Grid Interruption

- **Battery Operation**
- Traditional Approach would be Feasible
- Increased Software Development Effort
- Requires Active Switching between AC and DC Operation

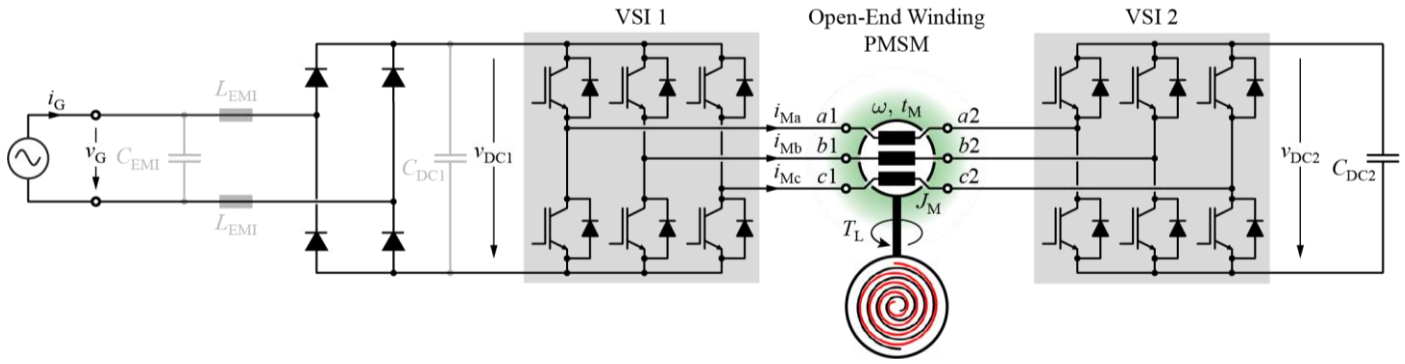
- **Employment of Identical Control Structure**
- Verification of DC-Operation at 1.2 kW @ 1000 rpm





→ Comprehensive Validation of the MPPB Concept

Part II
Dual-Inverter (DI) Topology



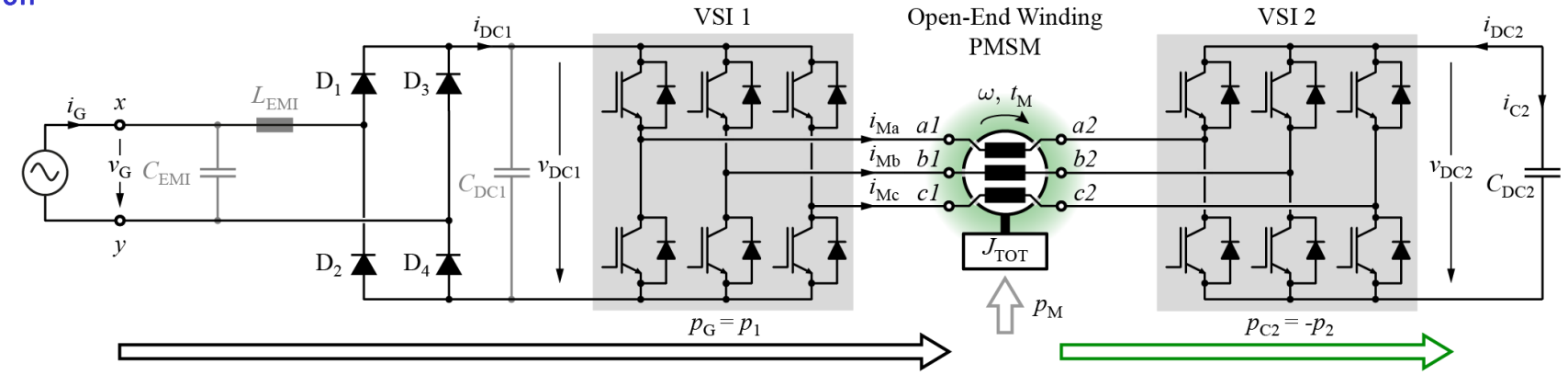
DI – Topology

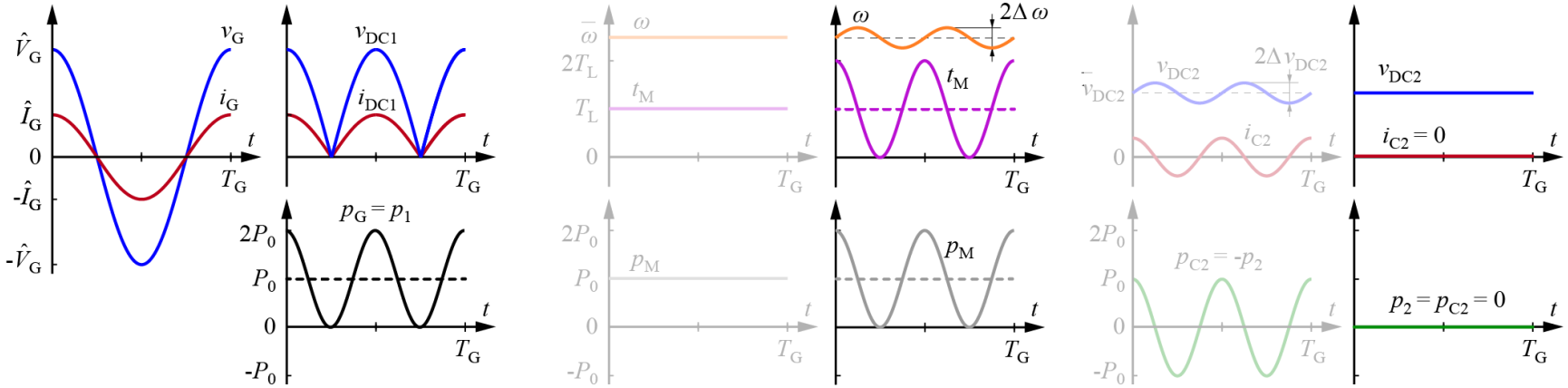
- **Dual-Inverter Implementation**

- **Avoids Boost Stage**
  - No Boost Inductor
  - No HF Bridge-Legs
  - Power Buffer Required

- **Apply MPPB Concept**
  - Electrolytic-Less

- **Implementation Effort**
  - Diodes
  - IGBT Six-Pack Modules
  - Film Capacitors
  - OEW PMSM



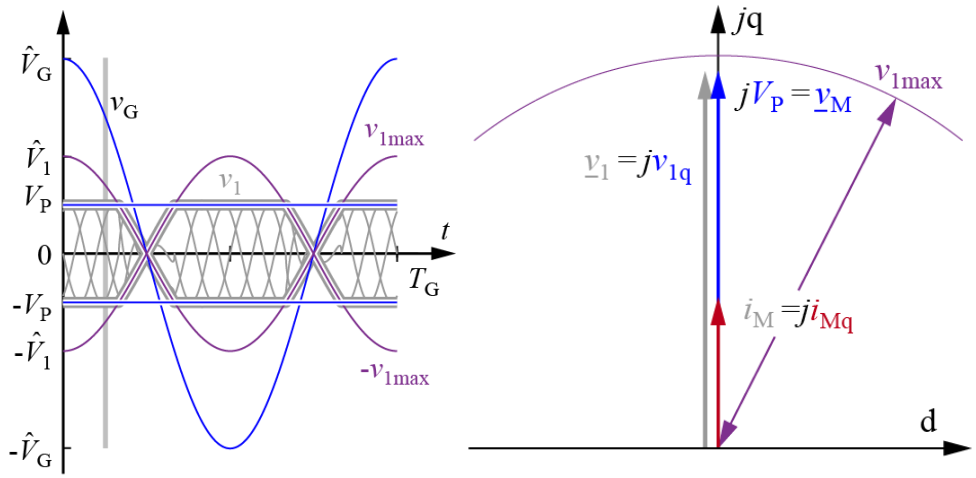


→ Investigate Operation to Ensure $p_2(t) = 0$ W

DI – Operation

- Ensure $p_2(t) = \underline{v}_2 \cdot \underline{i}_M = 0\ \mathrm{W}$ (Space Vector Representation)

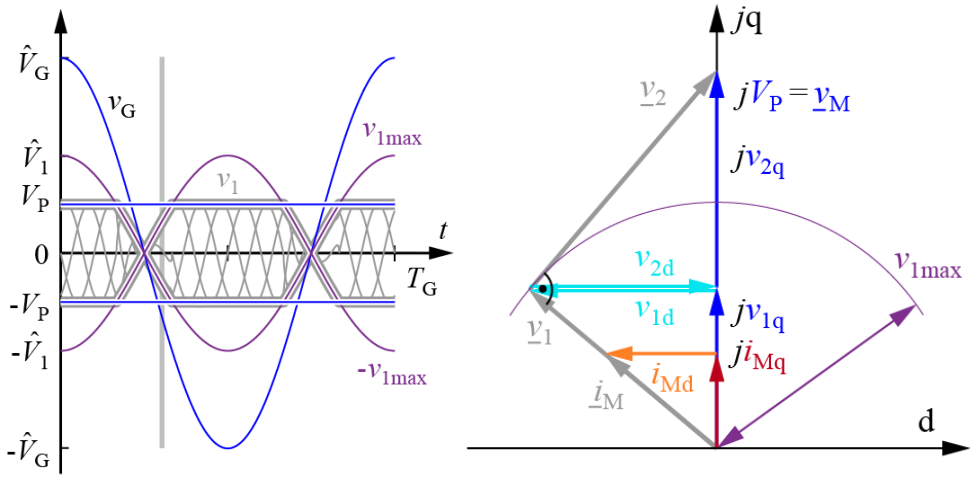
- Case I: $V_P < v_{1max}(t) = 0.5\, v_G(t)$
  - Ensure $v_2 = 0\ \mathrm{V}$ and $\underline{v}_1 = \mathrm{j}\, V_P$



- VSI 2 Provides No Voltage
- Zero d-Current Component

→ Performance Analysis

- Case II: $V_P \geq v_{1max}(t) = 0.5\, v_G(t)$
  - Ensure $\underline{v}_2 \perp \underline{i}_M$ and $\underline{v}_1 = \mathrm{j}\, V_P - \underline{v}_2$



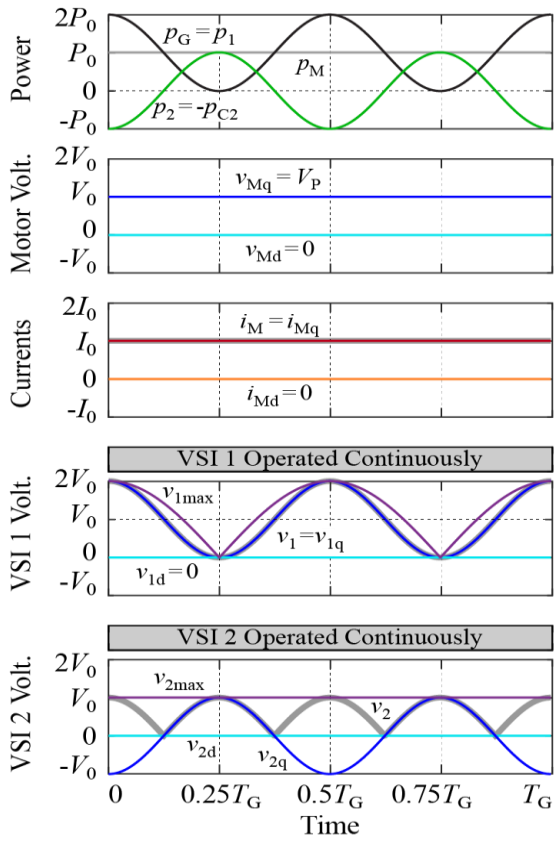
→ Select $|\underline{v}_1| = v_{1max}$ and $\underline{v}_1 \parallel \underline{i}_M$

- VSI 2 Provides Required Voltage Difference but No Active Power
- Non-Zero d-Current Component

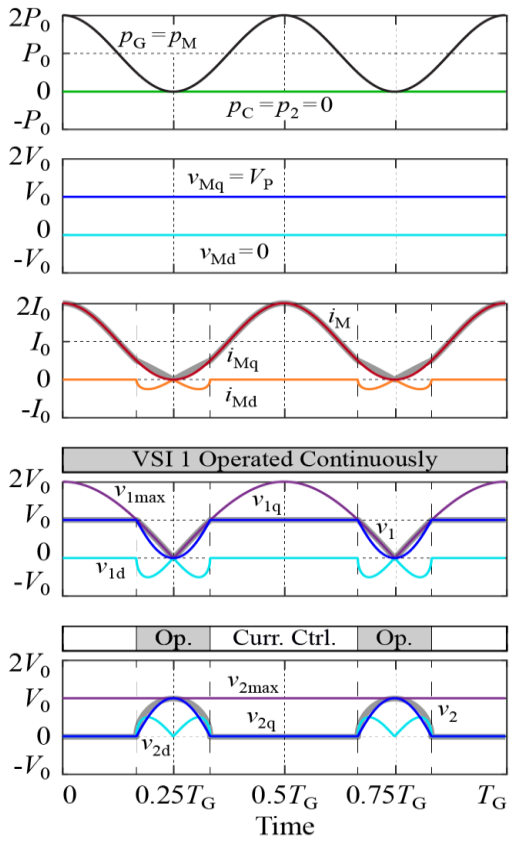
DI – Phase Current Stress

For V_{Gmin} = 360 Vrms

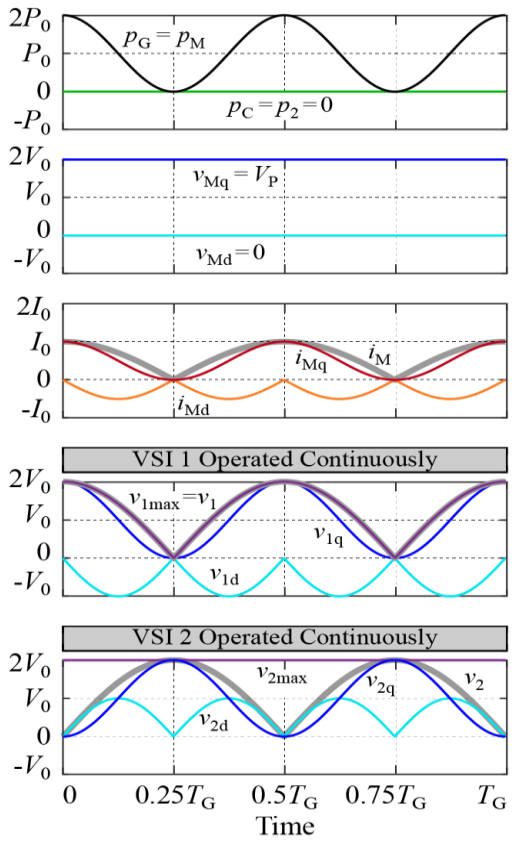
- Implementation **With Electrolytic Capacitors**
- For $V_P = V_0$ = 125 V - **Grid Voltage Limit**
- I_{PH0rms} = 33 A



- **Electrolytic-Less MPPB Implementation**
- For $V_P = V_0$ = 125 V
- I_{PHrms} = 41 A

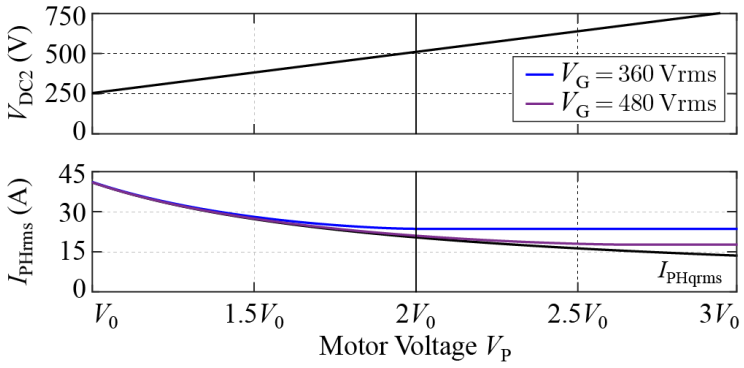


- **Electrolytic-Less MPPB Implementation**
- For $V_P = 2V_0$ = 250 V
- I_{PHrms} = 24 A



DI – Performance Evaluation

- Degree of Freedom: Motor Voltage V_P
- Influence on
  - Secondary DC-Link Voltage V_{DC2}
  - Phase Current Stress I_{PHrms}



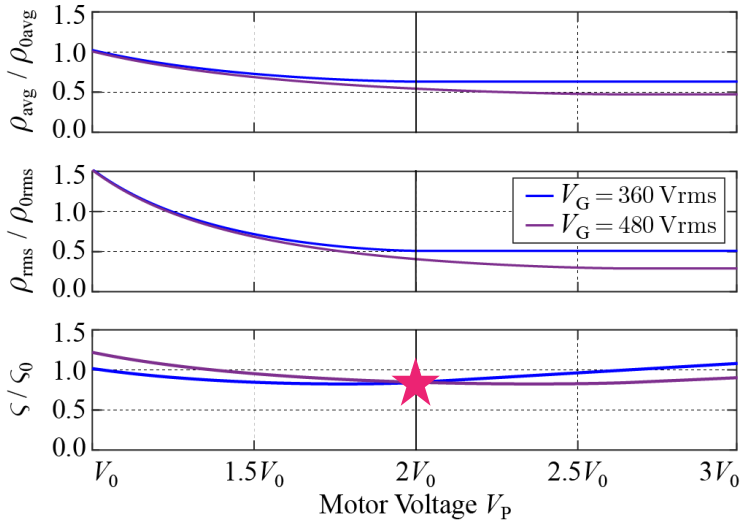
- Performance Indices
  - Conduction Losses

$$\rho_{avg} = \sum_k \left(I_{Davg,k} + I_{Tavg,k} \right)$$

$$\rho_{rms} = \sum_k \left(I^2_{Drms,k} + I^2_{Trms,k} \right)$$

  - Switching Losses

$$\varsigma = \sum_k \left\langle v_{T,k} + i_{T,k} \right\rangle_{T_G}$$



- System Specifications

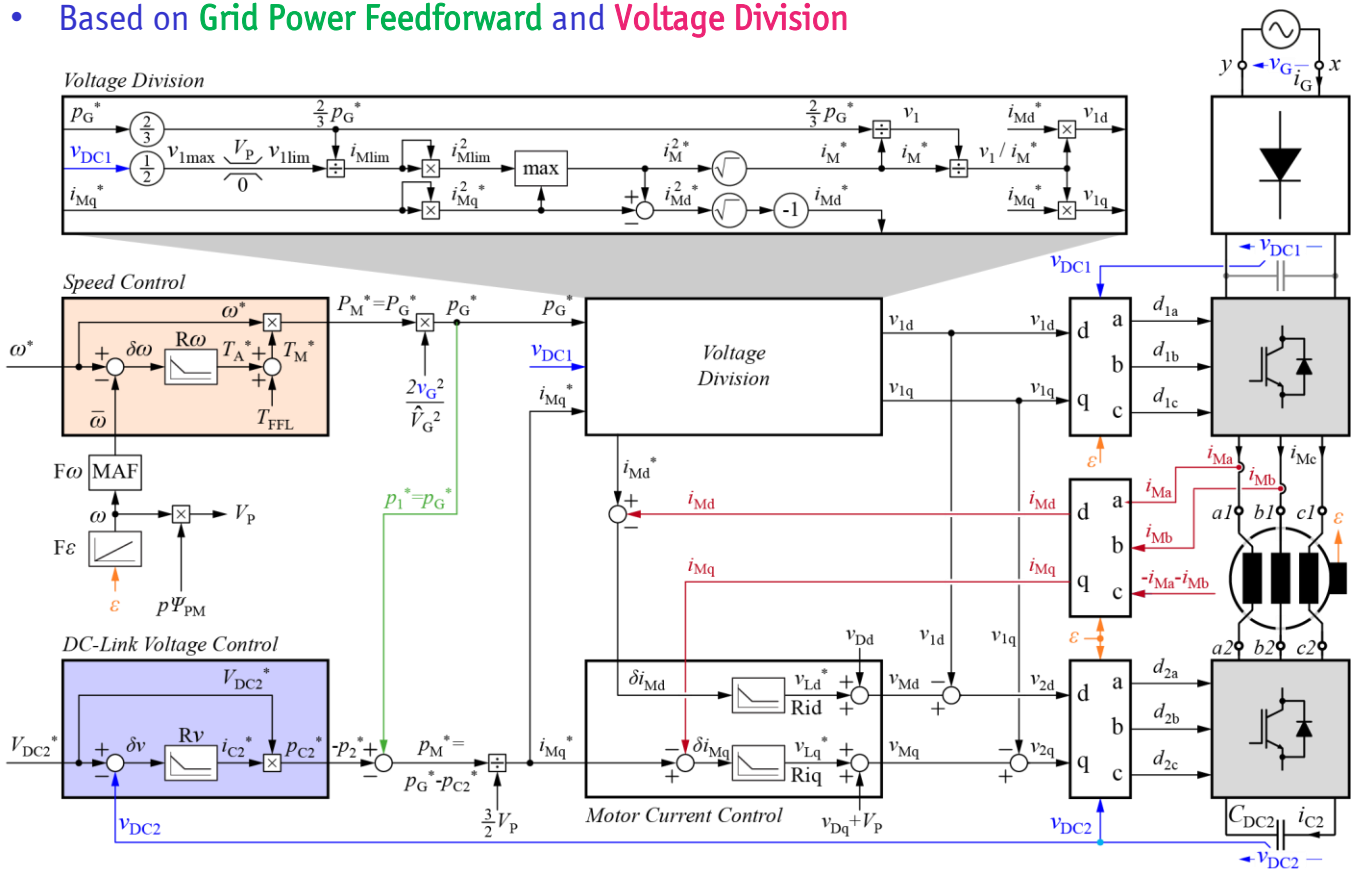
Mech. Output Power	7.5 kW
Mech. Speed	3700 rpm
Grid Voltage	360...480 Vrms
Grid Frequency	50 Hz
Switching Frequency	16 kHz

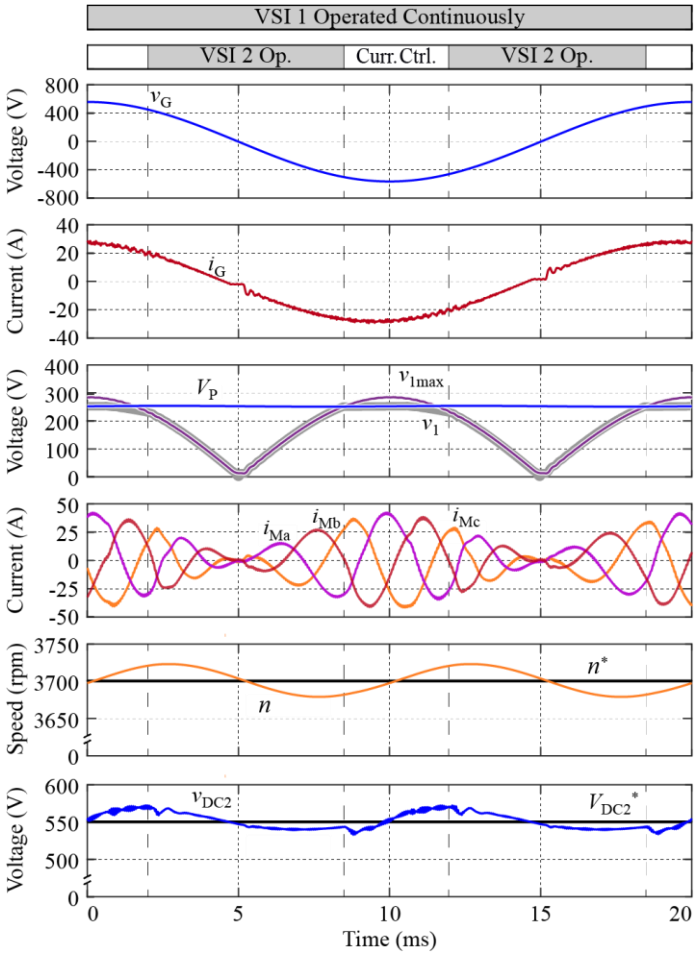
- Normalized to State-of-the-Art (with Electrolytic Capacitor)
  - AVG Conduction Losses: -45 %
  - RMS Conduction Losses: -45 %
  - Switching Losses: -15 %

→ Semiconductor Loss Reduction up to 30 % @ $V_P = 2V_0$

DI – Control

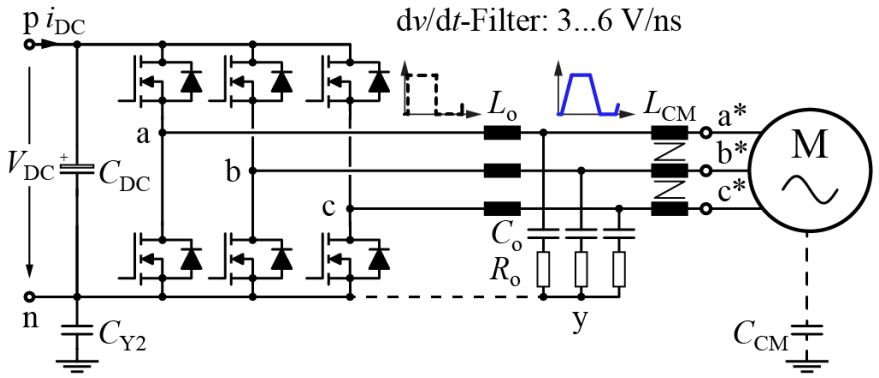
- **Control Objectives: PFC Operation, DC-Link Voltage and Average Speed Control**
- Implemented in Cascaded Fashion
- Based on Grid Power Feedforward and Voltage Division





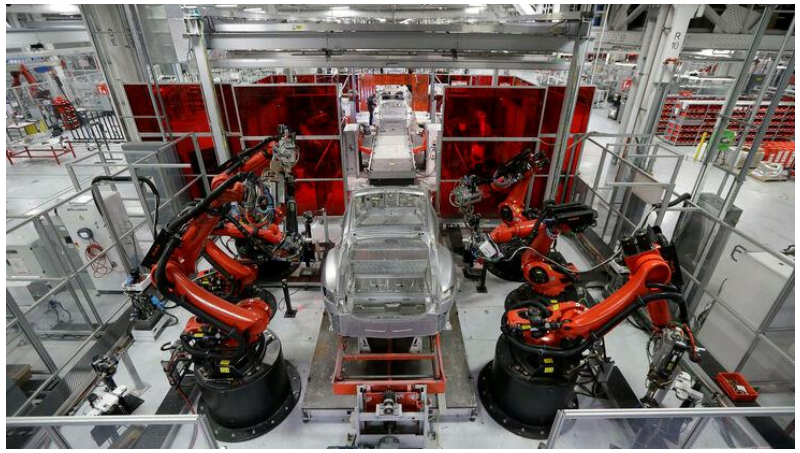
→ Verified by Circuit Simulation for $C_{DC2} = 50\ \mu F$ - only $6.7\ \mu F/kW$

Part III
dv/dt-Limited PWM-Based VSD Systems



Variable Speed Drive (VSD) Systems

Source: Tesla



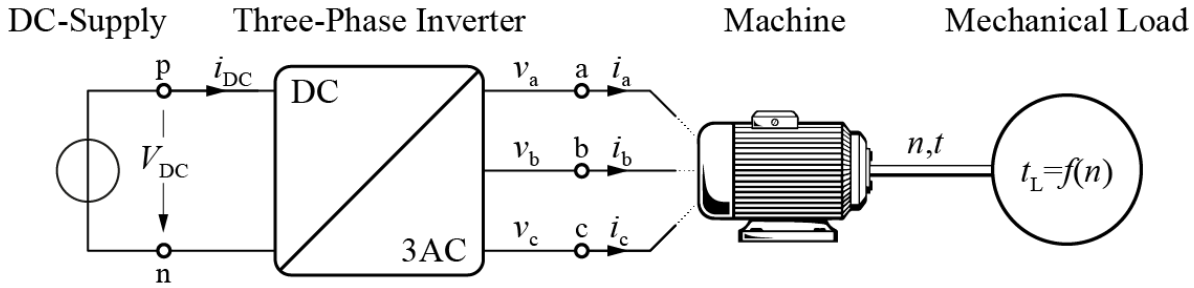
Application Fields

- Industry Automation / Robotics
- Material Machining / Processing
- Pumps / Fans / **Compressors**
- Transportation
- Etc.

→ Account for **60 % of Electrical Energy Consumed in Industry**

Common Specifications

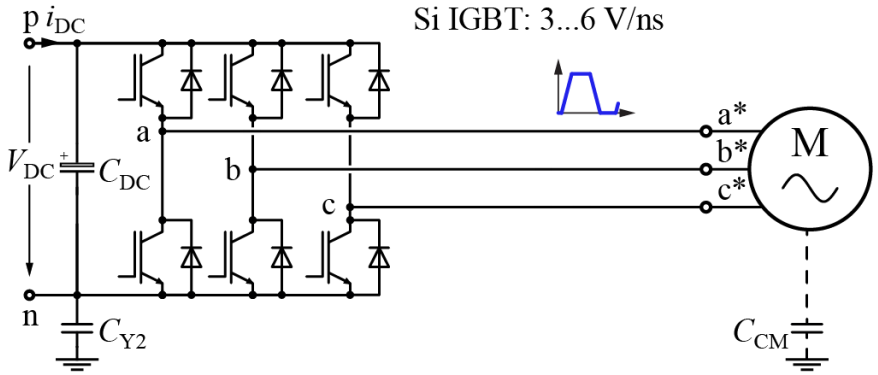
DC-Link Voltage	600…**800 V**
Power Range	1…**10 kW**
Switching Frequency	4…**16 kHz**
Semiconductor Technology	Si IGBT + Diode

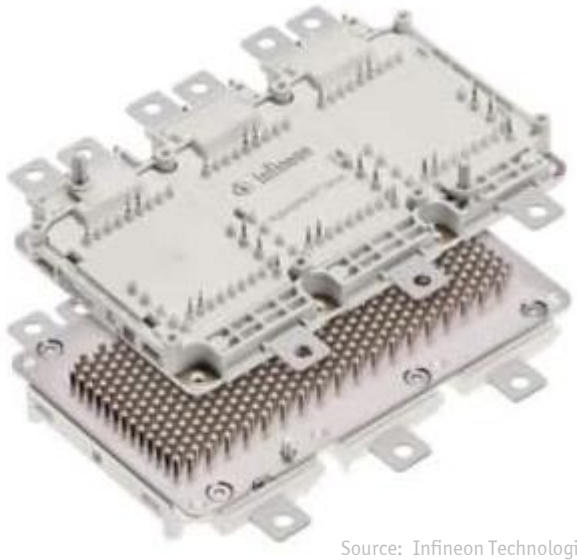


→ **Si IGBT: Limited Performance in Efficiency and Power Density!**

State-of-the-Art IGBT Inverter

- Si IGBT with Antiparallel Diodes (1.2 kV)

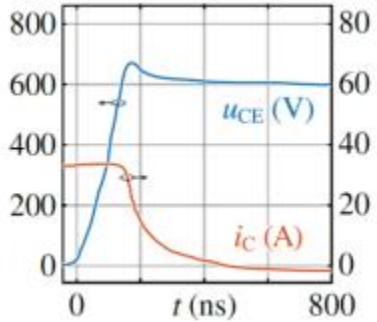




Source: Infineon Technologies

- Performance Characterization
  - Si IGBT with Si/SiC Diode
  - Bidirectional On-state Voltage Drop
  - Low Switching Speed

Large Chip Area
High Conduction Losses
High Switching Losses

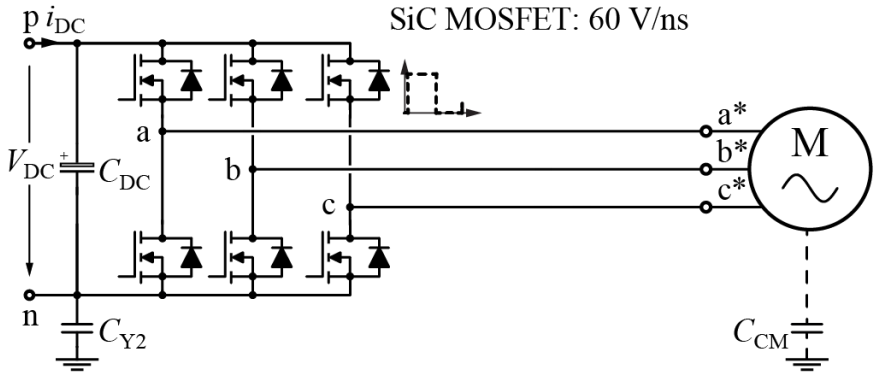


Source: Fuji

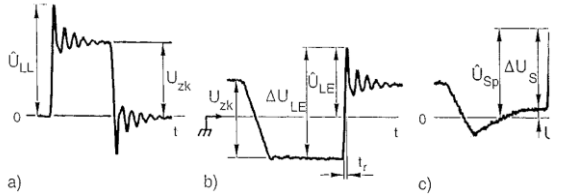
→ Performance Improvement with Silicon Carbide (SiC) ?

Next Generation SiC Inverter (1)

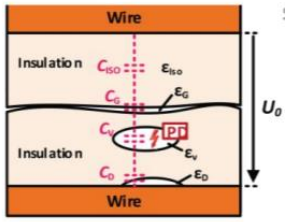
- SiC MOSFET with Internal Diodes (1.2 kV)



Voltage Spikes at Machine Terminals
(a) Line-to-Line Voltage
(b) Line-to-Earth Voltage
(c) Voltage Across First Coil



Source: Kaufhold et al /2000

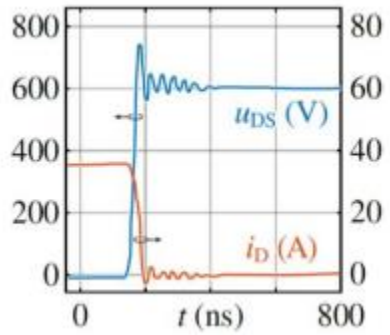


Source: Bakran / ECPE 2019

- Performance Characterization
- SiC MOSFET — Smaller Chip Area
- Low On-State Resistance — Lower Conduction Losses
- High Switching Speed — Lower Switching Losses

- High dv/dt at Machine Terminals — Partial Discharge Phenomena, Progressive Insulation Aging
- Increased EMI-Emissions — Radiated and Conducted

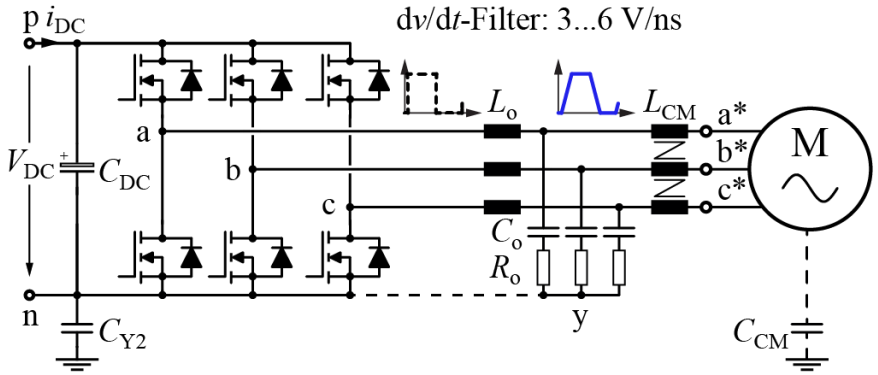
→ dv/dt Limitation Required!



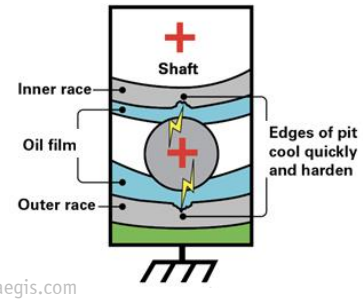
Source: Fuji

Next Generation SiC Inverter (2)

- SiC MOSFET with Internal Diodes (1.2 kV) with dv/dt-Limitation



CM Inductor LCM prevents
(a) CM-Current Spikes
(b) Bearing Currents:

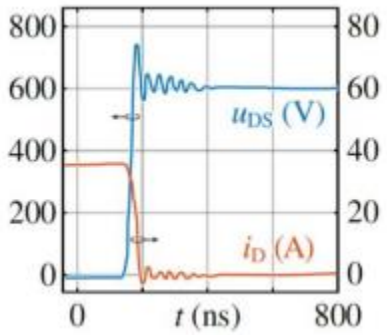


Source: www.est-aegis.com

- Performance Characterization
  - SiC MOSFET — Smaller Chip Area
  - Low On-State Resistance — Lower Conduction Losses
  - High Switching Speed — Lower Switching Losses

- Limited dv/dt at Machine Terminals — Prevent Partial Discharge Phenomena, Prevent Progressive Insulation Aging
- Reduced EMI-Emissions — Radiated and Conducted

→ Investigate dv/dt-Limitation Concepts



Source: Fuji

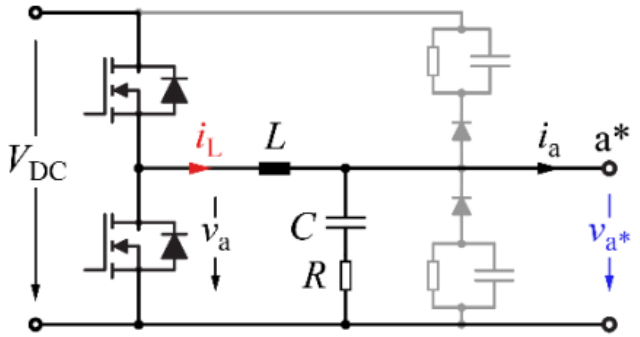
dv/dt-Limitation Comparison

Comparison of dv/dt-Limitation Techniques (1)

■ Passive Concept – Capacitive Losses

1.) LCR-Filter

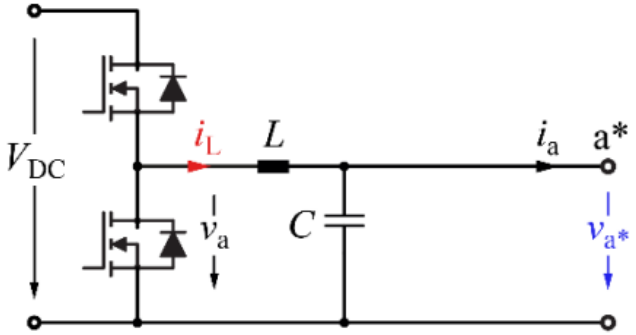
2.) Clamped LC-Filter



■ Hybrid Concept – Switching Losses (3 f_{sw})

1.) Two-Step Transition

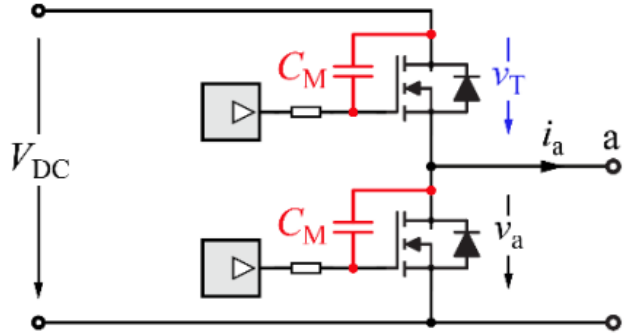
2.) Multi-Step Transition



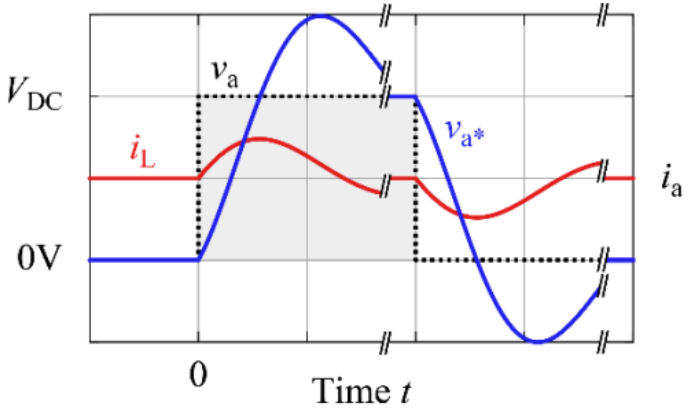
■ Active Concept – Overlap Losses

1.) Miller Capacitor C_M

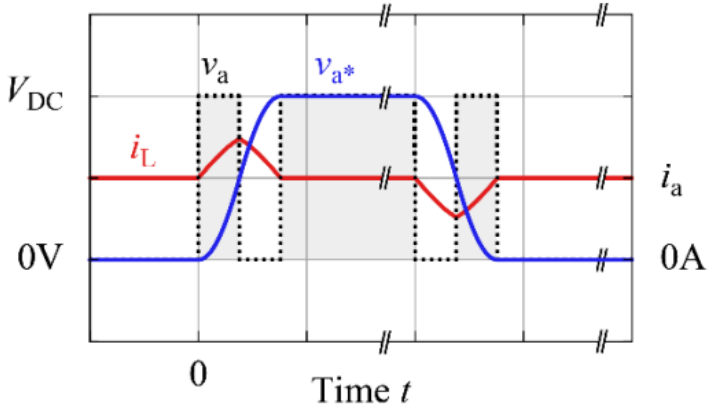
2.) Gate Current Control



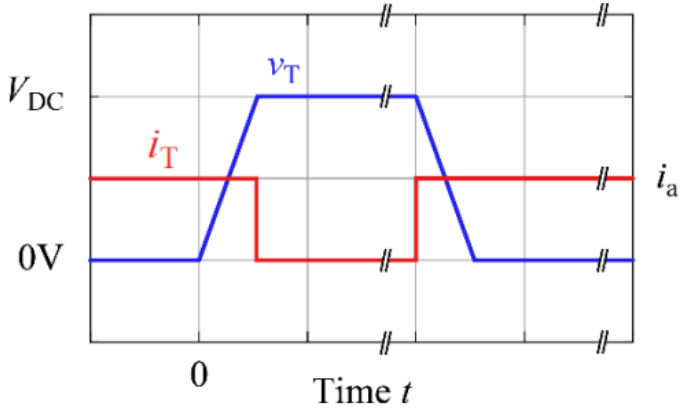
■ Output Voltage Waveforms – V_{DC} = 800 V, P_{out} = 10 kW, dv/dt = 6 V/ns



3.8 uH, 2.7 nF, 19Ω



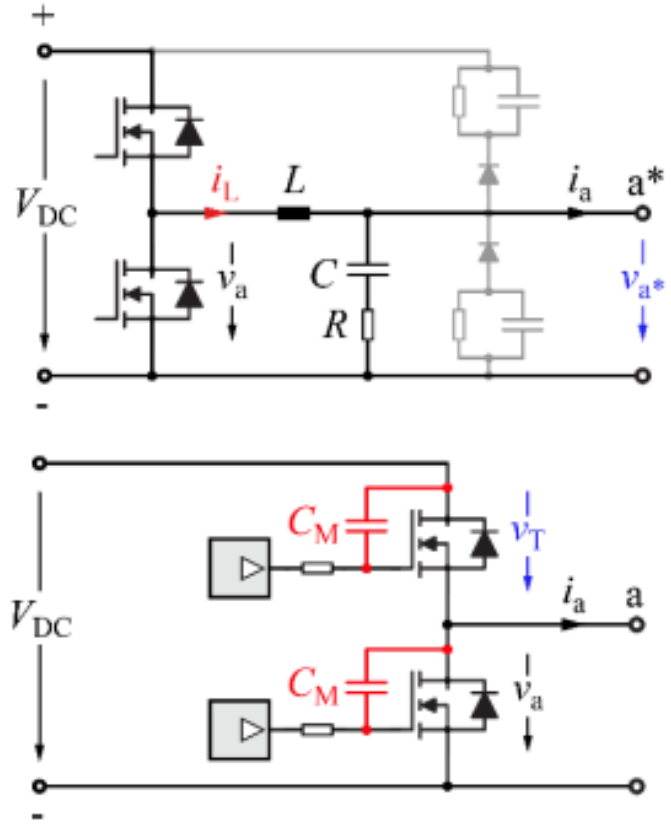
4.1 uH, 1.3 nF



50 pF

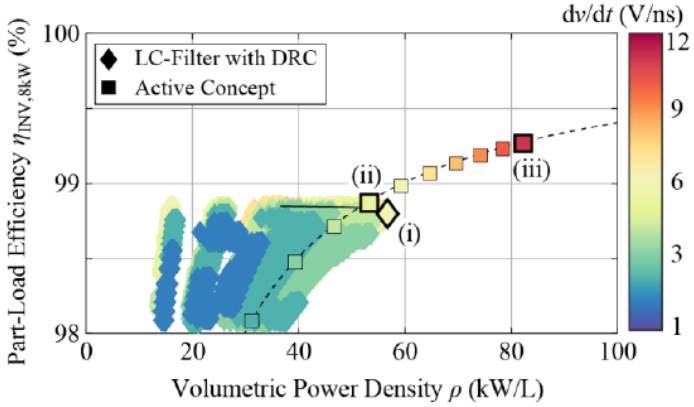
Comparison of dv/dt-Limitation Techniques (2)

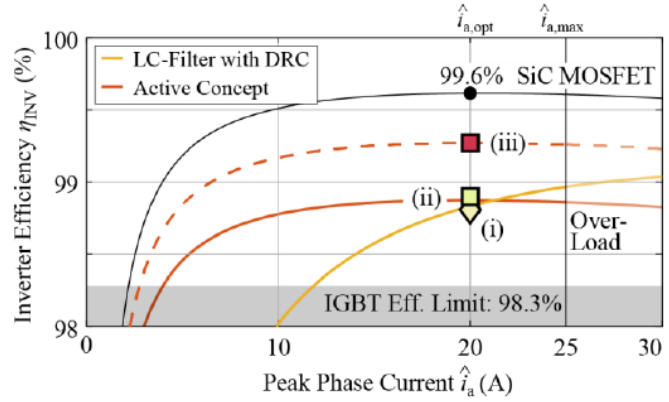
- Comparative Evaluation of Passive and Active Concept



→ Verify Results in the Lab!

- Specifications: V_{DC} = 800 V, P_{out} = 10 kW, f_{sw} = 16 kHz
  - 1.2 kV, 16 mΩ SiC-MOSFET with Kelvin-Soruce

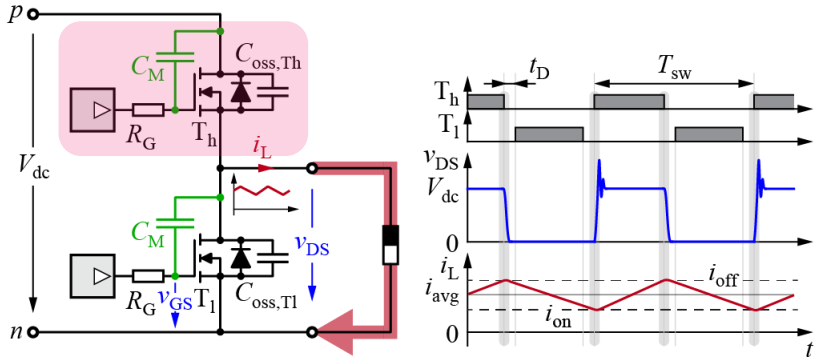




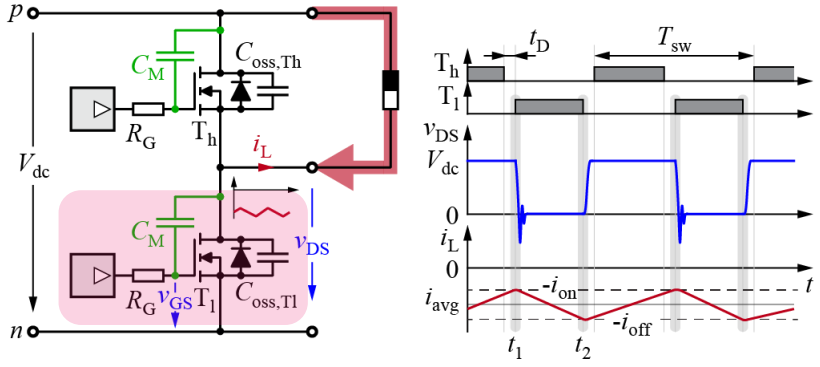
Miller Capacitor Based dv/dt-Limitation

MC – Employ External Miller Capacitor C_M

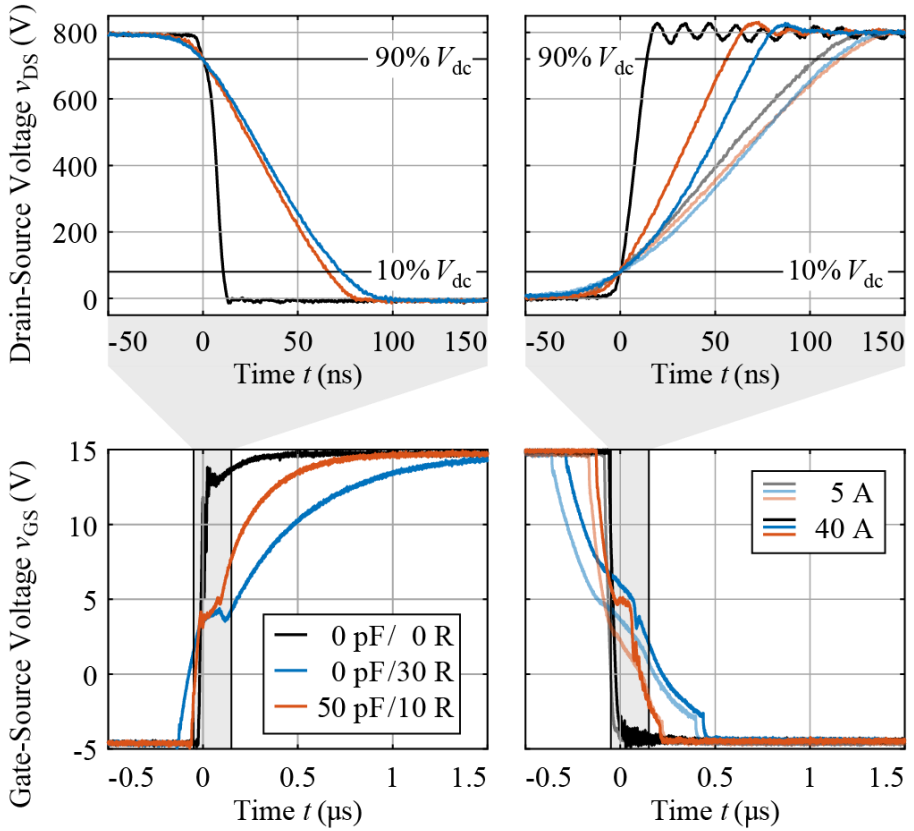
- Half-Bridge Switching Behavior
  - **Positive** Phase Current – **High Side Transistor** initiates Transitions



  - **Negative** Phase Current – **Low Side Transistor** initiates Transitions



- Voltage Transients: 1.2 kV / 16 mΩ 4-Pin SiC MOSFET (C3)
  - Turn-on
  - Turn-off



→ Slows down Switch-Node Voltage Transient – Negligible Effect on Gate Transient

MC – Current Dependency

Turn-on

- Voltage Slope Model

$$\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{on}} \approx \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{0}$$

Turn-off

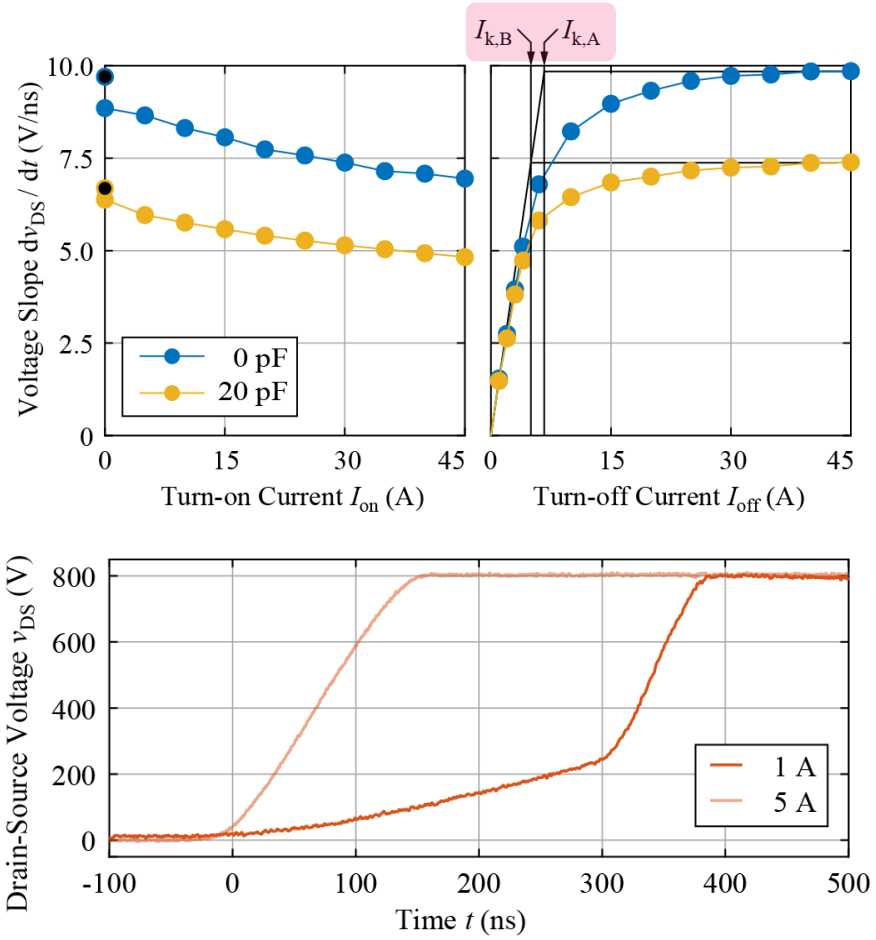
- Voltage Slope Model

$$\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{off}} \approx \begin{cases} \frac{I_{\mathrm{off}}}{I_{\mathrm{k}}} \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{0} & \text{if} \quad I_{\mathrm{off}} < I_{\mathrm{k}} \\ \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{0} & \text{if} \quad I_{\mathrm{off}} \geq I_{\mathrm{k}} \end{cases}$$

- With the **Kink Current** $I_{\mathrm{k}} = C_{\mathrm{eff}} \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{0}$

Turn-off @ Very Low Current

- Incomplete ZVS
- Inherently Covered
- dv/dt-Limitation Still met



Component Effort

- TO 247-4
- Gate Driver
- Miller Capacitor (pF)
- Gate Resistor

→ Negligible Capacitor Volume

→ Design Gate Drive for ZCS (Turn-on) and Maximum Turn-off Current

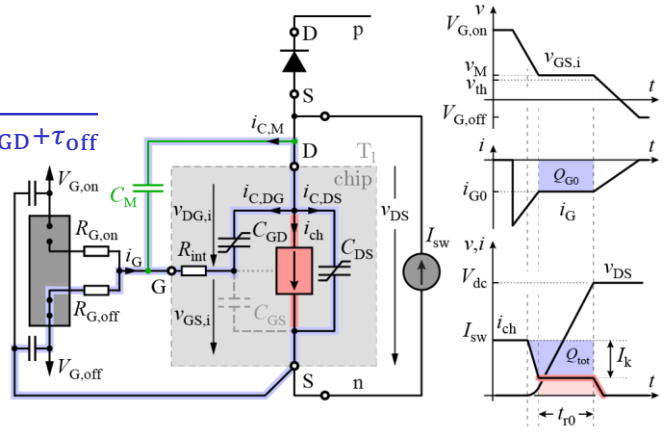
MC – Voltage Slope Model

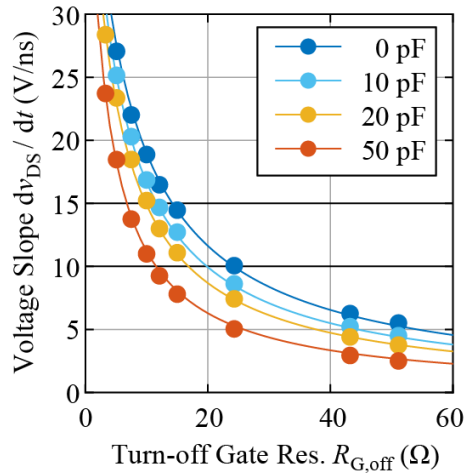
- **Turn-Off @ 45 A** with $R_{G,off}$ and C_M

$$\left.\frac{dv_{DS}}{dt}\right|_{off} = \frac{v_M - v_{G,off}}{R_{G,off}C_M + R_{G,off}C_{GD} + R_{int}C_{GD} + \tau_{off}}$$

- Miller Voltage v_M
- Sweep $R_{G,off}$ and C_M

→ Model match Measurement



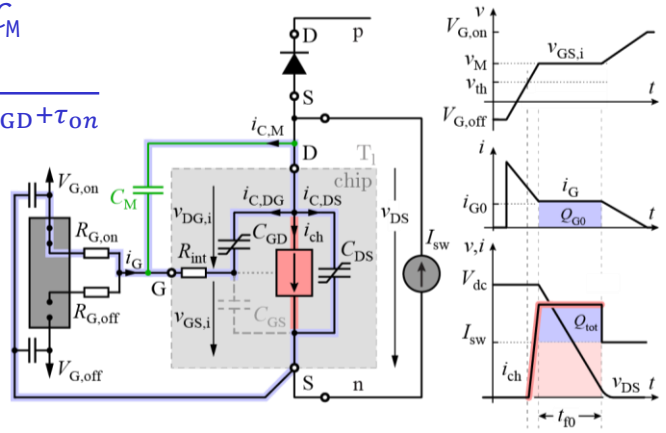


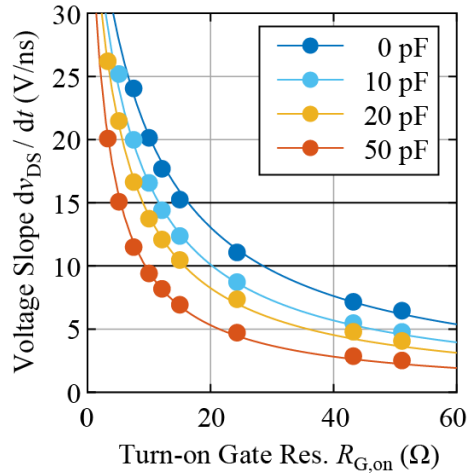
- **Turn-On @ 0 A (ZCS)** with $R_{G,on}$ and C_M

$$\left.\frac{dv_{DS}}{dt}\right|_{on} = \frac{v_{G,on} - v_{th}}{R_{G,on}C_M + R_{G,on}C_{GD} + R_{int}C_{GD} + \tau_{on}}$$

- Threshold Voltage v_{th}
- Sweep $R_{G,on}$ and C_M

→ Model match Measurement





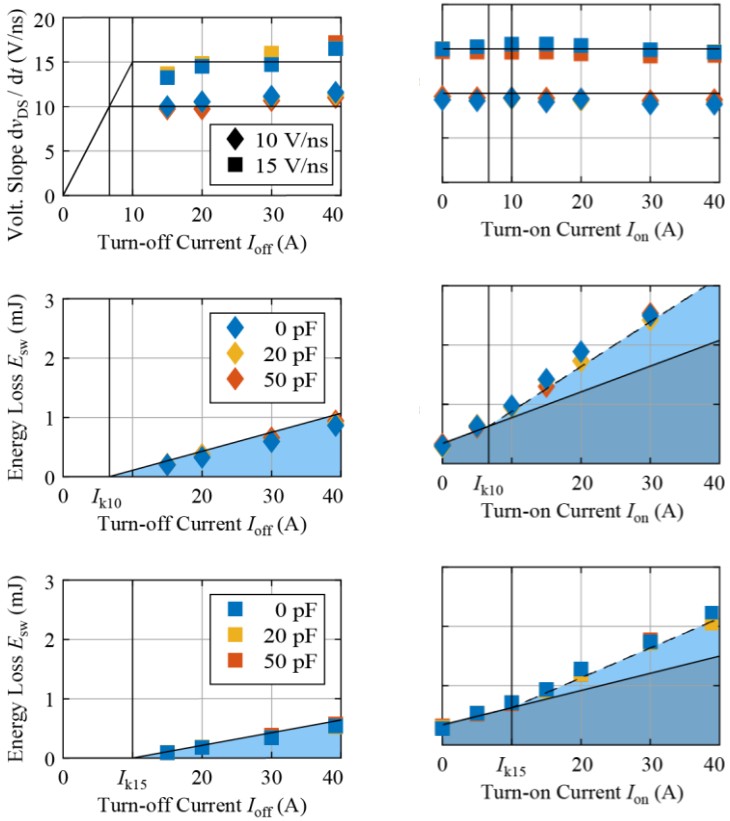
→ **Voltage Slope Limit depend only on Gate Drive**

→ **Switching Loss Dependency on Gate Drive Configuration?**

MC – Loss Model and Verification

Loss Measurements

- Turn-off
- Turn-on



→ Excellent Matching and Superior Performance

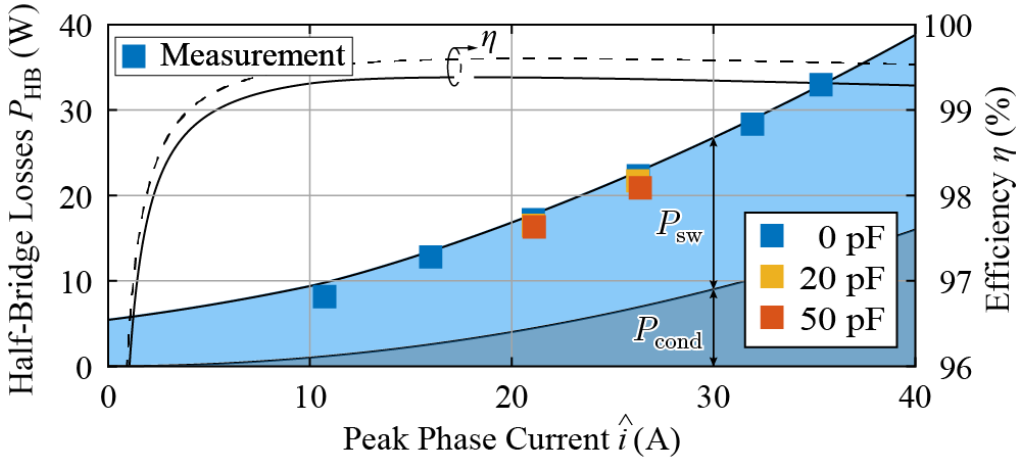
Switching Losses in CCM Operation – Piecewise Linear Loss Function

$$E_{sw}(I_{sw}) = \begin{cases} V_{DC}Q_{tot} + k_{on}I_{sw} & \text{if} \quad I_{sw} < I_k \\ V_{DC}Q_{tot} + k_{on}I_{sw} + k_{off}(I_{sw} - I_k) & \text{if} \quad I_{sw} \geq I_k \end{cases}$$

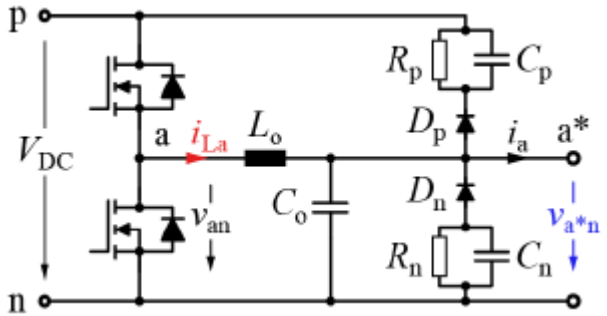
- With $k_{on} = \frac{1.35}{2} V_{DC}^2 \,/\, \left.\frac{dv_{DS}}{dt}\right|_0$ and $k_{on} = \frac{1}{2} V_{DC}^2 \,/\, \left.\frac{dv_{DS}}{dt}\right|_0$

Verification for Sinusoidal Phase Current @ 15 V/ns

- Inverter Efficiency: up to **99.4 %** @ f_{sw} = 16 kHz
- Loss Reduction of up to 8 % by Miller Capacitor (C_M = 50 pF)

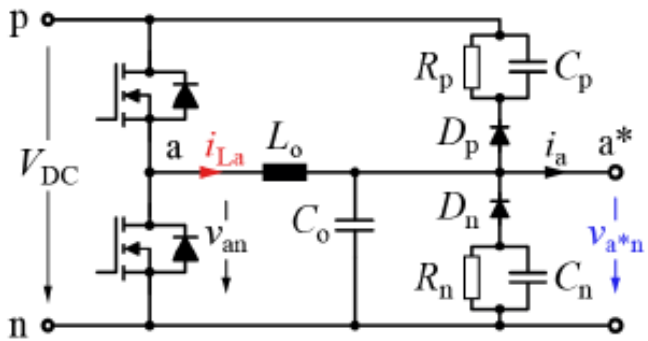


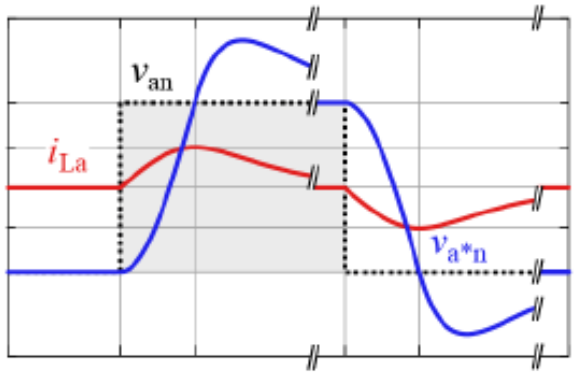
Passive Filter Based dv/dt-Limitation



PF – Theory

Topology and Waveforms



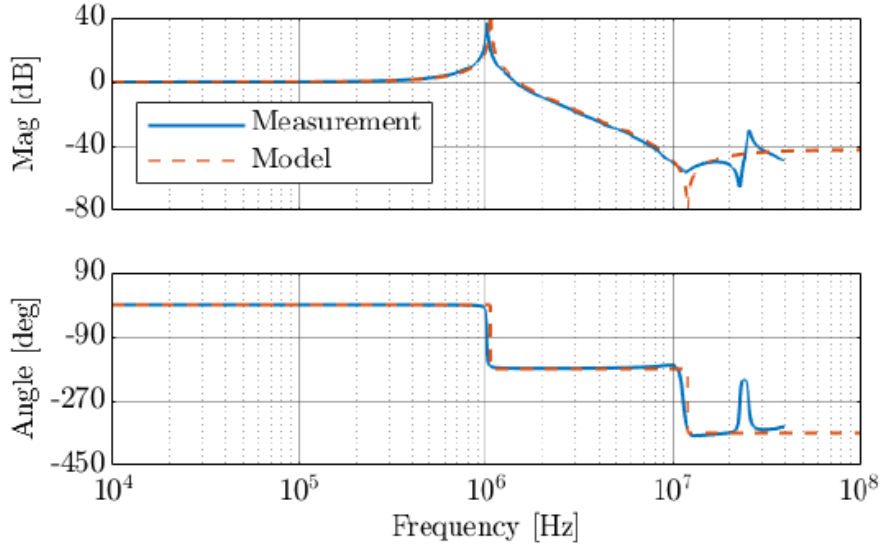


→ Implement in Hardware

Selected Components for 5 V/ns

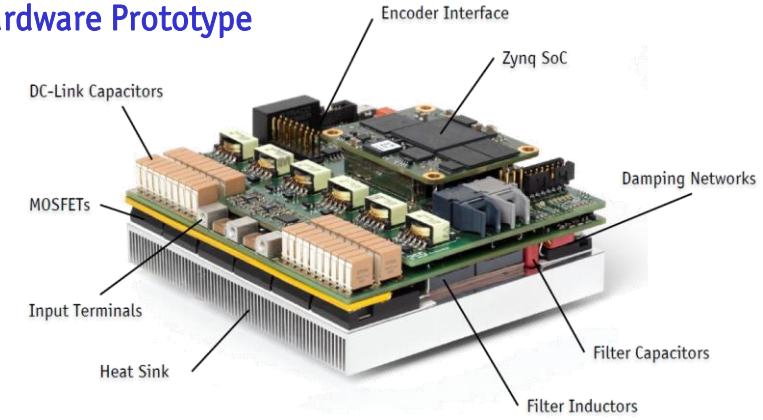
- Filter: L_o = 11.2 uH, C_o = 1.12 nF
- Damping Network: $R_p = R_n$ = 15 Ω, $C_p = C_n$ = 10 nF
- Transistor: 1.2 kV, 16 mΩ SiC-MOSFET with Kelvin-Soruce

Filter Transfer Function (Considering Winding Capacitance)



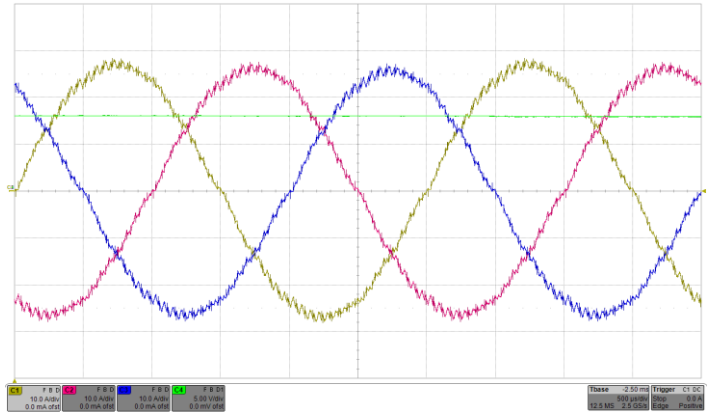
PF – Hardware and Measurement Results

Hardware Prototype

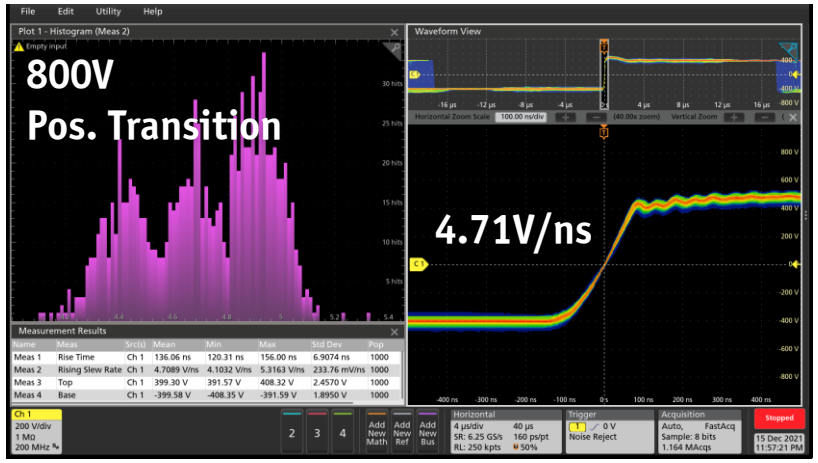


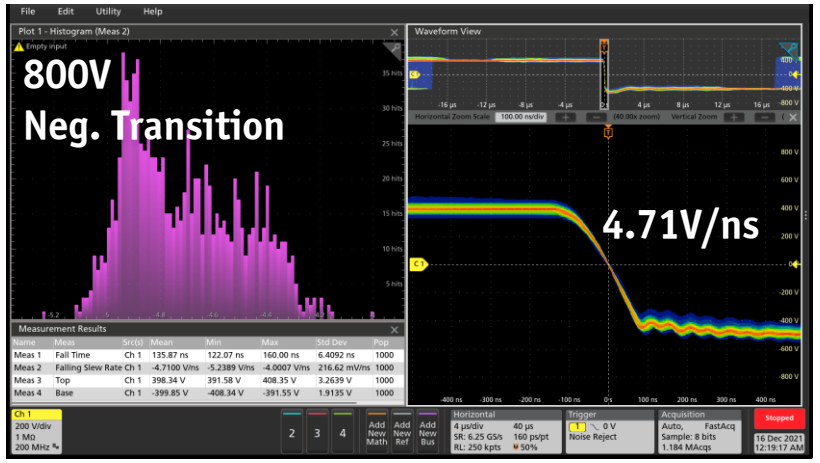
LxBxH = 10 x 9 x 3.9 cm → 28.5 kW/L and 99.0 %

Waveforms: Motor Currents @ 4 000 rpm, 25 Nm



Voltage Transition - Motor Terminal U vs. PE: < 5 V/ns due to Machine Capacitance





Results & Conclusions

Part I: Single-Inverter Topology

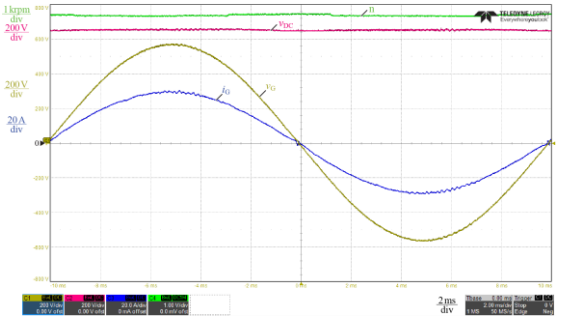
- **MPPB Concept**
  - Elim. Electrolytic Capacitors in 1Φ AC-Supplied VSD Systems
  - Performance Analysis: Motor and Inverter
- **Motor-Integrated Hardware Demonstrator**
  - Achieving 8 µF/kW within the DC-Link
  - Drive System Perf.: 0.91 kW/ltr. and 91.4 % @ 7.5 kW
  - In-Depth Validation

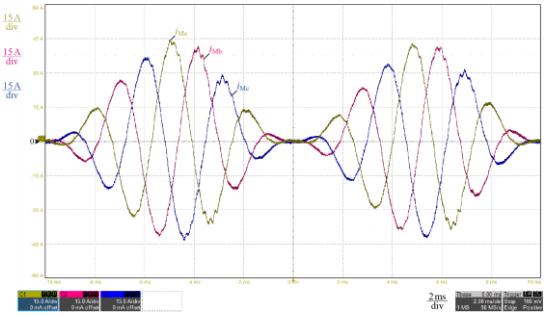
Part II: Dual-Inverter Topology

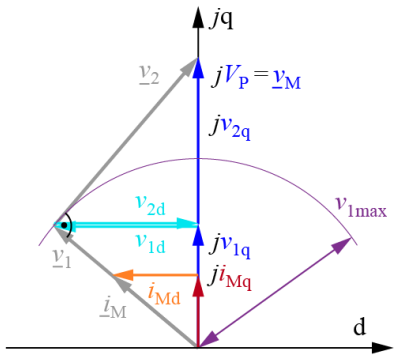
- **Dual-Inverter Employing the MPPB Concept**
  - Low Effort Implementation
  - Analysis of Operation and Control Structure
  - Semiconductor Loss Reduction of up 30 %

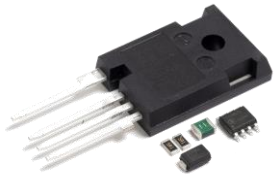
Part III: dv/dt-Limited PWM-Based VSD Systems

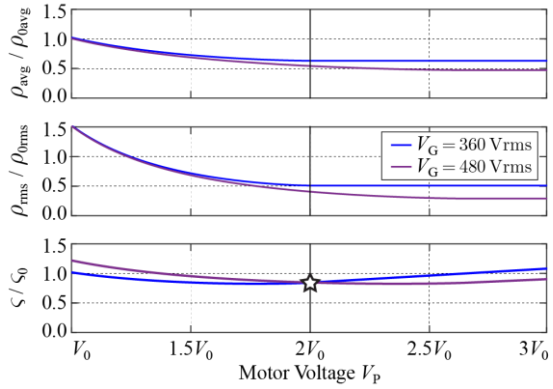
- **Miller Capacitor Based dv/dt-Limitation**
  - Protection of Motor Winding System
  - 99.4 % Inverter Eff. @ 15 V/ns and 16 kHz











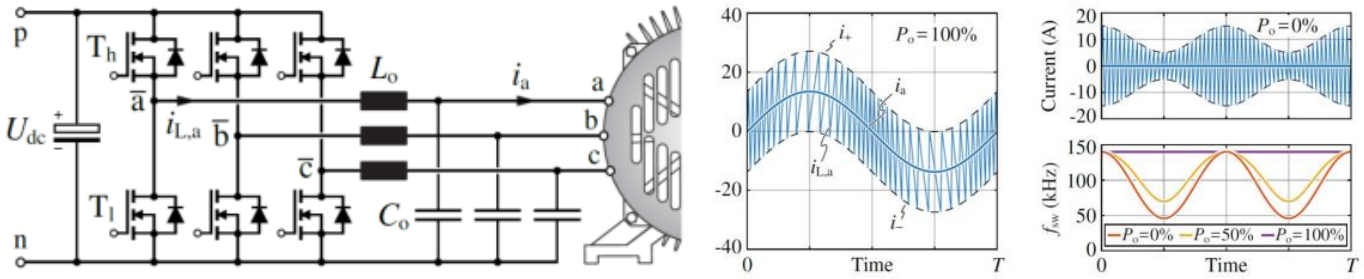
Outlook – Research Topics regarding VSD Concepts

1) Passive dv/dt-Filter

- Improved Performance at low dv/dt-Limits

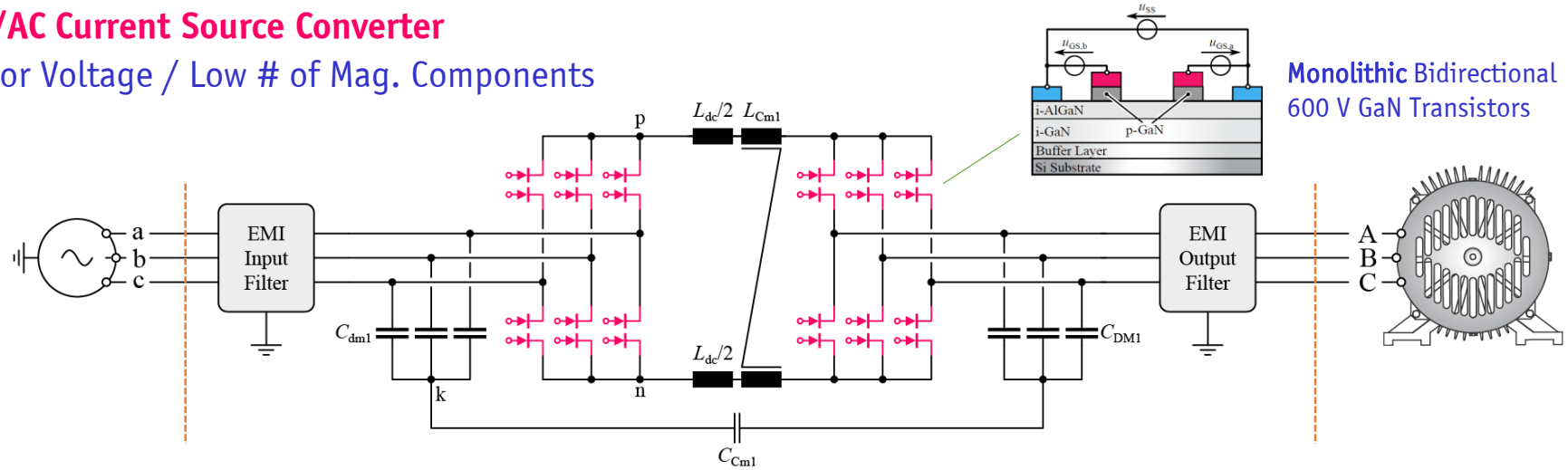
2) S-TCM Zero-Voltage-Switching Inverter

- Low Sw. Losses / Limited Sw. Freq. Variation / Sin. Motor Voltages



3) 3-Φ AC/AC Current Source Converter

- Sin. Motor Voltage / Low # of Mag. Components



Monolithic Bidirectional 600 V GaN Transistors

Same **EMC Requirements** at Grid and Motor Interfaces
(Operation with Unshielded Motor Cables)

Thank You!

March 4, 2022