

Power Electronics 4.0

Johann W. Kolar et al.

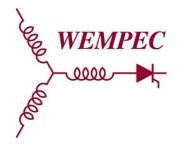


Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

May 18, 2022







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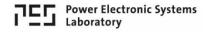
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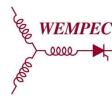
Outline

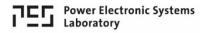
- **►** Introduction
- X-TechnologiesX-Concepts
- **Conclusions**

Acknowledgement

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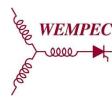




Power Electronics

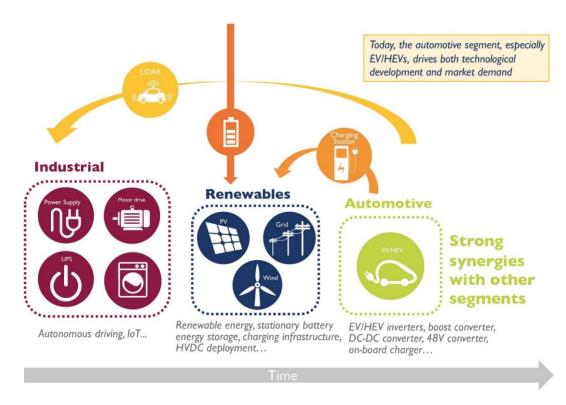
Driving Applications
Performance Indicators / Trends
Technology S-Curve





Driving Applications

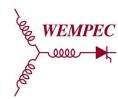
■ Global MEGA-Trends → Industry Automation | Renewable Energy | Sustainable Mobility | Urbanization etc.



Source: Status of Power Electronics Industry 2019 Report

- Clean Energy Transition → "All-Electric" Society
- UN Sustainable Development Agenda → There can be No "Plan B", because there is No "Planet B" (Ban Ki-moon)







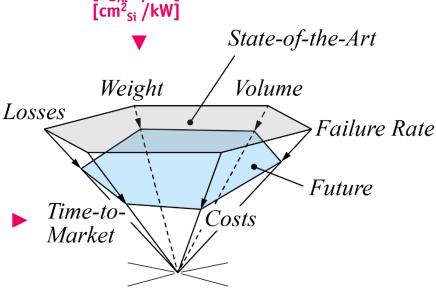


Performance Indicators / Trends

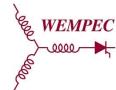
Environmental Impact...

 $[kg_{Fe} / kW]$ [kg_{Cu} /kW] [kg_{Al} /kW] [cm²_{Si} /kW]

- Power Density [kW/dm³]
 Power per Unit Weight [kW/kg]
 Relative Costs [kW/\$]
- Relative Losses [%]
- Failure Rate
- Manufacturability
- Recyclability / SustainabilityNetworked / IIoT

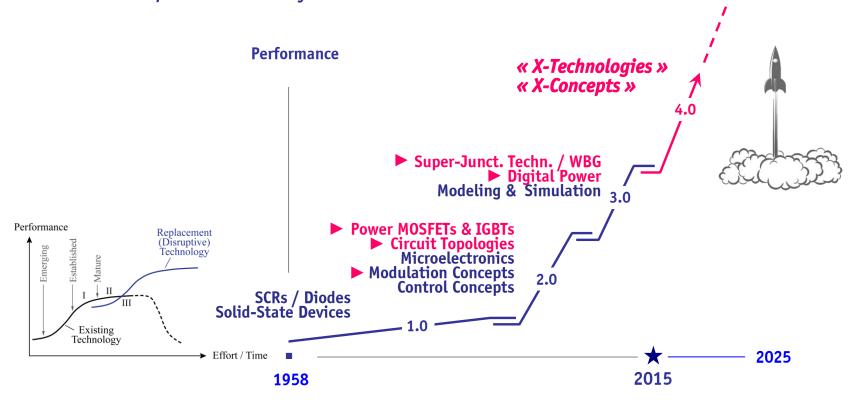




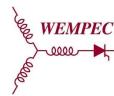


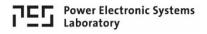
S-Curve of Power Electronics

- « X-Technologies » / "Moon-Shot" Technologies
 « X-Concepts » → Full Utilization of Basic Scaling Laws & « X-Technologies »
 Power Electronics 1.0 → Power Electronics 4.0
- 2...5...10x Improvement NOT Only 10%!







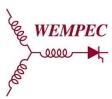


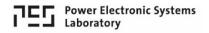


X-Technologies

SiC | GaN 3D-Packaging & Integration Digital Signal Processing



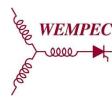


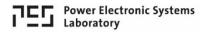












Low R*_{DS(on)} High-Voltage Devices

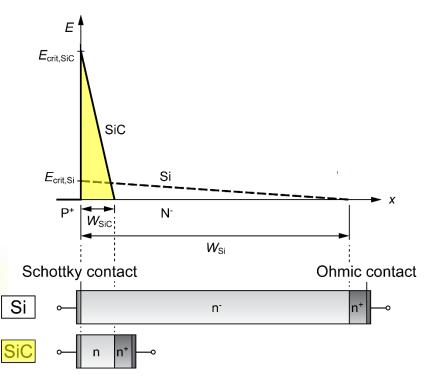
Higher Critical E-Field of SiC \rightarrow Thinner Drift Layer Higher Maximum Junction Temperature $T_{\rm j,max}$

at 300 K	Si	GaAs	4H/6H-SiC	GaN
Eg (eV)	1.12	1.4	3.0-3.2	3.4
Ec (MV/cm)	0.25	0.3	2.2-2.5	3
μn (cm²/Vs)	1350	8500	100-1000	1000
E r	11.9	13	10	9.5
Vsat (cm/s)	1x10 ⁷	1x10 ⁷	2x10 ⁷	3x10 ⁷
λ (W/cmK)	1.5	0.5	3 - 5	1.3

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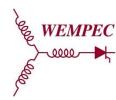
$$R_{\rm on}^* = rac{4V_B^2}{arepsilon \mu_n E_C^3} \leftarrow egin{array}{cccc} {
m For 1kV:} & {
m Si} & {
m SiC} \\ {
m W (\mu m)} & {
m 100} & {
m 10} \\ {
m N_D (cm^{-3})} & {
m 10^{14}} & {
m 10^{16}} \\ \end{array}$$

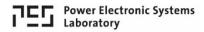
$$R_{\text{on,SiC}}^* \approx \frac{1}{300} R_{\text{on,Si}}^*$$



Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices





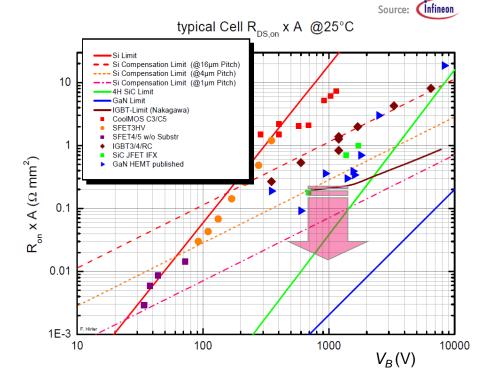


Low R*_{DS(on)} High-Voltage Devices

- SiC MOSFETs / GaN HEMTs (Monolithic AC-Switch)
 Low Conduction Losses & ZVS
- High Efficiency

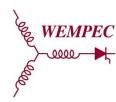
$$R_{\text{on}}^* = \frac{4V_B^2}{\varepsilon \mu_n E_C^3} \leftarrow$$

$$R_{\text{on,SiC}}^* \approx \frac{1}{300} R_{\text{on,Si}}^*$$



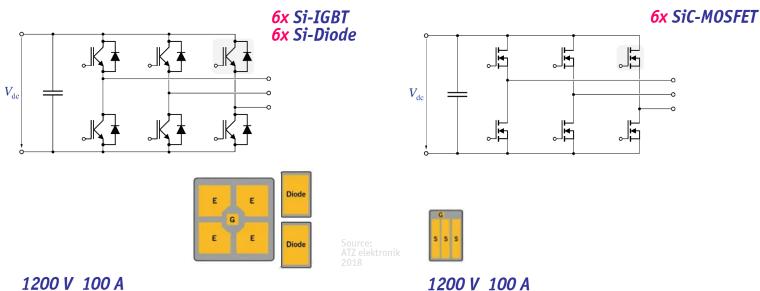
High-Voltage Unipolar (!) Devices → Excellent Switching Performance





Si vs. SiC

- Si-IGBT / Diode → Const. On-State Voltage, Turn-Off Tail Current & Diode Reverse Recovery Current → SiC-MOSFET → Massive Loss Reduction @ Part Load BUT Higher R_{th}

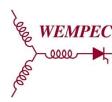


Die Size: $98.8 \text{ mm}^2 + 39.4 \text{ mm}^2$

Die Size: 25.6 mm²

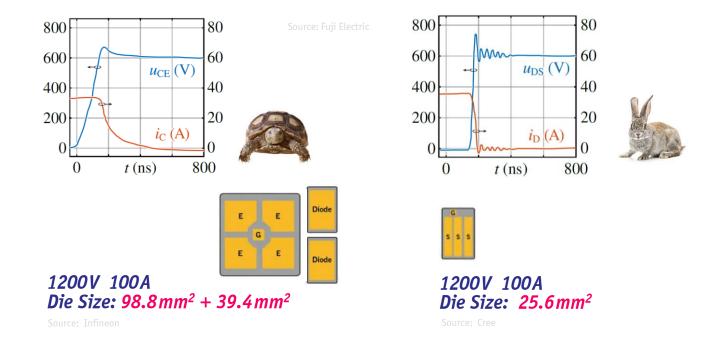
• Space Saving of >30% on Module Level (!)





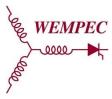
Si vs. SiC Switching Behavior

- Si-IGBT
- Si-IGBT → Const. On-State Voltage Drop / Rel. Low Switching Speed, SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed



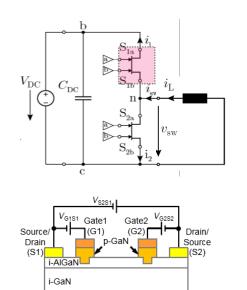
Extremely High di/dt & $dv/dt \rightarrow Challenges$ in Packaging / EMI





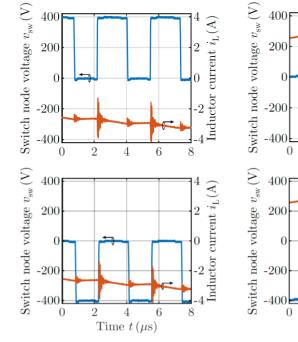
Monolithic 600V GaN Bidirectional/Bipolar Switch

- POWER AMERICA Program Based on Infineon's CoolGaNTM HEMT Technology (infineon Dual-Gate Device / Controllability of Both Current Directions
 Bipolar Voltage Blocking Capability | Normally-On or -Off



Buffer layer

Si substrate

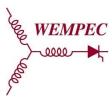


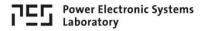
Time $t (\mu s)$

Panasonic

• Analysis of 4-Quardant Operation of $R_{DS(on)}$ = 140m Ω | 600V Sample @ \pm 400V

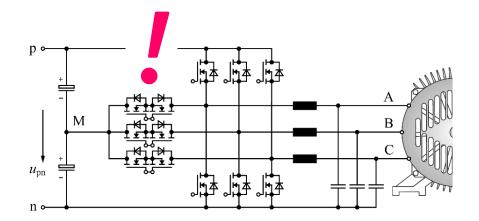


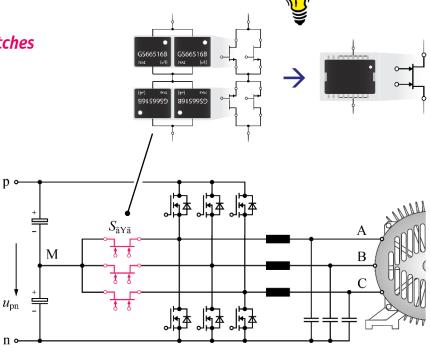




Example of 3-Level T-Type Inverter

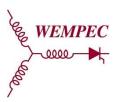
- Utilization of 600V Monolithic Bidirectional GaN Switches 2-Gate Structure Provides Full Controllability

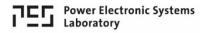




• Factor of 4 (!) Reduction of Chip Area vs. Discrete Realization





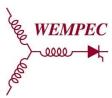












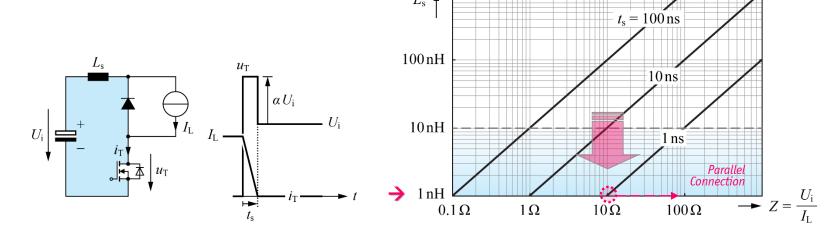
Circuit Parasitics

- Extremely High di/dt Commutation Loop Inductance L_s Allowed L_s Directly Related to Switching Time t_s \rightarrow

$$L\frac{di}{dt} = u$$

$$L_{s} \leq \frac{\alpha U_{i}}{I_{L}} = \alpha t_{s} \frac{U}{I_{L}}$$

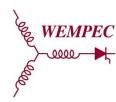
$$z$$



 $\alpha = 0.1$

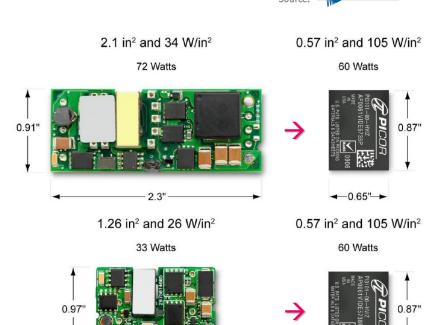
Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents (Z-Matching)



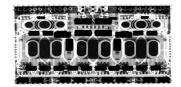


3D-Packaging / Heterogeneous Integration

- System in Package (SiP) Approach
 Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management
 Very High Power Density (No Bond Wires / Solder / Thermal Paste)
- PCBs Embedded Optic Fibres
- **Automated Manufacturing**
- Recycling (?)

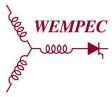


←0.65"**→**



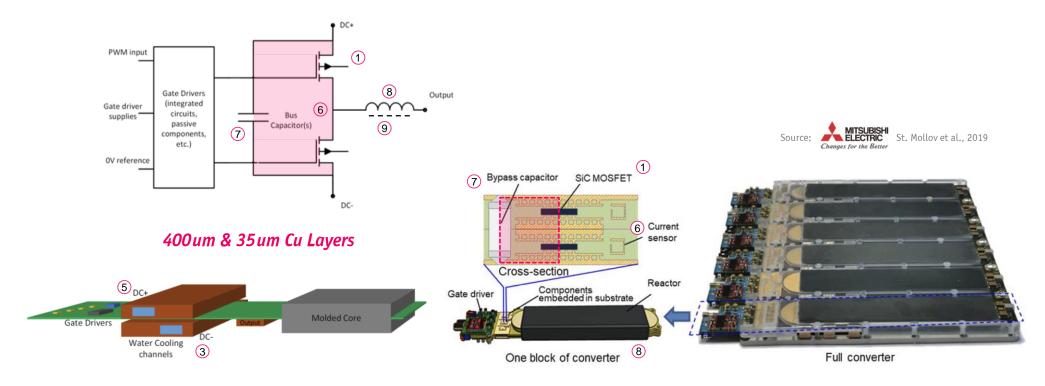
- Future Application Up to 100kW (!)
 New Design Tools & Measurement Systems (!)
 University / Industry Technology Partnership (!)





High-Power PCB-Embedding Technology

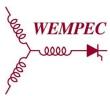
- PCB Integr. of SiC Chips / Passives / Sensors etc. → PCB Design Software / Custom Design / Low \$\$\$
 3D-Vertical Multilayer Structure → Ultra-Low Comm. & Gate Loop Ind. < 1nH / Low Sw. Losses & EMI
 Multi-Functional Use of Busbars → DC Supply & 2-Side Liquid Cooling of SiC Chips
- Results in Flat Structures (!)

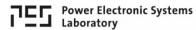


• 800 V DC-Link Bidirectional 100kW SiC DC/DC-Converter (24 x 18 x 1.7cm)





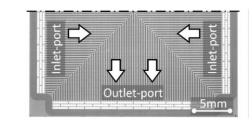


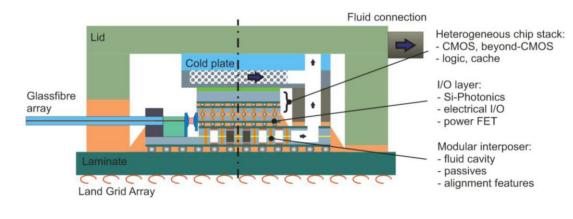


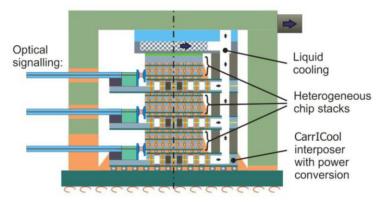


Remark Future uP Chip-Stack Packaging

- Slowing Transistor Techn. Node Scaling \rightarrow Vertical & Heterogeneous Integr. of ICs for Performance Gains
- **Extreme 3D-Integrated Cube-Sized Compute Nodes**
- **Dual Side & Interlayer Microchannel Cooling**



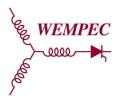


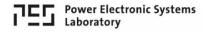


• Interposer Supporting Optical Signaling / Volumetric Heat Removal / Power Conversion





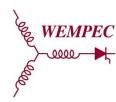


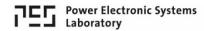






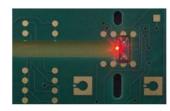


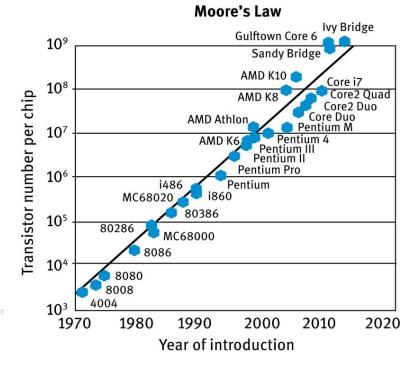




Digital Signal & Data Processing

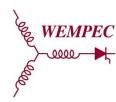
- Exponentially Improving uC / Storage Technology (!)
- Extreme Levels of Density / Processing Speed Software Defined Functions / Flexibility Continuous Relative Cost Reduction



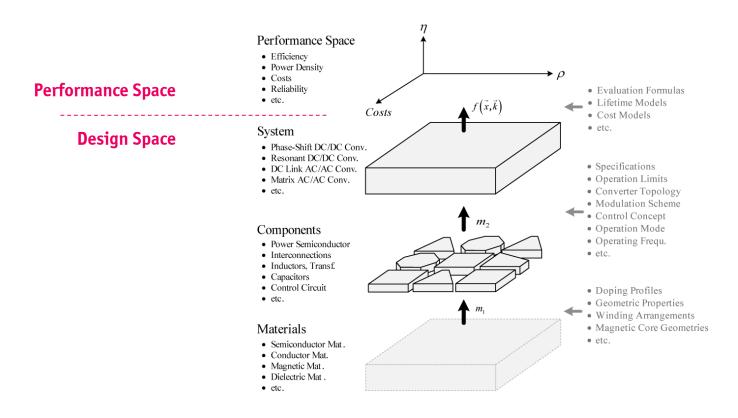


- Distributed Intelligence
- Fully Digital Control of Complex Systems Electrical/Optical/Wireless Signal Transfer
- Massive Comp. Power → Fully Automated AI-Supported Design / Digital Twins / Industrial IoT (IIoT)



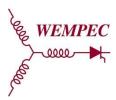


Abstraction of Power Converter Design

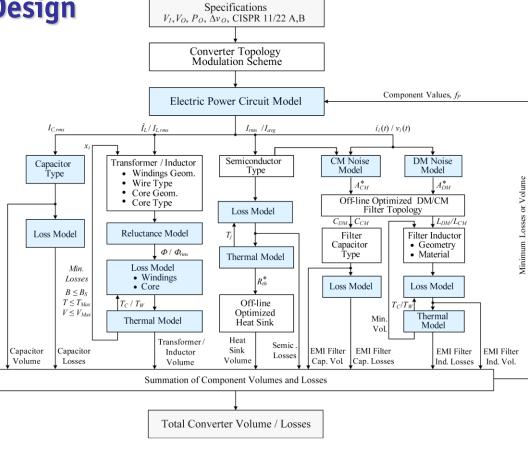


- Mapping of Design Space" into Converter "η-ρ-σ-Performance Space"
 Design Space Set of Selected Design- & Operating Parameters, Materials, Components, Topology, etc.



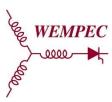


Mathematical Modeling of the Converter Design



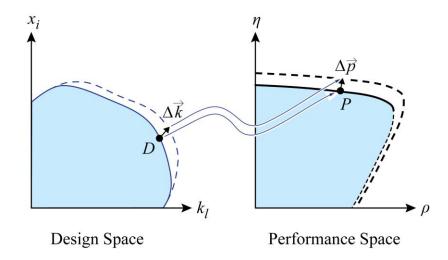
• Best Utilization of All Degrees of Freedom → Multi-Objective Optimization

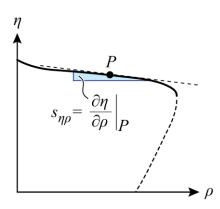




Multi-Objective Optimization

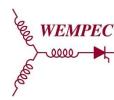
- Based on Mathematical Model of the Technology Mapping
 Multi-Objective Optimization → Best Utilization of the "Design Space"
 Identifies Absolute Performance Limits → Pareto Front / Surface

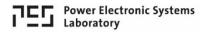




- Clarifies *Sensitivity* $\Delta \vec{p} / \Delta \vec{k}$ to Improvements of Technologies
- Trade-Off Analysis

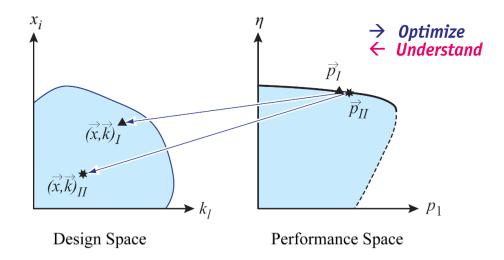


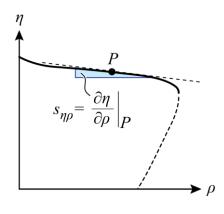




Design Space Diversity

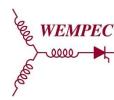
- **Equal Performance** \vec{p}_i for Largely Different Sets $(\vec{x}, \vec{k})_i$ of Design Parameters **E.g.** Mutual Compensation of Volume or Loss Contributions (e.g. Cond. & Sw. Losses)

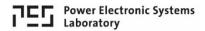




• Allows Consideration of Additional Performance Targets (e.g. Costs)

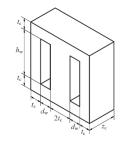


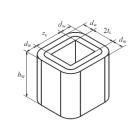




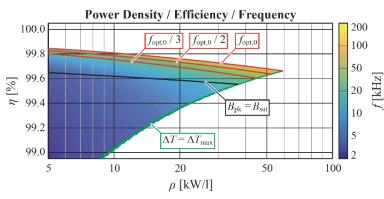
Design Space Diversity — Example

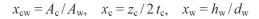
- Design of a Medium-Frequency Transformer
- Power Level & Power Density = const.
- Wdg./Core Loss Ratio, Geometry, n etc. as Design Parameters

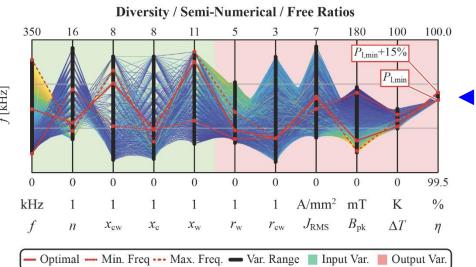






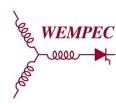






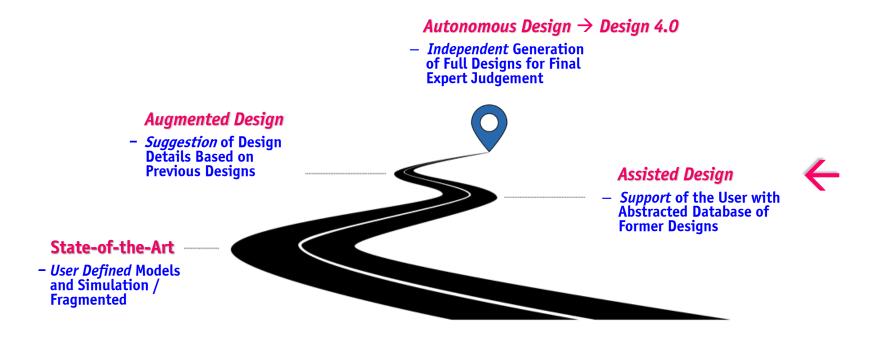
- Mutual Compensation Core & Winding Losses Changes
- ▶ Limits on Part Load Efficiency / Costs / Fixed Geometry → Restricted Diversity





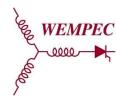
Design Automation Roadmap

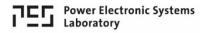
- End-to-End Horizon Cradle-to-Grave/Cradle Modeling & Simulation
- Design for Cost / Volume / Efficiency / Manufacturing / Testing / Reliability / Recycling



• AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)





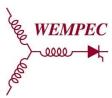


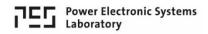


X-Concepts

Modularization
Functional Integration
Synergetic Association
Hybridization
Decentralization







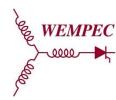


X-Concept



Modularization







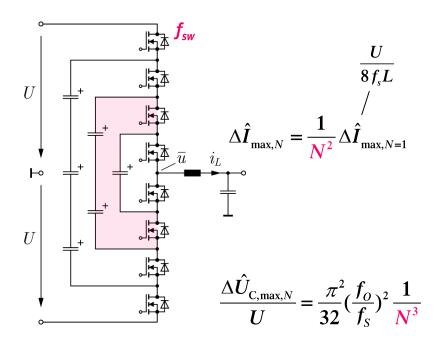
Scaling of Multi-Cell/Level Concepts

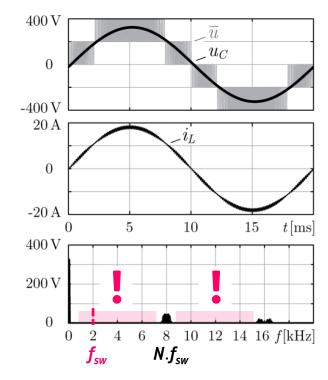
- Reduced Ripple @ Same (!) Switching Losses Lower Overall On-Resistance @ Given Blocking Voltage Application of LV Technology to HV



Half-Bridge Flying Capacitor Converter Switching Cell

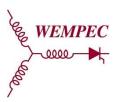
Source: R. Pilawa





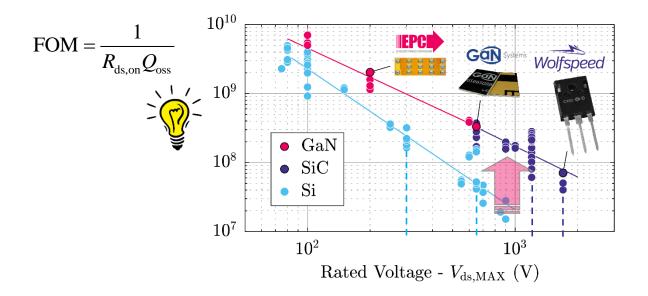
• Scalability / Manufacturability / Standardization / Redundancy





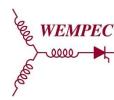
SiC/GaN Figure-of-Merit

- Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties FOM Determines Max. Achievable Efficiency @ Given Sw. Frequ.



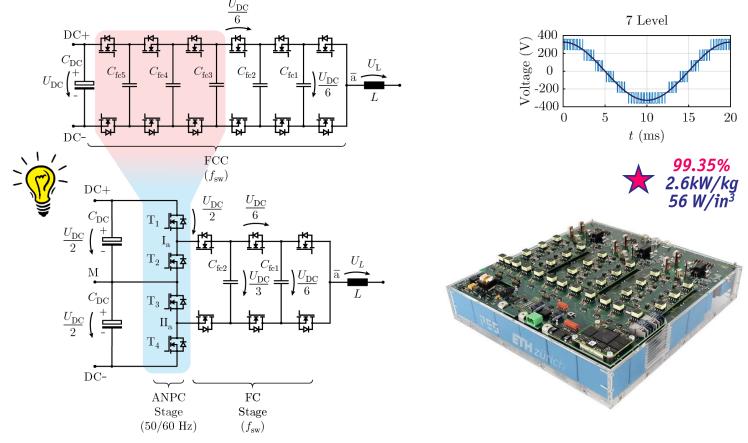
Advantage of Multi-Level over 2-Level Converter Topologies





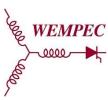
3-Ф Hybrid Multi-Level Inverter

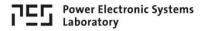
- Realization of a 99%++ Efficient 10kW 3-Ф 400V_{rms,ll} Inverter System
 7-Level Hybrid Active NPC Topology / LV Si-Technology







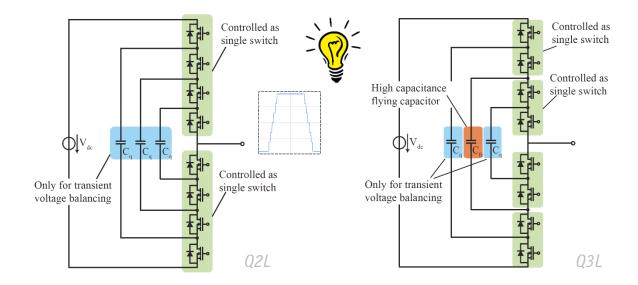




Quasi-2L & Quasi-3L Inverters

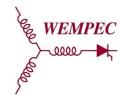
- Operation of N-Level Topology in 2-Level or 3-Level Mode
 Intermediate Voltage Levels Only Used During Sw. Transients

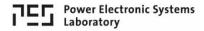




- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
 Low Voltage/Low R_{DS(on)}/Low \$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages







Quasi-2L & Quasi-3L Inverters

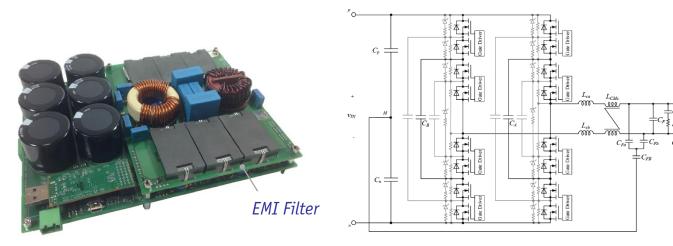
- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
 Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

Source: M. Schweizer



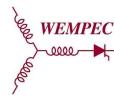
 $3.5kW/dm^3$ *Eff.* ≈ 99%

3.3kW @ 230V_{rms}/50Hz Equiv. $f_s = 48kHz$



- Reduced Average dv/dt → Lower EMI
 Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
 Low Voltage/Low R_{DS(on)}/Low \$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages



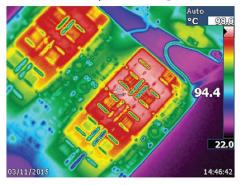


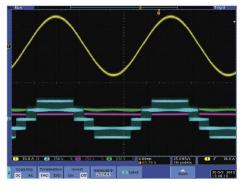
Quasi-2L & Quasi-3L Inverters

Source: M. Schweizer

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
 Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

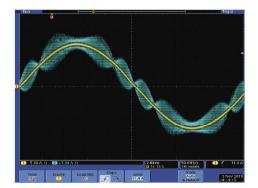
Operation @ 3.2kW







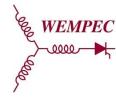
- Sw. Stage Output Voltage
- Flying Cap. (FC) Voltage
- Q-FC Voltage (Úncntrl.)

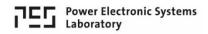


- Output Current
- Conv. Side Current

- Reduced Average dv/dt → Lower EMI
 Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
 Low Voltage/Low R_{DS(on)}/Low \$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages







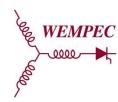


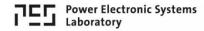
X-Concept



Functional Integration

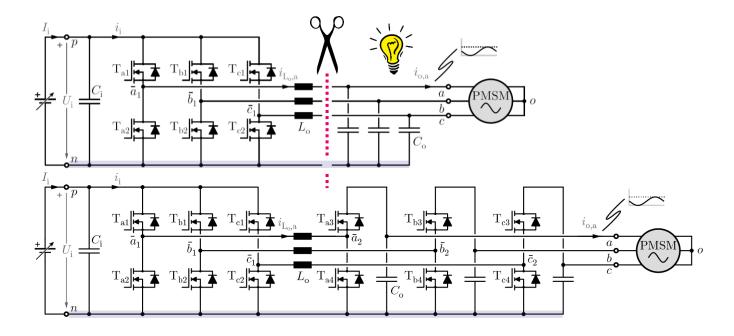






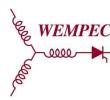
Buck-Boost 3-Ф Variable Speed Drive Inverter

- Generation of AC-Voltages Using Unipolar Bridge-Legs
 Utilize Filter Inductor for Boost Operation → Functional Integration



- Switch-Mode Operation of Buck OR Boost Stage → Single-Stage Energy Conversion (!)
 3-Ф Continuous Sinusoidal Output / Low EMI → No Shielded Cables / No Motor Insul. Stress

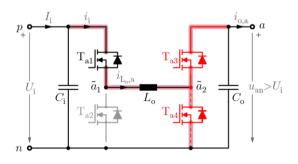




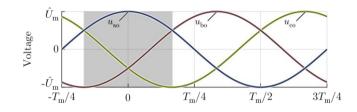


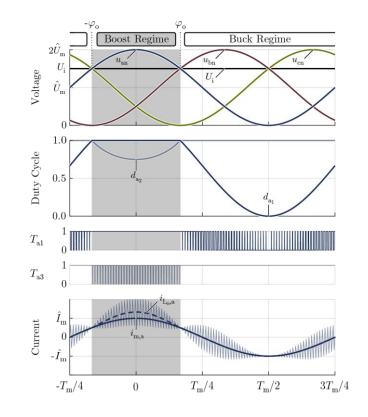
Boost-Operation $u_{an} > U_i$

■ Phase-Module



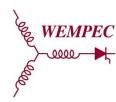
■ Motor Phase Voltages

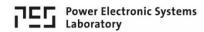




- Current-Source-Type Operation
 Clamping of Buck-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion

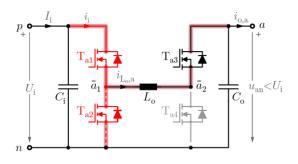




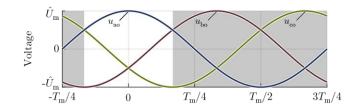


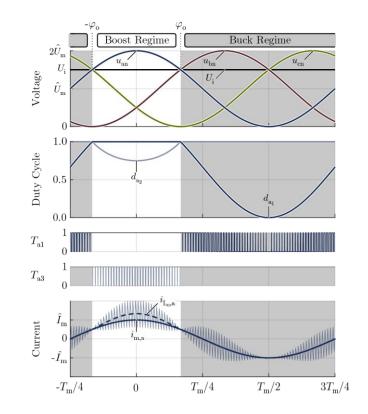
Buck-Operation $u_{an} < U_i$

■ Phase-Module



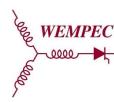
■ Motor Phase Voltages





- Voltage-Source-Type Operation
 Clamping of Boost-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion



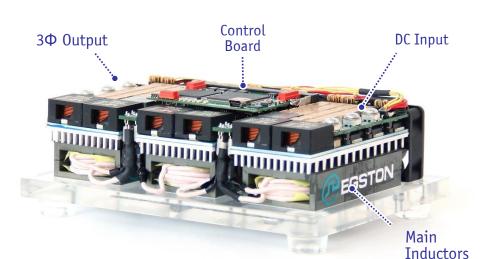


• DC Voltage Range 400...750V_{DC}

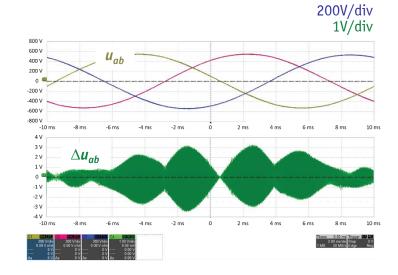
• Max. Input Current ± 15A

0...230V_{rms} (Phase) 0...500Hz Output Voltage

 Output Frequency 100kHz • Sw. Frequency



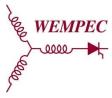


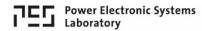


■ Dimensions \rightarrow 160 x 110 x 42 mm³





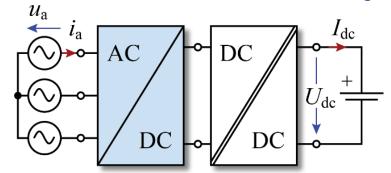




Isolated 3-Ф AC/DC Converters

- **Conventional Approach** \rightarrow Two-Stage | 3- \oplus PFC Rectifier & DC/DC Converter Stage
- **Functional Integration** → Utilizes AC/DC-Stage for Power Factor Corr. & HF AC Voltage Generation
 - → Transformer Stray Inductance Used as Current Source

Typ. 200...1000 V_{DC} EV Battery Voltage Range



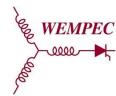
 i_a AC U_{dc} U_{dc}

320...530V_{rms} Line-to-Line

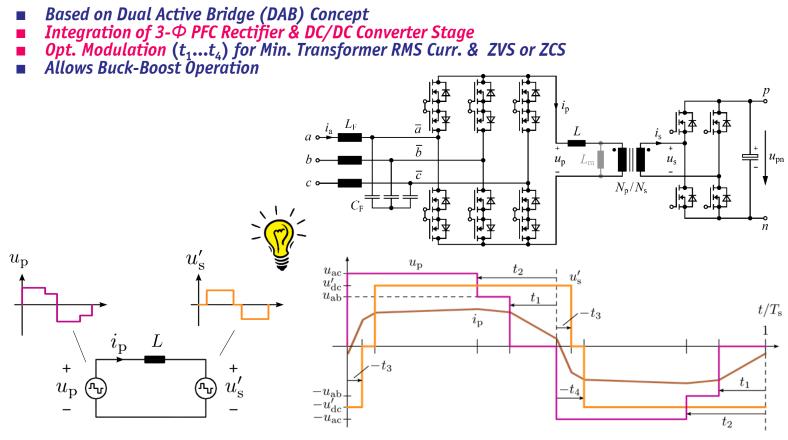
380 V_{DC} (260...400 V_{DC})
Datacenter Power Distribution

- Elimination of DC/DC Converter Input Stage & DC-Link \rightarrow Single-Stage Energy Conversion (!)
- Electric Vehicle Battery Charging | Datacenter Power Supply | AC Grid Interfaces of DC Micro-Grids





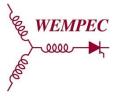
Isolated Matrix-Type 3-Ф PFC Rectifier



• Equivalent Circuit

• Transformer Voltages / Currents



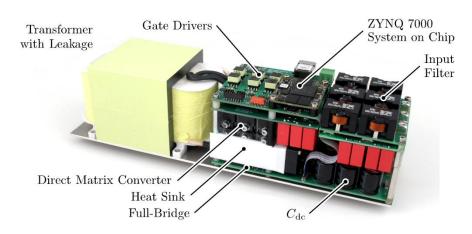




Isolated Matrix-Type 3- Ф PFC Rectifier

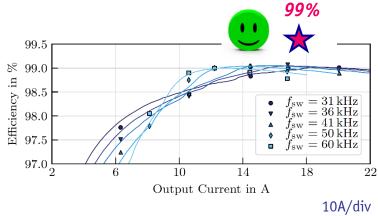
- Efficiency $\eta = 99\%$ @ 60% Rated Load (ZVS) Mains Current THD_I $\approx 4\%$ @ Rated Load Power Density $\rho \approx 4 \text{kW/dm}^3$

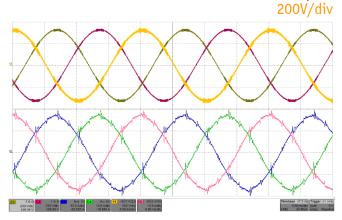
$$P_0$$
= 8 kW
 U_N = 400V_{AC} $\rightarrow U_0$ = 400V_{DC}
 f_S = 36kHz



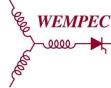


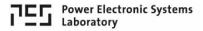
900V / $10m\Omega$ SiC Power MOSFETs Opt. Modulation Based on 3D Look-Up Table





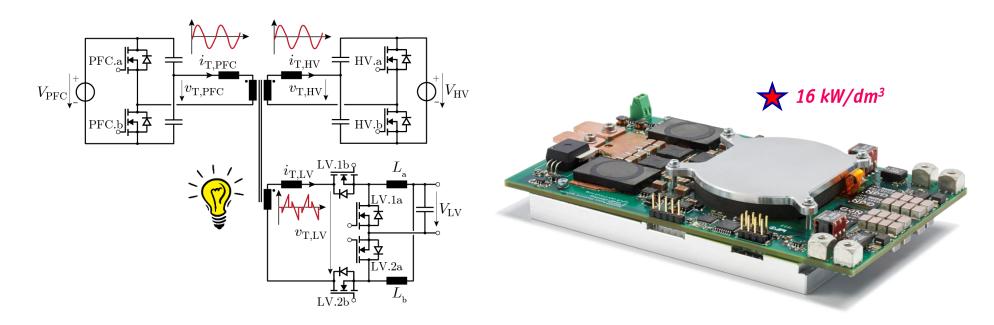






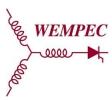
3-Port Resonant GaN DC/DC Converter

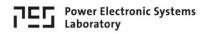
- Single Transformer & Decoupled Power Flow Control Charge Mode PFC \rightarrow HV (250...500V) SRC DCX / Const. f_{sw} , Min. Series Inductance / ZVS Drive Mode HV \rightarrow LV (10.5...15V) 2 Interleaved Buck-Converters / Var. f_{sw} / ZVS
- P = 3.6kW



- Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode
- PCB-Based Windings / No Litz Wire Windings → Fully Automated Manufacturing







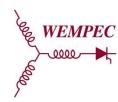


X-Concept



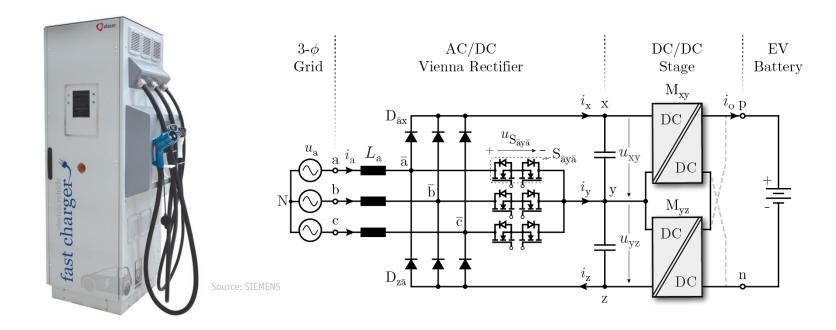
Synergetic Association





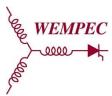
3-Ф EV-Charger Topology

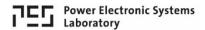
- Isolated Controlled Output Voltage
 Buck-Boost Functionality & Sinusoidal Input Current
 Applicability of 600V GaN Semiconductor Technology
 High Power Density / Low Costs



→ Conventional / Independent OR "Synergetic Control" of Input & Output Stage

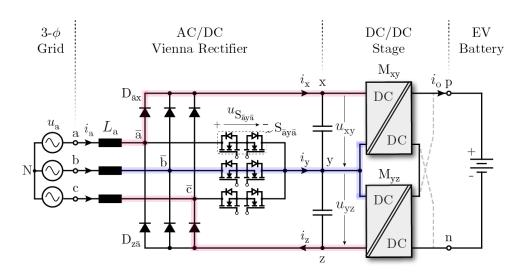


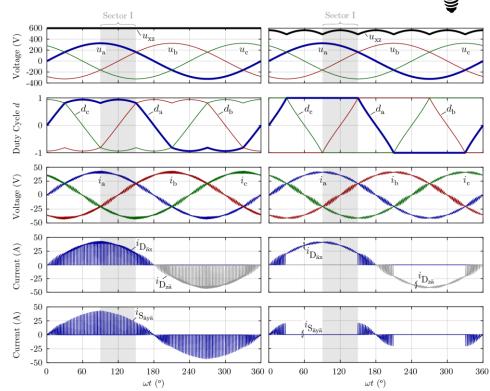




Synergetic Association

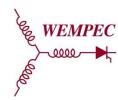
- 1/3-Modulation → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM
- Conduction Losses of the Switches ≈ -80% Switching Losses ≈ -70%

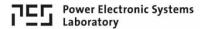


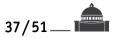


• Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses





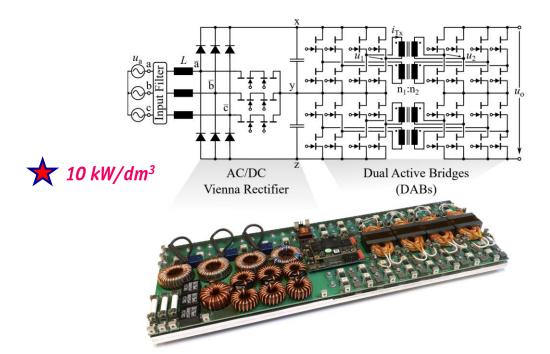


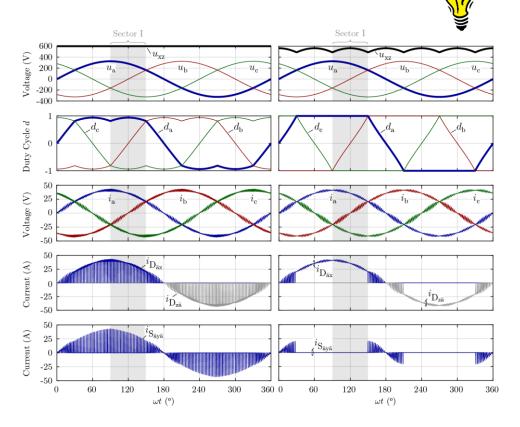


Synergetic Association

■ 1/3-Modulation → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM

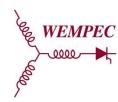
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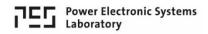




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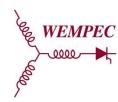


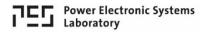
X-Concept



Hybridization

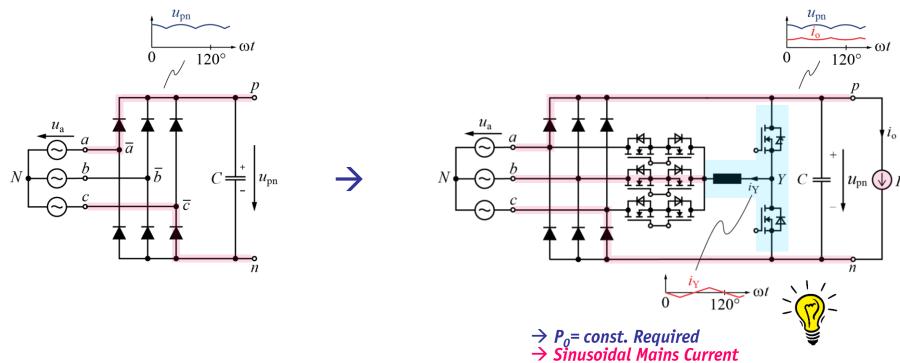






Hybrid Integrated Active Filter (IAF) PFC Rectifier

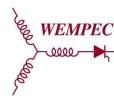
- Hybrid Combination of Mains- and Forced-Commutated Converter 3rd Harmonic Current Injection into Phase with Lowest Voltage Phase Selector AC Switches Operated @ Mains Frequency 3-Ф Unfolder

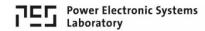


• Non-Sinusoidal Mains Current





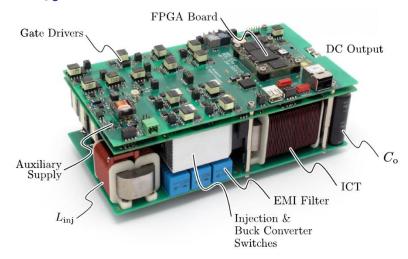




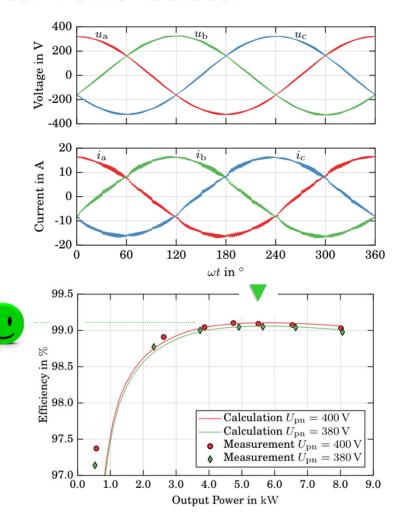
IAF PFC Rectifier & Buck Converter Demonstrator

- Efficiency $\eta > 99.1\%$ @ 60% Rated Load Mains Current THD_I \approx 2% @ Rated Load Power Density $\rho \approx 4 \text{kW/dm}^3$

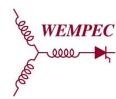
$$P_0$$
= 8 kW
 U_N = 400V_{AC} $\rightarrow U_0$ = 400V_{DC}
 f_S = 27kHz



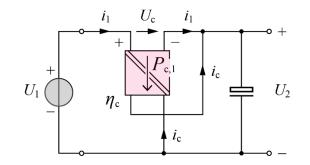
- SiC Power MOSFETs & Diodes
- 2 Interleaved Buck Output Stages
- **Controlled Output Voltage**







Partial/Differential Power Processing



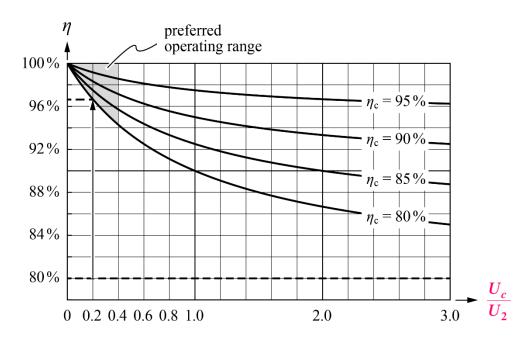
$$U_2 = U_1 - U_c$$

■ Reduced Converter Rating

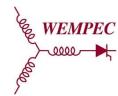
$$p_c = \frac{P_{c,1}}{P_1} = \frac{\frac{U_c}{U_2}}{1 + \frac{U_c}{U_2}}$$

■ Low Influence of Converter Efficiency on Overall Efficiency

$$\eta = \frac{P_2}{P_1} = \frac{(1 + \frac{U_c}{U_2} \eta_c)}{(1 + \frac{U_c}{U_2})}$$



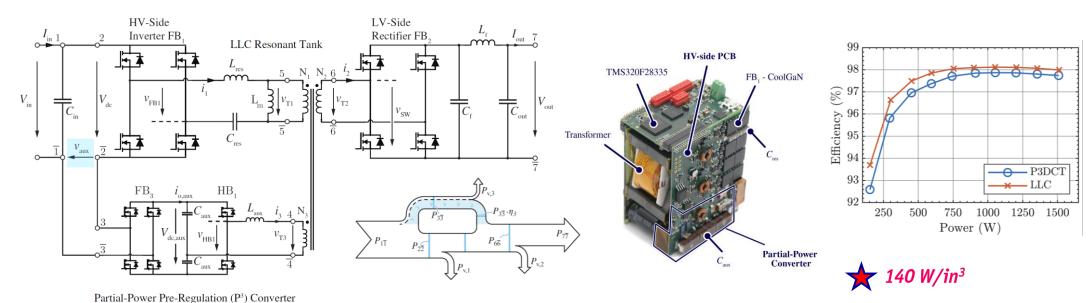






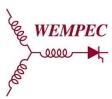
Partial-Power Pre-Regulated LLC DC-Transformer

- Aux. Converter Stage for ± 10% V_{in} Compensation | V_{in} = 340V ... 420V
 Const. Voltage Transfer Ratio / High Efficiency LLC «DC/DC Transformer» @ Const. Frequency | f_{sw} = 100kHz
 Const. Output Voltage | V_{out} = 48V



- - Rectangular Aux. Voltage Added or Subtracted (f_{aux} = 600kHz) from V_{in} Marginal Impact of Control on Overall Power Density & Efficiency

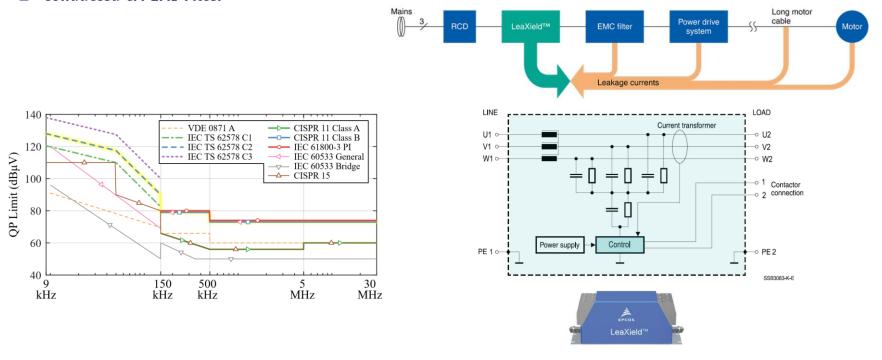






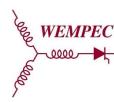
Hybrid EMI-Filter / Leakage Current Reduction

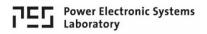
- Future Extension of EMI Limits 9kHz ... 150kHz | IEC TS 62578 Tech Spec. for Active Infeed Conv. Applications
- Earth Leakage Current "Compensation"
- Conducted CM EMI-Filter



- Prevents Unintentional Residual Current Device (RCD) Tripping w/o Isolation Transformer Attenuation of Cond. EMI Emissions in Wide Frequency Range 30/40/15dB @ 4/10/150kHz







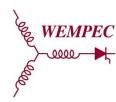


X-Concept



Decentralization

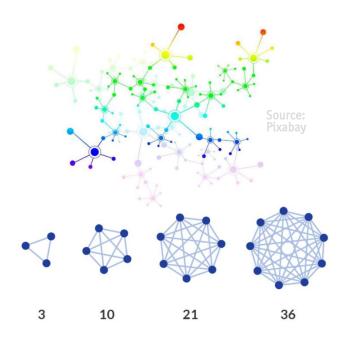


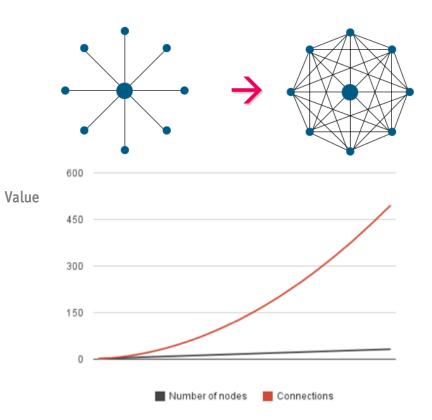


Networking Scaling

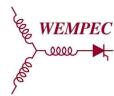
■ Metcalfe's Law

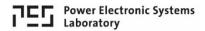
 Moving from Hub-Based Concept to Community Concept Increases Potential Network Value Over-Proportional → ~n(n-1) or ~n log(n)







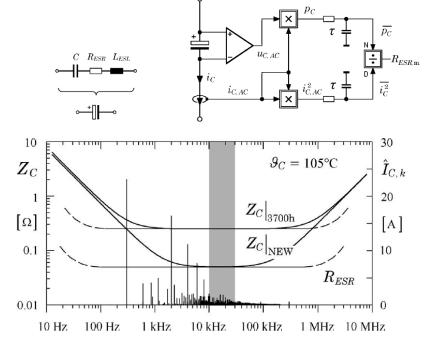


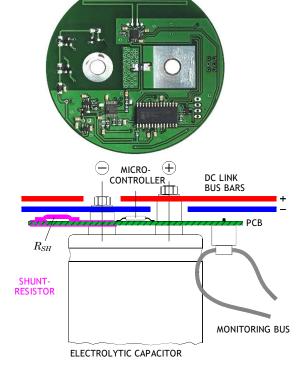


IIoT Starts with Sensors (!)

- **Condition Monitoring of DC Link Capacitors**
- On-Line Measurement of the ESR in "Frequency Window" (Temp. Compensated)
 Data Transfer by Optical Fibre or Near-Field RF-Link

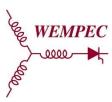


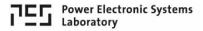




- Possible Integration into Capacitor Housing or PCB
- Additionally features Series Connect. Voltage Balancing

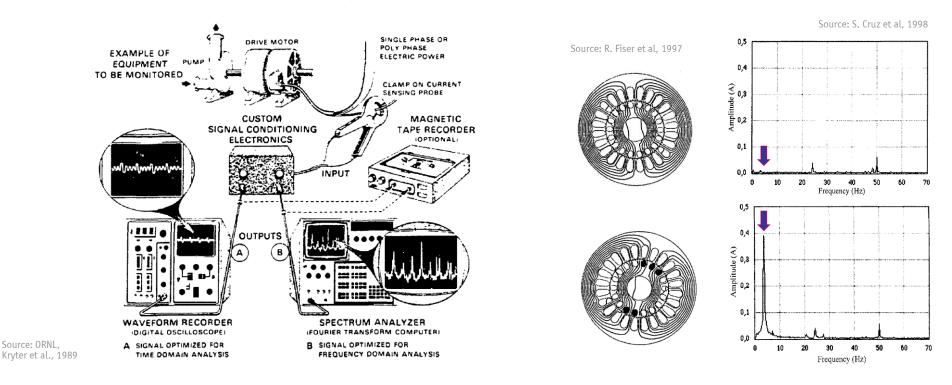






Motor Condition Monitoring / Fault Detection

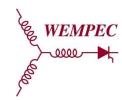
- Utilize the "Motor as Transducer" for Determining Aging / Wear of Motor and/or Mechanical Load
 Non-Intrusive Detection of Mechanical or Electrical Bearings or Stator & Rotor Abnormalities
 Motor Current Signature Analysis (MCSA) in Time & Frequency Domain



- ORNL (1989) MCSA Condition Monitoring of Motor-Valves in Nuclear Power Plant Safety Systems
- ANNs Discussed for Diagnostics since 25+ Years Improvements w/ Computing Power of Modern Inverters



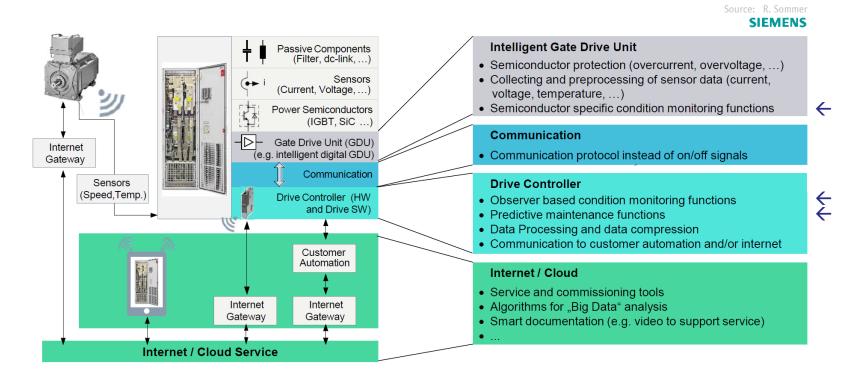
Source: ORNL,



Smart Inverter Concept

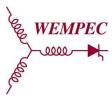


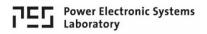
■ Utilize High Computing Power and Network Effects in the Cloud



• On-Line Protection / Monitoring / Optimization on Component | Converter | Drive | Application Level



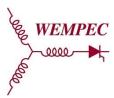


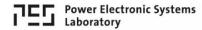






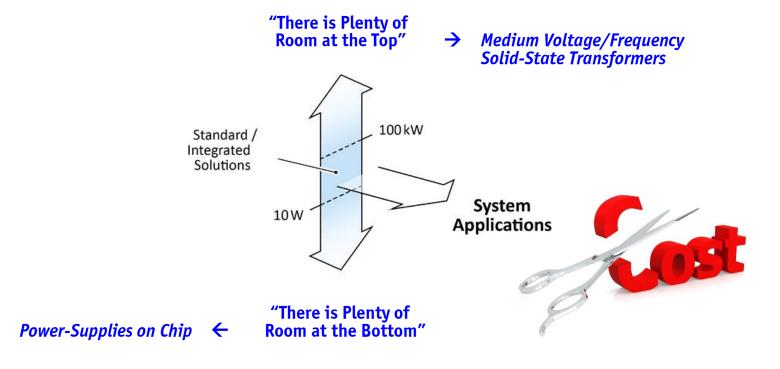






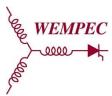
Future Application Areas

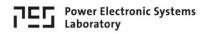
- WBG Driven Extension to Medium Voltage | Extension to Micro-Power Electronics
- Extreme Cost Pressure for Standardized Solutions (!)



- "There's Plenty of Room at the Bottom", Lecture by R. Feynman @ Caltech, 1959
- Key Importance of Technology Partnerships of Academia & Industry





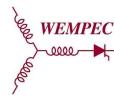




Source: www.roadtrafficsigns.com







Power Electronics → "Energy" Electronics

- Design Considering Converters as Standardized "Integrated Circuits" (PEBBs)
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

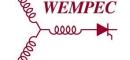


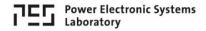
- "Converter" → "Systems" (Microgrid) or "Hybrid Systems" (Automation / Aircraft) → "Integral over Time" → "Energy"

$$p(t) \rightarrow \int_{0}^{t} p(t) dt$$

- Power Conversion
- → Energy Management / Distribution
- Converter Analysis
- → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
 → System Stability (Autonom. Cntrl of Distributed Converters)
 → Energy Storage & Demand Side Management
- Converter Stability
- Cap. Filtering
- Costs / Efficiency
- → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency

— etc.





Energy Electronics Systems Performance Figures/Trends

■ Complete Set of New Performance Indices

Power Density

Energy Density

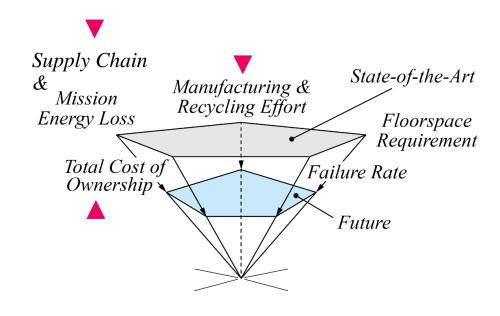
Environmental Impact

— TCO

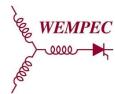
Mission Efficiency

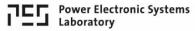
Failure Rate

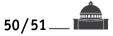
[kW/m²] [kWh/m³] [kWs/kW] [\$/kW] [%] [h⁻¹]









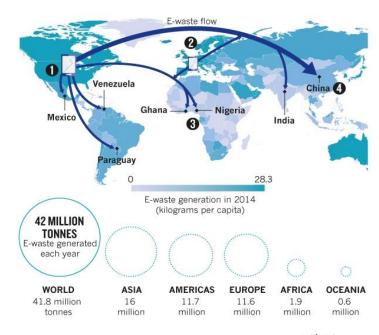




Remark Increasing E-Waste Problem

- 53'000'000 Tons of Electronic Waste Produced Worldwide in 2019 → 74'000'000 Tons in 2030
- Large Proportion Ends up in Africa & China \rightarrow Melting of PCBs & Cables etc. / Hazardous Substances Increasingly Complex Constructions \rightarrow No Repair or Recycling



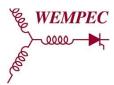


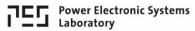


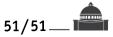
Source: nature

• Growing Global E-Waste Streams \rightarrow Increasing Attention of the Public / Upcoming Regulations











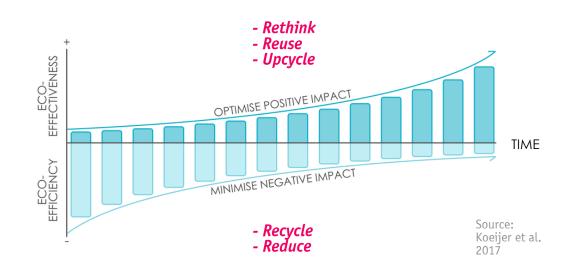
Remark Cradle-to-Cradle (C2C) Design Concept



- "Linear" Economy / Take-Make-Dispose → "Circular" Economy / Perpetual Flow & Maintained Value of Resources
- Resources Returned into the Product Cycle at the End of Use / Generation of Waste Minimized
- Maximized Use of Pure and Non-Toxic Reusable Materials

Source: https://circularphila delphia.org





- Decoupling of Economic Growth & Use of Resources
- Measures Covering the Entire Lifecycle ightarrow Design | Manufacturing | Consumption | Repair | Reuse | Recycling



