

# A New GaN T-Type Three-Switch Bridge-Leg for Cryogenic HTS Magnet Power Supplies

Mücahid Akbas, Daifei Zhang, Elias Bürgisser, Johann W. Kolar, and Jonas Huber

**Abstract**—Cryogenic step-down dc-dc converters for supplying high-temperature superconducting (HTS) magnets operate from low dc input voltages in the order of 1 V and provide high output/magnet currents. The proposed three-switch T-type (3STT) bridge-leg utilizes the (limited) reverse-blocking capability of standard GaN transistors to provide the same functionality (bipolar output voltage) as a conventional full-bridge (FB) topology. Advantageously, the 3STT features only a single transistor in the load current path (instead of two for the FB), reducing conduction losses by at least 50%. Loss measurements of a 25 A 3STT phase module demonstrator operating at 77 K (immersed in liquid nitrogen) verify the concept.

## I. INTRODUCTION

**A**IMING for improved energy efficiency of future particle accelerators such as the Future Circular Collider (FCC) at CERN [1], high-temperature superconducting (HTS) magnets could substitute normal conducting electromagnets [2], which are required to guide and shape the particle beam. HTS magnets operate at temperatures of 40 K to 60 K inside of a vacuum cryostat. Conventionally, they are supplied by low-voltage high-current power converters operating at ambient conditions outside of the cryostat [3]. This requires the feed-through of thick current leads into the magnet cryostat, which results in considerable heat leak-in (e.g., around 23 W for a 250 A magnet operating at 60 K and supplied from 300 K through optimized current leads [4]) and thus high energy consumption of the cryocoolers [5].

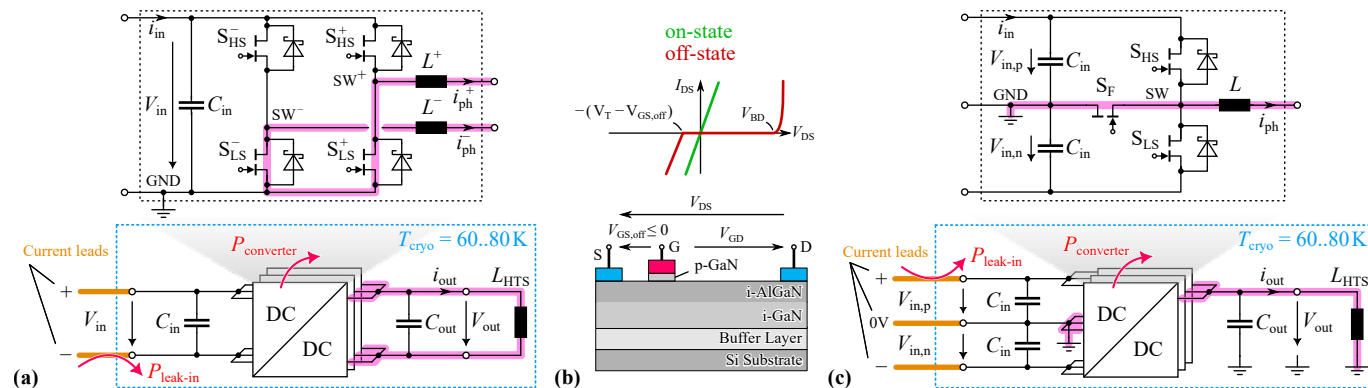
Therefore, new power supply approaches for HTS magnets have been proposed recently [6]–[11]. For example, placing a step-down dc-dc converter inside of the cryostat decouples

the magnet current from the lead current: With an HTS magnet load's typical parasitic resistance being in the order of  $1 \mu\Omega$ , the required steady-state output voltage for a magnet current of 250 A is only  $250 \mu\text{V}$ . Considering also the on-state resistances of the power transistors, a suitable dc input voltage is around  $V_{\text{in}} \approx 1 \text{ V} \dots 2 \text{ V}$ . This results in duty cycles of about  $D \approx 0.1 \dots 1\%$  and hence dc input currents that are two to three orders of magnitude lower than the magnet current, clearly enabling the use of much thinner current leads and hence lower leak-in losses. On the other hand, the power converter generates losses inside of the cryostat. To justify the increased design complexity that accompanies a cryogenic power converter, the total heat load of the cryocooler, i.e., the sum of the (now low) leak-in losses and the power converter losses, should be reduced to 1/4 of the conventional approach, i.e., to about 5 W to 6 W for the exemplary 250 A magnet considered here.

To ramp the magnet current up and, after a few hours in a typical mission profile, down again, a dc-dc converter with a bipolar output voltage is needed. Thus, given the high magnet current, typically parallel-interleaving of several full-bridge (FB) phase modules as shown in **Fig. 1a** is considered [9], which allows distributing the high load current to the phase modules and hence to more transistors than could practically be hard-paralleled. The interleaved operation enables ripple cancellation and hence reduces the output filtering effort, and, finally, lends itself to the implementation of redundancy concepts to maximize the availability of the overall converter system.

GaN power transistors are more suitable than silicon power transistors for cryogenic applications, as there are no adverse effects such as carrier freezeout in GaN; in contrast,

M. Akbas, D. Zhang, E. Bürgisser, J. W. Kolar, and J. Huber are with the Power Electronic Systems Laboratory, ETH Zürich, Switzerland.



**Fig. 1.** Cryogenic four-quadrant multiphase dc-dc converter using (a) full-bridge (FB) or (c) the proposed three-switch T-type (3STT) phase modules, which realize the mid-point switch S<sub>F</sub> using the (b) (limited) reverse voltage blocking capability of standard GaN HEMTs. The free-wheeling current paths, which are dominant in the considered low-output-voltage application, are highlighted.

the conduction losses decrease with temperature [12] and no degradation of the blocking voltage capability has been observed [13], [14].

Nevertheless, there are always *two* power transistors in the load current path of an FB topology, as highlighted in **Fig. 1a**. Therefore, expanding on [10], this letter describes the new three-switch T-type (3STT) bridge-leg topology shown in **Fig. 1c**, which advantageously features only *one* power transistor in the load current path and hence lower conduction losses. **Section II** explains the operating principle, **Section III** discusses the calculation of key loss components and demonstrates experimental results for operation of a 3STT phase module in liquid nitrogen (LN<sub>2</sub>) at 77 K, before **Section IV** concludes the paper.

## II. OPERATING PRINCIPLE

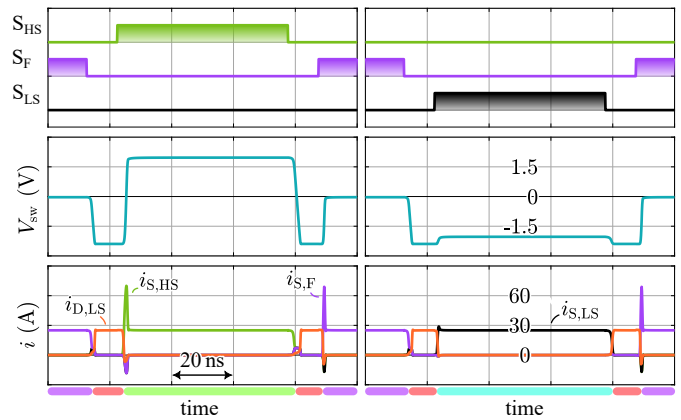
Three-level TT bridge-legs are known since the 1980s and widely used in high-power/high-voltage (e.g.,  $V_{in} = 800$  V) applications [15]. The midpoint switch then must provide symmetrical bidirectional voltage blocking capability of  $V_{in}/2$  and anti-series connections of two power transistors or recently available monolithic bidirectional switches are used.

However, in the considered application with typically  $V_{in,p} = V_{in,n} \leq 2$  V, the intrinsic structural symmetry of lateral GaN HEMT power transistors as illustrated in **Fig. 1b** can be utilized: In essence, a GaN HEMT turns on if the gate-source voltage exceeds the threshold voltage ( $V_{GS} \geq V_T$ ) in case of a positive drain-source voltage  $V_{DS}$ , or if  $V_{GD} \geq V_T$  ( $V_{GD}$  is the gate-drain voltage) in case of a negative (reverse)  $V_{DS}$ . As indicated in **Fig. 1b**, a negative off-state gate-source voltage  $V_{GS,off}$  increases the reverse-blocking voltage to  $V_T + |V_{GS,off}|$ , i.e., easily to a few volts.<sup>1</sup> Advantageously, the midpoint switch  $S_F$  is thus realized with a single unidirectional GaN HEMT, which leads to the proposed 3STT bridge leg from **Fig. 1c**. Compared to conventional FB phase modules, the proposed 3STT provides the same three output voltage levels ( $-V_{in}$ , 0,  $V_{in}$ ) but only a single transistor is in the load current path instead of two, reducing conduction losses at least by 50%. Note that the two input voltages,  $V_{in,p}$  and  $V_{in,n}$  must be provided and regulated externally, as the dc output voltage and current in general result in unbalanced loading of the two dc-link halves.

### A. Optimized Chip Area Allocation

Given the very low steady-state output voltage (low duty cycles), the load current flows through  $S_F$  for most of the time. Therefore, a further conduction loss reduction is possible by an asymmetric transistor configuration, i.e., by using more parallel transistors at the switch position  $S_F$ . Using, e.g.,  $N_{par} = 4$  parallel transistors for all switch positions, the proposed 3STT shows 1/2 of the conduction losses of a FB phase module (see **Fig. 1**). However, if the total of 16 transistors, each with an on-state resistance of  $R_{on}$ , of the FB are optimally allocated for low-duty-cycle operation, e.g.,

<sup>1</sup>Note that  $S_F$  must not be complemented with an anti-parallel Schottky (commonly used to lower dead-time conduction losses) to not compromise the reverse-blocking capability, see **Fig. 1c**.



**Fig. 2.** Transient simulation (LTspice) of commutations between (a)  $S_{HS}$  and  $S_F$  and (b) between  $S_F$  and  $S_{LS}$  for  $V_{in,p} = V_{in,n} = 2$  V, a positive output current of  $i_{out} = 25$  A, and a dead time of  $t_{dt} = 10$  ns.

the switches in the lower freewheeling path of the FB would be equipped with 7 transistors and the switches in the upper freewheeling path with 1 transistor only, an effective on-state resistance of  $R_{eff,FB} \approx 2/7 \cdot R_{on}$  results (with an adapted modulation using only the lower freewheeling path). Using the same 16 transistors in the 3STT, 14 could be allocated to the freewheeling path through  $S_F$  and 1 each to the other two switch positions, resulting in  $R_{eff,3STT} \approx 1/14 \cdot R_{on}$ . Advantageously, the conduction losses of the 3STT are now only 1/4 of those of the FB phase module. Ultimately, the optimal allocation of transistors to  $S_{HS}$ ,  $S_{LS}$ , and  $S_F$  depends on the specific application, as, e.g.,  $S_{HS}$  could be subject to higher current stress during ramp-up of the magnet current with higher output voltages and hence higher duty cycles compared to the steady state.

### B. Orientation of $S_F$

The orientation of  $S_F$  as shown in **Fig. 1c** allows  $V_{in,n} \gg V_{in,p}$  (as given by the voltage rating of the employed GaN HEMTs of, e.g., 100 V), which facilitates the implementation of HTS magnet quench protection schemes requiring quick energy extraction with large negative voltages (e.g., 80 V) [9]. If this feature is not needed, reversing the orientation of  $S_F$  simplifies the gate driver design as then the source terminal of  $S_F$  is on ground potential.

### C. Commutation Behavior

For the orientation of  $S_F$  as shown in **Fig. 1c**, the commutations between  $S_F$  and  $S_{LS}$  are like in any half bridge (see **Fig. 2b**). The commutations between  $S_{HS}$  and  $S_F$  deserve closer attention. Clearly, a dead time interval is needed, too, as the two switches must not be turned on simultaneously (which

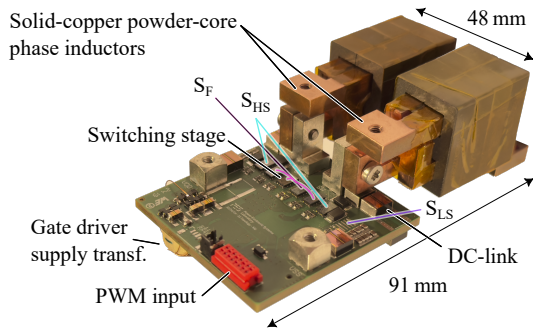


Fig. 3. Photo of the realized 3STT phase module demonstrator.

would short-circuit  $V_{in,p}$ ). For positive output current  $i_L > 0$ , as is typical for the considered HTS magnet application, this leaves only the anti-parallel diode of  $S_{LS}$  as a current path during the dead time, which is clearly visible in the switch-node voltage waveform shown in Fig. 2a, which temporarily goes towards  $-(V_{in,n} + V_{D,LS}(i_L))$ . Consequently, both commutations between  $S_{HS}$  and  $S_F$  involve the anti-parallel diode of  $S_{LS}$  and are hence effectively hard-switched. This, however, is tolerable due to the low switched voltage.<sup>2</sup>

### III. EXPERIMENTAL VERIFICATION

Fig. 3 shows a realized 3STT phase module using EPC2302 GaN HEMTs with  $N_{par,HS} = N_{par,F} = 4$  parallel devices for  $S_{HS}$  and  $S_F$ , and  $N_{par,LS} = 1$  for  $S_{LS}$  (no negative output voltages are used for the measurements). A half-bridge gate driver (LM5113) with an external digital signal isolator (ADUM1285CRZ) is used for  $S_{HS}$  and  $S_F$  and a single-channel driver (1EDN7550B) with fully differential inputs (and hence no need for a digital isolator) for  $S_{LS}$ . The gate resistors are  $0\Omega$  for all switches. The gate drive power supply uses a MAX256 switcher IC feeding a 100 kHz square wave voltage to a custom transformer with a toroidal nanocrystalline (Vitroperm 550 HF) core. There are three secondary windings connected to full-wave rectifiers using PMEG1020 diodes and acrylic film dc buffering capacitors, generating +6 V for  $S_{HS}$  and  $S_F$  (combined due to common source potential of  $S_{HS}$  and  $S_F$ ), -1 V negative supply voltage for  $S_F$  to extend the reverse blocking capability as discussed above, and +6 V for  $S_{LS}$ . Preliminary testing of the auxiliary power supply circuitry at RT and in LN<sub>2</sub> did show almost no change in losses.

Fig. 4 shows measured waveforms that confirm the commutation behavior between  $S_{HS}$  and  $S_F$  simulated above (see Fig. 2): During the dead time, the switch-node voltage swings to  $-V_{in,n}$  as  $D_{LS}$  temporarily is the only available path for the load current. In the following, further realization details and an estimation of the losses are given, which is then verified by loss measurements at room temperature (RT) and at 77 K in LN<sub>2</sub>.

#### A. Loss Estimation

In the following, straightforward loss estimates for a 3STT phase module (see Fig. 1c) are presented.

<sup>2</sup>For  $i_L < 0$  or for the opposite orientation of  $S_F$  (regardless of current direction), the commutations between  $S_{HS}$  and  $S_F$  would be as in a standard half bridge.

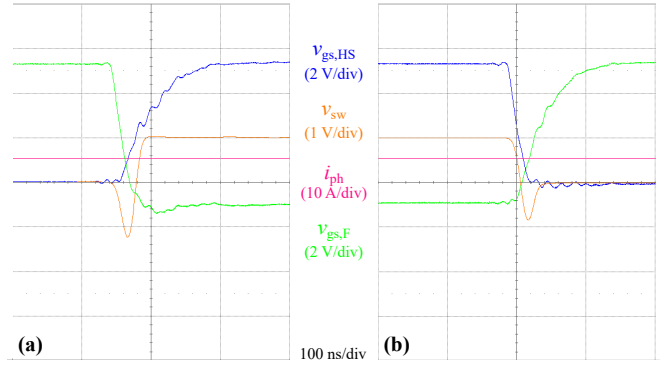


Fig. 4. Measured (at room temperature) switching transitions from (a)  $S_{HS}$  to  $S_F$  and (b) from  $S_F$  to  $S_{HS}$ , for  $I_{out} \approx 5$  A,  $V_{in,p} = V_{in,n} = 1$  V, and a dead time of  $t_d = 10$  ns. Note the undershoot of the switch-node voltage as the load current flows through  $D_{LS}$  during the dead time (see also Fig. 2).

1) *Transistor Conduction Losses:* With  $R_{on}$  denoting the on-state resistance of a single transistor,

$$P_{cond} = I_{ph}^2 / N_{par} \cdot R_{on}, \quad (1)$$

where  $I_{ph} = I_{out} / N_{phase}$  is the output current of one phase module and  $N_{par} = 4$  denotes the number of parallel transistors per switch position. Note that  $R_{on}$  at the operating temperature must be considered, i.e.,  $R_{on} = 1.3$  m $\Omega$  at room temperature and  $R_{on} = 800$   $\mu\Omega$  at 77 K for the considered EPC2302. The tight loss budget further implies so low per-transistor losses as to not result in any relevant temperature difference between the junction and the cold plate.

2) *Switching Losses:* Due to the very low switched voltage, only dead-time conduction losses must be considered,

$$P_{dead} = 2 \cdot V_F \cdot I_{ph} \cdot t_d \cdot f_{sw}, \quad (2)$$

where  $V_F = \{0.3$  V, 0.6 V $\}$  is the forward voltage drop of the anti-parallel Schottky diodes (PMEG3050) at RT and 77 K, respectively,  $t_d = 10$  ns is the dead time, and  $f_{sw} = 40$  kHz the transistor switching frequency.

3) *Gate Losses:* The total gate drive losses are

$$P_{gate} = N_{par} \cdot f_{sw} \cdot (Q_{g,HS} \cdot \Delta V_{gs,HS} + Q_{g,F} \cdot \Delta V_{gs,F}) \quad (3)$$

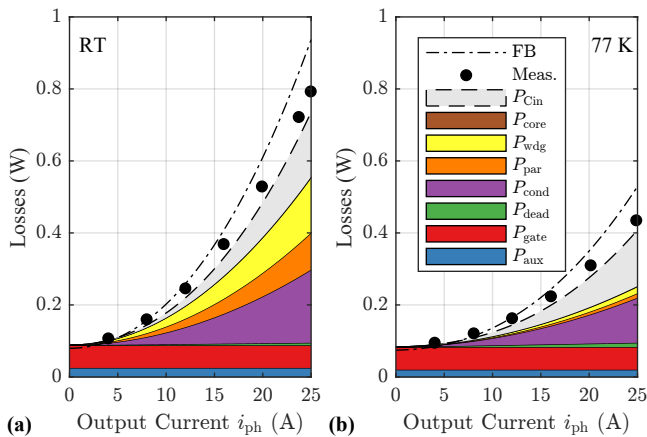
with the gate charges  $Q_{g,HS} = 28$  nC,  $Q_{g,F} = 32$  nC and the gate voltage swings  $\Delta V_{gs,HS} = 6$  V (0 V... 6 V) and  $\Delta V_{gs,F} = 7$  V (-1 V... 6 V for increased reverse blocking capability).

4) *Auxiliary Losses:* Auxiliary loss contributions from, e.g., the gate drive power supply or ICs are estimated as  $P_{aux} = 25$  mW at RT and  $P_{aux} = 20$  mW at 77 K based on measurements. Note that these losses could be further reduced by a different selection of components, dedicated design, etc.

5) *Other Conduction Losses:* The load current also causes ohmic losses in the PCB traces, connectors, etc., which are estimated with an additional resistance  $R_{par} \approx \{160$   $\mu\Omega$ , 20  $\mu\Omega\}$  at RT and 77 K, respectively, and each of the  $N_{ind} = 2$  phase inductors contributes  $R_{wdg} = \{120$   $\mu\Omega$ , 15  $\mu\Omega\}$  (measured).

6) *Phase Inductor Core Losses:* The phase inductor cores are each realized from 8 pieces of KoolMu 90 E-core segments (00K2510E090). The peak HF ac flux is

$$\hat{B}_{ac} = \frac{1}{2N_t f_{sw} A_c} \cdot (1 - D) \cdot D \cdot \frac{V_{in}}{N_{ind}} \quad (4)$$



**Fig. 5.** Measured and calculated losses of the 3STT phase module demonstrator from **Fig. 3** at (a) room temperature and (b) 77 K (immersed in LN<sub>2</sub>) for operation with  $f_{sw} = 40$  kHz,  $V_{in,p} = V_{in,n} = 1$  V, and  $R_{load} \approx 6$  m $\Omega$  (due to the measurement shunt, leading to high duty cycles and high input capacitor losses  $P_{Cin}$  compared to an HTS magnet load). The dashed lines indicate calculated losses of an equivalent FB phase module (same eff. switching frequency, same inductors,  $N_{par} = 4$  for all switches).

with  $N_t = 2$  turns, a core cross section of  $A_c = 4 \cdot 38.5$  mm<sup>2</sup>, and the duty cycle  $D \approx I_{out}R_{load}/V_{in}$ . Note that  $\hat{B}_{ac}$  is very small due to the dc current in the winding defining the required core cross section  $A_c$ . Hence, the core losses estimated with the Steinmetz equation  $p = k f_{sw}^\alpha \hat{B}^\beta$  with  $k = 40$  W/cm<sup>3</sup>,  $\alpha = 2$ ,  $\beta = 1.5$  (from the datasheet as literature reports little change for operation at cryogenic temperatures [16]) are found to be negligibly low; this would remain so even if very conservatively assuming an order of magnitude higher core losses due to performance degradation at cryogenic temperatures.

7) *Input Capacitor Losses:* For vacuum compatibility, the dc input capacitors are realized with  $N_{Cin} = 8$  paralleled 22  $\mu$ F acrylic film capacitors (Rubycon 16MU226MD35750) with an equivalent series resistance of  $ESR \approx 15 \dots 16$  m $\Omega$  each (measured at 77 K). Neglecting the output current ripple, the input capacitor losses are

$$P_{Cin} = I_{Cin,rms}^2 \cdot ESR / N_{Cin}, \quad I_{Cin,rms}^2 \approx (D - D^2) \cdot I_{out}^2, \quad (5)$$

i.e., increase with  $D$  for  $D < 0.5$ .

### B. Loss Measurements

The losses of the phase module demonstrator from **Fig. 3** operating with  $V_{in,p} = V_{in,n} = 1$  V, a switching frequency of  $f_{sw} = 40$  kHz, and dc output currents of up to  $I_{ph} = 25$  A have been measured at RT and immersed in LN<sub>2</sub> at 77 K.<sup>3</sup> Using  $V_{out} > 0$  implies switching between  $S_{HS}$  and  $S_F$  (both realized with  $N_{par} = 4$  EPC2302 GaN HEMTs). Precision multimeters (Agilent 34410A) are used to record the input and output voltages and the input and output currents (via precision shunts).

Note that the cabling and shunt resistor for measuring  $I_{ph}$  increase the effective load resistance to  $R_{load} =$

<sup>3</sup>The setup was lowered into a LN<sub>2</sub> bath and testing started once the absence of bubble formation indicated completion of the cooldown process and thermal steady-state. No further bubble formation or local boiling was observed during the experiments, which can be attributed to the very low overall losses distributed among many components.

{6.5 m $\Omega$ , 5.8 m $\Omega$ } at RT and 77 K, respectively. Hence,  $D$  and  $P_{Cin}$  increase significantly above the values expected with an HTS magnet load with a parasitic resistance of a few  $\mu\Omega$  only.<sup>4</sup>

**Fig. 5a** shows the measured losses at RT which match the calculations quite well. Clearly, the input capacitor loss contribution is relevant due to the current measurement shunt as discussed above. Further, the calculated losses for an equivalent FB phase module (all switches are realized with  $N_{par} = 4$ , same (effective) switching frequency and hence the same inductors, etc.) are clearly higher as  $P_{cond,FB} \approx 2P_{cond,3STT}$ .

**Fig. 5b** shows the results for operation at 77 K immersed in LN<sub>2</sub>. Again, a good match between calculation and experiments is observed, and the improvement compared to an FB phase module is clearly visible.

With  $R_{load} = 0$ , we expect  $P_{loss} \approx 0.26$  W at 77 K (instead of 0.41 W) as  $D$  reduces from  $D \approx 0.15$  to  $D \approx 0.0063$ ; i.e., with an HTS magnet load, the input capacitor losses would reduce to almost zero. Hence, a 250 A magnet PSU would require 10 parallel-interleaved phase modules<sup>5</sup> with losses of 2.5 W, not including leak-in losses (estimated  $< 0.5$  W)<sup>6</sup> and overall control circuitry (estimated around 1 W), i.e., total system losses of around 4 W, which is well below the targeted 5 W to 6 W. To achieve similar performance, more than 15 parallel FB modules with 16 transistors each (compared to the 12 transistors of the 3STT if realized symmetrically) would be required, i.e., a much higher realization effort.

## IV. CONCLUSION

By utilizing the (limited) reverse blocking capability of GaN transistors, the proposed 3STT bridge-leg topology achieves a conduction loss reduction of 50% compared to an equivalent FB realization, while using a smaller total transistor chip area. The operating principle of the 3STT is experimentally verified and detailed loss measurements at room temperature and at 77 K (immersed in LN<sub>2</sub>) confirm the expected performance. Further improvements are achievable with optimized chip area allocation to switch positions depending on the application. Specifically, for high-current HTS magnet power supplies, allocating more chip area to the freewheeling path can, e.g., reduce the 3STT conduction losses to 25% compared to a similarly optimized FB.

### ACKNOWLEDGMENT

This work was performed under the auspices and with support from the Swiss Accelerator Research and Technology (CHART) program.

<sup>4</sup>Note further that in a multi-phase converter, interleaving techniques reduce the input capacitor current.

<sup>5</sup>For completeness, note that it is possible to operate the realized phase module with higher currents: Testing a variant with  $N_{par,HS} = 4$ ,  $N_{par,F} = 8$ , and  $N_{par,LS} = 1$  in LN<sub>2</sub> at 77 K with 100 A output current, we measured losses of around 4 W. Thus, using only 2 to 3 phase modules to realize a 250 A system would result in 8 W to 12 W of losses—clearly exceeding the loss budget and highlighting the need to use more paralleled phase modules with lower per-module current.

<sup>6</sup>Even though the 3STT phase module requires a third current lead, the steady-state leak-in losses are slightly lower than those of an FB because of the lower steady-state power input covering mainly the lower converter losses.

## REFERENCES

- [1] CERN, "Future circular collider study: Exploring concepts and technologies for the next generation of powerful particle colliders," accessed 2024-05-14. [Online]. Available: <https://fcc.web.cern.ch/>
- [2] J. Kosse, M. Koratzinos, and B. Auchmann, "Reliability engineering of cryocooler-based HTS magnets for FCC-ee," *IEEE Trans. Appl. Supercond.*, vol. 34, no. 5, Aug. 2024.
- [3] E. Coulinge, S. Pittet, and D. Dujic, "Design optimization of two-quadrant high-current low-voltage power supply," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11 602–11 611, Nov. 2020.
- [4] R. McFee, "Optimum input leads for cryogenic apparatus," *Rev. Sci. Inst.*, vol. 30, no. 2, pp. 98–102, 02 1959.
- [5] V. Parma, "Cryostat design," in *CAS-CERN Accelerator School: Superconductivity for Accelerators*, Erice, Italy, Apr. 2014, pp. 353–399. [Online]. Available: <http://cds.cern.ch/record/1974062>
- [6] Y. Kondo, S. Fukano, A. Ninomiya, and T. Ishigohka, "Cryogenic low-voltage/high-current dc power source using multi-parallel-connected MOSFETs," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 2337–2340, Jun. 2009.
- [7] H. Kawashima, T. Ito, and S. Sugimoto, "Power supply for superconducting magnets," Poster presented at the *Appl. Supercond. Conf. (ACS)*, Honolulu, HI, USA, Oct. 2022.
- [8] A. Elwakeel, N. McNeill, R. Peña-Alzola, M. Zhang, and W. Yuan, "Cryogenic DC/DC converter for superconducting magnet application," *IEEE Trans. Appl. Supercond.*, vol. 32, no. 6, pp. 1–5, Sep. 2022.
- [9] D. Cao, D. Zhang, J. W. Kolar, and J. Huber, "Conceptualization of a cryogenic 250-A power supply for high-temperature-superconducting (HTS) magnets of future particle accelerators," in *Proc. 11th Int. Conf. Power Electron (ICPE/ECCE Asia)*, Jeju, Korea, May 2023, pp. 688–696.
- [10] M. Akbas, J. W. Kolar, and J. Huber, "New cryogenic T-type three-switch low-voltage high-current 4Q power supply for HTS magnets," in *Proc. Energy Convers. Congr. Expo (ECCE USA)*, Phoenix, AZ, USA, Oct. 2024.
- [11] H. Qian, P. Zhou, C. Wang, Y. Deng, and G. Ma, "Wireless power supply for HTS magnets: Circuit topology design and cryogenic testing," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, pp. 1–5, 2019.
- [12] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN power devices for cryogenic applications down to 4.2 K," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, Jul. 2021.
- [13] R. Ren, H. Gui, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, D. Costinett, B. J. Blalock, and B. B. Choi, "Characterization and failure analysis of 650-V enhancement-mode GaN HEMT for cryogenically cooled power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 66–76, Mar. 2020.
- [14] R. Chen and F. F. Wang, "SiC and GaN devices with cryogenic cooling," *IEEE Open J. Power Electron.*, vol. 2, pp. 315–326, 2021.
- [15] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-Type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.
- [16] H. Gui, R. Chen, J. Niu, Z. Zhang, L. M. Tolbert, F. F. Wang, B. J. Blalock, D. Costinett, and B. B. Choi, "Review of power electronics components at cryogenic temperatures," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5144–5156, May 2020.