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N. Nain,
Y. Zhang,
J. W. Kolar,
J. Huber

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Neha Nain, *Member, IEEE,* Yining Zhang,
Johann W. Kolar, *Fellow, IEEE,* and Jonas Huber, *Senior Member, IEEE*

Abstract*—Variable speed drives (VSDs) operating from the mains can be realized either with a voltage dc-link (voltage-source converter, VSC) or, alternatively, with a current dc-link (current-source converter, CSC), which has received renewed interest recently due to the availability of monolithic bidirectional GaN power transistors (M-BDS). Considering equally rated ac-ac VSC and CSC systems with sinusoidal output voltages (additional LC filter for the VSC, inherently present filter capacitors for the CSC), this paper first derives equivalent dc-dc converter models that accurately capture the dynamic behavior of the ac-ac converters and thus advantageously allow for a straightforward design and analysis of the converter control systems. Detailed experimental results obtained with realized ac-ac VSC and CSC prototypes (1.4 kW, 200 V line-to-line rms, 600 V GaN monolithic bidirectional power transistors in the CSC) show very close matching of the open-loop and the closed-loop behavior with that predicted by the dc-dc equivalent circuits. Therefore, these circuits are then utilized to compare the small-signal and large-signal output voltage control performance of the VSC and the CSC, indicating certain advantages for the CSC regarding small-signal bandwidth (5 kHz vs. 1.8 kHz for 72 kHz switching frequency, identical for both systems) and, in case of the CSC, highlighting the trade-off between control dynamics (dc-link current kept at the nominal value) and efficiency (dc-link current adapted to the load). Finally, a case study considering the time until nominal current is reached in an exemplary motor at standstill finds mixed comparative large-signal performance of VSC and CSC; a CSC variant with the output capacitor selected for equal high-frequency ripple as the VSC is slower than the VSC (by around 45% for the considered converter's specifications) whereas a CSC variant with the output capacitor selected for equal fundamental-frequency reactive power consumption as the VSC is faster (by around 40% for the considered converter's specifications).

I. Introduction

Typically, ac-ac variable speed drives (VSDs) are realized as a back-to-back configuration of an ac-dc rectifier stage and a dc-ac inverter stage [1]–[3]. The two stages share an intermediate energy storage element which allows independent control of the output voltage and frequency with respect to the grid. This energy storage element can either be a dc-link capacitor, in which case the system is referred to as a voltage-source converter (VSC), or a dc-link inductor, resulting in a current-source converter (CSC).

Over the past few decades, VSCs have become the preferred choice for low-voltage to medium-voltage VSDs, primarily due to advancements in Si-based power semiconductor devices such as MOSFETs and IGBTs (with an anti-parallel diode). These devices are capable of operating at switching frequencies typically upto 36 kHz (for 600 V power semiconductors and/or 400 V dc-link) and are particularly well-suited for VSCs due to their unipolar voltage blocking and bidirectional current conduction capability [4]. Wide-bandgap (WBG) power semiconductors, such as SiC and GaN, enable significantly higher switching frequencies *and* improved efficiency of VSDs [5]. However, the associated steeper slopes of the switched voltage at the inverter output terminals can adversely impact the lifetime of a motor as a result of higher common-mode currents flowing via the bearings, transient overvoltages in case of long motor cables, and generally increased conducted and radiated electromagnetic emissions necessitating the use of expensive shielded motor cables [6]–[8]. These issues can be mitigated by utilizing the high switching frequencies enabled by WBG devices, which facilitate the conversion of switched voltages into smooth sinusoidal waveforms using relatively compact LC output filters (see **Fig. 1a**) [5], [9], [10]. Furthermore, the integration of such an LC filter into the VSD has been demonstrated to enhance the overall efficiency of the drive system through reduced harmonic losses in the motor [5].

CSCs, on the other hand, inherently provide smooth output voltages due to the presence of ac-side filter capacitors (see **Fig. 1b**), which effectively buffer the switched current pulses provided by the CSC switching stage. However, unlike VSCs, CSCs require switching devices that possess *bipolar* voltage blocking and (at least) unidirectional current conduction capability. If this functionality is realized using standard WBG power transistors, a CSC requires four times the number of semiconductor devices compared to a VSC to achieve the same on-state resistance per switch position (see, e.g., Fig. 14 in [11]). Therefore, there has been ongoing research towards developing a monolithic bidirectional switch (M-BDS) capable of blocking both voltage polarities using the same drift region, which then, for a given on-state resistance, results in about the same chip area usage as a standard transistor with unipolar voltage blocking capability [12]–[19]. This research has resulted in mature GaN M-BDSs [20], which eliminate the above mentioned disadvantage of CSCs. This breakthrough thus necessitates new comparisons between CSC and VSC systems, both employing WBG devices and producing sinusoidal inverter output voltages.

Although there has been considerable research into the comparative analyses of CSC and VSC systems, most studies

N. Nain, Y. Zhang, J. W. Kolar, and J. Huber are with the Power Electronic Systems Laboratory, ETH Zurich, Switzerland.

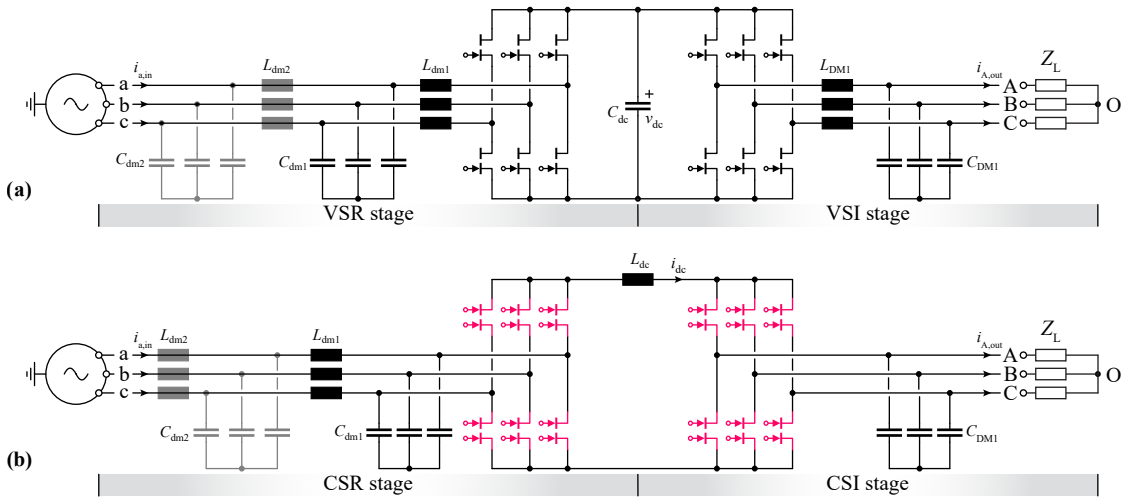

Fig. 1. Considered ac-ac **(a)** VSC and **(b)** CSC topologies providing sinusoidal output voltages to the load (here represented as a generic impedance Z_L). On the grid side, a DM EMI filter for compliance with CISPR 11 Class A is indicated, whereas the common-mode (CM) filter is not shown as it is not material for the targeted analysis of control dynamics. The second stage DM filter is not considered for the control design due to its high cut-off frequency.

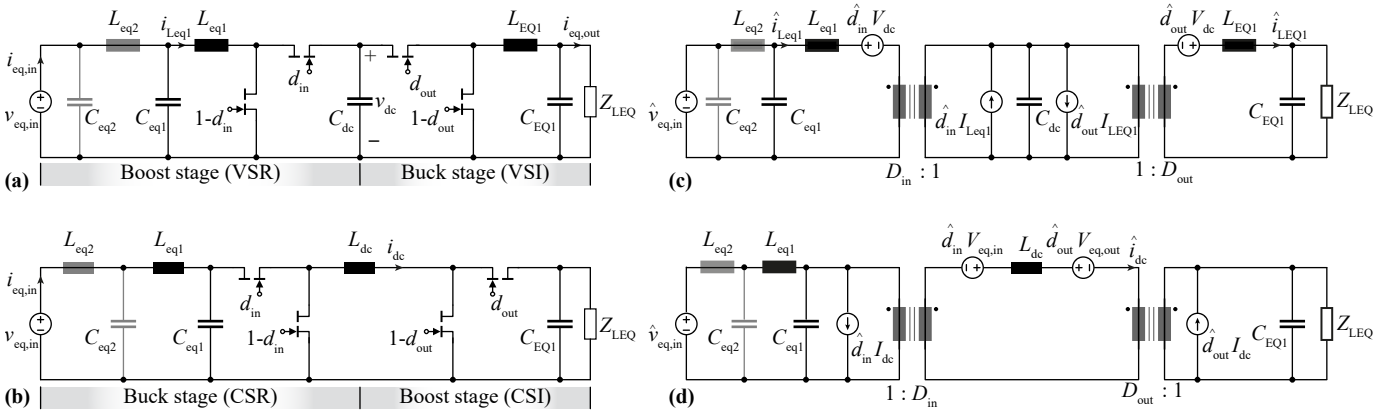

Fig. 2. Equivalent dc-dc model of the symmetric three-phase ac-ac **(a)** VSC and **(b)** CSC shown in **Fig. 1**. The modeling approach is based on ensuring identical instantaneous power flow and identical stored energy in the reactive elements between the ac-ac circuit and the dc-dc equivalent mode. **(c)** and **(d)** show the respective linearized dc-dc small-signal equivalent circuits suitable for the derivation of transfer functions.

have focused on system-level efficiency, power density, and semiconductor performance [21]–[24]. However, there remains a gap in the literature regarding the comparative analysis of the control dynamics between the two systems. The limited existing studies on control dynamics typically analyse VSC systems without an output LC filter, where VSCs demonstrate superior control dynamics—such as faster response to step changes in the output current (motor torque) reference compared to CSCs [4]. The inclusion of an LC filter at the output of the VSC inverter stage, however, impacts the dynamic response of VSC systems.

In this paper, therefore, we conduct a comparative analysis of the control dynamics between ac-ac VSC and CSC systems, both of which are designed for similar system efficiencies at the nominal operating point, have the same switching frequency, a two-stage differential-mode (DM) EMI filter towards the grid and most importantly, provide smooth output voltages with approximately the same switching frequency ripple to the load[1], i.e., the VSC is equipped with an LC output filter and CSC inherently features ac-side filter capacitors (see **Fig. 1**). The detailed comparison of the efficiency and power density of the ac-ac VSC and CSC systems is provided in [25].

A three-phase system with three balanced sinusoidally time-varying quantities x_a, x_b and x_c can be transformed into two constant quantities x_d and x_q by means of Park transformation, also widely known as dq-transformation, i.e.,

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}, \tag{1}$$

where θ is the reference angle of the rotating dq-coordinate frame [26]–[29]. This transformation has been widely used for modeling three-phase converters [28], [30] for control purposes, as PI controllers can track constant references in the dq-frame with zero steady-state error. Further, the d-component x_d represents active power flow and $x_q = 0$ results for unity power factor. It has been shown that the control dynamics and the stability of the system can be captured by the d-component alone as a result of negligible cross-coupling between the d-component and the q-component [31]. Therefore, by considering the d-component only, a balanced three-phase ac-dc converter can be accurately modeled as an equivalent

[1]We consider another case of same capacitive reactive power of the output filter as well.

TABLE I
KEY SPECIFICATIONS OF THE CONSIDERED AC-AC CSC AND VSC SYSTEMS.

Parameter		Value	Unit
Rated power	P_{n}	1.4	kW
Grid line-to-line rms voltage	$V_{\mathrm{g,n}}$	200	V
Nom. load phase rms current	$I_{\mathrm{l,n}}$	4	A
Nom. load line-to-line rms voltage	$V_{\mathrm{l,n}}$	200	V
Nom. dc-link voltage (VSC)	V_{dc}	400	V
Nom. dc-link current (CSC)	I_{dc}	7	A
Dead time for VSC		50	ns
Overlap time for CSC[2]		50	ns

Note: Capital V denote line-to-line rms voltages, capital I denote phase rms currents and subscript g and l denote a grid and load side quantities respectively.

dc-dc converter with identical power transfer capability, which effectively captures the control dynamics of the three-phase ac-dc system [31]–[33]. This simplification enables the application of dc-dc converter control design techniques to three-phase ac-dc systems. In this paper, we extend this modeling approach to ac-ac VSC and CSC systems: **Section II** presents the derivation of the dc-dc models for the ac-ac VSC and CSC systems. The validity of the derived models is confirmed through experimental verification of open-loop step responses and frequency responses using two 1.4 kW, 200 V (line-to-line rms) GaN-based demonstrator systems with specifications listed in **Tab. I**. Upon verifying the accuracy of the derived dc-dc models, they are employed for the control design of the ac-ac systems, as detailed in **Section III**. The designed closed-loop controllers are experimentally verified using hardware measurements of ac-ac VSC and CSC systems as well, where again a good match between ac-ac measurements and dc-dc equivalent models is found. Finally, **Section IV** provides a comparative analysis of the control dynamics of the VSC and CSC systems, utilizing simulation results of the experimentally validated dc-dc equivalent models, and **Section V** provides concluding remarks.

II. DC-DC MODEL DERIVATION

Symmetric three-phase ac-dc converters can be represented as equivalent dc-dc converters to simplify control-related analyses [31]–[33]. Based on this, to model a balanced three-phase ac-ac converter as an equivalent dc-dc converter, two primary conditions are enforced:

- At any given point in time, the instantaneous power (averaged over a switching cycle) is constant and same for both systems.
- The stored energy in each equivalent reactive element of the dc-dc equivalent circuit is equal to the total stored energy in the corresponding reactive elements of the ac-ac circuit (the switching frequency ripple components neglected).

The input ac-dc voltage-source rectifier (VSR) stage of a VSC can only operate with dc-link voltages v_{dc} that are equal to or greater than the grid line-to-line voltage amplitude, effectively functioning as a voltage booster. Consequently, this stage is modeled as a dc-dc boost converter (see **Fig. 2a**). Conversely, the output dc-ac voltage-source inverter (VSI) stage switches the dc-link voltage and can thus only generate line-to-line voltage amplitudes that are equal to or lower than v_{dc}, thus being modeled as a dc-dc buck converter.

In a CSC, the input current-source rectifier (CSR) stage can only operate with a dc-link current i_{dc} equal or greater than the input phase current amplitude $\hat{i}_{\mathrm{ac,in}}$, thereby functioning as a current booster and is thus modeled as dc-dc buck converter (stepping down the voltage but stepping up the current accordingly due to constant power flow). The output current-source inverter (CSI) stage, on the other hand, can only produce output current amplitudes $\hat{i}_{\mathrm{ac,out}}$ equal to or lower than the dc-link current i_{dc}, and is therefore modeled as a dc-dc boost converter, as shown in **Fig. 2c**.

A. Equivalent DC-DC Model Derivation

The derivation of dc-dc model begins with the scaling of the reactive elements on the ac-side[3]. In a balanced three-phase system with an open neutral point, the current flowing through one phase returns via the other two phases (in each 60° wide interval of the fundamental period, where one phase current is assumed to be positive and the other two negative). Therefore, to derive the equivalent filter components for the dc-dc model, it is logical to consider the effective reactive elements on the ac side as a series connection of one phase component with the parallel combination of the remaining two phase components. Assuming the three phase inductors and capacitors have the same values, respectively, this leads to

$$\begin{aligned} L_{\mathrm{eqx}} &= \frac{3}{2} L_{\mathrm{dmx}}, \quad C_{\mathrm{eqx}} = \frac{2}{3} C_{\mathrm{dmx}}, \\ L_{\mathrm{EQ1}} &= \frac{3}{2} L_{\mathrm{DM1}}, \quad C_{\mathrm{EQ1}} = \frac{2}{3} C_{\mathrm{DM1}}, \end{aligned} \tag{2}$$

where, x$\in [1, 2]$, L_{dm1}, L_{dm2}, C_{dm1} and C_{dm2} are the first and second stage grid-side DM filter components of the ac-dc VSR and CSR stage (see **Fig. 1**) and L_{eq1}, L_{eq2}, C_{eq1} and C_{eq2} are the equivalent filter components at the input side of the dc-dc model (see **Fig. 2ac**). L_{DM1} is the output filter inductor of the VSI stage, C_{DM1} the output filter capacitor of the VSI or the CSI stage (see **Fig. 1**) and L_{EQ1}, C_{EQ1} the corresponding equivalent filter elements at the output of the dc-dc models (see **Fig. 2ac**). It is important to note that with this scaling, the filter resonant frequencies of the three-phase ac-ac system and the equivalent dc-dc model are identical. Similarly, all other inductors, capacitors, and resistors on the ac-side can be appropriately scaled for the equivalent dc-dc model, e.g., the symmetric three-phase load impedance Z_{L}.

To ensure that the stored energy in equivalent elements of the dc-dc models correspond to that of the ac-side reactive

[2]The CSC requires a four-step commutation sequence [34] and an overlap time of 50 ns is used between each step of the commutation sequence.

[3]Note that only the DM filter components are relevant for control considerations; hence the CM filter components are ignored.

elements of the ac-ac circuits, the following relationships must hold for the equivalent dc voltages and currents, e.g.,

$$\begin{aligned} \frac{1}{2}L_{\text{eq2}} \cdot i_{\text{Leq2}}^2 &= \frac{1}{2}L_{\text{dm2}} \cdot \sum_{\text{x=a,b,c}} i_{\text{Ldm2,x}}^2, \\ \frac{1}{2}C_{\text{eq2}} \cdot v_{\text{Ceq2}}^2 &= \frac{1}{2}C_{\text{dm2}} \cdot \sum_{\text{x=a,b,c}} v_{\text{Cdm2,x}}^2, \end{aligned} \tag{3}$$

where $i_{\text{Ldm2,x}}$ represents the current through L_{dm2} and $v_{\text{Cdm2,x}}$ is the voltage across C_{dm2} for phase x (x∈[a,b,c]). The variables i_{Leq2} and v_{Ceq2} denote the current through L_{eq2} and voltage across C_{eq2} in the equivalent dc-dc model, respectively. The energy equivalence expressed in (3) is applied consistently to all the reactive elements on both, the input and output sides. By applying this principle along with the scaling relationship in (2), we find

$$\begin{aligned} i_{\text{eq,in}} &= \hat{i}_{\text{ac,in}}, \quad v_{\text{eq,in}} = \frac{3}{2}\hat{v}_{\text{ac,in}}, \\ i_{\text{eq,out}} &= \hat{i}_{\text{ac,out}}, \quad v_{\text{eq,out}} = \frac{3}{2}\hat{v}_{\text{ac,out}}, \end{aligned} \tag{4}$$

where, $\hat{i}_{\text{ac,in}}$ and $\hat{i}_{\text{ac,out}}$ are the amplitudes of the input grid and output load phase currents, respectively, and $\hat{v}_{\text{ac,in}}$ and $\hat{v}_{\text{ac,out}}$ are the amplitudes of the input grid and output load phase-to-neutral voltages in the three-phase ac-ac system. The terms $i_{\text{eq,in}}$, $i_{\text{eq,out}}$, $v_{\text{eq,in}}$ and $v_{\text{eq,out}}$ represent the input source and output load dc currents and dc voltages in the equivalent dc-dc model. Note that according to (4), the input and output powers of the ac-ac system and the equivalent dc-dc model are identical.

The dc-link components and associated quantities, including the dc-link capacitor C_{dc} and the dc-link voltage v_{dc} of ac-ac VSC, as well as the dc-link inductor L_{dc} and the dc-link current i_{dc} of the CSC remain unchanged in the equivalent dc-dc model.[4] Ultimately, the three-phase two-level switching stages of the ac-ac VSC and CSC systems are modeled with a basic half-bridge configuration, which leads to the equivalent dc-dc converter models of **Fig. 2a** for the VSC and **Fig. 2b** for the CSC.

B. Linearization of the DC-DC Models

The obtained dc-dc models are averaged using state-space averaging according to [35], and subsequently linearized around a specific operating point. This facilitates the application of linear circuit analysis and the calculation of system transfer functions, which are important for the design of closed-loop control systems. The resulting linearized models are depicted in **Fig. 2b** for the VSC dc-dc equivalent model and in **Fig. 2d** for the CSC dc-dc equivalent model.

[4]The dc-link inductor, L_{dc}, of the CSC is often split into two parts in practical realizations (including the demonstrator system used here, see **Fig. 14**), i.e., $L_{\text{dc}}/2$ in the positive and $L_{\text{dc}}/2$ in the negative dc rail, to achieve a symmetrical arrangement and suppress common-mode EMI noise. However, this splitting does not affect the control dynamics compared to using a single inductor. Therefore, for simplicity, a single L_{dc} is depicted in the ac-ac CSC topology of **Fig. 1b** and the equivalent dc-dc models of **Fig. 2bd.**

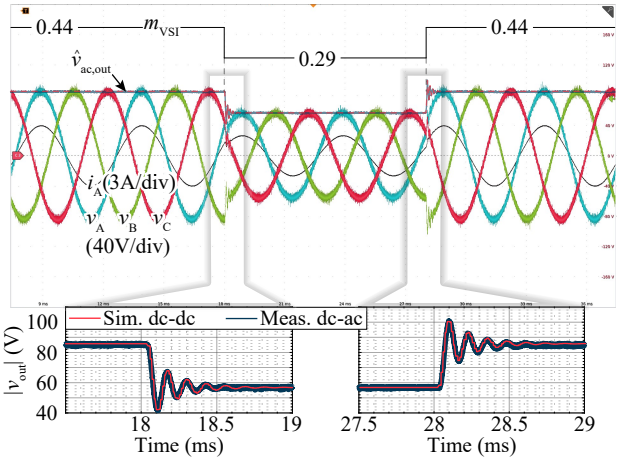

Fig. 3. Measured open-loop response of the dc-ac VSI prototype for 400 V dc-link voltage and a resistive load of 29 Ω: the VSI modulation index m_{VSI} steps from $m_{\text{VSI}} = 0.44$ to $m_{\text{VSI}} = 0.29$ and back again, resulting in the targeted peak load current values of 2 A and 3 A, respectively. The zoomed views show the close match of measured amplitudes (obtained via dq-transformation) and the simulated dc-dc model output voltage response (scaled according to (4)) to corresponding steps in the duty cycle $d_{\text{out,VSC}}$.

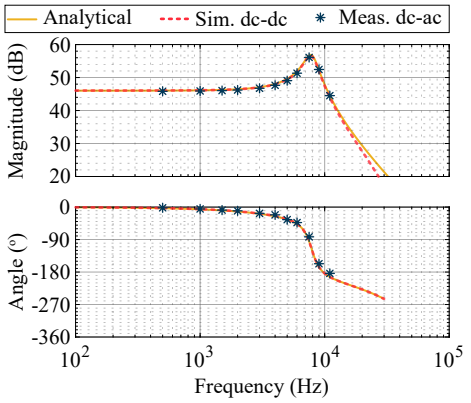

Fig. 4. Measured open-loop frequency response of the output voltage with respect to the modulation index of the dc-ac VSI stage, i.e., $\hat{v}_{\text{ac,out}}(s)/\underline{m}_{\text{VSI}}(s)$, for 400 V dc-link voltage, a 29 Ω load resistance, and $m_{\text{VSI}} = 0.41 \pm 0.01\sin(\omega_{\text{perturb}} \cdot t)$ corresponding to a steady-state operating point with 2 A rms output current. The simulated (PLECS ac sweep) frequency response of the dc-dc equivalent model output voltage to a corresponding perturbation of the duty cycle $d_{\text{out,VSC}}$ shows a close match, as does the transfer function analytically derived from the dc-dc model.

C. Experimental Validation

The derived dc-dc models and their corresponding small-signal models are validated by comparing their simulated open-loop step and frequency responses against ac-ac hardware measurements. Specifically, the transfer function from the modulation index of the output stage to the system output voltage is considered. The details of the two hardware prototypes with specifications according to **Tab. I** are described in [23], [25]. **Tab. II** summarizes the values of the relevant passive components. For the experimental validation, the ac-ac VSC utilizes the standard symmetrical sinusoidal PWM (SPWM), the ac-ac CSC utilzes the well-known space vector modulation (SVM) while the equivalent dc-dc models for both the VSC and the CSC utilize SPWM.

TABLE II
KEY COMPONENTS OF THE AC-AC VSC AND CSC HARDWARE PROTOTYPES USED FOR THE VALIDATION OF THE DC-DC MODELS.

Parameter		Value	Unit
Switching Frequency	f_s	72	kHz
VSC			
1st DM ind.	L_{dm1}, L_{DM1}	291	µH
1st DM cap.	C_{dm1}, C_{DM1}	1.8	µF
2nd DM ind.	L_{dm2}	22	µH
2nd DM cap.	C_{dm2}	3.6	µF
dc-link cap.	C_{dc}	16	µF
CSC			
1st DM ind.	L_{dm1}	220	µH
1st DM cap.	C_{dm1}	3.6	µF
	C_{DM1}	3.26	µF
2nd DM ind.	L_{dm2}	33	µH
2nd DM cap.	C_{dm2}	1.8	µF
dc-link ind.	L_{dc}	1.2	mH

1) VSC: For the VSC hardware, operating VSR in open-loop i.e., without closed-loop control of the grid-side phase inductor currents, can lead to excessively high and potentially damaging grid-frequency currents unless the inductor voltage is precisely controlled, which is challenging to achieve. Therefore, only the VSI stage and the corresponding load-side equivalent dc-dc model (i.e. the equivalent buck converter stage of **Fig. 2a**), with the nominal 400 V dc-source voltage v_{dc} applied to the dc-link capacitor, is considered for the open-loop step and frequency response verification; in **Section III**, the complete dc-dc model for the ac-ac VSC system is further validated under closed-loop control.

Fig. 3 illustrates the open-loop step response of the dc-ac VSI hardware prototype for a step change in the modulation index $m_{VSI} = \hat{v}_{ac,out}/(0.5 \cdot v_{dc})$ from $m_{VSI} = 0.29$ to $m_{VSI} = 0.44$. The step size is selected such that with a constant (nominal) resistive load of 29 Ω, the output peak current increases from 2 A to 3 A (corresponding to an increase of the output voltage amplitude from 58 V to 87 V).

To facilitate a one-to-one comparison of the measurement results with the equivalent dc-dc model simulations, the duty cycle $d_{out,VSC} = v_{eq,out}/v_{dc}$ of the VSC dc-dc model buck stage must be scaled as

$$d_{out,VSC} = \frac{3}{4} \cdot m_{VSI} \tag{5}$$

based on the calculation of m_{VSI} and the relation of $v_{eq,out}$ and $\hat{v}_{ac,out}$ according to (4). Note that a similar relationship exists between the VSR stage modulation index m_{VSR} and the input boost stage duty cycle $d_{in,VSC}$, i.e, $d_{in,VSC} = \frac{3}{4} \cdot m_{VSR}$, where $m_{VSR} = \hat{v}_{ac,in}/(0.5 \cdot v_{dc})$ and $d_{in} = v_{eq,in}/v_{dc}$[5]. According to (2), (4) and (5), the selected step of m_{VSI} from 0.29 to 0.44 corresponds to the duty cycle from $d_{out,VSC} = 0.22$ to $d_{out,VSC} = 0.33$ and to an output dc current and output dc voltage step between 2 A to 3 A and between 87 V to 130.5 V, respectively. The simulated step response is then, scaled down according to (4) to allow a direct comparison with the amplitudes extracted from the hardware measurement via dq-transformation. The zoomed-in view of the step-up and step-down responses shown in **Fig. 3** demonstrates a very close match between the amplitude calculated from the measured three-phase load voltages and the dc voltage output of the equivalent dc-dc model.

[5]Note that the duty cycle for the boost stage i.e., for the dc-dc equivalent of VSR and of CSI, is indicated for the upper switch, as opposed to the low-side switch (see **Fig. 2ac**) as commonly used for a boost converter. This is done to directly relate the duty cycle of the dc-dc stages with the modulation indices of the three-phase system.

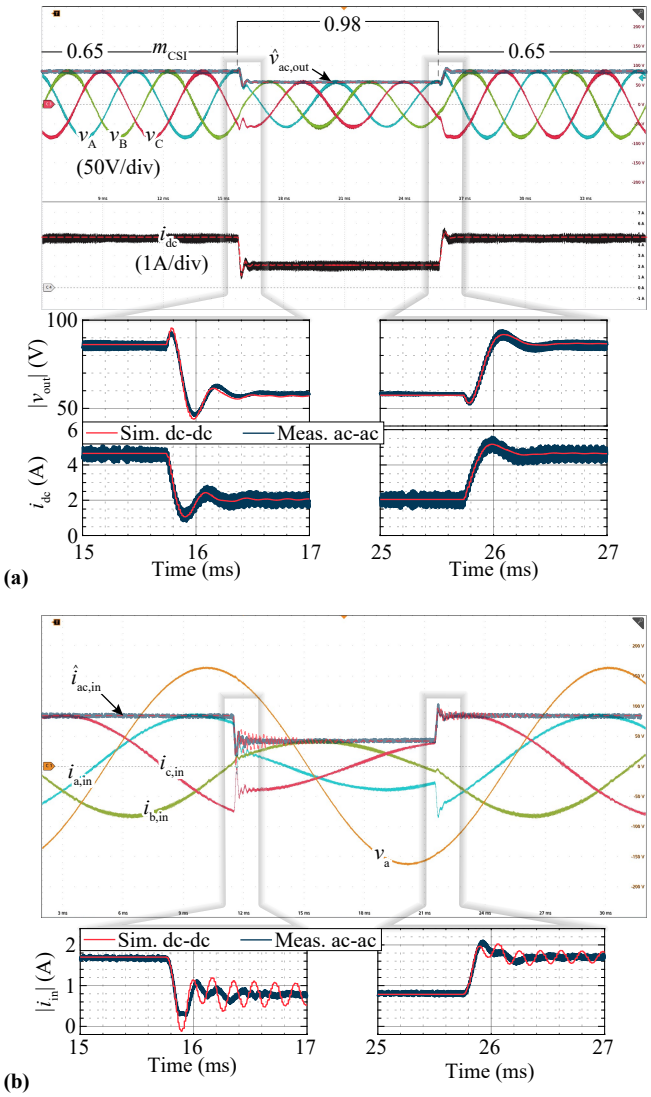

Fig. 5. Measured open-loop response of the ac-ac CSC prototype for 200 V (line-to-line rms) input voltage and a resistive load of 29 Ω: For a fixed CSR modulation index of $m_{CSR} = 0.35$, the CSI modulation index m_{CSI} steps from $m_{CSI} = 0.65$ to $m_{CSI} = 0.98$ and back again, resulting in the targeted load current values of 2 A and 3 A, respectively. **(a)** shows output and dc-link quantities and **(b)** shows input quantities. In both cases, the zoomed views show the close match of measured output voltage and input current amplitudes (obtained via dq-transformation) and the simulated dc-dc model's dc output voltage and dc input current responses to corresponding steps in the duty cycle $d_{out,CSC}$. Similarly, close correspondence is also found between measured and simulated dc-link current responses.

Further, **Fig. 4** presents the measured frequency response of the output voltage $\underline{\hat{v}}_{ac,out}(s)$ with respect to the VSI modulation index $\underline{m}_{VSI}(s)$ for 400 V dc-link voltage, output rms current of 2 A and a resistive load of 29 Ω. To obtain the measurements, a small signal perturbation of $0.01 \sin(\omega_{perturb} \cdot t)$ is superimposed

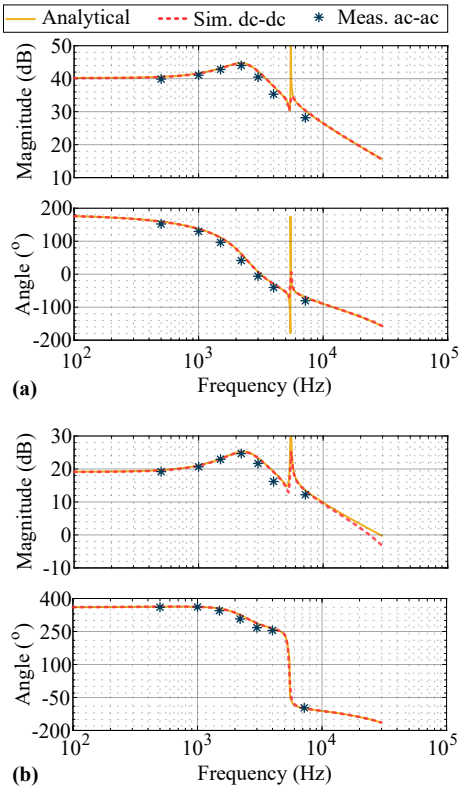

Fig. 6. Measured ac-ac CSC open-loop frequency response of **(a)** the output voltage with respect to the modulation index of the CSI stage, i.e., $G_{\hat{v}\mathrm{ac,out,mCSI}}(s) = \underline{\hat{v}}_{\mathrm{ac,out}}(s)/\underline{m}_{\mathrm{CSI}}(s)$ and **(b)** the dc-link current with respect to the modulation index of the CSR stage, i.e., $G_{\mathrm{idc,mCSR}}(s) = \underline{i}_{\mathrm{dc}}(s)/\underline{m}_{\mathrm{CSR}}(s)$. In both cases, nominal input voltage of 200 V (line-to-line rms) and nominal resistive load of 29 Ω is considered. The steady-state modulation indices $M_{\mathrm{CSR}} = 0.4$ and $M_{\mathrm{CSI}} = 0.79$ result in a steady-state output current of 2 A rms. A small-signal perturbation of $0.01\sin(\omega_{\mathrm{perturb}} \cdot t$ is superimposed on M_{CSI} for **(a)** and on M_{CSR} for **(b)**. A close match with the corresponding analytical (small-signal model) and simulated (PLECS ac sweep) frequency responses of the dc-dc equivalent circuit, i.e., **(a)** of the output dc voltage with respect to the output boost stage duty cycle $\underline{d}_{\mathrm{out,CSC}}(s)$, and **(b)** of $\underline{i}_{\mathrm{dc}}(s)$ with respect to the duty cycle of the input buck stage $\underline{d}_{\mathrm{in,CSC}}(s)$ are observed.

on the steady-state $M_{\mathrm{VSI}} = 0.41$, where $\omega_{\mathrm{perturb}}$ is the frequency of perturbation. The required magnitude and angle of the frequency response of $\underline{\hat{v}}_{\mathrm{ac,out}}(j\omega)$ with respect to $\underline{m}_{\mathrm{VSI}}(j\omega)$ at $\omega_{\mathrm{perturb}}$ is then obtained with the fast Fourier transformation (FFT) of the measured output ac voltage $v_{\mathrm{ac,out}}$ and the m_{VSI} signal. The thus obtained measured frequency response of the three-phase dc-ac VSI again matches closely to that of the simulated dc-dc equivalent circuit.

Further, **Fig. 4** also includes the analytical transfer function $G_{\mathrm{veq,out,dout,VSC}}(s) = \underline{v}_{\mathrm{eq,out}}(s)/\underline{d}_{\mathrm{out}}(s)$ derived from the small-signal model of the dc-dc model's output buck stage (see **Fig. 2b**), also matching closely with the measurements.

2) CSC: In contrast to the VSC, both stages of the CSC, i.e., CSR and CSI, can be operated safely in open-loop. **Fig. 5** shows the open-loop measurement results for the CSR modulation index fixed to $m_{\mathrm{CSR}} = \hat{i}_{\mathrm{ac,in}}/i_{\mathrm{dc}} = 0.35$, whereas the CSI modulation index $m_{\mathrm{CSI}} = \hat{i}_{\mathrm{ac,out}}/i_{\mathrm{dc}}$ is stepped from $m_{\mathrm{CSI}} = 0.65$ to $m_{\mathrm{CSI}} = 0.98$ and back; the values are selected such that the output current changes between from 2 A and 3 A for a nominal line-to-line input voltage of $V_{\mathrm{gn}} = 200$ V and a nominal load resistance of 29 Ω; the resulting output voltage amplitudes then change between 58 V and 87 V as in the VSI case discussed above.

Note that also the dc-link current and the ac input current amplitude directly follow the steps in m_{CSI} as dictated by the power balance at the two ac and the dc interfaces of the CSC.

Further, **Fig. 5** also compares the measurement results against simulation results of the dc-dc equivalent circuit for a corresponding dc input voltage of $v_{\mathrm{eq,in}} = 244$ V and a corresponding step change of the duty cycle $d_{\mathrm{out,CSC}} = i_{\mathrm{out,eq}}/i_{\mathrm{dc}}$ from $d_{\mathrm{out,CSC}} = 0.65$ to $d_{\mathrm{out,CSC}} = 0.98$ and back. Note that, unlike for VSC, there is no additional scaling required between $d_{\mathrm{out,CSC}}$ and m_{CSI}. According to (4), this operating point corresponds to a step change in output dc current and output dc voltage from 2 A to 3 A and from 87 V to 130.5 V, respectively. Thus, as with the VSI, the simulated step response of the dc-dc model is scaled-down according to (4) to enable a direct comparison with the ac-ac hardware measurements: The zoomed-in view of the step-up and step-down responses demonstrate excellent alignment between the amplitudes (obtained via dq-transformation) of the measured three-phase load voltage, grid current[6] and the dc-link current of the ac-ac hardware, and the corresponding simulated dc output voltage, dc input current, and dc-link current of the equivalent dc-dc model.

Finally, **Fig 6a** displays the measured frequency response of the output voltage $\underline{\hat{v}}_{\mathrm{ac,out}}(s)$ with respect to the CSI modulation index $\underline{m}_{\mathrm{CSI}}(s)$, and **Fig 6b** shows the frequency response of the dc-link current $\underline{i}_{\mathrm{dc}}(s)$ with respect to the CSR modulation index $\underline{m}_{\mathrm{CSR}}(s)$. In both cases, the steady-state modulation indices of $M_{\mathrm{CSI}} = 0.79$, $M_{\mathrm{CSR}} = 0.4$ are used with a nominal input voltage of 200 V (line-to-line rms) and a nominal resistive load of 29 Ω resulting in load current of 2 A rms. A small-signal perturbation of $0.01\sin(\omega_{\mathrm{perturb}} \cdot t)$ is superimposed on M_{CSI} for the frequency response measurement $G_{\hat{v}\mathrm{ac,out,mCSI}}(s) = \underline{v}_{\mathrm{ac,out}}(s)/\underline{m}_{\mathrm{CSI}}(s)$ (**Fig 6a**) and on M_{CSR} for the frequency response measurement $G_{\mathrm{idc,mCSR}}(s) = \underline{i}_{\mathrm{dc}}(s)/\underline{m}_{\mathrm{CSR}}(s)$ (**Fig 6a**). Similar as for the VSC, $\omega_{\mathrm{perturb}}$ is the frequency of perturbation. The required magnitude and angle of the frequency response of $\underline{\hat{v}}_{\mathrm{ac,out}}(j\omega)$ with respect to $\underline{m}_{\mathrm{CSI}}(j\omega)$ and of $\underline{i}_{\mathrm{dc}}(j\omega)$ with respect to $\underline{m}_{\mathrm{CSR}}(j\omega)$ at $\omega_{\mathrm{perturb}}$ is then obtained with the FFT of the measured output ac voltage $v_{\mathrm{ac,out}}$, m_{CSI}, the measured dc-link current i_{dc}, and m_{CSR}. These measurements are compared with the simulated frequency responses obtained with the dc-dc model, i.e., of the output voltage $\underline{v}_{\mathrm{eq,out}}(s)$ with respect to the output duty cycle $\underline{d}_{\mathrm{out,CSC}}(s)$ and the dc-link current with respect to the input duty cycle $\underline{d}_{\mathrm{in,CSC}}(s)$. **Fig. 6** also includes a comparison of the theoretically derived transfer functions $\underline{v}_{\mathrm{eq,out}}(s)/\underline{d}_{\mathrm{out}}(s)$ and $\underline{i}_{\mathrm{dc}}(s)/\underline{d}_{\mathrm{in}}(s)$, based on the small-signal model of **Fig. 2d**. Both, dc-dc simulation and analytical transfer functions closely match the corresponding measurements of the three-phase ac-ac CSC.

[6]Note that the difference in the ringing amplitude of the measured grid current and the simulated input current is due to the undamped first stage input LC filter operated in open-loop. The unavoidable parasitic damping effects that are present in the hardware are not modeled in the dc-dc simulations. However, the rise and fall times of the measured grid current and the simulated input current match very well.

III. Control Design

With the dc-dc equivalent models experimentally verified, they can advantageously be employed for the design of closed-loop control systems for both, the VSC and the CSC. The motor inverter of a VSD is essentially a controllable voltage source. Hence, a typical cascaded control system features an outer motor speed control loop that calculates motor current references, and an inner motor current control loop that generates the output voltage reference for the motor inverter (see **Fig. 7** and **Fig. 9**). Therefore, the control objective for a VSC and a CSC motor drive is to regulate the output load voltage to the desired reference value obtained from the motor control system while ensuring that the grid currents remain in phase with the grid voltage. Note that motor speed and current control loops are not further considered here since they are identical for VSC and CSC systems and thus not pertinent to the targeted comparative analysis. Further, given the high cut-off frequency of the 2nd stage input EMI filters (≈18 kHz for VSC and ≈21 kHz for CSC) and the implemented passive LR parallel damping circuit, these filter stages can be ignored for the basic control considerations presented here.

The control design approach employs widely adopted and straightforward control structures that incorporate a combination of feedback and feedforward paths. All controllers are optimized to meet the following performance criteria:

1) Minimum phase margin of 45°.
2) Maximum overshoot of 30%.

The control bandwidth of the output voltage is then maximized while ensuring compliance with these criteria, using MATLAB's PID tuner.

A. VSC Control Design

The high-level control system for the VSC from **Fig. 1a** is shown in **Fig. 7**. The output voltage reference v_o^* is generated by the outer motor speed controller and the dc-link voltage reference v_{dc}^* is set to a fixed value of 400 V, providing approximately 20% modulation reserve for control at the nominal operating point from **Tab. I**, where both, m_{VSR} and m_{VSI} are 0.81. Based on the results of the previous section, the controllers for the VSC can thus be designed considering the equivalent dc-dc converter model from **Fig. 2ac**. There, the control of the boost and buck stages is decoupled by the dc-link capacitor[7] such that the buck stage regulates the output voltage assuming a constant dc-link voltage and the boost stage controls the dc-link voltage to its reference value, as depicted in **Fig. 8**.

1) Buck output stage control: The buck stage control, illustrated in **Fig. 8**, is implemented with a well-known cascaded two-loop control structure (see, e.g. [10]). The inner current control loop regulates the output filter inductor current i_{LEQ1} to its reference value i_{LEQ1}^*, which is set by the outer voltage control loop that controls the output voltage to the reference v_o^* obtained from the higher-level motor current controller (see **Fig. 7**). The inclusion of feedforward terms is known to improve the control bandwidth [36], [37]. Accordingly, the inner current control loop includes the feedforward of the measured output voltage v_o, while the outer voltage loop incorporates the feedforward of the measured load current i_o, i.e., the current reference i_{LEQ1}^* for the inner current controller results as the sum of i_o and the output of the voltage controller i_{CEQ1}^*.

With the feedforward of the measured output voltage, the plant transfer function for the inner current control loop $G_{VI}(s)$ is simply given by the filter inductor L_{EQ1}, i.e., $G_{VI}(s) = 1/(sL_{EQ1})$ and therefore, a simple P controller suffices, which is even found to enable higher bandwidth than a PI controller when used in cascade with an outer PI controller [36]. Given a switching frequency f_s of 72 kHz and a total delay of 1.75 switching periods (including measurement sampling: half a switching period, computation time: one switching period, and PWM update with regular single update PWM: a quarter of a period) modeled with the transfer function $G_{delay}(s) = \exp(-1.75s/f_s)$, a proportional gain $K_{P,VI} = 14.5$ V/A is selected achieving a phase margin of approximately 45° and a control bandwidth of around 5.3 kHz. The outer voltage control loop is designed using a PI controller of the form $K_{P,VV} + K_{I,VV}/s$, optimized for a worst case no-load condition, taking into account the dynamics of the inner current control loop and the feedforward of the measured output current with the plant transfer function $G_{VV}(s)$ as

$$G_{VV}(s) = \frac{G_{VI,Loop}(s) \cdot G_{CEQ1}(s)}{[1 + G_{VI,Loop}(s) + G_{VI}(s) \cdot G_{CEQ1}(s) - G_{VI}(s) \cdot G_{CEQ1}(s) \cdot G_{delay}(s)],} \quad (6)$$

where $G_{VI,Loop}(s) = G_{VI}(s) \cdot K_{P,VI} \cdot G_{delay}(s)$ is the inner current control loop gain and $G_{CEQ1}(s) = 1/(sC_{EQ1})$. The controller gains $K_{P,VV} = 0.029$ A/V and $K_{I,VV} = 153.5$ A/Vs result in an outer voltage control bandwidth of 1.8 kHz and a phase margin of around 52°.

2) Boost input stage control: Similar to the buck stage control, the boost stage control is also implemented using a cascaded two-loop control structure as shown in **Fig. 8**. The inner current control loop regulates the boost inductor current i_{Leq1} to the reference value i_{Leq1}^* set by the outer voltage control loop, which maintains the dc-link voltage at v_{dc}^*. The inner current control includes the feedforward of the voltage measured across the first stage filter capacitor v_{Ceq1}, simplifying the plant transfer function $G_{Vi}(s)$ to the first stage filter inductor L_{eq1}, i.e., $G_{Vi}(s) = 1/(sL_{eq1})$. Since $L_{eq1} = L_{EQ1}$, the same proportional controller used for the buck stage's inner loop, $K_{P,Vi} = 14.5$, is selected. The load current for the boost stage, i.e., the input current of the buck stage $i_{dc,in}^*$, calculated based on the output power according to

$$i_{dc,in}^* = \frac{i_o \cdot v_o}{v_{dc}^*}, \quad (7)$$

is used as a feedforward term in the dc-link voltage controller. The dc-link voltage controller is designed with a PI controller, $K_{P,Vv} + K_{I,Vv}/s$, considering the dynamics of the inner current

[7]Even for compact realizations of the dc-link capacitor, e.g., with MLCCs, the resulting capacitance and stored energy is high enough to achieve a good decoupling of the two stages.

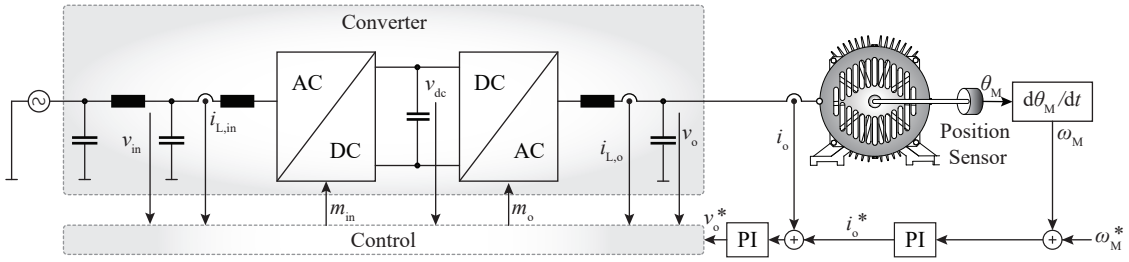

Fig. 7. Overview of a VSC driving a motor with an exemplary cascaded motor speed and current control implementation that generates the output voltage reference v_o^* for the VSC. The VSC output voltage control structure is then further detailed in **Fig. 8**.

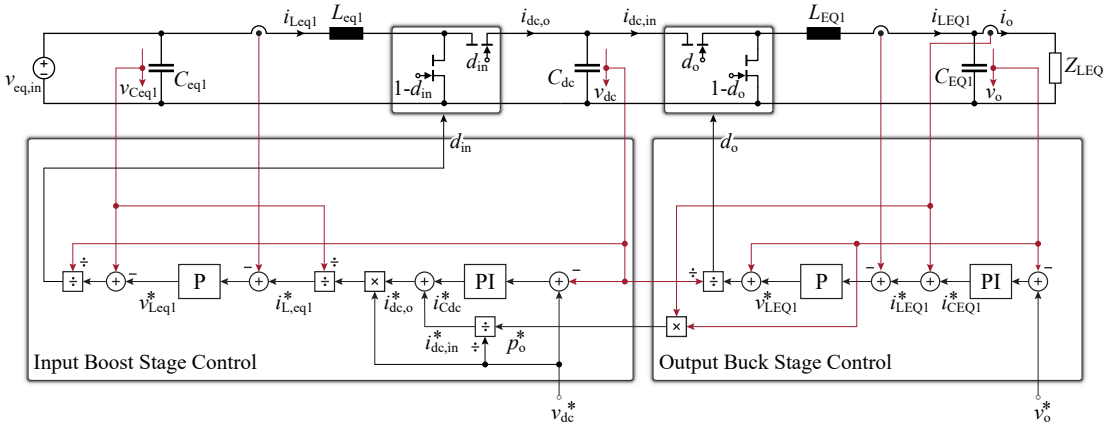

Fig. 8. Output voltage and input current control block diagram of the VSC; here shown together with the VSC equivalent dc-dc model (see **Fig. 2ac**) that is advantageously utilized for the design of the controllers. The 2nd stage input EMI filter is not considered for the control design due to its high cut-off frequency and hence, is not shown here.

control loop and the feedforward, optimized for no-load condition with the plant transfer function $G_{\mathrm{Vv}}(s)$ as

$$G_{\mathrm{Vv}}(s) = \frac{G_{\mathrm{Vi}}(s) \cdot K_{\mathrm{P,Vi}} \cdot G_{\mathrm{delay}}(s)}{[1 + G_{\mathrm{Vi}}(s) \cdot K_{\mathrm{P,Vi}} \cdot G_{\mathrm{delay}}(s)] \cdot sC_{\mathrm{dc}}}, \tag{8}$$

resulting in the controller gains $K_{\mathrm{P,Vv}} = 0.078\,\mathrm{A/V}$ and $K_{\mathrm{I,Vv}} = 4.31\,\mathrm{A/Vs}$. The sum of $i^*_{\mathrm{dc,in}}$ and the output of dc-link voltage controller i^*_{Cdc} forms the reference output current of the boost stage $i^*_{\mathrm{dc,o}}$. From this, i^*_{Leq1} is calculated based on power balance according to:

$$i^*_{\mathrm{Leq1}} = \frac{v^*_{\mathrm{dc}} \cdot i^*_{\mathrm{dc,o}}}{v_{\mathrm{Ceq1}}}. \tag{9}$$

B. CSC Control Design

Fig. 9 shows the high-level control system for the CSC from **Fig. 1b**. The output voltage reference v_o^* is generated by the outer motor speed controller, and the dc-link current reference i^*_{dc} can either be set to a constant value similar to the dc-link voltage in the VSC, e.g., to 7 A to maintain a 20% modulation reserve at the nominal operating point (both, m_{CSR} and m_{CSI} are 0.8 at the nominal operating point from **Tab. I**) or to a varying value proportional to the load current amplitude i_o. There is a trade-off between the overall system efficiency and the control dynamics amongst the two options for selecting the dc-link current reference i^*_{dc}: A constant i^*_{dc} at the nominal values enables faster control dynamics compared to selecting i^*_{dc} proportional to i_o, however, at the expense of reduced overall system efficiency [38]; this is discussed in detail in **Section IV**.

The control structure for both the cases, however, is identical; the CSC control is implemented such that the output boost stage regulates the output voltage v_o, assuming a constant dc-link current[8], while the input buck stage controls the dc-link current i_{dc} to its reference value i^*_{dc}. Based on the results of the previous section, the controllers for the CSC are designed using the equivalent dc-dc converter model from **Fig. 2bd**, as illustrated in **Fig. 10**.

1) Boost output stage control: As illustrated in **Fig. 10**, the output voltage control is implemented using a PI controller incorporating feedforward of the load current i_o, where the plant transfer function $G_{\mathrm{CV}}(s)$ is given by the output capacitor: $G_{\mathrm{CV}}(s) = 1/(sC_{\mathrm{EQ1}})$. To ensure that the output duty cycle d_o remains in the realizable range of $0 \ldots 1$, the output of the voltage controller i^*_{CEQ1} is constrained between a maximum value of $i^*_{\mathrm{dc}} - i_o$ (corresponding to max $d_o = 1$) and a minimum value of $-i_o$ (corresponding to min $d_o = 0$) with an anti-windup implemented to prevent the excessive integral of the error when these limits are applied. Given the switching frequency f_s of 72 kHz and the associated total delay of 1.75 switching periods (as discussed above for the case of the VSC, i.e., with $G_{\mathrm{delay}}(s) = \exp(-1.75s/f_s)$), a PI controller of the form $K_{\mathrm{P,CV}} + K_{\mathrm{I,CV}}/s$ with gains $K_{\mathrm{P,CV}} = 0.068\,\mathrm{A/V}$ and $K_{\mathrm{I,CV}} = 37.5\,\mathrm{A/Vs}$ achieves a bandwidth of 5 kHz and a phase margin of 45°.

[8]This is true for small-signal analysis where the energy stored in the dc-link inductor suffices without causing significant changes in the dc-link current. For a large signal analysis though, the control dynamics of the CSC are restricted by the limited energy of the dc-link inductor, see **Section IV**.

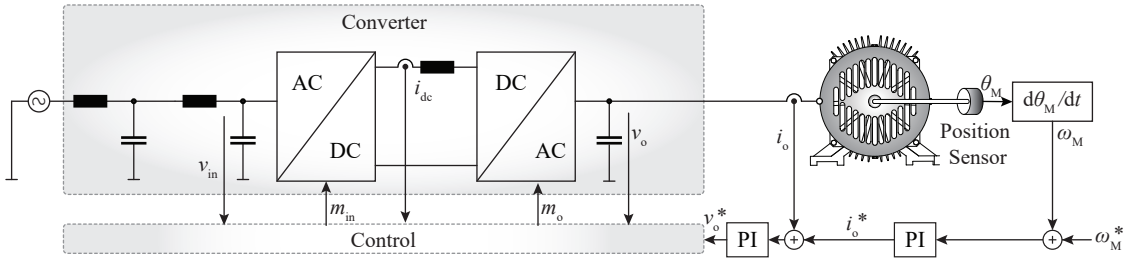

Fig. 9. Overview of a CSC driving a motor with an exemplary motor speed and current control implementation that generates the output voltage reference v_o^* for the CSC. The CSC output voltage control structure is then further detailed in **Fig. 10**

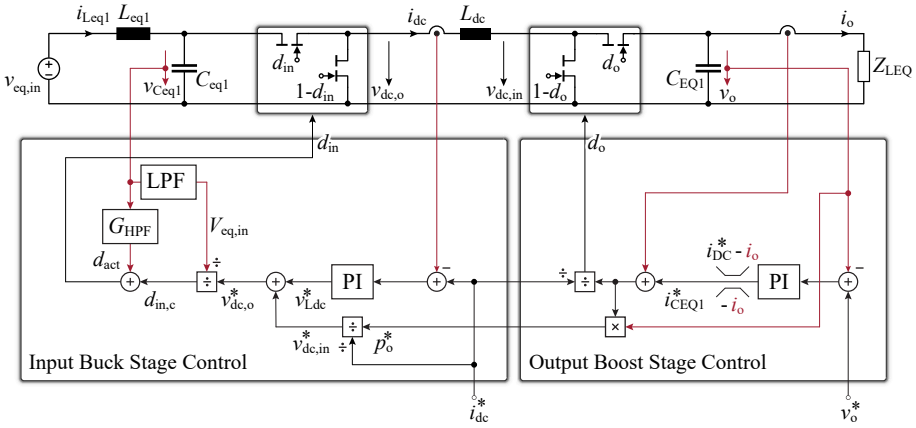

Fig. 10. Output voltage and input current control block diagram of the CSC; here shown together with the CSC equivalent dc-dc model (see **Fig. 2bd**) that is advantageously utilized for the design of the controllers. The 2nd stage input EMI filter is not considered for the control design due to its high cut-off frequency and hence, is not shown here.

2) Buck input stage control: There are two options to implement the control of the buck stage:

- Closed-loop control the dc-link current i_{dc} and (open-loop) generation of the input filter inductor current i_{Leq1} via modulation of the switching stage with the input duty cycle d_{in} [39], [40]; this method further requires active or passive damping of the first-stage input filter resonance.
- Closed-loop control of the input filter inductor current i_{Leq1} in cascade with closed loop-control of the input filter capacitor voltage v_{Ceq1} [33]; the dc-link current is indirectly controlled.

Of these two options, directly controlling the dc-link current is found to provide better control tracking and disturbance rejection [33] and is therefore used in this paper (see **Fig. 10**). The dc-link current is regulated to its reference value i_{dc}^* by means of adjusting the voltage v_{Ldc}^* applied to the dc-link inductor, using a PI controller. This voltage is the difference between the (average) dc input voltage of the output boost stage and the (average) dc output voltage of the input buck stage. Therefore, the average input voltage of the output boost stage $v_{dc,in}^*$, calculated based on the output power as

$$v_{dc,in}^* = \frac{(i_o + i_{CEQ1}^*) \cdot v_o}{i_{dc}^*}, \tag{10}$$

is used as a feedforward term in the dc-link current controller. The sum of the output of the dc-link current controller v_{Ldc}^* and the feedforward $v_{dc,in}^*$ forms the reference average output voltage $v_{dc,o}^*$ of the buck stage which is used to calculate the switching-stage duty-cycle $d_{in,c}$ according to

$$d_{in,c} = \frac{v_{dc,o}^*}{V_{eq,in}}, \tag{11}$$

where $V_{eq,in}$ is the low-pass filtered capacitor voltage (or the nominal grid voltage obtained with a PLL [41] for the three-phase ac input.)

Without active control of the input filter components (i.e., L_{eq1} and C_{eq1}), this, however, results in a right-half-plane zero (RHPZ) pair in the transfer function of i_{dc} to the controlled input duty cycle $d_{in,c}$, calculated from the small signal model of **Fig. 2d** as

$$\begin{aligned} G_{idc,dinc}(s) &= \frac{\underline{i}_{dc}(s)}{\underline{d}_{in,c}(s)} \\ &= \frac{s^2 L_{eq1} C_{eq1} V_{Ceq1} - s L_{eq1} D_{in} I_{dc} + V_{Ceq1}}{[s^3 L_{DC} L_{eq1} C_{eq1} + s^2 L_{eq1} C_{eq1} D_o^2 Z_o + \\ &\quad s(L_{DC} + D_{in}^2 L_{eq1}) + D_o^2 Z_o]}. \end{aligned} \tag{12}$$

Solving for the RHPZ results in

$$s = \frac{L_{eq1} D_{in} I_{dc} \pm \sqrt{(L_{eq1} D_{in} I_{dc})^2 - 4 L_{eq1} C_{eq1} V_{Ceq1}^2}}{2 L_{eq1} C_{eq1} V_{Ceq1}}. \tag{13}$$

The system specifications and components listed in **Tab. I** and **Tab. II**, respectively, result in a complex RHPZ pair and a pole pair at very similar frequencies, which corresponds to a 180° phase drop at the RHPZ frequency (= 5.7 kHz at 100% load)

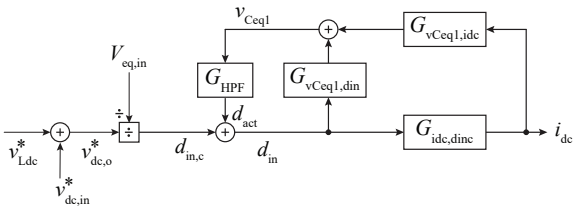

Fig. 11. The block diagram for the active damping of the input filter of CSC utilizing the first stage filter capacitor's voltage measurement.

and another 180° at the pole pair frequency (= 6.2 kHz at 100% load, see the dotted transfer function in **Fig. 12**). Therefore, it cannot be stabilized by a simple PI controller at the complex RHPZ-pair and pole-pair frequencies, and the bandwidth of the PI controller must be set lower than this frequency. As a side note, it is possible for the the transfer function (12) to have two real RHPZ at two different frequencies (instead of a complex RHPZ pair occuring at the same frequency) based on (13) if $(L_{eq1}I_{Leq1})^2 - 4L_{eq1}C_{eq1}V^2_{Ceq1} > 0$ (replacing I_{Leq1} for $D_{in}I_{dc}$) resulting in

$$\frac{1}{2}C_{eq1}V^2_{Ceq1} < \frac{1}{4}\left[\frac{1}{2}L_{eq1}I^2_{Leq1}\right]. \tag{14}$$

I.e., if the energy stored in the first-stage input filter capacitor is less than 1/4th of the energy stored in first-stage input filter inductor, $G_{idc,dinc}$ shows two real RHPZ at different frequencies, which is easier to control compared to a complex pair in the case at hand. It should be noted, however, that it is not possible to stabilize any of the zeros by moving it to left-hand side of the s-plane without resorting to (lossy) passive damping. Therefore, there will always be two RHPZ when directly controlling the dc-link current of the input buck stage (or CSR stage for ac-dc converter) in presence of an undamped input LC filter.

In order to realize a stable control system, thus either active or passive damping of the input filter is required. Passive damping, as mentioned earlier, can potentially move the RHPZ to the left-hand side of the s-plane, enabling higher control bandwidth but at the cost of either bulky capacitor in case of RC damping circuit, in parallel to input filter capacitor resulting in reduced power density (and reactive power in the ac system), or a loss of high frequency attenuation in case of an RL damping circuit, in parallel to the input filter inductor [42]. To avoid these issues, we utilize active damping in this work. There are different ways of implementing active damping of the input LC filter such as filter inductor voltage feedback (requiring an additional inductor voltage measurement) [43], limiting the rate of rise of the ac current references (requiring an additional filter inductor current measurement) [39], and high-pass filtered capacitor voltage feedback [33], [44], [45]. Utilizing the high-pass filtered capacitor voltage has been proven effective and requires the measurement of the filter capacitor voltage only, which is anyway present, e.g., for grid synchronization and the calculation of the buck stage duty cycle as discussed above. Therefore, no extra measurements are needed and thus, this method is considered here.

With active damping, the final duty cycle for the input buck stage is the sum of the contribution from the dc-link current controller $d_{in,c}$ and the active damping d_{act}, i.e., $d_{in} = d_{in,c} + d_{act}$. **Fig. 11** shows the implementation of the active damping, where $G_{vCeq1,idc}(s) = \underline{v}_{Ceq1}(s)/\underline{i}_{dc}(s)$ from i_{dc} to v_{Ceq1}, and $G_{vCeq1,din}(s) = \underline{v}_{Ceq1}(s)/\underline{d}_{in}(s)$ from d_{in} to v_{Ceq1}, respectively, and G_{HPF} is a simple first order high-pass filter multiplied with a damping factor K_d. Finally, from **Fig. 10** and **Fig. 11**, the transfer function of the plant (including the active damping) to be controlled by the dc-link current controller results in

$$G_{idc,vLdc^*}(s) = \frac{\underline{i}_{dc}(s)}{\underline{v}^*_{Ldc}(s)} = \frac{G_{idc,dinc}/V_{eq,in}}{[1 - G_{idc,dinc}\cdot G_{vCeq1,idc}\cdot G_{HPF} - G_{vCeq1,din}\cdot G_{HPF}]}, \tag{15}$$

where

$$G_{vCeq1,idc}(s) = -\frac{sL_{eq1}D_{in}}{s^2L_{eq1}C_{eq1}+1},$$
$$G_{vCeq1,din}(s) = -\frac{sL_{eq1}I_{DC}}{s^2L_{eq1}C_{eq1}+1},$$
$$G_{HPF}(s) = \frac{K_d\cdot s/\omega_c}{s/\omega_c+1}.$$

The negative expressions for $G_{vCeq1,idc}$ and $G_{vCeq1,din}$ result in the stabilizing negative feedback of the high-pass filtered v_{Ceq1}. The cut-off frequency ω_c of G_{HPF} should be chosen lower than the input filter resonance frequency but higher than the grid frequency, in case of three-phase system and is thus selected at 1 kHz[9].

Fig. 12 shows the plant transfer function $G_{idc,vLdc^*}$ at the nominal operating point for varying values of the damping factor K_d, where $K_d = 0$ implies no active damping. From **Fig. 12**, it is clear that increasing K_d provides higher damping, however, at the cost of lower phase (margin) and hence reduced achievable control bandwidth. Therefore, $K_d = 0.0035$ is selected. With that, **Fig. 13** shows the comparison between $G_{idc,vLdc^*}$ simulated with PLECS ac-sweep analysis and $G_{idc,vLdc^*}$ calculated using the derived analytical expression of (15) at the nominal operating point, showing an excellent match. In addition, **Fig. 13** also shows $G_{idc,vLdc^*}$ at 10% of the nominal load current. As the plant gain is lower at higher load current (e.g., nominal as indicated), the controller is designed for the nominal load case with a PI controller of the form $K_{P,Ci} + K_{I,Ci}/s$ for the plant transfer function of (15). The gains $K_{P,Ci}$ = 20 A/V and $K_{I,Ci} = 110.2 \times 10^3$ A/Vs result in a bandwidth of 2.7 kHz and a phase margin of 45°.

C. Experimental Verification with AC-AC VSC and CSC

The closed-loop controllers conveniently designed using the dc-dc equivalent circuits are now verified with the ac-ac VSC and CSC hardware prototypes shown in **Fig. 14** with specifications given in **Tab. I** and **Tab. II**.

1) VSC: **Fig. 15** shows closed-loop measurements of the ac-ac VSC operating with nominal resistive load of 29 Ω and with steps in the output voltage amplitude reference from 87 V to 58 V; this results in output current amplitude levels of 3 A and 2 A, respectively. Note that the controller gains obtained from

[9]Note that active damping is only required for the input stage.

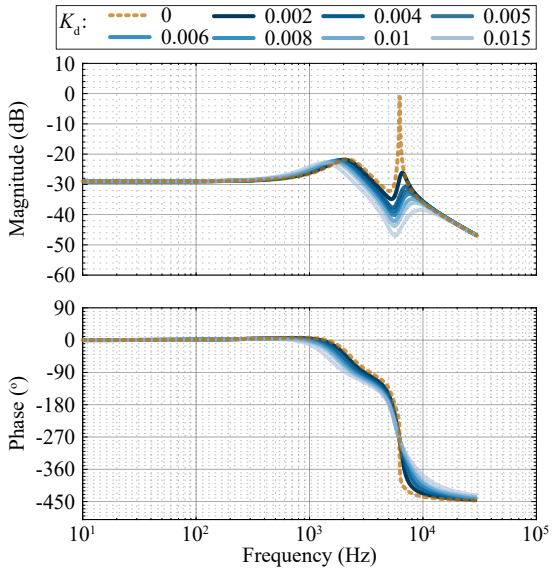

Fig. 12. Bode diagram of the plant transfer function (15) for the dc-link current controller of the CSC dc-dc equivalent circuit for varying damping factor K_d. $K_d = 0$ corresponds to the case without active damping.

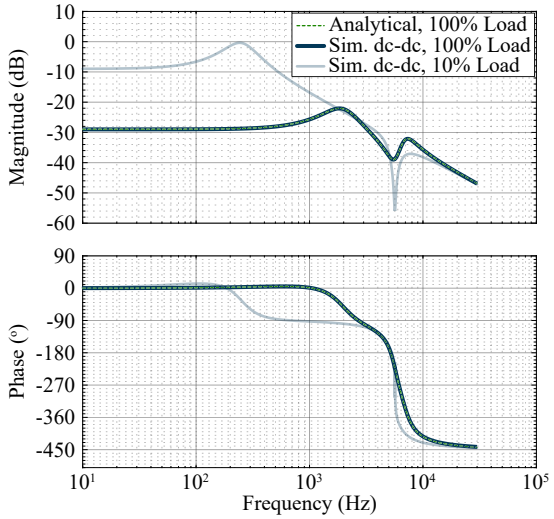

Fig. 13. Bode diagram of the plant transfer function (15) for the dc-link current controller of the CSC dc-dc equivalent circuit for nominal (100%) load current, nominal output voltage of the overall system, and active damping factor $K_d = 0.005$. In addition to the calculated curve, also simulation results (PLECS ac-sweep analysis) for 100% and 10% load current are shown; the former matches the simulation results very closely.

the dc-dc equivalent model as discussed above are directly used in the implementation of the ac-ac VSC controllers in a Xilinx Zynq SoC. **Fig. 17a** then compares the measured step-responses of the dc-link voltage, the output voltage amplitude and the input current amplitude (both extracted via dq-transformation) with the respective quantities obtained from simulations of the dc-dc equivalent circuit of the VSC (see also **Section II-C** for details on the required scalings for the comparison). A very close match confirms the validity of the control design conveniently carried out using the dc-dc equivalent models.

2) CSC: To implement the closed-loop control designed with the equivalent dc-dc model for the three-phase ac-ac CSC system, the output voltage controller gains $K_{P,CV}$, $K_{I,CV}$ and the

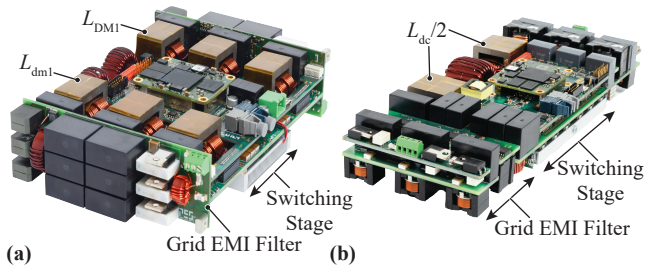

Fig. 14. Top view of the **(a)** VSC and **(b)** CSC demonstrator prototype utilized to verify the open-loop and closed-loop performance of the designed controller. Note that some of the output filter components were removed from the prototype to match the topology structures of **Fig. 1** (component values according to **Tab. II**)

high-pass filter damping factor K_d must be scaled by a factor of 1.5 for implementation in the ac-ac CSC control system. This is because the output voltage error and high-pass filtered v_{Ceq1} directly contribute to the duty cycle calculations, which for the CSC are defined by the ratio of ac-currents to dc-link current. Since the amplitude of the ac-side voltages are scaled by a factor of 1.5 in the equivalent dc-dc model while the amplitude of ac-side currents is kept the same according to (4), $K_{P,CV}$, $K_{I,CV}$ and K_d must be scaled accordingly.

Note further that the ac-ac CSC hardware utilizes the first-generation 600 V, 140 mΩ GaN M-BDS, which have reliably been tested to switch the dc-link current i_{dc} until 6 A. In order to not exceed this safe current limit of 6 A during step responses, the steady-state i_{dc} is maintained at 5 A for the hardware measurements. **Fig. 16** shows the closed-loop measurements of the ac-ac CSC operating with nominal resistive load of 29 Ω and with steps in the output voltage reference from 87 V to 58 V; this results in output current amplitude levels of 3 A and 2 A, respectively. **Fig. 17b** finally shows the comparison of the measured closed-loop step-up response of the dc-link current, the output voltage amplitude and the input current amplitude (both extracted via dq-transformation) against the respective quantities obtained from simulations of the dc-dc equivalent circuit of the CSC (see also **Section II-C** for details on the required scalings for the comparison). Again, a very close match is observed.

IV. Comparative Analysis

As indicated by the experimental results presented in the previous section and specifically by **Fig. 17**, the dc-dc equivalent circuits of both, the VSC and the CSC accurately capture the respective system dynamics, facilitate the design of closed-loop control systems, and the evaluation of the closed-loop control dynamics performance. Therefore, this section utilizes the dc-dc models, with the simulation values also corresponding to the dc-dc models, for the comparative evaluation of the output voltage control performance between the VSC and the CSC system with specifications and key component values given in **Tab. I** and **Tab. II**, respectively.

The controller gains derived in **Section III** for both systems using identical paradigms are summarized in **Tab. III** for convenience. Note that there are two different sets of controller gains for two different CSC realization variants: Given

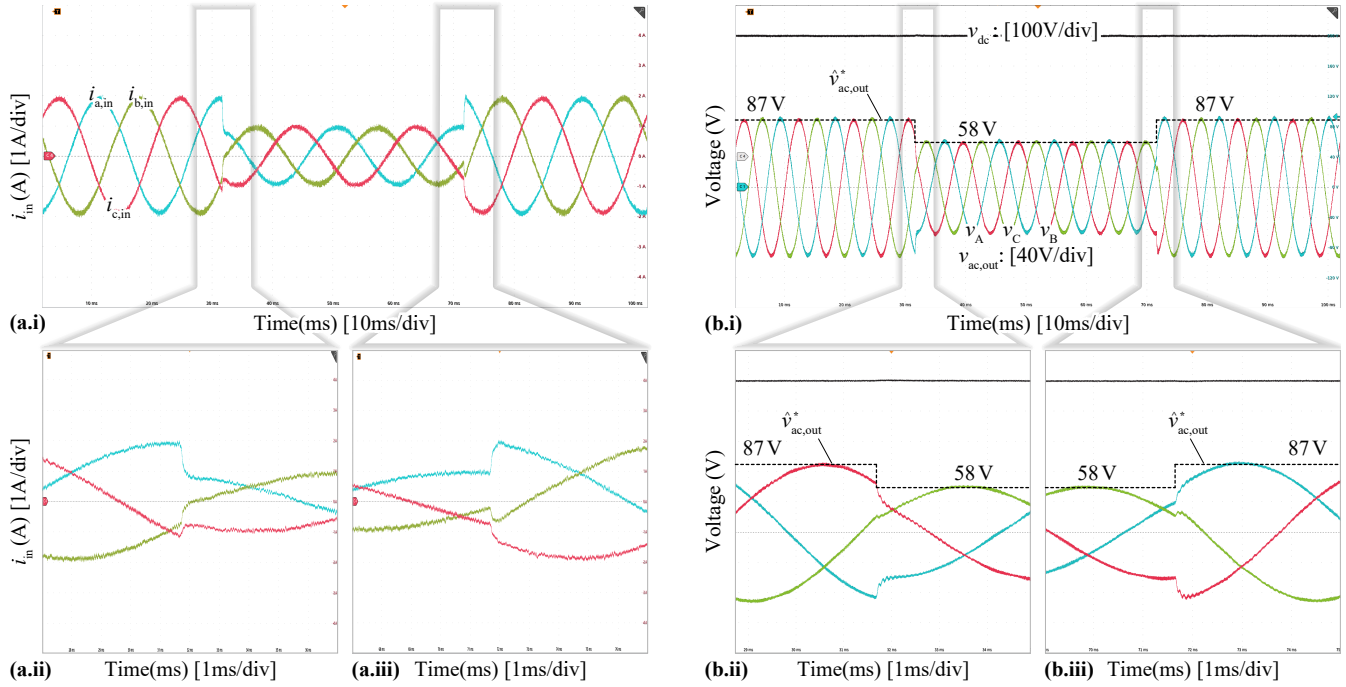

Fig. 15. Measured closed-loop step response of the VSC for a step in the output voltage amplitude reference from 87 V to 58 V and back, resulting in current amplitude levels of 3 A and 2 A with the nominal load of 29 Ω. The grid voltage is at the nominal value of 115 V (phase-to-neutral rms), and the dc-link reference voltage is 400 V. **(a.i)** shows the three-phase grid currents $i_{a,in}$, $i_{b,in}$ and $i_{c,in}$ with zoomed views of the steps given in **(a.ii)** and **(a.iii)**. **(b.i)** shows the three-phase load voltages v_A, v_B, v_C and the dc-link voltage v_{dc} with zoomed views of the steps highlighted in **(b.ii)** and **(b.iii)**.

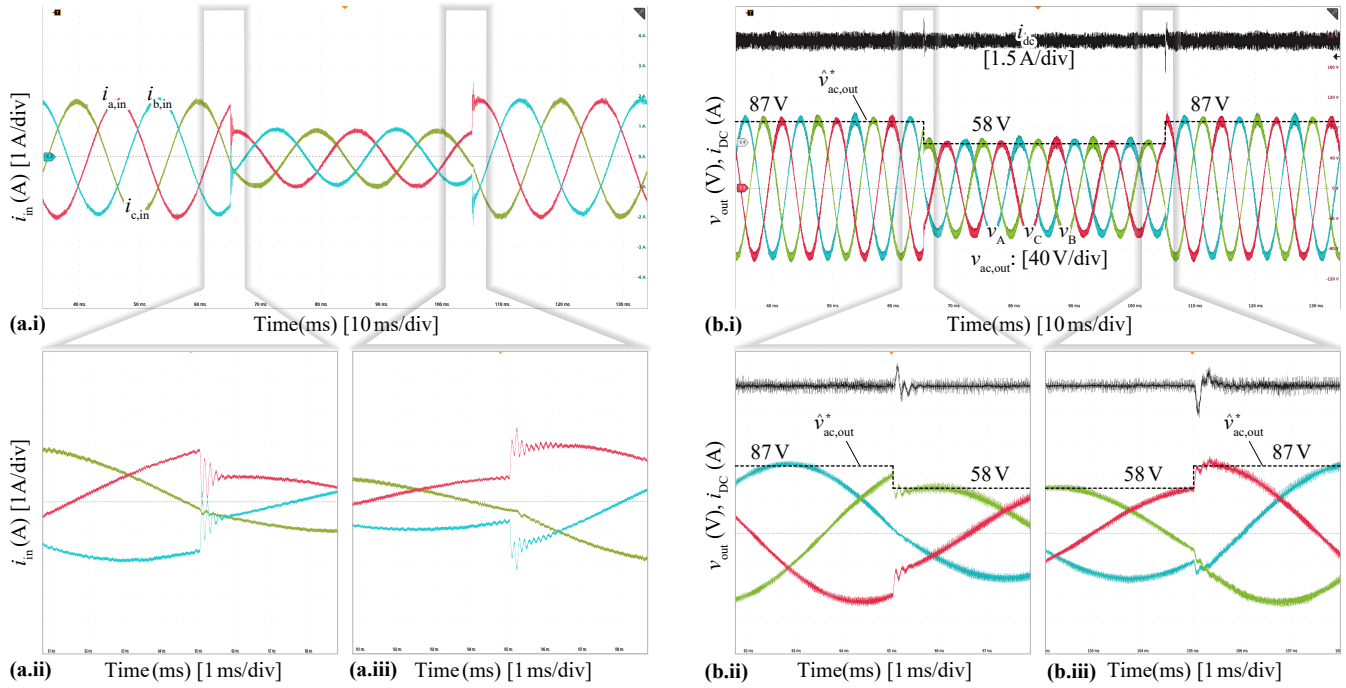

Fig. 16. Measured closed-loop step response of the CSC for a step in the output voltage amplitude reference from 87 V to 58 V and back, resulting in current amplitude levels of 3 A and 2 A with the nominal load of 29 Ω. The grid voltage is at the nominal value of 115 V (phase-to-neutral rms), and the dc-link current reference is selected as a constant value of 5 A. **(a.i)** shows the three-phase grid currents $i_{a,in}$, $i_{b,in}$ and $i_{c,in}$ with zoomed views of the steps given in **(a.ii)** and **(a.iii)**. **(b.i)** shows the three-phase load voltages v_A, v_B, v_C and the dc-link current i_{dc} with zoomed views of the steps shown in**(b.ii)** and **(b.iii)**.

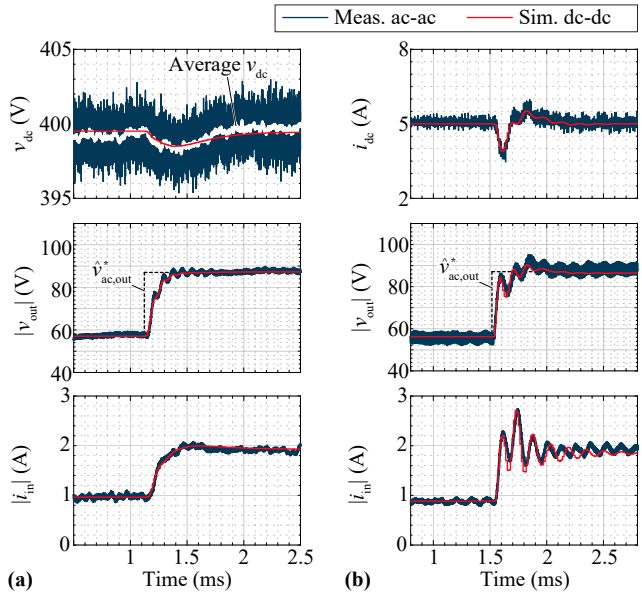

Fig. 17. Comparison of measured closed-loop ac-ac step-responses (see **Fig. 15** and **Fig. 16** for details) and simulated closed-loop dc-dc equivalent circuit responses for **(a)** VSC and **(b)** CSC. The output voltage reference steps from 58 V to 87 V). The shown amplitudes of the three-phase quantities are extracted from the measured quantities using dq-transformation; see also **Section II-C** for details on the required scalings for the comparison.

the different load-side filter structures of the CSC and the VSC (and, correspondingly, the dc-dc equivalent circuits), the output capacitor $C_{\mathrm{DM1,CSC}}$ of the CSC can either be selected such that the same voltage ripple Δv_{o} as for the VSC results ($C_{\mathrm{DM1,CSC}} = 11.25\,\mu\mathrm{F}$)[10] *or* such that the same fundamental-frequency reactive power Q_{r} consumption[11] occurs ($C_{\mathrm{DM1,CSC}} = 1.8\,\mu\mathrm{F}$)[12]. As the output voltage control dynamics depend on this capacitance, both cases are considered in the following comparative evaluation to convey a complete picture. Please note that in this section, i_{in}, i_{o} and v_{o} refer to the input source current, output load current and output load voltage of the dc-dc equivalent circuits, respectively.

A. Small-Signal Behavior

Fig. 18 shows the open-loop and closed-loop gains of the output voltage control loops of the VSC and the CSC. The CSC achieves a higher output voltage control open-loop crossover bandwidth (5 kHz vs. 1.8 kHz of the VSC).

Fig. 19 compares the simulated small-signal responses of the VSC and the CSC systems for a 10 V output voltage reference step (from 120 V to 130 V) with a 43 Ω resistive load (i.e., 50% of the nominal load). Note that here also the CSC variant with a lower $C_{\mathrm{DM1,CSC}}$ (same output capacitance as that of the VSC, but with higher high-frequency output voltage ripple) is considered; note also that the controller gains change accordingly as listed in **Tab. III**. As seen in **Fig. 19a**, both CSC variants exhibit faster small-signal output voltage dynamics, consistent with the loop gain comparison from **Fig. 18**. **Fig. 19b** and **Fig. 19c** show the corresponding changes in the dc-link quantities (v_{dc} for the VSC and i_{dc} for the CSC) and the input

[10]Note that this increased output capacitor of the CSC will result in higher reactive power in the ac-ac CSC compared to the VSC. However, this capacitive reactive power can be used to supply the reactive power of the motor [46]. Or the same output voltage ripple can be achieved by an additional LC filter stage with cut-off frequency higher than the control bandwidth, allowing to ignore the additional stage for the control design without necessarily increasing the output reactive power of the ac-ac CSC.

[11]Of course, reactive power would only actually be consumed in the ac-ac system, not in the dc-dc equivalent circuit considered here.

[12]Note that with the utilized filter structures, this results in around 6 times the output voltage ripple for CSC compared to VSC.

TABLE III
CONTROLLER PARAMETERS FOR COMPARATIVE ANALYSIS OF THE CONTROL DYNAMICS OF THE VSC AND THE CSC (DC-DC EQUIVALENT CIRCUITS).

Parameter		Value	Unit
VSC			
	Output Buck Stage		
v_{o} controller	$K_{\mathrm{P,VV}}$	0.029	A/V
	$K_{\mathrm{I,VV}}$	153.5	A/VS
i_{LEQ1} controller	$K_{\mathrm{P,VI}}$	14.5	V/A
	Input Boost Stage		
v_{dc} controller	$K_{\mathrm{P,Vv}}$	0.078	A/V
	$K_{\mathrm{I,Vv}}$	4.31	A/VS
i_{Leq1} controller	$K_{\mathrm{P,Vi}}$	14.5	V/A
CSC — Same output voltage ripple, $C_{\mathrm{DM1,CSC}}$ = 11.25 µF			
	Output Boost Stage		
v_{o} controller	$K_{\mathrm{P,CV}}$	0.236	A/V
	$K_{\mathrm{I,CV}}$	130	A/VS
	Input Buck Stage		
	$K_{\mathrm{P,Ci}}$	20	A/V
i_{dc} controller	$K_{\mathrm{I,Ci}}$	50e3	A/VS
	K_{d}	0.0033	
CSC — Same output reactive power, $C_{\mathrm{DM1,CSC}}$ = 1.8 µF			
	Output Boost Stage		
v_{o} controller	$K_{\mathrm{P,CV}}$	0.038	A/V
	$K_{\mathrm{I,CV}}$	20.7	A/VS
	Input Buck Stage		
	$K_{\mathrm{P,Ci}}$	27	A/V
i_{dc} controller	$K_{\mathrm{I,Ci}}$	150e3	A/VS
	K_{d}	0.005	

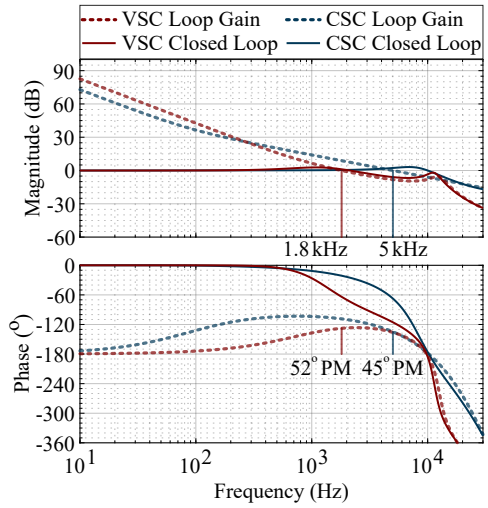

Fig. 18. Comparison of the output voltage control loop gains between the VSC and the CSC, both featuring equal output voltage ripple (i.e., $C_{\mathrm{DM1,CSC}}$ = 11.25 µF is selected). Both controllers are designed maximize the bandwidth while ensuring a minimum phase margin of 45°; details see **Section III**.

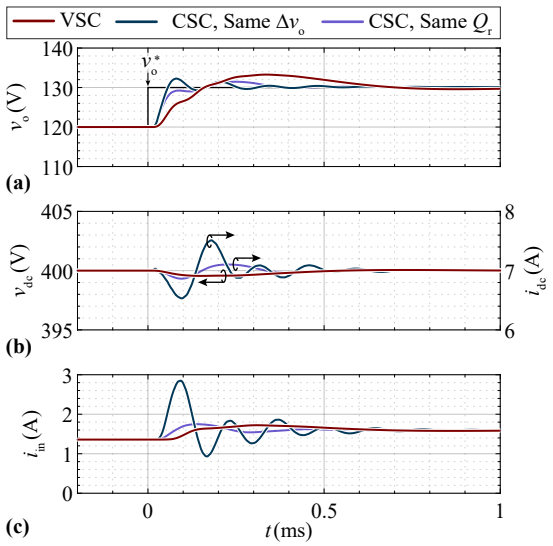

Fig. 19. Simulated small-signal step-response comparison of the CSC and the VSC (dc-dc equivalent circuits) for a small-signal step of the reference output voltage around half of the nominal value (from 120 V to 130 V) for a nominal resistive load of 43 Ω (equivalent to the nominal resistive load of 29 Ω for the ac system). Two variants of the CSC are considered (with two different output capacitor values such that either equal output voltage ripple Δv_o or equal fundamental-frequency reactive power Q_r consumption as the VSC results). The CSC shows slightly faster output voltage dynamics, as is expected from the loop gains shown in **Fig. 18**, however, with an increased overshoot of the input (source) current, especially for the case with equal output voltage ripple as the VSC (and hence larger output capacitor.)

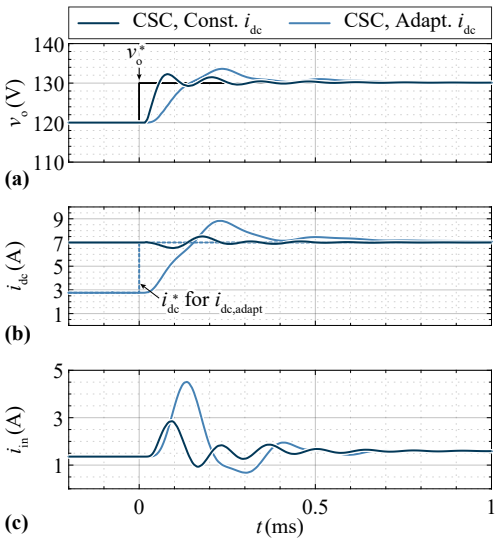

Fig. 20. Simulated responses of the CSC (dc-dc equivalent circuits) for a small-signal step in the reference output voltage around half of nominal value (from 120 V to 130 V) for a resistive load of 43 Ω with the dc-link current reference i_{dc}^* either fixed to the nominal value or adapted to the load power, which improves the system efficiency but compromises the output voltage control dynamics—even if the dc-link current reference is increased to the nominal value synchronously with the step in the output voltage reference as done here.

source current i_{in}, respectively. The feedforward of the output power to the input stage (see **Fig. 8** for the VSC and **Fig. 10** for the CSC, respectively) results in a simultaneous increase in i_{in} with v_o, minimizing deviations of the dc-link quantities from the respective reference values. However, in the CSC, the feedforward also causes a certain overshoot and ringing in the input current i_{in} due to the input filter resonance despite the active damping described in **Section III**. Note that a higher CSC output filter capacitor $C_{DM1,CSC}$ (i.e., corresponding to the CSC variant with equal output voltage ripple as the VSC but higher fundamental-frequency reactive power consumption) requires more energy from the dc-link inductor and/or the input stage to change its voltage quickly. Given the slower dynamics of the dc-link current controller compared to the output voltage controller, the CSC experiences greater undershoot in the dc-link current i_{dc} and higher overshoot in the input current i_{in} with larger output capacitor $C_{DM1,CSC}$. To mitigate this effect, the CSC output voltage controller could be slowed down, which, however, might reduce the CSC's advantage in small-signal output voltage dynamics compared to the VSC.

Finally, consider that in an ac-ac CSC, four switching devices simultaneously conduct the dc-link current i_{dc} at all times, leading to increased system losses if i_{dc} is maintained at a fixed nominal/maximum value. These losses can be mitigated by adapting the dc-link current reference i_{dc}^* in proportion to the maximum of the input grid or the output load current amplitudes, typically considering some margin in the order of 10% [38]. However, this comes at the cost of reduced output voltage control dynamics. To balance output voltage dynamics and efficiency, i_{dc}^* can be temporarily increased to its maximum during a step-response, as shown in **Fig. 20b**. After the output voltage stabilizes at the new reference, i_{dc}^* can be reduced again according to the load situation, thereby reducing losses. However, this approach causes a higher overshoot in i_{in}, as seen in **Fig. 20c**, due to the simultaneous demand for increased input current by both, the output power feedforward and the dc-link current controller[13]. Note that, following the duality principle, a similar adaptive strategy could be applied to the VSC by varying the dc-link voltage to reduce switching losses. However, first, the potential savings are relatively low because the fixed input (grid) voltage plus some control margin defines a minimum the dc-link voltage regardless of the output voltage, and, second, due to the typically much larger stored energy in the dc-link capacitor, quick changes of the dc-link voltage would be not possible. Therefore, the dc-link voltage of VSCs is typically kept at the nominal value at all times.

B. Large-Signal Behavior Case Study

To comparatively evaluate the large-signal response of the VSC and the CSC in a representative case, a typical PMSM machine, such as the 2.2 kW BMP1401R3NA2A synchronous motor [47] is considered and specifically the fastest achievable ramp-up time from zero to nominal output current (nominal torque) is analyzed, starting from standstill. The example motor's moment of inertia (16.46 kg cm^2), nominal torque value (6.37 Nm), and machine constant (=44 mV/min) result in a slow change of the back EMF during ramp-up (1.63 V/ms), which is negligible compared to the dynamics of the output voltage

[13]Note that the i_{dc}^* could alternatively be adjusted according to the load current (with some margin) during the output voltage reference step change, rather than increasing it to the maximum value. This approach eliminates overshoot in i_{in}, however, at the cost of further slowed down output voltage dynamics.

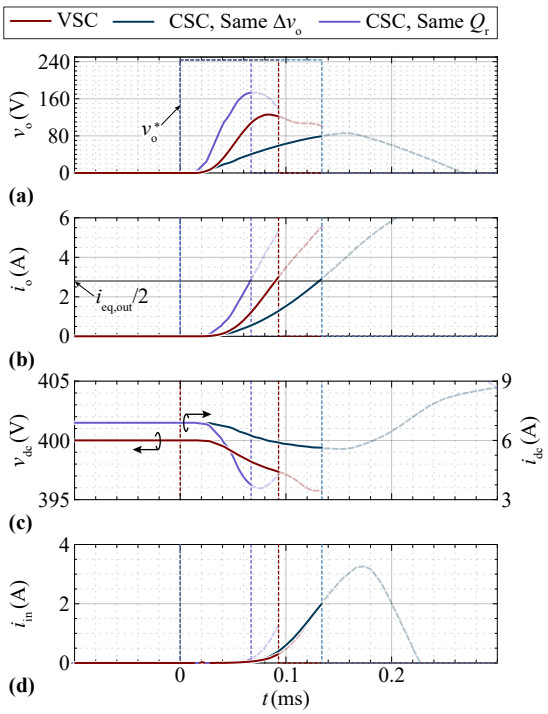

Fig. 21. Simulated large-signal ramp-up behavior considering an inductive load in the dc-dc equivalent circuits, which represents a BMP1401R3NA2A synchronous motor [47] at standstill. To exclude any effect of a higher-level motor speed/current control loop, the output voltage reference steps from zero to nominal (fastest possible reference change an outer motor speed/current controller could ask for), until the load current reaches half its nominal value, after which the voltage reference is stepped down back to zero. Again, two CSC variants are considered (with two different output capacitor values such that either equal output voltage ripple Δv_o or equal fundamental-frequency reactive power Q_r consumption as the VSC results), both operating with the dc-link current fixed to the nominal value. **(a)** Output voltages, **(b)** output currents, **(c)** dc-link voltage (VSC) and dc-link current (CSC), **(d)** input currents.

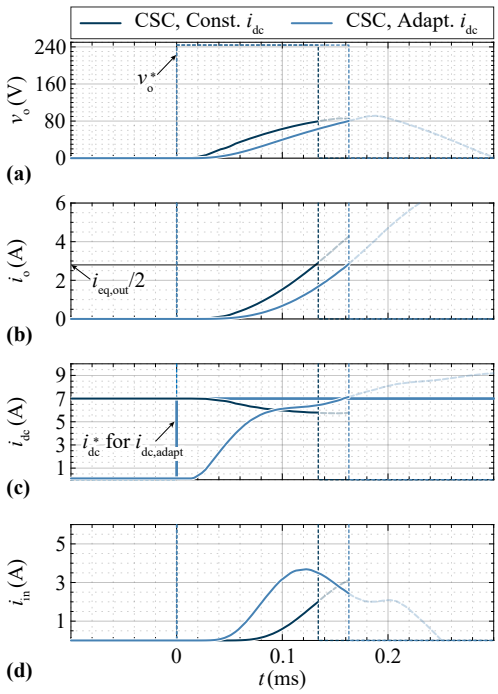

Fig. 22. Simulated large-signal ramp-up behavior considering an inductive load in the dc-dc equivalent circuits, which represents a BMP1401R3NA2A synchronous motor [47] at standstill as in **Fig. 21**, and comparing the performances of the CSC operating with fixed nominal dc-link current i_{dc} as in **Fig. 21** or, alternatively, with adaptive dc-link current to improve the efficiency. There, the dc-link current reference i_{dc}^* is stepped from zero to the nominal value synchronously with the output voltage reference step, yet still slower dynamics result. **(a)** Output voltages, **(b)** output currents, **(c)** dc-link currents, **(d)** input currents.

control of the VSC and CSC drives. Consequently, the motor load is modeled using the equivalent stator inductance with zero back EMF during start-up. For permanent magnet synchronous machines, the q-axis and d-axis inductances are typically similar (for the considered BMP1401R3NA2A, the q-axis and d-axis inductances are 1.76 mH and 1.47 mH, respectively). Therefore, for the qualitative comparative analysis, the q-axis inductance is used as the load inductor in the simulation of the dc-dc equivalent circuit. To exclude further external influences, no outer motor speed and/or current control loops are considered. Instead, to ramp-up the output current as quickly as possible, an output voltage reference step from zero to the nominal converter output voltage is applied to the VSC and the CSC. The increase of the output voltage leads to an increase of the load inductor current, and once the current reaches half of the desired reference value, the output voltage reference is ideally reduced to zero, allowing the load current to reach the reference value while the output voltage decreases as indicated in **Fig. 21a**. On a much slower time-scale, the output voltage reference would then gradually increase as the motor speeds up and the back EMF increases accordingly.

Note that the dc-dc equivalent circuits model the switching stage of the corresponding three-phase converter with a half-bridge in order to keep the equivalent circuits simple. However, whereas three-phase VSCs and CSCs allow the application of a negative control vector, this is not possible in a dc-dc equivalent circuit realized with half-bridges. The dc-dc equivalent circuits could be realized using full-bridges to capture this capability correctly, but this has not been done here as, first, the added complexity defeats the purpose of the dc-dc equivalent circuits, and, second, the correctly captured step-up dynamics are representative for the system behavior. However, this means that, in the considered motor start-up case study, only the first part of the responses until the output current reaches half of the nominal value are representative.

Thus the comparative analysis focuses on the time required for the load inductor current i_o to reach half the reference value following an output voltage reference step to the nominal value (i.e., the fastest possible reference command that a higher-level motor speed/current controller could ask for), as shown in **Fig. 21ab**. **Fig. 21cd** display the corresponding changes in the dc-link quantities (v_{dc} for the VSC and i_{dc} for the CSC) and the input source current i_{in}, respectively[14]. Advantageously, the CSC can immediately use the entire i_{dc} (kept at the nominal value for now) to charge the output capacitor, whereas the VSC output voltage increase is limited by the dynamics of the filter inductor current i_{LEQ1}, which must increase before the output voltage can increase. However, the energy stored in the CSC

[14]Note that the increase of the input source current is delayed relative to the reduction in the dc-link current for CSC as the input filter capacitor acts as storage in between the input source and the dc-link inductor.

dc-link inductor (29.4 mJ for the CSC under consideration with nominal i_{dc}) is typically much lower than the energy stored in the VSC dc-link capacitor (1.28 J for the VSC under consideration with nominal v_{dc}). Therefore, unlike the small-signal comparison, it is not immediately clear which system offers faster control dynamics. **Fig. 21** compares the large-signal response of VSC with both CSC variants discussed earlier (the CSC output capacitor is either selected such that the high-frequency output voltage ripple Δv_o equals that of the VSC *or* such that the fundamental-frequency reactive power consumption Q_r equals that of the VSC). The ramp-up of the output current of the CSC with same Δv_o is slower than the VSC (134 µs for CSC vs. 93 µs for VSC), whereas the CSC with same Q_r is faster (ramp-up time of 67 µs). This is because, during the large-signal step, the output stage duty cycle of the CSC is saturated at 1, allowing the entire i_{dc} to contribute to the output voltage increase in both cases. However, for the same reactive power, the CSC output capacitor equals the output capacitor of the VSC, i.e., $C_{DM1,CSC} = C_{DM1,VSC} = 1.8\,\mu F$, and hence there it is directly evident that the VSC dynamics are slower due to the filter inductor. However, for equal output voltage ripple, the CSC output capacitor increases by almost an order of magnitude to $C_{DM1,CSC} = 11.25\,\mu F$, which accordingly slows down the CSC's response time below that of the VSC. Note that the response time could be improved by increasing the circulating dc-link current, thus storing more energy in the dc-link inductor, but this would come at the cost of higher system losses and/or larger components.

Finally, **Fig. 22** compares the start-up response of the CSC for a fixed i_{dc}^* versus an adaptive i_{dc}^* that is selected proportional to the load current; only the CSC variant with equal output voltage ripple is considered here. Similar to the small-signal case (see **Fig. 20**), the dc-link current i_{dc}^* is temporarily increased to the nominal/maximum value synchronously with the output voltage reference step to achieve faster dynamics (compared to continuously adapting it in proportion to the actual and comparably slowly rising load current). In steady state, the dc-link current would then revert back to a value proportional to the load current to minimize losses. Still, the response time with adaptive dc-link current i_{dc}^* is obviously increased compared to the baseline case with a fixed nominal dc-link i_{dc}^* (163 µs vs 134 µs, implying an increase of around 22%). This highlights the trade-off between control dynamics and efficiency of the CSC; an adaptive dc-link current thus seems appropriate for applications that do not require a fast control dynamics such as fans and pumps.

V. Conclusion

VSDs operating from the three-phase mains are ac-ac converters that are typically realized as a back-to-back configuration of an ac-dc rectifier and a dc-ac inverter with, ideally, an output filter to provide smooth sinusoidal motor voltages. The standard approach today employs a voltage dc-link configuration (voltage-source converter, VSC) with a dc-link capacitor shared by the rectifier and the inverter stage. Alternatively, a current dc-link configuration (current-source converter, CSC) with a shared dc-link inductor could be employed. This paper investigates the output voltage control system design and performance of a VSC and a CSC (1.4 kW, 200 V line-to-line rms, 600 V GaN technology, 72 kHz switching frequency) which are designed for equal efficiency at the nominal operating point and provide smooth sinusoidal output voltage to motor.

Advantageously, both three-phase ac-ac converters can be mapped to dc-dc converter equivalent circuits that accurately capture the system dynamics and facilitate the design of the controllers. The VSC is mapped to a back-to-back configuration of a boost and a buck converter, whereas the CSC is mapped to a back-to-back configuration of a buck and a boost converter. Built VSC and CSC demonstrators are used to experimentally verify a very good accuracy of the dc-dc equivalent circuits regarding both, open-loop and closed-loop behavior.

Finally, the dc-dc equivalent circuits are used to evaluate the output voltage control dynamics of the VSC and the CSC. The CSC is found to have a higher small-signal output voltage control bandwidth compared to VSC. Regarding the large-signal performance, the fastest possible ramp-up of the output current (this implies that the CSC and VSC output voltage reference steps from zero to the nominal value) in an inductive load that represents a motor at standstill is investigated. There, two different CSC variants must be distinguished: either the output capacitor is selected such that equal fundamental-frequency reactive power consumption as for the VSC results, in which case the CSC can ramp the load current faster (by around 39% for the considered converter's specifications). Alternatively, the CSC output capacitor is selected such that equal high-frequency ripple as for the VSC (with its LC filter) occurs; then, the CSC load current ramp-up is slower than the VSC (by around 44% for the considered converter's specifications). Further, for the above discussed comparison, the dc-link current of the CSC has been considered at the nominal value at all times. To improve efficiency, however, the dc-link current could be adapted to the load, which, however, slows down the output voltage step responses (by around 22% for the case at hand).

All in all, employing dc-dc equivalent circuits for the modeling, analysis, design, and comparative evaluation of the control systems for both, three-phase ac-ac VSC and CSC converter has been found to be straightforward and highly accurate as confirmed by detailed experimental verification.

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