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***Abstract*—Variable speed drives (VSDs) operating from a three-phase mains are typically realized as ac-ac voltage dc-link/source converters (VSCs). However, compact VSC-based VSDs implemented with wide-bandgap (WBG) semiconductors such as SiC and GaN often require LC output filters to protect the motor from high dv/dt of the switched voltage. In contrast, ac-ac current dc-link/source converters (CSCs) featuring a back-to-back connection of a current-source rectifier (CSR) and current-source inverter (CSI) with a shared dc-link inductor inherently provide continuous motor voltages, making them an interesting alternative. Therefore, this paper first introduces the loss-optimal operating mode of an ac-ac CSC: using the minimum possible and hence time-varying dc-link current (defined by the maximum absolute value of CSR's and the CSI's phase currents), the conduction losses are minimized and either the CSR or the CSI operates with 2/3-PWM, i.e., at any given time, one phase terminal is clamped to the dc-link inductor while PWM is only needed to synthesize the remaining two phase currents, thus reducing switching losses. The respective other stage employs PWM in all three phases (3/3-PWM) and shapes the dc-link current. Closed-form expressions for the transistor conduction and switching losses facilitate a quantitative assessment of the efficiency improvements. Then, the paper proposes a synergetic control method that realizes loss-optimal operation for the entire output voltage and current range of the ac-ac CSC, with motor voltages lower and higher than the grid voltage, and ensures smooth transitions between operating points. Finally, detailed experimental results of a 1.4 kW, 200 V (line-to-line rms) ac-ac CSC demonstrator using first-generation 600 V, 140 mΩ monolithic bidirectional GaN transistors, grid-side and motor-side EMI filters, and a switching frequency of 72 kHz confirm the loss optimal operation and seamless transitions between operating points. Compared to conventional operation and in close alignment with calculation results, the measured nominal ac-ac efficiency increases by 0.3% to 97 % with the proposed loss-optimal operation, and part-load efficiency gains of up to 1% are observed.**

I. Introduction

Electric motor applications account for an estimated share of about 45% of the global electricity consumption [1]. Driven by the trends towards urbanization and ubiquitous automation, the demand for electric motor drive systems is expected to increase further [2]. Therefore, any investment towards improving the efficiency of motor-driven systems and/or thus reducing their over-all energy consumption is of utmost importance. Variable speed drive (VSD) systems enable significant energy savings in motor-driven applications, particularly for systems operating with variable load [1]–[6].

In typical applications, VSDs are supplied from a three-phase ac mains, i.e., are ac-ac power converters which are realized as a back-to-back connection of an ac-dc rectifier and a dc-ac inverter power stage. The two converter stages are coupled with a common intermediate energy storage element which can either be a dc-link capacitor (voltage-source converter, VSC) or a dc-link inductor (current-source converter, CSC) as shown in **Fig. 1**. The CSC consists of a grid-side current-source rectifier (CSR) and motor-side current-source inverter (CSI) that share a common dc-link inductor.

VSCs require semiconductor devices with only unipolar voltage blocking but bidirectional current conduction capability, whereas CSCs require bipolar-voltage-blocking devices with only unidirectional current conduction capability[1]. Thus, in the past, CSCs have been implemented with thyristors, GTOs and GCTs for high power applications where they were preferred over VSCs due to absence of large electrolytic capacitor

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[1]If a reversal of the polarity of the dc-side voltages of the rectifier and inverter stages is allowed for power regeneration from the load to the grid

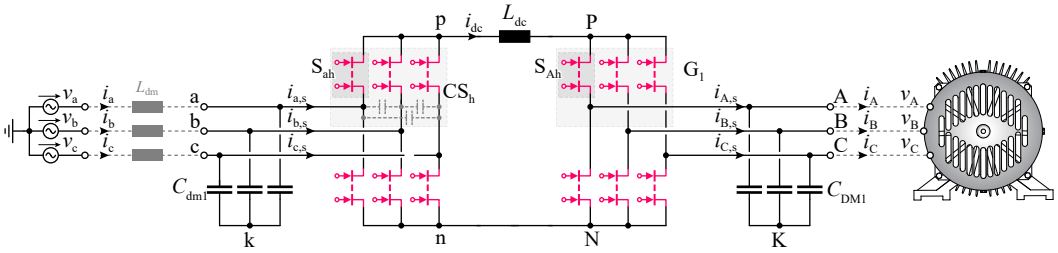

Fig. 1. Core structure of the power circuit of the considered ac-ac current-source converter (CSC), which is formed by a back-to-back arrangement of a current-source rectifier (CSR) and a current-source inverter (CSI), both employing monolithic bidirectional switches (M-BDSs); specifically, the employed first generation 600 V, 140 mΩ GaN M-BDSs facilitate interfacing a 200 V (line-to-line rms) three-phase ac mains. The dashed rectangle labeled CS_h indicates an exemplary commutation cell of the CSR, which consists of three M-BDSs and three delta-connected commutation capacitors. Note that the grid-side and motor-side EMI filter stages, that are employed in the finally built hardware demonstrator (cf. **Section IV**), are not shown here for the sake of clarity and the missing relevance for the proposed synergetic control method.

[7], [8], the capability of four-quadrant operation (supporting regenerative braking of the motor) by allowing reversal of the dc-side voltage polarity to reverse power flow without requiring extra components, smooth motor voltages, and inherent load short-circuit protection due to large dc-link inductor limiting the di/dt of the short circuit current [9]–[11].

CSCs have also been considered for low-power applications already more than two decades ago, realizing the bipolar-voltage-blocking device as a series connection of an IGBT and a diode or with reverse blocking IGBTs [12]–[14]. However, with switching frequencies thus limited to typically less than 16 kHz, the notion of a bulky dc-link inductor has emerged. But, as CSCs offer some key advantages including, but not limited to, inherently providing smooth output voltages to the motor without needing a dedicated LC filter, research towards CSCs with higher switching frequencies and hence compact dc-link inductors has continued, also driven by wide-bandgap (WBG) power semiconductors [15]–[22]. It should also be noted that the use of CSCs has not been limited to motor drive systems; CSCs have been and are still considered for a wide range of other applications such as data center power supplies [23]–[25], solid-state transformers [26], grid interfaces for renewable energy [27] and EV chargers [28], [29].

Until recently, the only way of implementing switching devices with bipolar voltage-blocking and bidirectional current-conducting capability (bidirectional switch, BDS, sometimes also called ac switch) for CSCs was an inverse-series connection of two transistors (or a transistor and a diode in applications where unidirectional current flow suffices). Both devices must be rated for the full blocking voltage to ensure the required bipolar voltage blocking capability. Consequently, the on-state resistance of such a series arrangement is twice that of a single transistor. The corresponding increase in conduction losses can be avoided by connecting a parallel branch of yet another inverse-series combination of two transistors, resulting in a BDS with the same on-state resistance as a single transistor but with four times the semiconductor chip area [30]. To address this clear drawback of CSCs compared to VSCs, there has been continuing research towards developing monolithic BDSs (M-BDSs) that realize a factor-of-four reduction of chip area, i.e., provide BDS functionality with the same on-state resistance and the same chip area as a unipolar voltage blocking device (the same drift region is used for blocking voltages of both polarities) [31]–[38]. By now, there are mature M-BDSs using GaN technology; specifically, 600 V, 140 mΩ devices [39] are available and have been characterized by the authors for application in CSCs [40], [41] and T-type VSC rectifiers [42]. Therefore, GaN M-BDSs are shown as switching devices[2] in **Fig. 1**, which depicts the core stage of the considered ac-ac CSC VSD.

VSDs are required to cover wide ranges of output voltage (proportional to the motor speed) and current (proportional to the motor torque) as indicated in **Fig. 2** for the ac-ac CSC system from **Fig. 1** with specifications listed in **Tab. I**. The 600 V blocking voltage of available GaN M-BDSs facilitates operation from a 200 V three-phase mains as used in the U.S. or in Japan. The wide output voltage range implies that the VSD must feature both, buck and boost capability as highlighted in **Fig. 2**. Pure buck operation occurs if the instantaneous maximum of the absolute motor voltages v_A, v_B and v_C is lower than the instantaneous maximum of the absolute three phase input voltages v_a, v_b and v_c, i.e., if $V_m < \sqrt{3}/2 \cdot V_g$ with V_m and V_g denoting the motor and mains line-to-line rms voltages. In analogy, pure boost operation occurs if $V_m > 2/\sqrt{3} \cdot V_g$. Between these two boundaries, the CSC operates in the transition region, i.e., changes sequentially between instantaneous boost and buck operation. Note that for high motor voltages of $V_m > 200$ V, the maximum motor current (motor power) is limited by the CSR's rated power of $P_n = 1.4$ kW. Please refer to **Appendix A** for a brief overview on the operating principle of CSCs.

Fig. 3 illustrates the phase current and voltage waveforms on the grid and the motor side of the ac-ac CSC during buck, transition, and boost mode for constant output current amplitude while the load voltage amplitudes increase over time (note that

[2]The depiction of GaN M-BDSs in this paper illustrates that both gates are normally-off, as indicated by two discontinuities in the connection between the two source terminals. Note that the use of dual-gate M-BDSs in CSC based VSDs also requires the implementation of multi-step commutation strategy similar to the BDS implemented with inverse-series connection of two transistors.

TABLE I
KEY SPECIFICATIONS OF THE CONSIDERED AC-AC CSC.

Parameter		Value	Unit
Rated power	P_n	1.4	kW
Grid line-to-line RMS voltage	$V_{g,n}$	200	V
Grid frequency	f_g	50	Hz
Nom. motor phase current	$I_{m,n}$	4	A
Nom. motor line-to-line RMS voltage	$V_{m,n}$	200	V
Max. motor line-to-line peak voltage	$\hat{V}_{m,m}$	400	V
Max. motor frequency	f_m	200	Hz

Note: Capital V denote line-to-line RMS voltages, capital I denote phase RMS currents and subscript g and m denote a grid and motor side quantity respectively.

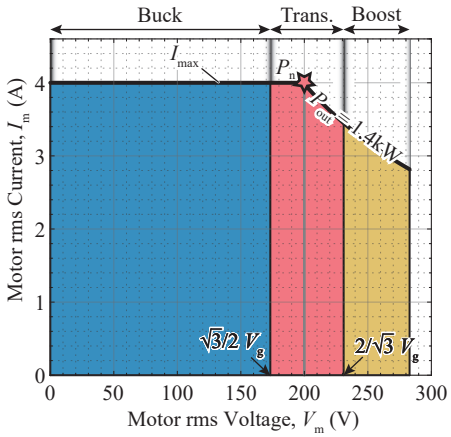

Fig. 2. Output voltage/current operating area of the ac-ac CSC from **Fig. 1** with specifications from **Tab. I**, where the buck, transition, and boost regions are indicated. For motor voltages above the nominal value of $V_m = 200$ V, the power rating of the CSR limits the maximum motor current (Given the fixed grid voltage, the rated power of 1.4 kW limits the maximum grid side current which results in lower current at the motor side for motor voltages higher than the nominal value of $V_m = 200$ V.). The current/power ratings follow from available first-generation 600 V, 140 mΩ GaN M-BDSs, and target switching frequency of $f_s = 72$ kHz [41].

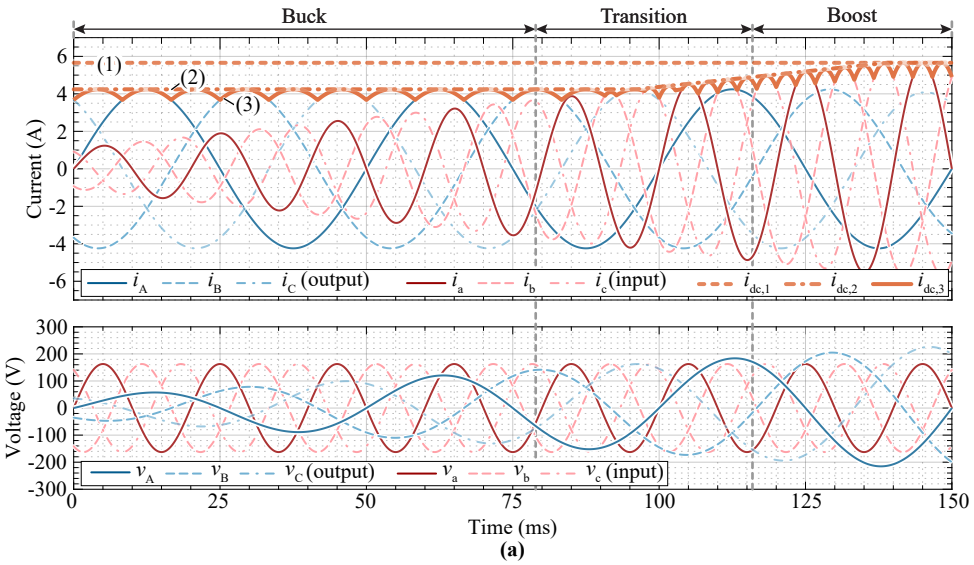

Fig. 3. Options for selecting the dc-link current i_{dc} in an ac-ac CSC operating with constant amplitudes of the output/motor currents i_A, i_B, i_C but increasing amplitudes of the output phase voltages v_A, v_B, v_C, i.e., increasing output power. Thus, the constant amplitudes of the mains voltages v_a, v_b, v_c imply increasing amplitudes of the mains currents i_a, i_b, i_c such that the input/output power balance is maintained (see also the **Appendix**). Note that in a motor application, an increase of the output/motor voltage is coupled to an increase of the output frequency; this increase in frequency is, however, not important for the explanation of the proposed synergetic control method and therefore not shown for the sake of better visibility. (1) Non-adaptive constant dc-link current at a level high enough for all operating points. (2) Adaptive constant dc-link current equal to the amplitude of the mains or motor phase currents (determined by the larger of the two) at a given operating point. (3) Variable dc-link current / synergetic control [40], where the dc-link current equals the instantaneous maximum of the absolute values of the grid and motor phase currents.

for a motor load, increasing output/motor voltage is coupled with increasing frequency; however, the increase in frequency is not shown in the figure for the sake of clarity and better visibility). Because of the thus increasing motor power and the fixed grid voltage $V_g = 200\,\mathrm{V}$, the grid currents increase, too, to maintain the input-output power balance.

In ac-ac CSC systems, generally the CSR controls the dc-link current i_{dc} to a reference value while the CSI modulates i_{dc} to synthesize the required ac output currents [8], [12], [16], [23], [43], [44]. There are three options for selecting the dc-link current reference.

1) Non-adaptive constant dc-link current: The standard method, which is straightforward to implement, employs a single, constant i_{dc} throughout the operating range [16], [45], analogous to maintaining a constant dc-link voltage in ac-ac VSC systems. The modulation indices for the CSR and the CSI are:

$$m_g = \hat{i}_g / i_{dc}, \quad m_m = \hat{i}_m / i_{dc}, \tag{1}$$

respectively, where, $\hat{i}_g$ and $\hat{i}_m$ are the amplitudes of the local average values of the CSR's and the CSI's ac-side currents ($i_{a,s}$ for CSR's phase a and $i_{A,s}$ for CSI's phase A in **Fig. 1**). Since both, $m_g, m_m \in [0, 1]$, i_{dc} must be at least equal to $\max\{\hat{i}_{g,max}, \hat{i}_{m,max}\}$, where $\hat{i}_{g,max}$ and $\hat{i}_{m,max}$ are the maximum amplitudes of i_g and i_m in the entire operating range. The curve $i_{dc,1}$ in **Fig. 3** corresponds to this option.

2) Adaptive constant dc-link current: However, the switching losses of both, the CSR and the CSI, depend directly on i_{dc}, and at any point in time, overall four M-BDSs as well as the dc-link inductor carry i_{dc}. Therefore, maintaining the dc-link current at a fixed high value leads to unnecessary high losses for part-load operating points. An alternative method [44] thus still employs a constant i_{dc} that is controlled by the CSR, but adapts it for changing load conditions. The minimum constant value of i_{dc} that is sufficient to cover grid and motor currents at a given operating point, $\hat{i}_g$ and $\hat{i}_m$, is therefore equal to $i_{dc} = \max\{\hat{i}_g, \hat{i}_m\}$. Note that this implies $i_{dc} = \hat{i}_m$ during buck mode and $i_{dc} = \hat{i}_g$ during boost mode. This corresponds to $i_{dc,2}$ in **Fig. 3**, whose magnitude is clearly lower than $i_{dc,1}$ for all part load operating points, hence resulting in lower losses. This mode of operation is hereafter referred to as the conventional operation for ac-ac CSC in this paper.

3) Variable dc-link current / synergetic control: However, there are still time intervals within each mains/motor period where $i_{dc,2}$ is higher than the instantaneous maximum absolute value of the six phase currents (three on the grid side, three on the motor side). As proposed in [46] for an ac-dc rectifier and in [47] for a dc-ac CSI, shaping i_{dc} to the six-pulse (in a three-phase system) envelope of the maximum absolute values of the phase currents not only leads to a further reduction of the conduction losses, but advantageously significantly reduces the transistor switching losses by avoiding high-frequency switching in some part of the fundamental ac period, i.e., realizes 2/3-PWM, which is further discussed in **Section II** below. The concept has further been discussed for dc-ac inverter applications [48], [49] and ac-dc rectifier applications [29], where in both cases additional dc-dc converter stages shape i_{dc} to the required six-pulse shape.

The applicability of this concept was extended to ac-ac CSCs by the authors in [40]. There, the CSI defines the dc-link current reference in the buck mode and the CSR does so in boost mode, see $i_{dc,3}$ in **Fig. 3**; in the transition region, both stages define sections of the dc-link current reference alternately. Advantageously, the respective other converter stage

can shape the dc-link current accordingly; the CSR and the CSI thus *synergetically* control the dc-link current to the minimum possible value at all times and, in doing so, realize the minimum possible conduction losses and significant switching loss savings for the stage operating with 2/3-PWM (further explanation in **Section II**).[3]

Whereas [40] introduces synergetic control of ac-ac CSCs, only simulation results are presented, and the paper puts a focus on detailed characterization results of the novel 600 V, 140 mΩ GaN M-BDS in a CSC commutation cell. A detailed discussion and derivation of the synergetic control concept as well as an experimental validation are missing. Therefore, this paper first provides an in-depth explanation of the loss-optimal operating modes of an ac-ac CSC in terms of space vector modulation in **Section II**, which further provides closed-form solutions for the semiconductor losses and briefly mentions the impact of synergetic control on the design of the dc-link inductor L_{dc}. **Section III** then presents the synergetic control structure that realizes loss-optimal operation of the ac-ac CSC throughout the operating area, ensuring seamless transitions between buck and boost operation. **Section IV** employs a full ac-ac CSC demonstrator with first-generation 140 mΩ, 600 V GaN M-BDSs to comprehensively validate the proposed synergetic control method in static and transient cases and to characterize the system-level efficiency improvements over the full output voltage/current range. Finally, **Section V** provides concluding remarks. In addition, **Appendix A** presents a concise overview of the basic operating principles of the current-source converters.

II. Loss-Optimal Operation of AC-AC CSCs

For understanding the modulation of CSCs, it is helpful to consider the (quasi) duality relationship [50] to VSCs: Whereas in ac-ac VSCs a (constant) dc-link *voltage* is pulse-width-modulated to synthesize the desired three-phase input/output low-frequency (LF) ac voltage waveforms, in ac-ac CSCs high-frequency (HF) switching is used to modulate a (typically constant) dc-link *current*, i_{dc}, into the desired three-phase input/output LF ac currents. Therefore, each CSC switching stage (CSR and CSI) comprises two commutation cells (see **Fig. 1**). Interfacing a three-phase ac system, each commutation cell comprises three BDSs, and each BDS connects the dc-link inductor to one of the three ac-side phase terminals. Further, there are three ac-side commutation capacitors in each commutation cell, which can be arranged in star or delta configuration; note that the dc-link inductor terminal is the commutation cell's switching node. Therefore, *at least one* (to ensure a path for the inductive i_{dc}) *and only one* (to avoid short-circuiting the ac-side commutation and filter capacitors) BDS in each commutation cell must be turned-on at all times.

[3]It should be noted that of the three options for selecting i_{dc}, non-adaptive constant dc-link current ($i_{\mathrm{dc}} = i_{\mathrm{dc},1}$ in **Fig. 3**) offers the highest system dynamics since a step increase of the output current reference only requires a change in m_{i} whereas for the other two options ($i_{\mathrm{dc}} = i_{\mathrm{dc},2}$ or $i_{\mathrm{dc},3}$ in **Fig. 3**), first the dc-link current must be increased with finite dynamics of the dc-link current control loop. However, a large share of applications (like fans or pumps) do not require high control dynamics and hence can benefit from the efficiency improvement achievable by adapting the dc-link current to the load.

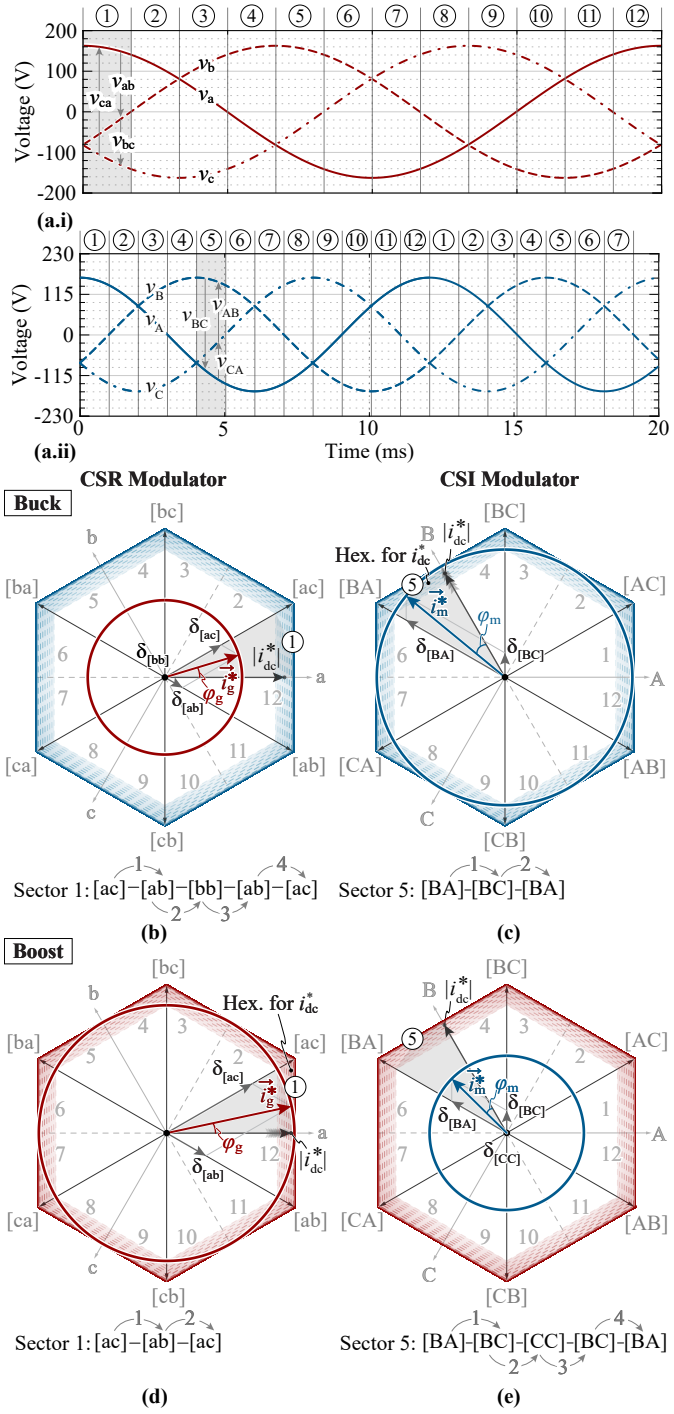

Fig. 4. Space-vector (SV) modulation of CSCs. **(a.i)** Three-phase grid voltage and **(a.ii)** three-phase motor voltage system with fundamental frequency of 50Hz and 80Hz divided into 12 sectors. SV diagrams for **(b), (d)** the CSR and **(c), (e)** the CSI of the ac-ac CSC, with exemplary CSR current reference SV $\vec{i}_{\mathrm{g}}^{\,*}$ in sector 1 and exemplary CSI current reference SV $\vec{i}_{\mathrm{m}}^{\,*}$ in sector 5, respectively, for buck (**(b), (c)**) and boost (**(d), (e)**) operation. For the proposed loss-optimal synergetic operation, the dc-link current i_{dc}^* varies according to (8)), which implies a continuous scaling of the hexagon size as indicated by the shaded areas. In buck operation, the CSI currents $i_{\mathrm{A,s}}^*$, $i_{\mathrm{B,s}}^*$ and $i_{\mathrm{C,s}}^*$ define i_{dc}; $\vec{i}_{\mathrm{m}}^{\,*}$ is thus advantageously synthesized without a zero vector and with only two switching transitions in each switching period (see **(c)**). In contrast, the SV sequence required to synthesize $\vec{i}_{\mathrm{g}}^{\,*}$ involves a zero vector ([bb] for sector 1) and a total of four switching transition (see **(b)**). These roles of the CSR and the CSI swap during boost operation (see **(d)** and **(e)**).

The switching states of a CSR or CSI are thus represented as [xy] where 'x' and 'y' denote the phases that connect to the dc-link in the high-side commutation cell (e.g., CS_h in **Fig. 1**) and in the low-side commutation cell, respectively. Each switching state corresponds to a *current* space vector (SV, representing the instantaneous phase currents) generated on the ac side: For a three phase system there are six active vectors with x ≠ y and length $2/\sqrt{3} \cdot i_{dc}$ (see **Fig. 4**), which implies energy transfer between the dc-link and the ac side. There are further three zero vectors (free-wheeling states[4]) where x = y, which corresponds to free-wheeling of i_{dc} from the high-side to the low-side commutation cell with (instantaneously) zero current routed to any of the three phases.

To synthesize a desired local average (over one switching period) ac-side current SV, e.g., $\vec{i}_g^*$ in **Fig. 4b**, the two adjacent active SVs and any of the three zero SVs are applied during respective dwell times, such that in average $\vec{i}_g^*$ results. Not that if only active vectors were used, the correct direction (angle) of $\vec{i}_g^*$ could be achieved, but the length would depend on i_{dc}; a zero vector is thus needed to scale the length of the synthesized SV accordingly.

It is thus useful to divide the corresponding current SV diagram into twelve sectors based on the active vectors and on the sequence of active and zero vectors used for synthesizing a desired ac-side current SV [15]. For instance, the grid current reference $\vec{i}_g^*$ in **Fig. 4b** is in sector 1 and thus synthesized using the two adjacent active vectors [ac] and [ab]; the choice of zero vector, however, presents a degree of freedom for modifying various performance indicators like overall switching losses, generated common-mode (CM) voltage, dc-link current ripple, etc.: In CSCs, a switching transition involves a fixed current i_{dc} and a time-varying line-to-line voltage. Again considering the exemplary sector 1 from **Fig. 4b** and assuming unity power factor operation, the line-to-line voltages are $|v_{bc}| < |v_{ab}| < |v_{ca}|$ (see **Fig. 4a**). Therefore, to avoid switching the line-to-line voltage with the highest magnitude, v_{ca}, the zero vector [cc] is not used in sector 1. The two remaining zero vectors [aa] (switching sequence: [ac]-[ab]-[aa]-[ab]-[ac]) and [bb] (switching sequence: [ac]-[ab]-[bb]-[ab]-[ac]) result in lower but identical switching losses, since both sequences lead to two hard and two soft commutations with the line-to-line voltage magnitudes $|v_{bc}|$ and $|v_{ab}|$.

For unity power factor, using the zero vector [aa] keeps phase a clamped to the positive dc-link current (i.e., the high-side commutation cell is not switching), but leads to the highest magnitude of the generated CM voltage, with the CM voltage of the CSR defined as $v_{CM} = (v_{pk}+v_{nk})/2$ (cf. **Fig. 2** and **Fig. 5** in [52]). Extending this criterion for the selection of the zero vector to the other sectors further leads to discontinuities in the local-average CM voltage at every second sector boundary. Instead, using [bb] (in the exemplary sector 1) results in the lowest CM voltage since $|v_a| > |v_b|$ are the phase voltages with the highest and the lowest magnitude in sector 1, respectively. Further, using the zero vector corresponding to the phase with the respective lowest instantaneous voltage value ([bb] in the exemplary sector 1) results in a continuous local average CM voltage [52], [53] and further results in a more uniform distribution of the instantaneous conduction and switching losses among the BDSs, which is particularly important for operation with very low ac fundamental frequencies (low motor speed) [54]. Therefore, we consider this variant (phase with lowest voltage magnitude defining the zero vector, i.e., switching sequence [ac]-[ab]-[bb]-[ab]-[ac] in the exemplary sector 1) for the further analysis.

For an ac-ac CSC with its back-to-back connected CSR and CSI, there are two independently working SV modulators responsible for synthesizing the CSR current vector $\vec{i}_g^* = \hat{i}_g^* \cdot e^{j\omega_g t}$ and the CSI current vector $\vec{i}_m^* = \hat{i}_m^* \cdot e^{j\omega_m t}$, respectively, using the common i_{dc} (see **Fig. 4**). The dwell times of the active and zero vectors of the CSR are

$$\begin{aligned} \delta_{[g+]} &= m_g \cdot \cos(\varphi_g - \pi/3) \\ \delta_{[g-]} &= m_g \cdot \cos(\varphi_g + \pi/3) \\ \delta_{[g0]} &= 1 - \delta_{[g+]} - \delta_{[g-]}, \end{aligned} \tag{2}$$

where $\delta_{[g+]}$ and $\delta_{[g-]}$ are the dwell times of the active vectors immediately leading and lagging $\vec{i}_g^*$ in counter-clockwise direction, and $\delta_{[g0]}$ is the dwell time of the zero vector. For example, considering $\vec{i}_g^*$ in sector 1 as shown in **Fig. 4b**, we have $\delta_{[g+]} = \delta_{ac}$, $\delta_{[g-]} = \delta_{ab}$ and $\delta_{[g0]} = \delta_{bb}$. Further, φ_g is the within-sector angle defined as

$$\varphi_g = \omega_g t - \lfloor \frac{\text{sect}_{CSR}}{2} \rfloor \cdot \frac{\pi}{3}, \tag{3}$$

where sect_{CSR} denotes the sector (see **Fig. 4**) of $\vec{i}_g^*$ and hence $\varphi_g \in [-\pi/6, \pi/6]$. Similarly, the dwell times of the CSI are

$$\begin{aligned} \delta_{[m+]} &= m_m \cdot \cos(\varphi_m - \pi/3) \\ \delta_{[m-]} &= m_m \cdot \cos(\varphi_m + \pi/3) \\ \delta_{[m0]} &= 1 - \delta_{[m+]} - \delta_{[m-]}, \end{aligned} \tag{4}$$

where $\delta_{[m+]}$ and $\delta_{[m-]}$ are the dwell times of the active vectors immediately leading and lagging $\vec{i}_m^*$ in counter-clockwise direction, and $\delta_{[m0]}$ is the dwell time of the zero vector. For example, for $\vec{i}_m^*$ in sector 5 as shown in **Fig. 4e**, we have $\delta_{[m+]} = \delta_{BA}$, $\delta_{[m-]} = \delta_{BC}$ and $\delta_{[m0]} = \delta_{CC}$. Finally, the within-sector angle is

$$\varphi_m = \omega_m t - \lfloor \frac{\text{sect}_{CSI}}{2} \rfloor \cdot \frac{\pi}{3},$$

with sect_{CSI} denoting the sector of $\vec{i}_m^*$.

A. Conventional Operation - Adaptive Constant DC-Link Current

As discussed above in **Section I**, the ac-ac CSC's CSR conventionally regulates i_{dc} to a constant value while the CSI uses this dc-link current to synthesize the desired motor currents. The reference value for i_{dc} is thus calculated as

$$i_{dc,conv}^* = \max\left(\hat{i}_g^*, \hat{i}_m^*\right), \tag{5}$$

corresponding to $i_{dc,2}$ in **Fig. 3** in the case of adaptive constant dc-link current. Therefore, during buck operation $i_{dc,conv}^* = \hat{i}_m^*$ as shown in **Fig. 5a** (left part) with simulated key waveform of the considered ac-ac CSC from **Fig. 1** with specifications

[4]The free-wheeling states are alternatively named as "shoot-through" states [51].

given in **Tab. I**. This implies that the CSR and CSI modulation indices are:

$$m_{\mathrm{g,conv}}\left(=\frac{\hat{i}^*_{\mathrm{g}}}{i^*_{\mathrm{dc,conv}}}\right)<1,\quad m_{\mathrm{m,conv}}\left(=\frac{\hat{i}^*_{\mathrm{m}}}{i^*_{\mathrm{dc,conv}}}\right)=1.$$

Similarly, for boost operation, $i^*_{\mathrm{dc,conv}}=\hat{i}^*_{\mathrm{g}}$ (see **Fig. 5a**, right part) implies $m_{\mathrm{g,conv}}=1$ and $m_{\mathrm{m,conv}}<1$.

From (2) and (4), clearly $m_{\mathrm{g,conv}}<1$ results in $\left(\delta_{[\mathrm{g}+]}+\delta_{[\mathrm{g}-]}\right)<1$ and hence $\delta_{[\mathrm{g}0]}>0$ at all times during buck operation, i.e., the CSR modulation must use zero vectors. Similarly, $m_{\mathrm{m,conv}}<1$ leads to $\left(\delta_{[\mathrm{m}+]}+\delta_{[\mathrm{m}-]}\right)<1$ and hence $\delta_{\mathrm{m}0}>0$ at all times during boost operation, i.e., the CSI modulation must use zero vectors. However, even the stage that defines $i^*_{\mathrm{dc,conv}}$ according to (5) and hence operates with unity modulation index requires zero vectors, since $m_{\mathrm{m,conv}}=1$ during buck operation also leads to $\left(\delta_{[\mathrm{m}+]}+\delta_{[\mathrm{m}-]}\right)<1$ if $\varphi_{\mathrm{m}}\neq 0$, and $m_{\mathrm{g,conv}}=1$ during boost operation results in $\left(\delta_{[\mathrm{g}+]}+\delta_{[\mathrm{g}-]}\right)<1$ if $\varphi_{\mathrm{g}}\neq 0$. The presence of a zero vector in the switching sequence results in a total of four switching transitions per switching period (two hard and two soft transitions; for example in **Fig. 4b**, the sequence [ac]-[ab]-[bb]-[ab]-[ac] leads to switching of $v_{\mathrm{cb}}, v_{\mathrm{ab}}, v_{\mathrm{ba}}$ and v_{bc}) and includes high-frequency modulation of i_{dc} to synthesize all three phase currents during a switching period (3/3-PWM).

Conventionally, thus, both, the CSR and the CSI, operate with 3/3-PWM irrespective of the operating point, as shown in **Fig. 5a**: The 3/3-PWM of the CSR and and the CSI is evident from the respective switched dc-side voltages v_{pn} and v_{PN}, which toggle between zero (zero vector) and the line-to-line voltages (active vectors) which correspond to the respective switching states, as well as from the switched currents $i_{\mathrm{a,s}}$ and $i_{\mathrm{A,s}}$, respectively (see **Fig. 1**), which toggle between zero (zero vector) and $\pm i_{\mathrm{dc,conv}}$ (active vector).

B. Proposed Loss-Optimal Operation

Again, as briefly introduced in **Section I**, selecting a time-varying dc-link current i_{dc} of a CSR or a CSI equal to the instantaneous maximum absolute value of the three ac phase current references eliminates the need for using zero vectors [29], [46]–[49]. The corresponding dc-link current references for the CSC's CSR and CSI, respectively, are

$$i^*_{\mathrm{dc,CSR}}(t)=\max\left\{|i^*_{\mathrm{a,s}}(t)|,|i^*_{\mathrm{b,s}}(t)|,|i^*_{\mathrm{c,s}}(t)|\right\}\text{ and}\qquad(6)$$

$$i^*_{\mathrm{dc,CSI}}(t)=\max\left\{|i^*_{\mathrm{A,s}}(t)|,|i^*_{\mathrm{B,s}}(t)|,|i^*_{\mathrm{C,s}}(t)|\right\}.\qquad(7)$$

Considering, for example, the CSI, the dc-link current thus equals (the absolute value of) one of the three phase currents during an entire sector. Therefore, the corresponding phase terminal is continuously connected to either the positive or the negative dc-link terminal, while only the two other phase currents must be synthesized with PWM (2/3-PWM). In the exemplary case shown in **Fig. 4c**, the switching sequence [BA]-[BC]-[BA] indicates that phase B is clamped to the positive dc-link terminal by the high-side commutation cell, while the low-side commutation cell operates two out of its three transistors with PWM, distributing the dc-link current between phases A and C. The corresponding absence of a zero vector advantageously reduces the number of switching transitions per switching period from four (3/3-PWM, see above) to two (one hard and one soft transition involving v_{AC} and v_{CA}).

The elimination of zero vectors with (6) and (7) can be easily verified with dwell time calculations according to (2) and (4), respectively. Maintaining $i^*_{\mathrm{dc,CSR}}(t)$ according to (6) implies $i^*_{\mathrm{dc,CSR}}(t)=\hat{i}^*_{\mathrm{g}}\cos(\varphi_{\mathrm{g}})\implies m_{\mathrm{g}}(t)=1/\cos(\varphi_{\mathrm{g}})$ which leads to $\delta_{[\mathrm{g}+]}+\delta_{[\mathrm{g}-]}=1\implies\delta_{[\mathrm{g}0]}=0\ \forall\varphi_{\mathrm{g}}$ [49]. Similarly, maintaining $i^*_{\mathrm{DC,CSI}}(t)$ according to (7) leads to $m_{\mathrm{m}}(t)=1/\cos(\varphi_{\mathrm{m}})\implies\delta_{[\mathrm{m}+]}+\delta_{[\mathrm{m}-]}=1\implies\delta_{[\mathrm{m}0]}=0\ \forall\varphi_{\mathrm{m}}$.

In an ac-ac CSC, the CSR and the CSI share the same dc-link current, which hence must be selected according to

$$i^*_{\mathrm{dc,syn}}(t)=\max\left\{i^*_{\mathrm{dc,CSR}}(t),i^*_{\mathrm{dc,CSI}}(t)\right\}.\qquad(8)$$

Doing so ensures that at any point in time, either the CSR *or* the CSI operates with 2/3-PWM, while the other stage must operate with 3/3-PWM and shape the dc-link current accordingly, i.e., the two stages operate in a synergetic manner to minimize the overall losses. This is visualized in **Fig. 3** and in the SV diagrams of **Fig. 4b,c** for buck operation where the CSI defines $i^*_{\mathrm{dc,syn}}(t)$ according to (7) and operates with 2/3-PWM. The dc-link current $i^*_{\mathrm{dc,syn}}(t)$ thus varies according to $\hat{i}^*_{\mathrm{m}}\cos(\varphi_{\mathrm{m}})$ with $\varphi_{\mathrm{m}}\in[-\pi/6,\pi/6]$, which corresponds to a scaling of the SV hexagon such that $\vec{i}^*_{\mathrm{m}}$ always coincides with its perimeter. In buck mode, the magnitude of $\vec{i}^*_{\mathrm{g}}$ is smaller than that of $\vec{i}^*_{\mathrm{m}}$, i.e., the circular trajectory of $\vec{i}^*_{\mathrm{g}}$ lies always within the hexagon, which implies 3/3-PWM for the CSR.

Fig. 5b shows simulated key waveforms, where buck operation occurs for $V_{\mathrm{m}}/V_{\mathrm{g}}<\sqrt{3}/2$. Then, the dc-link current's six-pulse shape is defined by the motor currents according to (7). The absence of free-wheeling states (zero vectors) during 2/3-PWM operation of the CSI is visible in the waveform of v_{PN}, which never reaches zero and only switches between two of the three line-to-line voltage absolute values ($|v_{\mathrm{XY}}|$ and $|v_{\mathrm{XZ}}|$, where X refers to the clamped phase with the highest absolute value of current). Further, note that the CSI's output current, e.g., $i_{\mathrm{A,s}}$, shows intervals without PWM operation when $i^*_{\mathrm{dc,CSI}}(t)=|i_{\mathrm{A}}(t)|$ and hence $|i_{\mathrm{A,s}}|=i_{\mathrm{dc,syn}}$, which allows clamping of phase A to the dc-link. On the other hand, 3/3-PWM operation of CSR results in switching of v_{pn} between zero and two other line-to-line voltages, and $i_{\mathrm{a,s}}$ is always switching between zero and $i_{\mathrm{dc,syn}}$.

Fig. 4d,e depict the SV diagrams for boost operation, where the roles of the CSR and the CSI are swapped, i.e., the CSR now defines $i^*_{\mathrm{dc,syn}}(t)$ according to (6) and operates with 2/3-PWM while the CSI operates with 3/3-PWM. Similarly, **Fig. 5b** shows boost operation for $V_{\mathrm{m}}/V_{\mathrm{g}}>2/\sqrt{3}$, where now v_{pn} never attains zero and the switched current of the CSR's phase a shows clamping intervals with $i_{\mathrm{a,s}}=i_{\mathrm{dc,syn}}$ when $i^*_{\mathrm{dc,CSR}}(t)=|i_{\mathrm{a}}(t)|$, i.e., the CSR operates with 2/3-PWM. On the other hand, v_{PN} switches between zero and line-to-line voltages and $i_{\mathrm{A,s}}$ always toggles between zero and $i_{\mathrm{dc,syn}}$, i.e., the CSI operates with 3/3-PWM. Note the change in frequency of $i_{\mathrm{dc,syn}}$ in boost compared to buck operation, which is a consequence of the generally different grid and motor frequencies.

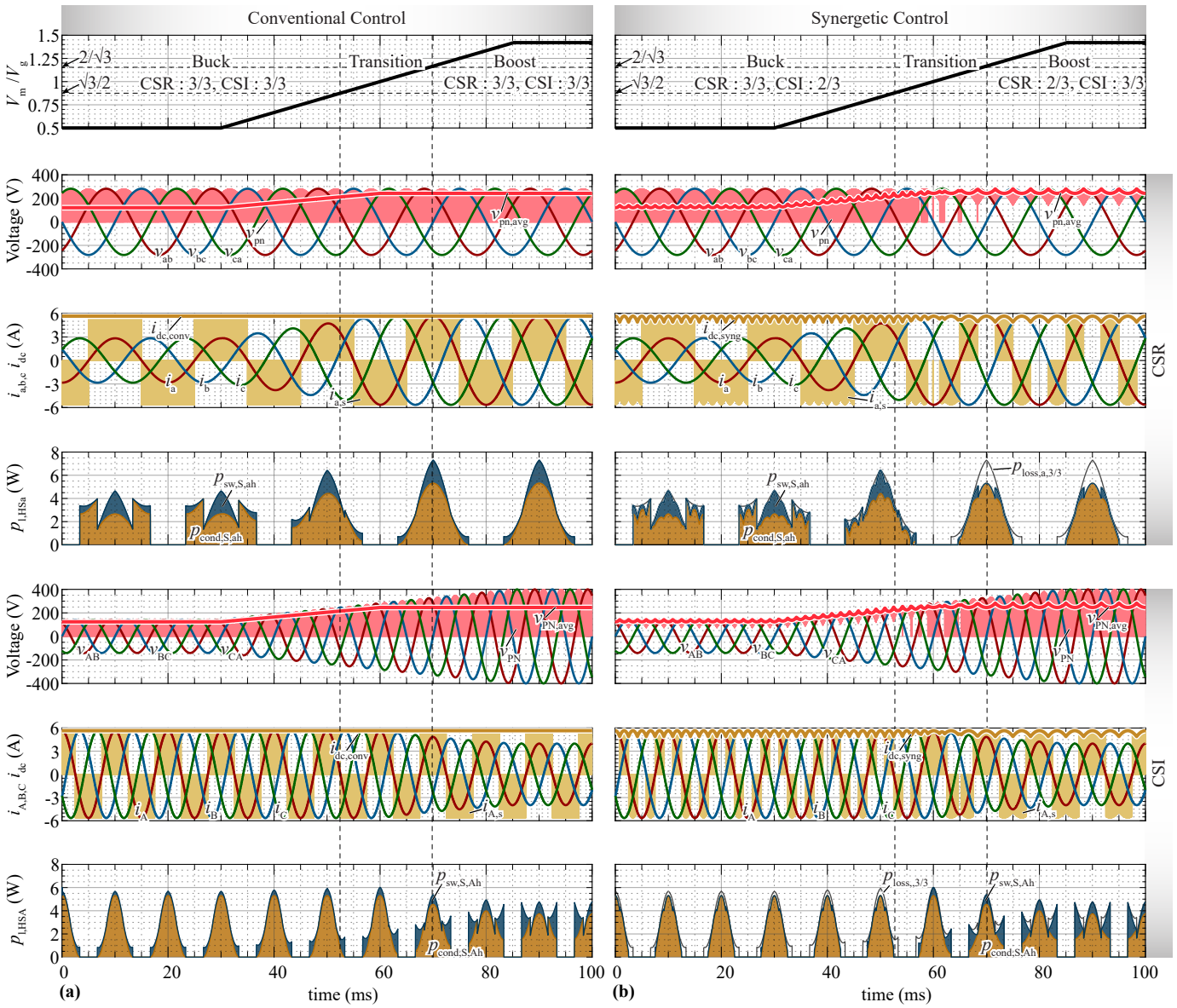

Fig. 5. Simulated key waveforms of the ac-ac CSC from **Fig. 1** with $V_{g,n} = 200\,\mathrm{V}$, $f_g = 50\,\mathrm{Hz}$, $f_m = 100\,\mathrm{Hz}$ and V_m increasing from 100 V to 283 V with a maximum power limit of $P_n = 1.4\,\mathrm{kW}$ according to **Fig. 2**. **(a)** Conventional and **(b)** proposed synergetic control: for $V_m/V_g < \sqrt{3}/2$ (buck), the CSR operates with 3/3-PWM and regulates i_{dc} such that the CSI operates with 2/3-PWM. Similarly, for $V_m/V_g > 2/\sqrt{3}$ (boost), the CSR operates with 2/3-PWM and defines the reference for i_{dc}, which is regulated by the CSI thus operating with 3/3-PWM. For $\sqrt{3}/2 < V_m/V_g < 2/\sqrt{3}$ (transition mode), both, the CSR and the CSI alternatingly operate with 2/3-PWM and 3/3-PWM. Conduction and switching losses are calculated considering measurements [40] of first-generation 600 V, 140 mΩ GaN M-BDSs. Note that in a motor application, an increase of the motor/output voltage is coupled to an increase of the output frequency; this increase in frequency is, however, not important for the explanation of the proposed synergetic control method and therefore not shown for the sake of better visibility.

Note that the local average values of v_{PN} and v_{pn} follow the six pulse shape of $i_{dc,syn}$ but in opposite relation, i.e., $v_{PN,avg}$ and $v_{pn,avg}$ are at their maxima when $i_{dc,syn}$ is at it's minimum and vice versa, as expected from the constant power flow through the dc-side interfaces of the CSR and the CSI.

Finally, for $\sqrt{3}/2 < V_m/V_g < 2/\sqrt{3}$, i.e., in the transition region between buck and boost operation, the CSR and the CSI interchangeably operate with 2/3-PWM and 3/3-PWM depending on the instantaneous value of $\max\{i^*_{dc,CSR}(t), i^*_{dc,CSI}(t)\}$, which is visible in the waveforms of v_{pn} and v_{PN}, respectively.

It is therefore possible to always operate one of the ac-ac CSC's two stages with 2/3-PWM and hence with minimum possible dc-link current, which ensures minimum possible switching and conduction losses as discussed in the following; then, **Section III** introduces a synergetic control method that ensures this loss-optimal mode of operation.

C. Losses in Conventional and Loss-Optimal Operation

The quantitative reduction in losses achieved through loss-optimal operation / synergetic control of the ac-ac CSC are discussed based on closed-form expressions for transistor conduction and switching losses.

1) Conduction Losses: Since, at any point in time, four (and only four) M-BDSs conduct the dc-link current, the conduction

losses with conventional (see **Subsection II-A** above) operation of the ac-ac CSC are

$$P_{\mathrm{cond,conv}} = 4 \cdot i_{\mathrm{dc,conv}}^2 \cdot R_{\mathrm{ds,on}}, \tag{9}$$

where $R_{\mathrm{ds,on}}$ is the on-state resistance of an M-BDS and, $i_{\mathrm{dc,conv}}$ is calculated according to (5).

Instead, for loss-optimal operation, the dc-link current is shaped according to (8), i.e., always attains the minimum value necessary to synthesize the grid and motor currents (see **Fig. 5b**). This results in a lower rms value of

$$\begin{aligned} i_{\mathrm{rms,syn}} &= \sqrt{\frac{3}{\pi}\left[\int_{-\pi/6}^{\pi/6} \max\left\{\hat{i}_{\mathrm{g}}, \hat{i}_{\mathrm{m}}\right\}^2 \cos^2(\varphi)\, d\varphi\right]} \\ &\approx 0.956 \cdot i_{\mathrm{dc,conv}}. \end{aligned}$$

Therefore, the total conduction losses are

$$P_{\mathrm{cond,syn}} \approx 0.91 \cdot 4 \cdot i_{\mathrm{dc,conv}}^2 \cdot R_{\mathrm{ds,on}}, \tag{10}$$

i.e., reduced by around 9% compared to conventional operation. Note that the lower rms value of the dc-link current not only benefits the transistors, but also reduces the winding losses of the dc-link inductor L_{dc} accordingly.

Considering, first-generation 600 V, 140 mΩ M-BDSs [40], **Fig. 5** shows the instantaneous conduction losses $p_{\mathrm{cond,S,ah}}$ of a CSR M-BDS $\mathrm{S_{ah}}$ and $p_{\mathrm{cond,S,Ah}}$ of a CSI M-BDS $\mathrm{S_{Ah}}$ (see **Fig. 1**) for both, conventional and loss-optimal operation and a varying input/output voltage ratio, $V_{\mathrm{m}}/V_{\mathrm{g}}$. Considering the operation with adaptive constant dc-link current (see **Fig. 5a**), the dc-link current does not change with the input/output voltage ratio and hence the average conduction losses of $\mathrm{S_{ah}}$ and $\mathrm{S_{Ah}}$ are independent of the input/output voltage ratio and further equal to each other. A like observation holds for loss-optimal operation (see **Fig. 5b**), where the average conduction losses are reduced to about 91%.

Note, however, that the evolution of $p_{\mathrm{cond,S,ah}}$ within a fundamental period shows a more even distribution with lower peak value in buck operation compared to boost operation (the opposite behavior is observed for $p_{\mathrm{cond,S,Ah}}$). This is a consequence of the active/zero vector selection and the respective dwell times, e.g., in buck mode, in any switching period, $\mathrm{S_{ah}}$ is either used by the active vectors or by the zero vector, but not by both, which lowers the peak conduction losses for the short dwell times of the active vectors in buck mode (low grid current compared to the dc-link current).

2) Switching Losses: Conventionally, both stages of the the ac-ac CSC operate with 3/3-PWM. Considering, as an example, sector 1 of the CSR during buck operation (see **Fig. 4b**), there are four transitions per switching period, with switched voltages of $v_{\mathrm{cb}}, v_{\mathrm{ab}}, v_{\mathrm{ba}}$ and v_{bc}. Since the direction of the dc-link current i_{dc} is fixed, two of these transitions are hard-switching transitions (v_{ba} and v_{bc}) and two are soft-switching transitions (v_{cb} and v_{ab}), i.e., the overall switching losses are equivalent to those of two half bridges operating with the voltages v_{bc} and v_{ab}, and the current i_{dc}. Owing to the symmetry between sectors, the overall switching losses of the CSR-stage operating with 3/3-PWM and unity power factor are thus

$$\begin{aligned} P_{\mathrm{sw,csr,conv}} = f_{\mathrm{sw}} \cdot \frac{6}{\pi}\Bigg[\int_0^{\pi/6} \Big(&e_{\mathrm{sw}}\left(i_{\mathrm{dc,conv}}, v_{\mathrm{ab}}\right) \\ &+ e_{\mathrm{sw}}\left(i_{\mathrm{dc,conv}}, v_{\mathrm{bc}}\right)\Big)\, d\varphi_{\mathrm{g}}\Bigg], \end{aligned} \tag{11}$$

with f_{sw} denoting the switching frequency and where

$$e_{\mathrm{sw}}(i_{\mathrm{sw}}, v_{\mathrm{sw}}) = \mathrm{k_1} \cdot i_{\mathrm{sw}} \cdot v_{\mathrm{sw}} + \mathrm{k_2} \cdot v_{\mathrm{sw}}^2 \tag{12}$$

is the total half-bridge switching energy (i.e., sum of the turn-on and the turn-off energy), with i_{sw} and v_{sw} denoting the switched current and voltage, respectively. For the considered 600 V, 140 mΩ GaN M-BDS, the authors have presented corresponding calorimetric measurements[5] in [40], resulting in $\mathrm{k_1} = 2.16 \times 10^{-8}\,\mathrm{J/(VA)}$ and $\mathrm{k_2} = 1.3 \times 10^{-10}\,\mathrm{J/V^2}$.

Evaluating the integral from (11) then yields a closed-form expression for the CSR-stage switching losses:

$$P_{\mathrm{sw,csr,conv}} = \frac{3\hat{V}_{\mathrm{g}} f_{\mathrm{sw}}}{\pi}\left[\mathrm{k_1} i_{\mathrm{dc,conv}} + \mathrm{k_2}\hat{V}_{\mathrm{g}}\frac{4\pi - 3\sqrt{3}}{12}\right]. \tag{13}$$

Similarly, the switching losses of the CSI with conventional operation (3/3-PWM) under unity power factor are

$$P_{\mathrm{sw,csi,conv}} = \frac{3\hat{V}_{\mathrm{m}} f_{\mathrm{sw}}}{\pi}\left[\mathrm{k_1} i_{\mathrm{dc,conv}} + \mathrm{k_2}\hat{V}_{\mathrm{m}}\frac{4\pi - 3\sqrt{3}}{12}\right]. \tag{14}$$

Instead, with loss-optimal operation of the ac-ac CSC, the stage operating with 2/3-PWM has only two (instead of four) switching transitions per switching period. Considering, for instance, sector 5 of the CSI during buck operation (see **Fig. 4b**), the switched voltages are V_{AC} and V_{CA}. Again, since the direction of the dc-link current i_{dc} is fixed, there is only one hard and one soft transition. Following the derivation of (13), the overall switching losses of the stage operating with 2/3-PWM are

$$P_{\mathrm{sw,23,syn}} = \frac{3\hat{V}_{23} f_{\mathrm{sw}}}{\pi}\left[\frac{\mathrm{k_1}\hat{i}_{\mathrm{dc,syn}}}{4} + \mathrm{k_2}\hat{V}_{23}\frac{2\pi - 3\sqrt{3}}{12}\right], \tag{15}$$

where $\hat{i}_{\mathrm{dc,syn}}$ is the peak value of the loss-optimum dc-link current from (8), i.e., $\hat{i}_{\mathrm{dc,syn}} = \max\left\{\hat{i}_{\mathrm{g}}, \hat{i}_{\mathrm{m}}\right\} = i_{\mathrm{dc,conv}}$. Further, $\hat{V}_{23}$ is the peak line-to-line voltage of the stage operated with 2/3-PWM. For the same system parameters, operating the CSR or the CSI with 2/3-PWM instead of with 3/3-PWM thus reduces the switching losses of that stage by around 76% at the nominal operating point[6].

[5]Since a CSC commutation cell has three switches connected to a common switched node, the switching transition between any two of these switches forces a change of voltage across the third switch as well, which incurs additional C_{oss} losses. However, as confirmed by measurements in [40], the overall contribution over a mains period is small enough to be neglected.

[6]The reduction in switching losses with 2/3-PWM is calculated for the case where the zero vectors for 3/3-PWM are selected to minimize the amplitude of the switched voltage as discussed at the beginning of **Section II**. Choosing the zero vector differently can potentially result in even higher savings of switching losses. Further note that the reduction of switching losses depend on the ratio of $\mathrm{k_1}/\mathrm{k_2}$. Therefore, employing transistors with different switching loss characteristics will result in different savings of switching losses.

For loss-optimal operation of the ac-ac CSC, one of the stages still operates with 3/3-PWM (CSR during buck and CSI during boost operation) but, in contrast to the conventional case, with lower and time-varying dc-link current $i_{\mathrm{dc,syn}}$, whereby the shape of $i_{\mathrm{dc,syn}}$ depends on the fundamental frequency of the other stage operating with 2/3-PWM. This implies that the switching losses of the stage operated with 3/3-PWM are a function of both, φ_{g} and φ_{m}, which complicates the derivation of a closed-form solution. It has, however, been verified by simulation that the difference in switching losses of the stage operating with 3/3-PWM when the fundamental frequency of the other stage operating with 2/3-PWM is varied between 1 Hz and 200 Hz is negligible. Therefore, assuming the same fundamental frequency on the grid and motor side, the switching losses of the stage operating with 3/3-PWM are

$$P_{\mathrm{sw,33,syn}} = \frac{3\hat{V}_{33} f_{\mathrm{sw}}}{\pi}\left[\mathrm{k}_1 \hat{i}_{\mathrm{dc,syn}} \frac{\sqrt{3}\pi + 6}{12} + \mathrm{k}_2 \hat{V}_{33} \frac{4\pi - 3\sqrt{3}}{12}\right], \tag{16}$$

where $\hat{V}_{33}$ is the peak line-to-line voltage of the stage operating with 3/3-PWM. For operating the CSR or the CSI with 3/3-PWM according to loss optimal operation, that is, with the other stage operated with 2/3-PWM, the switching losses of that stage are reduced by around 4% at nominal operating point compared to conventional operation.

The total switching losses for conventional and loss-optimal operation of the ac-ac CSC are therefore

$$P_{\mathrm{sw,conv}} = P_{\mathrm{sw,csr,conv}} + P_{\mathrm{sw,csi,conv}} \quad \text{and} \tag{17}$$

$$P_{\mathrm{sw,syn}} = P_{\mathrm{sw,23,syn}} + P_{\mathrm{sw,33,syn}}, \tag{18}$$

respectively, whereby the roles (2/3-PWM, 3/3-PWM) of the CSR and the CSI change depending on the ratio of input to output voltage.

Fig. 5 shows the instantaneous switching losses $p_{\mathrm{sw,S,ah}}$ of the CSR's M-BDS S_{ah} and $p_{\mathrm{sw,S,Ah}}$ of the CSI's M-BDS S_{Ah} (see **Fig. 1**) for conventional and loss-optimal operation. For conventional operation, the CSR's switching losses do not depend on the output voltage (buck or boost mode) as a result of the fixed grid voltage and constant magnitude of $i_{\mathrm{dc,conv}}$ during the simulation, see **Fig. 5a**. In contrast, loss-optimal operation implies 2/3-PWM operation of the CSR during boost mode and thus considerably lower switching losses; this is also visually evident in **Fig. 5b** from the superimposed total loss envelopes for conventional operation. Note that even in buck mode (when the CSR operates with 3/3-PWM), there is a slight reduction of losses as expected from (16), i.e., because loss-optimal operation implies that the minimum possible dc-link current is used.

The switching losses of the CSI increase during the transition from buck to boost mode with both, conventional and loss-optimal operation, because of the increasing motor-side ac voltage. For loss-optimal operation, the CSI operates with 2/3-PWM in buck mode, which again results in loss savings as shown in **Fig. 5b**; since the load voltage is then relatively low (buck mode), the reduction in switching losses is less pronounced than in case of the CSR operating with 2/3-PWM in boost mode.

3) Comparison: Based on the closed-form expressions for semiconductor conduction and switching losses derived above, and considering first-generation 600 V, 140 mΩ GaN M-BDSs, **Fig. 6a** visualizes how loss-optimal/synergetic operation increases the semiconductor efficiency throughout the operating area. Similarly, **Fig. 6b** shows the percentage-point increase of the semiconductor efficiency and **Fig. 6c** shows the normalized semiconductor loss reduction. The semiconductor efficiency with loss-optimal/synergetic operation is necessarily higher than with conventional operation throughout the operating region, because always one stage operates with 2/3-PWM and the minimum possible dc-link current is used, irrespective of buck, boost, or transition region.

Note that the efficiency improvement depends on the selected device and switching frequencies; it will be higher for devices with larger chip area, i.e., designs using future M-BDSs with a lower on-state resistance and consequently higher output capacitance are expected to benefit more from loss-optimal/synergetic operation.

Further, note that the loss-optimal operation results in a slightly lower worst-case voltage-time area applied to the dc-link inductor. Therefore, and because of the lower dc-link current, in principle a minor reduction in size could be achieved if specifically designed for a CSC that always employs loss-optimal operation.

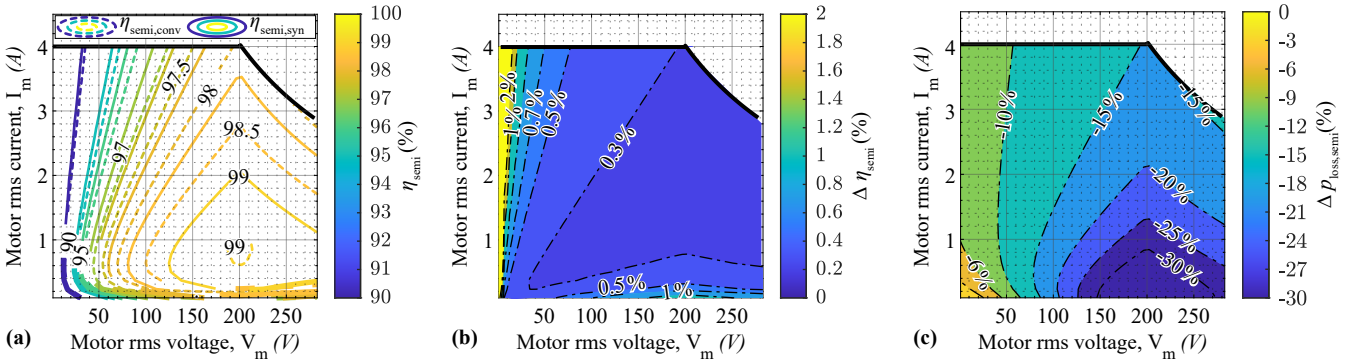

Fig. 6. Semiconductor loss reduction through loss-optimal operation of an ac-ac CSC using 600 V, 140 mΩ GaN M-BDSs and a switching frequency of $f_{\mathrm{sw}} = 72$ kHz. **(a)** Contours of semiconductor efficiencies in the operating area (see **Fig. 2**) for conventional, i.e. with adaptive constant i_{dc} ($\eta_{\mathrm{semi,conv}}$) and loss-optimal/synergetic ($\eta_{\mathrm{semi,syn}}$) operation. **(b)** Percentage-point change in semiconductor efficiency, $\Delta\eta_{\mathrm{semi}} = \eta_{\mathrm{semi,syn}} - \eta_{\mathrm{semi,conv}}$, and **(c)** relative reduction in semiconductor losses, $\Delta p_{\mathrm{loss,semi}} = (p_{\mathrm{loss,semi,syn}} - p_{\mathrm{loss,semi,conv}}) \cdot 100 / p_{\mathrm{loss,semi,conv}}$ achieved with loss-optimal/synergetic instead of conventional operation.

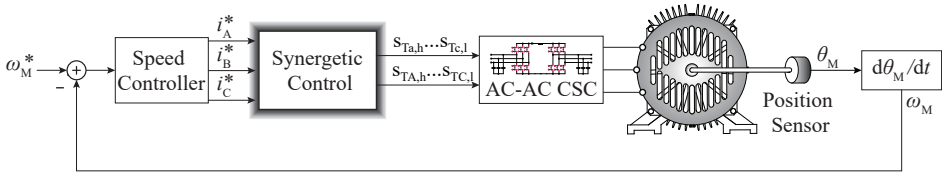

Fig. 7. Exemplary motor speed control loop that generates the motor current references, i_{M}^{*}, which are the inputs for the synergetic control structure from **Fig. 8**.

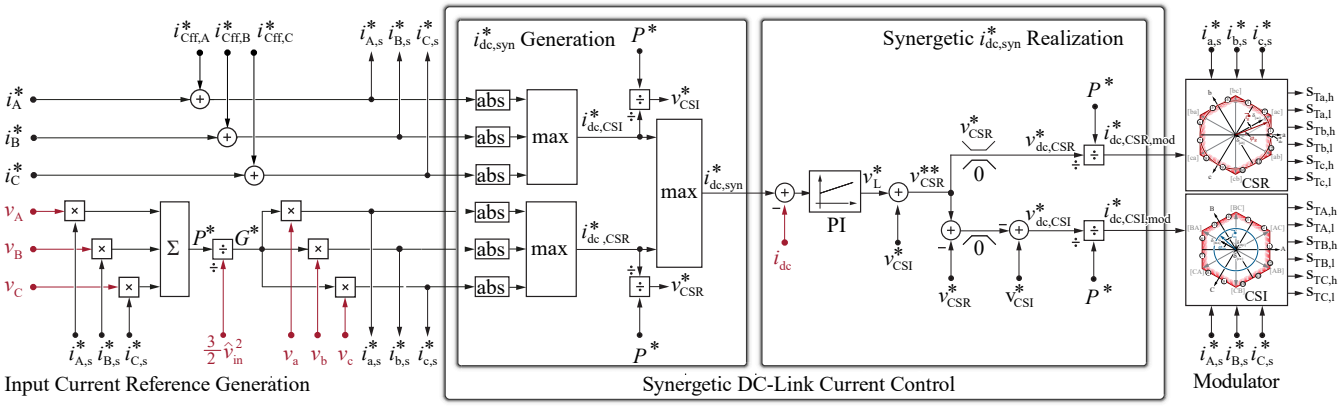

Fig. 8. Block diagram of the proposed synergetic control of the ac-ac CSC from **Fig. 1**, which ensures loss-optimal operation with minimum possible dc-link current and 2/3-PWM of either the CSR or the CSI. Based on instantaneous (local average) quantities, the control structure ensures seamless transitions between buck (motor voltages are lower than the grid voltages) and boost mode (the motor voltages are higher than the grid voltages) and facilitates operation in the transition region, where the system essentially changes between buck and boost mode sequentially over fundamental grid or motor period.

III. Synergetic Control Implementation

This section details the proposed synergetic control method [40] that ensures loss-optimal operation (minimum possible dc-link current and 2/3-PWM of the CSR or the CSI) as described above in **Section II** for any operating point (see **Fig. 2**). In a VSD, there is an outer motor speed control loop (see **Fig. 7**) that, by using, e.g., field-oriented control, ultimately generates the motor phase current references i_{A}^{*}, i_{B}^{*}, and i_{C}^{*}. These motor phase current references are then further processed by the proposed synergetic control method according to the block diagram shown in **Fig. 8** and discussed in the following. Note that all quantities used in the following refer to local average (over one switching period) values.

A. Input Current Reference Generation

The synergetic control of the ac-ac CSC requires both, input and output reference currents to obtain the required time-varying dc-link current value $i_{\mathrm{dc,syn}}^{*}$ with (8). The output current references are typically provided by an application-specific outer control loop (see **Fig. 7**). The feed-forward of the output filter capacitor (C_{DM1} in **Fig. 1**) currents, $i_{\mathrm{Cff,X}}^{*}$, $X \in [\mathrm{A,B,C}]$ can be added to the output current references to calculate the CSI current reference values $i_{\mathrm{A,s}}^{*}$, $i_{\mathrm{B,s}}^{*}$ and $i_{\mathrm{C,s}}^{*}$.

Aiming for unity power factor operation, the CSR current reference values $i_{\mathrm{a,s}}^{*}$, $i_{\mathrm{b,s}}^{*}$, and $i_{\mathrm{c,s}}^{*}$ are then generated from the power balance between motor and grid side as

$$i_{\mathrm{x,s}}^{*} = G^{*} \cdot v_{\mathrm{x}} \quad \text{with} \quad \mathrm{x} \in [\mathrm{a,b,c}] \quad \text{and} \quad G^{*} = \frac{P^{*}}{\frac{3}{2}\hat{v}_{\mathrm{g}}^{2}}, \tag{19}$$

where $v_{\mathrm{x}}, x \in [\mathrm{a,b,c}]$ are the measured grid phase voltages and $\hat{v}_{\mathrm{g}}$ is their amplitude, and G^{*} is the reference conductance. The power reference P^{*} is generated from the CSI current references and the measured output voltage according to $P^{*} = \sum\{v_{\mathrm{X}} \cdot i_{\mathrm{X,s}}^{*}\}, X \in [\mathrm{A,B,C}]$.[7],[8]

B. DC-link Current Reference Generation

The dc-link current reference i_{dc}^{*} is then calculated according to (6), (7), and (8) such that i_{dc}^{*} always equals the maximum absolute value of all six phase current references, which enables 2/3-PWM for the stage with the higher phase current references. A PI controller acts on the deviation of the measured dc-link current i_{dc} and the reference value i_{dc}^{*} to generate the dc-link inductor voltage reference, v_{L}^{*}, required to track i_{dc}^{*}.

Also, based on $i_{\mathrm{dc,CSR}}^{*}$ and $i_{\mathrm{dc,CSI}}^{*}$, which are the dc-link current references that would result in 2/3-PWM of the CSR or the CSI, respectively, the corresponding dc-link voltage references

$$v_{\mathrm{CSR}}^{*} = \frac{P^{*}}{i_{\mathrm{dc,CSR}}^{*}} \quad \text{and} \quad v_{\mathrm{CSI}}^{*} = \frac{P^{*}}{i_{\mathrm{dc,CSI}}^{*}} \tag{20}$$

are calculated, i.e., the dc-link voltage references that correspond to 2/3-PWM operation of the respective stage.

C. Synergetic Shaping of DC-link Current

The dc-link inductor voltage v_{L} is the difference between the two dc-side voltages v_{pn} and v_{PN}. To generate a desired

[7]Note that the power reference can also be obtained by the motor speed and torque reference, in which case, a measurement of output voltage will not be strictly required.

[8]Note that for non-unity power factor loads, e.g., an induction machine, the calculation of the (active) power reference P^{*} should be performed in the *dq* coordinate frame. The rest of the proposed synergetic control structure, however, remains the same.

reference inductor voltage v_{L}^{*}, at least one of the two dc-side voltage references must be modified accordingly. As one of the stages should operate with 2/3-PWM, the other stage is utilized for realizing v_{L}^{*} by accordingly adjusting its dc-side voltage reference. This is the core mechanism of the synergetic control method and the implementation is detailed in the following.

First, v_{L}^{*} is added to v_{CSI}^{*} to form a virtual dc-side voltage reference for the CSR, $v_{\mathrm{CSR}}^{**} = v_{\mathrm{CSI}}^{*} + v_{\mathrm{L}}^{*}$, which would be the dc-side voltage that the CSR must generate to enable 2/3-PWM of the CSI with v_{L}^{*} applied across L_{dc}.[9] However, this is only feasible if $i_{\mathrm{dc,CSI}}^{*} > i_{\mathrm{dc,CSR}}^{*}$ (or, equivalently, $v_{\mathrm{dc,CSI}}^{*} < v_{\mathrm{dc,CSR}}^{*}$), i.e., during buck operation. Assuming that v_{L}^{*} is small, this condition corresponds to $v_{\mathrm{CSR}}^{**} < v_{\mathrm{CSR}}^{*}$, i.e., the limiter in the upper signal path is not active and the dc-link current reference fed to the CSR modulator is

$$i_{\mathrm{dc,CSR,mod}}^{*} = \frac{P^{*}}{v_{\mathrm{dc,CSR}}^{*}} = \frac{P^{*}}{v_{\mathrm{L}}^{*} + v_{\mathrm{CSI}}^{*}} > i_{\mathrm{dc,CSR}}^{*}.$$

Hence the CSR operates with 3/3-PWM and controls the dc-link current. In the lower signal path, $v_{\mathrm{CSR}}^{**} - v_{\mathrm{CSR}}^{*} < 0$ is clamped at zero and hence the dc-link current reference fed to the CSI modulator is

$$i_{\mathrm{dc,CSI,mod}}^{*} = \frac{P^{*}}{v_{\mathrm{dc,CSI}}^{*}} = \frac{P^{*}}{v_{\mathrm{CSI}}^{*}} = i_{\mathrm{dc,CSI}}^{*},$$

which ensures 2/3-PWM operation of the CSI during buck operation. The modulator calculates the duty cycles for the transistors as discussed in **Section II**, i.e., in case a suitable dc-link current reference is used, no zero vectors are employed.

If, in contrast, $v_{\mathrm{CSR}}^{**} > v_{\mathrm{CSR}}^{*}$ (and hence $i_{\mathrm{dc,CSI}}^{*} < i_{\mathrm{dc,CSR}}^{*}$, i.e., boost mode), the limiter in the upper signal path clamps at v_{CSR}^{*} and the dc-link current reference fed to the CSR modulator becomes

$$i_{\mathrm{dc,CSR,mod}}^{*} = \frac{P^{*}}{v_{\mathrm{dc,CSR}}^{*}} = \frac{P^{*}}{v_{\mathrm{CSR}}^{*}} = i_{\mathrm{dc,CSR}}^{*},$$

ensuring 2/3-PWM operation of the CSR in boost mode. In the lower signal path, $v_{\mathrm{CSR}}^{**} - v_{\mathrm{CSR}}^{*} > 0$ is not clamped and hence $v_{\mathrm{dc,CSI}}^{*} = v_{\mathrm{CSI}}^{*} - (v_{\mathrm{L}}^{*} + v_{\mathrm{CSI}}^{*} - v_{\mathrm{CSR}}^{*}) = v_{\mathrm{CSR}}^{*} - v_{\mathrm{L}}^{*}$ results. The dc-link current reference of the CSI modulator thus becomes

$$i_{\mathrm{dc,CSI,mod}}^{*} = \frac{P^{*}}{v_{\mathrm{dc,CSI}}^{*}} = \frac{P^{*}}{v_{\mathrm{CSR}}^{*} - v_{\mathrm{L}}^{*}} > i_{\mathrm{dc,CSI}}^{*};$$

the CSI operates with 3/3-PWM and controls the dc-link current.

The proposed synergetic control method from **Fig. 8** thus ensures that always one stage operates with 3/3-PWM and controls the dc-link current such that the other stage can operate with 2/3-PWM. As the control structure works with instantaneous (local average) quantities, seamless transitions between operating points are achieved. Further, also the transition region is covered, where the roles of the CSR and the CSI swap multiple times during a fundamental grid or motor period.

TABLE II
KEY COMPONENTS OF THE REALIZED AC-AC CSC DEMONSTRATOR FROM **FIG. 10**.

Parameter		Value	Unit
Switching Frequency	f_{s}	72	kHz
dc-link ind.	2 x L_{dc} /2	2 x 600 2 x 00K3515E060 3 stacked, 54 turns	µH @ 6 A
EMI 1st st. CM ind.	L_{cm1}	4 VAC 500F 30x20x10, 2 stacked, 10 turns	mH @ 72 kHz
EMI 1st st. CM cap.	C_{cm1}	0.1	µF
EMI 1st st. DM ind.	L_{dm1}, L_{DM1}	220	µH
EMI 1st st. CSR DM cap.	C_{dm1}	3.6	µF
EMI 1st st. CSI DM cap.	C_{DM1}	3.26	µF
EMI 2nd st. CM ind.	L_{cm2}, L_{CM2}	2 x 1.1 2 x VAC 500F, 16x10x06, 9 turns	mH @ 72 kHz
EMI 2nd st. CM cap.	C_{cm2}, C_{CM2}	10	nF
EMI 2nd st. DM ind.	L_{dm2}, L_{DM2}	33	µH
EMI 2nd st. CSR DM cap.	C_{dm2}	1.8	µF
EMI 2nd st. CSI DM cap.	C_{DM2}	2.2	µF

IV. EXPERIMENTAL VERIFICATION

The proposed synergetic control method and the expected improvement of the system efficiency compared to conventional operation is experimentally verified with the ac-ac CSC hardware demonstrator shown in **Fig. 10** with specifications given in **Tab. I** and key component values listed in **Tab. II**. The demonstrator consists of two PCBs, a control and measurement PCB carrying a Xilinx Zynq 7000 SoC, and a power PCB with the CSR and CSI commutation cells based on first-generation 600 V, 140 mΩ GaN M-BDSs. Further details about the design of the hardware have been presented by the authors in [41] and are not reiterated here for the sake of brevity. All tests have been carried out with resistive load instead of a motor with the load resistor value manually adjusted to obtain desired output voltage for a given current reference.

A. Steady-State and Transient Waveforms

Fig. 11 shows measured key waveforms for buck operation with $V_{\mathrm{m}} < V_{\mathrm{g}}$ in **Fig. 11a**, for nominal operation with $V_{\mathrm{m}} = V_{\mathrm{g}}$ in **Fig. 11b**, and for boost operation with $V_{\mathrm{m}} > V_{\mathrm{g}}$ in **Fig. 11c**.

1) Buck Mode: In buck mode, the the dc-link current i_{dc} equals the absolute maximum of the load-side phase currents according to (7) and hence the CSI operates with 2/3-PWM; the absence of zero states is evident in the v_{PN} waveform in **Fig. 11a.ii**, which toggles only between line-to-line voltages but does not attain zero. Note further that the local average value of the dc-link current, $i_{\mathrm{dc,avg}}$, superimposed on the CSR measurements in **Fig. 11a.i** is always higher than the amplitude of the grid currents. Therefore, the CSR modulator must use both, active and zero states, which results in v_{pn} toggling between line-to-line voltages and zero in every switching period.

[9]Note that as a starting step, v_{L}^{*} could also be subtracted from v_{CSR}^{*} to form a virtual dc-side voltage reference of the CSI, $v_{\mathrm{CSI}}^{**} = v_{\mathrm{CSR}}^{*} - v_{\mathrm{L}}^{*}$, instead, which would then result in a different but functionally equivalent derivation of the final dc-link current references $i_{\mathrm{dc,CSR,mod}}$ and $i_{\mathrm{dc,CSI,mod}}$.

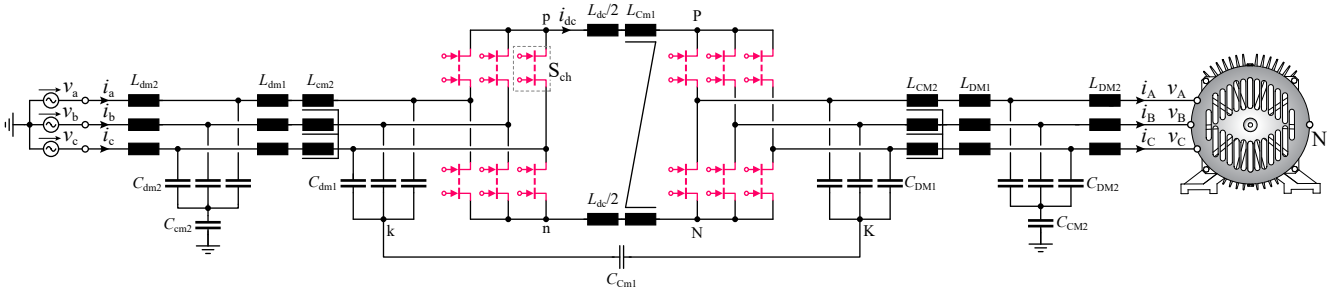

Fig. 9. Power circuit of the realized 200 V (line-to-line rms), 1.4 kW ac-ac CSC demonstrator using first-generation 600 V, 140 mΩ GaN M-BDSs, the corresponding hardware prototype is shown in **Fig. 10**.

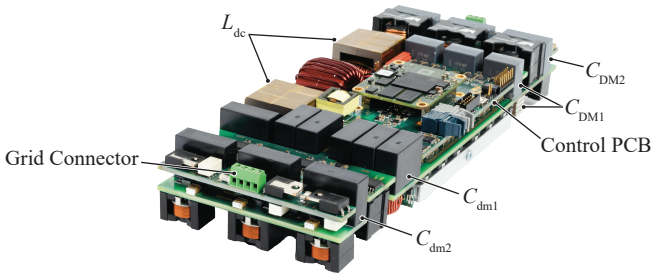

Fig. 10. Top view of the demonstrator prototype for the circuit of **Fig. 9**. The dimensions of 92 mm x 247 mm x 35 mm result in a power density of 1.8 kW/dm^3 (30 W/in^3) including the EMI filters on both, grid and motor side, which are designed for compliance with CISPR 11 Class A for 150 kHz–30 MHz and the upcoming IEC TS 62578 C2 for 9 kHz–150 kHz. **Tab. II** summarizes the key components used.

Note that S_{ch} switches both, positive and negative voltages during the grid period. Additionally, it is interesting to observe that since the dc-link current reference, i^*_{dc}, is determined from the load phase currents, the measured dc-link current, i_{dc}, varies with 6 times the load frequency of $f_m = 110$ Hz. Thus, corresponding to constant power flow, the local average values $v_{pn,avg}$ and $v_{PN,avg}$ of the switched dc-side voltages of the CSR and the CSI vary with 6 f_M, too, but show an inverted shape such that the $i_{dc,avg} \cdot v_{pn,avg} = i_{dc,avg} \cdot v_{PN,avg} = P = const.$

2) Transition Mode (Nominal Operating Point): At the nominal operating point ($V_{g,n} = 200$ V, $V_{m,n} = 200$ V and $P_n = 1.4$ kW, see **Fig. 2**), operation with different grid and load frequencies results in the instantaneous value of i^*_{dc} being alternatingly defined by the CSR or the CSI, which is clearly visible in particular in the local average waveforms $i_{dc,avg}$, $v_{pn,avg}$, and $v_{PN,avg}$ in **Fig. 11b**. Thus, the system operates in the transition mode, and at any point in time, one of the two stages employs 2/3-PWM while the other stage uses 3/3-PWM. This is clearly visible from the switched dc-side voltages v_{pn} and v_{PN}, which show mutually exclusive intervals during which the zero level (corresponding to the zero vector) is continuously avoided.

3) Boost Mode: In boost mode, the roles of the CSR and the CSI reverse compared to buck mode, i.e., the CSR operates with 2/3-PWM while the CSI uses 3/3-PWM. The dc-link current reference i^*_{dc} is now defined by the grid currents and therefore the local average value $i_{dc,avg}$ follows the grid phase currents and, like $v_{pn,avg}$ and $v_{PN,avg}$, shows a fluctuation at $6f_g$. The CSR's dc-side voltage v_{pn} now switches between line-to-line voltages while the CSI's dc-side voltage v_{PN} also attains zero. This is further confirmed by the measured voltage across the M-BDS S_{ch} (high-side commutation cell, phase c) of the CSR, $v_{S,ch}$: $v_{S,ch}$ is only HF-switching during half of the entire grid period (actively taking part in commutations for only one-third of the grid period where $v_{S,ch}$ switches between zero and a line-to-line voltage and passively for one-sixth of the grid period where $v_{S,ch}$ switches between two line-to-line voltages, the voltage across it is changed passively due to the commutations between the commutation cell's other two M-BDSs). For the remaining time period, S_{ch} is clamped either in the on-state ($v_{S,ch} = 0$ V) or in the off-state, where one of the other two M-BDSs of the commutation cell is clamped to on-state; in particular in the regions that correspond to the highest switched voltages with 3/3-PWM as seen from $v_{S,ch}$ during buck operation of **Fig. 11.a.i** where $v_{S,ch}$ HF-switches throughout the entire grid period (actively taking part in the commutations for two third of the period and passively for the remaining one third of the time).

4) Mode Transitions: The proposed synergetic control of the ac-ac CSC is also verified experimentally with varying output voltages V_m as shown in **Fig. 12**. Since the measurements were performed with a fixed resistive load of 50 Ω, increasing the output current reference from 1 A to 3 A also leads to a proportional increase of V_m. As can be seen in **Fig. 12**, the proposed control structure ensures a seamless transition from buck to boost mode while ensuring that at any point in time either the CSI or the CSR operate with 2/3-PWM.

B. Efficiency Measurement

To quantify the efficiency improvement achieved with synergetic operation compared to conventional operation of the ac-ac CSC throughout the operating area from **Fig. 2**, the efficiency of the hardware demonstrator supplying a resistive load from a mains with $V_{g,n} = 200$ V has been measured with a power analyzer (Yokogawa WT1800) and **Fig. 13** summarizes the results. Specifically, **Fig. 13a,d** show the efficiency $\eta_{ac-ac,conv}$ and the overall losses $P_{loss,ac-ac,conv}$ for conventional operation, and **Fig. 13b,e** likewise show $\eta_{ac-ac,syn}$ and $P_{loss,ac-ac,syn}$ for loss-optimal operation with synergetic control. The color inside of the indicated circles represent measured values whereas the colored contour surfaces in

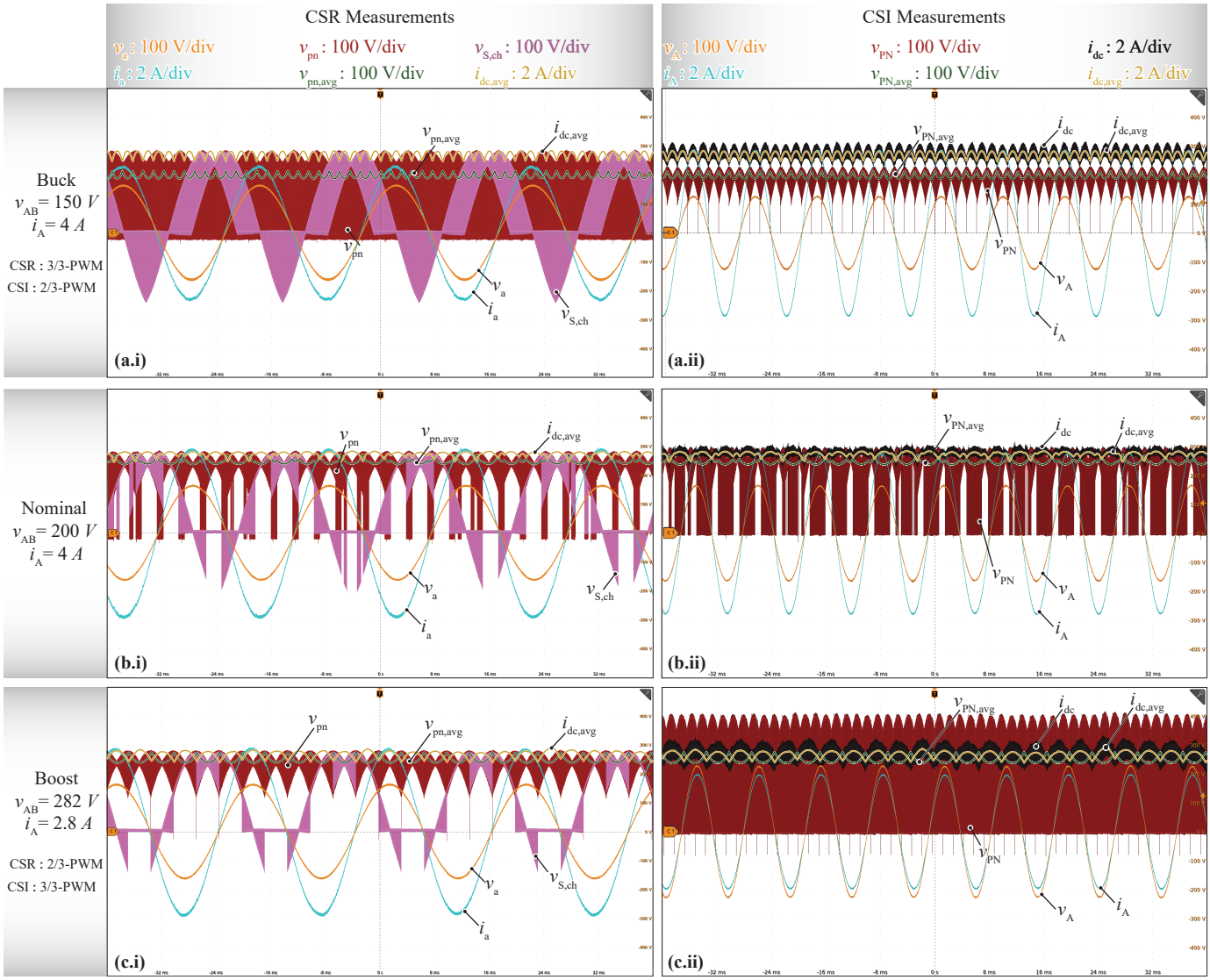

Fig. 11. Measured key waveforms of the ac-ac CSC demonstrator from **Fig. 10** operating with the proposed synergetic control, $V_{g,n}$ = 200 V, f_g = 50 Hz, f_m = 110 Hz, three different output voltages V_m and resistive load; **(a.i), (b.i), (c.i)** CSR and **(a.ii), (b.ii), (c.ii)** CSI. For both stages, one phase voltage, one phase current, and the switched dc-side voltage are shown. Further, $v_{S,ch}$ is the voltage measured across the M-BDS of phase c in the CSR's high-side commutation cell, and i_{dc} is the measured dc-link current. The local average values of the switched dc-side voltages of the CSR and the CSI, $v_{pn,avg}$ and $v_{PN,avg}$, as well as of the dc-link current, $i_{dc,avg}$, have been calculated from the measured data and superimposed on the oscilloscope screenshots. **(a)** In buck mode, i_{dc} is defined by the CSI, which thus operates with 2/3-PWM (v_{PN} does not attain zero) while the CSR operates with 3/3-PWM (v_{PN} does attain zero), whereas in **(c)** boost mode, the roles of the stages are swapped (note here, too, how $v_{S,ch}$ remains zero for certain intervals, which corresponds to clamping of S_{ch}); **(b)** transition mode, the dc-link reference is alternatingly defined by the CSR or the CSI, such that both stages alternatingly operate with 2/3-PWM and with 3/3-PWM.

the background are calculation results.[10] The similarity of the colors inside of the circles compared to the surrounding background thus indicates a generally excellent matching between calculation and measurements across the entire operating range for both, conventional and synergetic control. Finally, based on the calculated results, **Fig. 13c** shows the percentage-point gain in overall system efficiency, $\Delta\eta_{ac-ac} = \eta_{ac-ac,syn} - \eta_{ac-ac,conv}$, and **Fig. 13f** shows the relative change in losses, $\Delta p_{loss,ac-ac} = \left(P_{loss,ac-ac,syn} - P_{loss,ac-ac,conv}\right) / P_{loss,ac-ac,conv}$. An improvement in efficiency of 0.3% at part load operating point and over 1% at part load operation is measured. This corresponds to a reduction of the overall losses by around 10% at the nominal operating point. Note that the loss reduction / efficiency improvement achieved with the proposed synergetic control would be higher for designs with M-BDSs of lower $R_{ds,on}$ (and hence larger chip area and higher switching losses), and/or higher switching frequency.

Further, **Fig. 14a** shows the measured efficiency curves of the ac-ac CSC operating with synergetic control and conventional control for a fixed nominal load voltage $V_{m,n}$ = 200 V while varying the output current and hence, output power. **Fig. 14b** shows the efficiency curves for varying output voltage while limiting the output current according to the maximum power limit, i.e., the thick black boundary line in **Fig. 13**). Again,

[10]The transistor losses are obtained as discussed in **Section II**, the losses of magnetic components are calculated according to [55] and the auxiliary losses, accounting for the power requirements of the gate drives, controller, measurement circuitry and cooling fan are estimated based on similar systems.

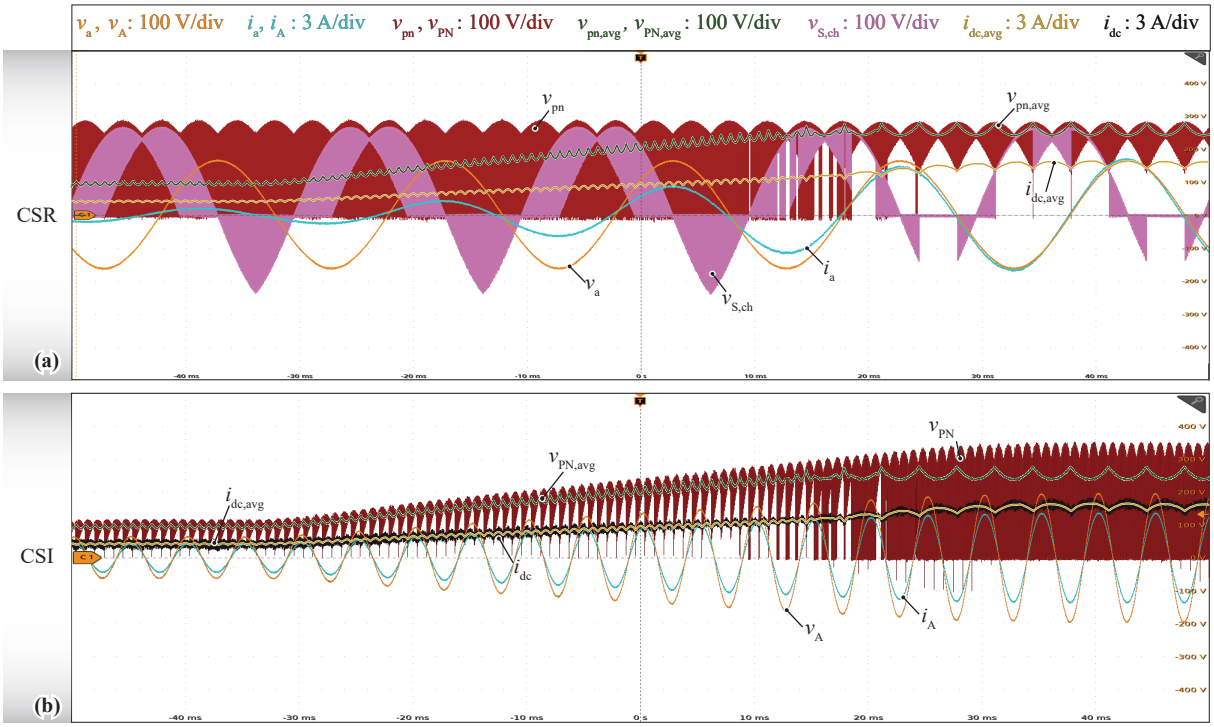

Fig. 12. Measured key waveforms of the ac-ac CSC demonstrator from **Fig. 10** operating with the proposed synergetic control with $f_g = 50\,\text{Hz}$ and $f_m = 200\,\text{Hz}$. The CSC operates with an input voltage of $V_{g,n} = 200\,\text{V}$ and supplies a three-phase resistive load of $50\,\Omega$, whereby the load current reference is gradually increased from 1 A corresponding to $V_m = 85\,\text{V}$ (buck mode; the CSR operates with 3/3-PWM and the CSI with 2/3-PWM) to 3 A corresponding to $V_m = 260\,\text{V}$ (boost mode; the CSR operates with 2/3-PWM and the CSI with 3/3-PWM). Clearly, a seamless transition is achieved, and at any point in time, either the CSR or the CSI operates with 2/3-PWM, which is highlighted by the absence of zero states in the respective dc-side switched voltages v_{pn} or v_{PN}. Note further the change in frequency of the local average values $v_{pn,avg}$, $v_{PN,avg}$ and $i_{dc,avg}$ from $6f_m = 1200\,\text{Hz}$ in buck mode to $6f_g = 300\,\text{Hz}$ in boost mode.

clear efficiency improvements are observed.

Finally, **Fig. 15a,c** show the calculated loss breakdowns of the ac-ac CSC, as well as measured losses for operation with conventional control and **Fig. 15b,d** shows the same for synergetic control; again once for a fixed nominal load voltage $V_{m,n} = 200\,\text{V}$ and varying output power, and once with varying output voltage while limiting the output current according to the maximum power limit, i.e., the thick black boundary line in **Fig. 13**). Again, a very good match between calculated and measured system losses is confirmed. **Fig. 15** further indicates that semiconductor losses account for the largest share of the total system losses. Within the semiconductor losses, the dominating contributor are the conduction loss P_{cond} since the available first-generation M-BDSs used for the realization of the ac-ac CSC demonstrator have a comparably high on-state resistance of $R_{ds,on} = 140\,\text{m}\Omega$. Note that because P_{cond} increases with the square of i_{dc}, the peak efficiency in **Fig. 14a** is achieved at relatively lower power. On the other hand, P_{cond} does not change when varying the output voltage while keeping the maximum possible output power as in **Fig. 15c,d**. Since synergetic operation ensures 2/3-PWM of one of the two stages for all operating points, the switching losses P_{sw} in **Fig. 15b,d** (synergetic control) are clearly lower compared to **Fig. 15a,c** (conventional control).

V. Conclusion

For variable speed drives (VSDs), ac-ac current-source converters (CSCs) are an interesting alternative to ubiquitously employed ac-ac voltage-source converters (VSCs), because CSCs inherently provide smooth sinusoidal motor voltages with a single magnetic component, i.e., the dc-link inductor that connects the grid-side current-source rectifier (CSR) and the motor-side current-source inverter (CSI).

To maximize the ac-ac conversion efficiency, this paper first describes loss-optimal operation over the full output voltage range: for any operating point, the minimum necessary dc-link current is used, which is defined by the maximum absolute value of any of the six phase currents (three on the grid side, three on the motor side). Therefore, using a corresponding time-varying dc-link current, conduction losses of the transistors and also of the dc-link inductor are minimized. Further, if the dc-link current is defined by the CSI (motor currents higher than the grid currents; buck mode), advantageously one of the CSI's phase currents directly corresponds to the dc-link current. That phase is thus permanently connected to the dc-link inductor (clamped) and only two out of three phase currents are synthesized using pulse-width modulation (PWM), i.e., 2/3-PWM of the CSI is achieved, which minimizes the switching losses. As the dc-link current is always higher than the CSR stage's phase currents, the CSR stage, on the other hand, must use PWM for forming all three phase currents (3/3-PWM), and it can thus be used to shape the dc-link current as needed for 2/3-PWM operation of the CSI stage. Conversely, if the dc-link current is defined by the CSR (motor currents lower than the grid currents; boost mode), the roles of the two stages are exchanged. To quantify the loss reduction compared to

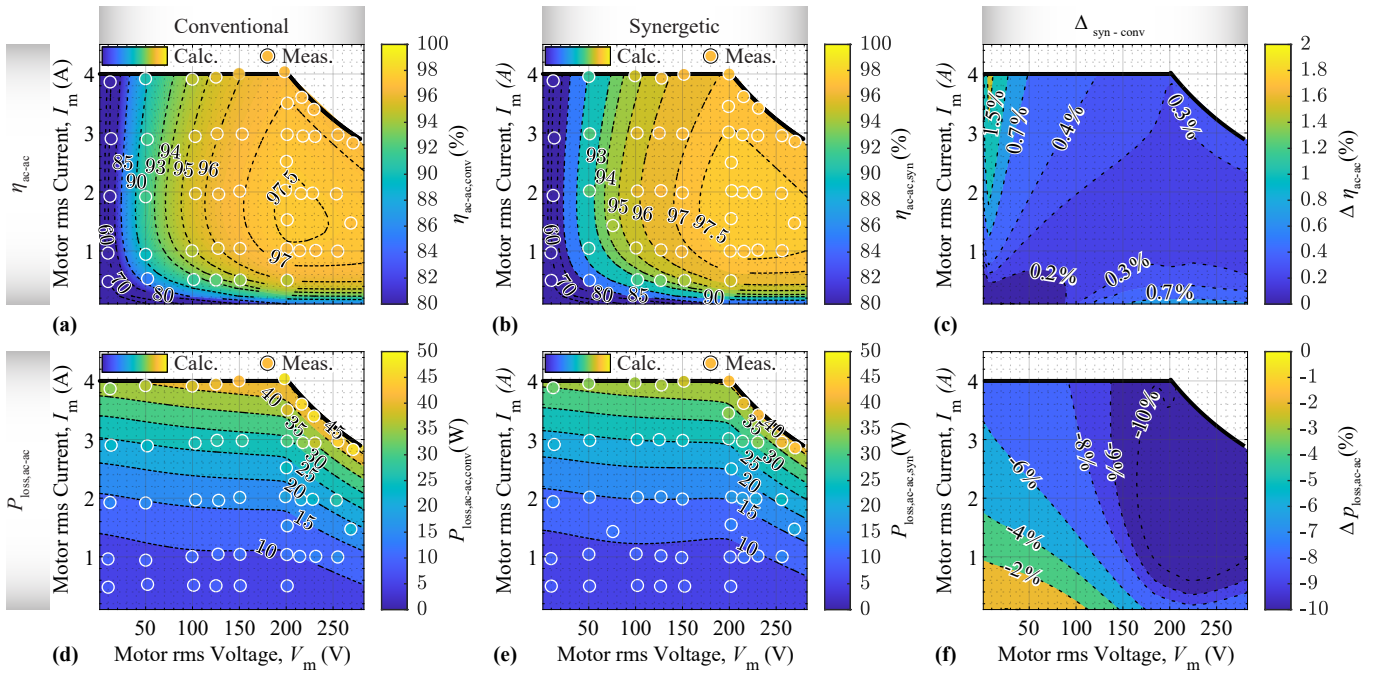

Fig. 13. Comparison of calculated and experimentally measured (Yokogawa WT1800) ac-ac system efficiency and losses of the CSC demonstrator from **Fig. 10** operating from a mains with $V_{g,n}$ = 200 V with resistive load and with **(a), (d)** conventional control (i.e. with adaptive constant i_{dc}), or **(b), (e)** the proposed synergetic control. The contours and the colored background represent calculated values and the colors inside of the white circles indicate measured values. The similarity of the colors within the white circles and the surrounding background indicate a close matching of calculations and measurements throughout the operating range. Therefore, calculated values are used to obtain **(c)** the percentage-point improvement of the ac-ac efficiency and **(f)** the relative reduction of the system losses achieved with synergetic control.

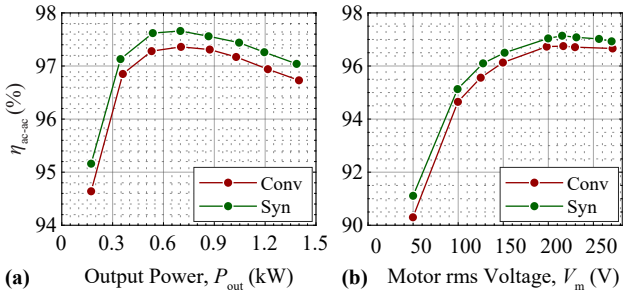

Fig. 14. Measured efficiency curves (Yokogawa WT1800) of the ac-ac CSC demonstrator from **Fig. 10** supplying a resistive load from a mains with $V_{g,n}$ = 200 V, using conventional control with adative constant i_{dc} and synergetic control for **(a)** varying output power at nominal load voltage $V_{m,n}$ = 200 V and **(b)** for varying load voltage V_m with maximum possible output power (depending on the output voltage, see the thick black envelope of operating area in **Fig. 13**). The measurements clearly demonstrate the improvement in efficiency achieved with synergetic control.

conventional operation with constant dc-link current, closed-form expression for conduction (−9%) and switching losses (−76% at the nominal operating point for the stage operating with 2/3-PWM; this depends on the employed power transistors) are provided.

The proposed synergetic control method then ensures operation of the ac-ac CSC in the described loss-optimal way for all operating points, i.e., with minimum possible dc-link current and either the CSR or the CSI stage operating with 2/3-PWM, and realizes smooth transitions between buck and boost mode (smooth exchange of 2/3-PWM and 3/3-PWM among the CSR and the CSI).

The paper then presents a comprehensive experimental verification using a 1.4 kW, 200 V ac-ac CSC demonstrator that employs first-generation 600 V, 140 mΩ monolithic bidirectional GaN transistors, a switching frequency of 72 kHz, and full grid-side and motor-side EMI filters. Measured key waveforms for different operating points as well as for the smooth transition between operating points validate the proposed synergetic control concept. Further, detailed efficiency measurements over the full output voltage and current range show efficiency increases of a least 0.3% and up to 1% for partial load regions, closely matching calculation results. Note that the efficiency improvement depends on the selected transistors and the switching frequencies; higher improvements would be realized with transistors of larger chip area (lower on-state resistance) and/or if higher switching frequencies were employed.

All in all, the proposed synergetic control of ac-ac CSCs facilitates a clear reduction of conversion losses by adapting the control strategy only, as has been detailed and comprehensively verified herein.

Acknowledgement

The authors would like to thank the *Else & Friedrich Hugel Fonds* for generously supporting this research on current dc-link ac-ac converters at the Power Electronic Systems Laboratory at ETH Zurich. The authors would also like to thank Kennith Kin Leong and Infineon Technologies AG, Villach, Austria for providing the first-generation 600 V, 140 mΩ monolithic bidirectional GaN transistor samples for this work.

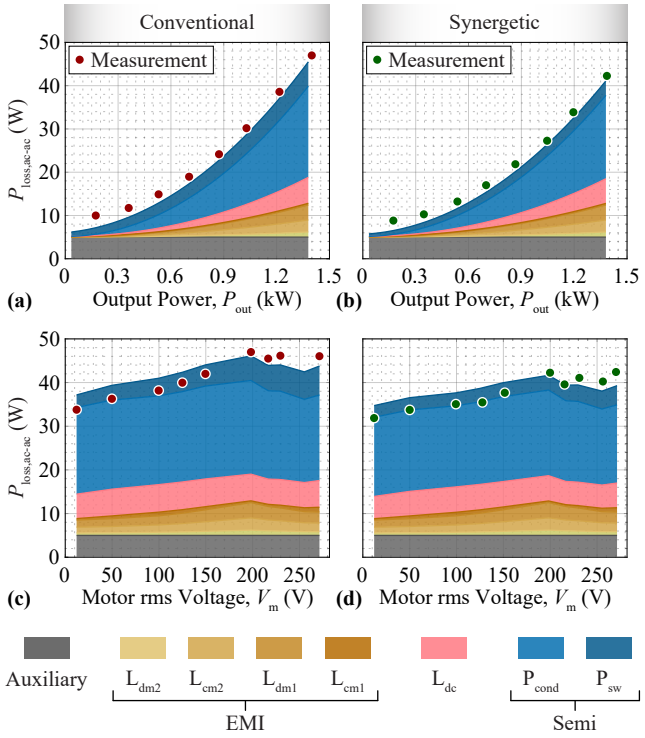

Fig. 15. Measured losses (Yokogawa WT1800) and calculated loss breakdowns of the ac-ac CSC demonstrator from **Fig. 10** supplying a resistive load from a mains with $V_{g,n} = 200\,\mathrm{V}$. **(a), (c)** Conventional control (see (5)) and **(b), (d)** proposed synergetic control (see (8)); as in **Fig. 14**, **(a), (b)** consider nominal motor voltage $V_{m,n}$ and varying output power, and **(c), (d)** consider varying V_m and respective maximum power (see thick black boundary line in **Fig. 13**). The results indicate very good matching between calculated and measured total system losses and highlight the reduction of the overall losses, and in particular of the switching losses achieved with synergetic control.

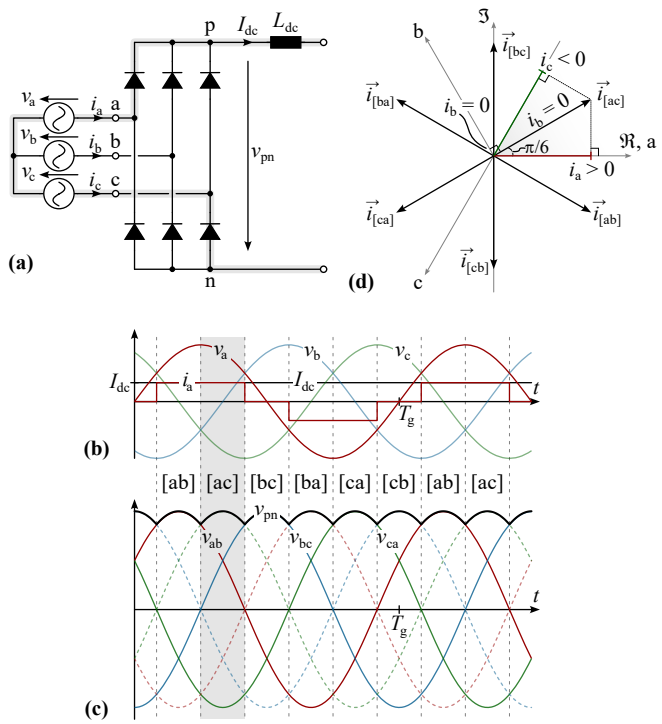

Fig. 16. Diode rectifier with impressed dc-side current I_{dc}. **(a)** Power circuit and key waveforms of **(b)** the three phase voltages and exemplary block-shaped phase current i_a, and of **(c)** the line-to-line voltages and the dc-side voltage v_{pn}. **(d)** Space vector (SV) representation with switching state [ac] highlighted; note that in each switching state, only two of the three phases conduct current.

Appendix A
Basic Operating Principles of Current-Source Converters

This appendix provides a brief introduction to the basic operating principle of a CSC. To do so, it is useful to first consider the diode rectifier from **Fig. 16**, where a constant dc-side current I_{dc} is assumed. The instantaneous values of the mains voltages directly define the switching state of the rectifier bridge, which connects the phase with the maximum voltage to node p and the phase with the minimum voltage to node n. The third phase is not connected to the dc side. Therefore, I_{dc} always flows in two of the three phases only, leading to the block-shaped phase currents with zero intervals shown in **Fig. 16b**, i.e., the rectifier bridge transforms the dc-side current into ac-side currents. Similarly, a transformation of the ac-side voltages to a dc-side voltage v_{pn} occurs: specifically, v_{pn} follows the envelope of the absolute values of the line-to-line voltages, i.e., $v_{pn} = \max\{|v_{ab}|, |v_{bc}|, |v_{ca}|\}$ and thus shows the characteristic six-pulse shape visible in **Fig. 16c**.

Each switching state of the rectifier bridge can be represented as a *current* space vector (SV) in the complex plane as shown in **Fig. 16d**. The switching state is denoted by [xy], where x denotes the phase connected to the dc-side terminal p and y denotes the phase connected to the dc-side terminal n. The orientation of the six SVs must be such that each is perpendicular to one of the three phase axes a, b, and c, such that each SV's projection to the phase axes leads to one phase current being positive, one being negative, and one being zero, as discussed above, e.g., SV [ac] is perpendicular to phase b and hence leads to zero current in phase b and a positive and negative current in phase a and c respectively. Consequently, to satisfy, e.g., $|i_a| = I_{dc}$ in the non-zero current intervals, the length of the current SVs is $|i_{[xy]}| = 1/\cos(\pi/6) I_{dc} = 2/\sqrt{3} \cdot I_{dc}$.

By replacing the rectifier diodes with switching elements featuring bipolar voltage blocking capability (e.g., a series connection of a diode and an IGBT, which supports unidirectional current conduction), the current-source rectifier (CSR) from **Fig. 17a** results. Advantageously, the turn-off capability of the switching elements enables a free selection of which phase terminals are connected to p and n, respectively, in the upper and lower commutation cell. **Fig. 17b** illustrates this basic functionality of the CSR switching stage by replacing each commutation cell with a three-pole switch.

Hence, PWM modulation can be employed to synthesize a certain local average value of the phase currents, e.g., $\langle i_a \rangle \propto v_a$ for PFC operation as shown in **Fig. 17c**.[11] Please refer to the main text, specifically to **Section II**, for a detailed description of SV PWM (dwell time calculations, switching sequences, etc.), as the discussion here is not specific to any variant.

Clearly, the maximum phase current amplitude is limited by the dc-link current, e.g., $\langle \hat{i}_a \rangle \leq I_{dc}$. More generally, for the

[11] Note that here we explicitly indicate local average values of switched quantities with $\langle \cdot \rangle$, whereas this is not done in the main text to improve legibility.

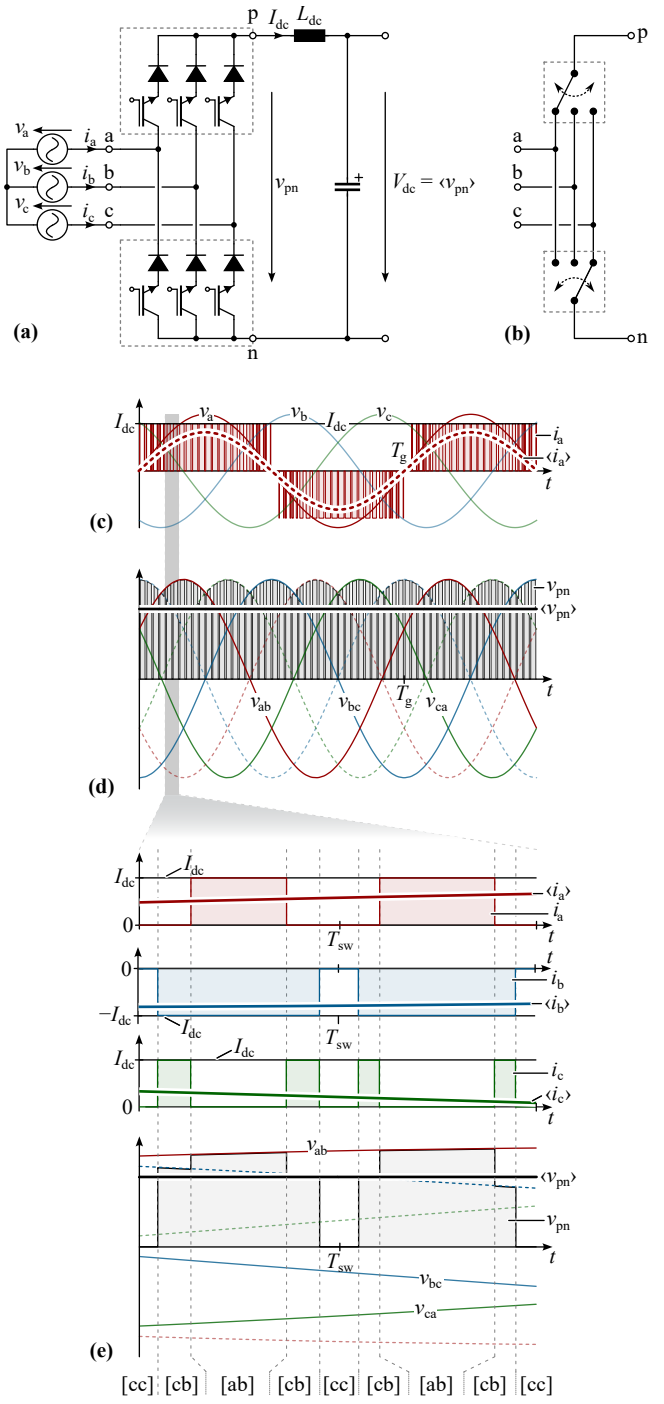

Fig. 17. Current-source rectifier and exemplary key waveforms assuming constant dc-link current I_{dc}. **(a)** Power circuit and **(b)** conceptual representation of the switching stage where each of the two commutation cells is replaced by a three-pole switch. **(c)** phase voltages and pulse-width-modulated phase current i_a with sinusoidal local average value $\langle i_a \rangle \propto v_a$, and **(d)** line-to-line voltages and dc-side switched voltage v_{pn} with constant local average value $\langle v_{pn} \rangle$. A low ratio of switching to fundamental frequency is used for visualization purposes. **(e)** Zoomed view of two switching periods: according to the indicated PWM switching sequence, I_{dc} flows either in two phases or freewheels, and the levels of v_{pn} correspond to the absolute values of the line-to-line voltages or zero (freewheeling).

modulation index m_g (see (1)) we have

$$m_g = \frac{\langle \hat{i}_g \rangle}{I_{dc}} \leq 1. \tag{21}$$

In a CSR, PWM of the switching stage translates the dc-side current into sinusoidal (local average) three-phase currents. At the same time, and as shown in **Fig. 17d**, the PWM of the switching stage synthesizes the dc-side voltage v_{pn} from the line-to-line voltages (active switching states, as in the diode rectifier) and zero voltage (freewheeling state). Unlike in the case of the diode rectifier, the controllable switches of the CSR allow to connect the nodes p and n directly, e.g., by turning on both switches associated with one phase, e.g. phase a for the switching state [aa], resulting in $v_{pn} = 0$. For active switching states, v_{pn} equals the respective line-to-line voltage, e.g., $v_{pn} = v_{ab}$ for the switching state [ab] as shown in **Fig. 17e**.

From the power balance on the ac-side and the dc-side, we have $\hat{i}_g \hat{v}_g \cdot 3/2 = I_{dc} v_{pn}$, which leads to $\langle v_{pn} \rangle = \sqrt{3/2} m_g V_g$ and an alternative expression for the modulation index

$$m_g = \sqrt{\frac{2}{3}} \frac{\langle v_{pn} \rangle}{V_g}, \tag{22}$$

where $\hat{v}_g$ is the mains phase-to-neutral peak voltage and V_g the mains line-to-line rms voltage. This highlights again how the switching stage performs both, a current and a voltage transformation. Note further that the maximum local average value of the dc-side voltage is thus limited to $\langle v_{pn} \rangle \leq \sqrt{3/2} V_g$. Finally, as constant dc-side output power $P = I_{dc} \langle v_{pn} \rangle$ implies $\langle v_{pn} \rangle = const.$, the output power is limited by the dc-link current to $P \leq \sqrt{3/2} V_g I_{dc}$ (for unity power factor operation).

Considering then finally the back-to-back configuration of a CSR and a CSI stage to realize ac-ac conversion as shown in **Fig. 18**, the average voltage across the shared dc-link inductor L_{dc} must be zero in steady state. Hence the local average values of the two dc-side voltages must be equal, i.e.,

$$\sqrt{\frac{3}{2}} m_g V_g = \langle v_{pn} \rangle = \langle v_{PN} \rangle = \sqrt{\frac{3}{2}} m_m V_m, \tag{23}$$

where V_m denotes the output-side (motor-side) line-to-line rms voltage and m_g the CSI stage modulation index. This simplifies to

$$V_m = \frac{m_g}{m_m} V_g, \tag{24}$$

which directly highlights the buck-boost capability of the ac-ac CSC system: appropriate selection of $m_g \in [0, 1]$ and $m_m \in [0, 1]$ enables both, $V_m \leq V_g$ and $V_m \geq V_g$.

Further, as there are no low-frequency energy storage elements, the (local average) power flow through the two ac-side and the two dc-side interfaces must be equal as indicated in **Fig. 18**. As we have $P \leq \sqrt{3/2} V_g I_{dc}$ on the grid side as discussed above, a corresponding power limit results for the motor side, too: For maximum grid-side power with $m_g = 1$, increasing $V_m > V_g$ implies reducing $m_m < 1$ and hence a reduction of the motor current, such that the power balance is maintained. Specifically, some derivations lead to

$$\langle \hat{i}_m \rangle \leq I_{dc} \cdot \min\left(1, \frac{V_g}{V_m}\right), \tag{25}$$

which describes the boundary for the maximum motor current in dependence of the motor voltage shown in **Fig. 2**.

The switching elements shown in **Fig. 18** i.e., a series connection of a diode and an IGBT, are capable of blocking

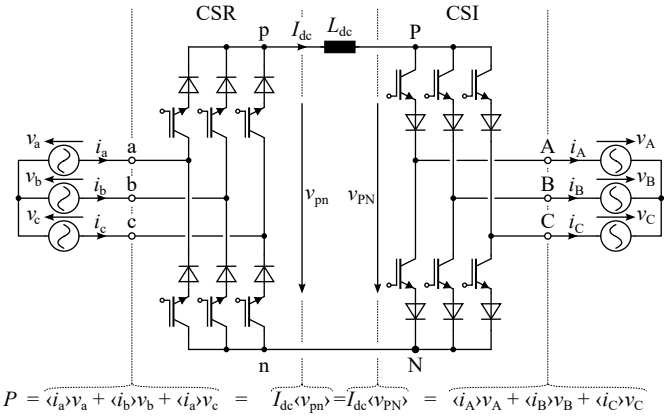

Fig. 18. AC-AC current-source converter, i.e., a back-to-back arrangement of a CSR and CSI with shared dc-link inductor L_{dc} and hence equal dc-link current I_{dc}. As there are no low-frequency energy storage elements, the (local average) power flow P through the two ac-side and two dc-side interfaces is equal and constant (assuming symmetric three-phase conditions).

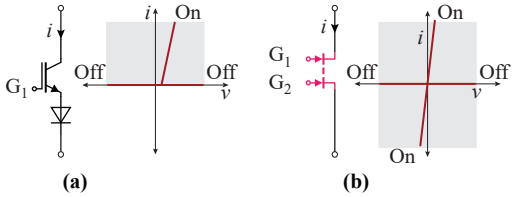

Fig. 19. Switch configurations for CSCs and their corresponding v-i characteristics for **(a)** a series connection of a IGBT and a diode (note that the IGBT can be replaced by another controllable switch), and **(b)** an M-BDS.

bipolar voltages but can only conduct current in one direction, as indicated by the corresponding v-i characteristic from **Fig. 19a**. As a result, the reversal of the power flow direction is possible only by reversing the polarity of the dc-side voltages $\langle v_{pn} \rangle$ and $\langle v_{PN} \rangle$ while the dc-link current direction must remain unchanged. If, instead, the switching elements are realized with monolithic bidirectional (M-BDS) GaN transistors (as is shown in **Fig. 1**), which are also capable of blocking bipolar voltages but can conduct current in both directions as shown by the v-i characteristics in **Fig. 19b**, the power flow reversal can be achieved again by changing the polarity of the dc-side voltages, or, alternatively, by reversing the dc-link current direction. This, however, shows slower dynamics (due to the dc-link inductance) compared to reversal of the dc-side voltage polarity.

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