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Analysis and Multi-Objective Evaluation of New Three-Phase PWM Inverter System

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MICHAIL MARIOS ANTIVACHIS

MSc ETH
born on 19.08.1991
citizen of Greece

accepted on the recommendation of

Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Hans-Peter Nee, co-examiner

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ETH Zurich
Power Electronic Systems Laboratory
Physikstrasse 3 | ETL H23
8092 Zurich | Switzerland

http://www.pes.ee.ethz.ch

To my Parents
Nikolaos and Kalliopi

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Michael Antivachis

Abstract

CURRENTLY the transportation sector accounts for a quarter of global CO_2 emissions. In order to decarbonize the transportation, a transition from internal combustion engine vehicles (ICV) to fully electric vehicles (EV) is necessary. Motor drive systems are a key component of EVs, thus innovation in power electronics and motor technology will partly determine the adoption rate of EVs.

This thesis focuses on the energy storage system of a fuel-cell electric vehicle (FCEV). In particular, each fuel-cell unit requires a continuous supply of oxygen, which is provided by means of an auxiliary, electric compressor. A compressor drive system, supplied by the fuel-cell or a battery controls the electric compressor. The examined compressor drive is placed onboard a FCEV, thus is expected to be compact and lightweight. It is well documented in literature, that high-speed motors/compressors benefit from a small volume, thus are ideal for power dense drive systems. However, until now there is no comprehensive analysis of inverter systems tailored to the special characteristics of high-speed motors. This thesis aims to bridge this technical gap, by exploring the performance limits of high-speed motor drives.

In the first part of the thesis, a conventional voltage source inverter (VSI) is paired with a high-speed motor. High-speed motors are sensitive to poor stator current quality, that induces high rotor losses. For this reason, an output filter must be added at the inverter AC output-side. Different types of output filter are discussed here, concluding that a full sine-wave output filter (FSF) fits best the needs of high-speed motor drives. An FSF adds volume/losses, thus negatively affects the inverter stage performance. Two new modulation strategies that take into account the special properties of an FSF, and reduce the inverter losses, are proposed in **Chapter 2**.

A high switching frequency is used for the VSI pulse width modulation (PWM), in order to guarantee a dynamic control of the high-speed motor. This requirement for high switching frequency is achieved by employing the latest generation of wide-bandgap (WBG) semiconductor devices. However, the combination of a high switching frequency and WBG devices, causes electromagnetic interference (EMI) concerns. The electromagnetic compatibility (EMC) of high-speed motor drives is analysed in **Chapter 3**. The motor drive is part of a larger system, thus should not cause EMI noise that disrupts nearby electronic equipment. In order to mitigate the EMI emissions, a filter is placed at the inverter DC input-side, in addition to the output FSF. Several EMI aspects are discussed here, culminating in a new filter design algorithm, that takes into account interrelations between the input and output filters.

In the second part of the thesis, buck-boost inverter topologies are investigated. High-speed motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance requirement, the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery. Several buck-boost inverter concepts are evaluated by means of multi-objective optimization tools. Hardware prototypes are built for the most promising inverter topologies, and are compared to state-of-the-art solutions, with respect to the achievable efficiency and power density. In **Chapter 4**, a conventional buck-boost inverter topology is examined, which features two energy conversion stages. As a result of the two energy conversion stages, this inverter topology suffers from a low efficiency and a relatively low power density. A new modulation strategy that synergetically combines the operation of the two inverter stages, and hence improves the inverter efficiency, is proposed. Subsequently, in **Chapter 5**, innovation in the inverter topology is pursued. A new buck-boost inverter topology is presented, based on the idea of modular three-phase systems. This inverter topology achieves buck-boost capability by using only a single energy conversion stage, and thus achieves a high performance. Finally, in an effort to improve the motor drive as a whole, inverter innovation is combined with motor innovation, in **Chapter 6**. As a result, the double-bridge inverter technology is proposed, where two VSIs are connected to the opposite sides of an open-end winding motor (no floating neutral point).

Chapter 7 briefly summarizes the key findings of this thesis and gives an outlook on future research.

Kurzfassung

DERZEIT verursacht der Transportsektor rund ein Viertel der weltweiten CO_2-Emissionen. Um diesen Anteil zu reduzieren ist ein Übergang von Fahrzeugen mit konventionellen Verbrennungsmotoren (ICV) zu Fahrzeugen mit komplett elektrischen Antrieben (EV) unerlässlich. Um diesen Übergang voranzutreiben und für den Endverbraucher attraktiver zu gestalten, sind insbesondere im Bereich der Leistungselektronik und der Motorentechnik grundlegende Innovationen erforderlich.

Die vorliegende Dissertation fokussiert auf Brennstoffzellen-Elektrofahrzeuge (FCEV), in welchen die Brennstoffzelleneinheit eine kontinuierliche Sauerstoffversorgung benötigt. Die Sauerstoffzufuhr wird mit Hilfe eines elektrischen Kompressors sichergestellt, welcher von einer leistungselektronischen Schaltung gespeist wird. Diese Schaltung bzw. das Antriebssystem bildet den zentralen Gegenstand der Arbeit und wird hinsichtlich Anforderungen und Betriebsverhalten im Detail untersucht. Da das Antriebssystem im Fahrzeug untergebracht werden muss, ist ein geringes Gewicht, sowie ein hohes Mass an Kompaktheit unerlässlich. Da Hochgeschwindigkeits-Motoren/Kompressoren hohe Kompaktheit aufweisen, sind sie für die gegenständliche Anwendung vorteilhaft einsetzbar, allerdings liegt in der Literatur bisher noch keine umfassende Analyse von Antriebssystemen, welche auf die speziellen Eigenschaften von Hochgeschwindigkeitsmotoren zugeschnitten sind, vor. Diese Lücke soll durch diese Arbeit geschlossen werden, indem die Grenzen der Leistungsdichte und Effizienz von Antriebssystemen für Hochgeschwindigkeitsmotoren im Detail untersucht werden.

Im ersten Teil der Arbeit wird ein konventioneller spannungsgespeister Wechselrichter (VSI) verwendet, um einen Hochgeschwindigkeitsmotor anzutreiben. Da oberschwingungsbehaftete Statorströme in Hochgeschwindigkeitsmotoren hohe Rotorverluste verursachen, muss zwingend ein Ausgangsfilter zwischen den Wechselrichter und den Motor geschaltet werden. Es werden unterschiedliche Ausgangsfilter-Schaltungen untersucht, wobei der Schluss gezogen wird, dass ein Voll-Sinus-Ausgangsfilter (FSF) den Anforderungen von Hochgeschwindigkeitsmotoren am besten gerecht wird. Da ein zusätzliches FSF jedoch sowohl die Verluste als auch das Gesamtvolumen des Systems erhöht, werden in **Kapitel 2** zwei neue Modulationsverfahren vorgestellt, welche die speziellen Eigenschaften von FSF berücksichtigen und eine Reduktion der auftretenden Verluste im Wechselrichter erreichen.

Um eine hohe Dynamik der Steuerung des Hochgeschwindigkeitsmotors zu gewährleisten, wird eine hohe Schaltfrequenz der VSI-Pulsweitenmodulation (PWM) verwendet. Um bei hoher Schaltfrequenz hohe Effizienz si-

cherzustellen, wird die neuste Generation von Wide-Bandgap (WBG) Halbleiterbauelementen eingesetzt, deren hohe Schaltgeschwindigkeit potentiell elektromagnetische Störungen (EMI) verursacht welche umliegende Systemkomponenten beeinträchtigen könnten. Entsprechend wird die elektromagnetische Verträglichkeit (EMV) von Hochgeschwindigkeitsantrieben in **Kapitel 3** im Detail untersucht. Um Störungen zufolge EMI sicher zu vermeiden, wird zusätzlich zum ausgangsseitigen FSF ein EMI-Filter am Eingang des Wechselrichters angeordnet. Um eine Grundlage für die Optimierung der gesamten EMI-Filterung zu schaffen, werden die EMI-Störaussendungen im Detail analysiert. Auf Basis dieser Analysen wird ein neuer Filterdesign-Algorithmus entwickelt, welcher auch die Wechselbeziehungen zwischen dem Eingangs- und dem Ausgangsfilter berücksichtigt.

Im zweiten Teil dieser Arbeit werden kombinierte Hoch-/Tiefsetz-Wechselrichter-Topologien untersucht. Da das Antriebssystem, je nach Betriebsmodus, entweder direkt von der Brennstoffzelle oder von einer Batterie gespiesen wird, muss der Wechselrichter nicht nur eine hohe Leistungsanforderung erfüllen, sondern auch einen weiten Eingangsspannungsbereich beherrschen. Dies erschwert das Design, weshalb verschiedene Hoch-/Tiefsetz-Wechselrichter-Topologien mittels Mehr-Ziel-Optimierung verglichen und bewertet werden. Die vielversprechendsten Wechselrichtertopologien werden anschliessend als Hardwareprototypen aufgebaut und hinsichtlich Effizienz und Kompaktheit mit bestehenden Lösungen verglichen. In **Kapitel 4** wird eine konventionelle Hoch-/Tiefsetz-Wechselrichter-Topologie untersucht, welche aus zwei in Serie geschalteten Energieumwandlungsstufen besteht. Aufgrund der zweifachen Energiekonversion weist diese Topologie jedoch eine relativ geringe Effizienz und Leistungsdichte auf. Um die Effizienz zu steigern, wird ein neues Modulationsverfahren vorgestellt, welches den Betrieb der beiden Stufen synergetisch kombiniert. Nachfolgend wird in **Kapitel 5** eine neue Wechselrichtertopologie vorgeschlagen, welche auf der Idee modularer Dreiphasensysteme basiert. Diese Topologie weist eine einstufige Energieumformung auf, wodurch eine deutlich höhere Effizienz der Energieumwandlung resultiert. Desungeachtet kann die neue Wechselrichterschaltung sowohl als Hoch- als auch als Tiefsetzsteller betrieben werden. Im Bestreben den Antrieb als Ganzes zu verbessern, wird abschliessen der Wechselrichter und der Hochgeschwindigkeitsmotor gemeinsam betrachtet, und in **Kapitel 6** eine Doppel-Brücken-Wechselrichtertopologie vorgestellt, in welcher zwei VSI-Schaltungen die gegenüberliegenden Statorwicklungsenden eines Motors mit offenen Wicklungen, d.h. ohne Sternpunkt speisen.

Kapitel 7 fasst die wesentlichen Ergebnisse der Arbeit zusammen und gibt einen Ausblick auf zukünftige Forschungsthemen.

Abbreviations

AC	Alternating Current
ACCMM	AC Common-Mode Modulation
B-VSI	Boost Voltage Source Inverter
BEV	Battery Electric Vehicle
c-FSF	Combined Full Sine-Wave Output Filter
CM	Common-Mode
CMF	Common-Mode Output Filter
CSI	Current Source Inverter
DB-VSI	Double-Bridge Voltage Source Inverter
d-FSF	Discrete Full Sine-Wave Output Filter
DC	Direct Current
DCCMM	DC Common-Mode Modulation
DM	Differential-Mode
DMF	Differential-Mode Output Filter
DPWM	Discontinuous Pulse Width Modulation
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EV	Electric Vehicle
FCEV	Fuel-Cell Vehicle
FSF	Full Sine-Wave Output Filter
GaN	Gallium Nitride
ICV	Internal Combustion Engine Vehicle
IMD	Integrated Motor Drive
IMMD	Integrated Modular Motor Drive
LISN	Line Impedance Stabilization Network
OCMM	Optimal CM modulation
PAM	Pulse Amplitude Modulation
PWM	Pulse Width Modulation
SB-VSI	Single-Bridge Voltage Source Inverter
Si	Silicon
SiC	Silicon Carbide
SM	Sinusoidal Modulation
SPWM	Sinusoidal Pulse Width Modulation
THM	Third Harmonic Injection Modulation
VSI	Voltage Source Inverter
WBG	Wide-Bandgap
Y-VSI	Y Voltage Source Inverter
ZSI	Z Source Inverter

Contents

1 Introduction

Climate change is one of the biggest challenges of the next decades. The transportation sector accounts for 24% of the global CO_2 emissions [1]. Furthermore, the transportation sector emissions are expected to grow at a faster rate than other sectors, posing a major challenge to the efforts to reduce emissions. The decarbonization of transportation requires three key steps as visualized in **Fig. 1.1**. Power electronics constitutes a main enabling technology in all three decarbonization steps.

(i) **Electrification of vehicles.** There are two main types of pure electric vehicles (EV): Fuel-cell electric vehicles (FCEV), which employ a fuel-cell electrochemical system that produces electricity onboard, and battery electric vehicles (BEV), which use a grid-charged battery pack. The main structure of FCEVs and BEVs is similar, since in either case the propulsion is achieved by the combination of a DC/AC inverter and an electric motor. Several power electronics converters are used in EVs. For example, in the case of FCEVs the fuel-cell DC bus supplies a DC/AC inverter, which in return controls an electric motor (powertrain). The fuel-cell requires continuous oxygen supply, which is provided by an onboard electric compressor. An auxiliary DC/AC converter, also supplied by the fuel-cell DC bus, controls this electric compressor [2–4]. FCEVs also include a small battery pack that provides the peak power demand, e.g. during acceleration. A DC/DC converter is needed in order to connect the battery DC bus with the fuel-cell DC bus [5, 6]. It is therefore evident, that power electronics technology is a main enabler of innovation in EVs.

(ii) **Charging infrastructure.** The EVs must be supported by an appropriate refuelling network. That is, hydrogen refuelling retail network

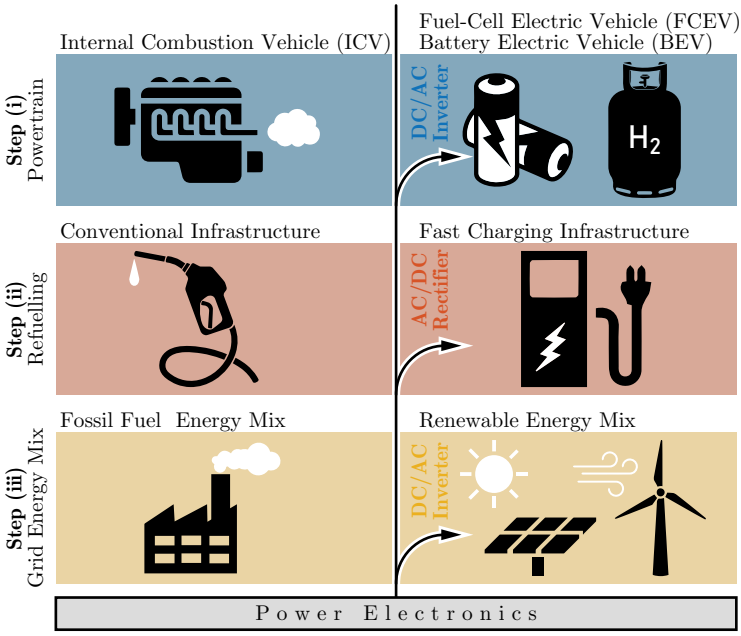


Fig. 1.1: Key steps leading to the decarbonization of the transportation sector. Power electronics is a main enabling technology.

for FCEVs and fast electric chargers for the case of BEVs. In the latter case of fast electric chargers, innovation in power electronics is necessary, in order to increase the power rating of the on-board/off-board chargers and accordingly reduce the charging time of a BEV [7–9].

(iii) **Renewable energy generation.** The EVs emit no CO_2 during use, but still contribute indirectly to carbon emissions. The BEVs rely on electricity, therefore the real emissions of BEVs depend on the energy mix of the grid. Similarly, FCEVs use hydrogen (H_2), whose production requires an energy-intensive process. Therefore, the carbon footprint of FCEVs depends on the power grid energy mix. In order to achieve a true decarbonization of the transportation sector, a renewable generation base [10,11] and a modernization of the power grid [12] is needed. Power electronics technology is a key component of this endeavour. For example, efficient and flexible DC/AC converter systems

are needed, in order to deliver the renewable power from solar panels or wind turbines to the current AC power grid.

This thesis focuses on the energy storage system of a FCEV. In particular, the auxiliary compressor drive, that is responsible for the oxygen supply of the fuel-cell, is investigated. More details regarding the exact application follow in **Sec. 1.3**.

1.1 Challenges

Inverter systems placed onboard EVs are expected to be compact and lightweight. Therefore, the power density ρ is the most important performance objective for inverters, for this application. The pursuit of high power density is assisted by recent developments in the power semiconductor technology. Wide-bandgap (WBG) semiconductor devices (SiC/GaN) allow to increase the inverter switching frequency by a factor of ten, compared to Si counterparts [13–15]. Accordingly, a drastic reduction of the passive components' volume can be achieved without compromising the inverter efficiency. A high inverter efficiency η is also desirable, since it allows for a better utilization of the battery/fuel-cell energy and reduces the size of the thermal management system.

The traditional requirement for high efficiency and power density does not suffice for modern drive systems. Besides a high performance, the inverter is expected to provide additional features:

(i) **High fundamental frequency.** The motor nominal speed (fundamental frequency) is directly related to the motor volume/weight [16–18]. By shifting towards higher rotational speeds the volume of the electric motor and the rotating mechanical components (e.g. compressor) can be drastically reduced and bulky gearboxes can be eliminated. Thereby, significant savings in terms of material cost can be achieved. Besides a challenging motor design, able to withstand the mechanical stress originating from the high rotational speeds [19, 20], the inverter must be able to generate voltages/currents with a fundamental frequency in the range of several kHz.

(ii) **Continuous output voltages.** Typically, slotless permanent magnet motors are used in high-speed applications, which are especially sensitive to poor stator current quality, that causes rotor losses [21–23]. In this case, the thermal management of the rotor is a main concern, due

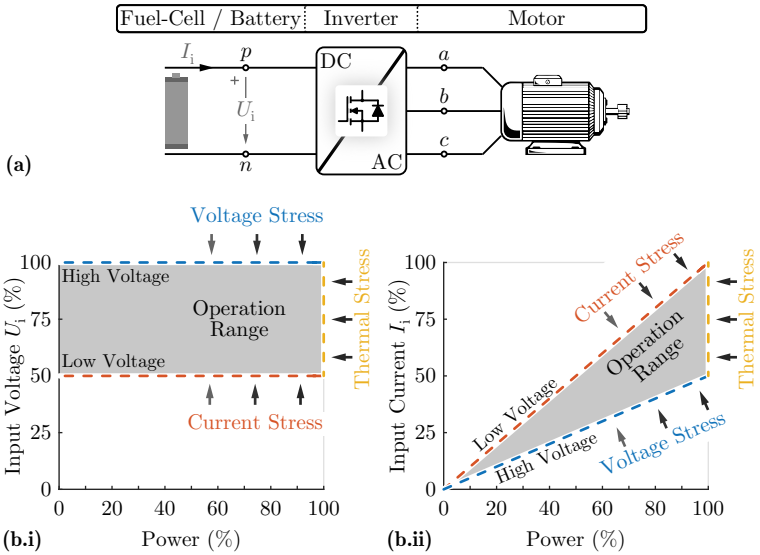


Fig. 1.2: (a) Drive system supplied by fuel-cell/battery, which must feature a wide voltage transfer ratio. **(b)** Voltage characteristics and **(c)** current characteristics of the fuel-cell/battery.

to the small rotor surface. In order to facilitate the motor cooling, the inverter must generate sinusoidal motor currents, that minimize the induced rotor losses.

(iii) **Electromagnetic compatibility.** The latest generation of WBG semiconductors allows for significantly better inverter performance but at the same time causes electromagnetic compatibility (EMC) concerns [24]. The high switching speeds of WBG semiconductor devices cause high du/dt [25–27], which stresses the motor insulation and induces bearing currents [28–33]. As a result, the motor reliability is jeopardised. The inverter must mitigate the du/dt, in order to ensure a safe motor operation [34–40].

An EV features several ancillary electronic systems such as driving aids, active suspension, and various sensors. These electronic systems are directly or indirectly supplied by the same DC bus as the inverter, and are sensitive to electromagnetic interference (EMI). In comparison to Si inverters, which employ a switching frequency in the tens of kHz,

an inverter with WBG semiconductor devices can use a switching frequency in the range of several hundred kHz [14,41]. These high switching frequencies of WBG inverters are within the regulated conducted EMI emissions frequency range of 150 kHz...30 MHz [42]. Therefore, WBG inverters intensify EMI emission problems. The inverter must mitigate the generated EMI noise in order to protect nearby equipment.

(iv) **Buck-boost functionality.** Motor drives supplied by a fuel-cell/battery have to cope with a wide DC input voltage variation, as is visualised in **Fig. 1.2**. In particular, the voltage of the fuel-cell highly depends on the operating point. A fuel-cell exhibits the highest voltage at no-load condition, while the lowest voltage appears at full-load condition [43]. The voltage of a battery also fluctuates, depending on the charging status and the operating temperature. The ratio between the maximum and the minimum voltage, for either battery or fuel-cell, can be as high as two. The inverter has to always guarantee the full speed range of the motor, independent of the DC input voltage fluctuation, i.e. the inverter must be able to generate the nominal motor voltage, which is proportional to the motor speed.

The demand for additional inverter features, often contradicts the requirement for a high efficiency/power density. For example, electromagnetic compatibility mandates the use of EMI filters which add to the inverter volume, while buck-boost functionality leads to over-dimensioning of the inverter components and hence additional losses. The interdependencies between the different inverter features, complicate the design process. It is particularly challenging to achieve a balance among the various inverter features and a high performance.

1.2 Aims and Contributions

The goal of this thesis is to research and apply innovative technical solutions, to fuel-cell powered, high-speed motor drives. Three innovation paths are investigated:

(i) **New modulation strategies.** There is a large number of operational motor drives, which feature conventional Si inverters. In fact, 40% of the worldwide electricity is consumed by motor drives [44, 45]. In this case, it is not desirable to only replace the Si inverter with a new

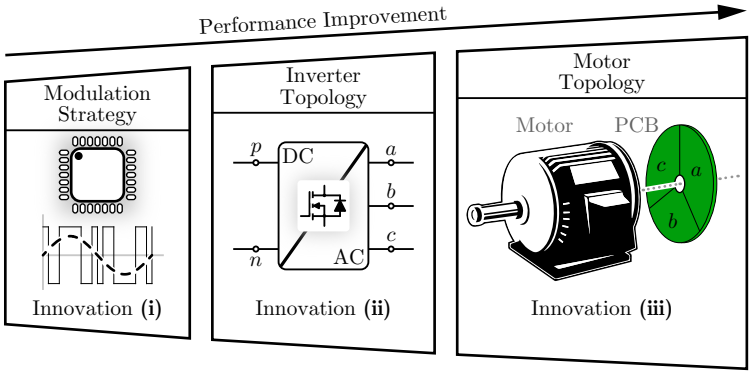


Fig. 1.3: Motor drive innovation roadmap.

WBG counterpart, but also improve the efficiency of the existing system. This goal can be achieved by means of new modulation strategies, which can be uploaded to the inverter, as a simple firmware update. New modulation strategies are proposed in this thesis, that improve the performance of state-of-the-art inverters.

(ii) **New inverter topologies.** The most readily available inverters are Si-based voltage source inverters (VSI). VSIs are well suited for Si devices, and thus utilize this semiconductor technology optimally. However, the performance of such inverter solutions is inherently limited by the inferior properties of Silicon. Recent advances in WBG semiconductor devices, bring in the forefront alternative inverter topologies. Literature shows that conventional VSIs might not be the best suited option for WBG semiconductor devices [45]. For this reason, new inverter topologies are investigated in this thesis.

(iii) **New motor topologies.** In order to achieve the best performance on a system level, it is desirable to coordinate the design of the inverter and the motor. A very efficient inverter could lead to a bulky motor and vice-versa, which is a sub-optimal solution [46]. Therefore, it is important to consider the efficiency and power density of the motor drive system as a whole (i.e. inverter and motor). The integration of the inverter and the motor in the same housing is the natural next step in inverter/motor design [45, 47, 48]. Thereby, the inverter is directly attached on the motor terminals and cumbersome/costly interconnect-

ing cables are eliminated. A common thermal management system can be used for the inverter and the motor, provided that the inverter is able to operate reliably in the high-temperature environment of the motor. An integrated motor drive (IMD) adds value for the end user, because the latter is not any more burdened with the complicated inverter/motor installation.

1.3 Performance Benchmark

This thesis focuses on two high-speed motor drive applications, supplied by a DC source. The specifications are defined according to the needs of the industry partner of this thesis: Celeroton AG.

Application I is presented in **Fig. 1.4** and summarized in **Tab. 1.1**. A $U_\mathrm{i} = 48\,\mathrm{V}$ battery supplies the inverter, which in return controls the high-speed $n = 500\,\mathrm{krpm}$, $P = 70\,\mathrm{W}$ electric compressor of **Fig. 1.5(b)**. The electric compressor houses internally the electric motor of **Fig. 1.5(a)**.

A commercially available inverter system based on Si semiconductor technology already exists for this motor drive application, and employs pulse amplitude modulation (PAM). The existing PAM system is visualized in **Fig. 1.6(a)**. According to PAM modulation, the VSI applies 120^o voltage blocks to the motor, with an amplitude equal to the DC link voltage U_DC. The motor fundamental voltage/current is controlled, by adjusting the DC link voltage U_DC, by means of a dedicated DC/DC buck converter. The PAM modulation causes block shaped motor currents, which result in high eddy current losses in the rotor [46]. In high-speed motors it is especially difficult to dissipate rotor losses due to the small rotor surface. This is a significant drawback of PAM inverters that needs to be addressed.

The main target for this application is to replace the PAM inverter with a pulse width modulated (PWM) inverter, in an effort to improve the motor current quality. A typical PWM inverter is shown in **Fig. 1.6(b)**. By employing a high switching frequency, a PWM inverter significantly improves the motor current quality, thus allows the reduction of the critical rotor losses. However, a high switching frequency inevitably leads to high switching losses of the semiconductor devices. In order to limit the switching losses, the latest GaN semiconductor technology is used. Even though a PWM inverter may be less efficient than a PAM inverter, the former allows to shift losses from the motor to the inverter, resulting in a better performance of the motor drive system as a whole. The performance limits of PWM inverters are explored in this thesis.

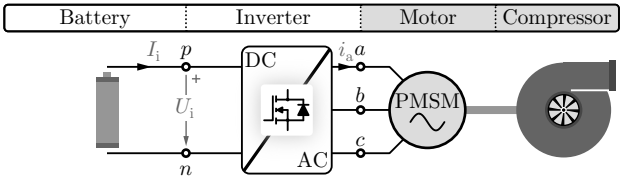


Fig. 1.4: High-speed motor drive **Application I**. The inverter is supplied with a constant DC voltage U_i, and controls the high-speed electric compressor of **Fig. 1.5(b)**.

Tab. 1.1: Specifications of high-speed motor drive **Application I**.

Inverter input voltage	$U_i = 48\,V$
Inverter power	$P = 0\,W...330\,W$
Inverter power density	$\rho \geq 1.32\,kW/dm^3$ $(0.25\,dm^3)$
Inverter efficiency	$\eta \geq 97\%$ $(9.9\,W)$
Motor speed	$n = 0\,rpm...500\,krpm$
Motor fundamental freq.	$f_m = 0\,Hz...8.3\,kHz$
Motor power	$P = 0\,W...200\,W$
Motor voltage (phase, PK)	$\hat{U}_m = 0\,V...19\,V$

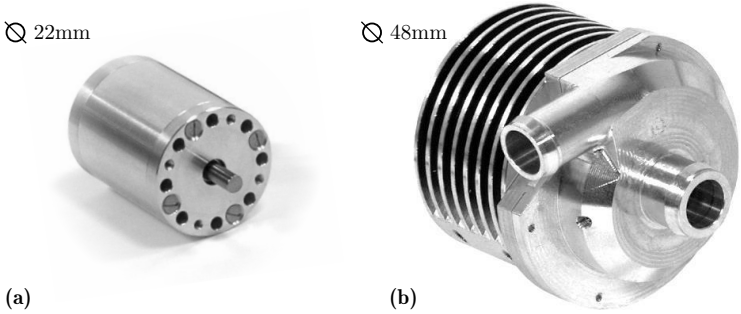


Fig. 1.5: (a) High-speed, 500 krpm, 200 W electric motor [49]. **(b)** High-speed, 500 krpm, 70 W electric compressor (including the motor) with ball bearings [50].

Application II is presented in **Fig. 1.7** and summarized in **Tab. 1.2**. A $n = 280\,krpm$ electric compressor provides compressed air to a 10 kW fuel-cell unit. An inverter, directly supplied by the fuel-cell DC voltage $U_i = 40\,V...120\,V$, controls the electric compressor. The electric compressor consumes approximately 10% of the fuel-cell power, i.e. $P = 1\,kW$. A ball bearing and a gas bearing variant of the $n = 280\,krpm$ electric compressor is

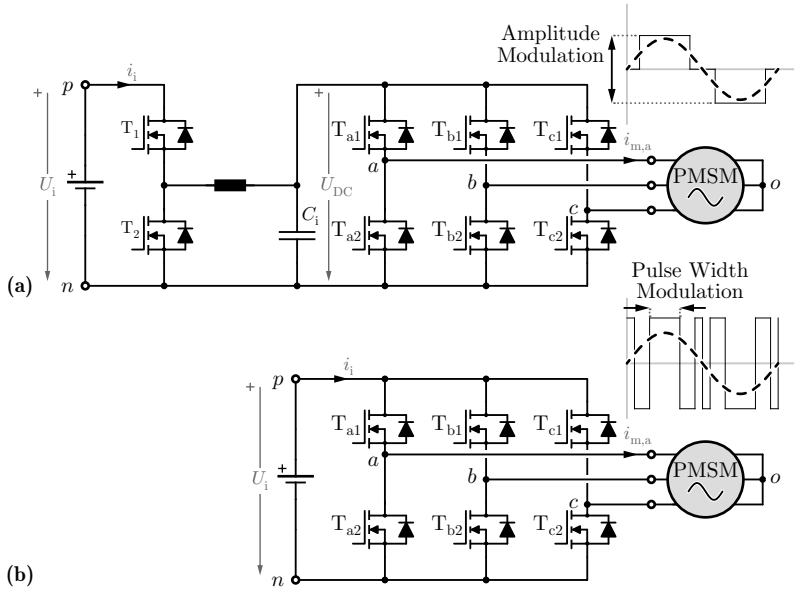


Fig. 1.6: (a) State-of-the-art inverter employing pulse amplitude modulation (PAM). A dedicated DC/DC buck converter controls the DC link voltage U_{DC}. **(b)** Pulse width modulated (PWM) inverter.

shown in **Fig. 1.8(b.i)** and **(b.ii)**, respectively. A stand alone $n = 280\,\mathrm{krpm}$ electric motor is depicted in **Fig. 1.8(a)**.

Besides the requirement for high quality motor currents, the inverter has to cope with the wide DC voltage variation of the fuel-cell, in this application. Under no-load condition the fuel-cell features the maximum DC voltage of $U_{\mathrm{i}} = 120\,\mathrm{V}$, while under full-load condition the fuel-cell exhibits the lowest DC voltage of $U_{\mathrm{i}} = 40\,\mathrm{V}$. The inverter systems must be able to guarantee the nominal motor speed/voltage independent of the fuel-cell voltage variation. To this end, novel buck-boost inverter solutions are developed and new modulation strategies are explored in this thesis.

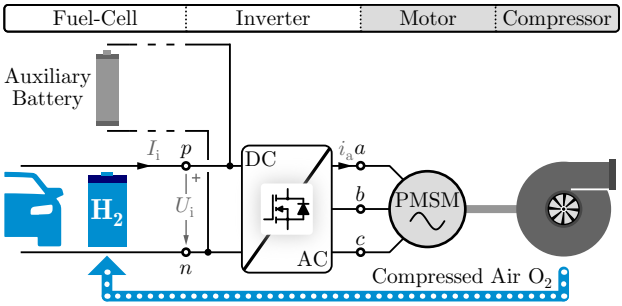


Fig. 1.7: High-speed motor drive **Application II**. The electric compressor of **Fig. 1.8(b.ii)** provides the air supply, needed for the operation of a fuel-cell. An inverter supplied by the fuel-cell, controls the high-speed compressor. An auxiliary battery, parallel to the fuel-cell, is used for the system startup.

Tab. 1.2: Specifications of high-speed motor drive **Application II**.

Fuel-cell Power	$P_{FC} = 0\,W...10\,kW$
Fuel-cell voltage	$U_i = 40\,V...120\,V$
Inverter power	$P = 0\,W...1100\,W$
Inverter power density	$\rho \geq 1.57\,kW/dm^3$ $(0.7\,dm^3)$
Inverter efficiency	$\eta \geq 95\%$ $(50\,W)$
Motor speed	$n = 0\,rpm...280\,krpm$
Motor fundamental freq.	$f_m = 0\,Hz...4.7\,kHz$
Motor power	$P = 0\,W...1000\,W$
Motor voltage (phase, PK)	$\hat{U}_m = 0\,V...40\,V$

1.4 Thesis Outline

The content of the thesis is divided into five main chapters and the conclusions. All the chapters can be read independently, since the interdependencies have been reduced to the strict minimum.

Chapter 2 focuses on PWM voltage source inverters (VSI), for high-speed motor drives. In order to guarantee sinusoidal motor voltages/currents, a filter is placed between the inverter and the motor. The additional losses and volume of the filter compromise the overall inverter performance. New modulation strategies are proposed, that mitigate the negative impact of the output filter. The proposed modulation concepts are validated on a hardware demonstrator, built for the application I (cf. **Tab. 1.1**).

Fig. 1.8: (a) High-speed, 280 krpm, 1 kW electric motor [51]. High-speed, 280 krpm, 1 kW electric compressor (including the motor) with **(b.i)** ball bearings [52] and **(b.ii)** gas bearings [53].

In **Chapter 3** the electromagnetic compatibility challenges, caused by WBG semiconductor devices, are discussed. A comprehensive input/output filter design algorithm is proposed, tailored to the needs of high-speed drives and WBG inverters. The theoretical considerations are verified on a purposely assembled hardware demonstrator, for the application II (cf. **Tab. 1.2**).

From this point on, buck-boost inverter topologies are analysed, which can cope with the wide DC voltage fluctuation of a fuel-cell. The application II (cf. **Fig. 1.7** and **Tab. 1.2**) is considered.

In **Chapter 4** a conventional buck-boost inverter solution is discussed, with two energy conversion stages. As a result of the two conversion stages, this inverter solution suffers from a low efficiency. A new modulation concept, that combines the control of the two conversion stages and results in a higher inverter efficiency, is proposed in this chapter. The performance of the new modulation strategy is verified on a hardware demonstrator.

In order to overcome the inherent limitations of two-stage inverters, a single-stage buck-boost inverter topology, denoted as Y-inverter, is proposed in **Chapter 5**. The advantages of the Y-inverter are highlighted in this chapter, while appropriate modulation strategies are developed. A hardware prototype is assembled and tested. The experimental results verify the superior performance of the Y-inverter, compared to a conventional two-stage inverter solution.

In **Chapter 6** innovation in the inverter stage is combined with innovation in the motor side. As a result, the double-bridge voltage source inverter (DB-VSI) technology is proposed, where two VSIs are connected to the opposite sides of an open-end winding motor (no floating neutral point). This inverter/motor solution achieves excellent efficiency and power density, which is validated by means of two hardware prototypes. Finally, the DB-VSI technology is applied on an IMD, (by the industry partner Celeroton AG), where the inverter is integrated in the compressor housing of **Fig. 1.8(b.ii)**.

Chapter 7 briefly summarizes key results and findings of this thesis. An outlook on future research is also given.

1.5 List of Publications

Key insights presented in this thesis have already been published or will be published in international scientific journals, conference proceedings, presented at workshops and/or have been protected by patents. The publications developed in the course of this thesis are listed below.

Journal Papers

- M. Antivachis, F. Dietz, C. Zwyssig, D. Bortis, and J. W. Kolar, "Novel high-speed turbo compressor with integrated inverter for fuel-cell air supply," *Frontiers in Mechanical Engineering*, 2020, early access. .
- M. Antivachis, D. Wu, and J. W. Kolar, "Analysis of double-bridge inverters for drive systems with open-end winding motors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020, early access. DOI: 10.1109/JESTPE.2020.3017085.
- M. Antivachis, N. Kleynhans, and J. W. Kolar, "Three-phase sinusoidal output buck-boost GaN Y-inverter for advanced variable speed AC drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020, early access. DOI: 10.1109/JESTPE.2020.3026742.

- M. Antivachis, P. Niklaus, D. Bortis, and J. W. Kolar, "Input / output EMI filter design for three-phase ultra-high speed motor drive GaN inverter stage" *CPSS Transactions on Power Electronics and Applications*, 2020, early access. .

- M. Antivachis, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 34-53, March 2020. DOI: 10.24295/CPSST-PEA.2020.00004.

- M. Antivachis, D. Bortis, A. Avila, and J. W. Kolar, "New optimal common-mode modulation for three-phase inverters with DC-link referenced output filter," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 331-340, December 2017. DOI: 10.24295/CPSST-PEA.2017.00030.

Conference Papers

- M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of Y-inverter against three-phase two-stage buck-boost DC-AC converter systems," in *Proc. of International Power Electronics Conference (IPEC-ECCE Asia)*, Niigata, Japan, May 2018, pp. 181-189. DOI: 10.23919/IPEC.2018.8507664.

- M. Antivachis, D. Bortis, L. Schrittwieser, and J. W. Kolar, "Three-phase buck-boost Y-inverter with wide DC input voltage range," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, March 2018, pp. 1492-1499. DOI: 10.1109/APEC.2018.8341214.

Patents

- M. Leibl, L. Schrittwieser, J. W. Kolar, D. Bortis, and M. Antivachis, "Konverter zur Übertragung von elektrischer Energie zwischen einem DC und einem AC-System," Swiss Patent Application No. *CH 01159/17*, September 2017. .

- J. W. Kolar, D. Bortis, and M. Antivachis, "Verfahren zur Ansteuerung eines mehrphasigen Wechselrichters und Verfahren zur Minimierung des Rippelstromeffektivwertes in der Ausgangsfilterinduktivität von

Dreiphasen-Pulswechselrichtersystemen," Swiss Patent Application No. *CH 01071/17*, August 2017. .

Workshops and Seminars

- J. W. Kolar, M. Guacci, M. Antivachis, and D. Bortis, "Next-generation SiC/GaN three-phase variable-speed drive PWM inverter concepts," Tutorial at the *9th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Nanjing, China, December 2020. .

- J. W. Kolar, M. Guacci, M. Antivachis, and D. Bortis, "Advanced 3-phase SiC/GaN PWM inverter concepts for future VSD applications," Tutorial at the *35th Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 2020. .

- J. W. Kolar, M. Guacci, M. Antivachis, and D. Bortis, "Advanced 3-Φ SiC/GaN PWM inverter & rectifier systems," Tutorial at the *45th Annual Conference of the IEEE Industrial Electronics Society 2019 (IECON)*, Lisbon, Portugal, October 2019. .

- D. Bortis, M. Guacci, M. Antivachis, and J. W. Kolar, "Future SiC/GaN variable speed drive inverter topologies - How to handle a double-edged sword," Presentation at the *2nd Wagner Automotive Symposium — Inverter Trends & Technology*, Wangen, Germany, November 2019. .

- J. W. Kolar, J. Azurza, M. Guacci, M. Antivachis, and D. Bortis, "Advanced 3-phase SiC/GaN PWM inverter and rectifier systems," Presentation at the *Centre for Power Electronics Annual Conference*, Loughborough, United Kindom, July 2019. .

- D. Bortis, J. W. Kolar, M. Antivachis, J. Azurza, M. Guacci, and D. Menzi, "Advanced three-phase PFC-rectifiers," Presentation at the *Presentation at the ECPE Cluster-Seminar*, Augsburg, Germany, May 2019. .

- J. W. Kolar, M. Antivachis, D. Bortis, D. Menzi, J. Miniböck, F. Krismer, and D. Rothmund, "Latest findings in three-phase AC/DC converter research," Presentation at the *Future Energy Technology Workshop*, Nuremberg, Germany, June 2018. .

Additional Contributions

- J. W. Kolar, J. Azurza Anderson, S. Miric, M. Haider, M. Guacci, M. Antivachis, G. Zulauf, D. Menzi, P. S. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittantiz, and D. Bortis, "Application of WBG power devices in future 3-Φ variable speed drive inverter systems," in *Proc. of IEEE International Electron Devices (IEDM)*, San Francisco, CA, USA, December 2020. .
- P. Niklaus, M. Antivachis, D. Bortis, and J. W. Kolar, "Analysis of the influence of measurement circuit asymmetries on three-phase CM/DM conducted EMI separation," *CPSS Transactions on Power Electronics and Applications*, 2020, early access. DOI: 10.1109/TPEL.2020.3025122.

2

Voltage Source Inverter - Advanced Modulation Strategies

This chapter summarizes the key research findings also presented in:

M. Antivachis, D. Bortis, A. Avila and J. W. Kolar, "New optimal common-mode modulation for three-phase inverters with DC-link referenced output filter," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 331-340, December 2017. DOI: 10.24295/CPSSTPEA.2017.00030.

Motivation

Voltage source inverters (VSI) followed by a full sine-wave output filter (FSF) have found broad acceptance in high-speed motor drives. However, the special characteristics of the FSF are usually not taken into consideration by the modulation strategy of the VSI. This chapter addresses this blind spot of literature, by introducing new modulation strategies tailored to an FSF.

Executive Summary

A two-level voltage source inverter (VSI) followed by a full sine-wave output filter (FSF) is typically used for high-speed, low-voltage drive systems. A limitation of this inverter solution lies in the additional losses occurring within the output filter. In particular, the output filter inductors, which suffer high current ripple, are a main driver of losses. This shortcoming can be addressed by means of an appropriate modulation strategy. This chapter details two new modulation strategies, tailored to the specific characteristics of a VSI with an FSF. By utilizing the instantaneous CM voltage as a degree of freedom, the output inductor's current ripple is reduced. It is deduced that a constant (DC) CM voltage injection (DCCMM) or a time varying (AC) CM voltage injection (ACCMM) yields the best performance, depending on the inverter operating point. In an effort to further reduce the inductor current ripple/losses, the two above modulation strategies are combined. The resulting modulation strategy is denoted as optimal CM injection modulation (OCMM). Finally, the proposed modulation strategies are tested on a 330 W hardware prototype driving a 400 krpm motor. There, an up to 11% reduction of the total inverter losses is observed.

High-speed, low-voltage drive systems spread across a wide range of applications such as turbocompressor systems, drills, medical equipment, and air-conditioning units [16, 17]. Typically, a two-level voltage source inverter (VSI) employing pulse width modulation (PWM) drives the high-speed motor, as illustrated in **Fig. 2.1**. A full sine-wave output filter (FSF), that features both differential-mode (DM) and common-mode (CM) attenuation, is placed between the VSI and the motor in order to ensure high motor voltage quality. An FSF offers two main advantages:

(i) Reduction of rotor losses. An FSF guarantees sinusoidal motor currents/voltages, that minimize the induced rotor losses [54]. The rotor losses are a main concern in high-speed motors, where it is difficult to extract heat from the rotor, due to its small surface/volume.

(ii) Suppression of $\mathrm{d}u/\mathrm{d}t$. An FSF suppresses the CM $\mathrm{d}u/\mathrm{d}t$ generated by wide-bandgap semiconductor devices. Thereby, the motor bearing is protected from excess voltage/current stress [34], which would lead to premature failure.

The selected FSF belongs to the family of DC link referenced filters [36–38], i.e. the capacitors C_o of the filter are connected/referenced to the negative DC rail n. The simplicity/low cost of a DC link referenced output filter, renders it a prominent choice in low-voltage drive systems, where cost is a main

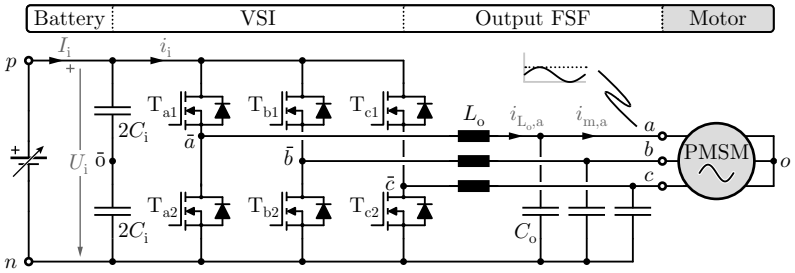


Fig. 2.1: Two-level voltage source inverter (VSI) with a full sine-wave output filter (FSF) driving a high-speed motor.

Tab. 2.1: Motor drive system specifications. The nominal operating condition is highlighted in bold.

Inverter input voltage	U_i	48 V
Inverter power	P	0 W…**330 W**
Inverter switching freq.	f_s	280 kHz
Inverter filter inductance	L_o	17 µH
Inverter filter capacitance	C_o	1.4 µF
Motor speed	n	0 rpm…**400 krpm**
Motor fundamental freq.	f_m	0 Hz…**6.6 kHz**
Motor power	P	0 W…**300 W**
Motor voltage (phase, PK)	$\hat{U}_m$	0 V…**19 V**

design driver. A high switching frequency f_s is typically preferred, in order to reduce the volume of the output filter's passive components.

The incorporation of an output filter allows for better motor voltage quality at the expense of decreased inverter performance, since the volume and losses of the output filter are added to the inverter stage. There has been extensive research towards modulation strategies that counterbalance the negative impact of an output filter [55–58]. According to literature, the available degree of freedom in the modulation of a VSI is the shape of the CM duty cycle $d_{\mathrm{CM}}(t)$ [59] which is injected to all three phases

$$\begin{aligned} d_{\mathrm{a}}(t) &= M_1 \cos(\omega_{\mathrm{m}} t) + d_{\mathrm{CM}}(t) \\ d_{\mathrm{b}}(t) &= M_1 \cos(\omega_{\mathrm{m}} t - \frac{2\pi}{3}) + d_{\mathrm{CM}}(t), \\ d_{\mathrm{c}}(t) &= M_1 \cos(\omega_{\mathrm{m}} t + \frac{2\pi}{3}) + d_{\mathrm{CM}}(t) \end{aligned} \tag{2.1}$$

where M_1 is the modulation index

$$M_1 = \frac{\hat{U}_{\mathrm{m}}}{\frac{1}{2} U_{\mathrm{i}}}, \tag{2.2}$$

and $\hat{U}_{\mathrm{m}}$ is the motor phase voltage amplitude. The CM duty cycle pattern $d_{\mathrm{CM}}(t)$ impacts the performance of the inverter. In the case of a VSI followed by a simple DM filter, for example, the injection of an approximately triangular CM duty cycle (space vector modulation) yields the lowest filter inductor current ripple [60]. A sinusoidal third harmonic injection results in a similar filter inductor current ripple. In contrast, the injection of a roughly rectangular CM duty cycle (discontinuous modulation), leads to a reduction of the switching losses but higher inductor current ripple [61, 62].

In the case of a VSI with an FSF, the formulation mechanism of the filter inductor current ripple $\Delta i_{\mathrm{L_o}}$ is fundamentally different compared to a simple DM filter. In particular, CM currents flow through the FSF capacitors C_{o} from/towards the negative DC rail n, resulting in a high overall current ripple across the filter inductor L_{o}. A high current ripple $\Delta i_{\mathrm{L_o}}$ results in high losses in the filter inductors. Therefore, a modulation strategy that minimizes the inductor current ripple is needed. However, the previously described modulation strategies correspond to a simple DM filter, and thus do not yield the desired inductor performance for the case of an FSF. Instead, the optimal shape of the CM duty cycle $d_{\mathrm{CM}}(t)$, that minimizes the current ripple of the filter inductors, must be revisited and redefined according to the special characteristics of the FSF at hand.

In response to those concerns, this chapter details the degrees of freedom, when selecting the modulation strategy of a VSI employing an FSF. In particular, two new modulation strategies that reduce the filter inductor current ripple are proposed in **Sec. 2.1**:

(i) DC CM injection modulation (DCCMM). A constant (DC) CM duty cycle $d_{\mathrm{CM}}(t) = -M_0$ is injected into all three phases.

(ii) AC CM injection modulation (ACCMM). A time varying (AC) CM duty cycle with arbitrarily large amplitude $d_{\mathrm{CM}}(t) = -M_{\mathrm{N}} \cos(N\omega_{\mathrm{m}} t)$ (N = 3, 6, 9,...) is injected into all three phases.

Subsequently in **Sec 2.2**, the stresses on the different inverter components are calculated. The proposed modulation strategies are tested on a 330 W hardware prototype driving a 400 krpm motor in **Sec. 2.3**. There, an up to 11% reduction of the total inverter losses is observed. Finally, a summary is given in **Sec. 2.4**.

2.1 Modulation Strategies

The inverter system shown in **Fig. 2.1**, features a two-level voltage source inverter (VSI), followed by a full sine-wave output filter (FSF). Sinusoidal motor voltages (with respect to the motor floating neutral point o) are desirable

$$\begin{aligned} u_{\mathrm{ao}}(t) &= u_{\mathrm{m,a}}(t) = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t) \\ u_{\mathrm{bo}}(t) &= u_{\mathrm{m,b}}(t) = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t - \frac{2\pi}{3}), \\ u_{\mathrm{co}}(t) &= u_{\mathrm{m,c}}(t) = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t + \frac{2\pi}{3}) \end{aligned} \tag{2.3}$$

where $\omega_{\mathrm{m}} = 2\pi f_{\mathrm{m}}$ is the motor angular frequency. The inverter generates the sinusoidal motor voltages by controlling the output terminal voltages $[u_{\mathrm{a\bar{o}}}, u_{\mathrm{b\bar{o}}}, u_{\mathrm{c\bar{o}}}]$ (with respect to the DC link mid-point $\bar{o}$). In the case of an FSF, the capacitors C_{o} are connected to the negative DC rail n. Each phase-leg is equivalent to a simple buck converter and is independent of the other two phases. This is different from a simple DM filter, where the capacitors C_{o} are connected to a floating star point, resulting in a coupling among the three phases. From now on, the analysis is focused on phase a, when possible, while the results can be easily extended to phases b and c.

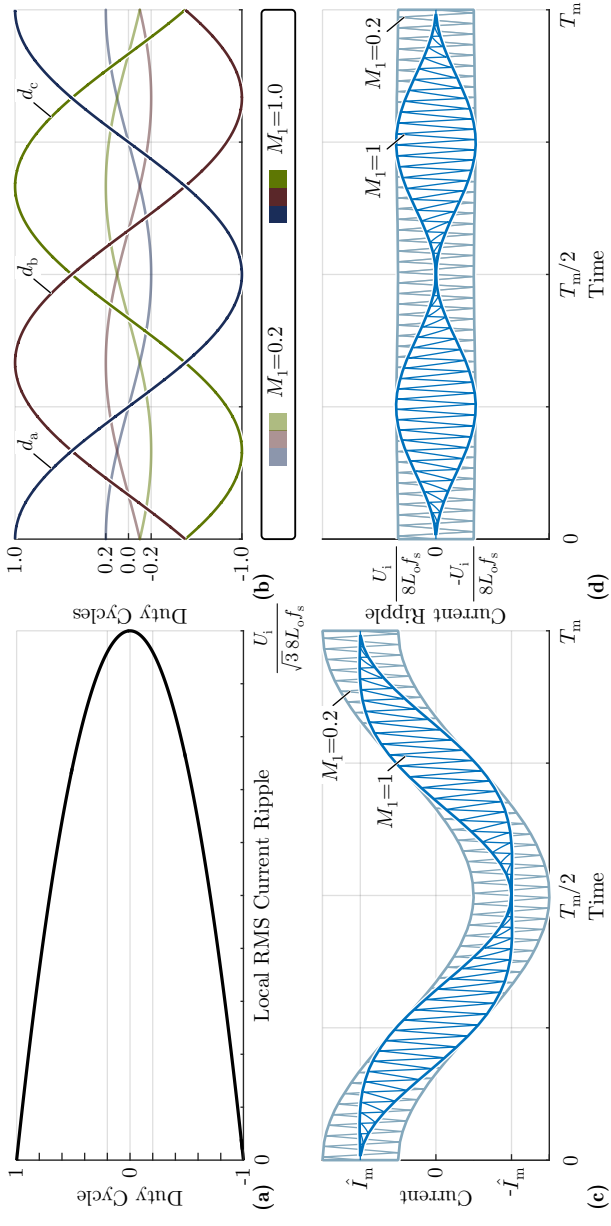


Fig. 2.2: Characteristic waveforms of sinusoidal modulation (SM). **(a)** Local RMS current ripple $\Delta i_{L_o,a,RMS}$ of the filter inductor L_o, as a function of the instantaneous duty cycle d_a. **(b)** Duty cycles for modulation index $M_I = 0.2$ and $M_I = 1$. **(c)** Current and **(d)** current ripple of the output filter inductor L_o.

2.1.1 Drawbacks of Sinusoidal Modulation (SM)

According to the conventional sinusoidal modulation (SM), all duty cycles are purely sinusoidal. In this case, the phase a duty cycle is

$$d_{\mathrm{a}}(t) = M_1 \cos(\omega_{\mathrm{m}} t), \tag{2.4}$$

and ranges within $d_{\mathrm{a}}(t) = -1...1$. The inverter phase a output voltage is in general proportional to the duty cycle d_{a}

$$u_{\mathrm{a\bar{o}}}(t) = d_{\mathrm{a}}(t)\frac{U_{\mathrm{i}}}{2} \overset{(2.1)}{=} M_1 \frac{U_{\mathrm{i}}}{2}\cos(\omega_{\mathrm{m}} t) + d_{\mathrm{CM}}(t)\frac{U_{\mathrm{i}}}{2}, \tag{2.5}$$

and is simplified, in the case of SM, to

$$u_{\mathrm{a\bar{o}}}(t) = M_1 \frac{U_{\mathrm{i}}}{2}\cos(\omega_{\mathrm{m}} t). \tag{2.6}$$

The inductor voltage is equal to the difference between the switch-node voltage and the inverter output voltage

$$u_{\mathrm{L_o,a}}(t) = u_{\mathrm{\bar{a}\bar{o}}}(t) - u_{\mathrm{a\bar{o}}}(t). \tag{2.7}$$

The switch-node $\bar{a}$ features a two-level PWM voltage $u_{\mathrm{\bar{a}\bar{o}}}(t)$, which assumes two values $u_{\mathrm{\bar{a}\bar{o}}} = \{-\frac{U_{\mathrm{i}}}{2}, +\frac{U_{\mathrm{i}}}{2}\}$. As a result, the inductor also features a two-level PWM voltage $u_{\mathrm{L_o,a}}(t)$, in the case of an FSF. The two-level PWM inductor voltage induces a high-frequency current ripple across the inductor. Note that, the inductor would feature a five-level PWM voltage in the case of a simple DM filter, which would result in a significantly lower inductor current ripple, compared to an FSF. The local (instantaneous) current ripple amplitude of the inductor L_{o} is

$$\Delta i_{\mathrm{L_o,a,PK}}(t) = (1 + d_{\mathrm{a}})(1 - d_{\mathrm{a}})\frac{U_{\mathrm{i}}}{8 L_{\mathrm{o}} f_{\mathrm{s}}}. \tag{2.8}$$

Accordingly, the local RMS current ripple is

$$\Delta i_{\mathrm{L_o,a,RMS}}(t) = \frac{\Delta i_{\mathrm{L_o,a,PK}}(t)}{\sqrt{3}} = (1 + d_{\mathrm{a}})(1 - d_{\mathrm{a}})\frac{U_{\mathrm{i}}}{8\sqrt{3} L_{\mathrm{o}} f_{\mathrm{s}}}, \tag{2.9}$$

and is visualized in **Fig. 2.2(a)**. The duty cycle $d_{\mathrm{a}} = 0$ maximizes the local current ripple of the filter inductor

$$\Delta I_{\mathrm{L_o,PK,max}} = \frac{U_{\mathrm{i}}}{8 L_{\mathrm{o}} f_{\mathrm{s}}}, \qquad \Delta I_{\mathrm{L_o,RMS,max}} = \frac{U_{\mathrm{i}}}{8\sqrt{3} L_{\mathrm{o}} f_{\mathrm{s}}}, \tag{2.10}$$

while the local current ripple retains a high values in the area closes to $d_a = 0$. In contrast, the current ripple is almost zero when the duty cycle d_a is in the vicinity of 1 or -1.

For SM and a low modulation index $M_1 = 0.2$, the duty cycles of all three phases remain close to zero for the whole fundamental period T_m, as shown in **Fig. 2.2(b)**. As a results, the current ripple **(2.9)** and hence the losses of the filter inductors are high. The inductor current and current ripple are visualised in **Fig. 2.2(c)** and **(d)**, respectively. For low modulation indexes, where the motor speed, voltage and power are low, high inductor current ripple/losses occur. Then, the ratio between losses and transmitted power is high, leading to a low part-load inverter efficiency. For a high modulation index $M_1 = 1$, the overall current ripple reduces (cf. **Fig. 2.2(c)** and **(d)**).

In order to reduce the current ripple occurring for low modulation indexes, the duty cycles should be modified. By moving the duty cycles away from the high current ripple zone of $d_a = 0$, it is possible to reduce the inductor current ripple. This can be achieved by means of a CM duty cycle injection, meaning that an identical signal $d_{CM}(t)$ (either constant or time varying) is added to the duty cycles of all three phases **(2.1)**. The positive impact of a CM duty cycle injection can be also explained from a frequency domain standpoint. In the case of SM modulation, the switch-node voltage $u_{\bar{a}\bar{o}}(t)$ features a fundamental frequency f_m component, which is related to the modulation index M_1. Furthermore, the switch-node voltage features switching frequency f_s harmonics, which are related to the PWM modulation. The switch-node voltage spectrum of a VSI employing SM is illustrated in **Fig. 2.3(a)**. The injection of a low-frequency CM duty cycle advantageously shapes the spectral content of the switch-node voltage: Energy is transferred from the switching frequency f_s harmonics to the low-frequency that corresponds to the injected CM pattern. By reducing the high-frequency harmonic content of the switch-node voltage, the harmonic content of the inductor voltage is simultaneously decreased. As a result, the current ripple is reduced and accordingly the output filter losses are limited. Two CM duty cycle patterns are proposed in this chapter:

(i) The constant CM injection (DCCMM) of **Fig. 2.3(b.ii)**, where all three-phase duty cycles are shifted downwards, $d_{CM}(t) = -M_0$. As shown in **Fig. 2.3(b.i)**, DCCMM shifts parts of the harmonic spectrum from the switching frequency f_s to the DC frequency component $f = 0$.

(ii) The time varying CM injection (ACCMM) of **Fig. 2.3(c.ii)**, where a sinusoidal CM duty cycle $d_{CM}(t) = -M_N \cos(N\omega_m t)$ ($N = 3, 6, 9, \ldots$)

with a repetition frequency Nf_m and with arbitrarily large amplitude M_N is added to all three-phase duty cycles. As shown in **Fig. 2.3(c.i)**, ACCMM shifts parts of the harmonic spectrum from the switching frequency f_s to the low-frequency component $f = Nf_\mathrm{m}$.

2.1.2 DC CM Injection Modulation (DCCMM)

The DC CM injection modulation (DCCMM) utilizes a constant CM signal $d_\mathrm{CM} = -M_0$ that shifts all instantaneous sinusoidal duty cycle signals $[d_\mathrm{a}, d_\mathrm{b}, d_\mathrm{c}]$ away from the high current ripple region around $d = 0$, towards a lower ripple zone close to $d = -1$. The phase a duty cycle is

$$d_\mathrm{a}(t) = M_1 \cos(\omega_\mathrm{m} t) - M_0, \tag{2.11}$$

while the inverter phase a output voltage **(2.5)** is proportional to the duty cycle d_a,

$$u_{\mathrm{a\bar{o}}}(t) = M_1 \frac{U_\mathrm{i}}{2} \cos(\omega_\mathrm{m} t) - M_0 \frac{U_\mathrm{i}}{2}. \tag{2.12}$$

The DCCMM modulation strategy is visualized in **Fig. 2.4(b)** for a modulation index of $M_1 = 0.2$. There, two different injection parameter M_0 values, $M_0 = 0.4$ and $M_0 = 0.8$, are depicted. Furthermore, the case of $M_0 = 0$ is shown, which is equivalent to simple SM. The effect of DCCMM on the inductor current and current ripple is shown in **Fig. 2.4(c)** and **(d)**, respectively. The current ripple envelope is contracting with increasing CM injection M_0, thus DCCMM positively impacts the inductor performance. The parameter value $M_0 = 0.8$ yields the lowest inductor current ripple, for the example at hand. It is noted, that DCCMM can also use negative injection values, i.e. $M_0 < 0$, with symmetric effects on the filter inductor current. For the conventional SM ($M_0 = 0$), the current ripple reaches its maximum value at the zero crossings of the duty cycle, which occur at the time instants $t = T_\mathrm{m}/4$ and $t = 3T_\mathrm{m}/4$. However, the time instances of the duty cycle zero crossing are changing for DCCMM. No duty cycle zero crossing occurs for example in **2.4(b)** when $M_0 = 0.4$ or $M_0 = 0.8$. In this case, the maximum current ripple is found at $t = 0$.

The CM injection parameter M_0 represents a degree of freedom, that can be optimized. Depending on the modulation index M_1, a different range of the injection parameter M_0 is available. The acceptable range of the M_0 can be easily derived by the constraint that all three duty cycle signals must not

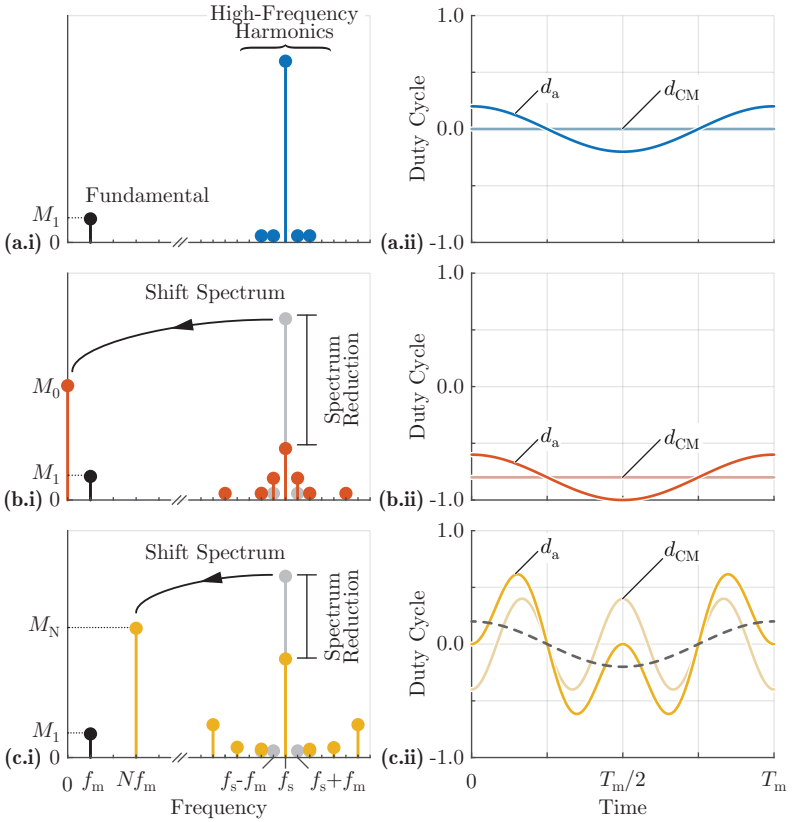


Fig. 2.3: (i) Spectrum of the switch-node voltage $u_{\bar{a}\bar{o}}$. **(ii)** Duty cycle $d_a(t)$ of phase a and CM duty cycle injection $d_{CM}(t)$, into all three phases. **(a)** Conventional sinusoidal modulation (SM). **(b)** DC CM injection modulation (DCCMM), where the duty cycle is shifted downwards by $d_{CM} = -M_0$. Spectral content is transferred from the switching frequency f_s to the DC component $f = 0$. **(c)** AC CM injection modulation (ACCMM), where a sinusoidal CM duty cycle $d_{CM}(t) = -M_N \cos(N\omega_m t)$ is injected. Spectral content is transferred from the switching frequency f_s to the CM duty cycle repetition frequency $f = Nf_m$.

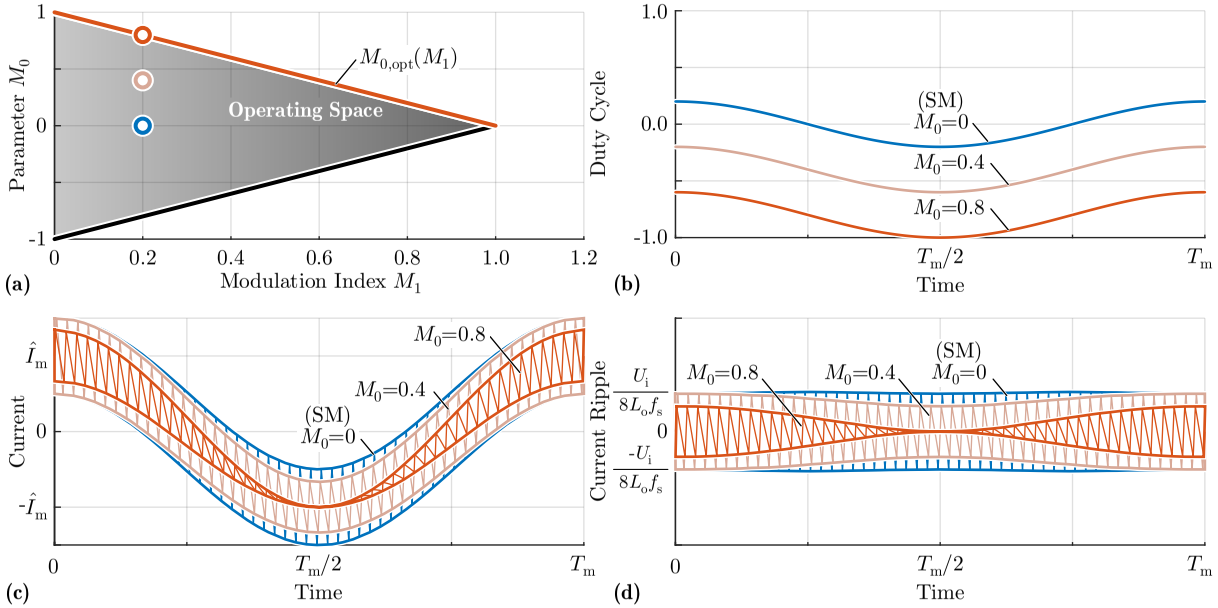


Fig. 2.4: DC CM injection modulation (DCCMM) characteristic waveforms. **(a)** Available injection parameter M_0 value range, depending on the modulation index M_1. **(b)** Phase *a* duty cycle for a modulation index $M_1 = 0.2$ and different values of the CM injection parameter M_0. **(c)** Current and **(d)** current ripple of the filter inductor L_o.

exceed the carrier boundaries (i.e. $-1 \leq d \leq 1$). Depending on the modulation depth M_1, the M_0 injection limits are shown in **Fig. 2.4(a)** and are

$$-(1 - M_1) \leq M_0 \leq 1 - M_1. \tag{2.13}$$

It is noted, that the feasible M_0 interval becomes wider for low modulation depths M_1. For the example $M_1 = 0.2$ of **Fig. 2.4**, the M_0 parameter can be freely selected within the interval $M_0 = -0.8... + 0.8$. In contrast, for $M_1 = 1$, the M_0 parameter value must be kept at zero, otherwise the instantaneous duty cycles would exceed the carrier boundaries. When $M_1 > 1$ (i.e. overmodulation), the DCCMM modulation is impractical, since it provokes undesired pulse dropping which in return significantly increases the inductor current ripple. Therefore, DCCMM is only advisable for the limited modulation index region $M_1 = 0...1$. The DCCMM is summarized in **Tab. 2.2**.

2.1.3 AC CM Injection Modulation (ACCMM)

In a second step, the AC CM injection modulation (ACCMM) is investigated. There, a time varying CM pattern $d_{\mathrm{CM}}(t) = -M_{\mathrm{N}} \cos(2\pi N f_{\mathrm{m}} t)$ (N = 3, 6, 9,...) is injected into the duty cycles of all three phases. This CM pattern features a sinusoidal shape, a repetition frequency of $N f_{\mathrm{m}}$ and an amplitude M_{N}. According to ACCMM, the high-frequency spectrum of the switch-node voltage $u_{\bar{a}\bar{0}}$ is reduced, and instead more spectral content is concentrated at the CM pattern repetition frequency $N f_{\mathrm{m}}$, as is illustrated in **Fig. 2.3(c)**. Hence, the high-frequency voltage across the inductor is reduced, resulting in lower current ripple/losses.

The repetition frequency of the CM signal $N f_{\mathrm{m}}$ is now selected. Special attention should be paid to the reactive current flowing through the filter capacitors C_{o}. The total N^{th} order harmonic current $\hat{I}_{\mathrm{C_o},N}$, caused by the ACCMM is

$$\hat{I}_{\mathrm{C_o,N}} = \frac{3}{2} M_{\mathrm{N}} U_{\mathrm{i}} N \omega_{\mathrm{m}} C_{\mathrm{o}}. \tag{2.14}$$

This reactive current is proportional to the amplitude M_{N} and the repetition frequency $N f_{\mathrm{m}}$ of the CM duty cycle pattern. Especially for high-speed motor drives, where the fundamental frequency f_{m} can be in the kHz range, the reactive currents at the frequency $N f_{\mathrm{m}}$ become significant, hence should be limited. Otherwise, additional conduction losses would occur, degrading the overall system performance. In the course of this research, which focuses on high-speed drive systems, the repetition frequency of the AC CM duty cycle must be set to the lowest possible value of $3 f_{\mathrm{m}}$. Thereby, the ACCMM reduces

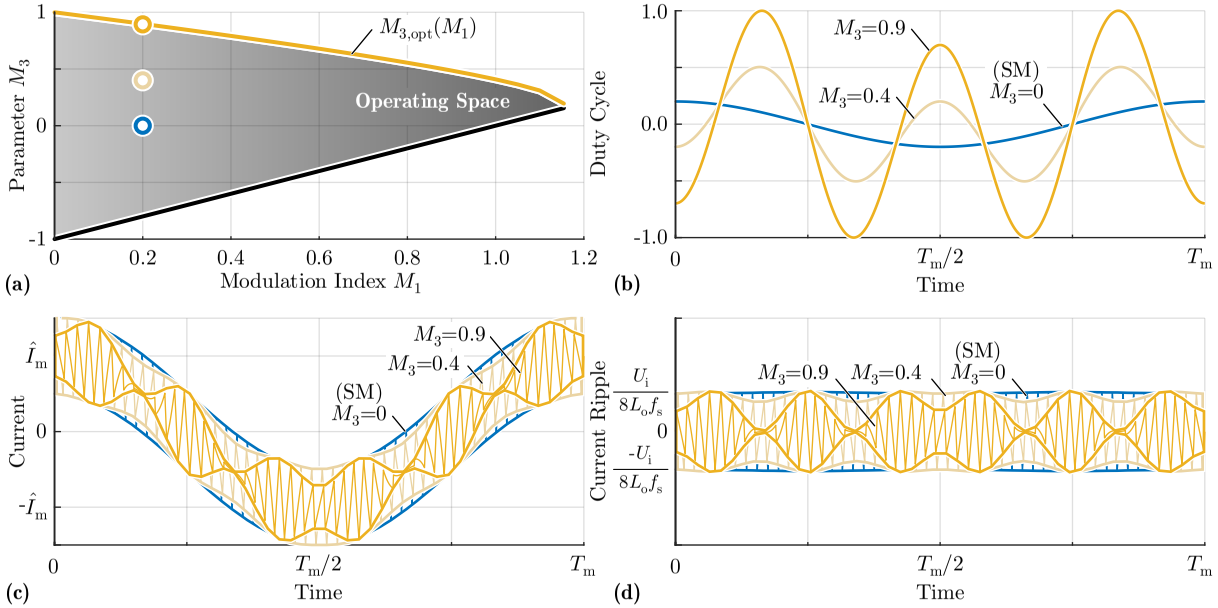


Fig. 2.5: AC CM injection modulation (ACCMM) characteristic waveforms. **(a)** Available injection parameter M_3 value range, depending on the modulation index M_1. **(b)** Phase *a* duty cycle for a modulation index $M_1 = 0.2$ and different values of the CM injection parameter M_3. **(c)** Current and **(d)** current ripple of the filter inductor L_o.

to a generalized version of the third harmonic injection modulation scheme (THM). According to the conventional THM, the amplitude of the third harmonic M_3 is typically set to 1/6 or 1/4, in order to extend the operating range of the inverter in the overmodulation area of $M_1 = 1...2/\sqrt{3}$. In contrast, for the proposed ACCMM, the amplitude of the third harmonic M_3 is considered as a degree of freedom that can be optimized. As the conventional THM, ACCMM can be used in the overmodulation region $M_1 = 1...2/\sqrt{3}$. As a result, the ACCMM can be used in a wider modulation index range of $M_1 = 0...2/\sqrt{3}$, compared to the restricted operating range of $M_1 = 0...1$ of the DCCMM.

From now on, an ACCMM where the CM duty cycle pattern features a repetition frequency of $3f_\mathrm{m}$ (third harmonic) is exclusively considered. According to ACCMM, the phase a duty cycle is

$$d_\mathrm{a}(t) = M_1 \cos(\omega_\mathrm{m} t) - M_3 \cos(3\omega_\mathrm{m} t), \tag{2.15}$$

while the inverter phase a output voltage **(2.5)** is proportional to the duty cycle d_a

$$u_{\mathrm{a\bar{o}}}(t) = M_1 \frac{U_\mathrm{i}}{2} \cos(\omega_\mathrm{m} t) - M_3 \frac{U_\mathrm{i}}{2} \cos(3\omega_\mathrm{m} t). \tag{2.16}$$

Therefore, in the case of ACCMM, the duty cycles and the inverter output voltages are non-sinusoidal. However, the difference between two inverter output voltages, which is equal to the motor line-to-line voltage, is still sinusoidal. In other words, it is possible to generate sinusoidal line-to-line motor voltages, by means of non-sinusoidal inverter output voltages. The ACCMM modulation strategy is visualized in **Fig. 2.5(b)**, for a modulation index of $M_1 = 0.2$. There, two different M_3 parameter values, $M_3 = 0.4$ and $M_3 = 0.9$, are depicted. Furthermore, the case of $M_3 = 0$ is shown, which is equivalent to simple SM. The effect of ACCMM on the inductor current and current ripple is shown in **Fig. 2.5(c)** and **(d)**, respectively. As can be noticed, ACCMM shapes the current ripple envelope in a way that it continuously alternates between high and low current ripple. The overall inductor current stress decreases as the M_3 parameter value increases, and the parameter value $M_3 = 0.9$ yields the lowest inductor current ripple for the $M_1 = 0.2$ example at hand. It is noted that, ACCMM can also use negative parameter values $M_3 < 0$, but the effect on the current is asymmetric, i.e. a parameter value $-M_3$ results in a different current ripple stress on the filter inductor L_o, compared to a parameter value $+M_3$.

The CM injection parameter M_3 represents a degree of freedom, that can be optimized. Depending on the modulation index M_1, a different range of the injection parameter M_3 is available. Similarly to the case of DCCMM, the

three duty cycles must be constrained within $-1 \leq d \leq 1$, in order to avoid pulse dropping. The M_3 parameter limits are shown in **Fig. 2.5(a)** and are

$$-(1 - M_1) \leq M_3 \leq M_{3,\max}(M_1), \tag{2.17}$$

where the maximum allowed parameter value $M_{3,\max}(M_1)$ is derived by numerically solving the non-linear equation

$$M_{3,\max}(M_1) : \begin{cases} M_1 \cos(\phi) - M_{3,\max} \cos(3\phi) = 1 \\ \phi = \sin^{-1}\left(\sqrt{\dfrac{9M_{3,\max} - M_1}{12M_{3,\max}}}\right) \end{cases} . \tag{2.18}$$

In analogy to DCCMM, the available range of M_3 parameter values for AC-CMM, is wider for low modulation depths M_1. The M_3 parameter is increasingly restricted, for higher modulation indexes M_1. For the example of **Fig. 2.5**, where $M_1 = 0.2$, the M_3 parameter can be freely selected within the interval $M_3 = -0.8 \ldots + 0.9$. For a modulation index $M_1 = 1.0$, the M_3 parameter is restricted within the interval $M_3 = 0 \ldots + 0.4$. The ACCMM is summarized in **Tab. 2.2**.

2.2 Component Stresses

A comprehensive analysis of the component stresses, depending on the employed modulation strategy, is performed in this section. A sinusoidal motor current $i_{\mathrm{m,a}}(t) = \hat{I}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t - \phi)$, lagging the motor voltage $u_{\mathrm{m,a}}(t) = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t)$ by a phase angle ϕ is assumed [55], i.e. non-unity power factor $\cos(\phi) < 1$.

2.2.1 DC CM Injection Modulation (DCCMM)

First, the RMS current ripple stress on the filter inductor L_{o} is analytically derived. The local RMS current ripple of **(2.9)** is integrated over the fundamental period T_{m} in order to derive the global (total) RMS current ripple

$$\Delta I_{\mathrm{L_o,RMS}} = \frac{U_{\mathrm{i}}}{8\sqrt{3} L_{\mathrm{o}} f_{\mathrm{s}}} \sqrt{\frac{1}{\pi} \int_0^{\pi} \left[(1 + d_{\mathrm{a}}(\theta))(1 - d_{\mathrm{a}}(\theta))\right]^2 d\theta}. \tag{2.19}$$

The resulting global RMS current ripple for DCCCM is

$$\Delta I_{\mathrm{L_o,RMS}} = \frac{U_{\mathrm{i}}}{8\sqrt{3} L_{\mathrm{o}} f_{\mathrm{s}}} \sqrt{\frac{3}{8} M_1^4 + M_1^2 (3M_0^2 - 1) + (M_0^2 - 1)^2}. \tag{2.20}$$

The RMS current ripple is a function of both the modulation index M_1 and the CM modulation parameter M_0, as is illustrated in **Fig. 2.6(a)**. The modulation parameter M_0 values represents a degree of freedom: For a given modulation index M_1, the parameter $M_0(M_1)$ should be selected such that the inductor RMS current ripple of **(2.20)** is minimized. It is reminded that the parameter M_0 is subject to the linear constraints of **(2.13)**. By selecting

$$M_{0,\text{opt}}(M_1) = 1 - M_1, \tag{2.21}$$

the minimum current ripple stress on the filter inductor is achieved. Therefore, it is optimal to select the maximum possible CM offset M_0 in order to minimize the current ripple of the filter inductor. The optimal selection $M_{0,\text{opt}}$ of the CM parameter M_0 is highlighted on **Fig. 2.6(a)**. For the example case of modulation index $M_1 = 0.2$ shown in **Fig. 2.4**, the parameter value M_0 is constrained in the interval $-0.8...+0.8$. From this M_0 interval, the parameter value $M_0 = 0.8$ yields the lowest RMS current ripple and thus should be selected. It is noted that the DCCMM is symmetric. That is, identical performance is attained, in terms of inductor RMS current ripple **(2.20)**, by using a positive parameter value $+M_0$ (in the considered example $M_0 = +0.8$) or a negative parameter value $-M_0$ (in the considered example $M_0 = -0.8$). By selecting the CM parameter M_0 according to **(2.21)** the optimum version of DCCMM is derived, that minimizes the inductor current ripple/losses.

Only the optimized DCCMM, highlighted in **Fig. 2.4(a)**, is from now on considered. The current ripple for the optimized DCCMM modulation is compared against the conventional sinusoidal modulation (SM) in **Fig. 2.7(a)**. The DCCMM reduces the inductor RMS current ripple compared to SM, over the whole modulation index M_1 range.

The RMS current stress on the semiconductor devices is now analytically derived. The local (instantaneous) RMS current of the low-side and high-side switches of phase-leg a are

$$i_{\text{Ta1,RMS}}(t) = \sqrt{\frac{1+d_{\text{a}}(t)}{2}}\, i_{\text{m,a}}(t), \quad i_{\text{Ta2,RMS}}(t) = \sqrt{\frac{1-d_{\text{a}}(t)}{2}}\, i_{\text{m,a}}(t). \tag{2.22}$$

In order to calculate the global (total) RMS current that is conducted by the semiconductor devices, an integration of **(2.22)** must be performed over the fundamental period T_{m}

$$I_{\text{T,RMS}} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{\text{T,RMS}}(\theta)^2 d\theta}. \tag{2.23}$$

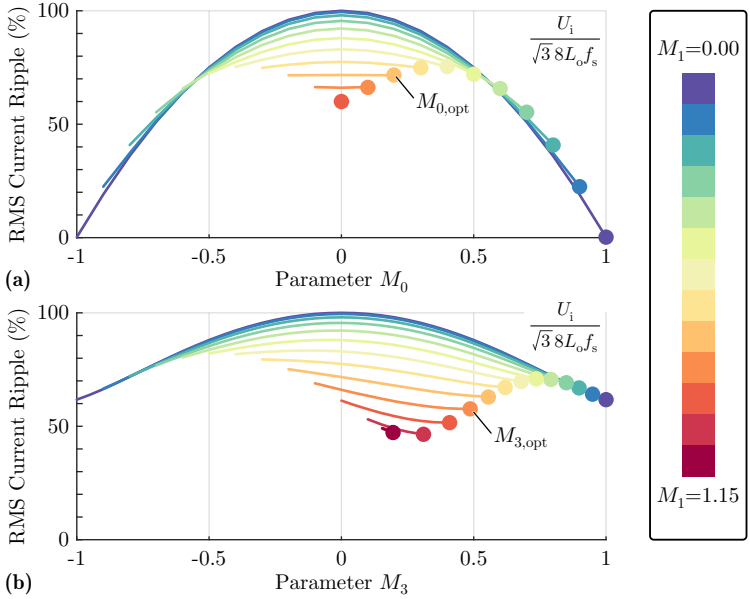


Fig. 2.6: RMS current ripple of the filter inductor L_o for **(a)** DCCMM and **(b)** ACCMM modulation strategies. The RMS current ripple is normalized with respect to the value $\frac{U_i}{8\sqrt{3}L_o f_s}$ of **(2.10)**. The current ripple depends on the modulation index M_1 and the CM injection parameter M_0/M_3. The optimal value of the CM injection parameter $M_{0,opt}/M_{3,opt}$, that minimizes the current ripple is highlighted.

The resulting semiconductor devices' RMS currents for DCCMM are plotted in **Fig. 2.7(b)** and are

$$I_{Ta1,RMS} = \frac{\hat{I}_m}{\sqrt{2}}\sqrt{\frac{1-M_0}{2}}, \quad I_{Ta2,RMS} = \frac{\hat{I}_m}{\sqrt{2}}\sqrt{\frac{1+M_0}{2}}. \tag{2.24}$$

The low-side switch $T_{a,2}$ conducts a higher RMS current compared to the high-side switch $T_{a,1}$. When the modulation index M_1 is low, and the injection parameter values M_0 are larger, then the current asymmetry becomes more pronounced. Because of the CM injection $d_{CM} = -M_0$, the duty cycles of all three phases are shifted downwards, therefore the relative on-time of the low-side switch $T_{a,2}$ is longer than the corresponding on-time of the high-side switch $T_{a,1}$. Hence, a higher RMS current stress and higher losses are caused on the low-side switches. For the example of **Fig. 2.4**, where the

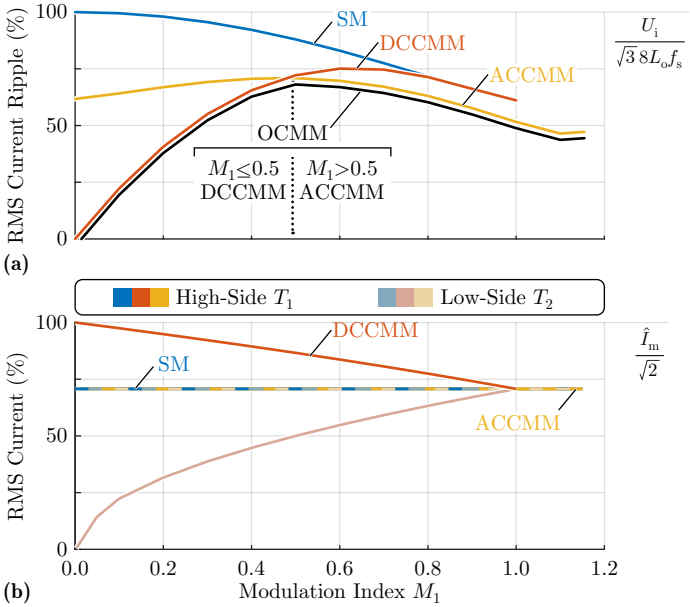


Fig. 2.7: Stresses on the inverter components for different modulation strategies: (blue) SM, (orange) DCCMM and (yellow) ACCMM. **(a)** RMS current ripple of the filter inductor L_o, normalized with respect to the value $\frac{U_i}{8\sqrt{3}L_o f_s}$ of **(2.10)**. **(b)** RMS current of the semiconductor devices, normalized with respect to the motor RMS current $\hat{I}_m/\sqrt{2}$.

modulation index is $M_1 = 0.2$ and the CM injection parameter is $M_0 = 0.8$, the low-side switch $T_{a,2}$ conducts approximately three times higher RMS current compared to the high-side switch $T_{a,1}$. Therefore, the current rating of the low-side switches should be carefully selected in order to ensure that the inverter can provide the needed motor current/torque for low modulation indexes. As the modulation index M_1 increases (and the parameter M_0 is accordingly reduced) the current sharing among the semiconductor devices becomes more symmetric. The component stresses caused by DCCMM are summarized in **Tab. 2.3**.

2.2.2 AC CM Injection Modulation (ACCMM)

The filter inductor L_o RMS current ripple is first derived. The local RMS current ripple is integrated over the fundamental period T_m according to **(2.19)**, resulting in the global RMS current ripple

$$\Delta I_{L_o,RMS} = \frac{U_i}{8\sqrt{3}L_o f_s}\sqrt{\frac{3}{8}M_1^4 - \frac{1}{2}M_1^3 M_3 + \frac{1}{4}(6M_1^2 - 4)M_3^2 - M_1^2 + \frac{3}{8}M_3^3 + 1.} \tag{2.25}$$

The RMS current ripple is a function of both the modulation index M_1 and the CM injection parameter M_3, as is illustrated in **Fig. 2.6(b)**. Similarly to the DCCMM, the modulation parameter M_3 value represents a degree of freedom: For a given modulation index M_1 the parameter $M_3(M_1)$ should be selected such that the inductor RMS current ripple of **(2.25)** is minimized. It is reminded that the parameter M_3 is subject to the linear constraints of **(2.17)**. By selecting

$$M_{3,opt}(M_1) = M_{3,max}(M_1), \tag{2.26}$$

where $M_{3,max}(M_1)$ is given in **(2.18)**, the minimum current ripple stress on the filter inductor is achieved. Therefore, it is optimal to select the maximum third harmonic amplitude in order to minimize the inductor current ripple. The optimal selection $M_{3,opt}(M_1)$ of the CM parameter M_3 is highlighted in **Fig. 2.6(b)**. For the example case of modulation index $M_1 = 0.2$ shown in **Fig. 2.5**, the parameter value M_3 is constrained in the interval $-0.8... + 0.9$. From this feasible interval, the parameter value $M_3 = 0.9$ yields the lowest RMS current ripple and thus is selected. It is noted that the ACCMM is not symmetric. That is, different current ripple is attained by using a positive parameter value $+M_3$ (in the considered example $M_3 = +0.8$) or a negative parameter value $-M_3$ (in the considered example $M_3 = -0.8$). By selecting the CM parameter M_3 according to **(2.26)** the optimum version of ACCMM is derived, that minimizes the inductor current ripple/losses. From now on, only the optimized ACCMM, highlighted in **Fig. 2.5(a)**, is considered. The current ripple for the optimized ACCMM modulation is compared against the conventional sinusoidal modulation (SM) in **Fig. 2.7(a)**. The ACCMM reduces the inductor RMS current ripple compared to SM, over the whole modulation index M_1 range. A key feature of the ACCMM is that it can be used in the overmodulation region $M_1 = 1...2/\sqrt{3}$, in contrast to the DCCMM.

The RMS current stress on the semiconductor devices is now analytically derived. In order to calculate the total RMS current that is conducted by the

semiconductor devices, an integration of the local RMS current must be performed according to **(2.23)**. The resulting RMS current stresses for ACCMM modulation are plotted in **Fig. 2.7(b)** and are

$$I_{\mathrm{Ta1,RMS}} = I_{\mathrm{Ta2,RMS}} = \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}} \frac{1}{\sqrt{2}}. \tag{2.27}$$

In the case of ACCMM, the current is symmetrically/equally distributed among the high-side switch T_{a1} and the low-side switch T_{a2}. This symmetric current distribution is an advantage of ACCMM compared to DCCMM, where the current stress on the semiconductor devices is asymmetric. The component stresses caused by ACCMM are summarized in **Tab. 2.3**.

2.2.3 Remaining Component Stresses

The overall semiconductor losses are roughly unaffected from the employed modulation strategy. Namely, the switching losses are similar for SM, DCCMM and ACCMM, since the same total number of switching transitions occurs, independent of the modulation strategy. The conduction losses are also independent of the modulation strategy and equal to

$$P_{\mathrm{cd}} = 3 \frac{\hat{I}_{\mathrm{m}}^2}{2} R_{\mathrm{T,on}}, \tag{2.28}$$

where $R_{\mathrm{T,on}}$ is the on-state resistance of each (unipolar) power semiconductor device. In the above conduction losses calculation the inductor current ripple is neglected. It is noted, that the asymmetric RMS current of the semiconductor devices in the case of DCCMM **(2.24)**, does not affect the total conduction losses, which are the same as in the case of SM or ACCMM.

The input capacitor C_{i} conducts the switched input current of the inverter $i_{\mathrm{i}}(t)$ (cf. **Fig. 2.1**), which in return causes losses due to the capacitor equivalent series resistance (ESR). This is a main concern particularly in the case of aluminium electrolytic capacitors, where high losses lead to high temperature that could reduce the capacitor lifetime. A simple expression relating the capacitor RMS current with the modulation index M_1 and the load power factor $\cos(\phi)$ is given in [63]

$$I_{\mathrm{C_i,RMS}} = \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}} \sqrt{2M_1 \left[\frac{\sqrt{3}}{4\pi} + \cos^2(\phi) \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M_1 \right) \right]}, \tag{2.29}$$

and is independent of the applied inverter modulation strategy. This analytic approximation assumes sinusoidal inverter output currents and thus

Tab. 2.2: Characteristic waveforms of SM, DCCMM and ACCMM modulation strategies.

	d_a	OP Range	Optimum Parameter
SM	$M_1 \cos(\omega_\mathrm{m} t)$	$M_1 = 0...1$	-
DCCMM	$M_1 \cos(\omega_\mathrm{m} t) - M_0$	$M_1 = 0...1$	$M_{0,\mathrm{opt}}(M_1) = 1 - M_1$
ACCMM	$M_1 \cos(\omega_\mathrm{m} t) - M_3 \cos(3\omega_\mathrm{m} t)$	$M_1 = 0...2/\sqrt{3}$	$M_{3,\mathrm{opt}}(M_1) = M_{3,\mathrm{max}}(M_1)$ **(2.18)**

Tab. 2.3: Component stresses summary, calculated for SM, DCCMM and ACCMM modulation strategies.

	$\Delta I_{\mathrm{L_o,RMS}}$	$I_{\mathrm{T1,RMS}}$	$I_{\mathrm{T2,RMS}}$
SM	$\frac{U_\mathrm{i}}{8\sqrt{3}L_\mathrm{o}f_\mathrm{s}}\sqrt{\frac{3}{8}M_1^4 - M_1^2 + 1}$	$\frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\frac{1}{\sqrt{2}}$	$\frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\frac{1}{\sqrt{2}}$
DCCMM	$\frac{U_\mathrm{i}}{8\sqrt{3}L_\mathrm{o}f_\mathrm{s}}\sqrt{\frac{3}{8}M_1^4 + M_1^2(3M_0^2 - 1) + (M_0^2 - 1)^2}$	$\frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\sqrt{\frac{1-M_0}{2}}$	$\frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\sqrt{\frac{1+M_0}{2}}$
ACCMM	$\frac{U_\mathrm{i}}{8\sqrt{3}L_\mathrm{o}f_\mathrm{s}}\sqrt{\frac{3}{8}M_1^4 - \frac{1}{2}M_1^3M_3 + \frac{1}{4}(6M_1^2 - 4)M_3^2 - M_1^2 + \frac{3}{8}M_3^3 + 1}$	$\frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\frac{1}{\sqrt{2}}$	$\frac{\hat{I}_\mathrm{m}}{\sqrt{2}}\frac{1}{\sqrt{2}}$

neglects the marginal increase of the input capacitor current stress caused by the output current ripple (up to 8% - [63]).

In the case of ACCMM, a circulating CM current with an amplitude $\hat{I}_{\mathrm{C_o},3} = \frac{3}{2} M_3 U_\mathrm{i} 3\omega_\mathrm{m} C_\mathrm{o}$ and a repetition frequency $3f_\mathrm{m}$ flows through the filter capacitors C_o according to **(2.14)**. This circulating CM current forms a return path through the input capacitor C_i, hence further increases the current stress on the input capacitor. However, the CM circulating current $\hat{I}_{\mathrm{C_o},3}$ is usually very small. A small capacitance value C_o is typically selected for high-speed drives in order to minimize the reactive phase current (fundamental frequency) $\hat{I}_{\mathrm{C_o},1} = \frac{1}{2} M_1 U_\mathrm{i} \omega_\mathrm{m} C_\mathrm{o} \leq 0.3\hat{I}_\mathrm{m}$. This small capacitance value, inherently also limits the circulating CM current $\hat{I}_{\mathrm{C_o},3}$. Therefore, the effect of the circulating CM current $\hat{I}_{\mathrm{C_o},3}$ can be disregarded. Accordingly, the analytic expression **(2.29)** can be used for the input capacitor design and loss estimation, when any of the discussed modulation schemes (SM, DCCMM or ACCMM) is employed.

2.2.4 Optimal CM Modulation (OCMM)

The two proposed modulation strategies, DCCCM and ACCMM, are now compared. According to **Fig. 2.7(a)**, DCCMM achieves a lower inductor current ripple compared to ACCMM, when the modulation index is low $M_1 = 0...0.5$. The opposite is true for high modulation indexes $M_1 = 0.5...1$, where ACCMM yields lower current ripple. Furthermore, only ACCMM can be used in the overmodulation region of $M_1 = 1...2/\sqrt{3}$. Therefore, it is preferable to use DCCMM for low modulation indexes $M_1 = 0...0.5$ and ACCMM for high modulation indexes $M_1 = 0.5...2/\sqrt{3}$. Both proposed modulation strategies result in a lower overall inductor current ripple compared to the conventional SM, as highlighted in **Fig. 2.7(a)**.

A combination of the two proposed modulation strategies is now investigated. In this case, the injected CM duty cycle is $d_\mathrm{CM}(t) = -M_0 - M_3 \cos(3\omega_\mathrm{m} t)$, resulting in a phase a duty cycle

$$d_\mathrm{a}(t) = M_1 \cos(\omega_\mathrm{m} t) - M_0 - M_3 \cos(3\omega_\mathrm{m} t), \tag{2.30}$$

and a phase a output voltage

$$u_{\mathrm{a\bar{o}}}(t) = M_1 \frac{U_\mathrm{i}}{2} \cos(\omega_\mathrm{m} t) - M_0 \frac{U_\mathrm{i}}{2} - M_3 \frac{U_\mathrm{i}}{2} \cos(3\omega_\mathrm{m} t). \tag{2.31}$$

The results reveal that merging the two modulation strategies (i.e. simultaneously $M_0 \neq 0$ and $M_3 \neq 0$) does not further reduce the filter inductor L_o

current ripple. Instead, for low modulation indexes $M_1 = 0...0.5$ the exclusive utilization of DCCMM (i.e. $M_0(M_1) = 1 - M_1$, $M_3 = 0$) allows for the lowest current ripple, while for high modulation indexes $M_1 = 0.5...2/\sqrt{3}$ the ACCMM is more effective (i.e. $M_0 = 0$, $M_3(M_1) = M_{3,\max}(M_1)$). The modulation scheme that transitions from DCCMM (below $M_1 = 0.5$) to ACCMM (above $M_1 = 0.5$) constitutes the optimal CM injection modulation (OCMM) and is depicted in **Fig. 2.7(a)**. The OCMM minimizes the inductor current ripple/losses over the whole inverter operating range $M_1 = 0...2/\sqrt{3}$.

Special attention is required for the transition from DCCMM to ACCMM. At the transition point $M_1 = 0.5$, the parameter M_0 must be decreased while the parameter M_3 must be increased. In the case of a step transition, the CM injection parameters would have to abruptly change from $[M_0 = 0.5, M_3 = 0]$ (below $M_1 = 0.5$) to $[M_0 = 0, M_3 = 0.74]$ (above $M_1 = 0.5$). Such an abrupt transition could cause unwanted transients in the FSF, hence should be avoided. Instead, a smooth transition is proposed, according to which the values of M_0 and M_3 are gradually adjusted. The transition from DCCCM to ACCMM occurs within a transition interval $M_1 = 0.4...0.6$, around the transition point $M_1 = 0.5$. The parameter M_0 is linearly decreased with respect to M_1, from $M_0 = 0.6$ at $M_1 = 0.4$, to $M_0 = 0$ at $M_1 = 0.6$. At the same time, the parameter M_3 is linearly increased from $M_3 = 0$ at $M_1 = 0.4$, to $M_3 = 0.74$ at $M_1 = 0.6$. The proposed smooth transition ensures an uninterrupted inverter operation, and that all the three-phase duty cycles remain within the carrier limits. However, the smooth transition causes marginally higher current ripple in the transition interval $M_1 = 0.4...0.6$, since the selection of M_0 and M_3 in this interval is suboptimal.

2.3 Experimental Validation

In order to validate the claimed performance benefits derived from the proposed modulation strategies, a hardware prototype is purposely assembled. A high-speed motor drive application, with the specifications of **Tab. 2.1**, is considered. The drive system at hand, features a nominal inverter power of $P = 330\,\mathrm{W}$, a motor rotational motor speed of $n = 400\,\mathrm{krpm}$ and is visualized in **Fig. 2.8(a)**. The test setup comprises the two-level VSI of **Fig. 2.8(b)**, which employs the latest generation of GaN semiconductor devices and an FSF (cf. **Fig. 2.1**). The inverter drives the high-speed permanent magnet motor (PMSM) of **Fig. 2.8(c)**. It is noted that the motor features a two-pole slotless design. This motor design allows for high mechanical rigidity able to withstand the mechanical forces, related to the high rotational speed. Si-

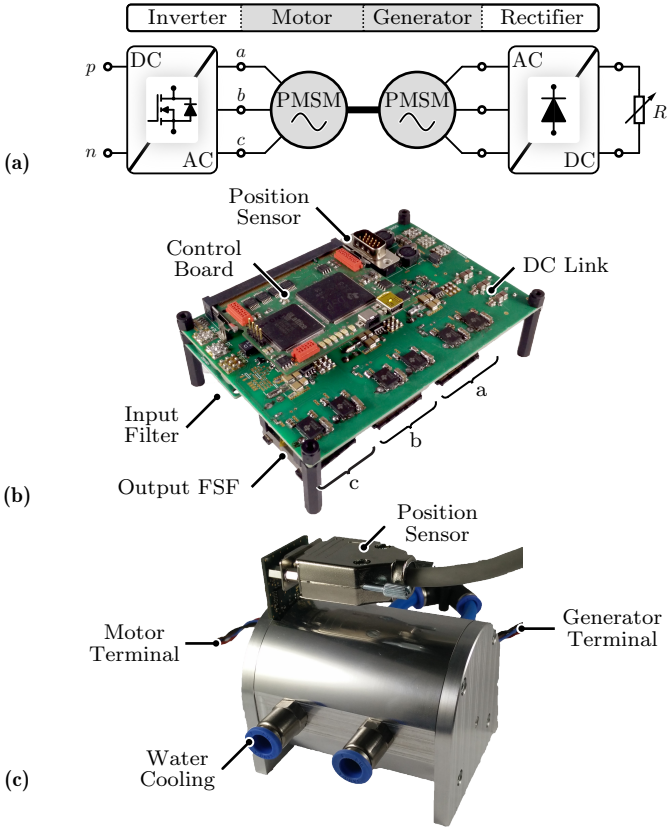


Fig. 2.8: **(a)** High-speed motor drive test setup employed for the experimental verification. **(b)** Inverter hardware prototype and **(c)** high-speed motor/generator test bench.

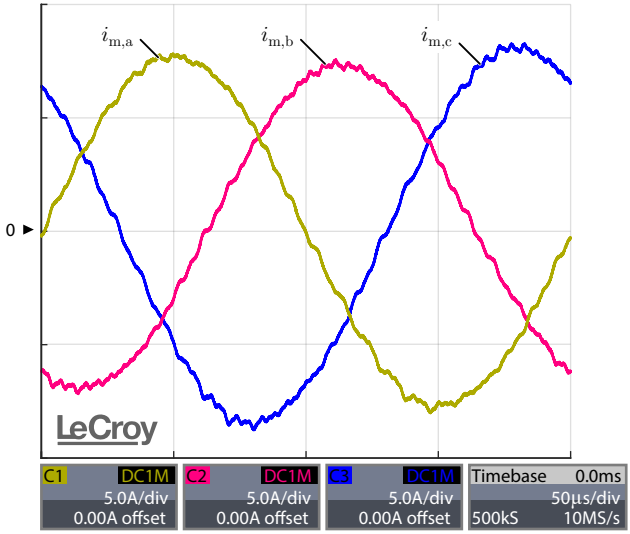


Fig. 2.9: Measured motor currents under a motor speed of $n = 300$ krpm and a motor power of $P = 300$ W. The slight imbalance of the phase currents originates from asymmetries in the motor windings.

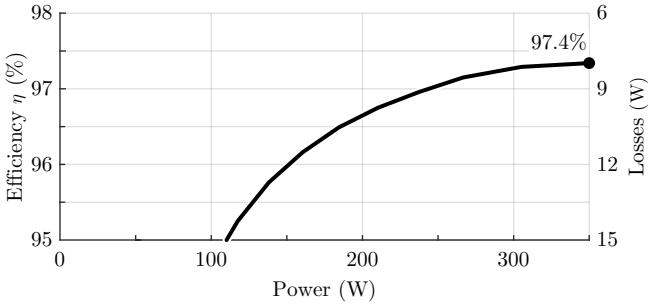


Fig. 2.10: Inverter efficiency curve for sinusoidal modulation (SM).

multaneously, this motor design inherently results in a low motor leakage inductance [22, 64], which in return necessitates the use of an FSF between the inverter and the motor. The motor hardware prototype is built in a back-to-back (B2B) configuration. That is, the motor is connected through a shaft to an identical generator (back-to-back). Subsequently, the generator is connected to a three-phase diode rectifier, as is illustrated in **Fig. 2.8(a)**. Finally, the diode rectifier is connected to an adjustable DC load. Thereby, the torque and the speed of the motor can be adjusted independently, offering maximum testing flexibility. A cascaded speed-torque controller in dq-axis reference frame is implemented using a digital signal processor (DSP), in order to drive the motor. A Hall sensor board, that is directly mounted on the motor, provides the motor position angle ε and speed ω. The conventional SM is initially employed in order to commission the inverter-motor test setup. The measured motor currents under nominal motor speed and power are plotted in **Fig. 2.9** and are sinusoidal. It is noted, that the motor currents are slightly asymmetric, due to winding manufacturing imperfections in the stator. The measured efficiency curve of the inverter is given in **Fig. 2.10**, where a nominal inverter efficiency of 97.4% is achieved.

In a next step, the two proposed modulation strategies, DCCMM and ACCMM, are implemented. Depending on the applied modulation depth M_1, the optimal injection parameter $M_{0,\mathrm{opt}}(M_1)$ **(2.21)** must be selected for DCCMM, or the parameter $M_{3,\mathrm{opt}}(M_1)$ **(2.26)** must be selected for ACCMM. For this reason, the optimal values of the CM injection parameters $M_{0,\mathrm{opt}}(M_1)$ and $M_{3,\mathrm{opt}}(M_1)$, are stored in a look-up table within the DSP memory and are accessed seamlessly during system operation. Experimentally measured waveforms of the filter inductor current, for SM, DCCMM and ACCMM, are plotted in **Fig. 2.11**. There, a modulation index of $M_1 = 0.2$, a motor speed of $n = 60\,\mathrm{krpm}$ (i.e. fundamental frequency $f_\mathrm{m} = 1\,\mathrm{kHz}$) and the nominal motor current $\hat{I}_\mathrm{m} = 10\,\mathrm{A}$ (i.e. nominal motor torque) are used. It is shown in **Fig. 2.11**, that both DCCMM and ACCMM reduce the overall inductor current ripple, compared to SM. In **Fig. 2.12** the RMS current ripple $\Delta I_{\mathrm{L_o,RMS}}$ of the filter inductor is experimentally measured and compared against the analytically calculated values of **Tab. 2.3** and **Fig. 2.7(a)**. An excellent matching between the analytic calculations and the experimental measurements is observed. Finally, the inverter losses are measured in the operating range $P = 0\mathrm{W}...330\mathrm{W}$ for the different modulation strategies. The achieved loss reduction by employing DCCMM or ACCMM, compared to the conventional SM, is shown in **Fig. 2.13**. The loss reduction, which originates from the minimization of the inductor RMS current ripple, is especially visible for low

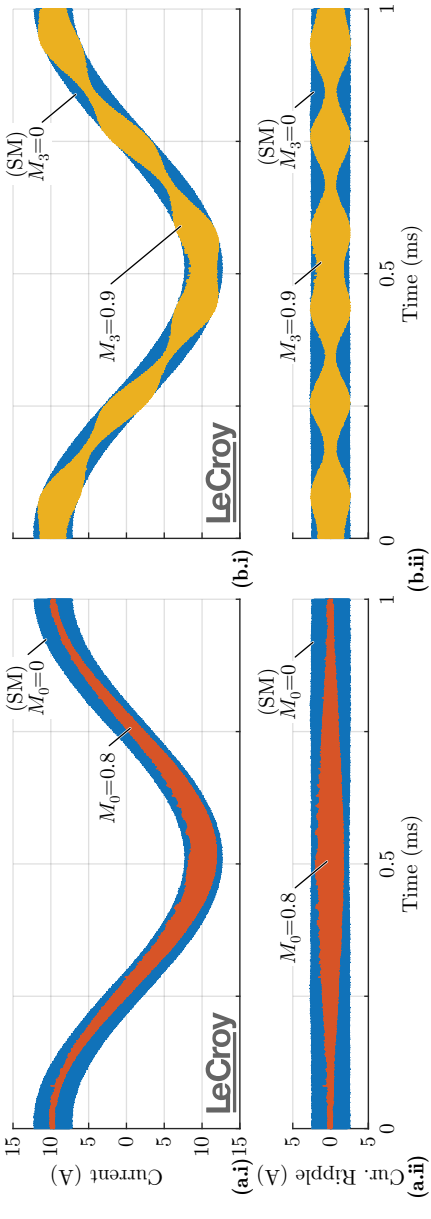


Fig. 2.11: Measured current waveforms for **(a)** DCCMM and **(b)** ACCMM. **(i)** Current and **(ii)** current ripple of the filter inductor L_o. The waveforms are recorded for a fundamental motor frequency of f_m = 1 kHz, and a modulation index of M_1 = 0.2.

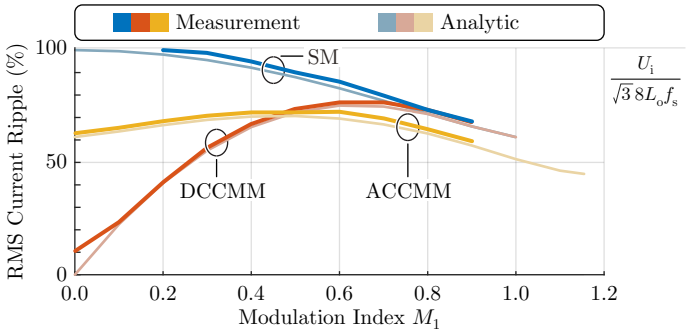


Fig. 2.12: Measured inductor RMS current ripple $\Delta I_{L_o,RMS}$, compared against the theoretically calculated values of **Fig. 2.7(a)**.

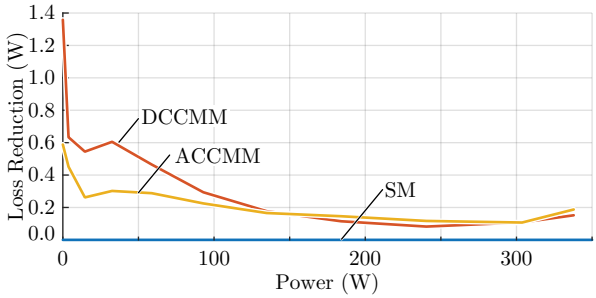


Fig. 2.13: Loss reduction achieved by the DCCMM and ACCMM modulation strategies, compared to the conventional SM.

modulation indexes M_1. This is expected, since for low modulation indexes, where a wider range of CM injection parameters M_0 or M_3 is available (cf. **Fig. 2.4** and **Fig. 2.5**, respectively), the DCCMM and ACCMM are more effective. In the best case, a reduction of the converter losses by $\simeq 1\,\mathrm{W}$ with respect to the nominal converter losses of 9 W is achieved, i.e. 11% loss reduction.

2.4 Summary

Two-level voltage source inverters (VSIs) are typically employed in high-speed low-voltage drive applications. A full sine-wave output filter (FSF) is placed at the VSI AC output-side, in order to ensure high-quality motor voltages (cf. **Fig. 2.1**). As a result of the FSF, the inverter suffers from a decrease

in efficiency, because of the additional losses occurring within the output filter. The main driver of losses within the FSF are the inductors that conduct a high current ripple. The inductors' current ripple/losses can be reduced by means of an appropriate modulation strategy. However, the unique characteristics of an FSF, with respect to the inductor current ripple formation, render conventional modulation strategies ineffective.

In order to address this problem, the degrees of freedom in the modulation of a VSI, followed by an FSF, are revisited. It is deduced that the main degree of freedom, when selecting a modulation strategy, is the injection of a CM duty cycle pattern $d_{\mathrm{CM}}(t)$ to all three phases. Two new modulation strategies are proposed in this chapter:

(i) DC CM injection (DCCMM), where a constant (DC) CM duty cycle is injected into all three phases.

(ii) AC CM injection (ACCMM), where a time varying (AC) CM duty cycle is injected into all three phases.

The two modulation strategies are summarized in **Tab. 2.2**. Subsequently, the stresses on the inverter components are analytically derived for both modulation strategies and summarized in **Tab. 2.3**. It is shown that both DCCMM and ACCMM significantly reduce the current ripple of the filter inductors, compared to a conventional sinusoidal modulation (SM). In particular, for low modulation indexes $M_1 = 0...0.5$ the DCCMM is more effective, while for high modulation indexes $M_1 = 0.5...2/\sqrt{3}$ the ACCMM yields superior performance.

Finally, the proposed modulation strategies are applied on a purposely assembled motor drive system, which includes a $n = 400\,\mathrm{krpm}$ motor and a $P = 330\,\mathrm{W}$ inverter. There, it is shown that the DCCMM and ACCMM reduce the inductor current ripple and the related losses. A loss reduction of up to 11% is measured, compared to a standard sinusoidal modulation (SM).

3

Voltage Source Inverter - Electromagnetic Compatibility

This chapter summarizes the key research findings also presented in:

M. Antivachis, P. Niklaus, D. Bortis, and J. W. Kolar, "Input / output EMI filter design for three-phase ultra-high speed motor drive GaN inverter stage" *CPSS Transactions on Power Electronics and Applications*, 2020, early access. .

Motivation

Electromagnetic compatibility is a main concern in modern motor drives. Wide-bandgap (WBG) inverters cause high EMI emissions, that can damage the motor and disturb nearby equipment. This chapter details the necessary measures, needed in order to mitigate the EMI emissions of a WBG inverter.

Executive Summary

Pairing wide-bandgap (WBG) inverters with high-speed motors results in compact and efficient motor drives, but requires special attention on electromagnetic interference (EMI) aspects. This chapter focuses on electromagnetic compatibility (EMC) of high-speed motor drives, supplied by a DC source. In order to protect the nearby equipment from the EMI noise of the WBG inverter, a filter that complies with conducted EMI regulations is placed at the inverter DC input-side. However, there is no clear mandate requiring from inverters to comply with conducted EMI regulations at the AC output-side, where only the motor is placed. For this reason, there is no full consensus whether it is necessary to use an output filter, and if so, what type of output filter would be suitable, i.e. if a differential-mode (DM), common-mode (CM) or both DM/CM output filter would fit best. A full sine-wave output filter (FSF) is proposed in this chapter, that features both DM and CM attenuation, and capacitors connected to the DC link. Besides the several well established benefits of an FSF, such as purely sinusoidal motor currents and the protection of the motor against high du/dt originating from the fast switching of the semiconductor devices, an FSF at the inverter output-side, also reduces the CM EMI emissions at the inverter input-side. Namely, since the inverter housing, the motor housing and the interconnecting shielded cable are all grounded, CM emissions generated at the inverter output-side are directly mapped to the inverter input-side, i.e. there is an input-to-output CM noise interrelation. An FSF reduces the output-side CM EMI emissions and thus mitigates the input-to-output CM noise mutual influence. Two types of full sine-wave output filters (c-FSF and d-FSF) are comparatively evaluated, in terms of volume, losses and EMI performance. The theoretical consideration are tested within the context of a high-speed 280 krpm, 1 kW motor drive, with 80V DC supply. The experimental results validate the good performance of the proposed filter concept.

Nomenclature

$u_{\bar{a}\bar{o},\mathrm{DM}}\vert_{f_\mathrm{m}}$	Switch-node $\bar{a}$ low-frequency DM voltage component (fundamental motor operation)
$u_{\bar{a}\bar{o},\mathrm{DM}}\vert_{f_\mathrm{s}}$	Switch-node $\bar{a}$ high-frequency DM voltage component (output DM EMI noise source)
$u_{\bar{i}\bar{o},\mathrm{CM}}\vert_{f_\mathrm{m}}$	Switch-node $\bar{i} \in \{\bar{a}, \bar{b}, \bar{c}\}$ low-frequency CM voltage component (third harmonic injection)
$u_{\bar{i}\bar{o},\mathrm{CM}}\vert_{f_\mathrm{s}}$	Switch-node $\bar{i} \in \{\bar{a}, \bar{b}, \bar{c}\}$ high-frequency CM voltage component (output CM EMI noise source)
$u_{\mathrm{ao},\mathrm{DM}}\vert_{f_\mathrm{s}}$	Inverter output terminal a high-frequency DM voltage
$u_{\mathrm{io},\mathrm{CM}}\vert_{f_\mathrm{s}}$	Inverter output terminal $i \in \{a, b, c\}$ high-frequency CM voltage
$u_{\bar{\mathrm{p}}\bar{\mathrm{n}},\mathrm{DM}}\vert_{\mathrm{fs}}$	Inverter input DM EMI noise source
$u_{\bar{\mathrm{p}}\bar{\mathrm{n}},\mathrm{CM}}\vert_{\mathrm{fs}}$	Inverter input CM EMI noise source
$u_{\mathrm{pn},\mathrm{DM}}\vert_{\mathrm{fs}}$	Inverter input terminal p, n DM EMI noise
$u_{\mathrm{pn},\mathrm{CM}}\vert_{\mathrm{fs}}$	Inverter input terminal p, n CM EMI noise
$i_{\bar{\mathrm{p}}}$	Inverter DC link switched current
I_p	Inverter input terminal p DC current
$A_\mathrm{DM}\vert_\mathrm{DMF}$	DM attenuation of the output DMF
$A_\mathrm{CM}\vert_\mathrm{DMF}$	CM attenuation of the output DMF
$A_\mathrm{DM}\vert_\mathrm{c\text{-}FSF}$	DM attenuation of the output c-FSF
$A_\mathrm{CM}\vert_\mathrm{c\text{-}FSF}$	CM attenuation of the output c-FSF
$A_\mathrm{DM}\vert_\mathrm{d\text{-}FSF}$	DM attenuation of the output d-FSF
$A_\mathrm{CM}\vert_\mathrm{d\text{-}FSF}$	CM attenuation of the output d-FSF
A_DM	DM attenuation of the input filter
A_CM	CM attenuation of the input filter

Low-voltage, high-speed drive systems, supplied by an isolated DC network, spread across a wide range of commercial applications [16, 17]. A $P = 1\,\mathrm{kW}$, $n = 280\,\mathrm{krpm}$ compressor drive application is considered in this chapter, which is visualised in **Fig. 3.1** and summarized in **Tab. 3.1**. The inverter is connected to the high-speed motor through a shielded, four conductor cable (three phases and protective earth). The isolated DC network $U_\mathrm{pn} = 80\,\mathrm{V}$, which constitutes the primary energy source of the motor drive, simultaneously supplies sensitive surrounding equipment, which must be protected against EMI emissions originating from the switched inverter. Therefore, an input filter complying with EMC regulations IEC 61800-3 [42] is mandatory.

In contrast to the DC input filter, it is not clear whether a filter should be placed at the inverter AC output and if so what kind of filter and how

Tab. 3.1: Specifications of high-speed drive system. The nominal operating condition is highlighted in bold.

Motor speed	n	0 rpm...**280 krpm**
Motor voltage	$\hat{U}_\mathrm{m}$	0 V...**40 V** (phase, PK)
Motor power	P	0 W...**1000 W**
Inverter output freq.	f_m	0 kHz...**5 kHz**
Inverter input voltage	U_pn	80 V
Inverter power	P	0 W...**1100 W**

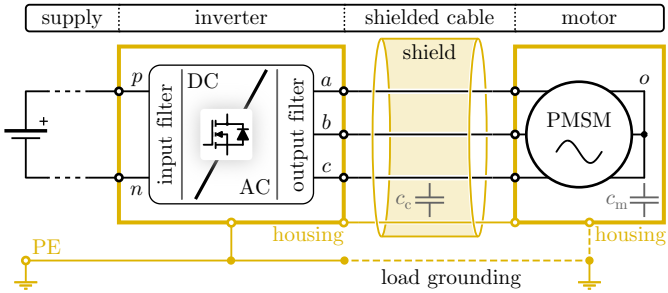


Fig. 3.1: High-speed motor drive system supplied by an isolated DC source. The motor can be either directly grounded (dashed yellow line applies) or only grounded through the shielded cable (dashed yellow line is not present).

strong its attenuation should be. A differential-mode output filter (DMF), as shown in **Fig. 3.2(a)**, is necessary when a high-speed motor is employed. High-speed motors are sensitive to poor current quality, which causes high rotor losses [21–23]. Thus, a DMF which allows for purely sinusoidal motor currents is required. Shifting towards higher rotational motor speeds n drastically decreases the volume of the motor and the rotating mechanical parts. Thereby, significantly higher motor power density is achieved that outweighs the decrease in inverter performance, due to the additional volume and losses originating from the DMF. In other words, a DMF allows to shift/exchange volume/losses from the motor towards the inverter, resulting in a better motor drive system performance as a whole. Furthermore, a DMF eliminates overvoltages at the motor terminals and wave reflections problems when long interface cables connect the inverter to the motor [65–67].

However, a DMF does not address the problem of common-mode (CM) EMI emissions. The high $\mathrm{d}u/\mathrm{d}t > 30\,\mathrm{kV/\mu s}$ that wide-bandgap (WBG) de-

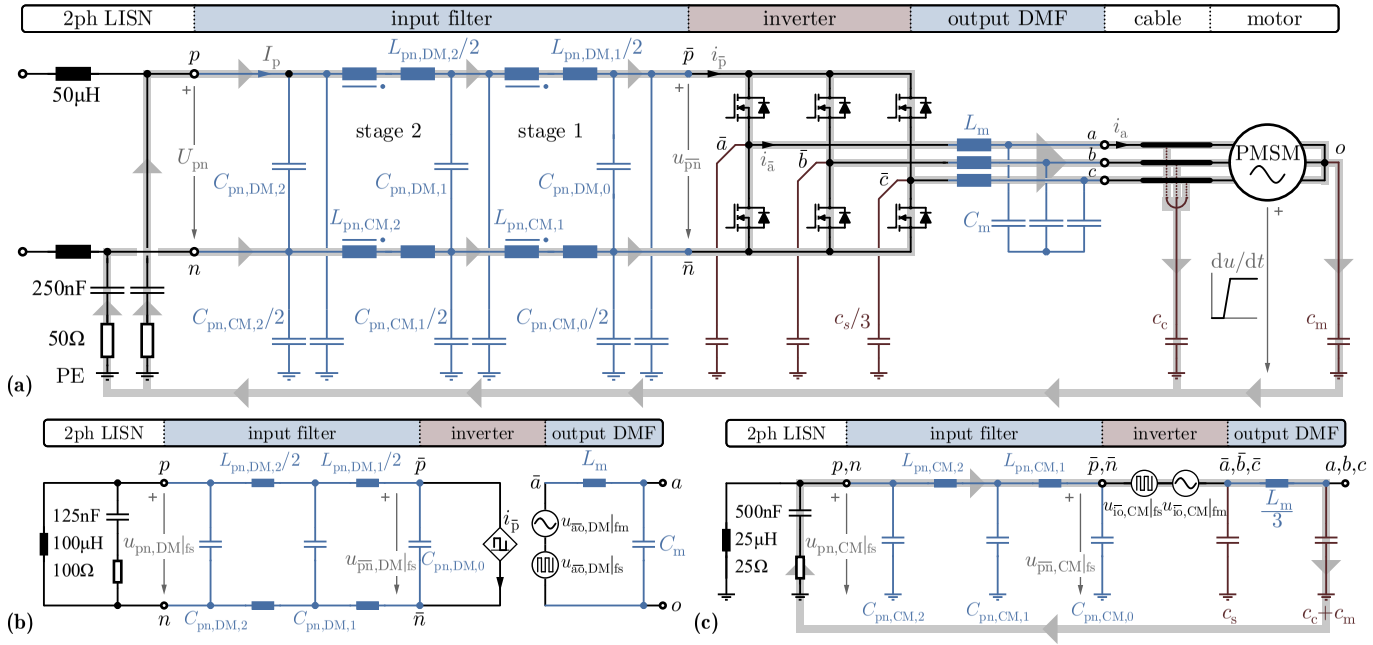


Fig. 3.2: **(a)** Inverter featuring a simple DM output filter (DMF) and a two-stage input filter. **(b)** DM and **(c)** CM equivalent circuits.

vices exhibit [25–27], enables low switching losses, but simultaneously electrically stresses the motor insulation and results in bearing currents [28–33]. As a result, high CM $\mathrm{d}u/\mathrm{d}t$ leads to premature motor failure. In order to guarantee high motor reliability, the DMF must be supplemented by a CM output filter (CMF), which mitigates high $\mathrm{d}u/\mathrm{d}t$. Another advantage of a CMF is described in literature: A CMF not only reduces the CM emissions at the AC output-side of the inverter, but also reduces the CM emissions at the DC input-side [68–72]. Namely, since the inverter housing, the motor housing and the interconnecting shielded cable are all grounded, CM emissions generated at the inverter output-side are directly mapped to the inverter input-side, i.e. there is an input-to-output CM noise interrelation. A CMF largely prevents CM emissions towards the inverter output and hence resolves the input-to-output CM noise interrelation problem.

For all the above reasons, a full sine-wave output filter (FSF), which features both DM and CM attenuation is recommended for WBG inverters. Three main categories of FSFs have been proposed in literature:

(i) DC link referenced output filter [34–40]. This is a passive output filter, which is capacitively connected/referenced to the negative/positive DC rails $\bar{p}/\bar{n}$. This type of output filter is analysed in detail within this chapter. In particular, two DC link referenced output filter variants, the c-FSF of **Fig. 3.4** and the d-FSF of **Fig. 3.5** are comparatively evaluated.

(ii) Passive CM noise cancellation output filter [73–76]. This type of filter offers similar performance to a DC link referenced filter but with additional complexity, hence it is not further considered in this work.

(iii) Active CM noise cancellation output filter [77,78]. This type of filter effectively reduces CM EMI emissions, by actively switching additional semiconductor devices. Thereby, significant switching losses are generated that compromise the inverter efficiency. For this reason, this output filter type is avoided.

First, the EMI emissions of the inverter, employing an FSF, are theoretically analysed in **Sec. 3.1**. Two FSF variants (c-FSF and d-FSF), are comparatively evaluated in terms of volume, losses and EMI performance. A comprehensive design algorithm for the input and output filter is given in **Sec. 3.2**. The experimental verification follows in **Sec. 3.3**, within the context of a 1 kW, 280 krpm, high-speed motor drive (cf. **Tab. 3.1**). The results verify the good performance of the proposed filter concept. Finally, a summary is given in **Sec. 3.4**.

3.1 Theoretical EMI Analysis

The considered two-level voltage source inverter employs a third harmonic injection modulation (THM) [56], in order to optimally utilize the DC link voltage. The duty cycles controlling the three phases are

$$\begin{aligned} d_{\mathrm{a}}(t) &= M\sin(\omega_{\mathrm{m}}t) - \frac{1}{6}\sin(3\omega_{\mathrm{m}}t) \\ d_{\mathrm{b}}(t) &= M\sin(\omega_{\mathrm{m}}t - \frac{2\pi}{3}) - \frac{1}{6}\sin(3\omega_{\mathrm{m}}t), \\ d_{\mathrm{c}}(t) &= M\sin(\omega_{\mathrm{m}}t + \frac{2\pi}{3}) - \frac{1}{6}\sin(3\omega_{\mathrm{m}}t) \end{aligned} \tag{3.1}$$

where M is the modulation index

$$M = \frac{\hat{U}_{\mathrm{m}}}{\frac{1}{2}U_{\mathrm{pn}}} = 0 \ldots \frac{2}{\sqrt{3}}, \tag{3.2}$$

and $\omega_{\mathrm{m}} = 2\pi f_{\mathrm{m}}$ is the motor angular velocity.

In order to facilitate the EMI analysis, the inverter switch-node $\bar{\mathrm{a}}$ $\bar{\mathrm{b}}$ and $\bar{\mathrm{c}}$ voltages are simplified into equivalent voltage sources [59] as illustrated in **Fig. 3.3**. The switch-node $\bar{a}$ voltage is analytically expressed as

$$u_{\bar{\mathrm{a}}\mathrm{o}}(t) = \underbrace{u_{\bar{\mathrm{a}}\mathrm{o},\mathrm{DM}}|_{f_{\mathrm{m}}} + u_{\bar{\mathrm{a}}\mathrm{o},\mathrm{DM}}|_{f_{\mathrm{s}}}}_{u_{\bar{\mathrm{a}}\mathrm{o},\mathrm{DM}}} + \underbrace{u_{\bar{\mathrm{i}}\mathrm{o},\mathrm{CM}}|_{f_{\mathrm{m}}} + u_{\bar{\mathrm{i}}\mathrm{o},\mathrm{CM}}|_{f_{\mathrm{s}}}}_{u_{\bar{\mathrm{i}}\mathrm{o},\mathrm{CM}}}. \tag{3.3}$$

From now on, the analysis focuses on phase a, however can be easily extended to the remaining two phases. In particular, the voltage component $u_{\bar{\mathrm{a}}\mathrm{o},\mathrm{DM}}|_{f_{\mathrm{m}}}$ of **(3.3)** is the fundamental frequency DM voltage, which generates the useful fundamental motor current/torque and depends on the modulation index

$$u_{\bar{\mathrm{a}}\mathrm{o},\mathrm{DM}}|_{f_{\mathrm{m}}}(t) = M\frac{U_{\mathrm{pn}}}{2}\sin(\omega_{\mathrm{m}}t). \tag{3.4}$$

The switch-node voltage component $u_{\bar{\mathrm{i}}\mathrm{o},\mathrm{CM}}|_{f_{\mathrm{m}}}$ is the low-frequency CM voltage and is the by-product of the employed THM modulation strategy

$$u_{\bar{\mathrm{i}}\mathrm{o},\mathrm{CM}}|_{f_{\mathrm{m}}}(t) = -\frac{U_{\mathrm{pn}}}{12}\sin(3\omega_{\mathrm{m}}t). \tag{3.5}$$

Finally, the $u_{\bar{\mathrm{a}}\mathrm{o},\mathrm{DM}}|_{f_{\mathrm{s}}}$ and $u_{\bar{\mathrm{i}}\mathrm{o},\mathrm{CM}}|_{f_{\mathrm{s}}}$ are the DM and CM high-frequency switch-node voltage components, respectively. Those voltage components are directly related to the PWM switching frequency f_{s} and are the cause behind

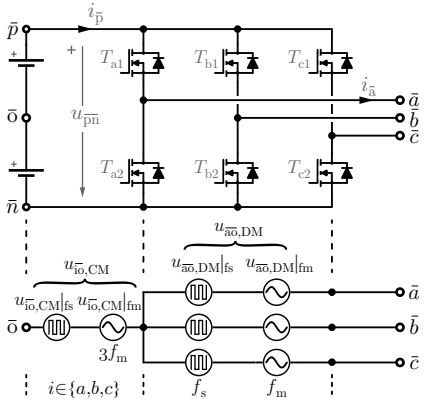


Fig. 3.3: Equivalent circuit of a two-level voltage source inverter.

EMI emissions. There is no closed form expression for the high-frequency switch-node voltage components $u_{\bar{a}\bar{o},DM}|_{f_s}(t)$ and $u_{\bar{i}\bar{o},CM}|_{f_s}(t)$ due to the complicated nature of the respective PWM waveforms. It is more convenient to analyse these voltage components in frequency domain. An upper bound of the high-frequency switch-node voltage components' spectrum is

$$\left[\hat{U}_{\bar{a}\bar{o},DM}|_{f_s}\right](nf_s) = \left[\hat{U}_{\bar{i}\bar{o},CM}|_{f_s}\right](nf_s) = \frac{2U_{pn}}{n\pi}, \tag{3.6}$$

where $n = 1, 3, 5\ldots$ is the harmonic order corresponding to the harmonic frequency $f = nf_s$. This spectrum is calculated by assuming a rectangular voltage waveform, with an amplitude $U_{pn}/2$, a 50% duty cycle and a repetition frequency equal to the switching frequency f_s. It is noted that the switch-node CM voltage components $u_{\bar{i}\bar{o},CM}|_{f_m}$ and $u_{\bar{i}\bar{o},CM}|_{f_s}$ are the same for all three phases $\bar{i} \in \{\bar{a}, \bar{b}, \bar{c}\}$.

3.1.1 Drawbacks of Differential-Mode Output Filter (DMF)

A simple DM output filter (DMF) is illustrated in **Fig. 3.2(a)**. There, the semiconductor devices, cable and motor parasitic impedances to protective earth (PE), are represented by the capacitors c_s, c_c and c_m, respectively. This capacitive representation is valid for frequencies ranging up to approximately 1 MHz [79]. In general, lower case notation, e.g. c_s, is used for parasitic elements. The semiconductor devices' parasitic capacitance c_s is low thanks

to the small packaging of the employed GaN semiconductor devices. In contrast, the cable/motor parasitic capacitances $c_c + c_m$ are significantly larger than c_s, due to the large physical dimensions of the cable and the motor housing.

The DMF generates sinusoidal currents for the high-speed motor. By employing the voltage source equivalent inverter model of **Fig. 3.3**, and applying the superposition technique, the DM equivalent circuit of the DMF is derived, in **Fig. 3.2(b)**. The DMF behaves as a second order filter with a DM attenuation

$$A_{DM}|_{DMF}(f) = \left| \frac{f_{r,DM}^2|_{DMF}}{f_{r,DM}^2|_{DMF} - f^2} \right|, \tag{3.7}$$

where f is the harmonic frequency and $f_{r,DM}|_{DMF}$ is the DM resonant frequency

$$f_m < f_{r,DM}|_{DMF} = \frac{1}{2\pi\sqrt{L_m C_m}} < f_s. \tag{3.8}$$

Only a small residual high-frequency DM voltage $u_{ao,DM}|_{f_s}$ appears at the inverter output terminal a with a spectrum

$$\hat{U}_{ao,DM}|_{f_s}(f) = A_{DM}|_{DMF} \cdot \hat{U}_{\bar{a}o,DM}|_{f_s}. \tag{3.9}$$

However, a DMF does not address the problem of CM EMI emissions. High-frequency CM voltage (and du/dt) is applied on the motor, which stresses its insulation and causes bearing currents. By employing the voltage source inverter model of **Fig. 3.3**, the CM equivalent circuit [69, 80] of the DMF is derived in **Fig. 3.2(c)**. The cable and motor parasitic capacitances can be lumped into a single capacitance $c_c + c_m$, for the sake of simplicity. The DMF does not attenuate CM voltage, i.e. it features a unity CM attenuation

$$A_{CM}|_{DMF}(f) = 1. \tag{3.10}$$

Even though a second order CM filter is formed by the DMF inductors $L_m/3$ and the parasitic capacitances $c_c + c_m$, the filtering effect can be neglected, because the cut-off frequency of this filter is in the range of several MHz, due to the small value of the parasitic capacitances ($\sim 100\,\mathrm{pF}$). The spectrum of the CM voltage at the inverter output terminals is

$$\hat{U}_{io,CM}|_{f_s}(f) = A_{CM}|_{DMF} \cdot \hat{U}_{\bar{i}o,CM}|_{f_s} = \hat{U}_{\bar{i}o,CM}|_{f_s}. \tag{3.11}$$

Therefore, the switch-node CM voltage $u_{\bar{i}o,CM}|_{f_s}$ (and high du/dt) is directly applied to the cable/motor. This is a major drawback of pure DM filtering.

Furthermore, a DMF results in high EMI emissions at the DC input-side. High $\mathrm{d}u/\mathrm{d}t$ is applied on the cable/motor parasitic capacitances $c_\mathrm{m} + c_\mathrm{c}$, inducing unwanted CM currents. These parasitic CM currents, form a return path through the DC input-side, thereby causing input CM EMI emissions, as is highlighted in **Fig. 3.2(a)**. This interdependence between the input-side and output-side CM EMI emissions can be quantified by considering the CM equivalent circuit of **Fig. 3.2(c)**. There, the equivalent input CM EMI noise source $u_{\bar{\mathrm{pn}},\mathrm{CM}|\mathrm{fs}}$ must be attenuated by the depicted two-stage input filter, such that the input terminal p/n voltage $u_{\mathrm{pn},\mathrm{CM}|\mathrm{fs}}$ lies within the required EMI limits. The spectrum of the input CM EMI noise source $u_{\bar{\mathrm{pn}},\mathrm{CM}|\mathrm{fs}}$ is approximately calculated based on the CM equivalent circuit of **Fig. 3.2(c)** as

$$\begin{aligned}\left\lceil \hat{U}_{\bar{\mathrm{pn}},\mathrm{CM}|\mathrm{fs}} \right\rceil (nf_\mathrm{s}) &\simeq \frac{c_\mathrm{s}+c_\mathrm{c}+c_\mathrm{m}}{C_{\mathrm{pn},\mathrm{CM},0}+c_\mathrm{s}+c_\mathrm{c}+c_\mathrm{m}} \left\lceil \hat{U}_{\bar{\mathrm{io}},\mathrm{CM}|\mathrm{fs}} \right\rceil \\ &\overset{(3.6)}{=} \frac{c_\mathrm{s}+c_\mathrm{c}+c_\mathrm{m}}{C_{\mathrm{pn},\mathrm{CM},0}+c_\mathrm{s}+c_\mathrm{c}+c_\mathrm{m}} \frac{2U_\mathrm{pn}}{n\pi}.\end{aligned} \tag{3.12}$$

The high-frequency switch-node CM voltage $u_{\bar{\mathrm{io}},\mathrm{CM}|\mathrm{fs}}$ **(3.6)** is the origin of CM EMI emissions. The input CM EMI emissions $u_{\bar{\mathrm{pn}},\mathrm{CM}|\mathrm{fs}}$ are proportional to the sum of the parasitic capacitances $c_\mathrm{s} + c_\mathrm{c} + c_\mathrm{m}$ (semiconductor devices, cable and motor) and inversely proportional to the input filter DC link CM capacitance $C_{\mathrm{pn},\mathrm{CM},0}$. Note that the cable inductance l_c is neglected in this calculation. Depending on the length of the cable and/or the motor housing a different total parasitic capacitance $c_\mathrm{c} + c_\mathrm{m}$ is formed. Consequently, the CM EMI noise at the input-side depends on the mechanical installation of the motor drive at the output-side, i.e. input-to-output CM noise mutual influence. Given the numerous applications of motor drives and the variety of end users, the interdependency of the input-side CM emissions and the output mechanical installation is unwanted. When only a DMF is employed, it is difficult to predict the CM EMI emissions at the DC input-side and it is equally challenging to design an appropriate input filter. For all the above reasons, a pure DM output filter should be avoided.

3.1.2 Combined Full Sine-Wave Output Filter (c-FSF)

In order to resolve the deficiencies of the simple DM output filter a full sine-wave output filter (FSF) is recommended, that features both DM and CM attenuation. The combined full sine-wave output filter (c-FSF), visualized in **Fig. 3.4(a)**, is first investigated. The c-FSF employs three individual in-

ductors and visually resembles the DMF of **Fig. 3.2(a)**. However, in contrast to a DMF, the filter capacitors $C_\mathrm{m}/2$ are directly connected to the positive/negative DC rails $\bar{p}/\bar{n}$. Thereby, CM emissions can return through the filter capacitors to the DC link and the semiconductor devices, which created the CM emissions in the first place. The same physical components C_m, L_m are utilized simultaneously for DM and CM output filter attenuation, justifying the name "*combined*" full sine-wave filter.

The c-FSF generates sinusoidal currents/voltages for the high-speed motor. By employing the voltage source inverter model of **Fig. 3.3**, the DM equivalent circuit of the c-FSF is derived in **Fig. 3.4(b)**. The c-FSF is equivalent to a second order filter with DM attenuation

$$A_\mathrm{DM}|_\text{c-FSF}(f) = \left| \frac{f^2_\mathrm{r,DM}|_\text{c-FSF}}{f^2_\mathrm{r,DM}|_\text{c-FSF} - f^2} \right|, \tag{3.13}$$

where $f_\mathrm{r,DM}|_\text{c-FSF}$ is the DM resonant frequency

$$f_\mathrm{m} < f_\mathrm{r,DM}|_\text{c-FSF} = \frac{1}{2\pi\sqrt{L_\mathrm{m}C_\mathrm{m}}} < f_\mathrm{s}. \tag{3.14}$$

The DM resonant frequency $f_\mathrm{r,DM}|_\text{c-FSF}$ is selected such that the fundamental voltages/currents are sinusoidal and the high-frequency switch-node DM voltage component $u_\mathrm{a\bar{o},DM}|_{f_\mathrm{s}}$ is effectively attenuated. The resulting DM voltage spectrum at the output terminal a is

$$\hat{U}_\mathrm{ao,DM}|_{f_\mathrm{s}}(f) = A_\mathrm{DM}|_\text{c-FSF} \cdot \hat{U}_\mathrm{a\bar{o},DM}|_{f_\mathrm{s}}. \tag{3.15}$$

The c-FSF resolves the CM EMI emissions problem: An FSF eliminates $\mathrm{d}u/\mathrm{d}t$ at the output-side, thus protects the motor bearing and windings from excessive electrical stress. By employing the voltage source inverter model of **Fig. 3.3**, the c-FSF CM equivalent circuit is derived in **Fig. 3.4(c)**. The CM equivalent circuit is formed by the parallel connection of all three filter inductors $L_\mathrm{m}/3$ and capacitors $3C_\mathrm{m}$. The c-FSF is equivalent to a second order filter with CM attenuation

$$A_\mathrm{CM}|_\text{c-FSF}(f) = \left| \frac{f^2_\mathrm{r,CM}|_\text{c-FSF}}{f^2_\mathrm{r,CM}|_\text{c-FSF} - f^2} \right|, \tag{3.16}$$

where $f_\mathrm{r,CM}|_\text{c-FSF}$ is the CM resonant frequency

$$f_\mathrm{m} < f_\mathrm{r,CM}|_\text{c-FSF} = \frac{1}{2\pi\sqrt{L_\mathrm{m}C_\mathrm{m}}} < f_\mathrm{s}. \tag{3.17}$$

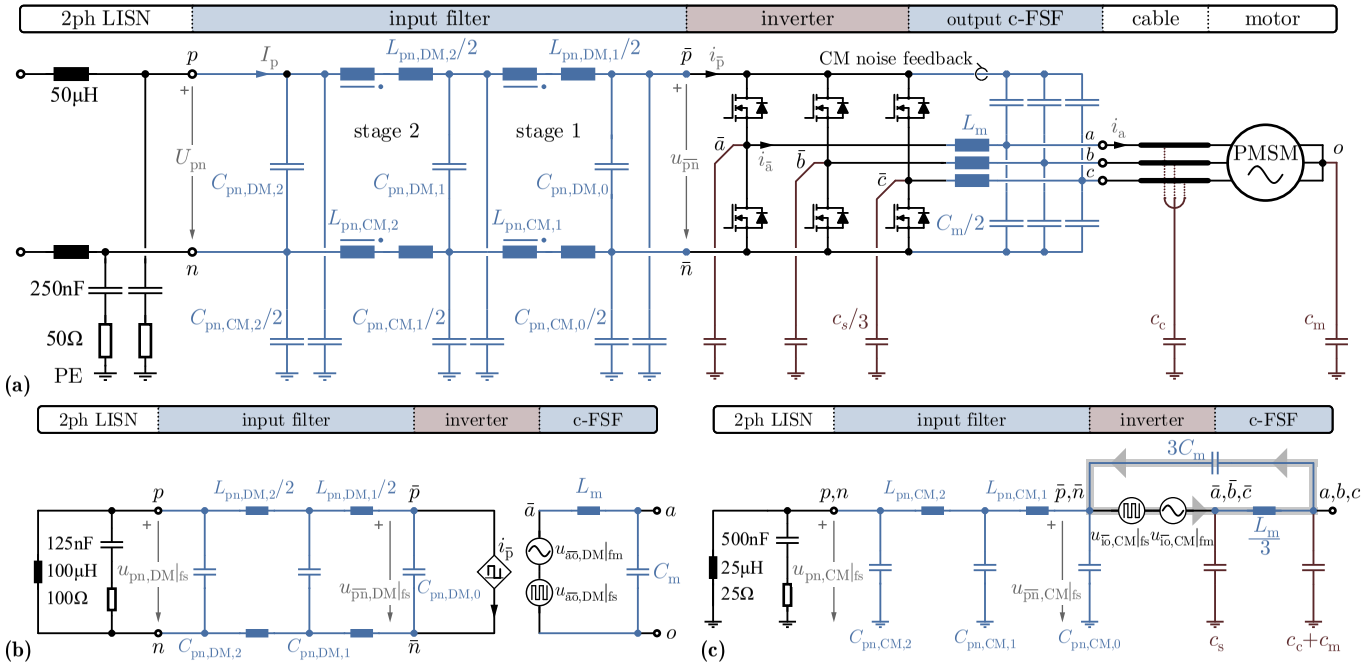


Fig. 3.4: (a) Inverter featuring a combined full sine-wave output filter (c-FSF). **(b)** DM and **(c)** CM equivalent circuits.

Accordingly, the spectrum of the CM voltage (worst case approximation) at the inverter output terminals is

$$\hat{U}_{\text{io,CM}}|_{f_\text{s}}(f) = A_{\text{CM}}|_{\text{c-FSF}} \cdot \hat{U}_{\bar{\text{io}},\text{CM}}|_{f_\text{s}}. \tag{3.18}$$

In the case of the c-FSF, the attenuation and resonant frequency of the DM and CM equivalent circuits are by definition equal, i.e. $A_{\text{DM}}|_{\text{c-FSF}}(f) = A_{\text{CM}}|_{\text{c-FSF}}(f)$ and $f_{\text{r,DM}}|_{\text{c-FSF}} = f_{\text{r,CM}}|_{\text{c-FSF}}$.

Furthermore, an FSF achieves low CM EMI emissions at the input: The cable parasitic capacitance c_c and the motor parasitic capacitance c_m do not conduct unwanted CM currents, which would close a loop through the DC input-side, thereby causing CM EMI noise. The CM EMI emissions at the input-side, can be quantified by considering the CM equivalent circuit of **Fig. 3.4(c)**. The spectrum of the equivalent input CM EMI noise source $u_{\bar{\text{pn}},\text{CM}|\text{fs}}$ is approximated

$$\begin{aligned}\left[\hat{U}_{\bar{\text{pn}},\text{CM}|\text{fs}}\right](nf_\text{s}) &\simeq \frac{c_\text{s}}{C_{\text{pn,CM},0} + c_\text{s}} \left[\hat{U}_{\bar{\text{io}},\text{CM}|\text{fs}}\right] \\ &\overset{(3.6)}{=} \frac{c_\text{s}}{C_{\text{pn,CM},0} + c_\text{s}} \frac{2U_\text{pn}}{n\pi}.\end{aligned} \tag{3.19}$$

The CM EMI emissions at the input are proportional to the parasitic capacitance c_s of the semiconductor devices. The overall input CM EMI emissions, in the case of a c-FSF, are significantly lower compared to the case of a DMF (cf. **Fig. 3.2**), where the input CM EMI emissions are proportional to the semiconductor/cable/motor parasitic capacitances $c_\text{s} + c_\text{c} + c_\text{m}$ **(3.12)**. Thanks to the c-FSF, the input CM emissions do nearly not depend on the mechanical installation at the output side (cable, motor). For all the above reasons, a c-FSF presents several advantages compared to a DMF counterpart, hence should be preferred.

3.1.3 Discrete Full Sine-Wave Output Filter (d-FSF)

A second FSF variant is now investigated. This output filter is denoted as discrete full sine-wave output filter (d-FSF) and is shown in **Fig. 3.5(a)**. The d-FSF employs a three-phase CM choke $L_{\text{m,CM}}$, in contrast to a c-FSF that employs three individual inductors (cf. **Fig. 3.4(a)**). The leakage inductance of the CM choke windings is used as DM inductance $L_{\text{m,DM}}$. The d-FSF uses "*discrete*" dedicated components for the DM attenuation ($L_{\text{m,DM}}, C_{\text{m,DM}}$) and the CM attenuation ($L_{\text{m,CM}}, C_{\text{m,CM}}$). Thereby, the DM and CM output filter parts are decoupled from each other and can be designed independently.

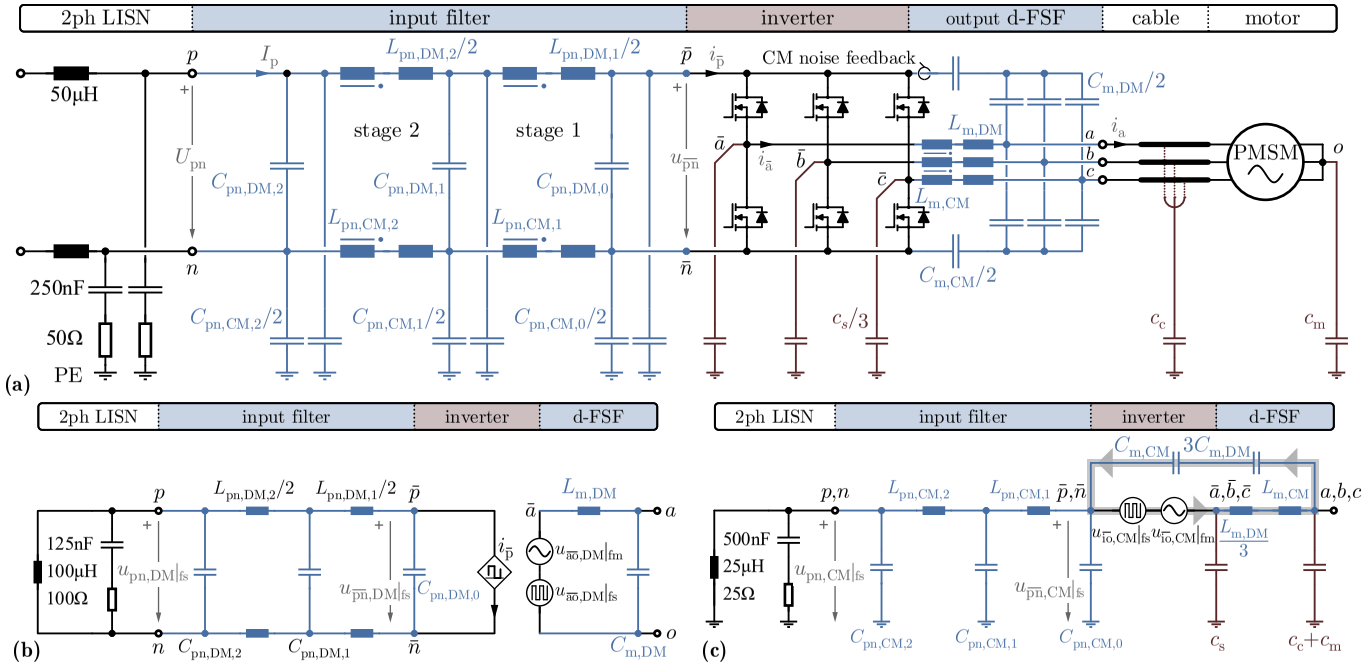


Fig. 3.5: **(a)** Inverter featuring a discrete full sine-wave output filter (d-FSF). **(b)** DM and **(c)** CM equivalent circuits.

The d-FSF generates sinusoidal motor currents/voltages. The DM equivalent circuit is shown in **Fig. 3.5(b)**. The d-FSF is equivalent to a second order filter with DM attenuation

$$A_{\mathrm{DM}}|_{\text{d-FSF}}(f) = \left| \frac{f_{\mathrm{r,DM}}^2|_{\text{d-FSF}}}{f_{\mathrm{r,DM}}^2|_{\text{d-FSF}} - f^2} \right|, \tag{3.20}$$

where $f_{\mathrm{r,DM}}|_{\text{d-FSF}}$ is the DM resonant frequency

$$f_{\mathrm{m}} < f_{\mathrm{r,DM}}|_{\text{d-FSF}} = \frac{1}{2\pi\sqrt{L_{\mathrm{m,DM}} C_{\mathrm{m,DM}}}} < f_{\mathrm{s}}. \tag{3.21}$$

The spectrum of the DM voltage at the inverter output terminal a is

$$\hat{U}_{\mathrm{ao,DM}}|_{f_{\mathrm{s}}}(f) = A_{\mathrm{DM}}|_{\text{d-FSF}} \cdot \hat{U}_{\bar{\mathrm{a}}\mathrm{o,DM}}|_{f_{\mathrm{s}}}. \tag{3.22}$$

The d-FSF resolves the CM EMI emissions problem. The CM equivalent circuit is shown in **Fig. 3.5(c)** and comprises a second order filter with CM attenuation

$$A_{\mathrm{CM}}|_{\text{d-FSF}}(f) = \left| \frac{f_{\mathrm{r,CM}}^2|_{\text{d-FSF}}}{f_{\mathrm{r,CM}}^2|_{\text{d-FSF}} - f^2} \right|. \tag{3.23}$$

The CM resonant frequency $f_{\mathrm{r,CM}}|_{\text{d-FSF}}$ is

$$f_{\mathrm{m}} < f_{\mathrm{r,CM}}|_{\text{d-FSF}} = \frac{1}{2\pi\sqrt{L'_{\mathrm{m,CM}} C'_{\mathrm{m,CM}}}} < f_{\mathrm{s}}, \tag{3.24}$$

where $L'_{\mathrm{m,CM}}$ is the equivalent CM inductance

$$L'_{\mathrm{m,CM}} = L_{\mathrm{m,CM}} + \frac{L_{\mathrm{m,DM}}}{3} \overset{L_{\mathrm{m,CM}} \gg L_{\mathrm{m,DM}}}{=} L_{\mathrm{m,CM}}, \tag{3.25}$$

and $C'_{\mathrm{m,CM}}$ is the equivalent CM capacitance

$$C'_{\mathrm{m,CM}} = \frac{C_{\mathrm{m,CM}} + 3C_{\mathrm{m,DM}}}{C_{\mathrm{m,CM}} \cdot 3C_{\mathrm{m,DM}}} \overset{C_{\mathrm{m,DM}} \gg C_{\mathrm{m,CM}}}{=} C_{\mathrm{m,CM}}. \tag{3.26}$$

The spectrum of the CM voltage (worst case approximation) at the inverter output terminals is

$$\hat{U}_{\mathrm{io,CM}}|_{f_{\mathrm{s}}}(f) = A_{\mathrm{CM}}|_{\text{d-FSF}} \cdot \hat{U}_{\bar{\mathrm{i}}\mathrm{o,CM}}|_{f_{\mathrm{s}}}. \tag{3.27}$$

The CM EMI emissions at the input-side, can be quantified by considering the CM equivalent circuit of **Fig. 3.5(c)**. The spectrum of the equivalent input CM EMI noise source $u_{\bar{\mathrm{p}}\mathrm{n,CM}}|_{\mathrm{fs}}$ is the same as in the case of a c-FSF **(3.19)**. This is expected, since both c-FSF and d-FSF largely attenuate CM emissions (and $\mathrm{d}u/\mathrm{d}t$) at the AC output-side.

3.1.4 Input Filter

An input filter with $N = 2$ stages is employed (cf. **Fig. 3.2(a)**) in order to ensure that the system complies with the IEC 61800-3 conducted EMI limits at the DC input-side [42]. The DC link comprises the DM capacitor $C_{\mathrm{pn,DM,0}}$ and the CM Y2 capacitors $C_{\mathrm{pn,CM,0}}$. Each of the subsequent filter stages $k = 1...2$, is identical and includes a second order DM filter ($L_{\mathrm{pn,DM,k}}$, $C_{\mathrm{pn,DM,k}}$) and a second order CM filter ($L_{\mathrm{pn,CM,k}}$, $C_{\mathrm{pn,CM,k}}$).

Considering the DM part of the input filter, the input filter attenuates the equivalent input DM noise source $u_{\mathrm{p\tilde{n},DM}|\mathrm{fs}}$, such that the input terminal p/n DM voltage $u_{\mathrm{pn,DM}|\mathrm{fs}}$ lies within the required EMI limits. The origin of the DM input EMI noise $u_{\mathrm{p\tilde{n},DM}|\mathrm{fs}}$ is the switched DC link current $i_{\tilde{\mathrm{p}}}$ of the inverter, which in return generates voltage ripple across the DC link DM capacitor $C_{\mathrm{pn,DM,0}}$. An upper bound of the input-side DM EMI noise source $u_{\mathrm{p\tilde{n},DM}|\mathrm{fs}}$ spectrum is

$$\left|\hat{U}_{\mathrm{p\tilde{n},DM}|\mathrm{fs}}\right|(nf_\mathrm{s}) = \frac{1}{n2\pi f_\mathrm{s} C_{\mathrm{pn,DM,0}}} \frac{2\hat{I}_\mathrm{m}}{n\pi}. \tag{3.28}$$

The input DM EMI noise source $u_{\mathrm{p\tilde{n},DM}|\mathrm{fs}}$ is not affected by the output filter type (DMF or FSF) [63]. The DM attenuation of the input filter is

$$A_\mathrm{DM}(f) = \left| \frac{f_{\mathrm{r,DM}}^4}{f_{\mathrm{r,DM}}^4 + f^4 - 3f^2 f_{\mathrm{r,DM}}^2} \right|, \tag{3.29}$$

where $f_{\mathrm{r,DM}}$ is the DM resonant frequency of each input filter stage

$$f_{\mathrm{r,DM}} = \frac{1}{2\pi\sqrt{L_{\mathrm{pn,DM,i}} C_{\mathrm{pn,DM,i}}}} < f_\mathrm{s}. \tag{3.30}$$

The spectrum of the DM EMI noise at the inverter input terminals p/n is

$$\hat{U}_{\mathrm{pn,DM}}|_{f_\mathrm{s}}(f) = A_\mathrm{DM} \cdot \hat{U}_{\mathrm{p\tilde{n},DM}}|_{f_\mathrm{s}}. \tag{3.31}$$

Considering now the CM part of the input filter, the input filter attenuates the equivalent input CM noise source $u_{\mathrm{p\tilde{n},CM}|\mathrm{fs}}$, such that the input terminal p/n CM voltage $u_{\mathrm{pn,CM}|\mathrm{fs}}$ lies within the required EMI limits. The input CM noise source $u_{\mathrm{p\tilde{n},CM}|\mathrm{fs}}$ depends on the employed output filter type. It is significantly higher in the case of a DMF **(3.12)**, compared to the case of an FSF **(3.19)**. The CM attenuation of the input filter is

$$A_\mathrm{CM}(f) = \left| \frac{f_{\mathrm{r,CM}}^4}{f_{\mathrm{r,CM}}^4 + f^4 - 3f^2 f_{\mathrm{r,CM}}^2} \right|, \tag{3.32}$$

where $f_{\mathrm{r,CM}}$ is the CM resonant frequency of each input filter stage

$$f_{\mathrm{r,CM}} = \frac{1}{2\pi\sqrt{L_{\mathrm{pn,CM,i}} C_{\mathrm{pn,CM,i}}}} < f_{\mathrm{s}}. \tag{3.33}$$

The spectrum of the CM EMI noise at the inverter input terminals p/n is

$$\hat{U}_{\mathrm{pn,CM}}|_{f_{\mathrm{s}}}(f) = A_{\mathrm{CM}} \cdot \hat{U}_{\mathrm{p\bar{n},CM}}|_{f_{\mathrm{s}}}. \tag{3.34}$$

3.2 Filter Design

3.2.1 Output Filter Design

The output filter should not interfere with the fundamental motor currents/voltages. Based on this objective, the c-FSF is first designed. The DM resonant frequency $f_{\mathrm{r,DM}}|_{\text{c-FSF}}$ of a c-FSF **(3.14)** should be amply spaced between the fundamental motor frequency f_{m} and the switching frequency f_{s}

$$f_{\mathrm{m}} a_{\mathrm{f}} \leq f_{\mathrm{r,DM}}|_{\text{c-FSF}} \leq f_{\mathrm{s}}/a_{\mathrm{f}}, \tag{3.35}$$

where $a_{\mathrm{f}} \geq 7$ is an empirical design parameter. A low resonant frequency is related to strong DM filter attenuation and hence good motor voltage quality. However, a very low resonant frequency $f_{\mathrm{r,DM}}|_{\text{c-FSF}} < f_{\mathrm{m}} a_{\mathrm{f}}$, leads to excessive output filter reactive power. On the other hand, a high DM resonant frequency yields smaller passive component values and accordingly a more compact output filter. A very high DM resonant frequency $f_{\mathrm{r,DM}}|_{\text{c-FSF}} > f_{\mathrm{s}}/a_{\mathrm{f}}$ potentially causes an excitation of the output filter resonance and thus excessively large currents. Based on the resonant frequency constraint of **(3.35)**, the following inequality must hold for the switching frequency

$$f_{\mathrm{m}} a_{\mathrm{f}} \leq \frac{f_{\mathrm{s}}}{a_{\mathrm{f}}} \rightarrow f_{\mathrm{s}} \geq a_{\mathrm{f}}^2 f_{\mathrm{m}}. \tag{3.36}$$

Thereby, a lower bound for the switching frequency f_{s} is calculated. It is noted that a high-speed motor drive, which features a high fundamental frequency, e.g. $f_{\mathrm{m}} = 5\,\mathrm{kHz}$, also requires a high switching frequency e.g. $f_{\mathrm{s}} \geq a_{\mathrm{f}}^2 f_{\mathrm{m}} = 245\,\mathrm{kHz}$. A comprehensive design algorithm for the output filter, tailored to high-speed motor drives, is presented in **Sec. 3.2.2**. A more general design algorithm, also applicable to conventional low-speed motor drives, is described in the following.

The c-FSF comprises three individual inductors L_m, each corresponding to one phase-leg. For a filter inductor L_m the maximum inductor current ripple amplitude (single-side) $\Delta I_{\mathrm{L_m}}$ can be calculated as

$$\Delta I_{\mathrm{L_m}} = \frac{U_\mathrm{pn}}{8 L_\mathrm{m} f_\mathrm{s}}. \tag{3.37}$$

Accordingly, in order to limit the current ripple to a maximum value $\Delta I_{\mathrm{L_m}}$ then the inductor L_m value should be

$$L_\mathrm{m} \geq \frac{U_\mathrm{pn}}{8 \Delta I_{\mathrm{L_m}} f_\mathrm{s}}. \tag{3.38}$$

The maximum occurring voltage ripple amplitude (single-side) $\Delta U_{\mathrm{C_m}}$ at the output filter capacitor C_m is

$$\Delta U_{\mathrm{C_m}} = \frac{\Delta I_{\mathrm{L_m}}}{8 C_\mathrm{m} f_\mathrm{s}} \overset{(3.37)}{=} \frac{U_\mathrm{pn}}{64 f_\mathrm{s}^2 L_\mathrm{m} C_\mathrm{m}} = \frac{\pi^2}{16} \left(\frac{f_{\mathrm{r,DM}}|_{\text{c-FSF}}}{f_\mathrm{s}} \right)^2 U_\mathrm{pn}. \tag{3.39}$$

Accordingly, in order to limit the voltage ripple to a maximum value of $\Delta U_{\mathrm{C_m}} \leq 1\,\mathrm{V}$, which is safe for the motor operation, the capacitance C_m values should be

$$C_\mathrm{m} \geq \frac{U_\mathrm{pn}}{64 f_\mathrm{s}^2 L_\mathrm{m} \Delta U_{\mathrm{C_m}}}. \tag{3.40}$$

The d-FSF comprises only one three-phase choke. The CM inductance of the choke $L_\mathrm{m,CM}$ is used for CM attenuation, while the leakage inductance of the choke $L_\mathrm{m,DM}$ is used for DM attenuation [81, 82]. The d-FSF is designed, similarly to the c-FSF. The same DM resonant frequency $f_{\mathrm{r,DM}}|_{\text{d-FSF}}$ constraints of **(3.35)** and switching frequency constraint of **(3.36)** apply for the d-FSF. Furthermore, the output filter DM inductor constraint of **(3.38)** and DM capacitor constraint of **(3.40)** are extended for the d-FSF:

$$L_\mathrm{m,DM} \geq \frac{U_\mathrm{pn}}{8 \Delta I_{\mathrm{L_{m,DM}}} f_\mathrm{s}}, \quad C_\mathrm{m,DM} \geq \frac{U_\mathrm{pn}}{64 f_\mathrm{s}^2 L_\mathrm{m} \Delta U_{\mathrm{C_{m,DM}}}}. \tag{3.41}$$

The d-FSF should not interfere with the third harmonic CM voltage $u_{\bar{\mathrm{io}},\mathrm{CM}}|_{f_\mathrm{m}}$ **(3.5)** of the THM modulation strategy **(3.1)**. Based on this objective, the CM resonant frequency is selected to be similar to the DM resonant frequency $f_{\mathrm{r,CM}}|_{\text{d-FSF}} \simeq f_{\mathrm{r,DM}}|_{\text{d-FSF}}$ **(3.35)**. The inductance of the CM choke $L_\mathrm{m,CM}$ is typically two orders of magnitude larger than its DM leakage inductance

Tab. 3.2: Design summary for an output FSF. Numeric values are given for a system with the specifications of **Tab 3.1**.

		Output c-FSF		**Output d-FSF**
Switching freq.	**(3.36)**	$f_\mathrm{s} = 350\,\mathrm{kHz}$, $a_\mathrm{f} = 7$	**(3.36)**	$f_\mathrm{s} = 350\,\mathrm{kHz}$, $a_\mathrm{f} = 7$
DM resonant freq.	**(3.14)**	$f_{\mathrm{r,DM}}\vert_{\text{c-FSF}} = 50\,\mathrm{kHz}$	**(3.21)**	$f_{\mathrm{r,DM}}\vert_{\text{d-FSF}} = 50\,\mathrm{kHz}$
DM attenuation	**(3.13)**	$A_{\mathrm{DM}}\vert_{\text{c-FSF}}(f_\mathrm{s}) = -33.5\mathrm{dB}$	**(3.20)**	$A_{\mathrm{DM}}\vert_{\text{d-FSF}}(f_\mathrm{s}) = -33.5\mathrm{dB}$
CM resonant freq.	**(3.17)**	$f_{\mathrm{r,CM}}\vert_{\text{c-FSF}} = 50\,\mathrm{kHz}$	**(3.24)**	$f_{\mathrm{r,CM}}\vert_{\text{d-FSF}} = 50\,\mathrm{kHz}$
CM attenuation	**(3.16)**	$A_{\mathrm{CM}}\vert_{\text{c-FSF}}(f_\mathrm{s}) = -33.5\mathrm{dB}$	**(3.23)**	$A_{\mathrm{CM}}\vert_{\text{d-FSF}}(f_\mathrm{s}) = -33.5\mathrm{dB}$
Inductance	**(3.38)**	$L_\mathrm{m} = 5\,\mu\mathrm{H}$, $\Delta I_{\mathrm{L_m}} = 5.7\,\mathrm{A}$	**(3.41)**	$L_{\mathrm{m,DM}} = 5\,\mu\mathrm{H}$, $\Delta I_{\mathrm{L_{m,DM}}} = 5.7\,\mathrm{A}$
			(3.42)	$L_{\mathrm{m,CM}} = 0.5\,\mathrm{mH}$
Capacitance	**(3.40)**	$C_\mathrm{m} = 2\,\mu\mathrm{F}$, $\Delta U_{\mathrm{C_m}} = 1\,\mathrm{V}$	**(3.41)**	$C_{\mathrm{m,DM}} = 2\,\mu\mathrm{F}$, $\Delta U_{\mathrm{C_{m,DM}}} = 1\,\mathrm{V}$
			(3.42)	$C_{\mathrm{m,CM}} = 20\,\mathrm{nF}$

Tab. 3.3: Design summary for an input filter with minimum volume and assuming an installed output FSF (c-FSF or d-FSF). Numeric values are given for a system with the specifications of **Tab 3.1**.

		DM Input Filter		**CM Input Filter**
Critical frequency	**(3.49)**	$f_\mathrm{c} = nf_\mathrm{s} = 350\,\mathrm{kHz}$, $n = 1$	**(3.49)**	$f_\mathrm{c} = nf_\mathrm{s} = 350\,\mathrm{kHz}$, $n = 1$
Filter stages		$N = 2$		$N = 2$
Min. attenuation	**(3.51)**	$A_{\mathrm{DM}} = -37.9\mathrm{dB}$	**(3.50)**	$A_{\mathrm{CM}} = -37.7\mathrm{dB}$
Max. resonant freq.	**(3.52)**	$f_{\mathrm{r,DM}} = 117.7\,\mathrm{kHz}$	**(3.52)**	$f_{\mathrm{r,CM}} = 118.1\,\mathrm{kHz}$
Inductance		$L_{\mathrm{pn,DM,k}} = 0.15\,\mu\mathrm{H}$		$L_{\mathrm{pn,CM,k}} = 65\,\mu\mathrm{H}$
Capacitance		$C_{\mathrm{pn,DM,k}} = 17\,\mu\mathrm{F}$		$C_{\mathrm{pn,CM,k}} = 33\,\mathrm{nF}$
Resonant freq.	**(3.30)**	$f_{\mathrm{r,DM}} = 99.7\,\mathrm{kHz}$	**(3.33)**	$f_{\mathrm{r,CM}} = 108.7\,\mathrm{kHz}$
Attenuation	**(3.29)**	$A_{\mathrm{DM}} = -43.9\mathrm{dB}$	**(3.32)**	$A_{\mathrm{CM}} = -40.6\mathrm{dB}$

A parasitic capacitance of the semiconductor devices $c_\mathrm{s} = 100\,\mathrm{pF}$, is assumed.

$L_{m,DM}$ [81, 82]. Therefore, a small CM capacitance $C_{m,CM}$ must be selected in order to counterbalance the high CM choke inductance value $L_{m,CM}$:

$$L_{m,CM} = 100 \cdot L_{m,DM}, \quad C_{m,CM} = C_{m,DM}/100. \tag{3.42}$$

The above output filter design guidelines **(3.38)**, **(3.40)**, **(3.41)** and **(3.42)** depend on the switching frequency f_s. The switching frequency represents a crucial design trade-off. A high switching frequency allows to reduce the volume of the passive filter components, but at the same time increases the semiconductor switching losses and accordingly requires a larger semiconductor heatsink volume. The equation **(3.36)** only provides a lower bound for the switching frequency f_s, but does not explicitly define it. In order to select an appropriate switching frequency, a multi-objective optimization routine, with respect to inverter efficiency η and power density ρ, is employed [15, 83], which assesses the performance of several inverter designs. The optimization routine includes the inductive components (inductors L_m, three-phase choke $L_{m,CM}$) [81, 84, 85], the ceramic filter capacitors, the 200 V rated GaN semiconductor devices [86] and the semiconductor heatsinks [87]. Based on the optimization results, a switching frequency of $f_s = 350\,\text{kHz}$ is selected. This switching frequency is 70 times higher than the fundamental frequency of the motor $f_m = 5\,\text{kHz}$, a fact that enables a highly dynamic motor control. A design guideline summary for the c-FSF and d-FSF and the selected benchmark designs are given in **Tab. 3.2**.

3.2.2 Output Filter Design for High-Speed Drives

The output filter passive components are subject to strict design constraints when used in high-speed drive systems. The design constraints are derived for the c-FSF of **Fig. 3.4**, but can be easily extended for the d-FSF of **Fig. 3.5**. Based on **(3.35)**, the DM resonant frequency of the c-FSF $f_{r,DM}$ should be

$$\underbrace{f_m a_f}_{f_{r,DM,min}} \leq f_{r,DM} = \frac{1}{2\pi\sqrt{L_m C_m}} \leq \underbrace{f_s/a_f}_{f_{r,DM,max}}. \tag{3.43}$$

A resonant frequency that adheres to the above constraints lies within the design space illustrated in **Fig. 3.6(a)**. For low switching frequencies $f_s < a_f^2 f_m$ the inequality $f_{r,DM,max} < f_{r,DM,min}$ results, therefore there is no feasible filter design. As the switching frequency increases and exceeds the value $f_s \geq a_f^2 f_m$, the inequality $f_{r,DM,max} \geq f_{r,DM,min}$ results, hence feasible filter designs exist. For the current analysis, an output filter with minimum volume is

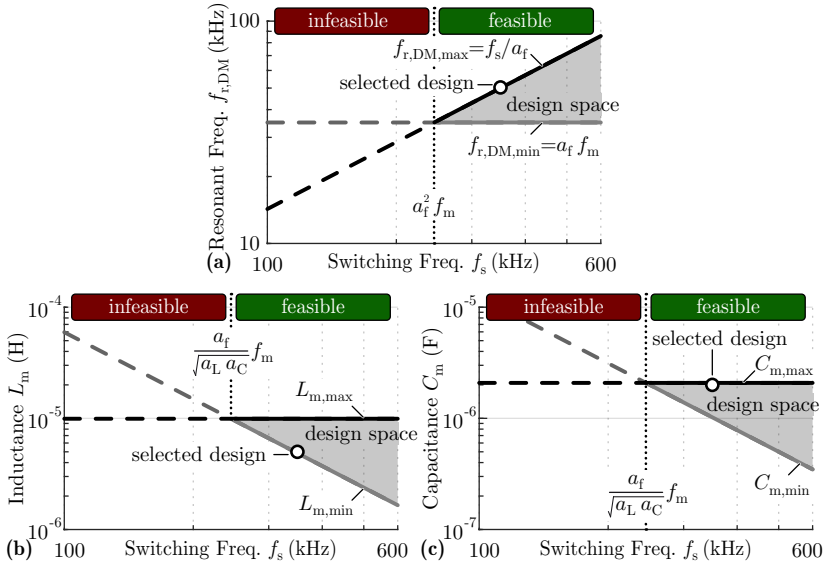


Fig. 3.6: Output filter design constraints for $a_f = 7$. **(a)** DM resonant frequency $f_{r,DM}$ design constraints, **(b)** inductor L_m and **(c)** capacitor C_m design constraints. The selected benchmark design of **Tab. 3.2**, which employs a switching frequency of $f_s = 350\,\text{kHz}$, is highlighted.

desired, therefore the highest possible DM resonant frequency within the available range **(3.43)** is selected, i.e. $f_{r,DM} = f_s/a_f$.

The selection of the DM resonant frequency $f_{r,DM}$, does not explicitly define the filter inductor/capacitor values. The inductor value L_m and the capacitor value C_m are selected based on reactive power considerations. For a transmitted power per phase $P = \hat{U}_m\hat{I}_m/2$ the reactive power consumption of the filter inductor L_m is

$$Q_L = \frac{\hat{I}_m^2\omega_m L_m}{2}, \quad a_L = \frac{Q_L}{P} = \frac{j\omega_m L_m \hat{I}_m}{\hat{U}_m}, \tag{3.44}$$

while the reactive power consumption of the filter capacitor C_m is

$$Q_C = \frac{\hat{U}_m^2\omega_m C_m}{2}, \quad a_C = \frac{Q_C}{P} = \frac{j\omega_m C_m \hat{U}_m}{\hat{I}_m}. \tag{3.45}$$

The reactive power consumptions Q_L and Q_C both scale linearly with the fundamental frequency f_m. Although the output filter reactive power is neg-

ligible for a fundamental frequency of $f_\mathrm{m} = 50\,\mathrm{Hz}$, it becomes significant for high-speed drive systems with fundamental frequency up to $f_\mathrm{m} = 5\,\mathrm{kHz}$. The reactive power values Q_L or Q_C should not exceed 30% of the active power P, i.e. $\{a_\mathrm{L}, a_\mathrm{C}\} < 0.3$. This limitation of the reactive power directly provides the maximum allowed inductance $L_\mathrm{m,max}$ and capacitance $C_\mathrm{m,max}$ values, given in **(3.46)** and **(3.47)**, respectively. Furthermore, based on the selected DM resonant frequency $f_\mathrm{r,DM} = f_\mathrm{s}/a_\mathrm{f}$ the minimum allowable inductance $L_\mathrm{m,min}$ and capacitance $C_\mathrm{m,min}$ are also calculated

$$\frac{1}{C_\mathrm{m,max}\omega_\mathrm{r,DM}^2} = \underbrace{\frac{a_\mathrm{f}^2\omega_\mathrm{m}R}{\omega_\mathrm{s}^2 a_\mathrm{C}}}_{L_\mathrm{m,min}} \leq L_\mathrm{m} \leq \underbrace{\frac{a_\mathrm{L}R}{\omega_\mathrm{m}}}_{L_\mathrm{m,max}}, \tag{3.46}$$

$$\frac{1}{L_\mathrm{m,max}\omega_\mathrm{r,DM}^2} = \underbrace{\frac{a_\mathrm{f}^2\omega_\mathrm{m}}{\omega_\mathrm{s}^2 a_\mathrm{L}R}}_{C_\mathrm{m,min}} \leq C_\mathrm{m} \leq \underbrace{\frac{a_\mathrm{C}}{\omega_\mathrm{m}R}}_{C_\mathrm{m,max}}, \tag{3.47}$$

where $R = \hat{U}_\mathrm{m}/\hat{I}_\mathrm{m}$ is the equivalent load resistance per phase. The feasible L_m and C_m design space is illustrated in **Fig. 3.6(b)** and **(c)**, respectively. There, for low switching frequencies $f_\mathrm{s} < \frac{a_\mathrm{f}}{\sqrt{a_\mathrm{C}a_\mathrm{L}}}f_\mathrm{m}$ the inequality $L_\mathrm{m,max} < L_\mathrm{m,min}$ holds, therefore there is no feasible inductor design. As the switching frequency increases and exceeds the value $f_\mathrm{s} \geq \frac{a_\mathrm{f}}{\sqrt{a_\mathrm{C}a_\mathrm{L}}}f_\mathrm{m}$, the inequality $L_\mathrm{m,max} \geq L_\mathrm{m,min}$ results, hence feasible inductor designs exist. Similarly, only switching frequencies $f_\mathrm{s} \geq \frac{a_\mathrm{f}}{\sqrt{a_\mathrm{C}a_\mathrm{L}}}f_\mathrm{m}$ allow for a feasible capacitor C_m design (cf. **Fig. 3.6(c)**).

In general, the resonant frequency $f_\mathrm{r,DM}$ constraints require a switching frequency $f_\mathrm{s} \geq a_\mathrm{f}^2 f_\mathrm{m}$ (cf. **Fig. 3.6(a)**), while the inductor L_m constraints and/or the capacitor C_m constraints require a switching frequency $f_\mathrm{s} \geq \frac{a_\mathrm{f}}{\sqrt{a_\mathrm{C}a_\mathrm{L}}}f_\mathrm{m}$. Since both switching frequency f_s inequalities must be satisfied it is reasonable to simplify as

$$\frac{a_\mathrm{f}}{\sqrt{a_\mathrm{C}a_\mathrm{L}}}f_\mathrm{m} = a_\mathrm{f}^2 f_\mathrm{m} \rightarrow a_\mathrm{C} = a_\mathrm{L} = \frac{1}{a_\mathrm{f}}. \tag{3.48}$$

The selection of the parameter a_f is crucial. Excessively high a_f values could over-constrain the filter design. Empirically, the parameter value $a_\mathrm{f} = 7$ is suggested.

In summary, a c-FSF is designed as follows:

(i) A switching frequency $f_\mathrm{s} \geq a_\mathrm{f}^2 f_\mathrm{m} = \frac{a_\mathrm{f}}{\sqrt{a_\mathrm{C}a_\mathrm{L}}}f_\mathrm{m}$ is selected.

(ii) The maximum possible DM resonant frequency $f_{\mathrm{r,DM}} = f_{\mathrm{s}}/a_{\mathrm{f}}$ is selected, in order to achieve minimum output filter volume.

(iii) The minimum possible inductance value $L_{\mathrm{m}} = L_{\mathrm{m,min}}$ of **(3.46)**, and the maximum capacitance value $C_{\mathrm{m}} = C_{\mathrm{m,max}}$ of **(3.47)** are selected. These passive component values yield the smallest output filter volume, since inductors are typically bulkier compared to capacitors.

3.2.3 Input Filter Design

A two-stage input filter is now designed. The conducted EMI emissions are regulated in the frequency range of 150 kHz...30 MHz. In this range, the critical frequency $f_{\mathrm{c}} = nf_{\mathrm{s}}$, which is related to the worst case EMI noise, is identified. The order n of the critical frequency is

$$n = \left\lceil \frac{150\,\mathrm{kHz}}{f_{\mathrm{s}}} \right\rceil. \tag{3.49}$$

For the inverter system at hand, the switching frequency is $f_{\mathrm{s}} = 350\,\mathrm{kHz}$, which exceeds 150 kHz, hence the critical frequency is $f_{\mathrm{c}} = f_{\mathrm{s}}$, i.e. $n = 1$.

The input filter design algorithm, assumes an installed FSF (c-FSF or d-FSF). As shown in **(3.19)**, an FSF result in a low equivalent CM noise source $u_{\bar{\mathrm{pn}},\mathrm{CM}|\mathrm{fs}}$ at the input. Thereafter, an FSF reduces the input CM EMI emissions and allows for a smaller input EMI filter. In this case, the minimum required input filter CM attenuation (dB) at the critical frequency f_{c} is

$$\begin{aligned} A_{\mathrm{CM}}(\mathrm{dB}) &= U_{\mathrm{limit}} - 10 - 6 - 20\log\left(\frac{\left\lceil \hat{U}_{\bar{\mathrm{pn}},\mathrm{CM}|\mathrm{fs}} \right\rceil (nf_{\mathrm{s}})}{10^{-6}\sqrt{2}}\right) \\ &\overset{(3.19)}{=} 63 - 20\log\left(\frac{1}{10^{-6}\sqrt{2}}\,\frac{c_{\mathrm{s}}}{C_{\mathrm{pn,CM},0} + c_{\mathrm{s}}}\,\frac{2U_{\mathrm{pn}}}{n\pi}\right), \end{aligned} \tag{3.50}$$

where $U_{\mathrm{limit}} = 79\mathrm{dB\mu V}$ is the limit mandated at $f = 350\,\mathrm{kHz}$ by the EMI regulations. Additionally 10dBµV are subtracted in order to account for component tolerances and further 6dBµV are subtracted in order to ensure that both 50 Ω LISN branches comply with the EMI regulations. Subsequently, the minimum required DM filter attenuation (dB) at the critical frequency f_{c}

is derived

$$\begin{aligned} A_{\mathrm{DM}}(\mathrm{dB}) &= U_{\mathrm{limit}} - 10 - 20\log\left(\frac{\left[\hat{U}_{\bar{\mathrm{pn}},\mathrm{DM}}|_{\mathrm{fs}}\right](nf_{\mathrm{s}})}{10^{-6}\sqrt{2}}\right) \\ &\overset{(3.28)}{=} 69 - 20\log\left(\frac{1}{10^{-6}\sqrt{2}}\frac{2\hat{I}_{\mathrm{m}}}{n\pi}\frac{1}{2\pi f_{\mathrm{s}} C_{\mathrm{pn,DM,0}}}\right), \end{aligned} \tag{3.51}$$

The required minimum DM attenuation A_{DM} is independent of the installed output filter (DMF or FSF). Accordingly, the input filter maximum allowed DM/CM resonant frequencies per stage are

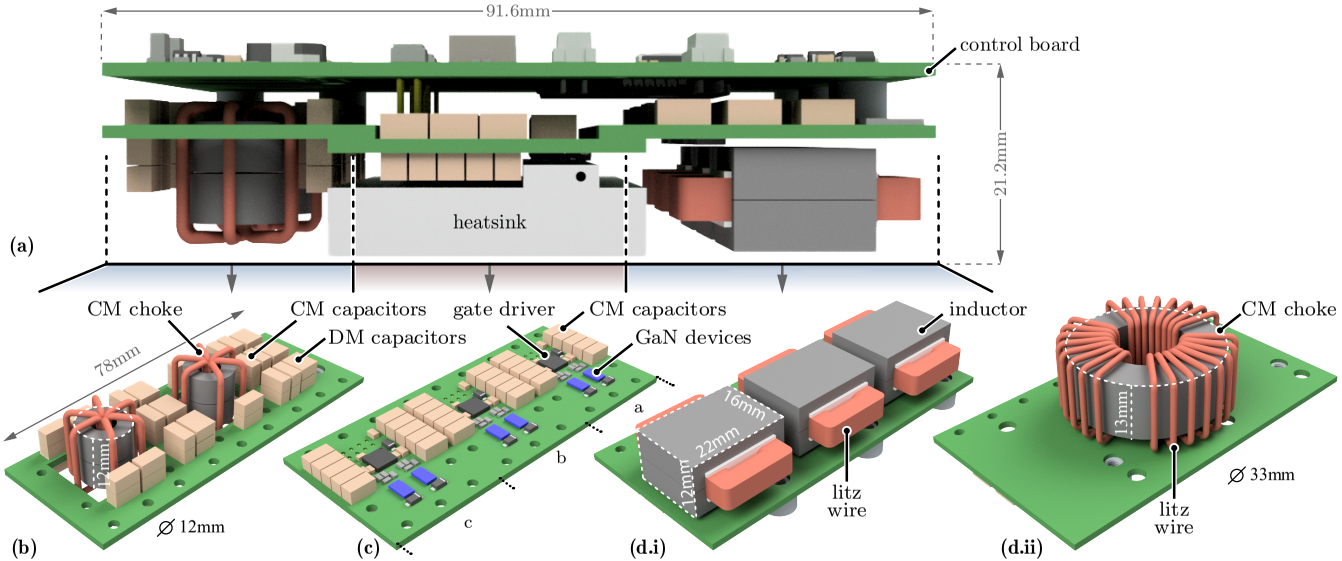
$$f_{\mathrm{r,DM}} = f_{\mathrm{s}}\sqrt[4]{A_{\mathrm{DM}}}, \quad f_{\mathrm{r,CM}} = f_{\mathrm{s}}\sqrt[4]{A_{\mathrm{CM}}}. \tag{3.52}$$

The input filter design is summarized in **Tab. 3.3**.

A benchmark two-stage input filer design is selected in **Tab. 3.3**. The input filter inductance ($L_{\mathrm{pn,DM,k}}$, $L_{\mathrm{pn,CM,k}}$) and capacitance ($C_{\mathrm{pn,DM,k}}$, $C_{\mathrm{pn,CM,k}}$) values of the benchmark design are selected such that the overall input filter volume is minimized [88]. A toroidal choke with two windings is used for the realization of the CM inductor $L_{\mathrm{pn,CM,k}}$. The stray inductance of each winding is used as DM inductance $L_{\mathrm{pn,DM,k}}$. The selected total input filter CM capacitance $C_{\mathrm{pn,CM}} = C_{\mathrm{pn,CM,0}} + C_{\mathrm{pn,CM,1}} + C_{\mathrm{pn,CM,2}} = 100\,\mathrm{nF}$ is very large. This large CM capacitance is only allowed in the case of motor drives supplied by a DC source (cf. **Fig. 3.1**). There, no low-frequency ground currents flow through the input filter CM capacitors $C_{\mathrm{pn,CM,k}}$. On the contrary, if a single-phase grid would supply the motor drive, then large CM currents would flow through the capacitors $C_{\mathrm{pn,CM,k}}$, that would violate the 3.5 mA limit, mandated by [42].

3.3 Experimental Validation

In order to validate the proposed filter concepts, an inverter prototype is assembled for a $P = 1\,\mathrm{kW}$, $n = 280\,\mathrm{krpm}$ high-speed motor drive, with the specifications of **Tab. 3.1**. The hardware prototype PCB assembly is presented in **Fig. 3.7(a)**. The experimental setup features a modular design, i.e. multiple interchangeable boards are connected together. The input filter board and the corresponding component values (measured) are depicted in **Fig. 3.7(b)**. The designed power board, employing the latest generation of 200 V rated GaN semiconductor devices, is depicted in **Fig. 3.7(c)**. The power board also includes the DC link, i.e. the input filter DM capacitor $C_{\mathrm{pn,DM,0}}$ and the CM



(b)			(c)			(d.i)			(d.ii)		
N=2 stages	k = [1,2]		MOSFET	EPC 2034		L_{m} 5.0µH	N87 ELP 22/6/16 4 turns		$L_{m,CM}$ 0.6mH	VAC500 R 30/20/10 8 turns	
$C_{pn,CM,k}$ 35.2nF	X7R Y2 ceramic		f_s	350kHz		C_{m} 2.0µF	X7R ceramic		$L_{m,DM}$ 3.0µH	choke leakage inductance	
$L_{pn,CM,k}$ 73µH	VAC500 R 10/7/5 3 turns		$C_{pn,CM,0}$ 39.6nF	X7R Y2 ceramic					$C_{m,CM}$ 18nF	X7R ceramic	
$C_{pn,DM,k}$ 17.6µF	X7R ceramic		$C_{pn,DM,0}$ 19.8µF	X7R ceramic		*can be reconfigured as DMF			$C_{m,DM}$ 2.0µF	X7R ceramic	
$L_{pn,DM,k}$ 0.3µH	choke leakage inductance										

Fig. 3.7: (a) Modular inverter hardware prototype. **(b)** Two-stage input filter followed by **(c)** power board. **(d.i)** c-FSF (cf. **Fig. 3.4**) and **(d.ii)** d-FSF (cf. **Fig. 3.5**). The c-FSF can be reconfigured into a DMF (cf. **Fig. 3.2**). The measured component values slightly differ from the theoretical values given in **Tab. 3.2** and **3.3**, due to non-idealities in the manufacturing.

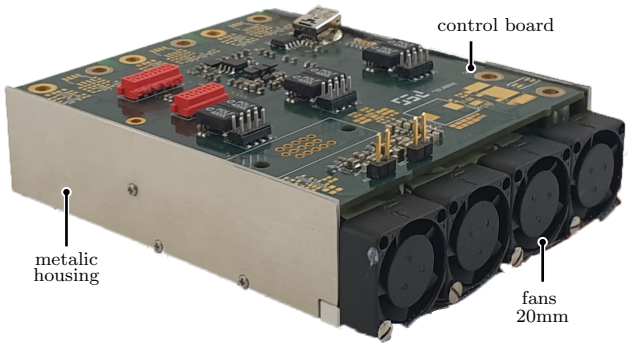


Fig. 3.8: Inverter hardware prototype with dimensions 99.6 mm × 80 mm × 23.7 mm. A power density of 5.8 kW/dm^3 (95 W/in^3) is achieved.

capacitors $C_{\text{pn,CM,0}}$. Placing these filter capacitors close to the semiconductor devices minimizes the parasitic inductances and therefore improves the EMI performance. The c-FSF and d-FSF boards, as well as the component values (measured) are illustrated in **Fig. 3.7(d.i)** and **(d.ii)**, respectively. It is noted, that the c-FSF board can be reconfigured as a simple DMF (cf. **Fig. 3.2**). A control board is vertically attached to the PCB assembly and finally a custom heatsink [89], an active thermal management system and a metallic housing are added. The assembled hardware demonstrator is shown in **Fig. 3.8**. A grounded metallic housing is mandatory for end user safety and is a common practice in drive systems. Furthermore, the grounded housing contributes to the parasitic capacitance formation, hence must be used for meaningful EMI noise measurements.

The c-FSF uses three ELP inductors L_{m} (cf. **Fig. 3.7(d.i)**), which require a total volume of 12.7 cm^3. The efficiency of the whole inverter system with an installed c-FSF is 96.6%. In comparison, the d-FSF uses one three-phase choke $L_{\text{m,CM}}$ (cf. **Fig. 3.7(d.ii)**), which requires a volume of 11.1 cm^3, The leakage inductance of the three-phase choke is used as the d-FSF DM inductor $L_{\text{m,DM}}$ (i.e. no dedicated DM inductors are employed) [81, 82]. The lower volume for the d-FSF is achieved thanks to the VAC 500F nanocrystalline magnetic material [90], used for the toroidal core. This material features a high saturation flux density of $\hat{B}_{\text{s}} = 1\,\text{T}$, which allows for a compact realization of the three-phase choke. In contrast, the c-FSF uses ELP cores, made of N87 ferrite material, which features a saturation flux density of only $\hat{B}_{\text{s}} = 350\,\text{mT}$. This

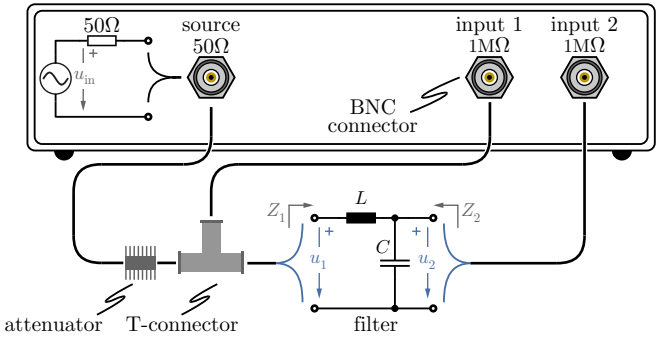


Fig. 3.9: Measurement setup for a filter transfer function, featuring the Omicron Labs Bode 100 frequency response analyser.

low saturation flux density, leads to a bulkier realization of the c-FSF. The efficiency of the whole inverter stage with an installed d-FSF is 96.1%. The high losses of the d-FSF (+5 W compared to c-FSF) originate from the three-phase CM choke windings. All the three-phase winding must mechanically fit within the inner diameter of the CM choke. Due to the limited available space, thinner wires must be used which accordingly result in high conduction losses.

3.3.1 Filter Attenuation Measurements

The attenuation of the input/output filter boards is experimentally measured, with a frequency response analyser, as is illustrated in **Fig. 3.9**. The c-FSF board attenuation is first measured. Namely, the DM attenuation $A_{\mathrm{DM}}|_{\text{c-FSF}}$ measurement **(3.13)** is shown in **Fig. 3.10(a)**, while the CM attenuation $A_{\mathrm{CM}}|_{\text{c-FSF}}$ measurement **(3.16)** is depicted in **Fig. 3.10(b)**. For low frequencies f both the DM attenuation $A_{\mathrm{DM}}|_{\text{c-FSF}}$ and the CM attenuation $A_{\mathrm{CM}}|_{\text{c-FSF}}$ match well with the theoretical approximation. However, for high frequencies $f > 4\,\mathrm{MHz}$ the CM attenuation $A_{\mathrm{CM}}|_{\text{c-FSF}}$ of **Fig. 3.10(b)** diverges from the theoretical approximation. In this frequency range, the CM performance of the c-FSF is degrading due to parasitic effects, i.e. self-resonance of the employed passive components and/or parasitic mutual coupling between the passive components [91].

Subsequently, the d-FSF is measured. The DM attenuation $A_{\mathrm{DM}}|_{\text{d-FSF}}$ **(3.20)** is illustrated in **Fig. 3.11(a)**. The theoretical approximation matches well the experimental measurement for low frequencies, but diverges for

high frequencies $f > 1\,\text{MHz}$, due to parasitic effects. It is noted, that by shorting two out of the three windings of the CM choke in the measurement setup of **Fig. 3.11(a)**, a leakage inductance of $1.5L_{\text{m,DM}}$ results. Therefore, this experimental setup does not correspond to the exact DM attenuation $A_{\text{DM}}|_{\text{d-FSF}}$, which would require a leakage inductance of exactly $L_{\text{m,DM}}$. However, the difference between the depicted DM attenuation measurement and the real DM attenuation is only -3dB.

The CM attenuation $A_{\text{CM}}|_{\text{d-FSF}}$ **(3.23)** is plotted in **Fig. 3.11(b)**, The depicted theoretical approximation assumes a constant CM inductance $L_{\text{m,CM}} = 600\,\mu\text{H}$ and CM capacitance $C_{\text{m,CM}} = 18\,\text{nF}$ (cf. **Fig. 3.7(d.ii)**), hence in the cut-off region of the filter $f > 50\,\text{kHz}$ the attenuation drops with a slope of -40dB per frequency decade f. However, this does not agree with the measured attenuation profile which drops with a slope close to -30dB per frequency decade f. This difference between the slope of the theoretical approximation and the measurement is caused by the non-linear, frequency dependent behaviour of the CM choke inductance $L_{\text{m,CM}}(f)$. In particular, the three-phase choke employs the nanocrystalline core material VAC 500F [90], whose imaginary magnetic permeability μ'' dominates for frequencies $f > 20\,\text{kHz}$ [92]. As a result, the CM inductor, exhibits a highly resistive, frequency dependent behaviour $L_{\text{m,CM}}(f)$ [93]. Hence, the measured CM attenuation profile $A_{\text{CM}}|_{\text{d-FSF}}(f)$ (-30dB per frequency decade) lies in between a first order *RC* filter (-20dB per frequency decade) and a *LC* filter (-40dB per frequency decade). It is noted, that the non-linearity of the core material is taken into account in the design process of the three-phase choke. Thus, for the frequency $f_{\text{s}} = 350\,\text{kHz}$, for which the d-FSF is designed, the measured CM attenuation $A_{\text{CM}}|_{\text{d-FSF}}$ and the theoretical approximation match well.

Finally, the input filter board attenuation is measured. In **Fig. 3.12(a)** the DM attenuation A_{DM} **(3.29)** is measured. The DM attenuation A_{DM} diverges from the theoretical approximation for frequencies $f > 700\,\text{kHz}$, due to parasitic effects [91]. Furthermore, the measured DM attenuation A_{DM} exhibits two pronounced resonances, a fact that is expected in a two-stage filter **(3.29)**. The CM attenuation A_{CM} **(3.32)** is measured in **Fig. 3.12(b)**. The depicted theoretical approximation assumes a constant CM inductance $L_{\text{pn,CM,k}} = 73\,\mu\text{H}$ and CM capacitance $C_{\text{pn,CM,k}} = 35.2\,\text{nF}$ (cf. **Fig. 3.7(b)**). Hence, in the cut-off region of the two-stage filter $f > 150\,\text{kHz}$ the attenuation drops with a slope of -80dB per frequency decade f. However, this does not agree with the measured attenuation profile which drops with a slope close to -60dB per frequency decade. As explained before, this difference is expected, due

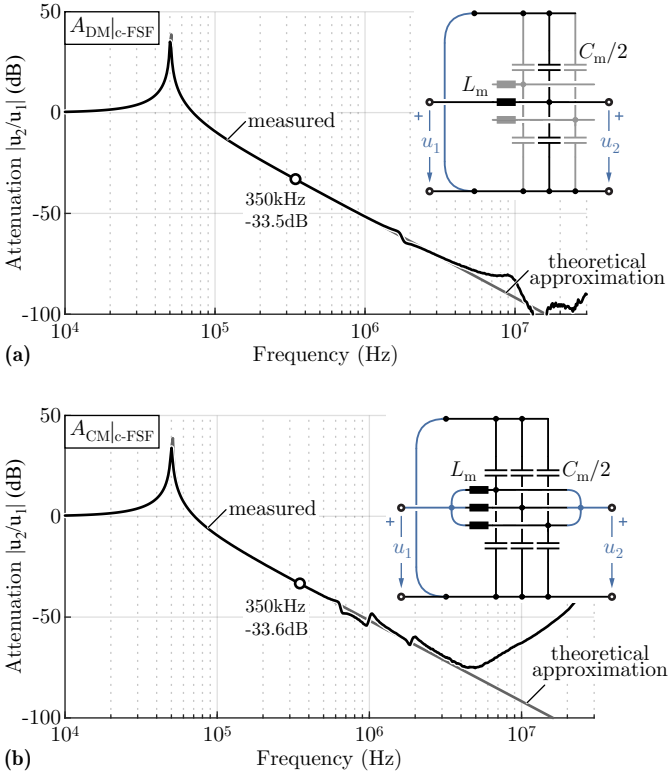


Fig. 3.10: c-FSF **(a)** DM attenuation $A_{\mathrm{DM}|\text{c-FSF}}(f)$ and **(b)** CM attenuation $A_{\mathrm{CM}|\text{c-FSF}}(f)$. The measured attenuation is compared against a theoretical approximation assuming constant $L_\mathrm{m} = 5\,\mu\mathrm{H}$ and $C_\mathrm{m} = 2\,\mu\mathrm{F}$, with respect to frequency f (cf. **Fig. 3.7(d.i)**).

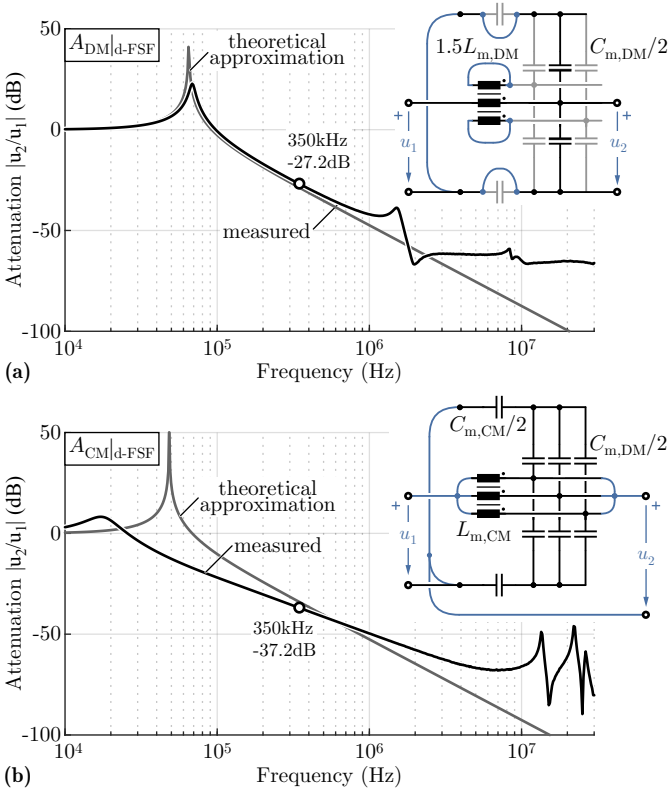


Fig. 3.11: d-FSF **(a)** DM attenuation $A_{\mathrm{DM}|\text{d-FSF}}(f)$ and **(b)** CM attenuation $A_{\mathrm{CM}|\text{d-FSF}}(f)$. The measured attenuation is compared against a theoretical approximation assuming constant $L_{\mathrm{m,DM}} = 3\,\mu\mathrm{H}$, $C_{\mathrm{m,DM}} = 2\,\mu\mathrm{F}$, $L_{\mathrm{m,CM}} = 600\,\mu\mathrm{H}$ and $C_{\mathrm{m,CM}} = 18\,\mathrm{nF}$, with respect to frequency f (cf. **Fig. 3.7(d.ii)**).

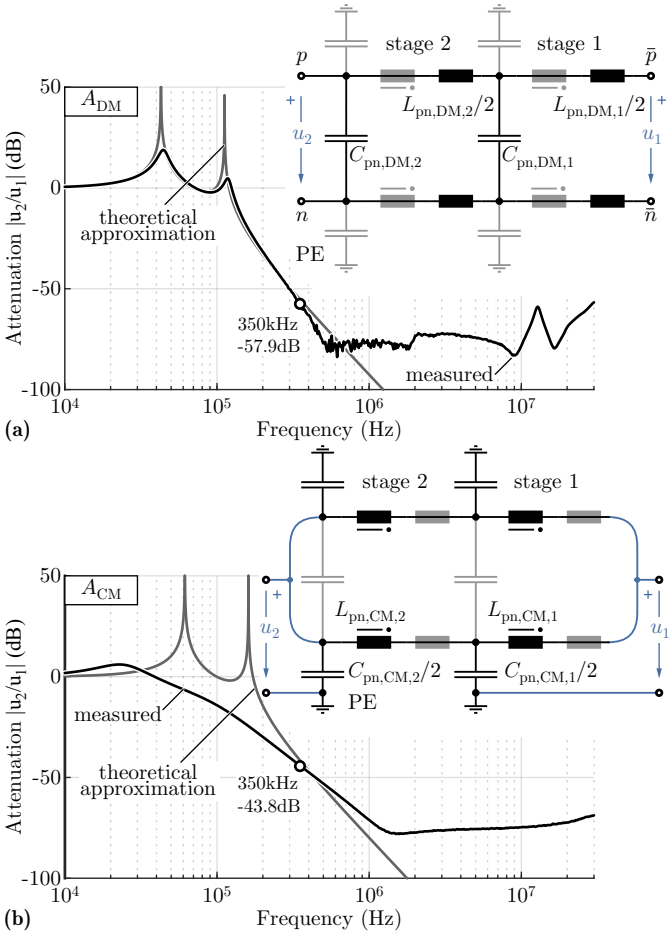


Fig. 3.12: Input filter **(a)** DM attenuation $A_{\mathrm{DM}}(f)$ and **(b)** CM attenuation $A_{\mathrm{CM}}(f)$. The measured attenuation is compared against a theoretical approximation assuming constant $L_{\mathrm{pn,DM,k}} = 0.3\,\mu\mathrm{H}$, $C_{\mathrm{pn,DM,k}} = 17.6\,\mu\mathrm{F}$, $L_{\mathrm{pn,CM,k}} = 73\,\mu\mathrm{H}$ and $C_{\mathrm{pn,CM,k}} = 35.2\,\mathrm{nF}$, with respect to frequency f (cf. **Fig. 3.7(b)**).

to the frequency dependent, effectively resistive nature of the material VAC 500F [90], used for the realization of the CM choke $L_{\mathrm{pn,CM,k}}$. The CM inductor behaves resistively for frequencies $f > 20\,\mathrm{kHz}$, thus the CM resonance of the filter is highly damped and the attenuation drops with a slope close to -60dB per frequency decade. However, a good match between the measured and theoretical CM attenuation A_{CM} is evident for the switching frequency $f_{\mathrm{s}} = 350\,\mathrm{kHz}$, for which the input filter is designed.

3.3.2 Parasitic CM Impedance Measurements

The different parasitic capacitances which conduct CM EMI currents are measured with an impedance analyser. Firstly, the motor-inverter interface cable CM parasitic capacitance c_{c} is measured (cf. **Fig. 3.1**). A shielded cable, featuring four $2.5\,\mathrm{mm}^2$ conductors, is used. In particular, the three conductors correspond to the three phases a, b and c while the fourth conductor is used exclusively for PE. In order to measure the shielded cable CM impedance, one side of the cable is connected to the impedance analyser, which measures its impedance Z over frequency f, while the other side of the cable is an open circuit as illustrated in **Fig. 3.13(b)**. The impedance measurement results for 1 m and 10 m shielded cables are plotted **Fig. 3.13(a)**. For low frequencies the capacitive behaviour c_{c} of the cable is dominant, while for high frequencies ($f > 2\,\mathrm{MHz}$ for the example case of the 10 m cable) the cables behave as a transmission line (terminated with open circuit). The impedance measurement results reveal that the total CM capacitance is proportional to the length of the cable and hence the normalized cable CM capacitance is $c'_{\mathrm{c}} = 470\,\mathrm{pF/m}$. In commercial motor drives, shielded cables have found wide acceptance, while unshielded cables are typically not preferred. The reason behind the popularity of the shielded cables is the radiated EMI noise certification [94, 95]. Namely, the shield of a shielded cable allows for a good PE connection between the inverter and the motor and mitigates the radiated EMI emissions.

Subsequently, the CM parasitic capacitance of the motor/compressor c_{m} is measured and is equal to $c_{\mathrm{m}} = 850\,\mathrm{pF}$. The 1 kW 280 krpm electric compressor [52] is shown in **Fig. 3.14(b)**, while the impedance measurement is depicted in **Fig. 3.14(a)**. A resistive load substitutes the electric compressor during the EMI measurements, for practical reasons. The CM parasitic capacitance of the resistive load is $c_{\mathrm{m}} = 650\,\mathrm{pF}$, while the impedance measurement is illustrated in **Fig. 3.14(a)**. The CM impedance of the resistive load is very

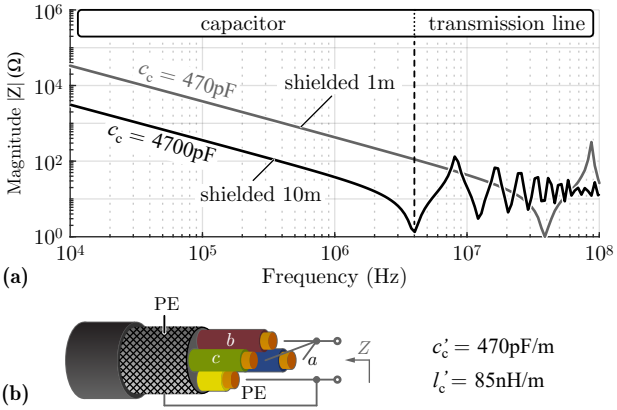


Fig. 3.13: (a) CM impedance measurement results for 1 m and 10 m shielded cables. **(b)** Cable CM impedance measurement setup, using the Keysight 4294A impedance analyser.

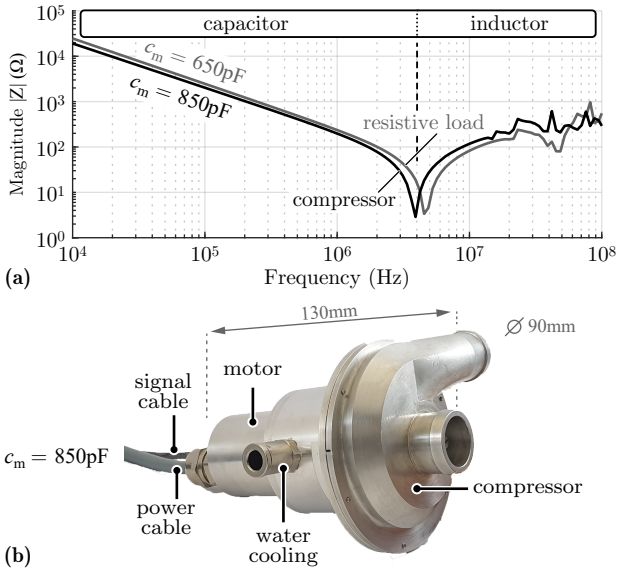


Fig. 3.14: (a) CM impedance measurement results and **(b)** 280 krpm electric compressor [52]. The Keysight 4294A impedance analyser is used.

similar to the respective motor CM parasitic impedance, therefore both loads behave similarly in terms of EMI.

It is difficult to measure the parasitic capacitance c_s of the semiconductor devices. Low-voltage GaN devices feature very compact ceramic packaging, hence c_s is very small. In this case, other factors, such as the PCB layout, the placement of the passive components and the housing, significantly affect the c_s parasitic capacitance value. For this reason, a conservative estimate of the semiconductor devices' parasitic capacitance of $c_s = 100\,\text{pF}$ is assumed.

3.3.3 Conducted EMI Measurements

In a first step, the motor voltage quality is assessed. To this end, the test setup of **Fig. 3.15** is employed, where the EMI emissions at the inverter output-side are measured. There, high output emissions are related to poor motor voltage quality. Note that, the load current flows through the three-phase LISN, which is designed for 50 Hz operation. Therefore, a low fundamental frequency of $f_m = 50\,\text{Hz}$ must be used by the inverter stage, during the EMI measurements. The output-side EMI emissions, i.e. the sum of DM and CM emissions for phase-leg a, are shown in **Fig. 3.16**. No results are shown for the DMF, because the high CM EMI emissions in this case **(3.11)**, would saturate/damage the LISN. For both c-FSF and d-FSF, the residual EMI emissions at the inverter output terminals a are in the range of 1 V. This voltage value does not electrically stress the motor and ensures a safe operation [71, 96]. However, the c-FSF achieves lower overall EMI emissions spectrum compared to the d-FSF, especially for higher frequencies. The worse d-FSF performance is partially explained by the inferior DM attenuation $A_{\text{DM}}|_{\text{d-FSF}}$ of the d-FSF (cf. **Fig. 3.11(a)**), compared to the respective DM attenuation $A_{\text{DM}}|_{\text{c-FSF}}$ of the c-FSF (cf. **Fig. 3.10(a)**).

However, the d-FSF suffers from an additional EMI performance problem, that is not captured by the attenuation measurements of **Fig. 3.11**. The DM inductance $L_{\text{m,DM}} = 3\,\mu\text{H}$ is realized as the leakage inductance of the three-phase choke. By definition the high-frequency DM current ripple that flows through the leakage inductance, generates a DM magnetic fringing-field that closes via a path through the air around the choke [97]. This DM magnetic fringing field couples additional EMI noise to the surroundings of the choke, depending on the mechanical placement of the inverter components, hence compromises the overall performance of the d-FSF. In contrast, the c-FSF does not suffer from this DM magnetic fringing filed problem. The ELP cores

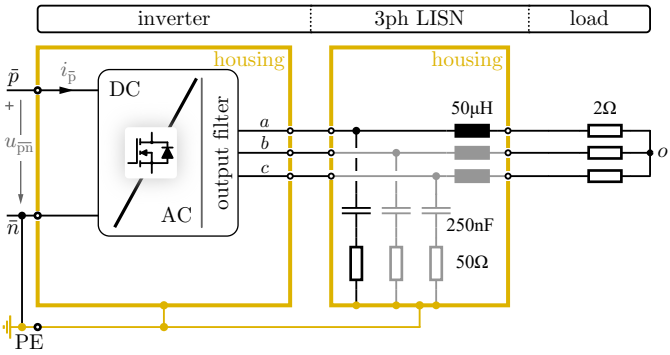


Fig. 3.15: Measurement setup for the EMI emissions at the inverter AC output-side. A three-phase LISN (Rohde&Schwarz ENV432) is placed between the inverter and the load, and an EMI test receiver (Rohde&Schwarz ESCI7) processes the LISN output *a*. No filter is installed at the input of the inverter and the negative DC rail $\bar{n}$ is shorted with PE.

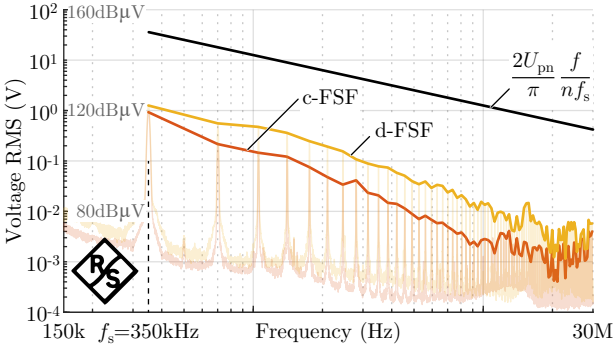


Fig. 3.16: Conducted EMI noise measurement results at the AC output-side, corresponding to the measurement setup of **Fig. 3.15**. The inverter transmits the full power and uses a fundamental frequency of $f_m = 50\,\text{Hz}$ The conducted EMI noise is measured with a IEC 61800-3 quasi-peak (QP) detector and 4 kHz step size.

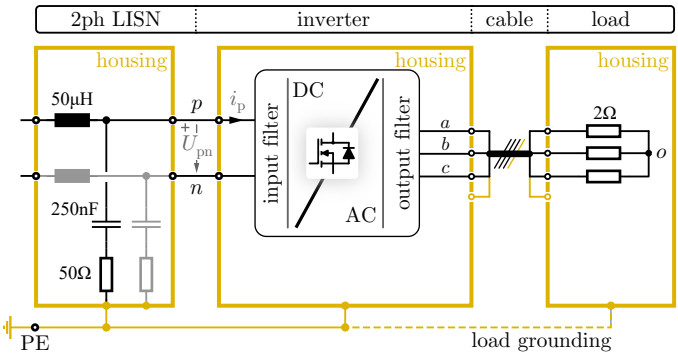


Fig. 3.17: Measurement setup for the EMI emissions at the inverter DC input-side. A two-phase LISN (Rohde&Schwarz ENV432) is placed between the inverter and the DC power supply, and an EMI test receiver (Rohde&Schwarz ESCI7) processes the LISN output *p*. The load can be either directly grounded (dashed yellow line applies) or only be grounded through the shielded cable (dashed yellow line not present).

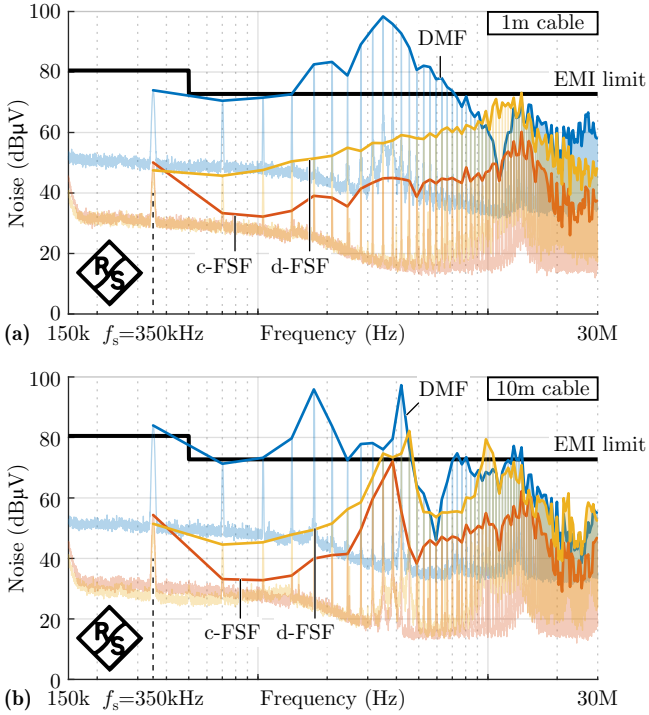


Fig. 3.18: Conducted EMI noise measurement results at the DC input-side for **(a)** 1 m shielded motor cable and **(b)** 10 m shielded motor cable. The results correspond to the measurement setup of **Fig. 3.17** and the load is grounded only through the shielded cable. The inverter transmits the full power and uses a fundamental frequency of f_m = 50 Hz. The conducted EMI noise is measured with a IEC 61800-3 quasi-peak (QP) detector and 4 kHz step size.

employed for the realization of the filter inductors L_{m}, enclose the windings and accordingly keep all the magnetic flux inside the core material.

In a second step, the inverter EMI emissions at the DC input-side are experimentally measured. To this end, the test setup of **Fig. 3.17** is employed, while the input-side EMI measurement results are shown in **Fig. 3.18**. The results are presented for all analysed output filters (i.e. DMF, c-FSF or d-FSF), and for different shielded cable lengths (i.e. 1 m or 10 m). Furthermore, the load is grounded only through the shielded cable, i.e. the dashed line of **Fig. 3.17** can be neglected.

The simple DMF (considered for comparison purposes only) exhibits the worst performance. In this case, the motor drive fails to comply with the EMI regulations, due to excessive EMI noise across the whole frequency spectrum. The reason behind the low performance of the DMF, is its lack of CM attenuation **(3.10)**. Excessive CM $\mathrm{d}u/\mathrm{d}t$ is applied to the shielded cable/motor, thus high parasitic CM currents flow through the cable/motor parasitic capacitances, towards PE. These parasitic currents form a return path from the DC input-side, thereby resulting in high CM EMI emissions at the input (cf. **Fig. 3.2(a)**). Furthermore, the severity of the input EMI emissions depends on the cable parasitic capacitance c_{c} value, which is linearly dependent on the cable length (cf. **Fig. 3.13**). In particular, the long 10 m cable causes 84dBµV of conducted noise emissions, opposed to 74dBµV caused by the short 1 m cable, at 350 kHz. Furthermore, the peaks of the EMI noise at f >1 MHz frequency range clearly correlate with the local minima of the corresponding cable impedances of **Fig. 3.13**. Besides high $\mathrm{d}u/\mathrm{d}t$ stress on the motor, a DMF results in an unwanted input-to-output CM noise mutual influence. Hence, the DMF should be avoided in WBG inverters.

The c-FSF achieves the best EMI performance and complies with EMI regulations at the input-side, regardless of the output-side cable configuration. In particular, the long 10 m cable causes a conducted noise of 54dBµV at 350 kHz, which is close to the 50dBµV caused by the short 1 m cable. Besides a good motor voltage quality, the input EMI measurements highlight a second advantage of the c-FSF. The input-side EMI emissions are significantly lower and less dependent on the cable configuration, compared to a DMF. For this reasons, the c-FSF is an excellent choice for WBG inverters.

The d-FSF achieves an intermediate performance, i.e. worse performance than the c-FSF, but significantly better performance than the simple DMF. In particular, the c-FSF and d-FSF performances are similar at 350 kHz, for both the long 10 m and the short 1 m cable. However, as the frequency increases (f >1 MHz) the d-FSF performance is degrading, resulting in roughly

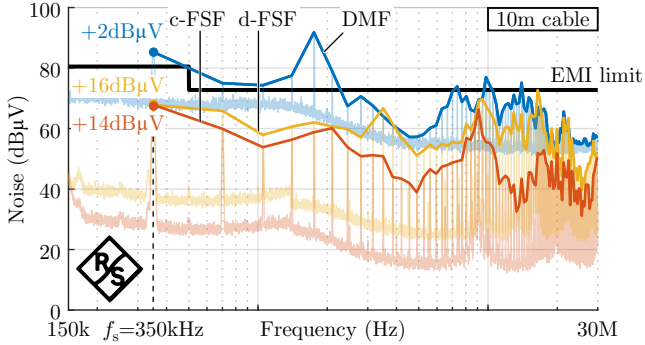


Fig. 3.19: Conducted EMI noise measurement results at the DC input-side for a 10 m shielded cable. The measurements of **Fig. 3.18(b)** are repeated, but the load is directly grounded. The comparative increase in the EMI noise at 350 kHz is highlighted in the figure.

10dBµV additional input EMI noise compared to the c-FSF. As a result, the d-FSF complies with the EMI regulations only for the short 1 m cable, but fails to comply for the long 10 m cable (at $f = 4$ MHz). The main reason behind the worse performance of the d-FSF at high frequencies is the DM fringing flux of the three-phase choke. As discussed before, this DM fringing flux couples unwanted EMI noise to components in the vicinity of the choke, thereby increasing the overall EMI emissions. Purposely placed shielding around the choke, helps to reduce the unwanted DM fringing field but does not completely eliminate the problem. The alternative three-phase choke realisation of [98, 99], with two coaxially placed toroidal cores, can reduce the DM magnetic fringing field, at the expense of added complexity. In summary, the DM fringing field is a significant drawback of the d-FSF and is especially critical for power dense systems where the thee-phase choke must be tightly packed in the inverter PCB assembly. For this reason, a c-FSF, which retains the DM flux inside the employed ELP cores, is a better option.

Finally, the effect of the load grounding technique on the input-side EMI noise profile is examined [68]. Instead of grounding the load only through the shielded cable, an alternative option, where the load is directly grounded (cf. **Fig. 3.17** - dashed yellow line applies) is investigated. The EMI measurement results corresponding to the different output filter variants are shown in **Fig. 3.19**, for a 10 m cable. It is evident that directly grounding the load increases the EMI emissions at 350 kHz, for all output filter options. By directly

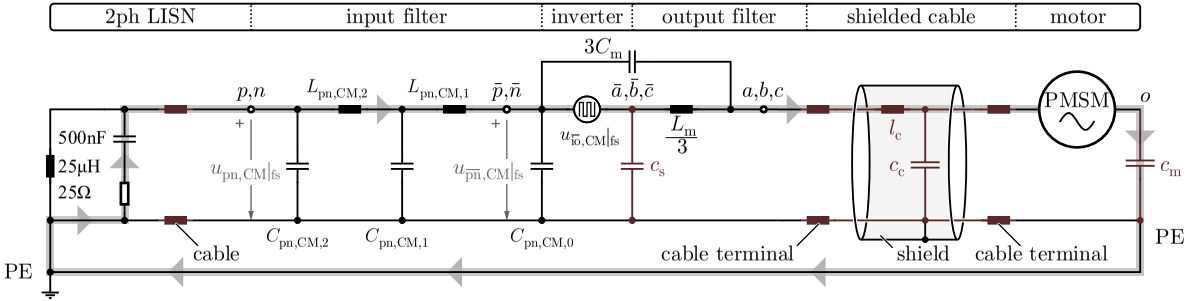


Fig. 3.20: Effect of direct motor grounding on the input-side conducted EMI emissions. Output-side parasitic CM currents can directly flow to PE (instead of returning to the inverter DC link via the cable shield), and form a return path at the input-side. These parasitic currents partially flow through the LISN (grey path), thus increase the input-side conducted EMI emissions. A two-stage input filter and a c-FSF are assumed.

grounding the load, output-side parasitic CM currents can directly flow to PE (via the PE connection and not only through parasitic capacitances), instead of returning to the inverter DC link via the cable shield. As highlighted in **Fig. 3.20** these parasitic CM currents form a return path at the input-side and partially flow through the LISN. As a result, additional CM EMI emissions are measured at the input-side. The end user of the drive system should be conscious that directly grounding the motor increases the EMI noise profile at the input-side, especially in the case of long motor cables. Ideally, the inverter should be integrated in the same housing as the motor [45, 47]. Thereby, the interconnecting cable is eliminated, resulting in an excellent EMI performance for the drive system.

3.4 Summary

High-speed motors are gaining ground compared to conventional low-speed counterparts, thanks to their low volume/weight. Simultaneously, wide-bandgap (WBG) semiconductor devices enable efficient and compact inverter solutions. These recent developments in motor and semiconductor technology allow for significantly better motor drive performance, but pose electromagnetic interference (EMI) concerns. Electromagnetic compatibility (EMC) in high-speed motor drives, supplied by an isolated DC source, is analysed in this chapter (cf. **Fig. 3.1**). A filter that complies with conducted EMI regulations is typically required at the inverter DC input-side, in order to protect the nearby equipment from EMI noise. There is however no clear mandate requiring from inverters to comply with conducted EMI regulations at the AC output-side, where only the motor is placed. The optimal input/output filter solutions, for a 1 kW inverter prototype (cf. **Fig. 3.8**), driving a 280 krpm electric compressor (cf. **Fig. 3.14(b)**), are explored in this chapter.

A full sine-wave output filter (FSF) is proposed, which features differential-mode and common-mode (DM/CM) attenuation. An FSF presents three key advantages:

(i) Sinusoidal motor currents. High-speed motors are sensitive to poor stator current quality, which induces high rotor losses. An FSF guarantees sinusoidal motor currents, thanks to its DM attenuation.

(ii) High motor reliability. The fast switching transitions of the latest WBG semiconductor devices generate high CM $\mathrm{d}u/\mathrm{d}t > 30\,\mathrm{kV/\mu s}$, which can damage the motor bearing/insulation. An FSF features CM attenuation, which mitigates high $\mathrm{d}u/\mathrm{d}t$ and protects the motor. The ex-

perimental results of **Fig. 3.16** verify the good motor voltage quality, when an FSF is installed.

(iii) Low input-side CM EMI emissions. Since the inverter housing, the motor housing and the interconnecting shielded cable are all grounded, CM emissions generated at the inverter output-side are directly mapped to the inverter input-side (i.e. input-to-output CM noise mutual influence). This problem is amplified in the case of WBG inverters, where high switching frequencies are employed. An FSF uses capacitors which are connected to the DC link. Thereby, CM emissions can return through these capacitors to the DC link and the semiconductor devices, which created the CM emissions in the first place. An FSF reduces CM emissions at the inverter output, hence simultaneously mitigates the input-side CM emissions. The experimental results of **Fig. 3.18** reveal a significant reduction of the CM EMI emissions at the input-side, when an FSF is installed at the output-side.

Two implementation variants of an FSF are comparatively evaluated, in terms of volume, losses and EMI performance:

(i) Combined full sine-wave output filter (c-FSF) of **Fig. 3.4**. This filter variant employs three individual inductors (ELP core type), each corresponding to a phase-leg.

(ii) Discrete full sine-wave output filter (d-FSF) of **Fig. 3.5**. This filter variant utilizes a single three-phase toroidal CM choke. The stray inductance of the phase windings is used as DM inductance.

For the application at hand, the d-FSF benefits from a lower volume ($11.1\,\mathrm{cm}^3$) compared to the c-FSF ($12.7\,\mathrm{cm}^3$) but generates 5 W of additional losses. Subsequent EMI measurements (cf. **Fig. 3.16** and **3.18**) reveal that the c-FSF exhibits significantly better EMI performance compared to the d-FSF. The main drawback of a d-FSF is the DM fringing magnetic field, which is caused by the leakage inductance of the three-phase choke. This fringing field results in an unwanted magnetic coupling in the vicinity of the choke, which in return causes high overall EMI emissions. In contrast, the c-FSF retains the magnetic flux inside the employed ELP cores, hence is a better solution.

4

Boost Voltage Source Inverter - Advanced Modulation Strategy

This chapter summarizes the key research findings also presented in:

M. Antivachis, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 34-53, March 2020. DOI: 10.24295/CPSSTPEA.2020.00004.

Motivation

Conventional buck-boost inverters comprise two energy conversion stages (i.e. a DC/DC stage and a DC/AC stage) and thus suffer from low efficiency. The DC/DC and the DC/AC stage are typically controlled independently. In this chapter, a new modulation strategy is presented, where the control of the DC/DC stage is synergetically combined with the control of the DC/AC stage, resulting in a higher inverter efficiency.

Executive Summary

Three-phase DC/AC power electronics converter systems used in battery-powered variable-speed drive systems or employed in three-phase mains-supplied battery charger applications usually feature two power conversion stages. In both cases, typically a DC/DC stage is attached to a three-phase DC/AC stage in order to enable buck-boost functionality and/or a wide input-output voltage operating range. However, a two-stage solution leads to a high number of switched bridge-legs and hence results in high switching losses, if the degrees of freedom available for controlling the overall system are not utilised. If the DC/DC stage is used to vary the DC link voltage with six times the AC-side frequency, a pulse width modulation (PWM) of always only one phase of the three-phase DC/AC stage is sufficient to achieve three-phase sinusoidal output currents. The clamping of two phases (denoted as 1/3 PWM) leads to a drastic reduction of the DC/AC stage switching losses, which is further accentuated by a DC link voltage which is lower than for the conventional modulation schemes. This chapter details the operating principle of a three-phase buck-boost converter system using 1/3 PWM and outlines an appropriate control system design. Subsequently, the switching losses and the voltage/current stresses on the converter components are analytically derived. There, a more than 66% reduction of the DC/AC stage switching losses is calculated without any increase of the stress on the remaining converter components. The theoretical considerations are finally verified on a hardware demonstrator, where the proposed modulation strategy is experimentally compared against several conventional modulation techniques and its clear performance advantages are validated.

Three-phase DC/AC converter systems for E-mobility applications are currently in high demand. Such three-phase converters appear either in inverter systems, such as variable-speed motor drives [47,48], or in three-phase PWM rectifier systems, used for fast battery charging [7, 100]. Since both types of power electronics systems are typically installed on a vehicle it is required that the converters are highly efficient while maintaining a high power density. At the same time, three-phase inverters and/or rectifiers in E-mobility applications have to cope with a wide input-output voltage range.

In particular, a motor drive supplied by a battery must generate a controllable three-phase output AC voltage in an amplitude range $\hat{U}_{\mathrm{m}} = 0...\hat{U}_{\mathrm{m,max}}$. Simultaneously, the input battery DC voltage varies depending on the state-of-charge, loading and temperature between $U_{\mathrm{b}} = U_{\mathrm{b,min}}...U_{\mathrm{b,max}}$. Accordingly, the operation area of the inverter system is defined by all possible combinations of the DC input and the AC output voltage. As the motor line-

to-line voltage amplitude $\hat{U}_{\mathrm{m,LL}} = \sqrt{3}\hat{U}_{\mathrm{m}}$ can exceed the battery voltage U_{b}, a boost-type DC/DC converter stage that generates an adequately high DC link voltage u_{DC}, is typically placed in front of the buck-type three-phase DC/AC converter stage as shown in **Fig. 4.1(a)**.

In analogy, three-phase fast battery chargers also have to operate within a wide voltage operating area. There, the output DC battery voltage varies in a range $U_{\mathrm{b}} = U_{\mathrm{b,min}}...U_{\mathrm{b,max}}$ depending on the vehicle type and charging status, while the input three-phase grid AC voltage can also fluctuate in a range $\hat{U}_{\mathrm{m}} = \hat{U}_{\mathrm{m,min}}...\hat{U}_{\mathrm{m,max}}$. The level of U_{b} can be lower than the input grid line-to-line voltage amplitude $\hat{U}_{\mathrm{m,LL}} = \sqrt{3}\hat{U}_{\mathrm{m}}$. Therefore, a buck-type DC/DC stage that adapts the DC link voltage u_{DC} to U_{b} is typically placed after the three-phase boost-type PFC rectifier stage as is shown in **Fig. 4.1(b)**. All in all, both systems, i.e. the variable-speed motor drive and the battery charging system, feature the same two-stage converter structure, just with opposite direction of the power flow. Unfortunately, this two-stage solution suffers from high switching losses and large heatsink volume originating from the fact that both converter stages are typically independently modulated with a high switching frequency. In the following, the example of a variable-speed motor drive system shown in **Fig. 4.1(a)** is analysed in detail, however, the same considerations also apply to the battery charging system of **Fig. 4.1(b)**.

For conventional sinusoidal PWM [55] of the DC/AC stage shown in **Fig. 4.2(a.ii)**, purely sinusoidally varied duty cycles are employed for all phases (i.e. no third harmonic component [60] is injected). This modulation strategy results in continuous switching of all three DC/AC stage half-bridges (in the following denoted as 3/3 PWM) and accordingly leads to high switching losses (cf. **Fig. 4.2(a.i)**). At the same time, 3/3 PWM requires a high DC link voltage u_{DC} equal or larger than $2\hat{U}_{\mathrm{m}}$ ($\hat{U}_{\mathrm{m}}$ denotes the motor phase voltage amplitude) which is generated by the DC/DC stage, as shown in **Fig. 4.2(a.iii)**. In order to reduce the switching losses, different clamping methods have been proposed in literature such as discontinuous PWM [56, 61], which always operates only two out the three DC/AC half-bridges (denoted as 2/3 PWM, cf. **Fig. 4.2(b.i)**) and results at least in a 33% reduction of the DC/AC stage switching losses [62]. Typical duty cycles for 2/3 PWM are illustrated in **Fig. 4.2(b.ii)**. There, negative clamping is used, i.e. at any given point in time one of the low-side switches of the DC/AC stage is permanently turned-on and clamps the corresponding phase to the negative DC rail. It is noted that 2/3 PWM employs non-sinusoidal duty cycles and/or output phase voltages of the DC/AC stage (measured against the negative DC

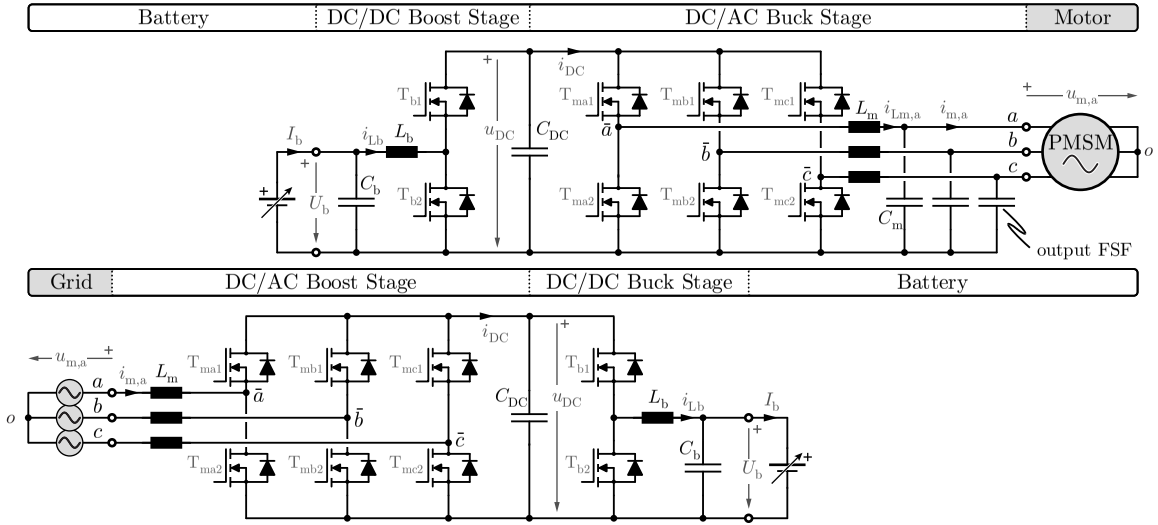


Fig. 4.1: For a variable speed motor drive application **(a)** supplied by a battery, a DC/DC boost-type converter stage is typically placed in front of the DC/AC converter stage in order to adapt the battery voltage U_b to the DC link voltage u_DC required for generating the (speed dependent) motor voltage $\hat{U}_\mathrm{m}$. For a battery charging application **(b)** supplied from a three-phase AC grid, the battery voltage U_b can be higher or lower than the grid line-to-line voltage $\sqrt{3}\hat{U}_\mathrm{m}$. For this reason, a buck-type DC/DC stage is placed after the boost-type DC/AC (rectifier) stage in order to generate a DC output voltage U_b lower than the DC link voltage u_DC.

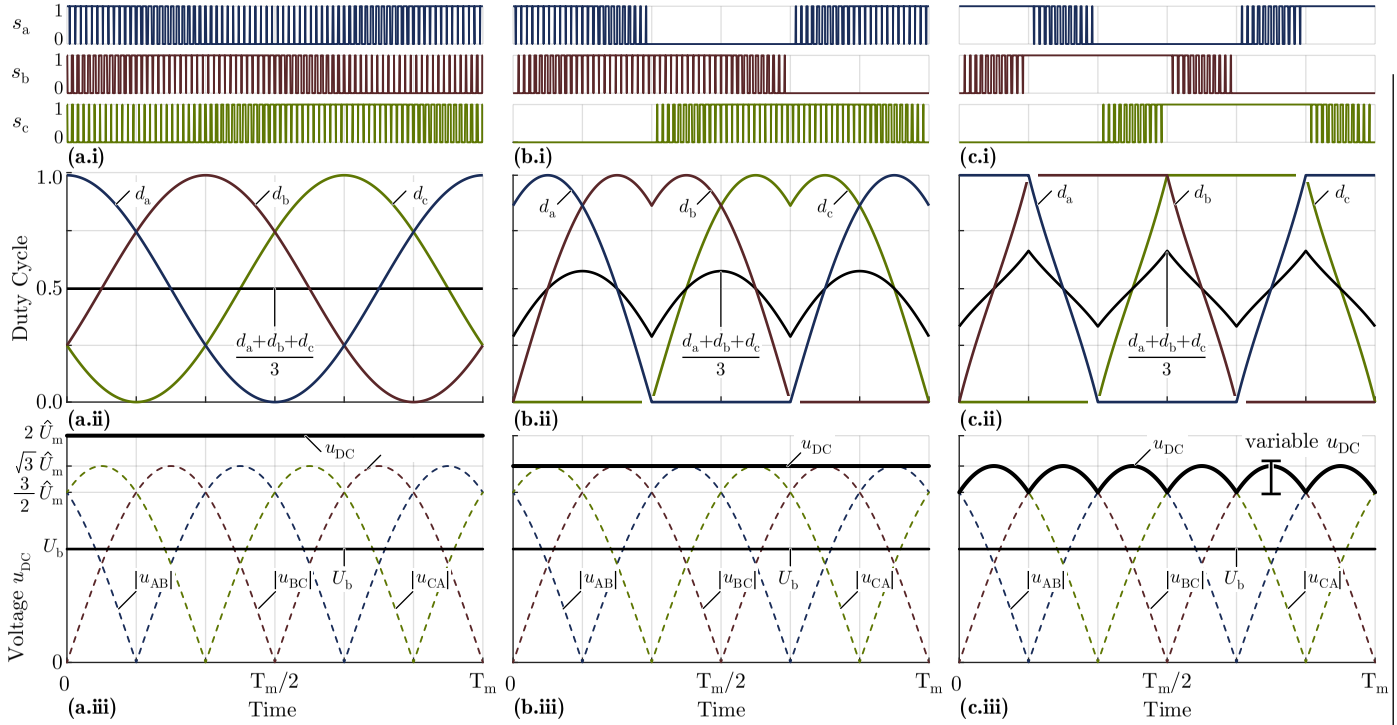


Fig. 4.2: PWM strategies of a three-phase two-level DC/AC inverter. **(i)** Gate signals of the three DC/AC stage bridge-legs, **(ii)** duty cycles of the bridge-legs and **(iii)** DC link voltage u_{DC}. **(a)** Characteristic waveforms of 3/3 PWM: purely sinusoidally varying duty cycles, continuous switching of all three-phases, and a high DC link voltage $u_{DC} = 2\hat{U}_m$. **(b)** Characteristic waveforms of 2/3 PWM: always two out of the three-phases are switched and the third phase is clamped to the negative DC link rail. The DC link voltage can be lowered to $u_{DC} = \sqrt{3}\hat{U}_m$. **(c)** Characteristic waveforms of 1/3 PWM: always only one out of the three-phases is switched. The DC link voltage is varying over time, has a six-pulse shape (resulting from proper control of the DC/DC stage) and is equal to the largest instantaneous motor line-to-line voltage.

rail) but still allows to generate a purely sinusoidal three-phase line-to-line voltage system thanks to the open motor star point o (cf. **Fig. 4.1(a)**). Besides lower switching losses, 2/3 PWM results in a lower DC link voltage requirement for the same output voltage modulation range, compared to 3/3 PWM and accordingly leads to a lower voltage stress on the converter components. In particular, the DC link voltage in the case of 2/3 PWM should be equal or higher than the line-to-line motor voltage amplitude $u_{\mathrm{DC}} \geq \sqrt{3}\hat{U}_{\mathrm{m}}$ as depicted in **Fig. 4.2(b.iii)**.

Both, 3/3 PWM and 2/3 PWM, employ a constant DC link voltage u_{DC} and the DC/DC stage and DC/AC stage are controlled independently. However, a constant DC link voltage u_{DC} is actually not required. As shown in [101–105] the modulation of the DC/DC and the DC/AC stage can be synergetically combined which results in a significant performance improvement. If the DC/DC stage is used to vary the DC link voltage with six times the output frequency f_{m}, a PWM of always only one phase of the DC/AC stage is sufficient to achieve three-phase sinusoidal output currents. The clamping of two phases (denoted as 1/3 PWM in the following) leads to a 66% reduction of the DC/AC stage switching losses compared to 3/3 PWM [106–109] and the corresponding DC link voltage is lower than for the conventional modulation schemes. The gating signals and the duty cycles for 1/3 PWM are plotted in **Fig. 4.2(c.i)** and **(c.ii)**, respectively, while the time-varying DC link voltage is depicted in **Fig. 4.2(c.iii)**.

In the following, the 1/3 PWM strategy is explained in more detail (**Sec. 4.1**) and an appropriate control structure for the overall converter system is presented. Subsequently, the switching losses of 1/3 PWM are analytically derived and compared against traditional PWM modulation strategies in **Sec. 4.2** and **4.3**. Furthermore, the voltage and/or current stresses on the different converter components are calculated in order to allow a complete assessment of the 1/3 PWM scheme. In **Sec. 4.4**, a versatile hardware demonstrator is assembled and tested, employing either 1/3 PWM, 2/3 PWM or 3/3 PWM which enables a comprehensive comparison among the different modulation strategies. Accordingly, the drastic switching loss reduction achieved by means of 1/3 PWM is experimentally verified. Finally, a summary is given in **Sec. 4.5**.

4.1 Modulation Strategies

4.1.1 1/3 PWM Modulation Strategy

The DC/AC stage operated with 1/3 PWM generates the three-phase sinusoidal motor voltages which are plotted in **Fig. 4.4(c)**

$$\begin{aligned} u_{\mathrm{m,a}}(t) &= u_{\mathrm{ao}} = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t) \\ u_{\mathrm{m,b}}(t) &= u_{\mathrm{bo}} = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t - \frac{2\pi}{3}) \\ u_{\mathrm{m,c}}(t) &= u_{\mathrm{co}} = \hat{U}_{\mathrm{m}} \cos(\omega_{\mathrm{m}} t + \frac{2\pi}{3}), \end{aligned} \tag{4.1}$$

where $\omega_{\mathrm{m}} = 2\pi f_{\mathrm{m}}$ is the fundamental angular velocity. 1/3 PWM features a variable DC link voltage $u_{\mathrm{DC}}(t)$ generated by the preceding DC/DC stage, whose shape is always defined by the largest absolute motor line-to-line voltage u_{ab}, u_{bc} or u_{ca}. Therefore, the DC link voltage has a six-pulse shape that varies between a minimum value of $\sqrt{3}\hat{U}_{\mathrm{m}} \cos(\frac{\pi}{6}) = \frac{3}{2}\hat{U}_{\mathrm{m}}$ and a maximum value of $\sqrt{3}\hat{U}_{\mathrm{m}}$. The accordingly required duty cycle d of the DC/DC stage high-side switch is shown in **Fig. 4.3(b)** and the gating signal is plotted in **Fig. 4.3(a)**. In **Fig. 4.3(d)** the battery current I_{b} and the DC link current $\bar{i}_{\mathrm{DC}}$ are depicted. The local average value of the DC link current $\bar{i}_{\mathrm{DC}}$ also fluctuates because the DC link voltage u_{DC} is not constant. The product $p(t) = u_{\mathrm{DC}}(t) \cdot \bar{i}_{\mathrm{DC}}(t)$ of DC link voltage and current is constant in order to ensure a constant instantaneous power delivery $p(t)$ to the motor.

Using the 1/3 PWM scheme, the DC/AC stage is controlled by the duty cycles d_{a}, d_{b}, d_{c} depicted in **Fig. 4.4(b)**. For the first 60° interval of the fundamental period, (highlighted in grey, cf. **Fig. 4.4**), where the line-to-line voltage $|u_{\mathrm{ca}}|$ is the largest, the duty cycle of phase a is $d_{\mathrm{a}} = 1$ (i.e. phase a is clamped to the positive DC link rail), the duty cycle of phase c is $d_{\mathrm{c}} = 0$ (i.e. phase c is clamped to the negative DC link rail), while only the duty cycle of the middle phase b varies within $d_{\mathrm{b}} = 0...1$. This means that the six-pulse shaped DC link voltage u_{DC} is directly applied between phases a and c i.e. $u_{\mathrm{a\bar{c}}} = u_{\mathrm{DC}}$ and only phase b i.e. the phase with the middle voltage value, is actively switched with PWM. Hence, neglecting the reactive voltages/currents of the L_{m}-C_{m} filter, the motor line-to-line voltage results as $u_{\mathrm{ac}} \simeq u_{\mathrm{a\bar{c}}} = u_{\mathrm{DC}}$. Therefore, during the first 60° an appropriate sinusoidal line-to-line voltage is applied between the motor terminals a and c, even though in the DC/AC stage no switching action for the corresponding phases a and c is taking place. Accordingly, only the remaining motor terminal b voltage must be actively generated by the DC/AC stage by means of

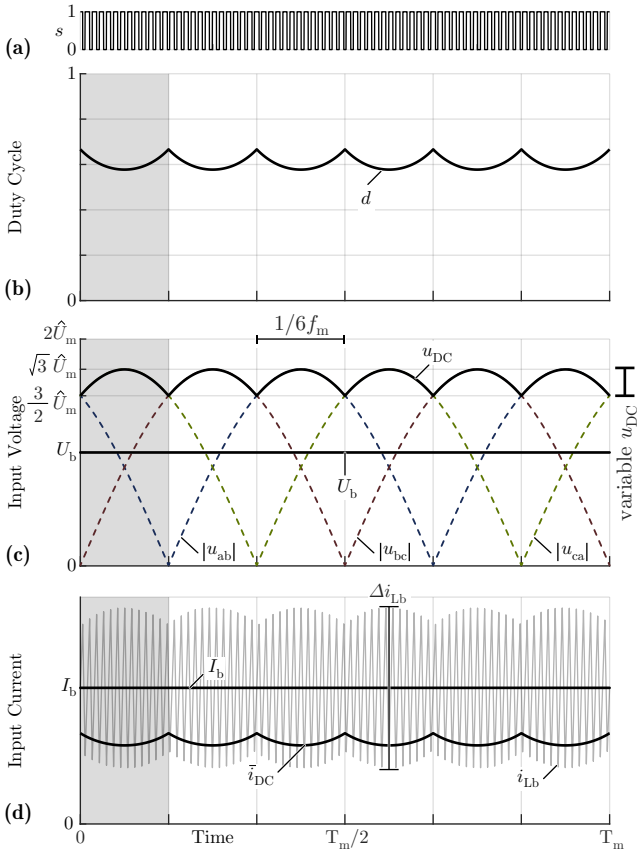


Fig. 4.3: Characteristic waveforms of the DC/DC stage, for 1/3 PWM operation of the converter system of **Fig. 4.1(a)**, where a low switching frequency f_s is assumed for clear visualisation. **(a)** Gate signal of the DC/DC stage high-side switch and **(b)** duty cycle. **(c)** Variable DC link voltage u_{DC} featuring a six-pulse shape and **(d)** battery current and (local average) DC link current.

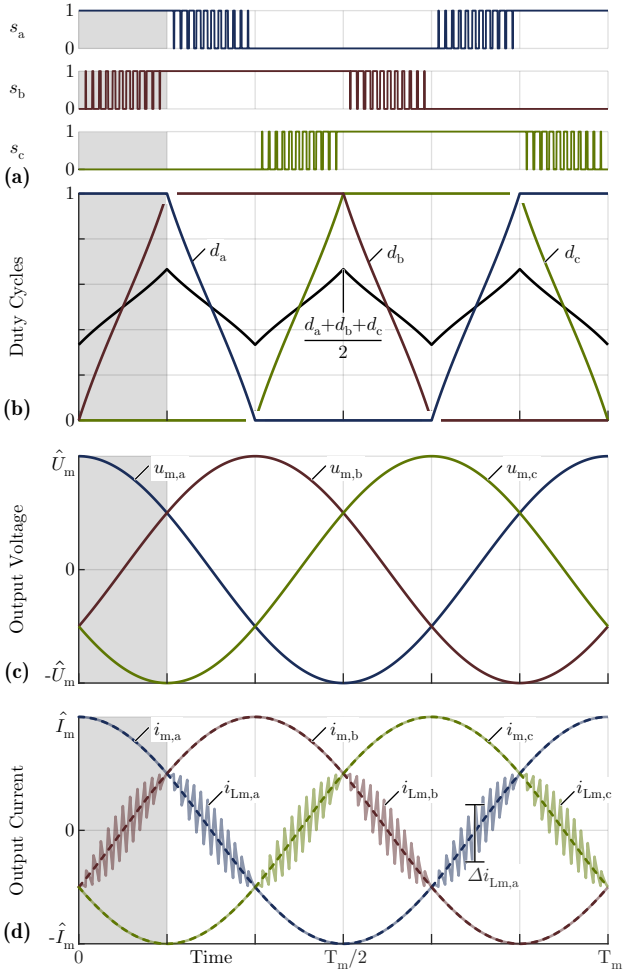


Fig. 4.4: Characteristic waveforms of the DC/AC stage, for 1/3 PWM operation of the converter system of **Fig. 4.1(a)**, where a low switching frequency f_s is assumed for clear visualisation. **(a)** Gate signals and **(b)** duty cycles. **(c)** motor terminal voltages and **(d)** motor phase currents and filter inductor currents.

switching phase b. It is noted that, the open star connection of the motor o, $u_{\mathrm{m,a}} + u_{\mathrm{m,b}} + u_{\mathrm{m,c}} = 0$, is a prerequisite for 1/3 PWM, since it allows to generate a three-phase voltage system by actively controlling only two voltages at any point in time. For the considered example, only the line-to-line voltage $u_{\mathrm{a\bar{c}}}$ and the phase voltage $u_{\mathrm{\bar{b}}}$ are actively controlled. The same principle applies for the remaining 60° intervals of the fundamental period T_{m}, while the roles of phases a, b and c are exchanged. The sinusoidal motor currents and filter inductor L_{m} currents are plotted in **Fig. 4.4(d)**. As can be noticed, always only the inductor current of the middle (PWM operated) phase exhibits a pronounced high-frequency current ripple, while the two other inductors conduct smooth sinusoidal motor currents, which in turn also reduces the high-frequency losses in the filter inductors. The DC/AC stage inductor current ripple shape is unique to the full sine-wave filter (FSF) of **Fig. 4.1(a)**. This FSF belongs to the family of DC link referenced filters, where the filter capacitors C_{m} are connected/referenced to the negative DC link rail. A complete analysis of FSFs can be found in **Chapter. 3**.

In the following, the analytic calculation of fundamental quantities and/or waveforms for 1/3 PWM is performed. In a first step, the time behaviour of the DC link voltage u_{DC} is formulated. To this end, the maximum instantaneous line-to-line motor voltage is required which based on **(4.1)** has a six-pulse shape and is

$$u_{\mathrm{m,LL,max}}(t) = u_{\mathrm{m,max}}(t) - u_{\mathrm{m,min}}(t), \tag{4.2}$$

where $u_{\mathrm{m,max}}(t) = \max\left\{u_{\mathrm{m,a}}, u_{\mathrm{m,b}}, u_{\mathrm{m,c}}\right\}$ and $u_{\mathrm{m,min}}(t) = \min\left\{u_{\mathrm{m,a}}, u_{\mathrm{m,b}}, u_{\mathrm{m,c}}\right\}$. The DC link voltage is subsequently derived (cf. **Fig. 4.3(c)**) as

$$u_{\mathrm{DC}}(t) = \begin{cases} U_{\mathrm{b}}, & u_{\mathrm{m,LL,max}}(t) \leq U_{\mathrm{b}} \\ u_{\mathrm{m,LL,max}}(t), & u_{\mathrm{m,LL,max}}(t) > U_{\mathrm{b}}. \end{cases} \tag{4.3}$$

As long as the actual maximum line-to-line motor voltage $u_{\mathrm{m,LL,max}}(t)$ is below the battery voltage U_{b}, the boost-type DC/DC converter cannot control the DC link voltage to a six-pulse shape and thus clamps the DC link voltage $u_{\mathrm{DC}} = U_{\mathrm{b}}$ by permanently turning-on the high-side switch T_{b1}. On the other hand, as soon as the line-to-line motor voltage amplitude $\sqrt{3}\hat{U}_{\mathrm{m}}$ exceeds the battery voltage U_{b} (for higher speeds), the DC/DC stage can control the DC link voltage to the six-pulse voltage $u_{\mathrm{DC}} = u_{\mathrm{m,LL,max}}(t)$. The duty cycle of the high-side switch T_{b1} of the DC/DC stage is then given as (cf. **Fig. 4.3(a)** and **(b)**)

$$d(t) = \frac{U_{\mathrm{b}}}{u_{\mathrm{DC}}(t)}. \tag{4.4}$$

In a second step, the duty cycles d_a, d_b and d_c of the DC/AC stage for 1/3 PWM are calculated, which is based on the same algorithm used for 2/3 PWM [59] (cf. **Fig. 4.2(b)**). The duty cycle of each phase ranges within 0...1 and is split into a differential-mode (DM) and a common-mode (CM) part. The DM part is purely sinusoidal and is calculated for phases *a*, *b* and *c* based on **(4.1)** and **(4.3)** as

$$d_{\{a,b,c\},DM}(t) = \frac{u_{m,\{a,b,c\}}(t)}{u_{DC}(t)}. \tag{4.5}$$

The CM part or offset of the duty cycle, which is common to all three phases, is

$$d_{CM}(t) = -\min\left\{d_{a,DM}(t), d_{b,DM}(t), d_{c,DM}(t)\right\}. \tag{4.6}$$

The total duty cycle is the sum of both components and lies within $[0, 1]$

$$d_{\{a,b,c\}}(t) = d_{\{a,b,c\},DM}(t) + d_{CM}(t). \tag{4.7}$$

Based on these duty cycle calculations, when the instantaneous motor line-to-line voltage is lower than the battery voltage $u_{m,LL,max}(t) \leq U_b$, the DC/DC stage clamps the DC link voltage to the battery voltage $u_{DC} = U_b$. Then, the DC/AC stage operates with 2/3 PWM resulting in the waveforms shown in **Fig. 4.2(b)**. On the other hand, for $u_{m,LL,max}(t) \geq U_b$, the DC/DC stage is activated and generates a DC link voltage $u_{DC} = u_{m,LL,max}(t)$, which in case of $\hat{U}_m \geq 2U_b/3$ shows a six-pulse shape. Then, the DC/AC stage is operating with 1/3 PWM (cf. **Fig. 4.4(b)**). In other words, 1/3 PWM results from the generalization of 2/3 PWM, since the same algorithm (cf. **Fig. 4.5**) is used for the calculation of the DC/AC stage duty cycles throughout the whole DC link operation range. Depending on the relationship between the battery voltage U_b and the motor voltage $\hat{U}_m$, the converter can transition continuously from 2/3 PWM to 1/3 PWM and vice-versa.

A complete control block diagram for 1/3 PWM is conceptualised in **Fig. 4.5**. There, a standard cascaded speed-torque (speed-current) motor controller in a d-q reference frame is employed, in order to maintain the motor speed ω at the desired setpoint ω^*. The three-phase motor currents $i_{m,a}$, $i_{m,b}$, $i_{m,c}$, as well as the motor rotation angle ε and the motor speed ω are measured and fed as input to the motor controller. The motor controller outputs the motor terminal voltage references $u^*_{m,a}$, $u^*_{m,b}$, $u^*_{m,c}$, which the inverter must generate. Based on these reference voltages, the DC/DC stage duty cycle d is calculated employing **(4.2)**-**(4.4)**. At the same time, the DC/AC stage duty cycles d_a, d_b and d_c are derived based on **(4.5)**-**(4.7)**.

A transition example from 2/3 PWM to 1/3 PWM is shown in **Fig. 4.6**. There, the motor voltage and current is gradually increased, as highlighted

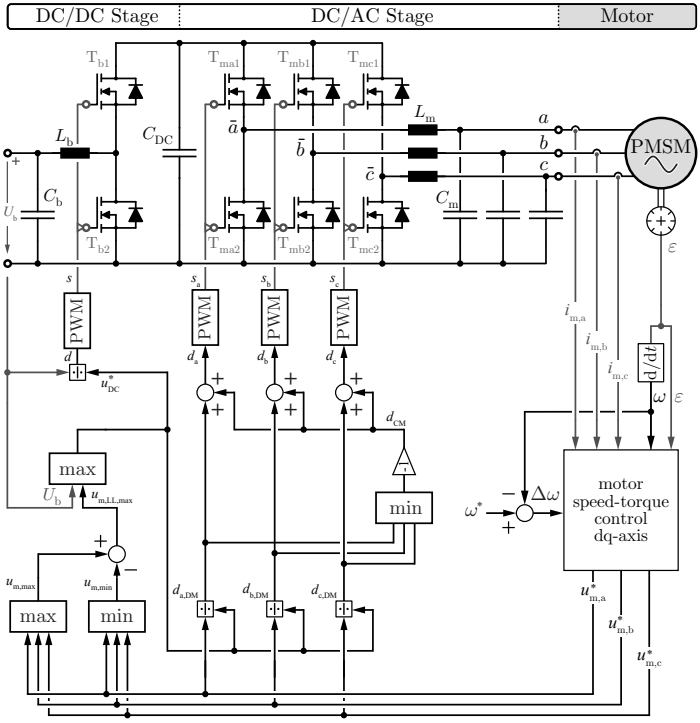


Fig. 4.5: Control block diagram for 1/3 PWM. The cascaded speed/torque motor controller maintains the motor speed ω at the desired setpoint ω^*. In return, the motor controller outputs the three motor terminal voltage references $u^*_{\mathrm{m},\{\mathrm{a,b,c}\}}$ that the inverter must generate. Based on these voltage references, the corresponding duty cycles of the DC/DC stage d and DC/AC stage $d_{\{\mathrm{a,b,c}\}}$ are derived.

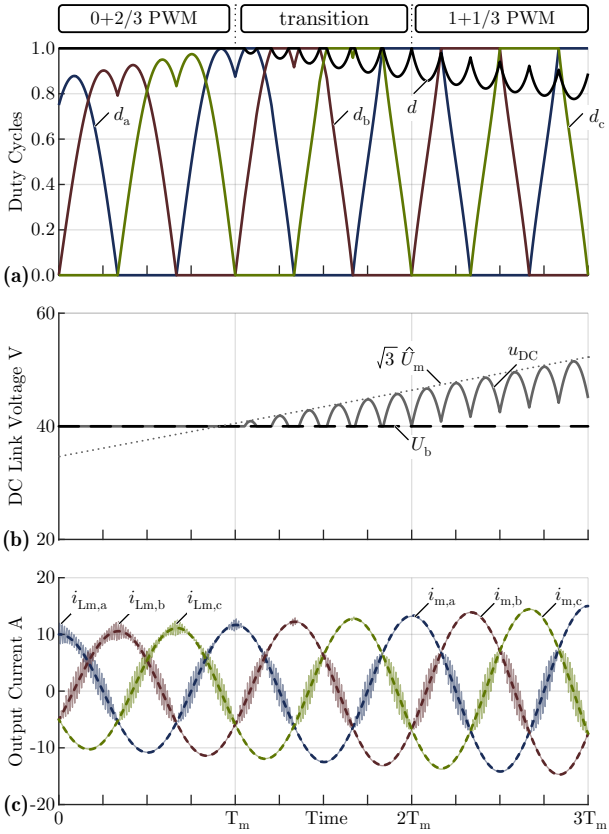


Fig. 4.6: Simulation results showing a smooth transition from 2/3 PWM to 1/3 PWM, where the motor voltage is gradually increased. When the motor voltage is low ($\hat{U}_m \leq U_b/\sqrt{3}$), 2/3 PWM is employed. When the motor voltage is high ($\hat{U}_m > 2U_b/3$), exclusively 1/3 PWM is used. During the transition, where $U_b/\sqrt{3} < \hat{U}_m \leq 2U_b/3$ is valid, 2/3 PWM and 1/3 PWM are occurring alternately.

in **Fig. 4.6(c)**. During $t < T_m$, the motor voltage is low, $\hat{U}_m \leq U_b/\sqrt{3}$, therefore exclusively 2/3 PWM is employed. In particular, the DC/DC stage is deactivated, which means that the battery is directly connected to the DC link $u_{DC} = U_b$. This operating regime is denoted as 0+2/3 PWM in **Fig. 4.6**, '0' indicating that the DC/DC stage is not switched and '2/3' denoting that two out of three DC/AC half-bridges are switched. In contrast, for $t > 2T_m$, the motor voltage is high, $\hat{U}_m \geq 2U_b/3$, therefore exclusively 1/3 PWM is employed. In this case, the DC/DC stage is activated and controls the DC link voltage to $u_{DC} = u_{m,LL,max}(t)$. This operating regime is denoted as 1 + 1/3 PWM, with '1' indicating that the DC/DC stage is switched. During $T_m < t \leq 2T_m$, the motor voltage is $U_b/\sqrt{3} < \hat{U}_m \leq 2U_b/3$ and both modulation schemes are alternatively employed, while a smooth transition between the two modulation regimes is achieved without unwanted transients.

It is noted that during 1/3 PWM operation of the DC/AC stage, the motor voltage cannot be abruptly increased. In order to increase the motor line-to-line voltage, a higher, six-pulse shaped DC link voltage $u_{DC}(t)$ must first be generated by the DC/DC stage. Therefore, the maximum rate at which the motor line-to-line voltage can be increased is defined by the dynamic response of the DC/DC stage. Consequently, 1/3 PWM exhibits a limited control bandwidth of the motor line-to-line voltage, depending on the value of the DC link capacitor C_{DC}. A large C_{DC} value would slow down the dynamics of the DC/DC stage and hence would impede the converter from quickly changing the motor line-to-line voltage. For this reason, a careful selection of the DC link capacitor C_{DC} is necessary, as described later in **Sec. 4.2**. 1/3 PWM is hence not suitable for drive systems where high dynamic response of the motor torque/speed is required. Instead, 1/3 PWM is more suitable for drive systems with low dynamics that are mostly operated under steady state conditions, as compressor drives.

4.1.2 Alternative 2/3 PWM Modulation Strategy

Sec. 4.1 focuses on a negative (n) clamping 2/3 PWM algorithm **(4.5)-(4.7)**, which is accordingly extended for 1/3 PWM. However, an alternative positive&negative (p&n) clamping 2/3 PWM scheme [56] could be used, i.e. at any given point in time one of the high-side or low-side switches of the DC/AC stage is permanently turned-on and clamps the corresponding phase to the positive or the negative DC rail, respectively. Typical duty cycles and gate signals for such 2/3 PWM scheme are depicted in **Fig. 4.7**. The p&n clamping 2/3 PWM duty cycle calculation algorithm is similar to the respec-

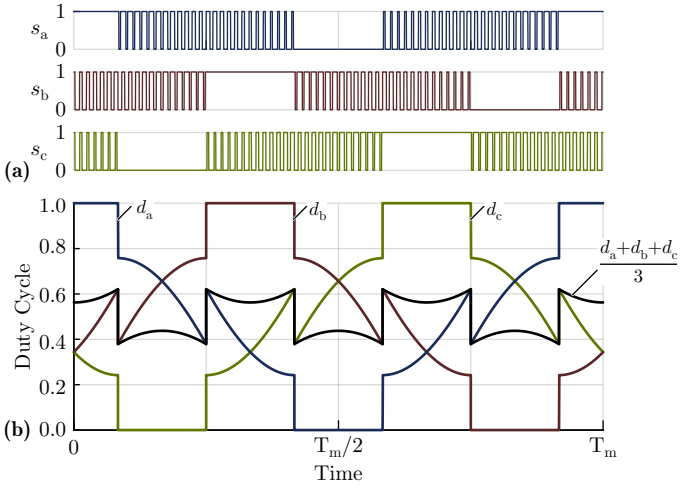


Fig. 4.7: Alternative 2/3 PWM strategy, with positive&negative (p&n) clamping, of a three-phase two-level DC/AC inverter. **(a)** Gate signals and **(b)** non-sinusoidal duty cycles of the DC/AC stage.

tive calculations for the negative clamping 2/3 PWM scheme. Namely, the DC/AC stage duty cycles are split into a DM and a CM part. The DM part is purely sinusoidal and is given by **(4.5)**, while the CM part is

$$\begin{aligned} d_{\mathrm{CM}} = 0.5 + \left[0.5 - \max\left\{|d_{\mathrm{a,DM}}|, |d_{\mathrm{b,DM}}|, |d_{\mathrm{c,DM}}|\right\}\right] \cdot \\ \operatorname{sign}\left[\max\left\{d_{\mathrm{a,DM}}, d_{\mathrm{b,DM}}, d_{\mathrm{c,DM}}\right\} - |\min\left\{d_{\mathrm{a,DM}}, d_{\mathrm{b,DM}}, d_{\mathrm{c,DM}}\right\}|\right]. \end{aligned} \tag{4.8}$$

The main advantage of p&n clamping 2/3 PWM is that it ensures equal current distributions between the high-side and the low-side semiconductor devices of the DC/AC stage

$$I_{\mathrm{Tma1,RMS}}|_{2/3\,\mathrm{PWM}} = I_{\mathrm{Tma2,RMS}}|_{2/3\,\mathrm{PWM}} = \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\frac{1}{\sqrt{2}}. \tag{4.9}$$

Thereby, the drive system can always conduct the nominal motor current amplitude $\hat{I}_{\mathrm{m}}$ without overstressing the low-side switches $T_{\mathrm{m\{a,b,c\}2}}$ and hence ensures nominal motor torque during motor acceleration, starting from standstill. In contrast, n clamping 2/3 PWM suffers from an asymmetric current stress for low modulation indexes M, as described in **Sec. 4.2**.

The disadvantage of the p&n clamping 2/3 PWM is that the discontinuous duty cycles (cf. **Fig. 4.7**) lead to discontinuous DC/AC stage output voltages.

Tab. 4.1: Motor drive specifications. The worst case operating condition of the two-stage DC/AC converter, where the highest component stresses appear, is highlighted in bold.

Battery voltage	U_b	**40 V**...60 V
Inverter fundamental freq.	f_m	0 Hz...**5 kHz**
Inverter power	P	0 W...**500 W**
Motor speed	n	0 rpm...**280 krpm**
Motor voltage amplitude	$\hat{U}_\mathrm{m}$	0 V...**40 V** (phase, PK)

The discontinuities of the output voltage (i.e. abrupt CM voltage steps) can excite the FSF of **Fig. 4.1(a)**, hence p&n clamping 2/3 PWM is not suitable for the application at hand. In contrast, n clamping 2/3 PWM features continuous duty cycles (cf. **Fig. 4.2(b.ii)**), thus can be used for a DC/AC stage with an FSF.

4.2 Component Stresses for $\cos(\phi) = 1$

In this section, the switching losses and the voltage/current stresses on the different converter components are calculated for the drive system with the specifications of **Tab. 4.1**. The analysis is performed for 1/3 PWM as well as for the conventional 2/3 PWM (negative clamping) and 3/3 PWM over the whole operating range of the motor. For the considered application example, the battery voltage ranges within $U_\mathrm{b} = 40\,\mathrm{V}...60\,\mathrm{V}$, however, for the following analysis the lowest battery voltage $U_\mathrm{b} = 40\,\mathrm{V}$ is considered, where the highest current stress in the DC/DC stage appears. The motor voltage ranges within $\hat{U}_\mathrm{m} = 0\,\mathrm{V}...40\,\mathrm{V}$ (phase amplitude), while the maximum motor voltage $\hat{U}_\mathrm{m} = 40\,\mathrm{V}$ operation yields the highest component stresses. For the sake of simplicity, a resistive load R is assumed, hence a unity power factor (PF) $\cos(\phi) = 1$ is obtained. An analysis for a non-unity power factor $\cos(\phi) < 1$ is given in **Sec. 4.3** In order to further simplify the analysis, the current ripple of the DC/DC stage inductor L_b and the DC/AC stage filter inductors L_m is neglected, unless stated otherwise.

In a typical DC/AC two-level inverter, the modulation index is defined as the ratio between motor phase voltage amplitude and half the DC link voltage

$$M_\mathrm{m} = \frac{\hat{U}_\mathrm{m}}{\frac{1}{2}u_\mathrm{DC}}, \tag{4.10}$$

and ranges within $0...2/\sqrt{3}$. However, since a DC/DC stage precedes the DC/AC stage in the case at hand, it is desirable to relate $\hat{U}_\mathrm{m}$ to the battery supply voltage U_b instead of u_DC. Therefore, the modulation index is redefined as the ratio between motor voltage and half of the battery voltage

$$M = \frac{\hat{U}_\mathrm{m}}{\frac{1}{2}U_\mathrm{b}}. \tag{4.11}$$

The modulation index M can exceed the value of $2/\sqrt{3}$ thanks to the DC/DC stage that can boost the supplying battery voltage. For the system at hand (cf. **Tab. 4.1**), the modulation index ranges within $M = 0...2$. Thereby, the transferred power P, battery current I_b and motor fundamental phase current amplitude $\hat{I}_\mathrm{m}$ can be derived as a function of the modulation index

$$P = M^2 \frac{3U_\mathrm{b}^2}{8R},\ I_\mathrm{b} = M^2 \frac{3U_\mathrm{b}}{8R},\ \hat{I}_\mathrm{m} = M\frac{U_\mathrm{b}}{2R}, \tag{4.12}$$

where $R = 3\hat{U}^2_\mathrm{m,max}/2P_\mathrm{max} = 4.8\,\Omega$.

Semiconductor Voltage Stress

First, the voltage stress on the power semiconductor devices is analysed. The semiconductors of the DC/DC and of the DC/AC stage are blocking and/or switching the DC link voltage u_DC. A higher DC link voltage u_DC results in higher switching losses and hence a higher thermal stress on the semiconductor devices. Furthermore, the maximum DC link voltage $u_\mathrm{DC,max}$ with some additional safety margin dictates the voltage rating of the employed semiconductor devices. The maximum DC link voltage always appears for the maximum motor voltage (in the case at hand represented by ($M = M_\mathrm{max} = 2$), and is

$$\begin{aligned} U_\mathrm{DC,max}|_{3/3\ \mathrm{PWM}} &= 2\hat{U}_\mathrm{m,max} = M_\mathrm{max}U_\mathrm{b} \\ U_\mathrm{DC,max}|_{2/3\ \mathrm{PWM}} &= \sqrt{3}\hat{U}_\mathrm{m,max} = M_\mathrm{max}\frac{\sqrt{3}}{2}U_\mathrm{b} \\ U_\mathrm{DC,max}|_{1/3\ \mathrm{PWM}} &= \sqrt{3}\hat{U}_\mathrm{m,max} = M_\mathrm{max}\frac{\sqrt{3}}{2}U_\mathrm{b} \end{aligned} \tag{4.13}$$

Therefore, both 1/3 PWM and 2/3 PWM schemes lead to a 13% voltage stress reduction compared to 3/3 PWM.

Semiconductor Switching Losses

The reduction of the switching losses P_{sw} of the DC/AC stage is the main advantage of 1/3 PWM, compared to conventional 2/3 PWM. In the following, the switching losses for 1/3 PWM are analytically derived and compared against the conventional modulation strategies. To this end, the switching energy dissipation E_{sw} for each hard switching transition is approximated as a linear function of the commutation current I_{sw},

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}) = k_0 + k_1 I_{\mathrm{sw}}. \tag{4.14}$$

Accordingly, the switching power dissipation for a switching frequency f_{s} is

$$P_{\mathrm{sw}}(I_{\mathrm{sw}}) = f_{\mathrm{s}} E_{\mathrm{sw}} = f_{\mathrm{s}} \left[k_0 + k_1 I_{\mathrm{sw}}\right]. \tag{4.15}$$

The parameters k_0 and k_1 depend on the switched voltage U_{sw}. Namely the parameter k_0 represents the constant part of the switching losses and is calculated in literature [110] (assuming unipolar power semiconductors) as

$$k_0(U_{\mathrm{sw}}) = Q_{\mathrm{oss}}(U_{\mathrm{sw}}) \cdot U_{\mathrm{sw}}, \tag{4.16}$$

where Q_{oss} is the electric charge stored in the non-linear output parasitic capacitance C_{oss} of a MOSFET of a considered bridge-leg

$$Q_{\mathrm{oss}}(U_{\mathrm{sw}}) = \int_0^{U_{\mathrm{sw}}} C_{\mathrm{oss}}(u)\mathrm{d}u. \tag{4.17}$$

For the case at hand, the parameter $k_1(U_{\mathrm{sw}})$ depends on the semiconductor technology and the gate driver configuration [111, 112]. Since the DC link voltage does not drastically change for the different modulation strategies as shown in **(4.13)**, it can be assumed for a first step worst case consideration that the parameters k_0 and k_1 are the same regardless of the modulation strategy.

The expression given in **(4.15)** is used for the calculation of the switching losses of the DC/DC stage, which are the same regardless of the modulation strategy

$$P_{\mathrm{sw}} = f_{\mathrm{s,b}} \left[k_0 + k_1 I_{\mathrm{b}}\right]. \tag{4.18}$$

Subsequently the expression **(4.15)** for the switching losses is applied to the DC/AC stage, where the commutation current varies over time in a sinusoidal fashion. In order to account for the sinusoidal current waveform,

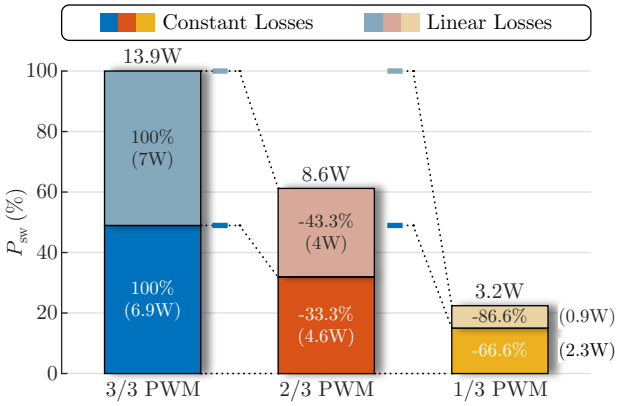


Fig. 4.8: Switching losses of the DC/AC stage under maximum motor voltage, i.e. $M = 2$ for the case at hand. For the calculations a unity power factor $\cos(\phi) = 1$ is assumed. Numerical values are derived for the worst case operating condition of **Tab. 4.1** and the parameters of **Tab. 4.5**.

an integration of **(4.15)** over the fundamental period T_m is performed. In the case of 3/3 PWM, the resulting sum of the switching losses for all three bridge-legs of the DC/AC stage (for assumed unity power factor $\cos(\phi) = 1$ load condition) is

$$P_\mathrm{sw}|_{3/3\,\mathrm{PWM}} = 3 f_\mathrm{s,m} \left[k_0 + k_1 \frac{2}{\pi} \hat{I}_\mathrm{m} \right]. \tag{4.19}$$

The switching losses comprise two components, a constant part $3 f_\mathrm{s,m} k_0$ which is independent of the converter load and a linear part $3 f_\mathrm{s,m} k_1 \frac{2}{\pi} \hat{I}_\mathrm{m}$ (proportional to the average value of a sinusoidal current half cycle) which increases linearly with the output current $\hat{I}_\mathrm{m}$ and is used to characterise the load state. The maximum switching losses of the DC/AC stage occur for maximum motor voltage/power i.e. $M = 2$ and are illustrated in **Fig. 4.8**. Similarly, the switching losses of the DC/AC stage employing 2/3 PWM are derived using **(4.15)**

$$P_\mathrm{sw}|_{2/3\,\mathrm{PWM}} = 3 f_\mathrm{s,m} \left[\underbrace{\frac{2}{3}}_{-33.3\%} k_0 + \underbrace{\left(1 - \frac{\sqrt{3}}{4}\right)}_{-43.3\%} k_1 \frac{2}{\pi} \hat{I}_\mathrm{m} \right]. \tag{4.20}$$

2/3 PWM yields a reduction of the constant part of the switching losses by 33.3% and of the linearly current dependent part of the switching losses by 43.3%, compared to 3/3 PWM, since each phase is switched for $2T_\mathrm{m}/3$ of the fundamental period T_m. Finally, the switching losses for 1/3 PWM are calculated,

$$P_\mathrm{sw}|_{1/3\,\mathrm{PWM}} = 3f_\mathrm{s,m}\left[\underbrace{\frac{1}{3}}_{-66.6\%}\,k_0 + \underbrace{\left(1-\frac{\sqrt{3}}{2}\right)}_{-86.6\%}k_1\frac{2}{\pi}\hat{I}_\mathrm{m}\right]. \tag{4.21}$$

With 1/3 PWM a drastic reduction of the switching losses is achieved, since each phase is switched only for $T_\mathrm{m}/3$ of the fundamental period T_m. Namely, a 66.6% reduction of the constant part and a 86.6% reduction of the linear part is possible compared to 3/3 PWM. Furthermore, 1/3 PWM notably outperforms 2/3 PWM in terms of switching losses. The switching losses of 2/3 PWM and 1/3 PWM for maximum motor voltage/current and $M = 2$ are plotted in **Fig. 4.8**. It is noted, that the reduction of the switching losses achieved by means of 1/3 PWM, simultaneously enables a lower semiconductor heatsink volume [87].

Semiconductor Current Stress

For the calculation of the conduction losses, the current ripple of the DC/DC stage inductor L_b and the DC/AC stage filter inductor L_m is neglected. Accordingly, the resulting total conduction losses are independent of the modulation strategy of both stages and are equal to

$$P_\mathrm{cd} = I_\mathrm{b}^2 R_\mathrm{Tb,on} + \frac{3}{2}\hat{I}_\mathrm{m}^2 R_\mathrm{Tm,on}, \tag{4.22}$$

where $R_\mathrm{Tb,on}$ and $R_\mathrm{Tm,on}$ are the on-state resistances of the DC/DC and DC/AC stage (unipolar) power semiconductor devices, respectively. However, the sharing of the conduction losses among the semiconductor devices, i.e. the sharing of the RMS current stress between the high-side and the low-side switches, changes depending on the modulation strategy. It is therefore important to analyse the current stress for each semiconductor device individually in order to provide a basis for the proper selection of the components in the design process.

The RMS current stress of T_b1 and T_b2 of the DC/DC stage is analytically derived for the different modulation techniques over the whole modulation

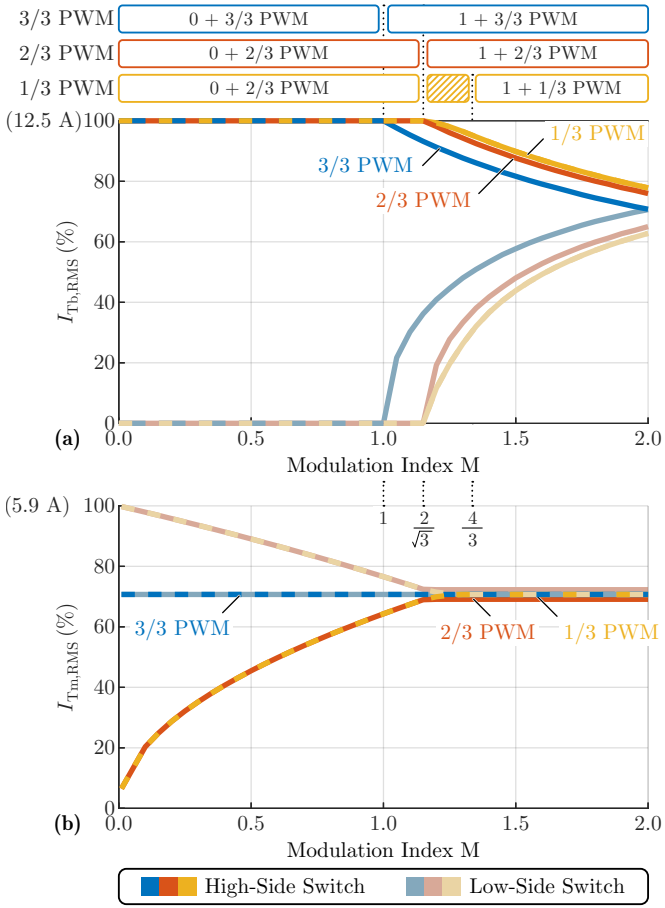


Fig. 4.9: Semiconductor device current stress for the three modulation strategies over the whole operating range, $M = 0...2$ considered in the case at hand. **(a)** Normalized RMS current of DC/DC stage high- and low-side semiconductor devices, with respect to the DC/DC stage RMS inductor current $I_{Lb,RMS}$. **(b)** Normalized RMS current of DC/AC stage high- and low-side semiconductor devices, with respect to the DC/AC stage RMS inductor current $I_{Lm,RMS}$. Numerical values are derived for the worst case operating condition of **Tab. 4.1** and the parameters of **Tab. 4.5**.

range and results as

$$I_{\mathrm{Tb1,RMS}}|_{3/3\ \mathrm{PWM}} = \begin{cases} I_{\mathrm{b}}, & M \leq 1 \\ I_{\mathrm{b}}\sqrt{\dfrac{1}{M}}, & M > 1 \end{cases} \tag{4.23}$$

$$I_{\mathrm{Tb2,RMS}}|_{3/3\ \mathrm{PWM}} = \begin{cases} 0, & M \leq 1 \\ I_{\mathrm{b}}\sqrt{1-\dfrac{1}{M}}, & M > 1 \end{cases} \tag{4.24}$$

$$I_{\mathrm{Tb1,RMS}}|_{2/3\ \mathrm{PWM}} = \begin{cases} I_{\mathrm{b}}, & M \leq \dfrac{2}{\sqrt{3}} \\ I_{\mathrm{b}}\sqrt{\dfrac{2}{\sqrt{3}M}}, & M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{4.25}$$

$$I_{\mathrm{Tb2,RMS}}|_{2/3\ \mathrm{PWM}} = \begin{cases} 0, & M \leq \dfrac{2}{\sqrt{3}} \\ I_{\mathrm{b}}\sqrt{1-\dfrac{2}{\sqrt{3}M}}, & M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{4.26}$$

$$I_{\mathrm{Tb1,RMS}}|_{1/3\ \mathrm{PWM}} = \begin{cases} I_{\mathrm{b}}, & M \leq \dfrac{2}{\sqrt{3}} \\ I_{\mathrm{b}}\sqrt{\dfrac{6\ln(3)}{\sqrt{3}\pi M}}, & M > \dfrac{4}{3} \end{cases} \tag{4.27}$$

$$I_{\mathrm{Tb2,RMS}}|_{1/3\ \mathrm{PWM}} = \begin{cases} 0, & M \leq \dfrac{2}{\sqrt{3}} \\ I_{\mathrm{b}}\sqrt{1-\dfrac{6\ln(3)}{\sqrt{3}\pi M}}, & M > \dfrac{4}{3}. \end{cases} \tag{4.28}$$

The current stresses of the semiconductor devices, normalized with respect to the DC/DC stage inductor (L_{b}) RMS current $I_{\mathrm{Lb,RMS}} = I_{\mathrm{b}}$, are shown in **Fig. 4.9(a)**. It should be noted that the sum of the instantaneous currents of T_{b1} and T_{b2} is equal to the L_{b} inductor current

$$i_{\mathrm{Tb1}}(t) + i_{\mathrm{Tb2}}(t) = i_{\mathrm{Lb}}(t). \tag{4.29}$$

However, the relationship between the RMS currents is non-linear,

$$I^2_{\mathrm{Tb1,RMS}} + I^2_{\mathrm{Tb2,RMS}} = I^2_{\mathrm{Lb,RMS}}. \tag{4.30}$$

When the modulation index is low and the DC/DC stage is deactivated (e.g. 1/3 PWM and $M \leq 2/\sqrt{3}$), the high-side switch T_{b1} of the DC/DC stage is clamped and therefore experiences the whole RMS current stress. However, this is typically not a problem since for low modulation indexes (low DC/AC stage output voltage and/or motor speed) the power P and thus battery current I_b is anyway low. 1/3 PWM leads to asymmetric current distribution between the high-side and the low-side switches similar to 2/3 PWM, while the asymmetry reduces as the modulation index and/or the transferred power increases. In summary, the asymmetric current distribution caused by 1/3 PWM for low modulation index M, does not require over-dimensioning of the DC/DC stage semiconductor devices. The (symmetric) stresses for high modulation indexes M are higher than the (asymmetric) stresses for low values of M, hence dominate the dimensioning of the DC/DC stage semiconductors.

Similarly, the RMS current stress of the semiconductor devices T_{m1} and T_{m2} of the DC/AC stage is analytically calculated as

$$I_{\mathrm{Tm1,RMS}}|_{3/3\ \mathrm{PWM}} = I_{\mathrm{Tm2,RMS}}|_{3/3\ \mathrm{PWM}} = \frac{\hat{I}_m}{\sqrt{2}}\frac{1}{\sqrt{2}} \tag{4.31}$$

$$I_{\mathrm{Tm1,RMS}}|_{2/3\ \mathrm{PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{\dfrac{3\sqrt{3}M}{4\pi}}, & M \leq \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{\dfrac{3}{2\pi}}, & M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{4.32}$$

$$I_{\mathrm{Tm2,RMS}}|_{2/3\ \mathrm{PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{1 - \dfrac{3\sqrt{3}M}{4\pi}}, & M \leq \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{1 - \dfrac{3}{2\pi}}, & M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{4.33}$$

$$I_{\mathrm{Tm1,RMS}}|_{1/3\ \mathrm{PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{\dfrac{3\sqrt{3}M}{4\pi}}, & M \leq \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\dfrac{1}{\sqrt{2}}, & M > \dfrac{4}{3} \end{cases} \tag{4.34}$$

$$I_{\mathrm{Tm2,RMS}}|_{1/3\ \mathrm{PWM}} = \begin{cases} \dfrac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{1-\dfrac{3\sqrt{3}M}{4\pi}}, & M \leq \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\dfrac{1}{\sqrt{2}}, & M > \dfrac{4}{3}. \end{cases} \tag{4.35}$$

The current stresses of the semiconductor devices, normalized with respect to the DC/AC stage inductor (L_{m}) RMS current $I_{\mathrm{Lm,RMS}} = \hat{I}_{\mathrm{m}}/\sqrt{2}$, are shown in **Fig. 4.9(b)**. The 3/3 PWM modulation results in symmetric current sharing between the high-side and low-side semiconductor devices of the DC/AC stage **(4.31)**. In contrast, 2/3 PWM and 1/3 PWM lead to a similar asymmetric current stress on the semiconductor devices **(4.32)-(4.35)**. In particular, higher current stress appears on the low-side switch of the DC/AC stage T_{ma2} when the modulation index is low (e.g. $M \leq 2/\sqrt{3}$ and 1/3 PWM). As the modulation index increases (e.g. $M > 4/3$ and 1/3 PWM) the RMS current sharing becomes more symmetric. The asymmetric current stress for low modulation indexes (i.e. low motor voltage $\hat{U}_{\mathrm{m}}$ and/or motor speed) is critical. Care has to be taken with the thermal design of the low-side switches T_{m2}, such that they can conduct the nominal motor current $\hat{I}_{\mathrm{m}}$ and hence ensure nominal motor torque during motor acceleration, starting from standstill. It is noted that an alternative 2/3 PWM implementation, which ensures symmetric current distribution for the whole operating range, is analysed in **Sec. 4.1.2**. However, this alternative 2/3 PWM is not applicable in case of an FSF.

Inductive Components

The inductor losses are investigated, in a first step. It is assumed that a two-stage DC/AC converter system is designed for conventional 3/3 PWM (e.g. features a cooling system that can withstand the high switching losses of 3/3 PWM) and that the inductive components cannot be changed. In particular, the DC/DC stage features an inductance L_{b} and the DC/AC stage employs an inductance L_{m}, regardless of the modulation scheme.

In general, there is a direct relation between the inductor losses and the RMS inductor current ripple $\Delta I_{\mathrm{L,RMS}}$, as a high RMS current ripple results in a high frequency RMS flux density and hence substantial core losses [85]. In addition, high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple $\Delta I_{\mathrm{L,RMS}}$ is a reasonable performance indicator for the design of the inductive components and is calculated in the following for the different modulation strategies over the whole operating range.

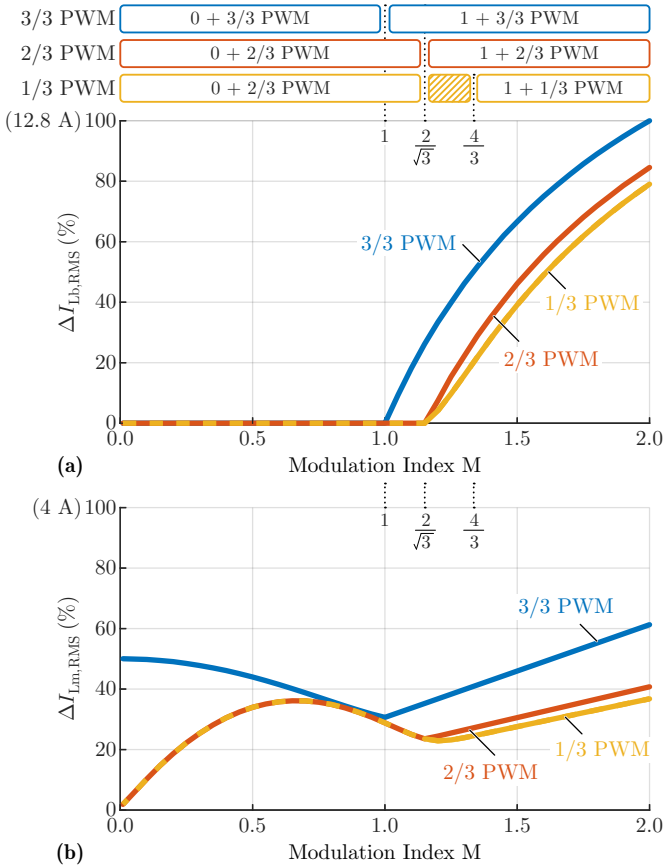


Fig. 4.10: Inductor RMS current ripple for different modulation strategies over the whole operating range $M = 0...2$ considered in the case at hand. In **(a)** the normalized RMS current ripple of the DC/DC stage inductor L_b is depicted. In **(b)** the normalized RMS current ripple of the DC/AC stage filter inductor L_m is plotted. Numerical values are derived for the worst case operating condition of **Tab. 4.1** and the parameters of **Tab. 4.5**.

For the DC/DC stage the same inductance value L_b is considered regardless of the modulation strategy. Subsequently, the RMS inductor current ripple $\Delta I_{\mathrm{Lb,RMS}}$ is calculated for the considered modulation strategies based on a numeric solver (i.e. no analytical solution). The RMS inductor current ripple, normalized with respect to the worst case local RMS current ripple

$$\Delta I_{\mathrm{Lb,RMS,max}} = \frac{\hat{U}_{\mathrm{m,max}}}{4\sqrt{3} f_{\mathrm{s,b}} L_\mathrm{b}}, \tag{4.36}$$

is plotted in **Fig. 4.10(a)**. When the modulation index is low and the DC/DC stage is deactivated (e.g. 1/3 PWM for $M \leq 2/\sqrt{3}$), the high-side switch T_{b1} of the DC/DC stage is clamped, therefore no current ripple appears on the inductor L_b. As the modulation index increases (e.g. 1/3 PWM for $M > 2/\sqrt{3}$) the inductor current shows a gradually increasing ripple. Due to the lower DC link voltage for the same DC/AC stage output voltage, 1/3 PWM exhibits significantly lower RMS inductor current ripple compared to 3/3 PWM (21% reduction of $\Delta I_{\mathrm{Lb,RMS}}$% occurs for $M = 2$) but only slightly lower ripple compared to 2/3 PWM.

Similarly, for the DC/AC stage the same inductance value L_m is considered independent of the modulation strategy. The RMS inductor current ripple $\Delta I_{\mathrm{Lm,RMS}}$ is calculated for all modulation strategies over the complete operating range based on a numeric solver (i.e. no analytic solution). The RMS inductor current ripple, normalized with respect to the worst case local RMS current ripple

$$\Delta I_{\mathrm{Lm,RMS,max}} = \frac{\hat{U}_{\mathrm{m,max}}}{4\sqrt{3} f_{\mathrm{s,m}} L_\mathrm{m}}, \tag{4.37}$$

is depicted in **Fig. 4.10(b)**. In particular for 1/3 PWM, when the modulation index is low, $M \leq 2/\sqrt{3}$, the DC link voltage is constant and equal to the battery voltage $u_\mathrm{DC} = U_\mathrm{b}$. As the modulation index gradually increases (i.e. $M = 0 \rightarrow 2/\sqrt{3}$), the current ripple RMS value initially increases, reaches a local maximum value and then decreases. When the modulation index exceeds the threshold value of $M = 2/\sqrt{3}$, the DC/DC stage is activated and the DC link voltage increases. Accordingly, the ripple of the DC/AC filter inductor which is proportional to the DC link voltage also increases. In general, 1/3 PWM yields similar current ripple RMS value as 2/3 PWM but lower current ripple compared to 3/3 PWM (40% reduction of $\Delta I_{\mathrm{Lm,RMS}}$% occurs for $M = 2$).

In a more general case, where there is not a pre-existing converter designed for 3/3 PWM, different inductance values can be advantageously selected for the different modulation strategies. Besides a smaller heatsink

volume for the DC/AC stage (thanks to the low switching losses), 1/3 PWM allows for smaller inductance values, which translates into further volume reduction. Accordingly, the minimum required inductance value L_b of the DC/DC stage and the inductance L_m of the DC/AC stage are analytically calculated.

In order to calculate the required inductance L_b, a worst case current ripple amplitude $\Delta I_\mathrm{Lb,PK}$ (single side peak value) is assumed. The same current ripple limit applies regardless of the modulation strategy and the required inductance is given by

$$L_\mathrm{b} \geq \frac{d_\mathrm{min}(1-d_\mathrm{min})U_\mathrm{DC,max}}{2\Delta I_\mathrm{Lb,PK} f_\mathrm{s,b}}, \quad d_\mathrm{min} = \frac{U_\mathrm{b}}{U_\mathrm{DC,max}}, \tag{4.38}$$

where $f_\mathrm{s,b}$ is the switching frequency of the DC/DC stage. Applying **(4.38)** to 3/3 PWM, where $U_\mathrm{DC,max} = 2\hat{U}_\mathrm{m,max}$ **(4.13)**, the required inductance is

$$L_\mathrm{b}|_{3/3\,\mathrm{PWM}} \geq \frac{\hat{U}_\mathrm{m,max}}{4\Delta I_\mathrm{Lb,PK} f_\mathrm{s,b}}. \tag{4.39}$$

Subsequently, **(4.38)** is applied to 1/3 PWM and 2/3 PWM. The 1/3 PWM and 2/3 PWM schemes require the same inductance value because both modulation schemes feature the same maximum instantaneous DC link voltage $U_\mathrm{DC,max} = \sqrt{3}\hat{U}_\mathrm{m,max}$ **(4.13)**. The inductance is calculated as

$$L_\mathrm{b}|_{1/3\,\mathrm{PWM}} = L_\mathrm{b}|_{2/3\,\mathrm{PWM}} \geq \frac{(1-\frac{1}{\sqrt{3}})\hat{U}_\mathrm{m,max}}{2\Delta I_\mathrm{Lb,PK} f_\mathrm{s,b}}. \tag{4.40}$$

Consequently, 2/3 PWM and 1/3 PWM require 15% lower inductance compared to 3/3 PWM for the DC/DC stage, resulting in an accordingly higher power density.

For the calculation of the DC/AC stage filter inductance L_m, a worst case current ripple amplitude $\Delta I_\mathrm{Lm,PK}$ (single side peak value) is considered. The same limit applies for all possible modulation strategies and the required inductance is given by

$$L_\mathrm{m} \geq \frac{U_\mathrm{DC,max}}{8\Delta I_\mathrm{Lm,PK} f_\mathrm{s,m}}, \tag{4.41}$$

where $f_\mathrm{s,m}$ is the switching frequency of the DC/AC stage. Applying **(4.41)** to 3/3 PWM, the required inductance is

$$L_\mathrm{m}|_{3/3\,\mathrm{PWM}} \geq \frac{\hat{U}_\mathrm{m,max}}{4\Delta I_\mathrm{Lm,PK} f_\mathrm{s,m}}. \tag{4.42}$$

The 2/3 PWM and 1/3 PWM schemes require the same DC/AC stage inductance L_m, which based on **(4.41)** is

$$L_\mathrm{m}|_{1/3\,\mathrm{PWM}} = L_\mathrm{m}|_{2/3\,\mathrm{PWM}} \geq \frac{\sqrt{3}\hat{U}_\mathrm{m,max}}{8\Delta I_\mathrm{Lm,PK} f_\mathrm{s,m}}. \tag{4.43}$$

Accordingly, 2/3 PWM and 1/3 PWM are reducing the DC/AC stage filter inductance requirement by 13% and hence yield a smaller inductor volume compared to 3/3 PWM.

DC Link Capacitor

The DC link capacitor C_DC must be carefully selected. On the one hand, the capacitance value should be small in order to allow the DC/DC stage to accurately control the DC link voltage to a six-pulse shape during 1/3 PWM operation (cf. **Fig. 4.3(c)**). In particular, the resonant frequency of the $L_\mathrm{b} - C_\mathrm{DC}$ filter $f_\mathrm{r,DC}$, must be $a_\mathrm{f} \sim 10$ times higher compared to the repetition frequency $6f_\mathrm{m}$ of the six-pulse shaped DC link voltage, under 1/3 PWM operation

$$f_\mathrm{r,DC} \geq a_\mathrm{f} \cdot 6f_\mathrm{m}, \text{ where } \quad f_\mathrm{r,DC} = \frac{1}{2\pi\sqrt{L_\mathrm{b} C_\mathrm{DC}}}. \tag{4.44}$$

Solving the inequality for C_DC provides an upper bound for the DC link capacitance

$$C_\mathrm{DC} \leq \frac{1}{144\pi^2 L_\mathrm{b} a_\mathrm{f}^2 f_\mathrm{m}^2}. \tag{4.45}$$

On the other hand, the capacitance value should be large enough in order to limit the DC link voltage ripple amplitude ΔU_DC to a sufficiently low value. In particular, the capacitor C_DC conducts the switched output current of the DC/DC stage as well as the switched input current of the DC/AC stage, both contributing to the DC link voltage ripple $\Delta u_\mathrm{DC}(t)$. Therefore, the DC link capacitance value must be

$$C_\mathrm{DC} \geq \frac{I_\mathrm{b,max}}{8 f_\mathrm{s,b} \Delta U_\mathrm{DC}} + \frac{\hat{I}_\mathrm{m,max}}{8 f_\mathrm{s,m} \Delta U_\mathrm{DC}}, \tag{4.46}$$

independent of the modulation strategy, in order to ensure a DC link voltage ripple amplitude less or equal to ΔU_DC. The design constraints of **(4.45)** and **(4.46)** define a design space within which the capacitance C_DC must be selected. The resulting DC link capacitance value is typically small since there

is no need for energy storage in a three-phase system (in contrast to a single-phase system). An approximate upper bound for the DC link capacitor RMS current stress is

$$I_{C_{\mathrm{DC}},\mathrm{RMS},\mathrm{max}} = \sqrt{\frac{I_{\mathrm{b},\mathrm{max}}^2}{4} + \frac{\hat{I}_{\mathrm{m},\mathrm{max}}^2}{4}}. \tag{4.47}$$

A detailed analysis of the DC link capacitor current stress can be found in [63]. In summary, the DC link capacitor must conduct a high-frequency switched current with high peak values, while a low capacitance value is typically required. For this reason, ceramic or film capacitors are suggested for the DC link implementation.

Motor Common-Mode Voltage

The motor common-mode (CM) voltage resulting from the different modulation strategies is now analysed. A motor CM voltage with high $\mathrm{d}u/\mathrm{d}t$ would results in parasitic CM currents which would partly flow through the motor bearing and could result in bearing damage [33]. For this reason, a full sine-wave output filter (FSF) $L_\mathrm{m} - C_\mathrm{m}$ is employed (cf. **Fig. 4.1(a)**) which protects the motor against CM (and differential-mode) voltages with high $\mathrm{d}u/\mathrm{d}t$ [34–38]. In particular, the FSF directly attenuates the switching frequency CM voltage generated by the DC/AC stage and hence only a small residual high-frequency (HF) motor CM voltage with an amplitude

$$\hat{U}_{\mathrm{m},\mathrm{CM}}|_{\mathrm{HF}} = \frac{1}{32}\frac{U_{\mathrm{DC},\mathrm{max}}}{L_\mathrm{m} C_\mathrm{m} f_{\mathrm{s,m}}^2} \tag{4.48}$$

remains at the motor terminals, where $U_{\mathrm{DC},\mathrm{max}}$ is given by **(4.13)**. When an FSF is employed, $\hat{U}_{\mathrm{m},\mathrm{CM}}|_{\mathrm{HF}}$ is noncritical concerning bearing currents and is marginally higher for 3/3 PWM as opposed to 2/3 PWM and 1/3 PWM because of the marginally higher DC link voltage $U_{\mathrm{DC},\mathrm{max}}$ of the former.

Furthermore, the motor CM voltage can feature a low-frequency (LF) component

$$u_{\mathrm{m},\mathrm{CM}}|_{\mathrm{LF}}(t) = u_{\mathrm{DC}}(t) \cdot \left(\frac{d_\mathrm{a} + d_\mathrm{b} + d_\mathrm{c}}{3} - \frac{1}{2}\right), \tag{4.49}$$

depending on the employed modulation scheme, as depicted in **Fig. 4.11**. In particular, 3/3 PWM features zero LF motor CM voltage $u_{\mathrm{m},\mathrm{CM}}|_{\mathrm{LF}}(t) = 0$, because the sum of the three-phase DC/AC stage duty cycles is constant over time (cf. **Fig. 4.2(a.ii)**). In contrast, 2/3 PWM and 1/3 PWM feature a time varying LF motor CM voltage [62] with a repetition frequency equal to $3f_\mathrm{m}$,

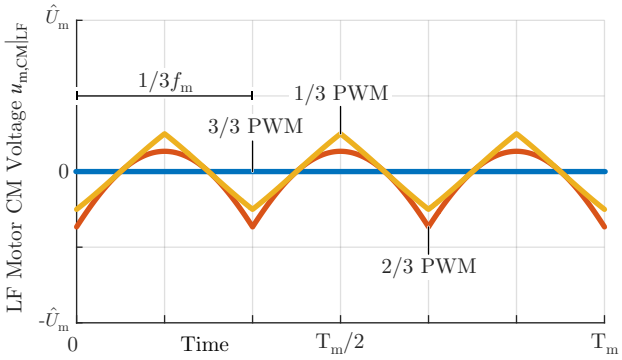


Fig. 4.11: Low-frequency component of the motor CM voltage $u_{\mathrm{m,CM}|\mathrm{LF}}(t)$, for the three examined modulation strategies of **Fig. 4.2**. Waveforms shown for maximum motor voltage, i.e. $M = 2$ for the case at hand.

since the sum of the three-phase DC/AC stage duty cycles is different from zero (cf. **Fig. 4.2(b.ii)** and **(c.ii)**, respectively). The LF motor CM voltage is also noncritical concerning motor bearing currents.

4.3 Component Stresses for $\cos(\phi) < 1$

The impact of a low load power factor (PF) on the overall design of the two-stage converter system is discussed. A converter system that can operate under any load voltage-current phase shift ϕ is desirable in this case study. Therefore, the stresses on the different system components are now analysed for a PF $\cos(\phi) < 1$. In particular, the load current is assumed to either lead or lag the load voltage by a phase shift angle $\phi = -90^{\mathrm{o}}...90^{\mathrm{o}}$ (i.e. capacitive or inductive load behaviour). Accordingly, the transferred apparent power $S = 0\,\mathrm{VA}...500\,\mathrm{VA}$, active power P, battery current I_b and load fundamental phase current amplitude $\hat{I}_\mathrm{m}$ can be derived as a function of the modulation index M and PF $\cos(\phi)$ as

$$\begin{aligned} S &= M^2 \frac{3U_\mathrm{b}^2}{8R}, \quad P = M^2 \frac{3U_\mathrm{b}^2}{8R} \cos(\phi), \\ I_\mathrm{b} &= M^2 \frac{3U_\mathrm{b}}{8R} \cos(\phi), \quad \hat{I}_\mathrm{m} = M \frac{U_\mathrm{b}}{2R}, \end{aligned} \tag{4.50}$$

where $R = 3\hat{U}_{\mathrm{m,max}}^2 / 2S_{\mathrm{max}} = 4.8\,\Omega$.

The switching losses of the DC/DC stage can directly be derived by substituting I_b from **(4.50)** in **(4.18)**. Since the battery current I_b decreases as the PF reduces, the DC/DC stage switching losses also decrease. The switching losses of the DC/AC stage for 3/3 PWM are independent of the PF and are therefore given by using **(4.19)**. On the other hand, the switching losses of the DC/AC stage for 2/3 PWM and 1/3 PWM depend on the PF, hence the phase shift ϕ has to be considered in the derivation of the local switching losses **(4.15)** of the DC/AC stage as

$$p_\mathrm{sw}(\vartheta) = f_\mathrm{s,m}\left[k_0 + k_1\hat{I}_\mathrm{m}|\cos(\vartheta-\phi)|\right]. \tag{4.51}$$

By averaging $p_\mathrm{sw}(\vartheta)$ over a 2π wide fundamental period the global average switching losses can be derived. For 2/3 PWM, the switching losses are calculated as

$$P_\mathrm{sw}|_{2/3\,\mathrm{PWM}} = \frac{3}{2\pi}\left[\int_0^{\frac{2\pi}{3}} p_\mathrm{sw}(\vartheta)\mathrm{d}\vartheta + \int_{\frac{4\pi}{3}}^{2\pi} p_\mathrm{sw}(\vartheta)\mathrm{d}\vartheta\right], \tag{4.52}$$

which for a voltage-current phase shift of $|\phi| \leq 30^\mathrm{o}$ results in

$$P_\mathrm{sw}|_{2/3\,\mathrm{PWM}} = 3f_\mathrm{s,m}\left[\frac{2}{3}k_0 + \left(1 - \frac{\sqrt{3}\cos|\phi|}{4}\right)k_1\frac{2}{\pi}\hat{I}_\mathrm{m}\right], \tag{4.53}$$

and for $|\phi| > 30^\mathrm{o}$ gives

$$P_\mathrm{sw}|_{2/3\,\mathrm{PWM}} = 3f_\mathrm{s,m}\left[\frac{2}{3}k_0 + \left(\frac{1}{2} + \frac{\sin|\phi|}{4}\right)k_1\frac{2}{\pi}\hat{I}_\mathrm{m}\right]. \tag{4.54}$$

The same procedure can be applied to calculate the DC/AC stage switching losses for 1/3 PWM where

$$P_\mathrm{sw}|_{1/3\,\mathrm{PWM}} = \frac{3}{2\pi}\left[\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} p_\mathrm{sw}(\vartheta)\mathrm{d}\vartheta + \int_{\frac{4\pi}{3}}^{\frac{5\pi}{3}} p_\mathrm{sw}(\vartheta)\mathrm{d}\vartheta\right], \tag{4.55}$$

which for a voltage-current phase shift of $|\phi| \leq 30^\mathrm{o}$ results in

$$P_\mathrm{sw}|_{1/3\,\mathrm{PWM}} = 3f_\mathrm{s,m}\left[\frac{1}{3}k_0 + \left(1 - \frac{\sqrt{3}\cos|\phi|}{2}\right)k_1\frac{2}{\pi}\hat{I}_\mathrm{m}\right], \tag{4.56}$$

while for $|\phi| > 30^\mathrm{o}$ gives

$$P_\mathrm{sw}|_{1/3\,\mathrm{PWM}} = 3f_\mathrm{s,m}\left[\frac{1}{3}k_0 + \frac{\sin|\phi|}{2}k_1\frac{2}{\pi}\hat{I}_\mathrm{m}\right]. \tag{4.57}$$

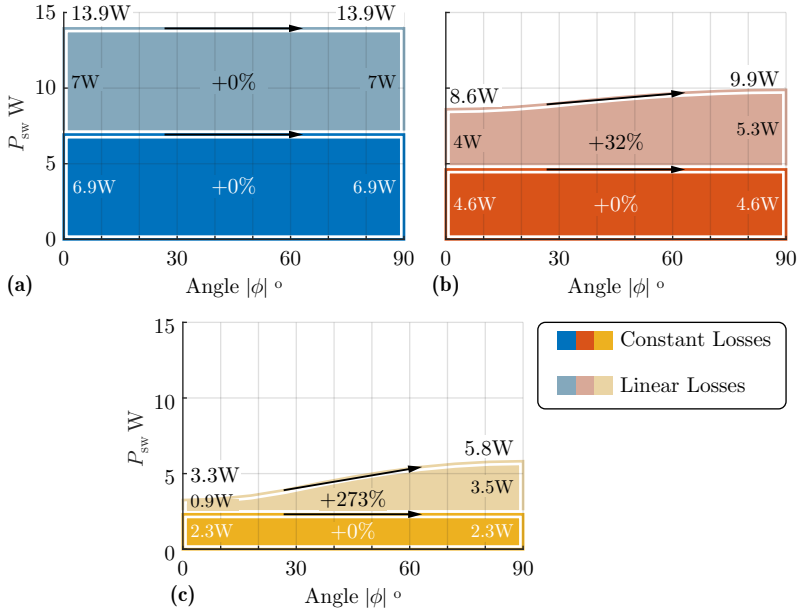


Fig. 4.12: Switching losses of the DC/AC stage as a function of the voltage-current phase shift ϕ of the load and the modulation scheme. **(a)** 3/3 PWM, **(b)** 2/3 PWM and **(c)** 1/3 PWM. There, the worst case operating point with the maximum motor voltage ($M = 2$ for the case at hand) is considered, while numerical values are derived for the worst case operating condition of **Tab. 4.1** and the parameters of **Tab. 4.5**.

In **Fig. 4.12**, the switching losses for all modulation schemes depending on the phase shift ϕ of the load are plotted. Compared to the load independent losses obtained with 3/3 PWM, the losses for 2/3 PWM and 1/3 PWM slightly increase with increasing phase shift, since in the middle phase a higher current has to be switched than with $\cos(\phi) = 1$. It is noted, that the switching losses are symmetric with respect to ϕ, i.e. the losses for a voltage-current phase shift $+\phi$ are equal to the respective losses for $-\phi$. It can be deduced from **Fig. 4.12**, that although the switching losses for 2/3 PWM and 1/3 PWM increase as the PF reduces, both still generate by far lower overall switching losses compared to 3/3 PWM.

For a complete converter system design, the stresses on the remaining components must be considered. The total conduction losses of the converter system can still be calculated from **(4.22)** over the whole PF range,

where the battery current I_b is substituted from **(4.50)**. Similarly, the mathematical formulas which describe the current stresses on the semiconductor devices of the DC/DC stage **(4.23)-(4.28)** and DC/AC stage **(4.31)-(4.35)** are still valid. The DC/DC stage semiconductor devices must hence be designed for the worst case operating condition with the maximum load voltage/power ($M = 2$) and unity PF ($\phi = 0°$), independent of the modulation strategy. For this operating condition, the maximum switching losses and conduction losses appear simultaneously on the DC/DC stage semiconductors, since I_b is maximum **(4.50)**. The same worst case operating condition applies for the DC/AC stage semiconductor devices, if they are designed for 3/3 PWM operation. However, if the DC/AC stage semiconductor devices are designed for 2/3 PWM or 1/3 PWM the worst case operating condition appears for the maximum load apparent power S but zero PF ($|\phi| = 90°$). For this operating condition, the maximum switching losses (cf. **Fig. 4.12**) and conduction losses (maximum load current $\hat{I}_m$) appear simultaneously on the DC/AC stage semiconductors. Finally, the proposed inductor values L_b for the DC/DC stage and L_m for the DC/AC stage **(4.39)-(4.40)** and **(4.42)-(4.43)**, respectively), as well as the recommended DC link capacitor value C_{DC} **(4.45)-(4.46)**, are applicable for $\cos(\phi) < 1$.

4.4 Experimental Validation

In order to verify the performance potential of the 1/3 PWM modulation, a hardware demonstrator is designed and built according to the specifications of **Tab. 4.1**.

4.4.1 Design Procedure

A two-stage converter system, shown in **Fig. 4.1(a)**, is designed for conventional 3/3 PWM. Later, 1/3 PWM is retrofitted to the system by means of a firmware update. In this case, the drive system features a cooling system that can withstand the high DC/AC stage switching losses of 3/3 PWM. In addition, the DC/DC stage inductor L_b and the DC/AC stage inductors L_m are designed for 3/3 PWM. The worst case operating condition that yields the highest component stresses is first identified, in order to design the converter. The worst case operating condition appears for maximum motor voltage/power and unity power factor, as highlighted in **Tab. 4.1**. The converter employs 200 V rated EPC 2034 semiconductor devices and a switching frequency of $f_s = 300\,\text{kHz}$ for both the DC/DC stage as well as the DC/AC

Tab. 4.2: DC/DC stage and DC/AC stage semiconductor design/stress summary for the worst case operating condition of **Tab. 4.1**. Numerical values are derived for the parameters of **Tab. 4.5**.

		DC/DC stage								
		$U_{DC,max}$		P_c [1]		P_{sw} [2]		$I_{Tb1,RMS}$		$I_{Tb2,RMS}$
3/3 PWM	**(4.13)**	80 V	**(4.22)**	1.7 W	**(4.18)**	10.1 W	**(4.23)**	8.8 A	**(4.24)**	8.8 A
2/3 PWM	**(4.13)**	69 V	**(4.22)**	1.7 W	**(4.18)**	10.1 W	**(4.25)**	9.5 A	**(4.26)**	8.1 A
1/3 PWM	**(4.13)**	69 V	**(4.22)**	1.7 W	**(4.18)**	10.1 W	**(4.27)**	9.7 A	**(4.28)**	7.8 A
		DC/AC stage								
		$U_{DC,max}$		P_c [3]		P_{sw} [4]		$I_{Tm1,RMS}$		$I_{Tm2,RMS}$
3/3 PWM	**(4.13)**	80 V	**(4.22)**	2.1 W	**(4.19)**	13.9 W	**(4.31)**	4.2 A	**(4.31)**	4.2 A
2/3 PWM	**(4.13)**	69 V	**(4.22)**	2.1 W	**(4.20)**	8.6 W	**(4.32)**	4.1 A	**(4.33)**	4.3 A
1/3 PWM	**(4.13)**	69 V	**(4.22)**	2.1 W	**(4.21)**	3.3 W	**(4.34)**	4.2 A	**(4.35)**	4.2 A

[1] On-state resistance $R_{Tb,on} = 10\,m\Omega$ at 100°C.

[2] Switching parameters $k_0 = 15.4\,\mu J$, $k_1 = 1.5\,\mu J/A$ for $U_{DC} = 80\,V$ [112].

[3] On-state resistance $R_{Tm,on} = 20\,m\Omega$ at 100°C.

[4] Switching parameters $k_0 = 7.7\,\mu J$, $k_1 = 1.5\,\mu J/A$ for $U_{DC} = 80\,V$ [112].

stage. Each half-bridge of the DC/AC stage features two semiconductor devices (i.e. single device per switch) while the DC/DC stage half-bridge employs four EPC 2034 semiconductor devices (i.e. two devices in parallel per switch). In **Tab. 4.2** the semiconductor voltage/current stresses and the conduction/switching losses are calculated for both the DC/DC stage and the DC/AC stage. The inductor performance is summarized in **Tab. 4.3**. Finally, the DC link capacitor value is selected considering a maximum allowed DC link voltage ripple amplitude of $\Delta U_{\mathrm{DC}} = 0.8\,\mathrm{V}$ ($\sim$ 1% of the DC link voltage). Based on **(4.45)** and **(4.46)**, the DC link capacitor value is constrained in the interval $11\,\mu\mathrm{F} \leq C_{\mathrm{DC}} \leq 29\,\mu\mathrm{F}$, from which the value of $C_{\mathrm{DC}} = 25\,\mu\mathrm{F}$ is selected.

According to **Tab. 4.2** and **Fig. 4.8**, the use of the 1/3 PWM scheme leads to a significant reduction of the DC/AC stage switching losses (3.3 W) compared to 3/3 PWM (13.9 W). As a result, a substantial overall efficiency η increase is achieved by means of 1/3 PWM. The inductor losses also decrease, since 1/3 PWM results in an RMS current ripple reduction of the DC/DC stage inductor L_{b} and DC/AC stage inductor L_{m} (cf. **Tab. 4.3**).

In a more general case, where there is not a pre-existing drive system designed for 3/3 PWM, different inductance values can be selected for the different modulation strategies. Besides a smaller semiconductor heatsink volume of the DC/AC stage, thanks to the low switching losses, 1/3 PWM allows for smaller inductance values. The inductor values and the resulting inductor RMS current ripple are summarized in **Tab. 4.4**. There, 1/3 PWM not only employs a smaller DC/DC stage inductance L_{b} and DC/AC inductance L_{m}, but also features lower RMS current ripples. Therefore, the inductors L_{b} and L_{m} can be realised in a more compact way, which translates into a lower overall volume for 1/3 PWM compared to 3/3 PWM.

It is noted that the equations summarized in **Tab. 4.2** - **4.4** serve as a general design guideline and can be extended for motor drive systems with different specifications. After the designer selects an appropriate switching frequency f_{s}, based on the available semiconductor technology, **Tab. 4.2** - **4.4** can be easily used in order to design the two-stage converter.

4.4.2 Experimental Results

The demonstrator system of **Fig. 4.13** with the parameter values of **Tab. 4.5** is assembled. The hardware prototype comprises a power and a control board. The power board includes the DC/AC stage and the DC/DC stage half-bridges, the respective gate drivers, a custom aluminium heatsink and

Tab. 4.3: Inductor design summary for a pre-existing drive system designed for 3/3 PWM. Numeric results derived for the worst case operating condition of **Tab. 4.1** and the parameters of **Tab. 4.5**.

		DC/DC stage			DC/AC stage	
		L_b	$\Delta I_{Lb,RMS}$ [1]		L_m	$\Delta I_{Lm,RMS}$ [1]
3/3 PWM	**(4.39)**	1.5 µH	12.8 A	**(4.42)**	4.7 µH	2.5 A
2/3 PWM	**(4.39)**	1.5 µH	10.8 A	**(4.42)**	4.7 µH	1.6 A
1/3 PWM	**(4.39)**	1.5 µH	10.1 A	**(4.42)**	4.7 µH	1.5 A

[1] The values are based on numerical solver.

Tab. 4.4: Inductor design summary for a system which is purposely designed for the employed modulation. Numeric results derived for the worst case operating condition of **Tab. 4.1** and the parameters of **Tab. 4.5**.

		DC/DC stage			DC/AC stage	
		L_b	$\Delta I_{Lb,RMS}$ [1]		L_m	$\Delta I_{Lm,RMS}$ [1]
3/3 PWM	**(4.39)**	1.5 µH	12.8 A	**(4.42)**	4.7 µH	2.5 A
2/3 PWM	**(4.40)**	1.27 µH	12.8 A	**(4.43)**	4.1 µH	1.8 A
1/3 PWM	**(4.40)**	1.27 µH	11.9 A	**(4.43)**	4.1 µH	1.7 A

[1] The values are based on numerical solver.

the four inductors. Four 25 mm fans are used for forced air cooling. The custom control board, which is placed on top of the power board, is used for the generation of the gating signals and the current/voltage measurement.

The 1/3 PWM modulation strategy is implemented in software and tested according to the control diagram of **Fig. 4.5**. The experimentally measured waveforms are shown in **Fig. 4.14** for maximum transferred power $P = 500\,\mathrm{W}$ and maximum motor phase voltage amplitude $\hat{U}_\mathrm{m} = 40\,\mathrm{V}$, i.e. modulation index $M = 2$. There, the six-pulse shape of the DC link voltage u_DC is clearly visible. Furthermore, the three motor line-to-line voltages are depicted. The DC link voltage is equal to the highest instantaneous motor line-to-line voltage. In addition, the gate signal of phase a of the DC/AC stage is shown, which reveals that the corresponding half-bridge is switched only for 1/3 of the fundamental period T_m. Subsequently, a transition from 2/3 PWM to 1/3 PWM is shown in **Fig. 4.15**. There, the output motor line-to-line voltages are gradually increased and a seamless transition (without unwanted transients) from 2/3 PWM to 1/3 PWM is achieved. The experimental measurements are verifying the theoretical consideration of **Sec. 4.1**. It should be pointed out that 1/3 PWM can be applied on existing converter systems as a firmware update. That is, no hardware modifications are needed in order to accommodate the 1/3 PWM scheme.

The converter efficiency characteristic is now measured over the whole output power range, $P = 0\,\mathrm{W}...500\,\mathrm{W}$, in order compare 1/3 PWM against the conventional modulation strategies 2/3 PWM and 3/3 PWM. The results are illustrated in **Fig. 4.16**. 3/3 PWM exhibits the worst performance of $\eta \simeq 96\%$ nominal efficiency due to the continuous switching of all three DC/AC stage half-bridges. Furthermore, when the modulation index exceeds $M > 1$, the DC/DC stage is activated, resulting in additional losses due to the DC/DC stage semiconductor devices and inductor. Therefore, a sharp decrease in efficiency appears for $M > 1$. 2/3 PWM outperforms 3/3 PWM with a nominal efficiency of $\eta \simeq 97.2\%$. When the modulation index exceeds $M > 2/\sqrt{3}$, the DC/DC stage is activated causing a steep drop in efficiency. 1/3 PWM features the highest nominal efficiency, $\eta \simeq 98\%$, thanks to the drastic reduction of the DC/AC stage switching losses. Note that 1/3 PWM does not suffer from an efficiency reduction for $M > 2/\sqrt{3}$ when the DC/DC stage is activated. This is attributed to the continuous transition between the 0 + 2/3 and the 1+1/3 modulation regimes of **Fig. 4.6**. Namely, for 0+2/3 modulation regime the DC/DC stage is not switching, while two phases of the DC/AC stage are switching. For 1 + 1/3 modulation regime the DC/DC stage half-bridge is switching, while only one phase of the DC/AC stage is switching. Therefore,

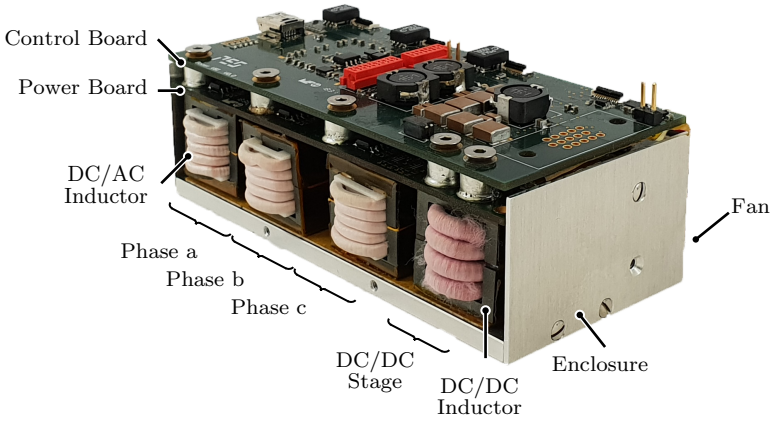


Fig. 4.13: Three-phase converter hardware prototype (cf. **Fig. 4.1(a)**) employed for experimentally verifying the main characteristics of 1/3 PWM. Dimensions 35 mm × 50 mm × 106 mm (11.32 in^3). Besides 1/3 PWM, the hardware prototype supports 2/3 and 3/3 PWM, thus allows for a direct comparison among the three modulation strategies.

Tab. 4.5: Parameter values of the hardware prototype shown in **Fig. 4.13** corresponding to the schematic diagram notation of **Fig. 4.1(a)**.

DC/DC stage	
Switching frequency $f_{s,b}$	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_b	1.5 µH
Capacitance C_b	10 µF
Capacitance C_{DC}	25 µF, (ΔU_{DC} = 0.8 V, a_f = 10)
DC/AC stage	
Switching frequency $f_{s,m}$	300 kHz
Switches (1 device)	200 V EPC 2034
Inductance L_m	4.7 µH
Capacitance C_m	2 µF

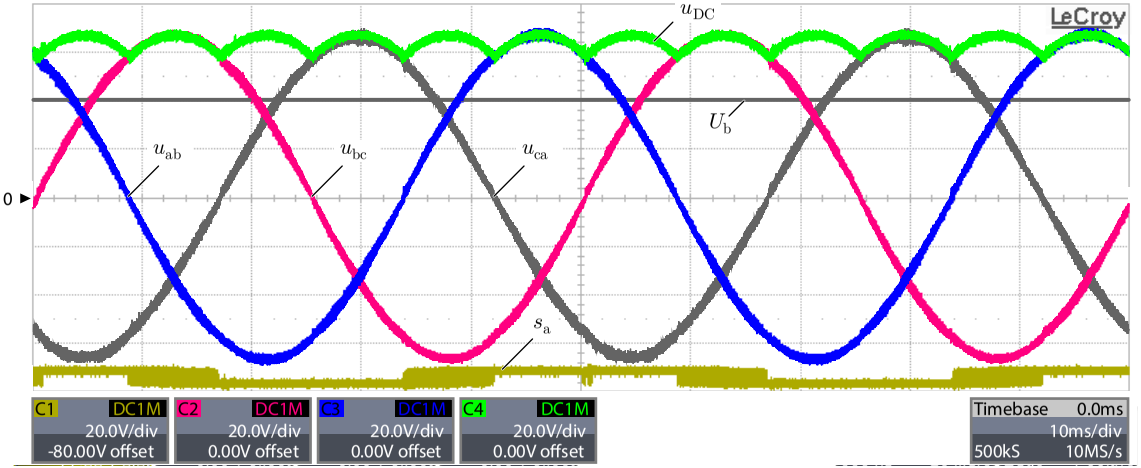


Fig. 4.14: Experimentally measured waveforms of 1/3 PWM for maximum power $P = 500\,\mathrm{W}$, maximum motor voltage $\hat{U}_\mathrm{m} = 40\,\mathrm{V}$, modulation index $M = 2$ and a fundamental frequency of $f_\mathrm{m} = 100\,\mathrm{Hz}$. The motor line-to-line voltages u_ab, u_bc and u_ca, the DC link voltage u_DC and the gating signal of phase a (s_a) are also depicted. The line-to-line voltage u_ca is not directly measured, but instead is reconstructed based on the two other measured line-to-line voltages u_ab and u_bc.

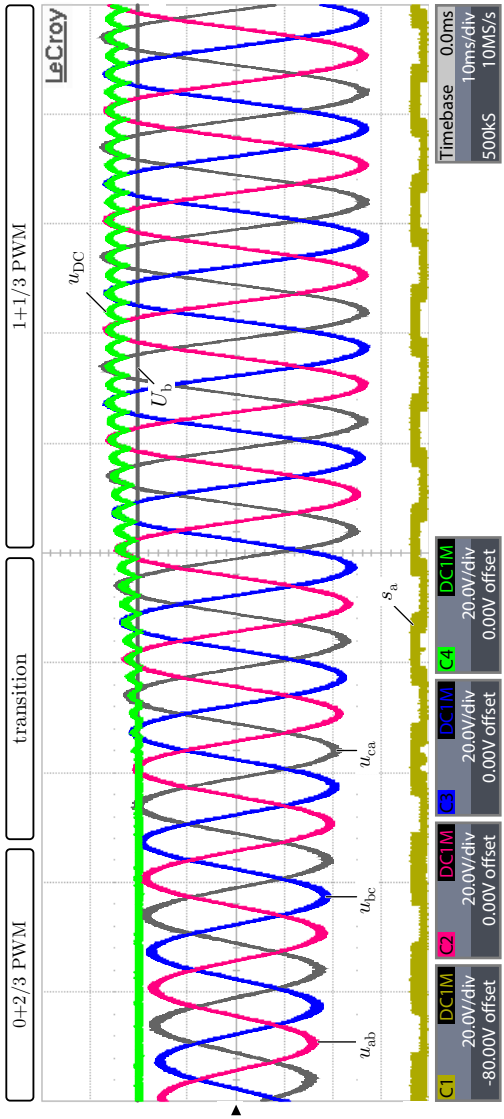


Fig. 4.15: Experimentally measured transition from 2/3 PWM to 1/3 PWM, where the modulation index (and hence the output AC voltage) is gradually increased: $M = 0.5 \rightarrow 1.5$. The motor line-to-line voltages u_{ab}, u_{bc} and u_{ca}, the DC link voltage u_{DC} and the gating signal of phase a (s_a) are also depicted. The line-to-line voltage u_{ca} is not directly measured, but instead is reconstructed based on the two other measured line-to-line voltages u_{ab} and u_{bc}.

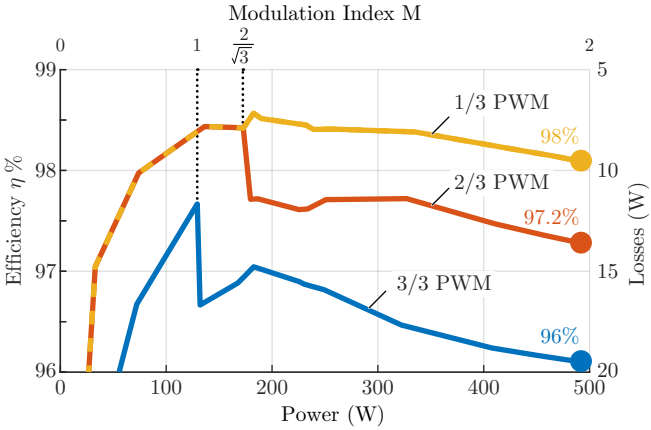


Fig. 4.16: Efficiency of the hardware prototype employing the 1/3 PWM modulation strategy in the whole operating power range $P = 0\,\text{W}...500\,\text{W}$. The efficiency measurement is also performed for the conventional 2/3 PWM and 3/3 PWM, and a clear comparative advantage in favour of 1/3 PWM is deduced.

in any case in total two half-bridges (including the DC/DC and the DC/AC stage) are switching, resulting in a smooth efficiency curve.

Overall, a 10 W (50%) reduction of the overall converter losses is experimentally achieved with 1/3 PWM compared to 3/3 PWM. It can be assumed that this 10 W losses reduction originates mainly from the reduction of the DC/AC stage switching losses under 1/3 PWM, while the rest of the loss contributions either remain the same (e.g. DC/DC stage semiconductor switching/conduction losses and DC/AC stage semiconductor conduction losses), or slightly decrease (e.g. DC/DC stage and DC/AC stage inductor losses), compared to 3/3 PWM. Therefore, the experimentally measured 10 W reduction of the DC/AC stage switching looses with 1/3 PWM, matches well with the respective theoretically calculated value of 10.7 W from **Fig. 4.8**.

Experimentally measured waveforms of the DC/DC stage inductor (L_b) current are shown in **Fig. 4.17(i)**, while the DC/AC stage inductor (L_m) current and current ripple are depicted in **Fig. 4.17(ii)** and **(iii)**, respectively. The results are plotted for the three considered modulation strategies and for a modulation index of $M = 1.75$. It should be noted that the DC/AC stage inductor current ripple shape is unique to the FSF of **Fig. 4.1(a)**, i.e. for filter capacitors C_m connected to the negative DC link rail. 3/3 PWM induces the highest current ripple for both the DC/DC stage inductor L_b and for the

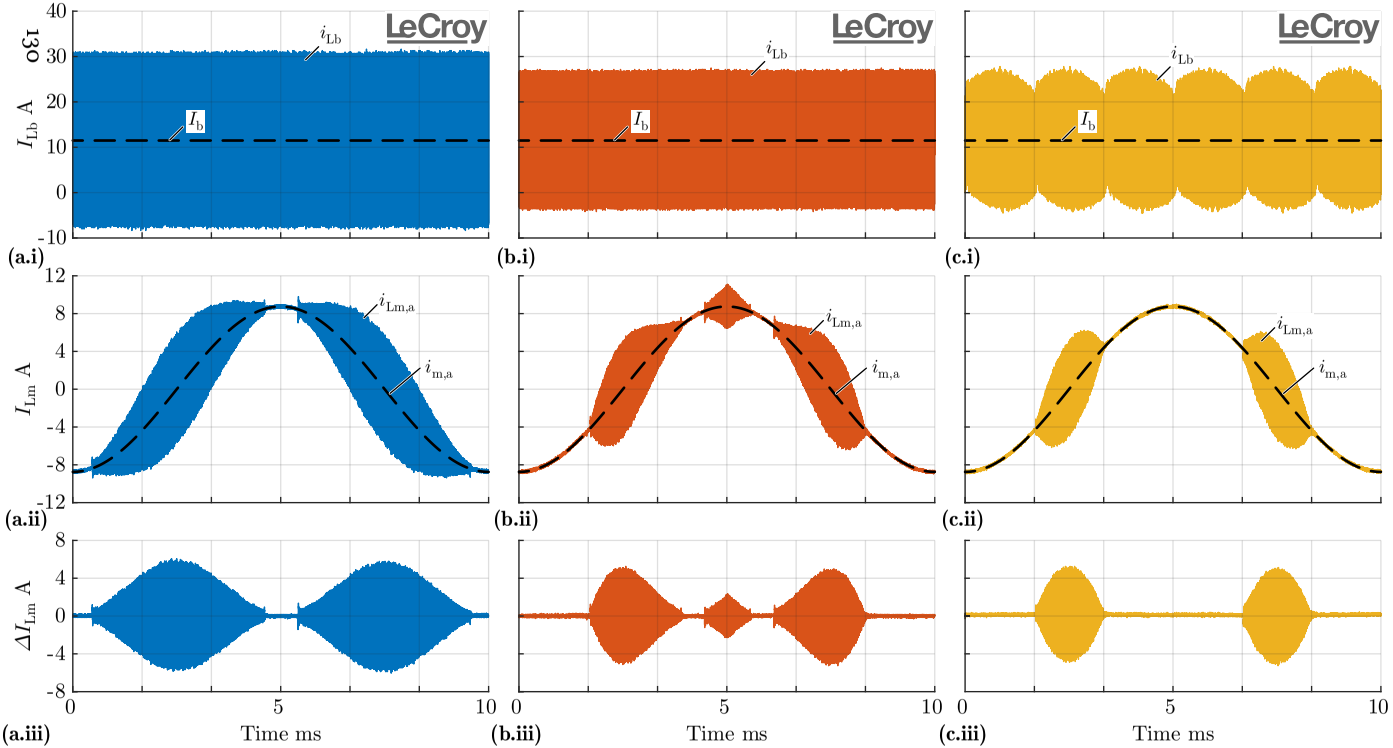


Fig. 4.17: Measured inductor currents for **(a)** 3/3 PWM, **(b)** 2/3 PWM, and **(c)** 1/3 PWM using the hardware demonstrator of **Fig. 4.13**, a modulation index of $M = 1.75$ ($P = 460\,\mathrm{W}$), and a fundamental frequency of $f_m = 100\,\mathrm{Hz}$. **(i)** DC/DC stage inductor L_b current. DC/AC stage L_m output filter inductor **(ii)** current and **(iii)** current ripple (shown for phase a).

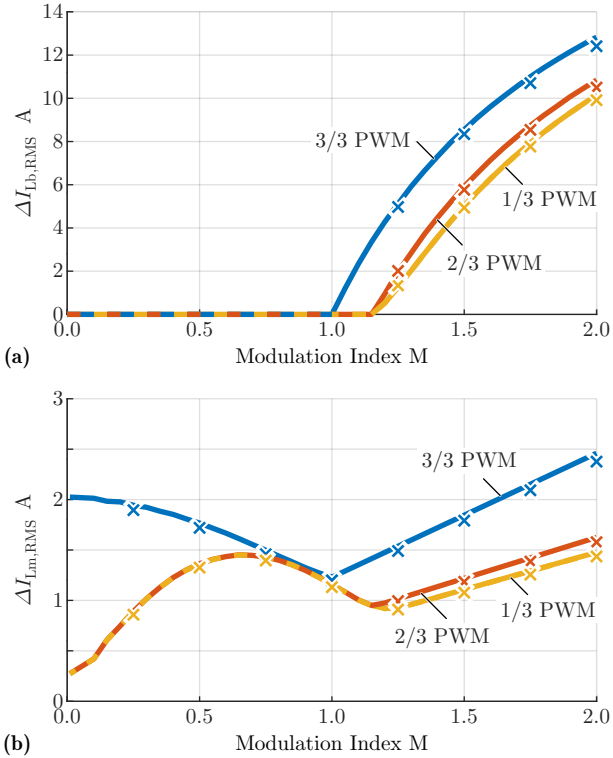


Fig. 4.18: Theoretically calculated inductor RMS current ripple (continuous lines) compared against experimental measurements (x marks). **(a)** Corresponds to the DC/DC stage while **(b)** refers to the DC/AC stage.

DC/AC stage inductors L_m. On the contrary, 1/3 PWM generates the lowest overall current ripple and hence the lowest inductor losses. The 2/3 PWM current ripple performance lies in between the values achieved for 1/3 PWM and 3/3 PWM.

Finally, the experimentally measured RMS inductor current ripple is compared against the theoretically calculated values of **Fig. 4.10**. The results are shown in **Fig. 4.18(a)** and **(b)** for the DC/DC and DC/AC stage, respectively. An excellent matching between the theoretical analysis and the experimental measurements is verified.

4.5 Summary

As shown in this chapter, 1/3 PWM can be applied to three-phase DC/AC converter systems which feature a separate DC/DC and DC/AC stage and are designed to cope with a wide input-output voltage variation (cf. **Fig. 4.1**). 1/3 PWM utilizes a variable DC link voltage instead of a constant DC link voltage used in conventional PWM modulation schemes (cf. **Fig. 4.3**). Thereby, it is possible to generate three-phase sinusoidal line-to-line output voltages by switching always only one out of the three DC/AC stage half-bridges (cf. **Fig. 4.4**). A main advantage of the 1/3 PWM modulation is that it can be easily retrofitted to existing three-phase converter systems by means of a firmware update. In order to quantify the performance advantage of 1/3 PWM, the semiconductor switching losses are analytically calculated and the remaining converter component stresses are comprehensively analysed (cf. **Tab. 4.2-4.4**). It is deduced that 1/3 PWM reduces the switching losses of the DC/AC stage by more than 66% compared to the conventional 3/3 PWM modulation strategy. 1/3 PWM also outperforms the more advanced 2/3 PWM by reducing the switching losses of the latter by at least a factor of two (cf. **Fig. 4.8**). Besides the lower switching losses, 1/3 PWM exhibits similar if not slightly lower current and/or voltage stresses on the remaining converter components compared to the 2/3 PWM modulation strategy. Therefore, 1/3 PWM is a promising modulation technique with substantial advantages over state-of-the-art approaches. Finally, a hardware demonstrator is assembled and tested (cf. **Fig. 4.13**). There, the uncomplicated operation of 1/3 PWM is experimentally validated (cf. **Fig. 4.14-4.15**). Furthermore, 3/3 PWM, 2/3 PWM and 1/3 PWM are applied to the same hardware demonstrator and the corresponding losses are measured over a wide power range. A 2% increase of efficiency, i.e. a loss reduction of 50% is measured for 1/3 PWM compared to 3/3 PWM for the considered application (cf. **Fig. 4.16**).

5
Y-Inverter

This chapter summarizes the key research findings also presented in:

- M. Antivachis, N. Kleynhans, and J. W. Kolar, "Three-phase sinusoidal output buck-boost GaN Y-inverter for advanced variable speed AC drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020, early access. DOI: 10.1109/JESTPE.2020.3026742.

- M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of Y-inverter against three-phase two-stage buck-boost DC-AC converter systems," in *Proc. of International Power Electronics Conference (IPEC-ECCE Asia)*, Niigata, Japan, May 2018, pp. 181-189. DOI: 10.23919/IPEC.2018.8507664.

- M. Antivachis, D. Bortis, L. Schrittwieser, and J. W. Kolar, "Three-phase buck-boost Y-inverter with wide DC input voltage range," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, March 2018, pp. 1492-1499. DOI: 10.1109/APEC.2018.8341214.

Motivation

Conventional buck-boost inverters comprise two energy conversion stages, thus suffer from high losses and require a relatively large volume. In order to overcome the performance barriers of state-of-the-art solutions, a new, single-stage buck-boost inverter topology is proposed in this chapter.

Executive Summary

Motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency η and power density ρ), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery that supplies the motor drive. A promising three-phase inverter topology, denoted as Y-VSI, is presented in this chapter. The Y-VSI is a modular three-phase inverter, and comprises three identical phase-modules connected to a common star "Y" point. Each phase-module is equivalent to a buck-boost DC/DC converter, which allows the AC output voltages to be higher or lower than the DC input voltage. Thereby, the Y-VSI effectively copes with the wide variation of the fuel-cell/battery voltage. Each phase-module can be operated in a similar fashion to a conventional DC/DC converter, independent of the remaining two phases. Accordingly, a straightforward and simple operation/control of the Y-VSI is possible. In addition, the Y-VSI features an integrated output filter. This allows for continuous/sinusoidal motor voltage waveforms, eliminating the need of an additional filter between the inverter and the motor. This chapter details the operating principle of the Y-VSI, and comparatively evaluates two modulation strategies. In order to validate the proposed concepts, a Y-VSI hardware prototype is assembled within the context of a high-speed motor drive. In the investigated drive system, a fuel-cell supplies the Y-VSI, which in return controls a 280krpm 1kW electric compressor. The Y-VSI hardware prototype is compared against a state-of-the-art hardware prototype, which features two energy conversion stages. It is shown that the Y-VSI is $\Delta\eta = +2.3\%$ more efficient and at the same time $\Delta\rho = +10\%$ more power dense compared to the conventional inverter solution.

The electrification of vehicles has created new application opportunities for the power electronics industry [47, 113, 114]. One such application example is shown in **Fig. 5.1(a)**. There, a 10 kW fuel-cell is depicted, which is part of a fuel-cell vehicle powertrain. An auxiliary drive system controls a high-speed 1 kW electric compressor, which in return provides the required oxygen for the fuel-cell unit operation [2]. This compressor drive system is directly supplied by the fuel-cell DC voltage $U_\mathrm{i} = 60\,\mathrm{V}...120\,\mathrm{V}$ and uses 10% of the fuel-cell power. The employed high-speed 280 krpm electric compressor [53] has a nominal phase voltage amplitude of $\hat{U}_\mathrm{o} = 40\,\mathrm{V}$. The system specifications are summarized in **Tab. 5.1**.

In general, motor drives placed on board of vehicles, demand efficient inverter systems in a small form factor. Besides the high performance, the new generation of inverter systems is expected to offer additional functionalities:

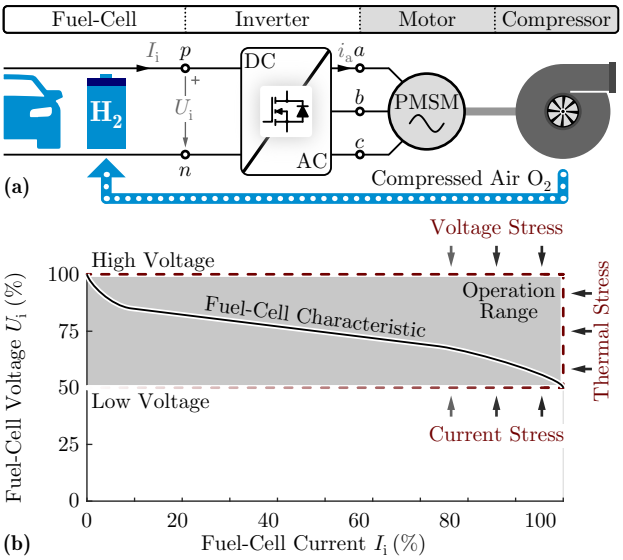


Fig. 5.1: Considered motor drive application. **(a)** An electric compressor provides oxygen to the fuel-cell, while a motor drive, directly supplied by the same fuel-cell, controls the electric compressor. **(b)** Fuel-cell voltage-current characteristic.

Tab. 5.1: Specifications of **Fig. 5.1** motor drive. The nominal operating condition is highlighted in bold.

Fuel-cell voltage	U_i	**60 V**...120 V
Fuel-cell power	P	0 W...**10 kW**
Inverter output freq.	f_m	0 Hz...**5 kHz**
Inverter power	P	0 W...**1100 W**
Motor speed	n	0 rpm...**280 krpm**
Motor voltage	$\hat{U}_m$	0 V...**40 V** (phase, PK)
Motor power	P	0 W...**1000 W**

(i) Buck-boost operation. The inverter system must cope with the wide voltage variation of a fuel-cell. The fuel-cell voltage is highly dependent on the operating point, as depicted in **Fig. 5.1(b)**. The fuel-cell voltage is high when no current is drawn, while the fuel-cell voltage is decreasing as the drawn current increases [43]. The inverter has to always guarantee the full speed range of the motor. That is, the inverter must be able to generate the nominal motor voltage, which is proportional to the motor speed, independent of the input voltage fluctuation. It is noted, that similar considerations apply for inverters supplied by a battery. In this case, the DC input voltage can significantly fluctuate, depending on the charging status and the operating temperature of the battery.

(ii) High quality motor voltage. High-speed motors are an essential component of power dense motor drives, thanks to their small volume/weight. However, such motors are sensitive to poor current quality, which induces high rotor losses [23, 64]. Therefore, the inverter must guarantee high quality, sinusoidal motor voltages/currents. In addition, the fast switching speeds of the latest generation of wide-bandgap (WBG) semiconductor devices cause high $\mathrm{d}u/\mathrm{d}t > 30\,\mathrm{kV/\mu s}$ [26, 27], which poses a great concern for the motor reliability. The most common problem is premature bearing failure due to high common-mode (CM) $\mathrm{d}u/\mathrm{d}t$ [33, 95, 115]. For the above reasons, a DM/CM sine-wave output filter must be placed between the inverter and the motor.

There has been extensive research in literature, towards inverter topologies with a wide input-to-output voltage ratio. A conventional voltage source inverter (VSI), only features buck-type functionality, hence cannot be directly used in the examined application. However, by exchanging the DC link capacitor of a VSI, with an *LC* DC link impedance network, then the Z-source inverter (ZSI) is derived [116, 117]. The ZSI utilizes shoot-through zero states [118, 119], and its unique DC link impedance network, in order to achieve buck-boost capability, i.e. generates AC output voltages which are higher or lower than the input voltage. However, the ZSI suffers from increased voltage/current stress under boost operation, a fact that effectively limits its usability [120–122].

Buck-boost inverters with two energy conversion stages, as shown in **Fig. 5.2**, have found broad acceptance. In order to enable boost functionality, a boost-type DC/DC converter is placed before a VSI. The dedicated boost-type DC/DC converter (DC/DC stage) adapts the fluctuating input voltage U_i to a

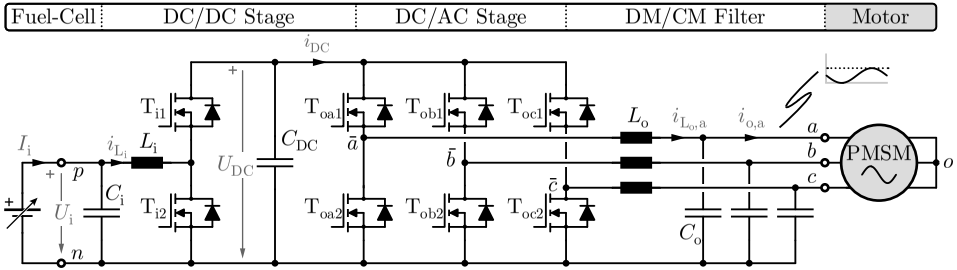


Fig. 5.2: State-of-the-art boost voltage source inverter (B-VSI) solution for a motor drive with a wide input-to-output voltage ratio. The B-VSI is a two-stage converter: a dedicated DC/DC stage steps-up the fuel-cell voltage U_i to a higher DC link voltage U_DC, while a DC/AC stage generates the three-phase motor voltage system. A differential-mode/common-mode (DM/CM) filter is placed between the inverter and the motor, in order to ensure continuous/sinusoidal motor voltages.

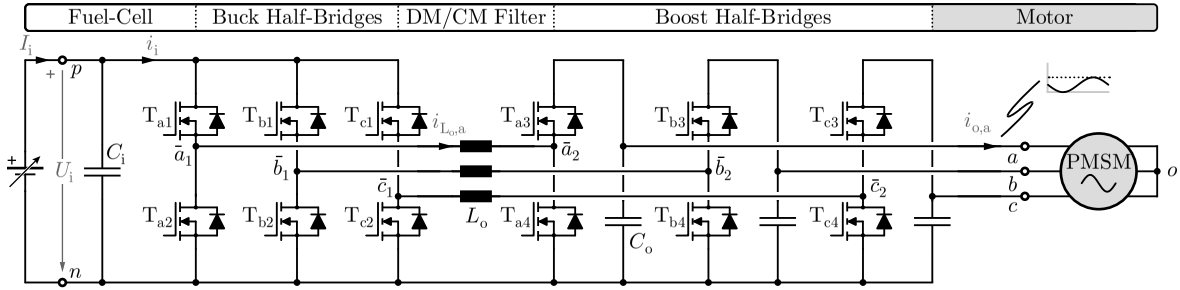


Fig. 5.3: Proposed Y voltage source inverter (Y-VSI) solution for a motor drive with a wide input-to-output voltage ratio. Three identical buck-boost phase-modules comprise the Y-VSI, as is highlighted in **Fig. 5.4**. The Y-VSI features an integrated differential-mode/common-mode (DM/CM) output filter, thereby sinusoidal motor voltages/currents are generated.

higher DC link voltage U_{DC}, when necessary. The DC link voltage supplies the VSI, which generates the AC motor voltages (DC/AC stage). A DM/CM filter is placed after the VSI in order to ensure high quality voltage for the motor. This popular inverter solution is denoted as boost-VSI (B-VSI). This two-stage inverter [106,108,109] processes the transmitted power twice, first in the DC/DC stage and then in the DC/AC stage, thus the overall performance is compromised. The increased number of inductive components and semiconductor losses originating from the DC/DC stage result in a low efficiency and a relatively large volume.

A current source inverter (CSI) based solution can be used instead of the B-VSI [123, 124]. The CSI is inherently a boost-type inverter [125–127], i.e. it generates AC output voltages which are strictly greater than the input voltage. In order to enable buck functionality, in addition to the inherent boost functionality of the CSI, a buck-type DC/DC converter must precede the CSI. Therefore, a two-stage inverter topology results, denoted as buck-CSI (B-CSI) [128, 129]. The switches of the CSI have to be realized with two anti-series connected devices (two anti-series MOSFETs or a MOSFET anti-series connected with a diode) [130], a fact that potentially leads to higher complexity, reliability concerns and higher conduction losses. This is a drawback of the B-CSI which limits its practical use.

In response to the shortcomings of the state-of-the-art inverter solutions, the Y-VSI inverter topology of **Fig. 5.3**, is proposed in this chapter. The Y-VSI is based on the well established idea of modular three-phase inverters [131–137], where three identical DC/DC converters are connected to a common star "Y" point. In the case of the Y-VSI, each phase-module is equivalent to a non-isolated buck-boost DC/DC converter, while the three phase-modules are connected to the negative DC rail n (star point). The modular concept employed by the Y-VSI is highlighted in **Fig. 5.4**. The Y-VSI benefits from four key features:

(i) Buck-boost capability. Thanks to the inherent buck-boost characteristic of each phase-module, the AC output voltage can be higher or lower than the DC input voltage.

(ii) High efficiency. The Y-VSI processes the transmitted power P in a unique way. In the typical case, only three out of the six half-bridges are switched, at any given point in time. As a result, low switching losses are generated and a high inverter efficiency is achieved.

(iii) High quality motor voltage. The Y-VSI features an integrated $L_o - C_o$ output filter, hence generates continuous/sinusoidal motor voltages.

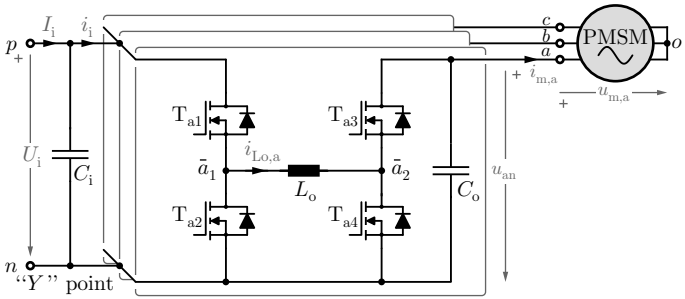


Fig. 5.4: Modular three-phase inverter concept. Three identical buck-boost DC/DC converters are referenced to a common star "Y" point (negative DC rail n) in order to assemble a modular three-phase inverter system.

Therefore, no additional filter is required, between the inverter and the motor.

(iv) Simple control strategy. Each phase-module can be controlled independent of the remaining two phases and employs a simple control configuration, similar to conventional DC/DC converters.

In a first step, the operating principle of the Y-VSI is explained in **Sec. 5.1**. In particular, two modulation strategies are proposed, while the uncomplicated control of the Y-VSI is highlighted. In **Sec. 5.2** and **Sec. 5.3**, the voltage/current stresses on the different inverter components are analytically derived, and a comprehensive design guideline is presented. The proposed concept is experimentally validated in **Sec. 5.4**. A Y-VSI hardware prototype and a conventional B-VSI hardware prototype are purposely assembled and compared for the specifications of **Tab. 5.1**. The experimental results validate the performance benefits derived from the Y-VSI technology. Finally, a summary is given in **Sec. 5.5**.

5.1 Modulation Strategies

A three-phase inverter system can be constructed in a modular way [132–137] as is visualised in **Fig. 5.4**. Three identical phase-modules, each comprising a non-isolated DC/DC converter, are connected to a common star "Y" point. Following this modular inverter concept, the Y-VSI of **Fig. 5.3** consists of three buck-boost DC/DC converters [138] connected to the negative DC rail

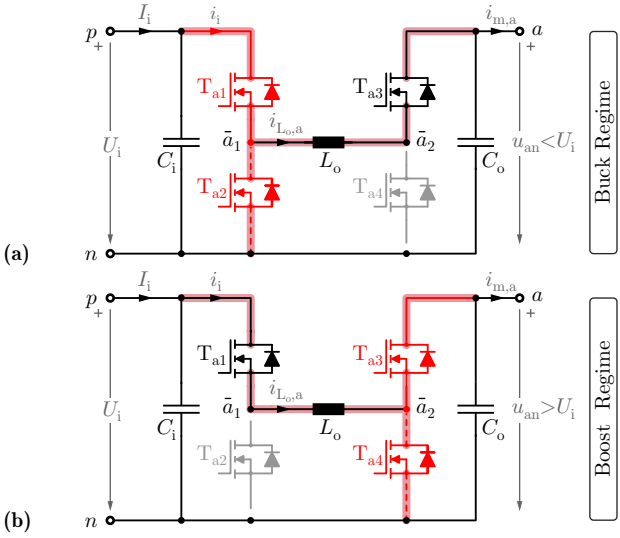


Fig. 5.5: (a) Buck regime of the Y-VSI, where the output voltage is lower than the input voltage $u_{an}(t) \leq U_i$ and **(b)** boost regime, where the output voltage is greater than the input voltage $u_{an}(t) > U_i$.

n (star point). The phase a module comprises two half-bridges, the buck half-bridge $\bar{a}_1$ and the boost half-bridge $\bar{a}_2$, connected to the opposite terminals of an inductor L_o. When the inverter output voltage is lower than the input voltage $u_{an} \leq U_i$, the Y-VSI operates in buck regime of **Fig. 5.5(a)**, where only the buck half-bridge $\bar{a}_1$ is switched. Contrary, when the inverter output voltage is higher than the input voltage $u_{an} > U_i$, the Y-VSI operates in boost regime of **Fig. 5.5(b)**, where only the boost half-bridge $\bar{a}_2$ is switched. Furthermore, phase a includes an output capacitor C_o, placed between the output terminal a and the negative DC rail n. The Y-VSI generates three sinusoidal motor phase voltages

$$\begin{aligned} u_{m,a}(t) &= u_{ao} = \hat{U}_m \cos(\omega_m t) \\ u_{m,b}(t) &= u_{bo} = \hat{U}_m \cos(\omega_m t - \frac{2\pi}{3}), \\ u_{m,c}(t) &= u_{co} = \hat{U}_m \cos(\omega_m t + \frac{2\pi}{3}) \end{aligned} \tag{5.1}$$

where $\omega_m = 2\pi f_m$ is the motor fundamental angular velocity. The resulting sinusoidal motor currents are

$$\begin{aligned} i_{m,a}(t) &= \hat{I}_m \cos(\omega_m t - \phi) \\ i_{m,b}(t) &= \hat{I}_m \cos(\omega_m t - \frac{2\pi}{3} - \phi) \\ i_{m,c}(t) &= \hat{I}_m \cos(\omega_m t + \frac{2\pi}{3} - \phi) \end{aligned}. \tag{5.2}$$

For the sake of simplicity, the motor voltage is considered to be in phase with the motor current (unity power factor $\cos(\phi) = 1 \leftrightarrow \phi = 0$). The modulation index that relates the motor phase voltage amplitude $\hat{U}_m$ to the fuel-cell voltage U_i is defined as

$$M = \frac{\hat{U}_m}{\frac{1}{2}U_i}. \tag{5.3}$$

The modulation index M can exceed the value of $2/\sqrt{3}$, which is the limit of a conventional VSI, thanks to the inherent buck-boost capability of the Y-VSI. Each phase-module is independent of the remaining two phases, thus the analysis is from now on focused on phase a, when possible.

5.1.1 Sinusoidal Modulation (SPWM)

The sinusoidal motor voltage u_{ao} cannot be directly generated by phase-module a. The motor phase voltage u_{ao} assumes negative values, during the negative half-cycle ($\pi/2 < \varphi < 3\pi/2$), while the output voltage of the phase a module (DC/DC converter) must be strictly positive $u_{an} \geq 0$. Instead of sinusoidal voltages, the phase-modules $[a, b, c]$ generate sinusoidal voltages with an offset u_{off}

$$\begin{aligned} u_{an}(t) &= \hat{U}_m \cos(\omega_m t) + u_{off} \\ u_{bn}(t) &= \hat{U}_m \cos(\omega_m t - \frac{2\pi}{3}) + u_{off}, \\ u_{cn}(t) &= \hat{U}_m \cos(\omega_m t + \frac{2\pi}{3}) + u_{off} \end{aligned} \tag{5.4}$$

such that the output voltages remains always positive e.g. $u_{an}(t) \geq 0$. In a first step, a constant offset voltage is selected

$$u_{off} = \hat{U}_m. \tag{5.5}$$

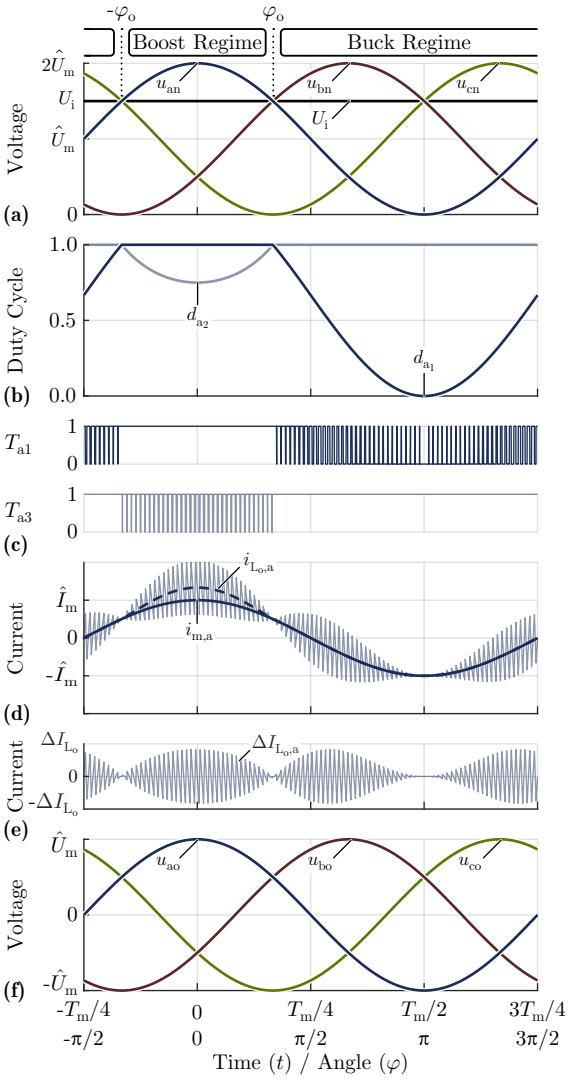


Fig. 5.6: Sinusoidal modulation strategy (SPWM) characteristic waveforms. **(a)** Inverter output voltages (offseted sinusoidal shape). **(b)** Phase *a* duty cycles followed by **(c)** gate signals. **(d)** Phase *a* filter inductor current and motor current, **(e)** filter inductor current ripple and **(f)** motor voltages.

Therefore, three sinusoidal voltages with the same constant offset voltage are generated with respect to the Y-VSI star point n. The phase a output voltage is

$$u_{\mathrm{an}}(\varphi) = \hat{U}_{\mathrm{m}}(\cos(\varphi) + 1). \tag{5.6}$$

The Y-VSI output voltages in this case are visualized in **Fig. 5.6(a)**. Even though the inverter output voltages are offseted sinusoids, the line-to-line voltages u_{ab}, u_{bc} and u_{ca} are sinusoidal. Accordingly, sinusoidal motor phase voltages/currents appear. Since the inverter output voltages have an offseted sinusoidal shape, the current modulation strategy is denoted as sinusoidal pulse width modulation (SPWM). It is noted that, the offset voltage $u_{\mathrm{off}} = \hat{U}_{\mathrm{m}}$ is common to all three phases, hence constitutes by definition a common-mode (CM) voltage component. A CM voltage component cannot drive any current in a three-phase motor with a floating neutral point o.

The characteristic waveforms of a Y-VSI employing SPWM are analysed in the following. Depending on the instantaneous motor voltage $u_{\mathrm{ao}}(t)$ value, the output inverter voltage $u_{\mathrm{an}}(t)$ can be higher or lower than the input voltage U_{i}. Accordingly, phase-module a operates in buck or boost regime as highlighted in **Fig. 5.6(a)**

$$\begin{array}{lll} \text{buck regime} & m_{\mathrm{a}}(\varphi) \leq 1, & +\varphi_{\mathrm{o}} < \varphi < 2\pi - \varphi_{\mathrm{o}} \\ \text{boost regime} & m_{\mathrm{a}}(\varphi) > 1, & -\varphi_{\mathrm{o}} < \varphi < +\varphi_{\mathrm{o}} \end{array}, \tag{5.7}$$

where m_{a} is the modulation factor, showing the instantaneous ratio between the inverter output voltage and the input voltage

$$m_{\mathrm{a}}(\varphi) = u_{\mathrm{an}}(\varphi)/U_{\mathrm{i}}. \tag{5.8}$$

The transition angle from boost to buck regime is

$$\varphi_{\mathrm{o}} = \cos^{-1}\left(\frac{U_{\mathrm{i}} - \hat{U}_{\mathrm{m}}}{\hat{U}_{\mathrm{m}}}\right) \overset{(5.3)}{=} \cos^{-1}\left(\frac{2}{M} - 1\right). \tag{5.9}$$

During buck regime in **Fig. 5.6(c)**, the half-bridge $\bar{a}_1$ (devices $T_{\mathrm{a1}} - T_{\mathrm{a2}}$) is operated with the switching frequency f_{s}, while the high-side switch T_{a3} of the half-bridge $\bar{a}_2$ is continuously turned-on (clamped). In this case, phase-module a reduces to a simple buck converter as highlighted in **Fig. 5.5(a)**. During boost regime in **Fig. 5.6(c)**, the half-bridge $\bar{a}_2$ (devices $T_{\mathrm{a3}} - T_{\mathrm{a4}}$) is operated with the switching frequency f_{s}, while the high-side switch T_{a1} of the half-bridge $\bar{a}_1$ is continuously turned-on (clamped). In this case, phase-module a reduces to a simple boost converter as highlighted in **Fig. 5.5(b)**.

Depending on the instantaneous output voltage reference $u_{\mathrm{an}}(t)$, the inverter transitions seamlessly between buck and boost regime.

The two half-bridges $\bar{a}_1$ and $\bar{a}_2$ are operated in a mutually exclusive fashion. That is, only one half-bridge is in switching operation, while the high-side switch of the other half-bridge is continuously turned on. In total, only three half-bridges are switched, at any given point in time. As a result, low switching losses are generated and high inverter efficiency is achieved. Note that a simple VSI employing SPWM results in continuous switching of three half-bridges, which is the same as for the Y-VSI. A VSI is a single-stage inverter from a power conversion perspective. Accordingly, a Y-VSI can also be considered as a single-stage inverter topology, based on the number of switched half-bridges.

The characteristic waveforms of phase a, which are illustrated in **Fig. 5.6**, are half-period symmetric. Therefore, the analytic expressions of those waveforms are calculated for only half of the fundamental period, i.e. in the interval $0 < \varphi = \omega_{\mathrm{m}} t < \pi$. The duty cycles d_{a_1} and d_{a_2} which control the high-side switches of the half-bridges $\bar{a}_1$ and $\bar{a}_2$, respectively, are now calculated. Each point in time t of the offseted sinusoidal output voltage $u_{\mathrm{an}}(t)$, can be considered as a quasi-static operating point of the DC/DC converter phase-module. This is true because the switching frequency is much higher compared to the motor fundamental frequency $f_{\mathrm{s}} \gg f_{\mathrm{m}}$. Thereby, the duty cycles d_{a_1} and d_{a_2} can be derived

$$d_{\mathrm{a}_1}(\varphi) = \min\left[1, m_{\mathrm{a}}(\varphi)\right] = \begin{cases} 1, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ m_{\mathrm{a}}(\varphi), & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}, \tag{5.10}$$

$$d_{\mathrm{a}_2}(\varphi) = \min\left[1, \frac{1}{m_{\mathrm{a}}(\varphi)}\right] = \begin{cases} \dfrac{1}{m_{\mathrm{a}}(\varphi)}, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ 1, & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}. \tag{5.11}$$

The resulting duty cycles for the SPWM modulation are visualized in **Fig. 5.6(b)** and are calculated based on **(5.6)** as

$$d_{\mathrm{a}_1}(\varphi) = \begin{cases} 1, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ \dfrac{M(1+\cos(\varphi))}{2}, & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}, \tag{5.12}$$

$$d_{\mathrm{a}_2}(\varphi) = \begin{cases} \dfrac{2}{M(1+\cos(\varphi))}, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ 1, & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}. \tag{5.13}$$

Tab. 5.2: Y-VSI characteristic waveforms, for sinusoidal modulation (SPWM) and discontinuous modulation (DPWM).

	SPWM ($M \geq 1$)	
$u_{\mathrm{off}}(\varphi)$	$\hat{U}_{\mathrm{m}}$	
$u_{\mathrm{an}}(\varphi)$	$\hat{U}_{\mathrm{m}}(\cos(\varphi)+1)$	
φ_{o}	$\cos^{-1}\left(\frac{2}{M}-1\right)$	
$d_{\mathrm{a_1}}(\varphi)$	$1,$	$0 < \varphi \leq \varphi_{\mathrm{o}}$
	$\frac{M(1+\cos(\varphi))}{2},$	$\varphi_{\mathrm{o}} < \varphi \leq \pi$
$d_{\mathrm{a_2}}(\varphi)$	$\frac{2}{M(1+\cos(\varphi))},$	$0 < \varphi \leq \varphi_{\mathrm{o}}$
	$1,$	$\varphi_{\mathrm{o}} < \varphi \leq \pi$
$i_{\mathrm{L_{o,a}}}(\varphi)$	$\hat{I}_{\mathrm{m}}\cos(\varphi)\frac{M}{2}(\cos(\varphi)+1),$	$0 < \varphi \leq \varphi_{\mathrm{o}}$
	$\hat{I}_{\mathrm{m}}\cos(\varphi),$	$\varphi_{\mathrm{o}} < \varphi \leq \pi$
	DPWM ($M \geq 4/3$)	
$u_{\mathrm{off}}(\varphi)$	$-\min[u_{\mathrm{ao}}(\varphi), u_{\mathrm{bo}}(\varphi), u_{\mathrm{co}}(\varphi)]$	
$u_{\mathrm{an}}(\varphi)$	$\hat{U}_{\mathrm{m}}(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3})),$	$0 < \varphi < 2\pi/3$
	$0,$	$2\pi/3 < \varphi < \pi$
φ_{o}	$\cos^{-1}\left(\frac{2}{\sqrt{3}M}\right)+\frac{\pi}{6}$	
$d_{\mathrm{a_1}}(\varphi)$	$1,$	$0 < \varphi \leq \varphi_{\mathrm{o}}$
	$\frac{M(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3}))}{2},$	$\varphi_{\mathrm{o}} < \varphi \leq 2\pi/3$
	$0,$	$2\pi/3 < \varphi \leq \pi$
$d_{\mathrm{a_2}}(\varphi)$	$\frac{2}{M(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3}))},$	$0 < \varphi \leq \varphi_{\mathrm{o}}$
	$1,$	$\varphi_{\mathrm{o}} < \varphi \leq \pi$
$i_{\mathrm{L_{o,a}}}(\varphi)$	$\hat{I}_{\mathrm{m}}\cos(\varphi)\frac{M}{2}(\cos(\varphi)-\cos(\varphi+\frac{2\pi}{3})),$	$0 < \varphi \leq \varphi_{\mathrm{o}}$
	$\hat{I}_{\mathrm{m}}\cos(\varphi),$	$\varphi_{\mathrm{o}} < \varphi \leq \pi$

Each phase-module features an integrated output filter ($L_\mathrm{o} - C_\mathrm{o}$) which allows for the continuous output voltages of **Fig. 5.6(a)**. The filter inductor characteristics are now analysed. The inductor current comprises a fundamental current component $i_{\mathrm{L_o}}(\varphi)$ and a current ripple $\Delta i_{\mathrm{L_o}}(\varphi)$ which is the result of the PWM operation. The low-frequency inductor current component is

$$i_{\mathrm{L_o,a}}(\varphi) = \frac{i_{\mathrm{m,a}}}{d_{\mathrm{a_2}}} = \begin{cases} \hat{I}_\mathrm{m} \cos(\varphi) \dfrac{1}{d_{\mathrm{a_2}}}, & 0 < \varphi \leq \varphi_\mathrm{o} \\ \hat{I}_\mathrm{m} \cos(\varphi), & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \tag{5.14}$$

In the case of SPWM, the inductor current is depicted in **Fig. 5.6(d)** and is calculated based on **(5.2)** and **(5.13)** as

$$i_{\mathrm{L_o,a}}(\varphi) = \begin{cases} \hat{I}_\mathrm{m} \cos(\varphi) \dfrac{M}{2} (\cos(\varphi) + 1), & 0 < \varphi \leq \varphi_\mathrm{o} \\ \hat{I}_\mathrm{m} \cos(\varphi), & \varphi_\mathrm{o} < \varphi \leq \pi \end{cases}. \tag{5.15}$$

The inductor current waveform is non-sinusoidal. The maximum inductor current occurs during boost regime for $\varphi = 0$ and is

$$\hat{I}_{\mathrm{L_o}} = \hat{I}_\mathrm{m} M, \tag{5.16}$$

which is greater than the motor current amplitude $\hat{I}_\mathrm{m}$. The inductor current of **(5.15)** can be approximated by a simpler waveform

$$i_{\mathrm{L_o,a}}(\varphi) = \hat{I}_\mathrm{m} \left(\frac{M+1}{2} \cos(\varphi) + \frac{M-1}{2} \right), \tag{5.17}$$

which allows to calculate the RMS current of the filter inductor

$$I_{\mathrm{L_o,RMS}} = \frac{\hat{I}_\mathrm{m}}{\sqrt{2}} \frac{\sqrt{3M^2 - 2M + 3}}{2}. \tag{5.18}$$

The current ripple of the inductor $\Delta i_{\mathrm{L_o}}$ is isolated in **Fig. 5.6(e)**. The maximum occurring current ripple value (single-side amplitude) is

$$\Delta I_{\mathrm{L_o}} = \max \left[1, 4 \frac{M-1}{M} \right] \cdot \frac{U_\mathrm{i}}{8 L_\mathrm{o} f_\mathrm{s}}. \tag{5.19}$$

Finally, the output capacitor C_o is analysed. The voltage u_an across the capacitor is continuous, thus the Y-VSI provides a high quality voltage for the motor and no additional filtering is required at the AC output side. A

voltage ripple Δu_{C_o} is superimposed to the filter capacitor C_o voltage due to the PWM operation of the Y-VSI. The maximum occurring voltage ripple value (single-side amplitude) is

$$\Delta U_{C_o} = \Delta U_{an} = \max\left[\frac{U_i}{64 L_o C_o f_s^2}, \frac{M\hat{I}_m}{8 C_o f_s}\right]. \tag{5.20}$$

A voltage ripple of $\Delta U_{an} < 2\,\mathrm{V}$ should be achieved, in order to avoid parasitic bearing currents [71, 96].

The characteristic waveforms, corresponding to SPWM modulation strategy, are summarized in **Tab. 5.2**. The derived formulas are valid for a modulation index $M \geq 1$. For this modulation index range, the Y-VSI transitions between buck and boost regime (cf. **Fig. 5.5** and **5.6**). For a lower modulation index $M = 0...1$ the Y-VSI operates exclusively in buck regime, over the whole fundamental period, hence is equivalent to a simple VSI. The properties of the Y-VSI in the modulation range $M = 0...1$ are discussed in **Sec. 5.3**.

5.1.2 Discontinuous Modulation (DPWM)

The offset voltage u_{off} of **(5.4)**, was selected to be constant for the sinusoidal modulation (SPWM), in **(5.5)**. However, this is not necessary: The offset voltage u_{off} is a degree of freedom that can be utilized in order to further improve the inverter performance. By selecting a time-varying offset voltage $u_{off}(t)$ significant performance advantages can be achieved.

In the case of a two-level VSI, this degree of freedom has been extensively detailed in literature. By employing a time-varying offset voltage and/or common-mode voltage injection [59], different modulation strategies are derived: For example, in the case of third harmonic injection [55], a sinusoidal offset voltage (third harmonic) is injected, while in the case of triangular voltage insertion [60], a triangular offset voltage is used. These modulation strategies allow for an optimal utilization of the VSI DC link voltage. In the case of discontinuous modulation (DPWM) [61], it is possible to generate a three-phase voltage system for the motor by switching only two out of the three phases of the VSI. Accordingly, the switching losses of the VSI are significantly reduced. There are many variants of DPWM [62], but in all cases a discontinuous offset voltage is injected.

The DPWM modulation concept is now extended for the Y-VSI. In particular, the time-varying offset voltage is

$$u_{off}(t) = -\min[u_{ao}(t), u_{bo}(t), u_{co}(t)]. \tag{5.21}$$

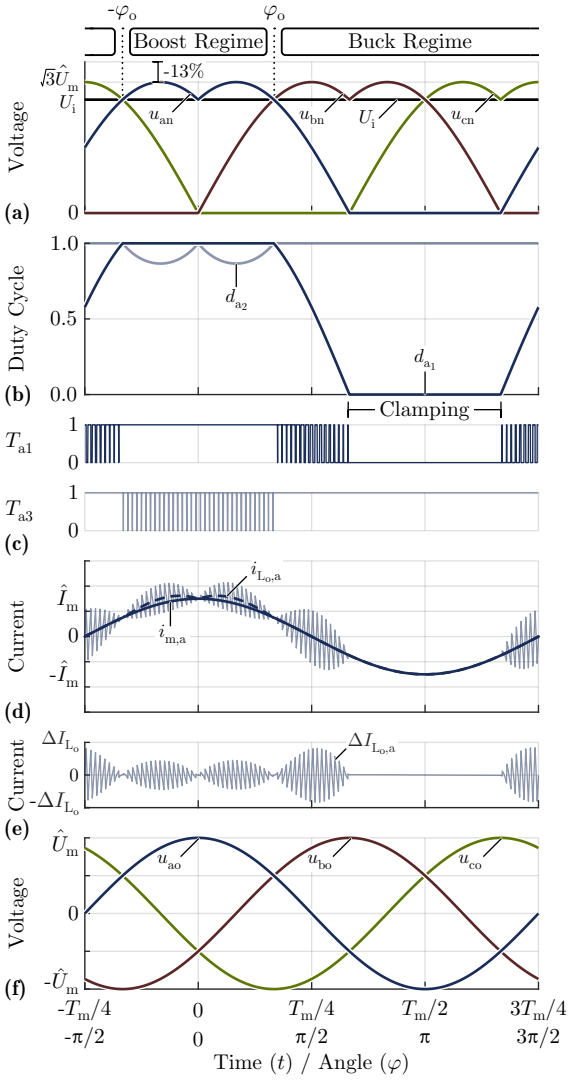


Fig. 5.7: Discontinuous modulation strategy (DPWM) characteristic waveforms. **(a)** Inverter output voltages (non-sinusoidal shape). **(b)** Phase *a* duty cycles followed by **(c)** gate signals. **(d)** Phase *a* filter inductor current and motor current, **(e)** filter inductor current ripple and **(f)** motor voltages.

The Y-VSI output voltages are equal to the sum of the respective motor voltages and the offset voltage, according to **(5.4)**. The three-phase output voltages are illustrated in **Fig. 5.7(a)**, while the output voltage of phase a in particular is

$$u_{\mathrm{an}}(\varphi) = \begin{cases} u_{\mathrm{ao}} - u_{\mathrm{bo}}, & -\dfrac{2\pi}{3} < \varphi < 0 \\ u_{\mathrm{ao}} - u_{\mathrm{co}}, & 0 < \varphi < \dfrac{2\pi}{3} \\ u_{\mathrm{ao}} - u_{\mathrm{ao}}, & \dfrac{2\pi}{3} < \varphi < \dfrac{4\pi}{3} \end{cases} \tag{5.22}$$

$$u_{\mathrm{an}}(\varphi) = \begin{cases} \hat{U}_{\mathrm{m}} \left[\cos(\varphi) - \cos(\varphi - \dfrac{2\pi}{3}) \right], & -\dfrac{2\pi}{3} < \varphi < 0 \\ \hat{U}_{\mathrm{m}} \left[\cos(\varphi) - \cos(\varphi + \dfrac{2\pi}{3}) \right], & 0 < \varphi < \dfrac{2\pi}{3} \\ 0, & \dfrac{2\pi}{3} < \varphi < \dfrac{4\pi}{3} \end{cases} . \tag{5.23}$$

According to DPWM, the phase with the most negative motor voltage is clamped to the negative DC rail n, for one third of the fundamental period $T_{\mathrm{m}}/3$. Phase a in particular is clamped for the interval $\frac{2\pi}{3} < \varphi < \frac{4\pi}{3}$ in **Fig. 5.7(c)**. The output voltages of **Fig. 5.7(a)** have a non-sinusoidal shape, however the line-to-line motor voltages are sinusoidal. Therefore, it is possible by means of DPWM to generate a sinusoidal three-phase motor voltage system with non-sinusoidal inverter output voltages. The DPWM modulation benefits from two key advantages compared to SPWM:

(i) Reduction of the total number of Y-VSI switching transitions by 33%. During one third of the fundamental motor period $T_{\mathrm{m}}/3$ (i.e. the interval $\frac{2\pi}{3} < \varphi < \frac{4\pi}{3}$), the phase-module a is clamped, thus no switching losses are generated from this phase-module.

(ii) Reduction of the voltage stress on the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ by 13%. The phase a boost half-bridge $\bar{a}_2$ processes/switches the output voltage u_{an}. The DPWM can generate the same motor phase voltage amplitude $\hat{U}_{\mathrm{m}}$ as SPWM, but with the non-sinusoidal output voltages of **Fig. 5.7(a)**. The maximum value of the output voltage is $U_{\mathrm{an,PK}} = \sqrt{3}\hat{U}_{\mathrm{m}}$ which is 13% lower compared to the respective value for SPWM $U_{\mathrm{an,PK}} = 2\hat{U}_{\mathrm{m}}$.

The characteristic waveforms of a Y-VSI employing DPWM are analysed in the following. Depending on the instantaneous motor voltage $u_{\mathrm{ao}}(t)$ value,

the output inverter voltage $u_{\mathrm{an}}(t)$ can be higher or lower than the input voltage U_{i}. Accordingly, the phase-module a operates in boost regime (cf. **Fig. 5.5(b)**) or buck regime (cf. **Fig. 5.5(a)**). The two operation regimes are highlighted in **Fig. 5.7(a)** and are analytically expressed in **(5.7)**. The angle φ_{o}, where the transition from boost to buck regime occurs, is

$$\varphi_{\mathrm{o}} = \cos^{-1}\left(\frac{U_{\mathrm{i}}}{\sqrt{3}\hat{U}_{\mathrm{m}}}\right) + \frac{\pi}{6} \overset{(5.3)}{=} \cos^{-1}\left(\frac{2}{\sqrt{3}M}\right) + \frac{\pi}{6}. \tag{5.24}$$

The duty cycles d_{a_1} and d_{a_2}, that control the half-bridges $\bar{a}_1$ and $\bar{a}_2$, are illustrated in **Fig. 5.7(b)** and are calculated based on **(5.10)** and **(5.11)** as

$$d_{\mathrm{a}_1}(\varphi) = \begin{cases} 1, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ \dfrac{M(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}))}{2}, & \varphi_{\mathrm{o}} < \varphi \leq \dfrac{2\pi}{3} \\ 0, & \dfrac{2\pi}{3} < \varphi \leq \pi \end{cases}, \tag{5.25}$$

$$d_{\mathrm{a}_2}(\varphi) = \begin{cases} \dfrac{2}{M(\cos(\varphi) - \cos(\varphi + \frac{2\pi}{3}))}, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ 1, & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}. \tag{5.26}$$

The integrated output filter is finally analysed, starting from the filter inductor L_{o}. In the case of DPWM, the inductor current is depicted in **Fig. 5.7(d)** and is calculated based on **(5.2)**, **(5.14)** and **(5.26)** as

$$i_{\mathrm{L_o,a}}(\varphi) = \begin{cases} \hat{I}_{\mathrm{m}} \cos(\varphi) \dfrac{M}{2} (\cos(\varphi) - \cos(\varphi + \dfrac{2\pi}{3})), & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ \hat{I}_{\mathrm{m}} \cos(\varphi), & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}. \tag{5.27}$$

The inductor current waveform is non-sinusoidal, and is approximated by a simpler waveform

$$i_{\mathrm{L_o}}(\varphi) = \hat{I}_{\mathrm{m}} \left(\frac{M\sqrt{3} + 2}{4} \cos(\varphi) + \frac{M\sqrt{3} - 2}{4} \right). \tag{5.28}$$

The maximum inductor current is greater than the motor current amplitude $\hat{I}_{\mathrm{m}}$ and occurs during boost regime

$$\hat{I}_{\mathrm{L_o}} = \hat{I}_{\mathrm{m}} \frac{\sqrt{3}}{2} M, \tag{5.29}$$

while the RMS current of the filter inductor is

$$I_{\mathrm{L_o,RMS}} = \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}} \frac{\sqrt{9M^2 - 4\sqrt{3}M + 12}}{4}. \tag{5.30}$$

A current ripple is superimposed to the inductor current due to the PWM operation of the Y-VSI (cf. **Fig. 5.7(d)**). The current ripple of the inductor $\Delta i_{\mathrm{L_o}}$ is isolated in **Fig. 5.6(e)**, while the maximum occurring current ripple value (single-side amplitude) is

$$\Delta I_{\mathrm{L_o}} = \max \left[1, 4 \frac{\frac{\sqrt{3}}{2}M - 1}{\frac{\sqrt{3}}{2}M} \right] \cdot \frac{U_{\mathrm{i}}}{8 L_{\mathrm{o}} f_{\mathrm{s}}}. \tag{5.31}$$

Finally, the output capacitor C_{o} is analysed. A voltage ripple is superimposed to the continuous output voltages of **Fig. 5.7(a)**, due to the PWM operation of the Y-VSI. The maximum occurring voltage ripple value across the filter capacitor C_{o} (single-side amplitude) is

$$\Delta U_{\mathrm{C_o}} = \Delta U_{\mathrm{an}} = \max \left[\frac{U_{\mathrm{i}}}{64 L_{\mathrm{o}} C_{\mathrm{o}} f_{\mathrm{s}}^2}, \frac{\frac{\sqrt{3}}{2} M \hat{I}_{\mathrm{m}}}{8 C_{\mathrm{o}} f_{\mathrm{s}}} \right]. \tag{5.32}$$

A voltage ripple of $\Delta U_{\mathrm{an}} < 2\,\mathrm{V}$ should be achieved, in order to avoid parasitic bearing currents.

The characteristic waveforms, corresponding to DPWM modulation strategy, are summarized in **Tab. 5.2** and are valid for a modulation index $M \geq 4/3$. For this modulation index range, the Y-VSI alternates between buck and boost regime (cf. **Fig. 5.5** and **5.7**). For a low modulation index $M = 0 \ldots 2/\sqrt{3}$ the Y-VSI operates exclusively in buck regime, over the whole fundamental period, hence is equivalent to a simple VSI. The properties of the Y-VSI in the modulation range $M = 0 \ldots 2/\sqrt{3}$ are discussed in **Sec. 5.3**. Finally, for a modulation index $M = 2/\sqrt{3} \ldots 4/3$, the Y-VSI alternates several times between buck and boost regime during the fundamental period. The analytic formulas of **Tab. 5.2** can be used as an approximation in the modulation range $M = 2/\sqrt{3} \ldots 4/3$.

5.1.3 Control System

A complete control system is now conceptualized for the Y-VSI and is illustrated in **Fig. 5.8**. The goal of the control system is to maintain the desired motor speed set-point $\omega = \omega^*$. To this end, a standard cascaded speed-torque

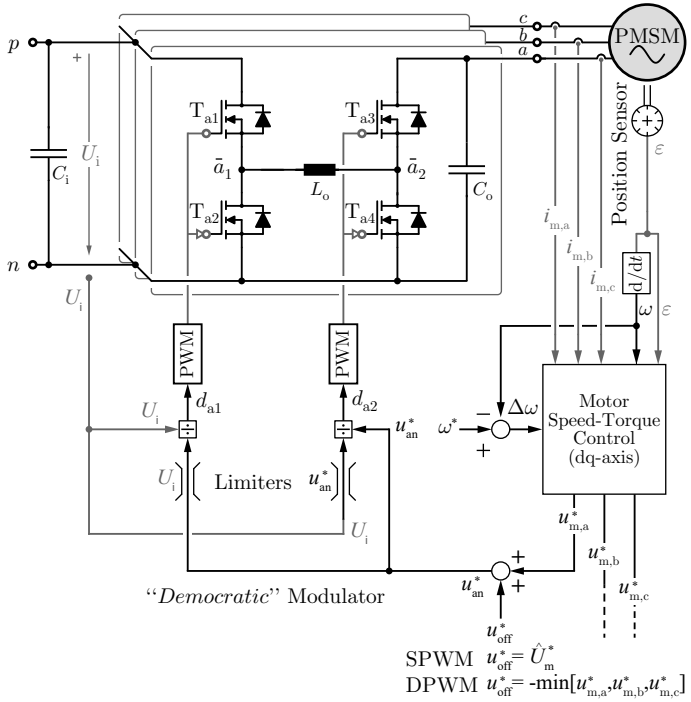


Fig. 5.8: Y-VSI control block diagram. A standard cascaded speed-torque controller is used, in order to maintain the desired motor speed set-point $\omega = \omega^*$. The motor controller outputs the three motor voltage references, e.g. $u^*_{m,a}$, that the Y-VSI must generate. Each phase-module of the Y-VSI is operated independently, hence only phase a is depicted. The modulator translates the inverter output voltage reference u^*_{an} into appropriate duty cycles d_{a1} and d_{a2}.

controller, referenced to the dq-axis frame, is used for the motor. The motor controller receives the speed ω, the position angle ε, and the terminal currents $[i_{\mathrm{m,a}}, i_{\mathrm{m,b}}, i_{\mathrm{m,c}}]$ as input. In return, the motor controller outputs the motor terminal voltage references $[u^*_{\mathrm{m,a}}, u^*_{\mathrm{m,b}}, u^*_{\mathrm{m,c}}]$.

The Y-VSI ensures that the motor voltages $[u_{\mathrm{m,a}}, u_{\mathrm{m,b}}, u_{\mathrm{m,c}}]$ follow the respective sinusoidal references $[u^*_{\mathrm{m,a}}, u^*_{\mathrm{m,b}}, u^*_{\mathrm{m,c}}]$. Each phase-module of the Y-VSI is operated independently, hence the control block diagram is visualized for only phase a in **Fig. 5.8**. An offset voltage u^*_{off} is added to the motor terminal voltage reference $u^*_{\mathrm{m,a}}$, in order to form the strictly positive phase-module output voltage reference u^*_{an}. The added offset depends on the employed modulation strategy In the case of SPWM, the offset is constant and is given by **(5.5)**, while in the case of DPWM the offset is time-varying and is given by **(5.21)**. Finally, the modulator translates the voltage reference u^*_{an} directly into the duty cycles d_{a1} and d_{a2}. The depicted block diagram of the modulator in **Fig. 5.8** is based on the formulas **(5.10)** and **(5.11)**. The modulator follows a "*democratic*" strategy, in the sense that both the buck half-bridge $\bar{a}_1$ and boost half-bridge $\bar{a}_2$ are switched (but not simultaneously) in order to generate the reference voltage u^*_{an}.

The control system presented in **Fig. 5.8** is suitable for motor drive applications with slow dynamic response, such as compressor drives (cf. **Fig. 5.1**). In the case of servo drives, which require fast dynamic response, the inductor L_{o} current must be directly controlled.

5.2 Component Stresses for a High Modulation Index

In this section, the stresses on the different inverter components are analytically derived. The presented results are general and can be used for drive systems (or grid connected inverters) with any specifications. The analytic expressions are applied to a drive system of **Fig. 5.1** and **Tab. 5.1**. For the considered drive application example, the nominal fuel-cell voltage is $U_{\mathrm{i}} = 60\,\mathrm{V}$, while the motor voltage ranges within $\hat{U}_{\mathrm{m}} = 0\,\mathrm{V}...40\,\mathrm{V}$ (phase voltage amplitude). The nominal motor voltage/power operation ($\hat{U}_{\mathrm{m}} = 40\,\mathrm{V}, P = 1\,\mathrm{kW}$), that corresponds to a modulation index of $M = 4/3$, yields the highest component stresses. For the sake of simplicity, a resistive load $R = 3\hat{U}^2_{\mathrm{m,max}}/2P_{\mathrm{max}} = 2.4\,\Omega$ is assumed, which corresponds to a unity power factor, $\cos(\phi) = 1$. Thereby, the transferred power P, fuel-cell current I_{i} and motor fundamental phase current amplitude $\hat{I}_{\mathrm{m}}$ can be derived as a

function of the modulation index

$$P = M^2 \frac{3U_\mathrm{i}^2}{8R},\ I_\mathrm{i} = M^2 \frac{3U_\mathrm{i}}{8R},\ \hat{I}_\mathrm{m} = M \frac{U_\mathrm{i}}{2R}. \tag{5.33}$$

In order to further simplify the analysis, the current ripple of the filter inductor L_o is neglected, unless stated otherwise. Furthermore, the two half-bridges comprising each phase-module (e.g. half-bridges $\bar{a}_1$ and $\bar{a}_2$ for phase-module a) are assumed to be identical.

5.2.1 Sinusoidal Modulation (SPWM)

The component stresses are analytically derived for a modulation index range $M = 1...2$. For this modulation range the Y-VSI generates motor voltage amplitudes $\hat{U}_\mathrm{m}$ greater than the input voltage U_i (buck and boost regime). For a low modulation index $M = 0...1$, the Y-VSI is equivalent to a simple two-level VSI (buck regime) as shown in **Fig. 5.5(a)**. The component stresses for a low modulation index case are derived in **Sec. 5.3.1**.

Semiconductor Voltage Stress

The semiconductors of the buck half-bridges $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are blocking/switching the DC input voltage U_i independent of the employed modulation strategy,

$$U_{\mathrm{T}_1} = U_{\mathrm{T}_2} = U_\mathrm{i}. \tag{5.34}$$

In contrast, the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ are blocking the time-varying inverter output voltages (e.g. voltage $u_\mathrm{an}(\varphi)$ for half-bridge $\bar{a}_2$), which depend on the employed modulation strategy. Therefore, the maximum inverter output voltage value from **Fig. 5.6(a)** defines the voltage stress on the boost half-bridge semiconductor devices,

$$U_{\mathrm{T}_3} = U_{\mathrm{T}_4} = 2\hat{U}_\mathrm{m}. \tag{5.35}$$

Semiconductor Current Stress

The RMS current stress of the semiconductor devices is plotted in **Fig. 5.9** and is analytically approximated by

$$I_{\mathrm{T1,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{-\frac{\sqrt{3}}{\pi^2} M^2 + (1 - \frac{\sqrt{3}}{\pi^2}) M + 1 - \frac{2}{\sqrt{3}}}, \tag{5.36}$$

$$I_{\mathrm{T2,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{+\frac{\sqrt{3}}{\pi^2} M^2 - (1 - \frac{\sqrt{3}}{\pi^2}) M + \frac{2}{\sqrt{3}}}, \tag{5.37}$$

$$I_{\mathrm{T3,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{+\frac{1}{2\pi^2} M^2 - \frac{8}{15} M + \frac{3}{2}}, \tag{5.38}$$

$$I_{\mathrm{T4,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{-\frac{1}{2\pi^2} M^2 + \frac{8}{15} M - \frac{1}{2}}, \tag{5.39}$$

where the RMS current of the inductor $I_{\mathrm{L_o,RMS}}$ is given by **(5.18)**. As shown in **Fig. 5.9**, the current stress on the semiconductor devices is asymmetric and depends on the modulation index M. In the most extreme case example, for the modulation index range $M = 0...1$, the high-side switch T_{a3} conducts the total motor current, while the low-side switch T_{a4} conducts no current. Therefore, the current rating of the semiconductor devices must be carefully selected in order to account for this asymmetric current stress.

Semiconductor Conduction Losses

The conduction losses of the Y-VSI semiconductor devices are

$$P_{\mathrm{cd}} = 6 I^2_{\mathrm{L_o,RMS}} R_{\mathrm{T,on}} \tag{5.40}$$

where $R_{\mathrm{T,on}}$ is the on-state resistance of each (unipolar) power semiconductor device and $I_{\mathrm{L_o,RMS}}$ is the RMS current of the filter inductor L_{o}. It is reminded that, the current ripple is neglected, for the inductor RMS current calculation. Therefore, the conduction losses are calculated for SPWM based on **(5.18)** and **(5.40)**

$$P_{\mathrm{cd}} = 6 \frac{\hat{I}^2_{\mathrm{m}}}{2} \frac{3M^2 - 2M + 3}{4} R_{\mathrm{T,on}}. \tag{5.41}$$

Semiconductor Switching Losses

In a half-bridge, the switching energy dissipation E_{sw}, associated with a hard switching transition, is approximated as a linear function of the commutation current I_{sw} as

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}) = k_0 + k_1 I_{\mathrm{sw}}. \tag{5.42}$$

Accordingly, the switching power dissipation for a switching frequency f_{s} is

$$P_{\mathrm{sw}}(I_{\mathrm{sw}}) = f_{\mathrm{s}} E_{\mathrm{sw}} = f_{\mathrm{s}} \left(k_0 + k_1 I_{\mathrm{sw}}\right). \tag{5.43}$$

The parameters k_0 and k_1 depend on the commutation (switched) voltage U_{sw}. Namely, the parameter k_0 represents the constant part of the switching

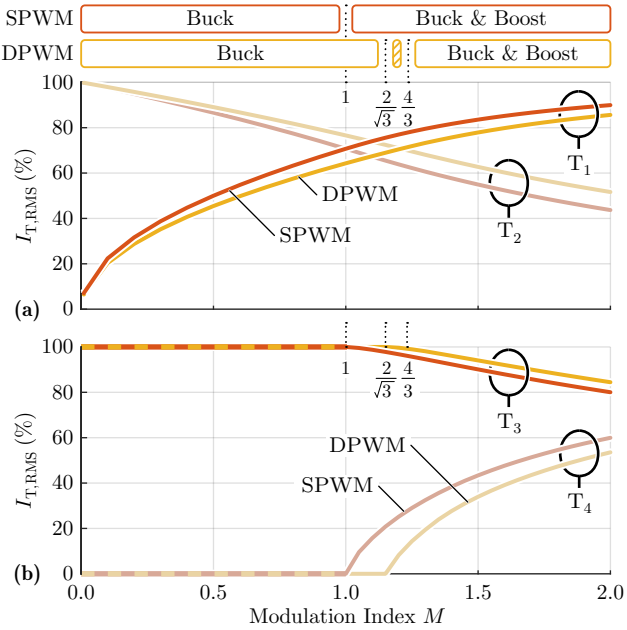


Fig. 5.9: (a) Buck half-bridge high-side T_1 and low-side T_2 switch RMS current stress, normalized with respect to the RMS inductor current $I_{\mathrm{L_o,RMS}}$. **(b)** Boost half-bridge high-side T_3 and low-side T_4 switch RMS current stress, also normalized with respect to $I_{\mathrm{L_o,RMS}}$.

losses and is calculated in literature [110] (assuming unipolar power semiconductors) as

$$k_0(U_{\mathrm{sw}}) = Q_{\mathrm{oss}}(U_{\mathrm{sw}}) \cdot U_{\mathrm{sw}} \tag{5.44}$$

where Q_{oss} is the electric charge stored in the non-linear output parasitic capacitance C_{oss} of the MOSFET

$$Q_{\mathrm{oss}}(U_{\mathrm{sw}}) = \int_0^{U_{\mathrm{sw}}} C_{\mathrm{oss}}(u)\mathrm{d}u. \tag{5.45}$$

Besides the commutation voltage U_{sw}, the parameter k_1 depends on the semiconductor technology and the gate driver configuration [111, 112].

The switching losses of the Y-VSI are now derived, staring from the buck half-bridges. The buck half-bridge $\bar{a}_1$ is switched only during the buck regime of **Fig. 5.6**, i.e. when $u_{\mathrm{an}}(\varphi) \leq U_{\mathrm{i}}$. The commutation voltage of the buck

half-bridge $\bar{a}_1$ is constant and equal to the input voltage $U_{\mathrm{sw},1} = U_{\mathrm{i}}$. The commutation current is equal to the inductor current and hence varies over time $i_{\mathrm{sw},1}(\varphi) = i_{\mathrm{L_o,a}}(\varphi)$. An integration of the local (instantaneous) switching losses of **(5.43)** must be performed over the fundamental period T_{m} in order to derive the total switching losses caused by the buck half-bridges

$$P_{\mathrm{sw},1} = \frac{3f_{\mathrm{s}}}{\pi} \int_{\phi_{\mathrm{o}}}^{\pi} \left[k_0 + k_1 i_{\mathrm{L_o}}(\varphi)\right] \mathrm{d}\varphi. \tag{5.46}$$

The switching parameters k_0 and k_1 are calculated for the constant commutation voltage of $U_{\mathrm{sw},1} = U_{\mathrm{i}}$. The resulting sum of switching losses for the three buck half-bridges, when SPWM modulation is used, is

$$P_{\mathrm{sw},1} = 3f_{\mathrm{s}} \left(k_0 \frac{\pi - \varphi_{\mathrm{o}}}{\pi} + k_1 \frac{2}{\pi} \hat{I}_{\mathrm{m}} (1 - \frac{1}{2} \sin(\varphi_{\mathrm{o}})) \right), \tag{5.47}$$

where the sinus of the transition angle φ_{o} is

$$\sin(\varphi_{\mathrm{o}}) \overset{(5.9)}{=} \frac{2}{M} \sqrt{M-1}. \tag{5.48}$$

Furthermore, the switching parameters k_0 and k_1 of **(5.47)** are calculated for the constant commutation voltage of the buck half-bridges $U_{\mathrm{sw},1} = U_{\mathrm{i}}$.

The boost half-bridge $\bar{a}_2$ is switched only during the boost regime of **Fig. 5.6**, i.e. when $u_{\mathrm{an}}(\varphi) > U_{\mathrm{i}}$. The commutation voltage of the boost half-bridge $\bar{a}_2$ is equal to the inverter output voltage and hence varies over time $u_{\mathrm{sw},2}(\varphi) = u_{\mathrm{an}}(\varphi)$. The commutation current is equal to the inductor current $i_{\mathrm{sw},2}(\varphi) = i_{\mathrm{L_o,a}}(\varphi)$ and is also time-varying. An integration of the local switching losses of **(5.43)** must be performed over the fundamental period T_{m} in order to derive the total switching losses caused by the boost half-bridges

$$P_{\mathrm{sw},2} = \frac{3f_{\mathrm{s}}}{\pi} \int_{0}^{\phi_{\mathrm{o}}} \left[k_0(\varphi) + k_1(\varphi) i_{\mathrm{L_o}}(\varphi)\right] \mathrm{d}\varphi, \tag{5.49}$$

where the switching parameters $k_0(\varphi)$ and $k_1(\varphi)$ are varying over time and depend on the instantaneous commutation voltage $u_{\mathrm{sw},2}(\varphi)$. The resulting sum of switching losses for the three boost half-bridges, when SPWM modulation is used, is approximated by

$$P_{\mathrm{sw},2} = 3f_{\mathrm{s}}(k_0 + k_1 M \hat{I}_{\mathrm{m}}) \frac{\sin(\varphi_{\mathrm{o}})}{\pi}, \tag{5.50}$$

where $\sin(\varphi_{\mathrm{o}})$ is given in **(5.48)**. The switching parameters k_0 and k_1 of **(5.50)** are calculated for the highest commutation voltage of the boost half-bridges

$U_{\mathrm{sw},2} = u_{\mathrm{an}}(0) = 2\hat{U}_{\mathrm{m}}$. The total switching losses of the Y-VSI are the sum of the perspective buck half-bridges' and boost half-bridges' switching losses

$$P_{\mathrm{sw}} = P_{\mathrm{sw},1} + P_{\mathrm{sw},2}. \tag{5.51}$$

Passive Components Selection

The integrated output filter ($L_{\mathrm{o}} - C_{\mathrm{o}}$) of the Y-VSI is now analysed in detail, starting from the filter inductors L_{o}. The current of the filter inductor is non-sinusoidal, as is described by **(5.15)** and shown in **Fig. 5.6(d)**. The maximum current stress on the inductor depends on the modulation index M, is given in **(5.16)** and is plotted in **Fig. 5.10(a)**. The peak current ripple of the filter inductor is given by **(5.19)**. Accordingly, in order to limit this current ripple to a maximum value of $\Delta I_{\mathrm{L_o}}$, the inductance value must be selected as

$$L_{\mathrm{o}} \geq \max\left[1, 4\frac{M-1}{M}\right] \cdot \frac{U_{\mathrm{i}}}{8\Delta I_{\mathrm{L_o}} f_{\mathrm{s}}}, \tag{5.52}$$

where $M = M_{\mathrm{max}}$ is the highest possible modulation index within the inverter operating range. In general, there is a direct relation between the inductor losses and the RMS inductor current ripple $\Delta I_{\mathrm{L_o,RMS}}$, as a high RMS current ripple results in a high frequency RMS flux density and hence substantial core losses [85]. In addition, a high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple $\Delta I_{\mathrm{L_o,RMS}}$ is a reasonable performance indicator for the design of the inductive components and is calculated in the following. The local (instantaneous) RMS current ripple of the filter inductor is

$$\Delta i_{\mathrm{L_o,a,RMS}}(\varphi) = \begin{cases} 4m_{\mathrm{a}}(1-m_{\mathrm{a}})\dfrac{U_{\mathrm{i}}}{8\sqrt{3}L_{\mathrm{o}}f_{\mathrm{s}}}, & 0 < \varphi \leq \varphi_{\mathrm{o}} \\ 4\dfrac{m_{\mathrm{a}}-1}{m_{\mathrm{a}}}\dfrac{U_{\mathrm{i}}}{8\sqrt{3}L_{\mathrm{o}}f_{\mathrm{s}}}, & \varphi_{\mathrm{o}} < \varphi \leq \pi \end{cases}, \tag{5.53}$$

where $m_{\mathrm{a}}(\varphi)$ is the modulation factor and is given in **(5.8)**. The relation between the local RMS current ripple of the inductor $\Delta i_{\mathrm{L_o,a,RMS}}$ and the modulation factor m_{a} is visualized in **Fig. 5.11**. In order to calculate the global (total) RMS current ripple, an integration of the local RMS current ripple **(5.53)** over the fundamental period T_{m} is performed. The global RMS current ripple is calculated numerically and is plotted in **Fig. 5.10(b)**. Finally, the filter capacitors C_{o} are selected. The peak voltage ripple across the filter capacitor

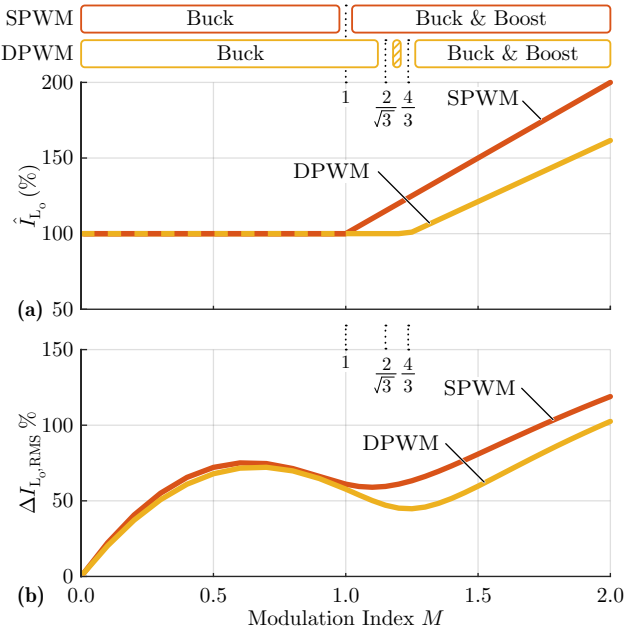


Fig. 5.10: Filter inductor L_o current stress, calculated for SPWM and DPWM modulation strategies. **(a)** Maximum inductor current, normalized with respect to the motor current amplitude $\hat{I_m}$ and **(b)** inductor RMS current ripple, normalized with respect to the value $\frac{U_i}{8\sqrt{3}L_o f_s}$.

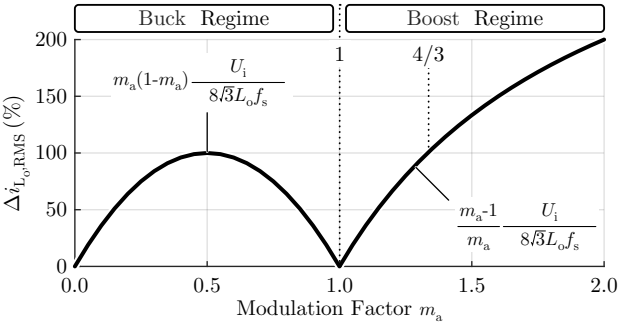


Fig. 5.11: Local (instantaneous) RMS current of the filter inductor L_o, normalized with respect to $\frac{U_i}{8\sqrt{3}L_o f_s}$. The local RMS current ripple depends on the modulation factor $m_a(\varphi) = u_{an}(\varphi)/U_i$ of **(5.8)**.

is given in **(5.20)**. Accordingly, in order to limit this voltage ripple (single-side amplitude) to a maximum value of ΔU_{C_o}, the capacitance value must be selected as

$$C_o \geq \max\left[\frac{U_i}{64 L_o \Delta U_{C_o} f_s^2}, \frac{M\hat{I}_m}{8\Delta U_{C_o} f_s}\right]. \tag{5.54}$$

A voltage ripple of $\Delta U_{C_o} = \Delta U_{an} < 2\,\mathrm{V}$ should be selected, for a safe motor operation. Finally, an *RC* damping circuit is placed in parallel to the filter capacitor C_o, in order to avoid unwanted resonances of the output filter [134].

5.2.2 Discontinuous Modulation (DPWM)

The component stresses are analytically derived for a modulation index range $M = 4/3...2$. For this modulation range the Y-VSI generates motor voltage amplitudes $\hat{U}_m$ greater than the input voltage U_i (buck and boost regime). For a low modulation index $M = 0...2/\sqrt{3}$, the Y-VSI is equivalent to a simple two-level VSI (buck regime) as shown in **Fig. 5.5(a)**. The component stresses for a low modulation index case are derived in **Sec. 5.3.2**.

Semiconductor Voltage Stress

The semiconductors of the buck half-bridges $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are blocking/switching the DC input voltage U_i independent of the employed modulation strategy

$$U_{T_1} = U_{T_2} = U_i. \tag{5.55}$$

In contrast, the boost half-bridges $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ are blocking the time-varying inverter output voltages (e.g. $u_{an}(\varphi)$ for half-bridge $\bar{a}_2$), which depend on the employed modulation strategy. Therefore, the maximum inverter output voltage value from **Fig. 5.7(a)** defines the voltage stress on the boost half-bridge semiconductor devices

$$U_{T_3} = U_{T_4} = \sqrt{3}\hat{U}_m. \tag{5.56}$$

Semiconductor Current Stress

The RMS current stress on the semiconductor devices is plotted in **Fig. 5.9** and is analytically approximated by

$$I_{T_1,RMS} = I_{L_o,RMS}\sqrt{-\frac{\sqrt{3}}{4\pi}M^2 + \frac{5}{7}M - \frac{1}{6}}, \tag{5.57}$$

$$I_{\mathrm{T2,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{+\frac{\sqrt{3}}{4\pi} M^2 - \frac{5}{7} M + \frac{7}{6}}, \tag{5.58}$$

$$I_{\mathrm{T3,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{+\frac{1}{4\pi} M^2 - \frac{\sqrt{3}}{\sqrt{8}} M + 1 + \frac{2}{\pi}}, \tag{5.59}$$

$$I_{\mathrm{T4,RMS}} = I_{\mathrm{L_o,RMS}} \sqrt{-\frac{1}{4\pi} M^2 + \frac{\sqrt{3}}{\sqrt{8}} M - \frac{2}{\pi}}, \tag{5.60}$$

where the RMS current of the inductor $I_{\mathrm{L_o,RMS}}$ is given by **(5.30)**. As shown in **Fig. 5.9**, the current stress on the semiconductor devices is asymmetric and depends on the modulation index M. In the most extreme case example, for the modulation index range $M = 0...2/\sqrt{3}$, the high-side switch T_{a3} conducts the total motor current, while the low-side switch T_{a4} conducts no current. Therefore, the current rating of the semiconductor devices must be carefully selected in order to account for this asymmetric current stress.

Semiconductor Conduction Losses

The conduction losses of the Y-VSI semiconductor devices are described by **(5.40)** and are proportional to the square of the inductor RMS current $I_{\mathrm{L_o,RMS}}$. By using the expression **(5.30)** for the RMS inductor current, the conduction losses are calculated for DPWM

$$P_{\mathrm{cd}} = 6 \frac{\hat{I}_{\mathrm{m}}^2}{2} \frac{9M^2 - 4\sqrt{3}M + 12}{16} R_{\mathrm{T,on}}. \tag{5.61}$$

Semiconductor Switching Losses

First, the switching losses of the buck half-bridges are calculated. The buck half-bridge $\bar{a}_1$ is switched during the buck regime of **Fig. 5.7**, i.e. when $u_{\mathrm{an}}(\varphi) \leq U_{\mathrm{i}}$. Thanks to DPWM, the switching transition of the buck half-bridge $\bar{a}_1$ during the buck regime are reduced compared to SPWM. More precisely, no switching transitions occur during the denoted clamping region of **Fig. 5.7**. The commutation voltage of the buck half-bridge $\bar{a}_1$ is constant and equal to the input voltage $U_{\mathrm{sw,1}} = U_{\mathrm{i}}$. The commutation current is equal to the inductor current and hence varies over time $i_{\mathrm{sw,1}}(\varphi) = i_{\mathrm{L_o,a}}(\varphi)$. An integration of the local switching losses according to **(5.46)** is performed in order to derive the total switching losses caused by the buck half-bridges. The resulting sum of switching losses for the three buck half-bridges, when

DPWM modulation is used, is

$$P_{\mathrm{sw},1} = 3f_{\mathrm{s}}\left(k_0\frac{\frac{2\pi}{3}-\varphi_{\mathrm{o}}}{\pi}+k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}\left(\frac{4-\sqrt{3}}{4}-\frac{1}{2}\sin(\varphi_{\mathrm{o}})\right)\right), \tag{5.62}$$

where the sinus of the transition angle φ_{o} is

$$\sin(\varphi_{\mathrm{o}}) \overset{(5.24)}{=} \frac{3\sqrt{3M^2-4}+2\sqrt{3}}{6M}. \tag{5.63}$$

The switching parameters k_0 and k_1 of **(5.62)** are calculated for the constant commutation voltage of the buck half-bridges $U_{\mathrm{sw},1} = U_{\mathrm{i}}$.

Subsequently, the switching losses of the boost half-bridges are calculated. The boost half-bridge $\bar{a}_2$ is switched only during the boost regime of **Fig. 5.7**, i.e. when $u_{\mathrm{an}}(\varphi) > U_{\mathrm{i}}$. The commutation voltage of the boost half-bridge $\bar{a}_2$ is equal to the inverter output voltage and hence varies over time $u_{\mathrm{sw},2}(\varphi) = u_{\mathrm{an}}(\varphi)$. The commutation current is equal to the inductor current $i_{\mathrm{sw},2}(\varphi) = i_{\mathrm{L_o,a}}(\varphi)$ and is also time-varying. An integration of the local switching losses according to **(5.49)** is performed in order to derive the total switching losses caused by the boost half-bridges. The resulting sum of switching losses for the three boost half-bridges, when DPWM modulation is used, is approximated by

$$P_{\mathrm{sw},2} = 3f_{\mathrm{s}}\left(k_0+k_1\frac{M\sqrt{3}}{2}\hat{I}_{\mathrm{m}}\right)\frac{\sin(\varphi_{\mathrm{o}})}{\pi}, \tag{5.64}$$

where $\sin(\varphi_{\mathrm{o}})$ is given in **(5.63)**. The switching parameters k_0 and k_1 of **(5.64)** are calculated for the highest commutation voltage of the boost half-bridges $U_{\mathrm{sw},2} = u_{\mathrm{an}}(\frac{\pi}{6}) = \sqrt{3}\hat{U}_{\mathrm{m}}$. The total switching losses of the Y-VSI are the sum of the respective buck half-bridges' and boost half-bridges' switching losses **(5.51)**. According to DPWM, the phase with the most negative motor voltage is clamped to the negative DC rail n, for one third of the fundamental period $T_{\mathrm{m}}/3$ (cf. **Fig. 5.7**). Thereby, it is possible to reduce the total number of switching transitions of the Y-VSI by 33% compared to SPWM. Accordingly, a significant reduction of the switching losses is achieved thanks to DPWM.

Passive Component Selection

The integrated output filter ($L_{\mathrm{o}} - C_{\mathrm{o}}$) of the Y-VSI is now analysed. It is assumed that a Y-VSI inverter, designed for SPWM modulation, pre-exists. In this case, the filter inductors L_{o} and the filter capacitors C_{o} are selected

based on **(5.52)** and **(5.54)**, respectively. The current of the filter inductor is non-sinusoidal, as described by **(5.27)** and shown in **Fig. 5.7(d)**. The maximum current of the inductor depends on the modulation index M, is given in **(5.29)** and is plotted in **Fig. 5.10(a)**. The DPWM results in a lower maximum current and hence a lower stress on the inductor, compared to SPWM. Subsequently, the RMS current ripple of the inductor $\Delta I_{\mathrm{L_o,RMS}}$, which is directly related to the inductor losses, is calculated. In order to calculate the global (total) RMS current ripple, an integration of the local RMS current ripple **(5.53)** over the fundamental period T_m is performed. The global RMS current ripple is calculated numerically and is plotted in **Fig. 5.10(b)**. It is deduced that DPWM causes less current ripple stress on the filter inductor compared to SPWM.

5.2.3 Remaining Component Stresses

The capacitor C_i conducts the switched input current $i_\mathrm{i}(t)$ of the Y-VSI. The worst case current, flowing through the input capacitor over a switching period T_s is $i_\mathrm{i}(t) = \frac{1}{2}\hat{I}_\mathrm{o}\mathrm{rec}(2\pi f_\mathrm{s} t)$. The input capacitor current is in this case rectangular, with 50% duty cycle and has an amplitude of $\hat{I}_\mathrm{o}/2$. Accordingly, a high (local) RMS current stress on the input capacitor $I_{C_\mathrm{i},\mathrm{RMS}} = \hat{I}_\mathrm{o}/2$ results. Based on the rectangular current waveform $i_\mathrm{i}(t) = \frac{1}{2}\hat{I}_\mathrm{o}\mathrm{rec}(2\pi f_\mathrm{s} t)$, the worst case voltage ripple (single-side amplitude) across the input capacitor C_i and/or the fuel-cell is

$$\Delta U_\mathrm{i} = \frac{\hat{I}_\mathrm{m}}{8 f_\mathrm{s} C_\mathrm{i}}. \tag{5.65}$$

Therefore, in order to limit the input voltage ripple to a sufficiently low value ΔU_i the input capacitance must be

$$C_\mathrm{i} \geq \frac{\hat{I}_\mathrm{m}}{8 f_\mathrm{s} \Delta U_\mathrm{i}}. \tag{5.66}$$

The resulting input capacitance value C_i is inversely proportional to the switching frequency f_s and is typically small. It is noted here, that there is no need for low-frequency energy storage in the input capacitor C_i, for a balanced three-phase system. In summary, the input capacitor must conduct a high-frequency switched current with a high RMS value $I_{C_\mathrm{i},\mathrm{RMS}}$, while a low capacitance C_i is typically required. Therefore, ceramic or film capacitors are suggested for the C_i realization.

5.3 Component Stresses for a Low Modulation Index

5.3.1 Sinusoidal Modulation (SPWM)

For the sake of completeness, the component stresses of the Y-VSI are derived for a low modulation index $M = 0...1$. For SPWM within this modulation index range, the Y-VSI continuously operates in buck regime, according to **Fig. 5.5(a)**. There, the boost half-bridges (e.g. $\bar{a}_2$) are clamped, while only the buck half-bridges (e.g. $\bar{a}_1$) are switched. In this case, the Y-VSI is equivalent to a simple two-level VSI. The RMS current stress on the semiconductor devices is

$$\begin{aligned} I_{\mathrm{T1,RMS}} &= \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{\frac{M}{2}}, \quad & I_{\mathrm{T2,RMS}} &= \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{1-\frac{M}{2}}, \\ I_{\mathrm{T3,RMS}} &= \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}, & I_{\mathrm{T4,RMS}} &= 0, \end{aligned} \tag{5.67}$$

and is plotted in **Fig. 5.9**.

The conduction losses of the Y-VSI semiconductor devices are described by **(5.40)** and are proportional to the square of the inductor RMS current $I_{\mathrm{L_o,RMS}}$. For the examined modulation range $M = 0...1$, the filter inductor current is equal to the motor current, hence

$$I_{\mathrm{L_o,RMS}} = \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}. \tag{5.68}$$

The resulting conduction losses are

$$P_{\mathrm{cd}} = 6\frac{\hat{I}_{\mathrm{m}}^2}{2}R_{\mathrm{T,on}}. \tag{5.69}$$

The switching losses are subsequently analysed. The boost half-bridges are clamped, hence exhibit no switching losses, i.e. $P_{\mathrm{sw,2}} = 0$. Therefore, only the buck half-bridges contribute to the switching losses. The equation **(5.46)** is used in order to derive the total switching losses caused by the buck half-bridges

$$P_{\mathrm{sw}} = P_{\mathrm{sw,1}} = 3f_{\mathrm{s}}(k_0 + k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}), \tag{5.70}$$

where the switching parameters k_0 and k_1 are calculated for the constant commutation voltage of $U_{\mathrm{sw,1}} = U_{\mathrm{i}}$.

5.3.2 Discontinuous Modulation (DPWM)

The component stresses of the Y-VSI are derived for DPWM and a low modulation index $M = 0...2/\sqrt{3}$. For DPWM within this modulation index range, the Y-VSI continuously operates in buck regime, according to **Fig. 5.5(a)**. The RMS current stress on the semiconductor devices is

$$\begin{aligned} I_{\mathrm{T1,RMS}} &= \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{\frac{3\sqrt{3}M}{4\pi}} & I_{\mathrm{T2,RMS}} &= \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{1-\frac{3\sqrt{3}M}{4\pi}} \\ I_{\mathrm{T3,RMS}} &= \frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}} & I_{\mathrm{T4,RMS}} &= 0 \end{aligned} . \tag{5.71}$$

The conduction losses of DPWM are the same as in the case of SPWM **(5.69)**. The switching losses are subsequently analysed. Similarly to SPWM, the boost half-bridges are clamped, therefore exhibit no switching losses, i.e. $P_{\mathrm{sw,2}} = 0$. Only the buck half-bridges contribute to the switching losses. The equation **(5.46)** is used in order to derive the total switching losses caused by the buck half-bridges

$$P_{\mathrm{sw}} = P_{\mathrm{sw,1}} = 3f_{\mathrm{s}}\left(\frac{2}{3}k_0 + \left(1-\frac{\sqrt{3}}{4}\right)k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}\right), \tag{5.72}$$

where the switching parameters k_0 and k_1 are calculated for the constant commutation voltage of $U_{\mathrm{sw,1}} = U_{\mathrm{i}}$.

5.4 Experimental Validation

The proposed Y-VSI inverter concept is tested within the fuel-cell application of **Fig. 5.1** and **Tab. 5.1**. A 10 kW fuel-cell unit requires a continuous supply of oxygen, which is provided by a 280 krpm high-speed electric compressor [53]. A motor drive system, directly supplied by the fuel-cell controls the electric compressor. The compressor drive system uses 10% of the fuel-cell power, i.e. 1 kW.

5.4.1 Design Procedure

The previously derived component stresses in **Sec. 5.2** depend on the switching frequency f_{s}, however the switching frequency is till now not explicitly defined. The switching frequency f_{s} represents a crucial design trade-off. A high switching frequency allows to reduce the volume of the passive filter

components, but at the same time increases the semiconductor switching losses and accordingly requires a larger semiconductor heatsink volume. In order to select an appropriate switching frequency, a multi-objective optimization routine, with respect to inverter efficiency η and power density ρ, is employed [15, 83, 139], which assesses the performance of several Y-VSI inverter designs. The optimization routine includes the 200 V rated GaN semiconductor devices (EPC 2034 MOSFETs [112]), the semiconductor heatsinks [87], the inductive components L_o, [84, 85] and the ceramic capacitors C_o, C_i.

Based on the optimization results, a switching frequency of $f_s = 300\,\text{kHz}$ is selected for the Y-VSI. The boxed volume of the integrated AC filter (L_o and C_o) is $36.4\,\text{cm}^3$. Subsequently, the number of parallel semiconductor devices per switch ($T_{a1} - T_{a4}$ of **Fig. 5.3**) is selected. A low number of parallel devices yields low (capacitive) switching losses, but high conduction losses. On the contrary, a high number of parallel devices results in high switching losses but low conduction losses. The number of parallel devices is determined by the minimum of the overall semiconductor losses (i.e. sum of conduction and switching losses). In the case at hand, two parallel devices per switch are optimal. A breakdown of the semiconductor losses into conduction and switching losses is depicted in **Fig. 5.12**. As expected, DPWM modulation yields lower semiconductor losses (-33.2%) compared to SPMW modulation, mainly thanks to the reduced number of switching transitions. The Y-VSI component parameters are given in **Tab. 5.4**.

Using the analytic formulas derived in **Sec. 5.2**, the inverter component stresses are calculated and summarized in **Tab. 5.3**. There, the SPWM and DPWM modulation strategies are compared. The **Tab. 5.3** serves as a general design guideline and can be extended for motor drive systems with different specifications. After the designer selects an appropriate switching frequency f_s, based on the available semiconductor technology, **Tab. 5.3** can be easily used in order to design a Y-VSI inverter.

For the sake of completeness, a conventional B-VSI (cf. **Fig. 5.2**) is designed for the specifications of **Tab. 5.1**. The detailed design process of a B-VSI can be found in **Chapter 4**. The selected B-VSI benchmark design, features the same switching frequency of $f_s = 300\,\text{kHz}$, for both the DC/DC stage as well as the DC/AC stage. The boxed volume of the DC/DC stage filter (L_i, C_i and C_{DC}) is $10.7\,\text{cm}^3$, while the boxed volume of the DC/AC stage filter (L_o and C_o) is $32\,\text{cm}^3$. Therefore, the total filter volume of the B-VSI is $42.7\,\text{cm}^3$. Note that the filter volume of the B-VSI ($42.7\,\text{cm}^3$) is higher than the respective volume for the Y-VSI ($36.4\,\text{cm}^3$), due to the higher number of four inductors. In addition, the same 200 V rated GaN devices are used, as in

Tab. 5.3: Component stresses summary for a Y-VSI employing SPWM or DPWM modulation strategy. The numeric values are calculated for the motor drive of **Tab. 5.1**, and for the nominal operating condition, i.e. modulation index $M = 4/3$.

		SPWM		**DPWM**
T_1, T_2 voltage PK	**(5.34)**	$U_{T1} = U_{T2} = 40\,\text{V}$	**(5.55)**	$U_{T1} = U_{T2} = 40\,\text{V}$
T_3, T_4 voltage PK	**(5.35)**	$U_{T3} = U_{T4} = 80\,\text{V}$	**(5.56)**	$U_{T3} = U_{T4} = 69.3\,\text{V}$
T_1 current RMS	**(5.36)**	$I_{T1,\text{RMS}} = 11.2\,\text{A}$	**(5.57)**	$I_{T1,\text{RMS}} = 10.4\,\text{A}$
T_2 current RMS	**(5.37)**	$I_{T2,\text{RMS}} = 8.5\,\text{A}$	**(5.58)**	$I_{T2,\text{RMS}} = 9.7\,\text{A}$
T_3 current RMS	**(5.38)**	$I_{T3,\text{RMS}} = 13.2\,\text{A}$	**(5.59)**	$I_{T3,\text{RMS}} = 14.0\,\text{A}$
T_4 current RMS	**(5.39)**	$I_{T4,\text{RMS}} = 4.9\,\text{A}$	**(5.60)**	$I_{T4,\text{RMS}} = 2.8\,\text{A}$
Conduction losses total	**(5.41)**	$P_{\text{cd}} = 11.8\,\text{W}$ $R_{T,\text{on}} = 20\,\text{m}\Omega$, for 100 °C	**(5.61)**	$P_{\text{cd}} = 9.8\,\text{W}$ $R_{T,\text{on}} = 20\,\text{m}\Omega$, for 100 °C
Switching losses buck	**(5.47)**	$P_{\text{sw},1} = 7.7\,\text{W}$ $^*k_0 = 6.77\,\mu\text{J}$, $k_1 = 0.68\,\mu\text{J/A}$, for U_{T1}	**(5.62)**	$P_{\text{sw},1} = 2.9\,\text{W}$ $^*k_0 = 6.77\,\mu\text{J}$, $k_1 = 0.68\,\mu\text{J/A}$, for U_{T1}
Switching losses boost	**(5.50)**	$P_{\text{sw},2} = 8.7\,\text{W}$ $^*k_0 = 10.91\,\mu\text{J}$, $k_1 = 1.09\,\mu\text{J/A}$, for U_{T3}	**(5.64)**	$P_{\text{sw},2} = 6.2\,\text{W}$ $^*k_0 = 8.58\,\mu\text{J}$, $k_1 = 0.86\,\mu\text{J/A}$, for U_{T3}
Losses total		$P_{\text{cd}} + P_{\text{sw},1} + P_{\text{sw},2} = 28.3\,\text{W}$		$P_{\text{cd}} + P_{\text{sw},1} + P_{\text{sw},2} = 18.9\,\text{W}$
Efficiency reduction		$\Delta\eta = -2.8\%$		$\Delta\eta = -1.9\%$
Filter inductor	**(5.52)**	$L_o = 5\,\mu\text{H}$	**(5.52)**	$L_o = 5\,\mu\text{H}$
Current ripple PK		$\Delta I_{L_o} = 3.6\,\text{A}$		$\Delta I_{L_o} = 3.6\,\text{A}$
Current PK	**(5.16)**	$\hat{I}_{L_o} = 22.2\,\text{A}$	**(5.29)**	$\hat{I}_{L_o} = 19.3\,\text{A}$
Current RMS	**(5.18)**	$I_{L_o,\text{RMS}} = 13.3\,\text{A}$	**(5.30)**	$I_{L_o,\text{RMS}} = 12.8\,\text{A}$
Filter capacitor	**(5.54)**	$C_o = 2\,\mu\text{F}$	**(5.54)**	$C_o = 2\,\mu\text{F}$
Voltage ripple PK		$\Delta U_{C_o} = 0.7\,\text{V}$		$\Delta U_{C_o} = 0.7\,\text{V}$

*Switching parameters k_0 and k_1 are calculated based on [112].

the case of the Y-VSI. In particular, two parallel devices per switch are used for the DC/DC stage and one device per switch is used in the DC/AC stage. The semiconductor losses of the conventional B-VSI (cf. **Chapter 4**), are depicted in **Fig. 5.12**. The selected number of parallel devices yields the lowest overall semiconductor losses. Note in **Fig. 5.12(a)** that the DC/AC stage switching losses (15.5 W) are higher than the DC/AC stage conduction losses (8.3 W). Therefore, using two instead of one parallel device per switch for the DC/AC stage would further increase the switching losses. The increase in the switching losses would outweigh the decrease in the conduction losses, thereby resulting in higher overall semiconductor losses. Thus, one device per switch is optimal. The B-VSI component parameters are summarized in **Tab. 5.5**.

Fig. 5.12(a) reveals that the Y-VSI employing SPWM generates 20.1% less semiconductor losses, compared to the B-VSI employing SPWM, for the same switching frequency of $f_s = 300\,\text{kHz}$. The superior performance of the Y-VSI can be explained as follows. The B-VSI features two energy conversion stages. In the case of SPWM, one half-bridge is switched at the DC/DC stage and three half-bridges are switched at the DC/AC stage. Therefore, in total four half-bridges are switched. In addition, all the half-bridges switch the high DC link voltage $U_{DC} = 80\,\text{V}$. The Y-VSI processes the transmitted power $P = 1\,\text{kW}$ in a completely different way. When SPWM is employed, only one half-bridge per phase-module is switched, at any given point in time (cf. **Fig. 5.6**). Therefore, a Y-VSI requires the switching of only three half-bridges in total, at any given point in time. Furthermore, the buck half-bridge $\bar{a}_1$ of the Y-VSI switches the low input voltage $U_i = 60\,\text{V}$, while the boost half-bridge $\bar{a}_2$ switches the time-varying output voltage $u_{an}(t) \leq 80\,\text{V}$ **(5.6)**. Note that both these voltages are lower than the high DC link voltage $U_{DC} = 80\,\text{V}$ of a B-VSI. For the above reasons the Y-VSI benefits from low semiconductor losses. It is noted, that the semiconductor losses reduction achieved by means of the Y-VSI, simultaneously enables a low semiconductor heatsink volume [87].

A similar analysis is performed for DPWM modulation in **Fig. 5.12(b)**. There, the Y-VSI generates 35.3% less semiconductor losses than the B-VSI, which can be explained as follows. According to DPWM, only two half-bridges of the Y-VSI are switched at any given point in time (cf. **Fig. 5.7**). Contrary, three half-bridges in total (one half-bridge of the DC/DC stage and two half-bridges of the DC/AC stage) are switched, in the case of the B-VSI. Therefore, the B-VSI generates considerably higher semiconductor losses than the Y-VSI.

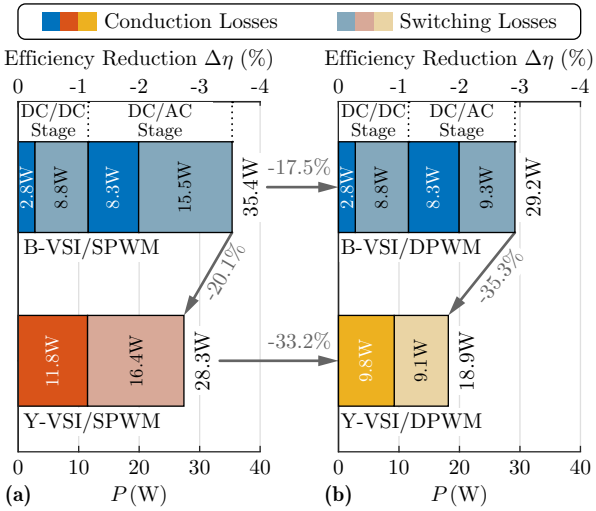


Fig. 5.12: Breakdown of the semiconductor losses of the Y-VSI and the B-VSI (cf. **Chapter 4**) into conduction and switching losses, for **(a)** SPWM and **(b)** DPWM. The numeric values are calculated for the nominal specifications of **Tab. 5.1**, i.e. modulation index $M = 4/3$.

5.4.2 Experimental Results

Two inverter hardware prototypes are purposely assembled:

(i) Y-VSI of **Fig. 5.3**. The hardware prototype is shown in **Fig. 5.13** and the respective component parameters are given in **Tab. 5.4**. Experimentally measured waveforms for SPWM are shown in **Fig. 5.14(a)**, where the three output voltages of the inverter are offseted sinusoids. Experimentally measured waveforms for DPWM are shown in **Fig. 5.14(b)**. There, the three output voltages of the inverter are non-sinusoidal, however, the load line-to-line voltages are sinusoidal.

(ii) B-VSI of **Fig. 5.2**. The hardware prototype is depicted in **Fig. 5.15**, while the component parameters are summarized in **Tab. 5.5**. Experimentally measured waveforms are shown in **Fig. 5.16** for SPWM modulation. This hardware prototype serves as the state-of-the-art solution against which the Y-VSI hardware prototype is compared to.

In order to enable a meaningful comparison, both the above hardware demonstrators feature the same switching frequency of $f_s = 300\,\text{kHz}$. It is noted,

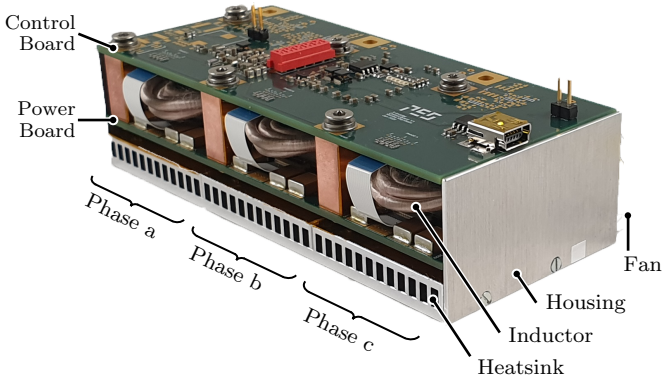


Fig. 5.13: Y-VSI hardware prototype (113 mm × 49 mm × 30 mm) achieving a power density of 6.6 kW/dm^3 (108 W/in^3).

Tab. 5.4: Parameter values of the Y-VSI hardware prototype, corresponding to the schematic diagram notation of **Fig. 5.3**.

Y-VSI	
Switching frequency f_s	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_o	5 µH
Capacitance C_o	2 µF
Capacitance C_i	10 µF

that during the experimental measurements the compressor is replaced by an equivalent resistive load $R = 2\,\Omega$. The resistive load significantly simplifies the test setup, but does not affect the operation or the performance of the inverter prototypes.

First, the performance of the two hardware prototypes is experimentally compared. The conventional B-VSI hardware prototype achieves a power density of $\rho = 6\,\mathrm{kW/dm^3}$ (including case, cooling system and control electronics). The Y-VSI hardware prototype achieves a power density of $\rho = 6.6\,\mathrm{kW/dm^3}$, which is $\Delta\rho = +10\%$ higher compared to the B-VSI. The Y-VSI benefits from a lower number of inductive components (three) compared to the B-VSI (four). This is the main reason behind the higher Y-VSI power density.

At $P = 1\,\mathrm{kW}$ nominal operation, the B-VSI achieves a low efficiency of $\eta = 96\%$ (i.e. 40 W of losses), for sinusoidal modulation strategy (SPWM). The majority of the losses originate from the semiconductor devices (i.e. 35.4 W calculated in **Fig. 5.12(a)**). As discussed in **Sec. 5.4.1**, there are two main reasons behind the B-VSI low efficiency. The B-VSI is a two-stage converter, as a result four half-bridges are switched at any given point in time (for SPWM). Furthermore, all the semiconductor devices process/switch the high DC link voltage $U_{\mathrm{DC}} = 80\,\mathrm{V}$.

By employing the SPWM of **Fig. 5.6**, the Y-VSI achieves a nominal efficiency of $\eta = 97.2\%$ (i.e. 28 W of losses), which is $\Delta\eta = +1.2\%$ more efficient compared to the B-VSI (also employing SPWM). The Y-VSI delivers power to the motor more efficiently than the B-VSI, as discussed in **Sec. 5.4.1**. That is, at any moment in time, only three out of the six half-bridges of the Y-VSI are operated with the switching frequency f_{s}, while the remaining three half-bridges are clamped. By employing the discontinuous modulation strategy (DPWM) of **Fig. 5.7**, the Y-VSI achieves an even higher efficiency of $\eta = 98.3\%$ (i.e. 17 W of losses). The Y-VSI is in this case $\Delta\eta = +2.3\%$ more efficient than the B-VSI, employing SPWM. The DPWM further reduces the number of switching transitions, thus adds to the previously described advantages of the Y-VSI. At each point in time, only two out of the six half-bridges are operated with the switching frequency f_{s}, while the remaining four half-bridges are clamped. The efficiency curves of the two inverter prototypes are plotted in **Fig. 5.17**.

Finally, the motor voltage quality is assessed. The voltage ripple Δu_{an} at the load terminal a is measured in **Fig. 5.16**, for the case of the B-VSI employing SPWM. The voltage ripple Δu_{an} is the result of the PWM operation of the half-bridge $\bar{a}$. In particular, the switch-node $\bar{a}$ two-level PWM voltage

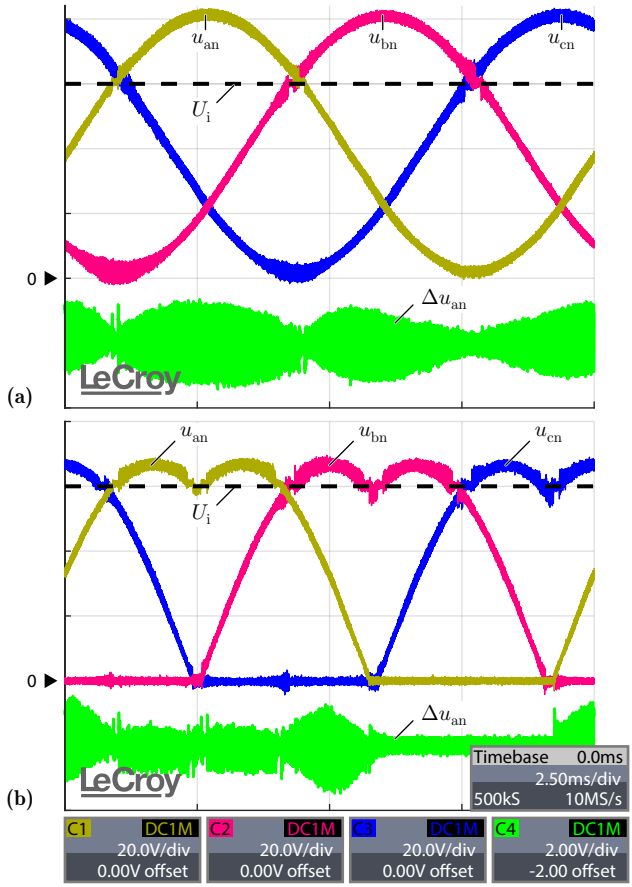


Fig. 5.14: Experimentally measured waveforms for the Y-VSI inverter employing **(a)** SPWM and **(b)** DPWM modulation, at nominal operating condition $P = 1\,\text{kW}$. Phase *a* (yellow), phase *b* (red) and phase *c* (blue) output voltages. Phase *a* output voltage ripple (green).

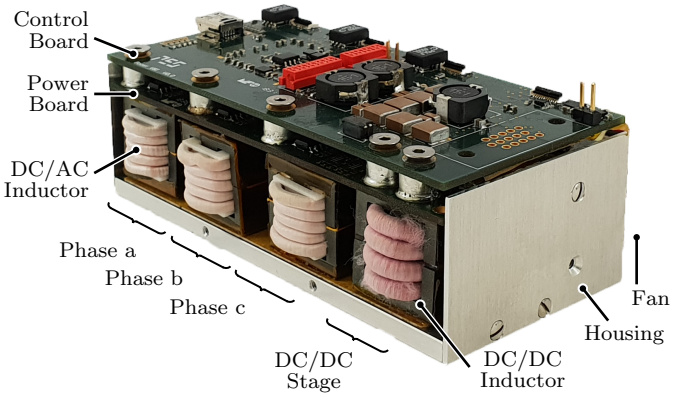


Fig. 5.15: B-VSI hardware prototype (106 mm × 50 mm × 35 mm) achieving a power density of 6 kW/dm^3 (98 W/in^3).

Tab. 5.5: Parameter values of the B-VSI hardware prototype, corresponding to the schematic diagram notation of **Fig. 5.2**.

B-VSI - DC/DC stage	
Switching frequency $f_{s,i}$	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_i	1.5 µH
Capacitance C_i	10 µF
Capacitance C_{DC}	25 µF
B-VSI - DC/AC stage	
Switching frequency $f_{s,o}$	300 kHz
Switches (1 device)	200 V EPC 2034
Inductance L_o	5 µH
Capacitance C_o	2 µF

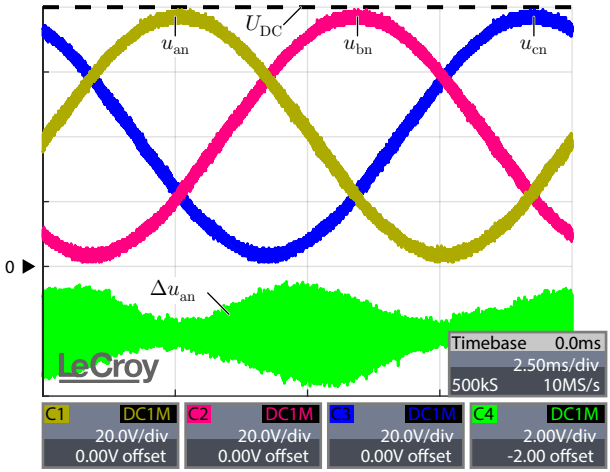


Fig. 5.16: Experimentally measured waveforms for the B-VSI inverter at nominal operating condition $P = 1\,\text{kW}$. Phase a (yellow), phase b (red) and phase c (blue) output voltages. Phase a output voltage ripple (green).

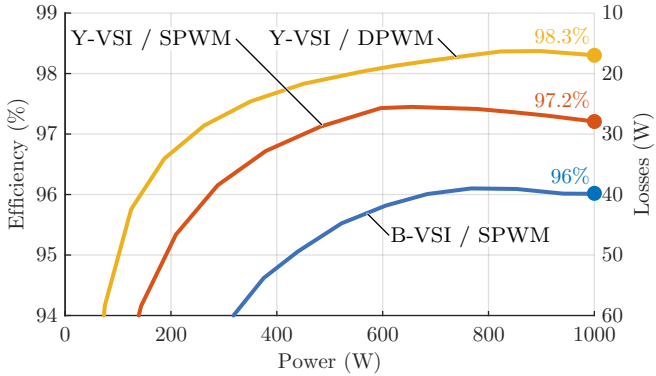


Fig. 5.17: Efficiency profile of conventional B-VSI (blue), Y-VSI employing SPWM (orange) and Y-VSI employing DPWM (yellow).

acquires two voltage values $u_{\bar{a}n} = \{0\,\text{V}, 80\,\text{V}\}$, and is processed by the full sine-wave output filter ($L_o = 5\,\mu\text{H}, C_o = 2\,\mu\text{F}$). Thanks to the DM/CM attenuation of the output filter (-31dB at the frequency $f_s = 300\,\text{kHz}$), a worst case voltage ripple value of only $\Delta U_{an} = 1.4\,\text{V}$ appears at the load terminal a. This voltage ripple value is low, hence ensures a safe motor operation.

The voltage ripple Δu_{an} of the load terminal a is also measured for the Y-VSI in **Fig. 5.14**. The voltage ripple Δu_{an}, is caused by the PWM operation of the half-bridges $\bar{a}_1$ and $\bar{a}_2$. Thanks to the integrated AC filter of the Y-VSI, the voltage ripple is $\Delta U_{an} < 1\,\text{V}$ (for either SPWM or DPWM). The Y-VSI benefits from a slightly better motor voltage quality than the B-VSI, for the system specifications at hand (i.e. modulation index $M = 4/3$). It is reminded that the B-VSI and Y-VSI employ the same AC filter component values, i.e. $L_o = 5\,\mu\text{H}, C_o = 2\,\mu\text{F}$. By comparing the voltage ripple generated by SPWM and DPWM modulation (cf. **Fig. 5.14**), it is evident that the latter DPWM results in an overall lower voltage ripple Δu_{an}. This is expected, since DPWM reduces the total number of switching transitions, which cause the voltage ripple in the first place.

5.5 Summary

Motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency η and power density ρ), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery. Therefore, buck-boost inverter topologies are required, which can guarantee the nominal speed/voltage range of the motor independent of the DC input voltage fluctuation.

A promising buck-boost inverter topology, denoted as Y-VSI, is presented in this chapter (cf. **Fig. 5.3**). The Y-VSI is based on a three-phase modular concept, where three identical phase-modules are connected to a common star "Y" point (cf. **Fig. 5.4**). The Y-VSI benefits from four key advantages:

(i) Buck-boost capability. Each phase-module comprises a buck-boost DC/DC converter, hence the Y-VSI can generate output AC voltages that are higher or lower than the input DC voltage.

(ii) High efficiency. The Y-VSI processes the transmitted power P in a unique way. In the typical case, only three out of the six half-bridges are switched, at any given point in time. As a result, low switching losses are generated, hence high inverter efficiency is achieved. Based

on the low number of switched half-bridges, the Y-VSI can be considered as a single-stage inverter.

(iii) Integrated AC output filter. The Y-VSI comprises an integrated output filter, hence generates sinusoidal motor voltages/currents. Furthermore, the Y-VSI protects the motor from high $\mathrm{d}u/\mathrm{d}t$, thus the long-term reliability of the motor is guaranteed. As a result, no additional filter is required between the inverter and the motor.

(iv) Straightforward control. Each phase-module is equivalent to a DC/DC converter, hence can be controlled independently, based on well established control concepts. As a result, the Y-VSI benefits from a simple and uncomplicated control system (cf. **Fig. 5.8**).

Two modulation strategies are comparatively evaluated for the Y-VSI:

(i) Sinusoidal modulation (SPWM) of **Fig. 5.6**, which features offseted sinusoidal output voltages.

(ii) Discontinuous modulation (DPWM) of **Fig. 5.7**. There, each output voltages is non-sinusoidal, however the difference between two output voltages, which is equal to the motor line-to-line voltage, is sinusoidal. By means of DPWM, it is possible to reduce the number of switching transitions of the Y-VSI by 33%, and hence significantly reduce the overall switching losses.

The stresses on the inverter components are analytically derived for both modulation strategies, and a summary is given in **Tab. 5.3**. A comparison of the two modulation strategies reveals that the latter DPWM yields higher efficiency than the former SPWM.

The Y-VSI performance is validated within the context of the application of **Fig. 5.1** and **Tab. 5.1**. In the application at hand, a motor drive system is supplied by a fuel-cell and controls a high-speed 280 krpm 1 kW electric compressor. The Y-VSI hardware prototype of **Fig. 5.13**, which achieves a power density of $\rho = 6.6\,\mathrm{kW/dm^3}$ and an efficiency of $\eta = 98.3\%$, is purposely assembled. The hardware prototype employs the latest generation of GaN power semiconductor devices and features a switching frequency of $f_\mathrm{s} = 300\,\mathrm{kHz}$. Finally, the Y-VSI is compared to the state-of-the-art inverter topology of **Fig. 5.2**, which features two energy conversion stages. The Y-VSI outperforms the state-of-the-art hardware prototype of **Fig. 5.15**, by $\Delta\eta = +2.3\%$ in terms of efficiency and by $\Delta\rho = +10\%$ in terms of power density.

In summary, the Y-VSI is a promising technology for modern variable speed motor drives. The integrated output filter of the Y-VSI allows for the safe use of WBG semiconductor devices. The high $\mathrm{d}u/\mathrm{d}t$ of WBG devices is effectively suppressed by the integrated filter, hence the motor reliability is ensured. Therefore, the Y-VSI fits well with applications, where high performance, sinusoidal motor voltages/currents and wide voltage operating range are of high importance.

6

Double-Bridge Voltage Source Inverter

This chapter summarizes the key research findings also presented in:

- M. Antivachis, F. Dietz, C. Zwyssig, D. Bortis, and J. W. Kolar, "Novel high-speed turbo compressor with integrated inverter for fuel-cell air supply," *Frontiers in Mechanical Engineering*, 2020, early access. .

- M. Antivachis, D. Wu, and J. W. Kolar, "Analysis of double-bridge inverters for drive systems with open-end winding motors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020, early access. DOI: 10.1109/JESTPE.2020.3017085.

Motivation

In order to improve the performance of variable speed drive systems, innovation only in the inverter stage is not enough. Simultaneous design innovation on the inverter and on the motor side is necessary. Following this premise, in this chapter a double-bridge voltage source inverter (DB-VSI), is paired with an open-end winding motor (no floating neutral point). This inverter/motor solution offers a wide input-output voltage transfer ratio and results in excellent motor drive performance.

Executive Summary

The double-bridge voltage source inverter (DB-VSI) is a promising inverter topology for high performance motor drives. A DB-VSI comprises two VSIs, connected to the opposite sides of an open-end winding motor (no floating neutral point). Thanks to its inherent properties, a DB-VSI requires only half the DC supply voltage, compared to a simple VSI, in order to generate the same motor voltage. Accordingly, by processing/switching only half of the DC supply voltage, the DB-VSI benefits from significantly lower semiconductor devices' switching losses. The DB-VSI technology is the main focus of this chapter. Namely, two different DB-VSI variants and/or modulation strategies are comparatively evaluated. After detailing the operating principle of each modulation strategy, the stresses on the inverter components are analytically derived. It is shown that the selection of the DB-VSI modulation strategy impacts the efficiency/power density of the inverter and the voltage quality of the motor. The theoretical considerations are subsequently verified within the context of a high-speed motor drive. In the investigated drive system, a fuel-cell supplies the inverter, which in return controls a 280 krpm 1 kW electric compressor. Two DB-VSI hardware prototypes are purposely assembled and compared against a third state-of-the-art hardware prototype of the same specifications. It is shown that, thanks to the DB-VSI technology it is possible to reduce simultaneously the volume and the losses by up to 50% compared to the state-of-the-art solution. The low DB-VSI volume enables a seamless integration of the inverter into the motor housing. Accordingly, the open-end winding motor is directly attached to the inverter, eliminating the need for cumbersome and costly interconnecting cables. A final, integrated (inverter/motor) hardware prototype is presented, that further highlights the advantages of the DB-VSI technology.

Motor drives, supplied by a fuel-cell (or a battery) must cope with a wide input voltage range [16, 17]. The supply voltage U_i can significantly fluctuate, depending on the power loading of the employed fuel-cell (or depending on the charging status/temperature of the employed battery). In this chapter, the fuel-cell application depicted in **Fig. 6.1**, with the specifications of **Tab. 6.1**, is examined. A 10 kW fuel-cell unit requires a continuous supply of oxygen, which is provided by the high-speed electric compressor. A motor drive system, directly supplied by the fuel-cell controls the electric compressor [2]. The employed high-speed 280 krpm compressor/motor is shown in **Fig. 6.2**. The compressor uses 10% of the fuel-cell power, i.e. 1 kW, and has a nominal phase voltage amplitude of $\hat{U}_o$=40 V [53]. The fuel-cell features a

Tab. 6.1: Variable-speed motor drive specifications. The nominal operating condition, where the highest component stresses appear, is highlighted in bold.

Fuel-cell voltage	U_i	**40 V**...120 V
Inverter fundamental freq.	f_o	0 Hz...**5 kHz**
Inverter power	P	0 W...**1100 W**
Motor speed	n	0 rpm...**280 krpm**
Motor voltage amplitude	$\hat{U}_\mathrm{o}$	0 V...**40 V** (phase, PK)
Motor power	P	0 W...**1000 W**

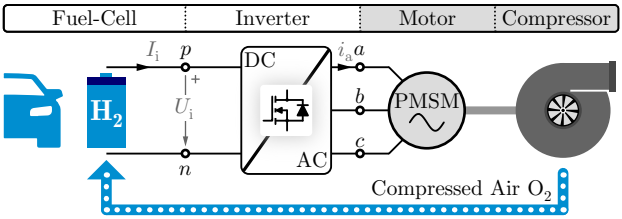


Fig. 6.1: Motor drive application for fuel-cells. An electric compressor provides oxygen to the fuel-cell, while a motor drive, directly supplied by the same fuel-cell, controls the electric compressor.

Fig. 6.2: High-speed 280 krpm electric compressor designed by Celeroton AG. [53].

nominal voltage of $U_\mathrm{i} = 40\,\mathrm{V}$ at full-load condition and a maximum voltage of $U_\mathrm{i} = 120\,\mathrm{V}$ at no-load condition.

Typically in such drive applications, a single-bridge voltage source inverter (SB-VSI) drives a motor with a floating neutral point, as depicted in **Fig. 6.3(a.i)**. A dedicated boost-type DC/DC stage must precede the inverter DC/AC stage in order to adapt the insufficient fuel-cell voltage U_i to a higher DC link voltage U_DC. The DC/DC stage guarantees that the nominal motor voltage can be generated, even if the input voltage U_i is inadequate. Thereby, the two-stage inverter solution of **Fig. 6.4** results. The SB-VSI solution exhibits low efficiency/power density due the two-stage energy conversion and the additional losses/volume originating from the DC/DC stage. In order to generate the nominal motor voltage amplitude of $\hat{U}_\mathrm{o} = \hat{U}_\mathrm{o,max}$, a high DC link voltage of $U_\mathrm{DC} = 2\hat{U}_\mathrm{o} = 80\,\mathrm{V}$ is required in the case of sinusoidal pulse width modulation (or a DC link voltage of $U_\mathrm{DC} = \sqrt{3}\hat{U}_\mathrm{o} = 69.3\,\mathrm{V}$ in the case of third harmonic injection modulation) [56] as is illustrated in **Fig. 6.3(a.ii)**. This high DC link voltage, is possessed/switched by all the semiconductor devices (DC/DC stage and DC/AC stage) resulting in high switching losses.

In order to address the shortcomings of the SB-VSI the promising double-bridge voltage source inverter (DB-VSI) technology [140–143] is investigated in this chapter. The DB-VSI features two VSIs which are connected to the opposite sides of an open-end winding motor as is visualised in **Fig. 6.3(b.i)**. An open-end winding motor allows access to both terminals of each phase winding (i.e. terminals a_1 and a_2 for the phase a), in contrast to a conventional motor with a floating neutral point which provides access to only one terminal per phase (cf. **Fig. 6.3(a.i)**). Historically, DB-VSI inverter technology originates from high voltage/power motor drives [144–148] and has been proposed as an alternative to multi-level inverters [149]. A DB-VSI controls the voltage on both sides of the open-end motor winding (in contrast to SB-VSI). Accordingly, the nominal motor phase voltage amplitude of $\hat{U}_\mathrm{o} = \hat{U}_\mathrm{o,max}$ can be generated by means of a DC supply voltage of only $U_\mathrm{i} = \hat{U}_\mathrm{o}$. The advantageous features of a DB-VSI are utilized in the investigated fuel-cell application [150]. Thanks to the excellent utilization of the DC supply voltage, it is possible to directly connect the DB-VSI inverter to the fuel-cell, without using a dedicated boost-type DC/DC stage. Opposite to the SB-VSI, the DB-VSI is a single-stage converter, thus the power P is processed only once and is delivered more efficiently to the motor. Furthermore, the semiconductor devices of the DB-VSI, process/switch the low fuel-cell nominal voltage of $U_\mathrm{i} = 40\,\mathrm{V}$. In contrast, the semiconductor devices of the SB-VSI must switch the high DC link voltage $U_\mathrm{DC} = 2\hat{U}_\mathrm{o} = 80\,\mathrm{V}$, in order to generate

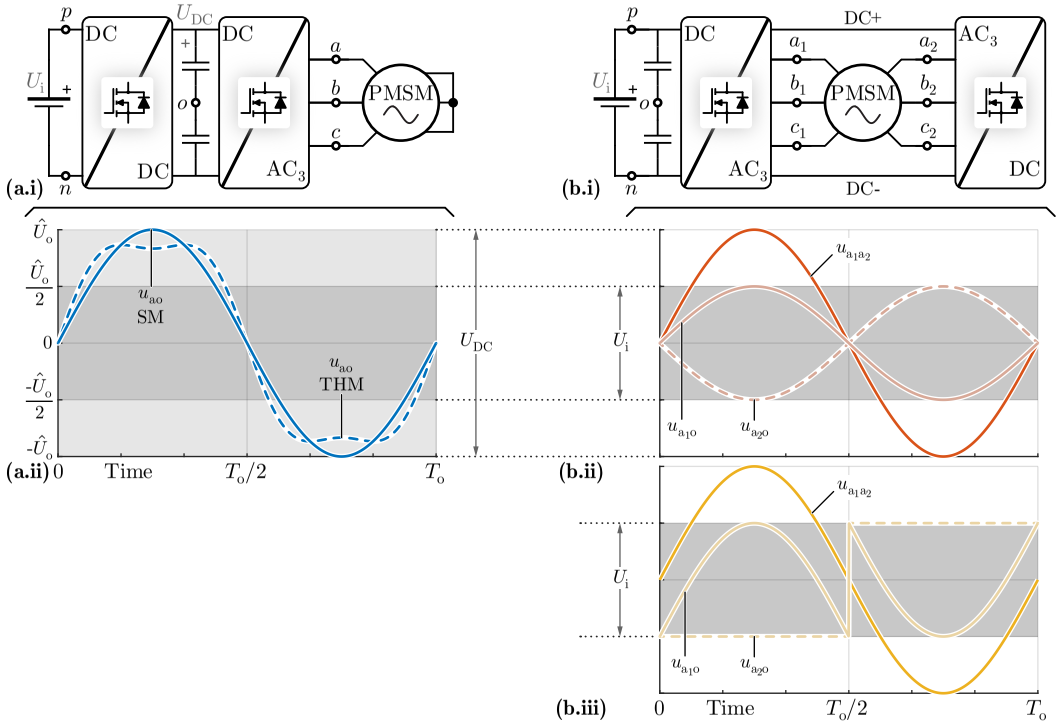


Fig. 6.3: (a.i) Single-bridge voltage source inverter (SB-VSI) driving a conventional motor with a floating neutral point and **(a.ii)** output voltage waveforms. A DC link voltage of $U_{DC} = 2\hat{U}_o$ is required in the case of simple sinusoidal modulation (SM) or $U_{DC} = \sqrt{3}\hat{U}_o$ in the case of third harmonic injection modulation (THM). **(b.i)** Double-bridge voltage source inverter (DB-VSI) driving an open-end winding motor. Output voltage waveforms for **(b.ii)** symmetric modulation and **(b.iii)** unfolder modulation.

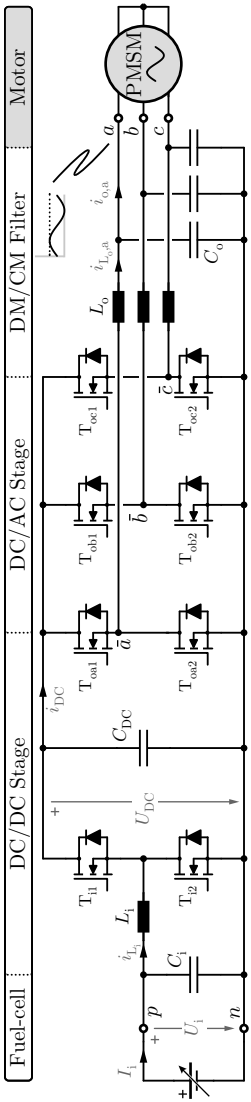


Fig. 6.4: State-of-the-art single-bridge voltage source inverter (SB-VSI) solution for motor drives with a wide input-output voltage range. The SB-VSI is a two-stage converter, i.e. a dedicated DC/DC stage steps up the input voltage U_i to a higher DC link voltage U_{DC}, while a DC/AC stage generates the three-phase motor voltage system. A differential-mode/common-mode (DM/CM) filter is placed before the motor in order to protect the latter from high du/dt.

the same motor phase voltage amplitude $\hat{U}_\mathrm{o}$. Since the switching losses (capacitive) of a unipolar semiconductor device scale with the square U_sw^2 of the commutation voltage U_sw, the DB-VSI can achieve lower overall switching losses than a SB-VSI. By utilizing the superior performance of the DB-VSI solution, this chapter aims for an integration of the inverter in the motor housing [45, 47, 48]. Accordingly, the open-end winding motor is directly attached to the inverter, eliminating the need for cumbersome and costly interconnecting cables.

The exact shape of the motor terminal voltages $u_{\mathrm{a_1o}}$ and $u_{\mathrm{a_2o}}$ depends on the employed DB-VSI modulation strategy, however the resulting motor phase voltage $u_{\mathrm{a_1a_2}} = u_{\mathrm{a_1o}} - u_{\mathrm{a_2o}}$ must be sinusoidal. Two DB-VSI modulation strategies are comparatively evaluated in this chapter. First the symmetric modulation [151–153] is investigated, where both motor terminal voltages $u_{\mathrm{a_1o}}$ and $u_{\mathrm{a_2o}}$ (of phase a) are actively controlled and have a complementary sinusoidal shape ranging within $-U_\mathrm{i}/2 \ldots + U_\mathrm{i}/2$, as illustrated in **Fig. 6.3(b.ii)**. The symmetric modulation requires continuous operation of both VSIs with a high switching frequency f_s. In order to generate continuous/sinusoidal voltages for the motor, two output filters ($L_\mathrm{o} - C_\mathrm{o}$) are employed and placed between the two switched VSIs and the motor. As a result, the $\mathrm{DB_{II}}$-VSI inverter variant of **Fig. 6.5** is derived, where the subscript "II" denotes that both VSIs are switched. Sinusoidal motor voltages are necessary in the case of high-speed motors, in order to limit the generated rotor losses [21, 46, 64]. The thermal management of the rotor is a main concern in high-speed motors, since the high rotational speed and the small rotor volume impede the rotor cooling. As a further advantage, the output filters mitigate the high $\mathrm{d}u/\mathrm{d}t > 30\,\mathrm{kV/\mu s}$, caused by the latest generation of GaN semiconductor devices [26, 27]. If not mitigated, high common-mode (CM) $\mathrm{d}u/\mathrm{d}t$ would lead to premature bearing failure due to parasitic CM currents [33, 154, 155], while differential-mode (DM) $\mathrm{d}u/\mathrm{d}t$ would stress the insulation of the motor windings [32].

In an effort to extract more performance from a DB-VSI, the unfolder modulation [37, 156] is investigated. There, only one out of the two VSIs is continuously operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. It is thereby possible to generate a three-phase voltage system for the motor, with the discontinuous, non-sinusoidal terminal voltages $u_{\mathrm{a_1o}}$ and $u_{\mathrm{a_2o}}$ of **Fig. 6.3(b.iii)**. Thanks to the unfolder modulation, the switching losses are cut in half compared to the respective losses of the symmetric modulation, since the VSI which is operated with the low fundamental motor frequency f_o exhibits negligi-

ble switching losses. Furthermore, the VSI operated with the fundamental frequency f_o can be directly connected to the respective motor terminals. It is hence possible to omit half the filter passive components of the DB_{II}-VSI inverter (symmetric modulation). As a result, the simplified and more compact DB_I-VSI inverter variant of **Fig. 6.8** is derived, where the subscript "I" denotes that only one VSI is switched.

In **Sec. 6.1**, the operating principle of the symmetric modulation and the unfolder modulation is explained. Subsequently, the stresses on the different inverter components are analytically derived in **Sec. 6.2**. Three hardware prototypes are purposely designed and assembled in **Sec. 6.3**, corresponding to the DB_{II}-VSI (symmetric modulation), the DB_I-VSI (unfolder modulation) and the conventional SB-VSI. An experimental comparison of the efficiency η and power density ρ of the three hardware prototypes validates the superior performance of the DB-VSI inverter technology compared to a conventional SB-VSI and highlights the trade-offs between the two DB-VSI modulation strategies. The experimental verification is completed by integrating a DB-VSI inverter and a high-speed compressor into the same housing. The conclusions are drawn in **Sec. 6.4**.

6.1 Modulation Strategies

A DB-VSI inverter comprises two VSIs connected to the opposite sides of an open-end winding motor. Each VSI controls the voltage on one side of the open-end winding motor e.g. voltages u_{a_1o} and u_{a_2o} for phase a, and thus a three-phase motor voltage system is indirectly generated. The exact waveforms of the motor terminal voltage u_{a_1o} and u_{a_2o} depend on the employed modulation strategy. However, the motor phase voltages, which are equal to the differences of the motor terminal voltages, e.g. $u_{a_1a_2} = u_{a_1o} - u_{a_2o}$, must be sinusoidal regardless of the employed modulation strategy

$$\begin{aligned} u_{a_1a_2}(t) &= \hat{U}_o \sin(\omega_o t), \\ u_{b_1b_2}(t) &= \hat{U}_o \sin(\omega_o t - \frac{2\pi}{3}), \\ u_{c_1c_2}(t) &= \hat{U}_o \sin(\omega_o t + \frac{2\pi}{3}), \end{aligned} \tag{6.1}$$

where $\omega_o = 2\pi f_o$ is the fundamental motor angular frequency. The modulation index M is defined as the ratio of the motor voltage amplitude with

respect to the half of the fuel-cell voltage

$$M = \frac{\hat{U}_\mathrm{o}}{\frac{1}{2}U_\mathrm{i}} = 0...2. \tag{6.2}$$

Each phase-leg is operated independent of the other two phases. Therefore, the analysis of the DB-VSI focuses only on phase-leg a, when possible. The derived results can be easily extended to the other two phases b and c.

6.1.1 $\mathrm{DB_{II}}$-VSI Inverter - Symmetric Modulation

The $\mathrm{DB_{II}}$-VSI of **Fig. 6.5** employs a symmetric modulation: Two complementary sinusoidally shaped duty cycles d_{a_1} and d_{a_2}, ranging within 0...1, control the two half-bridges of phase a as shown in **Fig. 6.6**. Subsequently, the duty cycles d_{a_1} and d_{a_2} are compared to the respective carriers, in order to derive the gating signals of the semiconductor devices. In the case of symmetric modulation, the same carrier is used for the two half-bridges $\bar{a}_1$ and $\bar{a}_2$ of phase a [151]. Furthermore, an identical carrier is also used for phases b and c. The duty cycles d_{a_1} and d_{a_2} are derived as

$$d_{\mathrm{a}_1} = \frac{1 + d_\mathrm{a}}{2}, \quad d_{\mathrm{a}_2} = \frac{1 - d_\mathrm{a}}{2}, \tag{6.3}$$

where d_a is a helping variable

$$d_\mathrm{a}(t) = \frac{u_{\mathrm{a}_1\mathrm{a}_2}}{U_\mathrm{i}} = \frac{\hat{U}_\mathrm{o}}{U_\mathrm{i}} \sin(\omega_\mathrm{o} t) \overset{(6.2)}{=} \frac{M}{2} \sin(\omega_\mathrm{o} t). \tag{6.4}$$

The terminal motor voltages $u_{\mathrm{a}_1\mathrm{o}}$ and $u_{\mathrm{a}_2\mathrm{o}}$, which are proportional to the control duty cycles d_{a_1} and d_{a_2}, have a complementary sinusoidal shape as shown in **Fig. 6.3(b.ii)** and are equal to

$$\begin{aligned} u_{\mathrm{a}_1\mathrm{o}} &= \left[d_{\mathrm{a}_1}(t) - \frac{1}{2} \right] U_\mathrm{i} = +\frac{\hat{U}_\mathrm{o}}{2} \sin(\omega_o t) \\ u_{\mathrm{a}_2\mathrm{o}} &= \left[d_{\mathrm{a}_2}(t) - \frac{1}{2} \right] U_\mathrm{i} = -\frac{\hat{U}_\mathrm{o}}{2} \sin(\omega_o t). \end{aligned} \tag{6.5}$$

The motor phase voltage is also sinusoidal $u_{\mathrm{a}_1\mathrm{a}_2} = u_{\mathrm{a}_1\mathrm{o}} - u_{\mathrm{a}_2\mathrm{o}} = \hat{U}_\mathrm{o} \sin(\omega_o t)$.

As a result of the symmetric modulation, both VSIs are continuously operated over time with the switching frequency f_s as is illustrated in **Fig.**

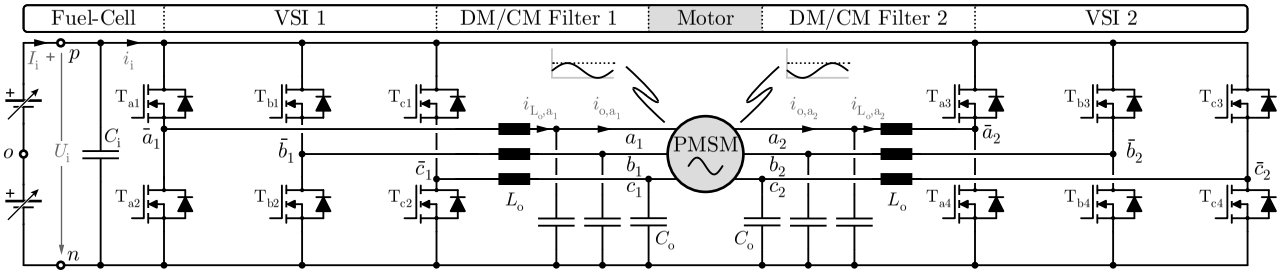


Fig. 6.5: DB_{II}-VSI inverter solution driving an open-end winding motor. A symmetric modulation is employed i.e. both VSIs are continuously operated with the switching frequency f_s. A DM/CM output filter is placed at each side of the open-end winding motor in order to protect the latter from high du/dt.

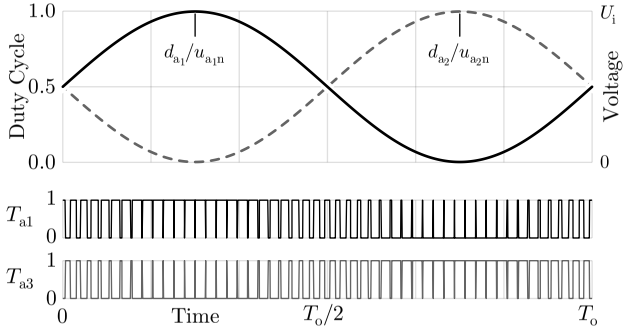


Fig. 6.6: Symmetric modulation: Two complementary sinusoidal duty cycles control the two half-bridges $\bar{a}_1$ and $\bar{a}_2$ of phase a, resulting in continuous switching over time.

6.6. Accordingly, both switch-node voltages $u_{\bar{a}_1 o}$ and $u_{\bar{a}_2 o}$ feature a two-level PWM voltage profile, as shown in **Fig. 6.7(b.i)**. In order to protect the motor from the switch-node PWM voltages ($\mathrm{d}u/\mathrm{d}t$), two DM/CM output filters ($L_o - C_o$) are used (one for each VSI), as visualized in **Fig. 6.5**. Those DM/CM output filters are based on passive components and belong to the family of DC link referenced filters [34, 35], i.e. the filter capacitors C_o are connected/referenced to the negative DC rail n. This feedback connection of the capacitors C_o to the DC link allows to suppress both the DM and the CM $\mathrm{d}u/\mathrm{d}t$ of the semiconductor devices, resulting in a continuous/smooth motor phase voltage.

The motor voltage quality, is now analysed in detail. To this end, each three-phase switch-node voltage system, e.g. $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$, is substituted by a voltage equivalent circuit [59, 155]. Accordingly, the $\mathrm{DB_{II}}$-VSI of **Fig. 6.5** can be represented by the equivalent circuit of **Fig. 6.7(a)**. For example, the two-level PWM voltage of the switch-node $\bar{a}_1$, illustrated in **Fig. 6.7(b.i)**, is broken down into

$$u_{\bar{a}_1 o} = u_{\bar{o}_1,\mathrm{CM}} + u_{\bar{a}_1,\mathrm{DM}}. \tag{6.6}$$

The quantity $u_{\bar{o}_1,\mathrm{CM}}$ is the switch-node CM voltage. As shown in **Fig. 6.7(b.ii)**, $u_{\bar{o}_1,\mathrm{CM}}$ is a four-level PWM voltage and can be further broken down into

$$u_{\bar{o}_1,\mathrm{CM}} = u_{\bar{o}_1,\mathrm{CM}}|_{f_o} + u_{\bar{o}_1,\mathrm{CM}}|_{f_s}, \tag{6.7}$$

where $u_{\bar{o}_1,\mathrm{CM}}|_{f_o}$ is the low-frequency (LF) CM voltage component and $u_{\bar{o}_1,\mathrm{CM}}|_{f_s}$ is the high-frequency (HF) CM voltage component. The quantity $u_{\bar{a}_1,\mathrm{DM}}$ of **(6.6)** is the DM switch-node voltage. As depicted in **Fig. 6.7(b.iii)**, $u_{\bar{a}_1,\mathrm{DM}}$ is a five-level PWM voltage and can be further broken down into

$$u_{\bar{a}_1,\mathrm{DM}} = u_{\bar{a}_1,\mathrm{DM}}|_{f_o} + u_{\bar{a}_1,\mathrm{DM}}|_{f_s}, \tag{6.8}$$

where $u_{\bar{a}_1,\mathrm{DM}}|_{f_o}$ is the LF DM voltage component and $u_{\bar{a}_1,\mathrm{DM}}|_{f_s}$ is the HF DM voltage component. The LF voltage terms $u_{\bar{o}_1,\mathrm{CM}}|_{f_o}$ and $u_{\bar{a}_1,\mathrm{DM}}|_{f_o}$ are directly related to the employed modulation strategy and the corresponding duty cycles d_{a_1} and d_{a_2}. The HF terms $u_{\bar{a},\mathrm{DM}}|_{f_s}$ and $u_{\bar{o},\mathrm{CM}}|_{f_s}$ are related to the PWM switching frequency f_s. The different switch-node voltage components of **(6.7)**-**(6.8)** are illustrated in **Fig. 6.7(b)**. Note that, the breakdown of a switch-node voltage into HF/LF and DM/CM voltage components **(6.6)**-**(6.8)** can be extended to the second VSI switch-node voltage system $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$.

The two-level PWM switch-node voltages $u_{\bar{a}_1 o}$ and $u_{\bar{a}_2 o}$ of phase a are processed by the two DM/CM filters. As a result, the motor terminal voltages $u_{a_1 o}$ and $u_{a_2 o}$ are smooth and continuous. The DM/CM output filters allow

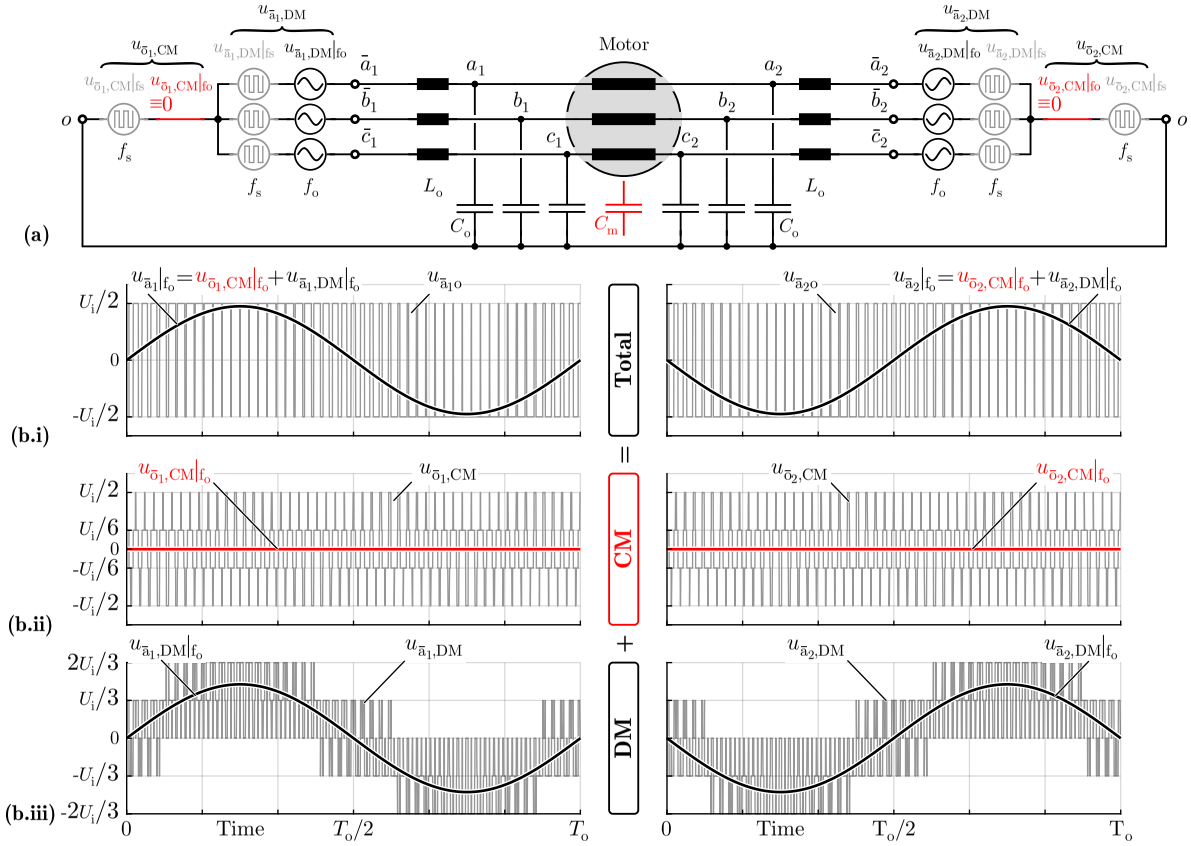


Fig. 6.7: Voltage equivalent circuit of the DB_{II}-VSI inverter. Each switch-node voltage is broken down into four components, e.g. for $\bar{a}_1$: low-frequency (LF) common-mode (CM) voltage ($u_{\bar{o}_1,CM}|_{f_o}$), LF differential-mode (DM) voltage ($u_{\bar{a}_1,DM}|_{f_o}$), high-frequency (HF) CM voltage ($u_{\bar{o}_1,CM}|_{f_s}$) and HF DM voltage ($u_{\bar{a}_1,DM}|_{f_s}$).

the LF switch-node voltage components to pass through intact, resulting in the motor terminal voltages of **(6.5)**. In contrast, the DM/CM output filters attenuate the HF switch-node voltage components resulting into a voltage ripple Δu_{a_1} and Δu_{a_2} at the motor terminals, as is derived in the following. For a filter inductor L_o The maximum inductor current ripple amplitude (single-side) $\Delta I_{\mathrm{L_o}}$ can be calculated as

$$\Delta I_{\mathrm{L_o}} = \frac{U_\mathrm{i}}{8 L_\mathrm{o} f_\mathrm{s}}. \tag{6.9}$$

Accordingly, the maximum occurring voltage ripple amplitude (single-side) $\Delta U_{\mathrm{C_o}}$ at the output filter capacitor C_o is

$$\Delta U_{\mathrm{C_o}} = \frac{\Delta I_{\mathrm{L_o}}}{8 C_\mathrm{o} f_\mathrm{s}} \overset{(6.9)}{=} \frac{U_\mathrm{i}}{64 f_\mathrm{s}^2 L_\mathrm{o} C_\mathrm{o}}. \tag{6.10}$$

The voltage ripple $\Delta u_{\mathrm{C_o}}$ (with a repetition frequency equal to the switching frequency f_s) appears across the capacitors of the two used output filters, since both VSIs are continuously operated with the switching frequency f_s. In other words, a voltage ripple appears on either side of the open-end winding motor i.e. at the motor terminals $[a_1, b_1, c_1]$ and $[a_2, b_2, c_2]$ when symmetric modulation is employed with a maximum value of

$$\Delta U_{\mathrm{a_1o}} = \Delta U_{\mathrm{a_2o}} = \Delta U_{\mathrm{C_o}} = \frac{U_\mathrm{i}}{64 f_\mathrm{s}^2 L_\mathrm{o} C_\mathrm{o}}. \tag{6.11}$$

After quantifying the voltage of the open-end winding motor terminals individually, the motor CM voltage is now analysed. The CM voltage at each side of the open-end winding motor is

$$\begin{aligned} u_{\mathrm{o_1,CM}}(t) &= \frac{u_{\mathrm{a_1o}} + u_{\mathrm{b_1o}} + u_{\mathrm{c_1o}}}{3} \\ u_{\mathrm{o_2,CM}}(t) &= \frac{u_{\mathrm{a_2o}} + u_{\mathrm{b_2o}} + u_{\mathrm{c_2o}}}{3}. \end{aligned} \tag{6.12}$$

The motor CM voltage is defined at the middle of the motor winding as

$$u_{\mathrm{o,CM}}(t) = \frac{u_{\mathrm{o_1,CM}} + u_{\mathrm{o_2,CM}}}{2}. \tag{6.13}$$

Accordingly, a zero CM voltage is calculated in the case of symmetric modulation, based on **(6.5)**,**(6.12)** and **(6.13)**

$$u_{\mathrm{o_1,CM}} = u_{\mathrm{o_2,CM}} = u_{\mathrm{o,CM}} = 0, \tag{6.14}$$

which guarantees low electric stress on the motor. The symmetric modulation is summarized in **Tab. 6.2**.

Tab. 6.2: Symmetric modulation (DB_{II}-VSI) and unfolder modulation (DB_{I}-VSI) summary.

	DB_{II}-VSI	**DB_{I}-VSI**
d_{a_1}	$\frac{1}{2}(1+d_a)$	$\begin{cases} d_a, & d_a \geq 0 \\ 1+d_a, & d_a < 0 \end{cases}$
d_{a_2}	$\frac{1}{2}(1-d_a)$	$\begin{cases} 0, & d_a \geq 0 \\ 1, & d_a < 0 \end{cases}$
u_{a_1o}	$+\frac{1}{2}\hat{U}_o \sin(\omega_o t)$	$\hat{U}_o \sin(\omega_o t) - \frac{1}{2}U_i \mathrm{rec}(\omega_o t)$
u_{a_2o}	$-\frac{1}{2}\hat{U}_o \sin(\omega_o t)$	$-\frac{1}{2}U_i \mathrm{rec}(\omega_o t)$
ΔU_{a_1o}	$\frac{U_i}{64 f_s^2 L_o C_o}$	$\frac{U_i}{64 f_s^2 L_o C_o}$
ΔU_{a_2o}	$\frac{U_i}{64 f_s^2 L_o C_o}$	0
$u_{o,CM}$	0	$-\frac{1}{6}U_i \mathrm{rec}(3\omega_o t)$

A sinusoidal motor voltage $u_{a_1a_2} = \hat{U}_o \sin(\omega_o t)$ and the variable $d_a = \frac{1}{2}M \sin(\omega_o t)$ are assumed.

6.1.2 DB_{I}-VSI Inverter - Unfolder Modulation

The DB_{I}-VSI of **Fig. 6.8** employs an unfolder modulation. That is, only one out of the two VSIs is continuously operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. The resulting discontinuous duty cycles d_{a_1} and d_{a_2} for phase a are shown in **Fig. 6.9** and are calculated as

$$d_{a1} = \begin{cases} d_a, & d_a \geq 0 \\ 1+d_a, & d_a < 0 \end{cases}, \quad d_{a2} = \begin{cases} 0, & d_a \geq 0 \\ 1, & d_a < 0 \end{cases}, \tag{6.15}$$

where d_a is given in **(6.4)**. The motor terminal motor voltages u_{a_1o} and u_{a_2o} are proportional to the control duty cycles d_{a_1} and d_{a_2}, respectively and are

$$\begin{aligned} u_{a_1o} &= \left[d_{a_1}(t) - \frac{1}{2} \right] U_i = \hat{U}_o \sin(\omega_o t) - \frac{U_i}{2} \mathrm{rec}(\omega_o t) \\ u_{a_2o} &= \left[d_{a_2}(t) - \frac{1}{2} \right] U_i = -\frac{U_i}{2} \mathrm{rec}(\omega_o t), \end{aligned} \tag{6.16}$$

where rec(x) is a rectangular function

$$\mathrm{rec}(x) = \begin{cases} 1, & 0 < x \leq \pi \\ -1, & \pi < x \leq 2\pi \end{cases} . \tag{6.17}$$

The two motor terminal voltages are non-sinusoidal and discontinuous as shown in **Fig. 6.3(b.iii)**, but result in a sinusoidal motor phase winding voltage $u_{\mathrm{a_1a_2}} = u_{\mathrm{a_1o}} - u_{\mathrm{a_2o}} = \hat{U}_\mathrm{o} \sin(\omega_o t)$. Only the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ which is operated with the switching frequency f_s requires a dedicated output filter. In contrast, the VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ which is operated with the fundamental motor frequency f_o does not require a dedicated output filter, hence can be directly connected to the respective motor terminals $[a_2, b_2, c_2]$. Therefore, the simplified filter configuration of the $\mathrm{DB_I}$-VSI shown in **Fig. 6.8** is derived.

The motor voltage quality is now analysed in detail. To this end, the $\mathrm{DB_I}$-VSI of **Fig. 6.8** can be represented by the equivalent circuit of **Fig. 6.10(a)**. Similar to the $\mathrm{DB_{II}}$-VSI analysis, each switch-node voltage is broken down into HF/LF and DM/CM voltage components as described by **(6.6)**-**(6.8)**. In particular, the switch-node voltage $u_{\bar{\mathrm{a}}_1\mathrm{o}}$ of the half-bridge $\bar{a}_1$, which is operated with the switching frequency f_s, features a two-level PWM voltage profile as illustrated in **Fig. 6.10(b.i)**. Accordingly, this switch-node voltage can be broken down into a four-level PWM CM voltage component $u_{\bar{\mathrm{o}}_1,\mathrm{CM}}$ of **Fig. 6.10(b.ii)** and a five-level PWM DM voltage component $u_{\bar{\mathrm{a}}_1,\mathrm{DM}}$ of **Fig. 6.10(b.iii)**. In contrast, the switch-node voltage $u_{\bar{\mathrm{a}}_2\mathrm{o}}$ of the half-bridge $\bar{a}_2$, which is operated with the motor fundamental frequency f_o, features a two-level rectangular (not PWM) voltage profile with a repetition frequency equal to the fundamental frequency f_o (cf. **Fig. 6.10(b.i)**). This switch-node voltage can be broken down according to **(6.6)** into a two-level rectangular CM voltage component $u_{\bar{\mathrm{o}}_2,\mathrm{CM}}$ with repetition frequency equal to three times the fundamental frequency $3f_\mathrm{o}$ (cf. **Fig. 6.10(b.ii)**) and a five-level rectangular DM voltage component $u_{\bar{\mathrm{a}}_2,\mathrm{DM}}$ with a repetition frequency equal to the fundamental frequency f_o (cf. **Fig. 6.10(b.iii)**).

The switch-node $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ voltages of the switching frequency operated VSI are processed by the output filter: The output filter allows the LF switch-node voltage components to pass through intact, resulting in the LF motor terminal voltage $u_{\mathrm{a_1o}}$ of **(6.16)**. In contrast, the output filter attenuates the HF switch-node $\bar{a}_1$ voltage components, resulting in a small motor terminal voltage ripple $\Delta u_{\mathrm{a_1o}}$. The voltage ripple $\Delta u_{\mathrm{a_1o}}$ at the motor terminal a_1 is equal to the voltage ripple $\Delta U_{\mathrm{C_o}}$ across the output filter capacitor C_o which is given in **(6.10)**. The switch-node $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ voltages of the fundamental frequency operated VSI are directly applied to the respective motor terminals $[a_2, b_2, c_2]$.

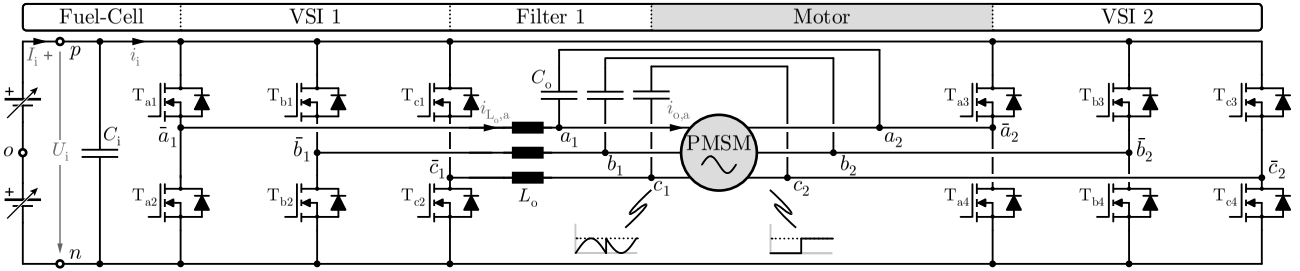


Fig. 6.8: DB_I-VSI inverter solution driving an open-end winding motor. An unfolder modulation is employed, i.e. only one VSI is operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. Only one output filter is placed between the high-frequency operated VSI and the motor, in order to protect the latter against high du/dt.

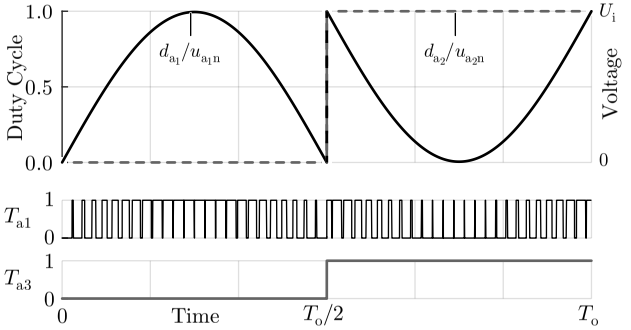


Fig. 6.9: Unfolder modulation: Only half-bridge $\bar{a}_1$ is continuously operated with the switching frequency f_s, while the second half-bridge $\bar{a}_2$ of phase a is operated with the fundamental motor frequency f_o.

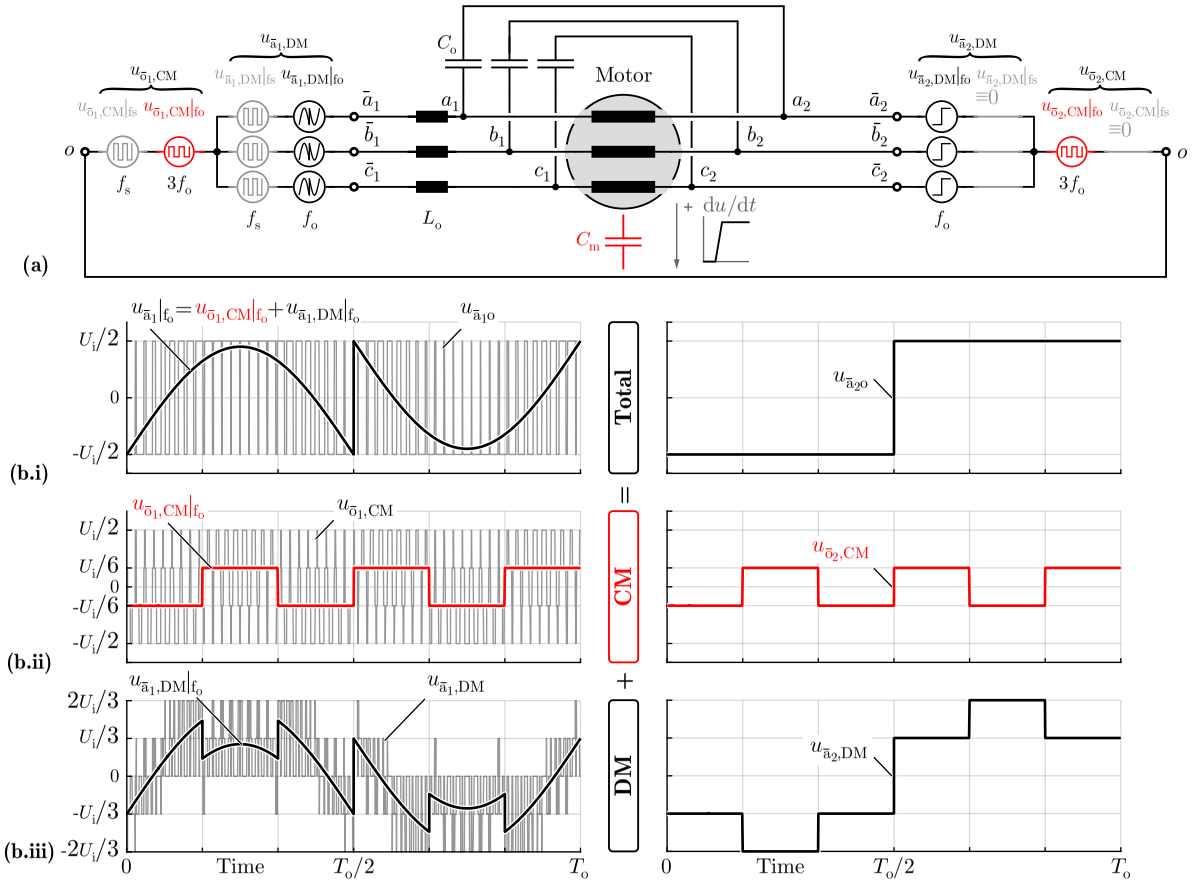


Fig. 6.10: Voltage equivalent circuit of the DB$_I$-VSI inverter. Each switch-node voltage is broken down into four components, e.g. for $\bar{a}_1$: low-frequency (LF) common-mode (CM) voltage ($u_{\bar{o}_1,CM}|_{f_o}$), LF differential-mode (DM) voltage ($u_{\bar{a}_1,DM}|_{f_o}$), high-frequency (HF) CM voltage ($u_{\bar{o}_1,CM}|_{f_s}$) and HF DM voltage ($u_{\bar{a}_1,DM}|_{f_s}$). The unfolder modulation causes a CM voltage on the motor, with a rectangular shape and a repetition frequency equal to three times the fundamental motor frequency $3f_o$.

Therefore, the motor terminal voltage u_{a_2o} of **(6.16)** results, while no voltage ripple appears at the motor terminals $[a_2, b_2, c_2]$. Accordingly, the worst case voltage ripple amplitude (single-side) at the motor terminals a_1 and a_2 is

$$\Delta U_{a_1o} = \frac{U_i}{64 f_s^2 L_o C_o}, \quad \Delta U_{a_2o} = 0. \tag{6.18}$$

The overall motor CM voltage is now analysed. The CM voltage at each side of the open-end winding motor is calculated based on **(6.12)** and **(6.16)**

$$u_{o_1,CM}(t) = u_{o_2,CM}(t) = -\frac{U_i}{6}\mathrm{rec}(3\omega_o t). \tag{6.19}$$

In the case of unfolder modulation, a residual LF CM voltage appears at the motor terminals which is highlighted in red in **Fig. 6.10(b.ii)**. This CM voltage has a rectangular shape, a repetition frequency equal to three times the fundamental motor frequency $3f_o$ and an amplitude of $\frac{U_i}{6}$. The CM voltages on the two sides of the open-end winding motor are equal. If the CM voltages $u_{o_1,CM}$ and $u_{o_2,CM}$ would not be equal, then substantial circulating CM currents would appear in the DB_I-VSI inverter. The CM motor voltage, calculated on the middle of the motor windings based on **(6.13)** is

$$u_{o,CM}(t) = -\frac{U_i}{6}\mathrm{rec}(3\omega_o t). \tag{6.20}$$

The CM motor voltage features also a rectangular shape. At the edges of the rectangular motor CM voltage, $\mathrm{d}u/\mathrm{d}t$ appears on the motor bearing. Then, CM current can flow through the motor bearing, which is represented by the parasitic capacitor C_m in **Fig. 6.10(a)**. It is sown in [29], that the expected lifetime of the motor bearing decreases as higher CM RMS current flows through the bearing. For the case of the DB_{II}-VSI, $\mathrm{d}u/\mathrm{d}t$ appears only six times during a fundamental period T_o (cf. **Fig. 6.10(b.ii)**). Therefore, the bearing CM RMS current is low and hence non-critical for the motor reliability. The unfolder modulation is summarized in **Tab. 6.2**.

6.1.3 DB_{II}-VSI Inverter - Alternative Modulation Strategies

Two alternative modulation strategies that improve the efficiency of the DB_{II}-VSI (cf. **Fig. 6.5**) are now detailed. First, the hybrid modulation is analysed. This modulation strategy resembles the unfolder modulation of **Fig. 6.9**, but instead of an abrupt change of the duty cycles d_{a_1} and d_{a_2} at $t = T_o/2$, a

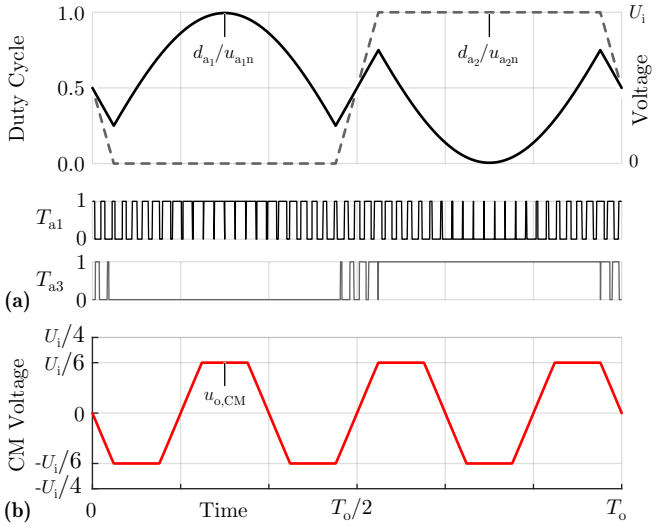


Fig. 6.11: (a) Hybrid modulation: Only half-bridge $\bar{a}_1$ is continuously operated with the switching frequency f_s, while the second half-bridge $\bar{a}_2$ of phase a is operated for a small fraction of the fundamental period with the switching frequency f_s. **(b)** CM voltage at the middle of the motor windings.

soft (gradual) transition takes place. The respective duty cycles of the hybrid modulation are illustrated in **Fig. 6.11(a)** and are analytically derived as

$$d_{a1} = \begin{cases} d_a, & d_a \geq \dfrac{d^*}{2} \\ \dfrac{1}{2} - \dfrac{d_a}{d^*} + d_a, & -\dfrac{d^*}{2} \leq d_a < \dfrac{d^*}{2} \\ 1 + d_a, & d_a < -\dfrac{d^*}{2} \end{cases}, \tag{6.21}$$

$$d_{a2} = \begin{cases} 0, & d_a \geq \dfrac{d^*}{2} \\ \dfrac{1}{2} - \dfrac{d_a}{d^*}, & -\dfrac{d^*}{2} \leq d_a < \dfrac{d^*}{2} \\ 1, & d_a < -\dfrac{d^*}{2} \end{cases}, \tag{6.22}$$

where d_a is given in **(6.4)** and d^* is a design parameter that defines the slope of the soft transition at $t = T_o/2$. According to the hybrid modulation, the

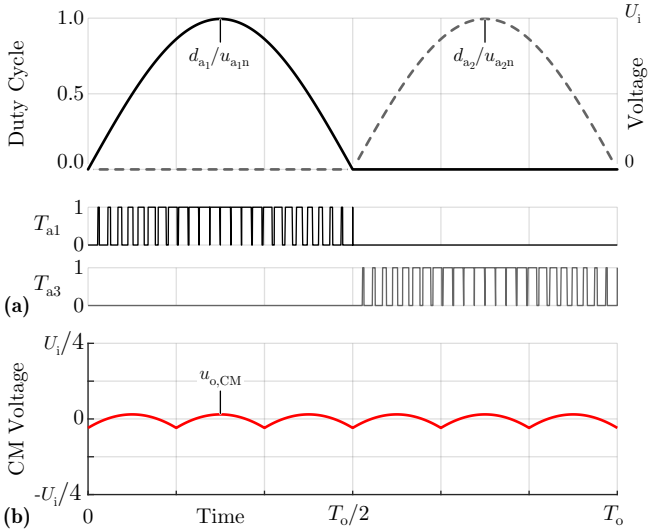


Fig. 6.12: (a) Alternative unfolder modulation: Both half-bridge $\bar{a}_1$ and $\bar{a}_2$ of phase a are partially operated, for half of the fundamental period T_o, with the switching frequency f_s. **(b)** CM voltage at the middle of the motor windings.

VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ is continuously operated with the switching frequency f_s. The second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ is partially operated with the switching frequency f_s, for only a fraction of the fundamental period T_o (around the zero crossing of the motor phase voltage). By reducing the switching transitions of the VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$, the hybrid modulation is able to achieve lower switching losses compared to the symmetric modulation. As a result of the hybrid modulation, a CM voltage appears on the motor windings which is visualized in **Fig. 6.11(b)**. The motor CM voltage is calculated based on the equivalent circuit of **Fig. 6.7**, has a trapezoidal shape and a repetition frequency equal to three times the fundamental frequency $3f_o$. In summary, the hybrid modulation allows to reduce the switching losses of the symmetric modulation at the expense of a higher CM voltage stress on the motor. It is finally noted, that for a design parameter $d^* = 2$ the hybrid modulation is equivalent to the symmetric modulation of **(6.3)**, while for $d^* = 0$ the hybrid modulation is equivalent to the unfolder modulation of **(6.15)**.

Subsequently, the alternative unfolder modulation is described, which is suitable for the DB_{II}-VSI of **Fig. 6.5**. The sinusoidally shaped duty cycles d_{a_1}

and d_{a_2} of **Fig. 6.12(a)** control the two VSIs and are equal to

$$d_{a1} = \begin{cases} d_a, & d_a \geq 0 \\ 0, & d_a < 0 \end{cases}, \quad d_{a2} = \begin{cases} 0, & d_a \geq 0 \\ -d_a, & d_a < 0 \end{cases}, \tag{6.23}$$

where d_a is given in **(6.4)**. Both half-bridge $\bar{a}_1$ and $\bar{a}_2$ of phase a are partially operated with the switching frequency f_s, for half of the fundamental period T_o. The alternative unfolder moudulation resembles the unfolder modulation of **Fig. 6.9**, in that only three out of the six in total half-bridges are operated with the switching frequency f_s at any given point in time. However, in contrast to the unfolder modulation, where only half-bridges belonging to the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are continuously operated with the switching frequency f_s, in the case of alternative unfolder modulation both VSIs share an equal amount of switching transitions over the fundamental period T_o. The alternative unfolder modulation reduces the overall switching transitions by half, compared to symmetric modulation, hence achieves lower switching losses for the DB_{II}-VSI. The main disadvantage of the alternative unfolder modulation strategy is the asymmetric RMS current stress which it causes on the semiconductor devices. As a result of the alternative unfolder modulation a CM voltage appears on the motor windings which is visualized in **Fig. 6.12(b)**. The motor CM voltage is calculated based on the equivalent circuit of **Fig. 6.7**, has an approximately sinusoidal shape and a repetition frequency equal to six times the fundamental frequency $6f_o$.

6.2 Component Stresses

In this section, the voltage/current stresses on the different DB-VSI components and the switching/conductions losses are analytically derived. The results are calculated for a drive system with the specifications of **Tab. 6.1**, however, the presented concepts are general and can be accordingly applied to drive systems with different specifications. For the considered application example, the nominal fuel-cell voltage is $U_i = 40\,\text{V}$, while motor voltage ranges within $\hat{U}_o = 0\,\text{V}...40\,\text{V}$ (phase amplitude). An inverter system that can operate under any load power factor (PF) $\cos(\phi) < 1$ is desirable in this case study. Hence, the output voltage-current phase shift is $\phi = -90^o...90^o$ (i.e. capacitive or inductive load behaviour). Accordingly, the transferred apparent power $S = 0\,\text{W}...1000\,\text{W}$, active power P, fuel-cell current I_i and motor fundamental motor current amplitude $\hat{I}_o$ can be expressed as a function of

the modulation index M **(6.2)** and the PF $\cos(\phi)$ as

$$\begin{aligned} S &= M^2 \frac{3U_\mathrm{i}^2}{8R}, \quad P = M^2 \frac{3U_\mathrm{i}^2}{8R} \cos(\phi), \\ I_\mathrm{i} &= M^2 \frac{3U_\mathrm{i}}{8R} \cos(\phi), \quad \hat{I}_\mathrm{o} = M \frac{U_\mathrm{i}}{2R}, \end{aligned} \tag{6.24}$$

where $R = 3\hat{U}_{\mathrm{o,max}}^2 / 2P_\mathrm{max} = 2.4\,\Omega$. The highest component stresses and semiconductor losses appear at nominal power $P = 1000\,\mathrm{W}$, nominal motor voltage $\hat{U}_\mathrm{o} = 40\,\mathrm{V}$ and unity power factor $\cos(\phi) = 1$. In order to simplify the analysis, the current ripple of the filter inductors L_o is neglected, unless stated otherwise.

First, the component stresses which are independent of the employed modulation strategy (symmetric or unfolder modulation) are derived. The voltage stress on the power semiconductor devices is analysed. All the semiconductor devices of a DB-VSI are blocking and/or switching the fuel-cell voltage U_i. Hence, the maximum fuel-cell voltage $U_\mathrm{i,max} = 120\,\mathrm{V}$ (at no load operating condition), with some additional safety margin dictates the voltage rating of the employed power semiconductor devices. For this reason, 200 V rated GaN semiconductor devices are selected.

In a second step, the RMS current stress on the semiconductor devices is calculated

$$\begin{aligned} I_{\mathrm{Ta_1,RMS}} &= I_{\mathrm{Ta_2,RMS}} = \frac{\hat{I}_\mathrm{o}}{\sqrt{2}} \frac{1}{\sqrt{2}} \\ I_{\mathrm{Ta_3,RMS}} &= I_{\mathrm{Ta_4,RMS}} = \frac{\hat{I}_\mathrm{o}}{\sqrt{2}} \frac{1}{\sqrt{2}}. \end{aligned} \tag{6.25}$$

The above current stress expressions neither depend on the modulation strategy, nor on the power factor $\cos(\phi)$. The current stresses are symmetric, i.e. the high-side and the low-side semiconductor devices of each of the employed half-bridges conduct the same RMS current. Hence, the DB-VSI inverter can conduct the nominal motor current $\hat{I}_\mathrm{o}$ and torque under any operating condition of the motor, e.g. during motor acceleration, starting from standstill. Assuming that the two VSIs of the DB-VSI are identical and based on the RMS current stresses of **(6.25)**, the resulting total semiconductor devices' conduction losses are

$$P_\mathrm{cd} = 6 \frac{\hat{I}_\mathrm{o}^2}{2} R_\mathrm{T,on}, \tag{6.26}$$

where $R_{T,on}$ is the on-state resistance of each (unipolar) power semiconductor device. It is reminded, that for the above calculation of the conduction losses, the current ripple of the filter inductors L_o is neglected.

The input capacitance value C_i is now selected. The capacitor C_i conducts the switched input current $i_i(t)$ of the DB-VSI. The worst case current, flowing through the input capacitor over a switching period T_s is $i_i(t) = \frac{1}{2}\hat{I}_o \mathrm{rec}(2\pi f_s t)$. The input capacitor current is in this case rectangular, with 50% duty cycle and has an amplitude of $\hat{I}_o/2$. Accordingly, a high (local) RMS current stress on the input capacitor $I_{C_i,RMS} = \hat{I}_o/2$ results. Based on the rectangular current waveform $i_i(t) = \frac{1}{2}\hat{I}_o \mathrm{rec}(2\pi f_s t)$, the worst case voltage ripple across the input capacitor C_i and/or the fuel-cell is

$$\Delta U_i = \frac{\hat{I}_o}{8 f_s C_i}. \tag{6.27}$$

Therefore, in order to limit the input voltage ripple to a sufficiently low value ΔU_i the input capacitance must be

$$C_i \geq \frac{\hat{I}_o}{8 f_s \Delta U_i}. \tag{6.28}$$

The resulting input capacitance value C_i is inversely proportional to the switching frequency f_s and is typically small. It is noted here, that there is no need for low-frequency energy storage in a balanced three-phase system. In summary, the input capacitor must conduct a high-frequency switched current with a high RMS value $I_{C_i,RMS}$, while a low capacitance C_i is typically required. Ceramic and film capacitors feature a low series resistance, thus can conduct the high RMS current $I_{C_i,RMS}$ without generating excessive losses. Therefore, ceramic or film capacitors are suggested for the C_i realization. Ceramic capacitors are in general more compact but more expensive than film capacitors. Therefore, the choice between the two capacitor types depends on the design priority, i.e. low volume or low cost.

6.2.1 DB_{II}-VSI Inverter - Symmetric Modulation

The switching losses for the symmetric modulation (DB_{II}-VSI) are now analytically calculated. To this end, the switching energy dissipation E_{sw} for each hard switching transition of a half-bridge is approximated as a linear function of the commutation current I_{sw} as

$$E_{sw}(I_{sw}) = k_0 + k_1 I_{sw}. \tag{6.29}$$

Accordingly, the switching power dissipation for a switching frequency f_s is

$$P_{sw}(I_{sw}) = f_s E_{sw} = f_s(k_0 + k_1 I_{sw}). \tag{6.30}$$

The parameters k_0 and k_1 depend on the switched voltage U_{sw}. Namely the parameter k_0 represents the constant part of the switching losses and is calculated in literature [110] (assuming unipolar power semiconductors) as

$$k_0(U_{sw}) = Q_{oss}(U_{sw}) \cdot U_{sw}, \tag{6.31}$$

where Q_{oss} is the electric charge stored in the non-linear output parasitic capacitance C_{oss} of a MOSFET

$$Q_{oss}(U_{sw}) = \int_0^{U_{sw}} C_{oss}(u)\mathrm{d}u. \tag{6.32}$$

The parameter $k_1(U_{sw})$ represents the linear, current dependent part of the switching losses, and is specific to the semiconductor technology and the gate driver circuit [86, 111].

Subsequently, the expression **(6.30)** for the switching losses is applied to the two switched VSIs of the DB_{II}-VSI inverter, where the commutation current varies over time in a sinusoidal fashion. In order to account for the sinusoidal current waveform, an integration of **(6.30)** over the fundamental period T_o is performed. The resulting sum of the switching losses for all three phases of the DB_{II}-VSI are

$$P_{sw}\left(\hat{I}_o\right) = 6f_s\left[k_0 + k_1\frac{2}{\pi}\hat{I}_o\right]. \tag{6.33}$$

The switching losses comprise two components, a constant part $6f_s k_0$ which is independent of the converter load and a linear part $6f_s k_1 2\hat{I}_o/\pi$ (proportional to the average value of a sinusoidal current half cycle $2\hat{I}_o/\pi$) which increases linearly with the output current $\hat{I}_o$ and is used to characterise the load state. The maximum switching losses occur for maximum motor voltage/power. Based on the above calculations, the switching losses are unaffected by the load power factor $\cos(\phi)$.

The passive components of the two DM/CM output filters are now selected. In particular, six inductors L_o and six capacitors C_o are employed in total. For a filter inductor L_o the maximum inductor current ripple amplitude (single-side) ΔI_{L_o} is given by **(6.9)**. Accordingly, in order to limit the current ripple to a maximum value ΔI_{L_o} the inductor L_o value should be

$$L_o \geq \frac{U_i}{8\Delta I_{L_o} f_s}. \tag{6.34}$$

The maximum occurring voltage ripple amplitude (single-side) ΔU_{C_o} at the output filter capacitor C_o is given by **(6.10)**. Therefore, in order to limit the voltage ripple to a maximum value $\Delta U_{C_o} \simeq 1\,\mathrm{V}$, which is safe for the motor operation, the capacitance C_o values should be

$$C_o \geq \frac{U_i}{64 f_s^2 L_o \Delta U_{C_o}}. \tag{6.35}$$

The inductor L_o losses are now investigated. In general, there is a direct relation between the inductor losses and the RMS inductor current ripple $\Delta I_{L_o,RMS}$, as a high RMS current ripple results in a high frequency RMS flux density and hence substantial core losses [85]. In addition, a high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple $\Delta I_{L_o,RMS}$ is a reasonable performance indicator for the design of the inductive components and is calculated in the following. The local (instantaneous) RMS current ripple of the half-bridge $\bar{a}_1$ (or $\bar{a}_2$) inductor is

$$\Delta i_{L_o,RMS}(t) = 4 d_{a_1}(1 - d_{a_1}) \frac{U_i}{8\sqrt{3} L_o f_s}. \tag{6.36}$$

The worst case local RMS current ripple occurs for $d_{a_1} = 0.5$ and is equal to

$$\Delta I_{L_o,RMS,max} = \frac{U_i}{8\sqrt{3} L_o f_s}. \tag{6.37}$$

In order to calculate the global (total) RMS current ripple, an integration of **(6.36)** over the fundamental period T_o is performed, resulting in a global RMS current ripple of

$$\Delta I_{L_o,RMS}(M) = \sqrt{\frac{3}{128} M^4 - \frac{1}{4} M^2 + 1} \cdot \frac{U_i}{8\sqrt{3} L_o f_s}. \tag{6.38}$$

The global RMS current ripple of the inductor is illustrated in **Fig. 6.13**, while the maximum value occurs for modulation index $M = 0$.

6.2.2 DB_I-VSI Inverter - Unfolder Modulation

In the case of unfolder modulation (DB_I-VSI) only the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ is operated with the switching frequency f_s. The expression **(6.30)** for the switching

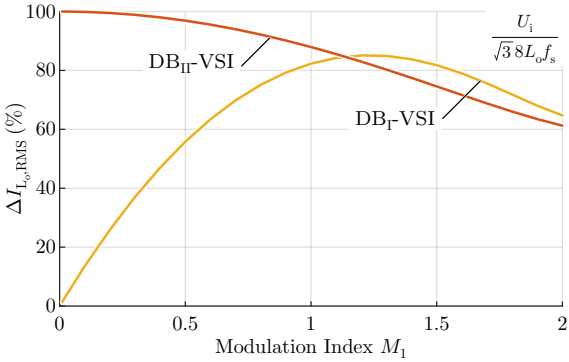


Fig. 6.13: Inductor RMS current ripple for (orange) DB_{II}-VSI employing symmetric modulation and (yellow) DB_{I}-VSI employing unfolder modulation. The RMS current ripple is normalized with respect to the maximum occurring local RMS current ripple $\Delta I_{L_o,RMS,max}$ **(6.37)**.

losses is applied to the switching frequency operated VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$. The resulting sum of the switching losses over a fundamental period T_o is

$$P_{sw}\left(\hat{I}_o\right) = 3 f_s \left[k_0 + k_1 \frac{2}{\pi} \hat{I}_o\right]. \tag{6.39}$$

The second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ is operated with the fundamental motor frequency f_o, hence exhibits negligible switching losses. Therefore, there is a loss imbalance between the first VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$, which generates both switching and conduction losses, and the second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$, which generates only conduction losses. The lower overall losses of the second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ allow for a smaller heatsink or even no heatsink at all for this VSI [87]. Thanks to the unfolder modulation, the overall switching losses are reduced by 50% compared to the symmetric modulation (DB_{II}-VSI) **(6.33)**.

Besides the lower switching losses, the unfolder modulation benefits from a simpler filter structure (cf. DB_{I}-VSI in **Fig. 6.8**) compared to the symmetric modulation (cf. DB_{II}-VSI in **Fig. 6.5**). The VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ which is operated with the fundamental motor frequency f_o can be directly connected to the respective motor terminals $[a_2, b_2, c_2]$. Therefore, only three inductive components L_o in total are required, opposed to six inductive components in the case of the DB_{II}-VSI inverter. The two separate inductors per phase of the DB_{II}-VSI **(6.34)** are combined into a single inductor in the case of the DB_{I}-VSI. Hence, each of the three DB_{I}-VSI inductors features twice the

inductance value compared to the inductance of each of the six DB_{II}-VSI inductors. The DB_{I}-VSI capacitance C_o value is selected to be half compared to the respective value of the DB_{II}-VSI capacitance **(6.35)**. Thereby, an output filter design with double the inductance but half the capacitance is selected for the case of the DB_{I}-VSI, which achieves the same overall attenuation as the respective DB_{II}-VSI output filter. Accordingly, the same maximum voltage ripple of $\Delta U_{C_o} \simeq 1\,\mathrm{V}$ appears across the filter capacitors.

The RMS current ripple stress of the inductor is finally calculated. In order to calculate the global (total) RMS current ripple, an integration of **(6.36)** over the fundamental period T_o is performed. The resulting global RMS current ripple of the DB_{I}-VSI is

$$\Delta I_{L_o,\mathrm{RMS}}(M) = \sqrt{\frac{3}{8}M^4 - \frac{16}{3\pi}M^3 + 2M^2} \cdot \frac{U_i}{8\sqrt{3}L_o f_s}, \tag{6.40}$$

and is illustrated in **Fig. 6.13**.

6.3 Experimental Validation

The proposed DB-VSI inverter concept is tested within the fuel-cell application of **Fig. 6.1** and **Tab. 6.1**. A 10 kW fuel-cell unit requires a continuous supply of oxygen, which is provided by the 280 krpm high-speed electric compressor of **Fig. 6.2**. A motor drive system, directly supplied by the fuel-cell controls the electric compressor. The compressor drive system uses 10% of the fuel-cell power, i.e. 1 kW.

6.3.1 Design Procedure

In order to design a DB-VSI inverter, the switching frequency f_s must be selected. The previously derived in **Sec. 6.2** component stresses depend on the switching frequency f_s, however the switching frequency is till now not explicitly defined. The switching frequency represents a crucial design tradeoff. A high switching frequency allows to reduce the volume of the passive components, but at the same time increases the semiconductor switching losses and accordingly requires a larger semiconductor heatsink volume. In order to select an appropriate switching frequency, a multi-objective optimization routine, with respect to inverter efficiency η and power density ρ, is emplyed [15, 83], which assesses the performance of several DB-VSI inverter designs. The optimization routine includes the 200 V rated EPC2034 GaN

Tab. 6.3: DB-VSI component stresses, calculated for symmetric and unfolder modulation, at the full-load operating condition of **Tab. 6.1**. Numerical values are derived for the hardware prototype parameters of **Tab. 6.4** and **6.5**.

		$\mathbf{DB_{II}}$**-VSI**		$\mathbf{DB_{I}}$**-VSI**
T_1, T_2, T_3, T_4 voltage PK		$U_T = 40\,V$		$U_T = 40\,V$
T_1, T_2, T_3, T_4 current RMS	**(6.25)**	$I_{T,RMS} = 8.3\,A$	**(6.25)**	$I_{T,RMS} = 8.3\,A$
Conduction losses	**(6.26)**	$P_{cd} = 8.3\,W$	**(6.26)**	$P_{cd} = 8.3\,W$
		$R_{T,on} = 10\,m\Omega$ for 100^oC		$R_{T,on} = 10\,m\Omega$ for 100^oC
Switching losses	**(6.33)**	$P_{sw} = 13.4\,W$	**(6.39)**	$P_{sw} = 6.7\,W$
		$^*k_0 = 3.6\,\mu J$, $k_1 = 0.4\,\mu J/A$ for U_T		$^*k_0 = 3.6\,\mu J$, $k_1 = 0.4\,\mu J/A$ for U_T
Total semiconductor losses		$P_{cd} + P_{sw} = 21.7\,W$		$P_{cd} + P_{sw} = 15\,W$
Efficiency reduction		$\Delta\eta = -2.2\%$		$\Delta\eta = -1.5\%$
Output inductor	**(6.34)**	$L_o = 2.5\,\mu H$	**(6.34)**	$L_o = 5\,\mu H$
PK current ripple	**(6.9)**	$\Delta I_{L_o} = 6.6\,A$ (40%)	**(6.9)**	$\Delta I_{L_o} = 3.3\,A$ (20%)
RMS current ripple	**(6.38)**	$\Delta I_{L_o,RMS} = 2.4\,A$	**(6.40)**	$\Delta I_{L_o,RMS} = 1.2\,A$
Output capacitor	**(6.35)**	$C_o = 4\,\mu F$	**(6.35)**	$C_o = 2\,\mu F$
PK voltage ripple	**(6.10)**	$\Delta U_{C_o} = 0.7\,V$ (1.7%)	**(6.10)**	$\Delta U_{C_o} = 0.7\,V$ (1.7%)
Input capacitor	**(6.28)**	$C_i = 10\,\mu F$	**(6.28)**	$C_i = 10\,\mu F$
PK voltage ripple	**(6.27)**	$\Delta U_{C_i} = 0.7\,V$ (1.7%)	**(6.27)**	$\Delta U_{C_i} = 0.7\,V$ (1.7%)

*Switching parameters are calculated based on [112].

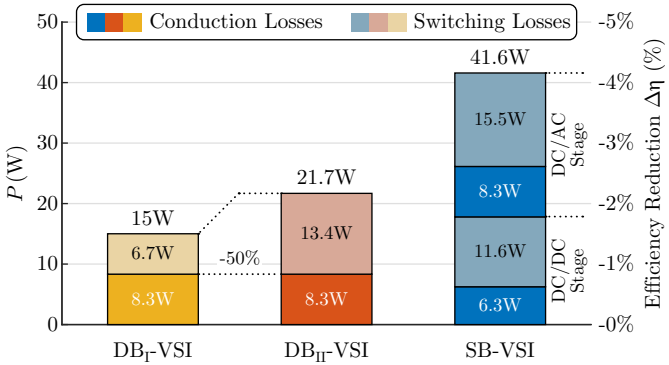


Fig. 6.14: Semiconductor losses breakdown into switching and conduction losses for (yellow) DB_I-VSI employing unfolder modulation, (orange) DB_{II}-VSI employing symmetric modulation and (blue) conventional SB-VSI. The numeric values are calculated for nominal motor power/voltage (i.e. modulation index $M = 2$), using the parameters of **Tab. 6.3**.

semiconductor devices [112], the heatsinks of the semiconductor devices [87], the inductive components L_o [81, 84, 85], and the ceramic capacitors C_o, C_i. Based on the optimization results, a switching frequency of $f_s = 300\,\text{kHz}$ is selected. The selected benchmark designs for the DB_{II}-VSI and DB_I-VSI are given in **Tab. 6.4** and **Tab. 6.5**, respectively. Using the analytic formulas derived in **Sec. 6.2**, the inverter component stresses are calculated and summarized in **Tab. 6.3**. There, the symmetric and unfolder modulation strategies are compared. Furthermore, the semiconductor losses of the selected DB-VSI designs are visualized in **Fig. 6.14**. The unfolder modulation generates the same semiconductor conduction losses but half the switching losses, compared to symmetric modulation.

Tab. 6.3 serves as a general design guideline and can be used for motor drive systems with different specifications. After the designer selects an appropriate switching frequency f_s, based on his/hers system specifications and the available semiconductor technology, **Tab. 6.3** can be easily used in order to design a DB-VSI inverter.

For the sake of completeness, a conventional SB-VSI (cf. **Fig. 6.4**) is designed for the specifications of **Tab. 6.1**. The detailed design process of a SB-VSI can be found in **Chapter 4**. The selected SB-VSI benchmark design, features the same switching frequency of $f_s = 300\,\text{kHz}$, for both the DC/DC stage as well as the DC/AC stage. The SB-VSI component parameters are

summarized in **Tab. 6.6**. The semiconductor losses of the selected SB-VSI design are depicted in **Fig. 6.14**. It is deduced, that the conventional SB-VSI inverter generates more than twice semiconductor losses compared to a DB-VSI solution, for the same switching frequency f_s. There are two main reasons for the high semiconductor losses in the case of the SB-VSI:

(i) Two-stage energy conversion. The power P is processed twice, first in the DC/DC stage and subsequently in the DC/AC stage.

(ii) High DC link voltage U_{DC}. The semiconductor devices of both the DC/DC stage and the DC/AC stage process/switch the high DC link voltage.

6.3.2 Experimental Results

Three inverter hardware prototypes are assembled:

(i) DB_{II}-VSI (symmetric modulation) of **Fig. 6.5**. The hardware prototype is shown in **Fig. 6.15** and the respective component parameters are given in **Tab. 6.4**.

(ii) DB_{I}-VSI (unfolder modulation) of **Fig. 6.8**. The hardware prototype is depicted in **Fig. 6.16** and the component parameters are summarized in **Tab. 6.5**.

(iii) Conventional SB-VSI of **Fig. 6.4**. The hardware prototype is depicted in **Fig. 6.17**, while the component parameters are summarized in **Tab. 6.6**. This hardware serves as the state-of-the-art solution against which the DB-VSI hardware prototypes are compared to.

In order to enable a meaningful comparison, all the above hardware demonstrators feature the same switching frequency of $f_s = 300\,\text{kHz}$. In addition, the gate driver circuit of the employed MOSFETs features a dead time of 40 ns, a turn-on gate resistance of $5\,\Omega$ and a turn-off gate resistance of $0\,\Omega$.

First, the performance of the three hardware prototypes is experimentally compared. The conventional SB-VSI hardware prototype achieves a power density of $\rho = 6\,\text{kW/dm}^3$ (including housing, cooling system and control electronics) and the lowest efficiency of $\eta = 96\%$ at $P = 1\,\text{kW}$ nominal operation. There are two main reasons behind the SB-VSI low efficiency:

(i) The SB-VSI employs two energy conversion stages (DC/DC stage and DC/AC stage), and thus suffers from high losses.

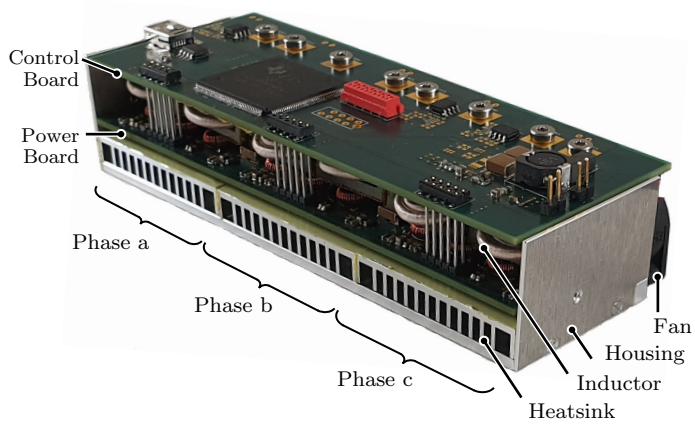


Fig. 6.15: DB_{Π}-VSI inverter hardware prototype employing symmetric modulation. Dimensions 132 mm × 49 mm × 29 mm, power density 5.8 kW/dm^3 (95 W/in^3).

Tab. 6.4: DB_{Π}-VSI hardware prototype parameter values, corresponding to the schematic diagram notation of **Fig. 6.5**.

DB_{Π}-VSI - Symmetric Modulation	
Switching frequency f_s	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_o	2.5 µH
Capacitance C_o	4 µF
Capacitance C_i	10 µF

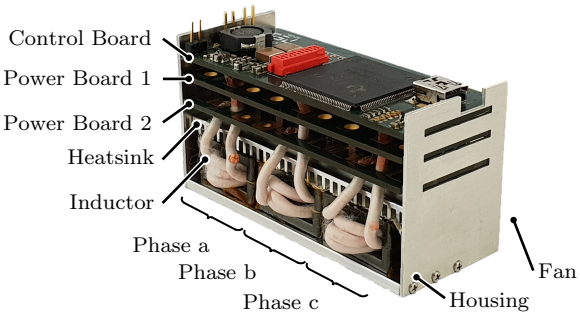


Fig. 6.16: DB_I-VSI inverter hardware prototype employing unfolder modulation. Dimensions 76 mm × 31 mm × 36 mm, power density 13.1 kW/dm^3 (215 W/in^3).

Tab. 6.5: DB_I-VSI hardware prototype parameter values, corresponding to the schematic diagram notation of **Fig. 6.8**.

DB_I-VSI - Unfolder Modulation	
Switching frequency f_s	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Inductance L_o	5 µH
Capacitance C_o	2 µF
Capacitance C_i	10 µF

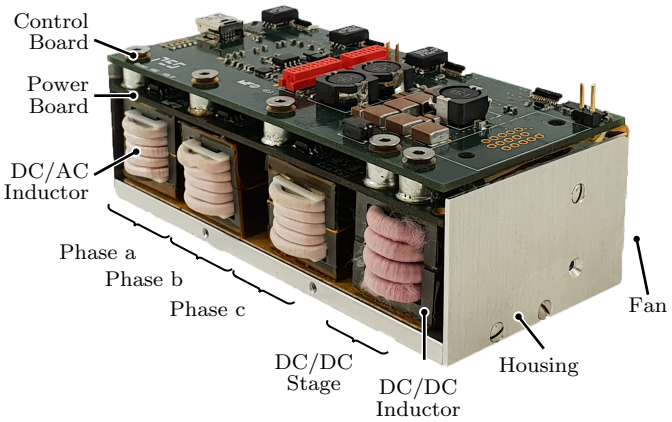


Fig. 6.17: SB-VSI inverter hardware prototype. Dimensions 106 mm × 50 mm × 35 mm, power density 6 kW/dm^3 (98 W/in^3).

Tab. 6.6: SB-VSI hardware prototype parameter values, corresponding to the schematic diagram notation of **Fig. 6.4**.

SB-VSI - DC/DC stage	
Switching frequency $f_{s,i}$	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
	*k_0 = 11 µJ, k_1 = 1.1 µJ/A for U_{DC}
	$R_{Ti,on}$ = 10 mΩ for 100°C
Inductance L_i	1.5 µH
Capacitance C_i	10 µF
Capacitance C_{DC}	25 µF
SB-VSI - DC/AC stage	
Switching frequency $f_{s,o}$	300 kHz
Switches (1 device)	200 V EPC 2034
	*k_0 = 5.5 µJ, k_1 = 1.1 µJ/A for U_{DC}
	$R_{To,on}$ = 20 mΩ for 100°C
Inductance L_o	5 µH
Capacitance C_o	2 µF

*Switching parameters are calculated based on [112].

(ii) The semiconductor devices of both the DC/DC stage and the DC/AC stage have to process/switch the high DC link voltage $U_{DC} = 80\,V$, a fact that leads to high switching losses.

The DB_{II}-VSI features in contrast a single energy conversion stage. By employing a symmetric modulation, the DB_{II}-VSI achieves a power density of $\rho = 5.8\,kW/dm^3$ and a nominal efficiency of $\eta = 97.4\%$. The DB_{II}-VSI is $\Delta\eta = +1.4\%$ more efficient than the SB-VSI for a similar power density. Even though the DB_{II}-VSI features two VSIs (six half-bridges) continuously operated with the switching frequency f_s (compared to only four half-bridges for the SB-VSI), the semiconductor devices only process/switch the low nominal fuel-cell voltage of $U_i = 40\,V$ (compared to the high DC link voltage $U_{DC} = 80\,V$ of the SB-VSI). Since the switching losses scale with the square of the commutation voltage, the DB_{II}-VSI, generates lower overall switching losses than the SB-VSI.

The DB_I-VSI achieves a very high power density of $\rho = 13.1\,kW/dm^3$ and the best nominal efficiency of $\eta = 98.1\%$. Compared to the SB-VSI, the DB_I-VSI allows to more than double the power density, $\Delta\rho = +118\%$, and at the same time increases the efficiency by $\Delta\eta = +2.1\%$. This remarkable performance leap is achieved thanks to the unfolder modulation:

(i) Only one VSI is continuously operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. As a results, the switching losses are kept low.

(ii) The fundamental frequency operated VSI can be directly connected to the motor, resulting in a simplified and more compact filter configuration.

The comparison of the performance of the three hardware prototypes performance is summarized in **Fig. 6.18** and **Tab. 6.7**, while the whole efficiency profile of the three inverter prototypes is illustrated in **Fig. 6.19**.

Finally, the motor voltage quality is assessed. Experimentally measured waveforms of the conventional SB-VSI are shown in **Fig. 6.22**, where a sinusoidal motor phase voltage u_{an} is generated. Superimposed to the motor phase voltage u_{an}, there is a voltage ripple Δu_{an} due to the PWM operation of the half-bridge $\bar{a}$. In particular, the switch-node $\bar{a}$ two-level PWM voltage acquires two voltage values $u_{\bar{a}n} = \{0\,V, 80\,V\}$ and is processed by a DM/CM output filter ($L_o = 5\,\mu H, C_o = 2\,\mu F$). Thanks to the attenuation of the output filter (-31dB at the frequency $f_s = 300\,kHz$), a worst case voltage ripple value of $\Delta U_{an} = 1.4\,V$ (single-side amplitude) is attained.

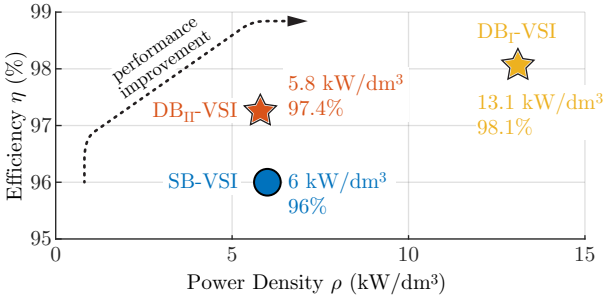


Fig. 6.18: Performance $[\rho, \eta]$ of (blue) conventional SB-VSI, (orange) DB_{II}-VSI and (yellow) DB_{I}-VSI hardware prototypes.

Tab. 6.7: Performance summary of the three inverter prototypes.

Inverter	Power Density ρ	Efficiency η
SB-VSI*	6kW/dm^3 (98W/in^3)	96%
DB_{II}-VSI	5.8kW/dm^3 (95W/in^3)	97.4%
DB_{I}-VSI	13.1kW/dm^3 (215W/in^3)	98.1%

*The efficiency is measured for an input voltage of $U_{\text{i}} = 60\,\text{V}$

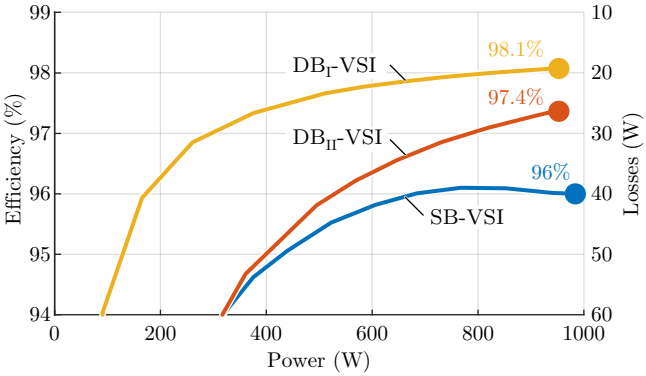


Fig. 6.19: Efficiency profile of (blue) conventional SB-VSI, (orange) DB_{II}-VSI and (yellow) DB_{I}-VSI. Note that, the efficiency of the SB-VSI is measured for an input voltage of $U_{\text{i}} = 60\,\text{V}$, while the efficiency of the DB-VSIs is measured for $U_{\text{i}} = 40\,\text{V}$.

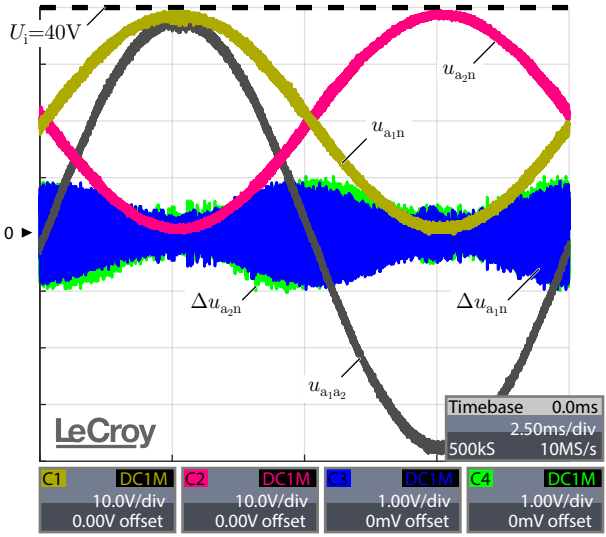


Fig. 6.20: DB_{II}-VSI inverter experimentally measured waveforms at nominal operating condition $M = 2, P = 1\,\text{kW}$: Motor terminal a_1 (yellow) voltage and (blue) voltage ripple, motor terminal a_2 (red) voltage and (green) voltage ripple, and (grey) phase a motor winding voltage.

The DB_{II}-VSI employs a symmetric modulation, while experimentally measured waveforms for phase a are depicted in **Fig. 6.20**. The DB_{II}-VSI features complementary sinusoidal motor terminals voltages u_{a_1n} and u_{a_2n}, resulting in an also sinusoidal motor phase winding voltage $u_{a_1a_2} = u_{a_1n} - u_{a_2n}$. In addition, each motor terminal a_1 and a_2 voltage shows a voltage ripple Δu_{a_1n} and Δu_{a_2n} due to the PWM operation of the respective half-bridges $\bar{a}_1$ and $\bar{a}_2$. Namely, each two-level PWM switch-node $\bar{a}_1$ and $\bar{a}_2$ voltage acquires two voltage values $u_{\bar{a}_1n} \equiv u_{\bar{a}_2n} = \{0\,\text{V}, 40\,\text{V}\}$ and is possessed by a DM/CM output filter ($L_o = 2.5\,\mu\text{H}, C_o = 4\,\mu\text{F}$). Thanks to the attenuation of the filter (the same -31dB attenuation at the frequency $f_s = 300\,\text{kHz}$ as the SB-VSI), a worst case voltage ripple of $\Delta U_{a_1n} = \Delta U_{a_2n} = 0.7\,\text{V}$, is attained, on either side of the motor. The worst case voltage ripple stress on phase a motor winding is the sum of the voltage ripple stresses of the respective terminals a_1 and a_2. Therefore, the overall voltage ripple stress in the case of the DB_{II}-VSI is $\Delta U_{a_1n} + \Delta U_{a_2n} = 1.4\,\text{V}$, which is the same as in the case of the SB-VSI.

The DB_{I}-VSI employs an unfolder modulation, while experimentally measured waveforms for phase a are illustrated in **Fig. 6.21**. The DB_{I}-VSI fea-

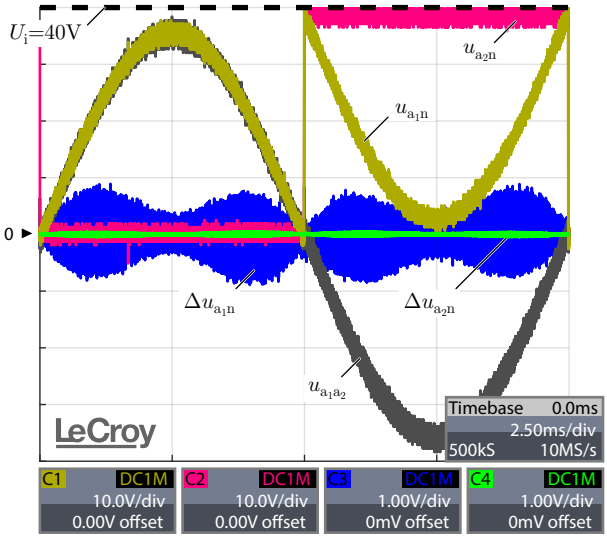


Fig. 6.21: DB_I-VSI inverter experimentally measured waveforms at nominal operating condition $M = 2, P = 1\,\text{kW}$: Motor terminal a_1 (yellow) voltage and (blue) voltage ripple, motor terminal a_2 (red) voltage and (green) voltage ripple, and (grey) phase a motor voltage winding voltage.

tures discontinuous motor terminals voltages u_{a_1n} and u_{a_2n}, however, the motor phase winding voltage $u_{a_1a_2} = u_{a_1n} - u_{a_2n}$ is sinusoidal. Only the motor terminal a_1 voltage shows a voltage ripple Δu_{a_1n} due to the PWM operation of the respective half-bridge $\bar{a}_1$, while the motor terminal a_2 voltage shows no voltage ripple $\Delta u_{a_2n} = 0$ because the respective half-bridge $\bar{a}_2$ is operated with the motor fundamental frequency f_o. In particular, the two-level PWM switch-node $\bar{a}$ voltage acquires two voltage values $u_{\bar{a}_1n} = \{0\,\text{V}, 40\,\text{V}\}$ and is processed by an output filter ($L_o = 5\,\mu\text{H}, C_o = 2\,\mu\text{F}$). Thanks to the attenuation of the filter (the same -31dB attenuation at the frequency $f_s = 300\,\text{kHz}$ as the SB-VSI), a worst case voltage ripple of $\Delta U_{a_1n} = 0.7\,\text{V}$ appears. The worst case voltage ripple stress on phase a motor winding is $\Delta U_{a_1n} + \Delta U_{a_2n} = 0.7\,\text{V}$, which is half compared to the respective value for the SB-VSI and/or the DB_{II}-VSI.

Although the DB_I-VSI benefits from a lower voltage ripple stress on the motor, it causes a residual CM voltage on the motor windings. In particular, at each discontinuity of the motor terminal voltages u_{a_1n} and u_{a_2n} of **Fig. 6.21** a CM du/dt appears on the motor. As illustrated in figure **Fig. 6.10**,

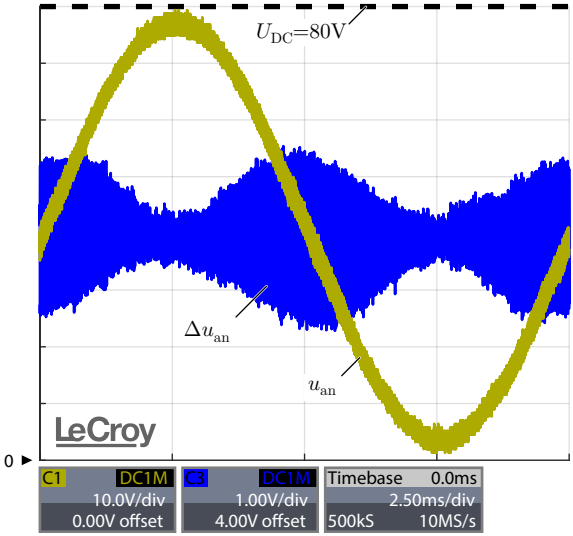


Fig. 6.22: SB-VSI inverter experimentally measured waveforms at nominal operating condition $M = 2, P = 1\,\mathrm{kW}$: Phase a (yellow) output voltage and (blue) output voltage ripple.

the $\mathrm{DB_I}$-VSI results in a motor CM voltage with rectangular shape and a repetition frequency equal to three time the motor fundamental frequency $3f_\mathrm{o}$. This rectangular LF CM voltage is a disadvantage of the $\mathrm{DB_I}$-VSI, but because of the low repetition frequency of $3f_\mathrm{o}$ it does not compromise the motor reliability over the drive system lifetime.

The DB-VSI technology allows for a performance improvement far beyond the SB-VSI state-of-the-art solution. The choice between the $\mathrm{DB_{II}}$-VSI (symmetric modulation) and $\mathrm{DB_I}$-VSI (unfolder modulation) inverter variants represents a crucial trade-off: The latter $\mathrm{DB_I}$-VSI offers exceptionally high performance, in terms of both efficiency and power density, but results in a residual CM voltage on the motor. In contrast, the former $\mathrm{DB_{II}}$-VSI solution sacrifices some of the performance but achieves a better motor voltage quality, with lower CM $\mathrm{d}u/\mathrm{d}t$. Besides the better performance of the DB-VSI technology compared to conventional SB-VSI solutions, the high DB-VSI power density enables a seamless integration of the inverter into the motor housing [45, 47, 48]. An integrated inverter-compressor example is depicted in **Fig. 6.23**. The integration of the inverter further adds to the DB-VSI con-

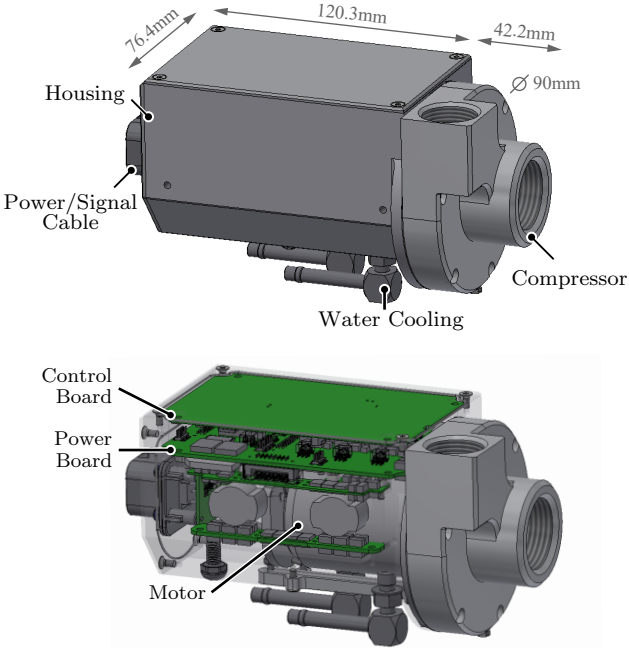


Fig. 6.23: Integrated high-speed 280 krpm compressor/inverter prototype, employing DB-VSI technology and designed by Celeroton AG.

cept advantages: The open-end winding motor is directly attached to the inverter, eliminating the need for cumbersome and costly shielded motor cables. Finally, the inverter integration adds value for the end user, since the latter receives a complete inverter-motor product and is not burdened with the complicated inverter-motor installation.

6.4 Summary

The double-bridge voltage source inverter (DB-VSI) technology is comprehensively analysed in this chapter. A DB-VSI comprises two independent VSIs connected to the opposite sides of an open-end winding motor (without neutral point). This inverter topology is an excellent choice for variable-speed motor drive systems, supplied by a fuel-cell (or a battery). The fuel-cell exhibits a wide DC voltage variation, which must be taken into account for

the inverter stage design. The DB-VSI excellently utilizes its DC input voltage, hence guarantees the full speed/voltage range of the motor, independent of the DC voltage fluctuation of the fuel-cell.

Two DB-VSI inverter variants and/or modulation strategies are comparatively evaluated:

(i) Symmetric modulation strategy of **Fig. 6.6**. This modulation corresponds to the DB_{II}-VSI variant of **Fig. 6.5** and the hardware prototype of **Fig. 6.15**.

(ii) Unfolder modulation strategy of **Fig. 6.9**. This modulation corresponds to the DB_{I}-VSI variant of **Fig. 6.8** and the hardware prototype of **Fig. 6.16**.

Both DB-VSI variants incorporate an AC output filter in order to protect the motor from du/dt originating from the wide-bandgap semiconductor devices' fast switching transitions. A comparison between the two modulation strategies reveals that the unfolder modulation offers exceptionally high performance, in terms of both efficiency and power density, but results in a residual CM voltage on the motor. In contrast, the symmetric modulation lowers the inverter performance to some extent but completely eliminates the motor CM voltage.

Finally, the DB-VSI topology is compared to the state-of-the-art inverter solution of **Fig. 6.4**, which features two energy conversion stages. Compared to the state-of-the-art hardware prototype of **Fig. 6.17**, the DB-VSI technology achieves a performance leap of $\Delta\eta = +2.1\%$ higher efficiency and $\Delta\rho = +118\%$ higher power density.

7 Conclusion

POWER electronics abound within a fuel-cell electric vehicle (FCEV) or a battery electric vehicle (BEV), thus is a key enabling technology for a sustainable transportation [113, 114]. In this thesis, high-speed motor drives, supplied by a fuel-cell, are investigated. In particular, high-speed compressor drives, that provide the required oxygen to a fuel-cell unit (for FCEVs), are analysed. A fundamental understanding of the interface between the inverter and the high-speed motor is provided, and the interdependencies between the inverter and the motor performance are highlighted. Several new inverter solutions and novel modulation strategies are proposed, for the application at hand. The presented concepts/results are general and can be easily extended for systems with different specifications.

7.1 Summary

In the first part of the thesis, low-voltage motor drives, supplied by a constant DC source, are discussed. In this case, a two-level voltage source inverter (VSI) is paired with a high-speed motor. A high switching frequency is used for the inverter pulse width modulation (PWM), in order to guarantee adequate resolution of the fundamental motor voltages/currents. This requirement for high switching frequency is achieved by employing the latest generation of wide-bandgap (WBG) power semiconductor devices. It is recommended to supplement the VSI with a full sine-wave output filter (FSF), that features both differential-mode (DM) and common-mode (CM) attenuation. The output FSF guarantees sinusoidal motor currents/voltages. This is crucial for high-speed motors that are sensitive to poor stator current quality, that induces high rotor losses. The small volume of a high-speed motor,

outweighs the decrease in the inverter performance, originating form the additional volume/losses of the output FSF. Therefore, an output FSF allows to shift volume/losses from the motor to the inverter, thereby improving the performance of the motor drive system as a whole. Furthermore, an output FSF mitigates the high $\mathrm{d}u/\mathrm{d}t$ originating from the fast switching transitions of WBG devices, which would cause insulation stress on the motor and common-mode (CM) bearing currents.

Despite its advantages, the output FSF is a main driver of losses in the inverter stage. In an effort to reduce the additional losses occurring in the output filter, the modulation strategy of the VSI is revisited in **Chapter 2**. The degrees of freedom in the operation of a VSI are explored, and the special characteristics of an output FSF are taken into account. As a result, two new modulation strategies, are proposed and tested on a 330 W inverter prototype, powered by a 48 V DC bus, and driving a 500 krpm electric compressor. The experimental results validate the performance improvements derived from the proposed modulation concepts.

Chapter 3 focuses on the electromagnetic compatibility (EMC) of high-speed motor drives, supplied by a DC source. WBG power semiconductor devices allow for a leap in inverter performance, but require special attention on electromagnetic interference (EMI) aspects. The high switching frequencies of WBG inverters cause EMI problems, since they lie within the regulated conducted EMI emissions frequency range of 150 kHz...30 MHz. Typically, an EMI filter that complies with IEC 61800 standards, is placed at the inverter DC input-side, in order to protect nearby sensitive equipment from EMI emissions. It is shown in this work, that an input filter is not enough and must be supplemented by an FSF at the inverter AC output-side. Besides the several well established benefits of an output FSF, such as purely sinusoidal motor currents and the protection of the motor against high $\mathrm{d}u/\mathrm{d}t$, an FSF at the inverter output-side, also reduces the CM EMI emissions at the inverter DC input-side. Namely, since the inverter housing, the motor housing and the shield of the interconnecting cable are all grounded, CM emissions generated at the inverter output-side are directly mapped to the inverter input-side i.e. there is an input-to-output CM noise interrelation. It is shown that an output FSF reduces the output-side CM EMI emissions and thus mitigates the input-to-output CM noise mutual influence. The proposed input/output filter approach is tested on a 1100 W inverter prototype, powered by an 80 V DC bus, and driving a 280 krpm electric compressor. The EMI measurement results highlight the good performance of the proposed filter concept.

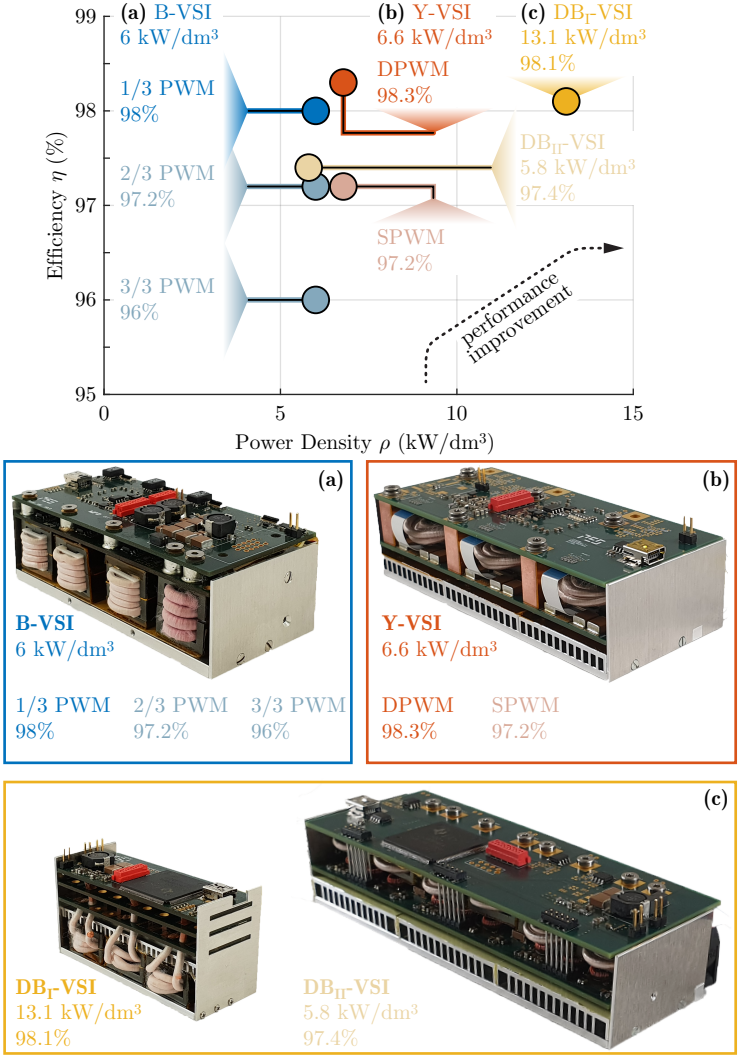


Fig. 7.1: Proposed buck-boost inverter topologies: **(a)** boost VSI (B-VSI), **(b)** Y-inverter (Y-VSI) and **(c)** double-bridge VSI (DB-VSI). The investigated high-speed motor drive application requires a $P = 1100\,\mathrm{W}$ inverter, powered by a $U_\mathrm{i} = 40\,\mathrm{V}...120\,\mathrm{V}$ fuel-cell, in conjunction with a $n = 280\,\mathrm{krpm}$ electric compressor.

In the second part of the thesis, buck-boost inverter topologies are investigated. High-speed motor drive systems supplied by a fuel-cell/battery are especially demanding when it comes to the design of the inverter. Besides a high performance (high efficiency η and power density ρ), the inverter has to cope with the wide DC voltage variation of the fuel-cell/battery. The inverter has to always guarantee the full speed range of the motor, independent of the DC input voltage fluctuation, i.e. the inverter must be able to generate the nominal motor voltage, which is proportional to the motor speed. Several novel buck-boost inverter solutions are proposed in this thesis, within the context of a high-speed motor drive. The application at hand requires a $P = 1100\,\mathrm{W}$ inverter, powered by a $U_\mathrm{i} = 40\,\mathrm{V}...120\,\mathrm{V}$ fuel-cell, in conjunction with a $n = 280\,\mathrm{krpm}$ electric compressor. The proposed inverter concepts and their respective performance are summarized in **Fig. 7.1**.

In **Chapter 4**, a conventional buck-boost inverter topology is examined, which features two energy conversion stages. There, a dedicated boost-type DC/DC stage first adapts the fuel-cell voltage (if necessary) and subsequently supplies a buck-type DC/AC stage. This inverter solution is denoted as boost-VSI (B-VSI) and is shown in **Fig. 7.1(a)**. The B-VSI results in a low efficiency and a relatively low power density, due to the additional losses/volume originating from the DC/DC stage. A new modulation strategy that synergetically combines the operation of the DC/DC stage and the DC/AC stage is proposed. It is thereafter possible to significantly increase the inverter efficiency (by 2% in the best case), compared to a conventional modulation. This new modulation strategy is particularly interesting, since it can be applied on already installed/operational motor drives, as a simple firmware update.

Subsequently in **Chapter 5**, innovation on the inverter topology is pursued. A promising inverter topology, denoted as Y-VSI, is proposed, based on the idea of modular three-phase systems. This inverter topology achieves buck-boost capability by using only a single energy conversion stage in contrast to the two-stage B-VSI. The modulation possibilities of the Y-VSI are explored and as a result two modulation strategies are proposed. Based on the theoretical analysis, the Y-VSI hardware prototype of **Fig. 7.1(b)** is assembled, which outperforms the conventional B-VSI (power density $\Delta\rho = +10\%$, efficiency $\Delta\eta = +2.3\%$, in the best case).

In an effort to further improve the motor drive performance as a whole, inverter innovation is combined with motor innovation, in **Chapter 6**. As a result, the double-bridge inverter technology (DB-VSI) technology is proposed. A DB-VSI comprises two VSIs, connected to the opposite sides of an open-end winding motor (no floating neutral point). After exploring all the

possibilities of the operation of a DB-VSI, two hardware demonstrators are assembled (cf. **Fig. 7.1(c)**). The performance of this inverter-motor combination greatly surpasses the previously described solutions (compared to the B-VSI, power density $\Delta\rho$ = +118%, efficiency $\Delta\eta$ = +2.1%, in the best case). The excellent performance of DB-VSI technology underlines the main message of this work, that motor drives benefit the most from simultaneous innovation in the inverter and the motor. Finally, an integrated motor drive (IMD) is assembled by the industry partner of this thesis research project (Celeroton AG), where a DB-VSI inverter and a high-speed compressor are placed in the same housing.

7.2 Outlook & Future Research

In this thesis, motor drive systems, supplied by a DC source are comprehensively analysed. Several inverter topologies are evaluated in terms of efficiency and power density, by means of multi-objective optimization tools. It is shown, that only a high inverter performance is not enough. Recent developments in the power electronics market require from inverters to offer additional features/functionalities:

(i) **High-frequency sinusoidal output voltages/currents.** High-speed motor technology is gaining importance in commercial applications, thanks to its low volume/weight. Hence, inverters must support high motor fundamental frequencies. In addition, the inverter must guarantee sinusoidal output currents, that high-speed motors require.

(ii) **Electromagnetic compatibility (EMC).** The inverter is part of a larger system, thus EMC is a key requirement that ensures uninterrupted system operation.

(iii) **Buck-boost functionality.** The DC voltage variation of fuel-cells/batteries, that usually supply the motor drive, demands inverters with buck-boost capability.

This demand for additional inverter features often contradicts the pursuit of high efficiency and power density and leaves ample room for further innovation.

Efficiency and power density are two key performance vectors for inverter systems in motor drives, but are not the only ones. In order to bridge

the gap between academic research and commercial applications the reliability, fault tolerance and cost of the inverter system must be assessed. Furthermore, the long lifetime of motor drives mandates a life cycle cost analysis. It is important to take into consideration the life cycle energy costs, instead of only the initial procurement cost of a motor drive product [157,158]. Such cost analysis, justifies the cost premium of advanced inverter/motor solutions, and illuminates areas worthy of further investment.

In the last part of the thesis an integrated inverter/motor prototype was presented, that underlined the advantages of a high integration level. In particular, an IMD benefits from a compact design, eliminates expensive motor cables and adds value for the end user, who is not any more burdened with the complicated motor drive installation. Despite the profound advantages of an IMD, this technology has not yet found wide acceptance in commercial applications. Further research and technological advancements are needed, in order to allow for commercial success of IMDs: First, the reliability of inverters must be improved in order to match the robustness of motors [47,159]. The placement of the inverter in the high-temperature, high-vibration environment of the electric machine, further intensifies reliability concerns. Currently, semiconductor devices, packaging, PCB and capacitors constitute reliability bottlenecks [160–162].

Contemporary IMDs are closely related to the application. Thereby, it is difficult to produce the same IMD in large numbers and benefit from economies of scale. As a result, IMDs only appear in niche applications, that put a high premium on low volume/weight and largely disregard costs (e.g. compressors for FCEVs). In order to overcome this market adoption barrier, inverter innovation must be coupled with motor innovation. In particular, integrated modular motor drive technology (IMMD) presents new opportunities for motor drives [163–165]. In an IMMD, the motor winding is broken down into winding modules (poles), each one of which is controlled by an independent inverter module. Each inverter/winding module constitutes an easily reproducible building block. Thereby, IMMDs could solve the market scalability problem of contemporary IMDs. Simultaneously, the modular nature of IMMDs inherently enables high fault tolerance, which to certain extend resolves the reliability problems of IMDs.

In the future, the design of the motor and the inverter will inevitably converge. The speed of this technology advancement depends on the capability of the power electronics community to address the highly multidisciplinary technical problems that lie ahead. In order to break the performance barriers, a power electronics engineer should master several scientific fields, besides

the traditional power electronics discipline. Expertise in motors design, thermal management and mechanical systems is a necessary side-condition for progress in motor drives.

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Curriculum Vitae

Personal Information

Name	Michael Antivachis
Date of birth	August 19, 1991
Place of Birth	Athens, Greece
Citizen of	Greece
Contact	antivachis@lem.ee.ethz.ch
	+41 44 632 64 94

Education

2016 – 2020	Doctorate, Power Electronic Systems Laboratory (PES) Swiss Federal Institute of Technology (ETH Zurich)
2014 – 2016	MSc, Master in Energy Science and Technology (MEST) Swiss Federal Institute of Technology (ETH Zurich) Distinction: Silver Medal of ETH Zurich
2009 – 2014	MSc / BSc, Diploma in Electrical and Computer Engineering National Technical University of Athens (NTUA)
2006 – 2009	High School Diploma Lycee Leonin Athens

Work Experience

2014 – 2020	Scientific Assistant, Power Electronic Systems Laboratory (PES) Swiss Federal Institute of Technology (ETH Zurich)
2013 – 2013	Power Systems Engineer (Internship) Public Power Corporation - Renewables (PPC-R), Athens