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Motor-Integrated Power Factor Corrected Single-to-Three-Phase AC/AC Converter Concepts

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For my family.

Für meine Familie.

Doing what you like is freedom.
Liking what you do is happiness.
FRANK TYGER

Lernen ist wie Rudern gegen den Strom.
Sobald man aufhört, treibt man zurück.
CHINESISCHES SPRICHWORT

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Michael Haider
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Abstract

WITH an increasing demand for transportation and the concurrent requirement for decarbonization, implementing an efficient, low emitting, and sustainable transportation sector is essential. In this context, railway-based transportation has been identified as the cleanest and the greenest high-volume transport mode. Thus, it has a vital role in creating a sustainable lifestyle and economy as it is frugal by design. However, further improvements are still required for next-generation systems within the railway sector, from the energy supply and distribution over the drivetrain down to the auxiliaries. Hence, the industry sector defines the requirements of commercial electrical and electro-mechanical auxiliary power conversion systems for the rolling stock as compact, lightweight, highly efficient, reliable, and redundant. For this reason, the latter is typically equipped with a Variable Speed Drive (VSD) system for the energy-efficient operation of compressors, pumps, fans, and blowers.

The main goal of this thesis is to explore conceptual and technological improvements for such auxiliary drive systems in railway vehicles. In particular, the focus is on the pressurized air supply system implemented by onboard compressor units. Those are required to charge the pressure tank, which supplies, e.g. the air brake and door control systems, and are operated from a tertiary winding of the single-phase traction transformer. However, air pressure is also required to raise the pantograph and electrically connect the railway vehicle to the overhead line. Thus, operation from an onboard battery is demanded during the startup. Consequently, the application needs a power electronic system to convert the single-phase AC — or DC, under battery operation — input voltage into a symmetrical three-phase voltage system with adjustable amplitude and frequency to control the motor speed. In addition, unity power factor grid operation has to be achieved in AC mode. The main target is to maximize the power density for the space- and weight-constrained mobility application.

The state-of-the-art implementation of a single-phase-supplied VSD system features a two-stage approach comprising a front-end Power Factor Correction (PFC) rectifier and an output-side Voltage Source Inverter (VSI). The instantaneous power mismatch between the pulsating input power, due to PFC operation, and the constant mechanical output power is covered by a large DC-link capacitance, restricting their practical implementation to electrolytic capacitors. However, electrolytic capacitors significantly limit the converter lifetime, which becomes even more of a concern at elevated op-

erating temperatures, thus preventing the desired motor integration required for ultra-high power density.

With the aim of avoiding electrolytic capacitors and any other kind of active power pulsation buffer circuitry, the only remaining option is to forward the pulsating input power directly to the motor. An approach introduced in this thesis as Motor-Integrated Power Pulsation Buffer (MPPB) concept, where the kinetic energy storage of the drivetrain, i.e. the motor (and load) inertia, is employed as Power Pulsation Buffer (PPB). The kinetically stored energy is typically at least one order of magnitude above the grid energy fluctuation due to PFC operation, leading to a comparably small speed ripple similar to single-phase motors.

The MPPB concept is first applied to a conventional two-stage approach. The proposed control structure ensures the desired average speed and sinusoidal input current for unity power factor operation. Further adaptions are proposed to facilitate improved operation without significant energy storage within the electrical system during abnormal supply conditions such as grid interruptions. A 7.5 kW, motor-integrated All-SiC hardware demonstrator validates the proposed MPPB concept and control, achieving a total boxed volume of only 8.2 L for the drive system (incl. the motor), which corresponds to a power density of 0.91 kW/L (15 W/in^3) including the EMI filter. The inverter bridge-leg power semiconductors feature an adapted gate drive configuration to slow down the $\mathrm{d}v/\mathrm{d}t$ of switching voltage transitions — with minimal effect on the remaining switching transitions — to prevent harm to the motor insulation. The introduced loss models are verified over the full torque range, revealing a nominal grid-to-motor-shaft efficiency of 91.4 %, which corresponds to 703 W of system losses and qualifies the converter for the highest efficiency class IES2 of EN50598-2 covering complete drive systems. For all loads over 5 kW or 66 % of nominal load the grid-to-motor-shaft efficiency remains above 90 %. Compared to the conventional implementation, a worst-case loss penalty of 17 % or 100 W occurs at nominal operation, while the averaged losses (over the full torque range) increase only from 447 W to 491 W, or by 9.8 %.

In a second step, the MPPB concept is applied to a dual-inverter topology with a three-phase Open-End Winding (OEW) motor. This approach allows to omit the boost-stage, including the High-Frequency (HF) bridge-legs and the boost inductors, reducing the system volume and lowering the realization effort. The operating principle, including the desired motor voltage division strategy to achieve the voltage set points for both VSIs under the defined control objectives, is thoroughly investigated. The detailed system analysis

reveals that the motor voltage can be selected independently of the grid peak voltage, in contrast to existing single-phase supplied dual-inverter concepts. The converter performance is evaluated concerning this degree of freedom, revealing a semiconductor loss reduction of 30 % compared to a state-of-the-art approach.

Kurzfassung

ANGESICHTS der steigenden Nachfrage nach Personen- und Warenbeförderung und der gleichzeitigen Forderung nach Dekarbonisierung, ist die Entwicklung eines effizienten, emissionsarmen und nachhaltigen Verkehrswesens von entscheidender Bedeutung. In diesem Zusammenhang hat sich der Schienenverkehr als der emissionstechnisch sauberste und daher umweltfreundlichste Verkehrsträger im Massentransport erwiesen und spielt damit eine entscheidende Rolle bei der Schaffung einer nachhaltigen Wirtschaft und eines nachhaltigen Lebensstils. Dennoch sind weitere Verbesserungen für Systeme der nächsten Generation des Eisenbahnsektors erforderlich, von der Energieversorgung und -verteilung über den Antriebsstrang bis hin zu den Hilfsbetrieben. Die Industrie definiert daher die Anforderungen an kommerzielle elektrische und elektromechanische Energieumwandlungssysteme für Schienenfahrzeuge als kompakt, leicht, hocheffizient, zuverlässig und redundant. Aus diesem Grund sind letztere in der Regel mit einem drehzahlvariablen Antriebssystem für den energieeffizienten Betrieb von Kompressoren, Pumpen, Lüftern und Gebläsen ausgestattet.

Das Hauptziel dieser Arbeit ist die Erforschung konzeptioneller und technologischer Verbesserungen für Hilfsbetriebe in Schienenfahrzeugen. Der Fokus liegt dabei insbesondere auf dem Druckluftsystem, welches durch bordseitige Kompressoranlagen realisiert wird. Diese werden über die Tertiärwicklung des Einphasen-Traktionstransformators versorgt und zur Aufladung des Druckbehälters benötigt, welcher z.B. die Druckluftbrems- und Türsteuerungssysteme speist. Druckluft wird jedoch auch benötigt, um den Stromabnehmer anzuheben und das Schienenfahrzeug elektrisch mit der Oberleitung zu verbinden. Während dem Aufstarrten des Fahrzeugs erfolgt die Energieversorgung des Druckluftsystems mittels einer Bordbatterie. Folglich benötigt die Antriebsapplikation ein leistungselektronisches System zur Umwandlung der einphasigen Wechselspannung - oder Gleichspannung bei Batteriebetrieb - in ein symmetrisches dreiphasiges Spannungssystem mit einstellbarer Amplitude und Frequenz, zur Regelung der Motordrehzahl. Darüber hinaus muss im Wechselstrombetrieb der Eingangsstrom in Phase zur Netzspannung liegen um Netzrückwirkungen zu minimieren. Das Hauptziel ist die Maximierung der Leistungsdichte für die Anwendung im genannten platz- und gewichtsbeschränkten Mobilitätssektor.

Der Stand der Technik für ein einphasig gespeistes Antriebssystem ist eine zweistufige Umrichtertopologie, welche einen aktiven Gleichrichter mit Leistungsfaktorkorrektur am Eingang und einen dreiphasigen Wechselrichter am Ausgang umfasst. Die momentane Leistungsabweichung zwischen der pul-

sierenden Eingangsleistung aufgrund des ohmschen Netzverhaltens und der konstanten mechanischen Ausgangsleistung wird durch eine große Zwischenkreiskapazität gedeckt, deren praktische Implementierung dank ihrer hohen Energiedichte auf Elektrolytkondensatoren beschränkt ist. Elektrolytkondensatoren schränken jedoch die Lebensdauer des Umrichtersystems wesentlich, ein Effekt, welcher sich bei erhöhten Betriebstemperaturen weiter ausprägt, und so die gewünschte Motorintegration, welche für die Maximierung der Leistungsdichte erforderlich ist, verhindert. Mit dem Ziel Elektrolytkondensatoren sowie jede andere Art aktiver Leistungspufferschaltungen zu vermeiden, bleibt nur die Möglichkeit, die pulsierende Eingangsleistung direkt an den Motor weiterzuleiten. Ein in dieser Arbeit vorgestellter Ansatz ist das Konzept des motorintegrierten Leistungspulsationspuffers, bei dem die kinetische Energiespeicherung des Antriebsstrangs, also die Massenträgheit des Motors (und der mechanischen Last), als Leistungspulsationspuffer verwendet wird. Die kinetisch gespeicherte Energie liegt typischerweise um mindestens eine Größenordnung über der durch den aktiven Gleichrichterbetrieb mit Leistungsfaktorkorrektur bedingten Schwankung der netzseitig bezogenen Energie, und führt zu einer vergleichsweise geringen Drehzahlwelligkeit an der Motorwelle, ähnlich wie sie bei Einphasenmotoren auftritt.

Das Konzept des motorintegrierten Leistungspulsationspuffers wird zunächst auf eine herkömmliche zweistufige Umrichtertopologie angewandt. Die vorgeschlagene Regelungsstruktur gewährleistet die gewünschte Durchschnittsgeschwindigkeit und einen sinusförmigen Eingangsstrom bzw. Leistungsfaktorkorrektur. Weitere Anpassungen werden vorgeschlagen, um einen verbesserten Betrieb ohne nennenswerte Energiespeicherung innerhalb des elektrischen Systems bei abnormalen Versorgungsbedingungen, wie z.B. Netzunterbrechnungen, zu ermöglichen. Ein 7.5 kW motorintegrierter All-SiC-Hardware-Demonstrator verifiziert das vorgeschlagene Konzept des motorintegrierten Leistungspulsationspuffers inklusive Regelung und erreicht ein Gesamtvolumen von nur 8.2 L für das gesamte Antriebssystem (einschließlich dem Motor und dem EMI-Eingangsfilter), was einer Leistungsdichte von 0.91 kW/L (15 W/in^3) entspricht. Die Leistungshalbleiter des dreiphasigen Wechselrichters verfügen über eine angepasste Gate-Treiberschaltung zur Verlangsamung der Schalttransienten der Wechselrichterausgangsspannung — mit minimaler Auswirkung auf den verbleibenden Schaltvorgang — um eine Schädigung der Motorisolation zu vermeiden. Die eingeführten Verlustmodelle werden über den gesamten Drehmomentbereich verifiziert und ergeben einen nominellen Wirkungsgrad zwischen Netz und Motorwelle von 91.4 %, was 703 W an Systemverlusten entspricht, und das Antriebssystem für die

höchste Effizienzklasse IES2 der EN50598-2 qualifiziert. Bei allen Lasten über 5 kW oder 66 % der Nennlast bleibt der Wirkungsgrad zwischen Netz und Motorwelle über 90 %. Im Vergleich zur konventionellen Implementierung ergeben sich bei Nennbetrieb Zusatzverluste von maximal 17 % oder 100 W, während die gemittelten Verluste (über den gesamten Drehmomentbereich) um lediglich 44 W bzw. um 9.8 % zunehmen.

In einem zweiten Schritt wird das Konzept des motorintegrierten Leistungspulsationspuffers auf eine Doppel-Wechselrichter-Topologie mit einem dreiphasigen Motor mit offenen Statorphasenwicklungen angewendet. Dieser Ansatz erlaubt es, die Hochsethsteller-Stufe bzw. deren phasenversetzt getakteten Halbbrücken und die Induktivitäten zu eliminieren, wodurch das Systemvolumen reduziert und der Realisierungsaufwand verringert wird. Das Funktionsprinzip, einschließlich der gewünschten Aufteilung der Motorspannung zwischen den beiden Wechselrichtern, und die Einhaltung der definierten Regelungsziele werden eingehend untersucht. Die detaillierte Systemanalyse zeigt, dass die Motorspannung unabhängig von der Netzspitzenspannung gewählt werden kann, im Gegensatz zu bestehenden einphasig gespeisten Doppel-Wechselrichter-Topologien mit Elektrolytkondensatoren. Die Bewertung der Umrichterverluste hinsichtlich dieses Freiheitsgrades zeigt eine mögliche Reduzierung der Halbleiterverluste um 30 % im Vergleich zum Stand der Technik.

Abbreviations

AC	Alternating Current
CAGR	Compound Annual Growth Rate
CCM	Continuous Current Mode
CM	Common-Mode
CSC	Current Source Converter
CSPI	Cooling System Performance Index
DC	Direct Current
DM	Differential-Mode
DPT	Double-Pulse Test
DRC	Diode-Resistor-Capacitor
DUT	Device-Under-Test
EMC	Electromagnetic Compatibility
EMF	Electromotive Force
EMI	Electromagnetic Interference
FC	Flying Capacitor
FOM	Fiugre-of-Merit
GaN	Gallium Nitride
GHG	Green House Gas
HF	High-Frequency
IGBT	Insulated Gate Bipolar Transistor
MAF	Moving-Average Filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPB	Motor-Integrated Power Pulsation Buffer
OEW	Open-End Winding
PCB	Printed Circuit Board
PFC	Power Factor Correction
PLL	Phase-Locked Loop
PMSM	Permanent Magnet Synchronous Motor
PPB	Power Pulsation Buffer
PV	Photovoltaics
PWM	Pulse-Width Modulation
Q2L	Quasi-Two-Level
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SOGI	Second-Order Generalized Integrator
SWER	Single-Wire Earth Return

THD	Total Harmonic Distortion
UIC	Union International Railways
VSD	Variable Speed Drive
VSI	Voltage Source Inverter
WBG	Wide-Bandgap
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

List of Symbols

C_1, C_2	DM-filter capacitors / capacitances
C_{CM0}	CM-motor capacitance
C_{CM1}, C_{CM2}	CM-filter capacitors / capacitances
C_{DC}	DC-link capacitor / capacitance
C_{DC1}, C_{DC2}	Primary, secondary DC-link capacitor / capacitance
C_{DS}	MOSFET drain-source capacitance
$C_{\mathrm{dQ,oss}}$	Charge-equivalent output capacitance
C_{eff}	Effective switch-node capacitance
C_{EMI}	EMI-filter capacitance
C_{GD}	MOSFET gate-drain capacitance
C_{GS}	MOSFET gate-source capacitance
C_{M}	Miller capacitance
C_{o}	Output-filter capacitance
c_{oss}	Differential MOSFET output capacitance
C_{oss}	MOSFET output capacitance
C_{par}	Parasitic switch-node capacitance
cl, CL	Closed-loop transfer functions
CSPI	Cooling System Performance Index
D_1, D_2, D_3, D_4	Bridge rectifier diodes
d_{1a}, d_{1b}, d_{1c}	Primary inverter duty-cycles
d_{2a}, d_{2b}, d_{2c}	Secondary inverter duty-cycles
d_{a}, d_{b}, d_{c}	Inverter duty-cycles
d_{B}	Boost duty-cycle
$\mathrm{d}v/\mathrm{d}t$	Motor terminal voltage slope
$\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$	Switch-node voltage slope
E_0	Resonant charging-discharging C_{oss}-losses of a MOSFET
e_{KIN}	Kinetic energy of the drivetrain
e_{Lq}	Magnetic energy of the q-axis motor inductance
e_{sw}, E_{sw}	Switching energy loss
$E_{\mathrm{sw,off}}$, $E_{\mathrm{sw,on}}$	Switching energy loss during turn-off / turn-on transition
f	Frequency
f_{BW}	Bandwidth
f_{CO}	Crossover frequency
f_{E}	Electrical motor frequency
f_{Emin}	Minimum electrical motor frequency in stationary operation with constant torque

f_{EQ}	Cutoff-frequency of a time-delay-equivalent low-pass filter
f_G	Grid frequency
f_i, f_{ii}, f_{iii}	Frequencies of harmonic motor current components
f_{Isw}	Inverter switching frequency
f_P	Power pulsation frequency
f_{PI}	Cutoff-frequency of a PI-controller
f_{PLL}	PLL frequency
G_D	Transfer function: time delay
G_{EQ}	Transfer function: time-delay-equivalent low-pass filter
G_F	Transfer function: filter
G_I	Transfer function: integrator
g_m	MOSFET transconductance
G_{PI}	Transfer function: PI-controller
I_0	Reference motor current space vector magnitude
I_B	Battery current
i_C	Instantaneous DC-link capacitor current
$\hat{I}_C$	DC-link capacitor current amplitude
$I_{C,LFrms}$	Low-frequency RMS DC-link capacitor current
i_{C2}	Instantaneous secondary DC-link capacitor current
i_{ch}	Instantaneous MOSFET channel current
I_{Davg}	Diode average current
i_{DC1}, i_{DC2}	Primary, secondary instantaneous DC-link current
I_{Drms}	Diode RMS current
i_G	Instantaneous grid current
$\hat{I}_G$	Grid current amplitude
$\hat{I}_{Gmax}$	Maximum grid current amplitude
i_I, I_I	Input current
I_k	Kink current
i_L	Instantaneous boost inductor current
i_L	Load current
$\underline{i}_M$	Motor current in space vector representation
$\hat{i}_M$, $\hat{I}_M$	Motor phase current amplitude
I_{M0}	Motor current space vector magnitude in conventional operation
i_{Ma}, i_{Mb}, i_{Mc}	Instantaneous motor phase currents
$I_{Ma,avg}$	Absolute global average current of motor phase a
$\hat{I}_{Ma,i}$, $\hat{I}_{Ma,ii}$, $\hat{I}_{Ma,iii}$	Amplitudes of the motor current harmonics in MPPB operation

i_{Md}	Instantaneous d-axis motor current
i_{Mlim}	Limited motor current amplitude
I_{Mmax}	Maximum motor current amplitude
i_{Mq}, I_{Mq}	Instantaneous / average q-axis motor current
i_{off}, I_{off}	Turn-off current
i_{on}, I_{on}	Turn-on current
$I_{\mathrm{PHa,rms}}$	RMS phase current in phase a
I_{PHavg}, I_{PH0avg}	Absolute average phase current for MPPB / conventional operation
I_{PHpk}, I_{PH0pk}	Peak phase current for MPPB / conventional operation
I_{PHqrms}	RMS q-current
I_{PHrms}, I_{PH0rms}	RMS phase current for MPPB / conventional operation
I_{sw}	Switched current
i_{T}	Switched transistor current
I_{Tavg}	Transistor average current
I_{Trms}	Transistor RMS current
j	Index variable
J_{M}	Motor inertia
J_{TOT}	Drivetrain inertia
k	Load torque exponent
k_0, k_1, k_2	Switching loss coefficients
k_{off}, k_{on}	Switching loss coefficient for turn-off / turn-on
k_{p}	Proportional controller gain
k_{T}	Torque constant
k_{V}	Voltage constant
L_{B}	Boost inductor
L_{CM0}, L_{CM1}, L_{CM2}	CM-filter inductors / inductances
L_{d}	d-axis motor inductance
L_{DM}	DM-filter inductor / inductance
L_{EMI}	EMI-filter inductance
L_{o}	Output-filter inductance
L_{q}	q-axis motor inductance
m	Index variable
M	Modulation index of the inverter
M_{I}	Modulation index of the primary inverter
M_{max}	Maximum modulation index
n	Instantaneous motor speed
ol , OL	Open-loop transfer functions
$\mathrm{ON}_{\mathrm{INV}}$	Inverter operating state (on/off)

ON_{PFC}	PFC rectifier operating state (on/off)
p	Number of pole pairs
P_0	Mechanical power
P_{0DC}	Mechanical power in DC-operation
p_1, p_2	Air pressures
p_1, p_2	Instantaneous primary / secondary inverter power
p_C, P_C	Instantaneous / average capacitor power
$\bar{p}_C$	Global average of capacitor power
p_{C2}, P_{C2}	Instantaneous / average secondary capacitor power
$\bar{p}_{C2}$	Global average of secondary capacitor power
p_G, P_G	Instantaneous / average grid power
$\tilde{p}_G$	AC component of the grid power
P_I	Average input power
p_{INV}, P_{INV}	Instantaneous / average inverter power
p_{Lq}	Instantaneous q-axis magnetization power
$\bar{p}_{Lq}$	Global average of q-axis magnetization power
p_M, P_M	Instantaneous / average motor power
p_{PFC}	Instantaneous PFC rectifier power
P_{VC}	Capacitive filter losses
P_{VDS}	Drive system losses
P_{VEL}	Losses of the electronic circuitry
P_{VHB}	Half-bridge losses
$P_{VHBcond}$	Half-bridge conduction losses
P_{VHBsw}	Half-bridge switching losses
P_{VI}, P_{VI0}	Inverter losses for MPPB / conventional operation
P_{VIcond}	Inverter conduction losses
$P_{VIdiode}$	Inverter diode conduction losses
$P_{VIfet,i}$, $P_{VI0fet,i}$	Losses of MOSFET inverter with dv/dt limitation of switching transitions for MPPB / conventional operation
$P_{VIfet,ii}$, $P_{VI0fet,ii}$	Losses of MOSFET inverter with output filter for MPPB / conventional operation
P_{VIigbt}, $P_{VI0igbt}$	Losses of IGBT inverter for MPPB / conventional operation
P_{VIsw}	Inverter switching losses
P_{VM}, P_{VM0}	Motor losses for MPPB / conventional operation
p_{VMa}, p_{VMb}, p_{VMc}	Local average of motor phase winding losses
P_{VMa}, P_{VMb}, P_{VMc}	Global average of motor phase winding losses
P_{VMcap}	Capacitive motor losses

P_{VMcond}	Motor winding conduction losses
P_{VMnl}	No-load motor losses
P_{VPH}, P_{VPH0}	Average phase conduction losses for MPPB / conventional operation
P_{VPHmax}	Maximum phase losses
P_{VR}	Rectifier losses
P_{VRemi}	EMI filter losses
P_{VRhb}	Rectifier half-bridge losses
P_{VRind}	Rectifier inductor losses
P_{VRun}	Unfolder losses
PM	Phase margin
Q_{G0}	Gate charge related to the Miller plateau
Q_{oss}	MOSFET output capacitance charge
Q_{tot}	Total switch-node capacitance charge
$R_{\mathrm{DS,on}}$	Drain-source resistance of a MOSFET
R_{G}	Gate resistor
$R_{\mathrm{G,on}}$, $R_{\mathrm{G,off}}$	Gate turn-on / turn-off resistor
R_{HS}	Thermal resistance of the heatsink
R_{int}	MOSFET internal gate resistance
R_{on}	(Differential) on-resistance
R_{s}	Stator winding resistance
s	Laplace variable
S_{UN}	Unfolder switching state
t,	Time
T,	Period of a signal
$\mathrm{T_a}$, $\mathrm{T_b}$, $\mathrm{T_c}$	Transistors of the inverter
T_{A}	Acceleration torque
T_{C}	Control computation time
T_{D}	Time delay
t_{f}, t_{f0}	Fall time
T_{FFL}	Feedforward load torque
T_{G}	Grid period
$\mathrm{T_h}$	High-side switch
$\mathrm{T_i}$, $\mathrm{T_{ii}}$, $\mathrm{T_{iii}}$	Transistors of the PFC rectifier
T_{Isw}	Inverter switching period
$\mathrm{T_l}$	Low-side switch
T_{L}	Load torque
t_{M}, T_{M}	Instantaneous, average motor torque
T_{MAF}	MAF-filter averaging time

T_{Mnl}	No-load motor torque
T_{P}	Power pulsation period
T_{PWM}	PWM period
t_{r}, t_{r0}	Rise time
$\mathrm{T_u}$	Transistors of the unfolder
V_0	Reference motor voltage space vector magnitude
$v_{0\mathrm{q}}$	Approximated q-axis voltage
$\dot{V}_1$	Air flow rate
$\underline{v}_1$	Primary inverter voltage in space vector representation
$\hat{V}_1$	Primary inverter phase voltage amplitude
$v_{1\mathrm{d}}$	Primary inverter voltage in d-representation
$v_{1\mathrm{lim}}$	Limited primary inverter voltage amplitude
$v_{1\mathrm{max}}$	Maximum primary inverter voltage amplitude
$v_{1\mathrm{q}}$	Primary inverter voltage in q-representation
$\dot{V}_2$	Air flow rate
$\underline{v}_2$	Secondary inverter voltage in space vector representation
$v_{2\mathrm{d}}$	Secondary inverter voltage in d-representation
$v_{2\mathrm{max}}$	Maximum secondary inverter voltage amplitude
$v_{2\mathrm{q}}$	Secondary inverter voltage in q-representation
v_α, v_β	Components of the orthogonal $\alpha\beta$–voltage system
V_{B}	Battery voltage
v_{DC}, V_{DC}	Instantaneous / average DC-link voltage
$\bar{v}_{\mathrm{DC}}$	Filtered DC-link voltage
v_{DC1}	Primary instantaneous DC-link voltage
v_{DC2}, V_{DC2}	Secondary instantaneous / average DC-link voltage
$\bar{v}_{\mathrm{DC2}}$	Filtered secondary DC-link voltage
v_{Dd}	d-decoupling term
v_{Dq}	q-decoupling term
v_{DS}	MOSFET drain-source voltage
V_{f}	Forward voltage drop
v_{G}, V_{G}	Grid voltage
$\hat{V}_{\mathrm{G}}$	Grid voltage amplitude
$V_{\mathrm{G,off}}$, $V_{\mathrm{G,on}}$	Negative and positive gate driver voltage
V_{Gmax}	Maximum grid voltage
V_{Gmin}	Minimum grid voltage
v_{GS}	MOSFET gate-source voltage
$v_{\mathrm{GS,i}}$	MOSFET internal gate-source voltage
v_{I}, V_{I}	Input voltage
v_{LB}	Instantaneous boost inductor voltage

v_{Ld}	Motor inductance d-axis voltage
v_{LISN}	Measured HF noise voltage
v_{Lq}	Motor inductance q-axis voltage
$\underline{v}_{\mathrm{M}}$	Motor voltage in space vector representation
v_{M}	Miller voltage
v_{Md}	Motor d-axis voltage component
v_{Mq}	Motor q-axis voltage component
v_{noise}	Noise voltage
V_{P}	Voltage induced by the revolving rotor field
v_{pk}	Voltage peak derived by SOGI
v_{T}	Switched transistor voltage
v_{th}	Threshold voltage
$\mathrm{Vol}_{\mathrm{DS}}$	Drive system volume
$\mathrm{Vol}_{\mathrm{HS}}$	Heatsink volume
α	Auxiliary variable
δ	Control error
Δn	Motor speed ripple amplitude
ΔT	Time-shift
Δv_{C}	Capacitor voltage ripple amplitude
Δv_{DC}	DC-link voltage ripple amplitude
$\Delta\omega$	Motor speed ripple amplitude
ε, ε_0	Mechanical rotor angles
η	Efficiency
$\eta_{\mathrm{CS,MPPB}}$, $\eta_{\mathrm{CS,CONV}}$	Converter system efficiency for MPPB operation / conventional operation
$\eta_{\mathrm{DS,MPPB}}$, $\eta_{\mathrm{DS,CONV}}$	Drive system efficiency for MPPB operation / conventional operation
$\eta_{\mathrm{M,MPPB}}$, $\eta_{\mathrm{M,CONV}}$	Motor efficiency for MPPB operation / conventional operation
θ	PLL-based grid angle
ϑ_{AMB}	Ambient temperature
ϑ_{HS}	Heatsink temperature
ϑ_{J}	Junction temperature
ρ_{avg}, $\rho_{0\mathrm{avg}}$	Sum of the average currents for MPPB / conventional operation
ρ_{rms}, $\rho_{0\mathrm{rms}}$	Sum of the squared RMS currents for MPPB / conventional operation
ς, ς_0	Sum of the averaged products of switched transistor voltage and current for MPPB / conventional operation

τ_{D}	Delay time constant
τ_{EQ}	Equivalent delay time constant
τ_{F}	Filter time constant
τ_{i}	Integral controller gain
τ_{I}	Integrator time constant
τ_{n}	Integral controller gain
τ_{off}	Fitting time constant
τ_{on}	Fitting time constant
τ_{th}	Thermal time constant
φ	Phase-shift
Ψ_{PM}	Permanent magnet flux
ω	Instantaneous angular motor speed
$\bar{\omega}$	Average angular motor speed
ω_{CO}	Angular crossover frequency
ω_{i}	Integral controller gain
$\bar{\omega}_{\mathrm{min}}$	Minimum average angular motor speed in stationary operation with constant torque
ω_{P}	Angular power pulsation frequency

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1 Introduction

Mobility is one of the most fundamental aspects within a globalized world, with an ever increasing need for people and freight to quickly move from one place to the other [1]. The transportation sector provides solutions to these needs and represents a commercial activity deriving its benefits from operational characteristics such as costs, capacity, efficiency, reliability, and speed. Fulfilling these properties has positive impacts on the society [2] and the economy [3], as it allows for better accessibility of employment and markets. Unfortunately, the transportation sector also causes congestion, accidents, and has a substantial environmental impact.

With the growing demand for mobility, these impacts are more frequently linked to environmental problems in air, water, and soil quality, acoustic noise, biodiversity, land consumption, and climate change [4], which are all unfavorable for humanity and nature. Many of these problems originate from burning fossil fuels for road vehicles, ships, trains, and airplanes. Transportation accounted for 14 % of all Green House Gas (GHG) emissions in 2018. The western world is even above average, as mobility accounts for 25 % [5] and 29 % [6] of Europe's and US's total GHG emissions, respectively, contradicting any GHG reduction targets. State-of-the-art mobility is clearly in contrast with the sustainable development goals defined by the United Nations [7], which can be interpreted as a "blueprint to achieve a better and more sustainable future for all".

The demand for transportation is expected to double by 2050 [8], while decarbonization has to be achieved in the same time frame to limit the consequences of global warming [9]. Facing these challenges, implementing an efficient, low emitting, and sustainable transportation sector is highly crucial.

Railways are the most promising approach in this regards. Trains carry already 8 % of the world's motorized passenger movements and 7 % of freight transport, but account for only 2 % of energy use within the transportation sector [10] and allow for the utilization of diverse energy sources, still, with a firm reliance on electrical energy, as three-quarters of passenger movements, and half of freight transportation relies on electricity [11]. These conditions feature also the increasing utilization of renewables [12], including wind power and Photovoltaics (PV) [13], as primary energy sources [14]. As such, the railway sector is the only mode of transportation achieving a reduction of GHG emissions down by 2 % between 2000 and 2018 [11]. Railway-based transportation has the potential to quickly become not only the cleanest, but also the greenest high-volume transport and has an essential role in creating a sustainable lifestyle and economy.

Thus, today's societal challenges can only be met with a railway system as the backbone of a well-connected sustainable transportation infrastructure. Utilizing rail´s full performance will be crucial to reduce GHG emissions drastically and comply with the Paris Agreement [15]. In the broad view, railway infrastructure should be integrated into the natural landscape and thus become a "green network" connecting different biotopes by 2050 [11]. In order to stay on track and achieve the sustainable development targets Union International Railways (UIC) has introduced a sustainability platform, focusing on "Energy and CO_2" [16], "Air Quality" [17], "Circular Economy" [18], "Noise and Vibration" [19], and "Sustainable Land Use" [20]. Their objectives are well aligned with governmental approaches towards a greener society [21, 22].

1.1 Motivation

In order for next-generation railway systems to meet the environmental and economic requirements, an improvement in the energy supply and distribution, and from the drivetrain down to the auxiliaries is urgently required [23]. Considering electrified railway with implemented regenerative braking [24], which allows the recovery of kinetic energy during braking intervals, the auxiliaries' energy consumption becomes more and more crucial. Hence, [25] forecasts a Compound Annual Growth Rate (CAGR) of 5 % in railway auxiliaries for 2022 driven by increasing rail electrification due to the sustainability targets and their economic viability.

Auxiliary applications on the rolling stock include braking and door control systems, battery charging, air supply, air conditioning, ventilation,

lighting, heating, information and control systems, train-control, and traction units for blowers, fans, and compressors [26]. All these units are operated under unique conditions and constraints. The most crucial aspect is safety, distinguishing three categories: first, "Emergency Loads" are required to ensure passenger safety, i.e. emergency ventilation and lights or the door control system; second, "Essential Loads" are needed to operate the train, i.e. the braking system and the train control; and third, "Non-essential Loads" are only needed for passenger comfort. Further examples are reliability and lifetime, to maximize the operational time, and environmental aspects such as a wide temperature operating range, minimization of dust, shocks, or vibrations. Additional aspects are noise emission limits and power quality, considering large voltage and frequency tolerances, voltage distortions, grid interruptions, and EMI compliance [27].

In summary, the main requirements for commercial electric power conversion systems for the rolling stock are compactness, light weight, high efficiency, high reliability and redundancy [28, 29]. Similar challenges are present for electro-mechanical conversion stages, which are typically equipped with a Variable Speed Drive (VSD) system for efficient operation of compressors [30], pumps [31], fans, and blowers [32].

1.2 Application

The focus of this thesis is the air supply system of railway vehicles, implemented by an onboard compressor unit [33] as indicated in **Fig. 1.1**. Such compressor units are required to charge the pressure tank, which supplies the air brake system, air suspension, sanding system, wheel flange lubrication, door control systems, the signal horn, and the pantograph rising [34]. Typically, these units are supplied from the traction transformer's tertiary winding with a single-phase AC voltage. However, as already mentioned air pressure is also required to raise the pantograph and connect the railway vehicle to the overhead line. Thus, operation from an onboard battery is demanded during the startup. Both, the air brakes and the door control system are safety-relevant functions and require the highest level of reliability. Consequently, multiple compressor units are installed in every second or fourth car of multi-unit rail coaches to achieve a distributed and redundant air-pressure network [35]. Given space- and weight constraints demand a minimal volume realization of the compressor unit to gain more space for passengers in the cars [36]. Also, extended maintainability intervals are highly preferred to

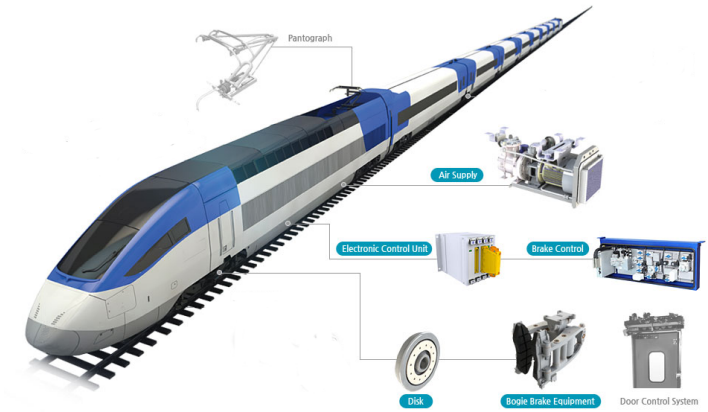

Fig. 1.1: Overview of a multi-unit rail coach with all components of the air brake system highlighted (taken from [37]). The air supply is also required to raise the pantograph and operate the door control system.

shorten the outage period of the considered cars.

Considering a compressor unit, a detailed mission profile reveals the required airflow rate at a given pressure, similar as described in [38]. For the application scenario at hand, a 7.5 kW oil-free scroll compressor [39] is selected, which benefits from long maintenance intervals besides high pressure and low noise generation (see [40] for a comparison of compressors).

During normal operation the compressor unit is directly supplied from the tertiary traction transformer winding ("grid operation"), a typical approach for auxiliary railway applications [41]. The nominal input voltage is given with 400 Vrms at 50 Hz. However, due to large grid tolerances, the input voltage can vary between 280 Vrms to 530 Vrms, i.e. by almost a factor of two. During start-up an additional battery is required and also employed during extended grid interruptions to minimize downtime. The nominal battery voltage is given with 100 Vdc and varies between 70 Vdc to 120 Vdc, depending on the state-of-charge. For this mode, the mechanical output power is limited to 1 kW, to prevent unnecessary overdimensioning.

A VSD system must be employed to reduce the overall energy consumption of the load [42], as analyzed in [43] specifically for compressor systems. Consequently, the application requires a power electronic system to convert the single-phase AC — or DC, under battery operation — input voltage into

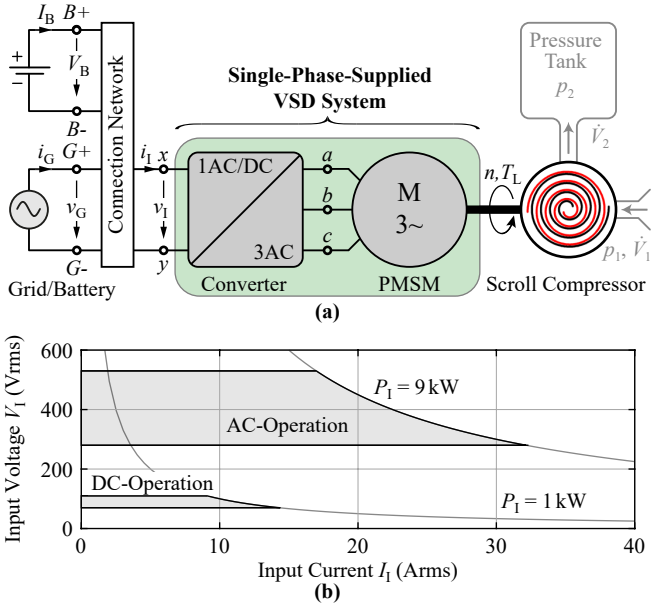

Fig. 1.2: (a) Single-phase-supplied VSD system to drive the scroll compressor of the air supply system of railway vehicles. The system can be supplied either from the tertiary traction transformer winding (AC) or from an onboard battery (DC). **(b)** Required converter input range, including reduced power level for DC-supplied operation.

a symmetrical three-phase voltage system with adjustable amplitude and frequency to control the motor speed. A three-phase Permanent Magnet Synchronous Motor (PMSM) is employed for high torque, low weight, high efficiency, and compactness [44]. The resulting VSD system with the different supply options is shown in **Fig. 1.2(a)**.

Accounting for acceleration phases and system losses, the VSD has to be designed for 9 kW output power (see **Fig. 1.2(b)**). Due to the power level, the single-phase-supplied drive system should feature unity power factor operation to minimize input current harmonic distortion and reactive grid power [45]. In addition, the system must comply with CISPR 11 / Class A [46] at the input terminals x and y. As the compressor units are mainly operated in part-load or with a low duty cycle, peak efficiency is not the primary concern. Still, the highest defined efficiency class for VSD systems, IES 2 according to [47], has to be fulfilled to align with the previously mentioned

Tab. 1.1: Compressor unit specifications.

Air Flow Rate at Pressure	850 L/min, 0.83 MPa
Nominal Speed (n_N)	3700 rpm
Nominal Mechanical Power, Grid ($P_{0,N}$)	7.5 kW
Nominal Mechanical Power, Battery ($P_{0DC,N}$)	1.0 kW
Nominal Grid Voltage ($V_{G,N}$)	400 Vrms
Grid Voltage Range (V_G)	280 Vrms to 530 Vrms
Grid Frequency (f_G)	50 Hz
Battery Voltage Range (V_B)	70 Vdc to 120 Vdc
EMI Standard (Input)	CISPR Class A [46]
Efficiency Standard	IES 2 [47]

sustainability targets. All key specifications are summarzied in **Table 1.1**.

The conventional implementation of a single-phase-supplied VSD system features a two-stage approach and is shown in **Fig. 1.3(a)**). It comprises a front-end Power Factor Correction (PFC) rectifier providing an almost constant DC-link voltage to the subsequent Voltage Source Inverter (VSI), which drives the motor and the scroll compressor at the requested speed with constant power [48]. Thus, an energy storage is required at the DC-link to buffer the power pulsation originating from desired ohmic load behavior in a single-phase grid, cf. **Fig. 1.3(b)**-**(d)**. For the considered application results a capacitance requirement in the mF-range due to the limited voltage ripple amplitude [49], and consequently, practical implementations are restricted to electrolytic capacitors.

Even though a very specific application is examined, the requirements for single-phase to three-phase variable-speed conversion are quite general as shown in literature, e.g. a 10 kW, 230 Vrms, single-phase VSD in [50] or a single-phase to three-phase VSD with PFC operation in [51, 52].

1.3 Challenges

Next-generation onboard compressor units for single-phase supplied railway vehicles must comply with several requirements, such as operation from the single-phase AC grid or from batteries while surviving supply interruptions

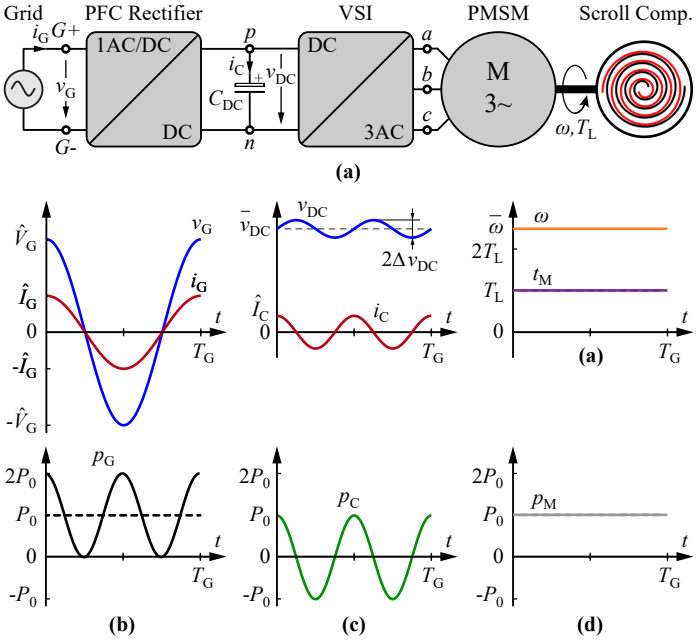

Fig. 1.3: (a) Conventional single-phase-supplied VSD system, comprising a front-end PFC rectifier with large electrolytic DC-link capacitor, and an inverter stage to drive the motor and the compressor, **(b)**-**(d)** Corresponding voltage, current, speed, torque and power waveforms over one grid period, indicating PFC operation and constant output power implying the requirement of a power pulsation buffer at the DC-link.

without system faults or trips. In AC operation, the conversion unit must achieve PFC operation and provide the nominal mechanical output power over the entire input voltage range, which can vary by almost a factor of two in the considered scenario. However, the targeted power density improvement and the enhanced lifetime under IES 2 compliance define the actual challenges addressed in this thesis.

- **Motor Integration**

  VSD systems with improved power density targets require full motor-integration of the power conversion unit [53], as this allows for combined cooling of the electronics and the motor [54], reduces the number of connectors, and improves the overall volume utilization. Additionally, it eliminates shielded cables [55] leading to cost and weight savings and exhibits an improved EMI behavior [53] due to the integration in a single housing. However, the system losses need to be strictly limited to enable suitable cooling concepts, i.e. passive cooling without fans or blowers. Accordingly, elevated operating temperatures result inside the integrated converter system in the range of 85 °C to 105 °C [56]. The resulting ambient temperature of the electrolytic capacitors employed in the DC-link to cope with the single-phase power pulsation, leads directly to a lifetime degradation and requires substantial overdimensioning [57, 58], and thus, prevents the necessary integration step.

- **Elimination of Electrolytic DC-link Capacitors**

  Due to the required capacitance value, which is typically in the mF-range, electrolytic capacitors are the only practical option for a passive Power Pulsation Buffer (PPB) in the DC-link. However, these components are still contributing a significant volume, i.e. around 25 % of the PFC rectifier volume in [59], and even limit the lifetime of the system [60]. Consequently, the electrolytic capacitor must not only be avoided for volume [59] and lifetime considerations [60] but also to enable full motor integration and meet the power density objective. In a straightforward approach, the electrolytic capacitor could be replaced by an active power pulsation buffer [61]. State-of-the-art solutions offer a wide variety of such concepts, which are comprising an active switching stage in combination with a buffer capacitor and are typically arranged in series or in parallel to the existing DC-link capacitor [62–65]. The buffer capacitor is operated with large voltage

ripple, which results in reduced capacitance requirement and/or allows to employ foil or ceramic capacitors. In contrast to electrolytic capacitors these capacitor technologies are not lifetime limited but are characterized by a substantially smaller energy density, which limits the achievable volume reduction. Furthermore, the associated switching stage causes certain loss contributions and incurs significant realization effort, complexity, and cost. Moreover, the increased component count is lowering the reliability, and thus active PPBs are not suitable for the considered application.

1.4 State-of-the-Art

For enabling the highly-desired motor integration of the converter system for single-phase to three-phase drive applications, alternatives to the traditional two-stage system with electrolytic DC-link capacitors are required. Concepts that synergetically utilize components are considered first. Ultra-low-cost implementations use the grid voltage effectively as one of the motor line-to-line voltages, and employ four power MOSFETs and a triac [66] but don´t allow a wider range speed control. For utilizing the motor star point as one of the connecting points to the single-phase grid, the motor leakage inductance may be utilized as boost inductor of a PFC rectifier stage [67], but this results in unacceptably high voltage stress (twice the grid peak voltage) as this application already operates at a high grid input voltage. The same issue occurs in a low-cost implementation that employs a front-end PFC rectifier stage with only one bridge-leg and a split DC-link [68]. Coupled power electronics approaches, like Z-source-based concepts [69] or matrix converters [70, 71] are further options. Matrix converters typically feature an (integrated) active PPB for power decoupling [72, 73], a basic requirement as the matrix converter doesn´t include energy storage. Current source structures [74, 75], in the end, only replace the PFC rectifier stage boost inductor with a DC-link inductor (since VSIs do not demand an output filter here), while requiring bidirectional switches, and therefore do not improve the potential for integration.

1.5 Aims and Contributions

At the latest with the announcement of the Google Little Box Challenge, power-dense single-phase AC/DC converter systems have become an im-

portant research topic, extending the knowledge base of converter systems employing Wide-Bandgap (WBG) devices as well as active PPB concepts. However, the existing literature lacks practical solutions for electrolytic-less single-phase supplied power factor corrected drive systems. Thus, this thesis aims to overcome this deficiency by the proposal of novel concepts, enabling ultra-high-power-density motor-integrated VSD systems operated from a single-phase supply for next-generation compressor, pump, or fan applications.

The PFC operation of the front-end rectifier defines the pulsating input power. With the requirement of avoiding electrolytic capacitors and any other kind of active power pulsation buffer circuitry, the only remaining option is to forward the pulsating input power directly to the motor. In this thesis a new Motor-Integrated Power Pulsation Buffer (MPPB) concept is introduced, which utilizes the kinetic energy stored in the drivetrain, i.e. the motor and the load inertia for power pulsation buffering.

With an approximately constant speed of the drivetrain, the motor torque is proportional to the input power pulsation, cf. **Fig. 1.4**, and varies between zero and twice the average load torque. Once the applied motor torque is larger than the (constant) load torque T_L, the rotating mass accelerates and stores the excessive input power in the form of kinetic energy. In the remaining intervals, characterized by a motor torque t_M below the load torque, the drivetrain decelerates, and releases kinetic energy which is utilized to supply the mechanical load. The kinetically stored energy (related to $\bar{\omega}$) is typically at least one order of magnitude above the energy storage requirement defined by the PFC operation. Thus, a comparably small speed ripple results and the corresponding speed fluctuation is similar to the DC-link voltage oscillation in a conventional system employing electrolytic capacitors.

Concerning the power flow, the introduced concept is similar to conventional single-phase motors, but in contrast, it also provides variable speed control and unity power factor operation at the input. The employment of the MPPB concept in various topological structures features different advantages and challenges, which are the main contributions in this thesis, as described in the following.

- **Single-Inverter Topology**

  In a first step, the MPPB concept is applied to the conventional two-stage system featuring a single-phase front-end PFC rectifier and a

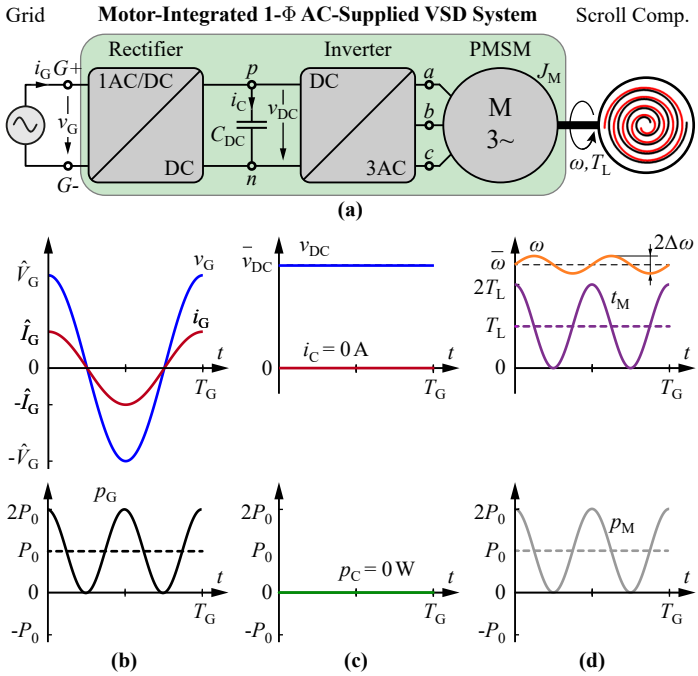

Fig. 1.4: (a) Electric power pulsation buffer-less single-phase supplied VSD system, comprising a front-end PFC rectifier with small DC-link capacitor, and a VSI to drive the motor and compressor, **(b)-(d)** Corresponding voltage, current, speed, torque and power waveforms over one grid period, indicating PFC operation and pulsating output power implying that no power pulsation buffer is required in the DC-link.

three-phase VSD inverter. The proposed control structure ensures the desired average speed and sinusoidal input current for unity power factor operation. A constant DC-link voltage is achieved through the corresponding voltage control and a grid power feed-forward, both affecting the inverter output power, i.e. the motor current setpoints. Further adaptions are proposed to facilitate improved operation without a significant energy storage within the electrical system during abnormal supply conditions such as grid interruptions.
A 7.5 kW, motor-integrated hardware demonstrator validates the proposed MPPB concept and control in **Chapter 2** with detailed analyses on the low-speed operation, possible control enhancements and the phase currents in **Appendix A**, **Appendix B** and **Appendix C**. For maximum performance, a permanent magnet motor and WBG devices are employed, achieving a total boxed volume of only 8.2 L for the drive system (incl. the motor), which corresponds to a power density of 0.91 kW/L (15 W/in^3). The introduced loss models are verified over the full torque range, revealing a nominal grid-to-motor-shaft efficiency of 91.4 %, which corresponds to 703 W of system losses and ensures IES 2 compatibility. For all loads over 5 kW or 66 % of nominal load the grid-to-motor-shaft efficiency remains above 90 %. Compared to the conventional implementation, a worst-case loss penalty of 17 % or 100 W occurs at nominal operation, while the averaged losses (over the full torque range) increase only from 447 W to 491 W, or 9.8 %.

- **Dual-Inverter Topology**

  In the second part of this thesis the MPPB concept is applied to a dual-inverter topology with a three-phase Open-End Winding (OEW) motor. This approach omits the boost PFC rectifier stage, i.e. the High-Frequency (HF) interleaved bridge-legs and the corresponding boost inductors, which reduces the system volume and the realization effort. Consequently, the topology requires only an Electromagnetic Interference (EMI) input filter, a diode-bridge, two VSIs stages implemented using six-pack modules and small foil capacitors.
  The operating principle and the corresponding closed-loop control structure, to achieve PFC operation, DC-link voltage balancing, and average speed control are investigated in **Chapter 3**. The desired motor voltage division strategy to achieve the voltage set points is described. The detailed system analysis reveals that the motor voltage can be selected independent of the grid voltage amplitude, in contrast to existing

single-phase supplied dual-inverter concepts. The converter performance is evaluated based on simple performance indices with respect to the motor voltage. For the considered compressor application with a wide input voltage range, a semiconductor loss reduction of at least 30 % can be obtained compared to a state-of-the-art approach, further reducing the converter volume. Finally, the proper operation is verified with a closed-loop circuit simulation.

WBG devices are widely employed for high-performance rectifier and inverter systems [76], as they benefit from lower conduction and/or reduced switching losses. Their performance improvements compared to Silicon-based devices result primarily from enhanced material properties. Thus, next-generation VSD systems replace Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) by Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), to achieve higher efficiencies through reduced bridge-leg losses and increased power densities through an order-of-magnitude increase in switching frequency and reduction of the DC-link capacitance.

However, fast switching WBG devices feature excessive voltage slew rates, potentially resulting in motor terminal surge voltages due to motor cable reflections and/or unequal voltage distribution over the motor windings which could lead to partial discharge phenomena and accelerated winding insulation aging. Sine wave filters would allow to overcome this problem, but the additional filter components and the required switching frequency increase (needed for maximum power density) contradict the possible performance gain. Instead, voltage slope limitation concepts, including gate drive modifications and $\mathrm{d}v/\mathrm{d}t$-limiting LC-filters, are analyzed and compared theoretically in [77].

For motor-integrated inverter systems, which are capable of sustaining higher voltage slope rates in the range of 10 V/ns to 15 V/ns, gate drive modifications have been identified as the most promising solution. This concept combines gate resistors with an external Miller capacitor across the bridge-leg power semiconductors to slow down the voltage transient, with minimal effect on the remaining switching transition. The detailed analysis and the experimental results of this concept, which is utilized for the single inverter realization in the first part of the thesis can be found in **Appendix D**. A conventional VSD system employing a SiC MOSFET bridge-leg-based two-level inverter system achieves a calculated semiconductor efficiency of 99.2 % for a voltage slope limitation of 10 V/ns and 99.4 % for a limit of 15 V/ns. Accordingly, the concept represents a promising solution for future high-performance motor-integrated WBG-based VSD systems.

1.6 List of Publications

The most significant contributions of this thesis and of further research projects are listed in the following.

1.6.1 Journal Papers

The main findings presented in this thesis have also been published in internationally refereed journals, as listed in the following:

[J5] **M. Haider**, D. Bortis, G. Zulauf, J. W. Kolar, Y. Ono, "Novel Motor-Kinetic-Energy-Based Power Pulsation Buffer Concept for Single-Phase-Input Electrolytic-Capacitor-Less Motor-Integrated Inverter System," *Electronics* 2022, 11, 280.

[J4] **M. Haider**, S. Fuchs, G. Zulauf, D. Bortis, J. W. Kolar, Y. Ono, "Analytical Loss Model for Three-Phase 1200 V SiC MOSFET Inverter Drive System Utilizing Miller Capacitor-Based Active dv/dt-Limitation," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 93–104, 2022.

Furthermore, in the course of the Ph.D. research, the author contributed to the following journal papers:

[J3] **M. Haider**, J. Azurza Anderson, N. Nain, G. Zulauf, J. W. Kolar, D. Xu, G. Deboy, "Analytical Calculation of the Residual ZVS Losses of TCM-Operated Single-Phase PFC Rectifiers," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 250–264, 2021.

[J2] **M. Haider**, J. Azurza Anderson, S. Mirić, N. Nain, G. Zulauf, J. W. Kolar, D. Xu, G. Deboy, "Novel ZVS S-TCM Modulation of Three-Phase AC/DC Converters," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 529–543, 2020.

[J1] L. Schrittwieser, M. Leibl, **M. Haider**, F. Thöny, J. W. Kolar, and T. Soeiro "99.3 % Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 126–140, 2019.

1.6.2 Conference Papers

Further core achievements presented in this Ph.D. thesis have been published in the proceedings of international conferences, in particular:

[C9] **M. Haider**, D. Bortis, S. Mirić, J. W. Kolar, Y. Ono, "Dual-Inverter Topology for Single-Phase Supplied Drive Systems Without Electrolytic Capacitor," in *Proc. of the IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Gyeongju, South Korea, Oct. 2021.

Best Paper Award

Further conference publications of the author:

[C8] J. W. Kolar, J. Azurza Anderson, S. Mirić, **M. Haider**, M. Guacci, M. Antivachis, G. Zulauf, D. Menzi, P. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti, D. Bortis, "Application of WBG Power Devices in Future 3-Phase Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword"," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2020.

[C7] D. Zhang, M. Guacci, **M. Haider**, D. Bortis, J. W. Kolar, J. Everts, "Three-Phase Bidirectional Buck-Boost Current DC-Link EV Battery Charger Featuring a Wide Output Voltage Range of 200 to 1000 V," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, Oct. 2020.

[C6] **M. Haider**, M. Guacci, D. Bortis, J. W. Kolar, Y. Ono "Analysis and Evaluation of Active/Hybrid/Passive dv/dt-Filter Concepts for Next Generation SiC-Based Variable Speed Drive Inverter Systems," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, Oct. 2020.

[C5] J. Azurza Anderson, **M. Haider**, D. Bortis, J. W. Kolar, M. Kasper, G. Deboy, "New Synergetic Control of a 20 kW Isolated VIENNA Rectifier Front-End EV Battery Charger," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, Canada, June 2019.

[C4] **M. Haider**, D. Bortis, J. W. Kolar, Y. Ono "Novel Single-Phase Buck+Boost PFC Rectifier with Integrated Series Power Pulsation Buffer," in *Proc. of the IEEE International Conference on Power Electronics (ECCE Asia)*, Busan, South Korea, May 2019.

[C3] **M. Haider**, D. Bortis, J. W. Kolar, Y. Ono "Sinusoidal Input Current and Average Speed Control of a Single-Phase Supplied Three-Phase Inverter Drive Without Electrolytic Capacitor," in *Proc. of the IEEE International*

Conference on Power Electronics and Motion Control (PEMC), Budapest, Hungary, Aug. 2018.

[C2] **M. Haider**, D. Bortis, J. W. Kolar, Y. Ono "Novel Sinusoidal Input Current Single-to-Three-Phase Z-Source Buck+Boost AC/AC Converter," in *Proc. of the IEEE International Conference on Power Electronics (ECCE Asia)*, Niigata, Japan, May 2018.

[C1] L. Schrittwieser, M. Leibl, **M. Haider**, F. Thöny, J. W. Kolar, T. B. Soeiro "99.3 % Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, March 2017.

1.6.3 Patents

The most innovative and original outcomes of the research, which could offer a competitive advantage if commercially exploited, have led to the filing of national and international patents. In particular:

[P10] **M. Haider**, J. W. Kolar, D. Bortis, and Y. Ono, "Ride-Through Capability for Single-Phase Supplied Drive Systems Without an Intermediate Energy Storage," 2021.

[P9] **M. Haider**, J. W. Kolar, D. Bortis, S. Mirić, and Y. Ono, "Electrolytic-Less Dual-Inverter Topology for Single-Phase Supplied Drive Systems," 2021.

[P8] **M. Haider**, J. W. Kolar, D. Bortis, and Y. Ono, "Inverter, Control of Inverter, Control Program of Inverter, Converter, Driving Unit," 2021.

[P7] **M. Haider**, M. Guacci, J. W. Kolar, D. Bortis, and Y. Ono, "Three-Phase Supplied Modular Machines - Phase-Modular Approach (TPSMM-II)," 2020.

[P6] **M. Haider**, M. Guacci, D. Bortis, J. W. Kolar, and Y. Ono, "Three-Phase Supplied Modular Machines - Mesh Topology (TPSMM-I)," 2020.

[P5] J. Azurza Anderson, **M. Haider**, S. Mirić, J. W. Kolar, "Power Conversion Method and Power Converter," 2020.

[P4] J. W. Kolar, D. Bortis, **M. Haider**, and Y. Ono, "Novel Single-Phase Buck+Boost PFC Rectifier with an Integrated Series Power Pulsation Buffer," 2018.

[P3] J. W. Kolar, D. Bortis, **M. Haider**, and Y. Ono, "AC-AC Converter," 2018.

[P2] J. W. Kolar, D. Bortis, **M. Haider**, and Y. Ono, "AC-AC Converter," 2017.

[P1] L. Schrittwieser, M. Leibl, **M. Haider**, F. Thöny, J. W. Kolar, "Magnetische Drossel, Umrichterabschnitt und Umrichter," CH Patent 713 573 B1, 2017.

2
Single-Inverter Topology

This Chapter summarizes the most relevant findings in the context of research on motor-integrated power-factor-corrected single-phase-supplied drive systems without electrolytic capacitors, which are also published in:

- **M. Haider**, D. Bortis, G. Zulauf, J. W. Kolar, Y. Ono, "Novel Motor-Kinetic-Energy-Based Power Pulsation Buffer Concept for Single-Phase-Input Electrolytic-Capacitor-Less Motor-Integrated Inverter System," *Electronics* 2022, 11, 280.

Motivation

The elimination of the electrolytic capacitors, typically implemented to cope with the occurring input power pulsation of the supplying single-phase grid, is essential to enable full motor integration in next-generation high-performance variable speed drive systems.

Executive Summary

Motor integration of singe-phase-supplied Variable Speed Drives (VSDs) is prevented by the significant volume, short lifetime and operating temperature limit of the electrolytic capacitors required to buffer the pulsating power grid. We eliminate the DC-link energy storage requirement by using the kinetic energy of the motor as a buffer. The proposed concept is called the Motor-Integrated Power Pulsation Buffer (MPPB), and we detail a control technique and structure that meets the requirements for nominal and faulted operation with a simple reconfiguration of existing controller blocks. A 7.5 kW, motor-integrated hardware demonstrator validates the proposed MPPB concept and loss models for a scroll compressor drive used in auxiliary railway applications. The MPPB drive with front-end CISPR 11 / Class A Electromagnetic Interference (EMI) filter, Power Factor Correction (PFC) rectifier stage, output-side inverter stage and motor achieves a power density of 0.91 kW/L (15 W/in^3). The grid-to-motor-shaft efficiency exceeds 90 % for all loads over 5 kW or 66 % of nominal load, and a worst-case loss penalty over a conventional system of only 17 %.

2.1 Introduction

Mobility, transportation, and industrial systems are increasingly electric, from the drivetrain to the auxiliaries, driven by improvements in battery performance and lifetime, government and private mandates to reduce greenhouse gas emissions, and an improved user experience. This electrification includes the traction systems in electric vehicles, but the auxiliary systems must also be electrified with power-dense, efficient, and reliable power conversion stages under unique operating conditions and constraints. In particular, electromechanical systems — including pumps, compressors, and blowers — are required on nearly every vehicle and require Variable Speed Drives (VSDs) for efficient operation.

We consider an on-board compressor system for the air brakes of railway vehicles, as shown in **Fig. 2.1(a)**. This oil-free scroll compressor [39] — selected for high pressure, low noise, and long maintenance intervals (see [40] for a comparison of compressors) — is used to charge the pressure tank that supplies the air brakes, pantograph, and other critical loads driven by air pressure, necessitating ultra-high-reliability. As such, the compressor system is supplied from a tertiary traction transformer winding during normal operation ("grid operation"), as is typical for auxiliary railway applications [41],

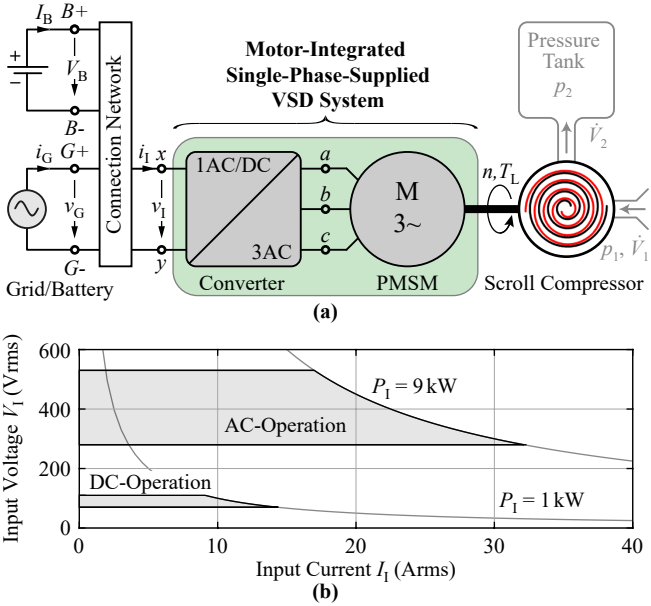

Fig. 2.1: **(a)** Motor-integrated single-phase-supplied Variable Speed Drive (VSD) system to drive the compressor of an air-brake system for railway vehicles. The system can be supplied either from the tertiary winding (AC) of the traction transformer or an on-board battery (DC-supplied operation). **(b)** Required converter input range, including reduced power for DC-supplied operation.

Tab. 2.1: Key system specifications.

Air Flow Rate at Pressure	850 L/min, 0.83 MPa
Nominal Speed (n_N)	3700 rpm
Nominal Mech. Power, Grid ($P_{0,N}$)	7.5 kW
Nominal Mech. Power, Batt. ($P_{0DC,N}$)	1.0 kW
Nominal Grid Voltage ($V_{G,N}$)	400 Vrms
Grid Voltage Range (V_G)	280 Vrms to 530 Vrms
Grid Frequency (f_G)	50 Hz
Battery Voltage Range (V_B)	70 Vdc to 120 Vdc
EMI Standard (Input)	CISPR 11 / Class A [46]

and from an on-board battery during startup or extended grid interruptions, with a reduced output power. The key specifications for this particular application are given in **Table 2.1**. While, in this work, we are focused on the single-phase to three-phase VSD power conversion system for this particular application, the requirements for single-phase to three-phase variable-speed conversion are quite general (e.g. a 10 kW, 230 Vrms, single-phase VSD in [50] or a single-phase to three-phase VSD with Power Factor Correction (PFC) operation in [51, 52]).

With a VSD system required to increase compressor performance [43], the application needs a power electronics system to convert the single-phase AC — or DC, under battery operation — input voltage into a symmetrical three-phase voltage system, where the magnitude and frequency can be adjusted to control motor speed (and, accordingly, output power). A three-phase Permanent Magnet Synchronous Motor (PMSM) is selected for high torque, low weight, high efficiency, and compactness [44]. The VSD is designed for 9 kW output power (see **Fig. 2.1(b)**), to meet the required 7.5 kW of mechanical output power (**Table 2.1**) while accounting for system losses and acceleration, must comply with CISPR 11 / Class A [46], and must operate under unity power factor operation to minimize harmonic distortion and reactive grid power [45].

Conventionally, these power conversion systems are realized with a two-stage system [49] comprising a front-end PFC rectifier, an electrolytic DC-link capacitor to buffer the power pulsation from the single-phase grid supply, and a VSD inverter to drive the motor and compressor [48]. For auxiliary motor drive applications, though, efficiency is not the primary concern — due to the low duty cycle of operation — and power density should be maximized for the space- and weight-constrained mobility application. The highest power density solution, in the end, is a motor-integrated drive system [53], which eliminates expensive shielded cables [55] and cable reflections [78] which allows for higher slew rates of the inverter stage power semiconductor switching voltage transitions and/or lower switching losses, exhibits better Electromagnetic Interference (EMI) behavior [53] from integration in a single housing, and allows for combined cooling of the electronics and motor [54]. Motor-integrated VSDs, in sum, result in lower installation and operating costs, but require integration of all drive components — even the EMI input filter [79]. The requirement for electrolytic capacitors as the single-phase power buffer, though, prevents motor integration, with the elevated operating temperatures of the integrated converter (85 °C to 105 °C) [56] degrading

lifetime and/or requiring substantial overdimensioning of these large capacitors [57, 58, 60].

For the highly-desired motor-integration of the converter system for these single-phase to three-phase drive applications, then, alternatives to the traditional two-stage approach with an electrolytic capacitor are required. Solutions that synergetically employ components are considered first. Ultra-low-cost implementations use the grid voltage effectively as one of the motor line-to-line voltages, and employ four power MOSFETs and a triac [66] but doesn't allow a wider range speed control. For utilizing the motor star point as one of the connecting points to the single-phase grid, the motor leakage inductance may be utilized as a boost inductor [67], but this results in unacceptably-high voltage stresses (twice the grid peak voltage) for this application, which already features a high grid input voltage. The same issue occurs in a low-cost implementation that employs a front-end PFC rectifier with only one bridge-leg and a split DC-link [68]. Coupled power electronics (rectifier to inverter) approaches, like Z-source-based concepts [69] or matrix converters [70, 71], typically feature an (integrated) active buffer for power decoupling [72, 73], a basic requirement since the matrix converter doesn't include energy storage which drives complexity and high component stresses. Current-source structures [74, 75], in the end, only replace the boost inductor with a DC-link inductor (since voltage-source inverters do not require an output filter here) while requiring bidirectional switches, and therefore do not improve the potential for integration. The synergetic approaches, then, do not hold the promise of eliminating the large energy storage components required to buffer the single-phase power pulsation — and if they do start to alleviate the requirement, the penalties appear unacceptably high.

Accordingly, we propose to use the motor (and load) inertia as a power buffer, eliminating the need for power buffering in the DC-link capacitors, an approach called the Motor-Integrated Power Pulsation Buffer (MPPB) and introduced in [80]. We utilize the conventional two-stage structure, with a single-phase front-end PFC rectifier and a three-phase VSD inverter, with the power flow shown for a conventional system and the MPPB system shown in **Fig. 2.2(a)**. Although particular rectifier and inverter topologies are selected and demonstrated here, the findings are applicable to any specific implementation of the rectifier and inverter.

The MPPB concept was previously proposed with the PFC rectifier omitted and the inverter stage directly supplied from a single-phase-grid diode bridge rectifier [81–83]. This concept results in a rectifier sine wave voltage at the DC-link, so the input current is only sinusoidal if the motor voltage stays

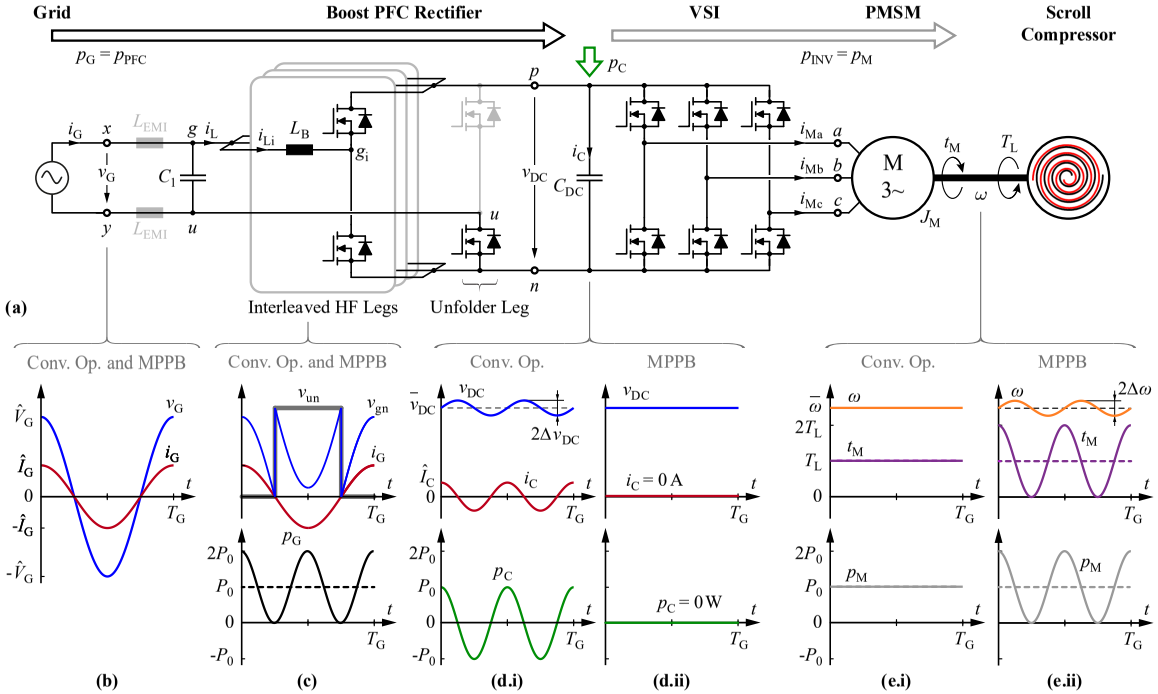

Fig. 2.2: (a) Implemented topology comprising a single-phase boost-type totem-pole PFC rectifier and a three-phase inverter, decoupled by a DC-link capacitor C_{DC}. The power flow is indicated with arrows. **(b-e)** Characteristic voltage, current, speed, torque, and power waveforms **(i)** for conventional operation with an electrolytic capacitor C_{DC} and **(ii)** for the proposed MPPB concept.

below the rectified input voltage. This concept, then, is limited to motors with a low back Electromotive Force (EMF) and/or applications where a large speed variation is acceptable — but in both cases, unity power factor cannot be achieved. In [84], a solution to this problem was proposed, where a reactive current component is injected into the motor to keep the back EMF of the motor below the input voltage. Here, the PFC rectifier can indeed be omitted, but the small motor inductance leads to large motor currents and excessive losses. With this constraint and the large fluctuating DC-link voltage, which increases system complexity, applications for this approach are restricted to drive systems with special low-voltage motors that do not operate at common voltages.

In this work, a single-phase-supplied electrolytic-less VSD system with dedicated rectifier and inverter stages that realizes high lifetime and reduced volume for motor integration is designed, modelled, and implemented. In **Section 2.2**, the rectifier and inverter topologies are selected, introduced, and evaluated with the concept and control of the novel proposed MPPB approach to eliminate electrolytic capacitors. In this Section, the operational limits for the proposed approach are evaluated for different load cases. The novel control concept for MPPB operation is derived and explained in detail, with verification based on circuit simulation, and finally the phase currents are investigated in detail to compare the performance of the novel MPPB approach to a conventional system. **Section 2.3** details the implementation of the motor-integrated drive system with volume and loss distributions, including showcasing the motor integration that is uniquely enabled by the novel, proposed MPPB approach. **Section 2.4** verifies the system operation in the time domain for steady-state and transients, loss models across the full torque range, and EMI requirements and compares the system losses between MPPB and conventional systems. In **Section 2.5**, the extended functionality required for the considered application is demonstrated, including ridethrough and battery-supplied operation. The novel control structure can also be employed for dc-supply operation with a single structure that simplify the implementation and maintenance effort of the system. **Section 2.6** concludes and summarizes the MPPB approach and results of the work, with appendices that specifically investigate low-speed operation in the context of the proposed approach (**Appendix A**), controller design and future enhancements (**Appendix B**) to reduce the DC-link voltage ripple (including novel feedforward terms), and the detailed phase currents under MPPB operation (**Appendix C**).

2.2 Topology Selection and Proposed MPPB Concept and Control

2.2.1 Topology

Although the proposed MPPB concept is applicable to a broad range of inverter and rectifier topologies, we select a particular configuration for the demonstration in this work to explain and, later, showcase the MPPB concept. Conventional systems in these applications utilize a two-stage design with a single-phase PFC rectifier, a large low- and high-frequency-decoupling DC-link capacitor, and a three-phase VSD inverter. A similar two-stage topology is desired here for a straightforward comparison and implementation of the MPPB concept relative to the state-of-the-art.

A single-phase PFC rectifier can be implemented with multiple topologies, components, and control scheme, and these options are reviewed extensively in [85]. A unidirectional boost PFC rectifier with a diode bridge, boost inductor, and transistor and diode pair is widely used for simplicity and low-cost [86]; here, instead, we select a totem-pole PFC with an unfolder bridge-leg (see **Fig. 2.2(a)**) to improve the performance by avoiding the diode conduction losses [87]. While Zero-Voltage Switching (ZVS) triangular-current-mode schemes could further reduce the semiconductor switching losses [88], a simple Pulse-Width Modulation (PWM) scheme with constant switching frequency is preferred for the simplicity of interleaving and operation across a wide AC input voltage range (see **Fig. 2.1(b)**). Finally, with a DC-link voltage above 750 V (the peak voltage of the maximum grid voltage), 1200 V power semiconductors must be used and we choose Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) over Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) for the lower loss characteristics.

Similarly, we select a straightforward two-level, three-phase inverter utilizing SiC MOSFETs and directly connected to the motor [89]. With SiC MOSFETs and no output filter, a voltage slew rate limitation is required to prevent motor isolation aging [90], with options and tradeoffs for this slew rate value and implementation highlighted in [77].

The resulting structure with the indicated power flow is shown in **Fig. 2.2(a)**, with the grid and rectifier input waveforms under conventional operation shown in **Fig. 2.2(b)** and **(c)** (see [87] for a more detailed explanation). This structure also supports the necessary DC-input operation, with the battery terminals directly connected to x and y. In this mode, the PFC rectifier operates as a conventional DC/DC boost converter.

2.2.2 MPPB Concept

At the single-phase grid input, unity-power-factor operation dictates that the drive system behaves as an ohmic load with a sinusoidal input current $i_G(t) = \hat{I}_G \cos(2\pi f_G t)$ in phase with the grid voltage $v_G(t) = \hat{V}_G \cos(2\pi f_G t)$, as shown in **Fig. 2.2(b)**. The instantaneous input power, however, varies as:

$$p_G(t) = v_G(t)\, i_G(t) = P_0 + \tilde{p}_G(t), \tag{2.1}$$

with $P_0 = \hat{V}_G \hat{I}_G/2$ (see **Fig. 2.2(c)**). A lossless system implies that $p_G(t) = p_{PFC}(t)$ and $p_M(t) = p_{INV}(t)$ and an instantaneous power balance results in:

$$p_G(t) = p_C(t) + p_M(t). \tag{2.2}$$

Thus, the twice-grid-frequency pulsation $\tilde{p}_G(t) = P_0 \cos(2\pi f_P t)$ with $f_P = 2f_G$ is then forwarded to the DC-link capacitor C_{DC}, under conventional operation, or, under the proposed MPPB approach, through the DC-link and the inverter to the motor.

Conventional Operation with Electrolytic Capacitor

First, we outline the system operation with conventional approach, utilizing a large electrolytic capacitor at the DC-link. The waveforms are shown in **Fig. 2.2(i)** for each stage.

Under constant speed $\omega(t) = \bar{\omega}$ and constant torque $t_M(t) = T_L$ operation, the motor power is constant ($p_M(t) = \omega(t)\, t_M(t) = p_{INV}(t) \equiv P_0$), as shown in **Fig. 2.2(e.i)**. With this constant power P_0 and the twice-line-frequency power pulsation, from the grid input, a large intermediate DC-link capacitor C_{DC} is used to cover for the active power mismatch between the two stages, where the instantaneous capacitor power is:

$$p_C(t) \equiv p_G(t) - p_M(t) = \tilde{p}_G(t) = P_0 \cos(2\pi f_P t) \tag{2.3}$$

and the average capacitor power is zero, $P_C = \bar{p}_C(t) = 0\,\mathrm{W}$, as it must be for periodic steady-state (see **Fig. 2.2(d.i)**).

With a nearly-constant DC-link voltage $v_{DC}(t) \approx \bar{v}_{DC}$ and under the power balance of the capacitor $p_C(t) = v_{DC}(t)\, i_C(t)$, the capacitor current must have an approximately sinusoidal waveform $i_C \approx \tilde{p}_G(t)/\bar{v}_{DC}$ with amplitude $\hat{I}_C \approx P_0/\bar{v}_{DC}$. This capacitor current causes a voltage ripple with amplitude

Δv_{DC}, which is typically limited to a certain percentage of the DC-link voltage v_{DC} to provide a nearly-constant voltage (as previously assumed) to the inverter. The required capacitance value C_{DC} is:

$$C_{\mathrm{DC}} = \frac{P_0}{2\pi f_{\mathrm{P}}} \frac{1}{\bar{v}_{\mathrm{DC}} \Delta v_{\mathrm{DC}}}, \tag{2.4}$$

and, for this application, a value in the mF range is required. This large capacitance value is, therefore, typically realized with electrolytic capacitors. The capacitor current, in addition to causing the voltage ripple, also results in a low-frequency Root Mean Square (RMS) current stress of the capacitor of $I_{\mathrm{C,LFrms}} = \hat{I}_{\mathrm{C}}/\sqrt{2} = P_0/\bar{v}_{\mathrm{DC}}\, 1/\sqrt{2}$.

For the nominal operating point of $f_{\mathrm{G}} = 50\,\mathrm{Hz}$, $\bar{v}_{\mathrm{DC}} = 650\,\mathrm{V}$ (see **Table 2.3**), $P_0 = 8\,\mathrm{kW}$ and a selected $\Delta v_{\mathrm{DC}} = 20\,\mathrm{V}$ (see **Fig. 2.2(d.i)**), the required capacitance is $C_{\mathrm{DC}} = 0.98\,\mathrm{mF}$ with a current stress of $I_{\mathrm{C,LFrms}} = 8.7\,\mathrm{A}$. This DC-link capacitance can be realized with four 1 mF capacitors *B43742A6108M000* [91] (rated for 500 V and 4.9 A at 105 °C), which are connected in a 2 x 2 array. This DC-link capacitor alone corresponds to a box volume of 1 l (61 in^3) and 6 W of losses before including the PFC and VSD high-frequency currents. We see, then, that the large — and required — electrolytic DC-link capacitor is a major limitation for power density, motor-integration, and converter lifetime [58, 60].

To overcome these limitations, alternate capacitor-based Power Pulsation Buffer (PPB) buffer concepts have been proposed in the literature [61]. These circuits all contain an active switching stage and a buffer capacitor stage (often separate, in series or in parallel, from the existing DC-link capacitor [62–65]) with a capacitor cycled with a large voltage ripple Δv_{C}. With a larger voltage ripple, the required capacitance value is much smaller (according to **Eqn. (2.4)**) and enables foil- or ceramic-based capacitor implementations, but the additional active switching stages incur significant realization effort, complexity, and cost for the overall drive system.

Motor Power Pulsation Buffer (MPPB) Concept

Rather than adding complexity to the drive system's electronics, the pulsating power component $\tilde{p}_{\mathrm{G}}$ can be removed from the converter system by enforcing $p_{\mathrm{C}}(t) \equiv 0\,\mathrm{W}$, rather than only enforcing the periodic steady-state condition $\bar{p}_{\mathrm{C}}(t) \equiv 0\,\mathrm{W}$. This condition is shown in **Fig. 2.2(d.ii)**. With this constraint and the power balance of **Eqn. (2.2)**, the only possible result is to forward to complete input power through the DC-link and the inverter to the motor [80]. The motor, then, is no longer operated

with a constant output power, but with the pulsating grid power itself as $p_M(t) = \omega(t)\, t_M(t) \equiv p_G = P_0\,[1 + \cos(2\pi f_P t)]$.

Due to the motor inertia J_M (and any additional load inertia), the speed ω changes slowly ($\omega(t) \approx \bar{\omega}$), resulting in a pulsating torque $t_M(t) \approx p_G(t)/\bar{\omega}$ at twice the grid frequency (**Fig. 2.2(e.ii)**). When the instantaneous input power is larger than the average power, positive torque is applied to the inertia and the rotating mass is accelerated (speed increases), with the excessive power stored as an increase in kinetic energy $e_{KIN} = J_M\omega^2/2$. In the other part of the mains period, when the input power drops below the average power, negative torque is applied and the rotating mass is decelerated. This causes a pulsating rotational speed $\omega(t)$ with an average $\bar{\omega}$, analogous to the DC-link voltage in the conventional system, where the amplitude of the speed ripple $\Delta\omega$ is (and recalling $P_0 = \bar{\omega} T_L$, where T_L is the load torque):

$$\Delta\omega \approx \frac{1}{2\pi f_P}\,\frac{P_0}{\bar{\omega} J_M} = \frac{1}{2\pi f_P}\,\frac{T_L}{J_M}. \tag{2.5}$$

This concept buffers the pulsating power in the inertia of the motor, an approach we call Motor-Integrated Power Pulsation Buffer. The basic operation is similar to the working principle of conventional single-phase motors [92, 93], although with the VSD capabilities required here and for most modern motors.

Another way to conceive of the approach, then, is that the motor acts as both a drive and a flywheel, which are used independently for peak power reduction in traction systems [94, 95], peak power supply within railway grids [96], smoothing of the output power of renewable power sources like wind power [97], or within dynamic voltage restorers [98]. Because low-speed motors have a large moment of inertia J_M and high-speed motors have high rotational speeds ω, the stored kinetic energy of the mechanical system is typically orders-of-magnitude larger than the required energy to buffer the electric power pulsation at the input, leading to a very small variation in the rotational speed ω around its average value $\bar{\omega}$ (for J_M according to **Table 2.2**, $\Delta\omega = 7.3$ rad/s = 70 rpm or 1.9 %). Analogous to capacitor current, though — although here with a DC offset of the average torque — the MPPB concept results in a large twice-line-frequency variation in the mechanical torque between zero and twice the average torque value. The MPPB concept offers a fundamental simplicity with the potential to significantly reduce or, theoretically, even eliminate the DC-link capacitor as energy storage.

In **Eqn.** (2.5), we observe a linear relationship between the speed ripple amplitude $\Delta\omega$ and the load torque T_L, and we need to investigate the validity of

the MPPB concept across the complete range of motor speeds. Under variable speed operation, the load torque may also depend on the current speed based on the load torque-speed-characteristic. We define this relationship around the nominal load torque $T_{\mathrm{L,N}}$ at a nominal average speed ω_{N}, with an exponential dependence between torque and speed as $T_{\mathrm{L}} = T_{\mathrm{L,N}} \left(\bar{\omega}/\omega_{\mathrm{N}}\right)^k$. The speed ripple under MPPB operation can then be defined as:

$$\Delta\omega \approx \frac{1}{2\pi f_{\mathrm{P}}} \frac{T_{\mathrm{L,N}}}{J_{\mathrm{M}}\omega_{\mathrm{N}}^k} \bar{\omega}^k. \tag{2.6}$$

For $k > 1$, which includes fans, blowers, or centrifugal pumps ($k = 2$), the load torque and speed ripple grow faster than the average speed ($\Delta\omega \propto \bar{\omega}^2$), so the worst-case ripple in both absolute and relative terms occurs at the nominal speed and nominal torque operating point. For $k = 1$, the ripple amplitude scales linearly with speed ($\Delta\omega \propto \bar{\omega}$) resulting in a constant relative ripple. It is important to point out that in both cases, i.e. for $k \geq 1$, the speed ripple will be much less than the average speed ($\Delta\omega << \bar{\omega}$) at all operating points — including speeds close to zero — if the condition is met at the nominal operating point, and we can define the time-varying speed as $\omega(t) \approx \bar{\omega}$.

For applications where $0 \leq k < 1$, however, the absolute speed ripple grows slower than the average speed ($\Delta\omega \propto \bar{\omega}^k$). This may occur for a constant torque load T_{L} (the $k = 0$ condition), of which an application could be a compressor with constant back pressure [99] — the use case considered in this work. In this case, the absolute speed ripple amplitude is in a first approximation (see **Eqn. (2.6)**) independent of the speed and constant. This condition results in a lower limit on the average speed, since an instantaneous negative speed needs to be prevented for MPPB operation (to avoid a transfer of energy from the motor to the DC-link). To a first approximation, this implies a lower absolute speed limit of $\bar{\omega} - \Delta\omega = 0\,\mathrm{rad/s}$ and a lower speed limit for continuous operation of $\bar{\omega}_{\mathrm{min}} \approx \Delta\omega$ (this limit does not apply to transient operation). In the vicinity of $\bar{\omega}_{\mathrm{min}}$, however, the approximation $\omega(t) \approx \bar{\omega}$ is no longer valid. Therefore, this lower speed limit is investigated in detail in **Appendix A**.

2.2.3 Control

Relative to the conventional control technique for a two-stage system, the MPPB control can be realized with identical high-frequency current control and a modification of only the coupling in the top-level structure between the PFC rectifier and the inverter. Therefore, we start by detailing the control

structure of a conventional system and then highlight the needed modifications for the MPPB technique.

Conventional Control Overview

In conventional single-phase-supplied VSD systems, the PFC rectifier and the inverter stage are decoupled from one another by the large intermediate DC-link capacitor. The control structures are also mostly decoupled, as shown in **Fig. 2.3(a)**.

The PFC rectifier control provides a constant DC-link voltage while drawing a sinusoidal current from the grid. Firstly, the power-pulsation-associated voltage ripple in the measured signal is eliminated, either by a Moving-Average Filter (MAF) [100] (shown here) or a conventional low-pass filter. The output of this filter, the obtained average value $\bar{v}_{\mathrm{DC}}$, is then compared to the reference V^*_{DC} and the DC-link voltage control derives the average capacitor power P^*_{C}, which can be taken as the average grid power P^*_{G} and is then used to generate the input current reference i^*_{G} for the grid current controller [101]. This results in the duty-cycle for the boost stage d_{B} and the corresponding switching state of the unfolder leg S_{UN}.

The task of the inverter control is to track the speed reference ω^*, a target that is typically accomplished with a control structure in the dq-coordinate system [102]. The speed control results in the reference motor torque T^*_{M}, or as shown here, in the reference motor power $P^*_{\mathrm{M}} = \omega^* T^*_{\mathrm{M}}$. Considering a rotor field-oriented control in a rotating dq-reference frame [103] this request can be translated to the torque generating current I^*_{Mq} by the torque constant k_{T} or, based on the power balance $P^*_{\mathrm{M}} = 3V_{\mathrm{P}}I^*_{\mathrm{Mq}}/2$, where V_{P} is the induced voltage (assumed proportional to the reference speed and aligned with the q-axis) and the dq-quantities correspond to the phase amplitudes. The motor current control, in the end, determines the duty cycles d_{a}, d_{b} and d_{c} of the inverter switching stages.

In the conventional approach, the DC-link capacitor compensates the difference of the instantaneous grid power $p_{\mathrm{G}}(t)$ and motor power P_{M}, so only the average power of the grid P_{G} and the inverter P_{M} have to be equal. To achieve this, the conventional control structure typically employs a feed-forward of the average motor power P^*_{M}, where the inverter stage directly informs the rectifier stage about the needed output power (**Fig. 2.3(a)**) and thus improves the control performance of the PFC rectifier. For PFC operation, P^*_{G} is not allowed to vary within a grid period T_{G}, which requires a slow

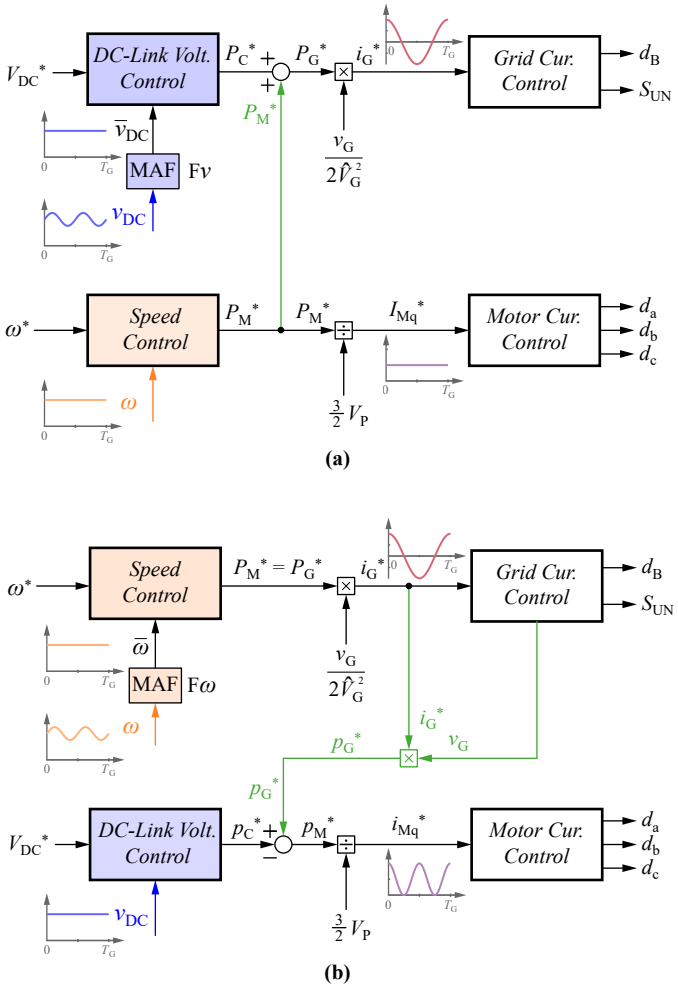

Fig. 2.3: Simplified control structure of **(a)** a conventional implementation of a single-phase-supplied VSD with an electrolytic capacitor and **(b)** the proposed MPPB concept without an electrolytic capacitor. Feedforward signals improve the control quality and are highlighted in green, with characteristic waveforms over one grid period shown adjacent to the relevant control signals.

DC-link voltage control and a bandwidth limited feedforward (or could be achieved with an additional low-pass filter, which is not shown here).

MPPB Control Overview

For the proposed MPPB control structure, the average grid power P_G must still match the average motor power P_M, as $P_G = P_M = P_0$. Here, though, the power pulsation is buffered by the motor inertia, causing a (small) speed ripple that should be eliminated in the signal measurement, as the DC-link voltage ripple was in the conventional control scheme.

The speed controller, then — which drives the required average motor power P_M^* from the difference between the reference speed ω^* and average speed $\bar{\omega}$ — defines the grid power $P_M^* = P_G^*$ and, therefore, the grid current i_G^* (see **Fig. 2.3(b)**). Again, P_G^* must be bandwidth limited (here, slow speed control) to prevent a distortion of the grid current.

The instantaneous input power $p_G^* = v_G i_G^*$ is derived and feedforwarded to the motor control, resulting in the time-varying q-current i_{Mq}^* that causes the torque pulsation. Here, though, a stable DC-link voltage v_{DC} must be ensured, and the DC-link voltage control block achieves this by deriving the instantaneous reference power p_C^* from the reference value V_{DC}^* and the unfiltered measurement v_{DC}.

According to the power balance **Eqn. (2.2)**, this quantity is then subtracted for the instantaneous motor power request:

$$p_M^*(t) = p_G^*(t) - p_C^*(t). \tag{2.7}$$

We see the elegance of the MPPB approach, then, which utilizes identical control blocks connected in a different configuration. The MPPB control, then, can be implemented with only software modifications and could even be retrofitted into existing deployments.

MPPB Control Details

In the proposed approach, the primary challenge is that the speed control defines the average grid power but the inverter must ensure that the *instantaneous* input power is forwarded to the motor — otherwise, with a small DC-link capacitance, the difference could charge the DC-link capacitor rapidly and lead to catastrophic failures. To address this critical challenge and highlight the other details of the MPPB control technique, the simplified control structure of **Fig. 2.3(b)** is extended and shown together with the power topology in **Fig. 2.4**.

To achieve high quality for both power and current alongside a high dynamic control at the output, the control structures are realized in a cascaded fashion. The outer loops for speed and DC-link voltage control provide the current setpoints for the grid and motor current control inner loops, with the motor current control implemented in the dq-coordinate system [102] using the mechanical rotor angle ε [103] provided by the encoder of the PMSM.

This encoder angle is also used to derive the instantaneous speed ω, shown at the bottom of **Fig. 2.4**, which is then filtered by a MAF [100] with $T_{\mathrm{MAF}} = T_{\mathrm{P}} = T_{\mathrm{G}}/2$ to eliminate the speed ripple in the measured signal. Inside the speed control block, $\bar{\omega}$ is compared to the reference ω^* and the speed controller Rω derives the reference average motor torque T_{M}^*, which results in the reference average motor power $P_{\mathrm{M}}^* = T_{\mathrm{M}}^* \omega^*$ and the average grid power as $P_{\mathrm{G}}^* = P_{\mathrm{M}}^*$.

The grid current controller requires the grid current reference as an input, which is translated from P_{G}^* using the power balance of the grid $\hat{I}_{\mathrm{G}}^* = 2P_{\mathrm{G}}^*/\hat{V}_{\mathrm{G}}$. This result is then limited to a maximum current amplitude $\hat{I}_{\mathrm{Gmax}}$, which is the minimum of *(a)* the maximum rectifier input current and *(b)* the current amplitude that corresponds to the power the inverter can deliver to the motor (the sum of the instantaneous mechanical output power and the system losses). The instantaneous grid current request, then, results from $i_{\mathrm{G}}^* = v_{\mathrm{G}} \hat{I}_{\mathrm{G}}^*/\hat{V}_{\mathrm{G}}$ and equals the inductor current as $i_{\mathrm{L}}^* = i_{\mathrm{G}}^*$. The grid current controller RiL compares the requested current to the measured inductor current, adds the resulting boost inductor voltage v_{LB}^* to the measured terminal voltage v_{G}, and translates this sum to the boost duty-cycle d_{B} and the switching state of the unfolder S_{UN}. For interleaved boost bridge-legs, an additional balancer control unit would need to be included [104].

The power feedforward term $p_{\mathrm{G}}^* = v_{\mathrm{G}} i_{\mathrm{G}}^*$ to the motor current control block, subsequently, is derived from the measured terminal voltage v_{G} and the reference grid current i_{G}^*. This feedforward term significantly reduces the control effort of the DC-link voltage controller, where the capacitor power request p_{C}^* is derived from the DC-link voltage reference V_{DC}^* and the measured and unfiltered DC-link voltage v_{DC}. The reference motor power p_{M}^*, the input to the motor current controller, results then from **Eqn. (2.7)**.

The motor current controller, here, avoids field weakening [105] for simplicity, and therefore $i_{\mathrm{Md}}^* = 0\,\mathrm{A}$ is selected and the produced torque is only proportional to the q-current i_{Mq}. The motor power balance results in $p_{\mathrm{M}}^* = 3 v_{0\mathrm{q}}^* i_{\mathrm{Mq}}^*/2$ as $i_{\mathrm{Md}}^* = 0\,\mathrm{A}$, with $v_{0\mathrm{q}}^* \approx V_{\mathrm{P}} = p \Psi_{\mathrm{PM}} \omega^*$ as the induced voltage that is dependent on the speed, the number of pole pairs p, and the permanent

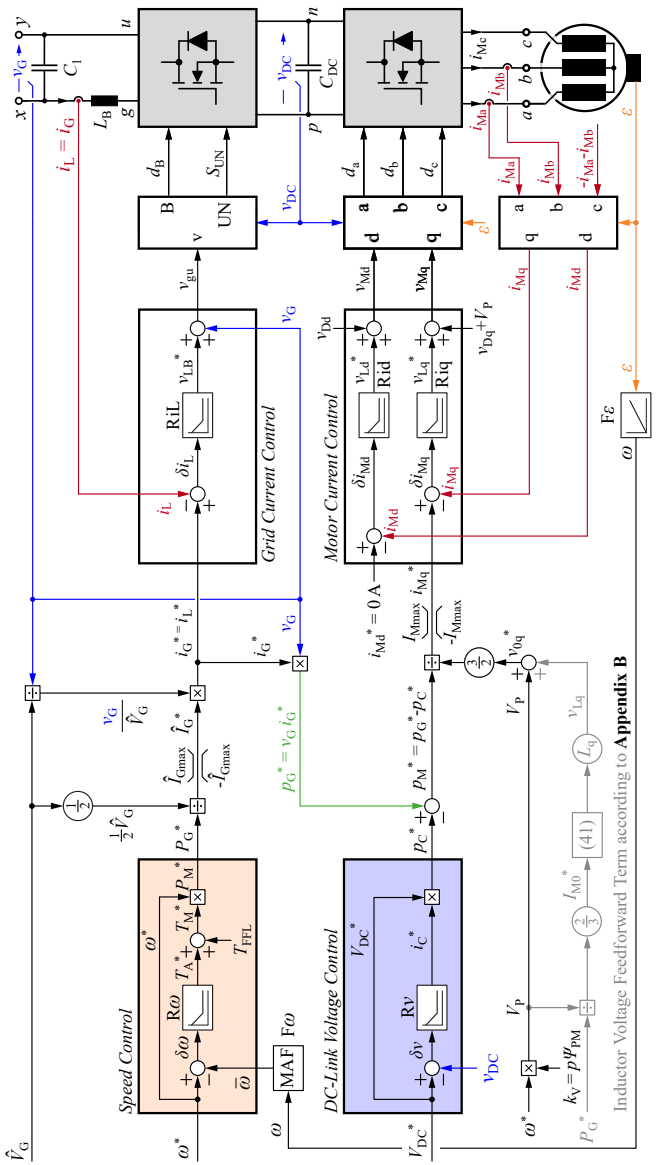

Fig. 2.4: Control structure of **Fig. 2.3(b)** with full implementation details, indicating the cascaded controller blocks, the dq-coordinate motor current control, and all required measurements. The addition of an inductor voltage feedforward term is described in **Appendix B**.

magnet flux Ψ_{PM} (or, more conventionally, the product of the latter two, the motor constant $k_V = V_P/\omega^* = p\Psi_{PM}$).

Inside the motor current controller, the current setpoints $i^*_{Md} = 0$ A and i^*_{Mq} are compared to the instantaneous current values i_{Md} and i_{Mq}, which are derived from the phase current measurements by the Park transform. The current controllers Rid and Riq then derive the reference motor inner inductor voltages v^*_{Ld} and v^*_{Lq}, which are translated to the inverter duty cycles d_a, d_b and d_c after including the motor voltage feedforward V_P and the decoupling terms $v_{Dd} = -\omega p L_q i^*_{Mq}$ and $v_{Dq} = \omega p L_d i^*_{Md}$ (which depend on the reference currents and the motor inductances L_d and L_q) for the required motor voltages v_{Md} and v_{Mq}. The motor current control supports the inclusion of an additional Common-Mode (CM) voltage component for overmodulation [106], if desired.

Simulation Results

With the concept and the detailed control structure for the proposed MPPB concept each outlined, we move to verify the approach through simulation for the nominal operating point of **Table 2.3**. We use the circuit parameters of **Table 2.2**, highlighting especially that we need only 60 µF of DC-link capacitance for an 8 kW system. The controller design for the simulation (and later, for the implementation) is described in further detail in the **Appendix B**.

The corresponding waveforms at a mechanical output power of 7.5 kW and 3700 rpm are shown in **Fig. 2.5**, where we see the grid current i_G in phase with the grid voltage v_G for unity-power-factor operation and the product of the grid current and grid voltage resulting in pulsating input power, translated to a torque pulsation. The torque t_M pulsates, as expected, around the average of $T_L = 19.4$ Nm. When $t_M(t) > T_L$, the motor speed increases, and when $t_M(t) < T_L$, the motor speed decreases, resulting here in a symmetric speed ripple amplitude of $\Delta n = \pm 61$ rpm around the average of 3700 rpm. The DC-link voltage contains a low-frequency peak-to-peak ripple of around 34 Vpkpk, a direct consequence of the limited control bandwidth of the DC-link voltage control and a limitation that can be addressed through the improvements discussed in **Appendix B**. Overall, the simulation results verify the correct and expected operation and we move to evaluate the performance of the MPPB-operated system.

2.2.4 Performance Evaluation

Aside from the significant reduction in required DC-link capacitance, the MPPB concept has no effect on the performance of the PFC rectifier or on the

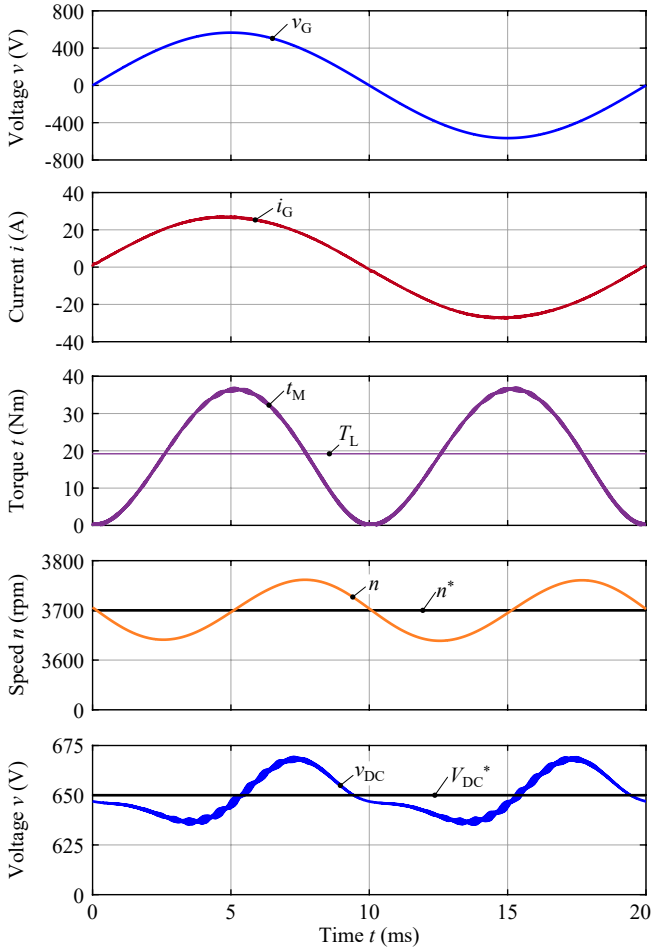

Fig. 2.5: Simulated waveforms of the grid voltage v_G, grid current i_G, motor torque t_M, rotational speed n, and DC-link voltage v_{DC} during steady-state, nominal operation, verifying the proposed MPPB concept and control structure.

performance of the EMI filter. We, therefore, analyze the effect of the proposed concept on only the motor and the inverter, starting with the time-domain impact and moving to an analysis of losses.

Time-Domain Waveforms

Under conventional operation, the magnitude of the q-current is given by $I_{M0} = 2P_0/(3V_P)$ and thus $i_{Md}(t) \equiv 0\,\text{A}$ and $i_{Mq}(t) = I_{M0}$. The phase currents are derived using the inverse Park transform [103] with $\varepsilon = p\bar{\omega}t + \varepsilon_0$:

$$\begin{bmatrix} i_{Ma} \\ i_{Mb} \\ i_{Mc} \end{bmatrix} = \begin{bmatrix} \cos(\varepsilon) & -\sin(\varepsilon) \\ \cos\left(\varepsilon - \frac{2\pi}{3}\right) & -\sin\left(\varepsilon - \frac{2\pi}{3}\right) \\ \cos\left(\varepsilon + \frac{2\pi}{3}\right) & -\sin\left(\varepsilon + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{Md} \\ i_{Mq} \end{bmatrix} \tag{2.8}$$

This results in three purely sinusoidal and symmetrical phase currents, each with the peak value I_{M0}, as shown in **Fig. 2.6(a)**. These phase currents are evaluated — and later, compared to the same values under MPPB operation — by the absolute average current I_{PH0avg}, the RMS value I_{PH0rms}, and the peak current I_{PH0pk} as (with T the minimum period of the signal):

$$I_{PH0avg} = \frac{1}{T}\int_0^T |i_{Ma}(\tau)|d\tau = \frac{2}{\pi}I_{M0} \tag{2.9}$$

$$I_{PH0rms} = \sqrt{\frac{1}{T}\int_0^T i_{Ma}^2(\tau)d\tau} = \frac{1}{\sqrt{2}}I_{M0} \tag{2.10}$$

$$I_{PH0pk} = \max i_{Ma}(t) = I_{M0}. \tag{2.11}$$

To analyze the proposed MPPB operation, we assume constant speed (with $\omega(t) \approx \bar{\omega}$), which results in a constant induced voltage $V_P = k_V\omega \approx k_V\bar{\omega}$, and the instantaneous q-current is $i_{Mq}(t) = 2p_M(t)/(3V_P)$. Using $p_M(t) = P_0\,[1 + \cos(2\pi f_P t)]$, we get the q-current proportional relationship to the instantaneous torque:

$$i_{Mq}(t) \approx I_{M0}\,[1 + \cos(2\pi f_P t)] \propto t_M(t), \tag{2.12}$$

where the magnitude I_{M0} is the same as under conventional operation.

Because the q-current is now, under MPPB operation, pulsating at twice-line-frequency, the phase currents i_{Ma}, i_{Mb} and i_{Mc} into the motor are no longer purely sinusoidal. These phase currents are found by applying the

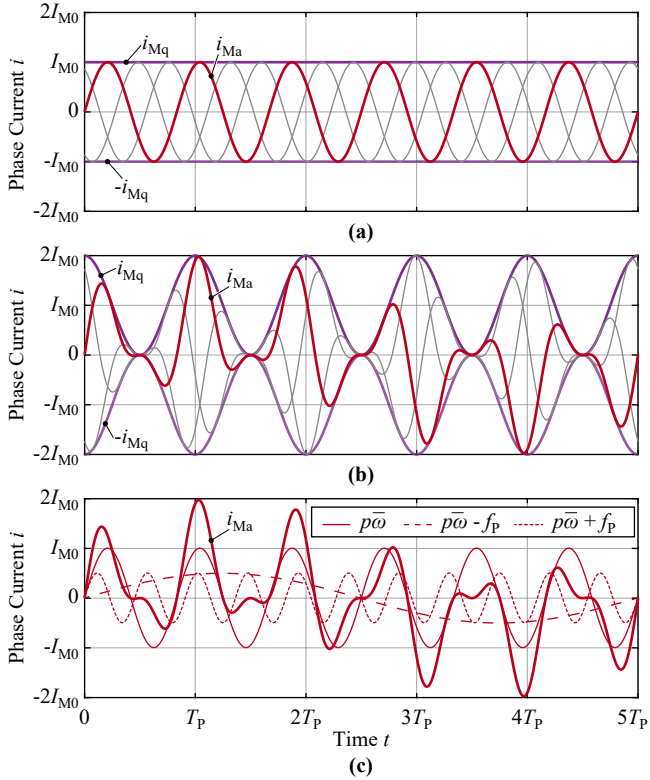

Fig. 2.6: Phase currents i_{Ma}, i_{Mb}, and i_{Mc} and the enveloping currents $\pm i_{Mq}$ for the **(a)** conventional and **(b)** MPPB operation for $f_P = 100\,\text{Hz}$ and $p\bar{\omega}/(2\pi) = 120\,\text{Hz}$. **(c)** Spectral decomposition of the first phase current i_{Ma} under MPPB operation.

inverse Park transform to the q-current, and are shown in **Fig. 2.6(b)** for $f_\text{P} = 100\,\text{Hz}$ and $p\bar{\omega} = 2\pi 120\,\text{Hz}$. The phase current, more precisely, is then $i_\text{Ma} = -i_\text{Mq} \sin(p\bar{\omega}t + \varepsilon_0)$, or:

$$\begin{aligned} i_\text{Ma}(t) &= -I_\text{M0} \sin(p\bar{\omega}t + \varepsilon_0) \\ &- \frac{I_\text{M0}}{2} \left[\sin(p\bar{\omega}t + 2\pi f_\text{P} t + \varepsilon_0) + \sin(p\bar{\omega}t - 2\pi f_\text{P} t + \varepsilon_0)\right]. \end{aligned} \tag{2.13}$$

In addition to the fundamental $p\bar{\omega}$ frequency, the phase currents now contain two additional harmonic components at the frequencies $|p\bar{\omega} + 2\pi f_\text{P}|$ and $|p\bar{\omega} - 2\pi f_\text{P}|$ with amplitude $I_\text{M0}/2$, as shown with the spectral decomposition of the phase current for phase a in **Fig. 2.6(c)**. For certain frequency ratios, we note that these individual sines may collapse into a single frequency, become DC-components, or even result in standing waves and an asymmetric phase stress. The precise effect of different frequency ratios is discussed in **Appendix C**, where we find that such effects occur only in the vicinity of certain speed values $\bar{\omega}$, which are all below or equal to the angular pulsation frequency $\omega_\text{P} = 2\pi f_P$, and we proceed under the assumption $|p\bar{\omega}| > \omega_\text{P}$ for the remaining analysis here.

We find that only the sinusoidal with frequency $p\bar{\omega}$ is phase-aligned with the induced voltage of the corresponding phase, and therefore only this component generates average torque to drive the load. Because this component is not influenced by the pulsating q-current, there is, as expected, no degradation in the mechanical average torque — but the additional components do increase current stress in the inverter and motor. The RMS current stress is calculated by a superposition of the purely-sinusoidal waveforms, with a $\sqrt{3/2}$ factor increase in RMS current. The average current remains unchanged while the peak current doubles as a result of the pulsating q-current. This large increase in peak current has a limited effect on the iron in the motor, since motors are typically designed in the thermal (rather than the saturation) limit and the flux is primarily defined by the permanent magnet Ψ_PM. The key current equations are summarized below and the relative increase of each current are shown in **Fig. 2.7(a)**.

$$I_\text{PHavg} = \frac{1}{T}\int_0^T |i_\text{Ma}(\tau)| d\tau = \frac{2}{\pi} I_\text{M0} \tag{2.14}$$

$$I_\text{PHrms} = \sqrt{\frac{1}{T}\int_0^T i_\text{Ma}^2(\tau) d\tau} = \frac{1}{\sqrt{2}}\sqrt{\frac{3}{2}} I_\text{M0} \tag{2.15}$$

$$I_{\mathrm{PHpk}} = \max\, i_{\mathrm{Ma}}(t) = 2I_{\mathrm{M0}}. \tag{2.16}$$

With the key current ratios defined, we move to analyze the relative inverter and motor losses between conventional and MPPB operation.

Motor Loss Analysis

The motor losses P_{VM} include both speed-dependent no-load losses P_{VMnl} and load-dependent conduction losses $P_{\mathrm{VMcond}} = 3R_{\mathrm{s}}I^2_{\mathrm{PHrms}}$, with R_{s} as the stator winding resistance. The motor losses under conventional operation P_{VM0} and under the proposed MPPB operation P_{VM} are:

$$P_{\mathrm{VM0}} = P_{\mathrm{VMnl}} + \frac{3}{2}R_{\mathrm{s}}I^2_{\mathrm{M0}} \tag{2.17}$$

$$P_{\mathrm{VM}} = P_{\mathrm{VMnl}} + \frac{9}{4}R_{\mathrm{s}}I^2_{\mathrm{M0}}, \tag{2.18}$$

where the MPPB operation incurs a 50% loss increase in conduction losses due to the increase in RMS current. If we assume an equal loss distribution between the no-load losses and the load-dependent conduction losses at the nominal operation point, which is typically close to an optimum design, MPPB operation incurs a motor loss penalty of only 25 %. This loss ratio, along with the inverter loss ratios of the next Section, is shown in **Fig. 2.7(b)**.

Inverter Loss Analysis

The inverter semiconductor losses P_{VI} comprise conduction P_{VIcond} and switching losses P_{VIsw}. The conduction losses are, most generally, written as $P_{\mathrm{VIcond}} = 3V_{\mathrm{f}}I_{\mathrm{PHavg}} + 3R_{\mathrm{on}}I^2_{\mathrm{PHrms}}$, where V_{f} is the on-state voltage drop and R_{on} is the (differential) on-resistance. The switching losses are written with a quadratic loss function $e_{\mathrm{sw}}(i) = k_0 + k_1 i + k_2 i^2$ [88, 108], which leads to $P_{\mathrm{VIsw}} = 3f_{\mathrm{Isw}}\left(k_0 + k_1 I_{\mathrm{PHavg}} + k_2 I^2_{\mathrm{PHrms}}\right)$ with the inverter switching frequency f_{Isw}. A quick review of these equations shows that the MPPB concept would only affect the ohmic part of the conduction losses and the quadratic part of the switching losses, both with an increase of 50 %, through the increase in RMS current.

If the semiconductors are implemented as IGBTs, conduction losses are given — to a first approximation — by the on-state voltage drop and the switching losses can be approximated by the linear part alone. For an IGBT-implemented inverter, then, the inverter losses are identical between conventional (P_{VI0igbt}) and MPPB operation (P_{VIigbt}):

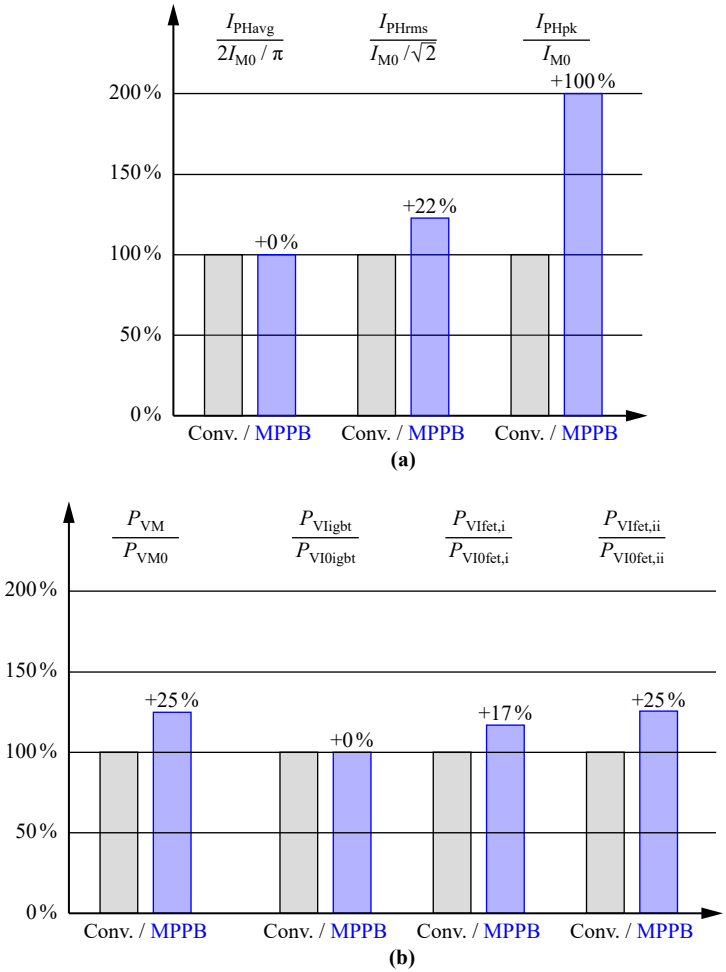

Fig. 2.7: Comparison of **(a)** loss-characteristic currents and **(b)** losses under conventional and MPPB operation at the nominal operating point. Loss penalty of the MPPB is evaluated for three inverter realizations: IGBT-based (P_{VIigbt}), MOSFET-based with external Miller capacitors to limit the $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ of the switching transitions ($P_{\mathrm{VIfet,i}}$), and MOSFET-based with explicit LC output filter stage designed for $\mathrm{d}v/\mathrm{d}t$-limitation of the voltage applied to the motor terminals [107] or full sine-wave output voltage shaping ($P_{\mathrm{VIfet,ii}}$).

$$P_{\mathrm{VI0igbt}} = \frac{6}{\pi} V_{\mathrm{f}} I_{\mathrm{M0}} + 3 f_{\mathrm{sw}} \frac{2}{\pi} k_1 I_{\mathrm{M0}} = P_{\mathrm{VIigbt}}. \tag{2.19}$$

IGBTs, however, suffer from high overall losses [109], and inverters with SiC MOSFET-based bridge legs and a $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ limitation should be considered too.

For a SiC MOSFET-based bridge-leg and external Miller capacitors to limit the voltage slew rate, the conduction losses can be considered ohmic and the switching losses are described well by the constant and linear part as shown in **Appendix D**, for inverter losses under conventional ($P_{\mathrm{VI0fet,i}}$) and MPPB operation ($P_{\mathrm{VIfet,i}}$) as:

$$P_{\mathrm{VI0fet,i}} = \frac{3}{2} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3 f_{\mathrm{sw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} \right) \tag{2.20}$$

$$P_{\mathrm{VIfet,i}} = \frac{9}{4} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3 f_{\mathrm{sw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} \right). \tag{2.21}$$

The motor acts as a resistive-inductive load with a reactive power demand, and therefore requires a current commutation path for the freewheeling current. The high voltage drop of the body diode of the utilized SiC MOSFETs is typically overcome with an anti-parallel SiC Schottky diode, but the MOSFET itself can also be utilized as a synchronous rectifier. In this case, the freewheeling diode only conducts during the dead time, and the additional losses from the body diode conduction can be neglected (this assumption is extensively analyzed in [110] and verified in **Section 2.3**). In this context, it should be also mentioned that early high-voltage SiC MOSFETs were associated with bipolar degradation on their intrinsic body diodes [111], but this problem has been solved for state-of-the-art 1.2 kV devices [112].

We see that conduction losses increase by 50% under the proposed MPPB operation. If we assume that each loss contribution (conduction, constant switching losses, and current-dependent switching losses) is 1/3 of the overall inverter losses, see **Appendix D**, at nominal operation, the inverter loss penalty is around 17 % for MPPB operation with a SiC MOSFET-based bridge leg and external Miller capacitors to limit the voltage slew rate.

Finally, we consider a realization with a hard switching SiC MOSFET-based bridge-leg with LC output filter designed for $\mathrm{d}v/\mathrm{d}t$-limitation of the voltage applied to the motor terminals [107] or full sine-wave output voltage shaping. We first note that the doubling of the peak current will negatively impact the performance of the filter inductor. Here, conduction losses remain

ohmic and the switching losses contain all of the terms, for conventional ($P_{\mathrm{VI0fet,ii}}$) and MPPB inverter losses ($P_{\mathrm{VIfet,ii}}$) of:

$$P_{\mathrm{VI0fet,ii}} = \frac{3}{2} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3 f_{\mathrm{sw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} + \frac{1}{2} k_2 I_{\mathrm{M0}}^2 \right) \tag{2.22}$$

$$P_{\mathrm{VIfet,ii}} = \frac{9}{4} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3 f_{\mathrm{sw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} + \frac{3}{4} k_2 I_{\mathrm{M0}}^2 \right). \tag{2.23}$$

If we consider an equal loss contribution of all four loss components (conduction losses and the three switching loss terms) at nominal operation, MPPB operation carries a 25 % loss penalty over conventional operation for the inverter, similar to the penalty in the motor.

A summary of these inverter loss penalties for different bridge-leg implementations are shown **Fig. 2.7(b)**, where we see that, although the MPPB concept increases the conduction losses by 50%, the maximum total loss penalty is 25 % — while realizing a potential volume reduction of up to 1 L (or 61 in^3) by eliminating the DC-link electrolytic capacitors.

2.3 System Design and Implementation

With the power density improvements — and possibility of motor integration — of the MPPB-operated system attractive, we move to design and implement the system proposed of **Fig. 2.2(a)**. This hardware demonstrator will allow a direct comparison between conventional and MPPB systems on volume and loss distributions. We focus on the motor-integrated converter system in this Section, with brief guidelines for motor selection and PFC rectifier and inverter designs.

2.3.1 Motor Selection and Characterization

With the output power $P_{0,\mathrm{N}} = 7.5\,\mathrm{kW}$ and speed requirements $n_{\mathrm{N}} = 3700\,\mathrm{rpm}$ leading to a torque specification of $T_{\mathrm{L,N}} = 19.4\,\mathrm{Nm}$, we select *1FT7-084* from Siemens [113].

At nominal operation $n_{\mathrm{N}} = 3700\,\mathrm{rpm}$, the motor frequency with $p = 5$ is $p\omega_{\mathrm{N}} = 2\pi\ 308\,\mathrm{Hz}$, which is sufficiently above $f_{\mathrm{P}} = 100\,\mathrm{Hz}$ to guarantee symmetric phase stresses in the motor and inverter (see **Appendix C**). The motor inertia of $J_{\mathrm{M}} = 4.5\,\mathrm{mkgm}^2$ corresponds to a speed ripple amplitude, using **Eqn. (2.5)**, of $\Delta\omega = 7.3\,\mathrm{rad/s} = 70\,\mathrm{rpm}$, or 1.9 % of the nominal speed. The minimal achievable speed in stationary operation for constant torque

$T_L(\omega) = T_{L,N}$ is, according to **Appendix A**, $\bar{\omega}_{min} = 5\,\text{rad/s} \approx 50\,\text{rpm}$. The torque constant is given with $k_T = T/I_{M0} = 0.92\,\text{Nm/A}$, and the given speed constant k_V, which relates the induced pole-wheel peak voltage V_P to the speed n as $k_V = V_P/n = 67.8\,\text{mV/rpm}$, resulting in a nominal phase voltage amplitude of $V_{P,N} = 250\,\text{Vpk}$. The nominal DC-link voltage can then be selected as $V_{DC,N} = 650\,\text{V}$, allowing boost PFC operation up to the nominal input voltage of $V_{G,N} = 400\,\text{Vrms}$ with a 15 % margin. For input voltages above nominal, the DC-link voltage is linearly increased up to 800 V at $V_{Gmax} = 530\,\text{Vrms}$, or a peak voltage of 750 Vpk.

The motor is measured to validate the datasheet and build a complete loss model. The stator phase resistance is measured at $R_s = 0.2\,\Omega$ at 40 °C (close to ambient since the winding temperature does not significantly increase during short-time operation and is also respected for the experimental analyses) and the motor inductances are measured at $L_d \approx L_q \approx 3.0\,\text{mH}$, both within 10 % of the datasheet values. The speed-dependent, no-load losses from iron losses and friction [114] are measured with the motor driven mechanically and the torque measured at nominal speed n_N, resulting in a no-load torque of $T_{Mnl} = 0.765\,\text{Nm}$ and no-load losses of $P_{VMnl} = \omega_N T_{Mnl} = 296\,\text{W}$.

At nominal speed, the motor current amplitude is $I_{M0} = (T_L + T_{Mnl})/k_T$, which at nominal load is $I_{M0,N} = 21.9\,\text{A}$. Under conventional operation, this RMS phase current is $I_{PH0rms,N} = I_{M0,N}/\sqrt{2} = 15.5\,\text{Arms}$ (cf. **Eqn. (2.10)**) and under the proposed MPPB operation, the phase current is $I_{PHrms,N} = \sqrt{3} I_{M0,N}/2 = 19\,\text{Arms}$ (cf. **Eqn. (2.15)**). With the no-load losses summed with the conduction losses for the total motor losses $P_{VM} = P_{VMnl} + P_{VMcond}$, or:

$$P_{VM} = \omega_N T_{Mnl} + \frac{9}{4} R_s \left(\frac{T_L + T_{Mnl}}{k_T} \right)^2 . \tag{2.24}$$

We note that the no-load torque increases the motor losses P_{VM} twice — once directly, through the P_{VMnl} term, and additionally by increasing the motor current as T_{Mnl}/k_T and therefore increasing the conduction losses $P_{VMcond} = 9 R_s I_{M0}^2/4$.

The MPPB-operated motor losses at the average torque are shown in **Fig. 2.8**, with the nominal losses under MPPB operation of $P_{VM,N} = 517\,\text{W}$ compared to 443 W under conventional operation. This motor loss increase is 16.7 %, less than the 25 % predicted in **Fig. 2.7(b)** since the no-load losses comprise more than half of the total motor losses.

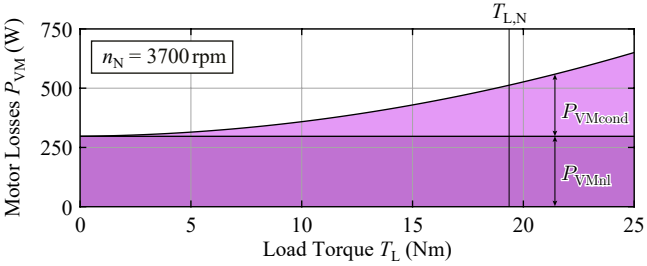

Fig. 2.8: Characterized motor losses P_{VM} under MPPB operation at load torque, comprising speed-dependent no-load losses P_{VMnl} and torque/current-dependent conduction losses P_{VMcond}.

2.3.2 Converter Design

The complete converter topology is shown in **Fig. 2.9** with the components of **Table 2.2**, and here we highlight the key pieces of the component selection.

Inverter Design

The inverter switching frequency must be outside the audible range (above 16 kHz [117]), but is determined more strictly by the control bandwidth. With a pulsation frequency of $f_P = 100\,\text{Hz}$, we design the DC link-voltage-control bandwidth 5× higher at 500 Hz, the motor-current-control bandwidth 5× higher than that at 2500 Hz, and the inverter switching frequency 10× higher at $f_{Isw} \approx 25\,\text{kHz}$. Due to EMI considerations [118], we select $f_{Isw} = 24\,\text{kHz}$.

1200 V power semiconductors are required to withstand a DC-link voltage that will be as high as 800 V (plus low- and high-frequency voltage ripple), and we employ SiC MOSFETs instead of IGBTs for high performance [109]. These MOSFETs operate at high voltage slew rates, or $\mathrm{d}v_{DS}/\mathrm{d}t$ values, which can lead to unequal distribution of the voltage across the motor windings and partial discharge phenomena resulting in progressive aging of the motor winding insulation [90,119]. Different solutions to this challenge are discussed and compared in [77], with gate drive modifications preferred, cf. **Appendix D**, for motor-integrated drives that support $\mathrm{d}v_{DS}/\mathrm{d}t$ values as high as 15 V/ns (since there are no cable reflections to consider).

We select the optimal chip area for the inverter power semiconductors, all of which are implemented as next-generation 16 mΩ SiC MOSFETs (*C3M0016120K* [115]). A gate driver with an output clamp variant is selected [120] that drives the transistors at the maximum positive ($V_{G,on} = 15\,\text{V}$)

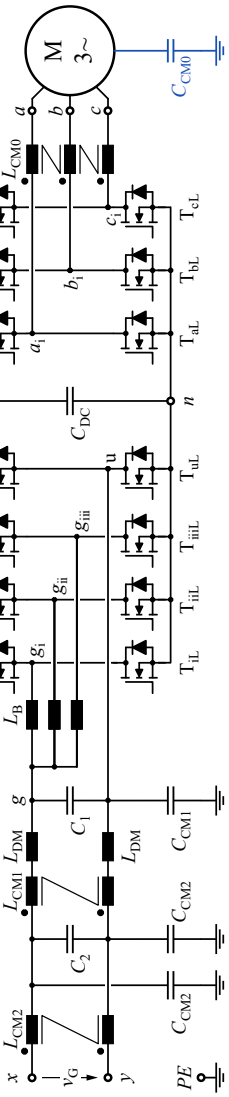

Fig. 2.9: Complete powertrain, with all included components, for the realized motor-integrated VSD system. Component list is detailed below, in **Table 2.2**.

Tab. 2.2: Component List

Motor Inertia	J_M	4.5 mkgm^2	Siemens *1FT7-084* [113]
CM-Motor Capacitor	C_{CM0}	1.9 nF	Siemens *1FT7-084* (measured)
Inverter Transistors	T_{aH}, T_{aL}, T_{bH}, T_{bL}, T_{cH}, T_{cL}	16 mΩ / 1.2 kV	Cree *C3M0016120K* [115]
PFC Unfolder Transistors	T_{uH}, T_{uL}	16 mΩ / 1.2 kV	Cree *C3M0016120K* [115]
PFC Boost Transistors	T_{iH}, T_{iL}, T_{iiH}, T_{iiL}, T_{iiiH}, T_{iiiL}	32 mΩ / 1.2 kV	Cree *C3M0032120K* [116]
DC-Link Capacitor	C_{DC}	3 × 20 µF / 900 V	Epcos *B32776E9206K000*, Foil
Boost Inductor	L_B	428 µH (each)	4 E-Cores / 30 Turns Flat Wire
DM-Filter Capacitor	C_1	4 × 1 µF	Epcos *B32914A5105M000*, X1
DM-Filter Capacitor	C_2	1 µF	Epcos *B32914A5105M000*, X1
DM-Filter Inductor	L_{DM}	4.7 µH (each)	Wuerth *74436410470*
CM-Filter Capacitor	C_{CM1}	2 × 20 nF	Vishay *440LS20-R*, Y1
CM-Filter Capacitor	C_{CM2}	2 × 20 nF (each)	Vishay *440LS20-R*, Y1
CM-Filter Inductor	L_{CM0}	75 µH	6 × VAC *L2025-W380*, 1 Turn
CM-Filter Inductor	L_{CM1}	1.6 mH	VAC *L2045-V102*, 9 Turns
CM-Filter Inductor	L_{CM2}	1.0 mH	VAC *L2045-V102*, 7 Turns

and minimum negative ($V_{G,off} = -4\,V$) gate drive voltages for enhanced noise immunity. A 15 Ω gate resistor is added for turn-on and turn-off to stay below $dv/dt = 15\,V/ns$ as investigated in **Appendix D**.

As previously mentioned, synchronous rectification is employed for the MOSFETs within the inverter [110], with the body diode therefore only conducting during the deadtime t_D. Under the worst-case condition, where the body diode conducts the full phase current within both dead time intervals of a switching period, and with the diode forward voltage drop $V_f = 4.6\,V$ [115] and the selected inverter deadtime of $t_D = 400\,ns$, the losses under nominal operation are $P_{VIdiode} = 3\,f_{sw} 2 t_D\,V_f I_{PHavg} = 3.7\,W$ (where I_{PHavg} is from **Eqn. (2.14)**). These losses represent less then 5 % of the calculated inverter losses $P_{VI} = 81.6\,W$ and can be safely neglected.

DC-Link Capacitor Selection

The minimum DC-link capacitance is determined by the high-frequency-voltage ripple caused by the PFC rectifier and the inverter [121]. Due to disturbances and the limited control bandwidth of the DC-link voltage control, though, we find a remaining low-frequency voltage ripple (see **Fig. 2.5**). This ripple could be addressed with increased bandwidth, but, in the end, this would require an increase in switching frequency and the corresponding increase in switching losses eliminates this option. Instead, to keep the peak-to-peak voltage ripple below 40 V, an increased DC-link capacitance of $C_{DC} = 60\,\mu F$ is selected based on circuit simulations. This capacitance requirement is only $7.5\,\mu F/kW$.

The chosen capacitors must be rated for at least 800 V, eliminating both ceramic *X6S* capacitors (which are only available up to 400 V, and would therefore requires hundreds of series-stacked capacitors) and *CeraLink* capacitors, where only small capacitance values are available. We select three 20 µF foil capacitors *B32776E9206K000* [122], resulting in a total volume of only 0.13 L (or $8\,in^3$) — equal to just 13% of the required electrolytic capacitor volume under conventional operation.

PFC Rectifier Design

Because the rectifier is not affected by the MPPB approach, we implement a conventional PFC rectifier design [59] (even in [59], the electrolytic capacitors comprise 25% of the overall converter volume!). This rectifier must be designed to provide the maximum power across the entire input voltage range (see **Fig. 2.1(b)**), with a maximum input current of 32 Arms (or 45 Apk).

The unfolder is implemented with the lowest-possible $R_{DS,on}$ device *C3M0016120K* [115], which results in a maximum of 19.6 W of conduction losses at the voltage minimum and 9.6 W at nominal operation. To limit the component stresses of the high-frequency bridge-leg, which is subject to high-frequency switching losses, we select an interleaved design with three branches. This supports an increase in effective switching frequency for the same semiconductor losses [123], an improved loss distribution, and the reuse of the design for future three-phase-supplied VSD systems. Each bridge-leg is operated with a switching frequency of 48 kHz to keep the frequency multiple below the stricter EMI considerations at 150 kHz. The high-frequency bridge-leg power semiconductors are again selected with the optimal chip area and implemented with 32 mΩ 4-pin devices (*C3M0032120K* [116]) for bridge-leg losses of $P_{VRhb} = 8.8$ W at nominal operation.

The PFC rectifier inductor design is selected from the optimal front of a Pareto optimization based on the guidelines of [124], and this selected inductor is implemented with 4 stacked *K4317E040* Kool-Mu cores with relative permeability of 40 and 30 turns of flat wire (7 mm × 0.5 mm) (note that the permeability of KoolMu is current-dependent, and the inductance varies between 428 µH and 342 µH [125]). The inductor has a boxed volume of 100 cm^3 (33.6 x 41.5 x 72 mm) and $P_{VRind} = 9.5$ W of expected losses at the nominal operating point. The filter capacitor C_1 is subject to a current ripple at the interleaved frequency of 144 kHz, with the first and second harmonic cancelled, and 4 µF capacitance is selected with an implementation of four parallel X-rated 1 µF capacitors.

EMI filter

This high-frequency bridge-leg interleaving also eliminates the 4^{th} and 5^{th} harmonic components, and the Differential-Mode (DM) EMI filter therefore needs to be designed to meet CISPR 11 / Class A [46] at the DM noise of the PFC rectifier at 288 kHz. With the design guidelines of [126], we find that CISPR 11 / Class A can be met with $C_2 = 1$ µF and $L_{DM} = 4.7$ µH.

The common-mode noise is typically defined by the parasitic capacitance to earth, which is often dominated by the thermal-interface-material layer between the power semiconductors and the grounded heatsink. Here, the largest parasitic capacitance originates from the motor [127] at $C_{CM0} = 1.9$ nF. The CM EMI filter, therefore, is designed for the inverter noise occurring at the 7^{th} harmonic of 168 kHz. Again, following the design of [126], we find that $C_{CM1} = C_{CM2} = 40$ nF, $L_{CM1} = 1.2$ mH, and $L_{CM2} = 0.8$ mH meets CISPR 11 / Class A at 168 kHz. Both CM inductors are evaluated at 168 kHz, and they

Tab. 2.3: Nominal Operating Point

Nominal Speed (n_N)	3700 rpm
Nominal Mech. Power, Grid ($P_{0,N}$)	7.5 kW
Nominal Grid Voltage ($V_{G,N}$)	400 Vrms
Grid Frequency (f_G)	50 Hz
DC-Link Voltage (V_{DC})	650 Vdc

employ *L2045-V102* nanocrystalline cores [128] with 7 and 9 turns, respectively. An additional CM choke on the motor side L_{CM0} — to damp high-frequency CM currents inside the system and reduce the potential for radiated emissions [129] — is implemented with six *L2025-W380* [128] cores with one turn each and provides a series impedance of 75 µH inductance and a damping resistance of 100 Ω at 168 kHz.

2.3.3 Volume and Loss Distribution

These selected components are summarized in **Table 2.2**, resulting in the system loss breakdown at the nominal operating point (**Table 2.3**) of **Fig. 2.10(a)**. We see that the rectifier (P_{VR} = 74.9 W) and inverter (P_{VI} = 81.6 W) stages comprise a nearly-equal contribution to the system losses, which are dominated by the motor (P_{VM} = 534 W). Beyond the no-load and conduction losses characterized in **Fig. 2.8**, the motor incurs an additional 16.6 W of capacitive switching losses, where the parasitic motor capacitance is charged and discharged with the PWM voltage impressed by the inverter bridge-legs. The total drive system losses are P_{VDS} = 703 W, corresponding to a system efficiency at nominal operation of η_{DS} = 91.4 %.

The volume distribution of the system is shown in **Fig. 2.10(b)**, where we see a boxed volume of the complete drive system (incl. the motor) at 8.2 L (or 500 in^3) resulting in a power density of 0.91 kW/L (15 W/in^3). The outer motor dimensions are 205 mm × 105 mm × 105 mm, for a total boxed volume of 4.9 L (or 300 in^3) that is 60 % of the system. The converter, at 3.3 L (or 200 in^3) , accounts for the remaining 40 % of the system volume (including the encoder). Without the MPPB concept, the electrolytic capacitor volume *alone* would account for 1 L (or 61 in^3), adding 30 % to the converter and 12 % to the total system — and preventing integration due to the lifetime considerations discussed previously.

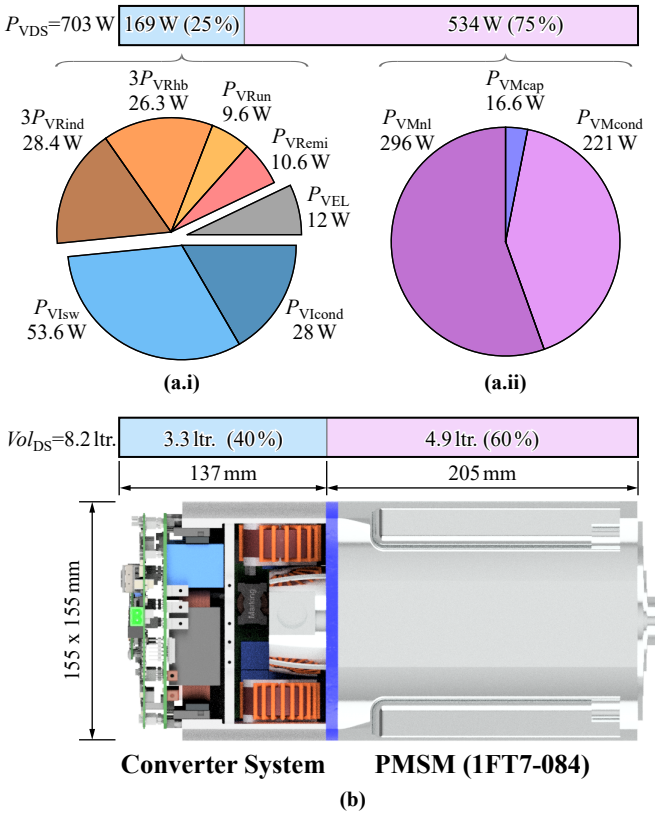

Fig. 2.10: (a) Loss breakdown at the nominal operating point for the **(i)** inverter and **(ii)** motor. **(b)** Volume distribution for the realized demonstrator.

2.3.4 Detailed Motor Integration and Implementation

The motor integration must allow a retrofitting of an existing motor within the same flange dimension, mandating an axial stator mount of the power electronics system (options for motor integration are surveyed in [130]). The implementation is shown in **Fig. 2.11**, with the 3-level stackup and construction detailed side-by-side.

Firstly, the end plate is replaced to provide an interface for the converter system. The first level of the integrated drive system (**Fig. 2.11(a)**) contains the EMI filter components, which are distributed around the encoder. Cables are mounted to the corresponding side walls to connect to the grid CM inductors, which are also connected to the filter Printed Circuit Board (PCB). The filter PCB contains all of the remaining DM and CM filter components, and is connected to earth and the motor housing. An earth- and housing-connected copper plate (not shown) is installed between the EMI filter and the motor-side CM inductor to provide shielding, and similarly, an aluminium plate is installed between the first and second levels to *(a)* shield the filter from the bridge-leg high-frequency noise and *(b)* provide mechanical stability.

The second converter level (**Fig. 2.11(b)**) contains all power components, including the power semiconductor bridge-legs, the boost inductors, and the DC-link capacitors. The bridge-legs are connected to the DC-link capacitors through the power PCB and to the motor windings through the motor-side CM inductor. Critically, we note here that the vast majority of the converter losses are generated in this second level, resulting in the highest temperature, and this is where the electrolytic capacitors would need to be placed to connect to the DC-link — making a system with electrolytic capacitors infeasible.

The third level (**Fig. 2.11(c)**) contains the gate drive, measurement, control, and logic circuitry on two separate PCBs, with the control unit on the top. Converter losses are cooled via the surface — and the thermal resistance (and insulation) can be improved through potting, if desired — with the large thermal capacitance improving the thermal characteristics significantly, since the system is not operated at full power for extended periods. The final motor-integrated drive is shown in **Fig. 2.12**.

2.4 Hardware Demonstration Verification

To evaluate the motor-integrated hardware demonstrator of **Fig. 2.12**, we evaluate the overall operation of the drive system across the continuously-varying operating points, motor drive speeds, and torque fluctuation. Full

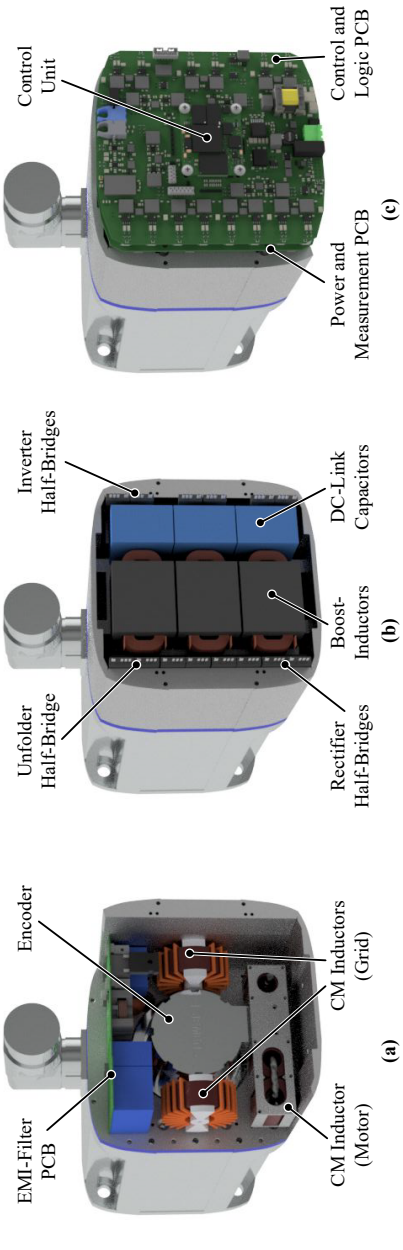

Fig. 2.11: Motor-integration of the VSD system, built up in three layers from left to right. **(a)** Encoder and filter components, **(b)** Power components, **(c)** Circuitry and Control Unit.

Fig. 2.12: Photograph of the complete motor-integrated, MPPB-operated, single-phase-supplied, variable-speed-drive system of **Fig. 2.1**.

operation cannot be validated with a resistor-inductor (RL) load alone, and a complete motor test bench is employed here (instead of driving the compressor itself). This test bench comprises a motor bed, the Device-Under-Test (DUT), a speed and torque sensor (*TM310* with a maximum torque bandwidth of 5 kHz from Magtrol [131]), and a load motor operated with a commercially-available drive system from Siemens with a constant load torque [99]. The identical setup was employed for the no-load measurements of **Section 2.3**. First, the concept is validated with time-domain measurements and waveforms. We then move to the loss model verification and EMI measurements before validating the extended functionality (distorted grid voltage, ridethrough operation, and battery-supply operation) in **Section 2.5**.

Note that, due to the limited availability of the optimal 16 mΩ power semiconductors specified in **Table 2.2**, all transistors are implemented as 32 mΩ device (*C3M0032120K* [116]) for the following measurements.

2.4.1 Time-Domain Waveforms and Operation

Firstly, the theoretical aspects of **Section 2.2** are verified for the nominal operating point, as described in **Table 2.3**. The measured waveforms are shown in **Fig. 2.13**, where we observe the grid current (20.6 Arms) and voltage in-phase for unity-power-factor operation (measured at 99.95 %) at 8.2 kW input power, a steady DC-link voltage near the reference of 650 V, and a speed equal to the reference of 3700 rpm with a speed ripple so small that it is not visible on this oscilloscope capture. The low-frequency ripple of the DC-link voltage is investigated in depth in **Appendix B** and corresponds here to 35 Vpkpk, nearly identical to the simulation results of 34 Vpkpk shown in **Fig. 2.5**. The measured motor currents are shown in **Fig. 2.14**, corresponding to a phase current stress of 18.5 Arms and, again, matching the theoretical results in both behavior and predicted amplitude. Overall, the system behavior is correct and expected, validating the MPPB approach and the predicted operation.

2.4.2 Efficiency

With the foundational operation of the MPPB approach verified, we move to verify the introduced loss model at nominal speed and DC-link voltage across the required mechanical output power range. Grid power input is measured with the *Yokogawa WT3000 precision power analyzer* and the mechanical quantities are measured with a speed and torque sensor. For all calculations, the measured stator phase resistance of $R_s = 0.2\,\Omega$ is used, as

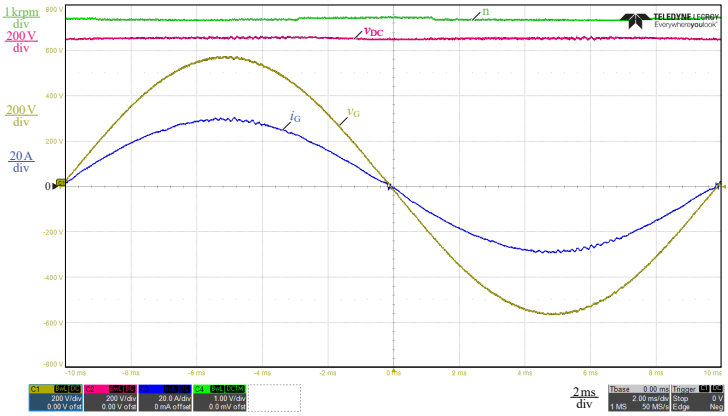

Fig. 2.13: Measured waveforms under steady-state, nominal operation: grid voltage (yellow), DC-link voltage (red), grid current (blue), and speed (1000 rpm/div, green).

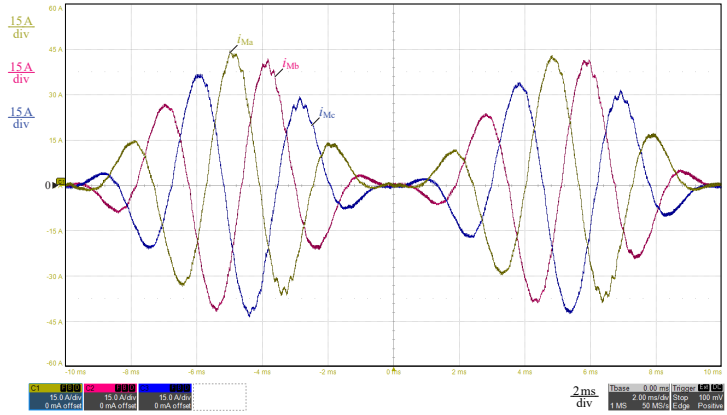

Fig. 2.14: Measured three-phase motor current waveforms under steady-state, nominal operation.

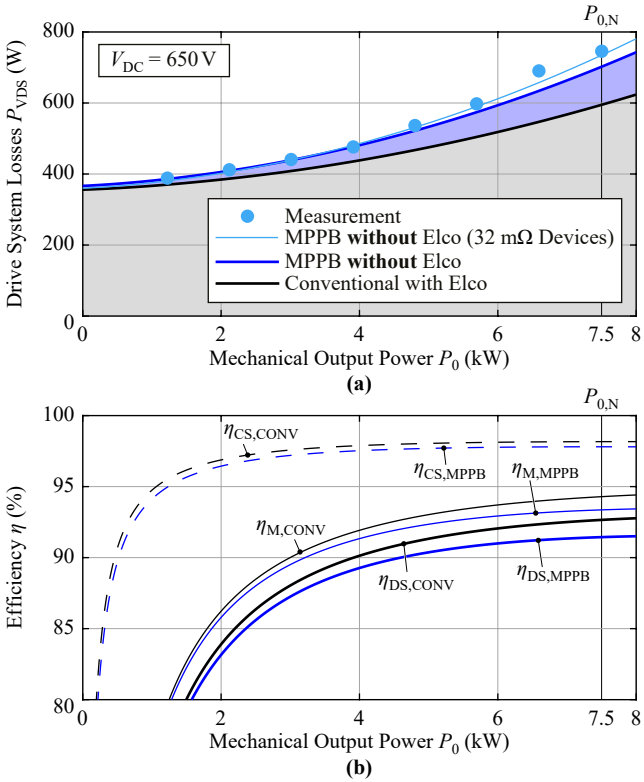

Fig. 2.15: (a) Drive system losses across mechanical output power P_0 at nominal speed 3700 rpm with a DC-link voltage of 650 V. Measurements are indicated by bullets and match the introduced loss models. **(b)** Converter, motor, and drive system efficiencies for conventional operation (black) and MPPB operation (blue).

the system is verified for the short-time operation needed for this particular application. With the MPPB approach encompassing the complete system, the difference in the measured input (grid) and mechanical output powers are the drive system losses P_{VDS}. These measured losses are shown across load torque — and, accordingly, mechanical output power — as the bullet points in **Fig. 2.15(a)**. These measurements match the proposed loss model nearly precisely, validating both the proposed power converter and motor loss models under the proposed MPPB operation.

Next, we want to quantify the efficiency penalty associated with the significant power density increase of the MPPB concept, and compare the constructed MPPB system to a conventional system with an electrolytic capacitor. The conventional system features lower phase current stresses, leading to lower currents and lower conduction losses in the motor and the inverter bridge-legs, but suffers from additional losses in the DC-link electrolytic capacitors. At the nominal output power, the system losses increase from 600 W for a grid-to-motor-shaft efficiency of 92.6 % in the conventional system with an electrolytic capacitor to 703 W (91.4 %) with the MPPB approach, for a loss increase of 103 W, or 17 %. This loss increase is the maximum across the operating load area, both in absolute and relative terms, with the load-dependent difference highlighted in blue in **Fig. 2.15(a)**.

Fig. 2.15(b) shows the motor, converter, and drive system efficiencies for conventional and MPPB operation over the output power range, where we find that the converter efficiencies are nearly identical at around 98 %. The overall efficiency is primarily limited by the motor itself, with the extra losses in MPPB operation contributed mostly by the additional phase current stresses. The MPPB system achieves a grid-to-motor-shaft efficiency above 90 % for all loads above 5 kW (66 % of the nominal load), a high and flat efficiency for the exceptional power density of the motor-integrated, electrolytic-capacitor-less MPPB-operated system.

2.4.3 Conducted EMI

Because the drive system was tested in full operation on the motor bed, all measurements for conducted EMI are conducted according to CISPR 16 for floor-standing equipment [132]. As discussed in the introduction and highlighted in **Table 2.1**, the conducted EMI of the drive system in the frequency range of 150 kHz to 30 MHz must comply with the CISPR 11 / Class A QP limit [46] (limits shown in **Fig. 2.16**).

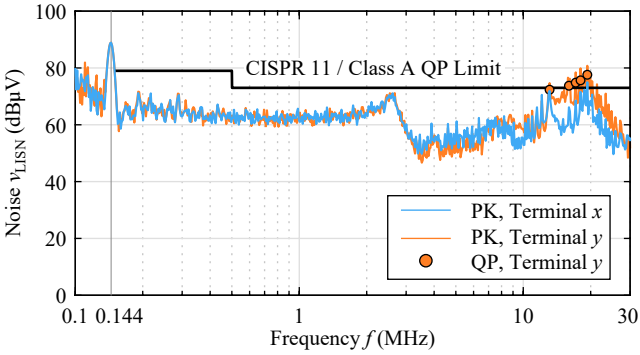

Fig. 2.16: Measured conducted maximum peak (PK) EMI noise emissions of the prototype drive system (with motor and converter mounted separately for safety and measurement), measured at a step size of 1 %, 10 ms measurement time, and with a bandwidth of 9 kHz for both phases x and y. Selected peaks (bullets) are measured with the quasi-peak (QP) detector with 1 s measurement time [46].

We scan both phases x and y of the drive system with a maximum peak detector with a step size of 1 %, a bandwidth of 9 kHz, and a measurement time of 10 ms, and report the results in **Fig. 2.16**.

Compliance with CISPR 11 / Class A across the vast majority of the frequency space is verified, with only certain frequencies above 15 MHz exceeding the limit and the largest QP violation of 4.6 dB at 19.3 MHz in phase y. Selected measurement points in this regime are verified with a CISPR 11 quasi-peak detector ("QP") with 1 s measurement time. These peaks, however, are only caused by the EMI test condition, where the converter and motor were separated and connected with a cable for safety and measurement, and the completed system will achieve CISPR 11 / Class A compliance across the full considered frequency range.

2.4.4 Transient Response

To this point, steady-state operation has been assumed. Next, the transient behaviour of the system is analyzed to verify the controller performance of the MPPB approach. **Fig. 2.17** shows the system behaviour for both a change in the reference speed and a step change in the instantaneous load torque.

The system begins in steady-state operation at 3000 rpm and with a nominal load torque of $T_{\mathrm{L,N}} = 19.4$ Nm, and there are steady-state speed, torque, and DC-link voltage ripples, as previously discussed. At $t = 1$ s, the reference

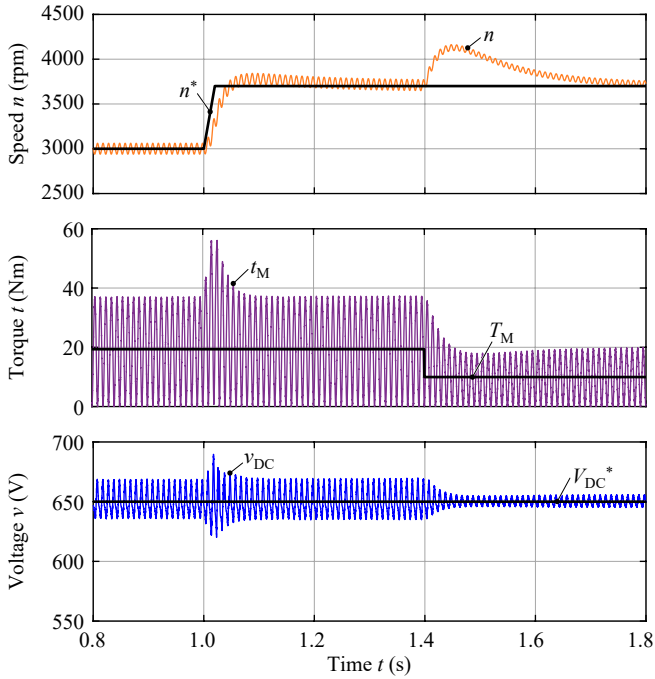

Fig. 2.17: Dynamic response of the proposed control structure with a speed step at $t = 1$ s and a load torque step at $t = 1.4$ s. The reference speed n^*, the speed n, the load T_L, the motor torque t_M, the DC-link voltage v_{DC}, and the DC-link voltage reference V_{DC}^* are presented. For both steps, the system requires around 350 ms to return to steady-state.

speed is increased linearly to $n^* = 3700$ rpm over 20 ms, and the input power and average motor power increase to ramp the motor speed to match this reference. The maximum applied instantaneous torque reaches 56 Nm, and this transient causes a small disturbance in the DC-link voltage with a maximum deviation of 40 V. This voltage disturbance decays after around 100 ms and the speed reaches steady state after 350 ms.

At $t = 1.4$ s, the load torque decays instantaneously to 10 Nm, which is approximately half of nominal torque. Again, the MPPB approach elegantly controls the system, with a short speed increase to 4169 rpm. The motor torque reaches steady state after 100 ms and the speed reaches steady state after 350 ms. It should be noted that the DC-link voltage ripple will scale with the motor torque, cf. **Fig. 2.17**.

2.5 Extended Functionality

To this point, we have assumed the system operates with a purely-sinusoidal grid input voltage, which is the nominal operating condition but not sufficient to meet the complete set of application requirements. In this Section, we validate drive system functionality under three abnormal conditions that are required for the application — with a distorted grid voltage, with a voltage sag on the grid, and with short- or long-term grid interruptions. These are analyzed and verified in turn.

2.5.1 Operation with a Distorted Grid Voltage

Industrial voltage supplies — and especially railway grids — can be heavily distorted [133, 134], with a grid voltage better described with the addition of a noise term v_{noise} as $v_{\text{G}} = \hat{V}_{\text{G}} \sin(2\pi f_{\text{G}}) + v_{\text{noise}}$. Under these conditions, we still must draw a sinusoidal input current to minimize the grid stress [135]. While the noise components could be eliminated with a low-pass filter, this filter necessarily introduces an additional phase shift ($v^*_{\text{G}} = \hat{V}_{\text{G}} \sin(2\pi f_{\text{G}} + \varphi)$) that degrades the power factor away from unity. Therefore, we address operation with a distorted grid voltage by reconstructing the fundamental of the grid voltage v^*_{G} around a Phase-Locked Loop (PLL) [136].

The PLL results in the input to the grid-current controller as $v^*_{\text{G}} = \hat{V}^*_{\text{G}} \sin(2\pi f_{\text{G}})$, as shown in **Fig. 2.18**. While PLLs based on a three-phase grid are simple to generate based on the orthogonal $\alpha\beta$–voltage system, the single-phase grid here requires an alternate approach. Instead, we use a Second-Order Generalized Integrator (SOGI) to derive v_α and v_β from the single-phase input voltage [137] based on the measured grid voltage v_{G} as the input. The SOGI outputs v_α, v_β and v_{pk} to the PLL block, which is used to derive the grid frequency f_{PLL} — fed back as the second input of the SOGI in a coupled system.

The PLL derives the phase angle $\theta = 2\pi f_{\text{G}} t$ and, following $\hat{V}^*_{\text{G}} = v_{\text{pk}}$, $v^*_{\text{G}} / \hat{V}^*_{\text{G}} = \sin\theta = \sin(2\pi f_{\text{G}} t)$, we can reconstruct the grid voltage $v^*_{\text{G}} = \hat{V}^*_{\text{G}} \sin(2\pi f_{\text{G}} + \varphi)$. This v^*_{G} is used for the grid current controller input and is also used for the power feedforward term, as shown in **Fig. 2.18**.

2.5.2 Operation under Grid Voltage Sag or Interruption

More specifically, the drive must operate correctly under two additional fault conditions: voltage sags, where the input voltage falls below the specified range, and grid interruption, where the grid provides no voltage for a period.

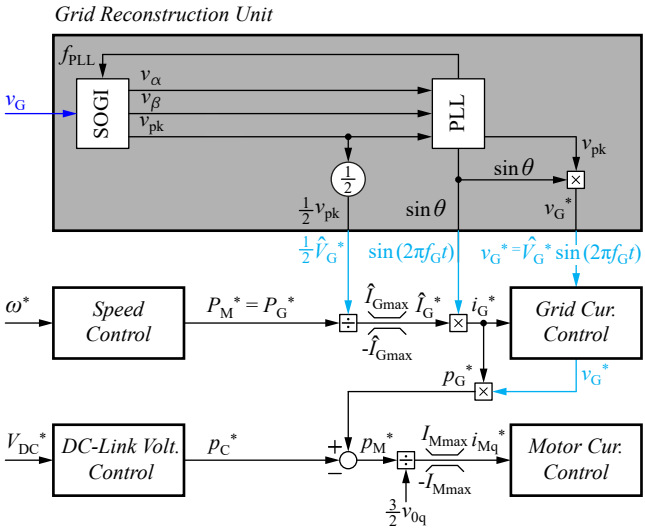

Fig. 2.18: Details of the Grid Reconstruction Unit control structure to achieve sinusoidal input current without a phase shift, even with heavily-distorted grid input voltages.

The exact conditions for each of these faults are discussed comprehensively in [138].

Continued operation under fault conditions increases system reliability, uptime, safety, and financial payback, and grid-tied industrial applications often require ridethrough operation to minimize downtime (e.g. in general converter systems [139, 140] or for drives [141, 142]). Under a fault, the system must both *(a)* not trip, keeping the system operational, and *(b)* apply the full requested torque, without significant delay, after the interruption or sag. We analyze how this will affect the MPPB concept, where no significant electrical or electrochemical energy storage is included.

Voltage Sag

The proposed MPPB system achieves the required operation under grid voltage sag by design, with:

- A large specified grid tolerance (of approximately ±30 %, see **Fig. 2.1(b)**) to cover the majority of sag cases with full power operation, and

- Even with the voltage outside of the specifications, the control structure detailed in **Fig. 2.18** will cover the voltage sag condition at reduced power, with the grid current limiter freezing speed control once the limit is reached. The control scheme guarantees rapid recovery, as shown later.

Grid Interruption

Railway systems regularly experience short-term grid interruptions in the range of several tens of milliseconds [143]. In conventional systems, these interruptions are easily covered by the DC-link capacitance energy storage — which is not present in the proposed MPPB approach, requiring a further investigation of the operation under grid interruption.

During the grid interruption, there is no sinusoidal input voltage and no power can be extracted from the grid. When the phase lock of the PLL is lost, the PFC rectifier stops operating (all gates are turned-off) and an idle power semiconductor state is entered, similar to the first state of startup. The PFC operation flag switches from $\mathrm{ON}_{\mathrm{PFC}} = 1$ (normal operation) to $\mathrm{ON}_{\mathrm{PFC}} = 0$, and the grid power request drops from the motor power $P_{\mathrm{G}}^{*} = P_{\mathrm{M}}^{*}$ to zero, $P_{\mathrm{G}}^{*} = 0\,\mathrm{W}$, as shown in **Fig. 2.19(a)** for ridethrough operation.

Without electrical (or other) energy storage within the system, the compressor can no longer be driven, and the load torque of the compressor slows the rotational speed of the motor (the compressor is supplied from the kinetic energy storage of the motor inertia). During this period, the speed controller is frozen — all stored variables are continuously initialized with the instantaneous values to prevent triggered step responses — but the inverter remains turned-on ($\mathrm{ON}_{\mathrm{INV}} = 1$) to maintain the DC-link voltage control, which is now decoupled from the grid input (since the feedforward term is now $p_{\mathrm{G}}^{*} = 0\,\mathrm{W}$). The DC-link voltage control, then, continues to ensure that the DC-link voltage is kept at the reference value; the DC-link is supplied again by the motor inertia and the rotating mass decelerates more quickly (and even more quickly if additional loads, like discharge resistors or logic supply or fans, are connected to the DC-link).

At this point, with the decelerating motor supplying the DC-link to maintain the reference voltage, we distinguish between two cases — short-term and long-term interruptions.

Short-term Interruption: If the grid returns while the system is still rotating (and supplying the DC-link), only the PFC rectifier needs to be resynchronized, and the grid power can be ramped to stabilize the mechanical speed of the motor. Because the DC-link voltage was maintained above the

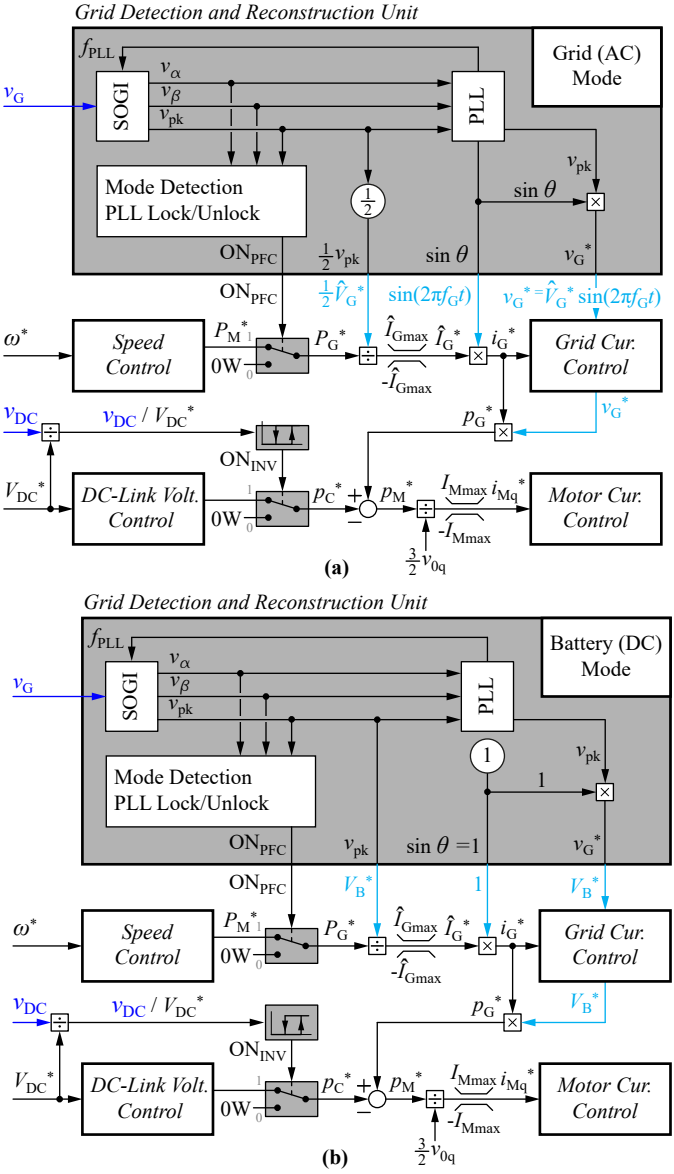

Fig. 2.19: Details of the control structure to implement startup or ridethrough operation for both **(a)** AC and **(b)** DC operation. Only the AC-referenced quantities change for DC-supplied operation, with no change in control structure or values.

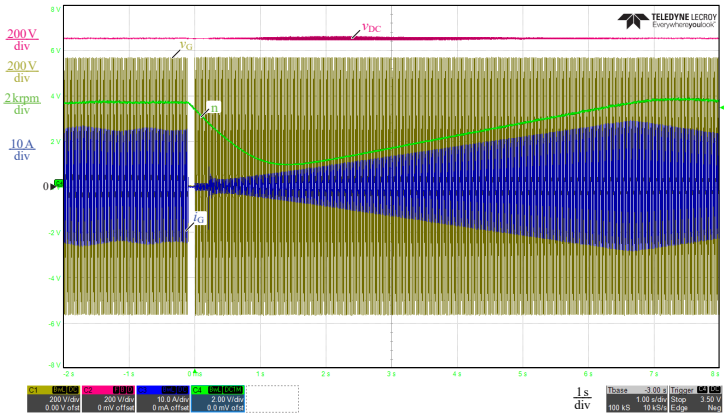

Fig. 2.20: Measured system transient performance for ridethrough of a 100 ms grid interruption at 3.4 kW mechanical output power: grid voltage (yellow), DC-link voltage (red), grid current (blue), and speed (2000 rpm/div, green).

voltage peak of the grid, no pre-charging state is required and the response time is fast.

This performance is verified in **Fig. 2.20**, where a 100 ms interruption at a power level of 3.4 kW results in a fast and stable recovery to the mechanical speed request. When the grid is interrupted, we observe that PFC operation stops and the grid current goes to zero. The speed drops linearly with $\mathrm{d}\omega/\mathrm{d}t = T_\mathrm{L}/J_\mathrm{M}$ (under constant torque operation, which is the worst-case condition). When the grid returned after 100 ms, the PFC synchronizes and ramps up the motor power, and we observe a reduction in the rate of the speed decay, which becomes zero at $\omega T_\mathrm{L} = P_\mathrm{G}$ (the speed minimum). From there, the control returns the motor to the desired steady-state speed, which we observe without significant DC-link voltage oscillations — even with the elimination of the DC-link energy storage capacitors provided by the MPPB approach. The recovery time could be even further shortened with the addition of a non-linear speed controller.

The survivable ridethrough time depends primarily on the speed before the interruption, the total kinetic energy, and the instantaneous load torque (or the pressure of the tank, see **Fig. 2.1**). If the motor stops rotating, the battery supply starts, the final extended functionality case that we explore.

Long-Term Interruption and Battery Supply Operation: The system will enter standstill if the motor speed decays to zero and the DC-link voltage can

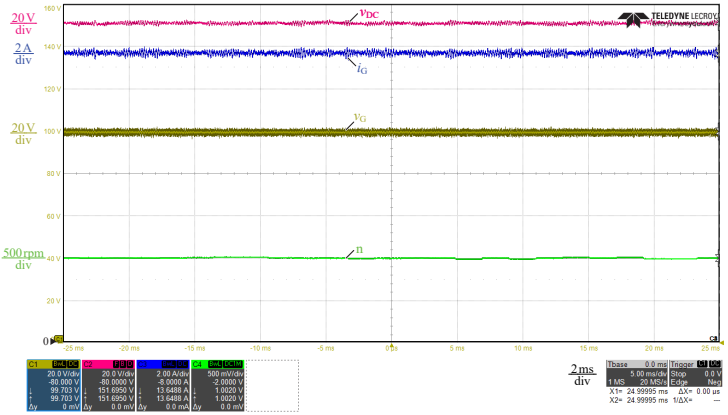

Fig. 2.21: Measured waveforms under under steady-state DC-supplied operation at 1.2 kW mechanical output power: grid voltage (yellow), DC-link voltage (red), grid current (blue), and speed (500 rpm/div, green).

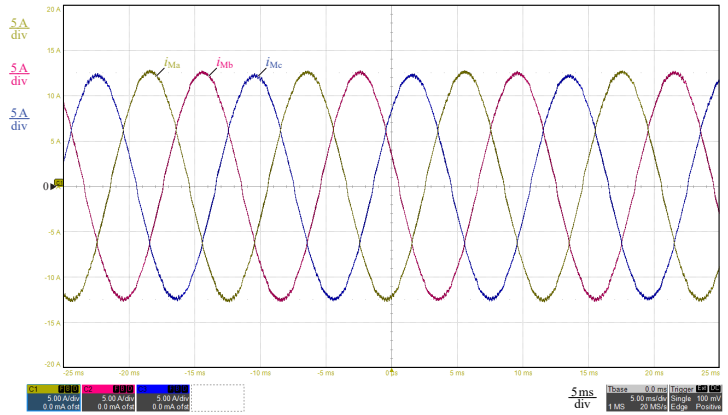

Fig. 2.22: Measured three-phase motor current waveforms under steady-state DC-supplied operation at 1.2 kW mechanical output power.

no longer be maintained (with no remaining kinetic energy). At this point, the DC-link and inverter control are turned off and the systems returns to a state similar to before initial startup.

The DC-link voltage controller is implemented with a hysteresis control based on the ratio of the instantaneous and reference DC-link voltages, and this supports the direct utilization of this concept for startup.

If the grid interruption is sustained, the switching network of **Fig. 2.1(a)** connects the battery supply instead of the grid, and the "DC-grid" is detected by the grid detection and reconstruction unit (see **Fig. 2.19(b)**). The identical control structure, with identical controller gains, is reused for DC-grid operation, with the grid-dependent variables in AC operation replaced by their DC equivalents (see the replacements between **Fig. 2.19(a)** and **Fig. 2.19(b)**). This implementation requires a single software code base for both operation modes, simplifying implementation, testing, and maintenance. Of course, the traditional approach, similar to **Fig. 2.3(a)**, could also be followed for DC-operation, but this would increase the software effort for design, validation, maintenance, and operation, where the two modes of operation would need to be actively switched during an extended grid voltage interruption. Because this introduces further complexity to the system, the approach of **Fig. 2.19** is preferred.

DC-grid operation with a battery voltage of 100 V and a DC-link voltage of 150 V is validated in **Fig. 2.21** and **Fig. 2.22**, with sinusoidal motor currents as shown in **Fig. 2.6** at a mechanical power of 1.2 kW at 1000 rpm. DC-grid operation and control is validated, and the MPPB system supports the required operation under fault conditions — even without DC-link energy storage.

2.6 Summary

Motor integration of Variable Speed Drive (VSD) systems is desired for power density, integration, cost, and reliability — but for single-phase-supplied applications, is limited by the need to provide buffering energy storage on the DC-link, which is typically accomplished with electrolytic capacitors. These electrolytic capacitors occupy significant converter volume and cannot be operated across a wide temperature range with high lifetime, preventing these VSDs from motor integration for the next-generation of electrified mobility.

In this work, we propose to use the kinetic energy stored in the motor inertia itself to buffer the pulsating power from the single-phase grid, translating DC-link voltage and current ripple to motor speed and torque ripple. We deem this concept Motor-Integrated Power Pulsation Buffer (MPPB), and

deeply analyze the control technique and structure required for nominal and grid fault-condition operation. The control is realized by rearranging the connections between the same top-level controllers — without changing the core controllers themselves — supporting retrofitting and a simple software change.

A hardware demonstrator is constructed to verify the proposed MPPB concept for a single-phase-supplied railway application that drives a scroll compressor for air brakes (and other loads that require high-reliability). The 7.5 kW demonstrator realizes complete Permanent Magnet Synchronous Motor (PMSM) integration in a total volume of 8.2 L (or 500 in^3) — and without the DC-link capacitors that would occupy an additional 1 L (or 61 in^3) and prevent integration. The MPPB system achieves over 90 % grid-to-motor-shaft efficiency for all loads over 5 kW or 66 % of the nominal load, with a worst-case loss penalty over a conventional electrolytic-capacitor-based system of only 17 %. The demonstrator will achieve CISPR 11 / Class A compliance at full integration and operates across the required suite of extended functionality, including for ridethrough and sustained grid faults.

The proposed MPPB concept shifts the required grid-buffering energy storage from an additional electrical element — large DC-link capacitors — to the motor that is already required for mechanical drive, achieving otherwise-unobtainable power densities and integration levels for single-phase-supplied variable-speed electric drives.

3
Dual-Inverter Topology

This Chapter summarizes the most relevant findings of research on electrolytic capacitor-less dual inverter topologies for single-phase-supplied drive systems, which are also published in:

- **M. Haider**, D. Bortis, S. Mirić, J. W. Kolar, Y. Ono, "Dual-Inverter Topology for Single-Phase Supplied Drive Systems without Electrolytic Capacitor," in *Proc. of the IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Gyeongju, South Korea, Oct. 2021.

Motivation

Building on the Motor-Integrated Power Pulsation Buffer (MPPB) introduced previously, this Chapter investigates the applicability of the MPPB for a dual-inverter structure to avoid the boost stage, eliminate the boost-inductor and the high-frequency bridge-leg, of the system proposed in Chapter 2 achieving reduced volume, cost and complexity.

Executive Summary

Single-phase-supplied Variable Speed Drive (VSD) systems are widely used in industrial applications and typically feature a two-stage design with a Power Factor Correction (PFC) boost rectifier and a three-phase Voltage Source Inverter (VSI). However, the electrolytic DC-link capacitor, which is needed to cope with the twice grid frequency power pulsation, and the required boost inductor are unfavourable in terms of reliability, volume, cost, and complexity. Therefore, the proposed new concept is based on a dual-inverter topology with a three-phase Open-End Winding (OEW) motor, avoiding high-frequency inductors, and controls the system such that the power pulsation is buffered in the inertia of the drivetrain. Accordingly, the DC-link capacitance can be reduced drastically, enabling an electrolytic capacitor-less system, featuring a higher power density and an increased lifetime. This Chapter presents the operating principle and the corresponding closed-loop control structure of the new approach and demonstrates PFC operation, DC-link voltage balancing and average speed control. Detailed analysis reveals that the motor voltage can be selected independently of the grid peak voltage in contrast to existing concepts. The converter performance is evaluated based on simple performance indices with respect to the motor voltage. Utilizing the new concept in the context of a 7.5 kW compressor application for railway brakes with a wide input voltage range, a semiconductor loss reduction of 30 % can be obtained compared to a state-of-the-art approach, further reducing the converter volume. Finally, the proper operation is verified with a closed-loop circuit simulation.

3.1 Introduction

In industrial applications such as Variable Speed Drive (VSD) systems for compressors, fans, blowers, or pumps in the lower kW range, electrical drive systems are often supplied from the single-phase AC grid in order to keep the grid interface simple [66]. Other application scenarios include higher power levels in case only a single-phase supply is available [50], i.e. in AC supplied railway systems [41, 45] or Single-Wire Earth Return (SWER) grids [144]. State-of-the-art VSD systems often employ three-phase Permanent Magnet Synchronous Motors (PMSMs) due to their high torque, low weight, high efficiency, and compactness [44]. Therefore, a power electronic system is required

to convert the single-phase AC input voltage into a symmetrical three-phase voltage system with adjustable amplitude and frequency to achieve variable speed control. In addition, the system has to keep the input current proportional to the input voltage (unity power factor operation) to minimize harmonic distortion and reactive power in the grid.

Usually, all these requirements are fulfilled by a two-stage system with a single-phase Power Factor Correction (PFC) rectifier and a three-phase Voltage Source Inverter (VSI), which are decoupled by an intermediate DC-link capacitor [51, 52]. Different topologies can be employed for the PFC rectifier [85] as well as the VSI [145]. However, the most common implementation features a unidirectional single-phase boost PFC rectifier, comprising a diode bridge with a downstream boost converter and a conventional three-phase two-level VSI [48].

The inherent power pulsation of the single-phase PFC rectifier with twice the grid frequency is typically covered by a sufficiently large electrolytic DC-link capacitor with a capacitance C_{DC} in the mF-range to keep the DC-link voltage of the subsequent VSI quasi constant [49]. In summary, a state-of-the-art single-phase-supplied drive system features a dedicated boost PFC rectifier input stage employing a boost inductor, a high-frequency bridge-leg and an electrolytic capacitor, which are all unfavourable in terms of reliability, volume, cost, and complexity.

Therefore, in the literature [82, 84, 146–148] a vast number of single-phase-supplied drive system concepts have been proposed, with the aim to avoid the boost converter and to connect the three-phase VSI directly to the diode bridge, which reduces the component count and eliminates the mentioned drawbacks. In fact, such approaches are plain simple and allow low-cost implementations, however, the input current becomes discontinuous, and PFC operation can no longer be achieved, since in the vicinity of the grid voltage zero-crossings the maximum achievable output voltage of the VSI, i.e. about half of the grid voltage amplitude, drops below the induced motor voltage, which means that the motor and input current controllability is lost. This becomes even more prominent with increasing induced motor voltage at higher rotational speeds, as it further extends the zero-current intervals and, in consequence, increases the current Total Harmonic Distortion (THD) [81, 83].

In order to regain PFC operation and complete motor current controllability, in [44] a *Single-Phase AC Dual-Inverter Topology* in combination with

an Open-End Winding (OEW) PMSM is proposed, where the second three-phase inverter (VSI 2) employing a floating DC-link capacitor is connected to the second winding ends, while the first winding ends are attached to the first VSI (VSI 1) which is directly connected to the single-phase diode bridge rectifier (cf. **Fig. 3.1(a)**). Due to the large motor inductances, typically in the mH-range, the switching frequency can be chosen very low, i.e. in the range of 2.5 kHz...16 kHz, and thus, both VSIs can be implemented with low-cost IGBT technology. Furthermore, the low switching frequency is not only advantageous in terms of switching losses but also for the EMI-filter requirement and the associated volume [118]. Control strategies aiming for constant rotational speed and torque operation, i.e. constant mechanical output power, are presented in [149, 150]. Related characteristic waveforms within one grid period are shown in **Fig. 3.1(b-d.i)**. As can be noted, since on the one hand, VSI 1 has to directly process the pulsating input power $p_G(t)$ (composed of a twice grid frequency power pulsation $\tilde{p}_G(t)$ with magnitude P_0 around an average input power P_0) in order to achieve PFC operation, and on the other hand, the motor is demanding a constant average output power $p_M(t) = P_0$, the second inverter has to cope with the twice grid frequency zero-mean pulsating power $p_{C2}(t) = \tilde{p}_G(t)$. If active Power Pulsation Buffer (PPB) concepts are disregarded [62–64, 151], this means that a large electrolytic DC-link capacitor C_{DC2} for VSI 2 is required to keep v_{DC2} roughly constant [150], which in turn again is a significant drawback concerning cost, volume, and especially converter lifetime [57, 58, 60].

In order to also eliminate the electrolytic capacitor in the *Single-Phase AC Dual-Inverter Topology*, a novel control strategy is proposed in the following, where the twice grid frequency power pulsation is buffered utilizing the inertia of the motor and/or drivetrain, which in the literature is also known as Motor-Integrated Power Pulsation Buffer (MPPB) [80]. As shown in **Fig. 3.1(b-d.ii)**, in this case, a torque t_M with a large torque ripple similar to single-phase motors is occurring for the three-phase motor, while the resulting speed ripple $\Delta\omega$ is relatively small, i.e. typically within a few percent of rated speed, which is a result of the comparably large system's moment of inertia J_{TOT}. As a consequence, VSI 2 is only needed to apply enough voltage to the motor in order to control the motor currents, thus the active power processed by VSI 2 is zero, which means that the secondary DC-link capacitor C_{DC2} can be small and remain floating, i.e. without electrical connection to other parts of the system.

In order to obtain this control behaviour, however, an adaption of the operating principle and voltage division strategy for both VSIs is needed, as

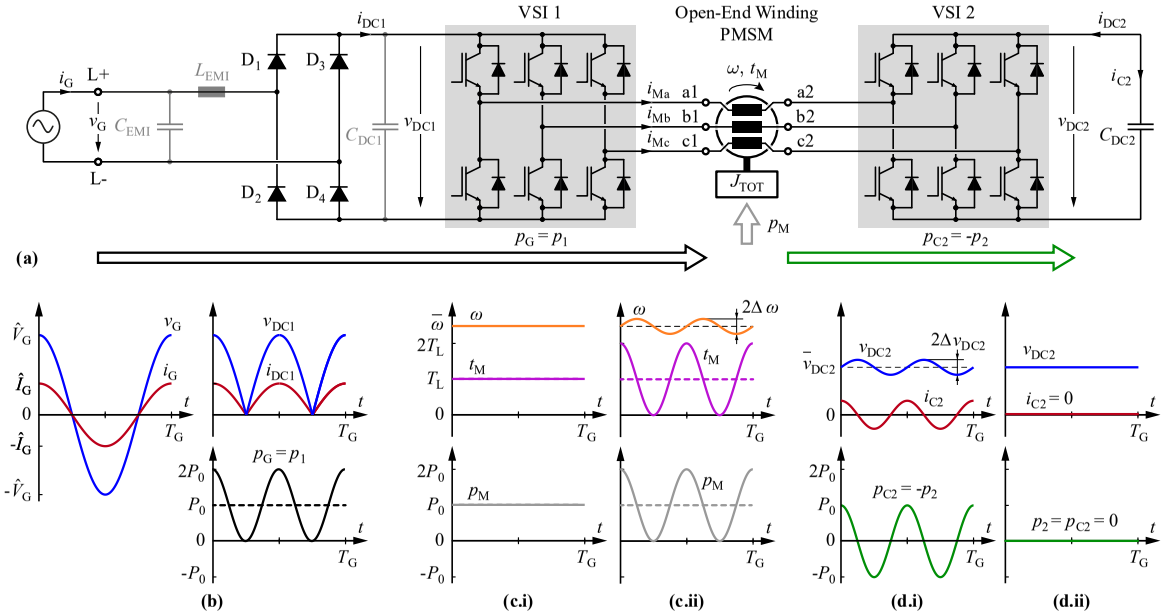

Fig. 3.1: (a) *Single-Phase AC Dual-Inverter Topology* comprising a first voltage source inverter (VSI 1) connected to the output of the diode bridge D_1-D_4, a three-phase PMSM with open-end windings, and a second voltage source inverter (VSI 2) with a floating DC-link capacitor C_{DC2}. The power flow is indicated with arrows. **(b-d)** Characteristic voltage, current, speed, torque, and power waveforms **(i)** for the state-of-the-art control scheme, where an electrolytic capacitor C_{DC2} is required to cover the pulsating power drawn from the grid [149,150] and **(ii)** for the proposed control scheme, where the input power pulsation is buffered by the inertia of the system, which allows to replace the electrolytic capacitor C_{DC2} with a low capacitance foil capacitor featuring long lifetime.

investigated in **Section 3.2**. Afterwards, the control structure ensuring PFC operation in combination with DC-link voltage balancing and average speed control is derived in **Section 3.3**. Detailed analysis reveals that in contrast to [149, 150] the motor voltage can be selected independently of the peak grid voltage, which introduces a further degree of freedom for the drive system optimization. **Section 3.4** illustrates this advantage for a 7.5 kW compressor application with a wide input voltage range, where the achievable system performance is evaluated and compared to the state-of-the-art. Finally, the proper closed-loop system operation is verified for the considered application by circuit simulations in **Section 3.5**. **Section 3.6** summarizes the main findings of the work and gives an outlook on future research.

3.2 Operating Principle and Motor Voltage Division Strategy

In the following, the operating principle and the corresponding characteristic waveforms of the *Single-Phase AC Dual-Inverter Topology* with and without electrolytic capacitor C_{DC2} are derived in order to highlight the advantages of the proposed control strategy.

In general, in both cases, the questions arise (i) how the motor input voltage has to be divided between the two three-phase inverters VSI 1 and VSI 2, and (ii) how the motor current has to be controlled such that PFC operation is guaranteed. At the single-phase grid input, PFC operation means that the drive system has to behave as an ohmic load with a sinusoidal input current $i_{\mathrm{G}}(t) = \hat{I}_{\mathrm{G}} \cos(2\pi f_{\mathrm{G}} t)$ in phase with the grid voltage $v_{\mathrm{G}}(t) = \hat{V}_{\mathrm{G}} \cos(2\pi f_{\mathrm{G}} t)$, whereas the instantaneous input power

$$p_{\mathrm{G}}(t) = v_{\mathrm{G}}(t)\, i_{\mathrm{G}}(t) = P_0 \frac{2v_{\mathrm{G}}^2(t)}{\hat{V}_{\mathrm{G}}^2} = P_0 + \tilde{p}_{\mathrm{G}}(t) \tag{3.1}$$

is forwarded directly to the motor $p_{\mathrm{M}}(t)$ and/or the secondary DC-link capacitor $p_{\mathrm{C2}}(t)$. The instantaneous power balance is therefore given as

$$p_{\mathrm{G}}(t) = p_{\mathrm{M}}(t) + p_{\mathrm{C2}}(t). \tag{3.2}$$

Since the secondary DC-link is floating, i.e. has no connection to the input, common-mode currents flowing through the VSIs and the motor are not possible (cf. **Fig. 3.1(a)**), thus the capacitor C_2 can only be charged/discharged

by three-phase motor currents. Consequently, in order to simplify the system analysis, all three-phase quantities are described by their corresponding voltage and current space vectors $\underline{v}_\mathrm{M}$, $\underline{v}_1$, $\underline{v}_2$ and $\underline{i}_\mathrm{M}$ in the rotor-oriented dq-frame, i.e. $\underline{i}_\mathrm{M}(t) = i_\mathrm{Md}(t) + j i_\mathrm{Mq}(t)$, where the d-axis is aligned with the flux of the permanent magnet. In addition, an ideal non-salient pole rotor PMSM with negligible synchronous reactance ($R_\mathrm{s} = 0$, $L_\mathrm{d} = L_\mathrm{q} \approx 0$) and a large moment of inertia J_TOT is assumed, which in all cases means that due to $L_\mathrm{d} = L_\mathrm{q} \approx 0$ (i) only the q-current component i_Mq is generating a mechanical torque, (ii) the motor terminal voltage is given by only the motor back-Electromotive Force (EMF) voltage, i.e. $\underline{v}_\mathrm{M} = jV_\mathrm{P}$, and due to the large J_TOT (iii) the rotational speed ω and thus $V_\mathrm{P} = \omega p \Psi_\mathrm{PM}$ are quasi constant.

3.2.1 Dual-Inverter With Electrolytic Capacitor

Based on the power balance given in **Eqn. (3.2)**, there are now different possibilities to divide the pulsating input power $p_\mathrm{G}(t)$ between the motor and the secondary DC-link capacitor. However, it has to be considered that at least the average power $P_\mathrm{C2} = \overline{p_\mathrm{C2}}(t)$ of the secondary converter or the capacitor C_DC2 is zero. This approach is applied in the state-of-the-art concept (cf. [149]), where the motor takes a constant power equal to the average input power, i.e. $p_\mathrm{M}(t) = P_\mathrm{M} = P_0$, and the capacitor has to cope with the twice grid frequency zero-mean pulsating power, i.e. $p_\mathrm{C2}(t) = \tilde{p}_\mathrm{G}(t)$. Hence, due to the constant power consumption and constant back-EMF voltage of the motor, in this case, the torque $t_\mathrm{M}(t) = T_\mathrm{L}$ and thus the q-component of the motor current $i_\mathrm{Mq}(t)$ must also be constant. In addition, the motor current can be minimized, by selecting its magnitude equal to the q-current component, i.e. $i_\mathrm{M}(t) = i_\mathrm{Mq}(t) = 2/3\ P_\mathrm{M}/V_\mathrm{P}$. The first three-phase inverter VSI 1 has to process the complete input power, i.e. $p_1(t) = p_\mathrm{G}(t)$, and as its d-voltage component is set to zero [149], i.e. $v_\mathrm{1d}(t) = 0\,\mathrm{V}$ or $v_1(t) = v_\mathrm{1q}(t)$, the power balance simplifies to $p_1(t) = 3/2\ i_\mathrm{M}(t)\ v_1(t) = p_\mathrm{G}(t)$. Consequently, since $i_\mathrm{M}(t)$ is constant, the magnitude of the VSI 1 output voltage $v_1(t)$ has to vary sinusoidally with twice grid frequency as $v_1(t) = \hat{V}_1\ \cos^2(2\pi f_\mathrm{G} t)$ where the peak inverter voltage is limited by the maximum modulation index M_max and the peak input voltage $\hat{V}_\mathrm{G}$ as $\hat{V}_1 = M_\mathrm{max}\,\hat{V}_\mathrm{G}/2$ (cf. **Fig. 3.2(a.i)**). Due to the neglected motor inductances, the corresponding voltage space vector $\underline{v}_1(t)$ is pointing in the same direction as the motor voltage space vector $\underline{v}_\mathrm{M} = jV_\mathrm{P}$ (cf. **Fig. 3.2(b.i)**). Since now, the sum of the inverter voltages must correspond to the motor voltage

$$\underline{v}_\mathrm{M}(t) = \underline{v}_1(t) + \underline{v}_2(t), \tag{3.3}$$

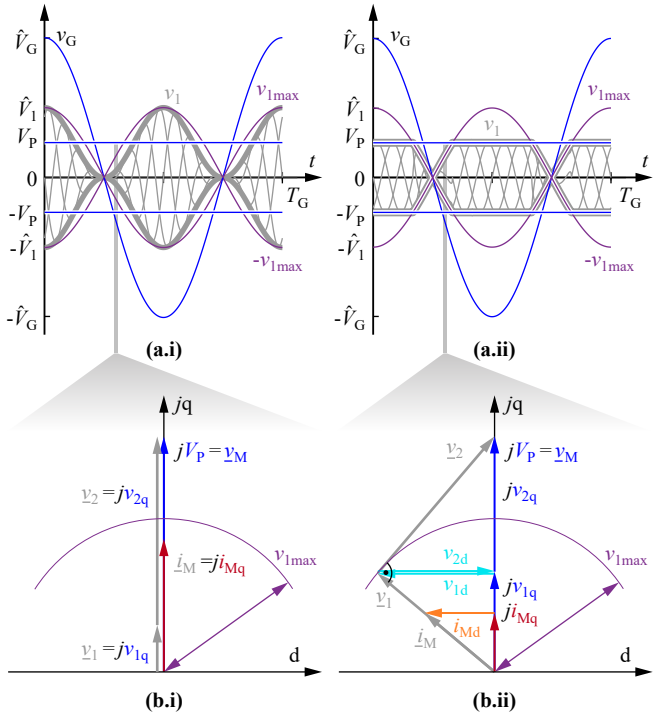

Fig. 3.2: (a) Voltage waveforms of the grid and the first inverter VSI 1 over one grid period $T_G = 1/f_G$ for **(i)** the state-of-the-art control scheme [149, 150] and for **(ii)** the proposed control scheme. **(b)** Corresponding space vector diagrams of the inverter and motor quantities in the dq-frame for $v_{1max} = |v_G|/2 < V_P$.

this means that in time intervals where $v_1(t)$ is smaller than V_P, the second inverter must add a voltage $\underline{v}_2(t)$ in phase with $\underline{v}_1(t)$ and $\underline{i}_M(t)$, i.e. VSI 2 delivers power from the secondary DC-link capacitor C_{DC2} to the motor, whereas in time intervals where $v_1(t)$ is larger than V_P, the second inverter must add a voltage $\underline{v}_2(t)$ out of phase by 180° with respect to $\underline{v}_1(t)$ and $\underline{i}_M$, i.e. VSI 2 delivers power from the motor to the secondary DC-link capacitor. Hence, in order to ensure that the average power P_{C2} within one grid half-period is zero, the motor voltage V_P must be equal to $\hat{V}_1/2$, which for a maximum modulation index $M_{max} = 1$ results in a maximum motor voltage of $V_P = \hat{V}_G/4$. In this case, the maximum voltage amplitude of VSI 2 is required at the grid

voltage zero-crossing, where it has to provide the full motor voltage V_P, thus the length of the voltage vector of VSI 2 varies between $-V_P$ and V_P, which requires a secondary DC-link of $V_{DC2} > 2V_P$. Furthermore, since the zero-mean pulsating input power is covered by the secondary DC-link capacitor, a large capacitance C_2 is needed to keep the voltage fluctuation within certain limits, which in [150] is given as

$$C_{DC2} > \frac{2P_0}{2\pi f_G \left(v_{DC2,max}^2 - v_{DC2,min}^2\right)}. \tag{3.4}$$

All corresponding characteristic waveforms of this control concept are shown in **Fig. 3.4(a)**.

3.2.2 Dual-Inverter Without Electrolytic Capacitor

Instead of keeping only the average power P_{C2} at zero, it is also possible to keep the instantaneous power directly at zero, i.e. $p_{C2}(t) = 0\,\mathrm{W}$. This means that the secondary converter is only needed to control the motor current and the complete pulsating input power is delivered directly to the motor, i.e. $p_M(t) = p_G(t)$. Due to the large J_{TOT} it is assumed that the rotational speed ω and thus the motor voltage amplitude V_P are still constant, the q-component of the motor current now has to vary sinusoidally with twice grid frequency,

$$i_{Mq}(t) = \frac{2}{3}\frac{p_M(t)}{V_P} = \hat{I}_M \cos^2(2\pi f_G t), \tag{3.5}$$

with $\hat{I}_M = 4/3\ P_0/V_P$, which clearly results in a proportional motor torque $t_M(t)$ (cf. **Fig. 3.1(c.ii)**). In contrast to the previously described concept, the voltage space vector of the secondary inverter $\underline{v}_2(t)$ must now be either zero or perpendicular to the motor current $\underline{i}_M(t)$ in order to guarantee that $p_{C2}(t) = p_2(t) = 0\,\mathrm{W}$. Considering **Eqn. (3.3)**, this means that $i_M(t) = i_{Mq}(t)$ is only possible in time intervals where $v_{1max}(t) = |v_G(t)|/2 \geq V_P$, and thus $\underline{v}_1(t)$ and $\underline{v}_2(t)$ can be selected to $\underline{v}_1(t) = jV_P$ (cf. **Fig. 3.2(a.ii)**) and $\underline{v}_2(t) = 0\,\mathrm{V}$, respectively. In time intervals where $v_{1max}(t) < V_P$, however, an additional negative d-current component $i_{Md}(t)$ must be flowing through the motor, such that $\underline{v}_2(t)$ can be kept perpendicular to the motor current $\underline{i}_M(t)$ (cf. **Fig. 3.2(b.ii)**). In contrast, $\underline{v}_1(t)$ is advantageously chosen in phase with $\underline{i}_M(t)$ and its magnitude is equal to $v_{1max}(t)$, i.e. $v_1(t) = v_{1max}(t)$ or $M_1 = 1$, such that the Root Mean Square (RMS) currents in both inverters and the motor are minimized. Hence, from the power balance at VSI 1,

i.e. $p_1(t) = 3/2\ \underline{v}_1(t)\ \underline{i}_M(t) = 3/2\ v_1(t)\ i_M(t) = p_G(t)$, the total motor current $i_M(t)$ can be calculated as

$$i_M(t) = \frac{2}{3}\frac{p_G(t)}{v_1(t)}, \tag{3.6}$$

and in combination with the given q-current component $i_{Mq}(t)$ also the d-current $i_{Md}(t)$ can be deduced as

$$i_{Md}(t) = -\sqrt{i_M^2(t) - i_{Mq}^2(t)}. \tag{3.7}$$

Furthermore, since $\underline{v}_1(t)$ and $\underline{i}_M(t)$ are selected to be in phase and $v_1(t) = v_{1max}(t)$, the d- and q-voltage components $v_{1d}(t)$ and $v_{1q}(t)$ of VSI 1 are proportional to the d- and q-current components $i_{Md}(t)$ and $i_{Mq}(t)$ of the motor, which results in

$$v_{1d}(t) = i_{Md}(t)\frac{v_1(t)}{i_M(t)} \quad \text{and} \quad v_{1q}(t) = i_{Mq}(t)\frac{v_1(t)}{i_M(t)}. \tag{3.8}$$

Finally, the remaining d- and q-voltage components $v_{2d}(t)$ and $v_{2q}(t)$ of the secondary inverter need to fulfil **Eqn. (3.3)** and are found as

$$v_{2d}(t) = -v_{1d}(t) \quad \text{and} \quad v_{2q}(t) = V_P - v_{1q}(t). \tag{3.9}$$

The corresponding characteristic waveforms of the proposed control concept are shown in **Fig. 3.4(b)** and **(c)**. It has to be mentioned that in this case the motor voltage V_P is no longer limited by the input voltage $v_G(t)$, since the secondary DC-link voltage V_{DC2} can be selected arbitrarily high - clearly limited by e.g. the blocking voltage capability of the used semiconductor switches. However, as will be shown in **Section 3.4**, this offers a further degree of freedom in the design of the single-phase-supplied drive system.

3.3 Control Structure

In the following, the closed-loop control structure to ensure the proposed operating behaviour of the single-phase-supplied dual-inverter drive system is described in detail. Basically, the drive system must operate the motor at the desired average speed, while on the one hand, PFC operation must be guaranteed at the input, and on the other hand, the DC-link voltage of the secondary inverter must be regulated to a certain target voltage. In principle, this can be done in analogy to a conventional cascaded motor control with

a slow outer *Speed Control* block and a fast inner *Motor Current Control* block, whereby the two mentioned conditions must be taken into account (cf. **Fig. 3.3**). In particular, the motor control has to be extended by (i) the additional *DC-Link Voltage Control* block, which demands a certain power p^*_{C2} to charge/discharge the secondary DC-link capacitor C_2 and together with the required input power p^*_G determines the instantaneous power consumption p^*_M and current i^*_{Mq} of the motor, and by (ii) the *Motor Voltage Division* block, which divides the motor voltage between the two three-phase inverters in such a way that only the second inverter is used for the motor current control while the first inverter adjusts its voltage to guarantee PFC operation. This means that the input current i_G is only defined by the impressed motor current i_M and the selected modulation index of VSI 1, which is in contrast to two-stage drive systems with dedicated boost PFC rectifiers, where an additional closed-loop grid current control is implemented [48, 80]. The individual control blocks of the proposed structure shown in **Fig. 3.3** are explained in the following.

3.3.1 Speed Control

Starting with the outermost control loop, the *Speed Control* block provides at its output the required average motor power P^*_M to reach the commanded rotational speed ω^*. At the input, the reference speed ω^* is compared with the average mechanical speed $\bar{\omega}$ calculated from the measured mechanical angle ε, which is also used for the dq-transformation [103]. As a consequence of the described power/torque pulsation, the actual mechanical speed ω, which is also used to calculate the amplitude of induced motor voltage V_P, features a certain ripple with twice grid frequency $2f_G$. Hence, a moving average filter (MAF) [100] with a time constant of $T_G/2$ is needed to obtain the average speed $\bar{\omega}$. The speed controller Rω then uses the calculated speed error $\delta\omega$ to determine the required torque T^*_A, which together with the optional feedforward load torque T_{FFL} gives the reference torque T^*_M and from this the required motor power P^*_M. Assuming a lossless system, P^*_M equals the average input power P^*_G, which based on **Eqn. (3.1)** leads together with the measured input voltage v_G to the commanded instantaneous input power p^*_G.

3.3.2 DC-Link Voltage Control

The amount of instantaneous power p^*_M that is actually delivered to the motor also depends on how much power p^*_{C2} has to be delivered/consumed by the

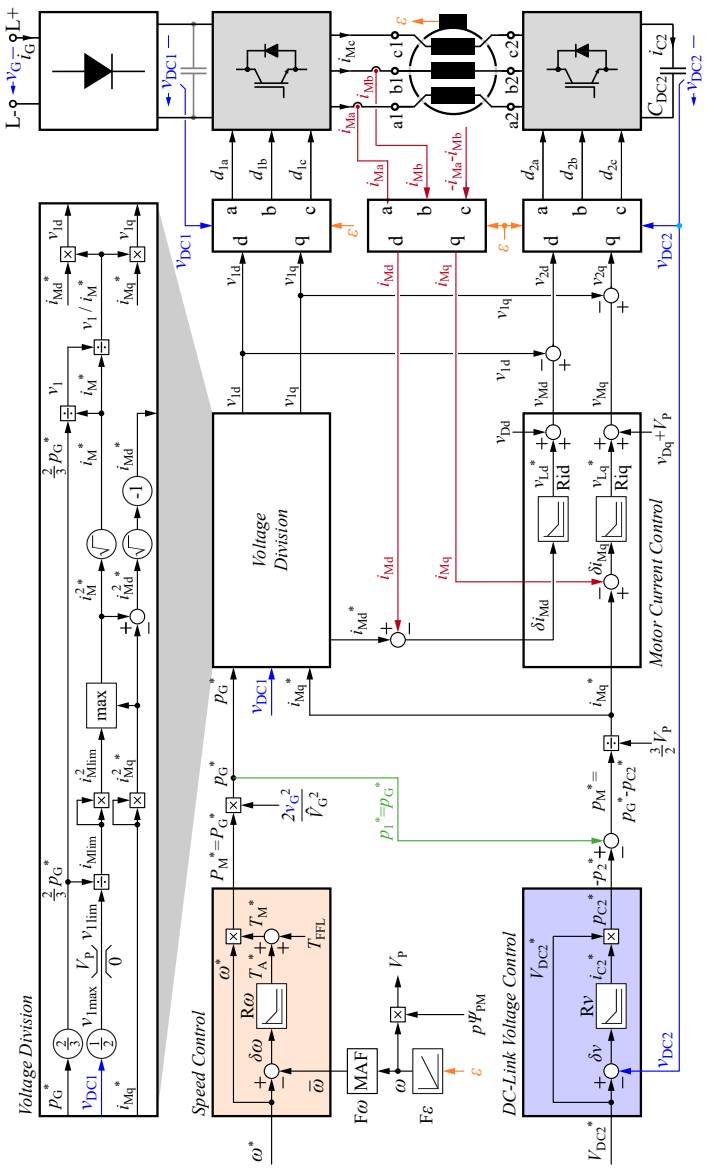

Fig. 3.3: Proposed control structure of the electrolytic capacitor-less *Single-Phase AC Dual-Inverter Topology*, consisting of four main blocks, i.e. *Speed Control*, *DC-Link Voltage Control*, *Voltage Division*, and *Motor Current Control*, to achieve average speed control, PFC operation, and voltage balancing at the secondary DC-link.

secondary inverter to charge/discharge the capacitor C_2, which is determined by the *DC-Link Voltage Control* block.

The reference voltage of the secondary DC-link V^*_{DC2} can be set according to the actual system's operating point, but must always be larger than $2V_P$ (cf. **Section 3.2**). The DC-link voltage controller Rv then compares V^*_{DC2} with the measured voltage v_{DC2} and translates the voltage error δv into the required capacitance current i^*_{C2}, which together with V^*_{DC2} results in the required power demand p^*_{C2} to bring the DC-link voltage back to its reference value. The instantaneous motor power $p^*_M = p^*_G - p^*_{C2}$ is then used to calculate the reference of the motor's q-current component i^*_{Mq} (cf. **Eqn. (3.5)**), which is finally forwarded to the two inner blocks.

3.3.3 Voltage Division

The reference values p^*_G and i^*_{Mq} commanded from the outer control loops are now processed in the inner *Voltage Division* block to calculate on the one hand, the d-current reference value i^*_{Md} needed for the *Motor Current Control* block, and on the other hand, the d- and q-voltages of the first inverter to guarantee PFC operation.

As described in **Section 3.2**, i^*_{Md} can directly be calculated from **Eqn. (3.6)** and **Eqn. (3.7)**, however, for i^*_M it has to be considered that the maximum achievable inverter voltage v_1 is given by the actual input voltage as $v_{1max} = |v_G|/2 = v_{DC1}/2$ and in addition is limited to the motor voltage V_P if $v_{1max} > V_P$.

In special cases where **Eqn. (3.6)** results in a motor current amplitude i^*_M which is smaller than the commanded q-component i^*_{Mq}, i^*_M has to be increased to i^*_{Mq} such that **Eqn. (3.7)** leads to a feasible d-current. Consequently, in order to still comply with the commanded input power p^*_G, the voltage v_1 of the first inverter has to be reduced. In the *Voltage Division* block this is implemented by recalculating v_1 from the commanded motor current i^*_M by using **Eqn. (3.6)** again. Subsequently, the individual voltage components v_{1d} and v_{1q} are calculated from v_1 based on **Eqn. (3.8)**.

3.3.4 Motor Current Control

Since now the two reference motor currents i^*_{Md} and i^*_{Mq} are known, the *Motor Current Control* block can be implemented in the same way as in the conventional cascaded motor control. There, the current controllers Rid and Riq translate the current errors δi_{Md} and δi_{Mq} into the reference inductor voltages

Tab. 3.1: Summary of the system specifications.

Nominal Mechanical Speed (n_N)	3700 rpm
Nominal Mechanical Power ($P_{M,N}$)	7.5 kW
Nominal Grid Voltage ($V_{G,N}$)	400 V
Grid Frequency (f_G)	50 Hz
Grid Voltage Range (V_G)	360 Vrms to 480 Vrms
Converter Power (P_G)	9 kW
Switching Frequency (f_{sw})	16 kHz

v^*_{Ld} and v^*_{Lq}. In addition, the motor voltages due to cross-couplings between d- and q-axis as well as the voltage induced by the moving permanent magnet rotor can be added as decoupling terms, i.e. $v_{Dd} = -\omega p L_q i^*_{Mq}$ and $v_{Dq} = \omega p L_d i^*_{Md}$, which leads to the required motor voltages v_{Md} and v_{Mq}. Finally, the already derived voltage components of VSI 1 v_{1d} and v_{1q} are subtracted to obtain the remaining voltages of VSI 2 v_{2d} and v_{2q}.

3.4 Comparative Evaluation

The performance of the proposed electrolytic capacitor-less solution is evaluated in the context of a 7.5 kW single-phase-supplied compressor system for railway brakes with the specifications given in **Tab. 3.1**. The system is supplied from the tertiary transformer winding of the railway vehicle, which in nominal operation provides a single-phase RMS voltage of 400 V/50 Hz, however, due to large voltage tolerances of the railway grid, can vary in a wide range between 360 V and 480 V.

Based on these specifications, in the following the influence of the proposed control strategy on the system design is compared with the state-of-the-art, i.e. the occurring voltage and current stresses, and characteristic waveforms are analyzed and compared.

3.4.1 Dual-Inverter With Electrolytic Capacitor

As given in [149] and also deduced in **Section 3.2**, for the state-of-the-art system the maximum acceptable motor voltage is limited to $V_P = \hat{V}_G/4$, which for the minimum grid voltage results in $V_P = 127$ V. Hence, a motor with a maximum motor constant of $k_V = p\Psi_{PM} = V_P/\omega = 0.33$ Vs can be selected, and for a maximum input power of 9 kW a motor peak current of

$i_{\mathrm{Mq}} = I_0 = 47\,\mathrm{A}$, i.e. a motor phase RMS current of $I_{\mathrm{PH0rms}} = I_0/\sqrt{2} = 33\,\mathrm{A}$, results. The corresponding waveforms are shown in **Fig. 3.4(a)**.

3.4.2 Dual-Inverter Without Electrolytic Capacitor

Assuming a motor with the same motor constant of $k_{\mathrm{V}} = 0.33\,\mathrm{Vs}$, the current stresses for the proposed control concept can directly be calculated, and result in a pulsating q-current with an average current of $I_0 = 47\,\mathrm{A}$ and a comparably small d-current component such that the phase current can be approximated by $I_{\mathrm{PHrms}} = \sqrt{3/2} I_{\mathrm{PH0rms}} = 41\,\mathrm{A}$ [80]. Thus, the elimination of the electrolytic capacitor comes at the expense of increased conduction losses and a poor utilization of VSI 2, which for the same motor voltage $V_{\mathrm{P}} = V_0 = \hat{V}_{\mathrm{Gmin}}/4$ is actually only needed in close vicinity of the grid voltage zero-crossings (cf. **Fig. 3.4(b)**). Consequently, for the proposed control concept a motor with a larger motor constant k_{V} should be selected, since no limitation by the grid voltage exists, and a higher motor voltage decreases the average q-current (cf. **Eqn. (3.5)**) and extends the operating interval of VSI 2. As shown in **Fig. 3.4(c)**, for example, doubling the motor voltage to $V_{\mathrm{P}} = 2V_0 = \hat{V}_{\mathrm{Gmin}}/2$ leads to a continuous operation of both VSIs and reduces the motor phase current to $I_{\mathrm{PHrms}} = 24\,\mathrm{A}$, which is below the phase current obtained with the state-of-the-art system, even though the d-current is increased now. Clearly, it has to be mentioned that the voltage stresses at the semiconductor devices of VSI 2 and the secondary DC-link capacitor C_{DC2} are now increasing.

In **Fig. 3.5(a)**, the dependency of the phase current and DC-link voltage stresses with respect to the selected motor voltage are illustrated for a range of $V_{\mathrm{P}} \in [V_0, 3V_0] = [127\,\mathrm{V}, 382\,\mathrm{V}]$. It can be noticed that for low motor voltages the q-current scales inversely proportional to the motor voltage, i.e. $I_{\mathrm{PHqrms}} = 1/\sqrt{3}\, P_0/V_{\mathrm{P}}$, and thus also the motor phase current I_{PHrms} reduces similarly. However, as soon as the motor voltage V_{P} exceeds $\hat{V}_{\mathrm{G}}/2$, the first inverter is operated continuously with $M = 1$ and i_{M} becomes proportional to $|i_{\mathrm{G}}|$ (cf. **Eqn. (3.6)**)). Thus, for a given input power this means that i_{M} remains unchanged even if the motor voltage is further increased. As shown in **Fig. 3.5(a)**, this transition point clearly depends on the actual grid RMS voltage and for the minimum grid voltage actually also represents the optimum design point. This can be verified by using simple performance indices to estimate the dependency of conduction and switching losses of both VSIs on the selected motor voltage [152].

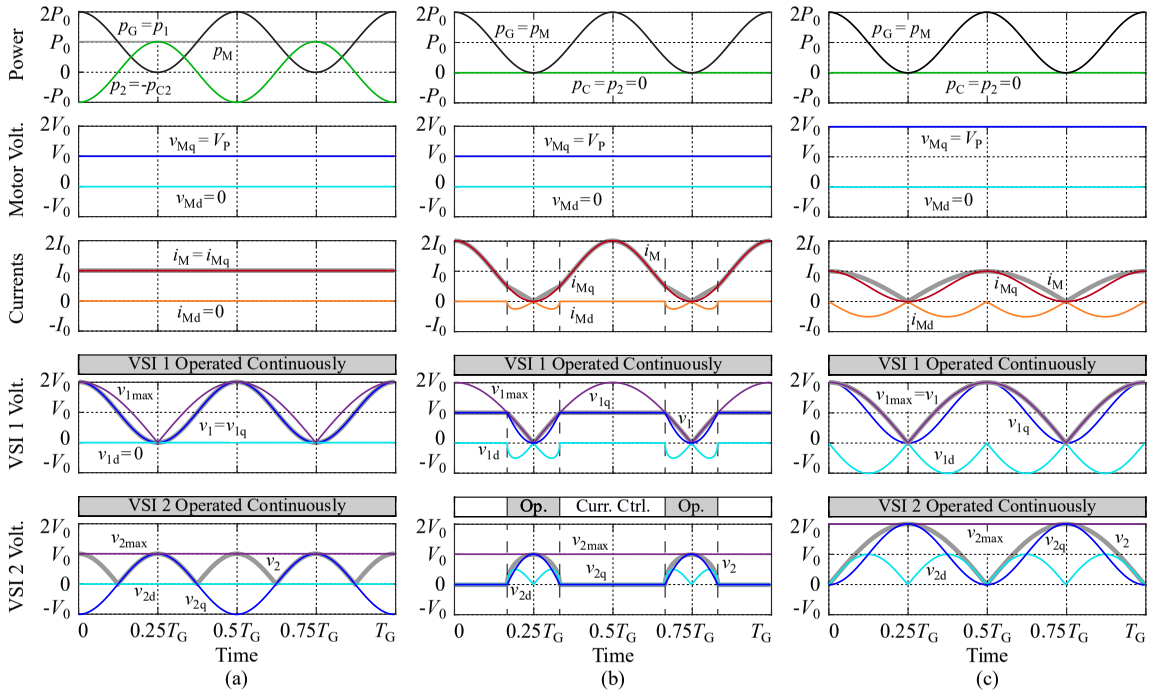

Fig. 3.4: Characteristic waveforms over one grid period T_G for **(a)** the state-of-the-art control scheme with an electrolytic capacitor for the maximum motor voltage $V_P = V_0 = \hat{V}_G/4$, **(b)** the proposed solution for $V_P = V_0 = \hat{V}_G/4$ causing increased motor currents and **(c)** the proposed solution for $V_P = 2V_0 = \hat{V}_G/2$, achieving a reduced motor current stress compared to (a).

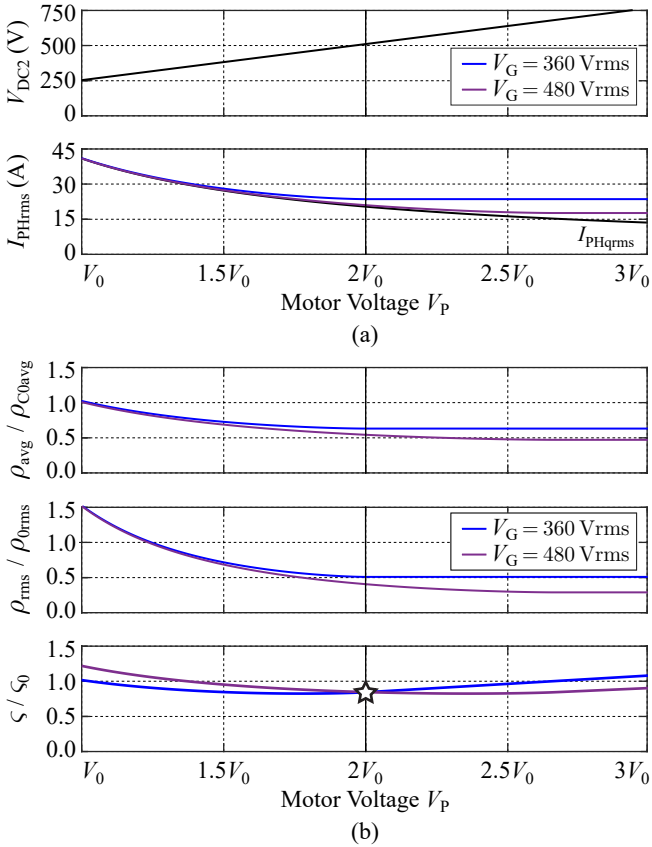

Fig. 3.5: Performance evaluation of the proposed electrolytic capacitor-less dual-inverter concept with respect to the motor voltage $V_P = V_0 ... 3V_0$; **(a)** Secondary DC-link voltage V_{DC2} and phase current stress I_{PHrms} for the minimum and maximum grid voltage. **(b)** Loss related performance indices scaled to the corresponding values of the state-of-the-art system, indicating a significant improvement for all indices at the selected motor voltage $V_P = 2V_0 = 255\,V$.

The conduction losses of inverters employing IGBTs with antiparallel diodes, depend on the average and RMS currents flowing through the devices. Assuming similar conduction behaviour for the IGBT and the antiparallel diode, the overall semiconductor conduction losses, can be assessed by the sum of the average currents and the sum of the squared RMS currents

$$\rho_{\mathrm{avg}} = \sum_j \left(I_{\mathrm{Davg},j} + I_{\mathrm{Tavg},j} \right) \tag{3.10}$$

$$\rho_{\mathrm{rms}} = \sum_j \left(I^2_{\mathrm{Drms},j} + I^2_{\mathrm{Trms},j} \right). \tag{3.11}$$

Furthermore, assuming a linear dependency of the semiconductor switching losses on both the switched voltage v_{T} and the switched current i_{T}, the overall switching losses can be assessed by the sum of the product $v_{\mathrm{T}} i_{\mathrm{T}}$ averaged over one grid period T_{G} as

$$\varsigma = \sum_j \langle v_{\mathrm{T},j}\ i_{\mathrm{T},j} \rangle_{T_{\mathrm{G}}}. \tag{3.12}$$

Fig. 3.5(b) shows the dependency of the introduced performance indices ρ_{avg}, ρ_{rms}, and ς scaled to the corresponding values of the state-of-the-art system, i.e. $\rho_{0\mathrm{avg}} = 180\,\mathrm{A}$, $\rho_{0\mathrm{rms}} = 6.7\,\mathrm{kA}^2$ and $\varsigma_0 = 62\,\mathrm{kVA}$, with respect to the selected motor voltage. For a given input voltage it clearly turns out that $\rho_{\mathrm{avg}}/\rho_{0\mathrm{avg}}$ and $\rho_{\mathrm{rms}}/\rho_{0\mathrm{rms}}$ decrease with increasing motor voltage as long as $V_{\mathrm{P}} \leq \hat{V}_{\mathrm{G}}/2$ and afterwards stay constant. On the other hand, ς/ς_0 also decreases until $V_{\mathrm{P}} = \hat{V}_{\mathrm{G}}/2$, however, afterwards increases again due to the increasing switched voltage v_{T}. Consequently, in terms of inverter losses, the optimum motor voltage is found at the transition point $V_{\mathrm{P}} = 2V_0 = \hat{V}_{\mathrm{Gmin}}/2$, where compared to the state-of-the-art system roughly 45 % lower conduction losses and around 15 % lower switching losses are achieved.

Assuming an inverter design with equal conduction and switching losses, an overall loss reduction of around 30 % can be obtained, which besides the elimination of the electrolytic capacitor also results in a substantially smaller heatsink volume.

3.5 System Verification

In a first step, the proper operation of the electrolytic capacitor-less drive system implementing the proposed closed-loop control structure of **Section 3.3**

Tab. 3.2: Summary of the motor and circuit parameters.

Voltage Constant (k_V)	0.65 Vs
Number of Pole Pairs (p)	5
Motor Inductance ($L_d = L_q$)	2.8 mH
Motor Inertia (J_M)	4.5 mkgm²
Drivetrain Inertia (J_{TOT})	13.5 mkgm²
EMI Capacitor (C_{EMI})	10 µF
EMI Inductor (L_{EMI})	70 µH
Input Capacitor (C_{DC1})	10 µF
DC-Link Capacitor (C_{DC2})	50 µF

is verified by circuit simulations. The simulation is conducted for the nominal operating point of the underlying application with an output power of 7.5 kW at 3700 rpm and an input supply voltage of 400 V/50 Hz. As deduced in **Section 3.4**, the performance optimum of the converter is achieved at $V_P = 2V_0 = 255$ V, resulting in a motor constant of $k_{Vopt} = 0.66$ Vs. Hence, the PMSM 1FT7-084 from Siemens [113], characterized by $k_V = 0.65$ Vs, is employed. The moment of inertia of the drivetrain is assumed to be $J_{TOT} = 13.5$ mkgm². The motor parameters and selected circuit parameters are summarized in **Tab. 3.2**.

The simulated steady-state waveforms for $V_G = 400$ Vrms and $V_P \approx 250$ V are shown in **Fig. 3.6**. The instantaneous voltage ratio v_{1max}/V_P defines the envelope of the motor phase currents i_{Ma}, i_{Mb} and i_{Mc}, which contains a fundamental component with $2f_G = 100$ Hz, as well as the required operation mode. As can be noted, since v_{1max} is exceeding V_P, there are time intervals where either both VSIs have to actively apply a voltage to the motor or where VSI 2 is only used to control the motor current, i.e. $v_1 < v_{1max}$ or $M_1 < 1$. It can be noticed that the resulting interval for $M_1 < 1$ is slightly extended compared to $v_{1max} > V_P$, which is a direct consequence of the non-zero reference capacitor power $p^*_{C2} \neq 0$ W. Regardless of this, the control keeps the grid current i_G sinusoidal and in phase with the grid voltage v_G, verifying PFC operation. The achieved THD is below 4 % and is mainly limited by the passive diode bridge, which causes current distortions in the vicinity of the voltage zero-crossings.

Furthermore, the speed controller ensures an average speed $\bar{\omega}$ equal to the reference, whereas the actual speed shows a ripple of

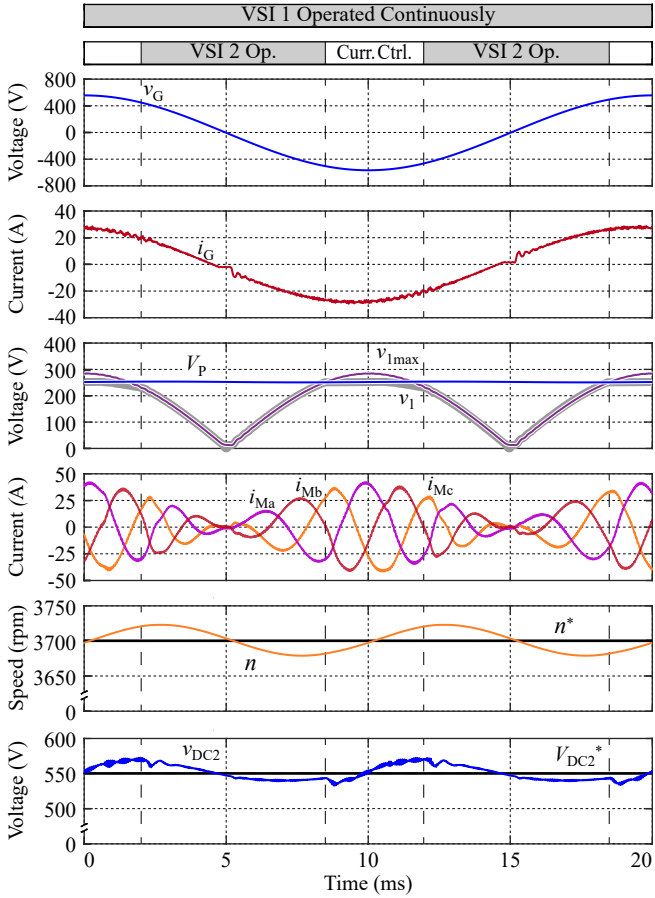

Fig. 3.6: Simulated steady-state waveforms for the proposed electrolytic capacitor-less single-phase AC dual-inverter concept showing the grid, dual-inverter, motor and DC-link waveforms as well as the operating mode within one grid period $T_G = 20\,\text{ms}$. The corresponding references are indicated by dashed lines.

$\Delta\omega = P_0/(4\pi f_G \bar{\omega} J_{TOT}) = 2.3\,\mathrm{rad/s}$, i.e. 22 rpm or around 0.6 % [80]. The DC-link reference voltage is set to $V^*_{DC2} = 550\,\mathrm{V}$, which is above $2V_P \approx 500\,\mathrm{V}$ to ensure full controllability even during voltage deviations. Theoretically, the secondary DC-link voltage would be constant, however, a limited controller bandwidth and disturbances are causing a certain voltage fluctuation of around 35 V. In a conventional system, this voltage ripple would correspond to a DC-link capacitance of 1.2 mF, which is 24 × larger than the capacitance used in the proposed solution without electrolytic capacitors.

3.6 Summary

In this Chapter, a novel control strategy for the single-phase AC dual-inverter topology is proposed, where twice grid frequency power pulsation is covered by the inertia of the drivetrain, such that no electrolytic DC-link capacitor is required. The corresponding operating principle, including the motor voltage division strategy and the motor current reference generation, and the introduced control structure, which ensures a sinusoidal input current, the requested average speed, and a certain DC-link voltage, are explained in detail. The proper operation is verified by circuit simulations, achieving a DC-link voltage ripple of 35 V in a 7.5 kW system with a DC-link capacitance of only 50 µF. In contrast to the state-of-the-art, the analyzed concept does not feature an inherent grid-voltage dependent limit on the maximum achievable motor voltage. Thus, the system performance is evaluated with respect to this additional degree of freedom. Simple performance indices assess the corresponding converter losses, and the loss minimum is achieved for a motor voltage equal to half the peak grid voltage. For the analyzed compressor application with a wide input voltage range, the semiconductor losses can be reduced by 30 % compared to the state-of-the-art dual-inverter system with electrolytic capacitor.

Hence, the proposed concept overcomes the limitations of a conventional operation of the single-phase AC dual-inverter topology and therefore is a promising solution to substantially improve the converter system's power density and avoid electrolytic capacitors, also increasing the converter's lifetime.

4

Conclusion and Outlook

The increasing demand for auxiliary systems in railway vehicles is driven by advancing rail electrification. It is further incentivized by the United Nation's sustainability goals as well as societal pressure to reduce Green House Gas (GHG) emissions and to limit the associated temperature increase to not more than 1.5 °C. At the same time it has to also be economically viable. In this context, the industry specifies the requirements for next-generation auxiliary systems like pumps, fans and compressors for the rolling stock as compact, lightweight, highly efficient, reliable, and redundant. The same challenges are valid for general electro-mechanical energy conversion systems commonly equipped with Variable Speed Drives (VSDs) to operate a general mechanical load with a desired speed.

This thesis focuses on railway vehicles' single-phase-supplied onboard compressor units to analyze and verify possible performance improvements. On the one hand, those are based on latest power semiconductor technology, i.e. Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). On the other hand, conceptual enhancements are proposed, like a novel Power Pulsation Buffer (PPB) concept for single-phase-supplied VSD systems, which is based on the stored kinetic energy of the drivetrain and accordingly allows to avoid lifetime-limited electrolytic capacitors for power pulsation buffering. After a detailed analysis, including the derivation of the corresponding control structure, the PPB concept is used to implement a motor integrated electrolytic capacitors-less variable speed compressor drive, which achieves very high power density and extended lifetime. In addition, theoretical considerations for utilizing the concept in a dual-inverter-based system are presented. The main findings of this thesis will be summarized, and future trends and research areas will be discussed in the following.

4.1 Results of this Thesis

The main achievements of this thesis are summarized in the following.

- **MPPB Concept**

  In order to eliminate the need for a DC-link energy storage, the pulsating power associated with single-phase Power Factor Correction (PFC) rectifier supply is forwarded through the DC-link and inverter to the motor. Accordingly, the motor generates a grid power proportional pulsating torque, which due to the drivetrain inertia, however, results in a minor speed ripple, i.e. the drivetrain inertia is employed as PPB, instead of an electrolytic capacitor in the DC-link. The basic concept is similar to the working principle of conventional single-phase motors, although VSD capability and unity power factor operation are achieved in addition.
  The proposed Motor-Integrated Power Pulsation Buffer (MPPB) concept offers fundamental simplicity with the potential to drastically reduce or, theoretically, even fully eliminate a DC-link energy storage capacitor. Consequently, a more compact system can be achieved, which also overcomes the lifetime limitations present in state-of-the-art electrolytic capacitors-based solutions.

- **MPPB Control Structure**

  Concerning control, MPPB operation can be achieved by the rearranging of outer control bocks of the control structure of a conventional two-stage system, comprising a PFC rectifier front-end and a Voltage Source Inverter (VSI) output stage decoupled by a DC-link capacitor. As the current control loops and sensors are unaffected, the concept can also be used in the course of retrofitting existing systems. The resulting control structure is still implemented in cascaded form, achieving the desired average speed control and ensuring a sinusoidal grid current and/or ohmic grid behavior. The intermediate DC-link voltage is balanced through the inverter/motor power setpoint, which defines the motor currents. However, due to existing disturbances residual low-frequency DC-link voltage fluctuations appear, which cannot be fully eliminated by the limited bandwidth DC-link voltage control. The resulting voltage ripple can be reduced by

- *a larger DC-link capacitance*
  as the increased energy storage reduces the voltage fluctuation for a given disturbance and/or residual differences of the rectifier stage power supply and the inverter stage input power. However, this measure would directly increase the converter volume and cost and thus should be omitted;

- *a control feedforward term*
  to eliminate or at least reduce the effect of the power flow disturbance. An in-depth analysis identifies the instantaneous (magnetization) power demand of the motor inductances, required by the time-varying q-current, as the primary cause of the disturbance. A compensation term which largely eliminates the disturbance is proposed;

- *an increased control bandwidth*
  originating from a higher switching frequency or timing improvements to reduce delay times (in the inner current control loop). While switching frequency is directly related to switching losses, the latter enables a bandwidth and voltage ripple improvement of around 60 % without increasing the system losses.

▸ **Extended Functionality**

Even though the proposed drive system does not employ any significant energy storage, grid interruptions should be survived without triggering protective measures to ensure maximum operability. In case of a short grid interruption, the PFC rectifier power supply is discontinued, however, the DC-link voltage should remain at the given voltage level to ensure minimal ramp-up time after the interruption. Thus, the inverter continues operation and supplies the DC-link from the kinetic energy stored in the rotating drivetrain. For extended interruptions, where the speed of the drivetrain decays to speed values close to zero due to the remaining load torque, the system switches to battery supply and continues operation at reduced power and/or speed. Advantageously, for AC and DC supply the same control concept can be employed, which minimizes the software-related implementation and maintenance effort.

- **Voltage-Slope-Limited Switching of SiC MOSFETs**

  Next-generation Wide-Bandgap (WBG) power semiconductors hold the promise of increasing the inverter's efficiency and power density. The performance enhancement is based on unipolar switching devices, which feature ohmic on-state characteristic and high switching speeds. However, the voltage slew rate applied to the motor must be limited in order to prevent surge voltages at the motor terminals resulting from cable reflections or an unequal distribution of the voltage across motor windings potentially resulting in partial discharge phenomena, which would damage the winding insulation.
  Theoretical considerations have shown that gate drive modifications are the most promising solution to limit the maximum voltage slope of the switching transitions in motor-integrated converter systems, which allow to program $\mathrm{d}v/\mathrm{d}t$-values such that no limitations concerning cable reflections need to be considered. For achieving the $\mathrm{d}v/\mathrm{d}t$-limitation, an external Miller capacitor is placed between drain and gate of each power MOSFET in combination with suitable gate resistor values. The maximum voltage slope occurs for turn-on at zero (load) current, i.e. Zero-Current Switching (ZCS), while the turn-off voltage slope saturates once an analytically calculated "kink current" is passed. Significant turn-off switching losses occur only after this point, which leads to the finding that switching losses in a bridge-leg are not quadratically dependent on the switched current (at least under limited voltage slope conditions). Instead, the dependence on current is piecewise linear, with the second linear function starting at the kink current value. The voltage slope and loss models are validated on a SiC MOSFET bridge-leg for a general purpose 10 kW 800 V DC-link VSD system with $\mathrm{d}v/\mathrm{d}t$-limitations of 10 V/ns and 15 V/ns, where an excellent matching between the model and the measured bridge-leg losses is found.

- **MPPB Performance Evaluation**

  The analysis of the motor phase currents reveals that the MPPB concept results in an increase of the phase current peak value of 100 %, contradicting the employment of inverter output filters. However, this finding has no significant effect on the motor, as the motor design is commonly limited by thermal properties and not by current-related magnetic saturation. Beneficially, the MPPB concept has no effect on the average value of the phase currents, which largely defines the loss

components of conventional Insulated Gate Bipolar Transistor (IGBT)-based inverter systems. However, the RMS value of the phase currents increases by ≈ 22 % which results in an increase of ≈ 50 % of corresponding loss components like power MOSFET conduction losses or motor winding losses. A detailed analysis shows that the phase current stresses remain symmetrical as long as the electrical frequency of the motor is different from the grid frequency or twice the grid frequency. Thus, a motor with a suitable number of pole pairs should be selected to avoid these critical frequencies in stationary operation and to ensure that the frequencies are only assumed during transients or at the startup. In this case overdimensioning can be avoided, and the nominal motor losses increase by around 25 %, assuming equal winding and no-load losses.
Assuming a conventional IGBT-based realization the inverter losses remain in a first approximation unchanged. For a high performance SiC-based inverter with modified gate drives ensuring $\mathrm{d}v/\mathrm{d}t$-limited switching an estimated worst-case loss penalty of 17 % has to be accepted, nevertheless a higher performance than for IGBT-based systems is achieved.
The revealed loss penalties are a comparable small cost for the achieved volume reduction and lifetime improvement gained by avoiding electrolytic capacitors.

- **Motor-Integrated Hardware Demonstrator**

  Avoiding the electrolytic capacitor DC-link energy storage enables full motor integration, which eliminates shielded cables and/or motor cable reflections, and accordingly allows higher $\mathrm{d}v/\mathrm{d}t$-limits of the switching transitions resulting in lower switching losses. Furthermore, the integration of inverter and motor in a single housing results in excellent Electromagnetic Compatibility (EMC) and allows to employ a combined cooling system for the power electronics and the motor.
  The implemented 7.5 kW hardware demonstrator utilizing the MPPB concept verifies the expected high performance and achieves a power density of 0.91 kW/L (15 W/in^3) or a total volume of 8.2 L (incl. the motor), while only the electrolytic DC-link capacitors of the conventional approach would occupy 1 L of additional volume. The system matches the loss models over the full torque range. It achieves a nominal grid-to-motor-shaft efficiency of 91.4 %, which corresponds to 703W of total system losses and ensures IES 2 compliance. For operation

with output powers above 5 kW or 66 % of nominal load the grid-to-motor-shaft efficiency remains above 90 %. Compared to a conventional implementation, a worst-case loss penalty of 17 % or 100 W has to be accepted at nominal operation, while the averaged losses (over the full torque range) increase only from 447 W to 491 W, or 9.8 %. The demonstrator system features extended functionality, including the ride-through capability employed during grid interruptions and would achieve CISPR 11 Class A compliance at full integration. In addition, the measured low-frequency DC-link voltage ripple of 35 Vpkpk matches the simulated value for a DC-link capacitance of only 60 µF and can be reduced to 10 Vpkpk with the discussed control enhancements.

- **Dual-Inverter Topology**

  The proposed MPPB approach can be extended to various other converter topologies as shown in the second part of the thesis using the example of a dual-inverter topology which advantageously allows to omit the boost-functionality of the front-end rectifier stage and/or a HF switching bridge-leg and a boost inductor, resulting in reduced system volume, cost and complexity. For implementing the dual-inverter approach, a first VSI is supplied by a single-phase diode-bridge rectifier input stage through a primary DC-link and drives the Open-End Winding (OEW) three-phase motor. The opposite ends of the motor phase windings and/or the second set of motor terminals is connected to a second VSI stage featuring a second DC-link. Accordingly, the system requires only an Electromagnetic Interference (EMI) filter, a diode bridge, the OEW motor, and two VSIs, which could be implemented using low-cost six-pack IGBT modules and film capacitor DC-links.
  The proper operation of the proposed approach is verified by circuit simulations, achieving a DC-link voltage ripple of 35 Vpkpk with a DC-link capacitance of only 50 µF. Moreover, it is shown that in contrast to a single-phase supplied state-of-the-art dual-inverter system with diode-bridge front-end and electrolytic DC-link capacitors, the maximum achievable motor voltage is not inherently restricted by a grid-voltage-dependent limit. Using simple performance indices to assess the converter losses, the system performance is analyzed with regard to this additional degree of freedom and a loss minimum is identified for a motor voltage equal to half the grid voltage amplitude. The analysis also shows that the worst-case semiconductor losses can be reduced by 30 % compared to the state-of-the art.

Hence, the proposed concept overcomes the operating limitations of a conventional approach, besides improving the converter system's power density and avoiding electrolytic capacitors, resulting in extended lifetime.

4.2 Future Trends and Research Areas

This thesis proposes and analyzes several concepts enabling high power density implementations of single-phase-supplied motor-integrated VSD systems. Also, potential further research topics have been identified in the course of discussions of obtained results, which should be investigated in the future, as they could potentially further improve the system's performance regarding power density, efficiency and complexity.

- **Single-Inverter Topology**

  The performance of the built hardware demonstrator is mainly limited by the utilized semiconductor devices. The employment of multi-level bridge-legs could overcome this limitation, as low-voltage power transistors benefit from a higher Fiugre-of-Merit (FOM) leading to lower conduction and/or lower switching losses. Consequently, the two-level bridge-legs could be replaced by T-type or Flying Capacitor (FC) bridge-legs to improve the performance. Such approaches are especially beneficial for bridge-legs with $\mathrm{d}v/\mathrm{d}t$-limiting gate drives in combination with Quasi-Two-Level (Q2L) operation. The current dependent switching losses scale inversely with the number of levels resulting in substantially improved efficiency. In addition, the Q2L operation does not require larger capacitance values in the FC bridge-legs resulting in a negligible increase of the system volume compared to a two-level inverter approach.

- **Dual-Inverter Topology**

  The proposed and theoretically analyzed concept of the dual-inverter topology should be built and verified experimentally. First, detailed loss and EMI noise models should be developed. Subsequently, the performance penalty of low-cost six-pack IGBT modules, instead of latest generation SiC MOSFETs with $\mathrm{d}v/\mathrm{d}t$-limited switching, should be evaluated to include economic viability in the system analysis.

- **Drive System Considerations**

  Ongoing research regarding Pulse-Width Modulation (PWM)-operated power electronic converter systems for motors drives directly focuses on analyzing and improving the motor's lifetime under higher switching frequencies and elevated $\mathrm{d}v/\mathrm{d}t$ of the inverter output voltages. This direction is motivated by increased requirements on power density and efficiency, which promotes the application of WBG devices also in drive systems.
  On the other hand, these devices cause high $\mathrm{d}v/\mathrm{d}t$ switching transients and increased Common-Mode (CM) currents in the motor. The accordingly increased motor winding insulation stress requires advanced insulation systems and/or isolated motor bearings. Both result in increased motor costs and thus, raise the question of whether drive systems featuring continuous output voltages in combination with standard motors designed for AC-line operation, i.e. sinusoidal voltage supply, would be a more economical solution.
  However, inverters with sine-wave output filters are unfavorable for the proposed MPPB concept due to the doubled motor peak currents (compared to operation with constant instantaneous power supply), the additional passive components, and the necessary switching frequency increase required to achieve low filter volume and to meet the defined control objectives despite low-pass filtering. A promising alternative would be a single-to-three phase converter system with intermediate current DC-link, also called Current Source Converter (CSC). The main drawback of CSCs is the required reverse blocking capability of the employed switches, i.e. the series connection of a power diode and a unipolar power transistor per switch resulting in higher conduction losses, cooling effort and costs. However, the recent availability of monolithic bidirectional Gallium Nitride (GaN) power transistors allows to overcome this limitation and motivates further research in this direction. The MPPB concept could be directly employed in this context as it omits the need for energy storage or a power pulsation buffer. The required DC-link current would be defined by the maximum of the input and output peak currents. Alternatively, the instantaneous grid-angle-dependent maximum could be taken for improved performance and thus, the DC-link current would pulsate with the grid power. In summary, the utilization of the MPPB concept in a CSC would be an interesting alternative for single-phase-supplied drive systems in order

to ensure continuous motor voltages and enable the employment of standard low-cost motors designed for conventional AC-line operation.

Appendices

A

Low-Speed MPPB Operation with Constant Load Torque

In this Appendix, we investigate the low-speed limit of a Motor-Integrated Power Pulsation Buffer (MPPB)-operated system with a constant load torque. This investigation is performed with an abstracted system, where the Variable Speed Drive (VSD) is taken as lossless and forwards the complete grid power (see **Eqn. (2.1)**) to the motor.

The motor power is therefore given, and the inner motor torque is $t_M = p_G/\omega$. The torque difference $t_M - T_L$ is then applied to the motor (and the load) inertia J_M and defines the speed change of the motor, which can be written as:

$$J_M \frac{\partial}{\partial t}\omega(t) = t_M(t) - T_L = \frac{p_G(t)}{\omega(t)} - T_L. \tag{A.1}$$

We conduct the analysis for the use case described here, with a constant load torque T_L = cst., i.e. $k = 0$ (as discussed in **Section 2.2**). This dynamic system is shown as control-oriented block diagram in **Fig. A.1(a)**, and with the system described by a non-linear differential equation, the analysis must be conducted numerically to determine the minimal achievable average speed $\bar{\omega}_{\min}$ for continuous MPPB operation.

We use the critical specifications for our application ($T_L = T_{L,N} = 19.4\,\text{Nm}$, $f_P = 100\,\text{Hz}$, $J_M = 4.5\,\text{mkgm}^2$) and visualize the behavior across speeds. For large average speeds, the behavior is identical to that shown in **Fig. 2.2(e.ii)**, with an approximately symmetric speed ripple defined by **Eqn. (2.5)** as $2\Delta\omega = 13.7\,\text{rad/s}$. The first analyzed case in this Section selects a grid power $P_0 = 388\,\text{W}$ to achieve $\bar{\omega} = 20\,\text{rad/s}$, recalling that in steady-state the average grid power P_0 must equal the average mechanical power $T_L\bar{\omega}$ (see **Fig. A.1(c.i)**).

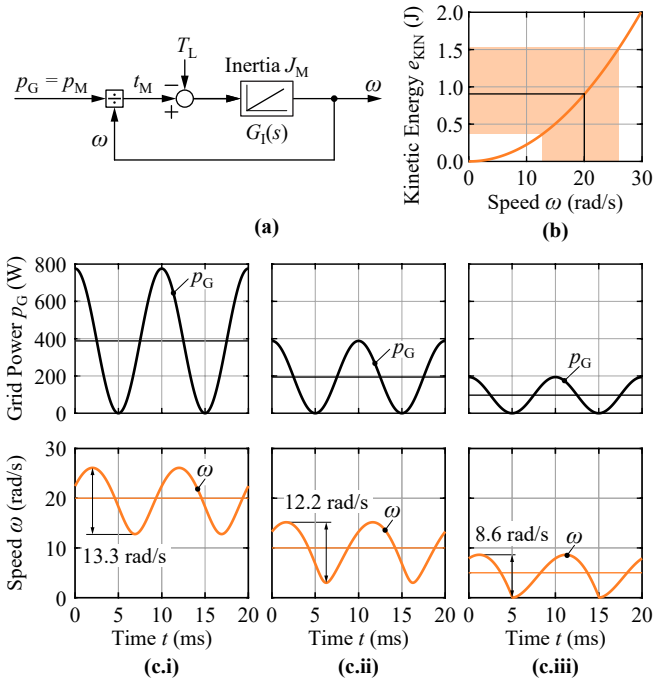

Fig. A.1: (a) Graphical representation of **Eqn. (A.1)** for a constant load torque T_L. **(b)** Kinetically-stored energy over speed with the indicated speed and energy range for operation at $\bar{\omega} = 20\,\text{rad/s}$ and $T_L = T_{L,N} = 19.4\,\text{Nm}$. **(c)** Grid power and instantaneous speed ω over one grid period for different average speeds **(i)** $\bar{\omega} = 20\,\text{rad/s}$, **(ii)** $\bar{\omega} = 10\,\text{rad/s}$, and **(iii)** $\bar{\omega} = 5\,\text{rad/s}$. The average values are indicated by the thin lines and the peak-to-peak speed ripples are annotated.

The corresponding time-domain waveform of the motor speed is shown in **Fig. A.1(c.i)**, where even though the average speed is only 5 % of the nominal speed, the system roughly behaves as expected. There is a slight asymmetry in the speed ripple amplitude (6.1 rad/s versus −7.2 rad/s) caused by the quadratic nature of the kinetic energy storage (see **Fig. A.1(b)**). The load power $T_\mathrm{L}\omega$ contains a significant fluctuation as it scales proportionally with the instantaneous speed $\omega(t) \neq \bar{\omega}$, i.e. the small ripple assumption is no longer valid. This actually reduces the toque pulsation $t_\mathrm{M} = p_\mathrm{G}\omega^{-1}$ seen by the system and results in a slight phase shift of the speed variation and reduces the peak-to-peak speed ripple slightly from 13.7 rad/s to 13.3 rad/s.

As we reduce the input power to half in **Fig. A.1(c.ii)**, the average speed is also halved to $\bar{\omega} = 10$ rad/s. A larger phase shift occurs, reducing the peak-to-peak ripple to 12.2 rad/s. The ripple amplitude asymmetry increases to 5.2 rad/s and −7.0 rad/s. With the ripple reduced, the instantaneous speed minimum also reduces.

Finally, through numerical methods, we find the minimum possible average speed for stationary MPPB operation (requiring $\omega(t) \geq 0$ rad/s) in the considered system as $\bar{\omega}_\mathrm{min} = 5$ rad/s ≈ 50 rpm (see **Fig. A.1(c.iii)** with $\omega(t)$ hitting zero).

B

Controller Design and Enhancements

In this Appendix, we detail the controller design and highlight enhancements to improve both steady-state and transient behavior in the Motor-Integrated Power Pulsation Buffer (MPPB) system.

We start our analysis with the inner-most control loop, the motor current controller, which is shown in **Fig. B.1(a)** (similar to the corresponding control loop of **Fig. 2.4**) and redrawn in **Fig. B.1(b)** in a more familiar model.

We investigate the control loop, design the necessary controller, highlight the bottlenecks and suggest improvement, and then repeat this process for the outer control loops, with a special emphasis on the DC-link voltage control with a feedforward term to reduce the low-frequency voltage ripple.

B.1 Motor Current Control Loop

The control implementation is a conventional digital controller, where the control loop of **Fig. B.1(b)** is executed discretely when the sawtooth carrier of the Pulse-Width Modulation (PWM) unit reaches the top or bottom of the range. This execution occurs synchronously with the duty-cycle updates [153] twice per PWM (switching) period $T_{\mathrm{PWM}} = T_{\mathrm{Isw}} = 1/f_{\mathrm{Isw}}$ of the inverter.

At the updated time instants, the reference value i^*_{Mq} is compared to the measured value i'_{Mq}, and the error δi_{Mq} is input to the controller Riq, which is characterized by its transfer function (with $\omega_{\mathrm{i}} = 1/\tau_{\mathrm{i}} = k_{\mathrm{p}}/\tau_{\mathrm{n}}$):

$$G_{\mathrm{PI}}(s) = k_{\mathrm{p}} + \frac{\omega_{\mathrm{i}}}{s} = k_{\mathrm{p}} + \frac{1}{s\tau_{\mathrm{i}}} = k_{\mathrm{p}}\frac{1 + s\tau_{\mathrm{n}}}{s\tau_{\mathrm{n}}}. \tag{B.1}$$

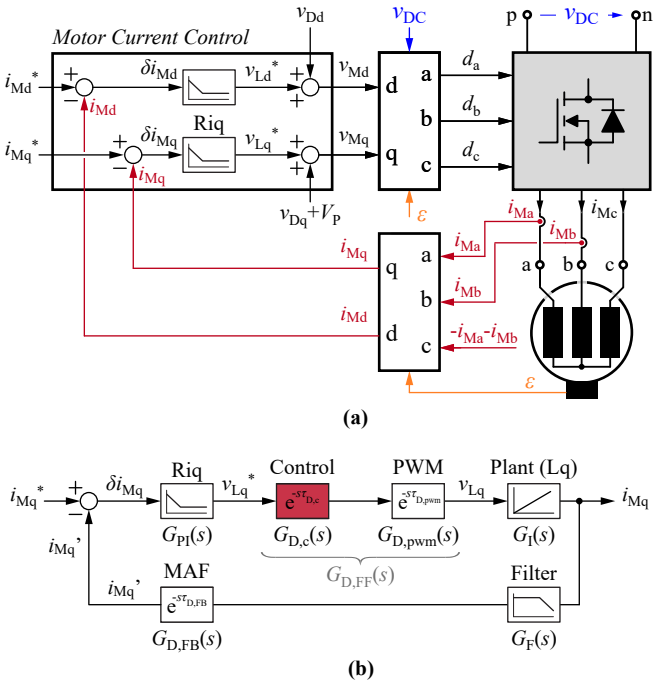

Fig. B.1: (a) Implementation of the motor current control (taken from **Fig. 2.4**) and **(b)** corresponding control loop for the q-current.

The controller output v_{Lq}^{*} is converted to a duty cycle and applied to the plant. In this process, a feedforward delay $\tau_{\mathrm{D,FF}}$ occurs, which comprises the delay between the controller execution and the duty-cycle update $\tau_{\mathrm{D,c}} = T_{\mathrm{Isw}}/2$ and the delay between the duty-cycle update and its influence to the plant $\tau_{\mathrm{D,pwm}}$, which is a result of the PWM operation itself. The average delay in the control loop can be approximated as a dead-time element of $\tau_{\mathrm{D,pwm}} = T_{\mathrm{Isw}}/4$ [154]. This feedforward term $\tau_{\mathrm{D,FF}} = \tau_{\mathrm{D,c}} + \tau_{\mathrm{D,pwm}}$ results in the transfer function of:

$$G_{\mathrm{D,FF}}(s) = G_{\mathrm{D,c}}(s) \cdot G_{\mathrm{D,pwm}}(s) = \exp\left(-s\tau_{\mathrm{D,FF}}\right). \tag{B.2}$$

The plant itself corresponds to the energy storage of the controlled quantity as an integrator $G_{\mathrm{I}}(s) = 1/(s\tau_{\mathrm{I}})$, which, for the motor current controller, equals the q-inductance $\tau_{\mathrm{I}} = L_{\mathrm{q}} = 3\,\mathrm{mH}$.

For the feedback, the instantaneous current value i_{Mq} is measured and the feedback path comprises a low-pass filter $G_{\mathrm{F}}(s) = 1/(1 + s\tau_{\mathrm{F}})$, with $\tau_{\mathrm{F}} = 1/\omega_{\mathrm{F}} = 1/(2\pi f_{\mathrm{F}})$ modelling the cut-off frequency of the sensor unit (here, $f_{\mathrm{F}} = 5\,\mathrm{MHz}$). A feedback delay is added to account for the time delay from the sensor to the controller execution, $G_{\mathrm{D,FB}}(s) = \exp\left(-s\tau_{\mathrm{D,FB}}\right)$, with the delay including $\tau_{\mathrm{D,FB}} = T_{\mathrm{MAF}}/2 + T_{\mathrm{D,vhdl}}$ since a Moving-Average Filter (MAF) filter [155] with $T_{\mathrm{MAF}} = T_{\mathrm{Isw}}$ is employed to eliminate all switching frequency components in the measured signal. $T_{\mathrm{D,vhdl}} = 2.1\,\mu\mathrm{s}$ accounts for the additional delay in the VHDL/C implementation.

The measured current is summed, with the appropriate sign, with the requested current, and the loop is closed.

B.2 Motor Current Controller Design

The current controller is designed around the phase margin criteria, where the phase margin PM defines the phase reverse (referenced to 180°) at the crossover frequency f_{CO} of the open loop transfer function $OL(s)$, which is $OL(s) = G_{\mathrm{PI}}(s) \cdot G_{\mathrm{D,FF}}(s) \cdot G_{\mathrm{I}}(s) \cdot G_{\mathrm{F}}(s) \cdot G_{\mathrm{D,FB}}(s)$.

We replace the delay with an equivalent low-pass filter (Pade approximation) with the time constant $\tau_{\mathrm{D}} = \left(\tau_{\mathrm{D,FF}} + \tau_{\mathrm{D,FB}}\right)\ 2\sqrt{3}/\pi$, arriving at $G_{\mathrm{D,FF}}(s) \cdot G_{\mathrm{D,FB}}(s) \approx G_{\mathrm{D}}(s) = 1/(1 + s\tau_{\mathrm{D}})$, and define the equivalent time constant $\tau_{\mathrm{EQ}} = \max\left(\tau_{\mathrm{F}}, \tau_{\mathrm{D}}\right)$ (assuming $\tau_{\mathrm{F}} >> \tau_{\mathrm{D}}$ or $\tau_{\mathrm{F}} << \tau_{\mathrm{D}}$, which is typically valid), arriving at the simplified equivalent delay term:

$$G_{\mathrm{D,FF}}(s) \cdot G_{\mathrm{D,FB}}(s) \cdot G_{\mathrm{F}}(s) \approx G_{\mathrm{EQ}}(s) = \frac{1}{1 + s\tau_{\mathrm{EQ}}} \tag{B.3}$$

and the simplified open loop transfer function $ol(s)$:

$$ol(s) = G_{\mathrm{PI}}(s) \cdot G_{\mathrm{I}}(s) \cdot G_{\mathrm{EQ}}(s) = \frac{k_{\mathrm{p}} + sk_{\mathrm{p}}\tau_{\mathrm{n}}}{s^2\tau_{\mathrm{I}}\tau_{\mathrm{n}} + s^3\tau_{\mathrm{I}}\tau_{\mathrm{n}}\tau_{\mathrm{EQ}}}. \tag{B.4}$$

The phase margin criteria for $ol(j\omega)$ are:

$$|ol(j\omega_{\mathrm{CO}})| = 1 \tag{B.5}$$

$$\arg\left[ol(j\omega_{\mathrm{CO}})\right] = PM - 180^\circ, \tag{B.6}$$

with the phase margin PM achieved at the angular cross-over frequency $\omega_{\mathrm{CO}} = 2\pi f_{\mathrm{CO}}$. Solving for the controller gains results in the fully-analytical expressions:

$$k_{\mathrm{p}} = \frac{\tau_{\mathrm{I}}}{\tau_{\mathrm{EQ}}} \cdot \sqrt{\frac{1 + 1/\alpha}{1 + \alpha}} \quad \text{and} \quad \tau_{\mathrm{n}} = \alpha\tau_{\mathrm{EQ}} \tag{B.7}$$

with $\alpha = \left(2\tan^2 PM + 1\right) + \sqrt{\left(2\tan^2 PM + 1\right)^2 - 1}$, and the crossover frequency result of:

$$f_{\mathrm{CO}} = \frac{1}{2\pi} \frac{1}{\tau_{\mathrm{EQ}}} \frac{1}{\sqrt{\alpha}}. \tag{B.8}$$

The proposed control loop, with $f_{\mathrm{lsw}} = 24\,\mathrm{kHz}$ and a phase margin of $PM = 40^\circ$, results in the controller gains of $k_{\mathrm{p}} = 23.4$ and $\omega_{\mathrm{i}} = 85.2\,\mathrm{rad/ms}$. With these controller gains, the full (OL) and simplified (ol) open-loop transfer functions are shown in **Fig. B.2**, with the indicated phase margin $PM = 40^\circ$ at the cross-over frequency $f_{\mathrm{CO}} = 1.2\,\mathrm{kHz}$, verifying the introduced approach.

The closed-loop transfer function can be calculated as:

$$CL(s) = \frac{i_{\mathrm{Mq}}}{i^*_{\mathrm{Mq}}} = \frac{G_{\mathrm{PI}}(s) \cdot G_{\mathrm{D,FF}}(s) \cdot G_{\mathrm{I}}(s)}{1 + OL(s)} \tag{B.9}$$

and simplified by $cl(s) = \frac{G_{\mathrm{PI}}(s) \cdot G_{\mathrm{I}}(s)}{1 + ol(s)}$, resulting in the simplified closed-loop transfer function:

$$cl(s) = \frac{k_{\mathrm{P}} + sk_{\mathrm{P}}(\tau_{\mathrm{n}} + \tau_{\mathrm{EQ}}) + s^2k_{\mathrm{P}}\tau_{\mathrm{n}}\tau_{\mathrm{EQ}}}{k_{\mathrm{P}} + sk_{\mathrm{P}}\tau_{\mathrm{n}} + s^2\tau_{\mathrm{I}}\tau_{\mathrm{n}} + s^3\tau_{\mathrm{I}}\tau_{\mathrm{n}}\tau_{\mathrm{EQ}}} \approx \frac{k_{\mathrm{P}}}{k_{\mathrm{P}} + s\tau_{\mathrm{I}}}, \tag{B.10}$$

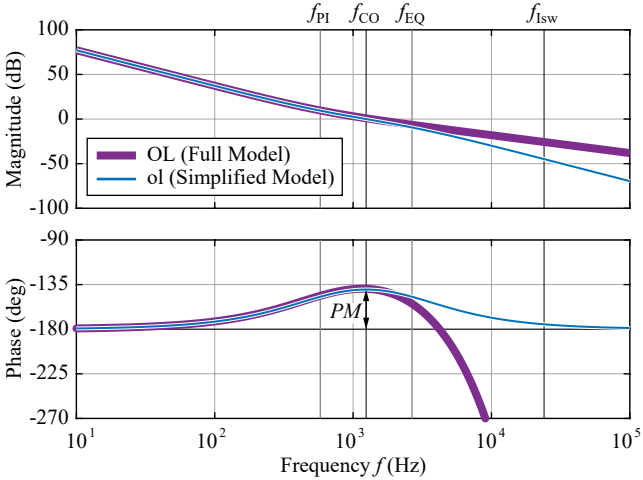

Fig. B.2: Bode plot of the full-model OL and simplified-model ol for loop and controller parameters. The phase margin PM is indicated at the crossover frequency f_{CO}, with the inverter switching frequency f_{Isw}, the cut-off frequency of the equivalent low-pass filter f_{EQ}, and the PI-controller cut-off frequency $f_{PI} = 1/(2\pi\tau_i)$ also highlighted.

where the approximation $cl(s) \approx 1/(1 + s\tau_I/k_P)$ can be used as an equivalent time constant for the design of an outer control loop (including for the DC-link voltage controller).

In case, the described system would employ a pure proportional controller, the analytical calculation results in:

$$f_{CO} = \frac{1}{2\pi} \frac{1}{\tau_{EQ} \tan PM} \tag{B.11}$$

$$k_P = \frac{\tau_I}{\tau_{EQ}} \frac{\sqrt{1 + 1/\tan^2 PM}}{\tan PM} \tag{B.12}$$

$$ol(s) = \frac{k_p}{s\tau_I + s^2\tau_I\tau_{EQ}} \tag{B.13}$$

$$cl(s) = \frac{k_p + sk_p\tau_{EQ}}{k_P + s\tau_I + s^2\tau_I\tau_{EQ}} \approx \frac{k_P}{k_P + s\tau_I} \tag{B.14}$$

B.3 Motor Current Control Improvements

The inner current controller is primarily limited by the sum of the delays, or the equivalent time constant of the controller. Next, we therefore investigate the timing constraints of the structure to find options for improvement.

As mentioned previously, the duty cycle of the PWM unit is only updated once the carrier reaches top or bottom, for an update rate of twice per switching period T_{PWM}. This behavior is shown in **Fig. B.3(a)**.

The ADC, however, operates in free run and gives new samples asynchronously. These samples are summed by an accumulator, which implements the first part of the MAF. The second part of the MAF — the division by the sample length — is performed within the controller itself. To ensure that averaging occurs over the full switching period with the double-update rate of the duty cycle, we implement two 180°-phase-shifted accumulators, one for the top update and one for bottom update of the PWM (Accu. I and Accu. II in **Fig. B.3(b)**). The data read-out and reset is synchronized with the duty-cycle update, similar to a synchronous sampling structure [156].

After the read-out of the MAF, the controller derives the new duty cycles, the calculation of which requires the control computation time T_{C}. Although T_{C} may be significantly smaller than $T_{\mathrm{PWM}}/2$, its result (the new duty cycle) can only be used at the next duty-cycle update, which is defined by the sawtooth carrier. In the end, then, the time difference $\Delta T = T_{\mathrm{PWM}}/2 - T_{\mathrm{C}}$ is wasted by waiting every half-cycle, as highlighted in **Fig. B.3(b)**.

To improve this time delay, the accumulator read-out can be shifted forward by ΔT (minus some margin) rather than synchronized with the duty-cycle, and the accumulator read-out now occurs shortly before the duty cycle update. We introduce a forward shift of T_{C} plus some margin (**Fig. B.3(c)**), and $\tau_{\mathrm{D,c}}$ is reduced from half the switching period to T_{C} alone. Here, $T_{\mathrm{C}} = 260\,\mathrm{ns}$ to account for the VHDL implementation of the current controller.

The PI controller gains are again calculated based on the phase-margin criteria of 40°, leading to a controller with $k_{\mathrm{p}} = 37.7$, $\omega_{\mathrm{i}} = 221.5\,\mathrm{rad/ms}$ and $f_{\mathrm{CO}} = 2.0\,\mathrm{kHz}$. The crossover frequency of the open-loop transfer function, then, is increased by nearly 60 % with this proposed delay reduction.

Finally, we want to evaluate and compare the closed-loop transfer function:

$$CL'(s) = \frac{i'_{\mathrm{Mq}}}{i^*_{\mathrm{Mq}}} = \frac{OL(s)}{1 + OL(s)}. \tag{B.15}$$

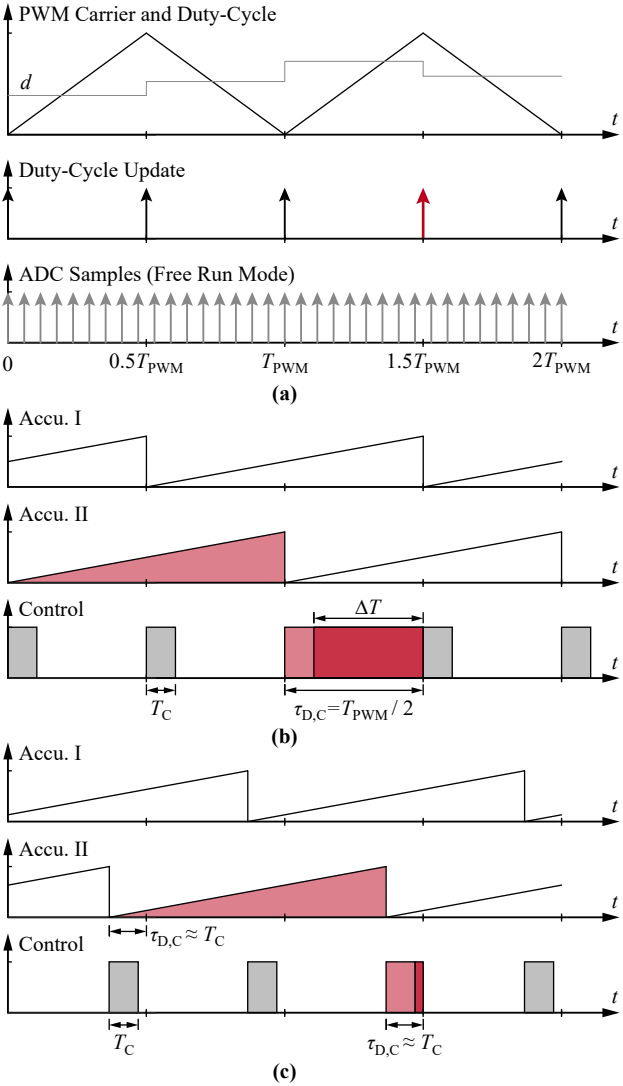

Fig. B.3: (a) PWM waveforms with indicated duty-cycle update and ADC sample timing. We highlight the timing considerations of the accumulators and the controller execution for the **(b)** conventional and **(c)** improved implementation of the duty-cycle update timing.

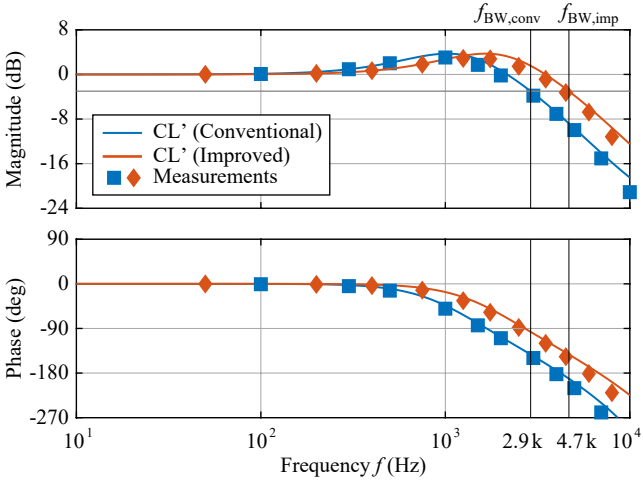

Fig. B.4: Model and verification measurement of the closed-loop transfer function $CL'(s) = i'_{\mathrm{Mq}}/i^*_{\mathrm{Mq}}$ for the conventional and improved implementation.

(Note that i_{Mq} cannot be evaluated directly in the selected implementation with the MAF filter before the dq-transform block). The original and improved closed-loop transfer function is shown in **Fig. B.4**, with the indicated −3 dB bandwidth for each implementation highlighted.

We observe excellent matching between the model and the measurements, with the small deviation around the resonances due to the neglected motor phase resistance. The improvement in timing improves the bandwidth from $f_{\mathrm{BW}} = 2.9\,\mathrm{kHz}$ to $f_{\mathrm{BW}} = 4.7\,\mathrm{kHz}$, an improvement of 60 %.

B.4 DC-Link Voltage Control Improvements

The same procedure can be applied to the DC-link voltage controller, where a particular improvement to the low-voltage ripple is sought. The equivalent time constant is now defined by the inner current controller $\tau_{\mathrm{EQ,V}} = \tau_{\mathrm{I}}/k_{\mathrm{P}}$, which would, in this case, be located in the feedforward path.

To achieve a bandwidth separation of around 4× from the inner current control, the phase margin target is $PM_{\mathrm{VDC}} = 62°$. The conventional controller gain is $k_{\mathrm{p,V}} = 0.117$, $\omega_{\mathrm{i,V}} = 56.7\,\mathrm{rad/s}$ and $f_{\mathrm{CO,V}} = 309\,\mathrm{Hz}$ and the improved controller gain is $k_{\mathrm{p,V}} = 0.188$, $\omega_{\mathrm{i,V}} = 147\,\mathrm{rad/s}$ and $f_{\mathrm{CO,V}} = 500\,\mathrm{Hz}$.

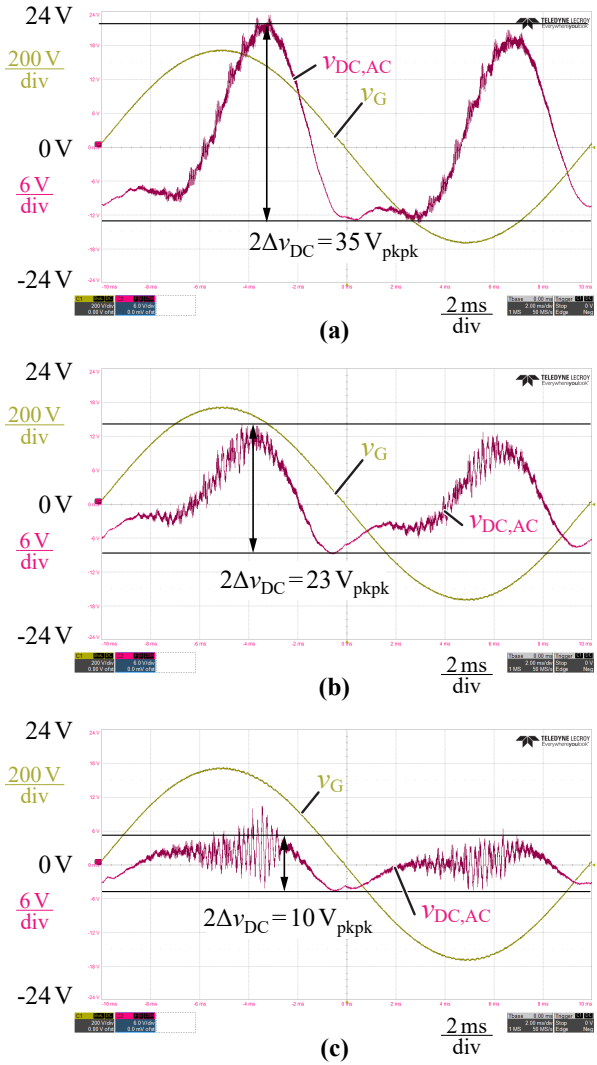

Fig. B.5: Measured grid voltage v_G and AC-component of the DC-link voltage $v_{DC,AC}$ at nominal operation for **(a)** conventional current control, **(b)** improved current control, and **(c)** improved current control with inductor voltage feedforward (see **Fig. 2.4**).

For each controller and timing implementation, the measured AC component of the DC-link voltage (measured with a high-pass filter) is shown in **Fig. B.5(a)** for the conventional controller and **(b)** for the improved controller operation. In the conventional case, the voltage ripple is $2\Delta v_{\mathrm{DC}} = 35\,\mathrm{Vpkpk}$, which is almost identical to the simulation results of **Fig. 2.5** (the simulation employs the same controller configuration). With the improved controller setting, the DC-link voltage ripple is reduced to $2\Delta v_{\mathrm{DC}} = 23\,\mathrm{Vpkpk}$.

Interestingly, the voltage ripple reduces by a 60 % factor, which can be explained straightforwardly. The timing structure allows higher controller gains while maintaining stability, which increases the gain of the open-loop transfer function and enables a higher crossover frequency. Because the open-loop transfer function appears in the denominator of the disturbance transfer function, the impact of any disturbances below the crossover frequency are reduced by the improved open-loop transfer function.

Even with this improvement, though, these results imply a significant amount of disturbance power at low frequencies (multiples of 100 Hz) that is resulting in a relatively large DC-link voltage fluctuation. We therefore look at the motor itself, and particularly at the waveforms surrounding the motor inductance (**Fig. B.6**).

Starting with the q-current (from **Eqn. (2.12)**), and considering the motor inductance $L_{\mathrm{q}} = 3\,\mathrm{mH}$, we can compute the magnetically-stored energy within the motor over several grid periods as $e_{\mathrm{Lq}}(t) = i_{\mathrm{Mq}}^2(t) L_{\mathrm{q}}/2$. We then find the magnetization power with $p_{\mathrm{Lq}}(t) = de_{\mathrm{Lq}}(t)/dt$, shown in **Fig. B.6**, which is the disturbance quantity. The inductive power demand of the motor, with a zero average ($\bar{p}_{\mathrm{Lq}}(t) = 0\,\mathrm{W}$), is acting as the low-frequency disturbance. The peak power is almost 1 kW, which is about 13 % of the average output power.

To address this disturbance in the control architecture, we calculate the inductor voltage that results from the q-current change as $v_{\mathrm{Lq}}(t) = p_{\mathrm{Lq}}(t)/i_{\mathrm{Mq}}(t) = L_{\mathrm{q}} di_{\mathrm{Mq}}(t)/dt$. The resulting voltage can be used as a feedforward term, along with the induced voltage V_{P}. We note that the derivation of the voltage requires a differentiation, with the associated concerns of robustness, but because the instantaneous grid phase angle is known from the Phase-Locked Loop (PLL) the inductor voltage can be calculated open-loop.

For a sinusoidal input, then, the inductor voltage can be calculated as $v_{\mathrm{Lq}}(\theta) = I_{\mathrm{M0}} L_{\mathrm{q}} f(\theta)$, with the function $f(\theta)$ as:

$$f\left(2\pi f_{\mathrm{G}} t\right) = 4 \cdot 2\pi f_{\mathrm{G}} \cdot \cos\left(2\pi f_{\mathrm{G}} t\right) \cdot \sin\left(2\pi f_{\mathrm{G}} t\right). \tag{B.16}$$

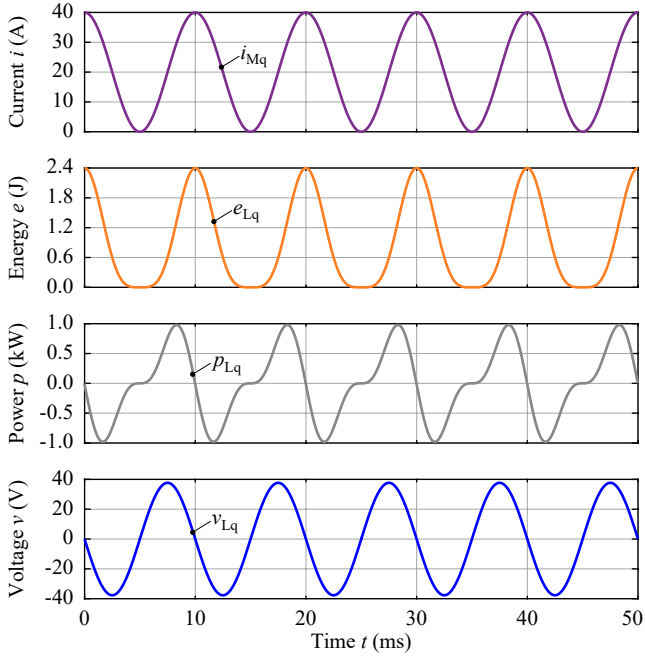

Fig. B.6: Motor inductance waveforms: q-current i_{Mq}, stored magnetic energy e_{Lq}, corresponding magnetization power p_{Lq}, and q-inductor voltage v_{Lq}, which can be used as a feedforward term to reduce the DC-link voltage ripple.

The feedforward term is implemented as shown in **Fig. 2.4**, and, with this improvement, the corresponding DC-link voltage measurement is shown in **Fig. B.5(c)**. The voltage ripple is reduced another 55 % — beyond the timing improvement — to a much-improved ripple of $2\Delta v_{DC} = 10$ Vpkpk.

C

Motor Phase Current Analysis under MPPB Operation

In this Appendix, we detail the phase currents in the inverter and motor under Motor-Integrated Power Pulsation Buffer (MPPB) operation, including an investigation of the loss-characteristic currents and different frequency ratios between the electrical motor frequency $f_\mathrm{E} = p\bar{\omega}/(2\pi)$ and the power pulsation frequency f_P.

First, we analyze the Root Mean Square (RMS) phase current stress under a variety of frequency ratio cases, and subsequently move to an average current analysis. For completeness, the analytical equations for all three phase currents are given below in **Eqn. (C.1)**, **Eqn. (C.2)**, and **Eqn. (C.3)**.

$$\begin{aligned} i_\mathrm{Ma}(t) = &- I_\mathrm{M0} \sin\left(p\bar{\omega}t + \varepsilon_0\right) \\ &- \frac{I_\mathrm{M0}}{2} \sin\left(p\bar{\omega}t + 2\pi f_\mathrm{P} t + \varepsilon_0\right) \\ &- \frac{I_\mathrm{M0}}{2} \sin\left(p\bar{\omega}t - 2\pi f_\mathrm{P} t + \varepsilon_0\right) \end{aligned} \tag{C.1}$$

$$\begin{aligned} i_\mathrm{Mb}(t) = &- I_\mathrm{M0} \sin\left(p\bar{\omega}t + \varepsilon_0 - \frac{2\pi}{3}\right) \\ &- \frac{I_\mathrm{M0}}{2} \sin\left(p\bar{\omega}t + 2\pi f_\mathrm{P} t + \varepsilon_0 - \frac{2\pi}{3}\right) \\ &- \frac{I_\mathrm{M0}}{2} \sin\left(p\bar{\omega}t - 2\pi f_\mathrm{P} t + \varepsilon_0 - \frac{2\pi}{3}\right) \end{aligned} \tag{C.2}$$

$$
\begin{aligned}
i_{\mathrm{Mc}}(t) = &- I_{\mathrm{M0}} \sin\left(p\bar{\omega}t + \varepsilon_0 + \frac{2\pi}{3}\right) \\
&- \frac{I_{\mathrm{M0}}}{2} \sin\left(p\bar{\omega}t + 2\pi f_{\mathrm{P}} t + \varepsilon_0 + \frac{2\pi}{3}\right) \\
&- \frac{I_{\mathrm{M0}}}{2} \sin\left(p\bar{\omega}t - 2\pi f_{\mathrm{P}} t + \varepsilon_0 + \frac{2\pi}{3}\right)
\end{aligned} \tag{C.3}
$$

C.1 RMS Current Stress

The phase currents are the superposition of three sinusoidal waveforms: $f_{\mathrm{i}} = f_{\mathrm{E}}$ with amplitude I_{M0} and $f_{\mathrm{ii}} = f_{\mathrm{E}} + f_{\mathrm{P}}$ and $f_{\mathrm{iii}} = f_{\mathrm{E}} - f_{\mathrm{P}}$, each with amplitude $I_{\mathrm{M0}}/2$. Depending on the ratio of f_{E} and f_{P}, though the coincidence of sines will vary, potentially leading to asymmetric phase current stresses.

We analyze the current amplitudes, maximum phase losses $P_{\mathrm{VPHmax}} = \max\,(P_{\mathrm{VMa}}, P_{\mathrm{VMb}}, P_{\mathrm{VMc}})$, and total losses $P_{\mathrm{VMcond}} = P_{\mathrm{VMa}} + P_{\mathrm{VMb}} + P_{\mathrm{VMc}}$ with $P_{\mathrm{VMj}} = \bar{p}_{\mathrm{VMj}}(t)$, $j = a, b, c$, for a variety of motor speeds (and resulting frequencies), with the results summarized in **Table C.1** for the speed ratio cases. The phase losses are benchmarked to $P_{\mathrm{VPH0}} = R_{\mathrm{s}} I_{\mathrm{M0}}^2/2$, which are the phase losses under conventional operation. For the first four cases in **Table C.1**, the corresponding phase currents (i_{Ma}, i_{Mb}, and i_{Mc}) and local conduction losses $p_{\mathrm{VMj}}(t) = R_{\mathrm{s}} i_{\mathrm{Mj}}^2(t)$, $j = a, b, c$, are shown in **Fig. C.1(a)** to **(d)** for phase a with $f_{\mathrm{P}} = 100\,\mathrm{Hz}$ and worst-case conditions. While the analysis is conducted for $f_{\mathrm{E}} \geq f_{\mathrm{Emin}} = p\bar{\omega}_{\mathrm{min}}/(2\pi) = 4\,\mathrm{Hz}$, with f_{Emin} derived as in **Appendix A**, the results are also, of course, valid for $f_{\mathrm{E}} \leq -f_{\mathrm{Emin}}$ (the opposite direction of rotation).

We now walk through each case to better detail the calculations behind the results of **Fig. C.1** and **Table C.1**.

Case a, $f_{\mathrm{E}} > f_{\mathrm{P}}$

In this case, the superposition maintains three distinct frequencies with the amplitudes given in **Table C.1** . The RMS stress is the superposition of the three sines, as:

$$
I_{\mathrm{PHrms}}^2 = \frac{1}{2} I_{\mathrm{M0}}^2 + \frac{1}{2}\frac{I_{\mathrm{M0}}^2}{4} + \frac{1}{2}\frac{I_{\mathrm{M0}}^2}{4} = \frac{3}{2}\frac{I_{\mathrm{M0}}^2}{2}. \tag{C.4}
$$

Tab. C.1: Overview of phase current stress, with a special emphasis on asymmetry, at different motor speeds and frequency ratios with I_{M0} equal to the q-current magnitude in conventional operation.

Condition	$f_i =$ f_E	$f_{ii} =$ $f_E + f_P$	$f_{iii} =$ $f_E - f_P$	$\hat{I}_{Ma,i}/$ I_{M0}	$\hat{I}_{Ma,ii}/$ I_{M0}	$\hat{I}_{Ma,iii}/$ I_{M0}	$P_{VPHmax}/$ P_{VPH0}	$P_{VMcond}/$ P_{VPH0}
(a) $f_E > f_P$	$f_E > 0\,\mathrm{Hz}$	$> 0\,\mathrm{Hz}$	$> 0\,\mathrm{Hz}$	1	1/2	1/2	3/2	9/2
(b) $f_E = f_P$	$f_E > 0\,\mathrm{Hz}$	$2f_E > 0\,\mathrm{Hz}$	$= 0\,\mathrm{Hz}$	1	1/2	$\frac{1}{2}\sin(\varepsilon_0)$	7/4	9/2
(c) $f_P/2 < f_E < f_P$	$f_E > 0\,\mathrm{Hz}$	$> 0\,\mathrm{Hz}$	$< 0\,\mathrm{Hz}$	1	1/2	1/2	3/2	9/2
(d) $f_P/2 = f_E$	$f_E > 0\,\mathrm{Hz}$	$3f_E > 0\,\mathrm{Hz}$	$-f_E < 0\,\mathrm{Hz}$	$\sqrt{\frac{5}{4} - \cos(2\varepsilon_0)}$	1/2	–	5/2	9/2
(e) $f_{Emin} < f_E < f_P/2$	$f_E > 0\,\mathrm{Hz}$	$> 0\,\mathrm{Hz}$	$< 0\,\mathrm{Hz}$	1	1/2	1/2	3/2	9/2

The conduction losses are $P_{\mathrm{VPH}} = 3/2\, P_{\mathrm{VPH0}}$ for a single phase and $P_{\mathrm{VMcond}} = 9/2\, P_{\mathrm{VPH0}}$ for the three-phase system. The waveforms are shown in **Fig. C.1(a)** at $f_{\mathrm{E}} = 120\,\mathrm{Hz}$, where we verify symmetrical stresses across the three phases.

Case b, $f_{\mathrm{E}} = f_{\mathrm{P}}$

With the frequencies equal, the result is two distinct frequency components with a DC-offset, since $f_{\mathrm{iii}} = 0\,\mathrm{Hz}$. The DC magnitude in phase a is $I_{\mathrm{M0}}/2\,\sin\varepsilon_0$, and, since both sines are multiples of the power pulsation frequency, there is a standing wave, as shown in **Fig. C.1(b)**. Because the phase currents are locked with the power pulsation frequency, the conduction losses of the phases are asymmetric.

The RMS stress in phase a is $I^2_{\mathrm{PHa,rms}} = \left(5 + 2\sin^2\varepsilon_0\right)/4\, I^2_{\mathrm{M0}}/2$, which now depends on ε_0, or the position at which the frequencies lock. For $\varepsilon_0 = 0$, which is the minimum stress for phase a, the RMS current is $I^2_{\mathrm{PHa,rms}} = 5/4\, I^2_{\mathrm{M0}}/2$ and for $\varepsilon_0 = \pi/2$, the maximum stress for phase a, the RMS current is $I^2_{\mathrm{PHa,rms}} = 7/4\, I^2_{\mathrm{M0}}/2$. The maximum conduction loss for a phase, then, is $P_{\mathrm{VPHmax}} = 7/4\, P_{\mathrm{VPH0}}$, an increase of 16 % for losses in a particular phase. Because the two remaining phases are 120°-phase-shifted, though, the total losses remain the same at $P_{\mathrm{VMcond}} = 9/2\, P_{\mathrm{VPH0}}$.

Case c, $f_{\mathrm{P}}/2 < f_{\mathrm{E}} < f_{\mathrm{P}}$

This case again results in three distinct frequencies, like in *Case a*, with the waveforms shown in **Fig. C.1(c)** for $f_{\mathrm{E}} = 80\,\mathrm{Hz}$.

Case d, $f_{\mathrm{P}}/2 = f_{\mathrm{E}}$

Here, two sine functions collapse into one, with $f_{\mathrm{i}} = -f_{\mathrm{iii}} = f_{\mathrm{E}}$, so for $f_{\mathrm{P}} = 100\,\mathrm{Hz}$, the result is $f_{\mathrm{i}} = -f_{\mathrm{iii}} = f_{\mathrm{E}} = 50\,\mathrm{Hz}$ with an amplitude of $I_{\mathrm{M0}}\sqrt{5/4 - \cos(2\varepsilon_0)}$. f_{ii} oscillates at $3f_{\mathrm{E}}$ with an amplitude of $I_{\mathrm{M0}}/2$.

These conditions result with $i_{\mathrm{Ma}}(t)$ equal to nearly $i_{\mathrm{Mq}}(t)$, as shown in **Fig. C.1(d)** for $f_{\mathrm{E}} = 50\,\mathrm{Hz}$. The asymmetry between the phases is increased further, with the RMS current stress for phase a of $I^2_{\mathrm{PHa,rms}} = [6 - 4\cos(2\varepsilon_0)]/4\, I^2_{\mathrm{M0}}/2$ for $\varepsilon_0 = 0$ (minimum stress for phase a) and $I^2_{\mathrm{PHa,rms}} = 1/2\, I^2_{\mathrm{M0}}/2$ and for $\varepsilon_0 = \pi/2$ (maximum stress for phase a) at $I^2_{\mathrm{PHa,rms}} = 5/2\, I^2_{\mathrm{M0}}/2$. The maximum conduction losses for a particular phase are $P_{\mathrm{VPHmax}} = 5/2\, P_{\mathrm{VPH0}}$, an increase in 66 % over the symmetric case. Again, the total losses remain the same due to the phase shift between the phases.

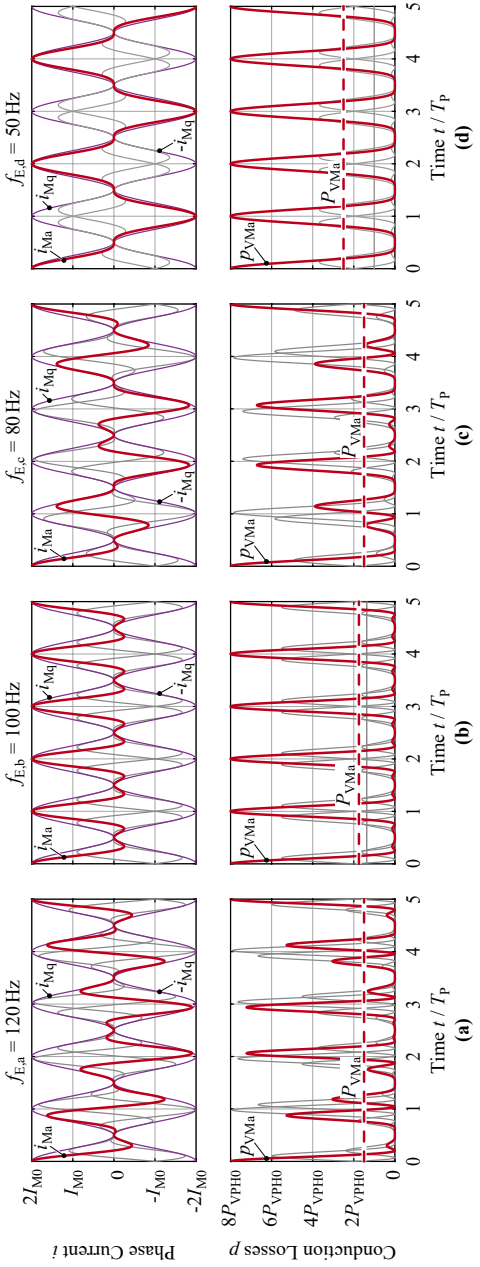

Fig. C.1: (a)-(d) Motor phase currents and corresponding local conduction losses for different electrical frequencies f_E and f_P = 100 Hz, indicating asymmetrical phase stress for particular cases of frequency ratios.

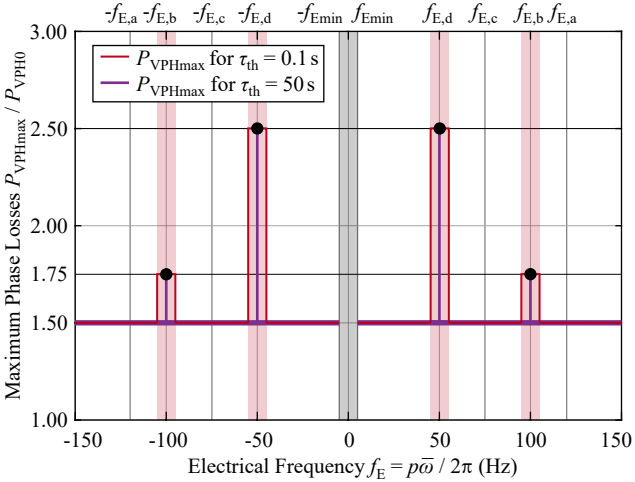

Fig. C.2: Maximum phase conduction losses P_{VPHmax} over the electrical frequency f_{E} with the illustration of the restricted operating areas for different thermal time constants τ_{th}. The prevented speed operating range according to **Appendix A** is indicated by the grey area. The • indicates the analytical calculations of **Table C.1**.

Case e, $f_{\mathrm{Emin}} < f_{\mathrm{E}} < f_{\mathrm{P}}/2$

This case is identical to *Case c*.

The total losses for this condition, even at the maximum phase stress, remain the same as for every other frequency ratio. With total losses identical, we primarily need to consider the thermal time constant of the key components — the motor and the inverter power semiconductors — in the vicinity of these key corner cases to verify safe operation.

We approximate the motor winding time constant as $\tau_{\mathrm{th}} = 50\,\mathrm{s}$ and a faster time constant of $\tau_{\mathrm{th}} = 0.1\,\mathrm{s}$ for the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) power semiconductors [157]. With these time constants, we can design the system to operate outside restricted frequency ranges as $|p\bar{\omega}| = 2\pi f_{\mathrm{P}}$ (see *Case b*), $|p\bar{\omega}| = \pi f_{\mathrm{P}}$ (see *Case d*), and $|\bar{\omega}| > |\bar{\omega}_{\mathrm{min}}|$, with a 0.01 Hz width for the slow motor time constant and a 5 Hz width for the faster power semiconductor time constant. These results are illustrated in **Fig. C.2**, where the maximum losses and the restricted frequency ranges are highlighted. Note that the motor frequencies corresponding to these restricted frequency ranges can be influenced via the number of pole pairs in the selected motor.

C.2 Absolute Average Current

With the RMS current analyzed for each case, we turn to analyze the average current stress of phase a, $I_{\mathrm{Ma,avg}}$, for each frequency ratio assuming a non-zero speed, i.e. $|\bar{\omega}| > 0\,\mathrm{rad/s}$.

We define $I_{\mathrm{Ma,avg}} = \frac{1}{T}\int_0^T |i_{\mathrm{Ma}}(\tau)|d\tau$ with T as the minimum period of i_{Ma}. Starting from $|i_{\mathrm{Ma}}(t)| = i_{\mathrm{Mq}}(t)|\sin(p\bar{\omega}t + \varepsilon_0)|$ with $i_{\mathrm{Mq}}(t) \geq 0\,\mathrm{A}$, we substitute $i_{\mathrm{Mq}}(t) = I_{\mathrm{M0}} + I_{\mathrm{M0}}\cos(2\pi f_{\mathrm{P}} t)$ and splitting the equation as $I_{\mathrm{Ma,avg}} = I^{i}_{\mathrm{Ma,avg}} + I^{ii}_{\mathrm{Ma,avg}}$, the results for each part are:

$$I^{i}_{\mathrm{Ma,avg}} = \frac{I_{\mathrm{M0}}}{T}\int_0^T |\sin(p\bar{\omega}\tau + \varepsilon_0)|d\tau = \frac{2}{\pi}I_{\mathrm{M0}} \tag{C.5}$$

$$I^{ii}_{\mathrm{Ma,avg}} = \frac{I_{\mathrm{M0}}}{T}\int_0^T [|\sin(p\bar{\omega}\tau + \varepsilon_0)|\cos(2\pi f_{\mathrm{P}}\tau)]\,d\tau. \tag{C.6}$$

Applying the Fourier transform reveals that $I^{ii}_{\mathrm{Ma,avg}} \equiv 0\,\mathrm{A}$ if $p\bar{\omega}/(2\pi) = f_{\mathrm{E}} \neq f_{\mathrm{P}}/(2m)$ with $m = 1, 2, 3, \ldots$, so these cases have a symmetrical current stress of $I_{\mathrm{Ma,avg}} = 2/\pi\, I_{\mathrm{M0}}$.

For $f_{\mathrm{E}} = f_{\mathrm{P}}/(2m)$ with $m = 1, 2, 3, \ldots$, the average current stress is asymmetrical across phases, with numerical calculations showing a worst-case increase of 33.3 % for $m = 1$, 6.7 % for $m = 2$, and $< 3\,\%$ for $m \geq 3$.

The sum $I_{\mathrm{Ma,avg}} + I_{\mathrm{Mb,avg}} + I_{\mathrm{Mc,avg}} = 6/\pi\, I_{\mathrm{M0}}$, though, remains constant, similar to the constant total losses in the RMS analysis. There are, therefore, no further restrictions on the frequency ratio for the MPPB operation from the average current stress.

D

Performance Evaluation of a dv/dt-Limited 1200V SiC MOSFET

This Appendix summarizes the most relevant research findings concerning the employment of SiC MOSFETs in next-generation VSD inverter systems for improved efficiency and power densities without harming the motor winding insulation, also published in:

- **M. Haider**, S. Fuchs, G. Zulauf, D. Bortis, J. W. Kolar, Y. Ono, "Analytical Loss Model for Three-Phase 1200 V SiC MOSFET Inverter Drive System Utilizing Miller Capacitor-Based Active dv/dt-Limitation," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 93–104, 2022.

Motivation

In order to break the performance limit of insulated gate bipolar transistors, this Appendix evaluates the performance of silicon carbide metal oxide semiconductor field effect transistors under the side condition of a limited voltage slope to protect the motor winding insulation.

Executive Summary

Next-generation Variable Speed Drive (VSD) systems utilize Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) to achieve both high efficiency through reduced bridge-leg losses and high power density through an order-of-magnitude increase in switching frequency or reduction of the DC-link capacitance. These systems, however, must contend with the high voltage slew rate ($\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$) of these next-generation power semiconductors, especially in the context of protecting the motor from partial discharge phenomena, surge voltages from cable reflections, and unequal distribution of the voltage across motor windings. We assess the attractiveness of an external Miller capacitor across the bridge-leg power semiconductors to limit the maximum voltage slew rate in a system. To evaluate this technique, we propose a maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ model, finding that the maximum turn-on slew rate occurs at Zero-Current Switching (ZCS) with an increase in $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ as the device junction temperature increases. During the turn-off transition, the applied $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ saturates at a particular current. We then find a switching loss model, arriving at a piecewise-linear dependence of bridge-leg switching losses on current under $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$-limited conditions, a finding that runs counter to the widely-utilized quadratic current dependence.
The proposed models are validated on a SiC MOSFET bridge-leg designed for a 10 kW 800 V DC-link VSD system, where the Miller capacitor-based technique achieves lower losses for the same maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ than a gate resistor-only $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$-limiting value. This SiC MOSFET bridge-leg achieves peak calculated bridge-leg efficiencies of 99.2 % for a $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ limitation of 10 V/ns and 99.4 % for a limit of 15 V/ns.

D.1 Introduction

Variable Speed Drive (VSD) inverter systems are critical for the efficient electrification of the mobility, manufacturing, and logistics sectors, with VSD-driven industrial motors projected for over 30 % of electricity growth to 2040 [158]. More broadly, VSD-driven motors are rapidly replacing single-speed motors for higher efficiency, better control, and lower operating costs.

For the switching power semiconductor devices, state-of-the-art VSD inverters use Insulated Gate Bipolar Transistors (IGBTs), often with a blocking voltage of 1200 V, accompanied by anti-parallel freewheeling diodes. IGBTs

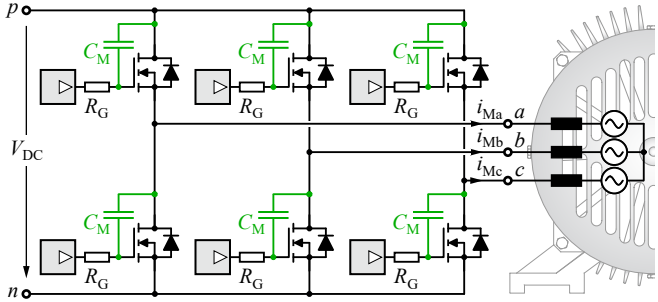

Fig. D.1: Three-phase Variable Speed Drive (VSD) PWM inverter system employing SiC MOSFETs with gate control — in this case, a gate driver with gate resistor R_G and explicit Miller feedback capacitor C_M — to limit the voltage slew rate applied to the motor terminals a, b, c and prevent partial discharge phenomena and/or progressive insulation aging.

incur high switching losses due to the bipolar on-state carriers, and these switching losses limit the switching frequency of industrial drives that utilize IGBTs to 4 kHz to 16 kHz, typically.

With the most recent commercialization and adoption of Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), these switching frequencies can be extended by nearly an order-of-magnitude, enabling full sine-wave filtering [159, 160] and higher performance on both power density and efficiency (including at partial load [161]), simultaneously. Relative to IGBTs with the same blocking voltage, SiC MOSFETs incur significantly lower switching losses due to the unipolar carrier characteristic, lower conduction losses due to fundamental material improvements [109, 162] and the lack of an on-state voltage drop in forward or reverse conduction, and support synchronous rectification. Further, the internal body diode of the MOSFETs eliminates the need for external freewheeling diodes. Overall, SiC MOSFETs support smaller overall chip areas, lower conduction and switching losses, and higher switching frequencies for smaller high-frequency motor losses and lower DC-link capacitance for given switching frequency voltage ripple.

These next-generation VSD systems (like the three-phase VSD shown in **Fig. D.1**) must contend, though, with new complications introduced by the faster switching speeds of SiC MOSFETs. High slew rate voltages, or $\mathrm{d}v/\mathrm{d}t$ values, at the output of the VSD can lead to partial discharge phenomena and progressive insulation aging of the motor [90, 119], unequal distribution of

the voltage across the motor windings, and/or surge voltages from reflections in long motor cables. VSD systems must meet critical standards that protect industrial motors from these deleterious effects [163, 164]. One method of dv/dt-limiting is to implement a full sine-wave LC-filter to limit the dv/dt applied to the motor, but this approach carries the familiar drawbacks of additional high-power passive components: volume, design and realization effort, and cost [165]. Alternatively, the voltage slope applied to the motor can be limited directly through other techniques, but with industrial IGBTs featuring switching speeds of only 1 V/ns to 5 V/ns [166] while SiC MOSFETs can achieve slew rates of up to 100 V/ns, a deeper exploration of dv/dt-limiting concepts is required.

The most straightforward approach to limit the dv/dt applied to the motor is with a dv/dt-filter, where an LC-filter with a resonant frequency above the switching frequency is implemented between the switching stage and the motor terminals (or the cable). Different passive filter implementations to limit dv/dt applied to the motor include a damped LCR-filter [167] or an undamped LC-filter with Diode-Resistor-Capacitor (DRC) damping [168], which utilizes a pair of diodes but does not require active control. Combined Differential-Mode (DM) and Common-Mode (CM) filters, further, feature capacitors connected to the DC-link rails [107, 169] and limit both bearing currents [170] and radiated electromagnetic emissions [129]. Finally, as a combination of a passive filter and an active control scheme, an undamped LC-filter can be combined with an adaptive switching cycle to enforce resonant transitions without overshoot [171, 172]. Each of these concepts reduces the filter requirements relative to a bulky full sine-wave filter, but still require the design, implementation, and realization of multiple passive components that diminish the benefits of the adoption of SiC MOSFETs in VSD systems.

Alternatively, the dv/dt applied to the motor can be limited through gate drive control of the MOSFET directly. The simplest approach is to increase the resistance of the gate resistor to increase the gate time constant [173] (including with multiple discrete gate resistance values [174]), leading to slower switching transients and higher switching losses but lower dv/dt slew rates. An improvement to this approach, as shown in **Fig. D.1**, is to implement a conventional gate driver with gate resistor and an additional Miller feedback capacitor connected between the gate and drain of each MOSFET [56, 175]. The additional Miller capacitor influences the transient of the switch-node voltage but, unlike an oversized gate resistor, does not have a meaningful effect on the gate time constant. A larger Miller capacitance prevents, *a priori*, fast voltage transients instead of filtering them out, linearizes the gate

voltage (especially valuable for Gallium Nitride (GaN) [56]), and is small in both capacitance value and size. Further, unlike alternative gate drive modifications that require additional active circuits [176, 177] or closed-loop concepts to control $\mathrm{d}v/\mathrm{d}t$ [178–180], the Miller capacitor concept is simple, compact, and straightforward to implement.

Despite the performance promised by the Miller capacitor concept for next-generation VSD systems, there is limited literature on the optimal Miller capacitor configuration for SiC MOSFETs [176], with more for GaN-based systems [56, 177, 181]. None of this prior work, however, includes *(a)* accurate modeling and analysis for SiC MOSFETs or *(b)* the effect of the Miller capacitor on overall system performance beyond $\mathrm{d}v/\mathrm{d}t$, most notably on switching losses and the shorter dead-time (and lower diode conduction losses) supported by the faster gate time constant.

Motor-integrated VSD systems support $\mathrm{d}v/\mathrm{d}t$ values as high as 10 V/ns to 15 V/ns, as no cable reflections need to be considered with direct motor integration. In [77], we analyzed a number of approaches to meet these $\mathrm{d}v/\mathrm{d}t$ requirements in an $V_{\mathrm{DC}} = 800\,\mathrm{V}$ VSD system, and found the Miller capacitor solution promised the best analytical performance. In the following, we extend this work into a complete switching loss model for SiC MOSFETs with an external Miller capacitor, first revisiting the switching behavior of a bridge-leg and experimentally validating the effect of the Miller capacitor on the switching transient (**Section D.2**). From there, we find a parametric gate drive model to enable the selection of a gate resistor and Miller capacitor combination to achieve the desired voltage slew rate during turn-on and turn-off, and propose and validate a loss model for the switching losses across these voltage slew rates that unifies turn-on and turn-off switching loss models under soft- and hard-switching conditions (**Section D.3**). In **Section D.4**, these switching losses are validated on a 10 kW VSD, where the inverter losses are derived for sinusoidal current and then verified by measurements with both an external Miller capacitor and under conventional operation, achieving a peak bridge-leg efficiency of 99.4 % at a 15 V/ns slew rate limitation. In **Section D.5**, we provide a design approach for implementing $\mathrm{d}v/\mathrm{d}t$-limited VSD systems. **Section D.6** concludes the considerations and points to further improvements for Wide-Bandgap (WBG)-enabled, motor-integrated, next-generation VSD systems.

D.2 Switching Behavior with an External Miller Capacitor

D.2.1 Switching Behavior Explanation

To understand the external Miller capacitor (C_M) approach under investigation, we first must analyze the effect of C_M on the switching transient. To investigate this switching behavior, we consider a half-bridge configuration with a high-side T_h and a low-side transistor T_l connected to a DC-link with the voltage V_{DC} and driving an ohmic-inductive load with both positive and negative load currents i_L (such that either a strictly positive or strictly negative current is seen during a switching cycle). In **Fig. D.2**, the half-bridge power semiconductors are each shown with a gate driver and an explicit Miller feedback capacitor C_M.

For a positive load (and switched) current, the load is connected to the negative DC-link rail, as shown in **Fig. D.2(a.i)**. When T_h is conducting, the load current i_L is increasing (under $v_{DS} = V_{DC}$) until the switching transition occurs, at which time T_h is turned-off and $i_L = i_{off}$ (**Fig. D.2(b.i)**). This triggers a Zero-Voltage Switching (ZVS) turn-on transition [182] for the low-side switch T_l and a ZVS turn-off transition for the high-side switch T_h, where the effective switch-node capacitance is the combination of the output capacitances of the high-side $C_{oss,Th}$ and low-side transistor $C_{oss,Tl}$ and *both* Miller capacitors C_M (as both switches are off). This switch-node capacitance defines the slope as the switch-node voltage v_{DS} discharges from V_{DC} to zero, at which point the voltage transient ends and the load current flows through the low-side diode.

After the enforced dead-time t_D, the low-side transistor is turned-on and the load current commutates from the diode to the MOSFET channel (note that the low-side transistor, under a strictly positive current condition, cannot trigger any transitions and only enables synchronous rectification). While the low-side switch is on, the current decreases ($v_{DS} = 0\,V$) until T_l is turned-off again at $i_L \approx i_{on} > 0$ and the current commutates back from the channel to the low-side diode. Again, after an enforced dead-time t_D, T_h is turned on and a hard-switching event occurs $i_L = i_{on}$. This hard-switching event discharges $C_{oss,Th}$ and the high-side C_M while charging $C_{oss,Tl}$ and the low-side C_M to bring the switch-node voltage v_{DS} from zero to V_{DC}, and this fast transient typically causes a voltage overshoot caused by an oscillation between the equivalent output capacitance and the commutation loop inductance.

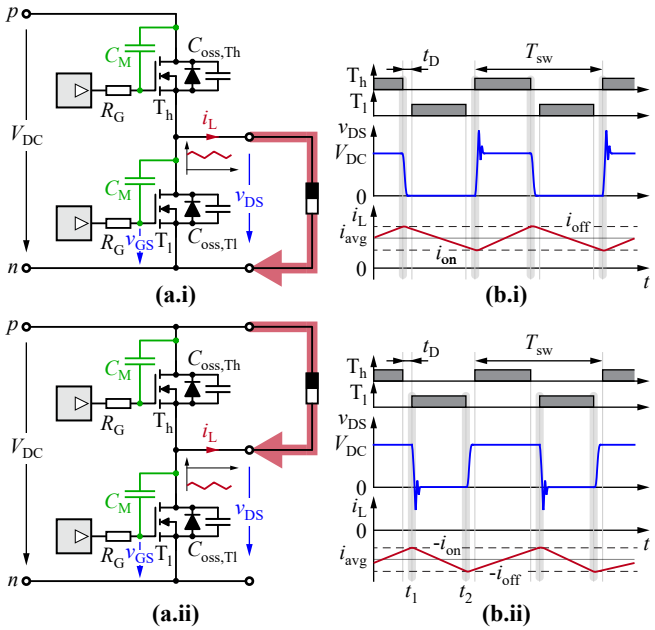

Fig. D.2: (a) Half-bridge power semiconductor bridge-leg comprising a high-side T_h and a low-side transistor T_l with individual gate drives and external Miller feedback capacitors C_M. **(b)** Characteristic bridge-leg waveforms: gate drive signals, switch-node voltage v_{DS}, and load current i_L. **(i)** Strictly positive load current i_L and **(ii)** a strictly negative load current i_L, both of which occur during a fundamental period.

Under a negative load current, where the load is equivalently connected to the positive DC-link rail (**Fig. D.2(a.ii)**), the behavior of T_h and T_l are reversed, with the high-side device transistor turned-on under ZVS and the low-side transistor hard-switched at turn-on, as shown in **Fig. D.2(b.ii)**.

D.2.2 Experimental Validation

To validate our understanding of the effect of the external Miller capacitance on the switching transition, we construct a half-bridge using two next-generation low-$R_{DS,on}$ SiC MOSFETs (*C3M0016120K* [115]) and a gate driver with an output clamp variant (for enhanced noise immunity) [120] that drives the transistors at the maximum positive ($V_{G,on} = 15\,V$) and minimum negative ($V_{G,off} = -4\,V$) gate drive voltages. The Miller capacitor is implemented with a

Mica capacitor [183], which has low dissipation factor, linear capacitance, and is rated for transients up to 20 V/ns [183]. Turn-on and turn-off behavior for the half-bridge is measured under Double-Pulse Test (DPT) conditions, and we define the rise time t_r and fall time t_f of v_{DS} as the time interval between 10 % and 90 % (or 90 % and 10 %) of the DC-link voltage V_{DC} with a resulting voltage slope $dv_{DS}/dt = 0.8V_{DC}/t_r$ or $dv_{DS}/dt = 0.8V_{DC}/t_f$ for $V_{DC} = 800$ V.

Firstly, we measure and analyze the behavior for $R_G = 0\,\Omega$ without a Miller capacitor ($C_M = 0$ pF), as reported in **Fig. D.3**. The turn-on transition occurs under Zero-Current Switching (ZCS) conditions ($I_{on} = 0$ A) and the measured slew rate is $dv_{DS}/dt = 60$ V/ns, with the turn-off transitions at $I_{off} = 5$ A and $I_{off} = 40$ A achieving voltage slew rates of 6.1 V/ns and 45 V/ns, respectively. We might expect the voltage slew rate to increase by a factor of 8 with an 8× increase in current; instead, we find an increase of 7.4 and encounter the saturation of dv_{DS}/dt under high-current switching conditions that was reported in [88]. For all of the measured turn-on and turn-off transitions in **Fig. D.3**, the drain-source voltage transitions nearly linearly between 10 % and 90 % (or 90 % and 10 %), justifying the previously-introduced derivation of voltage slope based on the rise (or fall) time. The power loop inductance can be estimated from the oscillation frequency of the commutation loop, which is measured at 71 MHz in **Fig. D.3(a.ii)** and corresponds to 20 nH, which originates primarily from the parasitic inductances of the two TO-247 packages. Even with a current slew rate of 2 A/ns, a reasonable value for the gate resistors considered here, the inductive voltage drop is only 40 V — less than 5 % of V_{DC}, and safely neglected in the subsequent analysis.

Next, the gate resistor is increased to $R_G = 30\,\Omega$ while maintaining zero Miller capacitance ($C_M = 0$ pF), which slows the turn-on voltage slew rate significantly to 8.8 V/ns. We find, perhaps unexpectedly, a negligible effect on the turn-off slew rate at 5 A (measured at 5.7 V/ns), but the high-current turn-off transient slew is reduced from 45 V/ns to 9.0 V/ns. The gate transient, as we see in **Fig. D.3(b)**, is also much slower relative to the reference case with $R_G = 0\,\Omega$.

Finally, an arbitrary Miller capacitance of $C_M = 50$ pF is added to the half-bridge, and a much lower gate resistance of $R_G = 10\,\Omega$ is selected to achieve the dv_{DS}/dt at turn-on as for the $R_G = 30\,\Omega$ case (**Fig. D.3(a.i)**). The gate transient is now faster than for the large gate resistance case (although still slower than for the $R_G = 0\,\Omega$, $C_M = 0$ pF case, as expected), and we again find little effect on the turn-off transition at 5 A (measured at 5.6 V/ns) but a large influence on the high-current transition (slew measured at 11.5 V/ns at 40 A).

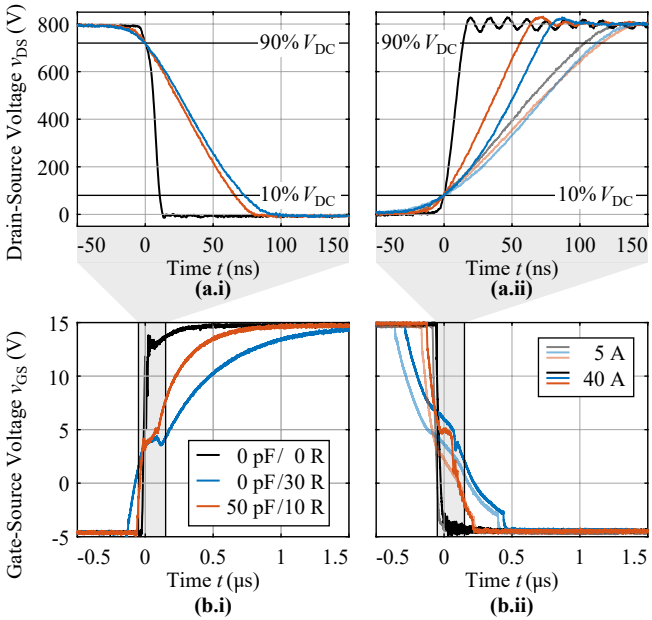

Fig. D.3: (a) Measured drain-source voltage v_{DS} and **(b)** measured gate-source voltage v_{GS} of a *C3M0016120K* low-side transistor T_1 (see **Fig. D.2(a)**), during **(i)** turn-on at zero current (t_1 in **Fig. D.2(a)**) and **(ii)** turn-off at 5 A (faded lines) and at 40 A (t_2 in **Fig. D.2(a)**) for different gate drive parameter combinations R_G and C_M. The change of the drain-source voltage is nearly linear between 10 % and 90 % (or 90 % and 10 %) of V_{DC} and is further linearized with the external Miller capacitor C_M. The turn-on voltage slew rate at zero current results with 8.8 V/ns for both gate drive parameter combinations of $R_G = 30\,\Omega$, $C_M = 0$ pF, and $R_G = 10\,\Omega$, $C_M = 50$ pF. In contrast, the turn-off voltage slew rate at $I_{off} = 40$ A differs for the two cases and results with 9.0 V/ns for $R_G = 30\,\Omega$, $C_M = 0$ pF and 11.5 V/ns for $R_G = 10\,\Omega$, $C_M = 50$ pF. The Miller plateau becomes visible at reduced voltage slopes, with non-zero values of R_G and C_M.

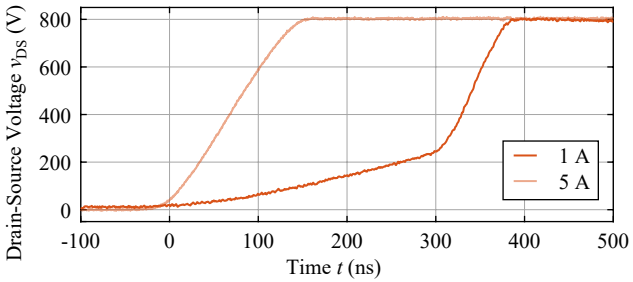

Fig. D.4: Measured drain-source voltage v_{DS} for a turn-off current of $I_{off} = 1\,A$, causing an incomplete ZVS transition, and a turn-off current of 5 A with a complete ZVS transition. Both configurations have $R_G = 10\,\Omega$ and $C_M = 50\,pF$. After the dead time $t_D = 400\,ns$ has passed, the complementary transistor turns on and enforces a rapid voltage transient similar to ZCS conditions at a reduced voltage difference. This case is inherently included in the selected half-bridge configuration and the dv_{DS}/dt limitation is still met.

At low current levels during turn-off, the rise time may become longer than the dead time t_D, which is selected to minimize the diode conduction losses. Under these conditions, a partial hard turn-on event occurs, causing an incomplete ZVS transition (see [182] for a more complete discussion). During this turn-off transition, the gate-source voltage decays to a negative voltage during the dead time, and, when the second transistor turns on after the dead time (but before the transition is complete), a ZCS-like transition occurs for the remaining voltage difference, with a fast dv_{DS}/dt transient. A measured waveform for this event is shown in **Fig. D.4** (for $R_G = 10\,\Omega$, $C_M = 50\,pF$) at a turn-off current of 1 A and a dead time of 400 ns. Because the low current (which must be the case to cause this condition) causes a slow transition during the dead-time, the slew rate limitation is still met under these conditions.

We see, then, that the Miller capacitor slows the voltage transient, as desired, and that the Miller capacitor can achieve different turn-on and turn-off voltage slew rates with the same gate resistor. For the same drain-source voltage slope, the Miller capacitance solution has a faster gate transition than a gate resistor alone, which could be beneficial. Most importantly, though, we find a significant dependence of the voltage slew rates dv_{DS}/dt on the switched current, an influence beyond the gate drive parameters R_G and C_M alone, and this warrants a deeper investigation.

D.2.3 Voltage Slew Rate Measurements over Switched Current

To understand the current dependence of the slew rate, the voltage slew rate $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ is measured across switched current with and without the Miller capacitor. We sweep the DPT measurements with switched currents from 0 A to 45 A for *both* turn-on and turn-off currents with gate resistors $R_{\mathrm{G,on}} = 30.1\,\Omega$ and $R_{\mathrm{G,off}} = 24.3\,\Omega$ and a Miller capacitance, when used, of 20 pF. The results are shown in **Fig. D.5**, alongside an image showing the relative volume contribution of the Miller capacitor, which is negligible compared to the SiC MOSFET and other gate drive components.

At turn-on, we find that $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ reduces with higher switched turn-on currents I_{on}, with the maximum slope occurring at ZCS ($\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}}$). This aligns with conventional theory with a transconductance g_{m}, where the Miller voltage increases at higher currents as $v_{\mathrm{M}} = v_{\mathrm{th}} + I_{\mathrm{on}}/g_{\mathrm{m}}$ and the slew rate goes as $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{on}} \propto V_{\mathrm{G,on}} - v_{\mathrm{M}}$. We also find a temperature dependence by applying continuous switching under ZCS (rather than the DPT) at around 100 °C junction temperature, which is indicated by the black dots in **Fig. D.5** and achieves higher a $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ than ZCS under DPT conditions (with a junction temperature near room temperature). The maximum measured voltage slope under turn-on (at the elevated junction temperature) is $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}} = 9.8\,\mathrm{V/ns}$ without the Miller capacitor and 7.4 V/ns with $C_{\mathrm{M}} = 20\,\mathrm{pF}$.

At low turn-off currents and under ZVS, the voltage slew rate $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ scales with the switched turn-off current I_{off}. At higher switched currents, though, the voltage slope $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ saturates, replicating the "kink current" I_{k} behavior found in [88]. The kink current is:

$$I_{\mathrm{k}} = C_{\mathrm{eff}} \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}}, \tag{D.1}$$

with $C_{\mathrm{eff}} = 2C_{\mathrm{dQ,oss}} + 2C_{\mathrm{M}} + C_{\mathrm{par}}$ and $C_{\mathrm{dQ,oss}}$ as the charge-equivalent capacitance [182] of the transistor between 10 % and 90 % of the DC-link voltage. Without an external Miller capacitance, and considering C_{M} and any parasitic capacitance C_{par} as negligible compared to $C_{\mathrm{dQ,oss}}$, the effective capacitance is $C_{\mathrm{eff}} \approx 2C_{\mathrm{dQ,oss}} = 666\,\mathrm{pF}$ and the kink current is $I_{\mathrm{k,A}} = 6.5\,\mathrm{A}$. With $C_{\mathrm{M}} = 20\,\mathrm{pF}$, the kink current is $I_{\mathrm{k,B}} = 4.9\,\mathrm{A}$ as a result of the reduced $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}}$, with these values labeled in **Fig. D.5** (although the kink current transition from rising slope to saturated is relatively smooth here).

In sum, then, the external Miller capacitance C_{M} maintains the behavior of the voltage slew rates across current, but reduces $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ overall and can

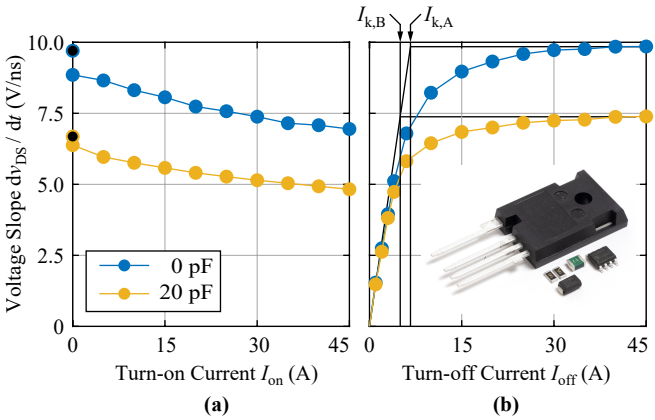

Fig. D.5: dv_{DS}/dt measurements from Double-Pulse Test (DPT) experiments on a *C3M0016120K* bridge-leg over switched current from 0 A to 45 A for **(a)** turn-on and **(b)** turn-off, with $R_{G,on} = 30.1\,\Omega$, $R_{G,off} = 24.3\,\Omega$ and two different Miller capacitors C_M. The black dots indicate continuous Zero-Current Switching (ZCS) measurements at 100 °C. In **(b)**, the size of the Miller capacitor (green) is compared to the gate drive components (gate driver, turn-on resistor, second resistor with an additional diode to achieve an independent turn-off resistance) and the SiC MOSFET to show the compactness of this solution.

be used with a gate resistor to achieve the desired voltage slope. That said, the important saturation current characteristic mandates a deeper investigation of the switching behavior during a transition, leading to an analytical model for both dv_{DS}/dt and switching losses for any gate resistance and Miller capacitor combination.

D.3 dv/dt and Loss Models

In this Section, we derive a dv_{DS}/dt model to find suitable gate drive configurations (for an arbitrary power semiconductor device) to achieve a desired dv_{DS}/dt and a related switching loss model for determining turn-on and turn-off losses. First, we return to a deeper investigation of the half-bridge during a switching transition to better understand the detailed models derived here.

D.3.1 dv/dt-Model

Fig. D.6(a) shows the equivalent half-bridge circuit present during the turn-off and turn-on transition of the low-side switch (T_l in **Fig. D.2(a)**), with the corresponding waveforms shown in **Fig. D.6(b)**. Here, we limit our focus to the switch-node voltage transient, with the broader gate and bridge-leg waveforms detailed in [174,176]. The switching current I_{sw} is assumed positive (hard-switching T_l at turn-on), constant during the switching transition, and with a magnitude greater than the kink current as $I_{sw} > I_k$. The waveforms use a straight-line approximation and C_{DS} represents the equivalent output capacitance between the drain and source, including the drain-source capacitance of T_l, the output capacitance of T_h (indicated in the figure only with a free-wheeling diode to which I_{sw} commutates) and any additional parasitic capacitances, such that $C_{DS} = C_{oss,Th} + C_{ds,Tl} + C_{par}$.

Turn-off Transition

At turn-off (**Fig. D.6(a.i)** and **Fig. D.6(b.i)**), the initial condition is with T_l turned on, such that the gate is charged to $V_{G,on}$. The gate driver applies $V_{G,off}$, and the internal gate-source voltage is reduced and clamped at the Miller voltage $v_{GS,i} = v_M = v_{th} + I_{sw}/g_m$. We assume a strict Miller plateau, such that $v_{GS,i} = v_M$ is strictly true and therefore no current flows to C_{GS}. Through KVL, we can then find $v_M - V_{G,off} = \left[R_{G,off}\,(C_M + C_{GD}) + R_{int}C_{GD}\right]\frac{dv_{DS}}{dt} + R_{G,off}R_{int}C_MC_{GD}\frac{d^2v_{DS}}{dt^2}$. Using the straight-line approximation such that $\frac{d^2v_{DS}}{dt^2} = 0$, we find our model for dv_{DS}/dt during the turn-off transition:

$$\left.\frac{dv_{DS}}{dt}\right|_{off} = \frac{v_M - V_{G,off}}{R_{G,off}C_M + R_{G,off}C_{GD} + R_{int}C_{GD} + \tau_{off}}, \tag{D.2}$$

with an additional fitting time constant τ_{off} to account for further delays, perhaps inside the semiconductor or the semiconductor package. With no external gate resistor ($R_{G,off} = 0\,\Omega$), the internal gate resistance R_{int} limits the voltage slew rate.

Turn-on Transition

At turn-on (**Fig. D.6(a.ii)** and **Fig. D.6(b.ii)**), T_l is turned off and the gate is therefore charged to $V_{G,off}$. The gate driver applies $V_{G,on}$, and we can follow the same analysis as for the turn-off model — with the important exception that $v_{GS,i} = v_{th}$ because the device is turned-on under ZCS to consider the

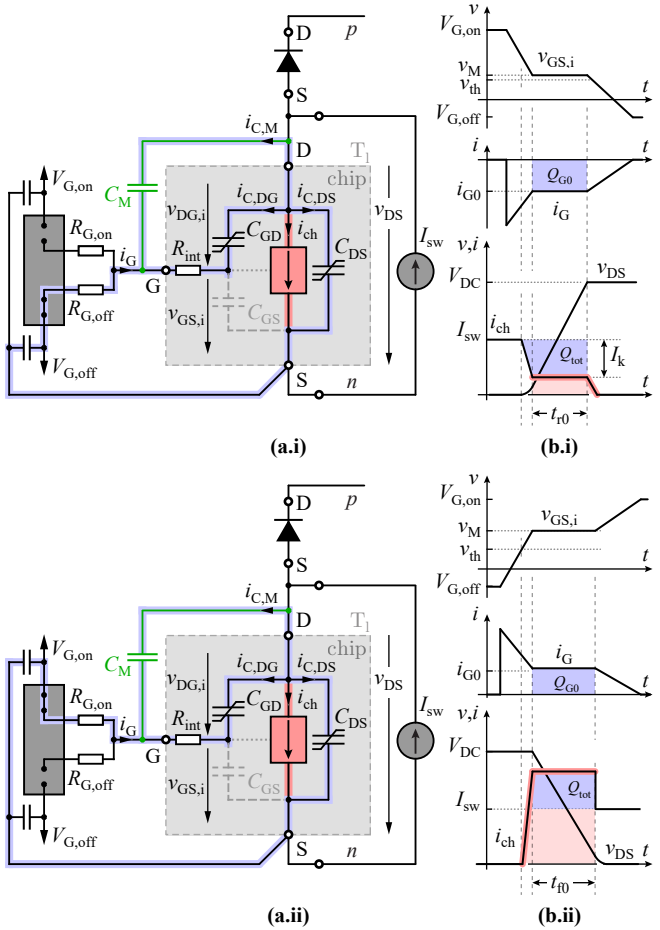

Fig. D.6: (a) Equivalent circuit of the bridge-leg of **Fig. D.2(a)** during the **(i)** turn-off and **(ii)** turn-on switching transitions of T_l for switched current greater than the kink current, or $I_{sw} > I_k$. The upper power transistor is only visualized as the body diode and the shown drain-source capacitance C_{DS} includes the parasitic capacitances $C_{ds,Tl}$, $C_{oss,Th}$, and C_{par}. **(b)** shows the corresponding time waveforms. The switched current I_{sw} is taken as constant during the turn-off transition (low ripple approximation) and the time behavior of the inner gate-source voltage ($v_{GS,i}$) of T_l is based on a straight-line approximation.

worst-case $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ (**Fig. D.6(b.ii)** shows the behavior for a current value I_{sw} different from zero). During turn-on, the voltage slew rate is:

$$\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{on}} = \frac{V_{\mathrm{G,on}} - v_{\mathrm{th}}}{R_{\mathrm{G,on}}C_{\mathrm{M}} + R_{\mathrm{G,on}}C_{\mathrm{GD}} + R_{\mathrm{int}}C_{\mathrm{GD}} + \tau_{\mathrm{on}}}. \tag{D.3}$$

C_{GD} corresponds to the charge-equivalent gate-drain capacitance. Although the local value (c_{GD}) is voltage-dependent and non-linear, the external Miller capacitor linearizes or even dominates the total gate-drain capacitance. The drain-source voltage change is therefore more linear, and we emphasize again that the Miller capacitor primarily influences the drain-source voltage transient without significant affecting the gate transient.

Experimental Validation

We validate the proposed $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ models in the same half-bridge configuration with four Miller capacitance values ($C_{\mathrm{M}} = [0, 10, 20, 50]\,\mathrm{pF}$) and several turn-on and turn-off resistors. Turn-off transitions are measured with DPT conditions at 40 A switched current and turn-on transitions are measured with continuous ZCS with a junction temperature of 100 °C.

The results are reported in **Fig. D.7**, with the modeled voltage slope shown as lines and the measured slope as dots. The turn-on model is fit to the measurements with $v_{\mathrm{th}} = 6.0\,\mathrm{V}$, $C_{\mathrm{GD}} = 24.5\,\mathrm{pF}$, $R_{\mathrm{int}} = 2.2\,\Omega$ and $\tau_{\mathrm{on}} = 143\,\mathrm{ps}$, and the turn-off model is fit with $v_{\mathrm{M}} = 8.7\,\mathrm{V}$, $C_{\mathrm{GD}} = 45.7\,\mathrm{pF}$, $R_{\mathrm{int}} = 2.5\,\Omega$ and $\tau_{\mathrm{off}} = 151\,\mathrm{ps}$. These parameters are quite similar, as desired, with the large deviation for C_{GD} assumed to originate in the different contribution of C_{GS} between turn-on and turn-off since the Miller plateau is not perfectly flat [184, 185].

The proposal models match the measurements across gate driver circuit values, supporting the selection of suitable gate resistor-Miller capacitor combinations to achieve the desired voltage slew rate in any application. In **Fig. D.7**, our targets of $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}} = 10\,\mathrm{V/ns}$ and $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}} = 15\,\mathrm{V/ns}$ are highlighted, with the Miller capacitance and gate resistor values that result in those maximum slew rates summarized in **Table D.1**.

D.3.2 dv/dt-Related Loss Model

Loss Measurements

We see in **Table D.1**, then, that different gate drive parameter combinations can achieve the same maximum voltage slew rate, but recall from **Fig. D.3**

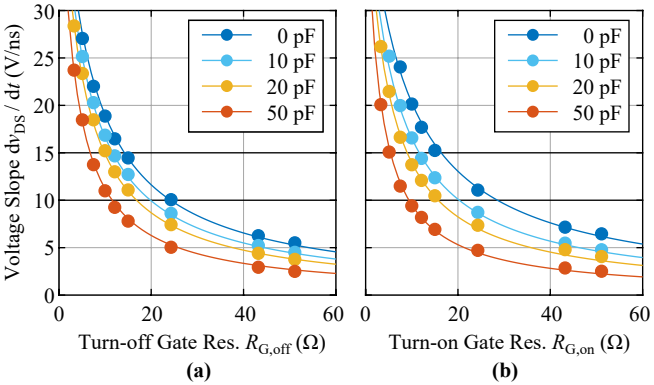

Fig. D.7: Measured voltage slope for different Miller capacitors and gate resistors for **(a)** turn-off at 40 A and **(b)** turn-on at zero current. The proposed model of **Eqn. (D.2)** and **Eqn. (D.3)** is shown overlaid as the solid lines, where we find excellent matching between the model and the measurement. Maximum considered voltage slew rates of 10 V/ns and 15 V/ns are highlighted.

Tab. D.1: Required gate resistors $R_{G,on}$ and $R_{G,off}$ for different voltage slopes and external Miller capacitor values; turn-off at 40 A, turn-on at zero current.

Gate Resistors $R_{G,on}$, $R_{G,off}$	$\left.\frac{dv_{DS}}{dt}\right\|_{max} = 10\,V/ns$	$\left.\frac{dv_{DS}}{dt}\right\|_{max} = 15\,V/ns$
$C_M = 0$ pF	30.1 Ω, 24.3 Ω	15.0 Ω, 15.0 Ω
$C_M = 20$ pF	16.2 Ω, 16.2 Ω	8.6 Ω, 10.0 Ω
$C_M = 50$ pF	9.5 Ω, 11.0 Ω	5.2 Ω, 6.8 Ω

that the time-domain behavior can be quite distinct among them. Here, we explore if this degree of freedom can be used to minimize switching losses, and derive a suitable — and novel, for turn-on losses — model for switching losses.

We use the thermal transient measurement method [108] to conduct ZCS-only, turn-off-only, and turn-on and turn-off loss measurements for all six sets of gate drive parameters that achieve our maximum voltage slew rates in **Table D.1**. These results are given in **Fig. D.8** across turn-on and turn-off currents, where we report the loss measurements alongside the measured $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ for a single transition (**Fig. D.8(a)**) under continuous half-bridge operation (**Fig. D.8(b)** and **Fig. D.8(c)**). We see, upon a quick examination, that the losses depend, to first order, upon $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ but that the tradeoff between gate resistor and Miller capacitor value has almost no influence, and we move to find a suitable loss model that explains this behavior.

Turn-off Loss Model

A detailed turn-off loss model is given in [88], and only a short summary is given here.

For currents below the kink current, only the resonant charging-discharging C_{oss}-losses [186] occur during turn-off, denoted as E_0. Above the kink current, the voltage slew rate $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ saturates and a portion of the load current flows through the channel, resulting in losses of $E_0 + k_{\mathrm{off}}\,(I_{\mathrm{off}} - I_{\mathrm{k}})$, with $k_{\mathrm{off}} = \frac{1}{2} V_{\mathrm{DC}}^2 / \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}}$. Turn-off switching losses are, then:

$$\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{off}} = \begin{cases} \frac{I_{\mathrm{off}}}{I_{\mathrm{k}}} \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}} & \text{if} \quad I_{\mathrm{off}} < I_{\mathrm{k}} \\ \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}} & \text{if} \quad I_{\mathrm{off}} \geq I_{\mathrm{k}} \end{cases} \tag{D.4}$$

$$E_{\mathrm{sw,off}}(I_{\mathrm{off}}) = \begin{cases} E_0 & \text{if} \quad I_{\mathrm{off}} < I_{\mathrm{k}} \\ E_0 + k_{\mathrm{off}}\,(I_{\mathrm{off}} - I_{\mathrm{k}}) & \text{if} \quad I_{\mathrm{off}} \geq I_{\mathrm{k}} \end{cases} \tag{D.5}$$

with $I_{\mathrm{off}} > 0\,\mathrm{A}$. Note that the gate current flows as $i_{\mathrm{G}} = -i_{\mathrm{C,M}} - i_{\mathrm{C,DG}}$ (with the gate charge related to the Miller plateau $Q_{\mathrm{G0}} = i_{\mathrm{G0}} t_{\mathrm{r0}}$), which corresponds to the charge requirements of C_{M} and C_{GD} and must be absorbed by the gate driver itself. For our application here, we apply **Eqn. (D.1)** and find $I_{\mathrm{k10}} = 6.6\,\mathrm{A}$ for $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}} = 10\,\mathrm{V/ns}$ and $I_{\mathrm{k15}} = 10\,\mathrm{A}$ for $15\,\mathrm{V/ns}$.

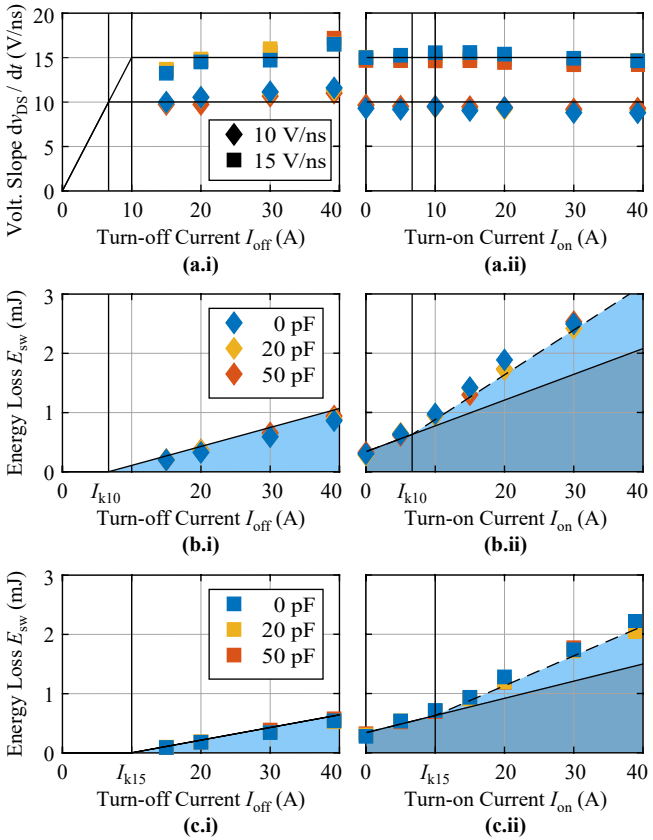

Fig. D.8: **(a)** Measured voltage slopes dv_{DS}/dt and switching losses for **(b)** $dv_{DS}/dt|_{max} = 10\,V/ns$ and **(c)** $dv_{DS}/dt|_{max} = 15\,V/ns$ at **(i)** turn-off and **(ii)** turn-on, verifying the proposed models. Diamonds indicate a maximum slope of $dv_{DS}/dt|_{max}$ of 10 V/ns (♦) and squares indicate a maximum slope of 15 V/ns (■). In **(b.i)** and **(c.i)**, turn-off losses (light blue) are directly measured and, subsequently, turn-on losses (dark blue) are extracted from a total loss measurement of **(b.ii)** and **(c.ii)** with the turn-off losses known (shown in light blue).

Turn-on Loss Model

During the turn-on transition, the charge corresponding to the total capacitance $Q_{\text{tot}} = Q_{\text{oss}}(V_{\text{DC}}) + \left(C_{\text{M}} + C_{\text{par}}/2\right) V_{\text{DC}}$ is charged/discharged via the channel, resulting in ZCS losses of $V_{\text{DC}} Q_{\text{tot}}$. If $\mathrm{d}v_{\text{DS}}/\mathrm{d}t$ is assumed as independent of load-current, a reasonable approximation from our findings in **Section D.2** (see **Fig. D.5**), then the current-dependent losses increase linearly with the current as $k_{\text{on}} I_{\text{on}}$ and can be considered the losses associated with $\mathrm{d}v_{\text{DS}}/\mathrm{d}t$-overlap. The turn-on losses, then, can be described as:

$$\left.\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t}\right|_{\text{on}} = \left.\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t}\right|_{\text{max}} \tag{D.6}$$

$$E_{\text{sw,on}}(I_{\text{on}}) = V_{\text{DC}} Q_{\text{tot}} + k_{\text{on}} I_{\text{on}}. \tag{D.7}$$

For turn-on losses, our model utilizes the values $Q_{\text{oss}}(V_{\text{DC}}) = 344\,\text{nC}$, $C_{\text{par}} = 100\,\text{pF}$ (PCB), and a neglected charge contribution from the Miller capacitor for $Q_{\text{tot}} = 384\,\text{nC}$. We fit $k_{\text{on}} = \frac{1.35}{2} V_{\text{DC}}^2 / \left.\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t}\right|_{\text{max}}$, with the factor of 1.35 interpreted as a waveform correction factor for the turn-on losses.

Unified Loss Model

Finally, we can unify the turn-off (cf. **Eqn. (D.5)**) and turn-on loss models (cf. **Eqn. (D.7)**), finding a linear piecewise function for half-bridge losses that is distinct, and novel, from the typical assumption of a quadratic loss model that is dependent on current.

With a simple summation, and neglecting the resonant charging-discharging C_{oss}-losses occurring during turn-off, denoted as E_0, which are always a small fraction of $V_{\text{DC}} Q_{\text{tot}}$ [186], the half-bridge switching losses $E_{\text{sw}}(I_{\text{sw}}) = E_{\text{sw,on}}(I_{\text{sw}}) + E_{\text{sw,off}}(I_{\text{sw}})$ at a low current ripple (i.e. $I_{\text{sw}} \approx I_{\text{on}} \approx I_{\text{off}}$) result in a piecewise linear function:

$$E_{\text{sw}}(I_{\text{sw}}) = \begin{cases} V_{\text{DC}} Q_{\text{tot}} + k_{\text{on}} I_{\text{sw}} & \text{if} \quad I_{\text{sw}} < I_{\text{k}} \\ V_{\text{DC}} Q_{\text{tot}} + k_{\text{on}} I_{\text{sw}} + k_{\text{off}} \left(I_{\text{sw}} - I_{\text{k}}\right) & \text{if} \quad I_{\text{sw}} \geq I_{\text{k}}. \end{cases} \tag{D.8}$$

These linear functions intersect at the value of the kink current I_{k}, which is dependent — along with k_{on} and k_{off} — on the selected maximum voltage slew rate $\mathrm{d}v_{\text{DS}}\mathrm{d}t|_{\text{max}}$. Critically, half-bridge switching losses are actually *piecewise-linear* on I_{sw}, rather than quadratic [108], with the kink current I_{k} playing a critical role as the intersection of these functions and the switched

Tab. D.2: Derived loss parameters for different voltage slope limitations.

Parameter	$\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right\|_{\max} = 10\,\mathrm{V/ns}$	$\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right\|_{\max} = 15\,\mathrm{V/ns}$
Q_{tot} (nC)	384	384
I_{k} (A)	6.6	10
k_{on} (µJ/A)	43	29
k_{off} (µJ/A)	32	21

current value after which switching losses start increasing more rapidly. This arises because of the lack of dependence — in either turn-on or turn-off losses — on $\mathrm{d}i/\mathrm{d}t$, as mentioned previously [174, 176].

The proposed model is validated in **Fig. D.8(b)** and **Fig. D.8(c)**, with the turn-off losses measured directly and with tight matching (cf. **Fig. D.8(i)**). Turn-on losses cannot be measured directly easily, so we instead measure half-bridge losses with a small current ripple, which are comprised of one turn-on and one turn-off transition, and report the total measured losses (cf. **Fig. D.8(ii)**). The obtained parameters for the switching loss model are reported in **Table D.2**.

D.4 Case Study: 10kW Motor Drive System

The derived $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ and loss models are validated by measuring the losses (thermally [108]) of a single *C3M0016120K* bridge-leg of a VSD system for an electric motor, as shown in **Fig. D.1**. The specifications for this motor drive are $V_{\mathrm{DC}} = 800\,\mathrm{V}$, $P_{\mathrm{M}} = 10\,\mathrm{kW}$, $\hat{i}_{\mathrm{M,N}} = 25\,\mathrm{A_{pk}}$, $\hat{i}_{\mathrm{M,opt}} = 20\,\mathrm{A_{pk}}$, $M = 0.8$, $M\cos\varphi = 0.68$ [77] with a inverter switching frequency $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$ to remain outside the audible range [117].

With large motor inductances, the output phase current is sinusoidal under Continuous Current Mode (CCM) with a low ripple. For a sinusoidal phase current $i_{\mathrm{Ma}} = \hat{i}_{\mathrm{M}}\sin(\varepsilon)$, the output power is $P_{\mathrm{INV}} = \frac{3}{4}\hat{i}_{\mathrm{M}}V_{\mathrm{DC}}M\cos\varphi$. The half-bridge losses will include both conduction and switching losses as $P_{\mathrm{VHB}} = P_{\mathrm{VHBcond}} + P_{\mathrm{VHBsw}}$, with conduction losses as $P_{\mathrm{VHBcond}} = \frac{1}{2}R_{\mathrm{DS,on}}\hat{i}_{\mathrm{M}}^2$ (with current ripple neglected) and the switching losses $P_{\mathrm{VHBsw}} = f_{\mathrm{sw}}\frac{1}{2\pi}\int_0^{2\pi} E_{\mathrm{sw}}(i_{\mathrm{Ma}}(\varepsilon))\mathrm{d}\varepsilon$. Using the derived loss model of

Eqn. (D.8) for the switching losses, the total half-bridge losses are:

$$P_{\text{VHB}} = \frac{1}{2} R_{\text{DS,on}} \tilde{i}_{\text{M}}^2 + f_{\text{sw}} \left(V_{\text{DC}} Q_{\text{tot}} + \frac{2}{\pi} k_{\text{on}} \hat{i}_{\text{M}} \right) + \begin{cases} 0 & \text{if} \quad \hat{i}_{\text{M}} < I_{\text{k}} \\ f_{\text{sw}} \frac{2}{\pi} k_{\text{off}} \left[\hat{i}_{\text{M}} \sqrt{1 - \left(\frac{I_{\text{k}}}{\hat{i}_{\text{M}}} \right)^2} - I_{\text{k}} \arccos \left(\frac{I_{\text{k}}}{\hat{i}_{\text{M}}} \right) \right] & \text{if} \quad \hat{i}_{\text{M}} \geq I_{\text{k}} \end{cases} \tag{D.9}$$

and the inverter efficiency is:

$$\eta = \frac{P_{\text{INV}}}{P_{\text{INV}} + 3P_{\text{VHB}}} \approx 1 - \frac{P_{\text{VHB}} \left(\hat{i}_{\text{M}} \right)}{\frac{1}{4} \hat{i}_{\text{M}} V_{\text{DC}} M \cos \varphi}. \tag{D.10}$$

The power semiconductor losses and bridge-leg efficiency are measured with the gate driver circuit parameters of **Table D.2** under the maximum voltage slew rates of 10 V/ns and 15 V/ns, with the results shown in **Fig. D.9**. The modeled conduction losses use an on-resistance value of $R_{\text{DS,on}} = 20\,\text{m}\Omega$, which corresponds to a junction temperature of 100 °C. The die area of the selected *C3M0016120K* SiC MOSFETs is optimal for a phase current of 20 A_{pk} [77], which we denote as $\hat{i}_{\text{M,opt}}$.

The loss measurements match well with the total loss predicted by the proposed loss model across maximum slew rate $\mathrm{d}v_{\text{DS}}/\mathrm{d}t|_{\text{max}}$ limits, phase current, and combinations of gate resistance and Miller capacitance. With the 10 V/ns maximum slew rate constraint, the measured bridge-leg losses are $P_{\text{VHB}} = 22.3\,\text{W}$ for $\hat{i}_{\text{M,opt}} = 20\,A_{\text{pk}}$ without the Miller capacitor and improve to 20.9 W with $C_{\text{M}} = 50\,\text{pF}$. Similarly, with the same 10 V/ns maximum slew rate but at $\hat{i}_{\text{M,N}}$, the measured bridge-leg losses are $P_{\text{VHB}} = 29.9\,\text{W}$ without the Miller capacitor and improve to 27.3 W with $C_{\text{M}} = 50\,\text{pF}$. With a higher slew rate limitation of 15 V/ns, the measured bridge-leg losses are reduced relative to the 10 V/ns case, as expected, from 17.2 W ($C_{\text{M}} = 0\,\text{pF}$) to 16.3 W ($C_{\text{M}} = 50\,\text{pF}$) at $\hat{i}_{\text{M,opt}}$ and from 22.3 W ($C_{\text{M}} = 0\,\text{pF}$) to 20.9 W ($C_{\text{M}} = 50\,\text{pF}$) at $\hat{i}_{\text{M,N}}$. For the slew rate limit of 10 V/ns, the maximum calculated bridge-leg efficiency reaches 99.2 % at 17.0 A and for the maximum slew rate of 15 V/ns, the maximum calculated bridge-leg efficiency reaches 99.4 % at 18.1 A. Without the slew rate limitation (0 Ω gate resistance, which reaches a slew rate of 60 V/ns, as reported in **Section D.2**), the peak bridge-leg efficiency is 99.6 % (calculated based on [77]), as shown with the dotted line in each plot in **Fig. D.9**.

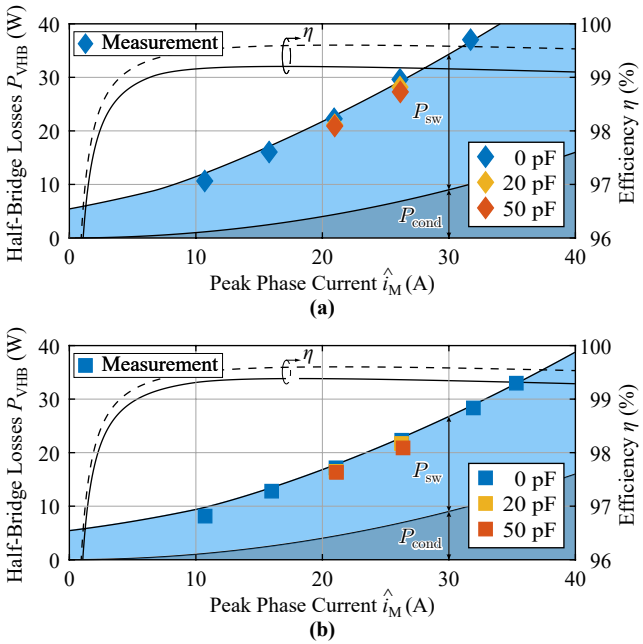

Fig. D.9: Measured semiconductor bridge-leg losses and the corresponding calculated bridge-leg efficiency over peak phase current $\hat{i}$ for **(a)** $\mathrm{d}v_{DS}/\mathrm{d}t|_{max} = 10\,\mathrm{V/ns}$ (♦) and **(b)** $\mathrm{d}v_{DS}/\mathrm{d}t|_{max} = 15\,\mathrm{V/ns}$ (■). Measurements are conducted across several load currents and gate drive circuit parameters (gate resistor and Miller capacitor values according to **Table D.1**) to validate the proposed model. The efficiency without a $\mathrm{d}v_{DS}/\mathrm{d}t$-limitation is calculated based on [77] and shown for comparison as the dashed line.

The combination of SiC MOSFETs and a slew rate limit enforced with an external Miller capacitance, then, enables high-performance VSD systems — without the significant size, weight, or cost associated with bulky filters — that dramatically exceed the IGBT bridge-leg efficiency limit of ≈ 98 % [77] while protecting motors from high voltage slew rates.

To evaluate the performance of the proposed Miller-capacitor-based approach, we compare the system volume and losses with a conventional $\mathrm{d}v/\mathrm{d}t$-LC-filter-based approach [168] to meet the same slew rate limitation. We derive a simple volume model and use the filter loss model from [77] for the comparison. The volume of the power stage is primarily driven by the volume of the heatsink. We assume a maximum heatsink temperature of $\vartheta_{\mathrm{HS}} = 85\,^{\circ}\mathrm{C}$ and an ambient temperature of $\vartheta_{\mathrm{AMB}} = 45\,^{\circ}\mathrm{C}$, and use the Cooling System Performance Index (CSPI) approach [187] with a typical CSPI of 20 W/KL to calculate the heatsink volume $\mathrm{Vol}_{\mathrm{HS}}$. The design equations for the heatsink volume are:

$$R_{\mathrm{HS}} = \frac{\vartheta_{\mathrm{HS}} - \vartheta_{\mathrm{amb}}}{3P_{\mathrm{VHB}}(\hat{i}_{\mathrm{M,N}})} \tag{D.11}$$

$$\mathrm{Vol}_{\mathrm{HS}} = \frac{1}{\mathrm{CSPI}\, R_{\mathrm{HS}}}. \tag{D.12}$$

For a three-phase inverter at nominal operation ($\hat{i}_{\mathrm{M,N}} = 25\,\mathrm{A_{pk}}$) and a slew rate limit of 15 V/ns ensured by the discussed gate drive modifications, the inverter heatsink volume is $\mathrm{Vol}_{\mathrm{HS}} = 81\,\mathrm{cm}^3$ (for maximum semiconductor losses of 64.6 W at $\hat{i}_{\mathrm{M,N}} = 25\,\mathrm{A_{pk}}$) with total losses of 50.5 W at $\hat{i}_{\mathrm{M,opt}} = 20\,\mathrm{A_{pk}}$. Without the slew rate limitation (0 Ω gate resistance, which reaches a slew rate of 60 V/ns, as reported in **Section D.2**), the peak bridge-leg efficiency is 99.6 % at 21.3 $\mathrm{A_{pk}}$ and the *power stage* heatsink volume is reduced by almost 40 % to 51 cm^3 (for maximum semiconductor losses of only 41 W at $\hat{i}_{\mathrm{M,N}} = 25\,\mathrm{A_{pk}}$).

Without the bridge-leg slew rate limitation, the $\mathrm{d}v/\mathrm{d}t$-LC-filter is now required to protect the motor winding system. We use, as a reference, an LC-filter with DRC damping branches (connected between the filter output and the positive and negative DC bus, [168]) this is designed for the same application scenario with 15 V/ns. If we consider the Permanent Magnet Synchronous Motor (PMSM) 1FT7084 from Siemens [113], the $\mathrm{d}v/\mathrm{d}t$-filter capacitor of a phase needs to be at least $C_{\mathrm{o}} = 1.5\,\mathrm{nF}$ [77], which can be implemented with a Mica capacitor [183] for a volume of only 0.1 cm^3 per phase. While this small capacitor volume can be easily neglected, the filter capacitors introduce additional capacitive switching losses, resulting in additional losses

of $P_{VC} = 3 f_{sw} C_o V_{DC}^2 = 46\,\text{W}$ that are dissipated in the damping resistors. An additional heatsink for these resistors (which we allow to reach $\vartheta_{HS,R} = 125\,°\text{C}$, as power resistors can be operated at high temperatures) requires a volume of $\text{Vol}_{HS,R} = 28.8\,\text{cm}^3$. According to [77], in each phase a filter inductor with $L_o = 1.2\,\mu\text{H}$ is required which causes a current swing of 28 A, thus the inductor must be designed to saturate above 58 A. This filter inductor can be implemented with the HCI Inductor from Würth Elektronik [188] for only $3\,\text{cm}^3$ of additional volume per phase.

Then, a $\text{d}v/\text{d}t$-limiting passive LC-filter with DRC damping (in each phase) achieves a system volume of $89.4\,\text{cm}^3$ and system losses at $\hat{i}_{M,opt}$ of 79 W, for an overall system volume increase of 10 % and an overall system loss increase at $\hat{i}_{M,opt}$ of 56 % compared to the Miller capacitor approach (efficiency reduction from 99.4 % to 99 %). Further, the relatively large filter inductors may prevent automated assembly of the power stage and the filter approach is sensitive to the selected motor since the filter capacitor C_o must dominate the motor capacitance [77]. The proposed Miller capacitor approach is, in contrast, not sensitive to the motor characteristics, as any additional parasitic capacitance only increases C_{eff} and the kink current I_k but does not influence the $\text{d}v/\text{d}t$ limit, which depends only on the gate drive configuration (cf. **Eqn. (D.2)** and **Eqn. (D.3)**). This increase in kink current reduces the turn-off losses, while the increased ZCS losses only occur inside the motor.

In sum, then, the combination of SiC MOSFETs and a slew rate limit enforced with an external Miller capacitance uniquely enables high-performance VSD systems — without the significant size, weight, or cost associated with bulky filters — that clearly exceed the IGBT bridge-leg efficiency limit of ≈ 98 % [77] while protecting motors from high voltage slew rates.

D.5 Design Procedure for Voltage-Slew-Rate-Limited Bridge Legs

With a voltage slew rate limitation on the bridge-leg itself attractive in many VSD systems, we provide a design procedure to implement the $\text{d}v_{DS}/\text{d}t$-limitations explored in this work. The goal of this Section is to summarize the critical design steps for a tangible and straightforward guide to apply active $\text{d}v_{DS}/\text{d}t$ limits in motor drives with a sinusoidal phase current with peak value $\hat{i}_M$.

[S1] The specification of the application must be defined, including the maximum slew rate $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\max}$ and DC-link voltage requirements.

[S2] Select the transistor technology based on the blocking voltage (the DC-link voltage, with margin) and other considerations, including cost and preferred manufacturers.

- For this transistor family, devices with a range of on-resistances are typical available.
- The loss minimum chip area — based on the on-resistance $R_{\mathrm{DS,on}}$ at the desired junction operating temperature $\vartheta_{\mathrm{J,op}}$, and the output charge $Q_{\mathrm{oss}}(V_{\mathrm{DC}}) = \int_0^{V_{\mathrm{DC}}} c_{\mathrm{oss}}(v)\mathrm{d}v$ (all of which can be determined from the datasheet) — is [77]:

$$R_{\mathrm{DS,on,opt}} = R_{\mathrm{DS,on}} \frac{1}{\hat{i}_{\mathrm{M}}} \sqrt{\frac{2V_{\mathrm{DC}}Q_{\mathrm{oss}}f_{\mathrm{sw}}}{R_{\mathrm{DS,on}}}} \tag{D.13}$$

[S3] With the power transistor now selected, we move to the configuration of a gate drive, where we have to distinguish two cases:

(a) For the known half-bridge configuration of **Section D.2**, with existing data from this work for the *C3M001612oK* [115]) and a gate driver with an output clamp variant, the designer may straightforwardly select:

- $C_{\mathrm{M}} = 50\,\mathrm{pF}$ should be selected for maximum performance, as it achieves minimal losses without causing instability through excessive gate ringing.
- A minimum effort implementation with no Miller capacitor ($C_{\mathrm{M}} = 0\,\mathrm{pF}$) and elevated gate resistors incurs a switching loss increase of 6 % to 8 %.
- The corresponding on and off resistances for the given $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\max}$-limit can be selected according to **Fig. D.7**.

(b) If, alternatively, the half-bridge power semiconductors and/or gate drivers have not been characterized:

- An evaluation bridge-leg must be constructed to conduct simple voltage slope measurements, as described in **Section D.2**.
- Testing should begin with $C_{\mathrm{M}} = 0\,\mathrm{pF}$, and the turn-on resistance should be gradually increased (with $R_{\mathrm{G,off}} = 0\,\Omega$)

until the voltage slope limit is reached under continuous ZCS conditions, with the switching frequency selected to achieve a junction temperature close to the maximum operating temperature $\vartheta_{\mathrm{J,op}}$ in the application.
- After this sweep is completed, $R_{\mathrm{G,on}}$ should be fixed and $R_{\mathrm{G,off}}$ can be selected such that the same voltage slope limit is achieved during turn-off at the maximum phase current and under DPT conditions (room temperature device).
- To further increase the performance, the prior two steps can be repeated for different Miller capacitor values, stopping before a maximum value where additional ringing occurs in the gate-source voltage during transients.

[S4] With the Miller capacitance selected, the effective capacitance is $C_{\mathrm{eff}} = 2C_{\mathrm{dQ,oss}} + 2C_{\mathrm{M}} + C_{\mathrm{par}}$, where $C_{\mathrm{dQ,oss}} = \int_{0.1V_{\mathrm{DC}}}^{0.9V_{\mathrm{DC}}} c_{\mathrm{oss}}(v)\mathrm{d}v$ is the charge-equivalent capacitance of the transistor between 10 % and 90 % of the DC-link voltage and C_{par} includes the parasitic capacitance of the PCB and the load.

[S5] Between C_{eff} and the slew rate limit $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|_{\mathrm{max}}$, the kink current I_{k} is fully-known from **Eqn. (D.1)**:

$$I_{\mathrm{k}} = C_{\mathrm{eff}} \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}},$$

and the loss coefficients are:

$$Q_{\mathrm{tot}} = Q_{\mathrm{oss}}(V_{\mathrm{DC}}) + \left(C_{\mathrm{M}} + C_{\mathrm{par}}/2\right) V_{\mathrm{DC}}$$
$$k_{\mathrm{on}} = \frac{1.35}{2} V_{\mathrm{DC}}^2 \Big/ \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}} \qquad k_{\mathrm{off}} = \frac{1}{2} V_{\mathrm{DC}}^2 \Big/ \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{max}}.$$

[S6] The half-bridge losses are, from **Eqn. (D.9)**:

$$P_{\mathrm{VHB}} = \frac{1}{2} R_{\mathrm{DS,on}} \hat{i}_{\mathrm{M}}^2 + f_{\mathrm{sw}} \left(V_{\mathrm{DC}} Q_{\mathrm{tot}} + \frac{2}{\pi} k_{\mathrm{on}} \hat{i}_{\mathrm{M}} \right) + \begin{cases} 0 & \text{if} \quad \hat{i}_{\mathrm{M}} < I_{\mathrm{k}} \\ f_{\mathrm{sw}} \frac{2}{\pi} k_{\mathrm{off}} \left[\hat{i}_{\mathrm{M}} \sqrt{1 - \left(\frac{I_{\mathrm{k}}}{\hat{i}_{\mathrm{M}}}\right)^2} - I_{\mathrm{k}} \arccos\left(\frac{I_{\mathrm{k}}}{\hat{i}_{\mathrm{M}}}\right) \right] & \text{if} \quad \hat{i}_{\mathrm{M}} \geq I_{\mathrm{k}} \end{cases}$$

[S7] An appropriate heatsink can now be designed, and the system can be implemented and validated.

D.6 Summary

Variable Speed Drive (VSD) systems utilizing next-generation Wide-Bandgap (WBG) power semiconductors hold the promise of boosting the efficiency, power density, and adoption of electric motors to electrify manufacturing, logistics, and mobility. To realize fully the loss reduction and frequency increase benefits of SiC MOSFETs, however, the voltage slew rate applied to the motor must be limited to values such that the motor will not be damaged by partial discharge phenomena, surge voltages from cable reflections, or unequal distribution of the voltage across motor windings.

In this work, we evaluate the potential of an external Miller capacitor to limit the maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ of a bridge-leg, and derive a detailed understanding of the switching behavior to derive analytical models — across switched current, gate resistance, and Miller capacitance — for the maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ and switching losses during the turn-on and turn-off transitions. The $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ model and matching measurements show that the maximum slew rate occurs, for turn-on, at Zero-Current Switching (ZCS) and at elevated temperatures, while the turn-off $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ saturates after an analytical "kink current" is passed. The kink current derivation, which can be understood in the context of the current paths during switching, helps us arrive at a critical finding for the broader field: that switching losses in a bridge-leg are not quadratic with current (at least under limited $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ conditions), as long modelled, but are rather piecewise linear on current, with the second linear function starting at the kink current itself.

The $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ and loss models are validated on a SiC MOSFET bridge-leg for a 10 kW 800 V DC-link VSD system with $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ limitations of 10 V/ns and 15 V/ns, where we find excellent matching between the model and the measured bridge-leg losses. The Miller capacitor-based technique achieves lower losses for the same maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ than a gate resistor-only technique, highlighting the promise of realizing VSD systems with SiC MOSFETs that simultaneously achieve high efficiency, high power density, and limited voltage slew rates.

Bibliography

[1] "Transportation, Economy and Society," http://transportgeography.org.

[2] "The Effects of Transport on the Economy, Society and Built Environment Mobility," http://verkehrsforschung.dlr.de.

[3] "Effects of Transportation on the Economy," http://www.nationalgeographic.org.

[4] "Transport, Energy and Environment," http://transportgeography.org.

[5] "How are Emissions of Greenhouse Gases by the EU Evolving?" http://ec.europa.eu.

[6] "Inventory of U.S. Greenhouse Gas Emissions and Sinks," http://www.epa.gov.

[7] "United Nations," http://www.un.org.

[8] "Worldwide Transport Activity to Double, Emissions to Rise Further," http://www.itf-oecd.org.

[9] *Global Warming of* 1.5 °C, International Panel on Climate Change (IPCC), 2018.

[10] *The Future of Rail*, International Energy Agency, 2019.

[11] "Sustainability," http://uic.org.

[12] *Renewables 2017: Analysis and Forecasts to 2022*, International Energy Agency, 2017.

[13] *Photovoltaics Report*, Fraunhofer ISE, 2021.

[14] "European Trains Go Down Renewable Route," http://ourworld.unu.edu/.

[15] "The Paris Agreement," http://unfccc.int/.

[16] "Energy Efficiency and CO_2 Emissions," http://uic.org.

[17] "Air Quality," http://uic.org.

[18] "Circular Economy," http://uic.org.

[19] "Noise and Vibration," http://uic.org.

[20] "Sustainable Land Use," http://uic.org.

[21] *Fostering Railway Sector through European Green Deal*, European Union (EU) - Agency for Railways, 2020.

[22] *Rail Environment Policy Statement - On Track for a Cleaner, Greener Railway*, United Kingdom (UK) - Departement for Transport, 2021.

[23] *Technologies and Potential Developments for Energy Efficiency and CO2 Reductions in Rail Systems*, International Union of Railways (UIC), 2016.

[24] "Regenerative Braking in Trains," http://www.ctc-n.org/.

[25] "Auxiliary Power Systems for Rolling Stock Market to Benefit From Growth in Railway Electrification Through 2022," http://www.businesswire.com.

[26] I. Fisher and G. Bolton, "Auxiliary Power Systems for Rolling Stock," in *Proc. of the Institution of Engineering and Technology Professional Development Course on Electric Traction System*, Manchester, UK, Nov. 2006, pp. 167–174.

[27] *Railway Applications – Electromagnetic Compatibility – Part 3-2*, International Electrotechnical Commission Std. IEC 62 236-3-2, 2008.

[28] "Auxiliary Power Supply System," http://www.toshiba.co.jp.

[29] "Auxiliary Converters: State-of-the-Art Technology, Reliability and Efficiency for All Rolling Stock," http://www.alstom.com.

[30] "Variable Speed Compressors for Improved Energy Efficiency," http://www.compair.com.

[31] "Variable Speed Drives," http://www.novometgroup.com/.

[32] "Variable Frequency Drives," http://airprofan.com.

[33] "Train Equipment: The Compressor," http://www.railway-technical.com.

[34] "Railway Technology," http://duerr-technik.eu/.

[35] *Braking Systems*, Japan Railway and Transport Review, 1999.

[36] "MoComp Auxiliary Converters," http://www.mobility.siemens.com.

[37] "Brake System," http://www.yujinltd.co.kr/.

[38] V. Petrenko, "Railway Rolling Stock Compressors Capacity and Main Reservoirs Volume Calculation Methods," *Procedia Engineering*, vol. 187, pp. 672–679, 2017, DOI: doi.org/10.1016/j.proeng.2017.04.430.

[39] "Air Compressor for Original Equipment Manufacturers (OEM) - Oil Free," Datasheet, SRL-7.5CB, Hitachi.

[40] B. Blunier, M. Pucci, G. Cirrincione, M. Cirrincione, and A. Miraoui, "A Scroll Compressor with a High-Performance Sensorless Induction Motor Drive for the Air Management of a PEMFC System for Automotive Applications," *IEEE Transactions on Vehicular Technology*, vol. 57, no. 6, pp. 3413–3427, March 2008, DOI: 10.1109/TVT.2008.919618.

[41] I. Çadirci, S. Varma, M. Ermis, and T. Gülsoy, "A 20 kW, 20 kHz Unity Power Factor Boost Converter for Three-Phase Motor Drive Applications from an Unregulated Single-Phase Supply," *IEEE Transactions on Energy Conversion*, vol. 14, no. 3, pp. 471–478, Sept. 1999, DOI: 10.1109/60.790899.

[42] R. Saidur, S. Mekhilef, M. Ali, A. Safari, and H. Mohammed, "Applications of Variable Speed Drive (VSD) in Electrical Motors Energy Savings," *Renewable and Sustainable Energy Reviews*, vol. 218, pp. 543–550, May 2012, DOI: doi.org/10.1016/j.rser.2011.08.020.

[43] Y. Kanemoto, Z. Ren, M. Hase, H. Tanaka, A. Iyozumi, T. Tsuchiya, K. Chiba, and K. Tashiro, "New Energy-Saving Air Compressors," in *Hitachi Review: Environmentally Conscious Technology in Industrial Fields Aiming for a Low-Carbon Society*, vol. 6, no. 5, 2017, pp. 530–535.

[44] Y. Lee and J. Ha, "Power Enhancement of Dual Inverter for Open-End Permanent Magnet Synchronous Motor," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, March 2013, pp. 1545–1551, DOI: 10.1109/APEC.2013.6520502.

[45] S. M. Mousavi Gazafrudi, A. Tabakhpour Langerudy, E. F. Fuchs, and K. Al-Haddad, "Power Quality Issues in Railway Electrification: A Comprehensive Perspective," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 3081–3090, May 2015, DOI: 10.1109/TIE.2014.2386794.

[46] *Industrial, Scientific and Medical Equipment - Radio-Frequency Disturbance Characteristics - Limits and Methods of Measurement*, CISPR International Special Committee on Radio Interference Std. CISPR 11, 2017.

[47] *Adjustable Speed Electrical Power Drive Systems - Part 9-2*, International Electrotechnical Commission Std. IEC 61 800-9-2, 2017.

[48] Y. Li and T. Takahashi, "A Digitally Controlled 4 kW Single-Phase Bridgeless PFC Circuit for Air Conditioner Motor Drive Applications," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (IPEMC)*, Shanghai, China, Aug. 2006, pp. 1–5, DOI: 10.1109/IPEMC.2006.4778020.

[49] A. Marcos-Pastor, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martínez-Salamero, "Minimum DC-Link Capacitance for Single-Phase Applications with Power Factor Correction," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 5204–5208, June 2020, DOI: 10.1109/TIE.2019.2922925.

[50] M. Swamy and C. Guddanti, "An Improved Single-Phase Active-Front-End Rectifier System for Use with Three-Phase Variable-Frequency Drives," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Fort Worth, TX, USA, March 2014, pp. 1558–1564, DOI: 10.1109/APEC.2014.6803514.

[51] C. B. Jacobina, E. C. Dos Santos, N. Rocha, and E. L. L. Fabrício, "Single-Phase to Three-Phase Drive System Using Two Parallel Single-Phase Rectifiers," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1285–1295, May 2010, DOI: 10.1109/TPEL.2009.2037420.

[52] J. S. Moghani and M. Heidari, "High Efficient Low Cost Induction Motor Drive for Residential Applications," in *Proc. of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Taormina, Italy, May 2006, pp. 1399–1402, DOI: 10.1109/SPEEDAM.2006.1649986.

[53] W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav, and M. Pietola, "A Review of Integrated Motor Drive and Wide-Bandgap Power Electronics for High-Performance Electro-Hydrostatic Actuators," *IEEE Transactions on Transportation Electrification*, vol. 4, no. 3, pp. 684–693, Sept. 2018, DOI: 10.1109/TTE.2018.2853994.

[54] B. Janjic, G. Ebelt, J. Mades, F. Di Santo, A. Frigo, G. Verlato, and C. Prearo, "Highly Integrated Synchronous Reluctance Motor Drive System with SiC-MOSFETs," in *Proc. of the European Conference on Power Electronics and Applications (EPE-ECCE Europe)*, Riga, Latvia, Sept. 2018, pp. 1–9.

[55] N. Hanigovszki, J. Landkildehus, G. Spiazzi, and F. Blaabjerg, "An EMC Evaluation of the Use of Unshielded Motor Cables in AC Adjustable Speed Drive Applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 273–281, Jan. 2006, DOI: 10.1109/TPEL.2005.861182.

[56] E. Persson and D. Wilhelm, "Gate Drive Concept for $\mathrm{d}v/\mathrm{d}t$ Control of GaN GIT-Based Motor Drive Inverters," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, pp. 27.6.1–27.6.4, DOI: 10.1109/IEDM13553.2020.9372095.

[57] M. L. Gasperi, "Life Prediction Model for Aluminum Electrolytic Capacitors," in *Proc. of the Industry Applications Society Annual Meeting (IAS)*, San Diego, CA, USA, Oct. 1996, pp. 1347–1351.

[58] A. M. Imam, T. G. Habetler, R. G. Harley, and D. M. Divan, "Condition Monitoring of Electrolytic Capacitor in Power Electronic Circuits using Adaptive Filter Modeling," in *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, Dresden, Germany, June 2005, pp. 601–607, DOI: 10.1109/PESC.2005.1581687.

[59] J. W. Kolar, J. Biela, and J. Miniböck, "Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2 % Efficiency vs. 7 kW/in^3 Power Density," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (IPEMC)*, Wuhan, China, May 2009, pp. 1–21, DOI: 10.1109/IPEMC.2009.5289336.

[60] M. L. Gasperi, "Life Prediction Modeling of Bus Capacitors in AC Variable-Frequency Drives," *IEEE Transactions on Industry Applications*, vol. 41, no. 6, pp. 1430–1435, Nov. 2005, DOI: 10.1109/TIA.2005.858258.

[61] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of Active Power Decoupling Topologies in Single-Phase Systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778–4794, July 2016, DOI: 10.1109/TPEL.2015.2477882.

[62] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-Compact Power Pulsation Buffer for Single-Phase DC/AC Converter Systems," in

Proc. of the IEEE International Power Electronics and Motion Control Conference (ECCE Asia), Hefei, China, May 2016, pp. 1–10, DOI: 10.1109/IPEMC.2016.7512730.

[63] M. Ghosh, R. Mitova, R. Srikanth, M. X. Wang, and D. Klikic, "Novel Active Ripple Filtering Schemes used in Little Box Inverter," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, Nuremberg, Germany, May 2017, pp. 1609–1616.

[64] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. C. N. Pilawa-Podgurski, "A High Power Density Series-Stacked Energy Buffer for Power Pulsation Decoupling in Single-Phase Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4905–4924, Aug. 2017, DOI: 10.1109/TPEL.2016.2601309.

[65] D. Neumayr, D. Bortis, and J. W. Kolar, "The Essence of the Little Box Challenge-Part B: Hardware Demonstrators and Comparative Evaluations," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 3, pp. 251–272, Sept. 2020, DOI: 10.24295/CPSSTPEA.2020.00022.

[66] N. F. Ershad and R. T. Mehrjardi, "A Low Cost Single-Phase to Three-Phase Power Converter for Low-Power Motor Drive Applications," in *Proc. of the IEEE Texas Power and Energy Conference (TPEC)*, College Station, TX, USA, Feb. 2018, pp. 1–6, DOI: 10.1109/TPEC.2018.8312061.

[67] J. I. Itoh and N. Ohtani, "Square-Wave Operation for a Single-Phase-PFC Three-Phase Motor Drive System Without a Reactor," *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 805–811, March 2011, DOI: 10.1109/TIA.2010.2102736.

[68] V. S. Chandekar, M. A. Chaudhari, and V. K. Chakravarthi, "A Low Cost Three-Phase Induction Motor Drive Operated on Single-Phase Input Source," in *Proc. of the International Conference on Smart Electric Drives and Power System (ICSEDPS)*, Nagpur, India, June 2018, pp. 375–379, DOI: 10.1109/ICSEDPS.2018.8536009.

[69] M. Haider, D. Bortis, J. W. Kolar, and Y. Ono, "Novel Sinusoidal Input Current Single-to-Three-Phase Z-Source Buck+Boost AC/AC Converter," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (ECCE Asia)*, Niigata, Japan, May 2018, pp. 4080–4087, DOI: 10.23919/IPEC.2018.8507381.

[70] Y. Nakata and J. I. Itoh, "An Experimental Verification and Analysis of a Single-Phase to Three-Phase Matrix Converter using PDM Control Method for High-Frequency Applications," in *Proc. of the IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Singapore, Dec. 2011, pp. 1084–1089, DOI: 10.1109/PEDS.2011.6147394.

[71] Y. Bak, J. S. Lee, and K. B. Lee, "Modulation and Control Strategy for a Single-Phase to Three-Phase Indirect Matrix Converter Drive," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Cincinnati, OH, USA, Oct. 2017, pp. 1065–1070, DOI: 10.1109/ECCE.2017.8095905.

[72] Y. Ohnuma and J. I. Itoh, "Novel Control Strategy for Single-Phase to Three-Phase Power Converter Using an Active Buffer," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (IPEMC)*, Wuhan, China, May 2009, pp. 1–10, DOI: 10.1109/IPEMC.2009.5157536.

[73] Y. Ohnuma and J. I. Itoh, "A Control Method for a Single-to-Three-Phase Power Converter with an Active Buffer and a Charge Circuit," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Atlanta, GA, USA, Sept. 2010, pp. 1801–1807, DOI: 10.1109/ECCE.2010.5618137.

[74] H. Haga, K. Nishiya, S. Kondo, and K. Ohishi, "High Power Factor Control of Electrolytic Capacitor Less Current-Fed Single-Phase to Three-Phase Power Converter," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (ECCE Asia)*, Sapporo, Japan, Sept 2010, pp. 443–448, DOI: 10.1109/IPEC.2010.5542194.

[75] H. Takahashi, R. Hisamichi, and H. Haga, "High Power Factor Control for Current-Source Type Single-Phase to Three-Phase Matrix Converter," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, San Jose, CA, USA, Sept. 2009, pp. 3071–3076, DOI: 10.1109/ECCE.2009.5316050.

[76] "The Potential of Wide-Bandgap Semiconductors," http://www.powerelectronicsnews.com/.

[77] M. Haider, M. Guacci, D. Bortis, J. W. Kolar, and Y. Ono, "Analysis and Evaluation of Active/Hybrid/Passive dv/dt-Filter Concepts

for Next Generation SiC-Based Variable Speed Drive Inverter Systems," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, Oct. 2020, pp. 4923–4930, DOI: 10.1109/ECCE44975.2020.9236148.

[78] Y. Xu, X. Yuan, F. Ye, Z. Wang, Y. Zhang, M. Diab, and W. Zhou, "Impact of High Switching Speed and High Switching Frequency of Wide-Bandgap Motor Drives on Electric Machines," *IEEE Access*, vol. 9, pp. 82 866–82 880, June 2021, DOI: 10.1109/ACCESS.2021.3086680.

[79] X. Deng, M. A. S. Mohamed, S. Lambert, and B. Mecrow, "Development of a High-Speed, Permanent Magnet, SiC-Based Drive with Integrated Input Filters," *IEEE Transactions on Energy Conversion*, vol. 35, no. 2, pp. 863–874, June 2020, DOI: 10.1109/TEC.2020.2973449.

[80] M. Haider, D. Bortis, J. W. Kolar, and Y. Ono, "Sinusoidal Input Current and Average Speed Control of a Single-Phase Supplied Three-Phase Inverter Drive Without Electrolytic Capacitor," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (IPEMC)*, Budapest, Hungary, Aug. 2018, pp. 756–763, DOI: 10.1109/IPEMC.2006.4778020.

[81] K. Inazuma, K. Ohishi, and H. Haga, "High-Power-Factor Control for Inverter Output Power of IPM Motor Driven by Inverter System Without Electrolytic Capacitor," in *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, Gdansk, Poland, June 2011, pp. 619–624, DOI: 10.1109/ISIE.2011.5984229.

[82] H. S. Jung, S. J. Chee, S. K. Sul, Y. J. Park, H. S. Park, and W. K. Kim, "Control of Three-Phase Inverter for AC Motor Drive with Small DC-Link Capacitor Fed by Single-Phase AC Source," *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1074–1081, March 2014, DOI: 10.1109/TIA.2013.2288238.

[83] J. H. Tau and Y. Y. Tzou, "PFC Control of Electrolytic Capacitor-Less PMSM Drives for Home Appliances," in *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, Edinburgh, UK, June 2017, pp. 335–341, DOI: 10.1109/ISIE.2017.80012699.

[84] G. Wang, N. Zhao, J. Qi, C. Li, and D. Xu, "High Power Factor Control of IPMSM Drive System Without Electrolytic Capacitor," in *Proc. of the IEEE International Power Electronics and Motion Control*

Conference (ECCE Asia), Hefei, China, May 2016, pp. 379–383, DOI: 10.1109/IPEMC.2016.7512316.

[85] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A Review of Single-Phase Improved Power Quality AC-DC Converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, Oct. 2003, DOI: 10.1109/TIE.2003.817609.

[86] M. J. Jacoboski, A. de Bastiani Lange, and M. L. Heldwein, "Closed-Form Solutions for Core and Winding Losses Calculation in Single-Phase Boost PFC Rectifiers," in *Proc. of the Southern Power Electronics Conference (SPEC)*, Santos, Brazil, Dec. 2019, pp. 1–6, DOI: 10.1109/COBEP/SPEC44138.2019.9065521.

[87] M. Nitzsche, S. Lu, M. Zehelein, J. Ruthardt, and J. Roth-Stielow, "Comprehensive Comparison of 99 % Efficient Totem-Pole PFC with Fixed (PWM) or Variable (TCM) Switching Frequency," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, Nuremberg, Germany, July 2020, pp. 207–214.

[88] M. Haider, J. Azurza-Anderson, N. Nain, G. Zulauf, J. W. Kolar, D. Xu, and G. Deboy, "Analytical Calculation of the Residual ZVS Losses of TCM-Operated Single-Phase PFC Rectifiers," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 250–264, Feb. 2021, DOI: 10.1109/OJPEL.2021.3058048.

[89] R. B. Prest, J. D. van Wyk, and J. Schultz, "Development of a Three-Phase Variable Speed Drive System for a Battery Fed Underground Mining Locomotive," in *Proc. of the International Conference on Power Electronics and Variable-Speed Drives*, London, UK, July 1988, pp. 233–236.

[90] M. Kaufhold, H. Aninger, M. Berth, J. Speck, and M. Eberhardt, "Electrical Stress and Failure Mechanism of the Winding Insulation in PWM-Inverter-Fed Low-Voltage Induction Motors," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 2, pp. 396–402, April 2000, DOI: 10.1109/41.836355.

[91] "Aluminum Electrolytic Capacitors: B43742, B43762," Datasheet, https://www.tdk-electronics.tdk.com/inf/20/30/db/aec/B43742_B43762.pdf, TDK.

[92] A. L. Kimball and P. L. Alger, "Single-Phase Motor-Torque Pulsations," *Transactions of the American Institute of Electrical Engineers*, vol. XLIII, pp. 730–739, Jan. 1924, DOI: 10.1109/T-AIEE.1924.5061027.

[93] K. Lee and J. I. Ha, "Single-Phase Inverter Drive for Interior Permanent Magnet Machines," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1355–1366, Feb. 2017, DOI: 10.1109/TPEL.2016.2553782.

[94] B. Szabados and U. Schaibie, "Peak Power Bidirectional Transfer from High Speed Flywheel to Electrical Regulated Bus Voltage System: A Practical Proposal for Vehicular Technology," *IEEE Transactions on Energy Conversion*, vol. 13, no. 1, pp. 34–41, Mar. 1998, DOI: 10.1109/60.658201.

[95] M. I. Daoud, A. Abdel-Khalik, S. Ahmed, and A. M. Massoud, "DC Bus Control of an Advanced Flywheel Energy Storage Kinetic Traction System for Electrified Railway Industry," in *Proc. of the IEEE Conference of the Industrial Electronics Society (IECON)*, Vienna, Austria, Nov. 2013, pp. 6596–6601, DOI: 10.1109/IECON.2013.6700223.

[96] M. L. Sough, D. Depernet, F. Dubas, B. Boualem, and C. Espanet, "PMSM and Inverter Sizing Compromise Applied to Flywheel for Railway Application," in *Proc. of the IEEE Vehicle Power and Propulsion Conference (VPPC)*, Lille, France, Sept. 2010, pp. 1–5, DOI: 10.1109/VPPC.2010.5729060.

[97] F. Diaz-Gonzalez, F. D. Bianchi, A. Sumper, and O. Gomis-Bellmunt, "Control of a Flywheel Energy Storage System for Power Smoothing in Wind Power Plants," *IEEE Transactions on Energy Conversion*, vol. 29, no. 1, pp. 204–214, March 2014, DOI: 10.1109/TEC.2013.2292495.

[98] L. Zhou and Z. P. Qi, "Modeling and Simulation of Flywheel Energy Storage System with IPMSM for Voltage Sags in Distributed Power Network," in *Proc. of the International Conference of Mechatronics and Automation*, Changchun, China, Aug. 2009, pp. 5046–5051, DOI: 10.1109/ICMA.2009.5246111.

[99] Y. Li, M. Liu, and J. Lau, "Development of a Variable Speed Compressor Power Model for Single-Stage Packaged DX Rooftop Units," *Applied Thermal Engineering*, vol. 78, pp. 110–117, March 2015, DOI: 10.1016/j.applthermaleng.2014.12.038.

[100] M. Xie, C. Zhu, L. He, and H. Wen, "An Experimental Study of MAF-SRF-PLL with Comb Compensator," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, March 2017, pp. 1310–1313, DOI: 10.1109/APEC.2017.7930865.

[101] J. J. Cabezas, R. Gonzalez-Medina, E. Figueres, and G. Garcera, "Comparison and Combination of Digital Controls for Single-Phase Boost PFC Converters in Avionic Power Systems," in *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, Edinburgh, UK, June 2017, pp. 645–650, DOI: 10.1109/ISIE.2017.8001322.

[102] T. Rudnicki, R. Czerwinski, and D. Polok, "Performance Analysis of a PMSM Drive with Torque and Speed Control," in *Proc. of the International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)*, Torun, Poland, June 2015, pp. 562–566, DOI: 10.1109/MIXDES.2015.7208586.

[103] K. S. Low, M. F. Rahman, and K. W. Lim, "The dq-Transformation and Feedback Linearization of a Permanent Magnet Synchronous Motor," in *Proc. of the IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Singapore, Feb. 1995, pp. 292–296, DOI: 10.1109/PEDS.1995.404906.

[104] W. Hu, C. Chen, S. Duan, W. Wan, L. Song, and J. Zhu, "Decoupled Average Current Balancing Method for Interleaved Buck Converters with Dual Closed-Loop Control," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (ECCE Asia)*, Nanjing, China, Dec. 2020, pp. 578–583, DOI: 10.1109/IPEMC-ECCEAsia48364.2020.9367656.

[105] S. Duan, L. Zhou, and J. Wang, "Flux Weakening Mechanism of Interior Permanent Magnet Synchronous Machines with Segmented Permanent Magnets," *IEEE Transactions on Applied Superconductivity*, vol. 24, no. 3, pp. 1–5, June 2014, DOI: 10.1109/TASC.2013.2280847.

[106] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A High-Performance Generalized Discontinuous PWM Algorithm," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, Sept. 1998, DOI: 10.1109/28.720446.

[107] B. Anirudh-Acharya and V. John, "Design of Output dv/dt Filter for Motor Drives," in *Proc. of the International Conference on Industrial and Information Systems (ICIIS)*, Mangalore, India, July 2010, pp. 562–567, DOI: 10.1109/ICIINFS.2010.5578641.

[108] M. Guacci, J. Azurza-Anderson, K. L. Pally, D. Bortis, J. W. Kolar, M. Kasper, J. Sanchez, and G. Deboy, "Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters using Advanced Measurement Techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, Sept. 2020, DOI: 10.1109/JESTPE.2019.2944268.

[109] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019, DOI: 10.1109/TPEL.2018.2834345.

[110] S. Yin, K. J. Tseng, C. F. Tong, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "A 99Rectification," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, March 2016, pp. 2942–2949.

[111] A. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs," *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 587–589, July 2007.

[112] X. Jiang, J. Wang, J. Chen, Z. Li, D. Zhai, X. Yang, B. Ji, and Z. J. Shen, "Investigation on Degradation of SiC MOSFET Under Surge Current Stress of Body Diode," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 77–89, March 2020.

[113] "Datasheet for SIMOTICS S-1FT7," Datasheet, 1FT7084-5SF75-1MG1, Siemens.

[114] W. Tong, S. Dai, S. Wu, and R. Tang, "Performance Comparison between an Amorphous Metal PMSM and a Silicon Steel PMSM," *IEEE Transactions on Magnetics*, vol. 55, no. 6, pp. 1–5, June 2019, DOI: 10.1109/TMAG.2019.2900531.

[115] "C3M0016120K Silicon Carbide Power MOSFET," Datasheet, https://assets.wolfspeed.com/uploads/2020/12/C3M0016120K.pdf, Cree, accessed: Oct. 7th, 2021.

[116] "C3M0032120K Silicon Carbide Power MOSFET," Datasheet, https://assets.wolfspeed.com/uploads/2020/12/C3M0032120K.pdf, Cree, accessed: Oct. 7th, 2021.

[117] A. Nakagawa, Y. Yamaguchi, T. Ogura, K. Watanabe, Y. Yasuhara, R. Sato, K. Endo, and K. Furukawa, "500 V Three-Phase Inverter ICs Based on a New Dielectric Isolation Technique," in *Proc. of the International Symposium on Power Semiconductor Devices and ICs*, Tokyo, Japan, May 1992, pp. 328–332.

[118] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Mühlethaler, T. Nussbaumer, and J. Miniböck, "Extreme Efficiency Power Electronics," in *Proc. of the International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, Germany, March 2012, pp. 1–22.

[119] P. Wang, G. C. Montanari, and A. Cavallini, "Partial Discharge Phenomenology and Induced Aging Behavior in Rotating Machines Controlled by Power Electronics," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 7105–7112, Dec. 2014, DOI: 10.1109/TIE.2014.2320226.

[120] "1EDI EiceDRIVER Compact, Output with Clamp Variant for IGBT," Datasheet, https://www.infineon.com/dgdl/Infineon-1EDIX0I12MF-DS-v02_00-EN.pdf?fileId=5546d46145f1f3a401462944e0190fd7, Infineon Technologies AG, accessed: Oct. 7th, 2021.

[121] M. Vujacic, M. Hammami, M. Srndovic, and G. Grandi, "Analysis of DC-Link Voltage Switching Ripple in Three-Phase PWM Inverters," *Energies*, vol. 11, no. 2, 2018, DOI: 10.3390/en11020471.

[122] "Metallized Polypropylene Film Capacitors (MKP): B32776," Datasheet, hhttps://www.tdk-electronics.tdk.com/inf/20/20/db/fc_2009/MKP_B32774_778.pdf, TDK.

[123] D. Neumayr, D. Bortis, and J. W. Kolar, "The Essence of the Little Box Challenge - Part A: Key Design Challenges and Solutions," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 2, pp. 158–179, June 2020, DOI: 10.24295/CPSSTPEA.2020.00014.

[124] P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "Minimum Loss Operation and Optimal Design of High-Frequency Inductors for Defined Core and Litz Wire," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 469–487, Sept. 2020, DOI: 10.1109/OJPEL.2020.3027452.

[125] "Kool Mμ E-Core 00K4317E040," Datasheet, https://www.mag-inc.com/Media/Magnetics/Datasheets/00K4317E040.pdf, Magnetics, accessed: Nov. 22th, 2021.

[126] P. Papamanolis, D. Bortis, F. Krismer, D. Menzi, and J. W. Kolar, "New EV Battery Charger PFC Rectifier Front-End Allowing Full Power Delivery in 3-Phase and 1-Phase Operation," *Electronics*, vol. 10, no. 17, 2021, DOI: 10.3390/electronics10172069.

[127] R. Martis, R. Siecoban, C. Martis, and L. Szabo, "Common and Normal Mode Currents in PMSM PWM Drives," in *Proc. of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Capri, Italy, June 2016, pp. 500–504, DOI: 10.1109/SPEEDAM.2016.7525877.

[128] "EMC Products Based on Nanocrystalline Vitroperm," Datasheet, https://www.vacuumschmelze.com/03_Documents/Brochures/EMC%20Nanocrystalline%20VITROPERM.pdf, Vacuumschmelze, accessed: Nov. 18th, 2021.

[129] R. De Maglie and A. Engler, "Radiation Prediction of Power Electronics Drive System for Electromagnetic Compatibility in Aerospace Applications," in *Proc. of the European Conference on Power Electronics and Applications (EPE-ECCE Europe)*, Birmingham, UK, Aug. 2011, pp. 1–9.

[130] S. Chowdhury, E. Gurpinar, G. J. Su, T. Raminosoa, T. A. Burress, and B. Ozpineci, "Enabling Technologies for Compact Integrated Electric Drives for Automotive Traction Applications," in *Proc. of the Transportation Electrification Conference and Expo (ITEC)*, Detroit, MI, USA, June 2019, pp. 1–8, DOI: 10.1109/ITEC.2019.8790594.

[131] "TM 300 Series In-Line Torque Transducers," Manual, TM 310, Magtrol.

[132] *Specification for Radio Disturbance and Immunity Measuring Apparatus and Methods - Part 3-2*, CISPR International Special Committee on Radio Interference Std. CISPR 16-2-1, 2007.

[133] M. Chomat, L. Schreier, and J. Bendl, "Active Front-End of Electric Drive under Unbalanced Voltage Supply," in *Proc. of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Pisa, Italy, June 2010, pp. 227–232, DOI: 10.1109/SPEEDAM.2010.5545072.

[134] D. Frugier and P. Ladoux, "Voltage Disturbances on 25 kV-50 Hz Railway Lines – Modelling Method and Analysis," in *Proc. of the International Symposium on Power Electronics, Electrical Drives, Automation*

and Motion (SPEEDAM), Pisa, Italy, June 2010, pp. 1080–1085, DOI: 10.1109/SPEEDAM.2010.5544858.

[135] M. Baumann and J. W. Kolar, "A Novel Control Concept for Reliable Operation of a Three-Phase Three-Switch Buck-Type Unity-Power-Factor Rectifier with Integrated Boost Output Stage under Heavily Unbalanced Mains Condition," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 2, pp. 399–409, April 2005, DOI: 10.1109/TIE.2005.843916.

[136] S. Gao and M. Barnes, "Phase-Locked Loop for AC Systems: Analyses and Comparisons," in *Proc. of the IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Bristol, UK, March 2012, pp. 1–6, DOI: 10.1049/cp.2012.0199.

[137] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A New Single-Phase PLL Structure Based on Second Order Generalized Integrator," in *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, Jeju, South Korea, June 2006, pp. 1–6, DOI: 10.1109/pesc.2006.1711988.

[138] T. Wymann and J. Pieder, "Power Loss Ride-Through in a Variable Speed Drive System," in *Proc. of the IEEE Petroleum and Chemical Industry Conference Europe*, Amsterdam, Netherlands, June 2014, pp. 1–9, DOI: 10.1109/PCICEurope.2014.6900057.

[139] P. Piya, M. Ebrahimi, M. Karimi-Ghartemani, and S. A. Khajehoddin, "Fault Ride-Through Capability of Voltage-Controlled Inverters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7933–7943, Oct. 2018, DOI: 10.1109/TIE.2018.2803765.

[140] C. Y. Tang, Y. T. Chen, and Y. M. Chen, "PV Power System with Multi-Mode Operation and Low-Voltage Ride-Through Capability," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7524–7533, Oct. 2015, DOI: 10.1109/TIE.2015.2449777.

[141] A. Van Zyl, R. Spee, A. Faveluke, and S. Bhowmik, "Voltage Sag Ride-Through for Adjustable-Speed Drives with Active Rectifiers," *IEEE Transactions on Industry Applications*, vol. 34, no. 6, pp. 1270–1277, Nov. 1998, DOI: 10.1109/28.739005.

[142] J. Holtz, W. Lotzkat, and S. Stadtfeld, "Controlled AC Drives with Ride-Through Capability at Power Interruption," *IEEE Transactions on Industry Applications*, vol. 30, no. 5, pp. 1275–1283, Sept. 1994, DOI: 10.1109/28.315239.

[143] *Railway Applications - Electronic Equipment Used on Rolling Stock*, British Standards Institution Std. EN 50 155, 2007.

[144] M. R. Hesamzadeh, N. Hosseinzadeh, and P. J. Wolfs, "Design and Study of a Switch Reactor for Central Queensland SWER System," in *Proc. of the Universities Power Engineering Conference (UPEC)*, Padova, Italy, Sept. 2008, pp. 1–5, DOI: 10.1109/UPEC.2008.4651481.

[145] A. A. Usmani, M. Shahrukh, and A. Mustafa, "Comparison of Different Three-Phase Inverter Topologies: A Review," in *Proc. of the International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT)*, Coimbatore, India, Feb. 2017, pp. 19–24.

[146] I. Takahashi and H. Haga, "Power Factor Improvement of Single-Phase Diode Rectifier by Fast Field-Weakening of Inverter Driven IPM Motor," in *Proc. of the IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Denpasar, Indonesia, Oct. 2001, pp. 241–246, DOI: 10.1109/PEDS.2001.975319.

[147] H. Lamsahel and P. Mutschler, "Permanent Magnet Drives with Reduced DC-Link Capacitor for Home Appliances," in *Proc. of the IEEE Conference of the Industrial Electronics Society (IECON)*, Porto, Portugal, Nov. 2009, pp. 725–730, DOI: 10.1109/IECON.2009.5415009.

[148] S. W. Kang, S. I. Kim, R. Y. Kim, and D. S. Hyun, "A Novel Power Factor Control for Synchronous Motor Drive System with Small DC-Link Capacitor," in *Proc. of the IEEE Vehicle Power and Propulsion Conference (VPPC)*, Beijing, China, Oct. 2013, pp. 16–20, DOI: 10.1109/VPPC.2013.6671656.

[149] F. Ludwig and A. Möckel, "Operation Method for AC Grid Powered PMSM with Open-End Winding in Dual-Inverter Topology for Power Factor Maximization," in *Proc. of the IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Glasgow, UK, April 2016, pp. 1–5, DOI: 10.1049/cp.2016.0227.

[150] M. Nishio and H. Haga, "Single-Phase to Three-Phase Electrolytic Capacitor-Less Dual Inverter-Fed IPMSM for Suppress Torque Pulsation," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 6537–6546, August 2021, DOI: 10.1109/TIE.2020.3000091.

[151] H. Shin and J. I. Ha, "Active DC-Link Circuit for Single-Phase Diode Rectifier System with Small Capacitance," in *Proc. of the*

IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shanghai, China, Nov. 2014, pp. 875–880, DOI: 10.1109/PEAC.2014.7037974.

[152] D. Menzi, D. Bortis, and J. W. Kolar, "A New Bidirectional Three-Phase Phase-Modular Boost-Buck AC/DC Converter," in *Proc. of the IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, China, Nov. 2018, pp. 1–8, DOI: 10.1109/PEAC.2018.8590670.

[153] J. K. Pandit, B. Sakthisudhursun, and M. V. Aware, "PR Controller Implementation using Double Update Mode Digital PWM for Grid Connected Inverter," in *Proc. of the International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Mumbai, India, Dec. 2014, pp. 1–6, DOI: 10.1109/PEDES.2014.7042014.

[154] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche, and J. A. Melkebeek, "Small-Signal Laplace-Domain Analysis of Uniformly-Sampled Pulse-Width Modulators," in *Proc. of the IEEE Power Electronics Specialists Conference (PESC)*, Aachen, Germany, June 2004, pp. 4292–4298, DOI: 10.1109/PESC.2004.1354760.

[155] J. Forbes, M. Ordonez, and M. Anun, "Improving the Dynamic Response of Power Factor Correctors Using Simple Digital Filters: Moving Average Filter Comparative Evaluation," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Denver, CO, USA, Sept. 2013, pp. 4814–4819, DOI: 10.1109/ECCE.2013.6647348.

[156] F. Briz, D. Díaz-Reigosa, M. W. Degner, P. García, and J. M. Guerrero, "Current Sampling and Measurement in PWM Operated AC Drives and Power Converters," in *Proc. of the IEEE International Power Electronics and Motion Control Conference (ECCE Asia)*, Sapporo, Japan, June 2010, pp. 2753–2760, DOI: 10.1109/IPEC.2010.5543175.

[157] G. Rohner, S. Mirić, D. Bortis, J. W. Kolar, and M. Schweizer, "Comparative Evaluation of Overload Capability and Rated Power Efficiency of 200 V Si/GaN 7-Level FC 3-Φ Variable Speed Drive Inverter Systems," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, June 2021, pp. 2177–2186, DOI: 10.1109/APEC42165.2021.9487125.

[158] *International Energy Agency*, World Energy Outlook, 2019.

[159] N. Mukherjee, J. Fuerst, F. Diepold, and F. A. Vega, "900 V GaN-Based Sine-Wave Inverters for Three-Phase Industrial Applications," in *Proc. of the IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Liverpool, UK, April 2018, pp. 3754–3759, DOI: 10.1049/joe.2018.8032.

[160] F. Maislinger, H. Ertl, G. Stojcic, and F. Holzner, "Efficiency and Motor-Performance Improvement using WBG-Inverters with Observer-Based Actively Damped LC-Sine Wave Filters," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, Nuremberg, Germany, May 2019, pp. 1595–1603.

[161] T. Bürger, K. Berberich, and S. Pruefling, "Silicon Carbide Semiconductors for the E-Powertrain," *ATZelektronik Worldwide*, vol. 13, no. 2, pp. 48–51, April 2018, DOI: 10.1007/s38314-018-0025-x.

[162] M. Slawinski, D. Heer, T. Villbusch, and M. Buschkuehle, "System Study of SiC MOSFET and Si IGBT Power Module Performance using Bidirectional Buck-Boost Converter as Evaluation Platform," in *Proc. of the European Conference on Power Electronics and Applications (EPE-ECCE Europe)*, Karlsruhe, Germany, Sept. 2016, pp. 1–8, DOI: 10.1109/EPE.2016.7695334.

[163] *Rotating Electrical Machines – Part 18-41*, International Electrotechnical Commission Std. IEC 60 034-18-41, 2014.

[164] *Motors and Generators - NEMA MG 1*, The Association of Electrical Equipment and Medical Imaging Manufacturers Std. NEMA MG 1, 2009.

[165] N. Hanigovszki, J. Landkildehus, and F. Blaabjerg, "Output Filters for AC Adjustable Speed Drives," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, March 2007, pp. 236–242, DOI: 10.1109/APEX.2007.357520.

[166] "User Guide for REF-22K-GPD-INV-EASY3B," Application Note, https://www.infineon.com/dgdl/Infineon-UG2020_28_REF-22K-GPD-INV-Easy3b-UserManual-v01_00-EN.pdf?fileId=5546d46277fc7439017802de2ffb672a, Infineon Technologies AG, accessed: Oct. 7th, 2021.

[167] J. He, C. Li, A. Jassal, N. Thiagarajanark, Y. Zhang, S. Prabhakaran, C. Feliz, J. E. Graham, and X. Kang, "Multi-Domain Design Optimization of dv/dt Filter for SiC-Based Three-Phase Inverters in High-Frequency Motor-Drive Applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5214–5222, Sept. 2019, DOI: 10.1109/TIA.2019.2922306.

[168] K. Sung-Jun and S. Seung-Ki, "A Novel Filter Design for Suppression of High Voltage Gradient in Voltage-Fed PWM Inverter," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Atlanta, GA, USA, Feb. 1997, pp. 122–127, DOI: 10.1109/APEC.1997.581442.

[169] D. A. Rendusara and P. N. Enjeti, "An Improved Inverter Output Filter Configuration Reduces Common and Differential Modes dv/dt at the Motor Terminals in PWM Drive Systems," *IEEE Transactions on Power Electronics*, vol. 13, no. 6, pp. 1135–1143, Nov. 1998, DOI: 10.1109/63.728340.

[170] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM Inverters on AC Motor Bearing Currents and Shaft Voltages," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 250–259, March 1996, DOI: 10.1109/28.491472.

[171] J. P. Ström, J. Korhonen, J. Tyster, and P. Silventoinen, "Active du/dt-New Output-Filtering Approach for Inverter-Fed Electric Drives," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3840–3847, Sept. 2011, DOI: 10.1109/TIE.2010.2093480.

[172] J. Korhonen, J. P. Ström, J. Tyster, P. Silventoinen, H. Saren, and K. Rauma, "Control of an Inverter Output Active du/dt Filtering Method," in *Proc. of the IEEE Conference of the Industrial Electronics Society (IECON)*, Porto, Portugal, Nov. 2009, pp. 316–321, DOI: 10.1109/IECON.2009.5414941.

[173] H. Kim, S. Acharya, A. Anurag, B. H. Kim, and S. Bhattacharya, "Effect of Inverter Output dv/dt with Respect to Gate Resistance and Loss Comparison with dv/dt Filters for SiC MOSFET based High Speed Machine Drive Applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Baltimore, MD, USA, Oct. 2019, pp. 2301–2306, DOI: 10.1109/ECCE.2019.8912249.

[174] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9032–9042, Nov. 2017, DOI: 10.1109/TIE.2017.2719603.

[175] G. Aggeler, F. Canales, J. Biela, and J. W. Kolar, "dv/dt -Control Methods for the SiC JFET/Si MOSFET Cascode," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 4074–4082, Aug. 2013, DOI: 10.1109/TPEL.2012.2230536.

[176] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A Review on Switching Slew Rate Control for Silicon Carbide Devices Using Active Gate Drivers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4096 – 4114, Aug. 2021, DOI: 10.1109/JESTPE.2020.3008344.

[177] B. Sun, R. Burgos, X. Zhang, and D. Boroyevich, "Active dv/dt Control of 600 V GaN Transistors," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Milwaukee, WI, USA, Sept. 2016, pp. 1–8, DOI: 10.1109/ECCE.2016.7854818.

[178] Y. Lobsiger and J. W. Kolar, "Closed-Loop IGBT Gate Drive Featuring Highly Dynamic di/dt and dv/dt Control," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Raleigh, NC, USA, Sept. 2012, pp. 4754–4761, DOI: 10.1109/ECCE.2012.6342173.

[179] S. Beushausen, F. Herzog, and R. W. De Doncker, "GaN-Based Active Gate-Drive Unit with Closed-Loop du/dt-Control for IGBTs in Medium-Voltage Applications," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, Nuremberg, Germany, July 2020, pp. 1372–1379.

[180] T. Cui, Q. Ma, P. Xu, and Y. Wang, "Analysis and Optimization of Power MOSFETs Shaped Switching Transients for Reduced EMI Generation," *IEEE Access*, vol. 5, pp. 20 440–20 448, Oct. 2017, DOI: 10.1109/ACCESS.2017.2758443.

[181] "Quick-Reference Guide to Driving CoolGaN 600 V HEMTs," Application Note, https://www.infineon.com/dgdl/Infineon-Gallium_nitride_quick_reference_guide_to_driving_CoolGaN_600V_HEMTs-ApplicationNotes-v01_00-EN.pdf?fileId=5546d4627aa5d4f5017b39fc2b043f2b, Infineon Technologies AG, accessed: Oct. 7th, 2021.

[182] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of Power MOSFETs Revisited," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016, DOI: 10.1109/TPEL.2016.2574998.

[183] "Multilayer RF Capacitors," Datasheet, https://www.cde.com/resources/catalogs/MC.pdf, CDE Cornell Dubilier, accessed: Oct. 7th, 2021.

[184] P. Hofstetter, R. W. Maier, and M. M. Bakran, "Influence of the Threshold Voltage Hysteresis and the Drain Induced Barrier Lowering on the Dynamic Transfer Characteristic of SiC Power MOSFETs," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, March 2019, pp. 944–950, DOI: 10.1109/APEC.2019.8721772.

[185] P. Friedrichs, "SiC Power Devices—Lessons Learned and Prospects After 10 Years of Commercial Availability," in *Proc. of the International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH)*, Palm Springs, California, USA, May 2011, pp. 1–6.

[186] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active Power Device Selection in High- and Very-High-Frequency Power Converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6818–6833, July 2019, DOI: 10.1109/TPEL.2018.2874420.

[187] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical Converter Power Density Limits for Forced Convection Cooling," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, Nuremberg, Germany, June 2005, pp. 608–619.

[188] "WE-HCI SMT High Current Inductor (7443556130)," Datasheet, https://www.we-online.com/katalog/datasheet/7443556130.pdf, WE, accessed: Oct. 7th, 2021.

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