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Dual Three-Phase Active Bridge Isolated Three-Phase AC and DC Four-Port Converter

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MORRIS JONATAN HELLER

MSc ETH
born on 08.02.1990
citizen of Luzern, Switzerland

accepted on the recommendation of

Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Paolo Mattavelli, co-examiner

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ETH Zurich
Power Electronic Systems Laboratory
Physikstrasse 3 | ETL H23
8092 Zurich | Switzerland

http://www.pes.ee.ethz.ch

Further, science is a collaborative effort.
John Bardeen

Es strebe von euch jeder um die Wette, Die Kraft des Steins in seinem Ring' an Tag zu legen.
Gotthold Ephraim Lessing

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Abstract

Power electronic converters play a central role in the transition from the existing grid to the smart grid of the future. One of the tasks of the converters is to manage the energy exchange between the existing three-phase grid and the various sources and loads in so-called (smart) microgrids. These microgrids connect local energy sources, storages, and loads and thereby promise an efficient integration of renewable energy sources. This requires efficient and at the same time cost-effective converters that combine galvanic isolation and multiple ac and dc ports in one. In this context, the Dual Three-Phase Active Bridge Converter (D3ABC) topology was introduced. The D3ABC topology consists of a primary-side and a secondary-side two-level three-phase Voltage Source Converter (VSC), each with a dc link capacitor, and three ac-side LC filters. The ac-side filter inductor of each phase of the primary-side VSC shares the magnetic core with the ac-side filter inductor of the same phase of the secondary-side VSC what allows galvanically isolated power transfer between the two sides. Due to the non-ideal coupling between the filter inductors, the mechanism of this power transfer is similar to that of a Dual Active Bridge (DAB) converter. Accordingly, the D3ABC topology can be regarded as an integration of two three-phase VSCs and three DAB converters that provide two three-phase ac ports (ac_1 and ac_2), two dc ports (dc_1 and dc_2), and galvanic isolation between the ports ac_1, dc_1 (primary side) and ac_2, dc_2 (secondary side).

This thesis extends the findings on the D3ABC topology with respect to conducted Electromagnetic Interference (EMI) and four-port operation. The findings are verified by measurements on a 8 kW hardware demonstrator of the D3ABC topology, designed for ac_1–dc_1/dc_2 rectifier operation. The demonstrator is designed for a nominal Root Mean Square (RMS) phase voltage of 230 V at ac_1 and dc link voltages of $V_{dc,1} = 800$ V at dc_1 and $V_{dc,2} = 400$ V at dc_2.

First, a comprehensive description of the operating principle of the D3ABC topology for ac_1–dc_1/dc_2 rectifier operation is given. Based on this description, a model for calculating the conducted EMI noise at the primary-side ac port, ac_1, is presented. The EMI model considers the effects of the power levels, P_1 and P_2, at the primary- and secondary-side dc ports, dc_1 and dc_2, respectively, on the EMI noise level. The evaluation of this EMI model reveals that the EMI noise at port ac_1 is nearly independent of the load on port dc_1, but increases with increasing load on port dc_2. Based on the EMI model, a volume-optimized ac_1-side EMI filter is designed for the hardware demonstrator for operation with nominal voltages and power levels of $P_1 = 5.0$ kW and $P_2 = 2.5$ kW

at the two dc ports. The optimized EMI filter has a total boxed volume of $0.17\,\mathrm{dm}^3 = 10.4\,\mathrm{in}^3$ ($0.09\,\mathrm{dm}^3 = 5.5\,\mathrm{in}^3$ for the Differential Mode (DM) part and $0.08\,\mathrm{dm}^3 = 4.9\,\mathrm{in}^3$ for the Common Mode (CM) part of the filter). The measurements of the conducted EMI noise of the hardware demonstrator with EMI filter reveals, at the considered operating point and at the first spectral component entering the EMI band regulated by CISPR 11 (at $f = 175\,\mathrm{kHz}$), a noise amplitude that is consistently between the minimum and maximum noise levels predicted by the model. The measurements further confirm compliance with the Quasi-Peak (QP) limit defined by CISPR 11 class A for the considered operating point.

Next, the description of the operating principle of the D3ABC topology is extended with respect to ac_1–$\mathrm{dc}_1/\mathrm{dc}_2$–$\mathrm{ac}_2$ four-port operation. The description shows that the D3ABC is capable of independent bidirectional power exchange between all four ports ac_1, dc_1, dc_2 and ac_2. However, it is found that the operation of the converter with ac voltages with different line frequencies, $f_1 \neq f_2$, at the ports ac_1 and ac_2, leads to a Low-Frequency (LF) power pulsation in the DAB part of the D3ABC. This power pulsation causes undesired fluctuations in the dc link voltages and distortions in the ac currents. It is found that filtering this power pulsation, e.g, by the dc link capacitance, is not an option and consequently a new modulation scheme based on analytical calculations is developed to eliminate the power pulsation. The calculations supported by numerical analyses reveal a theoretical maximum power in the DAB part of 8.5 kW for four-port operation with the new modulation scheme. Circuit simulation results for $\mathrm{ac}_1/\mathrm{ac}_2$ operation with primary-side and secondary-side RMS phase voltages (line-to-neutral) of 230 V and 115 V at ac_1 and ac_2 respectively, a power of 8 kW, and significantly different line frequencies, $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$, show that the derived modulation scheme nearly eliminates the power pulsation. In particular, the dc link voltages, $v_{\mathrm{dc},1}$ and $v_{\mathrm{dc},2}$, show constant values and the ac currents are sinusoidal. Since the operation with $f_1 \neq f_2$ leads to an increase of the currents in the converter, the experimental verification on the hardware demonstrator is conducted at half voltages resulting in a reduced power of 2 kW. Measurements of dc link voltages and ac currents on the hardware demonstrator agree well with simulation results. In particular, the measured dc link voltages, $v_{\mathrm{dc},1}$ and $v_{\mathrm{dc},2}$, exhibit nearly constant values.

Finally, the findings about the D3ABC topology that have emerged over the course of this thesis are discussed. As an example, a key insight is the trade-off that arises from integrating the ac-side filter inductors into the DAB transformers. On the one hand, this directly reduces the number of magnetic

components and power semiconductor switches, but at the same time the integration leads to challenges such as increased stresses on the converter components. The increased stress is mainly due to the fact that some of the remaining components are used for multiple tasks at the same time. Since the use of components for multiple tasks in this thesis defines an integrated converter topology such as the D3ABC, it can be assumed that the findings listed are not limited to the D3ABC topology but are in general characteristic for challenges in integrated converter topologies.

Kurzfassung

Umrichter mit Leistungselektronik spielen eine zentrale Rolle beim Übergang vom bestehenden Netz zum Smart Grid der Zukunft. Eine Aufgabe der Umrichter im Smart Grid ist die Steuerung des Energieaustauschs zwischen dem bestehenden Drehstromnetz und den verschiedenen Quellen und Lasten in sogenannten (Smart) Microgrids. Ein Microgrid verbindet lokale Energiequellen, -speicher sowie -verbraucher und verspricht damit eine effiziente Integration erneuerbarer Energiequellen. Dafür erfordert ein Microgrid effiziente und gleichzeitig kostengünstige Umrichter, die vorzugsweise eine galvanische Trennung und mehrere Wechsel- und Gleichstromanschlüsse in einem System vereinen. In diesem Zusammenhang wurde die Dual Three-Phase Active Bridge Converter (D3ABC)-Topologie eingeführt. Die D3ABC-Topologie besteht aus einem primärseitigen und einem sekundärseitigen dreiphasigen Spannungszwischenkreisumrichter (Voltage Source Converter, VSC) mit je einer Zwischenkreiskapazität und drei wechselspannungsseitigen LC-Filternetzwerken (d.h. einem Filternetzwerk pro Phase). Die wechselspannungsseitige Filterinduktivität jeder Phase des primärseitigen VSC teilt sich den Magnetkern mit der wechselspannungsseitigen Filterinduktivität der gleichen Phase des sekundärseitigen VSC, was eine galvanisch getrennte Leistungsübertragung zwischen den beiden Seiten ermöglicht. Aufgrund der nichtidealen magnetischen Kopplung zwischen den primär- und sekundärseitigen Filterinduktivitäten ist der Mechanismus dieser Leistungsübertragung ähnlich wie bei einem DAB Gleichspannungswandler. Dementsprechend kann die D3ABC-Topologie als eine Integration von zwei dreiphasigen VSCs und drei DAB Wandlern betrachtet werden, die zwei dreiphasige Wechselspannungsanschlüsse (ac_1 und ac_2), zwei Gleichspannungsanschlüsse (dc_1 und dc_2) und eine galvanische Trennung zwischen den Anschlüssen ac_1, dc_1 (Primärseite) und ac_2, dc_2 (Sekundärseite) zur Verfügung stellt.

Diese Dissertation erweitert die Erkenntnisse zur D3ABC-Topologie in Bezug auf leitungsgebundene elektromagnetische Verträglichkeit (EMV) und Vier-Port Betrieb. Die Überprüfung der gewonnenen Erkenntnisse erfolgt anhand von Messungen an einem Hardwaredemonstrator der D3ABC-Topologie, der für ac_1–dc_1/dc_2 Gleichrichterbetrieb ausgelegt ist. Der Demonstrator ist für eine nominale Sternspannung (Phase zu Neutralleiter) mit einem Effektivwert von 230 V an ac_1 und Zwischenkreisgleichspannungen von $V_{dc,1} = 800\,V$ an dc_1 und $V_{dc,2} = 400\,V$ an dc_2 dimensioniert.

Die Arbeit ist in zwei Teile gegliedert. Der erste Teil beschreibt umfassend das Funktionsprinzip der D3ABC-Topologie für den ac_1–dc_1/dc_2 Gleichrichterbetrieb. Auf der Grundlage dieser Beschreibung wird ein Modell zur

Berechnung leitungsgebundener elektromagnetischer Störaussendungen am primärseitigen Wechselspannungsanschluss, ac_1, vorgestellt. Dieses Modell berücksichtigt die Auswirkungen der an den primär- und sekundärseitigen Gleichspannungsanschlüssen dc_1 bzw. dc_2 vorliegenden Leistungspegel P_1 bzw. P_2 auf die leitungsgebundenen Störaussendungen. Die Auswertung dieses Modells zeigt auf, dass die am Anschluss ac_1 auftretenden leitungsgebundenen Störaussendungen nahezu unabhängig von der Last am Anschluss dc_1 sind, aber mit zunehmender Last am Anschluss dc_2 ansteigen. Das Modell zu leitungsgebundenen elektromagnetischen Störaussendungen dient als Grundlage für den Entwurf eines für den Betrieb mit Nennspannungen und Leistungen von $P_1 = 5.0\,\mathrm{kW}$ und $P_2 = 2.5\,\mathrm{kW}$ an den beiden Gleichspannungsanschlüssen volumenoptimierten wechselspannungsseitigen Netzfilters für den Hardwaredemonstrator. Das optimierte Netzfilter hat ein quaderförmiges Gesamtvolumen von $0.17\,\mathrm{dm}^3 = 10.4\,\mathrm{in}^3$ ($0.09\,\mathrm{dm}^3 = 5.5\,\mathrm{in}^3$ bzw. $0.08\,\mathrm{dm}^3 = 4.9\,\mathrm{in}^3$ der für die zur Unterdrückung von Gegentakt- bzw. Gleichtaktanteilen zuständige Teile). Die Messungen der leitungsgebundenen elektromagnetischen Störaussendungen des Hardwaredemonstrators mit Netzfilter zeigen, dass am betrachteten Betriebspunkt die Amplitude der ersten Spektralkomponente die in das von CISPR 11 geregelte Frequenzband eintritt (bei $f = 175\,\mathrm{kHz}$), konsistent zwischen den vom Modell vorhergesagten minimalen und maximalen Amplitudenwerten liegt. Die Messungen bestätigen ausserdem die Einhaltung des von CISPR 11 Klasse A definierten Grenzwertes für den betrachteten Betriebspunkt.

Der zweite Teil der Arbeit erweitert die Beschreibung des Funktionsprinzips der D3ABC-Topologie auf den ac_1–dc_1/dc_2–ac_2 Vier-Port Betrieb. Es stellt sich heraus, dass das D3ABC System zum unabhängigen bidirektionalen Leistungsaustausch zwischen allen vier Ports ac_1, dc_1, dc_2 und ac_2 fähig ist, der Betrieb des Umrichters mit Netzwechselspannungen unterschiedlicher Frequenzen, $f_1 \neq f_2$, an den Anschlüssen ac_1 und ac_2 jedoch zu einer niederfrequenten Leistungspulsation im DAB-Teil des D3ABC führt. Diese Leistungspulsation verursacht unerwünschte Schwankungen der Zwischenkreisspannungen und Verzerrungen der Netzströme. Da eine Filterung dieser Pulsation, z. B. durch die Zwischenkreiskapazität, nicht möglich ist, wird auf Grundlage analytischer Berechnungen ein neues Modulationsverfahren zur Beseitigung der Leistungspulsation entwickelt. Die analytischen Berechnungen, gestützt durch numerische Analysen, ergeben für den Vier-Port-Betrieb mit dem neuen Modulationsverfahren eine theoretische maximale übertragbare Leistung des DAB-Teils von 8.5 kW. Schaltungssimulationsergebnisse zeigen für einen ac_1/ac_2-Betrieb mit primär- und sekundärseitigen Phasen-

spannungen (Phase zu Neutralleiter) mit Effektivwerten von 230 V bzw. 115 V an ac_1 bzw. ac_2, einer Leistung von 8 kW und deutlich unterschiedliche Netzfrequenzen, $f_1 = 50\,\text{Hz}$ und $f_2 = 77\,\text{Hz}$, dass das hergeleitete Modulationsverfahren die Leistungspulsation nahezu vollständig beseitigt. Insbesondere weisen die Zwischenkreisspannungen $v_{\text{dc},1}$ und $v_{\text{dc},2}$ konstante Werte und die Netzströme sinusförmige Verläufe auf. Da der Betrieb mit $f_1 \neq f_2$ zu einer Erhöhung der Ströme im Umrichter führt, wird die experimentelle Verifikation am Hardwaredemonstrator bei halben Spannungen und somit bei einer reduzierten Leistung von 2 kW durchgeführt. Die Messungen der Zwischenkreisspannungen und Netzströme am Hardwaredemonstrator stimmen gut mit den Simulationsergebnissen überein. Insbesondere die gemessenen Zwischenkreisspannungen $v_{\text{dc},1}$ und $v_{\text{dc},2}$ zeigen nahezu konstante Werte.

In einem abschliessenden Teil der Arbeit werden die Erkenntnisse zur D3ABC-Topologie, die sich im Laufe dieser Arbeit ergeben haben, diskutiert. Eine wichtige Erkenntnis ist zum Beispiel der Kompromiss, der sich aus der Integration der wechselspannungsseitigen Filterinduktivitäten in die für die galvanische Trennung erforderlichen Transformatoren ergibt. Einerseits wird dadurch direkt die Anzahl der magnetischen Komponenten und der Leistungshalbleiterschalter reduziert, gleichzeitig führt die Integration jedoch auch zu Herausforderungen wie einer erhöhten Belastung der Umrichterkomponenten. Die erhöhte Belastung der Komponenten ist vor allem darauf zurückzuführen, dass einige der verbleibenden Komponenten für mehrere Aufgaben gleichzeitig verwendet werden. Da dies allgemein eine integrierte Umrichtertopologie wie den D3ABC kennzeichnet, kann davon ausgegangen werden, dass die aufgeführten Erkenntnisse nicht auf die D3ABC-Topologie beschränkt, sondern charakteristisch für typische Herausforderungen im Zusammenhang mit der Realisierung integrierter Umrichtertopologien sind.

Abbreviations

ac	Alternating Current
CAD	Computer Aided Design
CM	Common Mode
D3AB	Dual Three-Phase Active Bridge
D3ABC	Dual Three-Phase Active Bridge Converter
DAB	Dual Active Bridge
dc	Direct Current
DM	Differential Mode
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FPU	Floating-Point Unit
HF	High-Frequency
LF	Low-Frequency
LISN	Line Impedance Stabilization Network
NPC	Neutral Point Clamped
PC	Polycarbonate
PCB	Printed Circuit Board
PE	Protective Earth
PF	Power Factor
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse Width Modulation
DPWM	Discontinuous Pulse Width Modulation
QP	Quasi-Peak
RMS	Root Mean Square
TF	Transfer Function
THD	Total Harmonic Distortion
VNA	Vector Network Analyzer
VSC	Voltage Source Converter

Contents

1 Introduction

In 1891, a long-distance transmission of electric power over 175 km was presented at the Frankfurt Electrical Exposition. It was one of the main attractions and the catalyst for the commercial implementation of polyphase Alternating Current (ac) transmissions [1, 2]. The German firm Allgemeine Elektricitäts-Gesellschaft (AEG) and the Swiss firm Maschinenfabrik Oerlikon (MFO) designed and built the large-scale experiment under the direction of the chief electricians Mikhail Dolivo-Dobrowolsky (AEG) and Charles Brown (MFO). The transmission employed the three-phase ac system described by Dolivo-Dobrowolsky instead of the Direct Current (dc) or single-phase ac systems that were common at the time. In his description, Dolivo-Dobrowolsky acknowledges the inspirations by Galileo Ferraris, Friedrich August Haselwander, and many other pioneers at the time. This three-phase ac system transmitted a power of almost 300 hp (220 kW) over three 4 mm-thick copper conductors, using three sinusoidal ac currents that were 120 ° phase shifted with respect to each other. A synchronous machine at the hydropower plant in Lauffen generated the electrical power. Three-phase transformers stepped up the voltage in Lauffen to reduce the transmission losses. Another three-phase transformer stepped it down in Frankfurt for final consumption. The system impressed not only with its power and distance, but also with its efficiency and reliability. The great success of this demonstration of the use of three-phase ac systems for electrical power transmission is one of the reasons why three-phase ac systems have prevailed over alternative systems for power transmission in the following years [1].

Although only consistent development made today's grid possible, the three-phase system still forms the basis of the electrical grid. However, over the past decades, several challenges have led to significant changes in the requirements for the grid. According to [3], these include an unprecedented

increase in demand for electrical energy and the need to diversify power generation by integrating renewable energy sources to reduce carbon dioxide emissions. This is compounded by the intermittent and, in many cases, poorly predictable generation of these renewable energies. These requirements are often in contradiction with the capabilities of the existing grid. The existing grid is a strictly hierarchical system in which central power plants at the top of the chain ensure power delivery to customer's loads at the bottom as illustrated in **Fig. 1.1** on the left-hand side. The source has no information about sudden changes in demand, and consequently the grid responds poorly to such changes. The customer, on the other hand, has no information about sudden changes in generation and the related price fluctuations needed to adapt consumption or to provide incentives to feed excess energy back into the grid. The hierarchical structure further makes the grid prone to domino-like failures. According to [3] the next-generation power grid, known as the "smart grid", should address these shortcomings by implementing the measures listed in the following:

- A pervasive control and monitoring of systems based on the exchange of information on energy demand, energy supply, and system state such as active power, reactive power, voltage, current, etc.
- New ways of energy transactions where the customer (stakeholder) can decide whether to buy or sell energy from or to the grid depending on demand and supply.
- Advanced properties, such as self-healing by predicting looming failures based on the system state information and taking corrective actions.

However, due to the sheer size, a grid-wide implementation of these measures is time-consuming and expensive, rendering an immediate implementation in the sense of a revolution to the smart grid not viable. The implementation of smaller grids, so-called (smart) microgrids, however, enables an organic growth and evolution from the existing ac grid to the smart grid of the future. Reference [3] defines microgrids as interconnected local power generators and consumers. These microgrids can operate in stand-alone mode as well as in connection with the existing grid. A microgrid, as shown in Fig. 1.1, provides power to dc and ac loads of local homes and small businesses and enables efficient integration of renewable energy sources such as Photovoltaic (PV) arrays, wind turbines, and/or tidal turbines by combining them with peak shaving energy storage devices such as batteries. Power transmission within the microgrid, as Fig. 1.1 shows, can also employ dc voltages and currents instead of ac voltages and currents. In fact [4–6] argue

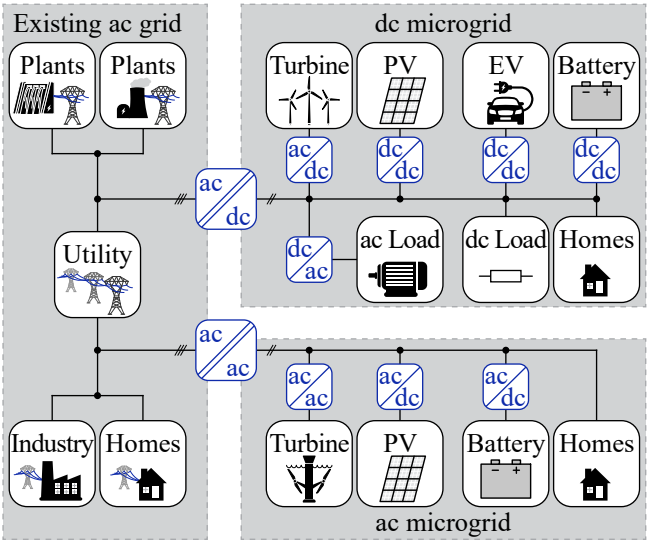

Fig. 1.1: Highly simplified representation of the existing ac grid (shown on the left-hand side, based on Fig. 5 in [3]) and examples for a dc microgrid (top right, based on Fig. 1 in [4]) and an ac microgrid (bottom right). Microgrids are local connections of energy sources, e.g., wind turbines, tidal turbines, and/or Photovoltaic (PV) arrays with dc and ac loads in homes and small businesses combined with peak shaving energy storage devices such as batteries. For internal connections, dc–dc, ac–dc, or ac–ac converters adjust the voltages and currents to ensure high grid quality. The connection of a microgrid to the existing ac grid is achieved by means of a suitable isolated bidirectional power converter.

that dc microgrids are superior to ac microgrids in terms of synchronization, voltage regulation, reactive power flow, efficiency, and system stability. This is partly due to the simpler structures of the converters used in dc microgrids, which promise higher efficiency.[1] The connection of a dc microgrid to the ac smart grid is achieved by means of a suitable bidirectional power converter. These converters ensure that the power quality in the microgrid remains independent of that in the connected smart grid and simplify the realization of island operation [4]. However, compared to other parts of a microgrid, the power converters used today add significantly to the overall cost and are comparatively prone to failures [5]. Future power converters used for this application should therefore be more cost-effective, efficient, reliable, and flexible in terms of controlling power transmission. Possible strategies for reducing costs include reducing the number of components in a converter and using standardized components. To increase efficiency, industrialized implementations of innovative technologies such as wide bandgap semiconductors are necessary. Reliability and continuity of service can be increased by using suitable grounding concepts, as discussed in [7]. These grounding concepts require galvanic isolation between the grid and the microgrid, which is ideally integrated in the power converter by a high-frequency transformer. Finally, converters with multiple power ports increase the flexibility for energy transactions and enable the implementation of innovative concepts, such as the Energy Internet described in [8].

In summary, the power converter for the smart grid of the future is characterized by:

- a small number of components,
- standardized components,
- high efficiency,
- galvanic isolation between grid and microgrid,
- multiple power ports (ac and dc).

[1] Converter topologies for dc–dc conversion are considered simpler than those for ac–dc (or dc–ac) conversion. In the same context, converter topologies for ac–dc conversion are considered simpler than those for ac–ac conversion.

1.1 Existing Converter Topologies

In the following sections, existing topologies for ac–dc converters with integrated galvanic isolation, as shown in Fig. 1.1 between the existing grid and the microgrid, are reviewed. One considered aspect is whether a topology is suitable for bidirectional multi-port operation, i.e., does the topology provide additional dc or ac ports and are there possibilities for expansion with additional dc or ac ports. Another aspect considered is the number of switches used in a topology. Switches are besides possible high unit prices, often associated with additional costs, e.g., for dedicated cooling and additional circuitry such as gate drivers, snubbers, and protection circuits. Therefore, switches often make up a major part of the hardware cost of a converter. It should be noted that, in the discussion presented in this section, the combination of a semiconductor switch with a diode is considered as one switch and single diodes are not counted. The aspects of efficiency and standardized components are not considered further here. The considered topologies are divided into three main groups in this thesis. **Subsection 1.1.1** and **Subsection 1.1.2** give some examples for multi-stage and single-stage converters, respectively. **Subsection 1.1.3** covers the integrated converters to which also the Dual Three-Phase Active Bridge Converter (D3ABC) described in **Subsection 1.1.4** belongs.

1.1.1 Multi-stage converter topologies

A straightforward implementation of an isolated ac/dc converter is as a two-stage or multi-stage converter, consisting of a non-isolated stage rectifying the three-phase ac to dc, followed by one or more isolated dc/dc converters connected in series with the rectifier's dc port. **Fig. 1.2** shows this arrangement with the non-isolated ac–dc converter on the left and the isolated dc/dc converter on the right (the double lines in the converter symbols indicate the isolation). The connection of two (or more) converters forms a dc link with constant voltage or constant current, which is stabilized by an energy storage element. The storage element is usually a capacitor for a voltage dc link as shown in Fig. 1.2(a) or an inductor for a current dc link as shown in Fig. 1.2(b).

Due to high energy storage density of capacitors and negligible leakage losses (compared to the conduction losses) of most used power semiconductors (e.g., MOSFETs, IGBTs, and diodes), the majority of the solutions implement a voltage dc link. Switches for bidirectional voltage dc link topologies usually need to conduct current in both directions but block voltage only

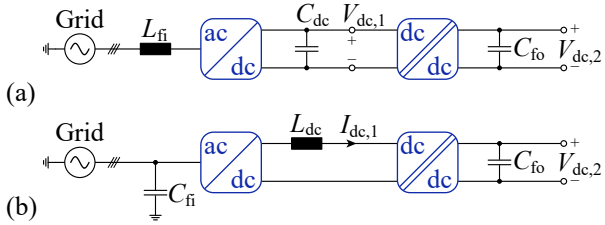

Fig. 1.2: Two-stage converter implementations, consisting of a non-isolated stage on the left-hand side rectifying the three-phase ac voltage to a dc voltage, followed by an isolated dc/dc converter connected in series with the rectifier's dc port on the right-hand side. The double lines in the symbols of the dc/dc converters indicate the isolation. The formed dc link is stabilized by (a) a capacitor for a voltage dc link or (b) an inductor for a current dc link. The capacitor C_{fi} and the inductor L_{fi} refer to components of the input filters and the capacitors C_{fo} refer to components of the output filters.

in one direction. A common realization of these switches is two anti-parallel connected semiconductors (e.g., an IGBT with a diode or a MOSFET with its parasitic body diode as shown in **Fig. 1.3(b)**), whereby in the conducting state only one of the two semiconductors conducts the current (with the exception of synchronous rectification) and in the blocking state the voltage is applied to both semiconductors (counting the anti-parallel diode separately). In comparison, switches for current dc link topologies featuring bidirectional power flow usually need to conduct current in only one direction but block voltage in both directions, i.e., require bipolar switches. A conventional realization of these switches is the inverse-series connection of two semiconductors (e.g., as shown in **Fig. 1.3(c)** and **Fig. 1.3(d)**), whereby in the conducting state both semiconductors conduct the current and in the blocking state the voltage is applied to only one of the two semiconductors. In the case of the MOSFET combined with a diode shown in Fig. 1.3(c), positive voltages are applied to the MOSFET and its parasitic diode and negative voltages appear across the dedicated diode. Consequently, for a given current and given semiconductors, a switch in a current dc link topology has higher, e.g., twice the conduction losses compared to a switch in a voltage dc link topology. However, new technologies such as monolithic bidirectional switches [9] allow the implementation of a bipolar and bidirectional switch (four-quadrant switch) in one semiconductor. Despite continuous development of this technology [10–13], it has only recently been applied in power electronics. Examples are in [14]

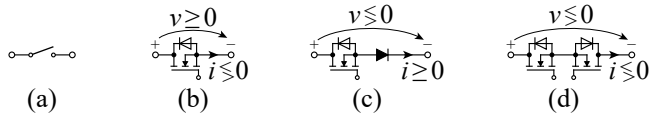

Fig. 1.3: Different possible semiconductor configurations for the implementation of a semiconductor switch. (a) A generic switch, (b) unipolar voltage blocking and bidirectional current conducting switch, (c) bipolar blocking and unidirectional conducting switch, and (d) bipolar blocking and bidirectional conducting (four-quadrant) switch.

for a bidirectional single-phase ac–dc converter, in [15] for a matrix converter, in [16] for a T-type rectifier, and in [17] for an ac–ac converter with current link. However, due to missing availability of monolithic four-quadrant switches with higher voltage blocking capability, this thesis does not consider the technology further.

In the context of voltage dc link multi-stage converters, the most common ac–dc rectifier topology is a two level six-switch Voltage Source Converter (VSC) (three half-bridges as shown in Fig. 1.7(b,c); e.g., used in [18]). Further common implementations include the three-level Neutral Point Clamped (NPC) VSC as in [19] or the VIENNA rectifier [20], which is often implemented as T-type VSC as in [21]. Examples of bidirectional isolated dc/dc converters are, the full-bridge Dual Active Bridge (DAB) converter as used in [18] and shown in **Fig. 1.4(a)**, the half-bridge DAB converter shown in **Fig. 1.4(b)**, and the bidirectional resonant converter used in [22] with LC resonant tank, L_r and C_r, instead of the leakage inductance L_σ shown in Fig. 1.4.[2] In addition, also unidirectional isolated dc/dc converters such as the forward converter (see [23]) and the flyback converter (see [24]) can be considered since in many cases a simple replacement of diodes by switches in these converters allows bidirectional power flow.

An advantage of a multi-stage implementation is the large energy storage capability of the dc link capacitor that decouples the individual converters in terms of power flow and allows an independent operation of each converter stage. Consequently, the number of available power ports can be easily increased by connecting additional converter stages to the dc link. Examples for a respective extension of the number of power ports are shown in [24] for a non-isolated dc port, in [21] for an isolated dc port, and in [25] for a three-phase ac port. However, the components needed for a large energy storage

[2] For the sake of simplicity, these two types of implementation will not be distinguished in the following, and both are referred to as DAB converters.

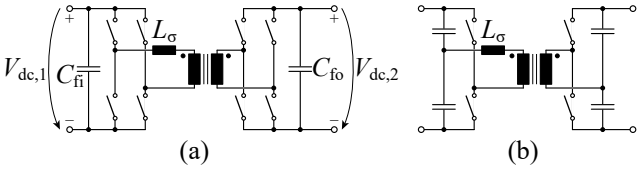

Fig. 1.4: Considered bidirectional isolated DAB converter with primary-side input voltage $V_{dc,1}$, secondary-side output voltage $V_{dc,2}$, and leakage inductance L_σ. (a) Full-bridge DAB implementation and (b) half-bridge DAB implementation.

capability in the dc link are usually associated with high prices, large volume, low reliability, etc. As an example, film capacitors have a high reliability but at the same time a low capacitance value per unit volume. In comparison, electrolytic capacitors have a large capacitance value per price but also a short life expectancy compared to other components of a converter. However, reducing the energy storage capability in the dc link can lead to instabilities in the control as described in [18], which in certain operating scenarios (e.g., a sudden load drop) can lead to overvoltage or overcurrent safety shutdowns and associated service interruptions. To stabilize the control, [18] employs advanced controller structures that require the inclusion of every converter connected to the dc link.

1.1.2 Single-stage converter topologies

Motivated by low price, low volume, and high reliability, literature contains numerous implementations of isolated ac/dc multi-stage converters with reduced dc link energy storage. Since the rectifier stage and the isolation stage are no longer decoupled in these converters, they are referred to as single-stage converters. **Fig. 1.5** shows a diagram of a single-stage implementation able to convert directly from three-phase ac to dc, including isolation. In a single-stage converter, the task of an eventually present dc link capacitance (see C_c in Fig. 1.5) is no longer to stabilize the dc link voltage but rather to provide a low-inductance, High-Frequency (HF) current path to reduce the commutation loop inductance and the associated overvoltage across the switches. Consequently, C_c filters only currents at switching frequency, which allows a significant reduction of the capacitance value.

An example of a common implementation are unfolder-based topologies. The idea of unfolder topologies is based on Power Factor Correction (PFC) diode rectifier topologies with sinusoidal phase currents as the isolated single-

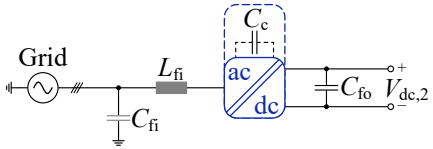

Fig. 1.5: Single-stage converter implementation able to directly convert power from a three-phase ac port to a dc port including isolation (indicated by the double lines). The task of the eventually present dc link capacitance, C_c, is no longer to stabilize the dc link voltage but rather to provide a low-inductance, HF current path inside the converter, to reduce the commutation loop inductance and the associated overvoltage across the switches. The capacitor C_{fi} and the inductor L_{fi} are the components of the input filter and the capacitor C_{fo} is part of the output filter.

phase ac/dc topology presented in [26]. The converter in [26] consists of a passive diode full-bridge stage as shown in **Fig. 1.6(a)** followed by a DAB dc/dc converter. The diodes "fold" the negative half-wave of the ac voltage up, resulting in a strictly positive voltage at the input of the dc/dc converter, allowing the use of unipolar switches. With this arrangement, the diodes and the switches of the subsequently connected dc/dc converter must be designed for a minimum blocking voltage sufficiently higher than the amplitude, $V_{ac,peak}$, of the grid voltage. The input current of the dc/dc converter is then controlled to be proportional to the input voltage of the dc/dc converter, resulting in a sinusoidal current in the grid. In the bidirectional unfolder topology [e.g., the one shown in **Fig. 1.6(b)**], the diodes in the full-bridge are replaced with switches resulting in the single-phase unfolder presented in [27]. The four switches of the unfolder are operated as a synchronous rectifier, i.e., they are switched on for a half grid period like the diodes before and are therefore operated at fundamental frequency of the ac grid voltage. Thus, assuming that the grid frequency is much smaller than the switching frequency used to operate the switches of the dc/dc stage, the switching losses of the switches of the unfolder are negligible.

For the extension of this concept from a single-phase unfolder to a three-phase unfolder, however, a simple three-phase diode rectifier as shown **Fig. 1.7(a)** is not suitable. This is due to the fact that the diodes in a three-phase rectifier are each switched on for only 1/3 of the grid period. Consequently, one phase leg is not conducting current for 1/3 of the grid period, leading to zero phase current intervals in the corresponding phase. Accordingly, the subsequently connected dc/dc converter cannot impress sinusoidal currents in all three phases. One way to overcome this deficiency is to use a current

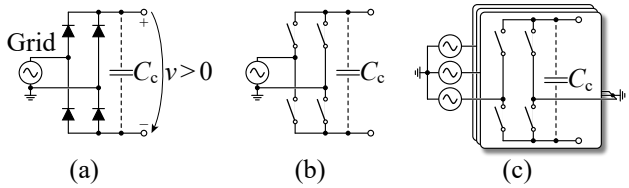

Fig. 1.6: Simplified circuits for (a) a single-phase diode rectifier, (b) a single-phase unfolder, and (c) a phase-modular three-phase unfolder.

injection circuit as shown in the isolated bidirectional Swiss rectifier-like DAB converter described in [28]. The topology in [28] employs 12 switches (6 switches in the three-phase unfolder and 6 switches to form the three bidirectional and bipolar switches of the current injection circuit) that are operated at fundamental frequency and 8 fast-switching switches for realizing the primary-side switching stage of the subsequently connected dc/dc converter.

Another way to implement a three-phase unfolder is a phase-modular approach, i.e., employing a single-phase unfolder as shown in **Fig. 1.6(c)** for each phase (see [29] for a detailed discussion of different possible realizations). However, the phase-modular approach increases the number of fast-switching switches significantly. For example, the isolated bidirectional phase-modular unfolder topology proposed in [30] uses 12 switches in the unfolder and 12 fast-switching switches with a maximum voltage of $V_{\mathrm{ac,peak}}$ to realize the primary-side switching stage of the subsequently connected DAB converter.

Although the switching losses of the unfolders and current injection circuits are negligible, their conduction losses still contribute significantly to the overall losses. In this context, the topology described in [31] avoids the need for an unfolder by adding a Common Mode (CM) offset voltage greater than or equal to the phase voltage amplitude to each phase, resulting in a strictly positive voltage at the input of the subsequently connected dc/dc converter. A small capacitor is placed between the virtual neutral point of the converter and the neutral point of the grid in order to hold the added CM voltage. This bidirectional topology uses the same 12 fast-switching switches to realize the primary-side switching stage of the dc/dc converter, but given the same input ac voltage for the three phases of the grid, the 12 switches must block at least twice the peak value of the grid phase voltage.

An alternative approach for realizing a single-stage ac/dc converter is based on indirect matrix converters. In this regard, the authors of [32, 33] replace the primary-side full-bridge of a DAB converter with the circuit shown

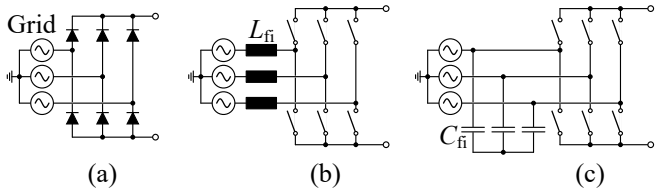

Fig. 1.7: Simplified circuits for three-phase rectifiers. (a) Three-phase diode rectifier. (b) Three half-bridges with inductors, L_{if}, and (c) Three half-bridges with capacitors, C_{if}, as input filter.

in **Fig. 1.7(c)**, using bidirectional and bipolar switches [realized according to in Fig. 1.3(d)], resulting in an isolated bidirectional matrix-type ac/dc converter. The 12 fast-switching primary-side switches are subject to a blocking voltage of $\sqrt{3}V_{\mathrm{ac,peak}}$.

In addition to the unfolder- and matrix-type topologies, numerous further implementations are documented, such as the implementation described in [34] with reduced switch count, the phase-modular interleaved totem-pole implementation described in [35], the phase-modular T-type three-phase DAB converter described in [36], or the nine-switch ac–dc/dc converter described in [37, 38].

In summary, single-stage converters are typically limited with regard to the number of the available ac and dc ports. Most commonly this is because, compared to the multi-stage converters, the primary-side dc link voltage is no longer kept constant and is therefore unusable as dc port. Extending the number of ports by adding more dc/dc converters to the output dc port is possible but comes with the disadvantages of a multi-stage converter.

1.1.3 Integrated converter topologies

An effective way to reduce the number of switches is to use switching nodes for multiple tasks simultaneously as **Fig. 1.8(a)** shows with a simplified single-phase circuit. There, the rectangular voltage v_{n} of the switching node formed by $\mathrm{S_l}$ and $\mathrm{S_h}$, shown in **Fig. 1.8(b)**, is applied to a transformer, which can be used, e.g., together with a secondary-side full-bridge and an output filter capacitor, to form an isolated dc port as shown in gray in Fig. 1.8(a). The same rectangular voltage is also applied to a filter inductor L_{f} that is connected to the grid, to perform the task of a rectifier. The grid current is controlled by adjusting the local average of the voltage at the switching node $\langle v_{\mathrm{n}} \rangle$, which

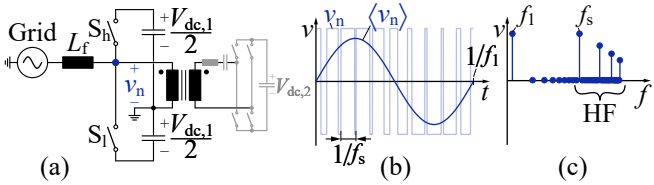

Fig. 1.8: (a) Simplified single-phase circuit that illustrates the use of a switching node formed by S_l and S_h for two tasks simultaneously. The switching is used to control the current in the grid and as a part of a dc/dc converter from $V_{dc,1}$ to $V_{dc,2}$ indicated in gray. (b) Voltage at the switching node in the time domain with switching frequency f_s. The local average of the voltage at the switching node, $\langle v_n \rangle$, has the same frequency as the grid, f_1. (c) Voltage at the switching node in the frequency domain with Low-Frequency (LF) component at f_1 and High-Frequency (HF) components at the switching frequency and above.

is defined as

$$\langle v_n \rangle_{T_s}(t) = \langle v_n \rangle(t) = \frac{1}{T_s} \int_0^{T_s} v_n(t+\tau)\,\mathrm{d}\tau,\ T_s = \frac{1}{f_s}. \tag{1.1}$$

The voltage at the isolated dc port is controlled, e.g., by changing the switching frequency f_s of the switches or the HF phase shift between the rectangular voltages created by the half-bridge on the grid side and the full-bridge on the isolated dc side. The waveform of $\langle v_n \rangle$ corresponds to the waveform of the Low-Frequency (LF) component of v_n at grid frequency f_1, which is separated from the HF components at switching frequency and above in the frequency domain as illustrated in **Fig. 1.8(c)**. Under the assumption $f_s \gg f_1$, the separation in the frequency domain allows the two tasks, i.e., rectification of the grid ac voltage and galvanic isolation using a HF transformer, to be controlled separately even though they are connected to the same switching node.

In literature, numerous solutions use this concept to implement a single-stage multi-port ac–dc/dc converter with an isolated dc port. As an example, the topology described in [39] and shown in **Fig. 1.9(a)** combines a three-phase VSC as shown in **Fig. 1.7(b)** with an isolated LLC dc/dc converter, which uses a single isolation transformer. There the LC resonant tank of the LLC dc/dc converter is split up into three parallel LC resonant tanks. Each input node of the three LC resonant tanks is connected to a switching node of the three-phase VSC. The three output nodes of the LC resonant tanks are connected and to the first primary-side terminal of the isolation

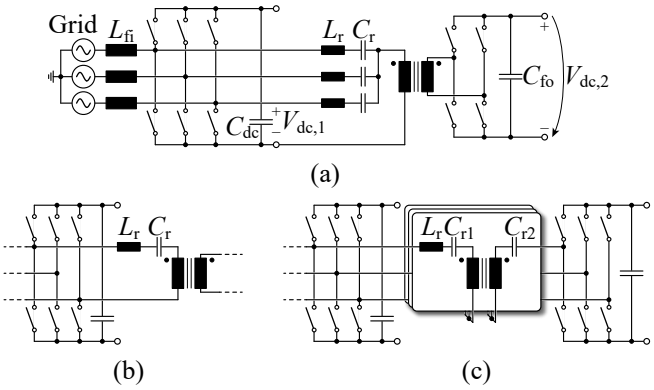

Fig. 1.9: Examples for integrated ac–dc/dc topologies combining an VSC with an isolated LLC dc–dc converter. (a) Topology presented in [39]. (b) Section of the circuit of the topology described in [40] showing an alternative connection of the LLC converter to the VSC. (c) Section of the circuit of the topology described in [41] using three LLC converters. In (c) the capacitor of the LC resonant tank, C_{r}, is split up into two capacitors, C_{r1} and C_{r2}, each placed on one side of the transformer.

transformer of the LLC. The second primary-side terminal of the isolation transformer is connected to the minus terminal of the dc link of the VSC. At the secondary side, a full-bridge converter is used to rectify the HF ac voltage of the transformer. With this arrangement, the CM voltage component created by the three-phase VSC is used for the power transfer to the isolated dc port. The resulting topology requires 10 fast-switching switches. It is very similar to the multi-stage ac–dc/dc converter described in [18], but uses the switches of the three-phase VSC in a combined manner, i.e., to realize three-phase PFC operation and to generate the HF voltage for an isolation transformer, thus saving 4 switches compared to [18]. However, this arrangement has the disadvantage that the Differential Mode (DM) voltage component of the three-phase ac–dc converter drives currents in the resonant tanks that do not contribute to power transfer.

Alternatively, [22, 40] connects the LC resonant tank of a LLC dc/dc converter between the switching nodes of only two half-bridges of a three-phase ac–dc VSC as indicated in the circuit shown in **Fig. 1.9(b)**. Therefore, this arrangement uses the DM part of the voltages of the two half-bridges for the power transfer to the isolated dc port, with the advantage that the CM part does not drive undesired currents in the LLC. However, according to [40],

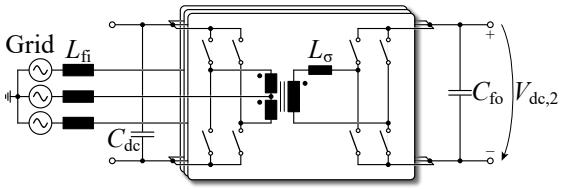

Fig. 1.10: Integrated ac–dc/dc converter topology proposed in [47, 48].

this topology is only suitable for low power due to the asymmetric loading of the half-bridges. The authors of [42] extend this concept by replacing the switches of one phase (phase c in [42]) of the VSC by capacitors, thus forming a split dc link whose midpoint is directly connected to phase b. The proposed implementation with unidirectional power flow requires only four fast-switching switches on the primary side and two HF rectifier diodes on the secondary side. However, this solution can only control the voltage present at one of the two dc ports.

An extreme example with regard to featuring a very low number of switches is the converter presented in [43] that achieves ac-dc/dc operation with only two switches (and 8 diodes), using the ideas of [44] and [45]. However, the solution in [43] can only control the voltage present at one of the two dc ports and the remaining voltage varies depending on the load. Furthermore, due to the diodes used in the rectifier stage and the LLC dc/dc converter, the topology only allows unidirectional power transfer.

In contrast, in the solutions presented in [46] and [41], the three switching nodes of a primary-side VSC are connected to the three LC resonant tanks of a three-phase LLC dc/dc converter as indicated in the circuit shown in **Fig. 1.9(c)**. Besides the three LC resonant tanks, the three-phase LLC dc/dc converter consists of a three-phase transformer in star-star connection and a three-phase rectifier that is connected to the secondary side of the transformer. Both solutions achieve a symmetric loading of the half-bridges and are capable of controlling the voltages at both dc ports (the topologies presented in [46] and [41] allow unidirectional and bidirectional power flow, respectively). However, both solutions require a dedicated three-phase HF transformer.

As an alternative to the three-phase LLC dc/dc converter, three separate LLC dc/dc converters can be used as suggested in [49]. On the primary side, this topology uses one full-bridge for each phase of the three-phase grid. The two switching nodes of each full-bridge are connected to one phase of the three-phase grid via two boost inductors (one from the switching node of

each half-bridge) and to the primary side of one LLC dc/dc converter. The secondary-side dc ports of the three LLC resonant converters are connected in parallel and share a common dc link capacitor. This solution uses 12 switches on the primary side and 6 diodes on the secondary side. However, the secondary-side diodes of the LLC converter would have to be replaced by switches to allow bidirectional power flow. This is realized in the topology described in [47, 48] and shown in **Fig. 1.10**, which uses a full-bridge on both the primary side and the secondary side for each of the three phases. Furthermore, three DAB converters are used instead of three LLC converters. For each phase, the primary-side winding of the DAB transformer is connected to the switching nodes of the respective full-bridge. Furthermore, the primary-side winding has a center tap that is connected to one phase terminal of the three-phase grid via a filter inductor. For power transfer to the secondary side, the secondary-side winding of the DAB transformer of a considered phase is connected between the switching nodes of the secondary-side full-bridge of the same phase. With its two switching nodes, each full-bridge can generate a DM and a CM voltage component. The CM voltage component created by the primary-side full-bridge of each phase is applied to the filter inductor of the same phase, to control the grid current. The power transfer between primary and secondary side is adjusted with a phase shift between the primary-side and secondary-side DM voltage components generated by the full-bridges. The authors of [50] use the CM voltage component generated by the secondary-side full-bridges to add another dc port (giving in total one ac port and three dc ports). The main drawback of this implementation is the high complexity and price of the topology, which requires 24 fast switching switches.

1.1.4 The D3ABC topology

The D3ABC topology shown in **Fig. 1.12** was introduced in [51]. The converter consists of a primary-side and a secondary-side two-level three-phase VSC leading to a total of 12 fast switching switches. In total, six LC filter networks are required between the VSCs and the ac ports, i.e., three on the primary side and three on the secondary side. Three transformers (one for each phase) between the primary and secondary sides enable isolated power transfer similar to three DAB converters. The power transfer over the DAB converters utilizes DM and CM voltage components of the VSCs by connecting the filter capacitors on primary and secondary sides to the mid-points of the respective dc links (C_{f1} and C_{f2} in Fig. 1.12). To reduce the number of magnetic

components, the D3ABC topology integrates the filter inductors of the LC filter networks of the same phase (e.g., primary-side phase a and secondary-side phase A) into the transformer of the DAB converter stage of the same phase. To accomplish this, the ac-side filter inductor of each phase of the primary-side VSC shares the magnetic core with the ac-side filter inductor of the same phase of the secondary-side VSC. The non-ideal coupling of the inductor windings allows galvanically isolated power transfer in each phase. Accordingly, the D3ABC can be regarded as an integration of two three-phase VSCs and three DAB converters. Consequently the D3ABC provides two three-phase ac ports (ac_1 and ac_2), two dc ports (dc_1 and dc_2), and galvanic isolation between the ports ac_1, dc_1 (primary side) and ac_2, dc_2 (secondary side). **Fig. 1.11** illustrates the four ports and the associated converter structures.

Another feature of the D3ABC topology worth mentioning is the arrangement of the two times three half-bridges, each with a dc link. This six-switch arrangement, also used in many of the topologies mentioned above, is very common and due to this, available as a single module. Packing multiple semiconductors into one module allows, for example, easy interfacing of cooling or reduction of the commutation loop inductance and the associated overvoltage across the switches. Both can extend the reliability and lifetime of the semiconductors. It also allows the component to be standardized, which facilitates mass production and thus lowers the unit price.

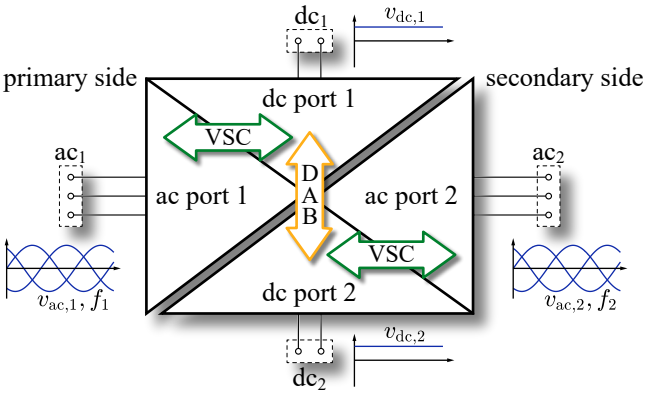

Fig. 1.11: Schematic representation of the D3ABC with two three-phase ac ports (ac_1 and ac_2), two dc ports (dc_1 and dc_2), and galvanic isolation between the ports ac_1, dc_1 (primary side) and ac_2, dc_2 (secondary side). The associated converter structures between ac_1–dc_1 and ac_2–dc_2 are VSCs and dc_1/dc_2 represents a three-phase DAB converter.

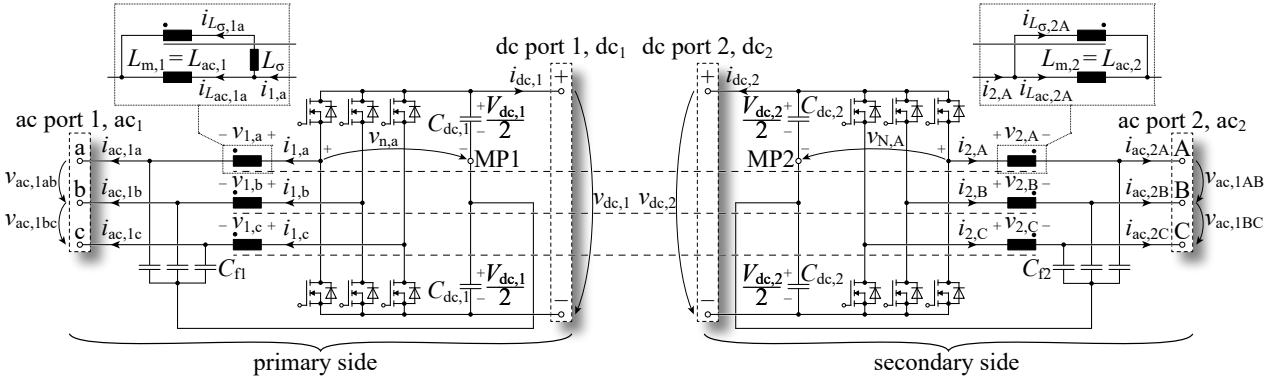

Fig. 1.12: Dual Three-Phase Active Bridge Converter (D3ABC) with primary-side ac and dc ports (ac_1, dc_1) and galvanically isolated secondary-side ac and dc ports (ac_2, dc_2).

1.2 Aims and Contributions

The first introduction of the D3ABC topology in [51] refers to the utilization for isolated ac rectifier operation from the three-phase grid connected to the primary-side ac port ac_1 to a load connected to the secondary-side dc port dc_2. Reference [51] further presents a modulation scheme suitable for rectifier operation that achieves sinusoidal grid currents with PFC. Finally, an efficiency/power density Pareto front is calculated from which a selected point for the design promises a power density $\geq 4\,\mathrm{kW/dm^3}$ and a full load efficiency $> 98\,\%$. The aim of this thesis is to verify the general operation of the D3ABC topology based on experimental results and to fundamentally expand the knowledge base of the D3ABC topology. In particular, this thesis comprises the following main contributions:

- **EMI Filter Design**
  The thesis describes an Electromagnetic Interference (EMI) filter design for conducted EMI noise at the primary-side ac port (ac_1) for ac_1–dc_1/dc_2 rectifier operation of the D3ABC. For this purpose, equivalent circuits for modeling the DM and CM EMI noise emissions are derived, which take converter component values as well as dependencies of the EMI noise components on the loads connected to the two dc ports (dc_1 and dc_2) into account. The derived models are based on data sheet values and use simplified equivalent circuits to estimate parasitic effects, which allows EMI filter optimization at an early stage of converter design.

- **Four-Port Operation**
  The thesis describes the operation of the D3ABC topology as an ac_1–dc_1/dc_2–ac_2 four-port converter. For this purpose, an advanced modulation scheme for the elimination of LF power pulsations is derived. The modulation scheme described allows operation with different line frequencies and amplitudes of the three-phase voltages at the two ac ports (ac_1 and ac_2) with power levels comparable to the ac_1/dc_2 operation.

- **Hardware Demonstrator**
  The thesis verifies the functionality of the D3ABC topology by measurements on a hardware demonstrator. In addition, all concepts derived in this work are verified by measurements on this hardware demonstrator.

1.3 Thesis Outline

According to the aims and contributions mentioned above, the thesis divides the core content into two chapters and a conclusion. Both chapters can be read independently since the interdependencies have been reduced to a strict minimum. The chapters contain the following:

- **Chapter 2**
  First, a simplified equivalent circuit of the D3ABC is derived which allows a comprehensive explanation of the operation of the converter. Based on this, the EMI noise sources and their main propagation paths are modeled. The model is used to design an ac-side volume optimized EMI filter for ac/dc operation. Measurements on the hardware demonstrator verify that the conducted EMI noise of the converter with the designed filter complies with the Quasi-Peak (QP) limit defined in CISPR 11 class A. This chapter is based on [52].

- **Chapter 3**
  The operating principle of the D3ABC is extended for operation as ac_1–dc_1/dc_2–ac_2 four-port converter. For this purpose, an advanced modulation scheme for the operation with different frequencies and amplitudes of the voltages at the two three-phase ac ports and the elimination of LF power pulsations related to this operation, is derived. The derived modulation scheme is verified by means of circuit simulations and measurements on the hardware demonstrator. This chapter is based on [53, 54].

- **Chapter 4**
  The final chapter summarizes the core findings of this thesis. These are complemented by a description of the general challenges of integrated topologies such as D3ABC that have occurred in the course of this thesis. These challenges of integrated topologies used in the smart grid of the future provide the ground for possible future research projects.

At this point it should be noted that in this thesis the specified power for the hardware demonstrator varies. Nevertheless, all measurements use the same hardware which is designed for ac_1/dc_2 rectifier operation with a power of 8 kW at dc_2. The EMI filter was designed for 2/3 of the power at dc_1 and 1/3 at dc_2. However, for practical reasons, the powers were rounded to 5 kW and 2.5 kW resulting in a total power of 7.5 kW. Finally, the power for measurements for four-port operation were reduced from 8 kW to 2 kW to prevent an overcurrent in the hardware components.

1.4 List of Publications

Key parts of this thesis have been published in international scientific journals or in the proceedings of main international conferences. The publications created as part of this thesis, or also in the scope of other related research projects, are listed below.

1.4.1 Journal papers

- M. J. Heller, F. Krismer, and J. W. Kolar, "EMI filter design for the integrated dual three-phase active bridge (D3AB) PFC rectifier," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14527–14546, Dec. 2022, DOI: 10.1109/TPEL.2022.3195343.

- M. J. Heller, F. Krismer, and J. W. Kolar, "Duty-cycle dependent phase shift modulation of dual three-phase active bridge four-port AC–DC/DC–AC converter eliminating low frequency power pulsations," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 705-722, Oct. 2022, DOI: 10.1109/OJPEL.2022.3213274.

1.4.2 Conference papers

- M. J. Heller, F. Krismer, and J. W. Kolar, "Modulation scheme optimization for a dual three-phase active bridge (D3AB) PFC rectifier topology," *in Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto (ON), Canada, Jun. 2019, DOI: 10.1109/COMPEL.2019.8769627.

- M. J. Heller, F. Krismer, and J. W. Kolar, "Quad-port AC–DC/DC–AC operation of isolated dual three-phase active bridge converter," *in Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix (AZ), USA, Jun. 2021, DOI: 10.1109/APEC42165.2021.9487240.

1.4.3 Further scientific contributions

- M. Guacci, M. J. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the origin of the C_{OSS}-losses in soft-switching GaN-on-Si power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679-694, May 2016, DOI: 10.1109/JESTPE.2018.2885442.

- D. Menzi, D. Bortis, G. Zulauf, M. J. Heller, and J. W. Kolar, "Novel iGSE-C loss modeling of X7R ceramic capacitors," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13367-13383, Dec. 2020, DOI: 10.1109/TPEL.2020.2996010.
- O. Raab, M. Guacci, A. Griffo, K. Kriegel, M. J. Heller, J. Wang, D. Bortis, M. Schulz, and J. W. Kolar, "Full-SiC integrated power module based on planar packaging technology for high efficiency power converters in aircraft applications," *in Proc. of the International Conference on Integrated Power Electronics Systems (CIPS)*, Berlin, Germany, Mar. 2020, DOI: not available.
- D. Menzi, M. J. Heller, and J. W. Kolar, "iGSE-C_X – A new normalized Steinmetz model for class II multilayer ceramic capacitors," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 138-144, Feb. 2021, DOI: 10.1109/OJPEL.2021.3060874.

2

EMI Filter Design for the D3ABC

Chapter Abstract

This chapter first gives a comprehensive description of the operating principle of the D3ABC for ac_1–dc_1/dc_2 rectifier operation. Based on this description, it derives a model for calculating the conducted EMI noise at the primary-side ac port of the D3ABC PFC rectifier. At the operating point considered, the D3ABC rectifies 7.5 kW from a three-phase grid with an Root Mean Square (RMS) value of 230 V of the line-to-neutral voltages and generates output dc voltages of $V_{dc,1} = 800\,V$ and $V_{dc,2} = 400\,V$ at the two dc ports. The EMI model takes the implications of the power levels provided at the primary-side and secondary-side dc ports, P_1 and P_2, respectively, on the conducted EMI noise into account and is used to design an ac-side EMI filter for a hardware demonstrator of the D3ABC topology that is volume-optimized for the considered specifications. The designed filter has a volume of $0.17\,dm^3 = 10.4\,in^3$ ($0.09\,dm^3 = 5.5\,in^3$ for the DM filter and $0.08\,dm^3 = 4.9\,in^3$ for the CM filter part). As part of the experimental verification of the model, the conducted EMI noise of the hardware demonstrator is measured under two different workload scenarios, i.e., $P_1 = 4\,kW$, $P_2 = 2.5\,kW$ and $P_1 = 0$, $P_2 = 6.5\,kW$. Measurements show that the level of conducted EMI noise increases with increasing load on the secondary side, which is consistent with the predictions of the noise model. The hardware demonstrator combined with the EMI filter complies with the CISPR 11 class A QP conducted EMI limit.

Tab. 2.1: Converter specification for the considered operating point.

Ac line voltage (phase-to-neutral, RMS)	$V_{\mathrm{ac1,rms}} = 230\,\mathrm{V}$
Ac line frequency	$f_1 = 50\,\mathrm{Hz}$
Primary-side dc link voltage	$V_{\mathrm{dc,1}} = 800\,\mathrm{V}$
Secondary-side dc link voltage	$V_{\mathrm{dc,2}} = 400\,\mathrm{V}$
Maximum total power	$P_1 + P_2 = 7.5\,\mathrm{kW}$
Primary-side power	$P_1 = 5\,\mathrm{kW}$
Secondary-side power	$P_2 = 2.5\,\mathrm{kW}$

2.1 Introduction

In this chapter, the D3ABC is considered as a three-phase PFC rectifier system which provides two independent dc voltages at its dc ports (cf. **Fig. 2.1**). This is required, for example, for the direct supply of a high power drive system (5 kW, 800 V) and a galvanically isolated dc distribution system powering auxiliaries (2.5 kW, 400 V) and is investigated in this chapter. **Table 2.1** summarizes the main specifications considered for the rectifier operation.

This chapter focuses on the analysis of conducted EMI in the D3ABC. The main aim is to derive an EMI model that provides insights into the origins of the EMI noise at the primary-side ac port (ac_1), taking the dependencies on the values of the converter components as well as the loads connected to the two dc ports into account. Furthermore, the derived EMI model should be suitable for filter optimization. In this regard, e.g., a converter optimization according to [51] can be complemented by the optimization of the EMI filter. **Section 2.2** describes the derivation of a simplified equivalent circuit, which enables a comprehensible explanation of the converter's operating principle. **Section 2.3** details the modeling of the EMI noise sources and the derivation of the electrical networks that describe the main propagation paths of conducted EMI noise. In this context, a model is developed that can be meaningfully used even during the design phase of the converter, when only few measurement data are available. On the basis of this modeling, **Section 2.4** describes the design of an EMI filter that is volume-optimized for the considered specifications, i.e., for defined limitations of conducted EMI and defined safety margins for DM and CM EMI noise. Finally, **Section 2.5** discusses the results of the experimental verification for two selected workload scenarios. A volume-optimized hardware demonstrator of the D3ABC with a total power density of $4.1\,\mathrm{kW/dm^3} = 67.4\,\mathrm{kW/in^3}$ is used for the experimental verification. Measurement results of the conducted EMI noise

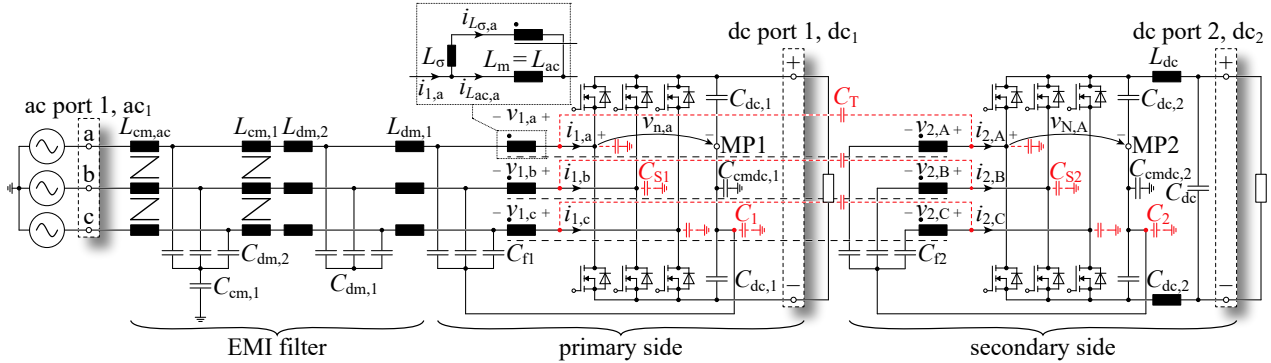

Fig. 2.1: Topology of the Dual Three-Phase Active Bridge Converter (D3ABC) PFC rectifier shown with EMI filter on ac port 1 (ac_1). The parasitic capacitances between the switching nodes and earth, the dc link mid-points and earth, and between the primary-side and secondary-side coils of the coupled boost inductors (transformers) are shown in red color.

show that the realized converter complies with the QP limit defined in CISPR 11 class A for operation according to Table 2.1.

2.2 Operating Principle for ac_1–dc_1/dc_2 Rectifier Operation

Due to the highly integrated character of the D3ABC topology, an overall analysis of the entire system would be relatively complex. However, this is not required, because the D3ABC can be separated into different functional parts, which allows a substantial simplification of the analysis. That separation is explained in this section and comprises the steps listed as follows.

1. The decoupling of the three-phase system into *three independent single-phase circuits* (**Subsection 2.2.1**).

2. The separation into *ac–dc operation without galvanic isolation*, i.e., on the primary side and on the secondary side, and *dc/dc operation with galvanic isolation* between the primary-side and secondary-side dc ports (**Subsection 2.2.2**).

2.2.1 Independent single-phase circuits

With the assumption of symmetric line voltages, defined as

$$v_{\mathrm{ac,a,b,c}}(t) = V_{\mathrm{ac1,peak}} \sin\left(2\pi f_1 t + \theta_{\mathrm{a,b,c}}\right), \tag{2.1}$$

$$V_{\mathrm{ac1,peak}} = \sqrt{2} V_{\mathrm{ac1,rms}},\ \theta_{\mathrm{a,b,c}} \in \{0^\circ, 120^\circ, 240^\circ\}, \tag{2.2}$$

line frequency f_1, and a modulation without LF CM voltage (e.g., third harmonic injection), the mid-point of the primary-side dc link, MP1, is on the same potential as the line star point. Furthermore, the D3ABC topology employs no CM filter inductors directly in series to the coupled boost inductors (L_{ac}, L_σ in Fig. 2.1). For these reasons, the three phases of the D3ABC without EMI filter, i.e., the parts of the circuit depicted in Fig. 2.1 that are marked with the curly braces referring to *primary side* and *secondary side*, can be separated into three single-phase circuits as shown in **Fig. 2.2(a)** where MP1 is connected to the line star point. There, the single complex impedance Z_{EMI} approximates the impedance of the EMI filter between the converter and the mains. The voltage source, v_{ac}, refers to one of the three phase voltages of the mains.

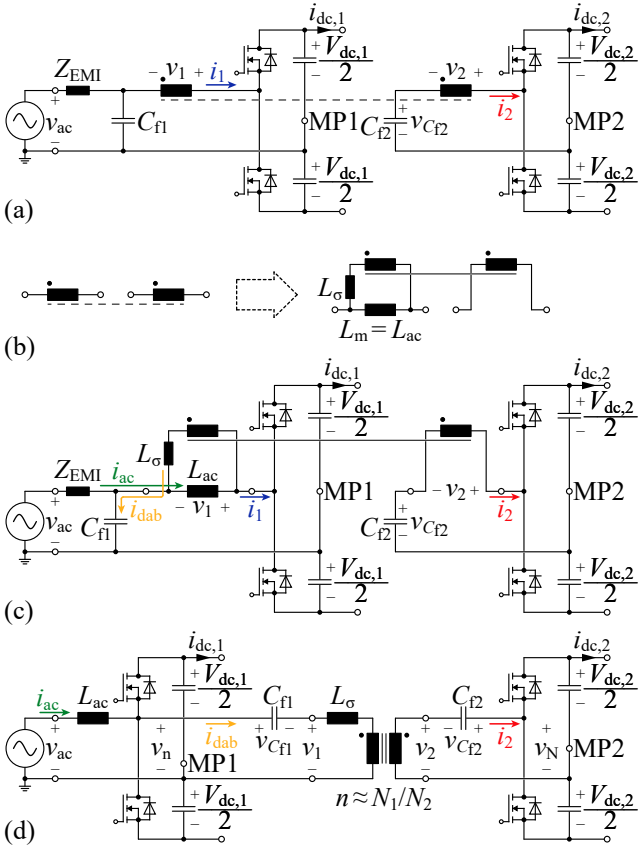

Fig. 2.2: Derivation of the single-phase equivalent circuit with decoupled circuits for ac_1–dc_1 and dc_1-dc_2 operations: (a) single phase of the D3ABC depicted in Fig. 2.1; (b) equivalent circuit of the transformer; (c) circuit of (a) with the transformer being replaced according to (b); (d) final equivalent circuit with separated junctions for the LF and HF components of the input current at the switching node of the considered primary-side half-bridge.

2.2.2 Separation of ac–dc and dc/dc operation

In a first step, it needs to be analyzed whether the power conversion between ac port 1 and dc port 1 (referred to as ac_1–dc_1 operation) and the power conversion between dc port 1 and dc port 2 (dc_1/dc_2 operation) can be considered separately. For this purpose, the spectrum of the active power at the switching node of the single-phase equivalent circuit depicted in Fig. 2.2(a), $P_1(f)$, is analyzed for a typical operating condition. The calculation of $P_1(f)$ for a given frequency f requires the phasor of the voltage, $\underline{V}_\mathrm{n}(f)$, and the complex conjugated phasor of the current, $\underline{I}_1^*(f)$, at the switching node,

$$P_1(f) = \Re\left[\underline{V}_\mathrm{n}(f)\underline{I}_1^*(f)\right]. \tag{2.3}$$

These phasors are determined from the corresponding time-domain waveforms. **Fig. 2.3(a)** shows example waveforms for v_n and i_1, which have been calculated for the ac_1/dc_2 operation as described in [51] with a switching frequency of $f_\mathrm{s} = 6\,\mathrm{kHz}$ (low switching frequency for the purpose of illustration). The calculation uses the voltages and frequency specified in Table 2.1, an output power of 7.5 kW at port dc_2, $2\pi f_\mathrm{s} L_\mathrm{ac} \approx 29.5\,\Omega$, $2\pi f_\mathrm{s} L_\sigma \approx 19.6\,\Omega$, and $n = 2.6$. Sinusoidal lines in Fig. 2.3(a) correspond to the local average values over one switching period. The local average value of v_n is calculated by integration of the instantaneous value,

$$\langle v_\mathrm{n}\rangle_{T_\mathrm{s}}(t) = \langle v_\mathrm{n}\rangle(t) = \frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} v_\mathrm{n}(t+\tau)\,\mathrm{d}\tau, \tag{2.4}$$

and $\langle i_1\rangle$ is calculated in the same way. Local average values $\langle v_\mathrm{n}\rangle$ and $\langle i_1\rangle$ highlight the LF components below switching frequency in the waveforms and illustrate that only a component at line frequency, $f_1 = 50\,\mathrm{Hz}$, is present.

Fig. 2.3(b) depicts the spectrum of the power in one phase calculated with (2.3), using the same settings as in Fig. 2.3(b), except for a higher switching frequency of 35 kHz. According to this result, the power transfer can be separated into a LF part at $f = 50\,\mathrm{Hz}$ with positive power (primary-side half-bridge consumes energy) and a HF part for $f \geq 35\,\mathrm{kHz}$ with negative power (primary-side half-bridge provides energy). The LF part of the spectrum, illustrated with the local average values $\langle v_\mathrm{n,a}\rangle$ and $\langle i_\mathrm{1,a}\rangle$ in Fig. 2.3(a), refers to a three-phase PFC rectifier operation without galvanic isolation from ac_1 to dc_1. The HF part of the spectrum achieves dc/dc power conversion with galvanic isolation from dc_1 to dc_2.

According to this result, a separation of the analysis for the ac_1–dc_1 and the dc_1/dc_2 operation is feasible, provided that f_s is several orders of magnitude

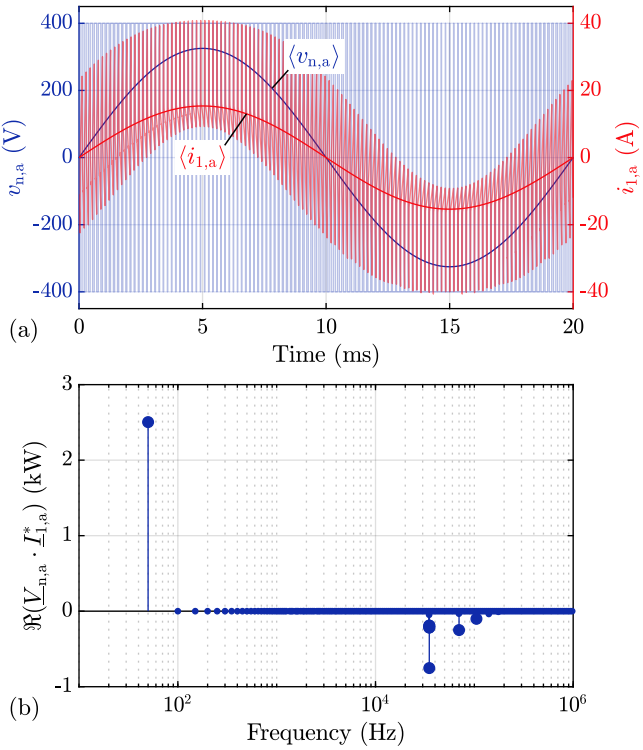

Fig. 2.3: (a) Waveforms of $v_n(t)$ and $i_1(t)$, defined in the single-phase circuit of Fig. 2.2(a), over a line period of 20 ms. For the purpose of illustration, the waveforms have been determined for a reduced switching frequency of $f_s = 6$ kHz. The shown sinusoidal characteristics, $\langle v_{n,a} \rangle$ and $\langle i_{1,a} \rangle$, refer to the local average values of the instantaneous values of $v_n(t)$ and $i_1(t)$. (b) Spectrum of the active power at the switching node of the primary-side half-bridge of a single phase, for a switching frequency of $f_s = 35$ kHz. The waveforms and the spectrum are calculated for the ac–dc operation described in [51] with the voltages and the mains frequency specified in Table 2.1, an output power of $P_2 = 7.5$ kW at dc$_2$, $2\pi f_s L_{ac} \approx 29.5\,\Omega$, $2\pi f_s L_\sigma \approx 19.6\,\Omega$, and $n = 2.6$.

higher than the line frequency f_l at ac_1. Therefore, the single-phase equivalent circuit is further modified, to clearly reveal this separation. In a first step, the coupled boost inductor (which can be considered like a transformer), is replaced by the equivalent circuit shown in **Fig. 2.2(b)**. This circuit consists of a magnetizing inductance L_m, a stray inductance L_σ, and an ideal HF transformer with a given turns ratio,

$$n \approx N_1/N_2. \tag{2.5}$$

The circuit resulting after this replacement is shown in **Fig. 2.2(c)**. In a final step, the paths for the LF current i_{ac} and the HF current i_{dab}, highlighted in Fig. 2.2(c), are separated. This final step is based on the results obtained for the frequency spectrum of the power depicted in Fig. 2.3(b) and denotes an approximation that is only valid if the assumptions listed below are met.

1. At line frequency of, e.g., $f_l = 50\,\text{Hz}$, it is assumed that the capacitances C_{f1} and C_{f2} and the capacitances in the EMI filter feature comparably high impedances and can be approximated by open circuits. Furthermore, all inductances feature very low impedances and can be replaced by short circuits in a first approximation. Based on these considerations, the LF component of i_{ac} passes through the line voltage source, v_{ac}, the magnetizing inductance, $L_m = L_{ac}$, and the half-bridge.

2. With regard to HF voltage and current components, it is assumed that the impedance of C_{f1} is much lower than the impedances of Z_{EMI} and L_{ac}. Accordingly, the HF current i_{dab} is mainly conducted from the switching node of the primary-side half-bridge through the transformer (the secondary-side dc link capacitance $C_{dc,2}$ and filter capacitance C_{f2}), the stray inductance L_σ, and the filter capacitance C_{f1}.[1]

Consequently, the junction connecting Z_{EMI}, C_{f1}, L_{ac}, and L_σ can be split into two junctions: the first junction connects Z_{EMI} to L_{ac} and the second junction connects L_σ to C_{f1}. Furthermore, the Z_{EMI} value is usually much lower than the impedance of L_{ac} and can be neglected. With this, the equivalent circuit depicted in **Fig. 2.2(d)** results, which is similar to the circuit described in [55, 56]. The derived circuit allows to separately analyze the conversion mechanisms that are relevant for the operation as rectifier (ac_1–dc_1) and isolated dc/dc converter (dc_1/dc_2). In addition, this figure points out that the magnetizing inductance, L_m, acts as boost inductance, L_{ac}, for ac_1–dc_1 operation.

[1] For simplicity, the triangular HF current in the boost inductance L_{ac} is neglected in this section, since it does not transfer active power.

Ac–dc conversion without isolation

According to Fig. 2.3, the local average values of v_n and i_1 are approximately sinusoidal with a frequency equal to the line frequency. Since Z_{EMI} and L_{ac} can be approximated by a short circuit at line frequency, the local average values of the voltages across this components are negligible,

$$\langle v_{Z\mathrm{emi}} \rangle \approx 0, \ \langle v_{L\mathrm{ac}} \rangle \approx 0. \tag{2.6}$$

For this reason, the voltage across the filter capacitor C_{f1} is approximately equal to the line voltage. Furthermore, the primary-side half-bridge must be controlled such that the local average voltage at the switching node, $\langle v_n \rangle$, is approximately equal to the voltage across C_{f1},

$$\langle v_n \rangle = \left(D_1 - \frac{1}{2} \right) V_{\mathrm{dc,1}} \approx v_{C\mathrm{f1}} \approx v_{\mathrm{ac}}. \tag{2.7}$$

Based on (2.1), (2.2), and (2.7), the duty cycles of the three primary-side half-bridges result,

$$D_{1,\mathrm{a,b,c}}(t) \approx \frac{1}{2} \left[1 + m_1 \sin \left(2\pi f_1 t + \theta_{\mathrm{a,b,c}} \right) \right], \tag{2.8}$$

using the modulation index $m_1 = 2V_{\mathrm{ac1,peak}}/V_{\mathrm{dc,1}}$. A controller slightly adjusts the duty cycles of (2.8) in order to achieve PFC rectifier operation with defined active and reactive power levels on the primary side as it is known for VSCs operated as PFC rectifiers.

Dc/dc conversion with isolation

The converter's dc/dc part represents a DAB converter with primary-side and secondary-side half-bridge circuits (e.g., as proposed in [57]). Due to (2.8), each primary-side half-bridge is operated with a time-varying duty cycle to achieve PFC rectifier operation. Furthermore, the basic modulation scheme of the D3ABC uses same duty-cycles, $D_1 = D_2 = D$, and the same switching frequency, f_s, for the primary-side and secondary-side half-bridges.

According to Fig. 2.2(d), the difference between the voltage at the switching node of the primary-side half-bridge, v_n, and the filter capacitance $v_{C\mathrm{f1}}$ is applied to the primary side of the transformer,

$$v_1 = v_n - v_{C\mathrm{f1}}. \tag{2.9}$$

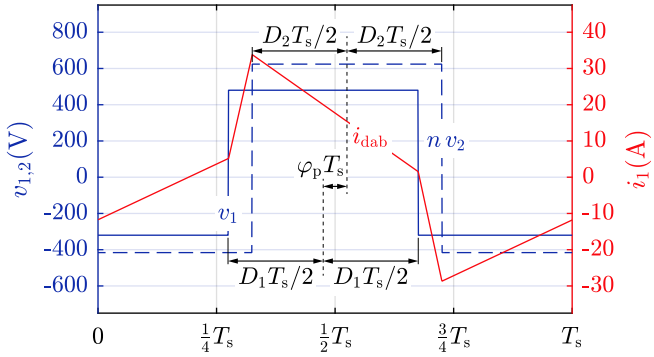

Fig. 2.4: Definitions of D_1, D_2, and HF phase shift φ_p[2], illustrated based on waveforms that have been calculated for one switching period, T_s, with $2\pi f_s L_\sigma \approx 19.6\,\Omega$, $n = 2.6$, $V_{dc,1} = 800\,V$, $V_{dc,2} = 400\,V$, $\varphi_p = \frac{\varphi}{2\pi} = 0.05$, and $D_1 = D_2 = 0.4$.

The same applies to the secondary side,

$$v_2 = v_N - v_{Cf2}, \tag{2.10}$$

where v_{Cf2} is determined similar to the primary side, i.e., the voltage across the secondary-side filter capacitor C_{f2} is approximately equal to the LF component of the voltage at the switching node of the secondary-side half-bridge,

$$v_{Cf2} \approx \langle v_N \rangle = \left(D_2 - \frac{1}{2}\right) V_{dc,2}, \tag{2.11}$$

in order to prevent saturation of the transformer. The difference between v_1 and $n\,v_2$ is applied to the transformer's stray inductance, L_σ, and causes a change of the inductor current, i_{dab}. The HF phase shift, φ_p[2], between the rectangular transformer voltages $v_1(t)$ and $v_2(t)$, as defined in **Fig. 2.4**, is used to control the power transferred between dc_1 and dc_2 [51],

$$P_{dc1-dc2} = \frac{nV_{dc,1}V_{dc,2}}{2f_sL_\sigma}\varphi_p\left(2D(1-D) - |\varphi_p|\right). \tag{2.12}$$

[2] To make the formulas easier to read, the relative phase shift $\varphi_p = \frac{\varphi}{2\pi}$ is used.

2.3 Noise Model of the D3ABC

An EMI model that can be used in the design phase is typically a mixture of physical and behavioral component models,[3] as presented, for example, in [61–63]. Procedures described therein propose the identification of the main sources of EMI noise, separation into DM and CM EMI noise components, and identification of main propagation paths of DM and CM EMI noise. Depending on availability, the parameterization of the model can be based on data sheet values, simulations, or measured data. Based on this, the attenuation of DM and CM EMI noise required to comply with EMI regulations can be determined. The required attenuation enables the design of a suitable EMI filter, which is typically optimized based on a certain cost function, e.g., minimum filter volume, while meeting certain constraints (e.g., maximum current ripple and maximum reactive power at line frequency) [64–66].

In the following, a complete EMI noise model of the D3ABC, i.e., valid for DM and CM EMI noise, is determined. This is used in a subsequent step to derive the DM and CM EMI noise models in **Subsection 2.3.1** and **Subsection 2.3.2**, respectively.

The six half-bridges represent the EMI noise source of the D3ABC topology. Based on the assumption of constant dc link voltages, each half-bridge can be replaced by a voltage source with a rectangular output voltage waveform similar to the voltage at the switching node of the half-bridge shown in Fig. 2.3(a), i.e., $v_{\mathrm{n,a}}$, $v_{\mathrm{n,b}}$, and $v_{\mathrm{n,c}}$ on the primary side and $v_{\mathrm{N,A}}$, $v_{\mathrm{N,B}}$, and $v_{\mathrm{N,C}}$ on the secondary side. These voltages are further divided into two CM voltage sources,

$$\begin{aligned} v_{\mathrm{cm},1} &= \frac{v_{\mathrm{n,a}} + v_{\mathrm{n,b}} + v_{\mathrm{n,c}}}{3}, \\ v_{\mathrm{cm},2} &= \frac{v_{\mathrm{N,A}} + v_{\mathrm{N,B}} + v_{\mathrm{N,C}}}{3}, \end{aligned} \tag{2.13}$$

for primary side and secondary side, respectively, and six DM voltage sources,

$$\begin{aligned} v_{\mathrm{dm},1,\mathrm{a,b,c}} &= v_{\mathrm{n,a,b,c}} - v_{\mathrm{cm},1}, \\ v_{\mathrm{dm},2,\mathrm{A,B,C}} &= v_{\mathrm{N,A,B,C}} - v_{\mathrm{cm},2}. \end{aligned} \tag{2.14}$$

[3] Behavioral models are parameterized on the basis of measured data and allow accurate predictions of conducted EMI [58–60]. However, the necessity of having comprehensive measurement data is in contradiction to the initial situation of a converter development, during which usable measurement data is only available to a limited extent. In contrast, physical models are based on component-specific physical interrelationships and hence rely, e.g., on material data and component geometries. Such models, though, are often highly simplified and therefore less accurate than behavioral models.

At this point it is to be noted that the three primary-side half-bridges and the three secondary-side half-bridges are operated with interleaving, i.e., the carrier signals of the Pulse Width Modulation (PWM) units are phase-shifted to each other by 120 °.[4] Waveforms for the primary-side DM and CM voltages, $v_{\mathrm{dm},1}$ and $v_{\mathrm{cm},1}$, calculated according to Subsection 2.3.3 and the respective local average values $\langle v_{\mathrm{dm},1,\mathrm{a}} \rangle$ and $\langle v_{\mathrm{cm},1} \rangle$ are shown in **Fig. 2.5(a)** (using a low switching frequency of 6 kHz for the purpose of illustration). The average value of $\langle v_{\mathrm{cm},1} \rangle$ is zero, i.e., no LF CM voltage is injected with this modulation scheme. The spectra of these voltages (for $f_{\mathrm{s}} = 35\,\mathrm{kHz}$) are shown in **Fig. 2.5(b)**.[5]

Replacing the half-bridges in Fig. 2.1 by the voltage sources that model the CM and DM voltage components defined in (2.13) and (2.14) and omitting the EMI filter components (i.e., the EMI filter, $C_{\mathrm{cmdc},1}$, and $C_{\mathrm{cmdc},2}$) results in the circuit depicted in **Fig. 2.6**. The inclusion of twice the dc link capacitance on the primary and secondary sides, $2C_{\mathrm{dc},1}$ and $2C_{\mathrm{dc},2}$, between the mid-points and the CM voltage sources is explained in more detail in **Appendix C**. The EMI filter is not part of Fig. 2.6, since the EMI noise models derived in this Section are the basis for the EMI filter design in Section 2.4. In order to characterize the HF EMI noise with a defined line impedance, a three-phase ac Line Impedance Stabilization Network (LISN) is placed between the converter and the three-phase ac line. According to [67], the simplified network of the LISN consists of three inductors, three capacitors, and three resistors, i.e., $3 \times 50\,\mu\mathrm{H}$, $3 \times 250\,\mathrm{nF}$, and $3 \times 50\,\Omega$, respectively, as shown in Fig. 2.6. The line voltage sources are approximated by short circuits with regard to HF EMI noise.

[4] With this, the CM voltage component at $f = f_{\mathrm{s}}$ is reduced by 11.5 dB (at the cost of an increase of the DM component at $f = f_{\mathrm{s}}$ by 6.8 dB). This significantly reduces parasitic ringing that may occur in the CM equivalent circuit (derived in Subsection 2.3.2 and depicted in Fig. 2.8(c)) at $f = f_{\mathrm{s}}$ due to the relatively small dc link capacitances, $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$, cf. Table 2.2 in Section 2.4.

[5] Compared to the primary side, the secondary-side voltages have the same shape and a different amplitude (the secondary-side dc link voltage is half of the primary-side dc link voltage) and are phase-shifted by the HF phase-shift, φ_{p}.

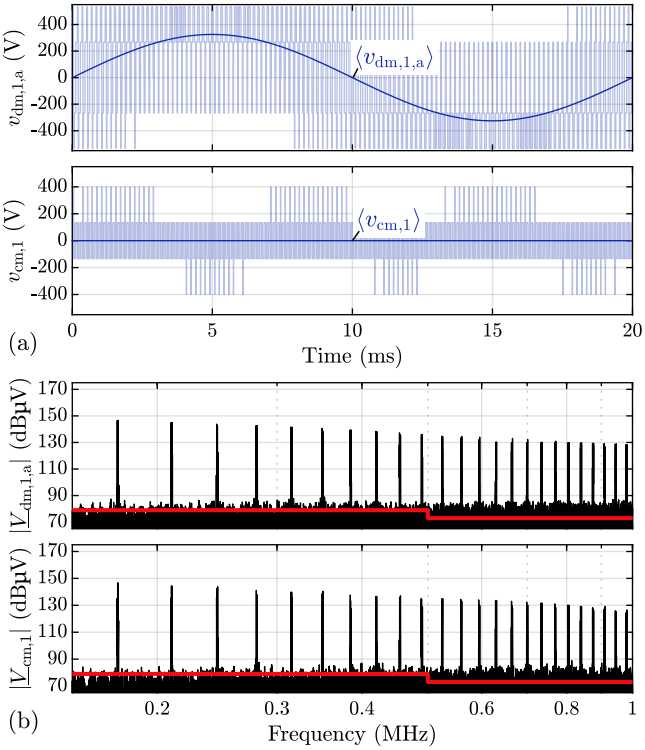

Fig. 2.5: Illustration of the DM and CM voltage components: (a) in time domain for a switching frequency of 6 kHz (low switching frequency for the purpose of illustration) and (b) in frequency domain for a switching frequency of 35 kHz and for the operating conditions specified in Table 2.1.

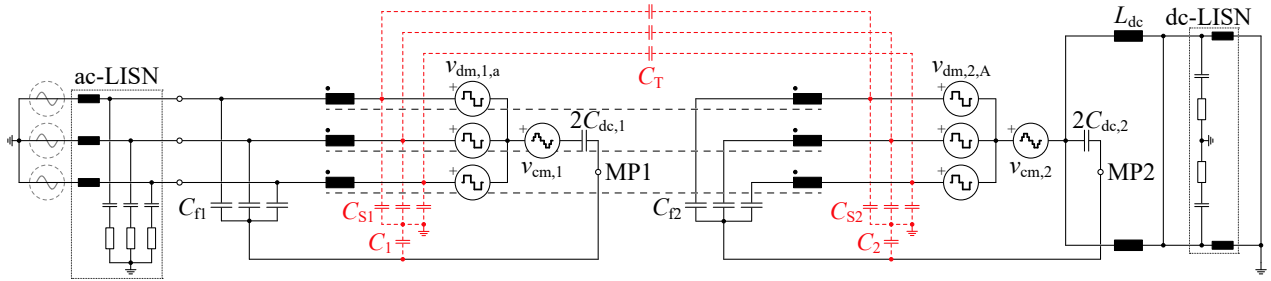

Fig. 2.6: The D3ABC topology (without EMI filter part) with the half-bridges being replaced by voltage sources that model DM and CM EMI noise components with respect to port ac_1. The inclusion of twice the dc link capacitance on the primary and secondary sides, $2C_{dc,1}$ and $2C_{dc,2}$, between the mid-points and the CM voltage sources is explained in more detail in Appendix C. A three-phase ac-LISN and a dc-LISN are connected to the ports ac_1 and dc_2, respectively, to define the terminating impedances at these ports.

The red capacitor symbols with dashed connecting lines in Fig. 2.6 represent the considered parasitic coupling capacitances of the physically largest components in the circuit (transformers and semiconductors with heat sink). Due to the sizes of these components, it is expected that their parasitic couplings are relatively high and therefore become relevant already at the first spectral component of the EMI noise that enters the regulated EMI frequency band, i.e., at $f = 175\,\mathrm{kHz}$. Since it is found that the self-resonance frequencies of all filter components are above 175 kHz (the lowest self-resonance frequency results for C_{f1} with a resonance frequency of 350 kHz), the modeling of self-resonances of converter components was omitted for the sake of clarity.

The HF properties of the loads connected to dc_1 and dc_2, e.g., characterized by parasitic inductances in series to each load or parasitic capacitances to Protective Earth (PE), have an impact on the EMI noise at ac_1. However, load characteristics depend on the application and their HF properties are a priori unknown. For this reason, loads are replaced by suitable substitutes in order to facilitate a complete (terminated) EMI noise model. With regard to the DM EMI noise at each dc port, parasitic resonances between the load and the dc link would lead to a significant increase in conducted EMI. For the analysis, it is therefore assumed that dc-LISN networks[6] are inserted between the respective dc link capacitors and the connected loads, such that resonances between the dc links and the loads can be excluded. In the context of CM EMI noise, it is mainly the parasitic earth capacitances of the load that have an impact on the conducted EMI. A detailed analysis reveals highest levels of EMI noise at ac_1 if the primary-side dc load has no parasitic capacitance to PE. This is achieved by placing a CM filter inductor between dc_1 and the dc-LISN. The high impedance value of the CM filter inductor (ideally) acts as an open circuit at HF and therefore the load connected to dc_1 is omitted in Fig. 2.6. On the secondary side, the worst-case is found to be present if the load features a large capacitance to PE which is clarified as part of the explanation of the CM EMI model in Subsection 2.3.2. There it becomes apparent that the effective CM impedance of the dc-LISN is low enough to be considered as worst-case load scenario. It is to be noted that the presented model is intended for the design of the ac-side EMI filter and therefore, the dc-side DM EMI noise sources of the model, such as described in [68], are not included.

[6] Fig. 2.6 depicts the network of the dc-LISN, which consists of two inductors (50 µH each), two capacitors (470 nF each), and two resistors (50 Ω each).

Due to the rectangular waveform characteristics of the DM and CM noise voltages, the corresponding amplitude spectra feature envelopes decreasing with −20 dB/dec. Therefore, the EMI noise levels for frequencies close to 150 kHz are most relevant for the design of the EMI filter, given that the switching frequency is below the frequency range that is regulated for EMI ($f \in [150\,\text{kHz},\ 30\,\text{MHz}]$). As a final note, the derived models are expected to be useful up to a frequency of approximately 1 MHz and attenuations of up to approximately 100 dB. The limitation related to damping is based on the fact that also very weak coupling between a filter node where high ac excitations are present (i.e., toward the switching stage) and a filter node with very low ac excitations (toward the grid) substantially increases the ac excitation at the grid-side node of the filter. Such coupling could be reduced by further improving the filter layout, e.g., by using a placement of the filter components that is similar to the schematic diagram of the filter (with this, the input-side and output-side filter components are located far from each other). However, in view of the need for a high power density, this typically is not possible in industrial designs, for which reason a certain reduction in filter attenuation is accepted.

2.3.1 DM EMI model of the D3ABC

To isolate the DM EMI noise component from the CM components, the CM voltage sources are set to zero, $v_{\text{cm},1} = v_{\text{cm},2} = 0$. Furthermore, a symmetric three-phase system is assumed and all component tolerances are neglected. Therefore, no CM voltage components can occur in the circuit and the noise levels in all three phases, a, b, and c, are the same. Accordingly, it is sufficient to analyze a single phase, e.g., phase a. Due to the absence of CM voltage components, the electric potentials at the star-points of the DM noise voltage sources, $v_{\text{dm},1,\text{a,b,c}}$ and $v_{\text{dm},2,\text{A,B,C}}$, and at the star-points formed by C_{f1}, C_{S1}, C_{f2}, and C_{S2} are all equal. For this reason, voltages across C_1, C_2, $2C_{\text{dc},1}$, and $2C_{\text{dc},2}$ are zero, i.e., these components can be replaced by short circuits, and the dc inductors, L_{dc}, as well as the dc-LISN can be neglected. Finally, each real transformer in Fig. 2.6 is replaced by the circuit in Fig. 2.2(b), which results in the single-phase equivalent circuit shown in **Fig. 2.7(a)**.

As indicated in Fig. 2.7(a), the total DM EMI noise, $v_{\text{dm,t}}$, that is applied to the LISN is equal to the voltage ripple across C_{f1}, which depends on the capacitor current. The capacitor current is composed of the currents through L_σ and L_{ac}, i.e., $i_{\text{dm,dab}}$ and $i_{\text{dm,bst}}$, respectively. For a meaningful design of C_{f1} and C_{f2}, which implies that the resonance frequencies of L_σ, C_{f1}, and C_{f2}

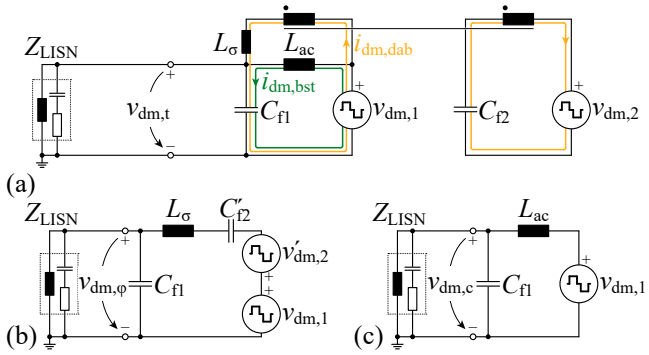

Fig. 2.7: Equivalent circuit for modeling the DM EMI part of the D3ABC: (a) total DM EMI model; (b) partial model related to the load-dependent DM EMI noise component; (c) partial model for calculating the load-independent DM EMI noise component.

are below the switching frequency, it can be assumed that $v_{\mathrm{dm,t}} \ll v_{\mathrm{dm,1}}$ and $v_{\mathrm{dm,t}} \ll v_{\mathrm{dm,2}}$ apply. Therefore, the feedback of $v_{\mathrm{dm,t}}$ on the currents $i_{\mathrm{dm,dab}}$ and $i_{\mathrm{dm,bst}}$ is negligible and the implications of the two currents on $v_{\mathrm{dm,t}}$ can be analyzed separately.

Following the path of the current $i_{\mathrm{dm,dab}}$, i.e., only the noise resulting from the DAB converter part power transfer (L_{ac} is accordingly left open), reveals the circuit shown in **Fig. 2.7(b)**. There, the primary-side referred values of the secondary-side filter capacitor, $C'_{\mathrm{f2}} = C_{\mathrm{f2}}/n^2$, and the secondary-side DM voltage source, $v'_{\mathrm{dm,2}} = n\,v_{\mathrm{dm,2}}$, are connected in series to the primary-side DM voltage source, $v_{\mathrm{dm,1}}$. It is to be noted that the total voltage across $v_{\mathrm{dm,1}}$ and $v'_{\mathrm{dm,2}}$ is equal to the voltage difference $v_{\mathrm{dm,1}} - v'_{\mathrm{dm,2}}$. Accordingly, $v_{\mathrm{dm,1}} - v'_{\mathrm{dm,2}} \approx 0$ results for zero HF phase shift, $|\varphi_{\mathrm{p}}|$, between $v_{\mathrm{dm,1}}$ and $v'_{\mathrm{dm,2}}$ if $V_{\mathrm{dc,1}} = nV_{\mathrm{dc,2}}$ applies. In this case, $i_{\mathrm{dm,dab}}$ is zero. With increasing value of $|\varphi_{\mathrm{p}}|$, i.e., increasing power transfer between dc_1 and dc_2, cf. (2.12), the voltage applied to L_σ, $v_{\mathrm{dm,1}} - v'_{\mathrm{dm,2}}$, and, with this, $i_{\mathrm{dm,dab}}$ increase. As a consequence, the EMI noise component, $v_{\mathrm{dm},\varphi}$ in Fig. 2.7(b), increases if the secondary-side load increases.

Following the path of the current $i_{\mathrm{dm,bst}}$ gives the circuit shown in **Fig. 2.7(c)**. This current features a triangular shape that is typical for VSCs. The HF components of $v_{\mathrm{dm,1}}$ are mainly defined by the line voltage and the dc link voltage and are practically independent of the load. For this reason, the related EMI noise component, $v_{\mathrm{dm,c}}$, is also independent of the load (assuming constant inductance L_{ac}).

The total DM EMI noise is obtained by means of superposition,

$$v_{\mathrm{dm,t}} = v_{\mathrm{dm},\varphi} + v_{\mathrm{dm,c}}. \tag{2.15}$$

2.3.2 CM EMI model of the D3ABC

For the analysis of the CM equivalent circuit of the converter's EMI model, the DM voltage sources in Fig. 2.6 are set to zero, $v_{\mathrm{dm,1,a,b,c}} = v_{\mathrm{dm,2,A,B,C}} = 0$. Consequently, the three primary-side phases of the D3ABC can be considered to be connected in parallel to each other and the same applies to the three phases of the secondary side. As for the analysis conducted for DM EMI noise, a symmetric three-phase system is assumed, with all component tolerances being neglected. With this, the circuit shown in **Fig. 2.8(a)** results for the D3ABC without EMI filter. In a subsequent step, the transformer is replaced by the equivalent circuit shown in Fig. 2.2(b), which leads to the network depicted in **Fig. 2.8(b)**.

The total CM EMI noise voltage at the LISN, $v_{\mathrm{cm,t}}$, is the sum of the CM EMI noise voltages across $3C_{\mathrm{f1}}$ and C_1. Accordingly, $v_{\mathrm{cm,t}}$ depends on the CM EMI noise currents in the capacitors $3C_{\mathrm{f1}}$ and C_1. In the presented analysis, these capacitor currents are split into the four partial currents (mesh currents) marked in Fig. 2.8(b): $i_{\mathrm{cm,dab}}$, $i_{\mathrm{cm,bst}}$, $i_{\mathrm{cm,p1}}$, and $i_{\mathrm{cm,p2}}$. The implications of these currents on $v_{\mathrm{cm,t}}$ are detailed in the following. It should be noted that $v_{\mathrm{cm,t}} \ll v_{\mathrm{cm,1}}$ and $v_{\mathrm{cm,t}} \ll v_{\mathrm{cm,2}}$ is assumed. Accordingly, the feedback of $v_{\mathrm{cm,t}}$ on $i_{\mathrm{cm,dab}}$, $i_{\mathrm{cm,bst}}$, $i_{\mathrm{cm,p1}}$, and $i_{\mathrm{cm,p2}}$ is negligible and each of the four four partial currents can be analyzed individually in the sense of a mesh current analysis (Maxwell´s circulating currents method), also considering, that impedances of the components (e.g., $C_{\mathrm{dc,1}}$ and $C_{\mathrm{dc,2}}$) coupling the mesh current equations are very low and/or can be neglected for a first step analysis.

Following the path of the current $i_{\mathrm{cm,dab}}$, i.e., $L_{\mathrm{ac}}/3$, $3C_{\mathrm{S1}}$, $3C_{\mathrm{S2}}$, and $3C_{\mathrm{T}}$ are left open, reveals the circuit shown in **Fig. 2.8(c)**, which is similar to Fig. 2.7(b) except for the dc link capacitances, $2C_{\mathrm{dc,1}}$ and $2C'_{\mathrm{dc,2}} = 2C_{\mathrm{dc,2}}/n^2$, and the parasitic capacitance C_1.[7] At the ac-side interface, marked with $v_{\mathrm{cm},\varphi}$, the parasitic capacitance C_1 is in series with the remaining circuit. The rms value of $i_{\mathrm{cm,dab}}$ increases with the HF phase shift, $|\varphi_{\mathrm{p}}|$, and, accordingly, the operating power of the isolated dc/dc part of the D3ABC is increased. For this reason, $v_{\mathrm{cm},\varphi}$ increases as the load on the secondary side increases.

Following the path of the current $i_{\mathrm{cm,bst}}$, i.e., $L_\sigma/3$, $3C_{\mathrm{S1}}$, $3C_{\mathrm{S2}}$, and $3C_{\mathrm{T}}$ are left open, gives the circuit shown in **Fig. 2.8(d)** that corresponds to the DM

[7] On the secondary side, a parallel path to $C_{\mathrm{dc,2}}$ exists, through C_2, $Z_{\mathrm{LISN}}/2$, and $L_{\mathrm{dc}}/2$, but the current in this parallel path is negligible.

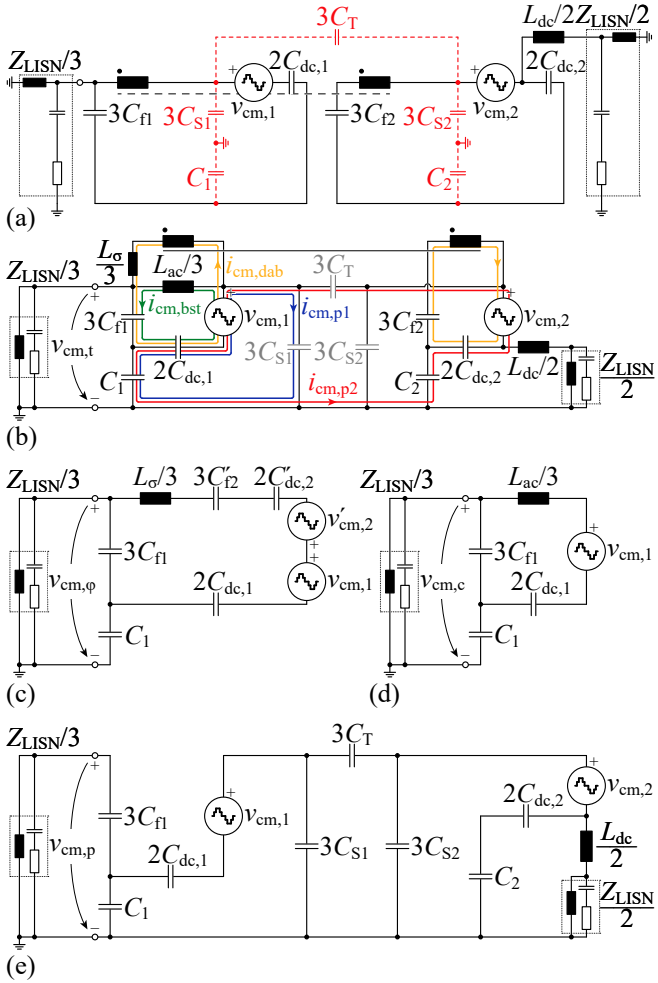

Fig. 2.8: Equivalent circuit for modeling the CM EMI part of the D3ABC: (a) total CM EMI model; (b) total CM EMI model with the transformer being replaced by the equivalent circuit depicted in Fig. 2.2(b); (c) partial model related to the secondary-side load-dependent CM EMI noise component; (d) partial model for calculating the secondary-side load-independent CM EMI noise component that is generated by the primary-side CM EMI noise voltage source; (e) partial model related to the CM EMI noise voltage that arises due to the parasitic capacitances C_{S1}, C_{S2}, and C_T.

circuit in Fig. 2.7(c), except for the additional dc link capacitance, $2C_{\mathrm{dc1}}$, and the capacitance C_1, which appears at the input of the network and in series to the remaining circuit. Since $v_{\mathrm{cm,1}}$ does not depend on the load, and assuming that $L_{\mathrm{ac}}/3$ is constant, the partial CM EMI noise voltage $v_{\mathrm{cm,c}}$ does not depend on the load either.

Finally, the circuit shown in **Fig. 2.8(e)** results if $L_\sigma/3$ and $L_{\mathrm{ac}}/3$ are left open. With this approximation, the filter capacitance $3C_{\mathrm{fl}}$ is in series to the remaining circuit. Mainly the primary-side CM voltage source $v_{\mathrm{cm,1}}$ contributes to the formation of $v_{\mathrm{cm,p}}$, by means of the current $i_{\mathrm{cm,p1}}$, which primarily flows through the series connected capacitors $2C_{\mathrm{dc1}}$, $\approx 3(C_{\mathrm{S1}} + C_{\mathrm{T}})$, and C_1. The current $i_{\mathrm{cm,p2}}$ that is generated by the secondary-side CM voltage source $v_{\mathrm{cm,2}}$ is comparably small and, consequently, the HF phase shift, φ_{p}, has a minor impact on $v_{\mathrm{cm,p}}$. A respective circuit simulation of the investigated D3ABC reveals that $v_{\mathrm{cm,p}}$ increases by less than 3 dB at 175 kHz if the output power at port dc_1 is decreased from 4 kW to 0 and, at the same time, the output power at port dc_2 is increased from 2.5 kW to 6.5 kW (these power values stem from the example workload scenarios 1 and 2 defined in **Subsection 2.5.3**).

It is worth noting that, according to the equivalent circuit in Fig. 2.8(e), the value of $i_{\mathrm{cm,p2}}$ increases as the CM impedance of the load connected to the secondary-side dc port, represented here by Z_{LISN}, decreases. Accordingly, the highest value for $i_{\mathrm{cm,p2}}$ results if Z_{LISN} is replaced by a short circuit. However, in terms of a worst-case estimation, it is sufficient if Z_{LISN} is much smaller than the impedance of $3C_{\mathrm{S2}}$. According to Subsection 2.4.1, C_{S2} has an estimated value of 200 pF for the hardware investigated in this work. Thus, in the considered frequency range of 150 kHz $< f <$ 1 MHz, the impedance of $3C_{\mathrm{S2}}$ is between 1.8 kΩ and 270 Ω, which is more than a factor of 10 larger than $Z_{\mathrm{LISN}}/2 = 25\,\Omega$. Consequently, the CM impedance of the dc-LISN sufficiently represents the worst case in the considered case.

The total CM EMI noise is obtained by means of superposition,

$$v_{\mathrm{cm,t}} \approx v_{\mathrm{cm},\varphi} + v_{\mathrm{cm,c}} + v_{\mathrm{cm,p}}. \tag{2.16}$$

2.3.3 Verification of the EMI models

To verify the derived EMI models, the spectra of the DM and CM noise calculated with the EMI models, i.e., without EMI filter, have been compared to the DM and CM noise spectra obtained from circuit simulations of the converter. The characterization of the DM and CM noise sources of the EMI models is a three-step process, which has been realized with MATLAB. First, the time-domain waveforms of the voltages at the six switching nodes over a

mains period are calculated based on the duty cycles and the HF phase shift defined by (2.8) and (2.12), for the operating conditions listed in Table 2.1. In a subsequent step, the waveforms of the DM and CM voltages, i.e., $v_{\mathrm{dm},1}(t)$, $v_{\mathrm{cm},1}(t)$, $v_{\mathrm{dm},2}(t)$, and $v_{\mathrm{cm},2}(t)$, are calculated, as shown in Fig. 2.5(a) for the primary-side DM and CM voltages. Finally, the corresponding spectra, e.g., depicted in Fig. 2.5(b), are determined. With this, the noise voltages at the mains-side interface of the converter, $v_{\mathrm{dm,t}}(t)$ in Fig. 2.7(a) and $v_{\mathrm{cm,t}}(t)$ in Fig. 2.8(b), are determined by superposition.[8]

In order to determine the expected upper and lower boundaries of the noise voltage measured by a CISPR-compliant QP detector, the spectra of $v_{\mathrm{dm,t}}(t)$ and $v_{\mathrm{cm,t}}(t)$, i.e., $V_{\mathrm{dm,rms}}(f)$ and $V_{\mathrm{cm,rms}}(f)$, are post-processed by estimating the minimum and maximum QP signal levels as proposed in [67] for a defined receiver bandwidth of $RBW = 9\,\mathrm{kHz}$. The estimation of the minimum QP signal level (in the following referred to as *Min* estimate) of the DM voltage at the LISN (in dBµV) can be calculated with

$$V_{\mathrm{dm,min}}(f) = 20\,\mathrm{dB\mu V}\log_{10}\left(\frac{1}{1\,\mu\mathrm{V}}\sqrt{\sum_{\xi=f-\frac{RBW}{2}}^{\xi=f+\frac{RBW}{2}} V_{\mathrm{dm,rms}}(\xi)^2}\right), \tag{2.17}$$

which represents an equal spectral power within RBW. In a similar way, [67] proposes an estimation of the maximum QP signal level (in the following referred to as *Max* estimate) calculated with

$$V_{\mathrm{dm,max}}(f) = 20\,\mathrm{dB\mu V}\log_{10}\left(\frac{1}{1\,\mu\mathrm{V}}\sum_{\xi=f-\frac{RBW}{2}}^{\xi=f+\frac{RBW}{2}} V_{\mathrm{dm,rms}}(\xi)\right). \tag{2.18}$$

The same expression can be used to evaluate the *Min*/*Max* estimates of the CM noise components. The lower and upper solid lines in **Fig. 2.9(a,b)** represent the calculated results for these boundaries.[9]

For comparison, a circuit simulation of the converter was performed using the operating conditions and component values listed in Table 2.1, Table 2.2, and Table 2.3. From the results of the simulation, the spectra and the *Min*/*Max* estimates were calculated (shown as dotted lines in Fig. 2.9(a,b)). It can be

[8] In anticipation of the findings of Section 2.4, the EMI models are parameterized using the values listed in Table 2.2 and Table 2.3 for the converter components and parasitic capacitances for these calculations.

[9] Due to the symmetry of the simulated circuit, the DM components of all phases are identical. Therefore, only the spectrum of phase a is shown.

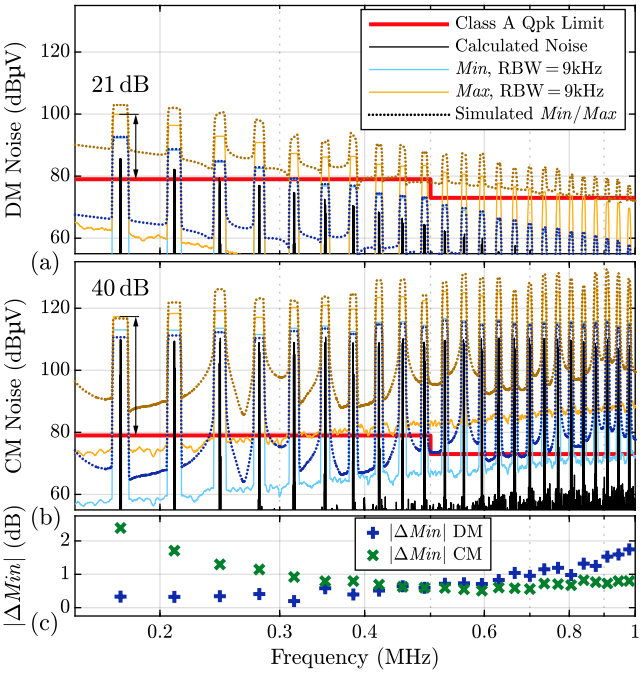

Fig. 2.9: Resultant EMI noise voltages at the LISN for the converter without EMI filter calculated by applying the DM and CM voltages shown in Fig. 2.5(b) to the equivalent circuits in Fig. 2.7 and Fig. 2.8: (a) DM, (b) CM. The solid black curves depict the calculated voltage spectra, and the lightblue and orange curves represent the *Min*/*Max* estimates determined with (2.17) and (2.18), respectively. The solid and dotted curves result if the voltages at the six switching nodes of the D3ABC are calculated numerically with MATLAB and simulated with a circuit simulator, respectively. (c) Shows the difference of the *Min* estimates between calculated and simulated noise at the harmonics of the switching frequency.

seen in Fig. 2.9(a,b) that the calculated and simulated *Min* estimates of the DM and CM EMI noises at the harmonics of the switching frequency agree well. **Fig. 2.9(c)** shows the absolute deviations at those harmonics that are less than 2.5 dB over the entire frequency range considered. The discrepancies in case of the *Max* estimates for both DM and CM EMI noise are largely related to the fact that the calculations of the waveforms of the voltages at the switching nodes assume a constant dc link voltage without ripple. The simulation considers the voltage ripple, leading to sidebands with higher amplitudes, which mainly increase the results of the *Max* estimates.

2.4 EMI Filter Design

This section describes the design of an EMI filter for a given hardware demonstrator of the D3ABC topology using the EMI noise models of Section 2.3. The power stage of the demonstrator has been optimized by means of an η–ρ-Pareto optimization as described in [51] in a preceding step. The separation between the EMI filter and the power stage is made according to the converter parts marked with curly braces in Fig. 2.1, i.e., all components between the port ac_1 and $L_{\mathrm{dm},1}$ (including $L_{\mathrm{dm},1}$) are part of the EMI filter, and all remaining components belong to the main converter part. This kind of separation is motivated by the fact that besides L_{ac} and L_{σ}, also the filter capacitors C_{fl} are subject to relatively large rms currents. For this reason, these passive components substantially contribute to the total converter volume and need to be included in the η–ρ-Pareto optimization of the D3ABC. **Appendix A** describes the design of the main converter part and the components of the resulting hardware demonstrator in more details. **Table 2.2** lists the relevant converter parameters and component values used for the EMI filter design.

Prior to the design of the EMI filter, the spectra of the EMI noise voltages that appear at the LISN without EMI filter part, cf. Fig. 2.6, are analyzed in a first step in **Subsection 2.4.1** in order to determine the required attenuation characteristics of the EMI filter. Thereafter, the design of the EMI filter is described in **Subsection 2.4.2** and **Subsection 2.4.3** for the DM and CM parts of the EMI filter, respectively. The EMI filter is designed to comply to the CISPR class A QP limit for $P_1 + P_2 = 7.5\,\mathrm{kW}$ at the port ac_1 ($P_1 = 5\,\mathrm{kW}$ at the port dc_1 and $P_2 = 2.5\,\mathrm{kW}$ at dc_2 as described in Section 2.1).

Tab. 2.2: Main component values of the D3ABC.

Switching frequency	$f_s = 35\,\text{kHz}$
Ac inductance	$L_{ac} = 3 \times 134\,\mu\text{H}$
Transformer turns ratio	$n = 2.6$
Stray inductance	$L_\sigma = 3 \times 88\,\mu\text{H}$
Primary-side dc link capacitor	$C_{dc,1} = 2 \times 12\,\mu\text{F}$
Secondary-side dc link capacitor	$C_{dc,2} = 2 \times 37\,\mu\text{F}$
Secondary-side dc filter inductor	$L_{dc} = 2 \times 14.7\,\mu\text{H}$
Primary-side filter capacitor	$C_{f1} = 3 \times 10\,\mu\text{F}$
Secondary-side filter capacitor	$C_{f2} = 3 \times 21.5\,\mu\text{F}$

2.4.1 EMI noise voltages without EMI filter part

In order to enable the estimation of the spectra of the DM and CM voltage components at the LISN without EMI filter, the values of the parasitic capacitances C_{S1}, C_{S2}, C_1, C_2, and C_T must first be estimated.

The parasitic capacitances from the switching nodes to PE, C_{S1} and C_{S2}, are partly determined by the metal areas on the back of the low-side transistors, since all MOSFETs are mounted on a conductive heat sink that is connected to PE, and partly due to the parasitic capacitances between the high-side gate driver and PE. A respective estimation reveals $C_{S1} \approx C_{S2} \approx 200\,\text{pF}$.

With regard to the parasitic capacitances that are present between the midpoints of the dc links and PE, C_1 and C_2, it is assumed that these capacitances are mainly due to the high-side transistors and the low-side gate drivers. However, compared to C_{S1} and C_{S2}, the low-side gate drivers of each side of the converter (primary and secondary) share a common supply, which reduces the value of the parasitic capacitances. Accordingly, a value of approximately 450 pF has been determined for C_1 and C_2.

Finally, the parasitic capacitance of each coupled inductor / transformer is estimated based on ideal plate capacitor approximations. For this, the overlapping areas between the coils of the primary side and the secondary side are approximated by a first plate capacitor, $C_{T,12}$. The areas between the coils and the magnetic core are approximated by two further plate capacitors, $C_{T,1c}$ and $C_{T,2c}$, for primary side and secondary side, respectively. These two capacitors are connected in series with the impedance of the magnetic core material. With respect to this impedance, reference [69] reveals a measured conductivity $\sigma \geq 0.5\,\text{S/m}$ for the ferrite core material 3C95, i.e., a material that is similar to the core material (N95) used as described in Appendix A. Further-

Tab. 2.3: Estimated values of the parasitic capacitances.

Primary-side switch-node capacitances	$3 \times C_{S1} = 3 \times 200\,\text{pF}$
Secondary-side switch-node capacitances	$3 \times C_{S2} = 3 \times 200\,\text{pF}$
Primary-side parasitic dc link capacitance	$C_1 = 450\,\text{pF}$
Secondary-side parasitic dc link capacitance	$C_2 = 450\,\text{pF}$
Parasitic transformer capacitances	$3 \times C_T = 3 \times 100\,\text{pF}$

more, it is found that the core impedance decreases for increasing frequency. A similar result was obtained for the measured impedance characteristic of another related ferrite material (N87) in [70]. There, the measurements show a decrease in impedance with increasing frequency throughout the entire frequency range between 100 kHz and 50 MHz. A comparison of the impedances of the parasitic capacitances and the impedance of the core at the relevant frequency of 175 kHz reveals that the impedance of the core can be neglected. Thus, the total parasitic capacitance, C_T, is calculated with

$$C_T = C_{T,12} + \frac{C_{T,1c} C_{T,2c}}{C_{T,1c} + C_{T,2c}}, \tag{2.19}$$

i.e., $C_{T,12}$ is connected in parallel to the series connection of $C_{T,1c}$ and $C_{T,2c}$. **Table 2.3** lists the values estimated for C_{S1}, C_{S2}, C_1, C_2, and C_T.

The values of the *Max* estimates for the DM and CM EMI noise determined in Subsection 2.3.3 and shown in Fig. 2.9 serve as a basis to define the required attenuations of the DM and CM parts of the EMI filter. It can be seen that the 5^{th} harmonic of the switching frequency, at $5f_s = 175\,\text{kHz}$, is the first harmonic component that enters the EMI frequency range defined by the CISPR regulation.

2.4.2 DM filter design

Fig. 2.10 depicts the flow chart of the DM EMI filter design procedure, revealing the individual design steps in simplified form. According to the spectrum of the *Max* estimate depicted in Fig. 2.9(a), the highest attenuation of 21 dB is required at the lowest frequency that is relevant for the EMI filter, $f \approx 5f_s = 175\,\text{kHz}$. Therefore, the EMI filter is designed with respect to this requirement. However, the required attenuation at 175 kHz is increased by 6 dB, to 27 dB, in order to take into account an eventual increase of the total EMI noise voltage due to superimposed CM noise voltage components.

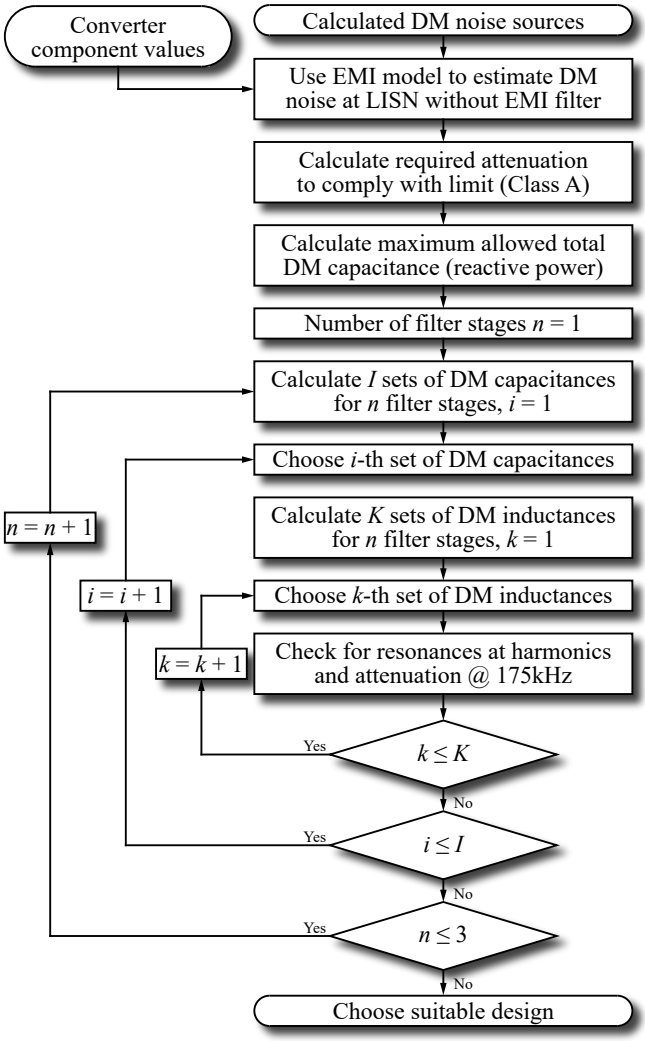

Fig. 2.10: Step by step illustration of the DM EMI filter design process. For the CM filter, the process is very similar, with the following differences: the maximum CM capacitance is limited by the maximum permissible line-frequency current on PE, the last filter stage has no CM capacitance, and the values of the CM filter capacitors, $C_{\text{cmdc},1}$ and $C_{\text{cmdc},2}$, must also be iterated.

In a first step, a single L–C filter stage was considered. However, to achieve the required attenuation, the resonance frequency of this filter stage would need to be equal to 33 kHz, which is very close to the switching frequency and leads to a HF rms current of more than 5 A at 35 kHz. A significant reduction of this HF current, e.g., to less than 1 A, could only be achieved by substantially increasing the filter inductance and / or capacitance, but this leads to an intolerable increase of the filter volume and / or the reactive power consumption at mains frequency.

For these reasons, the two-stage $L_{\mathrm{dm},1}$–$C_{\mathrm{dm},1}$–$L_{\mathrm{dm},2}$–$C_{\mathrm{dm},2}$ filter structure depicted in **Fig. 2.11(a)** has been considered in a second step. The resonance frequencies of this network are greater than the switching frequency to allow a small filter volume. In order to prevent resonant amplifications at the harmonics of the switching frequency, a forbidden frequency range was defined around the frequencies of the harmonic components of the EMI noise voltages,

$$f_{\mathrm{forbidden}} \in \left[k f_{\mathrm{s}} - \frac{\Delta f}{2},\ k f_{\mathrm{s}} + \frac{\Delta f}{2} \right], \qquad k \in \mathbb{N}, \tag{2.20}$$

where it was found that $\Delta f = 6$ kHz enables sufficiently low HF rms currents in the filter inductors. Furthermore, the compact off-the-shelf inductors that are used to realize $L_{\mathrm{dm},1}$ and $L_{\mathrm{dm},2}$ are subject to partial saturation (i.e., their inductances drop with increasing current; the considered peak value of the ac current is $I_{\mathrm{ac,peak}} = 16.4$ A). For this reason, the resonance frequencies of the filter depend on the instantaneous values of the phase currents, which must be taken into account when evaluating (2.20). Accordingly, the optimization of the EMI filter with respect to minimum filter volume is not straightforward and has been conducted by means of an exhaustive search over a range of possible component values.

This exhaustive search considers a set of initial inductances,

$$L_{\mathrm{dm},1}, L_{\mathrm{dm},2} \in \{3.3,\ 6.8,\ 8.2,\ 10,\ 12,\ 22\}\ \mu\mathrm{H}, \tag{2.21}$$

and a set of corresponding reduced inductances (to take partial saturation at $I_{\mathrm{ac,peak}} = 16.4$ A into account),

$$L_{\mathrm{dm},1,\mathrm{min}}, L_{\mathrm{dm},2,\mathrm{min}} \in \{3.2,\ 5.0,\ 6.1,\ 8,\ 9,\ 16.5\}\ \mu\mathrm{H}. \tag{2.22}$$

For each of the capacitances, $C_{\mathrm{dm},1}$ and $C_{\mathrm{dm},2}$, one ceramic capacitor with 56 nF in parallel to one or two film capacitors with

$$C \in \{100,\ 120,\ 150,\ 220,\ 330,\ 470\}\ \mathrm{nF} \tag{2.23}$$

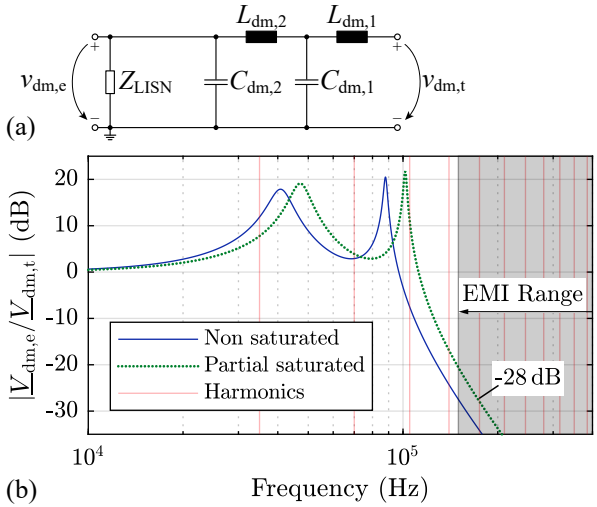

Fig. 2.11: (a) Implemented DM EMI filter circuit and (b) input-to-output TFs for non-saturated and partially saturated DM inductors (the inductance decreases with increasing current and reaches its minimum at the peak value of the ac current, $I_{ac,peak} = 16.4$ A, Z_{LISN} is approximated with a 50 Ω resistor).

is considered. **Table 2.4** lists the component values that result for the optimized EMI filter and **Fig. 2.11(b)** depicts the Transfer Functions (TFs) of the two-stage filter for unsaturated and partially saturated inductors. The vertical red lines in Fig. 2.11(b) indicate the harmonics of the switching frequency for $f_s = 35$ kHz. The filter achieves an attenuation of at least 28 dB at a frequency of 5 $f_s = 175$ kHz. Furthermore, according to the results of a circuit simulation, the total rms value of all spectral current components with frequencies greater than the line frequency, $f > 50$ Hz, is less than 800 mA in both DM filter inductors, $L_{dm,1}$ and $L_{dm,2}$. Thus, the HF currents in the inductors are much smaller than for the single-stage solution.

Since the second resonance frequency of the DM EMI filter is at 102 kHz, which is close to the third harmonic of the EMI noise at $f = 3 \times 35$ kHz = 105 kHz, the sidebands of the DM EMI noise at 102 kHz have been examined more closely in a circuit simulation. The simulation reveals that the maximum amplitudes of the DM EMI noise in the region at 102 kHz are 30 dB less than the peak at 105 kHz. In addition, the equivalent series resistances of $L_{dm,1}$ and $L_{dm,2}$ at 105 kHz are approximately equal to 1 Ω for each inductor (determined

by measuring the impedances of the components), which provides further attenuation of the resonance and consequently leads to a negligible increase in current due to the second resonance frequency of the DM EMI filter.

2.4.3 CM filter design

According to Fig. 2.9(b), the *Max* estimate of the CM EMI noise voltage slightly increases for increasing frequency. However, this increase will already be more than compensated for with a 2nd-order filter, since the filter's attenuation characteristic is −40 dB/decade. For this reason, the CM part of the EMI filter must provide an attenuation of 40 dB at $5f_s = 175\,\text{kHz}$ to meet the given limit. This attenuation is increased by 6 dB to ensure that the total EMI noise voltage, i.e., the superposition of its DM and CM voltage components, does not exceed the given limit and, in addition to this, by 10 dB to account for component tolerances and uncertainties in the estimations of the parasitic capacitances. With this, a required attenuation of 56 dB at 175 kHz results.

The considered CM part of the EMI filter is a third-order $L_{\text{cm},1}$–$C_{\text{cm},1}$–$L_{\text{cm},2}$ filter structure,[10] which is integrated into the previously determined DM part of the EMI filter according to Fig. 2.1, i.e., $L_{\text{cm},1}$ is connected in series to the three DM filter inductors $L_{\text{dm},2}$, the CM filter capacitor is inserted between the star point formed by the three DM filter capacitors $C_{\text{dm},2}$ and PE, and $L_{\text{cm},2}$ is inserted at the mains-side input of the EMI filter. In addition, CM filter capacitances, $C_{\text{cmdc},1}$ and $C_{\text{cmdc},2}$, are included between the midpoints of the primary-side and secondary-side dc links and PE as shown in Fig. 2.1. **Fig. 2.12(a)** depicts the CM equivalent circuit of the EMI filter (without $C_{\text{cmdc},1}$ and $C_{\text{cmdc},2}$, since these capacitors are in parallel to C_1 and C_2, cf. Fig. 2.1).

Now that the attenuation characteristic and the structure of the CM part of the EMI filter are defined, the component values need to be determined such that minimum filter volume results. In this regard, the stringent limitation of the maximum permissible line-frequency current on PE to a rms value of 3.5 mA confines the maximum allowable capacitances of the CM EMI filter capacitors to relatively small values. In a considered worst-case scenario, with an assumed line voltage imbalance of 6 % (according to IEC 60939-3) and capacitance tolerances of ±10 % (for both the DM and CM EMI filter capacitors), a maximum allowable value for the sum of the CM EMI filter capacitances,

[10] In the course of the design of the CM part of the EMI filter, four different filter structures were considered, starting from a 2nd-order structure ($L_{\text{cm},1}$–$C_{\text{cm},1}$) to a 5th-order structure ($L_{\text{cm},1}$–$C_{\text{cm},1}$–$L_{\text{cm},2}$–$C_{\text{cm},2}$–$L_{\text{cm},3}$), with the 3rd-order filter structure achieving the lowest total volume.

Tab. 2.4: Component values of the volume-optimized EMI filter.

DM filter inductance 1	$3 \times L_{\mathrm{dm},1} = 3 \times 12\,\mu\mathrm{H}$
DM filter capacitance 1	$3 \times C_{\mathrm{dm},1} = 3 \times 526\,\mathrm{nF}$
DM filter inductance 2	$3 \times L_{\mathrm{dm},2} = 3 \times 22\,\mu\mathrm{H}$
DM filter capacitance 2	$3 \times C_{\mathrm{dm},2} = 3 \times 356\,\mathrm{nF}$
CM filter inductance 1	$L_{\mathrm{cm},1} = 522\,\mu\mathrm{H}$
CM filter capacitance 1	$C_{\mathrm{cm},1} = 290\,\mathrm{nF}$
Ac-side CM filter inductance	$L_{\mathrm{cm,ac}} = 147\,\mu\mathrm{H}$
Primary-side dc link CM filter cap.	$C_{\mathrm{cmdc},1} = 82\,\mathrm{nF}$
Secondary-side dc link CM filter cap.	$C_{\mathrm{cmdc},2} = 19\,\mathrm{nF}$

$C_{\mathrm{cmdc},1} + C_{\mathrm{cm},1}$, of $C_{\mathrm{cm},\Sigma} = 399\,\mathrm{nF}$ is determined using the procedure described in [71].

The selection of suitable component values is conducted in the context of an exhaustive search. In a first step, $C_{\mathrm{cm},\Sigma}$ is distributed to $C_{\mathrm{cmdc},1}$ and $C_{\mathrm{cm},1}$ using five discrete values,

$$C_{\mathrm{cmdc},1} = \{0,\ 20\,\%,\ 40\,\%,\ 60\,\%,\ 80\,\%\}\, C_{\mathrm{cm},\Sigma}, \tag{2.24}$$

$$C_{\mathrm{cm},1} = C_{\mathrm{cm},\Sigma} - C_{\mathrm{cmdc},1}, \tag{2.25}$$

which, together with the required filter attenuation at $f = 175\,\mathrm{kHz}$, defines the maximum value of the inductance $L_{\mathrm{cm},1,\mathrm{max}}$. Based on this result, $L_{\mathrm{cm},1}$ is chosen using five discrete values,

$$L_{\mathrm{cm},1} = \{20\,\%,\ 40\,\%,\ 60\,\%,\ 80\,\%,\ 100\,\%\}\, L_{\mathrm{cm},1,\mathrm{max}}, \tag{2.26}$$

and $L_{\mathrm{cm,ac}}$ is calculated with the remaining required filter attenuation at $f = 175\,\mathrm{kHz}$. With this, 25 different designs result for the CM EMI filter, which have been evaluated with regard to the expected volume. The capacitor volumes are estimated with

$$V_{C,\mathrm{cm}} = p_0 + p_1 C, \tag{2.27}$$

using $p_0 = 1.2 \times 10^{-6}\,\mathrm{m}^3$ and $p_1 = 24\,\mathrm{m}^3\mathrm{F}^{-1}$ (referring to the F881 series of metallized polypropylene film capacitors manufactured by Kemet). Each inductor is optimized in terms of minimum volume, using a specifically implemented optimization procedure that is based on a scalable model of a three-phase CM EMI inductor with toroidal core.[11] Nanocrystalline material

[11] A simplified model is used to determine the inductance value and the current densities in the coils. The optimization procedure ensures that the inductance value of the resulting design does

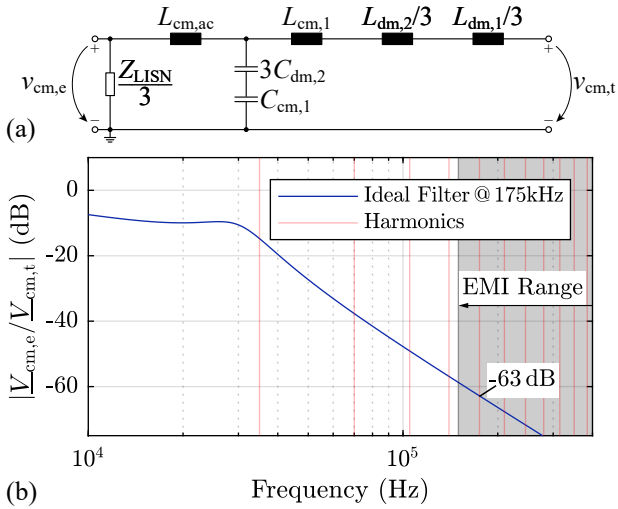

Fig. 2.12: (a) Implemented CM EMI filter circuit and (b) input-to-output TF of the CM EMI filter for the component values listed in Table 2.4 ($Z_{LISN}/3$ is approximated with a 16.7 Ω resistor).

is used for the cores of the CM EMI filter inductors and the three coils are made of solid copper wire. It is to be noted that the optimization method returns capacitors and core dimensions that are not directly available, since the optimization is based on scalable models. Therefore, the most suitable capacitors and cores have to be selected manually in a final step. Table 2.4 lists the final component values.

Fig. 2.12(b) depicts the frequency response of the EMI filter with respect to CM disturbances and for constant values of the CM EMI filter inductances.[12] At $f = 175$ kHz, the first filter stage, composed of $L_{cm,1}$ and $C_{cm,1}$, provides an attenuation of ≈ 40 dB and the second stage ($L_{cm,ac}$ and ac-LISN) ≈ 23 dB. The filter capacitors $C_{cmdc,1}$ and $C_{cmdc,2}$ have a negative effect on the attenuation at

not fall below the required inductance value given a permeability of 27 mH/m and the current densities in the coils remain below the maximum permissible current density of 10 A/mm^2 given a fill factor of 0.5. Since the CM voltage after the first stage is already low (e.g., 120 dBµV at 175 kHz, cf. Fig. 2.9(b)), possible saturation of the inductance cores is neglected.

[12] The permeability of nanocrystalline magnetic core material and, thus, the inductances of the CM filter inductors decrease for increasing frequency. The attenuation characteristic evaluated in the optimization and depicted in Fig. 2.12(b) was calculated for the inductances present at $f = 175$ kHz.

$f = 175\,\text{kHz}$ and require an additional attenuation of 5 dB. This is due to the fact that $C_{\text{cmdc,1}}$ and $C_{\text{cmdc,2}}$ attenuate the CM EMI voltage component caused by the currents $i_{\text{cm,p1}}$ and $i_{\text{cm,p2}}$, but not the voltage components that are due to the currents $i_{\text{cm,bst}}$ and $i_{\text{cm,dab}}$, cf. Fig. 2.8. Accordingly, $C_{\text{cmdc,1}}$ and $C_{\text{cmdc,2}}$ become mainly effective at high frequencies where the CM EMI noise currents $i_{\text{cm,bst}}$ and $i_{\text{cm,dab}}$ in Fig. 2.8(b) are well attenuated by the second-order filter structures $L_\sigma/3\text{–}3C_{\text{f1}}$ and $L_{\text{ac}}/3\text{–}3C_{\text{f1}}$, respectively. At 1 MHz, for example, inserting $C_{\text{cmdc,1}}$ and $C_{\text{cmdc,2}}$ increases the CM attenuation by 20 dB.

As a result, the EMI filter achieves a CM attenuation of 58 dB at $f = 175\,\text{kHz}$. Compared to the required attenuation of 56 dB determined at the beginning of this subsection, the total attenuation is 2 dB higher, which is related to the final step of the design of the CM part of the EMI filter, where suitable capacitors and cores have to be selected manually. In this regard, each component value resulting from the optimization is between a smaller and a larger available component. To be on the safe side, the larger component was always chosen for the realization.

2.5 Measurements

This section presents a verification of the EMI noise calculated with the EMI models derived in Section 2.3 using measurement results. In this regard, **Subsection 2.5.1** presents the realized hardware demonstrator including the EMI filter, **Subsection 2.5.2** describes the measurements of the DM and CM TFs of the EMI propagation paths and the realized EMI filter, and finally, Subsection 2.5.3 presents the results of EMI measurements and provides a comparison with the calculated EMI noise.

2.5.1 Hardware

Fig. 2.13(a) depicts the hardware demonstrator of the D3ABC detailed in Appendix A. The converter is operated as a bidirectional three-phase PFC rectifier, with the grid connected to the port ac_1 and the various dc loads connected to ports dc_1 and dc_2. The outer dimensions of the converter including the EMI filter are 150 mm × 240 mm × 54 mm = 5.91 in × 9.45 in × 2.13 in (width × depth × height).

The upper Printed Circuit Board (PCB) contains the control board with the sensors (e.g., phase current measurement), the primary-side power semiconductors, and their gate drivers. Furthermore, the filter capacitors, C_{f1}, and the DM filter inductors and capacitors of the first filter stage, $L_{\text{dm,1}}$ and $C_{\text{dm,1}}$,

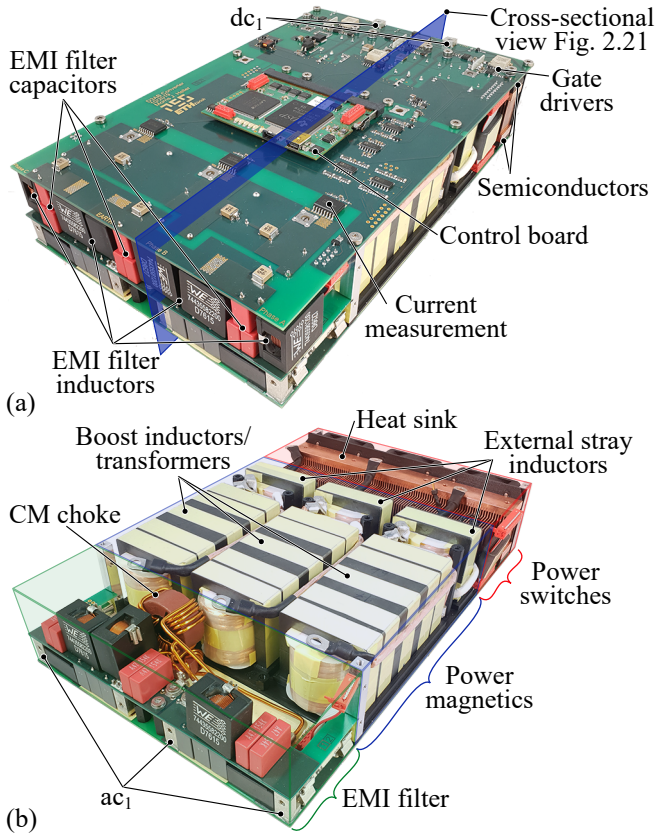

Fig. 2.13: Hardware demonstrator of a D3ABC detailed in Appendix A. The outer dimensions are 150 mm × 240 mm × 54 mm = 5.91 in × 9.45 in × 2.13 in (width × depth × height). (a) The upper Printed Circuit Board (PCB) contains control board, current sensors, and primary-side power semiconductors with their gate drivers. (b) Without upper PCB, the arrangement of the EMI filter, the boost inductors (transformers), the stray inductors, and the heat sinks for the power semiconductors are visible (from front to back). Dc port 2 is not visible on these pictures. The blue plane shows the location of the cross-sectional view in Fig. 2.21.

are soldered to the upper PCB as well. The picture in **Fig. 2.13(b)** shows the hardware demonstrator without upper PCB, revealing (from the front to the back) the arrangement of the EMI filter components (without C_{f1}, $L_{dm,1}$, and $C_{dm,1}$), the boost inductors/transformers, the external stray inductors, and the copper heat sink for the power semiconductors.

The power semiconductors are mounted with a thin layer of thermally conductive and electrically isolating foil onto a two-sided copper heat sink, with the semiconductors of the primary side mounted on top and those of the secondary side mounted on the bottom. The conductive heat sink is connected directly to the CM filter capacitors $C_{cmdc,1}$ and $C_{cmdc,2}$ and is grounded through PE.

Appendix A describes the design of the external stray inductor and the boost inductor/transformer as well as the components used for C_{f1}, C_{f2}. The components used for the EMI filter described in this chapter are summarized in **Table 2.5** (including C_{f1} and C_{f2}). The CM EMI filter inductors $L_{cm,1}$ and $L_{cm,ac}$ each have 3 coils with 5 and 3 turns, respectively, using a solid copper wire with a diameter of 1.8 mm. The DM and CM filter capacitors are realized by parallel connections of film capacitors and ceramic capacitors. The total volume of the designed EMI filter is 0.17 dm^3 (0.09 dm^3 for the DM part and 0.08 dm^3 for the CM part of the EMI filter).

2.5.2 Measured TFs of EMI propagation paths

The measurement results presented in this Section were obtained from small-signal measurements, i.e., the complete hardware setup was subject to voltages in the range of several volts. Accordingly, the port ac_1 was not connected to the three-phase ac lines in these measurements.

The aim of these measurements is to verify the EMI models derived in Section 2.3 together with the EMI filter using experimental results. According to the derived EMI noise models, four different noise sources need to be considered: $v_{dm,1}$, $v_{cm,1}$, $v_{dm,2}$, and $v_{cm,2}$. Each of these noise sources contributes to the noise voltage measured at the ac-LISN. Thus, all four TFs, from each noise source to the ac-LISN, must be known to calculate the voltage at the ac-LISN. The measurement of these four TFs is conducted directly on the hardware demonstrator, using a Vector Network Analyzer (VNA).

Fig. 2.14 depicts the measurement setup for measuring the TF from $v_{dm,1}$ to the ac-LISN as an example. A signal transducer injects the reference voltage of the VNA, i.e., a sinusoidal voltage with frequency f, at the switching nodes of two primary-side half-bridges of the power stage to emulate DM EMI noise.

Tab. 2.5: EMI filter components with their nominal values (A_L value at 100 kHz for the nanocrystalline magnetic cores).

Component	Mfr.	Part number	Nom. val.	#
C_{f1}	TDK	B32754C2106K000	10 µF	1
C_{f2}	TDK	C5750X6S2W225K250KA	2.2 µF	21
$L_{dm,1}$	Wurth	74435581200	12 µH	1
$C_{dm,1}$	Wurth	890334025039CS	470 nF	1
	Murata	GA355XR7GB563KW06L	56 nF	1
$L_{dm,2}$	Wurth	74435582200	22 µH	1
$C_{dm,2}$	Wurth	890334025022CS	150 nF	2
	Murata	GA355XR7GB563KW06L	56 nF	1
$C_{cmdc,1}$	Kemet	F881BC153(3)300(2)	15 nF	5
	Murata	GA355DR7GF472KW01L	4.7 nF	2
$C_{cmdc,2}$	Kemet	F881BC153(3)300(2)	15 nF	1
	Murata	GA355DR7GF472KW01L	4.7 nF	1
$L_{cm,1}$	Vac	W380	11.6 µH	1
$C_{cm,1}$	Kemet	R413I247000M1K	47 nF	6
	Murata	GA355DR7GF472KW01L	4.7 nF	2
$L_{cm,ac}$	Vac	W515	5.16 µH	1

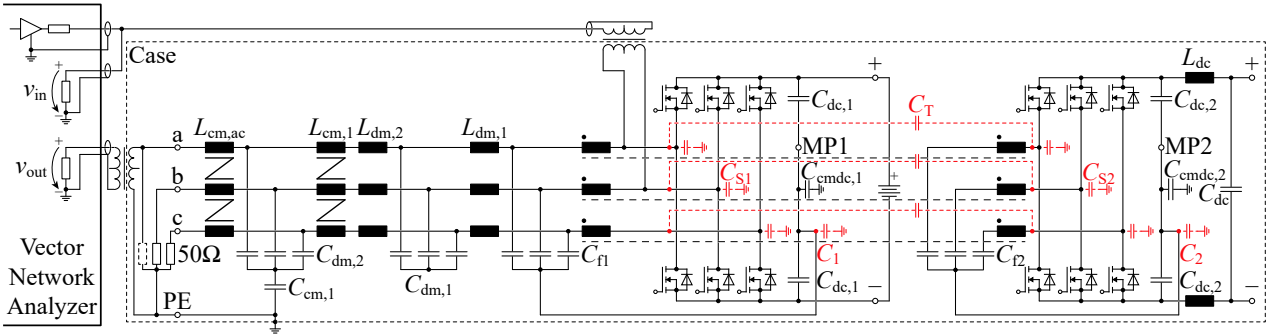

Fig. 2.14: Setup used to measure the TF of the EMI filter from the primary-side DM voltage source, $v_{dm,1}$, to the port ac_1 using a Vector Network Analyzer (VNA) that is connected to the hardware via two 1:1 transformers (T1-6T-X65+ by Mini-Circuits). The hardware is placed in an aluminum enclosure with the dimensions 400 mm × 310 mm × 110 mm, which emulates a converter housing. A 9 V battery connected to the primary-side dc link prevents a clipping of the input signal by the antiparallel diodes of the MOSFETs. The semiconductors on the secondary side are all turned on. Similar configurations are used to measure the remaining three TFs of the EMI filter, i.e., with respect to the CM components and as seen from the secondary side.

The VNA measures the reference voltage, v_{in}, and the voltage at port ac_1, v_{out}, where the three-phase lines would be connected through the ac-LISN. The HF impedance of the ac-LISN is emulated by three 50 Ω resistors, which are connected to port ac_1 (the resistor with dashed outline in Fig. 2.14 refers to the input resistance of the VNA). Due to the symmetry of the converter topology and the EMI filter network, it can be assumed that v_{in} is distributed equally between phase a and phase b and thus,

$$v_{\text{dm,1,a}} = \frac{v_{\text{in}}}{2},\ v_{\text{dm,1,b}} = -\frac{v_{\text{in}}}{2},\ v_{\text{dm,1,c}} = 0 \tag{2.28}$$

applies. In order to prevent the MOSFETs' antiparallel diodes from turning on and potentially clipping the reference voltage, the dc link of the half-bridges is precharged with a 9 V battery. Large resistors between the phases and in parallel with the dc link capacitors (intended for voltage measurement during operation of the converter) ensure that the potentials at the switching nodes will be approximately between the two potentials of the positive and the negative rails of the dc link. It should be noted that the non-linear output capacitances of the MOSFETs, C_{OSS}, are relatively large at 9 V dc link voltage. These capacitances are connected in parallel to the reference voltage source of the VNA. The additional loading of the VNA's output amplifier by C_{OSS} causes a voltage drop across the amplifier's inner impedance. However, due to the explicit measurement of the reference voltage at the system input, v_{in}, the impact of C_{OSS} on the measured TFs is minimized.

The remaining noise sources, in this case $v_{\text{cm,1}}$, $v_{\text{dm,2}}$, and $v_{\text{cm,2}}$, need to be set to zero. According to (2.28), the primary-side CM EMI noise voltage, $v_{\text{cm,1}}$, as defined in (2.13) is already zero for this measurement setup. Turning on all semiconductors on the secondary side sets the noise sources $v_{\text{dm,2}}$ and $v_{\text{cm,2}}$ to zero. It is to be noted that the measured TF needs to be multiplied by 2 to account for the 1/2 in the excitation (2.28). Furthermore, a signal transducer must be inserted between port ac_1 of the converter and the VNA to enable this measurement, since the VNA and the converter share a common ground potential. The signal transducers used are off-the-shelf devices (T1-6T-X65+ by Mini-Circuits), which feature a bandwidth of $f \in [15\,\text{kHz},\ 300\,\text{MHz}]$. To achieve reproducible measurements with respect to parasitic capacitances, the hardware is placed in an aluminum EMI enclosure with the dimensions 400 mm × 310 mm × 110 mm = 15.7 in × 12.2 in × 4.3 in (width × depth × height) to emulate a converter housing.

To measure the TF from $v_{\text{cm,1}}$ to the ac-LISN, the circuit shown in Fig. 2.14 is modified as described in the following. The switching nodes of the converter phases a, b, and c are connected together and the VNA applies the reference

voltage between this common switching node and the primary-side midpoint of the dc link, MP1, using a signal transducer (T1-6T-X65+). With this, the primary-side DM EMI noise sources are shorted, i.e., $v_{\mathrm{dm,1,a,b,c}} = 0$ applies. Note that by connecting the reference voltage to MP1, the primary-side dc link capacitances, $C_{\mathrm{dc,1}}$, are in parallel to the input voltage and are therefore not included in the measurement. Due to the low impedances of the dc link capacitors, negligible implications on the measurement results can be assumed. The dc link of the half-bridges is kept precharged with the previously mentioned battery.

For the measurements of the TFs from the secondary-side EMI noise sources, $v_{\mathrm{dm,2}}$ and $v_{\mathrm{cm,2}}$, to the ac-LISN, the reference voltage is applied in the same way as for the measurements on the primary side, but on the secondary side. The 9 V battery is placed in parallel to the secondary-side dc link and the primary-side MOSFETs are turned on instead of the secondary-side MOSFETs.

Fig. 2.15 depicts measured and calculated magnitude responses of the four TFs. The blue curves refer to measurement results that were obtained for a resolution bandwidth of 3 Hz, at 800 logarithmically distributed points in the frequency range $f \in [10\,\mathrm{kHz}, 30\,\mathrm{MHz}]$, and for a power level of the reference signal of 13 dBm.[13] The dash-dotted green and dotted curves represent calculated results that have been obtained using the equivalent circuit diagrams shown in Fig. 2.7 and Fig. 2.8 and the filter networks shown in Fig. 2.11 and Fig. 2.12. In this context, the dotted curves depict the results under the assumption of ideal impedances of all components according to Table 2.2, Table 2.3, and Table 2.4. Since the magnetic material of the CM filter inductors is highly dependent on the frequency, their A_{L} values were chosen to match the value of the material measured at $f = 175\,\mathrm{kHz}$. The dash-dotted green curves have been determined from measured frequency characteristics of all filter components. These frequency characteristics were measured separately for each component with an impedance measurement device (Agilent 4294A, 40 Hz to 110 MHz) before the hardware was assembled. With this approach, non-ideal effects such as frequency dependency, series resistances, and component self-resonances are taken into account.

According to Fig. 2.15, the measured magnitude responses are in good agreement with the predictions at low frequencies $f < 200\,\mathrm{kHz}$, except for the CM attenuations calculated with the linearized CM filter inductors (dotted curves) that match the measurements only at the design frequency of 175 kHz.

[13] The set power level of the reference signal refers to the power that is dissipated in a 50 Ω matching resistor if only this 50 Ω resistor is connected to the output of the VNA; 0 dBm is equal to 1 mW.

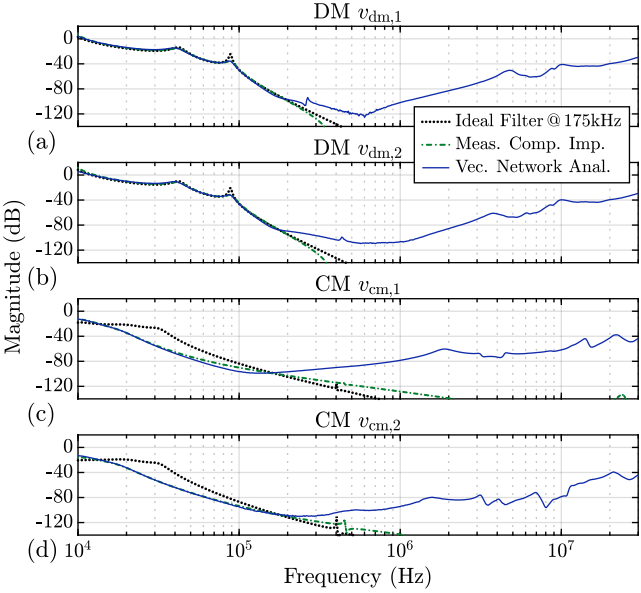

Fig. 2.15: Frequency responses of the EMI propagation paths of the whole converter measured from: (a) the primary-side DM voltage source, $v_{dm,1}$, (b) the secondary-side DM voltage source, $v_{dm,2}$, (c) the primary-side CM voltage source, $v_{cm,1}$, and (d) the secondary-side CM voltage source, $v_{cm,2}$. The dotted curves depict calculated results for constant component values, the dash-dotted green curves represent calculated results using measured impedance characteristics for all filter components, and the blue curves show the measured frequency responses of the filter. The dash-dotted green and the blue curves are in good agreement up to a frequency of $f = 200$ kHz. Parasitic effects, e.g., capacitive coupling between filter stages, prevent a further increase of the attenuation above this frequency.

For frequencies $f > 200\,\text{kHz}$ a continuing increase of the attenuation is predicted but the measured attenuation no longer increases. This discrepancy is explained by the simultaneous presence of parasitic capacitive couplings between filter components, further investigated in Subsection 2.5.3, and high filter attenuation in the range of 80 dB to 100 dB for $150\,\text{kHz} < f < 1\,\text{MHz}$. Due to these circumstances, a further increase of the attenuation is not feasible even at comparably low frequencies. In the context of an example, it is assumed that a parasitic coupling capacitance of 100 fF is effective in parallel with each phase of the EMI filter, i.e., between the line-side terminal of each phase and the switching node of the half-bridge of the same phase. A circuit simulation conducted in this regard reveals that the couplings caused by these parasitic capacitances are sufficient to prevent a further increase of the attenuation for $f > 200\,\text{kHz}$. Above $f > 200\,\text{kHz}$ the parasitic couplings between the components dominate the filter's attenuation characteristics.

For completeness, the calculated and measured TFs of the DM and CM parts of the EMI filter have been assessed as well. Similar to Subsection 2.5.2, the calculations are conducted using ideal impedances and measured impedance characteristics of the individual components. The measurements are carried out with the VNA connected to the hardware realization of the EMI filter. **Fig. 2.16(a)** shows the measured and calculated attenuation characteristics of the DM filter, which agree well for low frequencies, $f < 500\,\text{kHz}$. Above $f > 500\,\text{kHz}$, the model predicts a further increase in attenuation, however, the measured attenuation no longer increases. This discrepancy is again explained by the simultaneous presence of parasitic capacitive couplings between filter components and high filter attenuation in the range of 80 dB, due to which a further increase of the attenuation is not feasible as explained above. The comparison of the CM filter attenuation in **Fig. 2.16(b)** shows similar behavior, except that the CM attenuation calculated with the linearized CM filter inductances (dotted curve) agrees with the measurement only at the design frequency of 175 kHz.

2.5.3 EMI measurements

The conducted EMI noise of the D3ABC is measured for rectifier operation with load resistors connected to the ports dc_1 and dc_2 and for the operating voltages specified in Table 2.1. The three phases of the mains are connected to port ac_1 through an ac-LISN and the load resistors are connected to ports dc_1 and dc_2 via the dc-LISNs, respectively. To investigate the implication of the secondary-side power level on the level of conducted EMI noise at port

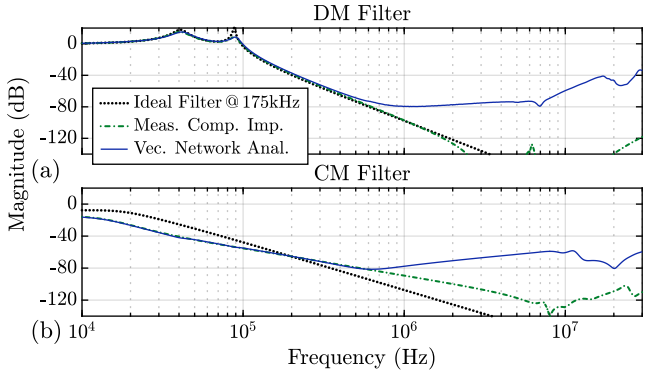

Fig. 2.16: Frequency responses of the (a) DM and (b) CM EMI filter. The dotted curves depict calculated results for constant component values, the dash-dotted green curves represent calculated results using measured impedance characteristics for all filter components, and the blue curves show the measured frequency responses of the filter. The dash-dotted green and the blue curves are in good agreement up to a frequency of $f = 500\,\text{kHz}$. Parasitic effects, e.g., capacitive coupling between filter stages, prevent a further increase of the attenuation above this frequency.

ac_1, two different scenarios with different loads, P_1 and P_2, are considered at the ports dc_1 and dc_2, respectively.

- Scenario 1 (S1): $P_1 = 4\,\text{kW}$, $P_2 = 2.5\,\text{kW}$
- Scenario 2 (S2): $P_1 = 0$, $P_2 = 6.5\,\text{kW}$

The total load, $P_1 + P_2 = 6.5\,\text{kW}$, is limited by the maximum allowed rms current of the employed ac-LISN, $I_{\text{LISN,rms}} < 10\,\text{A}$. To comply with this limit, the power P_1 is reduced from 5 kW, i.e., the power used to design the EMI filter in Section 2.4, to 4 kW.

To achieve reproducible EMI measurements, the hardware is placed in the same aluminum EMI enclosure used in Subsection 2.5.2, with which the parasitic ground capacitances are defined. Furthermore, a CM EMI filter inductor is connected to dc_1, to evaluate the worst-case workload scenario with regard to CM EMI noise as described in Section 2.3. This CM filter inductor is realized with a nanocrystalline core (W518 by Vacuumschmelze), which contains two windings with 5 turns each and features a CM inductance of 627 µH at $f = 100\,\text{kHz}$.

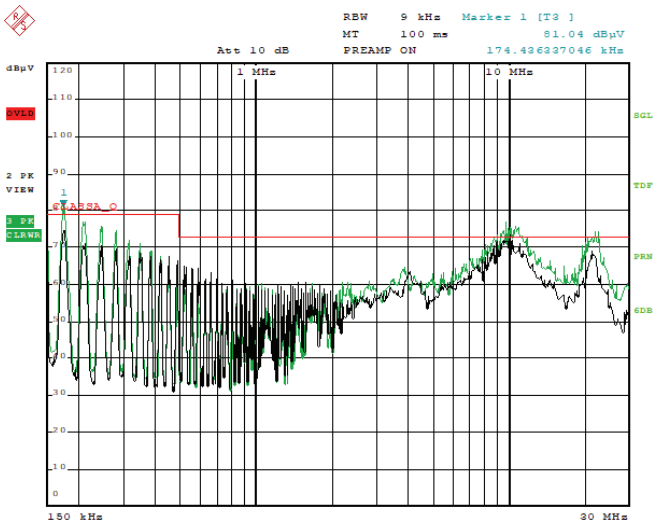

Fig. 2.17: Screenshot taken from the EMI test receiver (the shown result was measured for phase c). The converter operates as a PFC rectifier with a three-phase voltage source connected to port ac_1 ($f_\mathrm{m} = 50\,\mathrm{Hz}$, $V_\mathrm{ac,rms} = 230\,\mathrm{V}$), providing a total output power of 6.5 kW at the dc ports. The black curve, which was measured for an output power of $P_1 = 4\,\mathrm{kW}$ at dc_1 and $P_2 = 2.5\,\mathrm{kW}$ at dc_2, is below the CISPR class A limit for QP values (shown in red). The green curve, which was measured for $P_1 = 0$ and $P_2 = 6.5\,\mathrm{kW}$, slightly exceeds the limit at $f \approx \{175\,\mathrm{kHz}, 10\,\mathrm{MHz}, 21\,\mathrm{MHz}\}$.

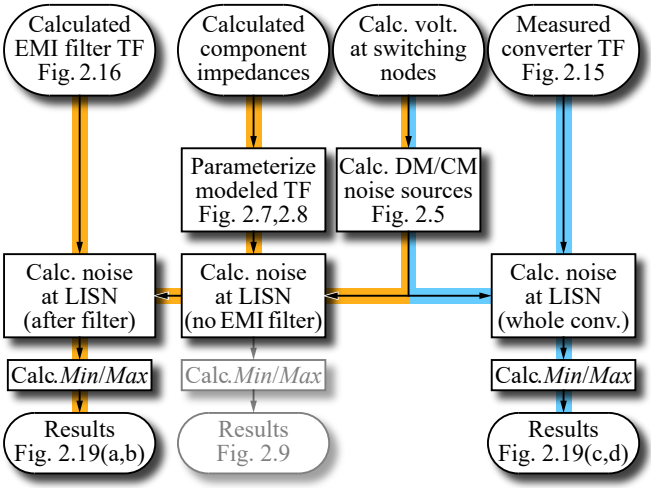

Fig. 2.18: Flow chart illustrating the procedures used to estimate EMI noise. The path on the left with orange background represents the fast calculation method which is solely based on analytical models and calculated (constant) component values. The path on the right with light blue background represents the accurate calculation method using measured TF to evaluate the EMI propagation paths.

The three measurement outputs of the ac-LISN, i.e., one for each phase, are connected one after another to a test receiver, which measures the EMI noise with a maximum peak detector (the maximum peak detector overestimates the EMI noise but allows for a substantially faster measurement compared to the QP detector). The EMI noise levels measured for phase a, b, and c are very similar (with deviations of less than 3.5 dB at $f = 175\,\text{kHz}$) with phase c showing the highest level of EMI noise. **Fig. 2.17** depicts a screenshot of the test receiver's monitor illustrating the spectra of the EMI noise levels in phase c (black curve: S_1, green curve: S_2). In case of S_1, the EMI noise is consistently below the class A QP limit. With regard to S_2, the EMI noise slightly exceeds the limit at $f = 175\,\text{kHz}$ by 2 dB and additionally at higher frequencies with a maximum exceedance of 4 dB at $f = 9.75\,\text{MHz}$.

In order to experimentally verify the derived model, the measured spectra of EMI noise are compared to corresponding EMI noise spectra. In this context, the spectra are calculated using two different methods, which provides a deeper insight into the capabilities and limitations of the models derived in Section 2.3. For the first method illustrated in **Fig. 2.18** on the left, the

rms value spectra of the DM and CM EMI noise for the converter, $v_{\mathrm{dm,t}}$ and $v_{\mathrm{cm,t}}$, are calculated for S1 and S2 as described in Subsection 2.3.3 taking into account the filter capacitances $C_{\mathrm{cmdc,1}}$ and $C_{\mathrm{cmdc,2}}$. In a subsequent step, these spectra are multiplied by the associated, i.e., DM or CM, calculated filter TFs shown in Fig. 2.16 (with respect to magnitude and phase). Finally, the DM and CM components are summed up for each workload scenario by means of superposition, which gives the spectrum of the total EMI noise, $V_{\mathrm{emi,rms}}(f)$. This enables the calculation of the *Min* estimate, $V_{\mathrm{emi,min}}$, and the *Max* estimate, $V_{\mathrm{emi,max}}$, based on (2.17) and (2.18) (there, $V_{\mathrm{dm,rms}}$ must be replaced by $V_{\mathrm{emi,rms}}$). Since this calculation method uses the model with calculated component values, it allows a fast EMI noise estimation at an early stage of the converter design. Therefore, it is in the following referred to as fast method.

For the second method, the rms value spectra of the DM and CM EMI noise voltage components, $v_{\mathrm{dm,1}}$, $v_{\mathrm{cm,1}}$, $v_{\mathrm{dm,2}}$, and $v_{\mathrm{cm,2}}$, are determined for S1 and S2 from the (rectangular) voltages at the switching nodes of the primary-side and secondary-side half-bridges as described in Subsection 2.3.3. In a subsequent step, these spectra are multiplied by the associated measured filter TF shown in Fig. 2.15. The resulting four noise spectra at the output of the filter, i.e., at the ac-LISN, are summed up for each workload scenario by means of superposition, which gives the spectrum of the total EMI noise, $V_{\mathrm{emi,rms}}(f)$. With $V_{\mathrm{emi,rms}}(f)$, again the *Min* and the *Max* estimates are calculated similarly to (2.17) and (2.18). Since this calculation method uses measured TFs of the actual hardware, it allows a more accurate estimation of the EMI noise and is therefore in the following referred to as accurate method.

Fig. 2.19(a) and **Fig. 2.19(b)** depict the obtained results for S1 and S2, respectively, using the fast method described above. The black curves reveal the measured EMI noise of phase c, the lightblue curves refer to the *Min* estimate and the orange curves to the *Max* estimate. The measured EMI noise level at the first spectral component entering the EMI regulated band, i.e., at $f = 175\,\mathrm{kHz}$, is as expected between $V_{\mathrm{emi,min}}$ and $V_{\mathrm{emi,max}}$. It is also evident that both, the measured and the estimated noise levels depend on the secondary-side load and show an increase in the measured noise level from 75 dBµV to 82 dBµV at $f = 175\,\mathrm{kHz}$ between scenario S1 in Fig. 2.19(a) and S2 in Fig. 2.19(b). This reveals a good agreement between measured and estimated noise levels at this frequency.

For harmonics above $f > 175\,\mathrm{kHz}$, the calculated attenuation is larger than the measured attenuation and the measurement is no longer located between the *Min*/*Max* estimates. To explain this discrepancy, the measured noise is compared to the results calculated with the accurate method as well.

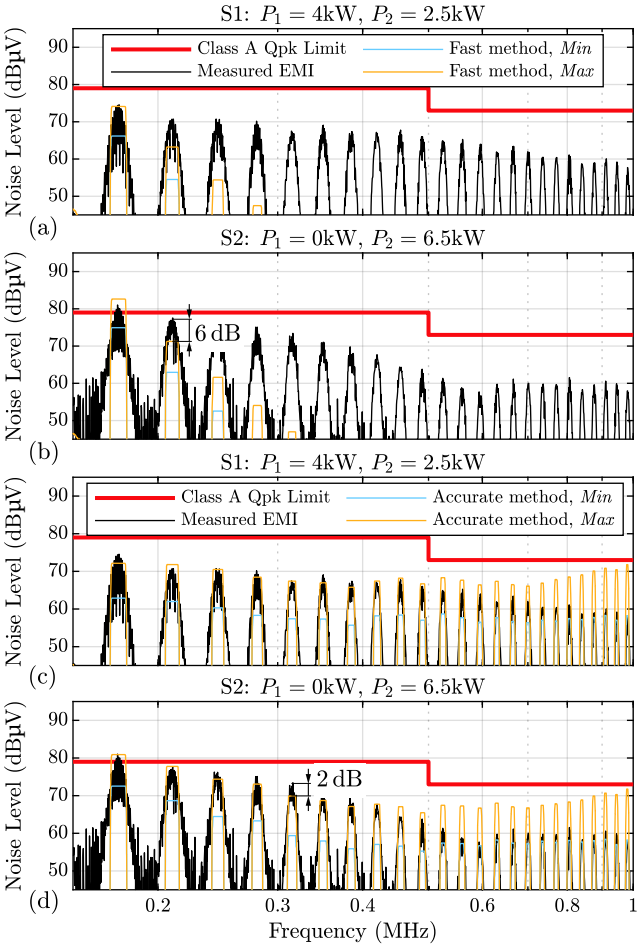

Fig. 2.19: Measured maximum peak EMI noise at phase c of the ac-LISN connected to the D3ABC. The converter operates as PFC rectifier with a three-phase voltage source connected to port ac$_1$ ($f_m = 50$ Hz, $V_{ac,rms} = 230$ V). The levels of EMI noise are measured for a total power of 6.5 kW and different distributions of the dc loads. The measured noise is compared to the *Min*/*Max* estimates obtained with the fast calculation method in (a) for $P_1 = 4$ kW and $P_2 = 2.5$ kW and in (b) for $P_1 = 0$ and $P_2 = 6.5$ kW and with the accurate calculation method in (c) for $P_1 = 4$ kW and $P_2 = 2.5$ kW and in (d) for $P_1 = 0$ and $P_2 = 6.5$ kW.

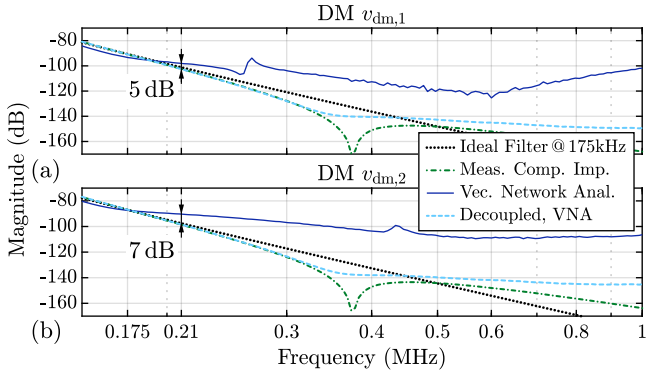

Fig. 2.20: Detailed view of the frequency responses depicted in Fig. 2.15(a) and Fig. 2.15(b). Each light blue dashed line shows the magnitude of the product of the measured TFs of the EMI filter and the converter without EMI filter, thus neglecting the parasitic couplings between converter and EMI filter. This has up to a frequency of $f = 450$ kHz a lower attenuation than predicted by the calculation (dotted line). The resonance at approximately 350 kHz is the self-resonance of the large filter capacitance C_{f1}.

Fig. 2.19(c) and **Fig. 2.19(d)** depict the results for S1 and S2, respectively. For this method, the measured EMI noise levels are mostly located between $V_{emi,min}$ and $V_{emi,max}$, revealing a good agreement between measured and estimated noise levels over the entire frequency range under consideration. The remaining mismatch of up to 2 dB at certain frequencies, e.g., at $f = 315$ kHz indicated in Fig. 2.19(d), can be explained by component tolerances (supported by the measured difference of EMI noise of 3.5 dB between phases) or neglected noise sources, such as the gate driver supply, which is operated at a switching frequency of $f \approx 350$ kHz.

Thus, although all the curves of the *Min*/*Max* estimates shown in Fig. 2.19 have been determined on the basis of calculated voltage waveforms, substantially different results are obtained depending on whether the fast or the exact calculation method is used. Therefore, it can be assumed that the total attenuation of the conducted EMI, i.e., from the noise source to the ac-LISN, does not reach the calculated values. Since the DM EMI noise components in the frequency range up to 400 kHz predominate the CM components in the noise calculations, it is appropriate to examine the achieved total DM attenuation of filter and converter in more details.

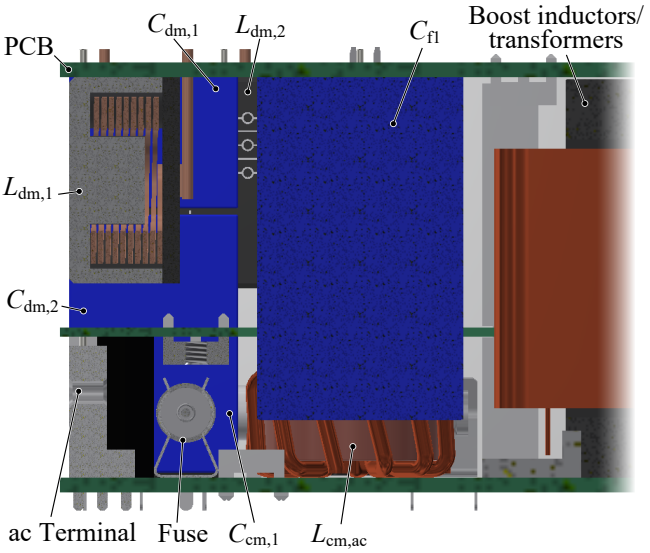

Fig. 2.21: Cross-sectional view created with a Computer Aided Design (CAD) software along the plane shown in Fig. 2.13(a) showing a part of the EMI filter. To achieve high power density, as required for industry-like demonstrator systems, the components are densely packed. This can lead to parasitic couplings between the converter and the EMI filter and between the different EMI filter stages.

As shown in **Fig. 2.20(a,b)**, the measured TFs of the DM EMI propagation paths (solid blue curves) achieve a lower attenuation than the calculated TFs already at the second harmonic, at 210 kHz (5 dB for $v_{\mathrm{dm},1}$ and 7 dB for $v_{\mathrm{dm},2}$). These discrepancies are also visible in Fig. 2.19(a,b) as a difference of 6 dB (only marked in Fig. 2.19(b)). However, if the TFs of the converter without filter and the filter itself are measured separately with a VNA and the resulting TFs are multiplied together, the dashed light blue curves in Fig. 2.20(a,b) result, which would reveal a substantially higher attenuation of up to 140 dB up to 1 MHz. At the interface between converter and EMI filter, the converter has the three filter capacitances C_{fl} and the EMI filter has the three filter inductances $L_{\mathrm{dm},1}$. The measured impedance $Z_{C\mathrm{fl}}$ is more than a factor of 100 smaller than the measured impedance $Z_{L\mathrm{dm},1}$ in the frequency range considered. Consequently, issues related to the input and output impedances at the interface between the converter and the EMI filter can be practically excluded. However, the reduced attenuation can be explained by means of parasitic couplings between the components of the EMI filter and the converter, since all components are densely packed to achieve a high power density of the converter. For example, the cross-sectional drawing of the converter shown in **Fig. 2.21** (i.e., along the plane shown in Fig. 2.13(a)) indicates that there is only a small gap between the large converter filter capacitor C_{fl} and the EMI filter capacitor $C_{\mathrm{dm},2}$. This leads to an increase in a parasitic capacitance that can be considered to be in parallel with several filter components ($L_{\mathrm{dm},1}$, $C_{\mathrm{dm},1}$, $L_{\mathrm{dm},2}$, $L_{\mathrm{cm},1}$). Consequently, this is a possible reason for the reduced attenuation of the realized EMI filter.

2.6 Conclusion

This chapter considers the D3ABC topology as a three-phase PFC rectifier without and with galvanic isolation, where the three-phase ac lines are connected to the primary-side ac port, ac_1, and different loads are connected to the primary- and secondary-side dc ports, dc_1 and dc_2. After a description of the general principle of operation of the investigated converter, models for calculating the conducted DM and CM EMI noises at the primary-side ac port, ac_1, are derived. These models prove valuable in the following aspects:

1. They provide a detailed insight regarding the sources and the propagation paths of conducted EMI in the D3ABC. In this regard, the main finding is that the level of conducted EMI noise at port ac_1 increases for increasing power at port dc_2, P_2, and that the EMI noise is almost independent of the power at port dc_1, P_1.

2. They enable the systematic design and optimization of the EMI filter for given specifications at an early stage of the converter design. This has been explained in the context of an example, for given dc link voltages (i.e., $V_{\mathrm{dc},1} = 800\,\mathrm{V}$, $V_{\mathrm{dc},2} = 400\,\mathrm{V}$), $P_2 = 2.5\,\mathrm{kW}$, and the QP limit of conducted EMI defined by CISPR 11 class A. The designed EMI filter has a total volume of $0.17\,\mathrm{dm}^3 = 10.4\,\mathrm{in}^3$ ($0.09\,\mathrm{dm}^3 = 5.5\,\mathrm{in}^3$ for the DM filter and $0.08\,\mathrm{dm}^3 = 4.9\,\mathrm{in}^3$ for the CM filter part) achieving together with the main part of the converter a volume of $1.94\,\mathrm{dm}^3$.

3. They correctly predict the conducted EMI noise at the ac port in the frequency range close to 150 kHz, where the largest magnitudes occur in the spectrum of the (unfiltered) EMI noise. Deviations at higher frequencies are due to parasitic effects (i.e., parasitic capacitances, inductances, and couplings between components) that are not accounted for in the simplified models.

A hardware demonstrator of the D3ABC topology, which includes the designed EMI filter, serves for the experimental verification of the derived models for conducted EMI noise. The measured frequency responses of the TFs from the EMI noise sources of the converter to the port ac_1 are in good agreement with the frequency responses predicted by the models up to a frequency of 200 kHz. In this regard, the model correctly predicts the increase in conducted EMI noise as a result of an increase of the power at port dc_2 from $P_2 = 2.5\,\mathrm{kW}$ to $P_2 = 6.5\,\mathrm{kW}$ (with a simultaneous decrease of the power at port dc_1 from $P_1 = 4\,\mathrm{kW}$ to $P_1 = 0$). Finally, the measurements of conducted EMI noise show that the hardware demonstrator meets the QP limit defined by CISPR 11 class A for $P_1 = 4\,\mathrm{kW}$ and $P_2 = 2.5\,\mathrm{kW}$.

3

Advanced Modulation for Four-Port Operation of the D3ABC

Chapter Abstract

This chapter investigates the operation of the Dual Three-Phase Active Bridge Converter (D3ABC) topology as a multi-port converter, by taking power transfers between all four ports of the converter, i.e., the two three-phase ac ports (ac_1 and ac_2) and the two dc ports (dc_1 and dc_2), into acount. The basic working principle of the D3ABC topology under multi-port operation and a strategy to achieve independent power transfer between the four ports are described. It has been found challenging to operate the converter if ac voltages with different line frequencies, $f_1 \neq f_2$, are present at the ports ac_1 and ac_2. Such operation causes LF power pulsations in the converter's dc links, leading to fluctuating dc link voltages and distorted phase currents. Therefore, a new duty-cycle dependent phase shift modulation scheme is proposed that eliminates such LF power pulsations. The new modulation scheme is developed on the basis of analytical considerations, which are supported by the results of numerical calculations, and verified by means of circuit simulations and experimental results. The hardware demonstrator designed for a rated power of 8 kW when operated from ac_1 to dc_2 at the European low-voltage ac mains ($V_{ac,1} = 230$ V rms line-to-neutral, $V_{dc,1} = 800$ V, $V_{dc,2} = 400$ V) is used for experimental verification. Since the operation with $f_1 \neq f_2$ leads to an increase of the currents in the converter, the experimental verification is conducted at half voltages resulting in a reduced power of 2 kW that is transferred from ac_1 to ac_2 at substantially different primary-side and secondary-side line frequencies of $f_1 = 50$ Hz and $f_2 = 77$ Hz. The measured results agree well with the simulated results. In particular, the dc link voltages show almost constant waveforms, which confirms the correct operation of the proposed modulation scheme.

3.1 Introduction

The D3ABC shown in **Fig. 3.1** provides four ports (two ac ports and two dc ports). Until here, only power transfer from the port ac_1 to the ports dc_1 and dc_2 has been investigated in this thesis. However, the primary-side and secondary-side structures of the D3ABC topology are the same, i.e., the converter mainly consists of a primary-side and a secondary-side two-level three-phase VSC. In addition, the ac-side inductor of each phase of the primary-side VSC shares the magnetic core with the ac-side inductor of the same phase of the secondary-side VSC, to achieve a magnetic coupling. The non-ideal coupling of the inductor windings allows galvanically isolated power transfer in each phase similar to a DAB converter. Accordingly, the D3ABC can be regarded as an integration of two three-phase VSCs and three DAB converters, which features an inherent symmetry with respect to the galvanic isolation barrier that separates the primary and secondary sides. Therefore, it is expected that the D3ABC allows for power transfers between all four ports.

In case of the D3ABC, the integration of several converter stages into a single converter stage is achieved by using the switching nodes of the half-bridges for multiple purposes. As a result, certain degrees of freedom are lost, which leads to various limitations. It turns out that the operation with non-synchronous input and output voltage waveforms, e.g., with different line frequencies, $f_1 \neq f_2$, at the primary-side ac port ac_1 and the secondary-side ac port ac_2, may cause LF power pulsations between the two dc links. This LF power pulsation is not sinusoidal but has a spectrum with a fundamental frequency component at $|f_1 - f_2|$.

If, for example, the grid frequency is $f_1 = 50.0\,\mathrm{Hz}$ at port ac_1 and $f_2 = 50.1\,\mathrm{Hz}$ at port ac_2, power pulsation with fundamental frequency of $|f_1 - f_2| = 0.1\,\mathrm{Hz}$ can occur in the primary-side and secondary-side dc links. These can lead to unacceptable fluctuations of the dc link voltages. Usually, these voltage fluctuations are counteracted by suitably adjusting the dc link capacitances [72], improving the utilizations of the dc link capacitors by using power pulsation buffers [73], or by involving an alternative means of energy storage, such as the kinetic energy stored in a rotating electric motor [74]. Alternatively, large filter capacitances connected to the ac ports could absorb the power pulsation. These filter capacitances could also be implemented as solid-state variable capacitors, as, e.g., shown in [75] and [76] for single-phase systems. However, since the minimum required storage capacities are inversely proportional to the frequency of the pulsation [77] and the

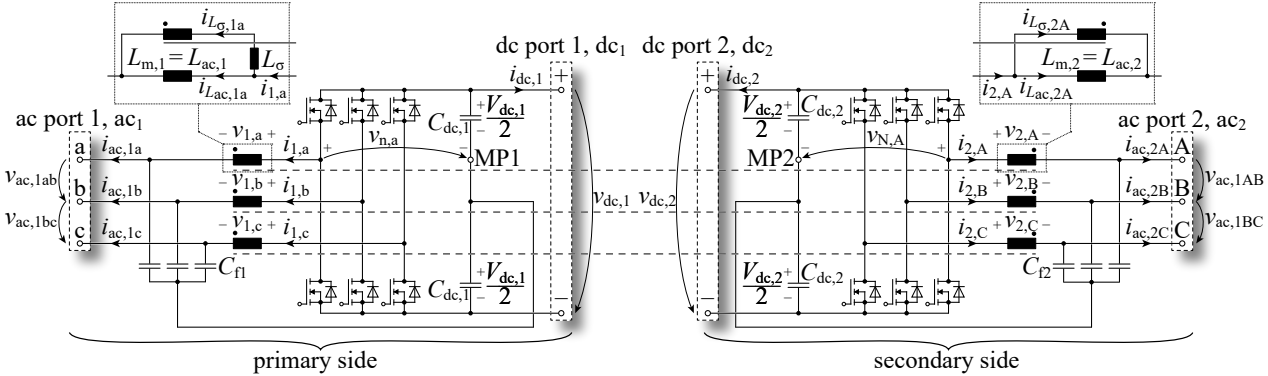

Fig. 3.1: Dual Three-Phase Active Bridge Converter (D3ABC) with primary-side ac and dc ports (ac_1, dc_1) and galvanically isolated secondary-side ac and dc ports (ac_2, dc_2) in the considered multi-port configuration with two dc sources/loads connected to the dc ports and two three-phase sources/loads connected to the ac ports. This illustration corresponds to the circuit in Fig. 2.1 (without EMI filter) but uses a π-type instead of the T-type equivalent circuit for the transformer.

frequency of the power pulsation can take on very small frequencies down to zero (0.1 Hz in the example described above), the issue actually cannot be solved in this way. Alternatively, the pulsating power could be supplied to the grid. However, a related study concludes that LF power pulsations can be subject to very restrictive limits, especially in the context of flicker [78], which rules out this option. Accordingly, the only remaining option is to adapt the modulation scheme such that pulsating power is suppressed in the dc links.

This chapter describes first in **Section 3.2** the multi-port operation of the D3ABC. Subsequently, a new modulation scheme for elimination of LF power pulsations is derived in **Section 3.3**. Finally, **Section 3.4** verifies the derived modulation scheme through circuit simulations and measurements on the hardware demonstrator.

3.2 Multi-Port Operation of the D3ABC

The systematic description of the operation of the D3ABC with different line frequencies at the ports ac_1 and ac_2 and the consequences of this kind of operation of the D3ABC, is divided into the four steps listed in the following.

1. The extension of the ac_1–dc_1/dc_2 operating principle of the D3ABC (cf. Section 2.2) to four-port, i.e., ac_1–dc_1/dc_2-ac_2 operation in **Subsection 3.2.1**.

2. The investigation of the known operation with synchronized three-phase ac voltages at the ports ac_1 and ac_2 (same line frequencies and no phase shift) in **Subsection 3.2.2**.

3. The operation with three-phase ac voltages with different line frequencies at ac_1 and ac_2 in **Subsection 3.2.3**.

3.2.1 Operating principle for a ac_1–dc_1/dc_2–ac_2 multi-port operation

This section extends the description of the operating principle of the D3ABC given in Section 2.2 by ac_1–dc_1/dc_2–ac_2 multi-port operation. In this chapter, symmetric three-phase systems are considered at the primary-side and secondary-side ac ports. Accordingly, three sinusoidal voltages are present at

Tab. 3.1: Parameters for the three operating scenarios considered. The given values for the ac voltages are the rms values of the line-to-neutral voltages.

Parameter	Var.	S1	S2	S3	S4
ac_1 voltage	$V_{ac,1}$	230 V	230 V	230 V	115 V
ac_1 line frequency	f_1	50 Hz	50 Hz	50 Hz	50 Hz
dc_1 voltage	$V_{dc,1}$	800 V	800 V	800 V	400 V
ac_2 voltage	$V_{ac,2}$	115 V	115 V	115 V	57.5 V
ac_2 line frequency	f_2	50 Hz	77 Hz	77 Hz	77 Hz
dc_2 voltage	$V_{dc,2}$	400 V	400 V	400 V	200 V
Power at port ac_1	$P_{ac,1}$	−7 kW	−7 kW	−8 kW	−2 kW
Power at port dc_1	$P_{dc,1}$	−1 kW	−1 kW	0	0
Power at port ac_2	$P_{ac,2}$	6 kW	6 kW	8 kW	2 kW
Power at port dc_2	$P_{dc,2}$	2 kW	2 kW	0	0

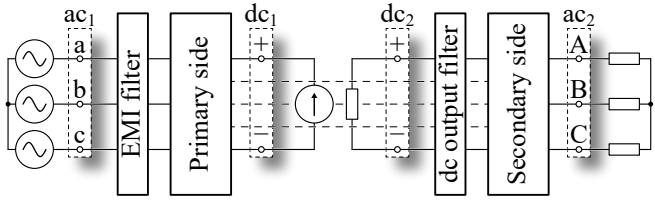

Fig. 3.2: Considered configuration of sources and loads for all circuit simulations and all measurements performed on the hardware demonstrator. The exact structure and component values of the EMI filter and the dc output filter can be found in **Chapter 2**. Since the hardware demonstrator was built for a rectifier operation between ports ac_1 and dc_2, ports dc_1 and ac_2 have no additional input/output filters.

ac_1 and ac_2, respectively,

$$v_{ac,1,a,b,c}(t) = \sqrt{2} V_{ac,1} \sin\left(2\pi f_1 t + \theta_{a,b,c}\right), \tag{3.1}$$

$$v_{ac,2,A,B,C}(t) = \sqrt{2} V_{ac,2} \sin\left(2\pi f_2 t + \theta_{A,B,C} + \Theta\right). \tag{3.2}$$

Here, $V_{ac,1}$ and $V_{ac,2}$ denote the rms values of the phase voltages, f_1 and f_2 denote the line frequencies, $\theta_{a,b,c} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$ and $\theta_{A,B,C} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$ the phase shifts of the primary-side and/or secondary-side phase voltages, respectively, and Θ the phase shift between the primary-side and secondary-side phase voltage systems.

In this chapter, three different operating scenarios, S1 to S4, are considered: S1 refers to multi-port operation with synchronized line voltages, S2

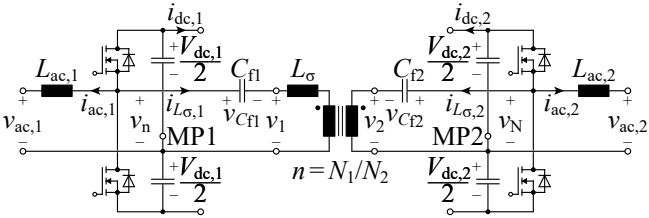

Fig. 3.3: Single-phase equivalent circuit with primary-side and secondary-side boost inductances, $L_{ac,1}$ and $L_{ac,2}$, stray inductance, L_σ, and ideal isolating HF transformer with turns ratio n.

to multi-port operation with different line frequencies, S3 to ac/ac operation with different line frequencies, and S4 to ac/ac operation with different line frequencies and reduced voltages as used for the hardware demonstrator. **Table 3.1** lists the parameters for S1 to S4. In this context, it is noted that the sign of the power is defined in the generator reference system, as seen by the D3ABC. Accordingly, a power flow directed from the D3ABC to an external component (e.g., a resistor) has a positive sign. A negative power is present if the power flow at the port under consideration is directed into the converter system. In the context of the bidirectional conversion capability of the D3ABC, this careful definition serves to unambiguously define the operating condition present at each port. **Fig. 3.2** shows the considered configuration of sources and loads, both for the circuit simulations and for the measurements performed on the hardware demonstrator. The resistor values are chosen so that the powers listed in Table 3.1 result. For scenarios S3 and S4, the current source at dc_1 and the resistor at dc_2 are removed.

As described in Section 2.2, the D3ABC can be divided into three independent converter systems, i.e., one converter system per phase. **Fig. 3.3** depicts the considered equivalent circuit of such a single-phase converter system. The primary-side dc link circuits of the three single-phase converter systems are combined in parallel connection and the secondary-side dc link circuits are also connected in parallel.

The energy exchange between ac_1 and the dc link capacitor connected to dc_1 is accomplished in analogy to a VSC. According to Section 2.2 the voltage across the filter capacitor v_{Cf1} is approximately equal to the line voltage. This applies for the secondary side as well, due to the symmetry of the D3ABC. Assuming that the ac-side filter inductors have low impedance at line frequency, the local averages value of the switched voltages generated by

the half-bridges (e.g., $v_{\mathrm{n,a}}$ and $v_{\mathrm{N,A}}$ for phase a in Fig. 3.1), calculated according to (2.4), are approximately equal to the voltages across the filter capacitros. Therefore,

$$\langle v_{\mathrm{n}} \rangle_{T_{\mathrm{s}}} = \left(D_1 - \frac{1}{2} \right) V_{\mathrm{dc,1}} \approx v_{C\mathrm{f1}} \approx v_{\mathrm{ac,1}}, \tag{3.3}$$

$$\langle v_{\mathrm{N}} \rangle_{T_{\mathrm{s}}} = \left(D_2 - \frac{1}{2} \right) V_{\mathrm{dc,2}} \approx v_{C\mathrm{f2}} \approx v_{\mathrm{ac,2}}, \tag{3.4}$$

result where D_1 and D_2 denote the relative turn-on times of the high-side transistors of the primary- and secondary-side inverters, respectively. These expressions can be modified in terms of the phases a, A, b, B and c, C, leading to the relations

$$D_{\mathrm{1,a,b,c}}(t) \approx \frac{1}{2} \left[1 + m_1 \sin\left(2\pi f_1 t + \theta_{\mathrm{a,b,c}} \right) \right], \tag{3.5}$$

$$D_{\mathrm{2,A,B,C}}(t) \approx \frac{1}{2} \left[1 + m_2 \sin\left(2\pi f_2 t + \theta_{\mathrm{A,B,C}} + \Theta \right) \right], \tag{3.6}$$

for the duty cycles of the six half-bridges. The method to control the power transfer between the ports ac_1 and dc_1 depends on what ac_1 is connected to. If ac_1 is connected to a three-phase resistive load, it is sufficient to set the three-phase ac voltages using the duty cycles calculated according to (3.5). If ac_1 is connected to a three-phase grid, a closed-loop control, e.g., the indirect current control described in [79], is used. This controller slightly adjusts $D_{\mathrm{1,a,b,c}}(t)$ in order to shape the mains-side phase currents according to the given requirements (e.g., sinusoidal with defined amplitude and in phase to the corresponding phase voltage). However, since the modulation scheme described in this paper is related to the operation of the DAB part of the D3ABC, it is irrelevant whether the duty cycles are determined by open- or closed-loop control. The same applies to the ports ac_2 and dc_2, whereas the power transfer between these two ports is controlled by slightly adjusting $D_{\mathrm{2,A,B,C}}$.

The energy exchange between the dc link capacitors connected to dc_1 and dc_2 is achieved in analogy to a DAB converter, i.e., the square-wave voltage (e.g. v_{n}) at the switching node of a primary-side half-bridge is shifted by a certain HF phase with respect to the square-wave voltage (e.g. v_{N}) at the switching node of the secondary-side half-bridge of the same converter phase. This leads to the formation of the typical transformer current of a DAB converter. The associated power flow between the primary-side and secondary-side dc link capacitors can be described using the local average

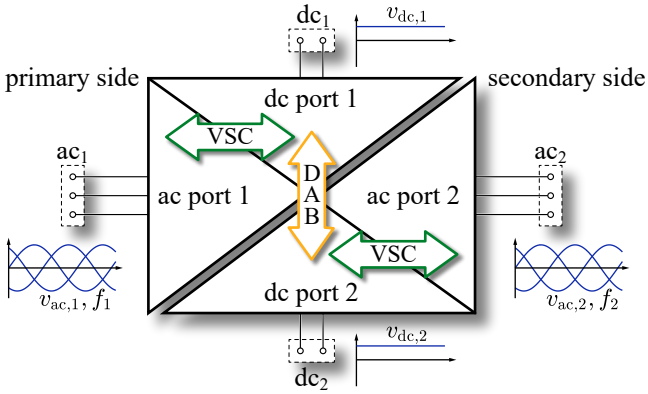

Fig. 3.4: The power transfer between the four ports of the D3ABC can be separated into ac_1–dc_1 and ac_2–dc_2 operation w/o galvanic isolation and dc_1/dc_2 operation w/ galvanic isolation. For ac_1–dc_1 and ac_2–dc_2 the corresponding VSCs are operated according to (3.5) and (3.6) to achieve PFC functionality. The power transfer dc_1/dc_2 is utilizing the DAB functionality, cf. (3.7).

value of the instantaneous power,

$$\langle p \rangle_{T_s}(t) = \langle p \rangle(t) = \frac{1}{T_s} \int_0^{T_s} p(t+\tau)\,\mathrm{d}\tau = \frac{1}{T_s} \int_0^{T_s} v_1(t+\tau)\; i_{L\sigma,1}(t+\tau)\,\mathrm{d}\tau. \quad (3.7)$$

Thereby the half-bridges on the primary and secondary sides are switched with the same switching frequency. **Fig. 3.4** illustrates the considered power transfers.

Fig. 3.5(a) exemplarily depicts the waveform of the primary-side transformer current in phase a, for operation according to S1 in Table 3.1 and over two mains periods. Since the switching frequency is much higher than the line frequency, the transformer current waveform, $i_{L\sigma,1}(t)$, appears as a continuous band.[1] **Fig. 3.5(b)** therefore shows a magnified view of a switching period in the region of the zero crossing of the line current ($t = 20\,\mathrm{ms}$), which

[1]The presumable phase shift of 180 ° between $v_{ac,1}$ and $i_{L\sigma,1}$ in Fig. 3.5(a) is not present in reality. Instead, the shape of the current band is a result of different positive and negative current peak values of $i_{L\sigma,1}(t)$ due to the DAB converter operation during a mains period. For more details, the reader is referred to Section II in [51].

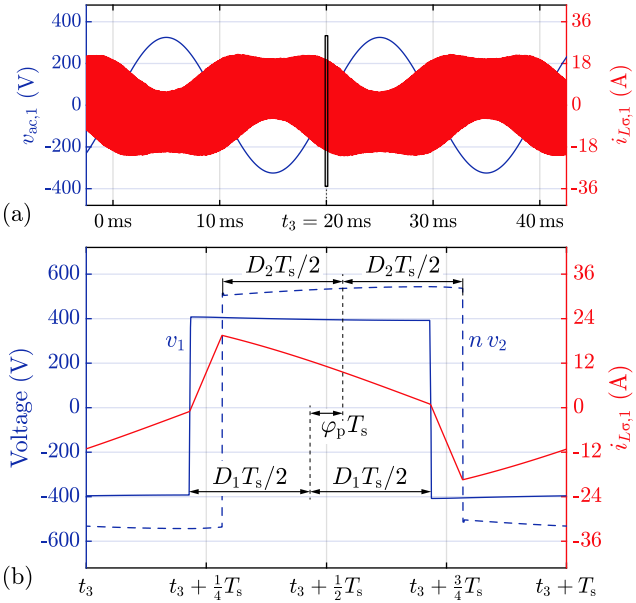

Fig. 3.5: Simulated voltage and current waveforms of phase a for operation according to S1 in Table 3.1. (a) Sinusoidal input voltage, $v_{ac,1}$, and primary-side transformer current, $i_{L\sigma,1}$. (b) Transformer current, $i_{L\sigma,1}$, together with the primary-side and secondary-side transformer voltages, v_1 and v_2, during one switching period, T_s, at $t_3 \approx 20$ ms. Subfigure (b) reveals the definitions of the duty cycles, D_1 and D_2, and the HF phase shift $\varphi_p = \frac{\varphi}{2\pi}$. Parameters as listed in Table 3.5.

reveals the characteristic waveform of the transformer current. It is worth noting that Fig. 3.5(b) is additionally used to define the duty cycles D_1 and D_2 and the HF phase shift φ_p. For phases a, b, and c the same picture results, except for a time displacement of $\pm 20\,\text{ms}/3 = \pm 6.67\,\text{ms}$.

3.2.2 Synchronized line voltages at ac_1 and ac_2

Fig. 3.6 presents the results of a circuit simulation for operation according to S1 in Table 3.1 and with synchronized line voltages at ac_1 and ac_2. In this context, Fig. 3.6(a) and Fig. 3.6(b) show the waveforms of the phase voltages and phase currents present at ac_1 and ac_2 as well as the dc voltages and dc currents present at dc_1 and dc_2 (it is to be mentioned that, for simplification, the dc link capacitors have been replaced by dc voltage sources in this simulation).

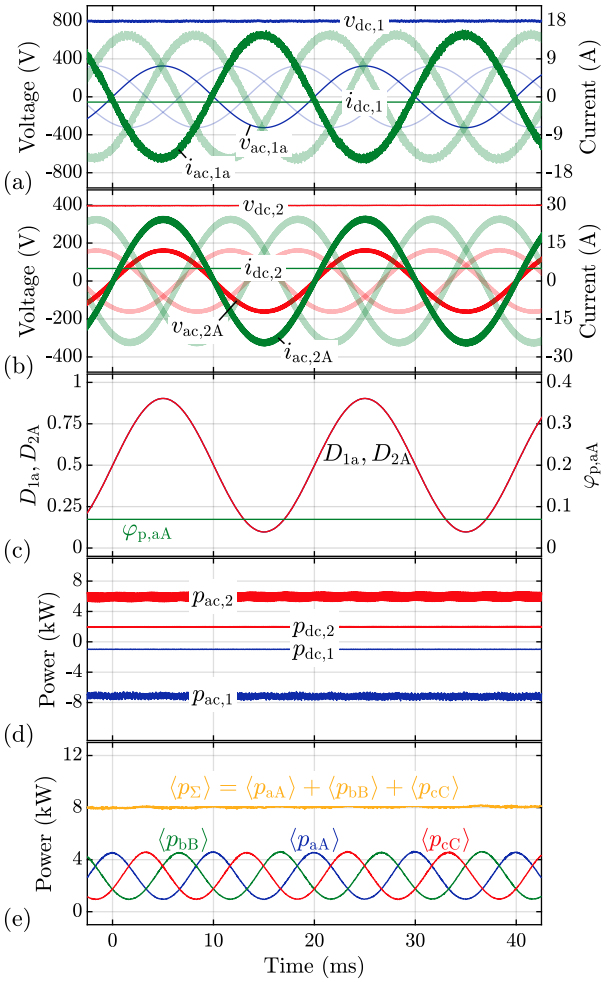

Fig. 3.6: Simulation results for the operation of the D3ABC with synchronized line voltages at the ports ac_1 and ac_2 (S1 in Table 3.1) using the parameters given in **Table 3.5**: (a) primary-side voltages and currents, (b) secondary-side voltages and currents, (c) duty cycles and the HF phase shift at phase a, (d) power levels at the four ports, and (e) local average values of the powers of the three DAB converter stages and the resulting total power, $\langle p_\Sigma \rangle$. Apart from switching-frequency fluctuations, the powers at the four ports and the total power of the DAB-part show practically constant waveforms, i.e., no LF components are present.

Fig. 3.6(c) depicts the waveforms of the duty cycles $D_{1a}(t)$ and $D_{2A}(t)$ as well as the HF phase shift $\varphi_{p,aA}$. Direct comparison of $v_{ac,1a}$ in Fig. 3.6(a) and $D_{1a}(t)$ in Fig. 3.6(c) reveals that, due to the relationship described by (3.3), $D_{1a}(t)-0.5$ is practically proportional to $v_{ac,1a}$ (the same is true for $D_{2A}(t)-0.5$ and $v_{ac,2A}$). Moreover, the modulation scheme described in [51] applies a constant HF phase shift, $\varphi_{p,aA}$, in the steady state.

Fig. 3.6(d) shows the instantaneous powers at the four ports of the D3ABC, which agree with the values for S1 listed in Table 3.1. It is well known that rectifier or inverter operation in the balanced three-phase system (e.g., power conversion between ac_1 and dc_1) results in a constant local average value of the power at the dc link. This explains the waveforms of $p_{ac,1}(t)$ and $p_{ac,2}(t)$ in this figure, which are practically constant except for switching-frequency fluctuations.

Fig. 3.6(e) reveals the waveforms of the local average values of the powers of the three DAB converter stages, $\langle p_{aA}\rangle$, $\langle p_{bB}\rangle$, and $\langle p_{cC}\rangle$, which, for the investigated mode of operation, are sinusoidal and phase-shifted with respect to each other by $\pm 120^\circ$. Accordingly, the total power of the DAB part of the D3ABC,

$$\langle p_\Sigma\rangle = \langle p_{aA}\rangle + \langle p_{bB}\rangle + \langle p_{cC}\rangle, \tag{3.8}$$

is constant. For this reason, no power pulsations with frequencies in the range of the line frequencies occur at the dc link capacitors, which allows the realization of the converter with comparably small dc link capacitors.

3.2.3 Operation with different line frequencies at ac_1 and ac_2

Fig. 3.7 presents the results of a circuit simulation for operation according to S2 in Table 3.1, i.e., for a line frequency of $f_2 = 77\,\mathrm{Hz}$ at ac_2. Accordingly, the voltages of corresponding phases of the three-phase system of the primary side [Fig. 3.7(a)] and the secondary side [Fig. 3.7(b)] are not synchronous anymore. According to (3.3) and (3.4), this leads to unequal duty cycles in corresponding converter phases (e.g., primary-side phase a and secondary-side phase A), as shown in the example of phases a and A in Fig. 3.7(c).

The sum of the powers in the three DAB converter stages, $\langle p_\Sigma\rangle$, shown in Fig. 3.7(e) contains pronounced LF components, in contrast to the simulation with $f_1 = f_2$ shown in Fig. 3.6(e). The pronounced LF components in $\langle p_\Sigma\rangle$ lead to variations in the dc link voltages and distortions in the phase currents. Since the phase current controller (implemented as described in [79]) keeps

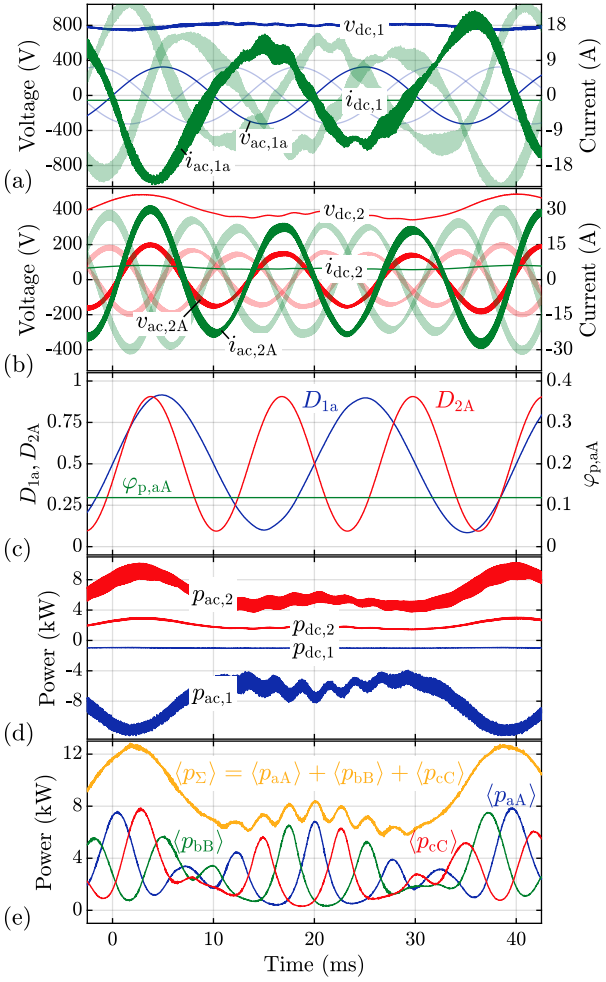

Fig. 3.7: Simulation results for converter operation according to S2 in Table 3.1, i.e., for a line frequency of $f_2 = 77\,\text{Hz}$ at ac_2: (a) primary-side voltages and currents, (b) secondary-side voltages and currents, (c) duty cycles and the HF phase shift at phase a, (d) power levels at the four ports, and (e) local average values of the powers of the three DAB converter stages and the resulting total power, $\langle p_\Sigma \rangle$. The pronounced LF components in $\langle p_\Sigma \rangle$ lead to fluctuating dc link voltages and distorted phase currents. As a result, the powers at the dc and ac ports are no longer constant.

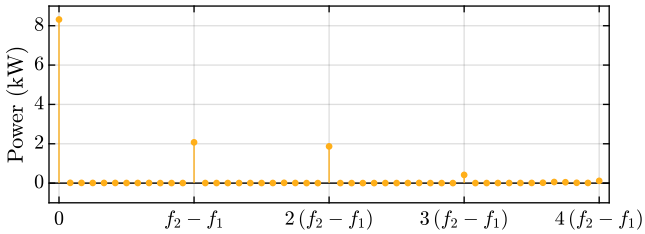

Fig. 3.8: The total power in the DAB part of the D3ABC, $\langle p_\Sigma \rangle$, as shown in Fig. 3.7(e), in the frequency domain. In addition to the dc component with a power of $\approx 8\,\mathrm{kW}$, spectral components at $f_2 - f_1 = 27\,\mathrm{Hz}$ and $2(f_2 - f_1) = 54\,\mathrm{Hz}$ are clearly visible.

the voltage on the primary-side dc link almost constant, a major part of the power pulsation is transferred to ac_1 and thus to the grid. However, the dc link voltage on the secondary side is not controlled (HF phase shift is kept constant) and therefore the power pulsation is split between the ports dc_2 and ac_2. This explains the non-constant power waveforms for the three ports ac_1, dc_2, and ac_2 shown in Fig. 3.7(d).

The non-sinusoidal total power, $\langle p_\Sigma \rangle$, plotted in Fig. 3.7(e) reveals spectral components at $f_2 - f_1 = 27\,\mathrm{Hz}$ and $2(f_2 - f_1) = 54\,\mathrm{Hz}$ in addition to the dc component with a power of $\approx 8\,\mathrm{kW}$, as shown in **Fig. 3.8**. As described in the introduction, especially the component at $f_2 - f_1$ is a challenge for filtering and should therefore be eliminated by using a suitable advanced modulation scheme.

3.3 Elimination of LF Power Pulsation

Based on the consideration that symmetric three-phase systems are present at the primary-side and secondary-side ac ports, the LF components in $\langle p_\Sigma \rangle$ exclusively occur in the DAB part of the D3ABC, as discovered in Subsection 3.2.3. Furthermore, according to (3.5) and (3.6), the waveforms of the three-phase line voltages at ac_1 and ac_2 already specify the waveforms of the primary-side and secondary-side duty cycles. Hence, only the HF phase shifts, $\varphi_{\mathrm{p,aA}}$, $\varphi_{\mathrm{p,bB}}$, and $\varphi_{\mathrm{p,cC}}$, remain as degrees of freedom to eliminate the LF power pulsations. This also implies that the power flow between the ports ac_1 and dc_1 or between ac_2 and dc_2 has no influence on LF components in the currents of the dc link capacitors. Consequently, the powers at dc_1 and dc_2 can be set to zero without limiting the generality.

It is to be noted that the derivations of the modulation schemes derived in this chapter can be largely based on the study of a single DAB converter phase, i.e., the DAB converter part of Fig. 3.3. Accordingly, the indices denoting the converter phases are omitted in these derivations to provide a more comprehensible description. Thus, the variables used in the course of the investigation of a single phase of the DAB part of the converter, e.g., p, D_1, D_2, or φ_p are to be replaced by the variables of the converter phase to be evaluated, e.g., by p_aA, $D_\mathrm{1,a}$, $D_\mathrm{2,A}$, and $\varphi_\mathrm{p,aA}$ in case of converter phases a-A.

3.3.1 DAB operating modes

In order to identify possible functions for the the phase shift φ_p that eliminate the power pulsation in the DAB converter part, the relation between phase shift and local average value of the instantaneous power $\langle p \rangle$ is investigated in a first step. According to (3.7), $\langle p \rangle$ depends on the waveforms of $v_1(t)$ and $i_{L\sigma,1}(t)$. The waveform of $i_{L\sigma,1}(t)$ depends on $v_1(t)$ and $n\,v_2(t)$, since the time derivative of $i_{L\sigma,1}(t)$ is proportional to the voltage across L_σ, which is equal to

$$\frac{\mathrm{d}i_{L\sigma,1}(t)}{\mathrm{d}t} = \frac{v_1(t) - n\,v_2(t)}{L_\sigma}, \tag{3.9}$$

given the circuit in Fig. 3.3. Consequently $i_{L\sigma,1}(t)$ results by integrating this voltage as

$$i_{L\sigma,1}(t) = I_0 + \int_0^t \left(\frac{\mathrm{d}i_{L\sigma,1}(\tau)}{\mathrm{d}\tau} \right) \mathrm{d}\tau, \tag{3.10}$$

where I_0 denotes the initial current at $t = 0$. For this reason, the waveform of $i_{L\sigma,1}(t)$ depends on $v_1(t)$ and $n\,v_2(t)$ and, subsequently, on D_1, D_2, and φ_p as defined in **Fig. 3.9**.

For the assumption that during a switching period the dc link voltages $V_\mathrm{dc,1}$ and $V_\mathrm{dc,2}$ and the voltages across the filter capacitors are constant, the voltage across L_σ changes at four points in time during this switching period, i.e., whenever a rising or a falling edge of $v_1(t)$ or $v_2(t)$ occurs. The instants of these events are termed $t_{1\uparrow}$, $t_{1\downarrow}$, $t_{2\uparrow}$, and $t_{2\downarrow}$, where the subscripts refer to rising ($\uparrow$) and falling ($\downarrow$) edges of $v_1(t)$ and $v_2(t)$, respectively. If $t_{1\uparrow}$ is used as a reference, the subsequent instants $t_{1\downarrow}$, $t_{2\uparrow}$, and $t_{2\downarrow}$ can occur in any order, as defined by the duty cycles, D_1 and D_2, and the phase shift, φ_p. In total, six permutations of $\{t_{1\downarrow},\ t_{2\uparrow},\ t_{2\downarrow}\}$ can be distinguished, representing the six operating modes of this DAB converter, which are consecutively numbered

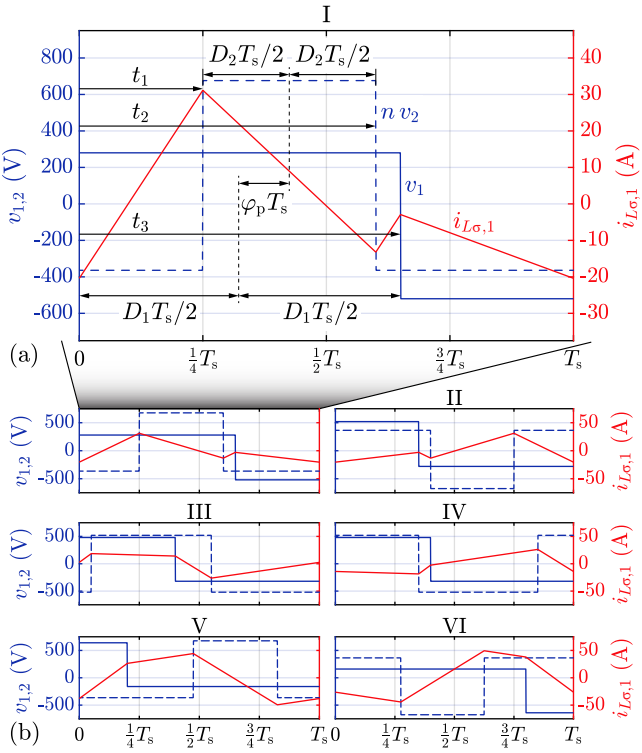

Fig. 3.9: (a) Definitions of D_1, D_2, and load angle φ with calculated waveforms over one switching period, T_s, with $2\pi f_s L_\sigma \approx 21\,\Omega$, $n = 2.6$, $V_{dc,1} = 800\,V$, $V_{dc,2} = 400\,V$, $D_1 = 0.4$, $D_2 = 0.5$ and $\varphi_p \approx 0.08$ and (b) all possible operating modes for this DAB converter.

with I to VI. Fig. 3.9(b) shows example waveforms for $v_1(t)$, $n\,v_2(t)$, and $i_{L\sigma,1}(t)$ for the six operating modes.

By way of example, (3.7) and (3.10) are evaluated for operating mode I, cf. Fig. 3.9(a), which features four time intervals with constant voltage across L_σ that are delimited with the times t_1, t_2, t_3, and T_s. The voltages $v_1(t)$ and $v_2(t)$ for operating mode I are defined as

$$v_1(t) = \begin{cases} +\frac{V_{\mathrm{dc},1}}{2} - v_{C\mathrm{f}1} & \forall \quad 0 \le t < t_2, \\ -\frac{V_{\mathrm{dc},1}}{2} - v_{C\mathrm{f}1} & \forall \quad t_2 \le t < T_\mathrm{s}, \end{cases} \tag{3.11}$$

$$v_2(t) = \begin{cases} -\frac{V_{\mathrm{dc},2}}{2} + v_{C\mathrm{f}2} & \forall \quad 0 \le t < t_1, \\ +\frac{V_{\mathrm{dc},2}}{2} + v_{C\mathrm{f}2} & \forall \quad t_1 \le t < t_3, \\ -\frac{V_{\mathrm{dc},2}}{2} + v_{C\mathrm{f}2} & \forall \quad t_3 \le t < T_\mathrm{s}, \end{cases} \tag{3.12}$$

with

$$t_1 = T_\mathrm{s}\left(\frac{D_1 - D_2}{2} + \varphi_\mathrm{p}\right),\ t_2 = T_\mathrm{s}\left(\frac{D_1 + D_2}{2} + \varphi_\mathrm{p}\right),\ \text{and}\ t_3 = T_\mathrm{s}\,D_1, \tag{3.13}$$

whereas the voltages across the filter capacitors $C_{\mathrm{f}1}$ and $C_{\mathrm{f}2}$ are given in (3.3) and (3.4), respectively. With the assumption of constant voltages across the filter capacitors, the average of the current $i_{L\sigma,1}$ has to be zero, allowing to solve for the current $I_{0,\mathrm{I}}$ resulting in

$$I_{0,\mathrm{I}} = \frac{1}{2L_\sigma}\left[nV_{\mathrm{dc},2}\,D_2\left(1 - D_1 - 2\varphi_\mathrm{p}\right) - V_{\mathrm{dc},1}\,D_1\left(1 - D_1\right)\right] \tag{3.14}$$

for mode I. With (3.9)-(3.14), (3.7) is evaluated for operating mode I resulting in

$$P_\mathrm{I} = P_0\left[\varphi_\mathrm{p}\,2D_2\left(1 - D_1\right)\right] \tag{3.15}$$

where P_0 contains all hardware-specific values,

$$P_0 = \frac{T_\mathrm{s}\,V_{\mathrm{dc},1}\,nV_{\mathrm{dc},2}}{2L_\sigma}. \tag{3.16}$$

For the operating modes II-VI, the expressions for P_II to P_VI are determined in the same manner.

Thereafter, the expressions for P_I to P_VI are solved with respect to φ_p for a given power level $P_{\mathrm{I-VI}} = P$ ($P > 0$ refers to power transferred from dc_1 to dc_2). It is found that operating modes V and VI are redundant, i.e., the same power is achieved with operating modes I to IV. However, operating modes V and VI

Tab. 3.2: Conditions for operating modes I to IV and solutions for the phase shift, φ_p, for each operating mode that sets the power level of a single DAB converter phase equal to the reference power, P.

Mode	Conditions	φ_p
I	$\lvert\varphi_\mathrm{p}\rvert < \frac{D_1-D_2}{2} \wedge D_1 > D_2$	$\varphi_{\mathrm{p,I}} = \frac{e_1}{2D_2(1-D_1)}$
II	$\lvert\varphi_\mathrm{p}\rvert < \frac{D_2-D_1}{2} \wedge D_1 < D_2$	$\varphi_{\mathrm{p,II}} = \frac{e_1}{2D_1(1-D_2)}$
III	$\varphi_\mathrm{p} > \frac{\lvert D_1-D_2\rvert}{2} \wedge \varphi_\mathrm{p} < \frac{D_1+D_2}{2}$	$\varphi_{\mathrm{p,III}} = e_3 - \sqrt{e_2 - e_1}$
IV	$\varphi_\mathrm{p} < -\frac{\lvert D_1-D_2\rvert}{2} \wedge \varphi_\mathrm{p} > -\frac{D_1+D_2}{2}$	$\varphi_{\mathrm{p,IV}} = -e_3 + \sqrt{e_2 + e_1}$
	$e_1 = P/P_0$	
	$e_2 = D_1\,(1-D_1)\,D_2\,(1-D_2)$	
	$e_3 = \frac{1}{2}\left[D_1\,(1-D_2) + D_2\,(1-D_1)\right]$	

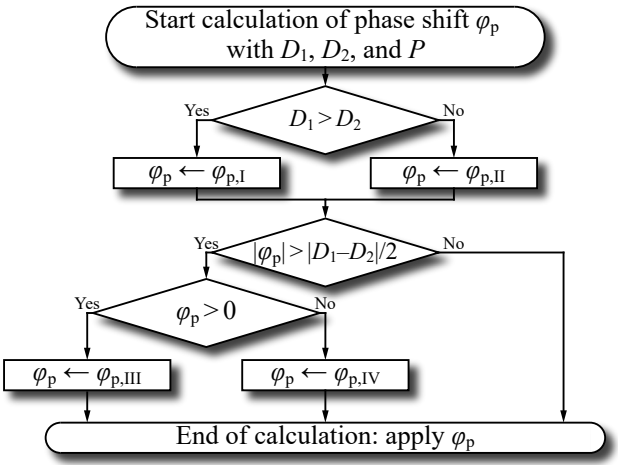

Fig. 3.10: Algorithm used to determine the current operating mode of the DAB and to calculate the HF phase shift φ_p, as given in **Table 3.2**.

Tab. 3.3: Expressions for the minimum and maximum power levels, $P_{\mathrm{I-IV,min}}$ and $P_{\mathrm{I-IV,max}}$, that are feasible in each operating mode.

	φ_p	Power
I	$\frac{D_1-D_2}{2}$	$P_{\mathrm{I,max}} = P_0\,[D_2\,(1-D_1)\,(D_1-D_2)]$
	$\frac{D_2-D_1}{2}$	$P_{\mathrm{I,min}} = P_0\,[-D_2\,(1-D_1)\,(D_1-D_2)]$
II	$\frac{D_2-D_1}{2}$	$P_{\mathrm{II,max}} = P_0\,[D_1\,(1-D_2)\,(D_2-D_1)]$
	$\frac{D_1-D_2}{2}$	$P_{\mathrm{II,min}} = P_0\,[-D_1\,(1-D_2)\,(D_2-D_1)]$
III	$\frac{D_1(1-D_2)+D_2(1-D_1)}{2}$	$P_{\mathrm{III,max}} = P_0\,[D_1\,(1-D_1)\,D_2\,(1-D_2)]$
	–	$P_{\mathrm{III,min}} = \begin{cases} P_{\mathrm{I,max}}, D_1 > D_2 \\ P_{\mathrm{II,max}}, D_1 < D_2 \end{cases}$
IV	–	$P_{\mathrm{IV,max}} = \begin{cases} P_{\mathrm{I,min}}, D_1 > D_2 \\ P_{\mathrm{II,min}}, D_1 < D_2 \end{cases}$
	$-\frac{D_1(1-D_2)+D_2(1-D_1)}{2}$	$P_{\mathrm{IV,min}} = P_0\,[-D_1\,(1-D_1)\,D_2\,(1-D_2)]$

lead to higher rms currents in the HF transformer than modes I to IV. For this reason, only the operating modes I to IV are further considered. **Table 3.2** lists the expressions of φ_p depending on the duty cycles, and the power in a single phase, P. Additionally, Table 3.2 contains the conditions for D_1, D_2, and φ_p that must be fulfilled such that a particular operating mode applies.

Fig. 3.10 illustrates the flow chart of the algorithm used to determine the current operating mode of the DAB and to calculate the corresponding HF phase shift φ_p given the current duty cycles D_1 and D_2 and the power level P. Table 3.2 lists the expressions used for $\varphi_{\mathrm{p,I}}$, $\varphi_{\mathrm{p,II}}$, $\varphi_{\mathrm{p,III}}$, and $\varphi_{\mathrm{p,IV}}$.

Finally, the expressions for the minimum and maximum power levels in each operating mode, $P_{\mathrm{I-IV,min}}$ and $P_{\mathrm{I-IV,max}}$, are derived. **Table 3.3** lists the expressions for the phase shifts that lead to minimum and maximum power levels as well as the functions for minimum and maximum power levels that can be achieved in a single phase and for a given operating mode.

3.3.2 Considered constraints

In a first step, three constraints are defined for the functions of the power waveforms of the three DAB converter phases,

$$\langle p_\Sigma \rangle (t) = \langle p_{\mathrm{aA}} \rangle (t) + \langle p_{\mathrm{bB}} \rangle (t) + \langle p_{\mathrm{cC}} \rangle (t) \stackrel{!}{=} P_\Sigma = \text{const.}, \tag{3.17}$$

$$\langle p_{\mathrm{aA}} \rangle (t) \stackrel{!}{=} \langle p_{\mathrm{bB}} \rangle (t - T/3) \stackrel{!}{=} \langle p_{\mathrm{cC}} \rangle (t + T/3), \tag{3.18}$$

$$|\langle p_{\mathrm{aA,bB,cC}} \rangle (t)| \leq P_{\max}(D_{\mathrm{1,a,b,c}}(t), D_{\mathrm{2,A,B,C}}(t)). \tag{3.19}$$

The first constraint, (3.17), formulates the suppression of the LF components in the total power, $\langle p_\Sigma \rangle (t)$. Constraint (3.18) enforces that the waveforms of $\langle p_{\mathrm{aA,bB,cC}} \rangle$ have the same shape except that they are phase-shifted with respect to each other by 120 °. There, T denotes the effective period of $\langle p_{\mathrm{aA,bB,cC}} \rangle$. The aim of (3.18) is to achieve even loading of the phases. Finally, the third constraint, (3.19), ensures that the power in each phase never exceeds the maximum possible power, $P_{\max}(D_{\mathrm{1,a,b,c}}(t), D_{\mathrm{2,A,B,C}}(t))$, of the corresponding converter phase. This third constraint also leads to a limit for the total power,

$$-P_{\Sigma,\max} \leq P_\Sigma \leq P_{\Sigma,\max}. \tag{3.20}$$

3.3.3 Simple modulation approach

A simple approach which fulfills (3.17) and (3.18) is to set the power level constant and equal in each of the three phases as

$$\langle p \rangle (t) = P_0 \, a_0. \tag{3.21}$$

with P_0 defined in (3.16) and a constant a_0. Thus, a_0 must be selected such that the third constraint (3.19) is also fulfilled.

In order to keep the power of each phase constant, it must be ensured that each phase can provide the required power for each combination of D_1 and D_2. This requirement and the resulting consequences in terms of maximum transferable power between the primary and secondary sides of the D3ABC are assessed on the basis of the expressions for the maximum power levels given in Table 3.3. The contour plot in **Fig. 3.11(a)** reveals the maximum power levels for operating modes I to III, normalized to P_0, i.e., $P_{\mathrm{I,max}}/P_0$, $P_{\mathrm{II,max}}/P_0$, and $P_{\mathrm{III,max}}/P_0$, for D_1, $D_2 \in [0,\ 1]$. The solid black contour lines labeled with 0.02, 0.04, and 0.06 are associated with mode III and represent the highest possible power for any combination of D_1 and D_2. The dashed and dotted black lines represent the maximum power levels of modes I and II, respectively, which are strictly less than the maximum power levels of mode III (and strictly greater than the minimum power of mode IV). It is to be noted that the minimum power achieved with mode IV, $P_{\mathrm{IV,min}}$, features the same characteristic as the maximum power of mode III, $P_{\mathrm{III,max}}$, but with a negative sign. Therefore, maximum possible power in reverse direction is achieved with mode IV. For the sake of clarity, the presented explanations are confined to a power transfer from the primary to the secondary side, i.e., operating modes I to III. However, an extension to bidirectional operation is directly feasible.

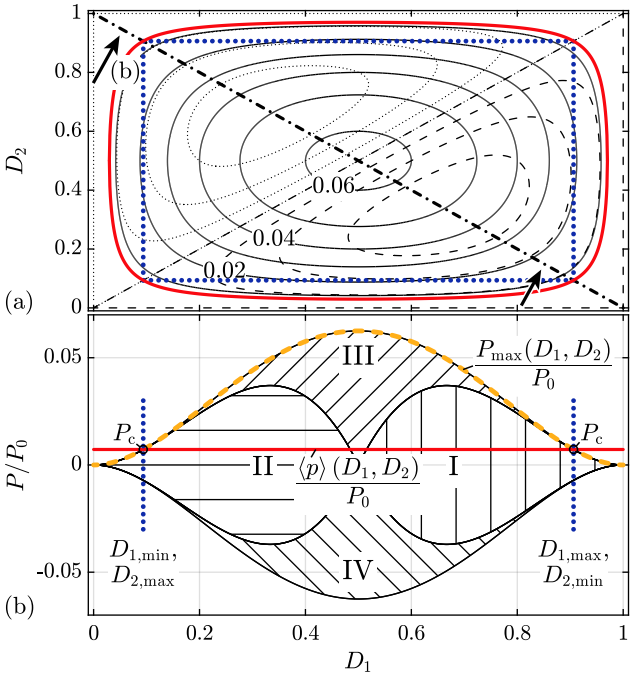

Fig. 3.11: (a) Contour plot of the maximum normalized power in a single DAB for modes I to III with respect to D_1 and D_2. The dotted blue rectangle refers the boundary of operation defined with (3.22) and (3.23). (b) Cross section through (a) projected onto the D_1-(P/P_0)-plane, which result for the cut edges defined by $D_2 = 1 - D_1$. Red line represents the maximum power that can be achieved with a constant power in the DAB converter part of one phase, which within the operating range is always below the maximum power (dashed orange line).

In order to fulfill (3.19), $\langle p \rangle$ must be less than $P_{\max}(D_1, D_2) = P_{\max,\mathrm{III}}$ in the complete range of D_1 and D_2,

$$\frac{1 - m_{\max}}{2} = D_{1,\min} \leq D_1 \leq D_{1,\max} = \frac{1 + m_{\max}}{2}, \tag{3.22}$$

$$\frac{1 - m_{\max}}{2} = D_{2,\min} \leq D_2 \leq D_{2,\max} = \frac{1 + m_{\max}}{2}, \tag{3.23}$$

where, for simplicity, same maximum modulation indices are considered on the primary and secondary sides,

$$0 \leq m_1 \leq m_{\max}, \quad 0 \leq m_2 \leq m_{\max}. \tag{3.24}$$

The dotted blue rectangle in Fig. 3.11(a) illustrates the boundary of the area defined with (3.22) and (3.23) for $m_{\max} = 0.81$, that results for operation according to Table 3.1. It should be noted that all four considered scenarios, S1 to S4, result in the same $m_{\max} = 0.81$. It is apparent from Fig. 3.11(a) that $P_{\max}(D_1, D_2)$ decreases if the duty cycles differ from 0.5 and reaches zero for duty cycles equal to 0 or 1.

Within the dotted blue rectangle, the lowest achievable power is present at the corners. To have a more detailed view of the corners, a cross-sectional drawing is shown in **Fig. 3.11(b)** for the dash-dotted diagonal intersection line shown in Fig. 3.11(a). The hatched areas represent the regions of corresponding operating modes I to IV [which correspond to volumes in the contour plot of Fig. 3.11(a)]. The white areas without labels, i.e., above mode III and below mode IV, denote unreachable power levels. The dashed orange line refers to the characteristic of the normalized maximum power of a DAB converter phase, $P_{\max}/P_0 = P_{\max,\mathrm{III}}/P_0$, for $D_2 = 1 - D_1$. In this view it is evident that the powers in the corners [marked as P_c in Fig. 3.11(b)] of the duty-cycle ranges defined with (3.22) and (3.23),

$$P_\mathrm{c} = \langle p \rangle \, (D_{1,\min}, D_{2,\max}) = \langle p \rangle \, (D_{1,\max}, D_{2,\min}), \tag{3.25}$$

are to be considered to determine the coefficients of (3.19), to ensure that the D3ABC never exceeds the maximum feasible power.

With (3.21) and (3.25) the coefficient a_0 can be determined,

$$a_0 = \frac{P_\mathrm{c}}{P_0} \tag{3.26}$$

using

$$\frac{P_\Sigma}{3} = P_\mathrm{c}, \tag{3.27}$$

since the power level in each of the three phases is equal and therefore the power level of each phase is one third of the total power. Consequently, to find $P_{\Sigma,\max}$, P_c is set equal to the respective maximum power,

$$P_c = P_{\max}(D_{1,\min}, D_{2,\max}) = \frac{P_0}{16}\left(1 - {m_{\max}}^2\right)^2. \tag{3.28}$$

The expression (3.28) substituted into (3.26) gives a maximum allowed value of

$$a_{0,\max} = \frac{1}{16}\left(1 - {m_{\max}}^2\right)^2. \tag{3.29}$$

To illustrate the implication of this result, Fig. 3.11 shows the characteristic of the power $\langle p\rangle|_{a_0=a_{0,\max}}$, defined in (3.21), that results for $a_0 = a_{0,\max}$. A constant power level for $\langle p\rangle(t)$ corresponds to a flat plane in the D_1-D_2-domain. The red contour line shown in Fig. 3.11(a) illustrates the intersection of the plane defined by $\langle p\rangle|_{a_0=a_{0,\max}}$ with the curved surface defined by $P_{\max}(D_1, D_2) = P_{\mathrm{III},\max}$. This shows nicely that within the entire operating range represented by the dotted blue rectangle, the power of a single DAB converter phase represented by the red line is less than or equal to the maximum power and that the corners are most critical. The solid red line in Fig. 3.11(b) depicts $\langle p\rangle|_{a_0=a_{0,\max}}$ directly. According to this, mainly modes I and II are used; mode III applies only for a small region where D_1 and D_2 are close to 0.5.

Finally, with (3.28) substituted into (3.27), the maximum total power,

$$P_{\Sigma,\max} = \frac{3}{16}P_0\left(1 - {m_{\max}}^2\right)^2, \tag{3.30}$$

is obtained. Given the considered maximum modulation index $m_{\max} = 0.81$ and the values listed for S1, S2, or S3 in Table 3.1 and **Table 3.5**, a maximum power of $P_{\Sigma,\max} = 2.9\,\mathrm{kW}$ results for the investigated D3ABC. This is significantly less than the rated power of 8 kW that is available for operation from ac_1 to dc_2, which the converter was designed for in Appendix A. This shortcoming is addressed in the following section, that proposes a duty-cycle dependent phase shift modulation approach to achieve higher power levels.

3.3.4 Advanced modulation approach

The relatively low achievable power level of the simple approach in **Subsection 3.3.3** is due to the fact that a single phase of the D3ABC can transfer only comparably low power between the primary and the secondary

side if the duty cycles of the same phase have values close to zero or one. Consequently, the development of an improved modulation scheme is based on the idea that the power shortfall of those DAB converter stages, which are operated at a given time with duty cycles close to zero or one, is compensated by an increased power of the remaining converter stages.

In the new approach, derived and analyzed in more detail in **Appendix B**, the power in each phase is adjusted based on a polynomial function that depends on the primary-side and secondary-side duty cycles,

$$\begin{aligned}\langle p\rangle\,(t) = P_0 \Big[\; & a_0 + a_1\tilde{D}_1(t) + a_2\tilde{D}_1(t)^2 + a_4\tilde{D}_1(t)^4 \\ & + b_1\tilde{D}_2(t) + b_2\tilde{D}_2(t)^2 + b_4\tilde{D}_2(t)^4 \;\Big] \\ \tilde{D}_1(t) = D_1(t) - \frac{1}{2},\; & \tilde{D}_2(t) = D_2(t) - \frac{1}{2}.\end{aligned} \tag{3.31}$$

The scaling factor P_0 in (3.31) is given in (3.16). Expression (3.31) is conceived in such a way that the constraints (3.17) and (3.18) are met for sinusoidal duty cycles according to (3.5) and (3.6), regardless of the values of the seven coefficients, $a_0 \ldots b_4$. Thus, the coefficients must be selected such that the third constraint (3.19) is also fulfilled.

The main findings discussed in the course of the explanation of the simple modulation approach in Subsection 3.3.3 also apply to the advanced approach. In this regard, the maximum power that can be transferred by each phase is $P_{\max}(D_1, D_2) = P_{\max,\mathrm{III}}$ as presented in **Fig. 3.12(a)** for $D_1, D_2 \in [0, 1]$ in form of a contour plot. In order to fulfill (3.19), $\langle p\rangle$ must be less than $P_{\max}(D_1, D_2)$ in the complete range of D_1 and D_2 defined by (3.22) and (3.23), respectively. Furthermore, again same modulation indices are considered on the primary and secondary sides. The dotted blue rectangle in Fig. 3.12(a) illustrates the boundary of the area defined with (3.22) and (3.23) for $m_{\max} = 0.81$, that results for operation according to Table 3.1.

Within the dotted blue rectangle the lowest achievable power is present at the corners. A cross-sectional drawing is shown in **Fig. 3.12(b)** for the dash-dotted diagonal intersection line shown in Fig. 3.12(a). The dashed orange line refers to the characteristic of the normalized maximum power of a DAB converter phase, $P_{\max}/P_0$, for $D_2 = 1 - D_1$. In view of this characteristic, it may be reasonable to assume that the power at the corners of the duty-cycle ranges defined with (3.22) and (3.23),

$$P_{\mathrm{c}} = \langle p\rangle\,(D_{1,\min}, D_{2,\max}) = \langle p\rangle\,(D_{1,\max}, D_{2,\min}), \tag{3.32}$$

has to be considered to determine the coefficients of (3.31), to ensure that the D3ABC never exceeds the maximum feasible power. However, at this

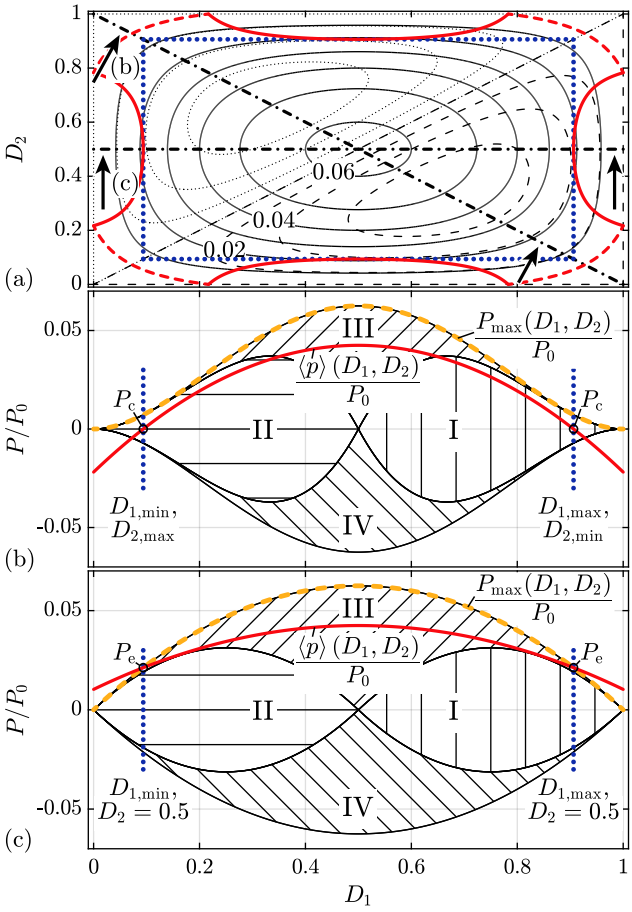

Fig. 3.12: (a) Contour plot of the maximum normalized power in a single DAB converter phase with respect to D_1 and D_2. The dotted blue rectangle refers the boundary of operation defined with (3.22) and (3.23). The red contour line illustrates the intersection of the plane defined by $\langle p\rangle\,(D_1, D_2)$ with the curved plane defined by $P_{\max}(D_1, D_2) = P_{\mathrm{III,max}}$ (dashed sections in the line are intersections with $P_{\mathrm{IV,min}}$). (b), (c) Cross sections through (a) projected onto the D_1-(P/P_0)-plane, which result for the cut edges defined by $D_2 = 1 - D_1$ and $D_2 = 0.5$, respectively. The red line anticipates the maximum power that can be achieved with the described method in the DAB converter part of one phase, which within the operating range is always below the maximum power (dashed orange line).

operating point also the polynomial (3.31) returns the lowest value within the considered ranges of D_1 and D_2 [in anticipation of the result, the shape of $\langle p \rangle$ is plotted as solid red line in Fig. 3.12(b)]. Since (3.31) is conceived such that the sum over the three phase powers is constant, i.e., the remaining converter phases compensate for the missing power, the operating point at the corner is not necessarily the most critical. Instead, it is found in the course of the derivation of useful expressions for the coefficients of $\langle p \rangle$ that the operating conditions $D_1 = 0.5$, $D_2 = D_{2,\mathrm{min,max}}$ and $D_2 = 0.5$, $D_1 = D_{1,\mathrm{min,max}}$ are of major importance. Therefore, **Fig. 3.12(c)** shows a corresponding cross-sectional drawing for $D_2 = 0.5$, i.e., for the dash-dotted horizontal intersection line marked in Fig. 3.12(a). The power at the edge of the operating range, e.g., $D_1 = D_{1,\mathrm{min}}$ and $D_2 = 0.5$, is denoted by P_e,[2]

$$P_\mathrm{e} = \langle p \rangle \left(D_{1,\mathrm{min}}, D_2 = 0.5\right) = \langle p \rangle \left(D_{1,\mathrm{max}}, D_2 = 0.5\right). \tag{3.33}$$

Based on these observations, the number of required coefficients can be reduced and the remaining coefficients determined. With (3.24) and due to the symmetry of the D3ABC (i.e., the primary and secondary sides can be swapped without changing the circuit), $a_1 = b_1$, $a_2 = b_2$, and $a_4 = b_4$ must hold true. Furthermore, the function of $\langle p \rangle$ is intended to be symmetric around the operating point $D_1 = D_2 = 0.5$, since maximum power can be transferred there, which leads to $a_1 = b_1 = 0$. Finally, to further simplify the problem, only a quadratic polynomial is considered in a first approach, i.e., $a_4 = b_4 = 0$ applies. With these considerations and simplifications, solely the coefficients a_0 and a_2 need to be determined such that (3.19) is fulfilled.

In the last step, a connection is made between the maximum transferrable power and the remaining coefficients, a_0 and a_2, to obtain the final expressions for a_0 and a_2. In this context, it is recalled that (3.31) is designed such that (3.18) is fulfilled. As a consequence, the global average values of the powers of the three phase, i.e., evaluated over $-\infty \leq t \leq +\infty$, are equal to one third of the total power. As a side note, it is worth noting that the average value of a sum

[2]Due to the definition (3.24), the same value for P_e results for $D_1 = 0.5$ and $D_2 = D_{2,\mathrm{min}}$ as well as $D_1 = 0.5$ and $D_2 = D_{2,\mathrm{max}}$.

term can be calculated by adding the average values of the individual terms,

$$\frac{1}{T}\int_0^T [y_1(t)+y_2(t)]\mathrm{d}t = \frac{1}{T}\int_0^T y_1(t)\mathrm{d}t + \frac{1}{T}\int_0^T y_2(t)\mathrm{d}t = \\ = \frac{1}{T_1}\int_0^{T_1} y_1(t)\mathrm{d}t + \frac{1}{T_2}\int_0^{T_2} y_2(t)\mathrm{d}t, \quad (3.34)$$

where T, T_1, and T_2 refer to the periods of $y_1(t) + y_2(t)$, $y_1(t)$, and $y_2(t)$, respectively. In this regard (3.34) is applied to (3.31) to establish a relation between P_Σ, a_0, and a_2,

$$\frac{P_\Sigma}{3} = P_0\left[a_0 + \frac{a_2\, {m_{\max}}^2}{4}\right]. \quad (3.35)$$

Furthermore, a_0 and a_2 can be expressed as functions of P_c and P_e,

$$a_0 = \frac{1}{P_0}\left(2P_\mathrm{e} - P_\mathrm{c}\right),\ a_2 = \frac{4}{P_0\, {m_{\max}}^2}(P_\mathrm{c} - P_\mathrm{e}), \quad (3.36)$$

by evaluating (3.31) at the operating points defined by (3.32) and (3.33) and subsequently solving for a_0 and a_2. If (3.36) is substituted into (3.35),

$$\frac{P_\Sigma}{3} = P_\mathrm{e} \quad (3.37)$$

results, i.e., only P_e defines the average power. Accordingly, P_c remains as a degree of freedom. A numerical inspection of (3.19) shows that any value of P_c that satisfies $|P_\mathrm{c}| \leq P_{\max}(D_{1,\max}, D_{2,\max})$ also satisfies (3.19). However, minimum rms values of the transformer currents result if P_e is set equal to the respective maximum power and P_c is set to zero,

$$P_\mathrm{e} = P_{\max}(D_{1,\min}, D_2 = 0.5) = \frac{P_0}{16}\left(1 - {m_{\max}}^2\right), \quad (3.38)$$

$$P_\mathrm{c} = 0 \quad (3.39)$$

as marked in Fig. 3.12(b,c). The expressions (3.38) and (3.39) substituted into (3.36) gives a maximum allowed value of

$$a_{0,\max} = \frac{1}{8}\left(1 - {m_{\max}}^2\right),\ a_{2,\max} = \frac{1}{4}\left(1 - \frac{1}{{m_{\max}}^2}\right) \quad (3.40)$$

for the coefficients a_0 and a_2.

A power level function $\langle p \rangle (D_1, D_2)$ according to (3.31) with the coefficients from (3.40) corresponds to a curved plane in the D_1-D_2-domain. The red contour line shown in Fig. 3.11(a) illustrates the intersection of the plane defined by $\langle p \rangle (D_1, D_2)$ with the curved plane defined by $P_{\max}(D_1, D_2) = P_{\mathrm{III,max}}$ (dashed sections in the line are intersections with $P_{\mathrm{IV,min}}$). This shows nicely that within the entire operating range represented by the dotted blue rectangle, the power of a single DAB converter phase represented by the red line is less than or equal to the maximum power. This is also verified by means of a numerical analysis presented in **Subsection 3.3.5**, which shows that the obtained function for $\langle p \rangle (D_1, D_2)$ is less than or equal to the maximum phase power, $P_{\max}$, in the entire range defined by (3.22) and (3.23). It is also evident that the edges of the boundary defined by (3.5) and (3.6) are the most critical (and not the corners). The solid red curves shown in Fig. 3.12(b) and Fig. 3.12(c) depict $\langle p \rangle (D_1, D_2)$, if (3.40) is applied.

Finally, with (3.38) substituted into (3.37) the maximum total power,

$$P_{\Sigma,\max} = \frac{3}{16} P_0 \left(1 - {m_{\max}}^2\right) \tag{3.41}$$

is obtained. Note that $P_{\Sigma,\max}$ represents the maximum power that can be transmitted between primary side and secondary side through the three DAB converter stages of the D3ABC, using (3.31) (with $a_4 = b_4 = 0$) and the maximum modulation indices at the two ac ports as defined in (3.24). Thereby it is irrelevant whether the power transmitted over the galvanic isolation is supplied by the ac or dc port (e.g., of the primary side) or whether the load being supplied is connected to the ac or dc port (e.g., of the secondary side). The limitation of $P_{\Sigma,\max}$ is rooted in the power limitation known from DAB converters, due to which the transmitted power above a certain HF phase shift φ_{p} does not increase further but decreases as shown in Fig. 5 in [51]. If, for example, $P_{\Sigma,\max}$ is to be increased for a given converter, either $m_{\max}$ must be decreased or P_0 increased. A decrease of $m_{\max}$ results in a reduction of the maximum possible ac voltages at the ac ports. An increase of P_0 is achieved, e.g., by decreasing the leakage inductance L_σ or the switching frequency f_{s}.

Inserting the values listed for S1, S2, or S3 in Table 3.1 and Table 3.5 into (3.16) and (3.41) gives a maximum power of $P_{\Sigma,\max} = 8.5\,\mathrm{kW}$, what is substantially higher than the maximum power of $P_{\Sigma,\max} = 2.9\,\mathrm{kW}$ achieved with the simple modulation approach described in Subsection 3.3.3. This value, $P_{\Sigma,\max} = 8.5\,\mathrm{kW}$, therefore represents the maximum theoretical total power for a specific hardware with given transformer parameters (L_σ, n) and given operating conditions ($V_{\mathrm{dc},1}$, $V_{\mathrm{dc},2}$, f_{s}). In this context, it is important to

emphasize that $P_{\Sigma,\max}$ represents a theoretical limit and must not be mistaken for the maximum permissible operating power of the converter, which is determined on the basis of the maximum permissible stresses of the designed or selected converter components. Consequently, the component stresses must be considered separately, which is done in Subsection 3.3.5 using a numerical analysis.

It is noted that the functions for a_0 and a_2 derived in this Section can be directly used to operate the D3ABC with modulation indices smaller than $m_{\max}$. In this regard, the possible total power, $P_{\Sigma,\max}$, increases for smaller modulation indices. The expressions (3.40) are valid for operation at maximum power. However, the results of a numerical analysis show that the power in the DAB part of the D3ABC can be adjusted by scaling both coefficients at the ratio $r_\mathrm{p} = P_\Sigma / P_{\Sigma,\max}$,

$$a_0 = a_{0,\max}\, r_\mathrm{p},\; a_2 = a_{2,\max}\, r_\mathrm{p}. \tag{3.42}$$

With this, currents with nearly minimal rms values result into the switching nodes on primary and secondary side, $I_{1,\mathrm{rms}}$ and $I_{2,\mathrm{rms}}$, of the D3ABC, as described in Subsection 3.3.5.

The calculation of the HF phase shifts $\varphi_{\mathrm{p,aA}}(t)$, $\varphi_{\mathrm{p,bB}}(t)$, and $\varphi_{\mathrm{p,cC}}(t)$ that correspond to the phase powers, $\langle p_{\mathrm{aA}}\rangle(t)$, $\langle p_{\mathrm{bB}}\rangle(t)$, and $\langle p_{\mathrm{cC}}\rangle(t)$, determined with (3.31) is based in the algorithm shown in Fig. 3.10 using the functions provided in Table 3.2.

Fig. 3.13 shows a pseudocode for a runtime-optimized implementation of the algorithm implemented on the hardware demonstrator's Digital Signal Processor (DSP). The expression for the intermediate variable e_1 used in this implementation has been derived based on (3.31) together with the coefficients (3.42). The constant $m_\mathrm{q} = m_{\max}^2$ defines the maximum modulation index that occurs during operation. The variables $D_1[1..3]$ and $D_2[1..3]$ denote the primary-side and secondary-side duty cycles present in each phase due to the line voltages, and the variables d_{11}, d_{12}, d_{22}, d_{21}, c_1, c_2, e_1, e_2, and e_3 serve as intermediate variables for calculating φ_p. Note: e_1 to e_3 correspond to the intermediate variables used in Table 3.2. The variable r_p denotes the scaling factor for the transferred power and has a value range of $-1 \leq r_\mathrm{p} \leq 1$ ($r_\mathrm{p} = 1$ corresponds to a power transferred from the primary to the secondary side equal to $P_{\Sigma,\max}$, moreover, if $r_\mathrm{p} < 0$, the power is transferred from the secondary to the primary side). The calculation is performed three times within a for-loop, once for each phase. The three lines highlighted in gray (two square roots and the division by a variable) indicate the most time-consuming calculations for the DSP used. The remaining calculations, i.e., additions, sub-

```
01  const m_q = 0.82 * 0.82                    // m_max * m_max
02  sub φ_p = calcPhi(D_1, D_2, r_p)
03     for i = 1 to 3                           // 3 phases
04        d_11 = D_1[i] * (1 - D_1[i])
05        d_12 = D_1[i] * (1 - D_2[i])
06        d_22 = D_2[i] * (1 - D_2[i])
07        d_21 = D_2[i] * (1 - D_1[i])
08        e_1 = d_11 + d_22 - (1 - m_q) / 2
09        e_1 = e_1 * (1 - m_q) * r_p / 4 / m_q
10        if D_1[i] > D_2[i]
11           c_1 = 2 * d_21                     // Mode I
12           c_2 = (D_1[i] - D_2[i]) / 2
13        else
14           c_1 = 2 * d_12                     // Mode II
15           c_2 = (D_2[i] - D_1[i]) / 2
16        end if
17        if abs(e_1) > (c_1 * c_2)
18           e_2 = d_11 * d_22
19           e_3 = (d_12 + d_21) / 2
20           if e_1 > 0
21              φ_p = e_3 - sqrt(e_2 - e_1)     // Mode III
22           else
23              φ_p = sqrt(e_2 + e_1) - e_3     // Mode IV
24           end if
25        else
26           φ_p = e_1 / c_1
27        end if
28     end for
29  end sub
```

Fig. 3.13: Pseudocode of the algorithm implemented on the DSP of the hardware demonstrator for real-time calculation of the HF phase shift φ_p. The three lines highlighted in gray (two square roots and the division by a variable) indicate the most time-consuming calculations for the DSP used.

tractions, multiplications, and divisions by constants have a comparatively short computing time due to the existing Floating-Point Unit (FPU). Using single-precision floating-point variables, the used DSP (TMS320F28335) can achieve a total calculation time that is less than one switching period. Consequently, the HF phase shifts of the phases, $\varphi_{\mathrm{p,aA}}(t)$, $\varphi_{\mathrm{p,bB}}(t)$, and $\varphi_{\mathrm{p,cC}}(t)$, are updated once per switching period.

3.3.5 Results of the numerical analysis

This section is divided into two subsections. The first subsection describes the implementation of the procedure used for numerical verification of the results and the second subsection discusses the obtained results.

Numerical derivation of the modulation scheme

The numerical procedure is used to numerically determine valid values for the coefficients a_0, $a_1 = b_1$, $a_2 = b_2$, and $a_4 = b_4$, i.e., values that satisfy condition (3.19). Regarding the studied operating point, the voltages given for S3 in Table 3.1 are considered, leading to $m_1 = m_2 = 0.81$. The component values considered are listed in Table 3.5. Loads on the dc ports are omitted, i.e., solely ac/ac operation is considered.

In a first step, $\langle p \rangle(t)$ is examined without fourth-order terms, i.e., for $a_4 = 0$. Initially, 200 uniformly distributed values in the range between −10 and +10 are considered for each coefficient, e.g., for a_0: $a_0 \in \{-10.0, -9.9, -9.8, ..., 9.9, 10.0\}$. There, the limits −10 and 10 are chosen sufficiently large to ensure that optimal solutions are not missed; e.g., $a_2 = 10$ leads to $\langle p \rangle > 40 P_{\mathrm{max}}$ for $D_1 = D_2 = 0.5$.

In the subsequent computational run, compliance with (3.19) is checked for each of the $200 \times 200 \times 200$ combinations of coefficients. For this purpose, $n_{\mathrm{D}} = 100$ evenly distributed values are calculated for each duty cycle, D_1 and D_2, within the ranges defined by (3.22) and (3.23), e.g., $D_1 \in \{0.095, 0.103, 0.111, ..., 0.905\}$. For each of the $n_{\mathrm{D}} \times n_{\mathrm{D}}$ combinations of duty cycles, $C_{\mathrm{D}} \in \{(0.095, 0.095), (0.103, 0.095), (0.111, 0.095), \ldots, (0.905, 0.905)\}$, the value of $\langle p \rangle$ that results for the currently considered coefficients is calculated according to (3.31). This value must be in between the minimum and the maximum power of the D3ABC for each duty-cycle combination of C_{D} ($P_{\mathrm{IV,min}}$ and $P_{\mathrm{III,max}}$, respectively, in Table 3.3). If the power is outside these limits, the corresponding set of coefficients is marked as invalid.

After this computational run, the ranges of invalid coefficients are examined in order to enable a refinement of the resolution of the coefficients. For example, if the results for the boundary regions of $a_0 \in \{-10.0, -9.9, -9.8\}$ and $a_0 \in \{9.8, 9.9, 10\}$ are marked as invalid for any combinations of a_1 and a_2, the following calculation run is performed for $-9.8 \leq a_0 \leq 9.8$, again for 200 uniformly distributed values. These boundaries are checked and adjusted individually for each coefficient. The above described computational run is repeated until the boundaries do not change between two runs. **Table 3.4** lists the resulting boundaries.

For $a_4 \neq 0$ the analysis is the same as for $a_4 = 0$. However, since it turned out during the investigation that $a_1 = 0$ leads to most valid solutions (an indication of this is also the narrowly defined range for a_1 in Table 3.4), the analysis for $a_4 \neq 0$ was performed for $a_1 = 0$. The boundaries for $a_4 \neq 0$ are also given in Table 3.4.

Tab. 3.4: Numerically determined boundaries for a_0, a_1, a_2, and a_4 for quadratic and fourth-order polynomials for $\langle p \rangle$, cf. (3.31).

	a_0	a_1	a_2	a_4
Quadratic polynomial $\langle p \rangle$	±0.048	±0.0092	±0.16	0
Fourth-order polynomial $\langle p \rangle$	±0.0496	0	±0.05488	±0.64

Three different criteria are used to further assess suitable values for the coefficients a_0, a_2, and a_4. The first criterion is the square of the rms value of the current into the switching node of a primary-side half-bridge (e.g. $i_{1,\mathrm{a}}$ in case of phase a, cf. Fig. 3.1), since this is a measure for the conduction losses in the converter.[3] The second criterion is the peak value of the current in L_σ, which is proportional to the peak value of the magnetic flux in the core of L_σ and is thus a measure for the size of the inductor's magnetic core.[4] The third criterion is the switching losses of the primary-side and secondary-side semiconductors, which are calculated based on the measured losses published in [80] and [81], respectively.

Due to the ac/ac operation of the inverter, the voltages and currents in each phase of the D3ABC change continuously. Therefore, the global time average values of the above evaluation criteria are calculated in a final step, i.e., the average values that result for a duration that approaches infinity, $T \to \infty$. Provided that the ratio between the two ac frequencies, f_1/f_2, is an irrational number,[5] this average value of $x(\tilde{D}_1, \tilde{D}_2)$ can be calculated according to

$$\langle x \rangle_{T\to\infty} = \frac{1}{\pi^2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} x(\tilde{D}_1, \tilde{D}_2)\Big|_{\substack{\tilde{D}_1=\frac{1}{2}m_1\sin(\alpha)\\ \tilde{D}_2=\frac{1}{2}m_2\sin(\beta)}} \mathrm{d}\alpha\mathrm{d}\beta. \tag{3.43}$$

[3] The rms value of the current into the switching node of a secondary-side half-bridge shows a similar characteristic and is therefore not explicitly shown.

[4] At a given total power, the peak currents in the primary-side and secondary-side filter inductors, $I_{L\mathrm{ac},1,\mathrm{peak}}$ and $I_{L\mathrm{ac},2,\mathrm{peak}}$, are practically independent of the investigated coefficients and were therefore disregarded.

[5] The effective period of the superposition of two sinusoidal signals with different frequencies approaches infinity, $T \to \infty$, if the ratio of the two frequencies is irrational. This guarantees that each duty-cycle combination occurs once within the range defined by (3.22) and (3.23). For the case considered in this chapter, i.e., $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$, the effective period is 1 s and thus, considerably higher than the periods of the two line frequencies. Accordingly, (3.43) approximates the mean values very well for this case.

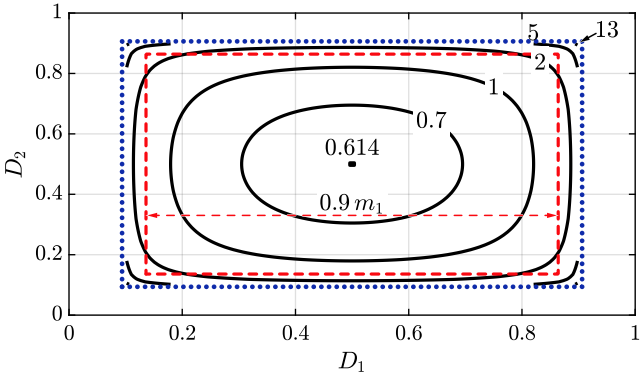

Fig. 3.14: Contour plot of the product $F_{D_1}F_{D_2}$ with the functions defined in (3.45) with $m_1 = m_2 = m_{\max} = 0.81$. The dotted blue rectangle refers to the boundary of operation defined with (3.22) and (3.23). The value at each point within this boundary can be understood as the joint probability density function of the duty-cycle combination (D_1, D_2). At the corners of the boundary the value of $F_{D_1}F_{D_2}$ approaches infinity. The integral over the area enclosed by the boundary is equal to 1. The red dashed rectangle with edge length $m_1 \sin(\pi/\sqrt{8}) \approx 0.9\,m_1$ corresponds to a median of the joint probability density function.

Using the substitution rule, the double integral from (3.43) can be rewritten into a double integral with respect to D_1 and D_2,

$$\langle x \rangle_{T\to\infty} = \int_{D_{2,\min}}^{D_{2,\max}} \int_{D_{1,\min}}^{D_{1,\max}} F_{D_1}F_{D_2}\, x(D_1, D_2)\, \mathrm{d}D_1 \mathrm{d}D_2, \tag{3.44}$$

$$F_{D_1} = \frac{2}{\pi m_1 \sqrt{1 - \frac{(2D_1-1)^2}{{m_1}^2}}},\ F_{D_2} = \frac{2}{\pi m_2 \sqrt{1 - \frac{(2D_2-1)^2}{{m_2}^2}}}. \tag{3.45}$$

Here, $F_{D_1}(D_1)$ and $F_{D_2}(D_2)$ can be considered as density functions and the product $F_{D_1}F_{D_2}$, shown in **Fig. 3.14**, can be understood as the joint probability density function of the occurrence of the duty-cycle combination (D_1, D_2).

Discussion of calculated component stresses

Fig. 3.15 presents the results for the global average values of $I^2_{\mathrm{l,rms}}$, $P_{\mathrm{sw,1}}$, and $P_{\mathrm{sw,2}}$ and the global maximum value of $I_{L\sigma,\mathrm{l,peak}}$ in a converter phase with respect to the total power of the D3ABC.

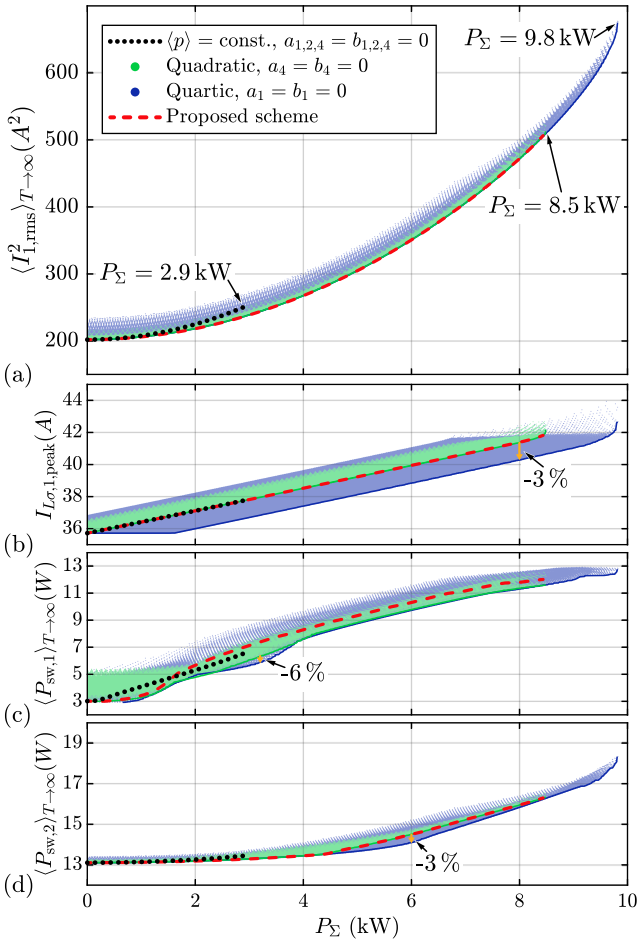

Fig. 3.15: Selected component stresses of a phase versus total power transmitted over the DAB part of the D3ABC, P_Σ, determined with a numerical analysis for quadratic and fourth-order polynomials of $\langle p \rangle$. Each point on the area corresponds to a combination of coefficient values which fulfill (3.19). The voltage and component values used are listed in Table 3.1 and Table 3.5, respectively and $f_1 \neq f_2$ is assumed. (a) Global time average value of the square of the rms current into a switching node on the primary side. (b) Global maximum value for the peak current in the leakage inductor. (c), (d) Global time average switching losses for a half-bridge on the primary and secondary side, respectively. The black dotted line and red dashed line correspond to the resulting component stresses for the simple and the advanced modulation approach, respectively.

The green areas represent the results calculated by numerical analysis, which are obtained by choosing a quadratic polynomial for $\langle p \rangle$, i.e., $a_4 = b_4 = 0$. The red dashed curves show the results that are obtained if the coefficients are calculated according to (3.42). A direct comparison of these two results indicates that the analytically calculated coefficients can be used to achieve practically the minimum rms currents. In addition, near-optimal peak currents in L_σ and switching losses are obtained. The maximum transmissible power is $P_{\Sigma,\max,D^2} = 8.5\,\mathrm{kW}$ which, apart from a slight deviation of 20 W (corresponding to 0.2 %), agrees well with the power calculated in **Subsection 3.3.4**.

The blue areas represent the additional solutions that can be obtained if a fourth-order polynomial is chosen for $\langle p \rangle$. It is mainly noticeable that the maximum transmittable power can then be increased to $P_{\Sigma,\max,D^4} = 9.8\,\mathrm{kW}$. Apart from this, small reductions of as much as −3 % in peak current values in L_σ can be achieved. However, a detailed analysis shows that this comes at the cost of an increase in the current rms values $I_{1,\mathrm{rms}}$ and $I_{2,\mathrm{rms}}$, e.g., at $P_\Sigma = 8\,\mathrm{kW}$ both $\langle I^2_{1,\mathrm{rms}} \rangle_{T\to\infty}$ and $\langle I^2_{2,\mathrm{rms}} \rangle_{T\to\infty}$ increase by 2 % respectively. Similarly, the switching losses depicted in Fig. 3.15(c) and Fig. 3.15(d), can be reduced by 6 % (for $P_\Sigma = 3.2\,\mathrm{kW}$) and 3 % (for $P_\Sigma = 5.2\,\mathrm{kW}$). However, this improvement is associated with an increase in $\langle I^2_{1,\mathrm{rms}} \rangle_{T\to\infty}$ and $\langle I^2_{2,\mathrm{rms}} \rangle_{T\to\infty}$ by 4 % and 2 %, respectively. Due to the limited advantages and the substantially higher effort required to analyze and implement the approach using the fourth-order polynomial for $\langle p \rangle$, it is not considered further here.

The black dotted lines in Fig. 3.15 refer to the results obtained with the simple modulation approach proposed in Subsection 3.3.3, i.e., for $\langle p \rangle = P_\Sigma/3 = \text{constant}$, which is equivalent to $a_{1,2,4} = b_{1,2,4} = 0$. Accordingly, the solutions calculated with this approach represent a subset of the solutions discussed in this section. Direct comparison shows that even this simple approach leads to near-optimal results for the chosen criteria. However, this choice of coefficients has the disadvantage of a comparatively low value for the maximum power of $P_{\Sigma,\max,D^0} = 2.9\,\mathrm{kW}$.

Finally, **Fig. 3.16** depicts the values of those coefficients that lead to minimum current rms values for the quadratic approach at given power P_Σ. In Fig. 3.15(a), these are the points located at the bottom edge of the green area. As can be seen from Fig. 3.16, the values of the coefficients are approximately proportional to the power P_Σ. In addition, the values of the coefficients at maximum power, $P_\Sigma = 8.5\,\mathrm{kW}$, agree with the values calculated with (3.40). Based on these results, the linear scaling of the coefficients is proposed according to (3.42).

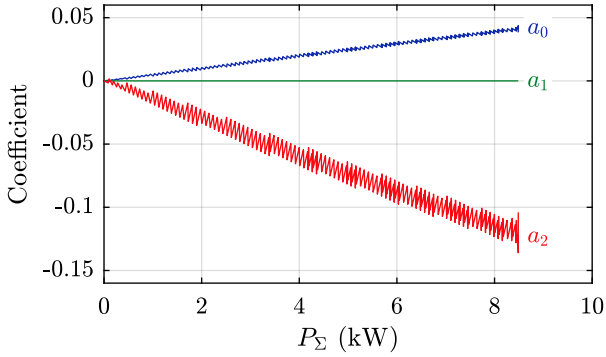

Fig. 3.16: Values of the coefficients for all points on the green area in Fig. 3.15(a) that lead to minimum values for $\langle I^2_{1,\mathrm{rms}} \rangle_{T\to\infty}$ at given power, P_Σ, i.e., the points located at the bottom edge of the green area. As can be seen, the values of the coefficients are approximately proportional to the power. Based on these results, the linear scaling of the coefficients is proposed according to (3.42).

3.4 Simulation and Experimental Verification

In this Section, the modulation scheme derived above for suppressing LF components in $\langle p_\Sigma \rangle$ when operating with $f_1 \neq f_2$ is verified using circuit simulations and hardware experiments. According to the explanation given at the beginning of Section 3.3, the power flow between the ports ac_1 and dc_1 or between ac_2 and dc_2 has no effect on the LF components in the currents of the dc link capacitors. Therefore, to simplify the setup, no power is fed into or drawn from the terminals dc_1 and dc_2. Instead, plain ac/ac operation with power flowing from ac_1 to ac_2 is considered, with a three-phase voltage source, which provides sinusoidal voltages according to (3.1) (with $\theta_{\mathrm{a,b,c}} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$), connected to ac_1 and a three-phase load connected to ac_2. The three-phase load is formed by the star connection of three 5 Ω resistors. Simulation and experiment both use the same converter components, according to Table 3.5, to allow for a direct comparison of the results.

The implemented control scheme is the same as described in Subsection 3.2.3, except that instead of the HF phase shift the variable r_p is constant.

Tab. 3.5: Switching frequency and main component values of the hardware demonstrator. All circuit simulations in this chapter use the same parameters.

Switching frequency	$f_s = 35\,\text{kHz}$
Primary-side dc link capacitors[6]	$C_{dc1} = 12\,\mu\text{F}$
Secondary-side dc link capacitors[6]	$C_{dc2} = 37\,\mu\text{F}$
Primary-side filter capacitors	$C_{f1} = 10\,\mu\text{F}$
Secondary-side filter capacitors	$C_{f2} = 21.5\,\mu\text{F}$
Primary-side ac inductances	$L_{ac,1} = 231\,\mu\text{H}$
Secondary-side ac inductances	$L_{ac,2} = 34\,\mu\text{H}$
Stray inductances	$L_\sigma = 89\,\mu\text{H}$
Transformers' turns ratio	$n = 2.6$

3.4.1 Simulation results

Fig. 3.17 depicts the result of the circuit simulation for converter operation according to S3 in Table 3.1, showing the primary-side voltages and currents in Fig. 3.17(a) and those of the secondary side in Fig. 3.17(b). Fig. 3.17(d) presents the waveforms of the instantaneous powers at the four ports of the D3ABC. The local average values of the instantaneous powers at the ports of the D3ABC are approximately constant, except for minor residual LF components. The phase powers of the DAB part, shown in Fig. 3.17(e), are shaped such that the sum of the three phase powers is almost constant, $\langle p_\Sigma \rangle = 8\,\text{kW}$. The remaining fluctuations in the power $\langle p_\Sigma \rangle$ are due to simplifications in the power calculation (e.g., piecewise linear currents in the inductors are assumed, thus neglecting the feedback effects of the voltages across the filter capacitors C_{f1} and C_{f2}), voltage distortions due to dead-time effects, and time delays caused by the signal processing and the PWM units. Due to these influences, the effective DAB power in the three phases deviates from the calculated power, which results in the small fluctuations of the total power $\langle p_\Sigma \rangle$. It is further apparent that the waveforms of $\langle p_{aA} \rangle$, $\langle p_{bB} \rangle$, and $\langle p_{cC} \rangle$ are similar except for a time shift, indicating that condition (3.18) is also satisfied.

[6] A specification of the dc link capacitances in per unit values would facilitate understanding whether a present power pulsation necessitates a large or small dc link capacitance. However, such normalization is not possible here, because the only reasonable characteristic frequency, which is required for such a normalization, is the fundamental frequency of the power pulsation, i.e., the difference frequency $|f_1 - f_2|$. This frequency depends on the operating conditions and is therefore not defined a priori.

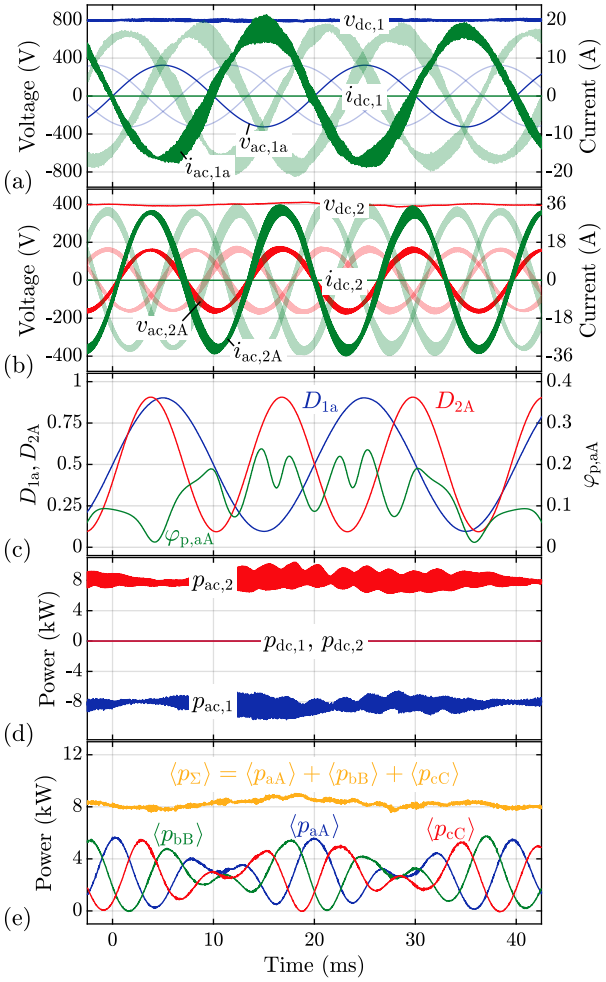

Fig. 3.17: Simulation results for converter operation according to S3 in Table 3.1, using the proposed modulation scheme: (a) primary-side voltages and currents, (b) secondary-side voltages and currents, (c) duty cycles and HF phase shift at phase a, (d) power levels at the four ports, and (e) local average values of the powers of the three DAB converter stages and the resulting total power. Compared to Fig. 3.7, the developed modulation scheme nearly eliminates the LF components in $\langle p_\Sigma \rangle$.

Fig. 3.17(c) shows the waveforms of the duty cycles and the HF phase shift, which the waveform of p_{aA} is based on. This figure reveals the highly dynamic changes of the HF phase shifts that are required to meet the constraints (3.17), (3.18), and (3.19) defined at the beginning of Subsection 3.3.2.

3.4.2 Experimental verification

Fig. 3.18 shows the hardware demonstrator of the D3ABC and reveals three of the four ports (port ac_2 is at the bottom of the hardware and therefore not visible on this picture). The demonstrator has been originally designed for operation from ac_1 to dc_2 (isolated rectifier operation) considering $f_1 = f_2$ as described in [51]. The maximum peak current in the leakage inductance for this operation with $f_1 = f_2$ is calculated to be $I_{L\sigma,1,\mathrm{peak}} \approx 20\,\mathrm{A}$, which is approximately half of the value that is calculated for operation with $f_1 \neq f_2$ as shown in Fig. 3.15. To avoid saturation of the leakage inductance (explicit inductors) when operating with $f_1 \neq f_2$, all voltages are reduced by a factor of 1/2 as listed for S_4 in Table 3.1. The reduction of the dc link voltages by 1/2 results according to (3.16) in a reduction of the power by a factor of 1/4, which leads to $P_\Sigma = 2\,\mathrm{kW}$.

To make the measurements obtained with the hardware demonstrator directly comparable with the simulation results, the simulations in Fig. 3.7 and Fig. 3.17 are repeated with reduced power according to S_4 in Table 3.1. Accordingly, Fig. 3.19 and Fig. 3.21 present corresponding simulation and measurement results, such that a direct comparison is possible. The simulation results shown in **Fig. 3.19(a)** and **Fig. 3.19(b)** are obtained when operating with constant HF phase shift, i.e., without the derived modulation scheme. The power in the DAB part of the D3ABC, $\langle p_\Sigma \rangle$, plotted in Fig. 3.19(b), shows pronounced LF components that, as Fig. 3.19(a) illustrates, lead to variations in the dc link voltages and distortions in the phase currents. The simulation results obtained with the derived modulation scheme depicted in **Fig. 3.19(c)** and **Fig. 3.19(d)** show that the LF components in $\langle p_\Sigma \rangle$ almost disappear and therefore the fluctuations of the dc link voltages are much smaller.

Fig. 3.20 and **Fig. 3.21** depict the measured waveforms during a time span of 50 ms. Fig. 3.20(a) shows the primary-side dc link voltage, phase voltages, and phase currents and Fig. 3.20(b) depicts secondary-side dc link voltage, phase voltages, and phase currents. Fig. 3.21 shows the dc link voltages, the phase voltages, and the phase currents of phases a/A, i.e., characteristic waveforms of the primary side and secondary side. Fig. 3.20(a) reveals a phase shift of 180 ° between the phase voltages and the phase currents, indicating

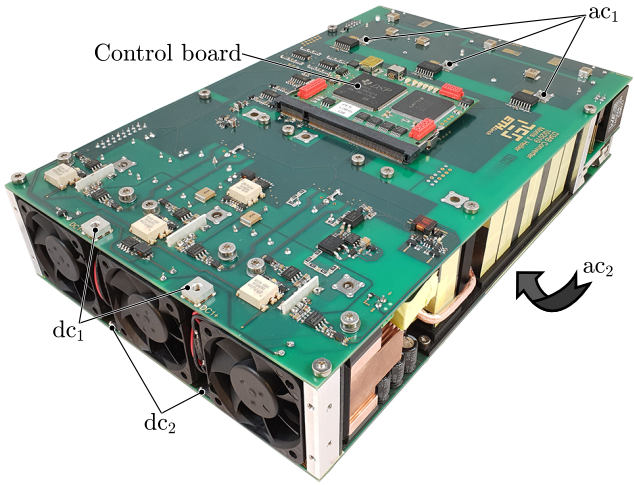

Fig. 3.18: (a) Hardware demonstrator of the D3ABC featuring an output power of 8 kW for rectifier operation with galvanic isolation, i.e., from ac_1 to dc_2. The port ac_2 is located at the bottom of the converter and is therefore not visible on this picture. The overall dimensions are 150 mm × 240 mm × 54 mm = 5.91 in × 9.45 in × 2.13 in (width × depth × height).

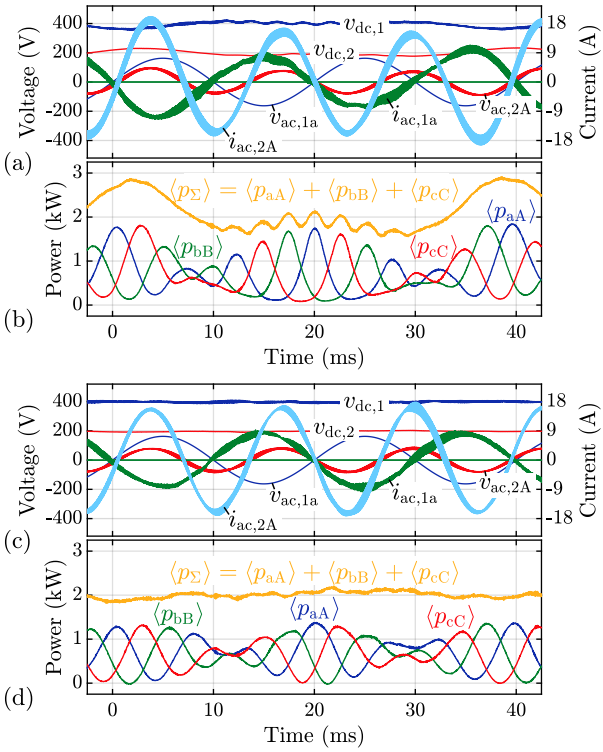

Fig. 3.19: Two simulation results for converter operation according to S4 in Table 3.1, w/o (a,b) and w/ (c,d) the proposed modulation scheme: (a) and (c) Dc link voltages, phase voltages, and phase currents of phases a/A on primary and secondary side. (b) and (d) Local average values of the powers of the three DAB converter stages and the resulting total power $\langle p_\Sigma \rangle$.

rectifier operation at ac_1. The waveforms in Fig. 3.20(b) of the output-side phase voltages, measured from the terminals to the star point of the load, are sinusoidal with a frequency of $f_2 = 77\,\mathrm{Hz}$ and in phase with the currents, indicating inverter operation at ac_2. The measurements shown in Fig. 3.21 agree well with the simulation results in Fig. 3.19(c). Specifically, the dc link voltages, $v_{dc,1}$ and $v_{dc,2}$, show almost constant waveforms, indicating that the LF power pulsations are eliminated by the modulation scheme.

A direct measurement of the power in the DAB part of the D3ABC, $\langle p_\Sigma \rangle$, would show the elimination of LF power pulsations even better. However, the power $\langle p_\Sigma \rangle$ is difficult to measure. **Fig. 3.22** shows two possible measurement methods to determine $\langle p_\Sigma \rangle$. The first method requires the dc link voltage and the current in the dc link, $v_{dc,1}$ and $i_{link,1}$. These measured values, multiplied and averaged over a switching period as in (3.7), result in $\langle p_\Sigma \rangle + p_{ac,1}$. Based on this measurement result, the waveform of $\langle p_\Sigma \rangle$ can be determined if the waveform of $p_{ac,1}$ is measured with, for example, a power analyzer. However, $i_{link,1}$ is not accessible, because this current is distributed over a planar conductor configuration, which realizes the connection between the dc link capacitance and the semiconductors to keep the commutation loop inductance as small as possible. The second method requires the voltages and the currents at the three switching nodes (e.g., $v_{n,a}$ and $i_{l,a}$ marked in Fig. 3.22 in case of phase a). These measured values, multiplied for each phase, averaged over one switching period, and summed up over all three phases, also give $\langle p_\Sigma \rangle + p_{ac,1}$. These voltages and currents are accessible, but both contain main switching frequency components. For this reason, the measurements of the powers at the switching nodes are not feasible with the available measurement equipment, e.g., the available power analyzer.

In a second experiment, the capability of the presented modulation scheme is further assessed by generating a three-phase voltage with time-changing frequency, f_2, and modulation index, m_2, at the port ac_2. An application scenario could be the power supply of an asynchronous machine with V/F speed control, i.e., with the voltage of the motor increasing proportional to the output frequency, e.g., when ramping up the asynchronous machine speed at port ac_2 from standstill. In this context, the voltage sources at port ac_1 remain unchanged. At port ac_2, the asynchronous machine is emulated by inductors, which are connected in parallel to the load resistors.

Fig. 3.23 depicts the measured waveforms of $v_{ac,1a}$, $i_{ac,1a}$, $v_{ac,2A}$, $i_{ac,2A}$, $v_{dc,1}$, and $v_{dc,2}$ during a time span of 1 s. Fig. 3.23(a) is measured with a purely resistive and Fig. 3.23(b) with a resistive-inductive load connected to ac_2. During the first 100 ms of the measurement, $v_{ac,2A} = i_{ac,2A} = 0$ apply.

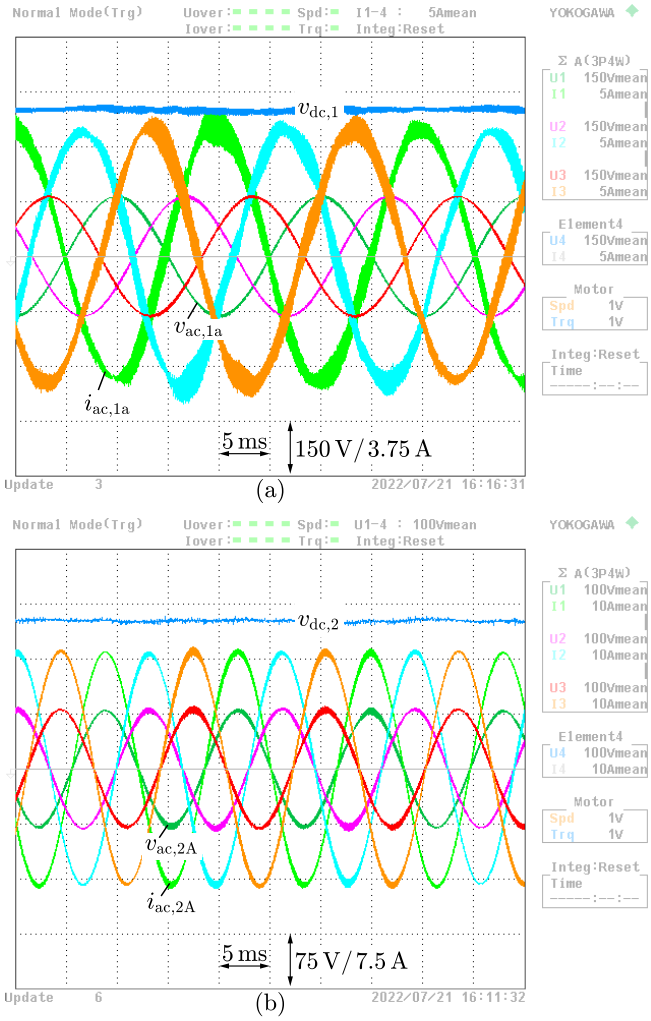

Fig. 3.20: Measurement results for converter operation according to S4 in Table 3.1. (a) primary-side voltages and currents and (b) secondary-side voltages and currents.

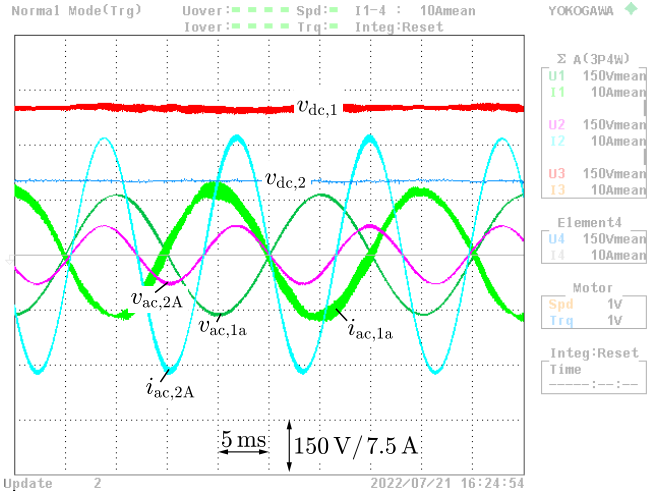

Fig. 3.21: Measurement results for the same operation as in Fig. 3.20 with waveforms from primary and secondary sides, i.e., dc link voltages as well as phase voltages and phase currents of phases a/A. The waveforms agree well with the simulation results in Fig. 3.19(c). Specifically, the dc link voltages, $v_{dc,1}$ and $v_{dc,2}$, show almost constant waveforms, indicating that the LF power pulsations are eliminated by the modulation scheme.

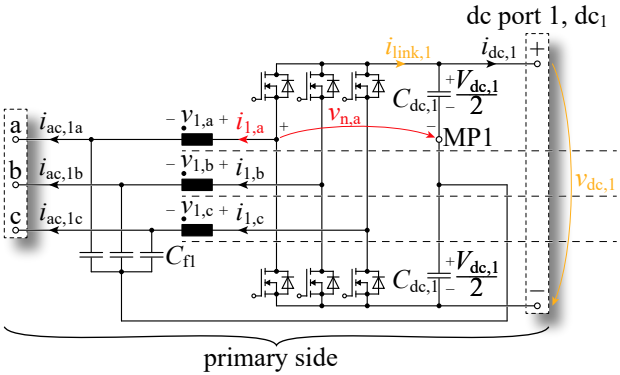

Fig. 3.22: Section of the D3ABC from Fig. 3.1 highlighting the voltages and currents that need to be measured to determine the power in the DAB part, $\langle p_\Sigma \rangle$. Either the dc link voltage and the current in the dc link need to be measured, $v_{dc,1}$ and $i_{link,1}$, or the voltages and currents of the three switching nodes (see $v_{n,a}$ and $i_{1,a}$ highlighted for phase a).

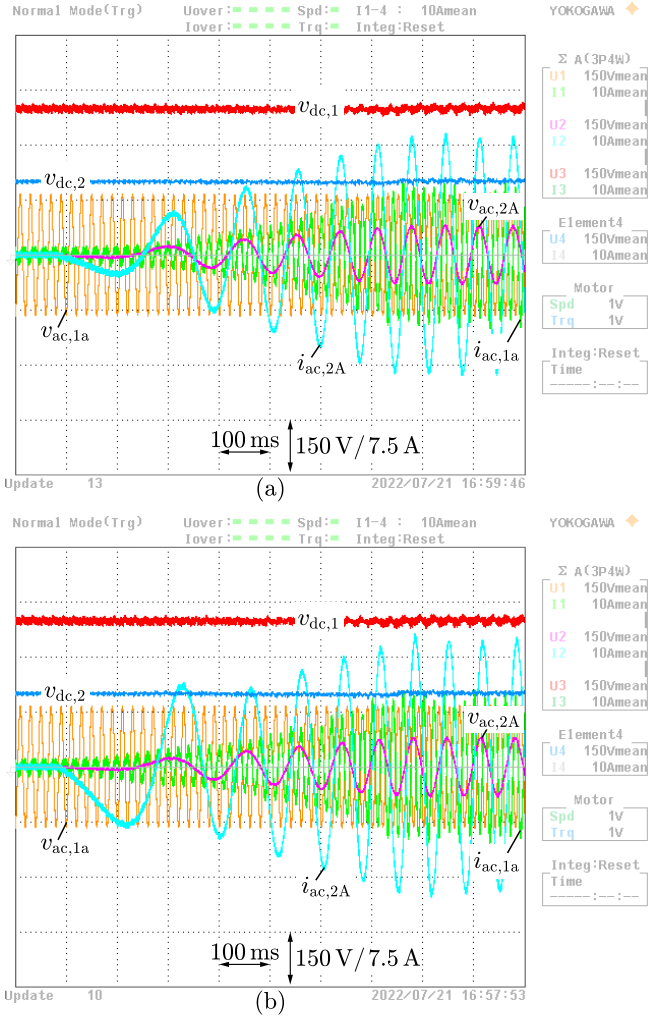

Fig. 3.23: (a) Measurement results for an example scenario where the modulation index and frequency are varied on the secondary side. The current in the primary-side phase a, $i_{ac,1a}$, increases as the voltage across the resistive load, $v_{ac,2A}$, increases. During this process, the primary- and secondary-side dc link voltages, $v_{dc,1}$ and $v_{dc,2}$, remain constant. (b) The same setup as (a) but with a resistive-inductive load.

Accordingly, a small amplitude results for the primary-side phase current, $i_{\mathrm{ac,1a}}$, since the power drawn from the voltage sources only has to cover the losses of the converter and the reactive power demand of the input filter. After $t = 5\,\mathrm{ms}$, the line frequency, f_2, and the modulation index at port ac_2 are increased at constant rates of $20\,\mathrm{Hz/s}$ and $1.07\,\mathrm{s}^{-1}$, respectively. At the same time, the amplitude of the phase current of the primary-side phase a, $i_{\mathrm{ac,1a}}$, increases proportionally to the output power, which increases quadratically over time. At $t \approx 750\,\mathrm{ms}$, the D3ABC reaches the final output frequency and amplitude of 15 Hz and 80 V, respectively. During the entire process, the primary- and secondary-side dc link voltages, $v_{\mathrm{dc,1}}$ and $v_{\mathrm{dc,2}}$, remain constant.

3.5 Conclusion

This chapter proposes a duty-cycle dependent phase shift modulation scheme to prevent LF power pulsations in the D3ABC. Such LF power pulsations occur, e.g., if the D3ABC is operated with different line frequencies, $f_1 \neq f_2$, at its primary-side and secondary-side ac ports. The new approach achieves a transmittable power of the DAB part of 8.5 kW.

The effectiveness of the developed modulation scheme is verified by means of circuit simulations and experimental evaluations. The circuit simulations are conducted for an output power of 8 kW, which is delivered to a three-phase resistive load at the secondary-side three-phase port ac_2. The rms values of the primary-side and secondary-side phase voltages are $V_{\mathrm{ac,1}} = 230\,\mathrm{V}$ and $V_{\mathrm{ac,2}} = 115\,\mathrm{V}$, respectively, and the line frequencies are $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$, respectively. The simulation results confirm constant power in the DAB part, resulting in approximately constant dc link voltages despite the relatively small dc link capacitances.

The experimental verification conducted for $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$ confirms the proper operation of the proposed modulation scheme, as well. Since the realized converter was designed for a power transfer between the ports ac_1 and dc_2, and power transfer between the ports ac_1 and ac_2 leads to higher currents in the power stage of the D3ABC. Accordingly, the experimental verification is conducted for a reduced power of 2 kW and the voltages are halved. The measured voltages and currents agree well with the simulation results.

In a second experiment, the operation with time-varying rms values and frequencies of the voltages at port ac_2 is investigated. A possible application of this is the V/F speed control of an asynchronous machine. In this operating scenario, the dc link voltages also exhibit constant characteristics. This

indicates that the proposed modulation scheme remains effective even in the case of time-varying modulation indices and/or line frequencies.

4 Conclusion and Outlook

This thesis investigates the D3ABC topology introduced in [51], which provides two three-phase ac ports (ac_1 and ac_2), two dc ports (dc_1 and dc_2), and galvanic isolation between ac_1, dc_1 (primary-side) and ac_2, dc_2 (secondary-side).

First, **Chapter 2** gives a comprehensive description of the operating principle of the D3ABC topology when operating as a bidirectional ac_1–dc_1/dc_2 rectifier. Based on this description, it derives models for calculating the conducted DM and CM EMI noise at the primary-side ac port, ac_1, taking into account the loads at ports dc_1 and dc_2 of the D3ABC. The evaluation of these EMI models reveals that the EMI noise at port ac_1 is nearly independent of the load on port dc_1, but increases as the load on port dc_2 increases. An example application uses these EMI models for the design of a volume optimized EMI filter for a hardware demonstrator. The measurements of the conducted EMI noise of the hardware demonstrator with EMI filter reveals that, at the considered operating point, the first spectral component entering the EMI band regulated by CISPR 11, which is at $f = 175\,\mathrm{kHz}$, shows an amplitude that is consistently between the minimum and maximum noise levels predicted by the model. Due to the low-pass characteristic of an EMI filter, the lower end of the regulated frequency range is most critical for the EMI filter design. Therefore, the estimates provided by the models are sufficient for the design and optimization of filters at an early stage of converter design. The hardware demonstrator combined with the designed EMI filter complies with the QP limit defined by CISPR 11 class A for a power of $P_2 = 2.5\,\mathrm{kW}$ at the secondary-side dc port, dc_2.

Second, **Chapter 3** extends the descriptions for the operating principle of D3ABC with respect to ac_1–dc_1/dc_2–ac_2 multi-port operation. According to the obtained findings, the D3ABC allows for independent bidirectional power

transfer between all four ports, ac_1, dc_1, dc_2, and ac_2, however, LF power pulsations can occur in the dc links of the D3ABC when operating with, for example, ac voltages with different frequencies at the two ac ports, $f_1 \neq f_2$. Consequently, an advanced modulation method is derived to eliminate these LF power pulsations. This modulation scheme allows a theoretical maximum power level of 8.5 kW in the DAB part of the D3ABC, which is comparable to the power level of 8 kW in ac_1–dc_1/dc_2 rectifier operation. Measurements on a hardware demonstrator (with half the rated voltages and reduced power of 2 kW) verify the functionality of the proposed modulation scheme.

The multi-port capability of the D3ABC topology makes it the perfect fit for managing the energy transfer between the existing three-phase grid and the various energy sources, storages, and loads in so-called microgrids. These microgrids allow an efficient integration of renewable energy sources and thus play a central role in the transition from the existing grid to the smart grid of the future.

4.1 Challenges of the D3ABC Topology

The integration of the boost inductors into the DAB transformers in the D3ABC topology allows to reduce the number of magnetic components as well as power semiconductor switches by using switching nodes for multiple tasks at the same time. In this context, integration constitutes a major advantage, but at the same time poses challenges, as described in the following.

- In the D3ABC topology, the ac-side filter capacitors must withstand the full line voltage while being subjected to high currents. The high currents result from the superposition of the triangular current ripples that originate from the PFC rectifier or inverter operation of the VSCs and the trapezoidal DAB converter currents. The high voltages and currents correspond to high component stresses. As a consequence, the ac-side filter capacitors are comparatively large and have relatively high losses.

- The superposition of the two current components further leads to a comparatively high EMI noise at the filter capacitances. To meet the limit despite the high noise, EMI filters with relatively high volume and/or losses are required.

- In order to place the resonance frequency of the series LC circuit formed by the elements C_{f1}, $C_{dc,1}$, C_{f2}, $C_{dc,2}$, and L_σ below the switching fre-

quency, the values of the components involved must not fall below a certain limit. Thus, the value of the stray inductance can be decreased only if the total capacitance, given by the series connection of the capacitors $3C_{f1}$, $2C_{dc,1}$, $3C_{f2}/n^2$, and $2C_{dc,2}/n^2$ is increased, which is accompanied by an increase of the volume. This especially applies for the given converter, since the capacitances have similar values and therefore all four capacitances must be increased in order to achieve an effective increase of the total capacitance. However, decreasing the stray inductance may be desirable to increase the active power and decrease the reactive power in the DAB part of the D3ABC.

- Since the duty cycles on the primary and secondary side can be different in ac_1/ac_2 operation with different line frequencies of the ac voltages, $f_1 \neq f_2$, large voltage-time areas occur across the stray inductances L_σ. This leads to high peak and rms values of the currents in the stray inductances, increasing their losses and/or volumes.

- If, e.g., only port ac_1 of the D3ABC is connected to an ac grid, the capacitor $C_{dc,1}$ is charged via the anti-parallel diodes in the VSC power semiconductors before the semiconductors are switched. However, at the same time, the voltages across the DAB transformers are small and therefore the capacitor $C_{dc,2}$ may remain uncharged. The uncharged capacitor $C_{dc,2}$ corresponds to a short on the secondary side of the transformers. Therefore, as soon as the primary-side semiconductors start switching, they apply the entire dc_1 voltage to the stray inductances. This requires the implementation of a special start-up procedure of the D3ABC to prevent saturation of the stray inductances L_σ (explicit inductors).

This listing shows that the challenges resulting from functional integration are mainly due to the fact that certain converter components are used for multiple tasks simultaneously. Since the use of components for multiple tasks in is an inherent property of an integrated converter topology such as the D3ABC, it can be assumed that the challenges listed above are not limited to the D3ABC topology, but are in general characteristic for the challenges in integrated converter topologies. Consequently, such challenges should be in the focus of research on integrated converters for future smart grid applications.

4.2 Outlook and Future Research

With the description of the EMI characteristics and the multi-port operation, important parts for the operation of the D3ABC topology in a microgrid in connection with the existing grid are given. A direct extension of the EMI models derived for ac–dc/dc operation would be to include simultaneous four-port operation. With regard to multi-port operation, the comparison of multi-stage and single-stage converter topologies remains. Interesting performance comparisons could consider multiple performance indicators, e.g., efficiency, power density, relative costs, maintainability or the implementation effort of the systems.

Since the performance of a converter also depends strongly on the application, the identification of alternative application areas for the D3ABC represents a further important topic. This includes possible adaptations of the D3ABC topology to ensure compatibility with identified applications. Along with performance evaluations of alternative, suitable circuit topologies, this would provide a deeper understanding of applications which the D3ABC is particularly suited for.

Appendices

A

Design of the D3ABC Hardware Prototype

The design of the D3ABC hardware prototype (without EMI filter) based on an η–ρ-Pareto optimization is detailed in [51] and is therefore, for the sake of brevity, not outlined further here. However, minor details were changed to refine the optimization. **Section A.1** describes the changes in the optimization and the resulting shifts in the Pareto front. Based on the new optimization, **Section A.2** explains the design of the individual hardware components and their assembly. Finally, **Section A.3** shows measurement results for the rectifier operation of the hardware prototype.

A.1 D3ABC η–ρ-Pareto front

The optimization is performed for the ac_1–$\mathrm{dc}_1/\mathrm{dc}_2$ rectifier operation as in [51] for nominal power at the secondary-side dc port, $P_2 = 8\,\mathrm{kW}$, with primary-side dc link voltage $V_{\mathrm{dc},1} = 800\,\mathrm{V}$, secondary-side dc link voltage $V_{\mathrm{dc},2} = 400\,\mathrm{V}$, and primary-side three-phase ac voltage $V_{\mathrm{ac},1} = 230\,\mathrm{V}$ (RMS, line-to-neutral) with a frequency of $f_1 = 50\,\mathrm{Hz}$. The changes to the optimization are described below.

First, the resonance frequencies of the resonant circuits shown in Fig. 2.7(b,c) and Fig. 2.8(c,d), e.g., formed by the series connection of $3C_{\mathrm{f1}}$, $2C_{\mathrm{dc},1}$, $3C'_{\mathrm{f2}}$, $2C'_{\mathrm{dc},2}$, and $L_\sigma/3$ in Fig. 2.8(c), can be close to the switching frequency. In this regard, the network depicted in Fig. 2.8(c) turned out to be most critical. To prevent excitation of this resonance, the optimization is

Tab. A.1: Considered comerciell available core sizes from TDK™ made of N95 magnetic material. *Cores only included for the stray inductance L_σ. †Cores only included for the transformer, L_{ac}.

E 20/10/11*	E 42/21/15	E 47/20/16†
E 35/18/10*	E 42/21/20	E 55/28/21†
E 40/16/12	E 42/33/20†	E 55/28/25†

extended by the condition that this resonance frequency,

$$f_{r,\sigma} = \frac{1}{2\pi\sqrt{\frac{L_\sigma}{3}\,C_r}} < \frac{f_s}{2}, \tag{A.1}$$

$$C_r = \frac{1}{\frac{1}{3C_{f1}} + \frac{1}{2C_{dc,1}} + \frac{n^2}{3C_{f2}} + \frac{n^2}{2C_{dc,2}}} \tag{A.2}$$

must be below half the switching frequency. This condition limits the choice of values of the involved components, C_{f1}, $C_{dc,1}$, C_{f2}, $C_{dc,2}$, and L_σ. However, compliance with this condition can be satisfied by two simple changes in the original optimization. First, the value of the leakage inductance is set to 90 % instead of 80 % of the maximum value of the leakage inductance defined by Eq. (17) in [51]. Second, the capacitor with the smallest capacitance involved (regarding the four capacitors of the considered series connection of $3C_{f1}$, $2C_{dc,1}$, $3C_{f2}/n^2$, and $2C_{dc,2}/n^2$), $C_{dc,2}$, the two CeraLink™ SP500 are replaced by 2×48 stacked C5750X6S2W225K250KA from TDK™ as shown in Fig. A.2(b).

In a next step, the originally proposed primary-side semiconductor switches, which are 25 mΩ/1200 V-devices (C2M0025120D by Cree), are replaced by 16 mΩ/1200 V-devices (C3M0016120K by Cree). This device has an on-resistance of 23 mΩ at a junction temperature of 125 °C. Switching losses are adapted from measurements in [80] for a switching voltage of $V_{sw} = 800$ V, an output capacitance of $C_{oss,Q} = 409$ pF, and a parasitic capacitance of $C_{par} = 300$ pF.

Finally, instead of scaled cores, dedicated cores are selected from a list of commercially available cores. Of the cores considered in **Table A.1**, which are made of TDK™'s N95 magnetic material, a stack of at most four cores is considered.

Fig. A.1 shows the new η–ρ-Pareto front resulting from these changes in green color. The Pareto front in Fig. A.1 is very similar to that in [51], with slightly higher efficiencs being achieved, which is mainly due to the reduced conduction losses in the primary-side semiconductors.

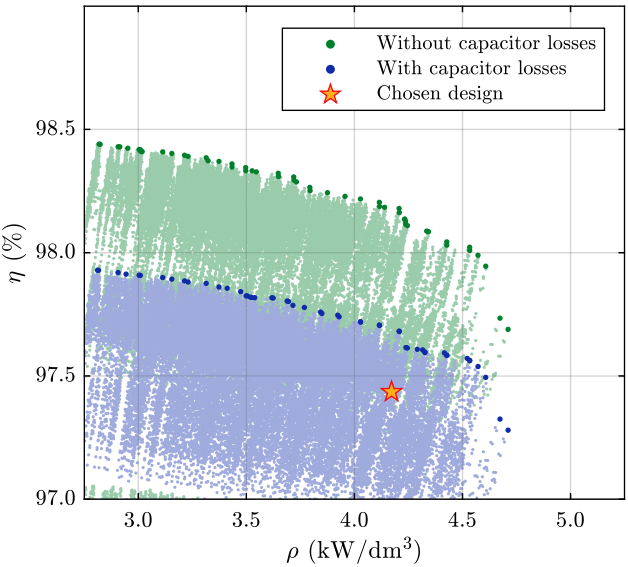

Fig. A.1: η–ρ-Pareto fronts of the D3ABC topology in green for similar loss and volume models as in [51] and in blue extended by the losses of capacitors, output filters and current sensors. The star marks the design chosen for the realization of the hardware prototype.

Tab. A.2: Components ESR values used to calculated conduction losses. For component stack, the specified ESR is for one component. The # of components refers to the total number used for converter.

Description	Component	ESR	#
Prim.-side filter capacitor	1×B32754C2106K000	5 mΩ	3
Prim.-side dc link capacitor	1×SP500	23.7 mΩ	2
Prim.-side current sensors	1×ACS733 + PCB	2 mΩ	3
Sec.-side filter capacitor	21×C5750X6S2W225K250	15.7 mΩ	3
Sec.-side dc link capacitor	48×C5750X6S2W225K250	14.6 mΩ	2
Sec.-side dc filter inductor	1×XAL1010-472ME	5.7 mΩ	2
	+ 1×PA4344.103ANLT	10.6 mΩ	2
Sec.-side current sensors	1×ACS733 + PCB	2 mΩ	3
Sec.-side dc current sensor	1×ACS733 + PCB	2 mΩ	1

The next step is to include the losses in the capacitors, the secondary-side output filter, as well as the current sensors used for current measurement / control. **Table A.2** lists the involved components and the relevant Equivalent Series Resistances (ESRs) obtained from the respective datasheets. Frequency-dependent ESRs are interpolated in the optimization from the data sheet values, but are only given for $f_s = 35\,\text{kHz}$ in the table.

If these losses are taken into account, the η–ρ-Pareto front shifts significantly downward as shown in blue in Fig. A.1. The additional losses occur mainly in the primary-side dc link capacitors, the secondary-side dc filter inductors, and the secondary-side filter capacitors. With regard to the primary-side dc link capacitors and the secondary-side dc filter inductors, the high ESRs in combination with high RMS currents are responsible for the high losses. However, for the secondary-side filter capacitors, LF polarization losses are predominant. These losses are modeled based on the loss data in [82] for the similar material X7T using an ESR at grid frequency (50 Hz) of 66 Ω and an effective capacitance, which is relevant with respect to the capacitor current, of 1.07 µF.

The design marked with the star in Fig. A.1 refers to the calculated efficiency and power density of the realized hardware demonstrator. The remaining distance between Pareto front and the star is due to the practical implementation of certain components in the converter, which leads to a certain increase of volume and losses, as explained in the following section.

Tab. A.3: Main parameters of the hardware design.

Switching frequency	$f_s = 35\,\text{kHz}$
Current ripple (peak-to-peak)	$r = 250\,\%$
Transformer turns ratio	$n = 2.6$
Calculated efficiency at full load	$\eta = 97.4\,\%$
Measured efficiency at full load	$\eta = 97.0\,\%$
Calculated power density	$\rho = 4.2\,\text{kW/dm}^3$
Final power density	$\rho = 4.1\,\text{kW/dm}^3$

A.2 Hardware components

Table A.3 summarizes the calculated values of the most important parameters of the hardware design marked with a star in Fig. A.1. Table A.3 further includes the measured efficiency discussed in Section A.3 and the final power density, resulting from the practical implementation of the components, which is detailed in the following.

First, a copper heat sink was optimized for cooling the power semiconductors using the design method described in [83]. The resulting heat sink is shown in **Fig. A.2(a)**. The primary-side semiconductors are mounted on top and the secondary-side semiconductors are mounted on the bottom of the heat sink, each with an electrically insulating thermal pad. The fins have a reduced height at the front, because further components are placed below and above the heat sink as visible in Fig. A.5(b). The heat sink has a total volume of $V_{\text{HS}} = 0.106\,\text{dm}^3$, which with the fans, the air duct, and the semiconductors gives $V_{\text{cool}} = 0.217\,\text{dm}^3$ (estimated was $V_{\text{cool}} = 0.126\,\text{dm}^3$).[1]

The η–ρ-Pareto optimization directly provides the main design parameters of the magnetic components, which, for the selected design, are given in **Table A.4**. **Fig. A.3** shows the assembly of a boost inductor/transformer in detail. First, the five turns of the secondary-side winding are wound onto the 3D printed Polycarbonate (PC) coil former shown in Fig. A.3(a). PC is used because of its high temperature resistance up to 80 °C. The secondary-side winding is isolated from the primary-side winding with a Mylar foil. The Mylar foil is then bonded to the coil former with insulating polyester

[1]The difference between the estimate and the effective volume for cooling is mainly due to the T-shaped extension of the fins, which can be seen in Fig. A.2. The heat sink was designed in such a way that the cooling capacity provided is sufficient even without the extended fins. A heat sink without extended fins reduces the total volume for cooling to $V_{\text{cool}} = 0.156\,\text{dm}^3$ which is close to the estimate.

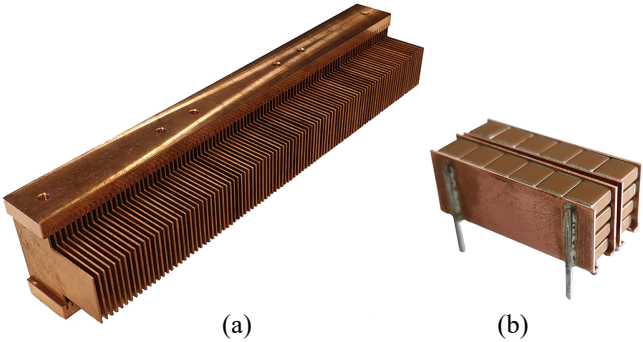

Fig. A.2: (a) Heat sink for the power semiconductors with dimensions 150 mm × 30 mm × 32 mm (width × depth × height). The heat sink has 98 fins with a sheet thickness of 0.5 mm and an air gap of 1 mm between them. (b) Secondary-side dc link capacitor made of 2 × 4 × 6 = 48 C5750X6S2W225K250 ceramic capacitors.

Tab. A.4: Assembly parameter of the magnetic components.

Boost inductor/transformer	
Inductance	$L_{ac} = 134\ \mu H$
Boxed volume	$V_{box} = 0.173\ dm^3$
Magnetic core (stacked)	Size = 4×E 42/21/20
Number of turns	$N_{1,2} = \{13, 5\}$
Air gap (distributed)	$l_{air} = \{0.5\ mm, 0.7\ mm, 0.5\ mm\}$
HF litz wire strands	$n_{1,2} = \{1200, 1200\}$
Strands diameter	$d_r = 71\ \mu m$
External stray inductor (placed on sec. side)	
Inductance	$L_\sigma = 88\ \mu H/n^2$
Boxed volume	$V_{box} = 0.058\ dm^3$
Magnetic core	Size = 1×E 42/21/15
Number of turns	$N = 12$
Air gap (distributed)	$l_{air} = \{1.5\ mm, 1.6\ mm, 1.5\ mm\}$
HF litz wire strands	$n = 1200$
Strands diameter	$d_r = 71\ \mu m$

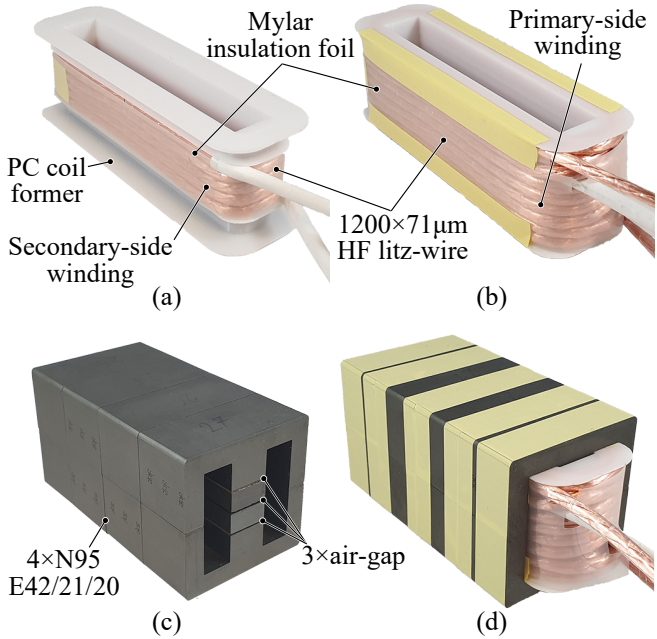

Fig. A.3: Assembly of a boost inductor/transformer. (a) Polycarbonate (PC) coil former with secondary-side winding. (b) Coil former with primary-side winding wound over the secondary-side winding. (c) Magnetic core material with distributed air gap of $l_{\text{air}} = \{0.5\,\text{mm}, 0.7\,\text{mm}, 0.5\,\text{mm}\}$. (d) Fully assembled transformer with the winding package placed in the core.

tape (not shown in the picture). Subsequently, the primary-side winding is wound over the Mylar foil and insulated from the magnetic core material with another Mylar foil as shown in Fig. A.3(b). The magnetic core shown in Fig. A.3(c) consists of 4 stacked E 42/21/20 N95 cores with a distributed air gap, cf. Table A.4. Fig. A.3(d) shows the fully assembled transformer with the winding package in the core, which is held together by polyester tape.

The assembly of the external stray inductance is similar and therefore not shown here. It should be noted that the core of the external stray inductor, 2×E 35/18/10 (point on the Pareto front) that was obtained by optimization was replaced by the theoretically larger 1×E 42/21/15. The E 42/21/15 has the same height as the core used for the transformer which allows a more optimal arrangement of the components.

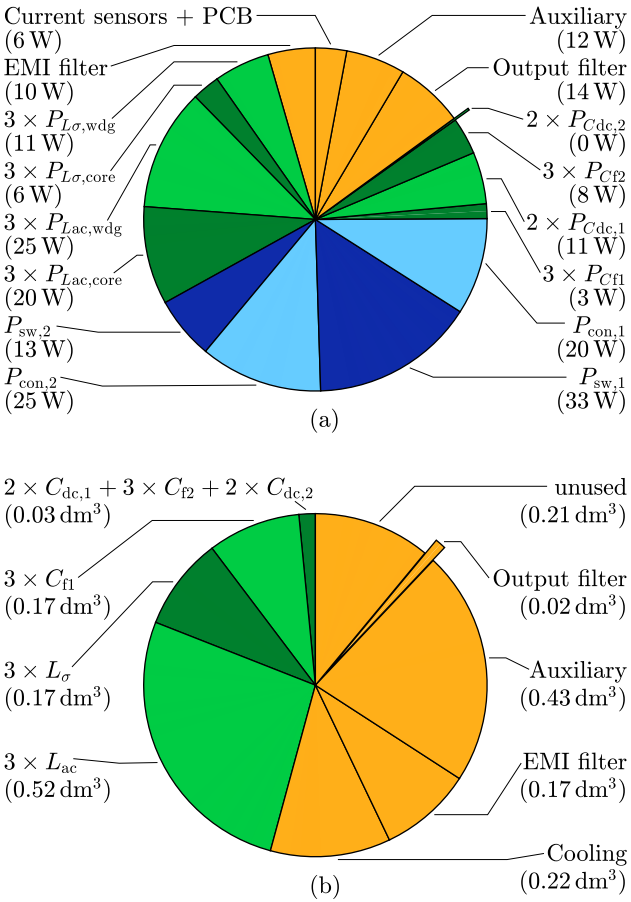

Fig. A.4: (a) Estimated loss distribution and (b) final volume distribution of the implemented hardware prototype with estimated efficiency of $\eta = 97.4\,\%$ and calculated power density of $\rho = 4.1\,\mathrm{kW/dm^3}$.

Finally, the EMI filter designed in Section 2.4 is used, which achieves a volume of 0.17 dm^3 (0.35 dm^3 was estimated).[2] The measured ESR of the EMI filter (measured from the primary-side ac terminals to the filter capacitances C_{f1}) is 22.5 mΩ (including precharge relays, PCB tracks, and connection terminals) measured with a 10 A dc current. This ESR corresponds to 9.6 W of losses (5 W was estimated in [51]) at full load. The distribution of the losses among the different converter components estimated with the models presented in [51] and the ESRs given in Table A.2 is shown in **Fig. A.4(a)**. The distribution of the boxed volumes among the different converter components of the final hardware prototype is shown in **Fig. A.4(b)**. The differently colored areas refer to auxiliary components such as current sensors, EMI filters, etc. in orange, to passive components such as capacitors and inductors in green, and to the power semiconductors in blue.

Fig. A.5(a) shows a picture of the realized hardware with the four ports labeled. **Fig. A.5(b)** shows the same hardware but with the upper PCB removed to allow a better view. The cooling fans blow air through the heat sink to the magnetic components in order to heat the core material of the magnetic components with the preheated exhaust air of the semiconductors. This arrangement is intentional to bring the core material to the optimum operating temperature of 80 °C at which the N95 core material shows minimal losses.

A.3 Measurement results

In the following, selected results of measurements with the hardware prototype are shown. **Fig. A.6** shows the measured phase voltages, $v_{ac,a}$, $v_{ac,b}$, and $v_{ac,c}$, together with the measured phase currents, $i_{ac,a}$, $i_{ac,b}$, and $i_{ac,c}$ for rectifier operation with nominal power at the secondary-side dc port, $P_2 = 8\,kW$, and no load on the primary-side dc port, $P_1 = 0$, (only four signals are measured at a time due to the limited number of measurement channels; for the purpose of reference, the voltage and current of phase a are shown in Fig. A.6(a) and Fig. A.6(b)). The waveforms of the phase voltages of phases a, b, and c depicted in Fig. A.6(a) are sinusoidal and phase-shifted by 120 ° with respect to each other, as described by (2.1). The currents in Fig. A.6(b) are sinusoidal and in phase with the corresponding phase voltages, resulting in a Power Factor (PF)

[2] The difference between the estimated and effective filter volume is due to the fact that [51] did not yet know about the EMI behavior of the D3ABC and therefore adopted the volume from the optimization with similar specifications and optimization objectives described in [84].

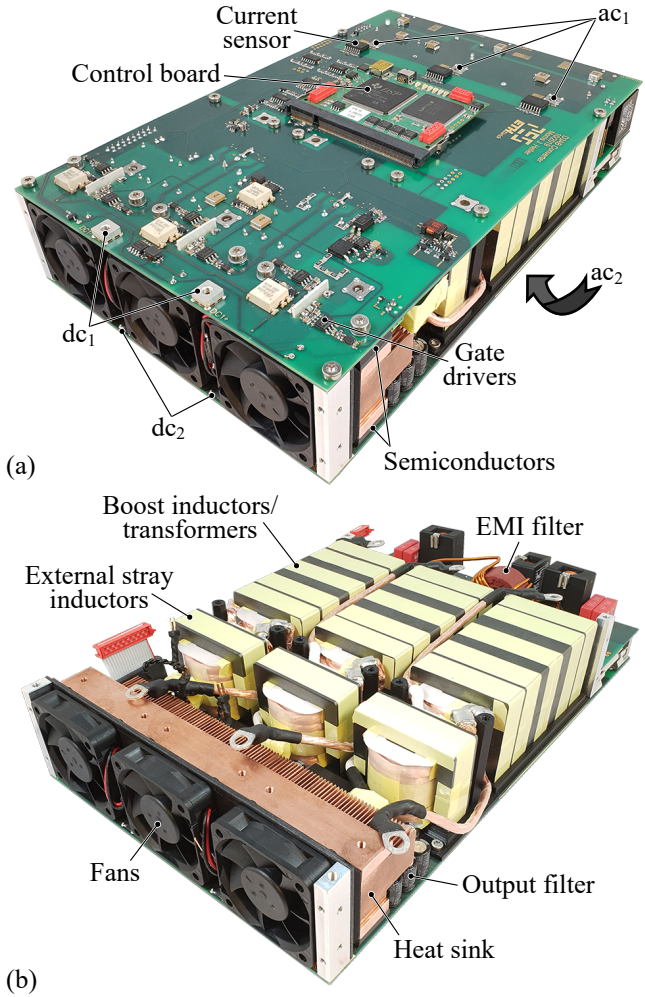

Fig. A.5: (a) Hardware demonstrator of the D3ABC featuring an output power of 8 kW for rectifier operation with galvanic isolation, i.e., from ac_1 to dc_2. The port ac_2 is located at the bottom of the converter and is therefore not visible on this picture. The overall dimensions are 150 mm × 240 mm × 54 mm = 5.91 in × 9.45 in × 2.13 in (width × depth × height). (b) Picture without top PCB revealing most of the components, e.g., heat sink, three coupled boost inductors, and three external stray inductors, which are used to increase the stray inductances of the coupled boost inductors according to the needs of the D3ABC. The labeled magnetic components are those of phase a.

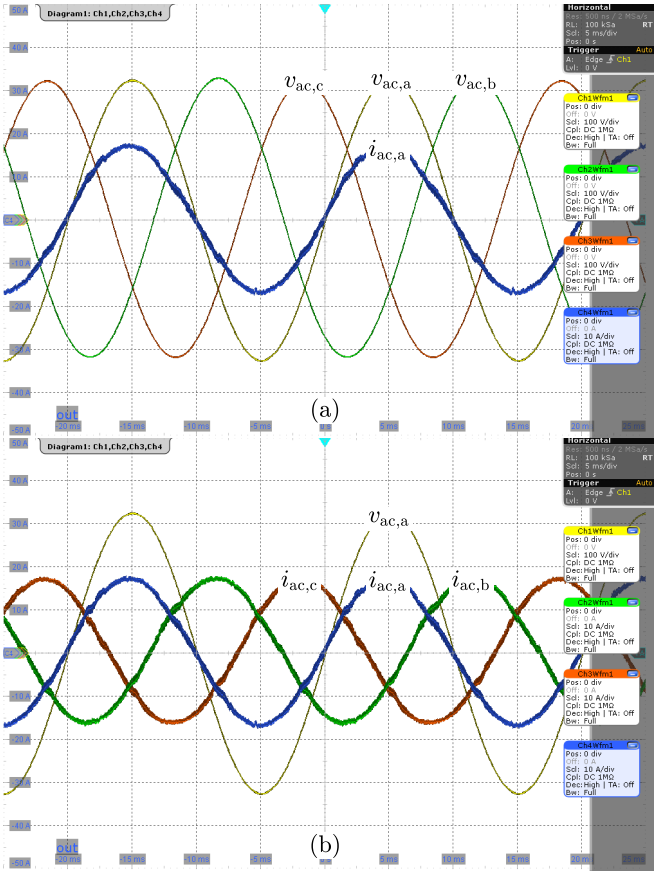

Fig. A.6: Screenshots from an oscilloscope measurement showing: (a) all three phase voltages (phase to neutral) and the phase current of phase a at port ac_1; (b) the phase voltage of phase a and all three phase currents at port ac_1. The converter operates as a PFC rectifier with a three-phase voltage source connected to the port ac_1 ($f_m = 50\,\text{Hz}$, $V_{ac,rms} = 230\,\text{V}$) and load resistors connected to the secondary-side dc port ($P_2 = 8\,\text{kW}$ on dc_2) and no load on the primary-side dc port ($P_1 = 0$ on dc_1).

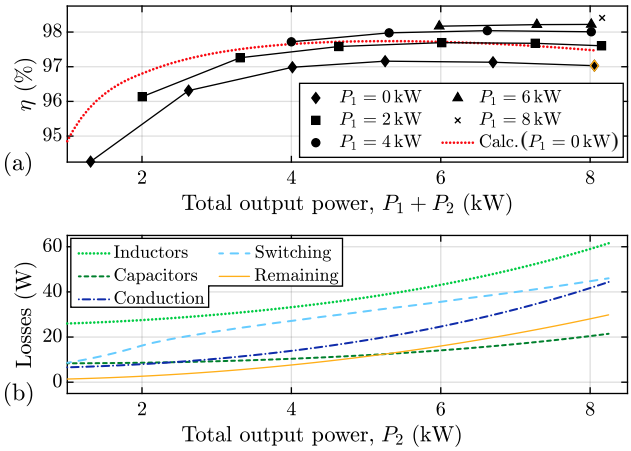

Fig. A.7: (a) Measured efficiency of the hardware in rectifier operation as a function of the loads on the primary-side and secondary-side dc ports, P_1 and P_2. The individual graphs show the efficiency for a given power $P_1 \in \{0, 2, 4, 6, 8\}$ kW and varying power P_2. (b) Changes of the individual losses as a function of the power P_2 ($P_1 = 0$). The inductor losses comprise of the losses in the boost inductor/transformer and the external stray inductor. The capacitor losses are the sum of the losses in the primary-side and secondary-side filter and dc link capacitors. The semiconductor losses are divided into conduction losses and switching losses. The yellow curve combines the remaining losses of the EMI filter, the output filter, and the current sensors. Additional losses due to the power demand of auxiliary components were neglected in these considerations, since the auxiliary circuits of the hardware were powered by a separate supply.

close to one, $\lambda = 0.994$. The Total Harmonic Distortion (THD) of the currents is THD $\leq 5.6\,\%$.

Fig. A.7(a) shows the measured efficiency of the hardware in rectifier operation as a function of the loads on the primary- and secondary-side dc ports, P_1 and P_2. The individual graphs show the efficiency for a given power $P_1 \in \{0, 2, 4, 6, 8\}$ kW and varying power P_2. The power P_2 is adjusted in discrete steps that satisfy

$$P_2 \in \min\left(\{0, 1.3, 2.7, 4.0, 5.3, 6.7, 8\}\,\mathrm{kW}, 8.0\,\mathrm{kW} - P_1\right) \tag{A.3}$$

so that the total power, $P_1 + P_2$, does not exceed the nominal power, $P_1 + P_2 \leq 8$ kW. Before the efficiency is read from the power meter, the converter was operated for a few minutes (until the value of the efficiency no longer changes)

at the considered operating point to bring the components to operating temperature. The point outlined in orange corresponds to the operating point ($P_1 = 0$ and $P_2 = 8\,\mathrm{kW}$) considered for the design and achieves an efficiency of 97.0 %. The green dotted line corresponds to the calculated efficiency as a function of power P_2 ($P_1 = 0$).

Fig. A.7(b) shows the calculated changes of the individual losses as a function of the power P_2 ($P_1 = 0$). The inductor losses comprise the losses in the boost inductor/transformer and the external stray inductor, the capacitor losses are the sum of the losses in the primary-side and secondary-side filter and dc link capacitors. The semiconductor losses are divided into conduction losses and switching losses. The yellow curve (labeled 'Remaining') is the sum of the losses of the EMI filter, the output filter, and the current sensors. Additional losses due to the power demand of auxiliary components were neglected in these considerations, since the auxiliary circuits of the hardware were powered by a separate supply.

A.4 Conclusion

This chapter refines the η–ρ-Pareto optimization for the D3ABC topology presented in [51] and subsequently implements a selected design in a hardware prototype. The loss models of the optimization are first extended by the losses in the capacitors, the output filter, and the current sensors. This results in a significant shift of the Pareto front of $\Delta\eta = -0.5\,\%$ at the desired power density of $\rho = 4\,\mathrm{kW/dm^3}$. The shift is mainly explained by substantial losses in the capacitors (due to high rms currents, LF polarization losses) and non-negligible resistances in the output filter. From the refined optimization, a design point with $\eta = 97.4\,\%$ and $\rho = 4.2\,\mathrm{kW/dm^3}$ is then detailed and implemented in a hardware prototype. For this design point, a suitable heat sink and a specific EMI filter is designed. The designed heat sink with fans and air duct has a volume of $V_{\mathrm{cool}} = 0.217\,\mathrm{dm^3}$, which is $0.091\,\mathrm{dm^3}$ larger than estimated in the optimization. In addition, the volume of the auxiliary circuits is also $0.130\,\mathrm{dm^3}$ higher than estimated. To compensate for this, the EMI filter and the output filter were designed with special attention to compactness, which explains the increased losses in these components. In return, the assembled hardware prototype achieves a power density of $\rho = 4.1\,\mathrm{kW/dm^3}$.

Finally, measurement results obtained on the realized hardware prototype in rectifier operation with rated power at the secondary-side dc port, $P_2 = 8\,\mathrm{kW}$, and without load at the primary-side dc port, $P_1 = 0$, show sinusoidal grid currents with a PF close to one, $\lambda = 0.994$, and a THD of less than

5.6 %. The measured efficiency at this operating point is $\eta = 97.0\,\%$. However, the origin of the additional losses, leading to $\Delta\eta = -0.4\,\%$ compared to the calculation (at $P_1 = 0$ and $P_2 = 8\,\mathrm{kW}$), is remaining, i.e. could not be determined.

B

Function of $\langle p \rangle$ for Advanced Modulation Approach

Subsection 3.3.4 presents an approach that increases the transferable power for the DAB part of the D3ABC. However, the used approach, i.e., the polynomial (3.31) used for $\langle p \rangle(t)$, is not further motivated in the mentioned section. Therefore, **Section B.1** first derives the function of $\langle p \rangle$ used in this approach based on general considerations. **Section B.2** then shows that the chosen approach is optimal with respect to the possible maximum power.

B.1 Derivation of the function for $\langle p \rangle(t)$

The derivation of the advanced modulation approach given in (3.31) starts with the simple approach which assigns a constant to $\langle p \rangle$,

$$\langle p \rangle (t) = P_0 \, a_0, \tag{B.1}$$

with constants a_0 and P_0. The constant P_0 contains all hardware specific terms that are independent of the modulation, cf. (3.16). Consequently, a_0 remains as degree of freedom for the modulation. Subsection 3.3.3 sets a_0 in a way that the highest possible maximum power of the DAB part $P_{\Sigma,\max}$ is achieved, but at the same time in each DAB converter phase the maximum phase power $P_{\max} = P_{\max,\mathrm{III}}$ is not exceeded. However, as Subsection 3.3.3 explains, the maximum power $P_{\Sigma,\max}$ is strongly constrained by the power $P_{\max}$ at the minimum and maximum duty cycles given by (3.22) and (3.23). **Fig. B.1** illustrates this by plotting $\langle p \rangle = P_0 \, a_0$, which corresponds to a horizontal line (marked with a_0) in the cross section view that was shown in Fig. 3.11(b).

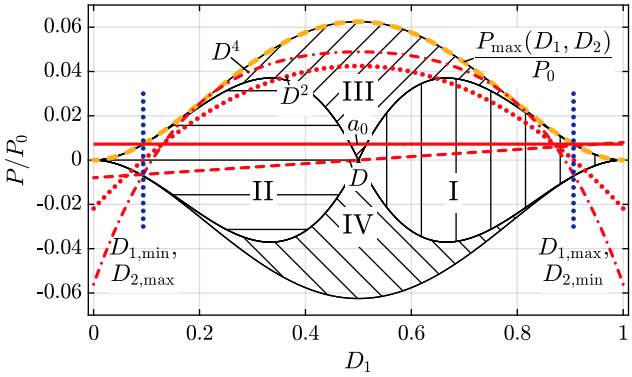

Fig. B.1: Cross section through Fig. 3.11(a) as shown in Fig. 3.11(b). Red lines marked with a_0, D, D^2, and D^4 represent the approaches for $\langle p \rangle$ with different functions that achieve a constant power in the DAB converter part. The approaches are within the operating range always below the maximum power (dashed orange line).

Although, the power $P_{\max}$ is strongly constrained at the minimum and maximum duty cycles, much higher power can be transmitted for other duty-cycle values, e.g., $D_{1,2} = 0.5$. Therefore, to utilize the higher power levels at these duty-cycle values the idea of making $\langle p \rangle$ dependent on the duty cycles is appealing. However, the question arises for which functions $f(D_1, D_2)$ for the power in each phase, $\langle p \rangle(D_1, D_2)$, the total power over all three phases $\langle p_\Sigma \rangle$, defined as

$$\langle p_\Sigma \rangle(t) = \langle p_{\mathrm{aA}} \rangle(D_{1\mathrm{a}}, D_{2\mathrm{a}}) + \langle p_{\mathrm{bB}} \rangle(D_{1\mathrm{b}}, D_{2\mathrm{b}}) + \langle p_{\mathrm{cC}} \rangle(D_{1\mathrm{c}}, D_{2\mathrm{c}}), \tag{B.2}$$

shows a constant waveform over time t, i.e., no power pulsation.

The derivation assumes that the duty cycles as a function of time t are sinusoidal with offsets equal to 1/2, as given in (3.5) and (3.6). However, for convenience, the derivation is done with $\tilde{D}_1$ and $\tilde{D}_2$ given as

$$\tilde{D}_{1,\mathrm{a,b,c}}(t) = D_{1,\mathrm{a,b,c}}(t) - \frac{1}{2} = \frac{1}{2} m_1 \sin\left(\omega_1 t + \theta_{\mathrm{a,b,c}}\right), \tag{B.3}$$

$$\tilde{D}_{2,\mathrm{A,B,C}}(t) = D_{2,\mathrm{A,B,C}}(t) - \frac{1}{2} = \frac{1}{2} m_2 \sin\left(\omega_2 t + \theta_{\mathrm{A,B,C}}\right), \tag{B.4}$$

in order to remove the offsets and use $2\pi f_1 = \omega_1$, $2\pi f_2 = \omega_2$, and $\Theta = 0$. The phase shifts are $\theta_{\mathrm{a,b,c}} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$, leading to duty cycles $\tilde{D}_{1,\mathrm{a,b,c}}(t)$ that are phase shifted by 120 ° to each other. The same applies to $\tilde{D}_{2,\mathrm{A,B,C}}(t)$, using $\theta_{\mathrm{A,B,C}} \in \{0\,^\circ, 120\,^\circ, 240\,^\circ\}$.

The first considered function is the linear function that uses only $\tilde{D}_1$, $f_{\tilde{D}}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1$. According to (B.2) $\langle p_\Sigma \rangle$ is the sum of all primary-side duty cycles, which leads to

$$\langle p_\Sigma \rangle(t) = \tilde{D}_{1a}(t) + \tilde{D}_{1b}(t) + \tilde{D}_{1c}(t) = 0. \tag{B.5}$$

This corresponds to a summation of three sinusoidal functions which are phase shifted by 120 °, i.e., $\langle p_\Sigma \rangle$ is equal to zero. Consequently, $f_{\tilde{D}}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1$ is a usable function for the phase power $\langle p \rangle$. Since this holds true for $\tilde{D}_1$, it also holds true for $\tilde{D}_2$. The functions for a_0, $\tilde{D}_1$, and $\tilde{D}_2$ can be added together resulting in

$$\langle p \rangle(t) = P_0 \left[a_0 + a_1 \tilde{D}_1(t) + b_1 \tilde{D}_2(t) \right], \tag{B.6}$$

as a first result for the proposed approach. An example for (B.6) with $a_0 = 0$ and $a_1 = b_1 > 0$ is drawn in Fig. B.1 (marked with D).

The next step considers quadratic functions of $\tilde{D}_1$, $f_{\tilde{D}^2}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1^2$. The derivation of $\langle p_\Sigma \rangle$ uses a trigometric identity (cf. Equ. 1.321.1 in [85]), which shows that the square of a sinusoidal function is equivalent to

$$\sin^2(x) = \frac{1}{2} - \frac{1}{2} \cos(2x). \tag{B.7}$$

If x in (B.7) is replaced by $\omega_1 t + \theta_{a,b,c}$ a cosine with double grid frequency is obtained. The frequency doubling leads to

$$\begin{aligned} \omega_1 t + 0\,^\circ &\xrightarrow{\times 2} 2\,\omega_1 t + 0\,^\circ, \\ \omega_1 t + 120\,^\circ &\xrightarrow{\times 2} 2\,\omega_1 t + 240\,^\circ, \\ \omega_1 t + 240\,^\circ &\xrightarrow{\times 2} 2\,\omega_1 t + 480\,^\circ = 2\,\omega_1 t + 120\,^\circ, \end{aligned} \tag{B.8}$$

i.e., three cosine functions which are phase shifted by 120 ° and consequently in $\langle p_\Sigma \rangle$ add up to zero. Therefore, for a function $f_{\tilde{D}^2}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1^2$ a total power

$$\langle p_\Sigma \rangle(t) = \tilde{D}_{1a}(t)^2 + \tilde{D}_{1b}(t)^2 + \tilde{D}_{1c}(t)^2 = \frac{3}{2} \tag{B.9}$$

results, where only the constant $3 \times 1/2 = 3/2$ remains. This extends the usable function for the approach to

$$\langle p \rangle(t) = P_0 \left[a_0 + a_1 \tilde{D}_1(t) + a_2 \tilde{D}_1(t)^2 + b_1 \tilde{D}_2(t) + b_2 \tilde{D}_2(t)^2 \right], \tag{B.10}$$

which is drawn with $a_1 = b_1 = 0$ and the parameter given by (3.40) in Fig. B.1 (marked with D^2).

The next logical step considers the function $f_{\tilde{D}^3}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1^3$. A sinus cubed is according to Equ. 1.321.2 in [85] equal to

$$\sin^3(x) = \frac{3}{4}\sin(x) - \frac{1}{4}\sin(3x). \tag{B.11}$$

The sum over the (phase-shifted) $\sin(x)$ functions of all three phases is, as already derived, equal to zero. The frequency tripling in $\sin(3x)$ with $x = \omega_1 t + \theta_{\mathrm{a,b,c}}$, however, leads to

$$\begin{aligned} \omega_1 t + 0\,^\circ &\xrightarrow{\times 3} 3\,\omega_1 t + 0\,^\circ, \\ \omega_1 t + 120\,^\circ &\xrightarrow{\times 3} 3\,\omega_1 t + 360\,^\circ = 3\,\omega_1 t + 0\,^\circ, \\ \omega_1 t + 240\,^\circ &\xrightarrow{\times 3} 3\,\omega_1 t + 720\,^\circ = 3\,\omega_1 t + 0\,^\circ, \end{aligned} \tag{B.12}$$

i.e, to three sine functions which are all in phase. These sine functions would therefore not cancle out in $\langle p_\Sigma \rangle$ and lead to a power pulsation with three times the mains frequency $3\omega_1$. Consequently, the function $f_{\tilde{D}^3}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1^3$ is not included in the approach.

Next is the function $f_{\tilde{D}^4}(\tilde{D}_1, \tilde{D}_2) = \tilde{D}_1^4$ where according to Equ. 1.321.3 in [85] a constant, a $\sin(2x)$, and a $\sin(4x)$ part are obtained. The sum over the $\sin(2x)$ components of the three phase powers is constant as already derived. Since the $\sin(4x)$ part can be divided into $\sin(2\times 2x)$, the same argumentation applies as for $\sin(2x)$ and the sum over the $\sin(4x)$ components of the three phase powers is constant as well. With this function added, the final approach presented in (3.31) results. An example of (3.31) with (B.13) is drawn in Fig. B.1 (marked with D^4).

It should be mentioned that all functions with $\tilde{D}_1^n$ for $n > 4$ lead to power pulsation, as, according to Equ. 1.320.3 in [85], all functions with odd $n > 1$ always have a $\sin(3x)$ component and, according to Equ. 1.320.1 in [85], those with even $n > 4$ have a $\sin(6x) = \sin(2 \times 3x)$ which both are not constant in $\langle p_\Sigma \rangle$. Further, functions with product terms of $\tilde{D}_1$ and $\tilde{D}_2$, e.g., $\tilde{D}_1 \times \tilde{D}_2$, also lead to power pulsations in case of $\omega_1 \neq \omega_2$ (with frequency $|\omega_1 - \omega_2|$ in the given example).

B.2 Examination of the maximum power

It was shown in Subsection 3.3.4 that the final approach (3.31) without $\tilde{D}_1^4$ part ($a_4 = b_4 = 0$) can achieve a maximum power of $P_{\Sigma,\max} =$

$3/16 P_0 \left(1 - m_{\max}^2\right)$. With the values for P_0 and $m_{\max}$ used for the numerical analysis in Subsection 3.3.5, this gives $P_{\Sigma,\max} = 8.5\,\mathrm{kW}$, which agrees well with the numerical results. A similar derivation for $a_4 = b_4 \neq 0$, which is not shown here for the sake of brevity, gives the coefficients

$$a_{0,\max} = \frac{1}{32}\left(2 - {m_{\max}}^4\right),\ a_{2,\max} = -\frac{1}{4}\left(1 - {m_{\max}}^2\right),\ a_{4,\max} = -\frac{1}{2}, \tag{B.13}$$

which results in a maximum power of

$$P_{\Sigma,\max} = \frac{3}{16} P_0 \left(1 - {m_{\max}}^2 + \frac{1}{8}{m_{\max}}^4\right). \tag{B.14}$$

It should be noted that, compared to the solution with $a_4 = b_4 = 0$ given in (3.41), the maximum power according to (B.14) does not approach zero for a maximum modulation index approaching one, $m_{\max} \longrightarrow 1$. Accordingly, modulation with $a_4 = b_4 \neq 0$ could possibly be interesting for operating scenarios in which very high modulation indices cannot be avoided. Using the previously used values for P_0 and $m_{\max}$ this leads to $P_{\Sigma,\max} = 9.8\,\mathrm{kW}$, which again agrees very well with the numerical results obtained in Subsection 3.3.5. Therefore, it is very likely that (B.14) refers to the highest power that can be achieved with (3.31). However, the remaining question is whether a different approach exists that can achieve even higher power.

To answer this, the case where each phase transmits the maximum phase power is considered. The maximum phase power is given by the function $P_{\max,\mathrm{III}}$. If the phase power is set equal to this maximum power, $\langle p \rangle = P_{\max,\mathrm{III}}$, a constant waveform of the total power $\langle p_\Sigma \rangle(t)$ is rather improbable, but in exchange it is guaranteed that the maximum possible power is transmitted at any time.

Substituting the duty cycles $D_1 = \tilde{D}_1 + 1/2$ and $D_2 = \tilde{D}_2 + 1/2$ with the definitions given in (B.3) and (B.4) and with $m_1 = m_2 = m_{\max}$ into the function of $P_{\max,\mathrm{III}}$ given in Table 3.3, results in

$$\begin{aligned}\langle p \rangle(t) = \frac{1}{16} P_0 \Big[\ & 1 - {m_{\max}}^2 \sin^2(\omega_1 t + \theta_1) - {m_{\max}}^2 \sin^2(\omega_2 t + \theta_2) \\ & + \underbrace{{m_{\max}}^4 \sin^2(\omega_1 t + \theta_1) \sin^2(\omega_2 t + \theta_2)}_{(1)} \Big].\end{aligned} \tag{B.15}$$

In (B.15) the constant in the rectangular bracket is equal to three and the $\sin^2$ components as shown in (B.9) are equal to $3/2$. What remains is the product of the $\sin^2$ components marked as (1) which is again simplified with

a trigometric identity. If the identity given in (B.7) is substituted for $\sin^2$, we get

$$(1) = \frac{1}{4} {m_{\max}}^4 \Big[1 - \cos(2\omega_1 t + 2\theta_1) - \cos(2\omega_2 t + 2\theta_2) + \underbrace{\cos(2\omega_1 t + 2\theta_1) \cos(2\omega_2 t + 2\theta_2)}_{(2)} \Big] \tag{B.16}$$

for the product term in the rectangular bracket of (B.15). In $\langle p_\Sigma \rangle$, again the constant in the rectangular bracket is equal to three and the cosine components as shown in (B.5) are equal to zero. What remains is the product of the cosine components marked by (2). According to Eq. 1.314.3 in [85], with $x = a + b$ and $y = a - b$ the product $\cos(a)\cos(b)$ is equal to

$$\cos(a)\cos(b) = \frac{1}{2}\cos(a+b) + \frac{1}{2}\cos(a-b). \tag{B.17}$$

The summation in the $\cos(a+b)$ part with $a = \omega_1 t + \theta_{\mathrm{a,b,c}}$ and $b = \omega_2 t + \theta_{\mathrm{A,B,C}}$ leads to

$$\begin{aligned} \omega_{1,2}\, t + 0\,^\circ &\xrightarrow{+} |\omega_1 + \omega_2|\, t + 0\,^\circ, \\ \omega_{1,2}\, t + 120\,^\circ &\xrightarrow{+} |\omega_1 + \omega_2|\, t + 240\,^\circ, \\ \omega_{1,2}\, t + 240\,^\circ &\xrightarrow{+} |\omega_1 + \omega_2|\, t + 480\,^\circ = |\omega_1 + \omega_2|\, t + 120\,^\circ, \end{aligned} \tag{B.18}$$

i.e., three cosine functions which are phase shifted by 120 ° and therefore add up to zero in $\langle p_\Sigma \rangle$. The subtraction in the $\cos(a-b)$ part, on the other hand, leads to

$$\begin{aligned} \omega_{1,2}\, t + 0\,^\circ &\xrightarrow{-} |\omega_1 - \omega_2|\, t + 0\,^\circ, \\ \omega_{1,2}\, t + 120\,^\circ &\xrightarrow{-} |\omega_1 - \omega_2|\, t + 0\,^\circ, \\ \omega_{1,2}\, t + 240\,^\circ &\xrightarrow{-} |\omega_1 - \omega_2|\, t + 0\,^\circ, \end{aligned} \tag{B.19}$$

i.e., three cosine functions which are in phase and therefore remain in $\langle p_\Sigma \rangle$.

With all parts for $\langle p_\Sigma \rangle$ added together, the result is

$$\langle p_\Sigma \rangle_{\max}(t) = \frac{3}{16} P_0 \left[1 - {m_{\max}}^2 + \frac{1}{4} {m_{\max}}^4 + \frac{1}{8} {m_{\max}}^4 \cos(2\,|\omega_1 - \omega_2|\, t) \right]. \tag{B.20}$$

In summary, if each DAB converter of the three phases is operated at the maximum possible power at any time, a total power $\langle p_\Sigma \rangle$ results as given in

(B.20). $\langle p_\Sigma \rangle_{\max}$ therefore corresponds to the maximum transmittable total power of the DAB part of the D3ABC at any time. However, $\langle p_\Sigma \rangle_{\max}$ shows a cosinusoidal pulsation with frequency $2\,|\omega_1 - \omega_2|$.

Now, if a modulation scheme should guarantee that the transmitted power $\langle p_\Sigma \rangle$ shows a constant waveform, the power P_Σ transmitted by this modulation scheme must be strictly smaller than the maximum total power, $P_\Sigma < \langle p_\Sigma \rangle_{\max}$. Consequently, the maximum constant power $P_{\Sigma,\max}$ of any modulation scheme is equal to the minimum of the maximum total power, $P_{\Sigma,\max} = \min(\langle p_\Sigma \rangle_{\max})$. The minimum of (B.20) occurs when $2\,|\omega_1 - \omega_2|$ is equal to -1, resulting in

$$\min(\langle p_\Sigma \rangle_{\max}(t)) = \frac{3}{16} P_0 \left(1 - {m_{\max}}^2 + \frac{1}{8} {m_{\max}}^4\right). \tag{B.21}$$

(B.21) is identical to (B.14), which is the maximum total power that can be achieved with the proposed approach (3.31). Consequently, a modulation scheme that is based on the approach proposed with (3.31) allows the maximum possible power transfer in the DAB part of the D3ABC.

B.3 Conclusion

This chapter motivates the approach given in (3.31), which is used in the context of the four-port operation of the D3ABC, to eliminate LF power pulsations. It is shown on the basis of trigometric identities that, with this approach, a constant waveform results for the total power in the DAB part of the D3ABC. Finally, it is proven that the maximum transferable power can be realized with the proposed approach.

C

Investigation of the Influence of the DC Link Capacitance on the Resonance Frequencies of the First AC-Side Filter Stage

The inductances and capacitances of the elements of the first filter stage of a VSC, e.g., L_{ac} and C_f as shown in **Fig. C.1**, are usually chosen so that the resulting resonance frequency is well below the switching frequency, f_s, of the converter. However, in the shown example it is not immediately obvious how the values of all the inductors and capacitors affect the resonance frequency. This is especially true for the dc link capacitors, C_{dc}, of which only two are present for the three phases. To better understand the impact of the dc link capacitances on the first ac-side filter stage, the resonance frequencies of the converter shown in Fig. C.1 were examined in a circuit simulation.

C.1 Circuit simulation

The schematic of the analyzed converter is shown in Fig. C.1. The component and voltage values used in the simulation are given in Table 2.2 and Table 2.1, respectively. In addition, each inductor has an ESR of 100 mΩ for damping. The operation and generation of the switching signals is described in **Subsection 2.2.2**, i.e., the converter behaves the same as the primary side of the Dual Three-Phase Active Bridge (D3AB) converter when it is not coupled to the secondary side. The inductors, $L_{net} = 1.7\,\text{mH}$, have a value more than 10× larger than $L_{ac} = 134\,\mu\text{H}$, so L_{net} and the mains can be neglected

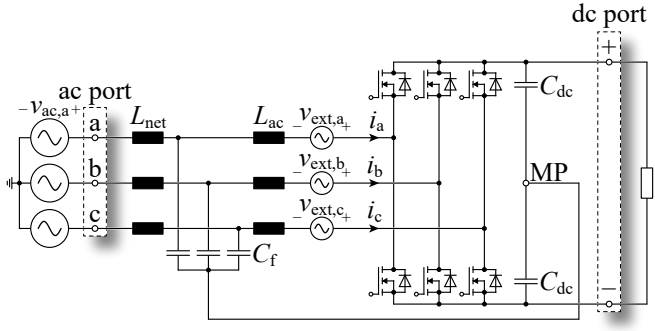

Fig. C.1: Investigated circuit of the VSC with a first ac-side filter stage considered in the circuit simulations. The VSC is operated as a rectifier, drawing power from the mains, v_{ac}, which is dissipated in the resistor connected to the dc link. The voltage sources, v_{ext}, are used to identify resonances in the first ac-side filter stage, which consists of a boost inductor, $L_{ac} = 134\,\mu H$, and a filter capacitor, $C_f = 10\,\mu F$, in each phase. The three grid side inductors L_{net} have a value more than 10× larger than L_{ac}, so L_{net} and the mains can be neglected for the following considerations.

when considering the resonance frequency of the first filter stage. In the considered operation, the converter draws a power of 8 kW from the mains, which is dissipated in the resistor connected to the dc link.

The three voltage sources, $v_{ext,a}$, $v_{ext,c}$, and $v_{ext,c}$, generate an excitation voltage given as,

$$\begin{aligned} v_{ext,a,b,c}(t) &= A\left(v_{ext,dm,a,b,c}(t) + v_{ext,cm}(t)\right), \\ v_{ext,dm,a,b,c}(t) &= \sin\left(2\pi f_{ext} t + \theta_{a,b,c}\right),\ \theta_{a,b,c} \in \{0°, 120°, 240°\}, \\ v_{ext,cm}(t) &= \sin\left(2\pi f_{ext} t\right), \end{aligned} \tag{C.1}$$

with frequency f_{ext} and amplitude A. These excitation voltages excite each phase with a small DM and CM voltage with amplitude $A = 1\,V$ and a constant frequency below the switching frequency $f_{ext} < f_s$, i.e., the excitation voltages have a negligible influence on the rectifier operation of the converter. After the simulation has reached steady state, the three phase currents, i_a, i_b, and i_c, are recorded over one mains period (e.g., shown in **Fig. C.2** for phase a) and then separated with

$$\begin{aligned} i_{cm} &= \frac{i_a + i_b + i_c}{3}, \\ i_{dm,a,b,c} &= i_{a,b,c} - i_{cm}, \end{aligned} \tag{C.2}$$

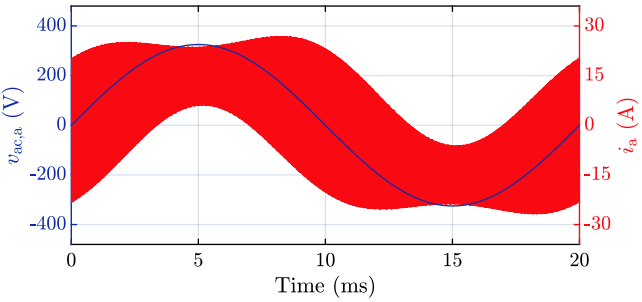

Fig. C.2: Simulated mains voltage, $v_{ac,a}$, and phase current, i_a, waveforms of phase a for rectifier operation. Component values and parameters used in the simulation are given in Table 2.2 and Table 2.1, respectively.

into DM and CM components. Finally, a post-processing extracts the components with frequency f_{ext} from the currents $i_{dm,a,b,c}$ and i_{cm}.

C.2 Simulation results

The circuit simulation, recording, and post-processing is done several times with a range of different excitation frequencies f_{ext}. The solid black line in **Fig. C.3** shows the extracted DM and CM current amplitudes in dBA as a function of the frequency f_{ext}. Both DM and CM characteristics show peaks in the amplitudes indicating the presence of series LC resonant circuits. The peak in the CM characteristic occurs at a higher frequency, i.e. it is closer to the switching frequency $f_s = 35\,\text{kHz}$, and therefore the CM component is investigated further. First, the simulation series is repeated using half the value for the dc link capacitances, $C_{dc}/2$. The green dashed line in Fig. C.3 shows the resulting current amplitudes. It can be seen that the resonance frequency in the CM component increases as expected (the first peak on the DM characteristic is determined by the series resonance frequency of L_{ac} and C_f). The same is true for the result shown as a blue dotted line in Fig. C.3 which is obtained with half the value for the filter capacitances, $C_f/2$, indicating that the CM resonance frequency depends on the values of both capacitances, C_{dc} and C_f.

This behavior of the CM resonance frequency can be explained as follows. By definition, the CM component of the currents, i_a, i_b, and i_c, is the component that is equal in all three phases. Assuming a symmetric mod-

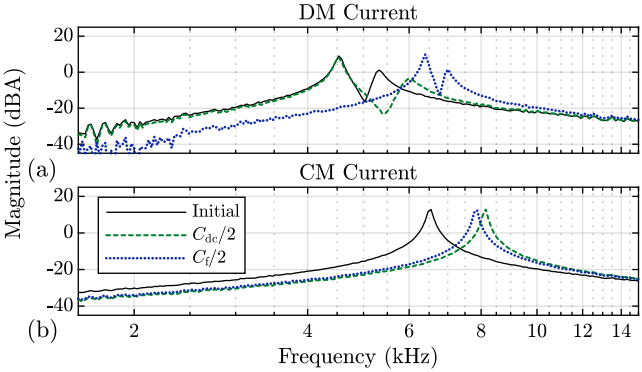

Fig. C.3: Simulated DM and CM current amplitudes in dBA (e.g., 20 dBA represents a current of 10 A) as a function of the excitation frequency f_{ext}. The solid black line shows the initial result, the green dashed line the result with half the value for the dc link capacitances, $C_{dc}/2$, and the blue dotted line with half the value for the filter capacitances, $C_f/2$. Initial case simulation parameters: $L_{ac} = 134\,\mu H$, $C_f = 10\,\mu F$, $C_{dc} = 12\,\mu F$. When two voltage sources are used instead of the dc link capacitors (corresponding to a very large dc link capacitance value), the DM and CM characteristics have the same resonant frequency given by L_{ac} in series with C_f.

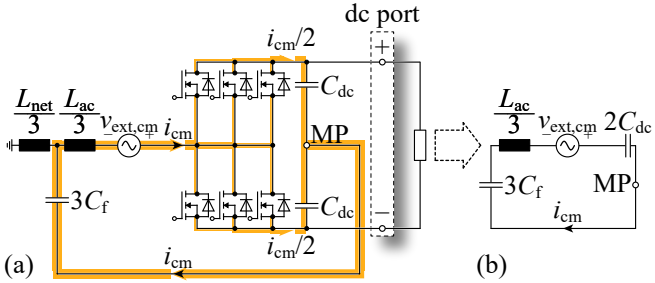

Fig. C.4: Derivation of the CM equivalent circuit. (a) Assuming a symmetric modulation scheme, half of the CM current, $i_{cm}/2$, is conducted through the positive rail and half through the negative rail of the dc link, recombined at the dc link mid-point, conducted through the three filter capacitors, $3C_f$, and, since the grid is decoupled by $L_{net}/3$, back through the three filter inductors, $L_{ac}/3$, closing the loop. (b) Resulting equivalent circuit, given the current path shown in (a).

ulation scheme, one would expect half of the CM current to be conducted through the positive rail and half through the negative rail of the dc link as illustrated in **Fig. C.4(a)**. Since the dc link capacitors have a much lower impedance than the load resistance at the frequencies considered, the two halves are each conducted through a dc link capacitor, C_{dc}, and recombine at the mid-point of the dc link, denoted by MP. From there, the CM current is conducted through the three filter capacitors, $3C_f$, and, since the grid is decoupled by $L_{net}/3$, which has more than 10× the impedance of $L_{ac}/3$, back through the three inductances, $L_{ac}/3$, closing the loop. This results in the series resonance circuit shown in **Fig. C.4(b)** which, given the values used in the simulations, shows a resonance at $f_r \in \{6.52\,\text{kHz}, 8.13\,\text{kHz}, 7.84\,\text{kHz}\}$. These resonance frequencies are in good agreement with the values obtained by the simulations.

Further simulations showed that the proposed equivalent circuit also holds for operation as an inverter instead of a rectifier, with different modulation schemes (e.g. interleaved carries, Discontinuous Pulse Width Modulation (DPWM) MIN/MAX), and different modulation depths (which take influence on the DM resonant frequencies). Furthermore, the simulation results indicate that no cross-coupling between DM and CM occurs due to the switching of the half-bridges (i.e., excitation with a pure DM signal leads to zero CM current and vice versa).

C.3 Conclusion

The derived CM equivalent circuit allows to calculate the resonance frequency of the first filter stage of a VSC. It was found that for CM current the two dc link capacitors are effectively connected in parallel, resulting in $2C_{\mathrm{dc}}$ in series with the effective capacitance, $3C_{\mathrm{f}}$, of the ac-side filter capacitors. The proposed equivalent circuit holds for operation as a rectifier and inverter, different modulation schemes, and different modulation depths.

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Curriculum Vitae

Personal Information

Name	Morris Jonatan Heller
Date of birth	February 8, 1990
Place of birth	Luzern, Switzerland
Citizen of	Luzern, Switzerland
Contact	mheller@lem.ee.ethz.ch
	morris_heller@hotmail.com
	+41 78 688 09 52

Education

2018 – 2022	Doctorate - Power Electronic Systems Laboratory (PES) Swiss Federal Institute of Technology - ETH Zurich Zurich, Switzerland
2015 – 2018	MSc Information Technology and Electrical Engineering Swiss Federal Institute of Technology - ETH Zurich Zurich, Switzerland
2011 – 2014	BSc in Science in Electrical Engineering Hochschule Luzern/FHZ, Horw, Switzerland
2006 – 2010	Apprenticeship as an Electronics Technician RUAG Aviation, Emmen, Switzerland

Work Experience

2018	Research Assistant - Power Electronic Systems Laboratory (PES) Swiss Federal Institute of Technology - ETH Zurich Zurich, Switzerland
2014 – 2015	Research Assistant Hochschule Luzern/FHZ, Horw, Switzerland
2010 – 2011	Electrical Technician RUAG Aviation, Emmen, Switzerland