Hybrid Integrated Voltage Regulators for Modern Microprocessor Applications

Diss. ETH No. 28006

Hybrid Integrated Voltage Regulators for Modern Microprocessor Applications

A thesis submitted to attain the degree of

DOCTOR OF SCIENCES of ETH ZURICH
(Dr. sc. ETH Zurich)

presented by

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2021

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It is not the strongest of the species that survives,
nor the most intelligent that survives.
It is the one that is the most adaptable to change.
– Inspired by Charles Darwin

O saber a gente aprende com os mestres e os livros.
A sabedoria, se aprende com a vida e com os humildes.
– Cora Coralina

Acknowledgments

Firstly, I would like to thank Prof. Johann W. Kolar for the trust and for giving me the opportunity to be part of the Power Electronic Systems (PES) laboratory as a scientific assistant and as a Ph.D. student. He was always very supportive and gave me all the means and freedom to conduct my research. His guidance and valuable scientific contributions were crucial for the successful conclusion of my work. Special thanks also go to Florian Krismer who was always supporting me on the publications and on the development of new ideas. He always ensured the accuracy and quality of my Ph.D. work. Thanks as well Prof. Marcelo L. Heldwein for supervising my master thesis and for creating my first link with the PES laboratory. I thank and appreciate very much the opportunity given to me by my managers Thomas Toifl, Robert Haas, Bruno Michel, and Angeliki Pantazi to conduct this research on power management at the IBM Research Laboratory in Zurich (ZRL).

I would also like to thank Prof. Eckart Hoene for taking his time reviewing this thesis and for accepting to be the co-examiner of my Ph.D. defense. A special thanks as well to Prof. Ulrike Grossner for being part of my defense session and for chairing it.

Many other very special people participated in the long journey of my Ph.D. studies. I would like to express here all my gratitude to them and to say that they made this very challenging period also very enjoyable and worth to remember. I would like to specially thank Toke Andersen, Arvind Sridhar, Riduan K. Aljameh, Dario Kneubuehler, Stephan Paredes, and Thomas Brunschwiler for all the support, collaboration, and friendship over the years we worked together at IBM, especially during the years of the CarrICool project. Thank you Beat Weiss and Ralph Heller for the very important contributions on the assembling of my demonstrators and measurement setup. Also very important, a big thanks to the other excellent students (besides Riduan K. Aljameh and Dario Kneubuehler) Marco Müller and Reto Christen that I had the luck to supervise.

Many thanks to the high-speed I/O group crew of IBM ZRL: Alessandro Cevrero, Ilter Özkaya, Hazar Yüksel, Pier-Andrea Francese, Christian Menolfi, Thomas Morf, Matthias Brändli, Marcel Kossel, Danny Luu, Serdar Yonar, and Jörg-Erik Sagmeister. It was a privilege to work closely with such talented and skilled people in the microelectronics field. I definitely learned a lot about the world of chip design from them. Many thanks for the support specially during the extremely critical times of the chip tape-outs.

Special thanks to Zoran Pavlovic, Santosh Kulkarni, Paul McCloskey, Caroline Rabot, Cian Ó Mathuna, Frederic Voiron, Mohamed Jatlaoui, and Wolfram Steller that worked in the power management working package of the CarrICool project outside IBM and ETH. It was a great and fruitful multidisciplinary collaboration between us. Thanks for the great time we had during the meetings and events around the world.

Thanks a lot to my office mates of IBM which I had the pleasure to spend quite some time inside and outside the office together: Giulia Prone, Diego Monserrat, Luca del Carro, Jens Ammann, Rahel Straessle, Ozgnur Ozsun, Gianmarco Gabrieli, Suiying Ye, Labinot Jakupi, Alessio Quercia, and Jonas Zürcher. Thanks Carina Joly, Shadi Fatayer, Fabio Scafirimuto, Nico Mosso, Patrick Ruch, Gerd Schlottig, Emanuel Lörtscher, Antonio La Porta, Martino Dazzi, and Ephraim Friedli for the nice time together and joyful conversations.

At the PES laboratory, I had the opportunity to share many memorable moments with friends and colleagues which contributed directly or indirectly to the accomplishment of this work. Thanks Gabriel Ortiz, Andreas Müsing, Hirofumi Uemura, Arda Tüysüz, David Boillat, Roman Bosshard, Yanick Lobsiger, Patricio Cortés, Luis J. C. B. Camurça, Grayson Zulauf, Riccardo Pittini, Thiago Soeiro, Jonas Huber, Dominik Bortis, Ralph Burkart, Matthias Kasper, Christoph Gammeter, Thomas Guillod, Michael Leibl, Oliver Knecht, Daniel Rothmund, Michael Flankl, Tobias Wellerdieck, Marcel Schuck, Pascal Püntener, Thomas Holenstein, Julian Böhler, Jon Azurza, Piotr Czyz, Michael Antivachis, Mattia Guacci, Michael Haider, Morris Heller, Emanuel Hubmann, Gustavo Knabben, David Menzi, Spasoje Miric, Dominik Neumayr, Pascal Niklaus, Rosario Giuffrida, Panteleimon Papamanolis, Jannik Schäfer, Yunni Li, and Daifei Zhang. It was a unique experience to share the office and working environment with so many smart students. I will also not forget the many fun occasions and adventures in the official PES events and in the non-official ones, like the ones at bQm =].

A big thanks to the entire staff of the PES laboratory: Peter Albrecht, Roswitha Coccia, Damaris Egger, Monica Kohn, Prisca Maurantonio, Yvonne Schnyder-Lieberherr, Peter Seitz, Claudia Stucki, and Marina Eisenstat. Their careful and supportive work is not only part of what makes the PES laboratory great and efficient, but also gives a family touch to the environment creating stronger bonds between the people.

During my Ph.D. studies, some difficulties arose which I could not handle myself alone. A very special thanks to three amazing, kind, and good hearted people, Monica Manni, Vânia Camurça, and Monica Kohn, for giving me strength and hope during the darkest moments I faced in my journey. Thank

you very much again for the support in these particular difficult moments to Arvind Sridhar, Thomas Brunchwiler, Riduan K. Aljameh, Angeliki Pantazi, Panteleimon Papamanolis, Pier-Andrea Francese, Gustavo Knabben, Levy F. Costa, Rodrigo Santos, Decio Haramura, Luis J. C. B. Camurça, Florian Krismer, and Prof. Johann W. Kolar.

Finally, thanks my dear salsa partner and girlfriend Valeria Bragaglia for all the love, support, patience, and resilience during this challenging period of my life. The biggest thanks go to my little sister Gabriela and to my parents Pedro and Ângela to whom I have strongest admiration and love. It was very difficult to live far from them, but they always made sure, despite the distance, that I never felt alone in my journey. Thanks as well all my other family members which were cheering for me in Brazil. They always welcomed me with open arms all the times I had the chance to go back to my homeland.

Zurich, October 2021

Pedro André Martins Bezerra

Abstract

The electricity consumption by Information and Communication Technologies (ICT) is expected to grow exponentially from 2020 reaching a share of 21 % of the global electricity usage by 2030. This increase in energy consumption is driven by new applications such as cloud computing, Internet of Things, mobile communication, automotive and Artificial Intelligence, as well as the increase of performance of microprocessors, which have nowadays tens of cores and operate at clock frequencies that reach 5 GHz. To cope with the high power demand of microprocessors without surpassing the maximum chip temperatures, advanced techniques, know as 'More than Moore', such as Dynamic Voltage and Frequency Scaling (DVFS) and granularity of voltage domains, are employed. These techniques require the Point-of-Load (PoL) Voltage Regulators (VRs) to be located very close to the microprocessor to provide fast response to load changes and to reduce losses in the package parasitics. Traditional VRs located on the motherboard are neither able to provide the fast dynamic requirements of modern microprocessor loads nor the necessary granularity of voltage domains due to their low switching frequency operation and large sizes.

Hybrid Integrated Voltage Regulators (IVRs) use the same transistors as the microprocessor die to implement the active parts of the power converter which allow them to operate efficiently at switching frequencies greater than 50 MHz. The high switching frequency operation reduces the size of the passive components, and improves the converter dynamic response to load changes compared to VRs located at the motherboard. In the considered work, a IVR is realized in a 14 nm CMOS technology, which provides high-speed short-channel transistor devices that feature lowest switching losses. However, the short-channel transistors are subject to relatively low breakdown voltages. Since the input voltage of the IVR exceeds the breakdown voltage of the short-channel transistors, a buck converter whose switching stage is composed of a Half-Bridge with Stacked Transistors (HBST) serves as the basic topology in this work. The HBST circuit is extended by an Active Neutral Point Clamping (ANPC) circuit with Independent Clamping Switches (ICS), to ensure balanced blocking voltages across the stacked transistors of the switching stage, maintain Zero Voltage Switching (ZVS) capabilities, and remain capable of disabling the power stage, i.e., to achieve high impedance at the switching node of the power stage, to enable phase-shedding when operated as part of a multi-phase converter. These features cannot be simultaneously achieved with state-of-the art realizations of HBSTs. In order to verify the feasibility and efficiency performance of the proposed HB com-

pared to the state-of-the-art HBSTs, a versatile chip capable of also generating the gate signals of a conventional HBST and a ANPC HBST is designed in 14 nm CMOS technology. This chip is used to implement a four-phase PCB-based IVR which uses off-chip discrete components to implement the input and output filters. A novel characterization methodology based on post-layout simulations, thermal inspections of the chip temperature, and electrical measurements, that allows for the separation of the on-chip losses from the off-chip losses, is proposed. The PCB-based IVR achieves a peak efficiency of 84.1 % at an output power of $P_{\mathrm{out}} = 640\,\mathrm{mW}$ and a switching frequency of $f_{\mathrm{s}} = 50\,\mathrm{MHz}$. At $P_{\mathrm{out}} = 890\,\mathrm{mW}$, a chip current density of $24.7\,\mathrm{A/mm^2}$ is achieved. Compared to the state-of-the art IVRs in 14 nm, the PCB-based IVR achieves similar efficiencies, but with approximately twice the chip current density. The performed loss analysis reveals that at least 25 % of the total chip losses are due to conduction losses in the resistances of the chip interconnects, i.e., metal layer stack and Power Distribution Network (PDN), at 50 MHz switching frequency operation.

The characterization of the PCB-based IVR indicates that the parasitic components of the package affect the linearity between the duty cycle and the input to output voltage conversion ratio at high switching frequencies and high output currents. Therefore, to reduce the parasitic components of the package, 2.5-D all-silicon IVRs are designed, experimentally investigated, and characterized. Finally, future research challenges in the area of power management related to the IVR design and package are presented.

Kurzfassung

Aufgrund erweiterter und neu entstehender Anwendungen in den Bereichen der Kommunikations- und Informationstechnologie, wie z.B. Cloudcomputing, Internet der Dinge (Internet of Things, IoT), Mobilkommunikation, Fahrzeugtechnik und künstliche Intelligenz, wird erwartet, dass der Stromverbrauch in diesen Bereichen ab dem Jahr 2020 exponentiell zunimmt und im Jahr 2030 bereits einen Anteil von 21% am weltweiten Stromverbrauch erreicht. Ein Teil dieser Zunahme ist auch auf die zunehmende Leistungsfähigkeit moderner Mikroprozessoren zurückzuführen, welche aktuell z.T. über Dutzende Rechenwerke verfügen und mit Taktfrequenzen von bis zu 5 GHz betrieben werden. Um einen unnötigen Anstieg des Leistungsbedarfs moderner Mikroprozessoren zu vermeiden – und auch, um zu gewährleisten, dass die maximal zulässige Chiptemperatur nicht überschritten wird – kommen moderne Konzepte zum Einsatz, die unter dem Begriff 'More than Moore' zusammengefasst werden, z.B. die dynamische Anpassung der Versorgungsspannung und der Taktfrequenz (Dynamic Voltage and Frequency Scaling, DVFS) und die Auftrennung der auf dem Chip implementierten Gesamtschaltung in Schaltungsdomänen mit unabhängigen Versorgungsspannungen. Für eine bestmögliche Realisierung dieser Konzepte sollten die zur Bereitstellung der Versorgungsspannungen erforderlichen Spannungsregler (sog. Point-of-Load Spannungsregler) möglichst nahe an den zugeordneten Schaltungsdomänen des Mikroprozessors platziert werden. Dies dient einerseits dazu, eine schnelle Reaktion auf Laständerungen zu gewährleisten; andererseits lassen sich mit einer geeigneten Platzierung der Spannungsregler auch die Verluste in den parasitären Komponenten der Zuleitungen zum Chip (z.B. Gehäuse, Bonddrähte) niedrig halten. Entsprechend geraten traditionelle, auf der Hauptplatine eines Rechners platzierte Spannungsregler im Zusammenhang mit den Erfordernissen welche sich aus den "More than Moore"-Konzepten ergeben an ihre technische Grenze. Beispielsweise lassen sich mit traditionellen Spannungsreglern die dynamischen Erfordernisse nicht erfüllen, da solche Spannungsregler nur mit vergleichsweise geringen Schaltfrequenzen betrieben werden können.

Der in dieser Arbeit untersuchte hybride integrierte Spannungsregler basiert auf der bekannten Topologie des Tiefsetzstellers, dessen Schaltstufen mit denselben Transistoren wie für den Mikroprozessor verwendet realisiert werden. Für die Realisierung der Schaltstufen des Spannungsreglers kommen sogenannte Short-Channel Transistoren einer modernen 14 nm CMOS Technologie zum Einsatz, welche nur sehr geringe Schaltverluste aufweisen und einen effizienten Betrieb bei Schaltfrequenzen von mehr als 50 MHz er-

möglichen. Der Betrieb der Spannungsregler bei so hohen Schaltfrequenzen ermöglicht einerseits eine ausreichend hohe Bandbreite der Ausgangsspannungsregelung und andererseits eine Verringerung der Baugrössen der für die Filterung der geschalteten Ausgangsspannungen der Spannungsregler benötigten passiven Komponenten. Jedoch hat die Verwendung der Short-Channel Transistoren den Nachteil, dass deren maximal zulässige Sperrspannung kleiner als die Eingangsspannung des Spannungsreglers ist. Folglich wird jeder Leistungsschalter der Halbbrücke durch eine Serienschaltung aus zwei Transistoren ersetzt. Diese Schaltungstopologie wird in der vorliegenden Arbeit um zwei Klemmschalter erweitert, deren Ansteuerung mit dedizierten Gatetreibern erfolgt. Im Gegensatz zu den bisher für integrierte Spannungsregler verwendeten Topologien lassen sich mit der nun resultierenden Topologie drei wichtige Eigenschaften zugleich erreichen: alle Schalttransistoren werden mit derselben Sperrspannung belastet, die Schaltstufe kann mit geringen Schaltverlusten betrieben werden (Zero Voltage Switching, ZVS) und der Ausgang der Schaltstufe lässt sich deaktivieren, d.h. die Ausgangsimpedanz der Schaltstufe kann auf hohe Impedanz umgeschaltet werden. Diese dritte Eigenschaft ist im Zusammenhang mit der Realisierung eines mehrphasigen Spannungsreglers wichtig, damit sich beim Betrieb bei niedriger Leistung der Wirkungsgrad durch Abschaltung einzelner Konverterphasen erhöhen lässt.

Im Rahmen der experimentellen Analyse und Verifikation von integrierten, in 14 nm CMOS Technologie hergestellten Spannungsreglern wurde als Demonstrator ein vierphasiger Tiefsetzsteller realisiert. Dieser Demonstrator besteht aus einem Chip, welcher die Schaltstufen, die Gatetreiber und die Logik zur Erzeugung der Steuersignale beinhaltet, und passiven Filterkomponenten, die auf einer Leiterplatte ausserhalb des Chip aufgelötet sind. Der Chip selbst ist mittels Bonddrähten elektrisch mit der Leiterplatte verbunden. Jede Schaltstufe der vier Konverterphasen besteht aus der vorgeschlagenen Halbbrücke mit dedizierten Gatetreibern für die Klemmschalter. Die im realisierten Demonstrator implementierte Ansteuerung der Schalttransistoren ermöglicht ausserdem die Emulation einer konventionellen Halbbrücke (ohne Klemmschalter) und der konventionellen Halbbrücke mit Klemmschaltern, d.h. ohne dedizierte Gatetreiber für die Klemmschalter. Die experimentelle Charakterisierung des Demonstrators erfolgt im Rahmen eines mehrschichtigen Analyseverfahrens, welches, unter Verwendung der Ergebnisse von Post-Layout Simulationen, thermischer Messungen der Chiptemperatur und elektrischer Messungen, die Trennung der Gesamtverluste in verschiedene Verlustanteile ermöglicht, z.B. zur Ermittlung der Verluste die im Chip und ausserhalb des Chips vorliegen. Der leiterplattenbasierte Demonstrator er-

reicht einen maximalen Wirkungsgrad von 84.1 % bei einer Ausgangsleistung von $P_{\text{out}} = 640\,\text{mW}$ und einer Schaltfrequenz von $f_{\text{s}} = 50\,\text{MHz}$. Bei einer Ausgangsleistung von $P_{\text{out}} = 890\,\text{mW}$ wird, bezogen auf die Chipfläche des Schaltungsteils welcher den Leistungstransistoren und den Gatetreibern zugeordnet ist, eine Stromdichte von 24.7 A/mm² erreicht. Hiermit werden mit dem realisierten Demonstrator eine etwa doppelt so hohe Stromdichte und ähnliche Wirkungsgradwerte erreicht wie in Veröffentlichungen zu integrierten, in 14 nm CMOS Technologie realisierten Spannungsreglern beschrieben. Die detaillierte Verlustanalyse zeigt, dass, bei einer Schaltfrequenz von 50 MHz, der Anteil der Leitverluste in den Widerständen der elektrischen Verbindungen innerhalb des Chips (Metal Layer Stack, Power Distribution Network) an den im Chip auftretenden Gesamtverlusten mindestens 25 % beträgt.

Im Zusammenhang mit der Charakterisierung des leiterplattenbasierten Spannungsreglers hat sich herausgestellt, dass die parasitären Widerstände und Induktivitäten der Verdrahtung zwischen Chip und Filterkomponenten (Bonddrähte, Leiterführung auf der Leiterplatte) die theoretisch lineare Beziehung zwischen dem eingestellten Tastverhältnis und dem tatsächlich vorliegenden Verhältnis von Ausgangsspannung zu Eingangsspannung stören. Eine deutliche Reduktion der parasitären Induktivitäten ist von einer 2.5-D All-Silicon Technologie zu erwarten. In dieser sind die passiven Komponenten des Spannungsreglers in einem zusätzlichen Substrat (Interposer) untergebracht, welches direkt mit dem Chip verbunden wird. Um mögliche Verbesserungen näher zu untersuchen, wurde daher neben dem leiterplattenbasierten Spannungsregler ein weiterer integrierter Spannungsregler auf Basis einer 2.5-D All-Silicon Technologie realisiert und experimentell charakterisiert. Den Abschluss dieser Arbeit bildet eine Erläuterung zukünftiger wissenschaftlicher Herausforderungen die sich im Bereich chip-integrierter Spannungsregler stellen, mit Fokus auf den Entwurf und das Packaging von Spannungsreglern.

Abbreviations

AC	Alternating Current
ANPC	Active Neutral Point Clamping
BEOL	Back End Of Line
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DVFS	Dynamic Voltage and Frequency Scaling
FEOL	Front End Of Line
HB	Half-Bridge
HBST	Half-Bridge with Stacked Transistors
HPC	High Performance Computing
HTSC	High Temperature Silicon Capacitors
ICT	Information and Communication Technology
IC	Integrated Circuit
ICS	Independent Clamping Switches
IVR	Integrated Voltage Regulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MIM	Metal Insulator Metal
MIPS	Million Instructions Per Second
MFlops	Million Floating point operations per second
MOS	Metal Oxide Semiconductor
MPU	Microprocessor Unit
NMOS	N-Channel Metal Oxide Semiconductor
PCB	Printed Circuit Board
PDN	Power Distribution Network
PMIC	Power Management IC
PMOS	P-Channel Metal Oxide Semiconductor
PoL	Point-of-Load
PWM	Pulse Width Modulation
SCC	Switched Capacitor Converter
TSV	Through Silicon Via
VR	Voltage Regulator
VD	Voltage Domain
WP	Working Package
ZVS	Zero Voltage Switching

Contents

1 Introduction

New Information and Communications Technology (ICT) applications such as cloud computing in data-centers, Internet of Things, mobile communication (5G), automotive, and Artificial Intelligence drive the needs for increased data processing capabilities of modern microprocessors, which, today, operate at clock frequencies up to 5 GHz [1] and have tens of cores in their more advanced versions [1–3]. However, this performance increase of microprocessors comes at the cost of increased power consumption, which can exceed 150 W per device [4] and is accompanied by high supply currents reaching values close to 100 A considering a typical package voltage of 1.8 V [5]. The increased energy demand of microprocessors and their wide range of applications lead to a large electricity consumption by ICT. Widely cited studies [6, 7] predict that the energy consumption of ICT grows exponentially, from a share of 11 % of the global electricity usage in 2015 to a share of 21 % by 2030, as shown in Fig. 1.1.

The performance of microprocessors has been achieved mainly by scaling down the transistors' sizes to increase the number of transistors per chip unit, causing the transistors to consume lower power and allowing operation at higher speed [9]. Fig. 1.2(a) shows the scaling of the number of transistors, chip clock speed, and power density as a function of time. Over the last 55 years the number of transistors per chip unit has been doubling every two years as announced by Moore in [9] and, from 1980 up to approximately the year 2004, transistors' clock frequency could be increased while the chip power density could be retained within a certain range, by applying the Dennard [10] scaling rules in planar CMOS transistors. However, the transistor sizes became so small that quantum effects such as tunneling started to manifest. Leakage losses, that were before negligible, started to become significant and the chip power density achieved its peak due to thermal limitations.

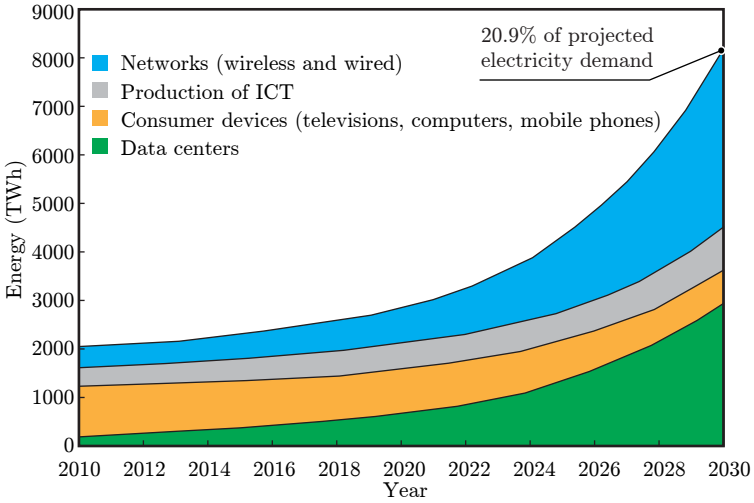


Fig. 1.1: Forecast of electricity demand of ICT over the years. The share of electricity demand by ICT is expected to grow exponentially from 2020 and reach 21% of the total energy consumption by 2030 [6–8]. Figure is reproduced from [8].

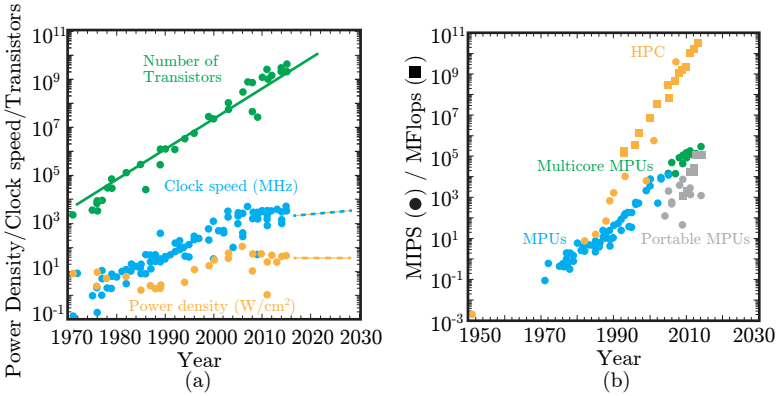


Fig. 1.2: (a) The scaling of the number of transistors, chip clock speed and power density as a function of time. (b) The performance of Microprocessor Units (MPUs) for computers, portable devices, and high-performance computing system as a function of time. The circles are data for Million Instructions Per Second (MIPS), while the squares are Million Floating point operations per second (MFlops); HPC refers to MPUs designed for High Performance Computing. Figure is reproduced from [7].

Despite the thermal limits reached in high power density designs, the data processing performance of the processors continued growing as seen in Fig. 1.2(b). To overcome the thermal limitations and keep the computational performance and transistor count growing in a sustainable manner, new techniques that go beyond the scaling law of Moore have been proposed by scientists and engineers. These technological changes, known as "More than Moore", include developments of transistor technologies, computational architectures, power management techniques, and chip packaging. Modern microprocessor systems feature today [11]:

- Nanometer scale 3-D transistor technology,
- Multiple cores,
- Multiple voltage domains per core,
- Dynamic voltage and frequency scaling,
- Advanced 3-D/2.5-D packaging.

Point-of-Load (PoL) converters play a very important role in the implementation of "More than Moore" concepts in modern microprocessor systems. Fig. 1.3 depicts an example structure of a datacenter supply chain with PoL buck converters which convert a DC voltage of 12 V to several low voltage domains that serve as input voltages for microprocessor chips in a computer board. These power converters implement the last voltage conversion close to the microprocessor and, therefore, are required to feature high efficiency, high power density, and a very fast dynamic response to effectively counteract any deviations of the microprocessors' input voltages in case of changes of the supply current demands of the microprocessors [11].

Furthermore, the concepts of independent Voltage Domains (VDs) for different cores or parts of the core and Dynamic Voltage and Frequency Scaling (DVFS) are effective countermeasures to reduce the power demands of microprocessors, since each core can be separately operated according to its workload [11]. This is achieved with a granular power delivery system that uses several independent Integrated Voltage Regulators (IVRs) for the different VDs, cf. Fig. 1.4. In that context, this thesis intends to contribute to the advances of IVRs, as part of PoL converters, by proposing, designing, and implementing a novel power stage circuit for an IVR suitable for modern microprocessor systems.

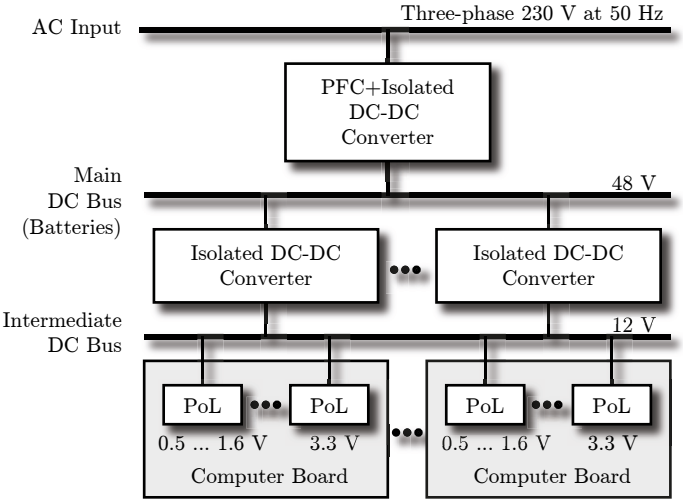


Fig. 1.3: Datacenter supply chain with PoL converters providing power to microprocessor chips.

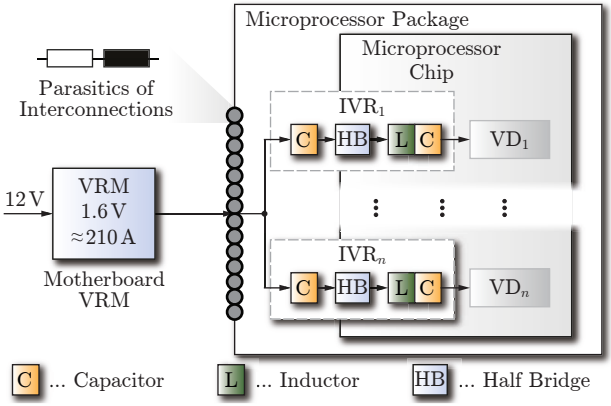


Fig. 1.4: Granular power delivery of a modern microprocessor system, where a single external voltage regulator provides power to multiple IVRs.

1.1 The CarrICool Project

This thesis was developed within a larger scope European Union project named CarrICool (FP7-ICT-619488). This project proposed the development and demonstration of a novel modular silicon interposer with integrated More-than-Moore elements for optical signaling, heat removal, and power delivery, providing a scalable solution for future 3-D on-chip and on-package systems. The proposed modular approach using a multi-functional silicon interposer is shown in Fig. 1.5(a). The interposer is built using a low-cost back-end chip technology and integrates fluid cavities for double-sided chip cooling, passive power components for IVRs, and alignment features for silicon photonics. The additional active components, used for managing the power and the data transferred to the microprocessor units and the memories, are located in an intermediate I/O layer of a CMOS chip bonded to the interposer. The final demonstrator of the CarrICool project serves as a building block of volumetric and scalable microprocessor systems. In future systems using 3-D chip stack, the proposed low-cost multi-functional silicon interposer efficiently enables the transfer of data and electrical power between the chip layer stacks while providing suitable liquid cooling infrastructure, cf. Fig. 1.5(b).

The activities of the CarrICool project were divided into five technical Working Packages (WPs). Individual demonstrators were assembled in each of the WPs which should have been combined in a single system at the end of the project. However, due to the several processing steps of the silicon wafers implemented by different partners and some fabrication problems, the final demonstrator could not be assembled in time. The work presented in this thesis was realized within the WP focused on developing power delivery circuits suitable for 2.5-D and 3-D microprocessor systems.

The demonstrator of the power delivery WP was initially planned to be composed by a chip assembled using the most advanced CMOS technology node existing at the time, and a customized silicon interposer containing the passive devices used in the IVR. The interposer should have integrated 3-D silicon inductors with magnetic core and 3-D deep-trench capacitors in a single chip, potentially increasing the IVR efficiencies and power density compared to the state-of-the-art. Due to errors during the fabrication process and handling of the silicon wafers by different partners, cf. Fig. 1.6, the initial goal of the power delivery WP of building an all-silicon demonstrator with 3-D inductors with magnetic core could not be achieved. At the end of the project, two demonstrators were still successfully assembled and tested and are discussed in the course of this thesis.

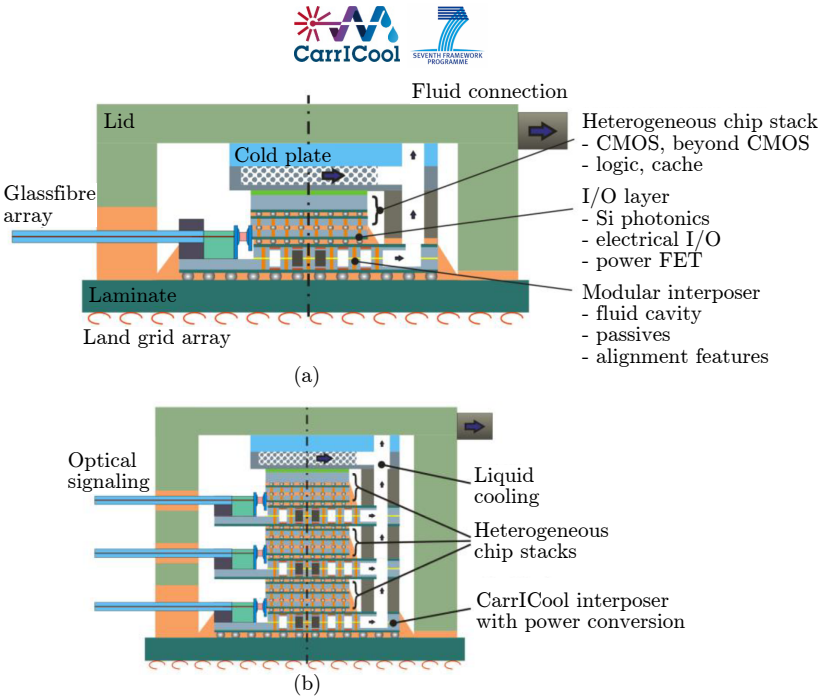
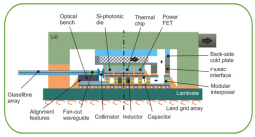


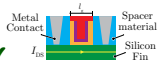
Fig. 1.5: (a) Cross-section of the planned final CarrICool demonstrator which integrates More-than-Moore elements, i.e. fluid cavities, passive power components, and silicon photonic features, in a silicon interposer platform. (b) The CarrICool demonstrator used as a building block of a volumetric microprocessor system providing scalable optical signaling, power delivery, and cooling infrastructures.



Initial Goal
- Single interposer containing cooling, optics and power delivery infrastructures

Selection of the PMIC technology and inductor topologies
- 14 nm Bulk of GlobalFoundries
- Helical and toroidal 3-D silicon inductors

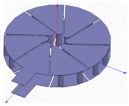
IBM 32 nm SOI
IBM 14 nm SOI
GF 14 nm Bulk ✓



System overall optimization and design of 3D-silicon inductors

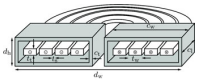
Design and tapeout of open-loop PMIC

PMIC 1 – Open loop



Failure on 3D inductors fabrication caused by project partner
- Highly resistive TSVs
- Failure on winding forming and core deposition

Selection of new inductor topologies
- Racetrack inductors
- Spiral air-core inductors



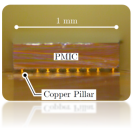
PMIC 2 – Analog control
PMIC 3 – Digital control
PMIC 4 – Dig. Con. + curr. balance
PMIC 5 – Internal osciloscope

Design and tapeout of closed-loop PMICs

Fabrication of the interposer
- Deep-trench capacitors
- Air-core inductors
- Area for placement of racetrack inductors

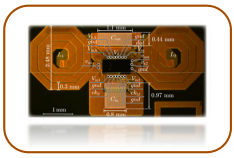
Failure on fabrication of racetrack inductors caused by project partner
- Too high parasitic resistance of inductors
- Low coupling factors

Failure on packaging process caused by project partner
- Wrong wafers used for packaging



Successful characterization of PMICs 1 and 2 in open loop
- PCB-based IVR
- Interposer-based IVR

Assembly of PCB- and interposer-based IVRs for PMIC characterization at IBM



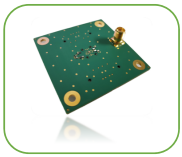


Fig. 1.6: Timeline of activities performed in the power delivery WP.

1.2 State-of-the-Art of Integrated Voltage Regulators

Literature reveals numerous different realizations of IVRs, ranging from on-package implementations to fully chip-integrated solutions. In case of on-package implementations, a common package accommodates all components of the IVRs and the microprocessor, however, the IVRs do not reside in the microprocessor die itself (off-die), cf. Fig. 1.7(a) [12]. On-package IVRs allow for reduced parasitics of the supply lines (resistances, lead inductances), as compared to conventional (off-package) VRs, however, they are still too large to be suitable for microprocessor applications that require very thin cases and tens of VDs, e.g., mobile phones, laptop computers, and tablets. By contrast, in case of fully chip-integrated (on-die) IVRs, all components reside on the microprocessor die, as shown in Fig. 1.7(b). Fully integrated IVRs realize very low parasitics of the supply lines and enable a reduction of the number of supply connections between the package and the microprocessor die, due to the reduced total input current. However, these benefits come at the cost of substantial chip area being sacrificed for the IVRs' components [13,14] and / or a highly challenging realization of chip-integrated inductors, e.g., due to the need of complex Through Silicon Vias (TSVs) [15] and additional Back End Of Line (BEOL) post-processing steps [14]. In addition, the chip technology node used for the microprocessor defines stringent design constraints, which considerably limit the flexibility of the converter design.

In an alternative approach, denoted as hybrid IVRs in this thesis, only the active switching stages of the IVRs and necessary parts of the DC capacitors reside on-die and the remaining passive components, in particular the inductors in case of buck-type solutions, are located in the package or in a lower-cost second chip (silicon interposer), as shown in Figs. 1.7(c) and (d). Hybrid IVRs can operate at very high switching frequencies of more than 100 MHz, due to the low switching losses of the microprocessor's transistors, and benefit from increased flexibilities for designing the passive components that reside in the package [16–18] or on the silicon interposer [19–22]. Compared to fully chip-integrated IVRs, hybrid solutions feature a reduction of the occupied microprocessor chip area and / or the use of less challenging connections between on-die and off-die components, at the cost of an increased number of connections to and from the microprocessor die. For both, package-based and interposer-based hybrid IVRs, high inductor and chip current densities, e.g., 3.2 A/mm^2 and 10.8 A/mm^2 respectively in [21], and efficiencies around 90 % have been reported [16,19].

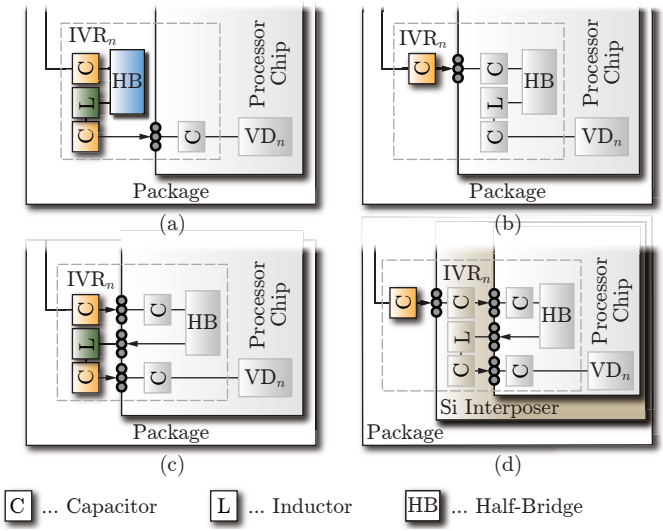


Fig. 1.7: Packaging solutions of IVRs providing granular power delivery in modern microprocessors. (a) Fully on-package IVR [12]; (b) fully on-die IVR [13–15]; (c) and (d) hybrid IVRs where the half-bridges are on the microprocessor die and the main passive components (inductors and capacitors) integrated into the package [16–18] or the silicon interposer [19–21].

1.2.1 Topologies of IVRs

Common topologies for IVRs are Switched Capacitor Converters (SCCs) [23] and buck converters with output inductors. Numerous examples of SCCs are documented in the literature, e.g., a standalone SCC topology with regulated output voltage (using pulse frequency modulation) [24], a SCC with a low dropout regulator in parallel to achieve low output voltage ripple [25], and a hybrid DC–DC converter, which comprises a 2:1 SCC and a 0.8 nH output inductor to achieve soft switching in order to increase the efficiency of the SCC [26]. The absence of inductors renders SCC topologies attractive with regard to chip integration, to avoid the challenges related to magnetic components (losses and required footprint area [18], the integration of magnetic materials [14], and, depending on the realization, the need for TSVs [15]). However, the topologies of SCCs are subject to a predefined voltage conversion ratio and generate increased losses when operated with input-to-output voltage ratios that deviate from the predefined ratio (for example, this can be observed in Figure 6 in [24], which depicts efficiency curves for an input voltage of 5 V and output voltages ranging from 3.2 V down to 2.6 V). Accordingly, inductor-type buck converters are often preferred if the ratio of input-to-output voltage is variable. Documented realizations include multi-phase buck converters with on-die inductors with a magnetic core [15], on-package air core inductors [16], and discrete inductors [27]. In addition, numerous improvements have been presented in the literature, e.g., the use of discontinuous conduction mode [17] and the implementation of a small SCC that is connected in parallel to the output of the buck converter [28], to achieve increased efficiencies under medium- and light-load conditions, respectively.

Since SCCs have been analyzed in detail in a previous PhD thesis at the Power Electronic Systems Laboratory of ETH Zurich [23], it has been decided to focus on a buck converter, which employs a switching stage realized in 14 nm CMOS technology, in this work.

1.2.2 Design and Evaluation of the IVR

All realizations of IVRs have in common that the converter design is not straightforward, since technically reasonable realizations are feasible within relatively wide ranges of values for different design variables, e.g., switching frequency and inductor current ripple in case of a buck converter. However, the values chosen for the design variables have an impact on the finally achieved efficiency. Accordingly, a systematic converter design approach,

using model-based optimization, is commonly conducted [29]. In this regard, a continuous verification and refinement as well as the identification of eventually present deficiencies of the used models is important, in particular in case of emerging technologies, to gain a better understanding of the technology and to improve the accuracies of subsequent optimizations. According to a literature research, most related work focuses on electrical or thermal characterizations of selected on-package and chip-integrated components. With regard to electrical characterization, references [18, 30–32], for example, present measured impedance characteristics of on-package conventional and coupled inductors, without and with magnetic core, or examine parasitic resistances and capacitances of key components in Through Silicon Interposers, i.e., metal layers for BEOL interconnects, TSVs, redistribution layer, and micro-bumps. In case of thermal characterizations, related publications typically focus on the identification of peak chip temperatures to avoid difficulties with overheating, e.g., observations of chip temperatures under different load conditions [33, 34] and thermal characterization of a microprocessor to derive guidelines for on-line thermal management [35, 36]. Only few publications discuss complete models of IVRs and provide experimental results for verification, e.g., [21, 37] for the realization of a buck-type IVR realized in 45 nm CMOS technology.

1.3 Aims and Contributions

The main goal of this thesis is to realize and experimentally characterize hybrid and multi-phase inductor-based IVRs based on latest 14 nm CMOS technology for a modern microprocessor application, which achieve a reliable operation with high efficiency in a wide range of switching frequencies (50 MHz to 150 MHz) and output voltages (0.8 V to 1.2 V).

1.3.1 Scientific Contributions

- A novel 2-level Half-Bridge (HB) topology suitable for CMOS technology is proposed and its efficiency performance is compared to other conventional HBs by means of Cadence® simulations. An energy-based numerical loss model is presented for the transistors of the HB by processing their voltage and current waveforms. The calculated transistor losses can be used for the converter design and the generation of a converter loss breakdown. The proposed HB topology is proven to be

suitable for high frequency multi-phase IVRs and is more reliable and slightly more efficient than the conventional solutions.

- Experimental verification of the proposed 2-level HB topology using a versatile four-phase hybrid buck IVR that employs discrete inductors and capacitors. The demonstrator achieves an efficiency of 84.1 % at an output power of $P_{\text{out}} = 640\,\text{mW}$ and a switching frequency of $f_s = 50\,\text{MHz}$. At $P_{\text{out}} = 890\,\text{mW}$, a chip current density [1] of $24.7\,\text{A/mm}^2$ is measured. The Power Management IC (PMIC), i.e., the active part of the IVR (power stage, gate drivers, PWM unit, dead time unit), is designed to be capable to emulating the switching behavior of the conventional HB topologies and the proposed topology. This allows for a direct experimental comparison of the different HB topologies with the same IVR.

- A novel methodology is proposed for the characterization of the chip. It is based on post-layout simulations, thermal inspections of the chip temperature, and electrical measurements and allows for the separation of the on-chip losses and off-chip losses. Furthermore, the method enables the separation of the DC losses and the AC losses of the PMIC chip.

- A hybrid 2.5D all-silicon demonstrator is designed, assembled, and experimentally characterized. The 2.5-D all silicon package reduces the parasitic inductances and capacitances of the package assembly, and, therefore, the IVR maintains a linear dependency of the output voltage on the duty-cycle at high switching frequencies and high output currents.

1.3.2 IVR Demonstrator Systems

Tab. 3.1 lists the specifications of the implemented IVR demonstrators which are intended to power the main voltage domain of a typical IBM ® microprocessor. Due to limited available chip area, the output power is scaled down. The input voltage of 1.6 V corresponds to twice the nominal voltage of a single short channel device of the 14 nm CMOS technology. The output voltage range, $0.8\,\text{V} \leq V_{\text{out}} \leq 1.2\,\text{V}$, is important for the implementation of DVFS. The IVR is supposed to operate with inductors of different values.

[1] Chip current density is defined in this work as $\rho_A = I_{\text{out,max}}/A_c$, where $I_{\text{out,max}}$ is the maximum output current of the chip and A_c is the total chip area used to implement the power switches and gate drivers.

Tab. 1.1: Specifications of the investigated four-phase IVR.

Parameters	Symbol	Value
Input voltage	V_{in}	1.6 V
Output voltage range	V_{out}	0.8 V to 1.2 V
Output power	P_{out}	800 mW
Min. output voltage	$V_{\text{out,min}}$	0.6 V

Therefore, the HB circuits are designed to operate reliably in a wide range of switching frequencies varying from 50 MHz to 150 MHz. Two demonstrators are designed and tested using the same PMIC containing the power HBs:

- A four-phase inductor-based buck converter with discrete inductors and capacitors soldered on a PCB carrier. The hardware and characterization details are shown in Chapter 3.

- A two-phase inductor-based buck converter with inductors and capacitors embedded in a silicon interposer. The experimental system and the obtained results are summarized in Chapter 4.

1.3.3 Performance Comparison and Benchmark

Tab. 1.2 shows the comparison of the implemented PCB-based IVR in terms of achievable efficiencies and chip current density with IVRs using an advanced 14 nm CMOS technology node. The comparison shows that the presented IVR achieves a similar peak efficiency compared to the state-of-the-art, which is related to the high resistance of the Power Distribution Network (PDN) in the advanced technology nodes that cause a significant amount of losses, as detailed in Chapter 3. For this reason, IVRs realized in more mature technology nodes, e.g., 32 nm, can achieve higher efficiencies than IVRs realized with more recent CMOS technology nodes. The achieved peak current density is, however, two times higher than the reported peak current density for state-of-the-art realizations.

Tab. 1.2: Performance and design values of the presented IVR compared to previously presented converters in 14 nm CMOS technology.

	This work	C. Schaef et al. [17]	H. K. Krishna-murty et al. [14]	H. K. Krishna-murty et al. [15]
Techn. node PMIC (nm)	**14**	14	14	14
Peak efficiency (%)	**84.1**	88	84 (on-die induct.)	80
Max. curr. density (A/mm^2)*	**24.7**	10.7	–	–
Input voltage (V)	**1.6**	1.6	1.5	1.3
Conv. ratio M at peak efficiency	**0.7**	0.75	0.77	0.77
HB topology	**ANPC**	HBST	HBST	HBST
Switching frequency (MHz)	**50**	70	100	90
Inductor value L (nH)	**36**	2.5	1.5 or 22**	4.8
Inductor technology	**discrete**	on-package	on-die or ext.	on-die
Inductor packaging	**bond-wire**	flip-chip	– / on-probe	–
Number of phases	**up to 4**	1	2	2

* Defined as the maximum output current of the IVR divided by the area of the enabled power switches, gate-drivers, and level shifters. This value was calculated using information found in the corresponding publications.
** Two realizations are presented, with on-die and external inductor.

1.4 List of Publications

Key results presented in this thesis have been published in international scientific journals and conference proceedings and have been presented at workshops. The publications created as part of this thesis, or also in the scope of other related projects, are listed below.

1.4.1 Journal Papers

- **P. A. M. Bezerra**, F. Krismer, J. W. Kolar, R. K. Aljameh, S. Paredes, R. Heller, T. Brunschwiler, P. A. Francese, T. Morf, M. A. Kossel, and M. Braendli, "Electrical and Thermal Characterization of an Inductor-Based ANPC-Type Buck Converter in 14 nm CMOS Technology for Microprocessor Applications," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 456-468, 2020. DOI: 10.1109/OJPEL.2020.3025658.

- **P. A. M. Bezerra**, F. Krismer, J. W. Kolar, R. K. Aljameh, S. Paredes, R. Heller, T. Brunschwiler, P. A. Francese, T. Morf, M. A. Kossel, and M. Braendli, "Experimental Efficiency Evaluation of Stacked Transistor Half-Bridge Topologies in 14 nm CMOS Technology," *Electronics*, vol. 10, no. 10, p. 1150, 2021. DOI: 10.3390/electronics10101150.

1.4.2 Conference Papers

- **P. A. M. Bezerra**, R. K. Aljameh, F. Krismer, J. W. Kolar, A. Sridhar, T. Brunschwiler, and T. Toifl, "Analysis and Comparative Evaluation of Stacked-Transistor Half-Bridge Topologies Implemented with 14 nm Bulk CMOS Technology," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, USA, July 2017. DOI: 10.1109/COMPEL.2017.8013307.

- **P. A. M. Bezerra**, F. Krismer, T. M. Andersen, J. W. Kolar, A. Sridhar, T. Brunschwiler, T. Toifl, M. Jatlaoui, F. Voiron, Z. Pavlovic, N. Wang, N. Cordero, C. Rabot, and C. O' Mathuna, "Modeling and Multi-Objective Optimization of 2.5D Inductor-Based Fully Integrated Voltage Regulators for Microprocessor Applications," in *Proc. of the IEEE Brazilian Power Electronics Conference / Southern Power Electronics Conference (COBEP/SPEC)*, Fortaleza, Brazil, November 2015. DOI: 10.1109/COBEP.2015.7420168.

- **P. A. M. Bezerra**, F. Krismer, R. M. Burkart, and J. W. Kolar, "Bidirectional Isolated Non-Resonant DAB DC–DC Converter for Ultra-Wide Input Voltage Range Applications," in *Proc. of the IEEE Power Electronics and Application Conference and Exposition (PEAC)*, Shanghai, China, November 2014. DOI: 10.1109/PEAC.2014.7038003.

1.4.3 Workshops and Seminars

- **P. A. M. Bezerra**, F. Krismer, and J. W. Kolar, "Towards the Integration of Voltage Regulators in Server Applications," presented at the *International Power Supply on Chip Workshop (PwrSoC)*, Hsinchu, Taiwan, October 2018. DOI: not available.

- **P. A. M. Bezerra**, T. Andersen, F. Krismer, and J. W. Kolar, "Multi-Objective Optimization of Fully Integrated Voltage Regulators: Switched Capacitor and Inductor-Based Converters," presented at the *ECPE PowerSoC Workshop "µPE: Powering Low-Power Systems"*, Munich, Germany, June 2015. DOI: not available.

1.4.4 Further Scientific Contributions

- T. Brunschwiler, G. Schlottig, A. Sridhar, **P. A. M. Bezerra**, P. Ruch, N. Ebejer, H. Oppermann, J. Kleff, W. Steller, M. Jatlaoui, F. Voiron, Z. Pavlovic, P. McCloskey, D. Bremner, P. Parida, F. Krismer, J. W. Kolar, and B. Michel, "Towards Cube-Sized Compute Nodes: Advanced Packaging Concepts Enabling Extreme 3D Integration," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, San Francisco, USA, December 2017. DOI: 10.1109/IEDM.2017.8268322.

- T. Brunschwiler, G. Schlottig, A. Sridhar, A. La Porta, O. Ozsun, J. Zürcher, R. Strässle, L. Del Carro, and **P. A. M. Bezerra**, "Scalable Packaging Platform Supporting High-Performance 3D Chip Stacks," in *Proc. of the IEEE Pan Pacific Microelectronics Symposium (Pan Pacific)*, Kauai, USA, February 2017. DOI: not available.

- R. K. Aljameh, **P. A. M. Bezerra**, F. Krismer, J. W. Kolar, A. Sridhar, T. Brunschwiler, T. Toifl, and B. Michel, "Control and Implementation Aspects of a Multiphase Inductor-Based FIVR in 14 nm Bulk CMOS for Microprocessor Applications," presented at the *International Power Supply on Chip Workshop (PwrSoC)*, Madrid, Spain, October 2016. DOI: not available.

- T. Andersen, **P. A. M. Bezerra**, F. Krismer, J. W. Kolar, A. Sridhar, T. Brunschwiler, T. Toifl, C. Rabot, Z. Pavlovic, C. O'Mathuna, S. Gaborieau, and C. Bunel, "CarrICool: Interposer Supporting Optical Signaling, Liquid Cooling, and Power Conversion for 3D Chip Stacks," presented at the *International Power Supply on Chip Workshop (PwrSoC)*, Boston, USA, October 2014. DOI: not available.

1.5 Thesis Outline

According to the goals and contributions mentioned above, the thesis is divided into two main chapters and conclusions.

- **Chapter 2** proposes a modified CMOS Active Neutral Point Clamped (ANPC) HB with independent Clamping Switches (ICS) built using FinFET 14 nm CMOS technology, which allows for soft switching of the main switches, features voltage balancing among the devices, and provides phase-shedding capability. This chapter presents a comparison of the proposed HB in terms of the achievable efficiencies and the resulting loss components by means of Cadence® simulations and inspections of the switching waveforms. This chapter is based on [29, 38, 39].

- **Chapter 3** presents a comprehensive characterization of a versatile four-phase PCB-based inductor-based IVR whose active part (HBs, gate drivers, gate signal generation units) is implemented in 14 nm CMOS technology. The embedded gate signal generator unit is able to emulate the switching behavior of the conventional HBs with stacked transistors. This allows to compare the proposed HB to the conventional HBs in the same demonstrator. The characterization of the IVR is based on post-layout simulations, electrical measurements, and thermal inspections of the chip surface. This chapter is based on [27, 39].

- **Chapter 4** summarizes the main conclusions of the previous chapters and presents an outlook on future research in integrated voltage regulators. This chapter also contains the results of different 2.5-D all-silicon IVRs developed in the course of this work.

2

CMOS Half-Bridge Topologies with Stacked Transistors

Chapter Abstract

This chapter evaluates three different topologies of CMOS half-bridge converters with respect to efficiency, implementation effort, suitability for on-chip integration, and multi-phase applications: the conventional half-bridge converter, the half-bridge converter with conventional Active Neutral Point Clamping (ANPC), and a proposed half-bridge converter with a modified circuit to achieve ANPC. The converters employ stacked transistors to allow for the use of advanced low voltage devices with superior switching performance compared to the higher voltage long-channel devices. In-depth analysis of the transient processes during switching for all three converters, based on Cadence® simulations, reveal that both half-bridge converters with ANPC achieve proper balancing of the blocking voltages of the main transistors and are capable to attain similar efficiencies of 90.5 % at an output power of 200 mW, input and output voltages of 1.6 V and 0.8 V, respectively, and a switching frequency of 150 MHz, which is 0.9 % higher than the one attained with the conventional half-bridge converter. Of the two ANPC half-bridge converters, the proposed topology allows to completely turn off its entire power stage or parts of it, its efficiency is found to be less sensitive to variations of dead time, and it achieves the peak efficiency at relatively higher dead time values. These qualities render the proposed topology particularly suitable for multi-phase systems and low load operation. The main contents of this chapter have been also presented in [29, 38].

The active parts of the IVR's power stage are normally implemented using complementary transistors and can be composed of high voltage long-channel devices or of stacked short-channel devices (cf. Fig. 2.1(a)). Compared to the realizations with long-channel devices, the stacked configuration allows the

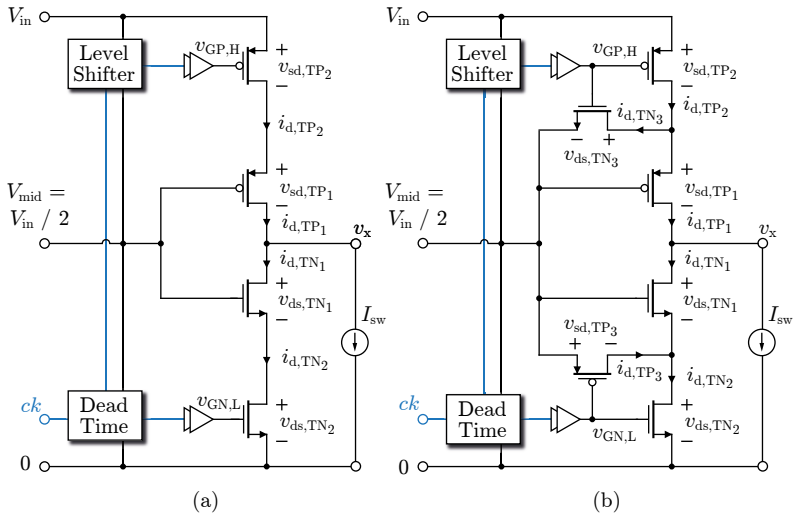


Fig. 2.1: Schematic representations of two-level HB power stages of IVRs in stacked configurations, including the dead time controller and level shifters. (a) CMOS Half-bridge with Stacked Transistors (CMOS HBST); (b) CMOS Active Neutral Point Clamped HBST (CMOS ANPC HBST).

use of the low voltage transistors of the technology node that features a better Figure of Merit FOM ($Q_g \cdot R_{ds,on}$) [19]. Moreover, the charge recycling mechanism, explained in [40], reduces the gate drive losses, which is beneficial with regard to high conversion efficiency at high switching frequencies.

To reduce high currents flowing from the motherboard to the microprocessor's package, it is desirable to use the highest input voltage possible that does not violate the maximum transistor's threshold voltage and to ensure equal voltage distribution among the series-connected devices. The two-level Half-Bridge with Stacked Transistors (HBST) configuration of Fig. 2.1(a) [40–42] has been employed successfully in many of Intel's IVRs using FinFET 22 nm technology [13, 16]. Recently, Intel also proposed a fully integrated voltage regulator with power transistors, decoupling capacitors, and inductors in the same die [43] using the HBST of Fig. 2.1(a), but using 14 nm technology. This configuration, however, does not assure equal voltage distribution among the devices and voltage spikes might occur during and after the switching transient [29], which reduces system reliability, efficiency, and lifetime. To

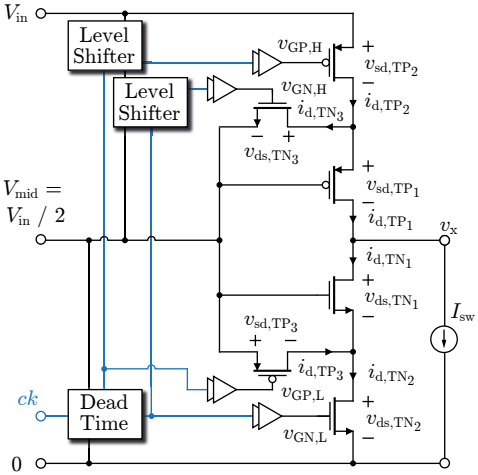


Fig. 2.2: Schematic representations of the CMOS ANPC HBST with Independent Clamping Switches (ICS).

avoid voltage unbalancing, clamping transistors can be added to the conventional CMOS HBST to actively clamp the potential between two stacked transistors to the middle potential [44] (cf. Fig. 2.1(b)). In this approach, denoted conventional Active Neutral Point Clamping (ANPC) HBST, common gate drivers are used for the main switches and the respective clamping switches. Therefore, the clamping switches TN_3 and TP_3 are both turned on if TP_2 and TN_2 are both turned off. In addition, TP_1 starts to conduct if its gate-drain voltage is less than $-0.3\,\mathrm{V}$ and TN_1 starts to conduct for a gate-drain voltage higher than $0.3\,\mathrm{V}$, which is found in Section 2.2 of this chapter, in the course of the investigation of the simulation results. For this reason, the output of the power stage cannot be switched to high impedance. Accordingly, phase shedding, which is used to increase part-load efficiency in multi-phase converters [45], is not possible.

This chapter proposes a modified ANPC HBST with Independent Clamping Switches (ICS) (cf. Fig. 2.2) built using FinFET CMOS technology, which allows for soft switching of the main switches and features voltage balancing among the devices and phase-shedding capability. Section 2.1 summarizes the specifications and the simulation setup used to design and evaluate the HBST topologies of Fig. 2.1 and Fig. 2.2. Since the three investigated topologies, HBST, ANPC HBST, and ANPC HBST with ICS, mainly differ with regard to

Tab. 2.1: Specifications of a single phase of the considered IVR.

Parameters	Symbol	Value
Input voltage	V_{in}	1.6 V
Output voltage range	V_{out}	0.8 V to 1.2 V
Output power	P_{out}	200 mW
Min. output voltage	$V_{\text{out,min}}$	0.6 V

their behavior during switching, the switching operations are inspected in Section 2.2 based on simulation results in order to gain a deeper understanding of the different topologies. Finally, in Section 2.3, the three HB topologies (conventional HBST, conventional ANPC HBST, and proposed ANPC HBST with ICS) are evaluated based on a comparison of losses and efficiencies computed by means of Cadence® simulations, using a 14 nm CMOS process environment (an evaluation of the three topologies based on experimental results is presented in Chapter 3). According to the simulation results, the conventional and the proposed ANPC power stages achieve similar efficiencies of 90.5 % at optimum dead times (simulated for a switching frequency of 150 MHz, an input voltage of 1.6 V, and a duty-cycle of 50%), which is 0.9 % higher than for the conventional HBST at same conditions. However, compared to the conventional ANPC HBST, the proposed ANPC HBST with ICS is better suitable for multi-phase systems and low load operation, since its entire power stage (or parts of it) can be completely turned off. In addition, it achieves an efficiency characteristic that is less sensitive to dead time variations.

2.1 Specifications and Simulated Schematics

The considered IVR is composed of a four-phase buck converter. Each phase of this buck converter employs a power stage, which is formed by slices that can be replicated in order to achieve the desired output power, to assure a symmetrical design, and to obtain a compact and scalable layout. Tab. 2.1 lists the specifications of a single phase of the considered IVR used to design the transistor's size of the HBs and Fig. 2.3 shows a complete schematic drawing of the ANPC HBST with ICS with main transistors ① and ⑤, clamping transistors ② and ⑥, multi-stage tapered gate drivers ③, ④, ⑦, ⑧, ⑨,

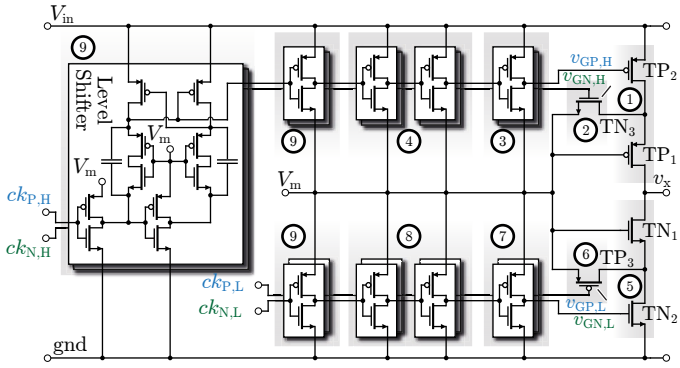


Fig. 2.3: Schematics of a designed CMOS ANPC HB with ICS including its tapered gate drivers and level shifters.

and level shifter (9). For the other simulated topologies, i.e., HBST and ANPC HBST, only the main power stage, composed by the main switches and the clamping switches, was changed.

The simulations have been conducted with the circuit simulator that is part of the Virtuoso Custom IC Design Environment by Cadence® (Version ICADV12.1) loaded with the 14 nm LPP FinFET PDK (Process Design Kit) of GlobalFoundries® [46]. The simulation results only include the parasitic resistances and capacitances of the Front-End-Of-Line (FEOL) and the first three metal layers of the the metal layer stack. Furthermore, all simulation results shown in this chapter consider equal transistors' gate widths for the main switches, $T_{w,TP_{1,2}} = T_{w,TN_{1,2}} = T_w$ ($\propto$ transistor area), and the clamping switches, $T_{w,TP_3} = T_{w,TN_3} = T_w/10$. It is to be noted that the simulations consider two-stage gate drivers, which, in case of the main switches, use transistors with gate widths of $T_{w,GDm_1} = T_w/10$ for the first stage and $T_{w,GDm_2} = T_w/50$ for the second stage. The simulated gate drivers of the clamping switches use transistors with same gate widths for first and second stages, $T_{w,GDc_{1,2}} = T_w/50$. Low voltage transistors of a 14 nm CMOS technology node realize main and clamping switches.

Fig. 2.4 depicts the investigated converter topologies with the body diodes of the power switches being included – only the transistors' parasitic capacitances have not been included for the sake of clarity. This equivalent circuit serves for explaining technology-specific details that appear in the presented switching waveforms. Two body diodes, which connect each transistor's

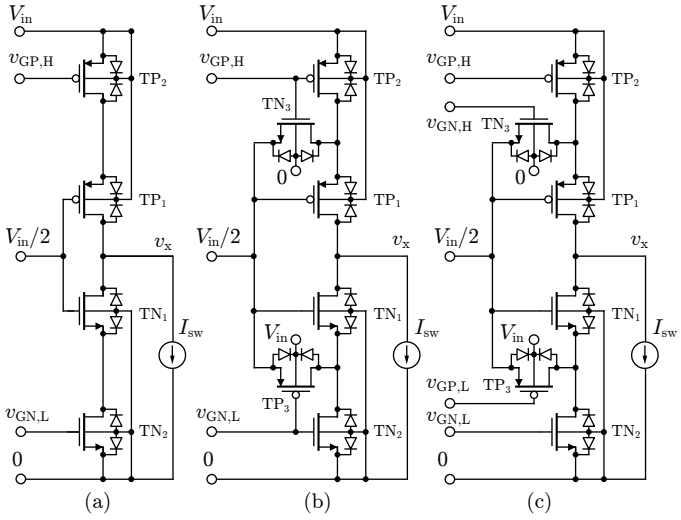


Fig. 2.4: Illustration of the converters' equivalent circuits, where two opposite series connected diodes are present in parallel to each transistor: (a) CMOS HBST, (b) CMOS ANPC HBST, and (c) CMOS ANPC HBST with ICS.

drain and source potentials to the substrate, are present for each MOSFET and the substrates of all PMOS and NMOS transistors are connected to V_{in} and 0, respectively, in order to assure that the diodes block during steady-state operation. Furthermore, all transistors are symmetric with regard to drain and source, i.e., gate-source and gate-drain voltages can control the MOSFET channel. Thus, same values for gate-source and gate-drain capacitances, $C_{gs} = C_{gd}$, apply. The drain-source capacitance, C_{ds}, is different and much less than C_{gs} and C_{gd}. For the main transistors, TP_1, TP_2, TN_1, and TN_2, equal chip areas apply. The chip area of each clamping transistor, TP_3 and TN_3, is 10% of the area of a main transistor, due to significantly lower current stresses. Thus, the clamping transistors' on-state resistances are approximately ten times higher than those of the main transistors.

2.2 Waveforms During Switching Transients

The investigated HBSTs are expected to generate substantial switching losses, due to the considered very high switching frequencies. Hence, in order

to attain in-depth understanding of the switching operations and clarify topology-dependent limitations related to switching (e.g. unbalanced blocking voltages in case of the conventional HBST, efficiency-optimal dead time values), this Section details the transient processes that take place during switching.

Fig. 2.5 presents typical gate voltages that are used to generate an output voltage, v_x, with a defined duty cycle at the switching node of the buck converter. Fig. 2.5(a) depicts the gate voltages $v_{GP,H}$ and $v_{GN,L}$ that are applied to the transistors TP_2 and TN_2, respectively. These waveforms are valid for all three topologies shown in Fig. 2.1 and Fig. 2.2. Fig. 2.5(b) shows that the same gate voltages, $v_{GP,H}$ and $v_{GN,L}$ are used respectively for the clamping switches TN_3 and TP_3 of the CMOS ANPC HBST. The ANPC HBST with ICS uses different signals than the conventional ANPC for TN_3 and TP_3 to allow for soft switching of the main switches, cf. Fig. 2.5(c). The presented gate voltages are measured with respect to the minus terminal of the power stage.[1] In the case of the CMOS HBST, solely the switching states of TP_2 and TN_2 determine the switching states of TP_1 and TN_1, respectively, e.g., if TP_2 is in the on-state and TN_2 in the off-state (with an assumed drain-source voltage of $V_{in}/2$), the gate-source voltages of TP_1 and TN_1 are equal to $-V_{in}/2$ and zero, respectively. Accordingly, TP_1 is in the on-state and TN_1 in the off-state. Fig. 2.5(d) illustrates the waveform of the voltage at the switching node, v_x, that results for the gate voltages of Fig. 2.5(a) to (c) and a positive output current, i_x, which is assumed to be constant and equal to 250 mA.

During the voltage transitions between zero and V_{in}, the actual waveform of the switched voltage depends on the topology. Furthermore, depending on the slope of the output voltage, $v_x(t)$, two entirely different switching operations are observed. For this reason, the presented explanation distinguishes between case 1 (v_x changes from V_{in} to 0) in Subsection 2.2.1 and case 2 (v_x changes from 0 to V_{in}) in Subsection 2.2.2.

2.2.1 Case 1: v_x changes from V_{in} to 0

Fig. 2.6 presents the simulated transient waveforms of all control voltages in Ⓘ, all drain-source voltages in Ⓘ to Ⓘ, the gate-source voltages of the

[1] Please note that TP_1, TP_2, and TP_3 are p-type MOSFETs; for this reason, negative gate-source voltages are needed to turn on TP_1, TP_2, and TP_3. In addition, the gate voltages of TP_2, and TN_3, $v_{GP,H}$ and $v_{GN,H}$, feature an offset of $V_{in}/2$, which is needed to keep the transistors' gate-source voltages within the permissible voltage range.

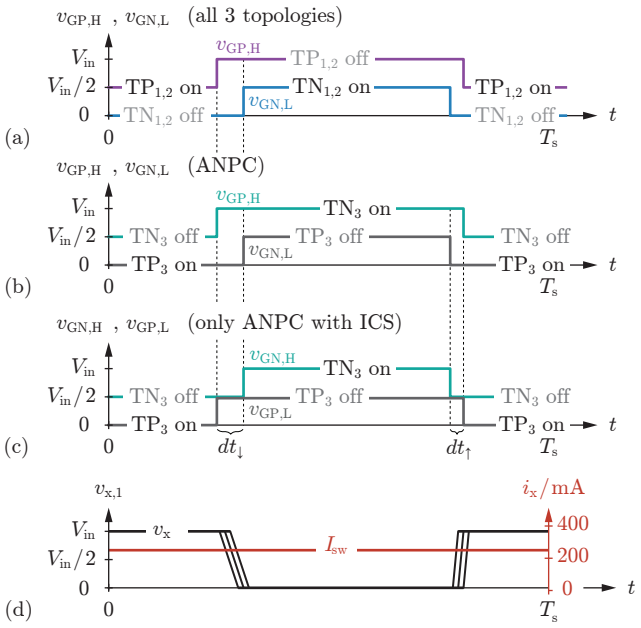


Fig. 2.5: Waveforms of the simplified gate voltages applied to the three HBST circuits, cf. Fig. 2.1 and Fig. 2.2, and for a programmed duty cycle of 50 %. (a) Gate voltages $v_{GP,H}$ and $v_{GN,L}$ that are applied to the transistors TP_2 and TN_2, respectively. These waveforms are valid for all 3 topologies of Fig. 2.1 and Fig. 2.2. (b) Gate voltages $v_{GP,H}$ and $v_{GN,L}$ of the transistors TN_3 and TP_3, respectively. These waveforms only apply to the ANPC HBST topology depicted in Fig. 2.1(b). (c) Gate voltages $v_{GN,H}$ and $v_{GP,L}$ of the transistors TN_3 and TP_3, respectively. These waveforms only apply to the ANPC HBST with ICS topology depicted in Fig. 2.2. (d) Illustration of the waveform of the switched output voltage, v_x, that results with the gate voltages of Fig. 2.5(a) to (c) and a positive output current, e.g., $i_x = 250\,\mathrm{mA}$. During the voltage transitions between zero and V_{in}, the actual waveform of the switched voltage depends on the topology.

main transistors in (V) and the instantaneous power values, i.e., the products of drain currents times corresponding drain-source voltages, in (VI).

The results for the conventional HBST are shown in Fig. 2.6(a). At the instant t_a the switch TP_2 is commanded to turn off and, after the delay time $t_1 - t_0$, the load current charges the effective output capacitances of TP_2 and TP_1 and discharges those of TN_1 and TN_2 and thus, low switching losses (ZVS) are achieved. A detailed examination of all currents during switching reveals that, because of $C_{gd} = C_{gs} \gg C_{ds}$, the drain current of TP_2 is less than the drain current of TP_1 during $t_1 < t < t_5$ and the same applies to TN_2 and TN_1, i.e., $|i_{d,TP_2}| < |i_{d,TP_1}|$ and $|i_{d,TN_2}| < |i_{d,TN_1}|$. Due to $|i_{d,TN_2}| < |i_{d,TN_1}|$, first almost only v_{ds,TN_1} decreases during $t_1 < t < t_3$ and thereafter v_{ds,TN_2} decreases to zero. However, even though $|i_{d,TP_2}| < |i_{d,TP_1}|$ applies, only v_{sd,TP_2} increases during $t_1 < t < t_2$, since TP_2 is turned off at $t = t_1$ and the gate current of TP_1, $i_{d,TP_1} - i_{d,TP_2}$, first needs to discharge the effective input capacitance of TP_1 in order to turn off TP_1 at $t = t_2$. The dead time is adjusted such that after the dead time, at $t = t_b$, v_{ds,TN_2} is close to zero and the switch TN_2 is turned on with low losses. The conventional HBST does not assure voltage balancing of the stacked transistors and $v_{sd,TP_1} \neq v_{sd,TP_2}$ occurs for $t > t_6$ in Fig. 2.6 (a) (II), which causes additional leakage losses.

In case of the conventional ANPC HBST, the waveforms shown in Fig. 2.6(b) result. At $t = t_a$ the high-side gate driver simultaneously turns off TP_2 and turns on TN_3, which forces v_{ds,TN_3} to decrease to zero during $t_1 < t < t_2$ and causes turn-on losses in TN_3. Accordingly, v_{sd,TP_2} is forced to increase to $V_{in} - V_{mid}$ and, due to $v_{gs,TP_1} = -v_{ds,TN_3}$, TP_1 is turned off. The drain source voltage of TN_2 remains at 0.8 V during this time interval since TP_3 is still in its on-state. Hence, v_{ds,TN_1} decreases and reaches zero at $t = t_2$. However, the load current continues to provide charge to the effective output capacitances of TN_1 and TP_1 during $t_2 < t < t_3$ and the voltages v_x and v_{ds,TN_1} continue to decrease. With decreasing v_x, $v_x < V_{mid}$, the gate of TN_1 being tied to V_{mid}, and TP_3 being switched on, the gate-drain voltage of TN_1 increases until the transistor is operated in its saturation region, controlled via the gate-drain voltage instead of the gate-source voltage, during the corresponding time interval, $t_3 < t < t_5$, which causes substantial losses.[2] Finally, at $t = t_b$, TN_2 and TP_3 are commanded to turn on and off respectively, and considerable turn-on losses in TN_2 are observed. The clamping switches TN_3 and TP_3, thus, enforce balanced blocking voltages of the transistors. For this, however, soft switching is sacrificed and increased switching losses result.

[2] The body diodes of TN_1 do not conduct during $t_3 < t < t_4$, due to the present wiring of the body diodes, cf. Fig. 2.4, and $v_x > 0$.

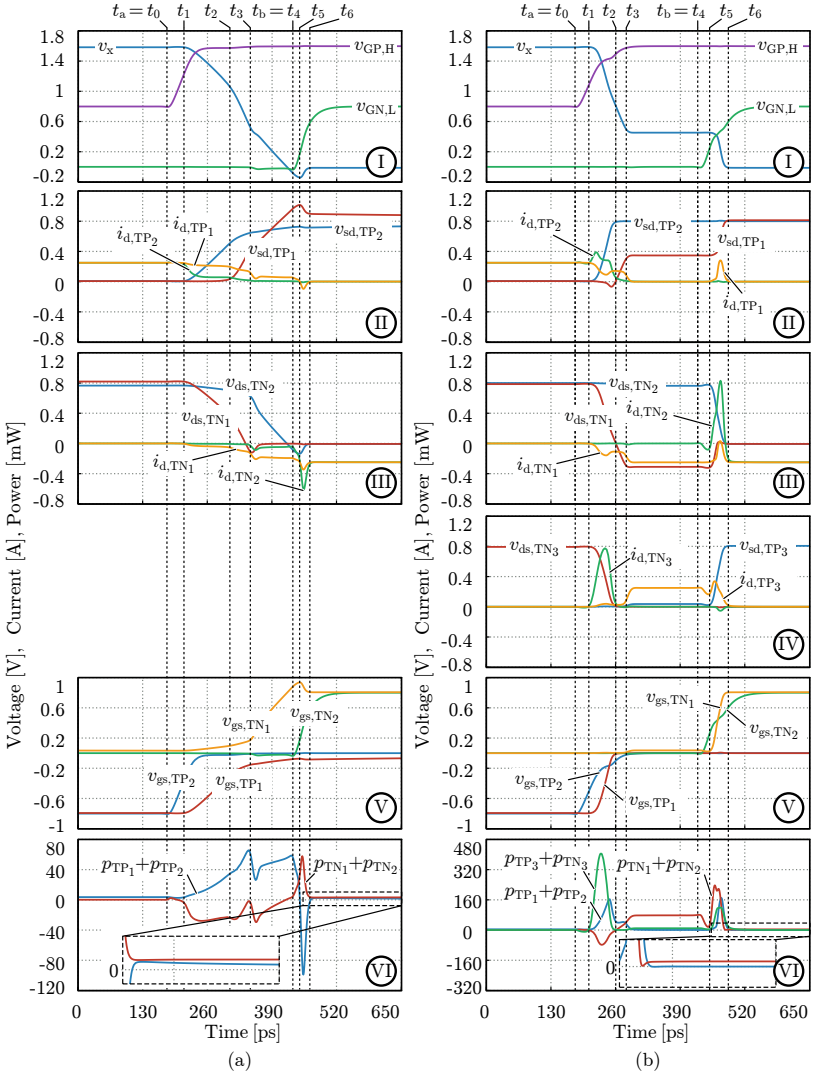


Fig. 2.6: Main waveforms, obtained from Cadence® simulations, of the conventional power stages of Fig. 2.1 during a transient change of v_x from V_{in} to 0 with positive current, I_{sw}. (a) Conventional HBST. (b) Conventional ANPC HBST. The waveforms were generated considering $V_{in} = 1.6\,V$ and $I_{sw} = 250\,mA$.

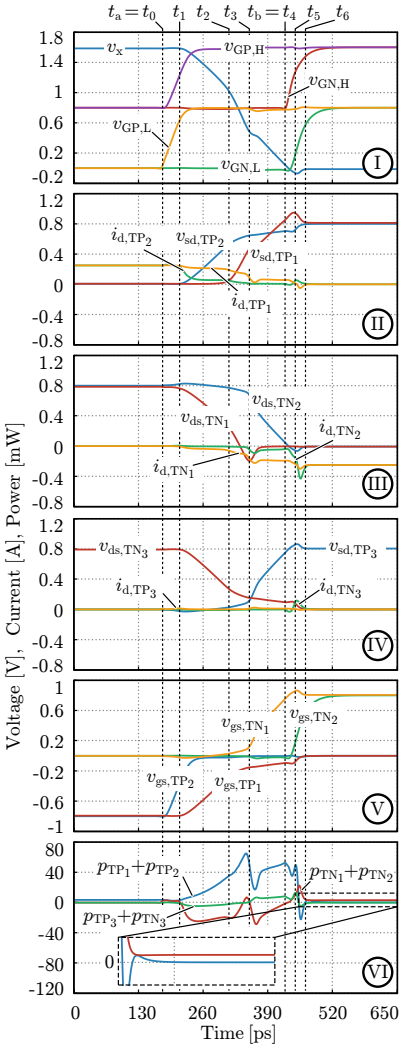


Fig. 2.7: Main waveforms, obtained from Cadence® simulations, of the ANPC with ICS of Fig. 2.2 during a transient change of v_x from V_{in} to 0 with positive current, I_{sw}. The waveforms were generated considering $V_{in} = 1.6\,V$ and $I_{sw} = 250\,mA$.

With regard to the proposed ANPC HBST with ICS both clamping switches, TN_3 and TP_3, are turned off during the dead time interval, $t_a < t < t_b$, cf. Fig. 2.7. For this reason, similar current and voltage waveforms result for the ANPC HBST with ICS and the conventional HBST. At $t = t_b$ the clamping switch TN_3 is turned on to balance the blocking voltages of TP_1 and TP_2. This concept simultaneously achieves both, low switching losses (ZVS) and balanced voltages at the transistor terminals in steady-state.

2.2.2 Case 2: v_x changes from 0 to V_{in}

Fig. 2.8 presents the simulated waveforms during a switching transient for case 2 and for the different investigated converter topologies. In case 2, TN_2 is switched off at $t = t_a$ and TP_2 is switched on at $t = t_b$.

Fig. 2.8(a) shows the waveforms simulated for the conventional HBST. The switch TN_2 turns off at t_1 when the gate-source voltage of TN_2 falls below the threshold voltage. Since TN_1 remains in the on-state, the load current provides charge to the drain-source and gate-drain capacitances of TN_2 during $t_1 < t < t_2$. Hence, v_{ds,TN_2} decreases and the gate-drain voltage of TN_2 increases until TN_2 enters the saturation region at $t = t_2$. Subsequently, during $t_2 < t < t_4$, negative drain-source voltage and negative drain current are present in TN_2. At $t = t_4$ the negative gate-source voltages of both PMOS transistors, TP_1 and TP_2, exceed the transistor's (negative) threshold voltages, which causes TP_1 and TP_2 to turn on and forces v_x to increase to V_{in} during $t_4 < t < t_5$. Very high instantaneous drain currents are present in TP_1, TP_2, and TN_1 and comparably high turn-on losses result. Furthermore, unbalanced transistor voltages v_{ds,TN_1} and v_{ds,TN_2} are observed for $t > t_5$.

The waveforms for the conventional ANPC HBST are depicted in Fig. 2.8(b). At $t = t_a$, TN_2 and TP_3 are commanded to turn off and on, respectively, which, during $t_1 < t < t_3$, causes v_{sd,TP_3} to decrease to a value close to zero and v_{ds,TN_2} to increase to V_{mid}. Furthermore, the load current provides charge to the effective output capacitances of TP_1 and TN_1, so v_{sd,TP_1} and v_{ds,TN_1} decrease during $t_2 < t < t_3$. Thus, positive gate-drain voltage is applied to TN_1, since TP_3 is switched on for $t > t_3$, and TN_1 is operated in the saturation region during $t_3 < t < t_5$ with the drain current being equal to the load current. During the subsequent time interval, $t_5 < t < t_6$, the transistors TP_1 and TP_2 are turned on, which forces their drain-source voltages to decrease to zero. At the same time TN_3 is turned off and v_{ds,TN_3} increases to V_{mid}. In comparison to the conventional HBST lower instantaneous losses are simulated, cf. Fig. 2.8(b) (VI).

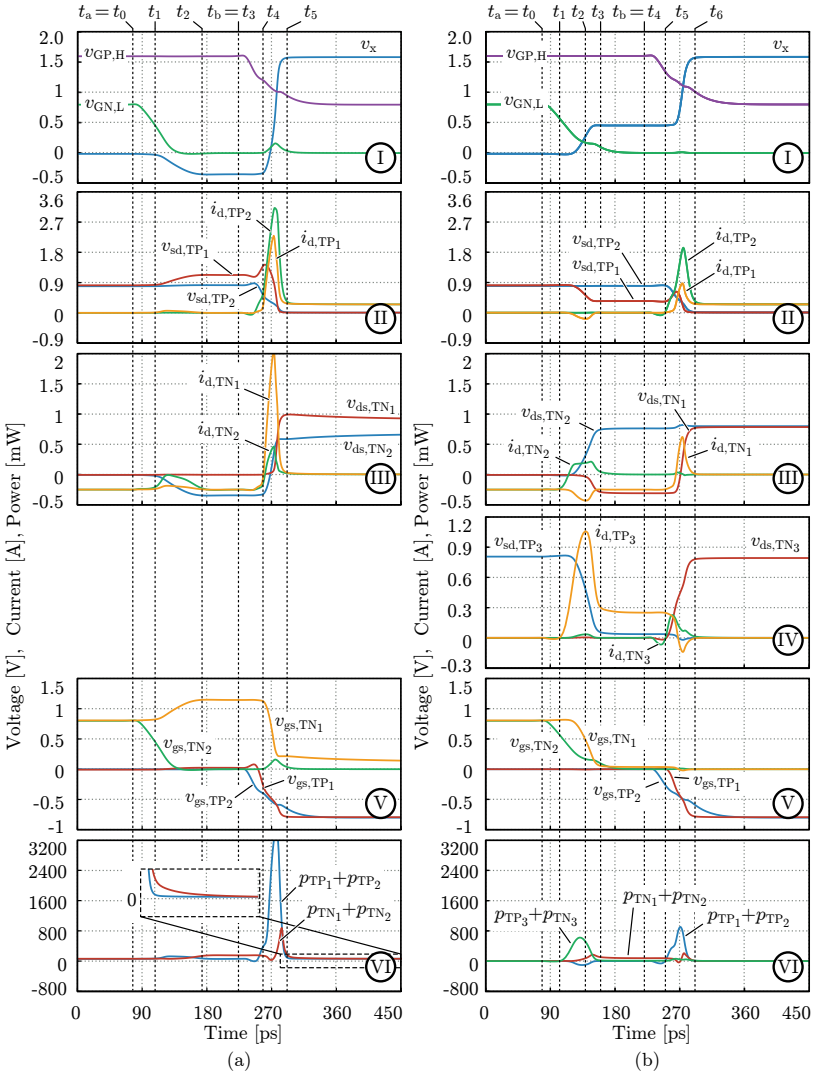


Fig. 2.8: Main waveforms, obtained from Cadence® simulations, of the conventional power stages of Fig. 2.1 during a transient change of v_x from 0 to V_{in} with positive current, I_{sw}. (a) Conventional HBST. (b) Conventional ANPC HBST. The waveforms were generated considering $V_{in} = 1.6\,V$ and $I_{sw} = 250\,mA$.

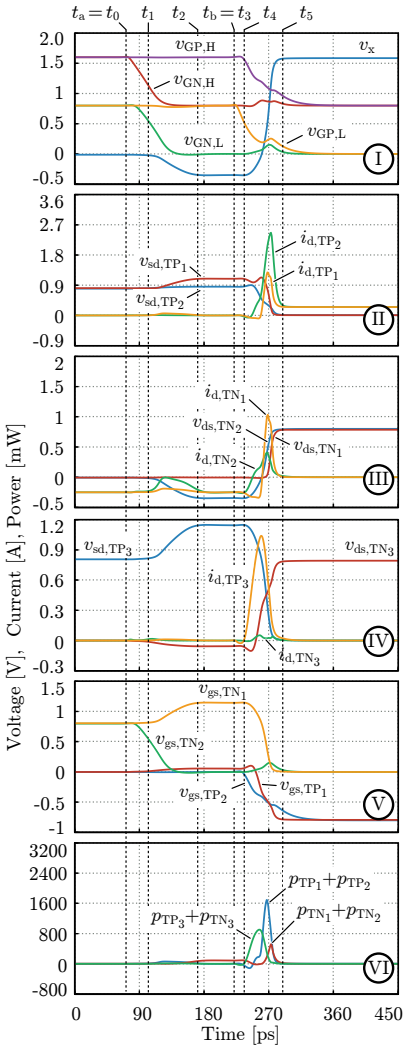


Fig. 2.9: Main waveforms, obtained from Cadence® simulations, of the ANPC with ICS of Fig. 2.2 during a transient change of v_x from 0 to V_{in} with positive current, I_{sw}. The waveforms were generated considering $V_{in} = 1.6\,V$, $I_{sw} = 250\,mA$.

The transient waveforms during switching and case 2 for the ANPC HBST with ICS are given in Fig. 2.9. During the dead time interval, both clamping switches, TN_3 and TP_3, are turned off and, for this reason, similar waveforms compared to Fig. 2.8(a) result. During $t_4 < t < t_5$, however, TP_3 ensures that the drain-source voltage of TN_1 does not exceed V_{mid}. The charging of the parasitic capacitances of TN_1 and TN_2 is, thus, partly achieved by means of TP_3 which leads to lower instantaneous losses than for the conventional HBST.

2.2.3 Discussion

A comparison of the instantaneous switching losses during the rising edge of v_x of the ANPC HBST without and with ICS reveals lower losses of 46 pJ for the ANPC HBST without ICS, compared to 55 pJ for the ANPC HBST with ICS (for the instantaneous power waveforms depicted in Fig. 2.8(b) (VI) and Fig. 2.9 (VI)). However, in the case of a falling edge of v_x, the ANPC HBST without ICS is subject to higher losses of 37 pJ (Fig. 2.6(b) (VI)), compared to 5 pJ for the ANPC HBST with ICS (Fig. 2.7 (VI)). In addition, the switching losses depend on the dead times, $dt_\uparrow$ and $dt_\downarrow$. Accordingly, it is not directly possible to draw a meaningful conclusion. For this reason, the characteristics of the overall simulated efficiencies of the three investigated topologies are compared to each other in the following Section 2.3.

2.3 Simulation Results and Performance Comparison

The transistor's conduction, leakage, gate charge, and switching losses are estimated using energy based models similarly to the approach described in [29]. With the proposed methodology, the estimated total losses deviate by less than 5% from the total losses calculated in Cadence® for all the simulated operating points, which, in general, is accurate enough for the purpose of design and optimization of power management systems. The Cadence® simulated efficiencies may differ from final measurement results, by reason of neglected parasitics of the wiring metals and chip interconnects, which affects the actually present switching losses.

Conduction losses of any power transistor TP_k and TN_k are calculated with

$$P_{\mathrm{cond,TP}_k} = \frac{1}{T_{\mathrm{sw}}} \int_{t_{\mathrm{begin,cond}}}^{t_{\mathrm{end,cond}}} v_{\mathrm{sd,TP}_k}\ i_{\mathrm{d,TP}_k} \mathrm{d}t,\ k = \{1, 2, 3\}, \tag{2.1}$$

and

$$P_{\mathrm{cond,TN}_k} = \frac{1}{T_{\mathrm{sw}}} \int_{t_{\mathrm{begin,cond}}}^{t_{\mathrm{end,cond}}} v_{\mathrm{ds,TN}_k}\ i_{\mathrm{d,TN}_k} \mathrm{d}t,\ k = \{1, 2, 3\}, \tag{2.2}$$

respectively, where T_{sw} is the switching period, $t_{\mathrm{begin,cond}}$ is the instant when the transistor is fully on and $t_{\mathrm{end,cond}}$ is the instant when the transistor is commanded to turn off. The leakage losses, $P_{\mathrm{leak,TN}_k}$ and $P_{\mathrm{leak,TP}_k}$, are similarly calculated, but the integration interval corresponds to the the time intervals between switching events, i.e., excludes the switching operations with their dead times.

The switching energies dissipated by the transistors of the half-bridges are calculated with

$$E_{\mathrm{sw,TP}_k} = \int_{t_{\mathrm{sw,begin}}}^{t_{\mathrm{sw,end}}} \left(v_{\mathrm{sd,TP}_k}\ i_{\mathrm{d,TP}_k} + v_{\mathrm{sg,TP}_k}\ i_{\mathrm{g,TP}_k}\right) \mathrm{d}t,\ k = \{1, 2, 3\}, \tag{2.3}$$

for PMOS and

$$E_{\mathrm{sw,TN}_k} = \int_{t_{\mathrm{sw,begin}}}^{t_{\mathrm{sw,end}}} \left(v_{\mathrm{ds,TN}_k}\ i_{\mathrm{d,TN}_k} + v_{\mathrm{gs,TN}_k}\ i_{\mathrm{g,TN}_k}\right) \mathrm{d}t,\ k = \{1, 2, 3\}, \tag{2.4}$$

for NMOS.[3] The instant $t_{\mathrm{sw,begin}}$ is the time the transistor is commanded to switch on or off and $t_{\mathrm{sw,end}}$ denotes the end of the switching process, i.e., there are no charge changes among the components present and v_{x} is nearly constant.

The gate driver losses are calculated for the gate drivers of TP_2, TP_3, TN_3, and TN_2, if ideally rectangular output voltages of the gate drivers, $v_{\mathrm{g0,TP}_2}(t)$, $v_{\mathrm{g0,TP}_3}(t)$, $v_{\mathrm{g0,TN}_3}(t)$, and $v_{\mathrm{g0,TN}_2}(t)$, are assumed. With this,

$$E_{\mathrm{gd,TP}_k} = \int_{t_{\mathrm{sw,begin}}}^{t_{\mathrm{sw,end}}} i_{\mathrm{g,TP}_k}\ \left(v_{\mathrm{g0,TP}_k} - v_{\mathrm{sg,TP}_k}\right) \mathrm{d}t,\ k = \{2, 3\}, \tag{2.5}$$

results for the PMOS transistors and

$$E_{\mathrm{gd,TN}_k} = \int_{t_{\mathrm{sw,begin}}}^{t_{\mathrm{sw,end}}} i_{\mathrm{g,TN}_k}\ \left(v_{\mathrm{g0,TN}_k} - v_{\mathrm{gs,TN}_k}\right) \mathrm{d}t,\ k = \{2, 3\}, \tag{2.6}$$

[3] The second terms in (2.3) and (2.4) take eventual additional losses during charging and discharging of the gate capacitances into account, which may arise in on-chip parasitic resistances, due to high gate currents.

for the NMOS transistors. The gate capacitances of TP_1 and TN_1 are charged by the other transistors of the HBST, which increases their switching losses.[4]

The total losses are estimated by summing up the conduction losses, leakage losses, gate driver losses, and switching losses of all transistors

$$P_{\text{tot}} = \sum_{k=1}^{3} \Big(P_{\text{cond,TN}_k} + P_{\text{cond,TP}_k} + P_{\text{leak,TN}_k} + P_{\text{leak,TP}_k} + (E_{\text{sw}_{\text{case1}},\text{TP}_k} + E_{\text{sw}_{\text{case2}},\text{TP}_k} + E_{\text{sw}_{\text{case1}},\text{TN}_k} + E_{\text{sw}_{\text{case2}},\text{TN}_k}) f_{\text{sw}} \Big) + \sum_{k=2}^{3} (E_{\text{gd}_{\text{case1}},\text{TP}_k} + E_{\text{gd}_{\text{case2}},\text{TP}_k} + E_{\text{gd}_{\text{case1}},\text{TN}_k} + E_{\text{gd}_{\text{case2}},\text{TN}_k}) f_{\text{sw}}. \tag{2.7}$$

Fig. 2.10, Fig. 2.11, and Fig. 2.12 present comparisons of the simulated efficiencies and losses breakdowns of the studied HBSTs when the deadtime interval during a falling edge of v_{x} ($dt_{\downarrow}$), switching frequency, and load current are varied, respectively. In Fig. 2.10 $dt_{\downarrow}$ is varied from 50 ps to 250 ps while the switching frequency and the load current are maintained constant at 150 MHz and 250 mA, respectively.[5] The efficiency curves of the proposed ANPC HBST and the conventional HBST are very similar in shape and have their peaks at the same dead time value of 200 ps. The difference in offset of the efficiency results is due to the increased switching losses in the PMOS transistors during the rising edge of v_{x} (case 2) for the conventional HBST, as explained in Subsection 2.2.2 and quantified in Fig. 2.10 ②. If the dead time is decreased to values below the optimal value, i.e., the value of $dt_{\downarrow}$ that yields best efficiency, incomplete discharging and charging of the transistors' effective output capacitances results, which leads to increased switching losses due to turn-on losses. This increase of the switching losses during the falling edge of v_{x}, for small dead times $dt_{\downarrow} < 200$ ps, can be seen in the losses breakdown of the proposed ANPC HBST and the conventional HBST,

[4] For example, in case of the conventional HBST, a turn-on of TP_2 leads to a turn-on of TP_1. During charging of the gate capacitance of TP_1, the transistor TP_2 forms the "charging resistor" for the gate current of TP_1. Accordingly, the gate driver losses of TP_1 are additional switching losses in TP_2 (which are already considered by means of the first term of (2.3)).

[5] At $dt_{\downarrow} = 150$ ps in Fig. 2.10, the conventional HBST, the conventional ANPC, and the proposed ANPC generate losses of 20.4 mW, 20.5 mW, and 19.2 mW, respectively. However, due to slightly different output voltages, the three topologies provide slightly different output power levels. As a result, the efficiency of the conventional ANPC ($\eta = 89.9\,\%$) is higher than that of the conventional HBST ($\eta = 89.7\,\%$), even though, the conventional ANPC generates more losses than the conventional HBST.

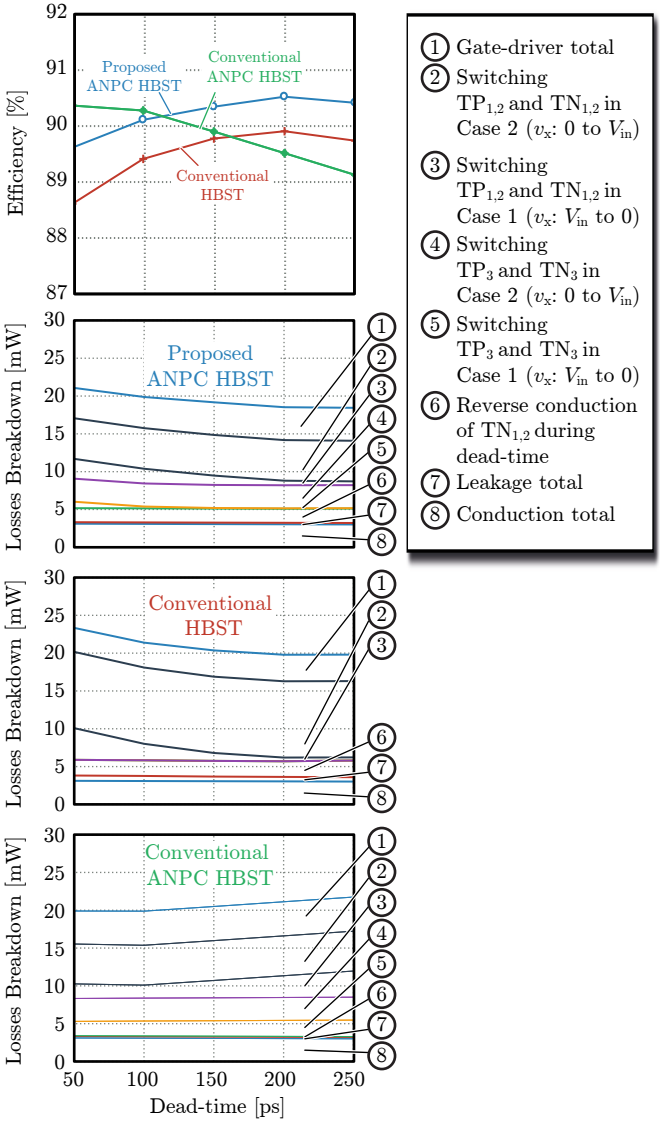


Fig. 2.10: Losses and efficiencies determined with Cadence® simulations for the topologies depicted in Fig. 2.1 and Fig. 2.2 for varying duration of $dt_{\downarrow}$ (the dead time interval during the falling edge of v_x), $f_{sw} = 150\,\text{MHz}$, $I_{sw} = 250\,\text{mA}$, $V_{in} = 1.6\,\text{V}$, and duty-cycle $D = 0.5$; the dead time interval during the rising edge of v_x is kept constant, $dt_{\uparrow} = 40\,\text{ps}$.

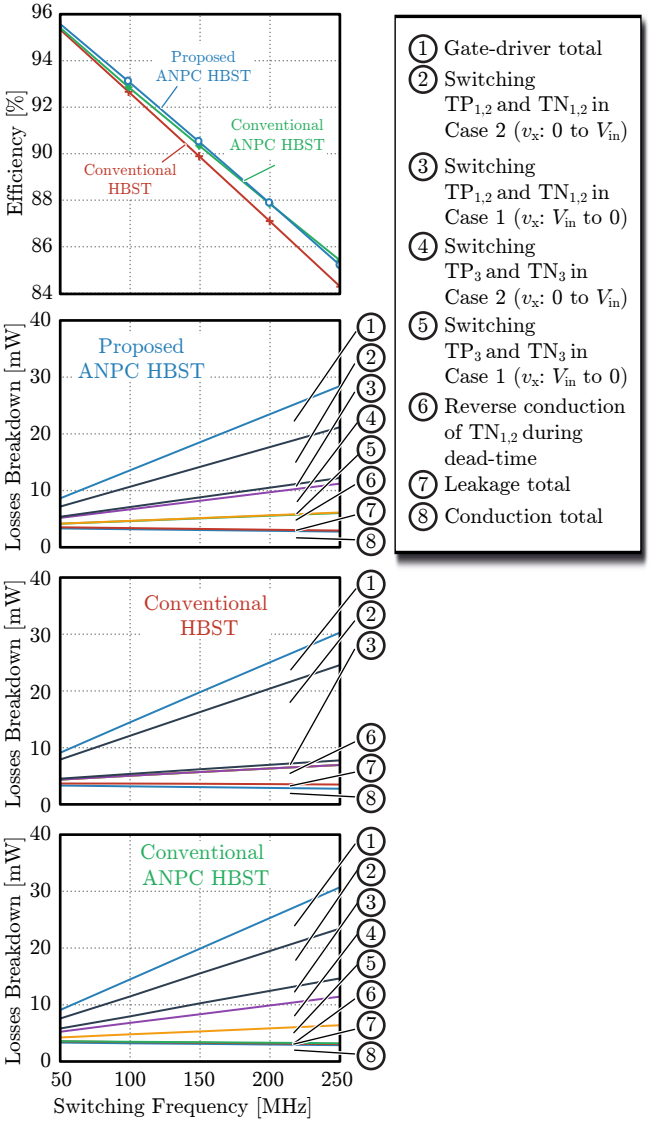


Fig. 2.11: Losses and efficiencies determined with Cadence® simulations for the topologies depicted in Fig. 2.1 and Fig. 2.2 for varying switching frequency and operation with optimal dead time during the falling edge of v_x, $I_{sw} = 250\,\text{mA}$, $V_{in} = 1.6\,\text{V}$, and duty-cycle $D = 0.5$; the dead time interval during the rising edge of v_x is kept constant, $dt_{\uparrow} = 40\,\text{ps}$.

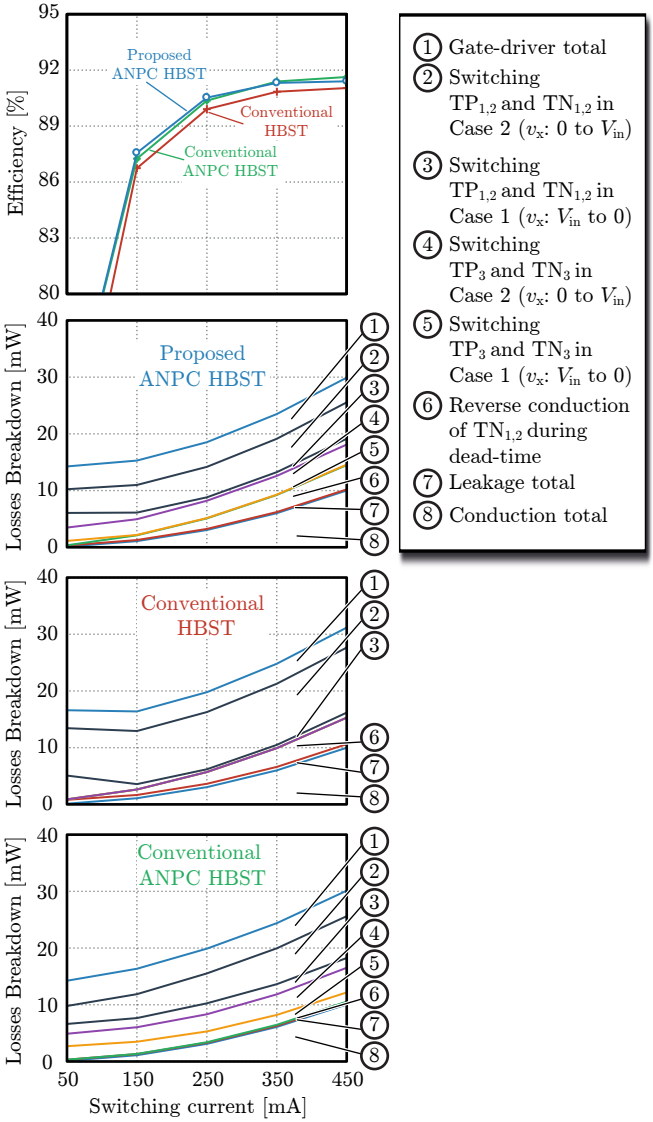


Fig. 2.12: Losses and efficiencies determined with Cadence® simulations for the topologies depicted in Fig. 2.1 and Fig. 2.2 for varying switching current at operation with optimal dead time during the falling edge of v_x, $f_{sw} = 150\,\text{MHz}$, $V_{in} = 1.6\,\text{V}$, and duty-cycle $D = 0.5$; the dead time interval during the rising edge of v_x is kept constant, $dt_{\uparrow} = 40\,\text{ps}$.

cf. Fig. 2.10 ③. Dead times larger than the optimal value only lead to more conduction losses due to the conduction of the load current through TN_2, which operates in the saturation region when v_x reaches values close to zero. It is also observed in Fig. 2.10 that the efficiency of the conventional ANPC HBST is highest for a very small dead time of $dt_{\downarrow} = 50\,\text{ps}$ and only decreases for increasing dead time. This behavior is caused by the additional conduction losses that are generated during the dead time interval when TN_1 conducts in the saturation mode, cf. Fig. 2.10 ③. According to the simulation results, the proposed power stage achieves improvements in efficiency of approximately 0.9 % compared to the conventional HBST if the optimum dead time during the falling edge of v_x is implemented (at switching frequency $f_{sw} = 150\,\text{MHz}$, input voltage $V_{in} = 1.6\,\text{V}$, duty-cycle $D = 0.5$, and given dead time during the rising edge of v_x of $dt_{\uparrow} = 40\,\text{ps}$).

To obtain a fair performance comparison, the optimal dead times are selected in order to maximize the efficiency for the cases where switching frequency and load current are varied, cf. Fig. 2.11 and Fig. 2.12. From Fig. 2.11 it can be seen that the difference in efficiency between the conventional and proposed ANPC HBST to the conventional HBST increases with increase of the switching frequency.[6] This trend is explained due to the increased value of switching losses during the switching transient of case 2, cf. Fig. 2.11 ②, for the conventional HBST. At a switching frequency of 250 MHz, the ANPC HBSTs can achieve efficiency gains of approximately 1 % compared to the conventional HBST.

From Fig. 2.12[7], it can be verified that the load change mainly affects the total conduction losses of the HBSTs when the optimal dead time is employed.

Some general features and trends are observed for the HBSTs from the losses breakdown independently of the implemented dead times, switching frequencies, and load currents:

[6] At $f_{sw} = 250\,\text{MHz}$ in Fig. 2.11, the conventional HBST, the conventional ANPC, and the proposed ANPC generate losses of 30.3 mW, 30.7 mW, and 28.4 mW, respectively. However, due to slightly different output voltages, the three topologies provide slightly different output power levels. As a result, the efficiency of the conventional ANPC ($\eta = 85.4\,\%$) is higher than that of the conventional HBST ($\eta = 84.3\,\%$), even though, the conventional ANPC generates similar losses than the conventional HBST.

[7] At $I_{dc} = 250\,\text{mA}$ in Fig. 2.12, the conventional HBST, the conventional ANPC, and the proposed ANPC generate losses of 30.2 mW, 30.1 mW, and 29.9 mW, respectively. However, due to slightly different output voltages, the three topologies provide slightly different output power levels. As a result, the efficiency of the conventional ANPC ($\eta = 91.6\,\%$) is higher than that of the conventional HBST ($\eta = 91\,\%$), even though, the conventional ANPC generates similar losses than the conventional HBST.

- According to ⑦ of Fig. 2.10, Fig. 2.11, and Fig. 2.12, the conventional HBST is subject to increased leakage losses due to the unbalance of the voltages after the switching transients.
- Switching losses of clamping transistors are higher for the conventional ANPC HBST topology due to the discharge of the gate capacitances of the PMOS main transistors during the dead time interval of case 1, cf. ⑤ of Fig. 2.10, Fig. 2.11, and Fig. 2.12.
- The gate driver losses are relatively high compared to the total switching losses due to the high values of gate currents, cf. ① of Fig. 2.10, Fig. 2.11, and Fig. 2.12. The high currents result from charging and discharging the gate capacitances of the transistors, which are particularly high compared to the drain-source capacitances in the investigated CMOS technology.
- With respect to dead time, the proposed ANPC HBST features a flatter efficiency curve and achieves the maximum efficiency at a considerably higher dead time than the conventional ANPC HBST. This is an advantage since very small and accurate dead times requires a more careful design of the dead time controller and can be limited by the technology node.

2.4 Summary

This chapter presents a comparative evaluation of three different topologies for buck converters using stacked transistors for IVRs. The evaluation is based on in-depth examinations of the internal processes in the power transistors of the considered converters, in particular with regard to the switching transients, using Cadence® simulations.

The first considered topology, the conventional HBST, features lowest implementation effort, however, considerably unbalanced blocking voltages appear for the main switches after the switching transients, which lead to overvoltages and reduce the reliability, lifetime, and efficiency of the converter ($\eta = 89.9\,\%$ at $f_{sw} = 150\,\mathrm{MHz}$, $I_{sw} = 250\,\mathrm{mA}$, and $dt_{\uparrow} = 40\,\mathrm{ps}$). The second topology, the conventional ANPC HBST, requires two additional clamping switches and, with this, achieves balanced blocking voltages. Compared to the first topology an increased efficiency of $90.4\,\%$ ($f_{sw} = 150\,\mathrm{MHz}$, $I_{sw} = 250\,\mathrm{mA}$, $dt_{\uparrow} = 40\,\mathrm{ps}$) is obtained, at a very short dead time of 50 ps. Due to its internal structure, however, the conventional ANPC HBST cannot turn

off the power stage. Also, the third topology, the proposed ANPC HBST, balances the blocking voltages and, in addition, is capable to turn off its power stage. The proposed ANPC HBST maintains soft switching, for this reason maximum efficiency of 90.5 % results at a dead time that is greater than for the conventional ANPC HBST ($dt_{\downarrow,\mathrm{opt}} = 200\,\mathrm{ps}$ at $f_{\mathrm{sw}} = 150\,\mathrm{MHz}$, $I_{\mathrm{sw}} = 250\,\mathrm{mA}$). In summary, both, the conventional and the proposed ANPC HBST, feature balanced blocking voltages of the main transistors and are expected to be capable of providing similar efficiencies. Of these two, however, only the proposed ANPC HBST is suitable for multi-phase converters since it can turn off its power stage. In Chapter 3, a versatile Power Management IC (PMIC) is implemented, which allows for the emulation of all three HBST topologies in order to enable experimental verification of the simulation results.

3

Hybrid IVR Demonstrators and Characterization

Chapter Abstract

This chapter presents a comprehensive characterization of a PCB- and inductor-based four-phase ANPC-type IVR that uses a Power Management IC (PMIC) implemented in a 14 nm CMOS technology node. In a first part, the IVR is characterized based on the results of electrical measurements, thermal inspections of the chip surface, and simulations, which enable the separation of the total losses into on-chip and off-chip loss components and the allocation of important loss components inside the chip. In a second part, an experimental evaluation of the conventional HBST, the ANPC HBST, and the ANPC HBST with ICS is presented. In this regard, it is found that the ANPC HBST with ICS not only ensures balanced blocking voltages across the series-connected transistors, cf. Chapter 2, but also achieves similar or higher efficiency than the conventional HBST and the conventional ANPC HBST. With all four phases being operational, the investigated IVR achieves a maximum efficiency of 84.1 % at an output power of $P_{\mathrm{out}} = 640\,\mathrm{mW}$ and a switching frequency of $f_{\mathrm{s}} = 50\,\mathrm{MHz}$. The thermal measurements reveal that the maximum efficiency of the PMIC itself is between 88 % and 90 % at $f_{\mathrm{s}} = 50\,\mathrm{MHz}$ and $P_{\mathrm{out}} \in [500\,\mathrm{mW},\ 600\,\mathrm{mW}]$; at $P_{\mathrm{out}} = 890\,\mathrm{mW}$, a chip current density of $24.7\,\mathrm{A/mm^2}$ is achieved. The findings in particular point out that the losses in the chip-internal interconnections, i.e., the conductors of the Power Distribution Network (PDN) and the twelve stacked metal layers below the PDN, have a substantial contribution to the total losses. Furthermore, the combination of Cadence® post-layout simulations with impedance networks obtained from an appropriate software tool, e.g., FastHenry, is found to establish a suitable toolbox for estimating losses in IVRs. The main findings described in this chapter have been also presented in [27, 39]

The main aim of this chapter is the identification and allocation of the loss components in a four-phase buck-type hybrid IVR, which employs a switching stage realized in 14 nm CMOS technology. Electrical and thermal measurements are conducted in order to enable a separation of on-chip losses (e.g., due to conduction and switching) and off-chip losses (e.g., in the inductors), which requires a physical separation of the chip and the inductors. The investigated IVR employs discrete inductors and capacitors that reside on a PCB; bond wires provide the electrical connections between chip and PCB, as illustrated in Fig. 3.1. Section 3.1 details the implemented Power Management IC (PMIC), i.e., converter specifications, the main schematic diagram of the semiconductor power stage, the chip lithograpy, and the gate signal generation unit. Section 3.2 describes the conducted thermal and electrical characterization procedures that serve for the separation of the total losses into on-chip and off-chip components and discusses the obtained results, which reveal that the losses in the metal layers and the Power Distribution Network (PDN) of the PMIC have a substantial contribution to the total losses. With all four phases being active, the complete IVR achieves a maximum efficiency of 84.1 % and a full-load efficiency of 83.0 % and a corresponding chip current density of 24.7 $\mathrm{W/mm^2}$. The maximum efficiency of the PMIC itself, which is subject to increased uncertainty due to the measurement with a thermal camera, is between 88 % to 90 % for output power levels between 500 mW and 600 mW. Finally, Section 3.3 presents a comparative evaluation of the three topologies investigated in Chapter 2, i.e., the conventional CMOS HBST, the conventional CMOS HBST ANPC, and the CMOS HBST ANPC with ICS, based on measured efficiencies. Compared to the conventional HBST, the ANPC HBST topologies guarantee the same voltages across the stacked transistors. However, it is found that the standard ANPC HBST is subject to increased switching losses and is less suitable for a multi-phase converter (no phase shedding possible). The ANPC HBST with ICS eliminates the shortcomings of the standard ANPC HBST (at the cost of 14 % more chip area compared to the conventional HBST).

3.1 Designed PMIC in 14 nm Technology

Tab. 3.1 lists the specifications of the investigated IVR, which is a prototype of an IVR intended for providing power to a Voltage Domain (VD) of a CPU core, and Fig. 3.2(a) depicts the schematics of the implemented PMIC. Since the input voltage of 1.6 V exceeds the transistors' maximum drain-source voltage of a short channel device of the employed CMOS technology

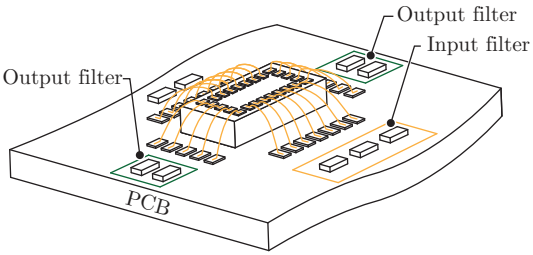
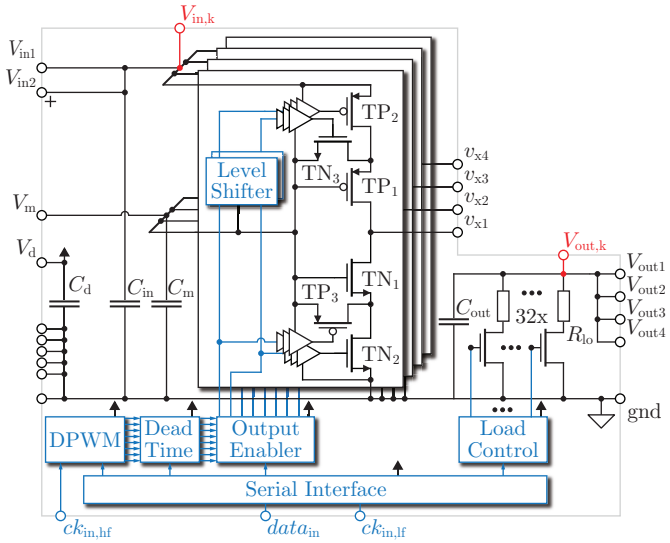


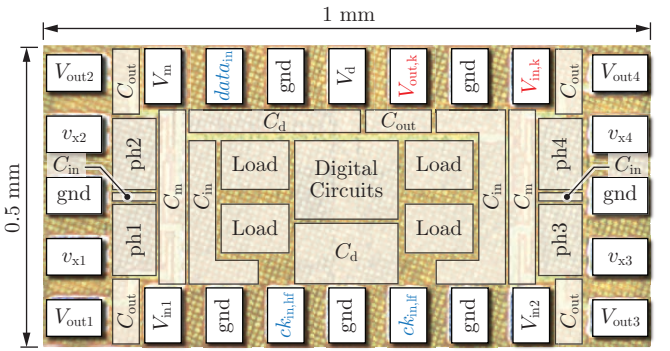
Fig. 3.1: Illustration of the investigated setup: the active switching stage resides in the Power Management IC (PMIC), the passive components (capacitors, inductors) on the PCB, and bond wires provide the electrical connections.

Tab. 3.1: Specifications of the investigated four-phase IVR.

Parameters	Symbol	Value
Input voltage	V_{in}	1.6 V
Output voltage range	V_{out}	0.8 V to 1.2 V
Output power	P_{out}	800 mW
Min. output voltage	$V_{\text{out,min}}$	0.6 V



(a)



(b)

Fig. 3.2: (a) Simplified schematic of the PMIC containing the four-phase CMOS ANPC HBST with ICS. (b) Chip micrography of the implemented PMIC with the pads according to (a); 'ph1' to 'ph4' denote the locations of the HBST of the four converter phases; 'C_{in}', 'C_m', 'C_{out}', and 'C_d' refer to the positions of the corresponding capacitors realized with MOS technology; loads and gate signal generation unit are located toward the center of the PMIC.

node, each switch of the realized buck converter is composed of two stacked transistors. Furthermore, TN_3 and TP_3 in Fig. 3.2(a) realize an Active Neutral Point Clamping (ANPC) circuit in order to avoid unbalanced voltages across the main power transistors during or after switching, to improve efficiency and reliability, as explained in Chapter 2 and [38]. The chip consists of four CMOS Half-Bridges with Stacked Transistors (HBST) with ANPC and ICS, an open-loop logic circuitry to generate the switches' gate signals, and a configurable internal resistive load.

The chip requires three supply voltages. The main supply is connected to the $V_{\text{in}\{1,2\}}$-pads, which share the converter input current. An auxiliary voltage is provided at the V_{m}-pad, to define the gate bias voltages for TP_1 and TN_1 and the source potentials of the clamping switches TN_3 and TP_3. There, the applied voltage needs to be controlled to half of the input voltage, $V_{\text{m}} = V_{\text{in}}/2$, to avoid additional leakage currents. The voltage supply of the auxiliary analog and digital circuits (open-loop logic circuitry, load control circuitry, serial interface, and flash memory) is connected to the V_{d}-pad. A two-wire unidirectional serial interface (pads $data_{\text{in}}$ and $ck_{\text{in,lf}}$ for data and clock inputs, respectively) serves for the configuration of gate signal generation unit and on-chip load; an on-chip flash memory stores the current configuration.

The signal provided at the $ck_{\text{in,hf}}$-pad controls the switching frequency of the CMOS ANPC HBST. The frequency of the given clock signal is divided by 16, e.g., a clock signal with a frequency of 1.6 GHz at the $ck_{\text{in,hf}}$-pad results in a switching frequency of 100 MHz. The switched output voltages are present at the $v_{\text{x}\{1,2,3,4\}}$-pads and applied to the external filter inductors. The filtered output voltages are connected back to the PMIC at the $V_{\text{out}\{1,2,3,4\}}$-pads, to utilize the chip-integrated configurable load. The chip includes two Kelvin pads, $V_{\text{in,k}}$ and $V_{\text{out,k}}$, to allow for accurate four-point voltage measurements of the input and output voltages, respectively. Seven ground pads are used in parallel to reduce the converter losses and provide a stable reference for the internal chip circuits.

Fig. 3.2(b) shows the micrography of the realized PMIC in 14 nm CMOS technology. The total chip area is $0.5\,\text{mm}^2$, from which $0.032\,\text{mm}^2$ are dedicated to the HBST of the four-phase converter [ph{1,2,3,4} in Fig. 3.2(b)], $0.027\,\text{mm}^2$ to the digital circuits, and $0.052\,\text{mm}^2$ to the four chip-internal loads. The power stages are placed at the edges of the chip, to achieve a layout that features short paths to the respective input and output pads, e.g., $V_{\text{in,1}}$ and $v_{\text{x,1}}$ in case of phase 1, in order to avoid excessive conduction losses in the PDN of the chip, as further detailed in Subsection 3.1.1. Chip-integrated buffering of the supply voltages V_{in}, V_{m}, and V_{d} and the voltage provided to

the load, V_{out}, is realized with a combination of Metal-Oxide-Semiconductor (MOS) and Metal-Insulator-Metal (MIM) capacitors. The MOS capacitors are placed in the Front End Of Line (FEOL) areas marked in Fig. 3.2(b) and MIM capacitors are placed in the entire BEOL area of the chip excluding the pads. Fig. 3.3(c) illustrates a cross-sectional drawing of the power stage, revealing FEOL, BEOL, and the general locations of MIM and MOS capacitors.

3.1.1 Power Stage

Fig. 3.3(a) depicts a detailed schematic drawing of a single phase (CMOS ANPC HBST with ICS) of the implemented PMIC. The output stage is composed of the main transistors (①: TP_1, TP_2; ⑤: TN_1, TN_2) and the clamping transistors (②: TN_3 and ⑥: TP_3). Four gate drivers, ③, ④, ⑦, ⑧, ⑨, are used for the main switches and the clamping switches, where each gate driver is composed of four inverter stages that are connected in series. Two level shifters ⑨ adjust the voltages of the input signals in order to be suitable for the high-side gate drivers.

Fig. 3.3(b) presents the layout of a single converter phase corresponding to the schematics of Fig. 3.3(a) and Fig. 3.3(c) depicts a drawing of the cross section of the chip, revealing the top metal layer (contains the pads), the two layers of the PDN with the MIM capacitor layer in between, and the 12 metal layers. The FEOL area of the complete power stage is $0.0081\,\text{mm}^2$. As already described in Chapter 2, all main transistors (① and ⑤) are of same size, each clamping transistor (② and ⑥) and the final inverter stage of each gate driver (③ and ⑦) require 1/10 of the area of one main transistor, and the second and third stages of each gate driver (④ and ⑧) together need 1/50 of the area of one main transistor. The two additional gate drivers for the clamping transistors and the additional level shifter increase the total chip FEOL area by approximately 14 % as compared to a conventional CMOS HBST. The remaining FEOL area is used to realize MOS capacitors (⑩).

Each phase of the CMOS ANPC HBST with ICS uses the gate signals depicted in Fig. 2.5(a) and Fig. 2.5(c) to generate a rectangular voltage with its main transistors at the respective output node, i.e., $v_{\text{x},i} = 0$ or $v_{\text{x},i} = V_{\text{in}}$ for $i \in \{1, 2, 3, 4\}$, and to balance the voltages across the stacked main transistors with the clamping transistors. The shown sequence is based on two complementary signals with dead time, $ck_{\text{P,H}}$ and $ck_{\text{N,L}}$, and uses separate dead times, $dt_{\downarrow}$ and

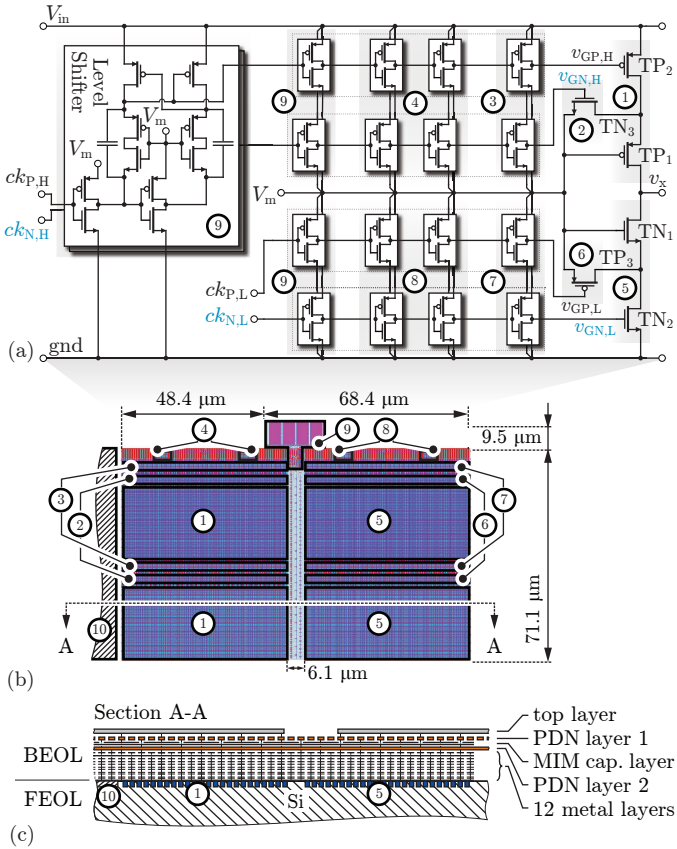


Fig. 3.3: (a) Schematics of a single converter phase of the CMOS ANPC HBST with ICS. (b) Layout picture of the designed CMOS ANPC HBST with ICS corresponding to the schematics of Fig. 3.3(a). The two clamping switches, two independent gate drivers, and one level shifter increase the chip FEOL area by approximately 14 % as compared to a conventional CMOS HBST.

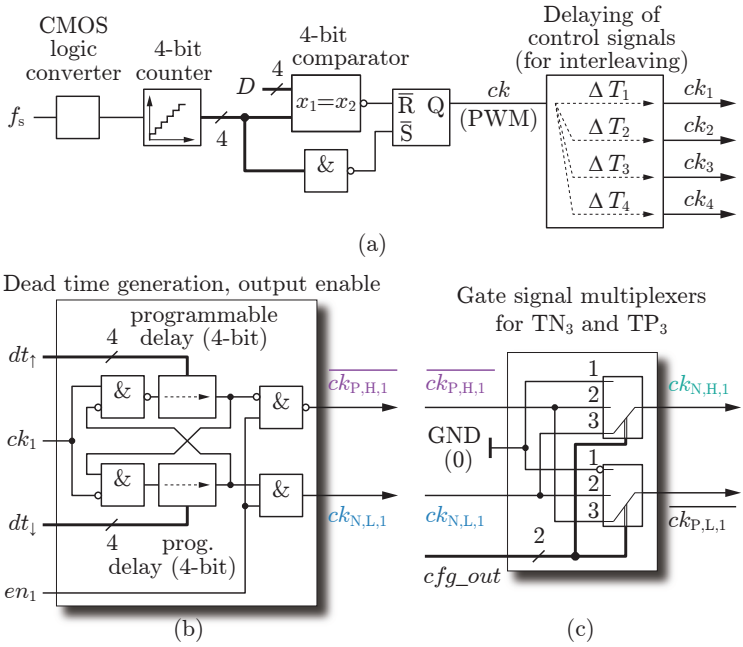


Fig. 3.4: Digital control signal generation unit for all 4 converter phases. (a) Digital Pulse Width Modulator (PWM) unit and configurable delay block. (b) Configurable dead time generation unit and output-side enable function for the example of Phase 1. (c) Multiplexers for the gate signals of TN_3 and TP_3 (Phase 1).

$dt_{\uparrow}$, for the falling and rising edges of the rectangular output voltage.[1] The duration of both dead times, $dt_{\downarrow}$ and $dt_{\uparrow}$, are programmable in order to enable the operating-point dependent optimization of the switching losses. Further details related to the operation of the CMOS ANPC HBST are presented in Chapter 2.

Fig. 3.4 depicts the functional blocks that generate the gate signals for the power transistors, i.e., the digital PWM unit (Fig. 3.4(a)), configurable dead time generation units (Fig. 3.4(b)), and gate signal multiplexers (Fig. 3.4(c)). The circuitries shown in Figs. 3.4(b and c) were separately implemented for each converter phase. The PWM unit receives the input clock from the clock signal ck_{in} and generates a PWM signal, ck, that features 16 discrete duty cycles. The output of the PWM unit is connected to the configurable delay block, which realizes the phase-shifted gate signals $ck_{\{1,2,3,4\}}$, in order to enable interleaving. Each dead time generation unit uses one output signal of the configurable delay block, e.g., ck_1 in the case of Converter Phase 1, to generate the gate signals depicted in Fig. 3.4(a) and includes an output enable logic that is controlled by en_1 to allow for the deactivation of selected converter phases (phase shedding). Two four-bit values, which represent $dt_{\uparrow}$ and $dt_{\downarrow}$, are used to configure the respective dead times. Finally, the multiplexer circuit employs the two-bit configuration signal *cfgout* to configure how the gate signals for the clamp switches are generated. With this, the three investigated topologies can be emulated: HBST (Position 1), ANPC HBST (Position 2), and ANPC HBST with ICS (Position 3). All the power switches feature also an additional manual configuration mode used for the characterization of the DC resistances of the transisors which is not depicted in Fig. 3.4 for sake of simplicity.

3.2 Characterization of the PCB-Based IVR

The employed procedure to characterize the converter losses takes calculated and simulated results as well as experimental results from electrical and thermal measurements into account, to accurately identify the different loss components of the investigated converter. The procedure comprises of the steps listed below.

[1]Please note that TP_1, TP_2, and TP_3 are p-type transistors, e.g., $v_{\text{GP,L}} = 0$ turns TP_3 on and $v_{\text{GP,L}} = V_{\text{in}}/2$ turns TP_3 off, cf. Fig. 2.5(c). Accordingly, the gate drivers ensure that TN_2, TP_2, TN_3, and TP_3 are turned off during both dead times.

1. Numerical estimation of the DC resistances of the power transistors' channels, the metal layers, the converter interconnections, and the PDN using numerical software tools (Cadence® post-layout simulations, FastHenry).

2. Electrical measurement of the converter's DC resistances and comparison to the numerical estimations in order to clarify whether all important contributions to the DC losses are considered.

3. Use of the chip-internal configurable resistive load to characterize the temperature rise of the chip with respect to on-chip power dissipation, which enables a separation of the converter's AC and DC losses.

4. Experimental evaluation at different operating points, using an external electronic load (chip-internal load is disabled): electrical measurements of input and output power levels and thermal measurement of the chip temperature. This enables a separation of on-chip and off-chip losses of the IVR.

Steps 1 and 2 are further detailed in Subsection 3.2.1, step 3 is discussed in Subsection 3.2.2, and step 4 in Subsection 3.2.3.

Fig. 3.5 depicts the employed experimental setup with a schematic overview in Fig. 3.5(a), the realization of the hybrid PCB-based four-phase IVR in Fig. 3.5(b), and a magnified view of the IVR in Fig. 3.5(c). The investigated IVR utilizes the PMIC of Fig. 3.2. High Temperature Silicon Capacitors (HTSC) with low equivalent series inductance (manufactured by IPDiA®) realize the DC capacitors, $C_{\text{in1}} = 43\,\text{nF}$, $C_{\text{d1}} = 10\,\text{nF}$, $C_{\text{m1}} = 10\,\text{nF}$, and $C_{\text{out}\{1,2,3,4\}} = 10\,\text{nF}$. Solenoidal inductors with magnetic cores (PFL1005-36NMR, manufactured by Coilcraft®) with $L_{\{1,2,3,4\}} = 36\,\text{nH}$ form the output inductors. All measurements are conducted with the high-accuracy equipment listed below.

- *N6781A*: two-quadrant measurement unit, providing the supply voltages and the load current.

- *DAU34970*: data acquisition unit used for all voltage measurements.

- *SC5000*: thermal camera to monitor the temperature distribution on the chip. The camera is equipped with the microscopic zoom lens Lo808X5 (1.9×1.4 mm).

Tab. 3.2 lists the specified relative and absolute measurement uncertainties, δ and ϵ, that apply for a certain value, X, for a corresponding measured value,

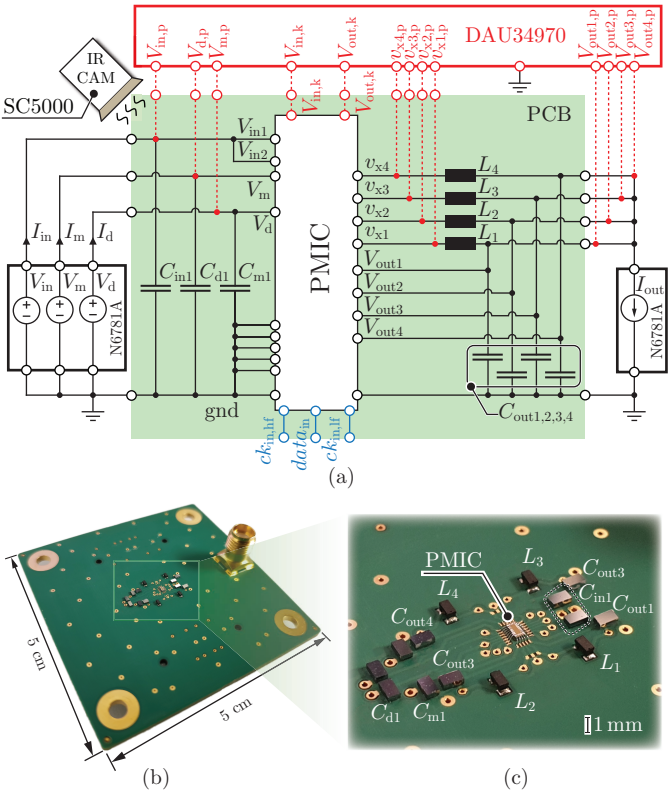


Fig. 3.5: (a) Measurement setup used for the loss characterization and the efficiency measurements. Aluminum bond wires are used to connect the PMIC to the PCB substrate; SMA connectors with coaxial cables provide the connections between PCB, measurement devices, and power supplies. (b) Picture of the corresponding assembled PCB-based IVR. (c) Magnified view of the center of the IVR with the PMIC in the middle.

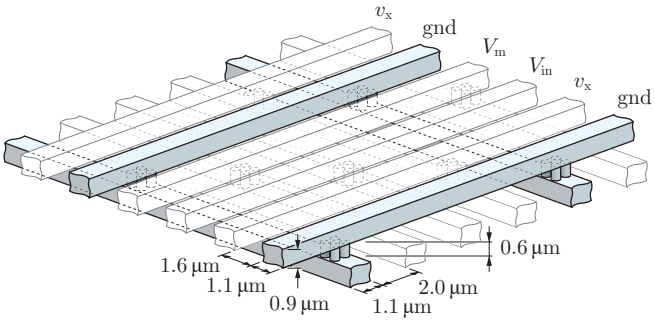


Fig. 3.6: The Power Distribution Network (PDN) consists of horizontal and orthogonally oriented conductors; four vias connect the conductors at each crossing. The PDN alternately provides connections for V_{in}, V_m, gnd, and v_x, where v_x denotes the switched voltage of the connected converter phase, e.g., $v_x = v_{x1}$ applies in case of the PDN for converter phase 1. A detailed description of the PDN is provided in [47].

X_{meas},

$$X \in \left[X_{meas}\,(1-\delta) - \epsilon,\; X_{meas}\,(1+\delta) + \epsilon\right]. \tag{3.1}$$

For all experiments, $V_{in,k} = 1.6\,V$ and $V_m = 0.8\,V$ apply.

3.2.1 DC Resistances

The DC losses substantially contribute to the total converter losses, which is partly due to the MOSFETs' on-state resistances. However, also the PDN is prone to increased losses in the 14 nm CMOS technology, due to very thin layers of metallization, and needs to be taken into account. Fig. 3.6 illustrates the layout of the PDN, which realizes an interleaved structure of the required power conductors (e.g., V_{in}, V_m, gnd, and, in case of converter phase 1, v_{x1}).

Tab. 3.2: Accuracies of DAU34970 (voltage) and N6781A (current).

Equipment	Measurement error	
	δ	ϵ
DAU34970	±0.0035 %	±50 µV
N6781A	±0.03 %	±250 µA

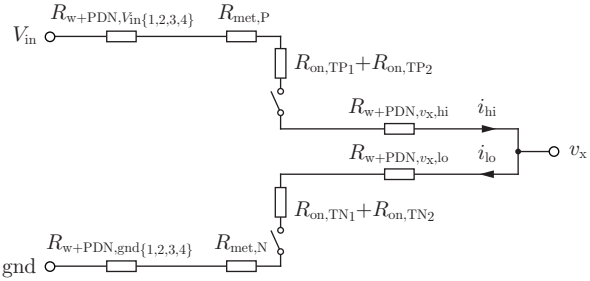


Fig. 3.7: Internal resistances of the PMIC arising from bond wires and PDN ($R_{\mathrm{w+PDN},V_{\mathrm{in}\{1,2,3,4\}}}$, $R_{\mathrm{w+PDN,GND}_{\{1,2,3,4\}}}$, $R_{\mathrm{w+PDN},v_{\mathrm{x}},\mathrm{hi}}$, $R_{\mathrm{w+PDN},v_{\mathrm{x}},\mathrm{lo}}$), metal layers stack and vias ($R_{\mathrm{met,P}}$, $R_{\mathrm{met,N}}$), and MOSFET channels ($R_{\mathrm{on,TP}_{\{1,2\}}}$, $R_{\mathrm{on,TN}_{\{1,2\}}}$).

It consists of horizontal conductors on a first layer, vertical conductors on a second layer, and vias at the crossings to connect the two layers to each other [47].

Fig. 3.7 depicts the network of the internal resistances of the PMIC, which arise from bond wires and PDN ($R_{\mathrm{w+PDN},V_{\mathrm{in}\{1,2,3,4\}}}$, $R_{\mathrm{w+PDN},v_{\mathrm{x}},\mathrm{hi}}$, $R_{\mathrm{w+PDN},v_{\mathrm{x}},\mathrm{lo}}$, $R_{\mathrm{w+PDN,gnd}_{\{1,2,3,4\}}}$), metal layers stack and vias ($R_{\mathrm{met,P}}$ and $R_{\mathrm{met,N}}$), and MOSFET channels ($R_{\mathrm{on,TP}_{\{1,2\}}}$ and $R_{\mathrm{on,TN}_{\{1,2\}}}$). FastHenry has been used to compute the resistances of the PDN and Cadence® post-layout simulations to determine the resistances of metal layers stack, vias, and MOSFETs; Tab. 3.3 lists the respective results. According to this result, the resistances of the metal layers stacks are comparably small, however, the effective resistances of the PDN are more than twice of the on-state resistances of two series-connected MOSFETs, e.g., in case of the high-side conduction path of phase 1, $R_{\mathrm{w+PDN},V_{\mathrm{in}\{1,2,3,4\}}} + R_{\mathrm{w+PDN},v_{\mathrm{x}},\mathrm{hi}} = 284\,\mathrm{m\Omega}$ and $R_{\mathrm{on,TP_1}} + R_{\mathrm{on,TN_1}} = 115\,\mathrm{m\Omega}$ apply, even though, the maximum conductor density possible with the given design rules has been utilized. Tab. 3.3 also reveals that $R_{\mathrm{w+PDN},V_{\mathrm{in}\{2,4\}}}$ are substantially larger than $R_{\mathrm{w+PDN},V_{\mathrm{in}\{1,3\}}}$, which is due to longer conduction paths, since the supply pads, V_{in1} and V_{in2} in Fig. 3.2, are located close to phases 1 and 3. Similarly, the increased resistance of $R_{\mathrm{w+PDN,gnd}_2}$, as compared to $R_{\mathrm{w+PDN,gnd}_{\{1,3,4\}}}$, can be explained based on the arrangement of the ground pads, because, due to layout-specific restrictions, the top-side pad sequence is V_{m} – *dat* – gnd instead of V_{m} – gnd – *dat*, which causes a disturbance of the symmetry.

The subsequent measurement of the DC resistances is conducted with the setup shown in Fig. 3.8, which allows for an experimental characterization of the high-side and low-side conduction paths, depending on whether $\mathrm{TP}_{\{1,2\}}$ or

Tab. 3.3: Computed values of the resistances shown in Fig. 3.7.

Parameters	Symbol	Value (mΩ)
Values obtained from Cadence® simulations		
PMOS channel at $T_j = 85°C$	$R_{on,TP_{\{1,2\}}}$	115/2
PMOS, metal layers stack	$R_{met,P}$	18
NMOS channel at $T_j = 85°C$	$R_{on,TN_{\{1,2\}}}$	103/2
NMOS, metal layers stack	$R_{met,N}$	25
Values obtained from FastHenry computations		
Bond wires + PDN of V_{in} (converter phases 1 to 4)	$R_{W+PDN,V_{in\{1,2,3,4\}}}$	{145, 185, 145, 182}
Bond wires + PDN of v_x, high-side on (same for all phases)	$R_{W+PDN,v_x,hi}$	139
Bond wires + PDN of v_x, low-side on (same for all phases)	$R_{W+PDN,v_x,lo}$	100
Bond wires + PDN of gnd (converter phases 1 to 4)	$R_{W+PDN,gnd_{\{1,2,3,4\}}}$	{159, 197, 155, 155}

$TN_{\{1,2\}}$ conduct. Accordingly,

$$R_{dc,hi,\{1,2,3,4\}} \in \left[\frac{\min\left(V_{in,p} - v_{x\{1,2,3,4\}}\right)}{\max\left(I_{out}\right)}, \frac{\max\left(V_{in,p} - v_{x\{1,2,3,4\}}\right)}{\min\left(I_{out}\right)} \right] \text{ and} \tag{3.2}$$

$$R_{dc,lo,\{1,2,3,4\}} \in \left[\frac{\min\left(v_{x\{1,2,3,4\}}\right)}{\max\left(-I_{out}\right)}, \frac{\max\left(v_{x\{1,2,3,4\}}\right)}{\min\left(-I_{out}\right)} \right] \tag{3.3}$$

result for the high-side and low-side conduction paths, respectively. Fig. 3.9 depicts calculated and measured DC resistances (measured at an output current of 200 mA). Due to chip-internal leakage currents, which cause losses between 10 mW and 11 mW, slightly different DC resistances of the high-side conduction paths result, depending on whether the input or the output currents are used for the calculation. Calculated and measured resistances match well, which confirms the significant contribution of the PDN identified above.

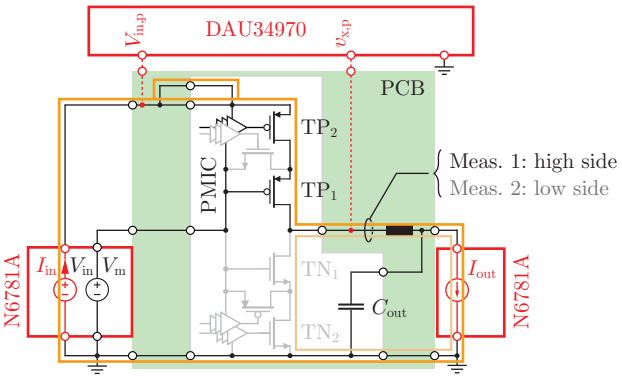


Fig. 3.8: Setup used to measure the DC resistances of high-side and low-side of a single converter phase; $v_{x,p}$ is the switching node of the measured phase, e.g., $v_{x1,p}$ in case of phase 1.

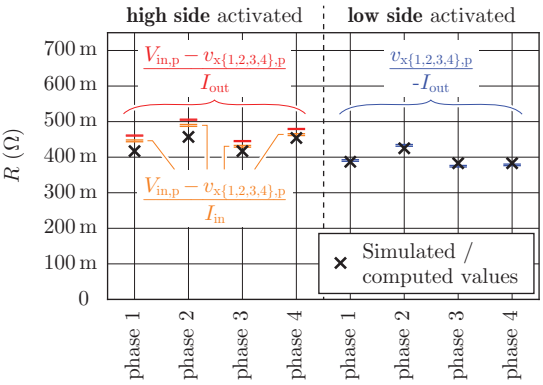


Fig. 3.9: Calculated and measured DC resistances of the four converter phases (measured at $I_{out} = 200\,mA$ and $T_{amb} = 20°C$); left: high-side resistances according to 'Meas. 1' in Fig. 3.8, right: low-side resistances according to 'Meas. 2' in Fig. 3.8. The high-side resistances are determined for input and output currents, revealing minor differences due to chip-internal leakage currents.

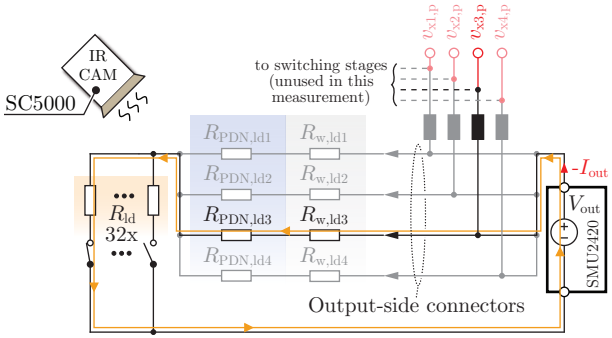


Fig. 3.10: Simplified equivalent circuit of the measurement setup used to identify the characteristic of power dissipation versus chip temperature for the example of a measurement at the load assigned to converter phase 3. The voltage at the switching node of the corresponding converter phase, i.e., v_{x3} in the depicted example, reveals the voltage that is present just outside the chip (similar to a Kelvin measurement).

3.2.2 Thermal Characterization

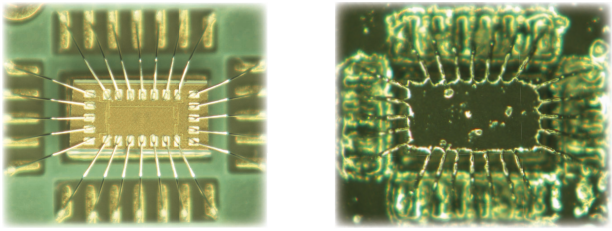
The relatively large resistance values of the chip-internal load enable an accurate electrical measurement of the losses in these resistors. Therefore, this load is utilized for the experimental characterization of the dependency of the chip temperature on the losses dissipated in the chip, using the measurement setup depicted in Fig. 3.10. During the thermal characterization, the transistors of the PMIC are turned off. All four loads have been utilized separately (not simultaneously).

Main measurement uncertainties are related to measurement accuracy and losses in the bond wires, because it is unclear, to what extent the losses in the bond wires contribute to heating up the chip. Accordingly, the respective power is within

$$P_{\text{heat}} \in \left[P_{\text{total}} - I_{\text{out}}^2 R_{\text{bw,eff}},\ P_{\text{total}}\right], \tag{3.4}$$

since only the current to the load, I_{out}, generates substantial losses in the bond wires; the implications of the losses in the bond wires due to the other currents, e.g., input and supply currents, are negligible. The total power includes the power levels at all ports (input, mid-point, output, supply of chip-internal digital components) and is determined with

$$P_{\text{total}} = V_{\text{in,p}} I_{\text{in}} + V_{\text{m,p}} I_{\text{m}} + V_{\text{d,p}} I_{\text{d}} + v_{\text{x,p}} I_{\text{out}}, \tag{3.5}$$



(a) (b)

Fig. 3.11: (a) Microscopic image of the PMIC chip; (b) microscopic image of the painted PMIC chip, using a high-emissivity black paint.

where $v_{x,p}$ denotes the voltage at the output node of the converter phase that corresponds to the tested internal load (e.g., $v_{x1,p}$ if load 1 is currently under test), since this node yields the most accurate measurement of the load voltage close to the PMIC (similar to a Kelvin pad). Aluminum wires with a length of 500 µm and a diameter of 20 µm realize the bond wires leading to a resistance of 42 mΩ. The input to every internal load is connected to the PCB via a single bond wire. The ground connection uses seven bond wires in parallel, however, due to the large resistance of the PDN, only a single bond wire may carry most of the return current through ground. Accordingly, based on a worst case assumption, the effective bond wire resistance may be up to

$$R_{\mathrm{bw,eff}} = 2 \times 42\,\mathrm{m\Omega} = 84\,\mathrm{m\Omega}. \tag{3.6}$$

Still, the uncertainty remains small, e.g., ±2.6 mW at a dissipated power of 170 mW and a load current of 250 mA.

With regard to the thermal measurements, the chip (cf. Fig. 3.11(a)) has been painted with high-emissivity black paint (cf. Fig. 3.11(b)) to achieve accurate results. In steady-state, the distributions of the surface temperatures are found to be similar for all considered excitations. Fig. 3.12 presents a thermal image of the chip that results if the load dissipates a power of 180 mW. The observed local areas of increased or reduced temperatures are linked to the layouts of top layer and PDN, e.g., reduced temperatures result at the pads. Further temperature gradients are found close to the edges of the chip, which, however, are far from the investigated chip-internal converter parts. The obtained result is different to what is found for chips used in high-power modules, where large temperature gradients may occur on the

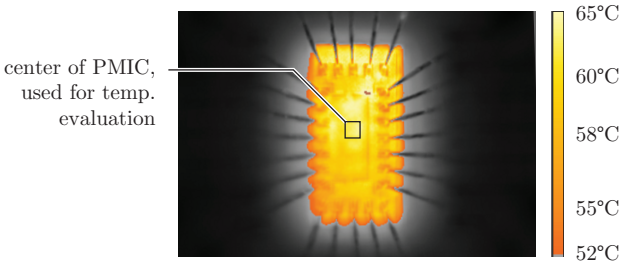


Fig. 3.12: Example of a thermal measurement of the load at a dissipated power of 178 mW. The temperature used for chip characterization is the mean value of the temperatures of 3×3 pixels in the center of the PMIC.

surface, e.g. in IGBTs as presented in [48], and is due to the comparably small chip volume and the placement of the chip on the PCB, providing thermal insulation. Due to these reasons and because the control circuitry, which generates only negligible losses, resides at the center of the chip, it is assumed that the losses in the on-chip load resistors and the converter phases have similar implications on the chip temperature at the center. Thus, the average temperature of 3×3 pixels in the middle of the chip is used as chip surface temperature, T_c, cf. Fig. 3.12. In the considered temperature range, the employed thermal camera, SC5000 (Flir), has an absolute accuracy of $\pm 1\,°C$. However, the presented setup uses the same camera and the same setup to identify the dependency of the chip temperature on the losses in a first step and to estimate the on-chip losses based on the chip temperature in a second setup that is conducted shortly after. Therefore, systematic errors are removed and only noise remains as a source of uncertainty for which an uncertainty equal to the standard deviation of $\pm 0.3\,°C$, typically found in the measurements, has been considered.

Fig. 3.13 depicts the experimental results for the power dissipation with respect to the difference between chip surface temperature and ambient temperature,

$$\Delta T_c = T_c - T_{amb}, \tag{3.7}$$

where the ambient temperature has been measured at the center of the chip prior to the load measurements and with no supply voltages being provided to the PMIC. The shown results have been obtained for different voltages at the load, ranging from 0.5 V to 0.85 V, and for each of the four load phases; the result reveals same temperature characteristics for all phases. With the known

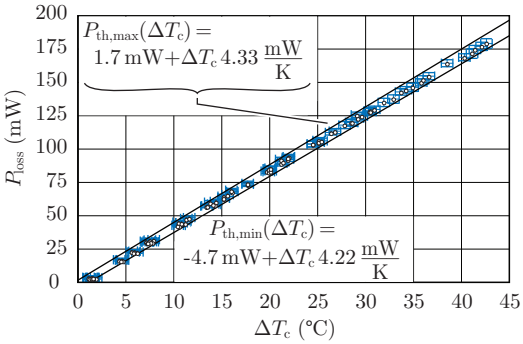


Fig. 3.13: Identified power dissipation characteristic with respect to chip temperature.

uncertainties of thermal and electrical measurements, the characteristics of upper and lower boundaries of the on-chip losses, which are found to be almost linear with respect to temperature, can be estimated using the bottom-right and the top-left corners of the uncertainty ranges of each measurement result. In this regard, a subsequent least mean square optimization yields

$$P_{\text{th,min}} = 4.22\,\frac{\text{mW}}{\text{K}}\Delta T_c - 4.7\,\text{mW}, \tag{3.8}$$

$$P_{\text{th,max}} = 4.33\,\frac{\text{mW}}{\text{K}}\Delta T_c + 1.7\,\text{mW}. \tag{3.9}$$

3.2.3 Efficiency Measurements and Loss Breakdown

With all four phases being operated, the IVR yields the losses and efficiencies presented in Fig. 3.14 for a voltage conversion ratio of

$$M = \frac{V_{\text{out,k}}}{V_{\text{in,k}}} = \frac{V_{\text{out,k}}}{1.6\,\text{V}} \approx 0.7 \tag{3.10}$$

and for three switching frequencies (50 MHz, 100 MHz, and 150 MHz). The total efficiency and the total losses,

$$\eta_{\text{IVR}} = \frac{P_{\text{out}}}{P_{\text{in}}}, \qquad P_{\text{loss,el}} = P_{\text{in}} - P_{\text{out}}, \tag{3.11}$$

are directly determined from the input and output power levels of the IVR measured with the setup of Fig. 3.5,

$$P_{\text{in}} = V_{\text{in,p}} I_{\text{in}}, \qquad P_{\text{out}} = V_{\text{out,k}} I_{\text{out}}. \tag{3.12}$$

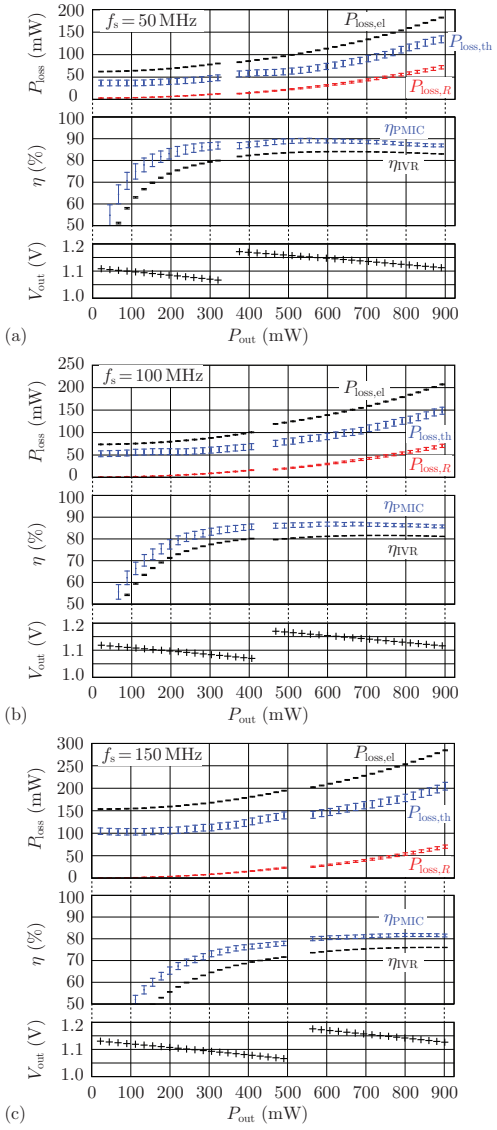


Fig. 3.14: Losses and efficiencies for $M = 0.7$ and two different switching frequencies: **(a)** $f_s = 50\,\text{MHz}$, **(b)** $f_s = 100\,\text{MHz}$, and **(c)** $f_s = 150\,\text{MHz}$; $P_{loss,el}$ and $P_{loss,th}$ denote the losses determined with electrical and thermal measurements, $P_{loss,R}$ refers to the resistive on-chip losses determined for the measured resistances of the PMIC's high-side and low-side current paths.

At the gaps observed in Fig. 3.14, e.g., at $P_{\text{out}} \approx 350\,\text{mW}$ in Fig. 3.14(a), the duty cycle is changed from 75 % (= 12/16) to 81 % (= 13/16) such that M remains close to 0.7.

The PMIC itself generates only a part of the total losses, which is determined from the chip temperature using (3.8), (3.9), cf. Fig. 3.13. Similar to Subsection 3.2.2, the uncertainty of the temperature measurement is set equal to the standard deviation found for the thermal measurements, which is ±0.3 °C,

$$P_{\text{loss,th}} \in \left[P_{\text{th,min}}(T_{\text{c}} - 0.3\,^{\circ}\text{C}), P_{\text{th,max}}(T_{\text{c}} + 0.3\,^{\circ}\text{C})\right]. \tag{3.13}$$

The depicted efficiency of the PMIC itself is calculated with

$$\eta_{\text{PMIC}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss,th}}}. \tag{3.14}$$

The on-chip losses, $P_{\text{loss,th}}$, can be further separated into a resistive loss component, $P_{\text{loss},R}$, and an additional loss component, $P_{\text{loss,add}}$, using the resistor network of Fig. 3.7 and the previously identified resistance values, cf. Subsection 3.2.1,

$$P_{\text{loss,th}} = P_{\text{loss},R} + P_{\text{loss,add}}, \tag{3.15}$$

where $P_{\text{loss},R}$ is calculated with the DC resistances, (3.2) and (3.3), and the currents through the high-side and low-side paths for all enabled converter phases, N (e.g., $N = 4$ applies in Fig. 3.14 and Fig. 3.15),

$$P_{\text{loss},R} = \sum_{n=1}^{N} \left(R_{\text{dc,hi},n} I_{\text{hi,rms}}^2 + R_{\text{dc,lo},n} I_{\text{lo,rms}}^2\right); \tag{3.16}$$

$I_{\text{hi,rms}}$ and $I_{\text{lo,rms}}$ are determined based on inductor rms current, $I_{L,\text{rms}}$, and duty cycle, D,

$$I_{\text{hi,rms}} = I_{L,\text{rms}}\sqrt{D}, \qquad I_{\text{lo,rms}} = I_{L,\text{rms}}\sqrt{1-D}, \tag{3.17}$$

using

$$I_{L,\text{rms}}^2 = \left(\frac{I_{\text{out}}}{N}\right)^2 + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2, \; \Delta I_L = \frac{V_{\text{out,k}}(1-D)}{f_{\text{s}} L}. \tag{3.18}$$

The additional loss component, $P_{\text{loss,add}}$, is the sum of switching losses, losses due to leakage currents, increased losses due to eddy current effects inside

the chip (Skin and Proximity effects), and power dissipation in the digital control circuitry. The calculation of the AC resistances of the PDN with FastHenry gives a negligible increase at the considered switching frequencies, due to the small physical dimensions, the losses due to leakage identified in Subsection 3.2.1 are in the range of 10 mW, and the power demand of the control circuitry is approximately 1 mW. For these reasons, it can be assumed that the resistive losses and the additional losses mainly resemble the conduction losses and the switching losses, respectively,

$$P_{\text{loss,cond}} \approx P_{\text{loss},R}, \qquad P_{\text{loss,sw}} \approx P_{\text{loss,add}}, \tag{3.19}$$

The results reveal that the losses in the PMIC typically contribute to more than two thirds of the total losses of the IVR and that the additional loss component increases if the switching frequency is increased, which confirms (3.19). In addition, also the off-chip losses,

$$P_{\text{loss,off-chip}} = P_{\text{loss,el}} - P_{\text{loss,th}}, \tag{3.20}$$

which contain the losses of inductor and PCB,[2] increase for increasing switching frequencies. At $f_s = 50$ MHz, the IVR achieves a maximum efficiency of 84.1 % at $P_{\text{out}} = 640$ mW. With respect to the active chip area of the power stages of all four phases (0.0324 mm^2), this efficiency is achieved at a chip current density of 17.3 A/mm^2. At full load, $P_{\text{out}} = 890$ mW (corresponding to a chip current density of 24.7 A/mm^2), the efficiency is 83.0 %. The maximum efficiency of the PMIC is in the range $\eta_{\text{PMIC,max}} \in [88\,\%, 90\,\%]$ at $f_s = 50$ MHz and output power levels between 500 mW and 600 mW; the corresponding full-load efficiency of the PMIC is between 86.3 % and 87.6 %. Please note that an increased range of uncertainty results for $\eta_{\text{PMIC,max}}$, compared to the electrically measured efficiency, due to the increased uncertainty of the thermal measurement.

Fig. 3.15 depicts the ranges of conduction losses, switching losses, and off-chip losses for full-load operation with $P_{\text{out}} = 0.9$ W, $M \approx 0.7$, and two different switching frequencies, i.e., $f_s = 50$ MHz in Fig. 3.15(a) and 150 MHz in Fig. 3.15(b), in order to provide a more detailed view on the three loss components. The shaded areas denote the uncertainty ranges that result for the available measurement data at the considered operating points, cf. Fig. 3.14. For $f_s = 50$ MHz, the range of the resistive losses, $P_{\text{loss},R} \in [68\,\text{mW}, 76\,\text{mW}]$, is similar to the range of the additional losses, $P_{\text{loss,add}} \in [51\,\text{mW}, 73\,\text{mW}]$. In

[2] A separation of the off-chip losses into the losses of inductor and PCB would require a detailed characterization of the high-frequency inductor losses in presence of DC bias.

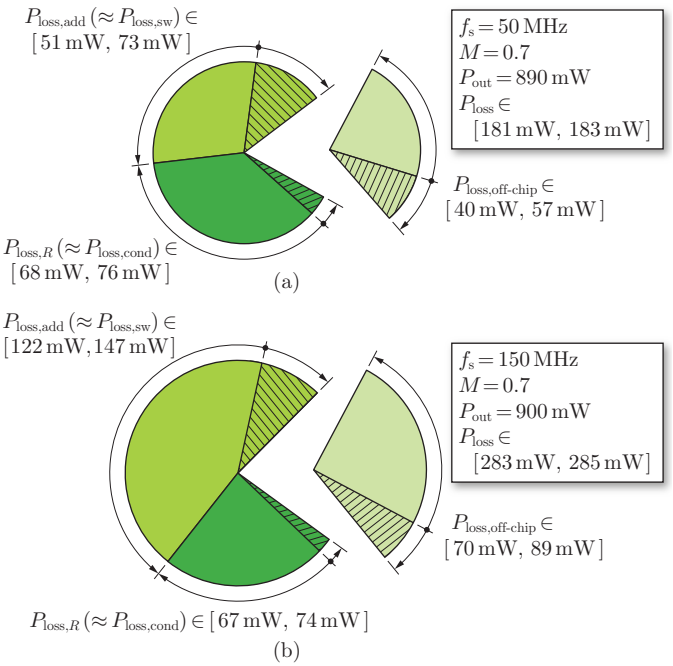


Fig. 3.15: Breakdown of the losses of the IVR for two different switching frequencies based on the data shown in Fig. 3.14, for an output power of 0.9 W, and two different switching frequencies: (a) $f_s = 50$ MHz, (b) $f_s = 150$ MHz; $P_{\text{loss,ac}} = P_{\text{loss,th}} - P_{\text{loss,dc}}$ and $P_{\text{loss,off-chip}} = P_{\text{loss,el}} - P_{\text{loss,th}}$ apply. The result reveals that an increase of the switching frequency leads to increased AC losses on the chip (switching losses, AC conduction losses) and increased off-chip losses (e.g., in the inductor).

contrast, for $f_s = 150$ MHz, the additional losses, $P_{\text{loss,add}} \in [122\,\text{mW}, 147\,\text{mW}]$, are approximately twice the resistive losses ($P_{\text{loss},R} \in [67\,\text{mW},\ 74\,\text{mW}]$).

In order to clarify the origin of the additional losses, a detailed simulation has been realized for converter phase 1. This simulation includes the parasitic components of metal layers 1 to 10 and models the parasitics of PDN and PCB with the simplified network depicted in Fig. 3.16, cf. [47]. The values of the presented parasitic inductances and resistances of PDN and PCB have been computed with FastHenry. Fig. 3.17 depicts the waveforms of the chip-internal input voltage of the half bridge of converter phase 1, V_{dd}, and the voltage at the corresponding chip-internal switching node, v_{x1}, determined with the

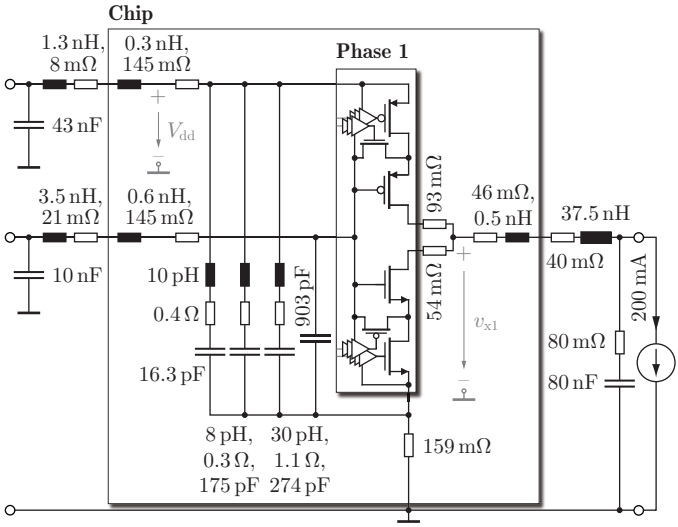


Fig. 3.16: Network used to model the parasitic components of PCB, bond wires, and PDN for the detailed simulation of converter phase 1. The framed block 'Phase 1' refers to a detailed simulation model that takes further parasitic components introduced by metal layers 1 to 10 into account.

detailed simulations and for three different switching frequencies of 50 MHz, 100 MHz, and 150 MHz. According to the obtained results, the additional parasitic components lead to several unwanted effects, e.g., increased turn-on and turn-off times and oscillations superimposed on supply voltages, output voltages, and output currents. Compared to the results of simplified Cadence® simulations that do not take the output current ripple and the parasitic components introduced by metal layers, PDN, bond wires, and PCB into account, as presented in Chapter 2, these parasitic components are indeed the main reason for the increased losses, in particular at high output currents, cf. Fig. 3.18. Remaining differences between simulated and measured losses are of relatively low value and may be reproduced by even more detailed simulations, e.g., the measured losses at $f_s = 50$ MHz are found to be larger than expected, which may originate from additional resonance effects in PCB and PDN.

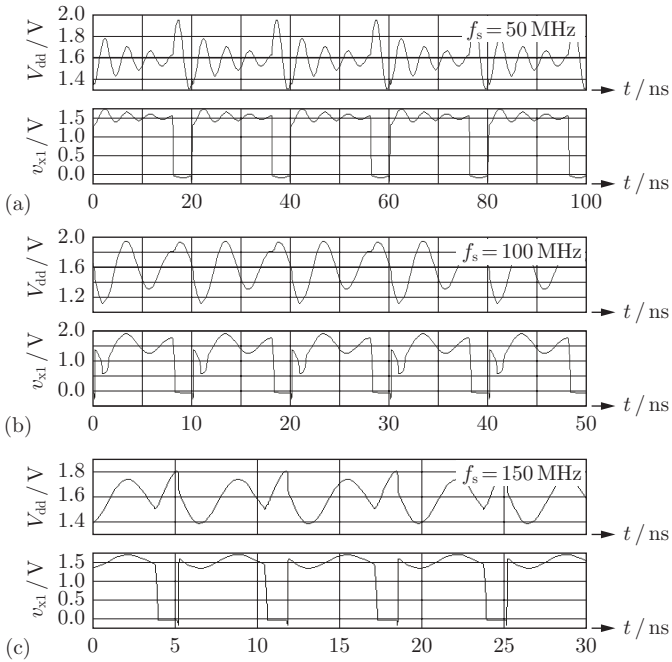


Fig. 3.17: Waveforms of the supply voltage and the voltage at the switching node of converter phase 1, V_{dd} and v_{x1}, cf. Fig. 3.16, obtained from a detailed Cadence® simulation and for different switching frequencies: (a) $f_s = 50$ MHz, (b) $f_s = 100$ MHz, (c) $f_s = 150$ MHz.

3.3 Experimental Evaluation of the CMOS HBST Topologies

According to the findings of Chapter 2, the CMOS ANPC HBST with ICS is expected to achieve a higher efficiency than the conventional CMOS HBST and the conventional CMOS ANPC HBST. For this reason, the focus of the previous Section has been mainly on the CMOS ANPC HBST with ICS. In order to complement the theoretical findings of Chapter 2 by experimental results, this Section presents an experimental evaluation of all three topologies, which comprises of the three investigated items listed below.

- Subsection 3.3.1: Characteristic of the ratio of output voltage to input voltage as a function of duty cycle and output current.

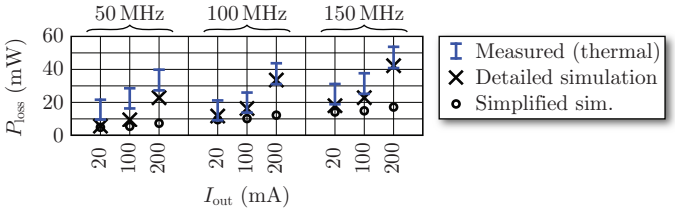


Fig. 3.18: Comparison of the losses of converter phase 1, determined with simplified and detailed simulations, to the measured on-chip losses. In contrast to the detailed simulation, cf. Fig. 3.16, the simplified simulation does not take parasitic components into account (e.g., due to metal layers, PDN, etc.), cf. Chapter 2. The depicted outcome reveals a substantial contribution of these parasitic components on the obtained losses; especially at high output currents, e.g., $I_{\text{out}} = 200\,\text{mA}$, these are mainly responsible for the differences between the results determined with simplified simulations and measurements.

- Subsection 3.3.2: Experimental characterization of the dependency of efficiency on the dead times.
- Subsection 3.3.3: Comparative evaluation of the efficiencies measured for the conventional HBST and the ANPC HBST, for different output currents, duty cycles, and switching frequencies.

Except for the last paragraph of Subsection 3.3.3, the presented investigations are confined to the first converter phase of the four-phase IVR. The measurements have been conducted according to Subsection 3.2.3, using the measurement setup depicted in Fig. 3.5(a).

3.3.1 Output Voltage Characteristic

The measured ratios of output voltage to input voltage, M, cf. (3.10), for the HBST and the ANPC HBST with ICS at $f_{\text{sw}} = 50\,\text{MHz}$ and $f_{\text{sw}} = 150\,\text{MHz}$ are depicted in Fig. 3.19(a) and Fig. 3.19(b), respectively. In most operating regions, $M(D, I_{\text{out}})$ is proportional to the duty cycle, D. However, at a switching frequency of 150 MHz and an output current of $I_{\text{out}} = 260\,\text{mA}$, M of the HBST is non-linear for $D \in [50\%, 80\%]$, which is similar to the result obtained in [49]. This is presumably due to an unstable chip-internal supply voltage of the HBST and was solved in [49] by using a capacitive interposer that reduces the parasitic inductances between on-chip and off-chip buffer capacitors. The ANPC HBST with ICS is more robust in this regard, i.e., M remains

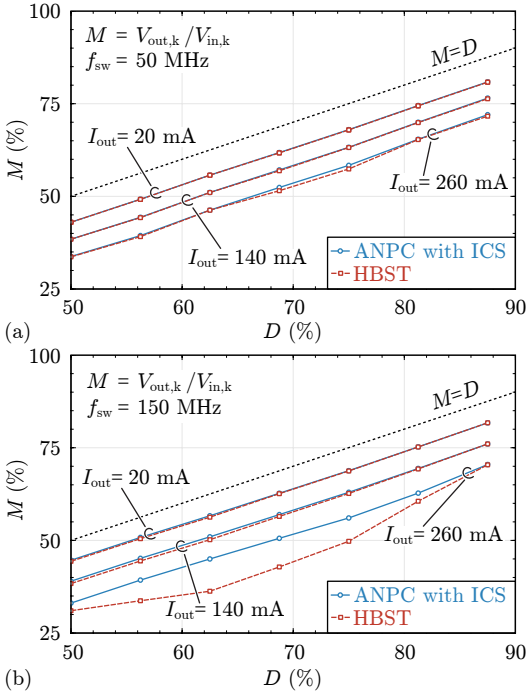


Fig. 3.19: Measured conversion ratio, M, of the PCB-attached IVR (f_{sw} = 150 MHz).

proportional to D, since the clamping switch TP_3 can take over a part of the excess current in the commutation loop during the rising edge of the switched voltage, $v_{x,1}$; cf. Fig. 2.8(a) ② (HBST) and Fig. 2.8(a) ③ (the peak of $i_{d,TP2}$ decreases from 3.2 A to 2.5 A). This leads to a reduction of the current peaks in the on-chip input capacitor that is connected between $V_{in1,2}$ and ground.

3.3.2 Impact of Dead Times on Efficiency

The characteristics of the converter efficiencies with respect to the dead times $dt_{\downarrow}$ and $dt_{\uparrow}$ are shown in Fig. 3.20(a),(b), respectively. The general characteristics depicted in Fig. 3.20(a) are similar to the simulated characteristics shown in Figure 2.10; however, the absolute values of the measured efficiencies are substantially lower, due to the additional conduction losses in the

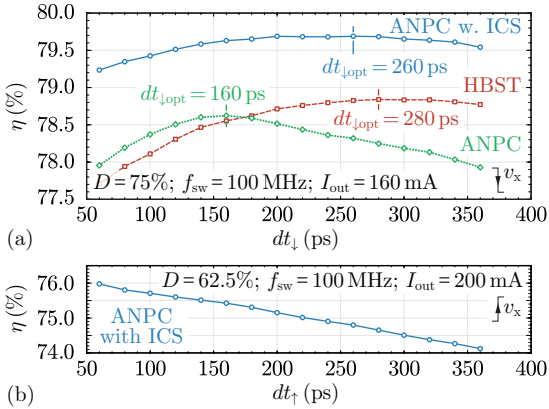


Fig. 3.20: Impact of dead times on efficiency. (**a**) Efficiencies of the considered topologies for different dead times during the falling edge of $v_{x,1}$ and (**b**) during the rising edge of $v_{x,1}$.

PDN and the metal layers of the chip. These relatively high conduction losses are inherent to the employed 14 nm CMOS technology, since PDN and metal layers use very thin conductors, cf. Subsection 3.2.1. With regard to a falling edge of $v_{x,1}$, maximum efficiency is obtained for $dt_\downarrow = dt_{\downarrow,opt}$. For a rising edge, the minimum possible dead time leads to the highest efficiency, since any increase of $dt_\uparrow$ increases the conduction losses during the dead time. The conventional ANPC HBST (without ICS) achieves only a comparably low maximum efficiency. For this reason, the efficiency evaluation given in the next Subsection considers only the HBST and the ANPC HBST with ICS.

3.3.3 Efficiency Results

The efficiencies measured for optimal dead times, different input-to-output voltage ratios

$$M_p = \frac{V_{out,k}}{V_{in,p}} = \{0.5,\ 0.7\}, \tag{3.21}$$

and for $f_{sw} = \{50\,\text{MHz},\ 150\,\text{MHz}\}$ are presented in Fig. 3.21.[3] Due to the internal resistances of the IVR, the output voltage decreases with increasing

[3]Section 3.2 describes how the measurement uncertainties shown in Fig. 3.21 have been calculated.

output current. Furthermore, the duty cycle is subject to 16 discrete values, as explained in Subsection 3.1.1. Accordingly, steps are observed in the measured efficiencies whenever the duty cycle is changed in order to adjust the output voltage such that the output voltage remains within a certain tolerance band. For example, the duty cycle is increased from 12/16 to 13/16 if I_{out} is increased from 260 mA to 280 mA at $M_{\text{p}} = 0.7$ in Fig. 3.21(a).

A single converter phase achieves a peak efficiency of 83.7 % at $f_{\text{sw}} = 50\,\text{MHz}$ and $I_{\text{out}} = 160\,\text{mA}$. The efficiency could be improved with advanced packaging technologies, e.g., flip-chip bonding of the chip to an interposer that contains the inductors and the capacitors. At high output currents, the results reveal a higher efficiency for the ANPC HBST with ICS, which indicates a possible relation between an increase of the losses of the HBST and the non-linear dependency of the output voltage on the duty cycle at high output currents; cf. Fig. 3.19. The efficiency increases by up to 3 % in the case of $M_{\text{p}} = 0.5$ and $f_{\text{sw}} = 50\,\text{MHz}$ and by up to 7 % for $M_{\text{p}} = 0.5$ and $f_{\text{sw}} = 150\,\text{MHz}$.

Finally, the measured efficiency with phase-shedding is depicted in Fig. 3.22 for the ANPC HBST with ICS and a total output current that ranges from zero to 780 mA ($V_{\text{in}} = 1.6\,\text{V}$, $M_{\text{p}} \approx 0.7$ and $f_{\text{sw}} = 50\,\text{MHz}$ apply; the observed steps in the efficiency are related to the change of the discrete duty cycle to maintain $M_{\text{p}} \approx 0.7$). The result reveals the great efficiency improvements that are feasible with phase shedding if the IVR is operated at reduced output power levels. By way of example, at $I_{\text{out}} = 140\,\text{mA}$, the efficiency increases from 72 % (four active converter phases) to 80 % (two active phases) to 83.4 % if only a single converter phase is active. The maximum achieved efficiency is 85.3 % for two active phases, and $I_{\text{out}} = 300\,\text{mA}$; at a maximum output current of 780 mA, the efficiency is 83.1% (for all four phases being active).

3.4 Summary

This chapter presents a detailed characterization of an inductor-based four-phase buck converter featuring CMOS APNC HBST, which is supported by the results of detailed simulations and extensive experiments, and an experimental evaluation of the conventional CMOS HBST, the conventional CMOS ANPC HBST, and the CMOS ANPC HBST with ICS. The investigated converter uses a PMIC assembled in a 14 nm CMOS technology node and allows for operation with switching frequencies between 50 MHz and 150 MHz. Its implemented open-loop circuitry allows for configurable dead times,

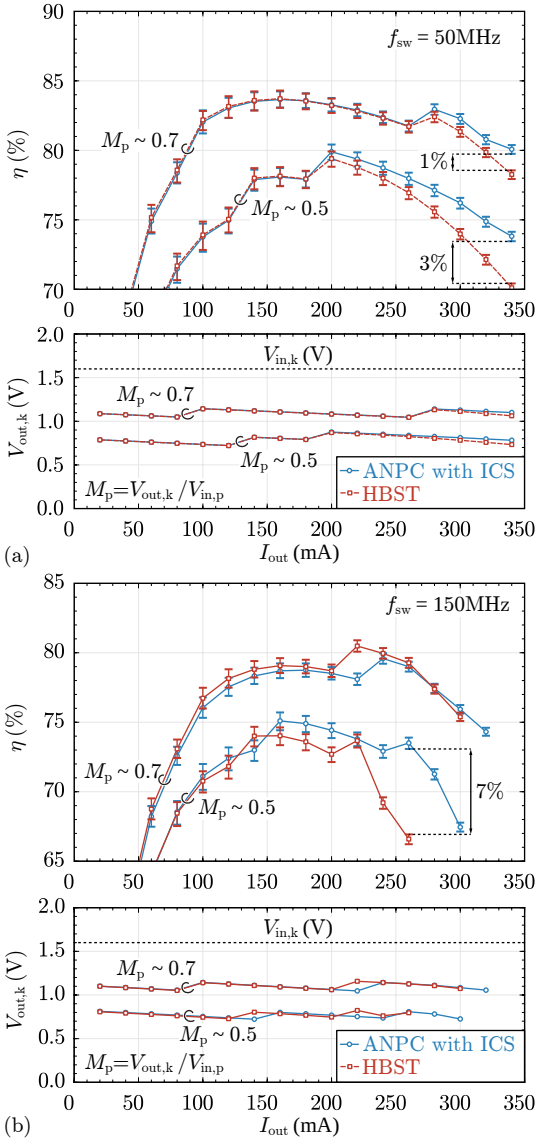


Fig. 3.21: Measured efficiencies and output voltages of the PCB-attached IVR: (a) f_{sw} = 50 MHz, (b) f_{sw} = 150 MHz.

Tab. 3.4: Performance and design values of the investigated ANPC HBST IVR in comparison to previously presented converters.

	This work	C.Schaef et al. [17]	H. K. Krishnamurty et al. [14]	H. K. Krishnamurty et al. [15]	E. A. Burton et al. [16]	F. Neveu et al. [19]	N. Sturcken et al. [21]
Techn. node PMIC (nm)	**14**	14	14	14	22	40	45
Peak efficiency (%)	**84.1**	88	84 (for on-die induct.)	80	90	91.5	75
Max. curr. density (A/mm^2)*	**24.7**	10.7	–	–	31	6.3	22.7
Input voltage (V)	**1.6**	1.6	1.5	1.2	1.7	3.3	1.8
Conv. ratio M at peak efficiency	**0.7**	0.75	0.77	0.77	0.62	0.73	0.67
HB topology	**ANPC**	stacked trans.	stacked trans.	stacked trans.	stacked trans.	stacked trans.	single trans.
Switching freq. (MHz)	**50**	70	100	90	140	100	up to 200
Inductor value L (nH)	**36**	2.5	1.5 or 22**	4.8	–	60	12.5
Inductor technology	**discrete**	on-package	on-die or ext.	on-die	on-package	discrete	silicon interp.
Inductor packaging	**bond-wire**	flip-chip	– / on-probe	_	flip-chip	flip-chip	flip-chip
Number of phases	**4**	1	2	2	16	1	8

* Defined as the maximum output current of the IVR divided by the area of the enabled power switches, gate drivers, and level shifters. This value was calculated using information found in the corresponding publications.

** Two realizations are presented, with on-die and with external inductor.

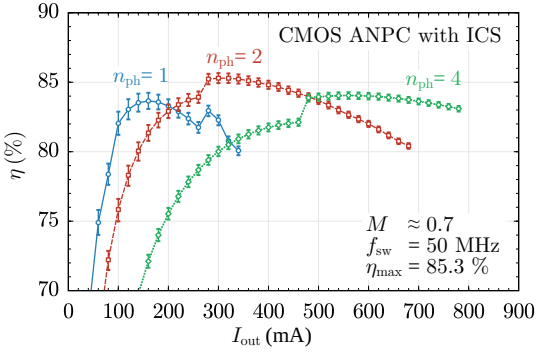


Fig. 3.22: Efficiencies measured for the ANPC HBST with ICS topology for one, two, or four phases being operational ($V_{in,k}$ = 1.6 V, $M_p \approx 0.7$, f_{sw} = 50 MHz).

to optimize switching losses, and realizes output stages that are capable of being deactivated, in order to facilitate phase-shedding, i.e., operation of a reduced number of converter phases, to increase the achieved efficiency at lower output power levels. With a FEOL chip area of only 0.0081 mm^2 for each phase of the four-phase converter, a very compact design has been achieved, consuming only a small amount of valuable chip area.

In order to gain detailed insights into the investigated IVR, the presented converter characterization consolidates the results of electrical measurements, thermal inspections of the chip surface, and simulations, which enables the separation of the total losses into on-chip and off-chip loss components as well as the allocation of important loss components inside the chip. In summary, and with all four phases being operational, the IVR achieves a maximum efficiency of 84.1 % at P_{out} = 640 mW and f_s = 50 MHz and a maximum full-load efficiency of 83.0 % at P_{out} = 890 mW with a corresponding chip current density of 24.7 A/mm^2. The maximum efficiency of the PMIC itself is between 88 % and 90 % for $P_{out} \in [500\,\text{mW}, 600\,\text{mW}]$. The results of Section 3.2 reveal that PDN and metal layers cause a considerable increase of the total losses, e.g., a simulation of the PMIC without PDN and metal layers reveals losses of only 30 mW at f_s = 100 MHz and P_{out} = 0.9 W; however, the corresponding measured losses of the PMIC are in the range between 140 mW and 156 mW, which can be reproduced with detailed simulations. Furthermore, the measured experimental results confirm that the combination of appropriate software tools, e.g., Cadence® to conduct detailed post-layout

circuit simulations and FastHenry to identify the impedances of PDN and PCB, enables a prediction of the expected losses with reasonable accuracy.

The comparative evaluation of the three investigated topologies, presented in Section 3.3, confirms the beneficial properties of the CMOS ANPC HBST with ICS with regard to high efficiency and robust operation. However, the CMOS ANPC HBST with ICS requires 14 % more chip area than the conventional HBST. With the use of phase-shedding, a maximum efficiency of 85.3 % is measured if only two phases are operational, for an output current of 300 mA and a switching frequency of 50 MHz.

Tab. 3.4 lists the performance and design values of the realized ANPC IVR and provides a comparison to previously presented results. The achieved maximum current density of the realized PMIC is amongst the highest documented values, however, the peak efficiency of 84.1 % is below the maximum documented efficiency of 91.5 %. According to Tab. 3.4, the efficiency of the IVR can be increased with advanced packaging technologies, e.g., flip-chip bonding of the PMIC on an interposer that provides the inductors and the capacitors. In addition, Tab. 3.4 indicates a trend that more mature CMOS technology nodes, e.g., 22 nm or 40 nm, enable the realization of more efficient IVRs. This trend matches the results of prior realizations with more mature CMOS nodes, where the losses in the PDN and metal layers have been relatively low, and the findings of this paper, which reveal substantial losses, there, due to the small values of maximum widths and thicknesses defined by the design rules. Therefore, even higher losses in the PDN and the metal layers would be expected in case of higher-integrated, e.g., 7 nm, CMOS nodes [50]. Accordingly, future research should also focus on alternative solutions that do not require a direct integration of the PMIC on the CPU die, e.g., 3-D realizations using chiplets [51], which extends the current design space with respect to system complexity, efficiency, and costs.

4 Conclusion and Outlook

The substitution of conventional PoL VRs located on the motherboard of microprocessor systems by IVRs is essential to enable the sustainable increase of microprocessors' computational performance and applications. DVFS and granularity of VDs require that the IVRs are located close to the microprocessor and provide very fast response to load changes. Furthermore, in a small silicon footprint area is important to limit the additional costs. High efficiency, power density, and full silicon integration are, therefore, essential requirements of IVRs for modern microprocessor applications. In Chapter 3, this thesis presented the characterization of an IVR demonstrator that uses discrete inductors and capacitors soldered to a PCB. In this chapter, the thesis reveals the experimental results obtained for a two-phase buck converter whose inductors and capacitors are embedded in a silicon interposer. Both realizations employ a PMIC realized in a 14 nm CMOS technology. The key contributions of this thesis are summarized in Section 4.1. The demonstration of the 2.5-D all-silicon IVR is presented in Section 4.2 to show the feasibility and benefits of using the designed PMIC with a silicon interposer containing the passive devices. Finally, an outlook to future research areas related to IVRs is presented in Section 4.3.

4.1 Hybrid IVRs for Microprocessor Applications

IVRs utilized in modern microprocessor applications feature HB topologies with stacked transistors to take advantage of the more efficient short-channel devices of the latest CMOS technology nodes. In Chapter 2, a comparative evaluation between a proposed ANPC-type HBST topology with ICS, the

ANPC HBST, and the HBST is presented. The comparison is based on an in-depth examination of the transistors' current and voltage waveforms. The results of the analysis allows for the generation of a loss breakdown of the HBs. The proposed ANPC HBST with ICS has ZVS capabilities, balances the blocking voltages across the transistors, and is able to operate with phase-shedding. In this context, the ANPC HBST with ICS outperforms both, the conventional HBST (unequal voltages across the stacked transistors occur) and the conventional ANPC HBST (no ZVS, phase-shedding not feasible). Simplified Cadence® simulations show that the proposed ANPC HBST with ICS can achieve a maximum efficiency of 93.1%. However, these simulations do not take into account the parasitic components of the majority of the chip metal stack, PDN, and package. Therefore, a more complete simulation and verification with experimental results has been carried out and shown in Chapter 3.

To experimentally characterize the efficiencies of the investigated HBs, a versatile PMIC that can generate the gate signal patterns for the HBST, ANPC HBST, and the ANPC HBST with ICS has been designed and implemented in 14 nm CMOS technology. It allows for operation with switching frequencies ranging from 50 MHz to 150 MHz, configurable dead-times and phase-shedding. In case of the hybrid four-phase PCB-based IVR (realized with discrete inductors and capacitors) presented in Chapter 3, this work employs a novel characterization methodology to separate the on-chip losses from the off-chip losses. This methodology is based on post-layout simulations, electrical measurements, and a temperature measurement of the chip surface. Measurements of the DC resistances of all phases are used to separate the on-chip AC losses from the DC losses. The losses determined with the simplified simulations of Chapter 2 and the detailed post-layout simulations are compared to the losses measured with the novel characterization methodology. The comparison demonstrated a good agreement between the losses calculated in the post-layout simulations and the measured losses for a wide range of switching frequency and output power. The simplified simulations are found to be accurate at low power where the total losses are predominantly switching losses.

The implemented PCB-based IVR achieves a peak efficiency of 84.1 % at $P_{\text{out}} = 640\,\text{mW}$ and $f_{\text{s}} = 50\,\text{MHz}$ and a maximum full-load efficiency of 83.0 % at $P_{\text{out}} = 890\,\text{mW}$ with a corresponding chip current density of $24.7\,\text{A/mm}^2$. Compared to the state-of-the art IVRs in 14 nm technology the presented demonstrator achieves similar efficiencies with approximately twice the chip current density. Compared to older technology nodes, the IVRs

built with 14 nm achieve lower efficiencies. The loss breakdown presented in Fig. 3.15(a) reveals that, at full output power and a switching frequency of 50 MHz, approximately half of the on-chip losses are due to conduction losses, and at least half of the chip conduction losses are due to the resistances of the package bond-wires and the PDN. This work also verifies that the bond-wires introduce parasitic inductances that limit the maximum output power of an IVR by causing voltage oscillations at the interconnection nodes (a similar finding has been described in [49]). Due to the verified significant impact of the package parasitics on the efficient and stable operation of an IVR, 2.5-D all-silicon IVRs are also investigated in this work and are presented in the next section.

4.2 2.5-D All-Silicon IVR Demonstrator

According to Section 3.3.1, the PCB-based IVR did not achieve a linear relationship between duty cycle and output voltage at high output power when operated as conventional HBST, which is presumably due to increased voltage ringing at the input node at high output currents that is caused by parasitic inductances of the package. To reduce these parasitic inductances, a 2.5-D all-silicon IVR is proposed, i.e., the same PMIC of Fig. 3.2 is flip-chip bonded to a silicon-based interposer that integrates deep-trench input and output capacitors and two air-core spiral inductors.[1] This setup features much shorter paths between the input capacitors (on the interposer) and the HBs inside the PMIC than the PCB-based IVR.

4.2.1 Characterization of the 2.5-D All-Silicon IVR

The 2.5-D IVR is shown in the microscopic picture of Fig. 4.1. Air-core spiral inductors of $L_{\{2,4\}} = 12$ nH are bonded to the HBs' switching nodes of phases 2 and 4 of the PMIC. Deep-trench capacitors (manufactured by IPDiA ®) of 80 nF are connected to the input and output nodes. Fig. 4.2 depicts the employed experimental setup used for efficiency measurements and to measure the DC resistances of the IVR. All measurements are conducted with the high-accuracy equipment listed in Tab. 3.2. The probing is done using picoprobes of GGB ® as shown in the microscope picture of Fig. 4.3.

[1] In addition, a second all-silicon demonstrator has been realized, whose interposer contained the capacitors and coupled race-track inductors. However, due to a miscommunication between two external companies only packaged chips from wafers with fabrication defects were delivered. For this reason, this second all-silicon demonstrator could not be tested.

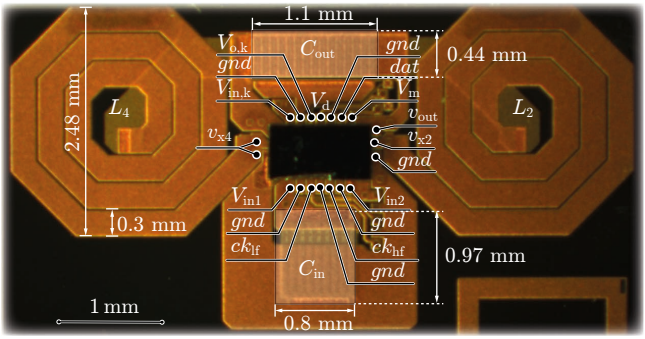


Fig. 4.1: 2.5-D all-silicon IVR with spiral air-core inductors and deep-trench capacitors embedded in the interposer.

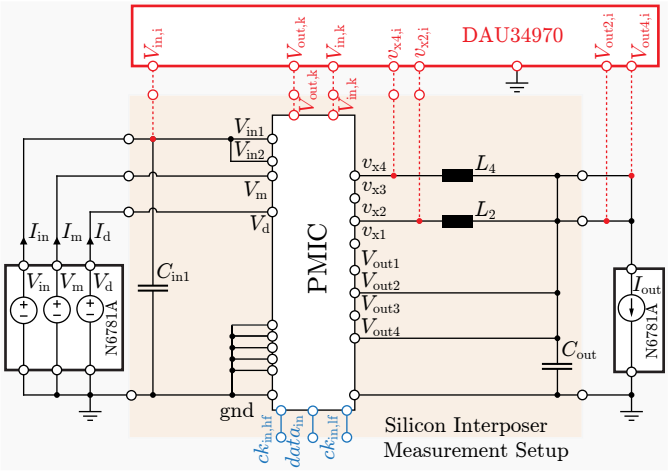


Fig. 4.2: Measurement setup used for the loss characterization and the efficiency measurements of the 2.5-D all-silicon IVR.

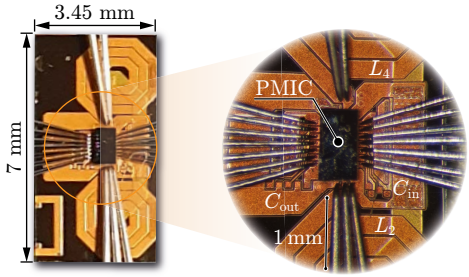


Fig. 4.3: Details of the probed 2.5-D all-silicon IVR.

The IVR's low- and high-side resistances are measured for phase 2 in a similar way as depicted in Fig. 3.8. The measured high-side resistance when $\mathrm{TP}_{\{1,2\}}$ are on and $\mathrm{TN}_{\{1,2\}}$ are off is, therefore,

$$R_{\mathrm{dc,hi,2}} = \frac{\left(V_{\mathrm{in,i}} - v_{\mathrm{x2,i}}\right)}{-I_{\mathrm{out}}} = 678\,\mathrm{m\Omega}. \tag{4.1}$$

The measured low-side resistance when $\mathrm{TN}_{\{1,2\}}$ are on and $\mathrm{TP}_{\{1,2\}}$ are off is

$$R_{\mathrm{dc,lo,2}} = \frac{\left(v_{\mathrm{x2,i}}\right)}{-I_{\mathrm{out}}} = 700\,\mathrm{m\Omega}. \tag{4.2}$$

The measured high- and low-side DC resistances of phase 2 are roughly twice the resistances measured for the PCB-based IVR as depicted in Fig. 3.9. The increased resistance values are attributed to the interconnects between the chip and the interposer, due to a failure in the flip-chip bonding. Accordingly, a reduction of the achieved IVR efficiencies compared to the PCB-based IVR is expected.

Fig. 4.4 presents the efficiency characterization of the 2.5-D all-silicon IVR calculated with (3.11). In ANPC with ICS mode of operation, an output voltage to input voltage ratio of 0.7, and for phase 2 being active, the demonstrator achieves a maximum efficiency of 77.7 % at $I_{\mathrm{out}} = 180\,\mathrm{mA}$ and $f_{\mathrm{s}} = 100\,\mathrm{MHz}$ and a maximum full-load efficiency of 73.4 % at $I_{\mathrm{out}} = 260\,\mathrm{mA}$. In HBST mode of operation, the IVR achieves a slightly lower maximum efficiency of 76.7 % at $I_{\mathrm{out}} = 140\,\mathrm{mA}$.

The measured ratios of output voltage to input voltage,

$$M = \frac{V_{\mathrm{out,k}}}{V_{\mathrm{in,k}}}, \tag{4.3}$$

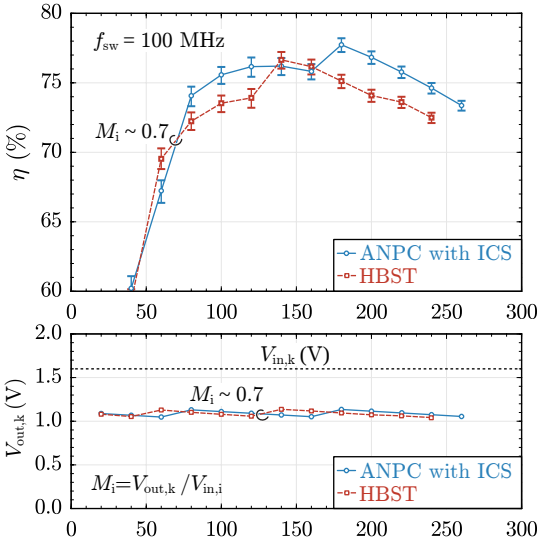


Fig. 4.4: Measured efficiencies and output voltages of the 2.5-D all-silicon IVR at f_{sw} = 100 MHz, an output voltage to input voltage ratio of 0.7, and for phase 2 being active.

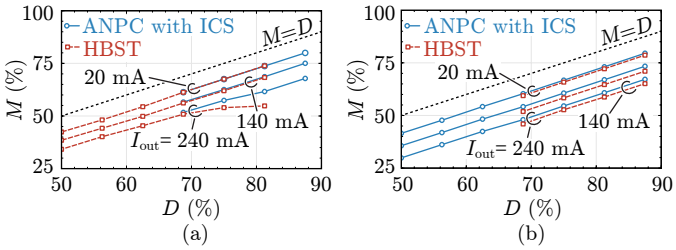


Fig. 4.5: Measured conversion ratio, M, at 100 MHz of (**a**) the PCB-based IVR of Fig. 3.5 and (**b**) the 2.5-D all-silicon IVR of Fig. 4.1. The 2.5-D all-silicon IVR can maintain the linearity of its output voltage regulation independently of the HB topology.

for the HBST and the ANPC HBST with ICS (with only phase 2 enabled) at $f_{sw} = 100\,\text{MHz}$ are depicted in Fig. 4.5(a) for the PCB-based IVR and in Fig. 4.5(b) for the 2.5-D all-silicon IVR. In most operating regions of Fig. 4.5(a), $M(D, I_{out})$ is proportional to the duty cycle, D. However, at an output current of $I_{out} = 240\,\text{mA}$, M of the HBST is non-linear for $D \in [70\%, 80\%]$ for the PCB-based IVR. The 2.5-D all-silicon IVR maintains the proportionality of $M(D, I_{out})$ to the duty cycle, D, independent of the emulated topology at all tested output currents. The increased value of input capacitance and the reduced package inductances are contributing to the mitigation of the voltage oscillations at the input node.

4.3 Outlook and Future Research Areas

Due to market performance demands, the semiconductor industry is subject to continuous improvement which also impacts the IVRs technologies. This section presents the expected critical technologies that aim to improve the performance of IVRs in modern microprocessor applications.

4.3.1 Novel Transistor Technologies

The transistors' sizes are still systematically reducing in modern CMOS technologies: currently, industry is using nodes with transistors featuring 14 nm, 7 nm and 5 nm nm CMOS gate length. In this thesis, an advanced 3-D FinFET transistor technology is used to implement the HBs employed in the Hybrid IVRs. Below 5 nm there is again the need to change the transistors' structures to mitigate the unacceptably high transistors' leakage currents in off state.

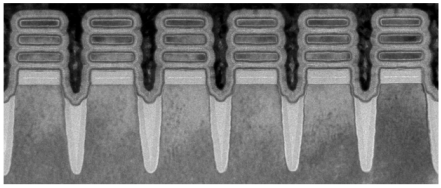


Fig. 4.6: Row of 2 nm nanosheet devices. Image reproduced from [52].

IBM recently announced the first chip using 2 nm nanosheet transistors [52]. This new technology has the potential to improve the overall chip efficiencies and reduce the carbon footprint of data centers . It is estimated that if every data center were to change its servers to 2nm-based processors enough energy could be saved to power 43 million homes [52].

4.3.2 Integrated Inductors with Magnetic Core

High energy density capacitors are for a long time present in commercial CMOS technology nodes as part of the design kit of chip manufacturers, since they are essential building blocks for digital and analog circuits. However, this is not the case for high energy density inductors. Only recently, inductors with thin films of magnetic material were incorporated in the design kit of a large chip manufacturer (TSMC ® [53]). The use of such inductor technology has the potential to reduce the total PoL footprint by a factor of 400 compared to on-board voltage regulators [53]. Furthermore, a reduction of the total size of the inductors can be achieved by using coupled inductors. Coupled racetrack inductors featuring a combination of direct and inversely coupled inductors in series have been designed in the course of this work, cf. Fig. 4.7(a), for the presented PMIC. These coupled inductors employ a NiFe core that is wrapped around the coils (manufactured by Tyndall, cf. Figs. 4.7(b),(c) and (d)).

However, advances in high-frequency magnetic materials, inductor topologies, and silicon integration are still needed to allow for a more broad availability of high energy density inductors in standard CMOS technologies or customized interposers.

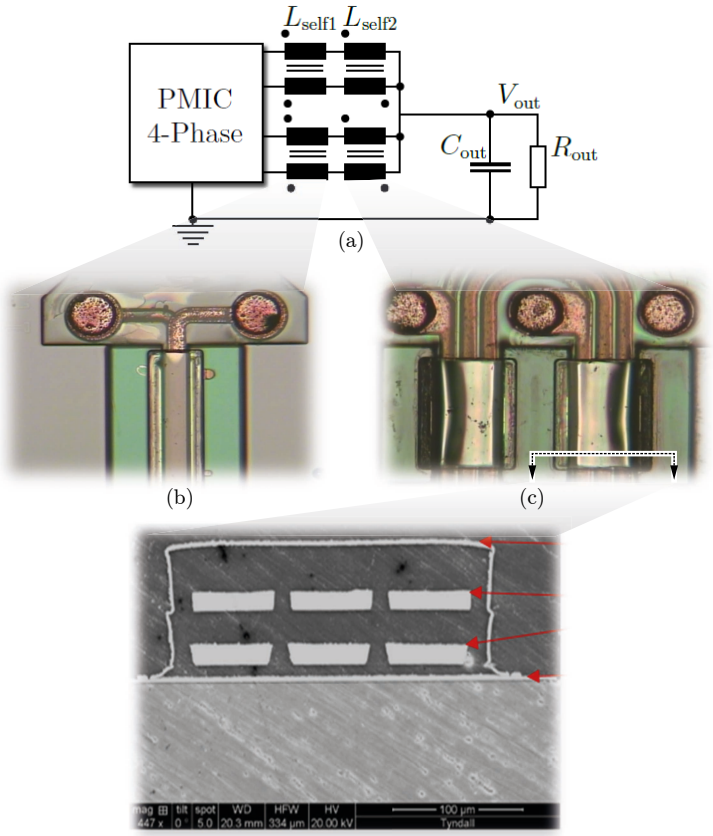


Fig. 4.7: (a) Four-phase inductor-based IVR with coupled inductor configuration designed to operate at 100 MHz switching frequency. (b) Magnified picture of the directly-coupled inductor's back side. This inductor features a self-inductance of 2.4 nH and a coupling factor of 0.95. (c) Magnified picture of the inversely coupled inductor. This inductor features a self-inductance of 21.6 nH and a coupling factor of −0.95. (d) Cross section view of the inversely coupled inductor showing the multi-layer coils used to reduce the footprint area. Figure adapted from [54].

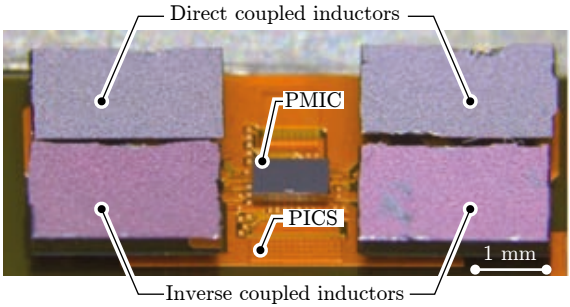


Fig. 4.8: All-silicon 2.5-D demonstrator implemented with the coupled inductors of Fig. 4.7.

4.3.3 Simulation Tools and IVR Multi-Objective Optimization

In this work, Cadence ® simulations have been used to investigate the working principles of the considered converter topologies. The results of these simulations enable the creation of energy-based loss models of the inner-most part of the power stage (transistors and a limited number of inner-most metal layers). However, it is found that these loss models facilitate the calculation of the converter losses with acceptable accuracy only at low output power levels. In case of high output power, the parasitic components of the PDN and the package generate a significant amount of losses for 14 nm technology. Thus, the results of a multi-objective optimization according to [29] (using energy-based loss models derived from simulations) need to be refined in a subsequent step by the additional loss contributions of the PDN and the package. This subsequent step currently requires post-layout simulations, packaging simulations, and measured DC resistances that include the contributions of the PDN and the package. The development of design tools that take into account all important parasitics of the chip layout and package, besides the transistors and passive components, are lacking specially for cutting-edge CMOS technologies.

4.3.4 Advanced Packaging

New package technologies are key enablers to improve the power densities of IVRs. For IVRs that have part of their components in the same chip as the load,

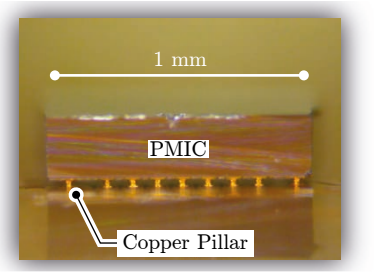


Fig. 4.9: PMIC of Fig. 3.2(b) connected to the silicon interposer using copper pillars.

the package should be designed to minimize the parasitic components, and add new functionalities such as active cooling. Microprocessor packages usually use flip-chip bonding (also known as Controlled Collapse Chip Connection (C_4)) with solder bumps as a method for interconnecting dies to other dies or PCBs. With the increase of the current densities in the interconnects, losses and voltage deviations start to become significant. Copper pillar bump technology [55] allows for smaller pitch, improved thermal conductivity, and reduced impact of electromigration on the resistances of the interconnects. The copper pillar bump technology is a promising technology to reduce package losses and parasitics and, therefore, it was chosen to connect the PMIC shown in Fig. 4.8 to the silicon interposer, cf. Fig. 4.9.

To support the vertical growth of microprocessor systems, which is a necessary future step to maintain the increase of computational performance of microprocessor systems for the next decades, a multi-functional interposer which simultaneously features TSVs and active cooling technologies is proposed in [56] and shown in Fig. 4.10. In this context, integration of IVRs into 3-D chip stacks is part of upcoming technologies to be developed.

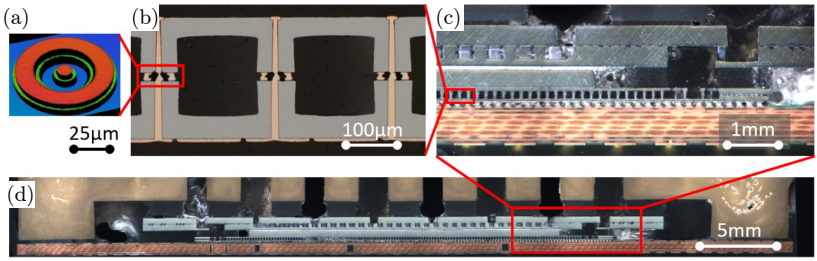


Fig. 4.10: (a) Interposer with sealing rings and (b) embedded TSVs. The sealing rings are required to prevent electrical shorts in case of water as a coolant. A cavity height of 160 μm and a pin-fin diameter of 75 μm was achieved for a TSV pitch, diameter and depth of 225 μm, 15 μm and 125 μm, respectively. (c), (d) Microscopic view of the dual side cooled thermal demonstrator module in 2-port and pin-fin configuration. Figure adapted from [56].

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