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Three-Phase Four-Quadrant Switched-Mode Ultra-High Bandwidth AC Power Source

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Abstract

Power-Hardware-in-the-Loop (P-HIL) simulations are an important tool in commissioning and testing of power electronic converters, where a device under test (DUT), e.g., a motor drive or a rectifier, is connected to a simulation environment that emulates the behavior of grids, electrical machines or other power electronic appliances in order to examine the behavior of the system under test in real-time conditions. One of the key components of such a test environment is the physical interface, which connects the DUT to the emulation model and converts the quantities calculated by the software simulation into the corresponding voltages, currents or other physical quantities, that are then made available to the DUT. This interface is generally formed by a power amplifier, which must be able to cover the voltage, current and power levels required by the tested equipment, while at the same time accurately reproducing the signals determined by the simulation model with as little distortion as possible. Consequently, the maximum available output frequency of the power amplifier ultimately limits the accuracy of the simulation and has to be sufficiently high such that all relevant dynamic phenomena occurring in the tested equipment can be covered, hence resulting in the need for power amplifiers with high bandwidths. Moreover, due to the emerging use of wide-bandgap (WBG) power semiconductor devices that enable ever higher switching frequencies and thus faster dynamics of the systems under investigation, there is also a constant need to continuously increase the bandwidth of the employed amplifiers in order to keep pace with technical developments, with typical applications targeting bandwidths above 20 kHz at output power levels in the range of 10 kW to 100 kW. Additionally, the test environment should be fully bidirectional and has to be able to cope with a wide variety of different loads due to the versatility of the connected devices under test. All in all, these requirements result in a challenging design process for such a high-bandwidth power amplifier.

State-of-the-art solutions are usually implemented using either linear amplifiers or conventional switched-mode topologies. However, linear amplifiers inherently suffer from high losses, which degrade their efficiency and require the installation of bulky and expensive cooling systems. Conventional two-level switched-mode topologies on the other hand are not able to reach the required output frequencies since their bandwidth is ultimately limited by the switching frequency of the employed semiconductors. Consequently, more advanced approaches are required for next-generation high-bandwidth power amplifiers in order to overcome the technical limitations of currently available systems.

This thesis therefore investigates a switched-mode four-quadrant high-bandwidth AC power amplifier intended as a test source for P-HIL testing applications with a single-phase power of 10 kW at an RMS output voltage of 230 V, aiming for full output power and voltage at frequencies from DC to 100 kHz.

In a first step, existing topologies are compared, including purely switched-mode architectures as well as analog and hybrid concepts that incorporate a combination of a switched converter with either an additional linear stage or an additional fast-switching switched-mode auxiliary stage. The cascaded-H-bridge (CHB) topology is identified as the most suitable candidate for implementation since it is expected to provide the highest achievable performance for a purely switched-mode topology with reasonable effort, with the advantage of the series-interleaved approach over a parallel-interleaved system originating from lower operating voltage of the employed semiconductors. Additionally, the CHB architecture inherently features a great degree of modularity as converter systems with varying voltage, power and frequency ratings can be realized by changing the number of converter cells, which is a favorable property in the light of a potential industrial realization.

Based on the selected topology, the entire design process of an ultra-high power bandwidth (UH-PBW) amplifier is then conducted, starting with the identification of key design parameters such as the number of converter cells and their respective operating voltage and switching frequency. By combining several constraints related to the output voltage quality as well as the reactive power demand of the output filter and the maximum output signal frequency, a relation between these quantities is identified, which is used to determine the minimum required number of converter cells with respect to the achievable switching frequency of the semiconductors. For the investigated system, an optimum number of six converter cells with a switching frequency of 300 kHz and a DC-link voltage of 100 V is found, enabling an effective switching frequency of 3.6 MHz for the entire CHB stack. Following these considerations, the full-bridge inverter stages of the cells are dimensioned.

In a further step, the design of the output filter is conducted, where a procedure based on a multi-objective filter design space optimization is utilized to dimension a two-stage LC filter that maximizes the achievable large-signal bandwidth of the system.

Besides the output stage of the UH-PBW amplifier also its power supply is discussed. Considering a typical CHB power supply structure, where each of the cells is supplied with an individual isolated DC-DC converter, a reduction

of the number of components can be achieved by utilizing a multi-port DAB converter. The investigated multi-port converter results from the Integration of Three Dual-Active Bridge (I3DAB) converters into a combined topology that combines the primary-side full-bridges of a conventional realization into a common three-phase two-level inverter, thereby featuring a common primary-side input port and three individual secondary-side ports. In this context, a novel optimized modulation scheme for this converter is proposed, enabling an efficiency improvement under certain asymmetric part load conditions that could occur if used as a CHB supply. The obtained findings are experimentally verified on the basis of a prototype system, proving a good matching between theoretical considerations and measured results, revealing efficiency improvements from 97 % to 97.5 % in case of asymmetrical loading of the three converter output ports.

In addition, the impact on the grid in case of low-frequency single-phase loads is investigated for a general (i.e., not restricted to the CHB topology) UH-PBW amplifier, where it is found that the occurring power pulsation causes low-frequency grid current distortions that complicate compliance with certain grid standards, such as IEC 61000. In order to mitigate these disturbances, sufficient decoupling between the power delivered to the output and the power consumed from the grid has to be ensured, or a derating of the output power for certain output frequencies has to be accepted. This results in a design constraint for the DC-link capacitance of a general three-phase PFC rectifier intended for the power supply of a UH-PBW amplifier.

Finally, the design of the control system of the converter is addressed, where a multi-objective Pareto optimization approach is used to determine the control gains of a linear cascaded control structure that enables fast control and disturbance rejection of the converter's output voltage. However, during the design of the control system, nonlinear effects originating from the natural sampled PWM modulator are discovered. These are a result of the locking mechanism that is required to avoid multiple switching events during a PWM carrier half-period that could increase the switching frequency of the MOSFETs above the PWM frequency. The observed modulator locking effect introduces excessive overshoot of the output voltage during transients. Consequently, countermeasures to mitigate these effects are introduced, including an adaption of the control parameters, a slew rate limitation of the reference signal or an advanced PWM modulator that enables a temporary increase of the PWM carrier frequency during transients.

In order to verify the dynamic behavior expected from the theoretical considerations, a single-phase prototype converter of the analyzed 230 V/10 kW

UH-PBW amplifier was constructed and experimentally tested in the course of this thesis. The prototype features a six-cell CHB topology with a DC-link voltage of 100 V per cell, enabling an effective switching frequency of 3.6 MHz and reaching full-power output for frequencies of up to 100 kHz. From the obtained results a very good agreement between dynamic modeling and measurements is found, proving that the CHB topology is a suitable solution for the implementation of a high-bandwidth power amplifier intended for the applications in a P-HIL simulation environment.

Kurzfassung

Power-Hardware-in-the-Loop (P-HIL) Simulationen sind ein wichtiges Werkzeug beim Testen und bei der Inbetriebnahme von leistungselektronischen Systemen, bei welchen ein Prüfling (z.B. ein Motorumrichter oder ein Gleichrichter) an eine Simulationsumgebung angeschlossen wird, die das Verhalten von Stromnetzen, elektrischen Maschinen oder anderen leistungselektronischen Komponenten emuliert, um das Verhalten des Prüfobjekts unter Echtzeitbedingungen zu untersuchen. Eine Schlüsselkomponente einer solchen Testumgebung ist die physikalische Schnittstelle, welche den Prüfling mit dem Emulationsmodell verbindet und die von der Simulationssoftware berechneten Grössen in entsprechende Spannungen, Ströme oder andere physikalische Grössen umsetzt und dem Prüfling zur Verfügung stellt. Diese Schnittstelle wird üblicherweise von einem Leistungsverstärker gebildet, welcher in der Lage sein muss, die benötigten Spannungen, Ströme und Leistungen zu liefern und gleichzeitig die vom Simulationsmodell berechneten Signale möglichst verzerrungsfrei wiederzugeben. Die maximal erreichbare Ausgangsfrequenz des Leistungsverstärkers limitiert dabei letztendlich die Genauigkeit der Simulationsergebnisse und muss hinreichend hoch sein, um alle im System vorkommenden dynamischen Phänomene abzubilden, weshalb Leistungsverstärker mit hoher Bandbreiten benötigt werden. Zudem besteht aufgrund der zunehmenden Verbreitung von Leistungshalbleitern mit grosser Bandlücke (s.g. Wide-Bandgap Devices), welche immer höhere Schaltfrequenzen und dadurch schnellere Systemdynamiken der untersuchten Systeme ermöglichen, die Notwendigkeit, die Bandbreite der verwendeten Leistungsverstärker stetig zu erhöhen, um mit der technischen Entwicklung Schritt zu halten. Die angestrebten Bandbreiten in typischen Anwendungen liegen dabei bei über 20 kHz bei Leistungen im Bereich von 10 kW bis 100 kW. Weiters sollte das Testsystem sowohl einen bidirektionalen Leistungsfluss ermöglichen als auch aufgrund der Vielfalt an unterschiedlichen Anwendungszwecken den Betrieb mit sehr unterschiedlichen Lasten zulassen. Die verschiedenen Anforderungen resultieren daher in einem sehr anspruchsvollem Entwicklungsprozess eines solchen breitbandigen Leistungsverstärkers.

Breitbandige Leistungsverstärker nach aktuellem Stand der Technik werden entweder als Linearverstärker oder als konventionelle Zweilevel-Schaltverstärker realisiert. Lineare Verstärker weisen jedoch inhärent hohe Verlustleistungen auf, welche zu einer schlechten Effizienz führen und den Einbau von sperrigen und teuren Kühlsystemen erfordern. Mit herkömmlichen Schaltverstärkern hingegen ist es nicht möglich, die benötigten Ausgangsfrequenzen zu erreichen, da deren Bandbreite letztlich direkt durch die maximale

Schaltfrequenz der verwendeten Halbleiter limitiert wird. Aus diesem Grund sind für die Entwicklung neuer breitbandiger Leistungsverstärker neue Konzepte notwendig, um die Leistungsfähigkeit dieser Systeme weiter zu erhöhen und die technischen Limitierungen aktueller Systeme zu überwinden.

In dieser Arbeit wird daher eine geschaltete Vier-Quadranten Breitband AC Leistungsquelle mit einer Leistung von 10 kW pro Phase bei einer Spannung von 230 V RMS untersucht, welche als Testquelle für P-HIL Simulationen gedacht ist und Ausgangsfrequenzen bei voller Leistung von DC bis 100 kHz erreichen soll.

In einem ersten Schritt wird dazu ein Vergleich bestehender Topologien durchgeführt, welcher sowohl rein geschaltete Architekturen als auch analoge und hybride Konzepte, die aus einer Kombination einer geschalteten Stufe mit einer zusätzlichen entweder linear arbeitenden oder schnell schaltendend Stufe bestehen, berücksichtigt. Die Topologie kaskadierte H-Brücken (Cascaded H-Bridge-CHB-Topologie) erweist sich dabei als am besten geeignete Option für eine Implementierung eines rein geschalteten Breitbandverstärkers, da sie die höchsten erreichbaren Bandbreiten mit vertretbarem Aufwand ermöglicht, wobei sich der Hauptvorteil der seriellen Kaskadierung gegenüber der parallelen Kaskadierung aus der reduzierten Sperrspannungsbeanspruchung der Halbleiter ergibt. Darüber hinaus zeichnet sich die CHB Topologie durch ein hohes Mass an Modularität aus, da unterschiedliche Konvertersysteme mit variierenden Leistungs-, Spannungs- und Ausgangfrequenzbereichen durch eine Anpassung der Zellenanzahl realisiert werden können, was im Hinblick auf eine mögliche industrielle Umsetzung eine sehr vorteilhafte Eigenschaft darstellt.

Basierend auf der gewählten Topologie wird anschliessend der gesamte Entwicklungsprozess eines breitbandigen Leistungsverstärkers behandelt, beginnend mit der Ermittlung der wichtigsten Grundparameter wie der Anzahl der Konverterzellen und der dazugehörigen Schaltfrequenz und Zellen-Zwischenkreisspannung. Ein Zusammenhang zwischen diesen Grössen lässt sich aus der Kombination verschiedener Randbedingungen wie der Qualität der Ausgangsspannung, der maximalen Blindleistung des Ausgangsfilters sowie der maximalen Ausgangsfrequenz ableiten, welcher dann die Bestimmung der benötigten Anzahl an Konverterzellen in Abhängigkeit der Schaltfrequenz der Zellen ermöglicht. Für das vorliegende System ergibt sich dabei eine optimale Anzahl von sechs Konverterzellen mit einer Schaltfrequenz von je 300 kHz und einer Zwischenkreisspannung von jeweils 100 V, was in einer effektiven Schaltfrequenz der gesamten kaskadierten Schaltstufe von

3.6 MHz resultiert. Darauf aufbauend werden die Wechselrichterstufen der Konverterzellen dimensioniert.

In einem nächsten Schritt erfolgt dann die Dimensionierung des Ausgangsfilters, wobei hierfür ein Filteroptimierungsverfahren zur Auslegung eines zweistufigen LC-Filters verwendet wird, das die erreichbare Ausgangsfrequenz des Systems maximiert.

Neben der Ausgangsstufe des Verstärkers ergeben sich weitere Untersuchungsaspekte in Bezug auf die Spannungsversorgung des Systems. Wird die typische Versorgungsstruktur eines CHB-Konverters, bei der jede Konverterzelle durch einen individuellen isolierten DC-DC Konverter versorgt wird, zugrunde gelegt, kann eine Reduktion der benötigten Bauteile durch den Einsatz eines Multi-Port Dual-Active Bridge (DAB) Konverters erreicht werden. Der untersuchte Multi-Port Konverter ergibt sich dabei aus der Integration von drei individuellen DAB Konverterstufen einer konventionellen Realisierung in eine gemeinsame Struktur (in einem s.g. I3DAB Konverter), bei der die primärseitigen Vollbrücken in einen gemeinsamen Dreiphasen Inverter zusammengefasst werden. Die resultierende Topologie weist schliesslich einen gemeinsamen Eingang und drei voneinander isolierte Ausgänge auf. Für diese Konverterstruktur wird ein neuartiges, optimiertes Modulationsschema präsentiert, welches eine Verbesserung des Wirkungsgrads unter bestimmten asymmetrischen Teillastbedingungen ermöglicht, die sich bei der Verwendung als Spannungsversorgung für einen kaskadierten H-Brücken Konverter ergeben können. Die entsprechenden theoretischen Analysen werden anschliessend anhand eines Prototypensystems experimentell verifiziert. Dabei zeigt sich eine gute Übereinstimmung zwischen den theoretischen Vorhersagen und den Messergebnissen, welche eine Effizienzsteigerung um 0.5 % von 97 % auf 97.5 % für bestimmte asymmetrische Arbeitspunkte belegen.

Weiters wird das Verhalten am Netz eines allgemeinen (d.h. nicht auf die kaskadierte H-Brücken Topologie eingeschränkten) Verstärkers beim Betrieb mit niederfrequenten Einphasenlasten untersucht, wobei sich herausstellt, dass die für eine einphasige Last charakteristische Leistungspulsation zu niederfrequenten Verzerrungen der Netzströme führt, welche das Einhalten von Netznormen wie der IEC 61000 erschweren. Um diese Störungen zu unterdrücken, muss eine ausreichende Entkopplung der Leistungsflüsse auf der Last- und der Netzseite sichergestellt werden, oder es muss eine Reduktion der Ausgangsleistung für bestimmte Ausgangsfrequenzen akzpetiert werden. Daraus ergibt sich ein Auslegungskriterium für die notwendige Zwischenkreiskapazität eines allgemeinen dreiphasigen PFC Gleichrichters, der zur

Spannungsversorgung eines breitbandigen Leistungsverstärkers verwendet wird.

Schliesslich wird der Entwurf des Regelsystems für den Verstärker beschrieben, wobei hierfür eine Mehrkriterien-Pareto-Optimierung zur Bestimmung der Regelparameter eines linearen kaskadierten Regelsystems eingesetzt wird, welches sowohl eine hohe Dynamik der Ausgangsspannung als auch eine hohe Störungsunterdrückung ermöglicht. Während des Reglerentwurfs zeigen sich jedoch nichtlineare Effekte welche eine Folge des s.g. "Natural Sampling" des PWM-Modulators sind und zu massivem Überschwingen der Ausgangsspannung während Transienten führen können. Diese sind die Konsequenz eines Verriegelungsmechanismus im verwendeten PWM-Modulator, welcher notwendig ist, um zusätzliche Schaltvorgänge innerhalb einer PWM-Halbperiode zu vermeiden, die zu einer Erhöhung der Schaltfrequenz der MOSFETs über die PWM-Frequenz hinaus führen würden. Um die resultierenden Störeffekte zu vermeiden, werden verschiedene Lösungsansätze präsentiert, darunter eine Anpassung der Regelparameter, eine Begrenzung der Anstiegsrate des Referenzsignals oder ein erweiterter PWM-Modulator, der eine vorübergehende Erhöhung der PWM-Trägerfrequenz während Transienten ermöglicht.

Um das aus den theoretischen Analysen zu erwartende dynamische Verhalten zu verifizieren, wurde im Rahmen dieser Arbeit abschliessend ein einphasiger Prototyp eines 230 V/10 kW Verstärkers aufgebaut und experimentell getestet. Der Prototyp weist eine sechszellige kaskadierte H-Brücken Topologie mit einer Zwischenkreisspannung von 100 V pro Zelle auf, die eine effektive Schaltfrequenz von 3.6 MHz ermöglicht und Ausgangsfrequenzen von 100 kHz bei voller Leistung erreicht. Die erzielten Ergebnisse zeigen eine sehr gute Übereinstimmung zwischen der dynamischen Modellierung und den Messresultaten und belegen, dass die kaskadierte H-Brücken Topologie eine geeignete Lösung für die Implementierung eines Leistungsverstärkers mit hoher Bandbreite für Anwendungen in einer P-HIL Simulationsumgebung darstellt.

Abbreviations

AC	Alternating Current
CHB	Cascaded H-Bridge
CM	Common-Mode
CMC	Common-Mode Choke
DAB	Dual-Active Bridge
DC	Direct Current
DM	Differential-Mode
DUT	Device Under Test
FPGA	Field-Programmable Gate Array
FFA	Fundamental Frequency Analysis
GaN	Gallium Nitride
HF	High-Frequency
HS	High-Side
HV	High-Voltage
IGBT	Insulated-Gate Bipolar Transistor
ILA	Integrated Logic Analyzer
ITAE	Integral of Time-Weighted Absolute Error
LF	Low-Frequency
LFT	Low-Frequency Transformer
LPA	Linear Power Amplifier
LS	Low-Side
LV	Low-Voltage
LVDS	Low Voltage Differential Signaling
MMC	Modular Multi-Level Converter
MRI	Magnetic-Resonance Imaging
NPC	Neutral Point Clamped
PFC	Power Factor Correction
P-HIL	Power-Hardware-in-the-Loop
PSPWM	Phase-Shifted Carrier PWM
PWM	Pulse-Width Modulation
Si	Silicon
SiC	Silicon Carbide
SINAD	Signal-to-Noise and Distortion
SPI	Serial Peripheral Interface
SRC	Series Resonant Converter
UH-PBW	Ultra-High Power Bandwidth
WBG	Wide-Bandgap

ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

Power amplifiers are key a component of Power-Hardware-in-the-Loop (P-HIL) test environments, where they act as interfaces between a virtual system model (e.g., of a power grid or of a load) and a device under test (DUT, e.g., an inverter stage) [1]. A typical example is the emulation of power grids, including transient phenomena and disturbances (e.g., unbalanced voltages, voltage dips, harmonics) [2–4], and possibly also the grid impedance characteristics [5, 6], or the comprehensive testing of grid-connected converters such as PFC rectifiers or PV inverters. The authors of [7] provide an up-to-date overview on grid-emulation concepts. Similarly, multi-area power system dynamics can be investigated using test benches with multiple grid and load emulators [8–11]. The emulation of electrical motors is another important field where P-HIL testing can advantageously enable flexible and fast analyses of motor drive inverter systems [12–17], whereby various coupling networks between amplifier and DUT inverter can be employed [18]. Considering, e.g., automotive drive drains, also the emulation of batteries [19] is of interest. Further applications for power amplifiers include injecting test signals into electric systems that can be characterized by their frequency-dependent impedance, e.g., impedance spectroscopy of batteries [20] and measurements of the grid impedance to accurately assess the control-loop stability of grid-connected converters [21]. Finally, gradient amplifiers for magnetic-resonance imaging (MRI) systems share similar requirements of high power, highly dynamic voltage adaption, and bandwidth [22, 23].

In general, the accuracy of emulated phenomena such as grid transients or slot effects in electric motors is ultimately limited by the bandwidth of the power amplifier. Also, as the switching frequencies of DUTs increase, e.g., due to the use of wide-bandgap (WBG) power semiconductors, so must the bandwidths of amplifiers used in P-HIL systems [24] to still accurately capture

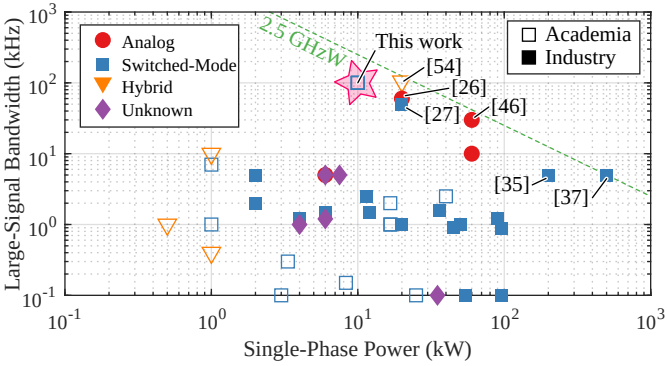


Fig. 1.1: Large-signal bandwidth (maximum output frequency at nominal voltage) vs. single-phase power (power of a single unit, i.e., without paralleling of multiple units) of typical AC power amplifier systems that can generate a single-phase output RMS voltage of at least 230 V, as reported in literature by industry [26–46] and academia [12–14, 38, 47–55]. The ultra-high power bandwidth (UH-PBW) amplifier system proposed in this thesis is highlighted.

the corresponding interactions between DUT and emulated environment. Similarly, considering, e.g., future aircraft onboard grids with grid frequencies of up to 1 kHz, or high-speed motors with similar or even higher fundamental frequencies, there is a need for power amplifiers that not only provide a high small-signal bandwidth, but that can also provide full voltage and power at high output frequencies of up to 50 kHz to 100 kHz [25].

Fig. 1.1 gives an overview of power amplifier systems reported by industry and academia. Typically, analog amplifiers need to be employed if ultra-high power bandwidths (UH-PBWs), i.e., higher than a few kilohertz, should be reached. However, the advent of WBG power semiconductors and the increasing computing power of digital control hardware, which facilitate higher switching frequencies and advanced (e.g., interleaved) converter topologies, enables switched-mode amplifiers to achieve *quasi-analog* amplifier performance and much higher efficiencies. The focus of this thesis is thus on the hardware realization for such a next-generation power amplifier. As a starting point, this chapter provides a comprehensive review of analog, switched-mode, and hybrid power amplifier topologies reported in the literature in **Section 1.1**. Based on this, the most promising approaches for next-generation UH-PBW power amplifiers are identified and discussed in

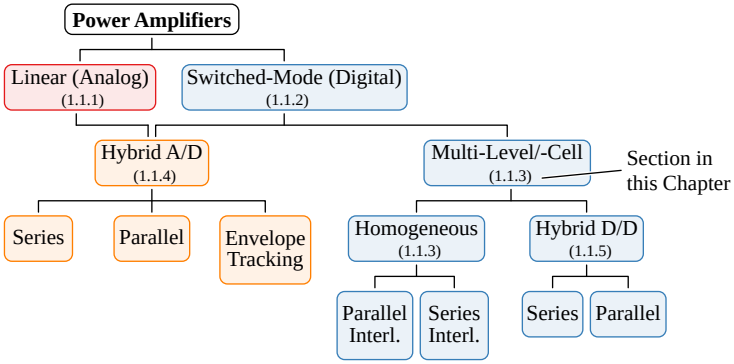


Fig. 1.2: Classification of power amplifier realization options as used in **Section II**; small identifiers refer to the corresponding subsections; the color coding corresponds to that used in **Fig. 1.1**.

Section 1.2. The content of these sections including the introductory section of this chapter are largely based on the topology review published in [56]. Furthermore, an outline of this thesis is provided in **Section 1.3**.

1.1 Types and Arrangements of Power Amplifiers

To provide a basis for identifying the most promising concepts and topologies for future power amplifiers that can meet the UH-PBW requirements outlined before, this section gives a comprehensive overview and a classification (see **Fig. 1.2**) of power amplifier concepts described in the literature. Whereas the focus of this section is on AC power amplifiers with output voltages in the range of 230 V RMS (single-phase) and output power levels in the order of several kilowatts to several tens of kilowatts, the following discussion considers also other examples with lower or higher output voltage and power capabilities as far as necessary to comprehensively cover all conceptually different solutions.

In the following, the terms “large-signal bandwidth”, “power bandwidth”, and “maximum output frequency” are used interchangeably to refer to the maximum frequency at which an amplifier can provide full-scale output voltage and current (i.e., power). Similarly, the publications summarized

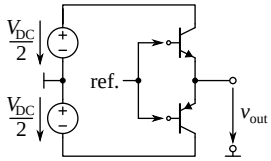


Fig. 1.3: Basic topology of a linear (analog) class-B amplifier. As suggested by its name, the power transistors are operated in their linear range, contrary to the switched-mode amplifier topologies discussed from **Section 1.1.2** on.

below do not all employ a consistent definition of the "small-signal bandwidth". Therefore, unless specifically mentioned otherwise, a generic definition as the maximum frequency where only a small fraction (e.g., 10 %) of the full-scale output voltage or current can be provided is used.

1.1.1 Linear (Analog) Power Amplifiers

Linear power amplifiers (LPAs) operate power transistors (see **Fig. 1.3**) in the linear range and hence can achieve very high bandwidths, high slew rates and low output impedances [57]. **Fig. 1.1** reflects these desirable characteristics and indicates that still many commercial high-bandwidth power amplifiers are of analog type. However, as known from electronics textbooks such as [58], the maximum efficiency of an analog class-B amplifier is given by

$$\eta_{\max,\,\text{Class B}} = \pi/4 \approx 78.5\,\%, \tag{1.1}$$

which it achieves only at the maximum output voltage ($\hat{v}_{\text{out}} = V_{\text{DC}}/2$) and with resistive load. The efficiency degrades in direct proportion to a reducing output voltage amplitude and also scales with the power factor $\cos\varphi$. This efficiency characteristic is an inherent property of the topology and cannot be improved, e.g., by employing larger transistors. Class-AB amplifiers achieve better linearity (reduced distortions around the output voltage zero crossings) by introducing a quiescent current that flows through both output-stage transistors and hence further reduces the efficiency. Similarly, operation with reverse power flow, i.e., as an active load, results in extreme power dissipation as then the sum of the supply power *and* the power fed back from the DUT is dissipated in the linear amplifier's transistors [57]. All in all, these low efficiencies, which imply high losses and correspondingly high cooling effort,

render conventional purely analog concepts unsuitable for future UH-PBW power amplifiers. For the sake of completeness it has to be noted that there is ongoing research on improving the efficiency of analog amplifiers. Following essentially the same approach discussed in **Section 1.1.3** below for switched-mode amplifiers, i.e., cascading of building blocks consisting of low-voltage (LV) power semiconductors and individual DC power supplies, [59] proposes a diode-clamped linear inverter. The system replaces the n-type and the p-type transistors of a class-B amplifier with series connections of n-type and p-type LV MOSFETs and a network of clamping diodes. Depending on the output voltage, at any point in time only a single LV MOSFET operates in the linear region, whereas all other LV MOSFETs are either fully turned-on or fully turned-off. Therefore, the efficiency increases with the number of series-connected LV devices to values exceeding 95 % for more than 20 series devices (e.g., using 40 V-MOSFETs for a total DC-link voltage of 800 V). However, the losses are not equally distributed among the power devices. A further improvement can be achieved if the DC voltages are not split equally but asymmetrically [60]. Similarly, [61] employs a flying-capacitor approach to ensure equal blocking voltages for the LV MOSFETs. Both systems feature unity *voltage* gain and hence require a high-voltage reference signal. The concepts have been proposed and tested for filter-less motor drives with sinusoidal output voltages or rectifier applications with a few kilowatts of power. However, so far no performance evaluation focusing on UH-PBW operation has been reported.

1.1.2 Switched-Mode (Digital) Amplifiers

The term "switched-mode amplifier" has been coined as early as in the 1950s [62–64], initially for inverters targeting applications such as servo drives and later for audio applications (class-D). By not operating the transistors in the linear range but only either in the off-state or in the fully saturated on-state (digital behavior), i.e., in switched-mode operation, amplifiers with significantly higher efficiencies could be realized. Importantly, their efficiencies do not depend strongly on neither the output voltage amplitude nor on the power factor, which is in stark contrast to LPAs.

As shown in **Fig. 1.4** for the simplest case of a single half-bridge stage, switched-mode/digital amplifiers employ pulse-width modulation (PWM) to generate a switched output voltage whose local average value follows a reference signal. Considering naturally sampled PWM with a triangular carrier and a purely sinusoidal reference signal, the spectrum of the switched

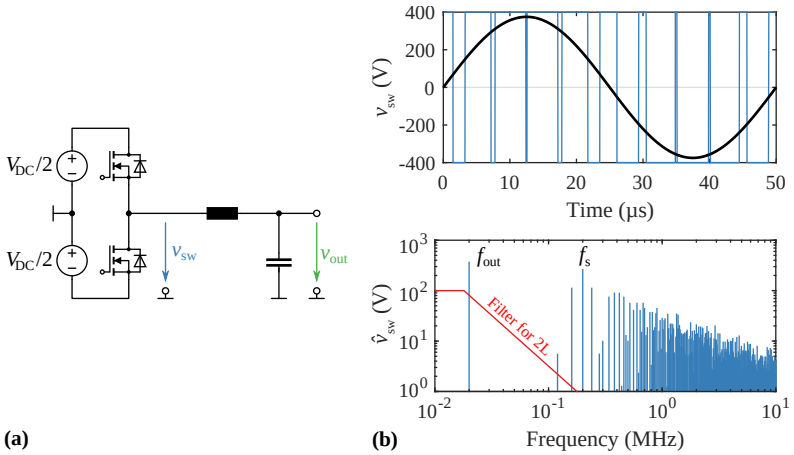


Fig. 1.4: (a) Basic topology of a digital amplifier incorporating a two-level half-bridge and **(b)** exemplary waveforms of the switched voltage v_{sw} and the corresponding spectrum $\hat{v}_{sw}$, considering $V_{DC} = 800\,V$, $f_{out} = 20\,kHz$, and a device switching frequency of $f_s = 200\,kHz$. The cutoff frequency of the LC output filter is selected to limit the maximum peak-to-peak voltage ripple of the output voltage, v_{out}, to $0.02 \cdot V_{DC}/2$. The solid black waveform is $v_{sw,(1)}$, i.e., the switched voltage's fundamental component that corresponds to the reference voltage.

voltage, v_{sw}, contains harmonics at multiples of the carrier frequency, i.e., at nf_s, and sidebands at $nf_s \pm 2f_{out}$ (and $\pm 4f_{out}$, etc., which are, however, already significantly lower in amplitude), where f_s denotes the switching frequency and f_{out} denotes the fundamental frequency of the (filtered) output voltage, v_{out} [65]. Thus, a low-pass output filter is required to separate the desired local average of the switched output voltage from the switching-frequency harmonics (see also **Fig. 1.4** and the in-depth discussion in **Section 1.2.1**). To do so, even with an ideal low-pass filter the maximum output frequency is limited to $f_{out} \leq f_s/3$, because otherwise the relevant sideband harmonic at $f_s - 2f_{out}$ would be in the filter's passband. According to [57], in practice only lower maximum output frequencies (for a given switching frequency) are feasible, i.e., typically $f_{out} \leq f_s/10$, taking into account characteristics of real filters with finite slopes such as the exemplary single-stage LC filter with −40 dB/dec shown in **Fig. 1.4b**.

The switching losses even of modern WBG SiC and GaN power semiconductors still limit f_s, if certain efficiency targets should be achieved and/or maximum cooling system volumes are limited. Nevertheless, in parallel to the development of power electronic inverter systems (drives, UPSs, etc.), two-level topologies have found and are still finding widespread applications as power amplifiers in applications where the achievable output frequencies / bandwidths are sufficient, e.g., for the emulation of 50 Hz grids. Thus, before discussing more advanced topological variations, i.e., multi-level and multi-cell topologies, that facilitate increasing the *effective* switching frequency and by doing so shift the fundamental limit discussed above to significantly higher frequencies, a brief overview on recent applications of two-level switched-mode amplifiers as AC power amplifiers is given.

Typical systems based on standard two-level (IGBT-based) inverters feature switching frequencies of around 10 kHz and power levels in the range of about 10 kVA to 50 kVA, achieve small-signal control bandwidths in the order of 1 kHz and are typically employed for applications with fundamental frequencies of up to 100 Hz [2, 8, 9, 12, 14, 15, 17, 66, 67]. Higher fundamental output frequencies can be achieved by employing special modulation patterns, as, e.g., reported in [13] for a 120 kVA machine emulator system that supports a maximum output frequency of 2.5 kHz with a switching frequency of 10 kHz only. Moving from IGBT to WBG power semiconductors facilitates higher switching frequencies above 100 kHz and correspondingly also higher small-signal bandwidths of up to several 10 kHz [5, 51, 68]. Special techniques such as synchronizing the amplifier's modulation to the PWM of the DUT inverter allows the emulation of motor current harmonics at the switching

frequency of a DUT inverter (10 kHz) [24]. Note that when only lower output voltage levels are required, significantly higher large-signal bandwidths can be achieved such as 50 kHz for a 45 V DC system reported in [69] because the employed LV power semiconductors allow much higher switching frequencies (e.g., 700 kHz) without excessive switching losses. These considerations already indicate that a further increase of the achievable bandwidths could be facilitated by either paralleling of multiple bridge-legs or by stacking multiple converter cells realized with LV power semiconductors.

1.1.3 Multi-Level/-Cell Digital Amplifiers

In order to increase the bandwidth of switched-mode power amplifiers, ultimately the cutoff frequency of the output low-pass filter must be increased. If the output voltage quality should not be compromised this implies that the harmonic content of the switched waveform must be shifted to higher frequencies. There are two basic strategies to achieve this without increasing the switching frequency of the power semiconductors: series-interleaving and parallel-interleaving, which is comprehensively explained in, e.g., [70]. A detailed technical analysis of multi-level and multi-cell amplifier scaling laws is provided later in **Section 1.2.1**, whereas the focus of this section is on providing an overview of corresponding examples found in the recent literature to give an impression of the use cases and achievable performance.

Parallel Interleaving

In the widest sense, the constant power flow of a three-phase power system [71] can be understood as a result of parallel-interleaving. As pointed out in [57], parallel operation of multiple systems to increase the effective operating frequency is known since 1916 from mercury-arc valve rectifiers with DC-side interphase reactors [72]. More specifically, as known since the early 1970s [73,74], two or more bridge-legs can be operated in a parallel-interleaved manner to generate a multi-level output voltage waveform with $N_{\mathrm{HB}} + 1$ voltage levels with N_{HB} denoting the number of parallel bridge-legs. The first switching-frequency harmonics occur around the *effective* switching frequency $f_{\mathrm{s,eff}} = N_{\mathrm{HB}} \cdot f_{\mathrm{s}}$ (see **Fig. 1.5**). Therefore, it can be shown (see **Section 1.2.1**) that a single-stage LC filter's cutoff frequency required for the same output voltage ripple increases (implying higher possible bandwidth) with the number of bridge-legs N_{HB} as

$$f_{0,\max} = N_{\mathrm{HB}}^{3/2} \cdot f_{0,\max,\mathrm{2L}} \tag{1.2}$$

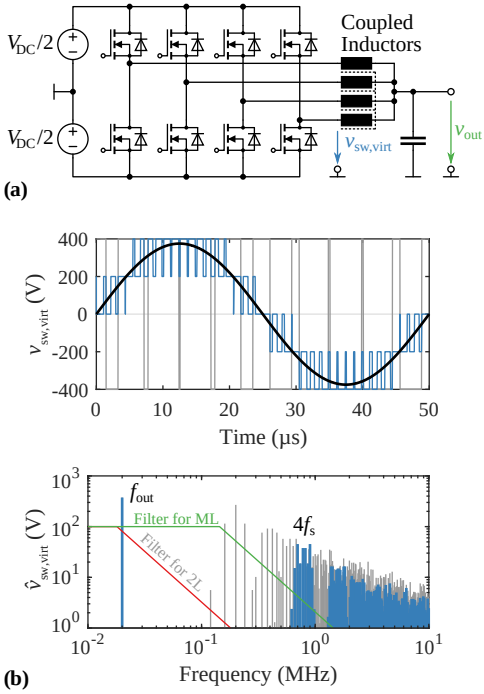


Fig. 1.5: (a) Parallel-interleaved topology of $N_{HB} = 4$ two-level bridge-legs resulting in a cancellation of all switching-frequency harmonics below $f_{s,eff} = N_{HB} f_s$, i.e., an N_{HB}-times higher effective switching frequency at roughly the same switching losses as occurring for **Fig. 1.4**, thereby enabling a significantly higher filter cutoff frequency. Compared to a single bridge-leg, the current stress of the power semiconductors is reduced. **(b)** Exemplary waveform of the switched voltage $v_{sw,virt}$ and the corresponding spectrum $\hat{v}_{sw,virt}$, considering $V_{DC} = 800\,V$, $f_{out} = 20\,kHz$, and a device switching frequency of $f_s = 200\,kHz$ (identical to the two-level topology in **Fig. 1.4**). The cutoff frequency of the LC output filter is selected to limit the maximum peak-to-peak ripple of the output voltage, v_{out}, to $0.02 \cdot V_{DC}/2$. Due to the cancellation of the switching frequency harmonics up to the effective switching frequency $N_{HB} f_s$, the cutoff frequency of the filter can be chosen higher by a factor of 8 compared to an equivalent two-level half-bridge (cf. **Fig. 1.6**). Note that $v_{sw,virt}$ is the sum of the four bridge-legs' individual switch-node voltages divided by N_{HB}. The operating principle of this concept is discussed in detail in **Section 1.2.1**. Note: the solid black waveform is $v_{sw,(1)}$, i.e., the switched voltage's fundamental component that corresponds to the reference voltage.

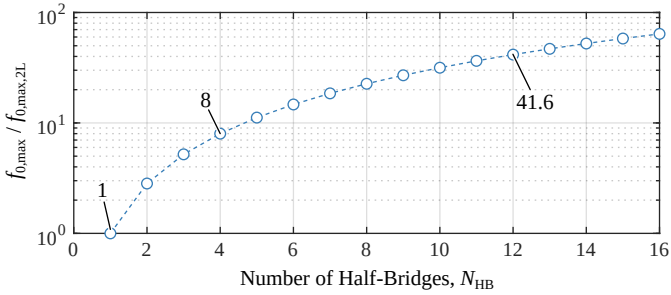


Fig. 1.6: Possible increase of a single-stage LC filter's cutoff frequency by adding additional half-bridges to a simple two-level topology (parallel or series interleaving, see **Fig. 1.5** and **Fig. 1.7**), for otherwise identical parameters (device switching frequency, allowed voltage ripple, etc.), see (1.2). Note that the 8 times higher cutoff frequency obtained for $N_{HB} = 4$ can be observed also in the examples shown in **Fig. 1.5** and **Fig. 1.7**.

whereby the switching frequency of each transistor (device switching frequency) is kept constant, see also **Fig. 1.6**. The power semiconductors still need to block V_{DC}, but the output current is shared among the bridge-legs. Thus, also compared to simply increasing the semiconductor current rating (i.e., the chip area) of a single bridge-leg to reach higher power levels, interleaved operation of several bridge-legs is advantageous. The concept has thus also been employed for digital amplifiers already in the 1990s [75], e.g., for driving MRI gradient coils [22]. More recently, high-power systems have been described, where even with the use of IGBTs relatively high effective switching frequencies and hence high small-signal and large-signal bandwidths have been achieved. For example, [76] demonstrates tracking of a 1 kHz reference signal with a "LinVerter" operating from a 320 V DC bus at up to 10 A output current. Similarly, [52] employs a full-bridge configuration with two times six interleaved IGBT bridge-legs switching at 20 kHz each (i.e., achieving an effective switching frequency of 240 kHz) to realize a 50 kVA (three-phase) amplifier with a bandwidth of 1 kHz for grid emulation applications. Parallel interleaving has also been used in industrial systems. For example, [35] and [77] describe a 200 kVA emulation system that achieves a large-signal bandwidth of 5 kHz and a small-signal bandwidth of 15 kHz using six parallel amplifier modules with six interleaved IGBT bridge-legs each, operating from an 800 V DC bus. Even higher power ratings can be achieved by paralleling more amplifier modules. Similarly, [37] and [38] describe a

high-power industrial motor emulator system with an overall output current rating of up to 1600 A RMS at a fundamental frequency of up to 5 kHz, which is facilitated by an effective switching frequency of 800 kHz. It can be assumed that also a digital amplifier that became available recently as a product [27] employs a parallel-interleaved topology to achieve an effective switching frequency of 1 MHz and thus the ability to provide a large-signal bandwidth of 50 kHz at an output power of up to 20 kW. Finally, recent work [78] targeting lower output voltages (45 V) and making use of state-of-the-art 150 V GaN transistors' capability of switching at up to a megahertz to reach an effective switching frequency of 4 MHz (four interleaved bridge-legs) demonstrates extreme performance in terms of bandwidth by reaching large-signal amplification of reference signals with a bandwidth of up to 350 kHz. Another recently proposed concept specifically targeting motor emulation for testing three-phase two-level inverters uses parallel bridge-legs with individual LC output filters to generate four voltage levels, and four AC-switches to alternately connect one voltage level to the emulator's phase terminal [79, 80]. Whereas the concept avoids introducing additional (very small) current ripple as compared to a parallel-interleaved alternative, the hardware effort (number of switches) as well as the control complexity are significantly higher.

Series Interleaving (Cascading of Converter Cells)

Several full-bridge converter cells can be connected in series at their AC terminals to form a cascaded H-bridge (CHB) converter, which has been proposed in 1971 [81]. Again, interleaved operation of these converter cells results in a multi-level output voltage waveform with $2N_{\text{cell}} + 1$ levels, where N_{cell} is the number of cascaded converter cells. The first group of switching-frequency harmonics occurs around $f_{\text{s,eff}} = N_{\text{HB}} \cdot f_{\text{s}}$ (see **Fig. 1.7**, and [82] for a formal analysis), where N_{HB} again denotes the number of bridge-legs and, considering full-bridge cells, $N_{\text{HB}} = 2 \cdot N_{\text{cell}}$ holds. CHB-based solutions require dedicated, i.e., isolated, power supplies for each of the cascaded cells. The topology thus inherently features galvanic isolation. It is furthermore fully modular, which facilitates scaling of output voltage or power ratings to higher levels by increasing the number of cells. In contrast to parallel-interleaved topologies, the blocking voltage of the cells' power semiconductors is reduced to $V_{\text{DC}}/(2N_{\text{cell}})$ (note that V_{DC} always refers to the total DC voltage of an equivalent parallel-interleaved or non-interleaved amplifier, see **Fig. 1.4**, **Fig. 1.5** and **Fig. 1.7**), which advantageously allows to employ devices with lower blocking voltages and hence lower switching losses. In case of MOS-

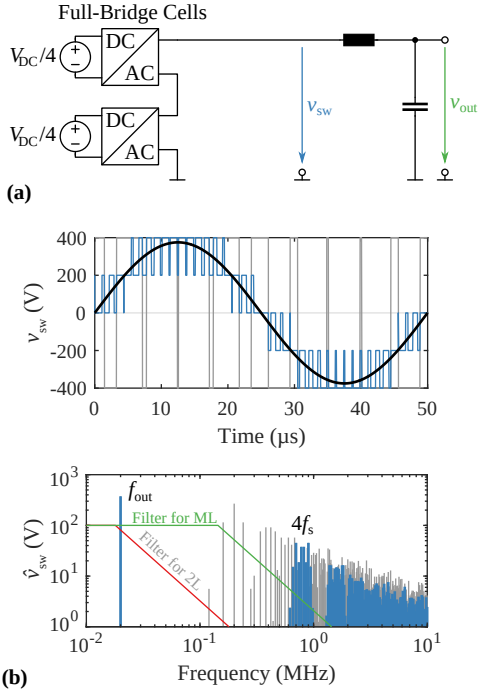


Fig. 1.7: (a) Series-interleaving of $N_{HB} = 2N_{cell} = 4$ two-level bridge-legs. Similar to the parallel-interleaved topology (cf. **Fig. 1.5**) series-interleaving results in a cancellation of all switching-frequency harmonics below $f_{s,eff} = N_{HB} f_s$, i.e., an N_{HB}-times higher effective switching frequency at roughly the same switching losses as occurring for **Fig. 1.4** results, enabling a significantly higher filter cutoff frequency. Compared to a single bridge-leg, the blocking voltage of the power semiconductors is reduced. **(b)** Exemplary waveform of the switched voltage v_{sw} and the corresponding spectrum $\hat{v}_{sw}$, again considering $V_{DC} = 800\,V$, $f_{out} = 20\,kHz$, and a device switching frequency of $f_s = 200\,kHz$. Again, the cutoff frequency of the LC output filter is selected to limit the maximum peak-to-peak voltage ripple of the output voltage, v_{out}, to $0.02 \cdot V_{DC}/2$. Compared to the parallel-interleaved topology with the same number of bridge-legs, identical frequency spectra result, rendering both concepts identical in terms of harmonic performance. Consequently, also for series-interleaving the cancellation of the switching frequency harmonics up to the effective switching frequency $N_{HB} f_s$ enables to chose the cutoff frequency of the filter higher by a factor of 8 compared to an equivalent two-level half-bridge (cf. **Fig. 1.6**). The operating principle of these concepts are discussed in detail in **Section 1.2.1**. Note: the solid black waveform is $v_{sw,(1)}$, i.e., the switched voltage's fundamental component that corresponds to the reference voltage.

FETs, devices with lower blocking voltage ratings advantageously also feature lower specific on-state resistances (which scales roughly with $V_B^{-2.5\cdots-2}$) [83].

Even though known for a long time and successfully applied especially in high-power and medium-voltage applications, the CHB structure has first been introduced to switched-mode amplifiers only shortly after the turn of the millenium [84]. Later, [85] described a system with grid-level output voltage ranges and a 2 kW power rating, which could achieve a closed-loop large-signal bandwidth of 5 kHz using six cascaded cells switching at 25 kHz each (effective switching frequency of 300 kHz). Similar results have also been reported in [50] or, for lower output voltages, in [86].

The scalability of the CHB concept renders it suitable also for applications with higher voltages such as gradient amplifiers for MRI systems [23] and medium-voltage grid simulation, as indicated by, e.g., a 6 MVA, 50 Hz system that can provide 35 kV output voltage (with a step-up transformer) [87]. Recently, [88] and [4] have introduced, a 1 MVA system with five cascaded cells and a total DC voltage of 6 kV, which achieves a small-signal bandwidth of 7 kHz. Series-interleaving has also been employed for special applications, e.g., with low power but high voltage as for supplying plasma reactors with a 15 kV (peak) square wave voltage at 5 kHz [89]. Fully utilizing the benefits of the CHB concept, [90] describes an amplifier for medical application (electroporation) that consists of 20 cascaded cells with 60 V DC each. Making use of 80 V GaN devices and a combination of staircase modulation and PWM operation of one cell with a switching frequency of 1 MHz, the amplifier can generate bursts of a 500 kHz sinusoidal output voltage with an amplitude of up to about 1 kV at 7 A RMS load current. A similar system described in [91] employs asymmetric cell voltages to optimize the tradeoff between switching losses and output voltage quality.

Series-interleaving of cascaded converter cells is an extremely powerful concept for future UH-PBW systems. Therefore, this approach is discussed in more detail in **Section 1.2.1** and the topology is ultimately selected for the implementation of the single-phase 10 kW demonstrator with a large-signal bandwidth of 100 kHz investigated in this thesis.

Series Interleaving (Multi-Level Bridge-Legs)

Multi-level bridge-legs such as neutral-point clamped (NPC) structures (patent filed in 1979 [92], also described in 1981 [93]) or flying-capacitor converter topologies (proposed in 1992 [94]) consist of power semiconductors that only require a blocking voltage rating that is lower than the total DC bus voltage, and advantageously generate an output voltage with multiple levels

and a higher effective switching frequency, i.e., they can be seen as a non-modular variant of the series-interleaved multi-cell topology discussed above. Therefore, the approach has been selected for certain digital power amplifiers discussed in the literature.

For example, [95] employs a five-level diode-clamped bridge-leg structure to realize a 7.5 kW (three-phase) amplifier with a switching frequency of 10 kHz and a filter cutoff frequency of 2 kHz. Similarly, but now making use of SiC power semiconductors, [48, 96, 97] propose a 10 kW three-phase AC power source based on three-level T-type bridge-legs [98] that operate with a switching frequency of 48 kHz, achieving a small-signal bandwidth of 7.1 kHz. The effective large-signal bandwidth is limited to about 300 Hz by the capacitive current consumption of the employed two-stage LC filter; paralleling of bridge-legs would thus become necessary to increase the maximum output frequency. Recently, [99] demonstrated an arbitrary voltage waveform generator with an eight-level flying-capacitor bridge-leg using GaN transistors that switch at 200 kHz. Even though the prototype is rated at only 500 W and operates with a relatively low DC-bus voltage of 200 V, it achieves a very high closed-loop bandwidth of 50 kHz that facilitates large-signal output waveforms with fundamental frequencies of up to 40 kHz.

Modular multi-level converter (MMC) structures [100] are a fully modular alternative for realizing bridge-legs with a single DC-side interface: in contrast to CHB topologies, the converter cells of an MMC bridge-leg do not need dedicated power supplies, i.e., the local DC capacitor voltages are maintained via appropriate control, and a single DC supply for the digital amplifier stage is sufficient. MMC-based grid emulators have been proposed in [101] and later, targeting emulation of grid faults and unbalanced conditions with a delta-wye coupling transformer [102] or in a transformer-less three-phase four-wire configuration [103]. Recently, a MMC topology has been proposed as an arbitrary waveform generator for dielectric testing of high-voltage grid assets; the full-scale system shall provide an output voltage of up to 100 kV and 10 kW of power with a large-signal bandwidth of 500 Hz [104]. Note, however, that MMC topologies are not suitable for operation with DC or very *low* output frequencies due to the increased energy exchange with the modules' floating capacitors [105].

Combination of Series and Parallel Interleaving

Of course, it is possible to parallel-interleave several multi-level bridge-legs, thereby combining the advantages of both concepts (current sharing, lower blocking voltage) in a single converter stage. An early reference from the

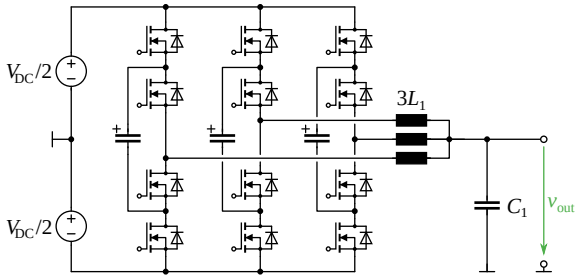


Fig. 1.8: Example for a combination of (flying-capacitor) multi-level bridge-legs and parallel interleaving as proposed in [25].

year 2000 combines several GTO multi-level bridge-legs (switching at the fundamental frequency) in a parallel-interleaved manner to realize an arbitrary waveform generator [106]. More recently, [39] proposed a motor emulator that consists of three parallel-interleaved three-level NPC bridge-legs operating from an 800 V DC bus, which allows to use 600 V or 650 V CoolMOS silicon MOSFETs. The emulator realizes output currents of more than 50 A RMS at a fundamental frequency of up to 2.5 kHz. Instead of three-level NPC bridge-legs, also multi-level flying-capacitor bridge-legs can be parallel-interleaved, as recently proposed in [25, 53]. This design shown in **Fig. 1.8** uses three three-level flying-capacitor bridge-legs operating from an 800 V DC bus, which are realized with 600 V GaN transistors. This facilitates a switching frequency of 800 kHz and hence an effective switching frequency of 4.8 MHz. The system achieves a large-signal bandwidth of 100 kHz at the rated power of 10 kW (single-phase).

1.1.4 Hybrid Analog/Digital Amplifiers

Generally speaking, analog amplifiers tend to achieve near-ideal behavior regarding the dynamic performance but suffer from high losses, whereas the opposite is true for digital amplifiers. Therefore, already in the 1980s combinations of analog and digital amplifiers to form *hybrid* amplifiers have been proposed [107] and classified into two main categories as shown in **Fig. 1.9** [108, 109]. Note that typical AC power source applications require a controlled voltage output. Hence, the following discussion focuses on these topologies even though **Fig. 1.9** shows the equivalent arrangements for amplifiers with a current-source output characteristic, too. Note that the

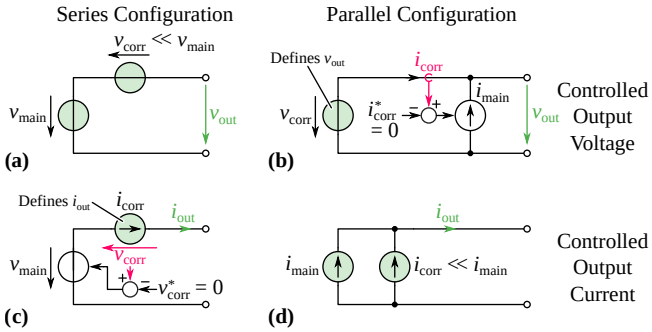


Fig. 1.9: Generic classification (introduced by Yundt in 1983 [108, 109]) of hybrid amplifier concepts. For concepts **(a)** and **(d)**, the main amplifier (index $_{\text{main}}$, i.e., the stage that provides the bulk power to the load) approximates the desired output as closely as possible and the correction amplifier (index $_{\text{corr}}$) compensates any remaining deviation; the output quantity (voltage or current) is the sum of both stages' contributions. In contrast, in case of concepts **(b)** and **(c)** the correction amplifier defines the output quantity directly and the main amplifier is controlled to adjust the load impedance seen by the correction amplifier (e.g., in case **(b)**, the main amplifier is controlled such that the correction amplifier's output current is minimized and ideally zero).

correction amplifier stage, which for A/D hybrid amplifiers is realized with an analog amplifier, could also be realized with a low-power / low-voltage digital amplifier with correspondingly higher bandwidth than the main amplifier. Such D/D hybrid amplifiers will be discussed below in **Section 1.1.5**. First, however, a brief overview on the different A/D hybrid amplifier concepts is given, including a third concept (envelope tracking) not shown in the classification from [108, 109] and **Fig. 1.9**. The interested reader finds a more detailed review of hybrid amplifier concepts published before 2011 in [110].

Series Configuration

In a series configuration (see **Fig. 1.9a**) of a main digital amplifier stage and an analog correction amplifier stage, the output voltage is the sum of the two amplifier's output voltages. Consequently, the goal is for the main amplifier to approximate the desired output voltage as closely as possible such that the remaining deviation, i.e., a voltage ripple, to be compensated by the correction amplifier is as low as possible. The analog correction amplifier then operates with relatively low voltage; even though it processes the full

load current, the processed power remains low. This *partial power processing* of the (analog) stage with low efficiency does have only a moderate impact on the system-level efficiency [111].

The concept can be implemented with a two-level digital amplifier with an output filter as shown in **Fig. 1.10a** and proposed in [112]. Alternatively, the series voltage can be coupled into the main power path via a transformer, which advantageously avoids that the analog correction amplifier must carry the full load current [107]; this is similar to older concepts for active harmonic filtering [113]. However, to avoid the bandwidth limitation introduced by an output filter suitable for two-level converters, most systems discussed in literature from as early as 1994 [115] (for MRI gradient amplifiers) employ multi-cell digital amplifier stages, which even without PWM can approximate a sinusoidal voltage relatively well as a staircase waveform. The magnitude of the voltage steps, i.e., the DC voltages of the cells, directly defines the required voltage capability of the analog stage. Furthermore, to achieve a clean output waveform, the linear amplifier's slew rate must be higher than the $\mathrm{d}v/\mathrm{d}t$ of the digital amplifier's switching transitions. Therefore, most systems described in the literature employ a $\mathrm{d}v/\mathrm{d}t$ filter at the output of the multi-cell digital amplifier. For example, [50, 116, 117] describe a 130 V RMS, 1 kW (single-phase) system consisting of nine cascaded converter cells with equal DC voltages, which achieves a large-signal bandwidth of 10 kHz and, thanks to the linear stage, a very high small-signal bandwidth of 600 kHz. The 140 V RMS, 500 W hybrid amplifier proposed in [47] achieves a similar small-signal bandwidth of 400 kHz, but uses only four cascaded cells that, however, feature unequal DC voltages and thus can realize 19 voltage levels (instead of nine voltage levels achievable with four cells that have equal DC voltages, see **Section 1.1.3**). In contrast to most systems discussed in the literature, it is also possible to operate the digital multi-cell amplifier of a hybrid D/A amplifier system not with staircase modulation but with (phase-shifted) PWM [118]. However, the LC filter required to attenuate the switching-frequency harmonics generated by the digital multi-cell amplifier then again limits the achievable power bandwidth.

Note that instead of providing an isolated power supply for each of the cascaded cells, it would be possible to move the isolation to the output, i.e., to sum the contributions of all cells and of the linear stage via a transformer [119]. However, in this case, saturation of the transformer core prevents operation with DC or low-frequency signals. Another option has been proposed in [49], where instead of a CHB multi-cell structure, an MMC topology has been

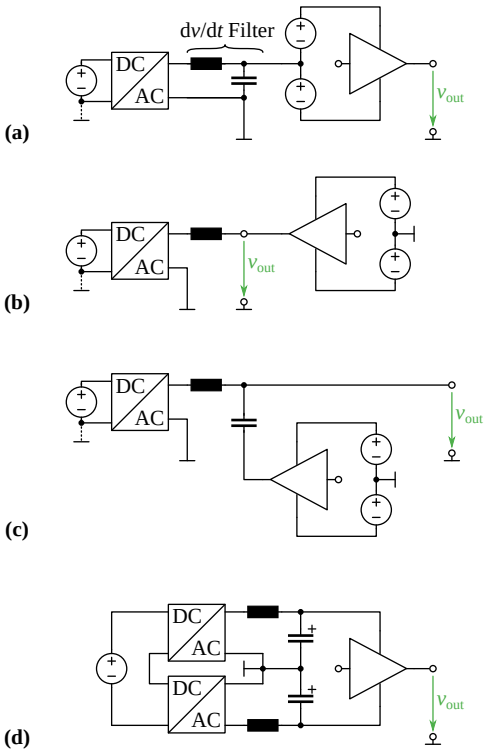


Fig. 1.10: D/A-hybrid amplifier concepts. **(a)** Series configuration (cf. **Fig. 1.9a**) of a digital main amplifier and a series-connected analog correction amplifier. A $\mathrm{d}v/\mathrm{d}t$ filter can be employed to reduce the slew rate requirement of the analog correction amplifier. **(b)** Parallel configuration (cf. **Fig. 1.9b**), i.e., the analog amplifier directly defines the output voltage while the digital main amplifier provides the bulk of the load current. **(c)** Capacitive coupling of the analog amplifier reduces its required voltage (and hence power) rating [114]. **(d)** Envelope-tracking configuration, where the supply voltage of the analog amplifier is adapted according to the output voltage set point in order to reduce losses.

employed and hence a single DC supply for the digital amplifier stage is sufficient.

The research in series A/D hybrid amplifiers using multi-cell digital amplifier stages is still ongoing, with [54, 120, 121] describing a 60 kVA, 400 V three-phase system consisting of a 12-cell CHB stage using nearest-level modulation (a sorting algorithm ensuring equal stresses of the cells), a $\mathrm{d}v/\mathrm{d}t$ filter, and a linear correction amplifier. The CHB cells operate with a DC voltage of 30 V and hence the linear amplifier can provide an output voltage of ±30 V to compensate the voltage steps. With a bandwidth of the LPA stage of 105 kHz, the system can realize full-scale sinusoidal test signals with up to 60 kHz. A similar system has recently been described in [122].

Parallel Configuration

Alternatively, the correction amplifier and the main (digital) amplifier can be connected to a common output in parallel as shown in **Fig. 1.9b** and **Fig. 1.10b**. Advantageously, the linear amplifier thus fully defines the output voltage and hence the transient behavior (bandwidth, slew rate). The digital main amplifier is controlled such that it provides most of the load current. The correction amplifier ideally compensates only the ripple current, i.e., acts as an active filter. Thus, the lower the ripple generated by the main amplifier is, the lower the current rating (and hence power rating) of the analog stage becomes. Therefore, multi-level (e.g., parallel-interleaved) digital stages are often considered. However, during transients that are faster than the main amplifier's bandwidth, the linear amplifier must (transiently) deliver the necessary load current, which ultimately could lead to thermal overload. These (and further) aspects of A/D hybrid amplifier systems have been thoroughly discussed in [75]. The direct parallel configuration as shown in **Fig. 1.10b** is most suitable for low-voltage, low-power applications such as audio amplifiers (see, e.g., [123–125]), because the linear amplifier stage must process the full voltage and feature a low high-frequency output impedance.

Fig. 1.10c shows a slightly different configuration proposed in [114], which couples the analog amplifier capacitively to the common output. This coupling capacitor, which can be seen as part of the digital stage's LC output filter, takes most of the output voltage and the linear amplifier's voltage capability is given by the remaining voltage ripple across the filter capacitor (which would appear if the correction amplifier was not present). According to [114], this implies that the power rating of the linear amplifier can be reduced from typically 10 % . . . 20 % to 1 % . . . 4 % of the output power rating, with corresponding benefits regarding the overall system efficiency, and a

simplified cooling system. Note that similar concepts are known from active EMI filters [126–128]. However, whereas the linear amplifier still ensures very high output voltage quality, it can only improve the small-signal dynamics, and the main amplifier stage with its LC low-pass filter defines the large-signal response. The 400 V, 4 kW prototype described in [114] nevertheless achieves a large-signal bandwidth of 10 kHz with a three-level NPC digital amplifier that switches at 100 kHz and features an LC low-pass filter with a cutoff frequency of 20 kHz. In [129], the same approach is used with a CHB main amplifier. Advantageously, the active filter (analog correction amplifier) can also compensate low-frequency switching distortions, i.e., subharmonics below $2N_{\text{cell}}f_{\text{s}}$, that may appear as a consequence of, e.g., unequal DC voltages of the CHB converter cells. Note that as an alternative to multi-level topologies, two-level digital main amplifiers with *two-stage* (4^{th} order) LCLC output filters could be employed [130], [131] to reduce the ripple current that the analog amplifier stage must process.

Envelope-Tracking Power Supply

Fig. 1.10d shows a third hybrid configuration (not shown in the classification from **Fig. 1.9**), where a digital stage adapts the supply voltage of a linear amplifier according to the desired output voltage, as proposed in 1985 for audio applications [132]. These so-called envelope-tracking approaches improve the efficiency of the analog amplifier, especially for operation with output voltages below the maximum (see **Section 1.1.1**). Thus, a high-power (115 V RMS, 1.5 kW) system described in [117, 133] reaches a peak efficiency that is only slightly higher than that of a linear amplifier with constant supply voltages for operation with maximum output voltage, but shows clear benefits at lower output voltages. However, the large-signal bandwidth of 1 kHz is essentially limited by the bandwidth of the tracking power supply. Therefore, the approach is rarely used for power amplifiers as considered here, but mainly for low-power or special applications such as driving piezoelectric transducers [134]. Note that envelope-tracking power supplies in radio-frequency (RF) applications are used to vary the supply voltage of the RF linear amplifier according to the *envelope* of the RF signal to be amplified, i.e., the bandwidth of the tracking power supply must be higher than the envelope of the output signal only [135] (interestingly, the envelope-tracking power supply proposed there is a parallel A/D hybrid configuration, achieving a maximum output frequency of 300 kHz at 50 W and 26 V).

1.1.5 Digital/Digital Hybrid Amplifiers

As discussed above, the correction amplifiers shown in **Fig. 1.9** can also be realized with digital amplifiers, which due to lower power requirements can operate with much higher switching frequencies than the main amplifiers. Hence, these digital correction amplifiers can achieve higher bandwidths and approximate the behavior of a linear amplifier with higher efficiency. The general goal remains to increase the LC output filter's cutoff frequency (for a given output voltage quality), which allows an increase of the overall amplifier systems' bandwidth. Essentially, the resulting systems are structurally very similar to series or shunt active filters, which have been investigated since the 1970ies for grid applications [136].

Series Configuration

Again, a correction voltage source can be added in series to a main amplifier stage (see **Fig. 1.9a**). A first option to do so couples the compensation voltage via a transformer into the main power flow path [107,137], as done for decades in power grid applications [113, 136]. This concept has recently been applied to a grid simulation system in [138, 139], where a standard 400 V, 5 kVA IGBT inverter is combined with a 100 V MOSFET inverter that is responsible for generating higher-order harmonics. Similarly, [140–142] use a three-phase transformer to combine the outputs of a 800 V, 12 A three-phase inverter switching at 20 kHz with a 100 V small-signal inverter operating at 200 kHz. In these examples, the low-frequency output transformer limits the achievable bandwidth, e.g., to 2 kHz in [140–142]. The roles of the main amplifier and the transformer-coupled small-signal stage are clearly separated (generation of fundamental and higher-order harmonics).

In contrast, a direct series connection of a slow-switching high-power, high-voltage inverter with a fast-switching low-voltage, low-power inverter directly aims at improving the harmonic content of the overall switched output voltage, which in turn allows an increase of the system's output filter cutoff frequency. Advantageously, the main amplifier stage is a multi-level inverter, which, e.g., can operate at the fundamental frequency. The correction amplifier needs a DC voltage that corresponds to the difference of two output voltage levels only, and can then operate with PWM to improve the spectrum of the overall output voltage waveform. Such systems have been proposed in the 1990s for MRI gradient amplifiers [115] or MV drive applications [143, 144], the latter combining a GTO inverter switching at the fundamental frequency with a PWM-operated IGBT inverter. The power amplifier concept

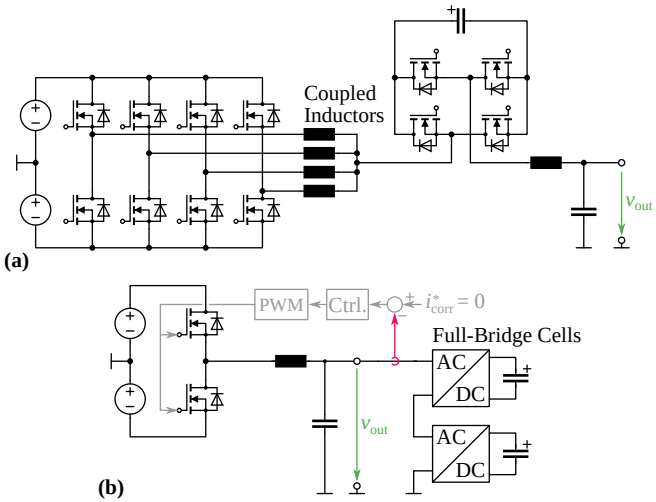


Fig. 1.11: D/D-hybrid amplifier concepts. **(a)** Series configuration (cf. **Fig. 1.9a**) of a multi-level (parallel-interleaved; series-interleaved would be possible, too) main amplifier stage and a series-connected digital correction stage (processing only distortion reactive power at a comparably low voltage level) [145]. **(b)** Parallel configuration (cf. **Fig. 1.9b**) of a multi-cell (series-interleaved) correction stage that directly defines the output voltage and a parallel-connected two-level main stage that delivers the bulk of the load current [55, 146]. Note that the correction stage processes only distortion reactive power and the cells thus do not require power supplies.

described in [50, 117] uses a similar concept by operating all except one cell of a CHB converter at the fundamental frequency only, generating a staircase waveform. The last cell operates with PWM such that the overall output voltage waveform is a multi-level PWM waveform. Compared to all cells operating with (interleaved) PWM, the effective switching frequency is much lower, however, requiring a lower output filter cutoff frequency. Similarly, but targeting HVDC circuit breaker testing, [147] proposes a 10 kV, 30 kA arbitrary voltage source that combines a low-voltage PWM-inverter with a multi-level Marx-type high-voltage staircase voltage generator.

The fast-switching cell can operate as an active filter only, i.e., without processing active power. Therefore, it is not necessary to provide an (isolated) power supply, as proposed in [148]. There, a diode-clamped 5-level inverter is combined with two series-connected H-bridges with flying DC capacitors controlled to two different DC voltages. This active filter improves the output voltage quality without significantly degrading the system's efficiency. Targeting MV applications, [149] similarly describes a CHB system with asymmetric DC voltages of the (supplied) cascaded cells, and two additional cells without a power supply that hence act as active filters only. More recent publications combine an active filter stage without external power supply with a parallel-interleaved multi-level inverter [145], as exemplarily shown in **Fig. 1.11a**, or instead with an MMC converter as proposed in [150] for driving underwater electroacoustic transducer systems. Both variants share the advantage of needing only a single DC supply (in contrast to CHB-based approaches). Whereas the MMC-based solution can advantageously make use of low-voltage semiconductors, its complexity is clearly much higher than that of a parallel-interleaved main power stage.

Recently, [19] proposed a D/D hybrid emulator for traction batteries, where the battery's resistance must be emulated with a minimum bandwidth of 20 kHz, however, only with relatively low power. Thus, a combination of an 80 kW standard converter delivering the bulk power (at up to 600 V and 500 Hz) and a series-connected low-power full-bridge active filter (100 V DC, ±300 A) operating with an effective switching frequency of 200 kHz is employed.

Parallel Configuration

Parallel configuration (see **Fig. 1.11b**) of two digital amplifier stages of different characteristics is possible, too. Such concepts have been proposed as active shunt filters for grid applications early on, e.g., in [151] and [152]. In the context of power amplifiers, the goal of parallel-connecting an active

filter stage is to shift the cutoff frequency of the required output filter to higher frequencies and hence enable improved dynamic performance of the amplifier system, as discussed earlier. For example, already in 1999, [153] demonstrated a 25 V RMS, 40 A RMS high-current amplifier system with a main stage switching at 100 kHz and a parallel-connected stage operating at 1 MHz, whereby the auxiliary stage compensates (reduces) the current ripple of the main stage by −29 dB.

For three-phase systems, [154] proposed an active filter approach that connects CHB converter stacks (without cell power supplies) between the main inverter's phases. These active filters remove the ripple current created by the main inverter and hence significantly improve the output voltage quality. Recently, [55,146,155] employed a similar topology using three 17-level CHB stacks (effective switching frequency of 1 MHz) in star-configuration to act as an active filter for a three-phase two-level main amplifier (switching frequency max. 14.5 kHz). **Fig. 1.11b** shows a schematic representation of this concept. A 60 kVA prototype achieves high-bandwidth (100 kHz) output voltages via the CHB system, whereas the current bandwidth of the main amplifier (and hence the power bandwidth of the overall system) is limited to about 2 kHz. This limitation is similar to that of D/A parallel-hybrid systems discussed above.

1.1.6 Discussion

Considering the many different amplifier topologies described in literature and described so far, analog amplifiers achieve extreme bandwidth but suffer from high losses. D/A hybrid topologies still employ analog amplifier stages with relatively high losses, and D/D hybrid systems are relatively complex as they combine different types of switched-mode amplifiers. In both cases, the power bandwidth remains limited by the stage processing the bulk power. Whereas this may be sufficient for certain applications, the most suitable approaches for high-power general-purpose UH-PBW amplifiers are parallel- or series-interleaved switched-mode topologies, as they combine high efficiency and, due to interleaving, high power bandwidth. Series-interleaved multi-cell systems are particularly interesting, as they inherently feature galvanic separation and low realization effort concerning inductive components. This, in addition, enables relatively straightforward scaling to higher power and especially higher voltage levels. Therefore, the following **Section 1.2** explains technical key considerations for the realization of parallel-interleaved and series-interleaved (multi-cell) UH-PBW amplifiers.

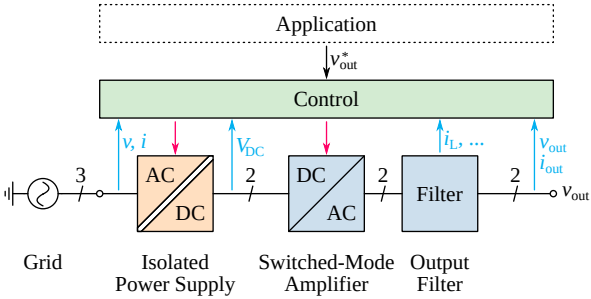


Fig. 1.12: Single-line overview diagram of a UH-PBW power amplifier *system*, which, in addition to the actual switched-mode amplifier and output filter (**Section 1.2.1**) also features a mains interface, i.e., an isolated power supply (**Section 1.2.2**), and a control system including voltage and current sensors (**Section 1.2.3**). The application-level software, which is not in the scope of this thesis, models, e.g., a specific grid behavior, or emulates a motor behavior, etc. Note that a system with a single-phase output is shown as a basic building block; three output phases could, e.g., be achieved by employing three switched-mode amplifiers and three filter stages.

1.2 Concepts for Future UH-PBW Amplifiers

As illustrated in **Fig. 1.12**, a general-purpose UH-PBW amplifier *system* consists of three subsystems. The following subsections discuss key aspects of these subsystems: the actual switched-mode amplifier stage including a low-pass output filter in **Section 1.2.1**, a typically isolated (to facilitate arbitrary reference potentials of the amplifier's output) mains interface in **Section 1.2.2**, and the control system including voltage and current sensors, high performance computing hardware and the corresponding firmware in **Section 1.2.3**.

1.2.1 Switched-Mode Amplifier and Output Filter

The output filter required to remove switching-frequency noise from a switched-mode amplifier's output voltage ultimately limits the feasible maximum full-power output frequency (reactive power consumption of the filter elements) as well as the small-signal bandwidth (quickly increasing filter attenuation above the cutoff frequency, e.g., −40 dB/dec for a single-stage LC filter). Therefore, realizing ultra-high power bandwidth necessitates a high filter cutoff frequency, and thus simple two-level topologies would require

extreme switching frequencies. Even the availability of modern WBG power semiconductors facilitates this only up to a point before either the efficiency becomes too low or the design becomes thermally unfeasible.

In contrast, as briefly discussed in the context of **Fig. 1.5**/**Fig. 1.7** and **Fig. 1.6** above, multi-level topologies facilitate an increase of the output filter cutoff frequency for otherwise fixed system parameters (device switching frequency and/or power conversion efficiency, maximum allowable output voltage ripple, etc.). Considering a multi-cell (CHB) converter with N_{CHB} cells and a single-stage LC filter, it can be shown (see, e.g., [84]) that the maximum cutoff frequency ensuring a certain relative peak-to-peak output capacitor voltage ripple $\hat{v}_{\mathrm{out,pp}}/V$ is given by

$$f_{0,\max} = \sqrt{\frac{32}{\pi^2} N_{\mathrm{CHB}}^3 f_{\mathrm{s}}^2 \frac{\Delta v_{\mathrm{out,pp}}}{V}}, \tag{1.3}$$

where f_s is the switching frequency of each bridge-leg and V is the sum of all the cells' DC voltages, i.e., $v_{\mathrm{out}} \in [-V, V]$. With the number of half-bridges being $N_{\mathrm{HB}} = 2N_{\mathrm{CHB}}$, the following generic expression is found,

$$f_{0,\max} = \sqrt{\frac{4}{\pi^2} N_{\mathrm{HB}}^3 f_{\mathrm{s}}^2 \frac{\Delta v_{\mathrm{out,pp}}}{V}}, \tag{1.4}$$

that equally holds also for parallel-interleaved operation of N_{HB} bridge-legs (note that in this case $V = V_{\mathrm{DC}}/2$ such that again $v_{\mathrm{out}} \in [-V, V]$). In the examples of **Fig. 1.4**, **Fig. 1.5** and **Fig. 1.7** with $f_{\mathrm{s}} = 200\,\mathrm{kHz}$, $V_{\mathrm{DC}} = 800\,\mathrm{V}$, $\hat{v}_{\mathrm{out}} = 375\,\mathrm{V}$, and $f_{\mathrm{out}} = 20\,\mathrm{kHz}$, the required filter cutoff frequency is calculated to limit the worst-case peak-to-peak output voltage ripple to $0.02 \cdot V_{\mathrm{DC}}/2$. By changing from a single bridge-leg shown in **Fig. 1.4** to four parallel-interleaved bridge-legs in **Fig. 1.5** or two stacked cascaded cells (four bridge-legs in total, too) in **Fig. 1.7**, the cutoff frequency can be increased from about 18 kHz to 144 kHz, i.e., by a factor of 8 as indicated by (1.2) and in **Fig. 1.6**.

With the cutoff frequency of a single-stage LC filter being $f_0 = 1/2\pi\sqrt{LC}$, the condition (1.4) describes a hyperbola in the L-C-plane, i.e., in the so-called *filter design space* [96] shown in **Fig. 1.13**. Filter designs with $f_0 \leq f_{0,\max}$ satisfy the voltage ripple criterion. For a fixed N_{HB}, $f_{0,\max}$ increases with f_s and hence the area where the combinations of L and C satisfy $f_0 \leq f_{0,\max}$ expands. However, the range of valid filter designs is further constrained by limiting the maximum allowable voltage drop across L at nominal output current, I_{out}, and maximum output frequency, $f_{\mathrm{out,max}}$, to

$$I_{\mathrm{out}} \cdot 2\pi f_{\mathrm{out,max}} L \leq p \cdot V_{\mathrm{out}}, \tag{1.5}$$

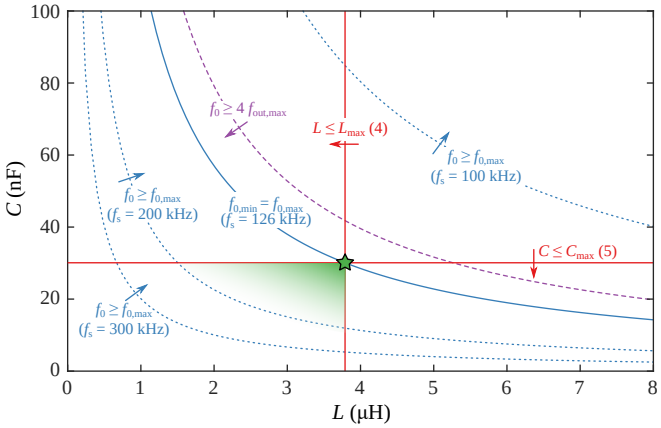


Fig. 1.13: Exemplary design space of a single-stage LC filter for a multi-level topology with $N_{HB} = 12$ half-bridges, $f_{out,max} = 100\,\text{kHz}$, $p = 0.15$, $q = 0.3$, and $\Delta v_{out,pp}/V = 2\,\%$. Note that the design space (green shading) collapses to a single point if $f_s = 126\,\text{kHz}$ is selected according to (1.8); see also f_s in **Fig. 1.14** for $N_{HB} = 12$. The $f_0 \geq 4 f_{out,max}$ criteria could be introduced to spectrally separate the maximum output frequency from the LC filter's resonance. Note that further criteria such as maximum permissible output impedance, etc. can be mapped to limiting curves in the design space [96].

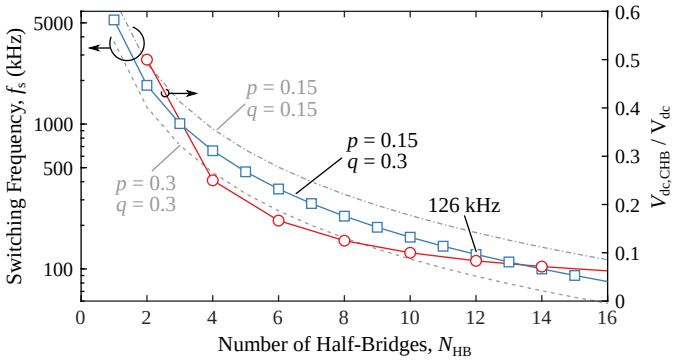


Fig. 1.14: Required device switching frequency in dependence of the topology's number of half-bridges (series- or parallel-interleaving) for $f_{out,max} = 100\,\text{kHz}$, $p = 0.15$, $q = 0.3$, and $\Delta v_{out,pp}/V = 2\,\%$. Note the sensitivity on p and q. For the series-interleaved topology ($N_{CHB} = N_{HB}/2$), the right axis shows the required DC voltage per cell normalized to the DC voltage of a corresponding parallel-interleaved structure.

i.e., to a fraction p of the nominal output voltage V_{out}. Similarly, the maximum current through C at nominal output voltage, V_{out}, and maximum output frequency, $f_{out,max}$ should be limited to

$$V_{out} \cdot 2\pi f_{out,max} C \leq q \cdot I_{out}, \tag{1.6}$$

i.e., to a fraction q of the nominal output current I_{out}. Both criteria result in straight-line boundaries in the filter design space of **Fig. 1.13**. Combining both limits results in a lower bound for the filter cutoff frequency as

$$f_{0,min} = f_{out,max} \cdot \frac{1}{\sqrt{pq}}. \tag{1.7}$$

This again represents a hyperbola in the design space, which is pinned to the intersection point of the limits from (1.5) and (1.6). Note that further criteria such as relating to the output impedance, etc. could be implemented in the design space, and a similar approach can also be considered for the design of two-stage LCLC filters. These aspects have been discussed in detail in [96] and **Section 3.2** of this thesis. Finally, by equating $f_{0,max}(f_s)$ from (1.4) to $f_{0,min}$ from (1.7), a closed-form expression for the required device switching frequency as a function of the number of bridge-legs, N_{HB}, and for given

p, q, $f_{\mathrm{out,max}}$, and $\Delta v_{\mathrm{out,pp}}/V$ can be obtained as

$$f_{\mathrm{s}} = \frac{\pi}{2}\sqrt{\frac{V}{\Delta v_{\mathrm{out,pp}}}} \cdot \frac{1}{\sqrt{pq}} \cdot \frac{1}{N_{\mathrm{HB}}^{3/2}} \cdot f_{\mathrm{out,max}}. \tag{1.8}$$

Note that if f_{s} is selected accordingly, the valid design space in **Fig. 1.13** collapses to a single point, where all criteria are met with the minimum possible switching frequency. The graph of (1.8) in **Fig. 1.14** clearly shows the necessity of employing either parallel-interleaving or cascading of converter cells to realize UH-PBW amplifiers that achieve maximum output frequencies in the order of 100 kHz. Whereas a non-interleaved class-D amplifier would need a switching frequency in the megahertz range, the same performance can be achieved with a multi-level system with, e.g., $N_{\mathrm{HB}} = 12$ bridge-legs, where a clearly feasible device switching frequency of about 126 kHz suffices (see **Fig. 1.13**).

So far, both concepts, parallel-interleaving of bridge-legs (see **Fig. 1.5**) or cascading of converter cells (see **Fig. 1.7**), show equivalently advantageous characteristics, i.e., the same total number of bridge-legs switching at the same frequency results in equal harmonic performance and hence equal filtering requirements. The complexity of a CHB system tends to be higher, as each cell requires a dedicated isolated power supply. In addition, countermeasures against common-mode ground currents through parasitic capacitances between the cells and ground must be considered [156]. However, as indicated in **Fig. 1.14**, the switched voltage in case of a CHB system reduces $\propto 1/N_{\mathrm{HB}}$. Thus, as mentioned earlier, MOSFETs with lower blocking voltage ratings and hence lower switching losses and lower specific on-state resistances (scales roughly with $V_{\mathrm{B}}^{-2.5\cdots-2}$ [83]) can be employed. Furthermore, whereas in a parallel-interleaved topology the output voltage ripple occurs at $N_{\mathrm{HB}} f_{\mathrm{s}}$, each individual inductor still operates with a current ripple at the single bridge-leg's switching frequency, f_{s}. This is in contrast to the CHB system, where the current ripple in the sole filter inductor already occurs at $N_{\mathrm{HB}} f_{\mathrm{s}} = 2N_{\mathrm{CHB}} f_{\mathrm{s}}$, facilitating more compact inductor designs. Similar benefits can also be achieved with multi-level bridge-legs, e.g., employing a flying-capacitor topology. However, a CHB system is *modular*, which simplifies development and testing, benefits from economies of scale in production, and facilitates scalability to higher output voltages, which is mainly limited by the isolation voltage rating of the cells' power supplies and communication interfaces. For this reason, the series-interleaved CHB topology (cf. **Fig 1.7**) is finally selected for the implementation of the UH-PBW amplifier in this

thesis. The design of the CHB switching stage and its corresponding output filter is covered in detail in **Chapter 3**.

1.2.2 Mains Interface

General-purpose UH-PBW amplifier systems require bidirectional power exchange with the feeding grid (to enable full four-quadrant operation), e.g., a 400 V three-phase mains. Furthermore, the amplifier output terminals must be galvanically isolated from the mains to ensure full flexibility and (to some extent) arbitrary definition of the output terminal's reference potential. In general, the amplifier's output voltage and current can have arbitrary frequencies between DC and $f_{\mathrm{out,max}}$, i.e., especially also $f_{\mathrm{out}} < f_{\mathrm{grid}}$ can occur. This leads to low-frequency power pulsations that can translate into low-frequency grid current distortions, violating relevant standards such as IEC 61000-3-11 (harmonics) and IEC 61000-3-12 (flicker). Thus, sufficient decoupling, i.e., sufficiently large DC bus capacitors must be provided (cf. [157] and **Section 2**) regardless of the amplifier topology.

Parallel-Interleaved Topologies

Parallel-interleaved UH-PBW amplifiers require a single isolated DC interface. **Fig. 1.15a** shows the most straightforward realization option, which consists of a low-frequency transformer (LFT) and a standard bidirectional three-phase PFC rectifier. Alternatively, to avoid the volume and weight penalty of an LFT, the three-phase PFC can directly interface the mains and a subsequent bidirectional isolated DC-DC converter provides the galvanic separation with a high-frequency (HF) transformer, see **Fig. 1.15b**. Thus, the DC voltage level can advantageously be selected independently from the grid voltage. For example, [158] employs a dual-active bridge (DAB) DC-DC converter, and [159] describes an isolation stage based on an unregulated series-resonant DC-DC converter ("DC transformer") and an integrated DC-bus midpoint balancing stage required by the amplifier's three-level bridge-legs.

CHB Topologies

Whereas parallel-interleaved topologies require a power supply with a single isolated DC interface, CHB systems need one isolated DC interface per cell. A first, robust approach shown in **Fig. 1.15c** employs a low-frequency multi-winding transformer and individually-controlled three-phase PFCs in each converter cell, see [87] and **Section 3.3**. By employing a special phase-shifting

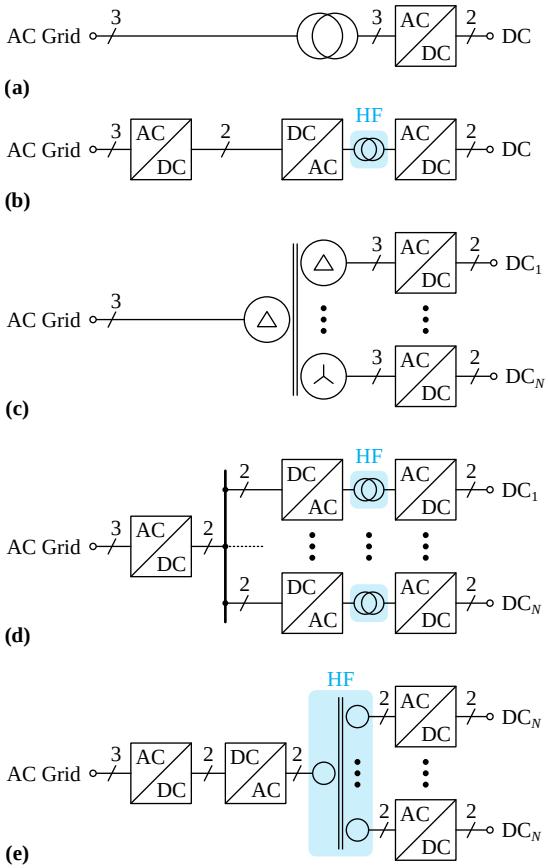


Fig. 1.15: Concepts for providing isolated DC supply voltages to the power amplifier stages. Parallel-interleaved amplifiers can be supplied **(a)** via a grid-frequency transformer and a PFC rectifier or **(b)** via a grid-side PFC rectifier and a downstream isolated DC-DC converter with a high-frequency (HF) isolation transformer. For series-interleaved power amplifier stages, multiple isolated DC ports are required: **(c)** shows a low-frequency multi-winding transformer with several secondary-side PFC rectifiers (one per cascaded cell). Alternatively, a shared PFC rectifier stage can be employed in combination with **(d)** several isolated DC-DC converters operating from a common DC bus, or **(e)** an integrated isolated DC-DC converter featuring a high-frequency multi-winding transformer [160].

multi-winding transformer, which achieves harmonic cancellation similar as known from multipulse rectifier systems, the input filters of the cells' three-phase active rectifiers can be omitted [4], resulting in more compact designs.

Alternatively, again high-frequency isolation concepts can be employed. **Fig. 1.15d** shows a solution with a shared grid-connected three-phase PFC rectifier and dedicated isolated DC-DC converters for each cell, which can be realized, e.g., as LLC series resonant converters [85, 155]. The primary-side DC-AC stages can be (partially) integrated, resulting in I3DAB [161] or I3SRC [162] structures. Ultimately, an integrated multi-port series-resonant DC-DC converter with an HF multi-winding transformer could be employed [160].

For the design of the UH-PBW amplifier prototype developed in this thesis, the low-frequency (LF) isolation approach depicted in **Fig. 1.15c** consisting of an LF isolating transformer and an individual PFC rectifier for each converter cell was finally selected. Although a low-frequency transformer may be relatively bulky, this approach was preferred over the high-frequency (HF) isolation concepts since it features high robustness against grid transients, straightforward scalability to higher voltage levels, and comparably low complexity (fewer switches as compared to a solution with individual isolated DC-DC converters, and independent per-cell local control of the PFC rectifier). Further details regarding the power supply of UH-PBW amplifiers are discussed in **Chapter 2**, where a detailed investigation of two specific aspects occurring in the design process of a UH-PBW system is provided. These include a dimensioning procedure for the DC-link capacitance of a PFC rectifier employed in the power supply of a UH-PBW amplifier, guaranteeing sufficient decoupling between grid and load power demand such that the low-frequency grid current distortions occurring from single-phase output loads are mitigated (**Section 2.1**), as well as an optimized modulation scheme for an integrated multi-port DAB DC-DC converter intended for a CHB converter that aims for an efficiency improvement for asymmetric part load operation (**Section 2.2**).

1.2.3 Amplifier Output Control

As indicated in **Fig. 1.12**, an amplifier's control system receives an output voltage (or output current) reference from a higher-level application (e.g., a power grid or a motor model; a discussion is beyond the scope of this thesis) and must ensure that the amplifier's output closely tracks that reference. To do so, the control system processes the reference and measured voltages and

currents to ultimately generate the gate signals for the amplifier's power transistors. In a wider sense, the control system also must ensure a constant DC input voltage of the amplifier, i.e., control the mains interface. As standard methods can be employed here, the following discussion only focuses on key aspects of the actual output voltage control of the amplifier.

Sensors, Sampling, Signal Processing, and Modulation

Multi-level systems essentially require several modulators that operate with phase-shifted carriers, whereby accurate phase-shifts are needed to ensure the beneficial cancellation of harmonics discussed above. As discussed, e.g., in [164], analog PWM modulation ("naturally sampled PWM") can achieve better performance in terms of bandwidth than regularly sampled PWM (i.e., single- or double-update mode, which introduces relatively long delays in the control loop); note that this can be improved by advanced multirate modulator techniques for parallel- or series-interleaved converters such as described in [165,166]). However, in case of analog implementations, component tolerances and temperature dependencies of their characteristics lead to difficulties in maintaining accurate carrier phase-shifts. Therefore, fully-digital implementations are preferable.

As shown in [167], oversampling can be used to approximate analog modulation. Oversampling ratios (i.e., number of PWM reference updates per PWM period) of about 8…16 already result in *quasi-analog* behavior. However, considering UH-PBW amplifiers with effective switching frequencies that can reach, e.g., the 5 MHz range, this first implies the need for current sensors with sufficiently high bandwidth to capture the corresponding current ripple, i.e., advanced hybrid sensors such as [168], featuring bandwidths of 20 MHz to 50 MHz, are needed. Second, the signal processing system must be capable of acquiring measurements at a sampling rate in the order of 80 MS/s (for an oversampling ratio of 16 and $f_{\mathrm{s,eff}} = 5\,\mathrm{MHz}$), and updating at least the current control loop at the same rate. Modern FPGAs can offer the corresponding computing power, but large parts of the controller must be programmed using a hardware description language such as VHDL. Finally, at these very high effective switching frequencies, which are much closer to typical FPGA clock frequencies (e.g., 100 MHz to 200 MHz) than in normal PWM converter topologies, care has to be taken regarding quantization effects, i.e., limited resolution of digitally generated PWM signals. This may become an issue especially for applications that require high resolution of the output voltage, e.g., to generate very low output voltages for controlling a current in a low-

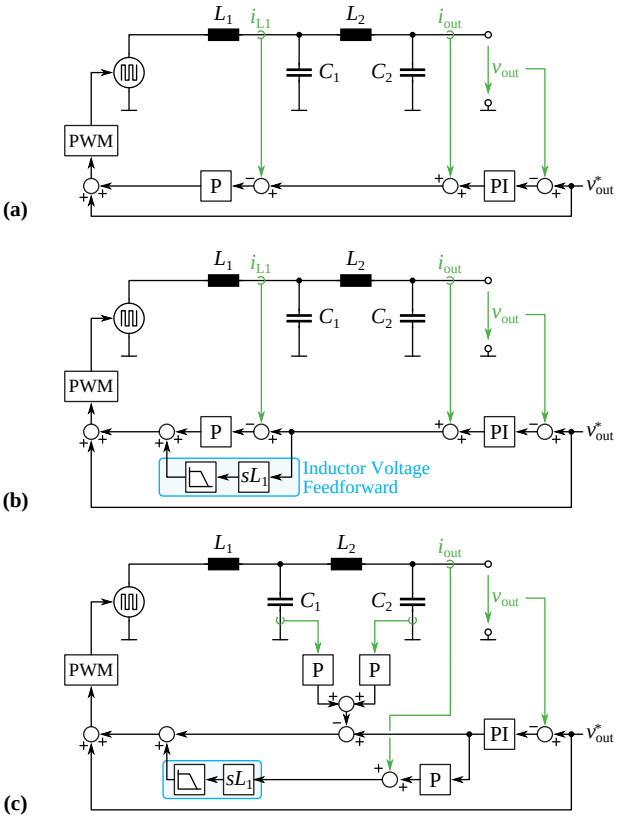


Fig. 1.16: Exemplary multi-loop control structures for switched-mode amplifiers with two-stage LCLC output filters. **(a)** Two-loop cascaded output voltage and inductor current control. **(b)** Control schematic of **(a)** extended by a feedforward of the inductor voltage to increase the current loop bandwidth, see [53]. **(c)** Alternative approach using capacitor current feedback to actively damp the filter's resonant pole, and direct PI control of the output voltage [97, 163]. The structures are simplified; i.e., delays, measurement and reference filters, etc. are not explicitly shown.

impedance load [53]. It may then become necessary to resort to advanced modulator implementations such as described in [169].

Control Structures

Even though so far only single-stage output filters have been discussed for the sake of clarity, practical power amplifier systems typically require a two-stage LCLC filter to achieve the desired output voltage quality [96]. Therefore, the following brief discussion of control structures considers such a two-stage filter, see **Fig. 1.16**.

Literature documents manifold methods for controlling the output voltage (or current) of an inverter with a two-stage LCLC filter. Whereas also advanced approaches such as (model) predictive control [39, 66, 146, 150] have been proposed, the most straightforward option is a cascaded control structure with an inner, fast current control loop and an outer, slower, voltage control loop, see **Fig. 1.16a**. The bandwidth of the current control loop can be improved by adding a feedforward of the inductor voltage [53], see **Fig. 1.16b**. An alternative multi-loop control scheme directly controls the output voltage with a PI controller, and employs capacitor current feedback to actively damp the filter's resonant pole [97, 163], see **Fig. 1.16c**. This structure has been found to achieve highest output voltage control bandwidth [53]. A detailed discussion and comparison of this and similar multi-loop control schemes is beyond the scope of this chapter; interested readers are referred to [53, 97, 163] instead, and to [170] for a detailed stability analysis and extensions for output impedance emulation (instead of direct output voltage or current control). Furthermore, the analysis and design of the control system for the CHB-based UH-PBW amplifier with a two-stage LC output filter designed in this thesis is covered in detail in **Chapter 4**.

1.2.4 Discussion

The main focus in the design process of a UH-PBW amplifier lies on the amplifier stage itself since this entity usually limits the achievable performance. In this regard, the advantageous properties of parallel- and series-interleaved topologies become clearly evident if the design of the switching stage is combined with the dimensioning of the output filter, where combining different constraints regarding the quality of the output voltage as well as the reactive power demand of the filter elements allows to derive an expression for the required switching frequency as a function of the number of half-bridges. The resulting $1/N_{\mathrm{HB}}^{3/2}$ dependency of the required switching frequency clearly shows

that a massive reduction of the required switching frequency can be accomplished by increasing the number of employed half-bridges. Furthermore, an advantage of the series-interleaved CHB topology over a parallel-interleaved approach arises from the $1/N_{HB}$ dependency of the DC-link voltage of the employed converter cells, which enables to use semiconductors with lower blocking voltage that allow higher switching frequencies. However, the CHB topology requires a more complex power supply since each converter cell requires its own isolated and bidirectional power supply, whereas in case of a the parallel-interleaved architecture only a single DC-link voltage is required.

Independent of the selected topology, also a careful design of the control unit is required, which refers to the measurement front-ends as well as the execution of the controllers and the PWM modulation on a high performance digital platform. In case of the PWM signal generation, natural sampled PWM modulation is preferred over uniform sampling modulation to avoid unnecessary sampling delay times of the modulator. Regarding data acquisition, oversampling with sampling rates of 8…16 times the effective switching frequency is advantageously employed. Considering effective switching frequencies in the megahertz range, this implies sampling rates in the order of 80 MHz. For this reason, high performance FPGAs that offer sufficient computational power are required for the execution of the control loop.

1.3 Thesis Outline

The focus of this thesis is the scientific investigation and development of a switched-mode 230 V/10 kW UH-PBW amplifier that enables large-signal output frequencies of up to 100 kHz, intended for application in a P-HIL testing environment. Although the converter is intended for the application as a three-phase test source being part of a P-HIL testing facility, only a single phase is considered in the development since a potential three-phase application can be composed from three identical single-phase units. An overview of the resulting system developed in the course of this thesis is provided in **Fig. 1.17**, with the key specifications listed in **Tab. 1.1**.

As already mentioned in **Section 1.2**, the system can be distributed into three main building blocks. These are the amplifier stage with the output filter that generate the output voltage, the power supply that provides the operating voltage for the amplifier stage and interfaces the grid and an output voltage control unit to control the amplifier stage. As stated in **Section 1.2.1**, the series-interleaved CHB topology is selected for the implementation of the amplifier stage, mainly since it allows to utilize power semiconductors with a

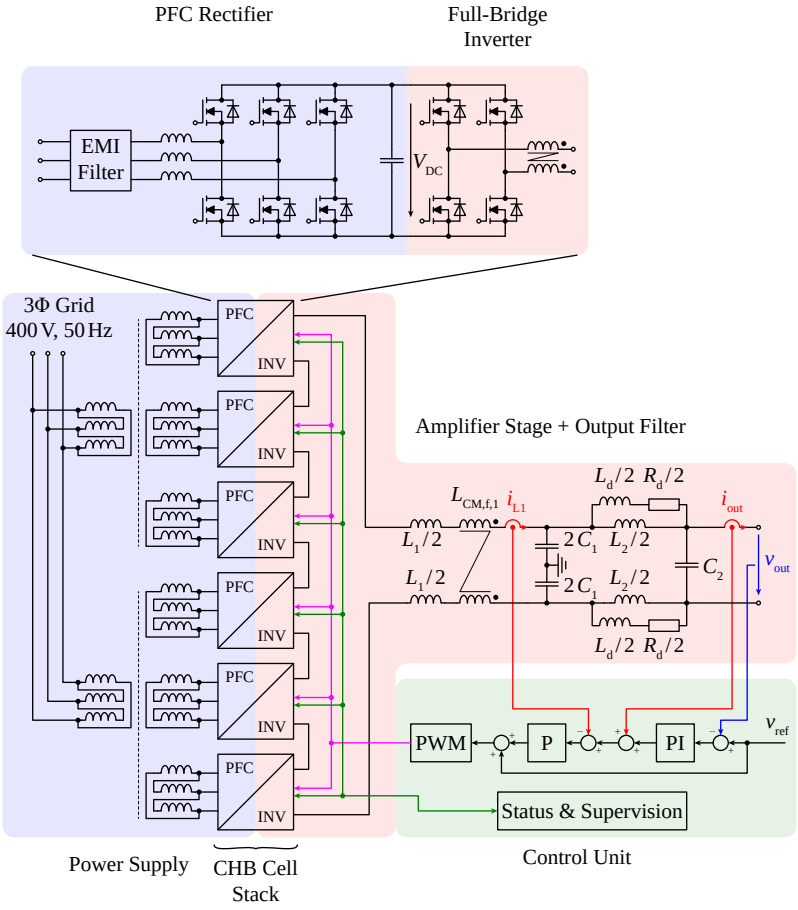


Fig. 1.17: Schematic overview of the UH-PBW amplifier system investigated in this thesis featuring a CHB topology. The system can be distributed into three main building blocks: the amplifier stage containing the full-bridge inverter stage and the output filter, the control unit and the power supply which incorporates two multi-winding LF transformers and an individual PFC rectifier for each converter cell.

Tab. 1.1: Key characteristics of the UH-PBW amplifier prototype shown in **Fig. 1.17** developed in this thesis.

Parameter	Value	
Single-phase AC power	10	kW
DC power	20	kW
Output voltage (AC peak)	325	V (nominal)
	470	V (max.)
Output voltage (DC)	±500	V
Output current (DC, AC peak)	61.5	A
Output current (AC RMS)	44	A
Cell DC voltage	100	V
Number of cells	6	
Switching frequency	300	kHz
Eff. sw. frequency	3.6	MHz
Min. output frequency	0	Hz
Max. output frequency	100	kHz (at nom. volt./power)

lower blocking voltage that enable higher switching frequencies compared to an equivalent parallel-interleaved converter. The CHB cell stack consists of $N_{\text{cell}} = 6$ converter cells, with the inverter half-bridges of the amplifier stage being operated with a switching frequency of 300 kHz, thereby resulting in a multi-level output voltage of the cell stack with 13 levels and an effective switching frequency of 3.6 MHz. Regarding the power supply, an LF isolation approach (cf. **Section 1.2.2**) is selected, i.e., each converter cell contains a three-phase PFC rectifier that generates a stabilized DC-link voltage of 100 V from the secondary-side of an LF multi-winding transformer that provides galvanic isolation and steps down the voltage. Furthermore, an output voltage control unit is required, where a fully-digital linear cascaded controller is implemented on a high performance FPGA.

The content of this thesis is structured into the following five chapters, among which each of the above mentioned sub-blocks is examined in a separate chapter:

- **Chapter 2** covers two independent aspects of the power supply for a UH-PBW amplifier system. On the one hand, it is investigated how LF single-phase loads operated at the amplifier's output can lead to distortions of the amplifier system's grid currents. The power pulsation

of the load may complicate compliance with certain grid standards. In order to mitigate these distortions, sufficient decoupling between load and grid power flow has to be ensured, where on the example of the IEC 61000-3-11 harmonic and IEC 61000-3-12 flicker standards, a dimensioning criterion for the DC-link capacitance of a three-phase PFC rectifier is presented such that compliance with these regulations can be guaranteed. On the other hand, an advanced modulation scheme for a multi-port DAB intended as power supply for a CHB converter is discussed, which improves the efficiency of the supply under certain asymmetric part load conditions.

- **Chapter 3** investigates the design process of the switched-mode amplifier stage and discusses important relations such as the required number of converter cells of the phase stack. Furthermore, a filter design optimization maximizing the large-signal bandwidth of the system while considering boundary conditions such as a limited voltage dip during load transients is conducted and details about the hardware implementation of the prototype are given.
- **Chapter 4** illustrates the design of a linear cascaded control structure for a UH-PBW amplifier and presents a Pareto optimization used to maximize the dynamic performance of the system. Furthermore, it is investigated how the locking mechanism of the natural sampled PWM modulator required to avoid multiple switching events per PWM period can degrade the transient response of the converter and according countermeasures are suggested.
- **Chapter 5** presents the experimental measurement results obtained from the prototype system designed and built in the course of this thesis and verifies the theoretical considerations obtained in the design process.
- **Chapter 6** summarizes the key results of this thesis and presents an outlook on further research.

1.4 List of Publications

Key findings obtained in this thesis have been published in international scientific journals or conference proceedings, others have been covered by according patents. A list of the publications created in the course of this thesis is given in the following:

- J. Böhler, J. Huber, J. Wurz, M. Stransky, N. Uvaidov, S. Srdic and J. W. Kolar, "Ultra-High-Bandwidth Power Amplifiers: A Technology Overview and Future Prospects," *IEEE Access*, 2022. DOI: 10.1109/ACCESS.2022.3172291, [PDF].
- J. Böhler, F. Krismer, T. Sen and J. W. Kolar, "Optimized Modulation of a Four-Port Isolated DC–DC Converter Formed by Integration of Three Dual Active Bridge Converter Stages," *Proc. of the IEEE International Telecommunications Energy Conference (INTELEC)*, Torino, Italy, October 2018. DOI: 10.1109/INTLEC.2018.8612312, [PDF].
- J. Böhler, F. Krismer and J. W. Kolar, "Analysis of Low Frequency Grid Current Harmonics Caused by Load Power Pulsation in a 3-Phase PFC Rectifier," *Proc. of the 2nd International Smart Grid and Renewable Energy Conference (SGRE)*, Doha, Qatar, November 2019. DOI: 10.1109/SGRE46976.2019.9020959, [PDF].
- F. Krismer, J. Böhler, G. Pammer and J. W. Kolar, "New Series-Resonant Solid-State DC Transformer Providing Three Self-Stabilized Isolated Medium-Voltage Input Ports," *Proc. of the 10th International Power Electronics Conference (ICPE/ECCE Asia)*, Busan, South Korea, May 2019. DOI: 10.23919/ICPE2019-ECCEAsia42246.2019.8797161, [PDF].
- J. W. Kolar, F. Krismer and J. Böhler, "Mehrphasiger potentialgetrennter Gleichspannungskonverter (in German)," World Patent Application WO2020070167A1, 2019. DOI: not available, [PDF].

2
Power Supply

Independent of the amplifier topology itself (see **Section 1.1**), every power amplifier requires a power supply that generates the necessary DC-link voltage (or voltages) for the amplifier stage and typically interfaces a feeding low-voltage (LV) (e.g., 400 V/50 Hz) three-phase grid. Since the power supply has to provide bidirectional power transfer capability in order to guarantee full four-quadrant operation of the amplifier system, an active front-end has to be employed. Additionally, the power supply has to provide sinusoidal grid currents in order to comply with various standards that grid connected appliances generally have to fulfill. Besides the well-known EMI regulations (e.g., CISPR 11) this also includes the IEC 61000-3-11 and IEC 61000-3-12 harmonic and flicker limitations. These are of special relevance for a UH-PBW amplifier system in case of operation with single-phase loads and low output frequencies, e.g., output frequencies below the grid frequency of 50 Hz. Due to the LF power pulsation occurring for these operating points, according LF distortions of the grid currents result, which complicate compliance with the IEC 61000-3-11 and IEC 61000-3-12 standards. Therefore, sufficient decoupling between load and grid power must be provided, which results in special considerations regarding the dimensioning of the DC-link energy storage, i.e., the size of the DC-link capacitance. These aspects are investigated in detail in **Section 2.1**, which presents a dimensioning procedure for the DC-link capacitor of a three-phase PFC rectifier operated with a generic single-phase inverter as a load that has to fulfill the IEC 61000 standards cited before. Although the investigation is conducted at the example of a single 700 V/20 kW PFC rectifier assuming an amplifier stage that requires a single power supply, the obtained design constraints are equally applicable to the distributed power supply of a CHB converter introduced below.

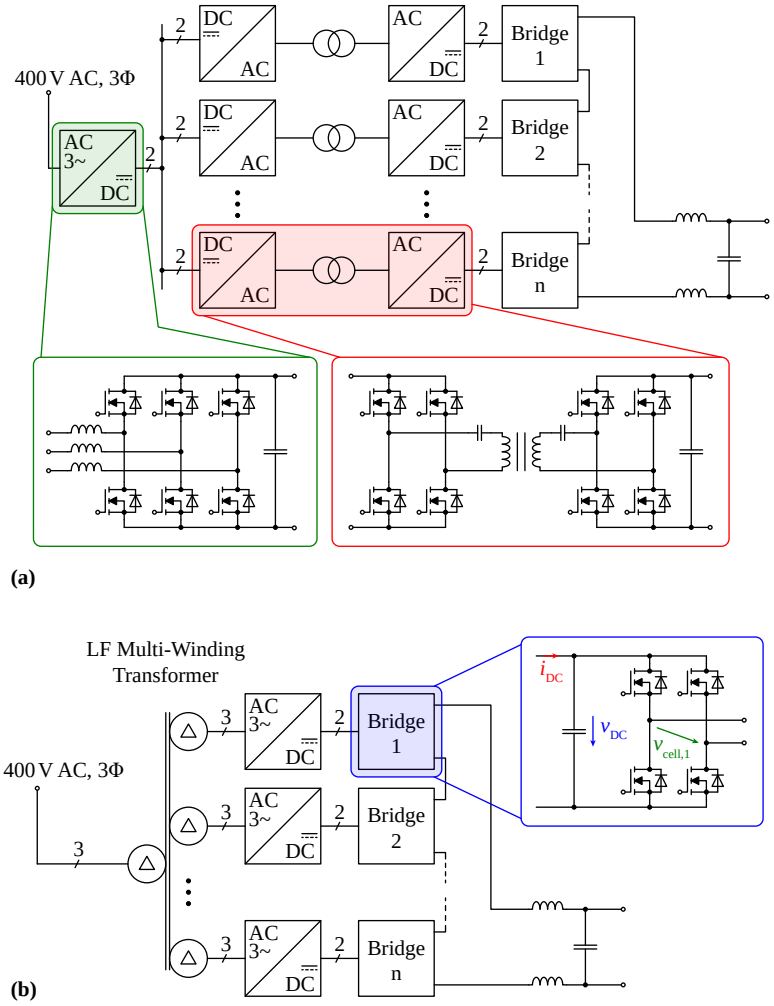


Fig. 2.1: Power supply structures for the CHB cells. **(a)** Individual isolated DC-DC converter for each cell and common front-end PFC rectifier. **(b)** LF transformer and individual PFC rectifier stage for each converter cell. Only the arrangement of a single output phase stack is shown.

Considering the CHB topology selected for the implementation of the UH-PBW amplifier in **Section 1.2.1**, it has to be mentioned that instead of a single DC-link voltage for the entire amplifier stage a separate isolated DC-link voltage is required for each of the converter cells, i.e., each cell requires an individual galvanically isolated bidirectional power supply. Typically two approaches can be distinguished on how to implement such a power supply structure, which are illustrated in **Fig. 2.1** and mainly differ by whether an LF transformer (as in [4, 87, 171]) or an HF transformer (e.g., in [85, 172–174]) is used.

The realization approach illustrated in **Fig. 2.1a** uses an individual isolated DC-DC converter incorporating an HF transformer for each cell to provide galvanic isolation and voltage scaling. The primary side (i.e., grid side) of the DC-DC converters is fed from a common DC-bus with a voltage of typically 650 V to 700 V for a 400 V/50 Hz grid, which is generated by a single non-isolated PFC stage directly connected to the grid. For the DC-DC converters, any bidirectional isolated DC-DC topology (e.g., a Dual-Active Bridge (DAB) converter [172], a Series Resonant Converter (SRC) [173], or an LLC converter [174]) can be used. Furthermore, instead of employing a dedicated DC-DC converter for each converter cell, a certain reduction of the component count can be achieved by employing multi-port DC-DC converter topologies such as the I3DAB or the I3SRC [161, 162]. Therefore, a novel modulation scheme for a multi-port I3DAB is presented in **Section 2.2**, which minimizes the RMS current and hence the conduction losses under certain asymmetric operating conditions that could occur if the investigated I3DAB converter is used as a cell power supply for a general three-phase CHB converter system.

In order to avoid the relatively high complexity of the described multi-stage power conversion, an interesting alternative is to employ an LF multi-winding transformer, where each cascaded converter cell is connected to a dedicated secondary winding by its own PFC rectifier, as illustrated in **Fig. 2.1b**. The main advantage of this approach lies in the reduced complexity of the system since no intermediate converter stage except the PFC lies between the cell and the grid. However, this comes at the price of a relatively high volume and weight of the required transformer. If only unidirectional power flow is required, the PFC rectifier stage can be replaced by a passive diode rectifier, which further reduces system complexity while still being able to achieve an acceptable power factor, especially if suitable winding combinations on the secondary side are employed to eliminate certain harmonics on the grid current [175, 176]. For the realization of the amplifier prototype ultimately the LF isolation approach from **Fig. 2.1b** has been cho-

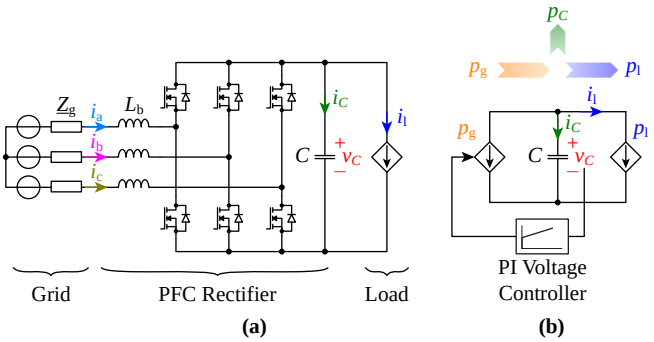


Fig. 2.2: (a) Schematic drawing of a two-level three-phase boost type PFC rectifier and **(b)** equivalent circuit illustrating the relations between instantaneous power levels at the DC side. The output load features a controlled-power sink characteristic, i.e., $p_l(t)$ tracks a defined time-varying reference.

sen due to its simplicity that allows for rapid development. Details about the implementation are given in **Chapter 3.3**.

2.1 Impact of Low-Frequency Power Pulsation on Grid Current Distortion

This section discusses the impact that LF single-phase loads operated at the output of the amplifier have on the grid currents of the UH-PBW system, where load frequencies ranging from DC to 200 Hz are considered. The investigation is based on the key findings that have already been published in [157] and considers the model depicted in **Fig. 2.2a**, consisting of a three-phase PFC rectifier stage which feeds a constant power sink used to model the power demand of the output amplifier stage via a common DC-link. For the load power consumed by the amplifier, the characteristic power demand of an ohmic resistor at a sinusoidal voltage is assumed, i.e., the consumed power demand exhibits a DC component corresponding to the average power and a superposed AC power pulsation of identical amplitude and twice the frequency of the excitation voltage.

Due to the limited internal energy storage capability of a PFC rectifier, i.e., because of its limited DC-link capacitance, low-frequency grid current distortions occur if a power stage connected to the load-side of the PFC

rectifier demands for a sinusoidal power waveform of adjustable amplitude, offset and low frequency, since a substantial part of this fluctuating power may appear at the grid side. In this regard, different regulations exist, e.g., the IEC 61000 harmonic and flicker standards, which define limits for the maximum allowable levels of distortion. For this reason, in order to still be able to comply with IEC standards, these grid current harmonics have to be limited, which implies a certain minimum energy storage, i.e., a minimum size of the DC-link capacitor of the PFC rectifier. Consequently, according design constraints for the minimum required DC-link capacitance are required, which are derived in the following. Alternative approaches found in literature to eliminate or attenuate the grid current distortions in a PFC rectifier caused by LF pulsating power demands include the use of (self-tuning) notch-filters [177–179], fuzzy controllers [180], adaptive PI-voltage controllers [181], the subtraction of a precalculated correction signal to reject the ripple voltage [182], and three-phase systems where the power fluctuations in the three different phases are phase-shifted by 120° [183–187]. However, the presented methods investigate power fluctuations with characteristic frequencies equal to twice the mains frequency or compensation mechanisms in three-phase systems, which both denote restrictions that cannot be transferred to the converter system investigated in the case at hand.

Since only low load frequencies are considered, the obtained findings are independent of the topology of the amplifier stage, i.e., the system modeled by the power sink in **Fig. 2.2a** could be a parallel-interleaved system or a CHB converter. In case of parallel interleaved power amplifiers, the obtained minimum of the DC-link capacitance can be directly applied to the design of the PFC's DC-link capacitor, whereas in case of a CHB converter the topology of the power supply structure (cf. **Fig. 2.1**) has to be considered. If the LF isolation approach is used, the required capacitance has to be rescaled according to the transformer's turns ratios and equally distributed between the CHB cells. In case of HF isolation, the dynamics of the incorporated DC-DC converters should generally be negligible for the considered frequencies, which allows to either place the required capacitance in the DC-link of the common PFC stage or again distributed between the converter cells.

This section is structured as follows: **Section 2.1.1** details the calculation of the rectifier's grid current waveforms for sinusoidal load-side power levels while **Section 2.1.2** summarizes the limitations set by the relevant IEC 61000 harmonic and flicker standards. **Section 2.1.3** investigates the implications of the rectifier's controller settings on the obtained grid current waveforms. Finally, **Section 2.1.4** combines the analytical findings to identify the frequency

Tab. 2.1: Specifications of the exemplary PFC rectifier.

Parameter	Value
Grid voltage amplitude (phase-to-neutral), $\hat{v}_\mathrm{g}$	$\sqrt{2} \times 230\,\mathrm{V}$
Grid frequency, f_g	50 Hz
DC-link voltage, $V_{C,0}$	700 V
Nominal output power, P_nom	20 kW
Output frequency, f_l	DC to 200 Hz
Maximum DC voltage ripple, $\hat{V}_{C,\mathrm{max}}$	70 V (10 % $V_{C,0}$)
Boost inductance, L_b	1.63 mH
Switching frequency, f_s	20 kHz

characteristic of allowable levels of output power, i.e., without violating the corresponding standards, and presents a dimensioning procedure for the DC-link capacitance of an exemplary PFC rectifier with a rated power of 20 kW.

2.1.1 Grid Current Waveforms

Fig. 2.2a depicts the circuit schematic of the considered three-phase PFC rectifier with grid-side boost inductors, L_b, a linear grid model, which is composed of three voltage sources with inner impedances, $\underline{Z}_\mathrm{g}$ (underlined designators denote complex-valued variables), and the load. **Tab. 2.1** lists the main system specifications.

The calculation of the PFC rectifier's grid current is based on the instantaneous value of the input power,

$$p_\mathrm{g}(t) = p_C(t) + p_\mathrm{l}(t), \tag{2.1}$$

where $p_C(t)$ is the instantaneous power of the DC-link capacitor,

$$p_C(t) = v_C\, C \frac{\mathrm{d}v_C}{\mathrm{d}t}, \tag{2.2}$$

and $p_\mathrm{l}(t)$ the fluctuating, sinusoidal power demand of the load,

$$p_\mathrm{l}(t) = P_0 - \hat{P}_\mathrm{l}\, \cos(2\pi f_\mathrm{l}\, t), \tag{2.3}$$

featuring DC bias, P_0, AC amplitude, $\hat{P}_\mathrm{l}$, and frequency, f_l. The analysis further considers small-signal excitations at the DC-link and, in this regard, assumes

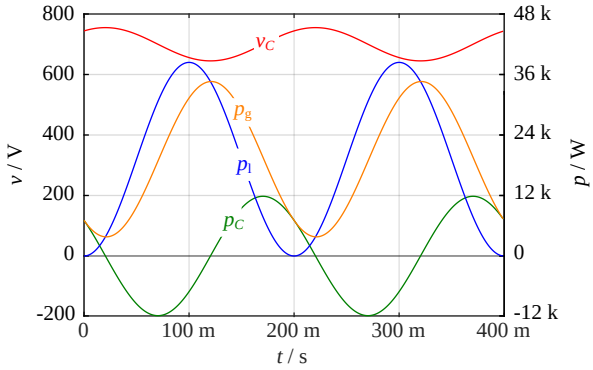


Fig. 2.3: Simulation waveforms of the DC-link voltage, v_C, and instantaneous power levels, p_g, p_C, and p_l (cf. **Fig. 2.2**) for $C = 10\,\text{mF}$, $K_p = 0.586\,\text{A/V}$, $T_i = 850\,\text{ms}$ and $p_l(t) = 20\,\text{kW}[1 - \cos(2\pi\,5\,\text{Hz} \times t)]$. Due to the low load frequency of 5 Hz and the specified maximum allowable amplitude of the DC-link voltage of 70 V, the energy storage capability of the DC-link capacitor is insufficient to cover the energy demand of the load and a high fluctuation of the power demand from the grid, p_g, results.

a sinusoidal voltage ripple being superimposed on the DC-link voltage, $V_{C,0}$,

$$v_C = V_{C,0} + \hat{V}_C \cos(2\pi f_l t + \varphi_C), \tag{2.4}$$

with amplitude $\hat{V}_C$ and phase-shift φ_C, which will be determined using the transfer functions derived in **Section 2.1.3** for the controlled system. The frequency of the superimposed voltage ripple stems from the load power demand (2.3). **Fig. 2.3** provides an illustration of the above equations, using

$$\begin{aligned} &P_0 = \hat{P}_l = 20\,\text{kW}, \quad K_p = 0.586\,\text{A/V}, \quad T_i = 850\,\text{ms}, \\ &C = 10\,\text{mF}, \quad \hat{V}_C = 55\,\text{V}, \quad f_l = 5\,\text{Hz}, \quad \varphi_C = -36.7^\circ, \end{aligned} \tag{2.5}$$

i.e., for a selected design, a defined voltage controller, and a typical operating point of the PFC rectifier. Expressions (2.1) to (2.4) enable the derivation of the grid current $i_g = i_d$, which, in the synchronous dq reference frame (d component oriented in the direction of the grid voltage v_g, $v_d = \hat{v}_g$), is

$$\begin{aligned} i_d = \frac{p_g}{\frac{3}{2} v_d} = \frac{2}{3 v_d} \Big[& P_0 - \hat{P}_l \cdot \cos(2\pi f_l t) \\ & - V_{C,0}\, \hat{V}_C\, 2\pi f_l C\, \sin(2\pi f_l t + \varphi_C) \Big], \end{aligned} \tag{2.6}$$

if the second-order terms are neglected that arise in the course of the evaluation of (2.2). **Fig. 2.4a** depicts the corresponding phase currents,

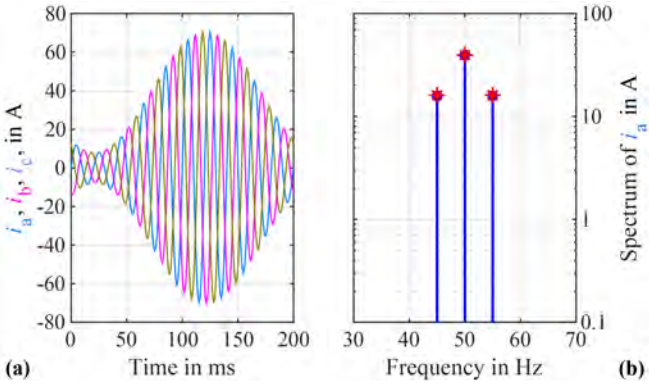


Fig. 2.4: (a) Simulated grid-side phase currents and **(b)** corresponding amplitude spectrum of each phase (same spectra result for all three phases; blue: simulation, red stars: calculation with (2.9)). The shown results consider operation according to (2.5), i.e., DC-link voltage and instantaneous power waveforms of **Fig. 2.3** apply. The common envelope of the phase currents is directly proportional to $p_g(t)$ since the amplitudes of the grid phase voltages are assumed to be constant.

$$i_{\{a,b,c\}} = i_d \sin(2\pi f_g t + \varphi_{\{a,b,c\}}), \tag{2.7}$$

$$\varphi_{\{a,b,c\}} = \{0, -120^\circ, 120^\circ\}, \tag{2.8}$$

for the operating point defined with (2.5). The spectra corresponding to $i_{\{a,b,c\}}(t)$, cf. **Fig. 2.4b**, reveal sidebands located at $f_g - f_l$ and $f_g + f_l$, where both sidebands feature identical amplitudes,

$$\hat{I}_{g,1} = \frac{1}{3v_d}\left[\hat{P}_l^2 + 2\,\hat{P}_l\,V_{C,0}\,\hat{V}_C\,2\pi f_l C\,\sin(\varphi_C) + (V_{C,0}\,\hat{V}_C\,2\pi f_l C)^2\right]^{\frac{1}{2}}. \tag{2.9}$$

It is worth noting that (2.9) defines a linear relation between $\hat{I}_{g,1}$ and $\hat{P}_l$ since the ripple amplitude $\hat{V}_C$ scales linearly with $\hat{P}_l$. Expression (2.9) has been successfully verified by means of circuit simulations at numerous different operating points and different DC-link capacitances. **Fig. 2.4b** reveals close matching of calculated (blue circles) and simulated (red stars) results for the operating point defined with (2.5). For the considered system it is found that the relative error between calculated and simulated sideband amplitude, $\hat{I}_{g,1}$, is below 2 %.

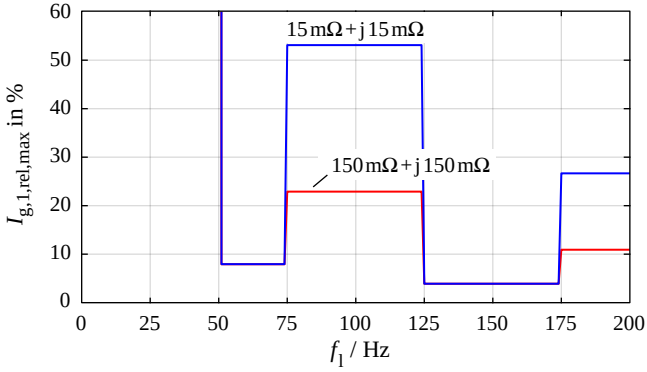


Fig. 2.5: Frequency characteristic of the maximum allowable sideband amplitudes of the grid current to comply with IEC 61000-3-12 (grid current harmonics), shown for two different grid impedances. The amplitudes are given as percentages of the frequency component at mains frequency, $\hat{I}_{g,0}$, which is proportional to the average output power, i.e., $\hat{I}_{g,0} = 2\,P_0/(3\,v_d)$.

2.1.2 Harmonic Limits and Flicker

This section summarizes the maximum allowable grid current distortions defined in the grid standards IEC 61000-3-11 and IEC 61000-3-12, for flicker and grid current harmonics, respectively. Both standards apply to the considered converter system with a rated power of $P_{nom} = 20\,\text{kW}$. Since the evaluation of the limits defined by both standards requires a defined value of the grid impedance, $\underline{Z}_g$, two substantially different grid impedances of $\underline{Z}_g = 15\,\text{m}\Omega + \text{j}\,15\,\text{m}\Omega$ and $\underline{Z}_g = 150\,\text{m}\Omega + \text{j}\,150\,\text{m}\Omega$ are taken as examples for a strong and a weak grid, respectively.

Harmonic Current Limitations (IEC 61000-3-11)

IEC 61000-3-12 defines relative current amplitudes that depend on the short circuit power ratio,

$$R_{sce} = \frac{S_{sc}}{P_{nom}} = \frac{3\,\hat{v}_g^2}{2\,Z_g} \cdot \frac{1}{P_{nom}} = \begin{cases} 374 \text{ for } Z_g = 21\,\text{m}\Omega, \\ 37.4 \text{ for } Z_g = 212\,\text{m}\Omega, \end{cases} \tag{2.10}$$

where $Z_g = |\underline{Z}_g|$ denotes the absolute value of the grid impedance. **Fig. 2.5** shows the envelopes of the maximum allowed relative RMS values of the

sideband currents (calculated with (2.9)),

$$I_{\mathrm{g},1,\mathrm{rel},\max} = \frac{\hat{I}_{\mathrm{g},1,\max}}{\hat{I}_{\mathrm{g},0}}, \tag{2.11}$$

that result for the two short circuit power ratios of (2.10) and as a function of the load frequency f_l ($\hat{I}_{\mathrm{g},0}$ denotes the amplitude of the spectral current component at mains frequency, i.e., at 50 Hz in **Fig. 2.4b**). The depicted result applies to a mains with a RMS phase voltage of 230 V and a frequency of 50 Hz. The discontinuities in the presented envelopes arise from the processing of the spectral components required by IEC 61000 which is also described in [188]. For $0 < f_\mathrm{l} < 50\,\mathrm{Hz}$ no limitation is given since both of the according interharmonic components end up at frequencies smaller than 100 Hz, where the standard does not specify any limitation.

Flicker Limitations (IEC 61000-3-12)

Concerning flicker, the maximum allowable voltage harmonic amplitudes are limited. Thus, the current components at the sideband frequencies need to be multiplied with the grid impedance to determine the distortion of the grid voltage. The obtained waveforms of the phase voltages are processed according to the procedure specified in IEC 61000-4-15 (named *flicker-meter*) that models the response of a human brain to flicker. In this thesis, a readily available implementation has been used [189] to assess flicker,[1] which implements the individual blocks of the human eye-brain model described in the standard. **Fig. 2.6** presents the results of the conducted computation, i.e., the envelopes of the maximum allowed absolute RMS value of each current sideband derived in **Section 2.1.1** as function of the load frequency f_l and for two different grid impedances. Even though the value of the spectral current component at mains frequency, $\hat{I}_{\mathrm{g},0}$, may have an impact on the calculated limits since the signal processing of the flicker-meter is highly nonlinear, the results of numerical evaluations for different values of the mains frequency component reveal that this dependency is negligible. Most stringent limitations are found to apply at low load frequencies, $f_\mathrm{l} \approx 9\,\mathrm{Hz}$, as well as in the vicinity of $f_\mathrm{l} = 100\,\mathrm{Hz}$. In both cases, at least one of the two sidebands ends up at frequencies close to the mains frequency where the standard defines

[1] According to the definitions given in IEC 61000-4-15, equal flicker qualifiers, $P_\mathrm{lt} = P_\mathrm{st}$, have been considered in order to correctly take the operation of the investigated converter system, with continuous LF AC output power, into account. Further related details are described in IEC 61000-4-15.

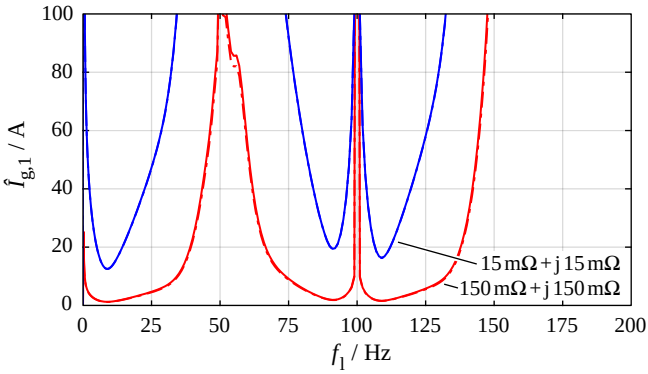


Fig. 2.6: Maximum acceptable sideband amplitudes of the grid current to comply with IEC 61000-3-11 (flicker), being evaluated for two different grid impedances. The shown limits are the maximum amplitudes of the sideband currents.

the strictest limits since the human eye exhibits the highest sensitivity to the eponymous flicker effects occurring in light bulbs at these frequencies.

2.1.3 DC-Link Voltage Controller

Fig. 2.7a presents the considered dynamic model of the controlled PFC rectifier in the synchronous *dq* reference frame, which is valid for Low-Frequency (LF) excitations, e.g., $f_l < 200\,\text{Hz}$. The control system employs a cascaded controller structure, however, the considered model omits the inner control loop, i.e., the phase current control loop used to realize PFC operation since the bandwidth of the inner control loop is assumed to be much higher than the maximum considered excitation frequency. The outer control loop serves for the stabilization of the DC-link voltage and comprises a PI voltage controller and the dynamic LF model of the PFC rectifier's power stage, which resembles the power balance scheme depicted in **Fig. 2.2b**: the power delivered to the DC-link capacitor is the difference between input power and load power,

$$p_g - p_l = \frac{3}{2} i_d v_d - p_l = p_C = v_C i_C, \tag{2.12}$$

and is used to determine the capacitor current and the DC-link voltage,

$$i_C = \frac{p_g - p_l}{v_C}, \qquad v_C(t) = v_C(0) + \frac{1}{C}\int_0^t i_C(\tau)\mathrm{d}\tau. \tag{2.13}$$

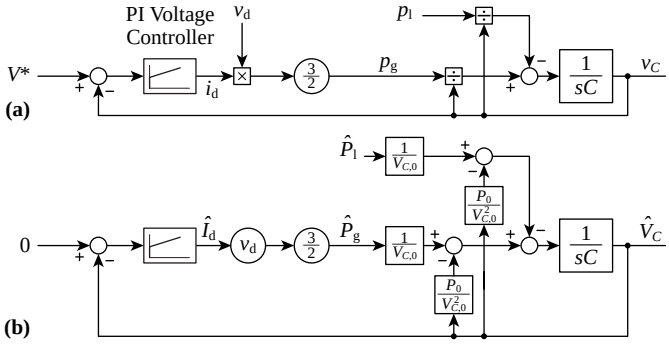


Fig. 2.7: (a) LF large-signal and **(b)** small-signal models of the PFC rectifier in the synchronous *dq* reference frame, for operation with defined load power.

In the course of the development of a small-signal model, the product $i_d \times v_d$ is replaced by a gain of v_d since v_d is assumed to be constant, and the division in (2.13), used to determine i_C, is linearized. Thus,

$$\frac{p_l}{v_C} \approx \frac{P_0}{V_{C,0}} - \frac{P_0}{V_{C,0}^2}\,\hat{V}_C + \frac{1}{V_{C,0}}\,\hat{P}_l \tag{2.14}$$

applies to p_l and a similar expression results for p_g.

Fig. 2.7b depicts the corresponding small-signal model of the PFC rectifier system, which enables the derivation of the transfer functions, e.g., from load power to DC-link voltage,

$$\underline{G}_C = \frac{\hat{V}_C}{\hat{P}_l} = -\frac{s\,T_i}{s^2\,C\,V_{C,0}\,T_i + K_p\,(1 + sT_i)\,\frac{3}{2}\,v_d}. \tag{2.15}$$

Fig. 2.8 shows the Bode plots of $\underline{G}_C$ for three exemplary capacitor values of $C = \{10\,\text{mF}, 20\,\text{mF}, 30\,\text{mF}\}$, $K_p = 0.586\,\text{A/V}$, and $T_i = \{17.3\,\text{ms}, 34.7\,\text{ms}, 52.0\,\text{ms}\}$. This transfer function is found to exhibit a maximum of

$$|\underline{G}_C|_{\max} = \frac{2}{3\,v_d\,K_p} < \frac{\hat{V}_{C,\max}}{\hat{P}_{l,\max}} \Rightarrow K_p \geq K_{p,\min} = \frac{2\,\hat{P}_{l,\max}}{3\,v_d\,\hat{V}_{C,\max}} \tag{2.16}$$

that is independent of C and T_i. This provides a design constraint for K_p since $|\underline{G}_C|_{\max}$ denotes the ratio between maximum ripple of the DC-link voltage, $\hat{V}_C$, and the given load power fluctuation, $\hat{P}_l$. In a final step, the controller's

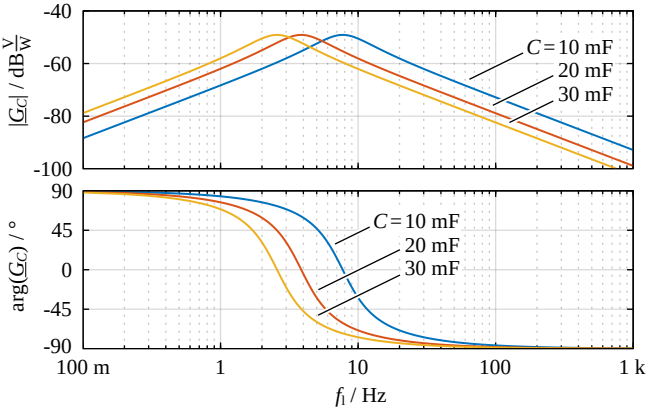


Fig. 2.8: Disturbance transfer function of the PFC rectifier, $\underline{G}_C$, for three different DC-link capacitances. Since the proportional gain of the PI controller is the same for all three cases, also the maximum values of the disturbance transfer functions are of same value.

integrator time constant, T_i, is determined for a defined phase margin of the open-loop transfer function,

$$PM = \arctan\left(\frac{3 v_\text{d} K_\text{p}}{2 C V_{C,0}} \sqrt{\frac{T_\text{i}^2}{2} + \sqrt{\frac{T_\text{i}^4}{4} + \left(\frac{2\,C\,T_\text{i}\,V_{C,0}}{3\,v_\text{d}\,K_\text{p}}\right)^2}}\right). \tag{2.17}$$

Fig. 2.9 depicts the Bode plots of the open-loop transfer functions for $C = \{10\,\text{mF}, 20\,\text{mF}, 30\,\text{mF}\}$, $K_\text{p} = K_{\text{p,min}}$, $PM = 45°$, and the specifications listed in **Tab. 2.1** and reflects a decrease of the resulting transition frequency, from 9 Hz to 3 Hz, for increasing DC-link capacitance.

2.1.4 Dimensioning Example

Fig. 2.10 illustrates the flowchart of the procedure that is used to determine the maximum allowable power fluctuation according to IEC 61000 with respect to load frequency. The procedure considers a discrete number of load frequencies and the load profile of an ohmic AC load, i.e., $\hat{P}_\text{l} = P_0$,

$$f_\text{l} \in \{f_{\text{l},1}, f_{\text{l},2}, \ldots f_{\text{l},n}\}, \tag{2.18}$$

$$p_{\text{l},i} = \hat{P}_\text{l}[1 - \cos(2\pi f_{\text{l},i} t)] \;\; \forall\, i \in \{1, \ldots n\}. \tag{2.19}$$

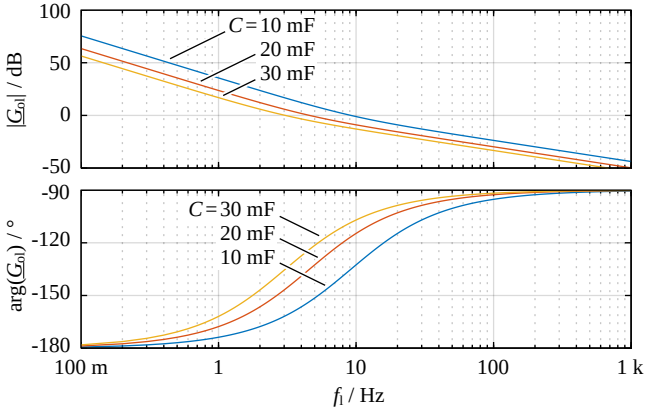


Fig. 2.9: Open-loop transfer functions of the PFC rectifier, $\underline{G}_{ol}$, for $K_p = K_{p,min}$, a phase margin of 45°, the specifications listed in **Tab. 2.1**, and three different DC-link capacitance values, $C = \{10\,mF, 20\,mF, 30\,mF\}$.

The values $f_{l,1} \dots f_{l,n}$ of (2.18) are selected such that improved frequency resolution is achieved in frequency ranges where strong implications on the allowable power fluctuations are expected, i.e., for $f_l < 10\,Hz$ and $90\,Hz < f_l < 110\,Hz$.

In the course of a binary search, the core function of the procedure, denoted *IEC 61000 fulfilled* in **Fig. 2.10**, first determines the phase current distortions according to (2.6), (2.7), and (2.9) for given operating conditions and for known disturbance transfer function, $\underline{G}_C$,

$$\hat{V}_C = \hat{P}_l\,|\underline{G}_C(2\pi f_l)|, \quad \varphi_C = \arg[\underline{G}_C(2\pi f_l)], \tag{2.20}$$

cf. **Section 2.1.3** and (2.15).[2] In a second step, the phase voltage distortion is calculated for a defined grid impedance and, finally, the algorithm tests whether the requirements of IEC 61000, as summarized in **Section 2.1.2**, are fulfilled. **Figs. 2.11** and **2.12** illustrate the dependency of the maximum allowable power levels on frequency and DC-link capacitance, $\hat{P}_{l,max}(f_l, C)$,

[2] The implemented binary search starts with a sufficiently high initial value for $\hat{P}_l$ (here, $\hat{P}_{l,init} = 500\,kW$ has been selected), uses an initial increment or decrement of $\Delta\hat{P}_l = \hat{P}_{l,init}/2$, and successively, i.e., after each evaluation of the methods that test for compliance with regard to IEC 61000, cuts $\Delta\hat{P}_l$ into one half ($\Delta\hat{P}_l \rightarrow \Delta\hat{P}_l/2$) and determines the next value of $\hat{P}_l$. This is repeated until $\Delta\hat{P}_l < \hat{P}_{l,init} \times 10^{-4}$ applies.

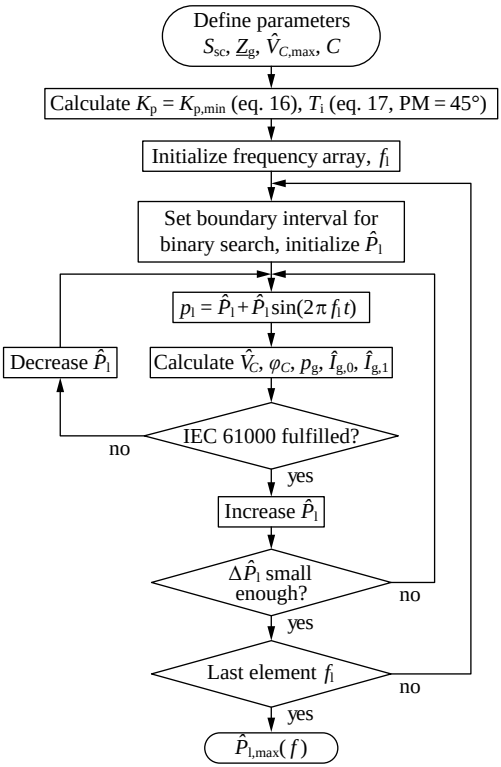


Fig. 2.10: Flow chart of the procedure to determine the maximum available load power at the PFC rectifier output without violating IEC 61000. The maximum feasible power for a predefined set of distinct frequencies is determined by means of a binary search algorithm. An ohmic AC load is assumed, i.e., $\hat{P}_l = P_0$; still, any other relation between $\hat{P}_l$ and P_0 could be used.

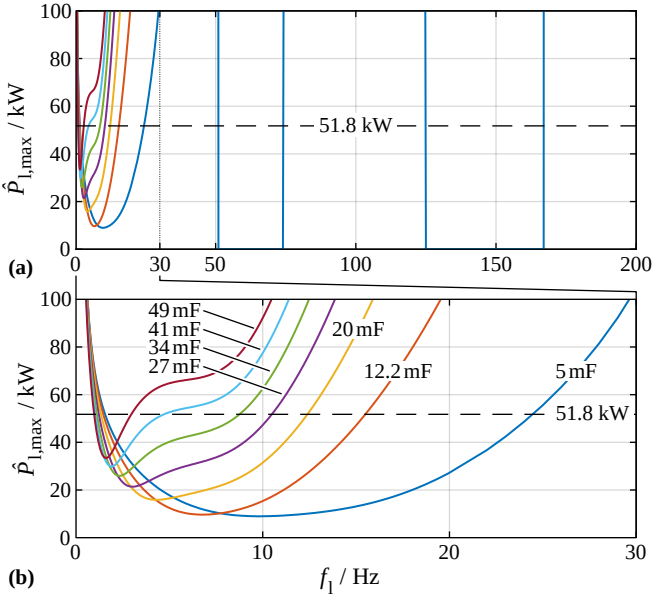


Fig. 2.11: (a) Maximum allowable output power over the entire load frequency range for different DC-link capacitances and a grid impedance of $\underline{Z}_g = 15\,\mathrm{m\Omega} + \mathrm{j}\,15\,\mathrm{m\Omega}$ (strong grid). For $C = 5\,\mathrm{mF}$ the harmonic current limitations cannot be fulfilled for $50\,\mathrm{Hz} \leq f_l \leq 75\,\mathrm{Hz}$ and $125\,\mathrm{Hz} \leq f_l \leq 167\,\mathrm{Hz}$. **(b)** Magnified view on $f_l \leq 30\,\mathrm{Hz}$. A minimum is found for $f_l \leq 10\,\mathrm{Hz}$, where the requirements for flicker set the most stringent limitations. According to these results, a capacitance of $C \geq 27\,\mathrm{mF}$ is needed to allow for operation with nominal power of $P_{nom} = 20\,\mathrm{kW}$ over the entire range of load frequency. Note that the considered IEC 61000 standard only applies to grid currents $\leq 75\,\mathrm{A}$, which corresponds to a maximum power level of 51.8 kW.

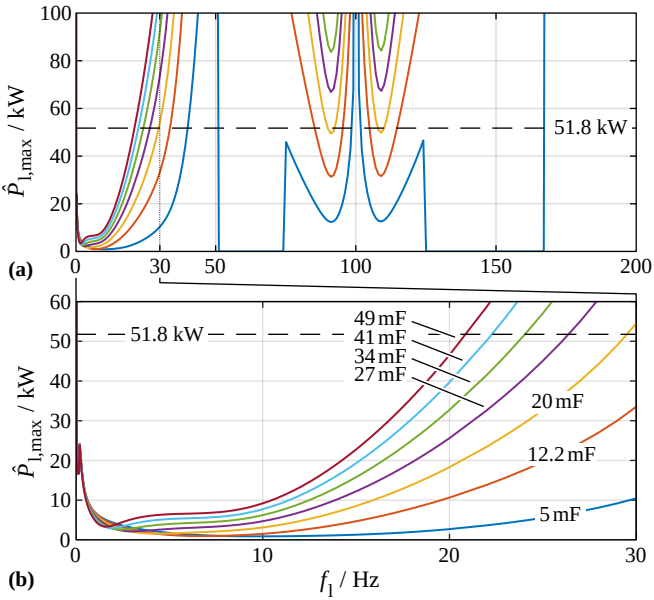


Fig. 2.12: (a) Maximum allowable output power over the entire load frequency range for different DC-link capacitances and a grid impedance of $\underline{Z}_g$ **= 150 mΩ + j 150 mΩ** (weak grid). For $C = 5\,\text{mF}$ the harmonic current limitations cannot be fulfilled for $50\,\text{Hz} \leq f_l \leq 75\,\text{Hz}$ and $125\,\text{Hz} \leq f_l \leq 167\,\text{Hz}$. **(b)** Magnified view on $f_l \leq 30\,\text{Hz}$. In comparison to **Fig. 2.11**, even with a high DC-link capacitance of 49 mF it is not possible to deliver output power levels exceeding 3.5 kW over the entire frequency range without violating the limits set for flicker.

for a strong grid and a weak grid, respectively, where

$$C \in \{5\,\mathrm{mF}, 12\,\mathrm{mF}, 20\,\mathrm{mF}, 27\,\mathrm{mF}, 34\,\mathrm{mF}, 41\,\mathrm{mF}, 49\,\mathrm{mF}\} \tag{2.21}$$

is selected for evaluation. The characteristics depicted in **Figs. 2.11** and **2.12** are mostly related to flicker limitations since IEC 61000-3-11 specifies relative limits for the harmonic current components, i.e., relative to the total RMS value of the phase current, cf. (2.9). For this reason, and because $P_0 = \hat{P}_1$ is considered, the relative distortion is found to be independent of $\hat{P}_1$ and, at a considered frequency, IEC 61000-3-11 is either fulfilled or cannot be fulfilled at all, which occurs for $C = 5\,\mathrm{mF}$ and $50\,\mathrm{Hz} < f_1 < 75\,\mathrm{Hz} \wedge 125\,\mathrm{Hz} < f_1 < 167\,\mathrm{Hz}$. Different to IEC 61000-3-11, the flicker standard IEC 61000-3-12 defines absolute values for the maximum allowable phase voltage distortions and the corresponding identified maximum allowable load power levels exhibit a minimum in the vicinity of 9 Hz for $C = 5\,\mathrm{mF}$ since the flicker standard sets the most stringent limitations, there. This minimum is shifted to lower frequencies with increasing DC-link capacitance, which can be observed in the magnified graphs presented in **Figs. 2.11b** and **2.12b**, because larger DC-link capacitances are capable of providing a larger amount of fluctuating energy for a defined capacitor voltage ripple. From **Fig. 2.11** it can be concluded that a capacitance of $C = 27\,\mathrm{mF}$ is sufficient for a strong grid. In case of a weak grid with $\underline{Z}_\mathrm{g} = 150\,\mathrm{m\Omega} + \mathrm{j}\,150\,\mathrm{m\Omega}$, the specified output power of 20 kW would require very high DC-link capacitances exceeding 50 mF. For this reason, a derating of the output power, according to the characteristics shown in **Fig. 2.12**, may be considered instead. Another solution could be the implementation of an active power pulsation buffer [190] in order to decrease the size of the DC-link capacitor, which, however, increases the complexity of the system.

2.1.5 Conclusion

This section develops a procedure to design the DC-link capacitor and the PI DC-link voltage controller for a converter system that utilizes a grid-connected three-phase PFC rectifier to provide LF pulsating power to a single-phase load inverter supplied from the DC-link, such that compliance with the relevant IEC 61000 grid standards is achieved. The requirements defined by IEC 61000-3-11 (harmonic current limitations) and IEC 61000-3-12 (flicker) are summarized, the computation of the emitted LF disturbances of the system is detailed, and the small-signal model that is required to identify design constraints for the voltage controller is discussed. The developed procedure is

explained using an example system with a rated power of 20 kW and a DC-link voltage of 700 V, where a DC-link capacitance of 27 mF is found to guarantee compliant full-power operation over the entire output frequency range in case of a strong grid (assumed grid impedance of 15 mΩ + j 15 mΩ). In case of weak grids, very high capacitances exceeding 50 mF may be required or the implementation of a derating according to the computed power limitation characteristic may be considered, instead. The results for the 20 kW converter system reveal that the requirement of a large DC-link capacitance is mainly related to flicker limitations that are most stringent at low frequencies. Thus, the result is subject to a physical constraint (high energy storage requirement) and only limited improvements are expected with extended concepts, e.g., nonlinear voltage control methods according to [191, 192], for controlling the DC-link voltage.

The presented analysis is applied in **Section 3.3.1** to dimension the DC-link capacitor of the 10 kW prototype CHB converter and to implement a power derating for certain operating frequencies in order to guarantee IEC 61000 compliance over the entire operating range.

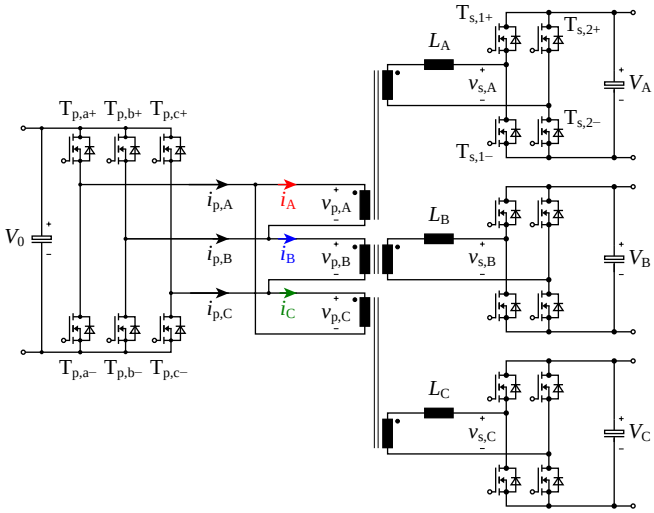


Fig. 2.13: Converter topology formed by Integration of Three (3) Dual Active Bridge (I3DAB) converter stages.

2.2 Optimized Modulation of a Multi-Port Dual-Active Bridge Converter

In case of the HF isolation approach being used for the power supply of the CHB converter it is possible to combine several of the isolated DC-DC converter stages into a multi-port converter by combining their primary bridges in order to reduce the number of components, thereby reducing the implementation effort. If DAB converters are employed as isolating DC-DC converters, this results in the structure depicted in **Fig. 2.13** referred to as Integration of Three Dual-Active Bridge converters (I3DAB). The resulting topology was already described in [172] for a CHB converter intended for power grid applications, where it was suggested that all three output ports (A to C) feed another cell of the same phase stack, thereby always resulting in the same power flow for all three ports. However, this limits the number of cells in a cell stack to multiples of three, which is an undesirable restriction for the general case of a CHB system.

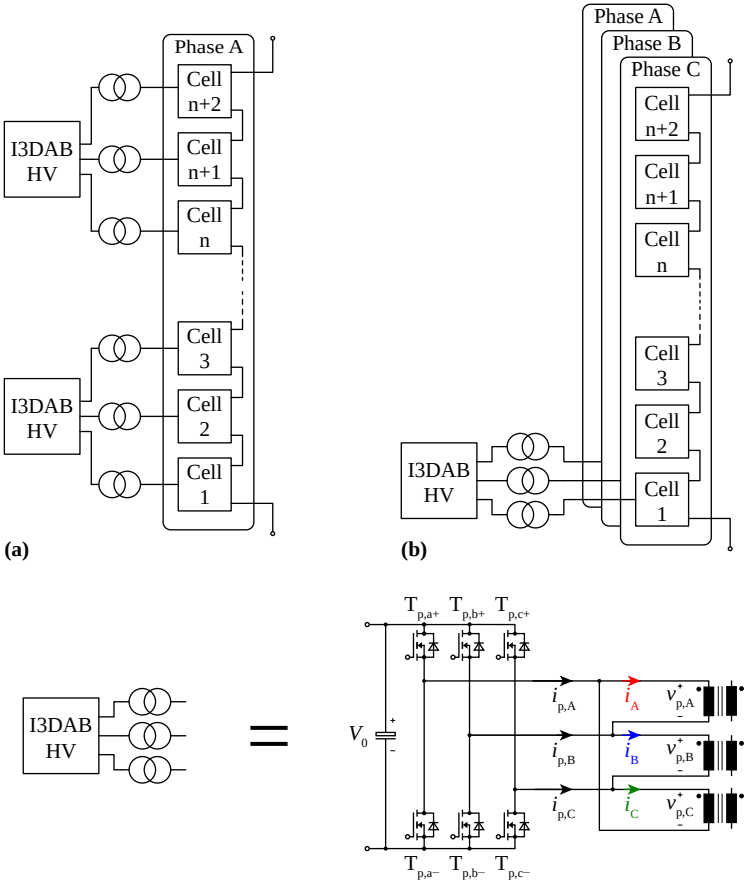


Fig. 2.14: Different arrangements of the I3DAB's secondary-side ports between the converter cells. **(a)** All three ports are connected to a single phase, requiring a multiple of three for the number of cells per phase stack. The output power of all converter ports is identical. **(b)** Each port of the I3DAB converter is connected to a cell in a different phase stack. For a three-phase system, an arbitrary number of cells can be used for each cell stack, however, the power flow of each of the I3DAB's output ports is not equal in this arrangement.

If the cell stack is part of a three-phase system as it is the case for the UH-PBW amplifier system investigated in this thesis, another arrangement could be chosen, where the output ports of each I3DAB converter are distributed between the three phase stacks of the three phases, as illustrated in **Fig. 2.14**. This allows for arbitrary numbers of converter cells per stack if three phase stacks for three phases are required, which is usually the case if the UH-PBW amplifier is employed as a power source in P-HIL applications. However, the (average) power flow through the three ports is typically not equal anymore in such a scenario since it depends on the individual loads of each CHB phase, which generally differ.

In the original modulation scheme described in [172] (referred to as "conventional modulation"), the I3DAB's three-phase bridge on the primary side is operated symmetrically with fixed duty cycles of all primary bridges and the power flow is controlled by the secondary-side duty cycles and phase shifts between primary and secondary side voltages. For this reason, although the originally suggested control scheme was intended for equal loads on all three converter ports, the converter could handle unequal loads as well since each of the ports is controlled individually. However, it is found that in case of unequal loading of the three converter ports, so far unused degrees of freedom in the modulation can be utilized to reduce the RMS currents in the converter compared to what would result from the conventional symmetrical modulation, resulting in a novel modulation scheme referred to as "optimized modulation".

In the following, the theoretical analysis of this novel modulation approach is presented in **Sections 2.2.1** to **2.2.3**, which describe the findings as published in [161]. The proposed optimized modulation scheme also resulted in a patent application [193]. Furthermore, in order to verify the theoretical considerations, an according experimental verification was conducted with a demonstrator system [194, 195], with the results presented in **Section 2.2.4**. Finally, the obtained results are summarized in a conclusion in **Section 2.2.5**.

2.2.1 System Description

The investigated I3DAB converter, depicted in **Fig. 2.13**, uses three High Frequency (HF) transformers, a three-phase two-level inverter on the primary side, and three full-bridges on the secondary side to power the isolated output ports of the three converter phases A, B, and C. The primary-side winding of each HF transformer is connected to the switching nodes of two adjacent phases of the three-phase inverter, which is illustrated in **Fig. 2.15**

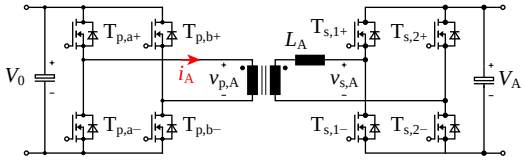


Fig. 2.15: Phase A of the I3DAB converter. This figure reveals the known topology of a conventional DAB converter.

for phase A, and, thus, the system of **Fig. 2.13** has strong similarities to the parallel connection of three DAB converters, since the transformers' stray inductances are utilized for power transfer. For this reason, the basic operating principles of the DAB and the I3DAB converters are the same: the primary-side and secondary-side power converters apply alternating voltage waveforms to the HF transformer and stray inductance of the corresponding phase, e.g., $v_{\mathrm{p,A}}(t)/n_{\mathrm{A}} - v_{\mathrm{s,A}}(t)$ to L_{A} in case of phase A, in order to generate the transformer currents and provide the required output power. **Fig. 2.16** depicts examples of these voltage and current waveforms and defines the three control variables that are available for phase A, i.e., the duty cycles of $v_{\mathrm{p,A}}$ and $v_{\mathrm{s,A}}$ and the phase shift between $v_{\mathrm{p,A}}$ and $v_{\mathrm{s,A}}$,

$$0 \leq D_{\mathrm{p,A}} \leq 1,\ 0 \leq D_{\mathrm{s,A}} \leq 1,\ \text{and}\ -\frac{\pi}{2} \leq \varphi_{\mathrm{A}} \leq \frac{\pi}{2}. \tag{2.22}$$

Corresponding definitions apply to the duty cycles and phase shifts of phases B and C, however, due to the integration of the three DAB converters' primary-side full-bridges into a single three-phase two-level inverter,

$$D_{\mathrm{p,A}} + D_{\mathrm{p,B}} + D_{\mathrm{p,C}} \leq 2 \tag{2.23}$$

applies. Detailed analysis reveals that the selection of $D_{\mathrm{p,A}} + D_{\mathrm{p,B}} + D_{\mathrm{p,C}} < 2$ is feasible and extends the parameter space for optimization, however, further improvements are only achievable for operation with low power levels at two or three output ports and at the cost of increased complexity due to additional boundary conditions. For these reason, the presented analysis is confined to

$$D_{\mathrm{p,A}} + D_{\mathrm{p,B}} + D_{\mathrm{p,C}} = 2. \tag{2.24}$$

Thus, compared to the operation of three parallel DAB converters, the total degrees of freedom for the control of the three output power levels reduces

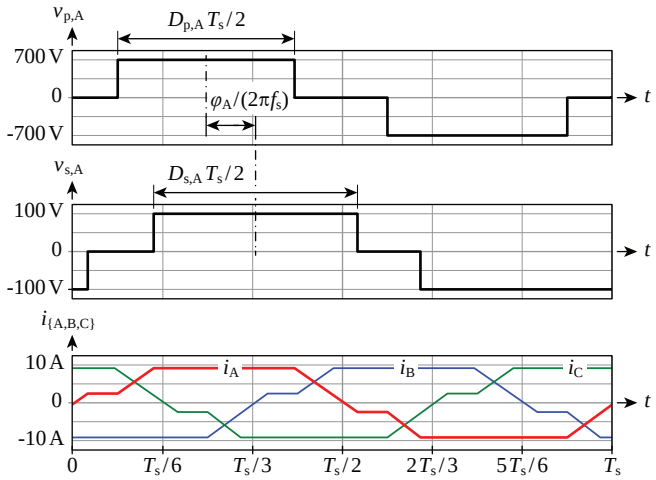


Fig. 2.16: Exemplary voltage and current waveforms for phase A of the I3DAB converter. Since the operating principles of both converter structures is the same, the depicted waveforms show large similarities to the voltages and currents occurring in a standard (single-port) DAB converter.

Tab. 2.2: Specifications of the investigated I3DAB converter.

Nominal DC voltage at input port V_0	700 V
Nominal DC voltages at all output ports, V_A, V_B, V_C	100 V
Rated power at all output ports, $P_{\mathrm{A},0}$, $P_{\mathrm{B},0}$, $P_{\mathrm{C},0}$	4 kW
Maximum short-time power, $P_{\mathrm{A,max}}$, $P_{\mathrm{B,max}}$, $P_{\mathrm{C,max}}$	6.7 kW
Switching frequency, f_s	50 kHz

from nine to eight (two primary-side duty cycles, three secondary-side duty cycles, and three phase shifts). Furthermore, it is not possible to simultaneously operate all phases with primary-side duty cycles greater than 2/3, because $D_{\mathrm{p,A}} > 2/3 \ \wedge D_{\mathrm{p,B}} > 2/3 \ \wedge D_{\mathrm{p,C}} > 2/3$ violates (2.24).

Fig. 2.16 presents the principal waveforms obtained with the conventional modulation strategy described in [196], which operates the primary-side inverter with constant duty cycles of $D_{\mathrm{p},\{\mathrm{A,B,C}\}} = 2/3$ and, thus, utilizes only six degrees of freedom, i.e., $D_{\mathrm{s},\{\mathrm{A,B,C}\}}$ and $\varphi_{\{\mathrm{A,B,C}\}}$. Consequently, a rectangular voltage as shown in **Fig. 2.16** with an active pulse duration of 2/3 of the switching period is applied to the primary side of each transformer. Based on the findings related to minimization of apparent power and subsequent simplifications, the conventional modulation strategy suggests the secondary-side full-bridges to be operated with duty cycles of

$$D_{\mathrm{s},\{\mathrm{A,B,C}\}} = \frac{2}{3} + (2-\sqrt{2})\left|\frac{\varphi_{\{\mathrm{A,B,C}\}}}{\pi}\right| \quad \forall \quad \left|\varphi_{\{\mathrm{A,B,C}\}}\right| \leq \frac{\pi}{2}. \tag{2.25}$$

The respective phase shifts, $\varphi_{\{\mathrm{A,B,C}\}}$, are selected in order to provide the required output power levels. Based on these considerations and the specifications listed in **Tab. 2.2**, the transformers' turns ratios, $n_{\{\mathrm{A,B,C}\}}$, and stray inductances, $L_{\{\mathrm{A,B,C}\}}$, can be determined. The DAB converter achieves most efficient operation if the turns ratio is equal to the ratio of input to output DC voltages [197] and, thus,

$$n_\mathrm{A} = n_\mathrm{B} = n_\mathrm{C} = \frac{700\,\mathrm{V}}{100\,\mathrm{V}} = 7 \tag{2.26}$$

results. According to **Tab. 2.2**, the system provides a maximum power of 6.7 kW at all three output ports and, for this reason, all three stray inductances must not exceed

$$L_{\{\mathrm{A,B,C}\},\mathrm{max}} = \frac{V_0 V_{\{\mathrm{A,B,C}\}}}{9 f_\mathrm{s}\, n_{\{\mathrm{A,B,C}\}}\, P_{\{\mathrm{A,B,C}\},\mathrm{max}}} = 3.3\,\mu\mathrm{H}. \tag{2.27}$$

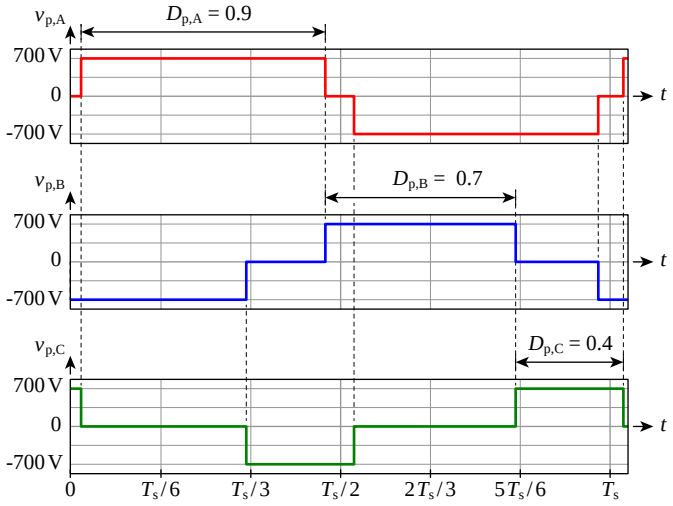


Fig. 2.17: General voltage waveforms on the primary side for $D_{p,A} = 0.9$, $D_{p,B} = 0.7$, and $D_{p,C} = 0.4$. The dashed lines illustrate the switching instants of the primary-side half-bridges.

Based on this result and the considerations of an acceptable increase of the reactive power in the HF converter parts at nominal power (4 kW) and practicable sensitivities of the converter's output DC voltages with respect to changing control parameters at low power,

$$L_{\{A,B,C\}} = 80\,\% L_{\{A,B,C\},max} = 2.7\,\mu H \tag{2.28}$$

has been selected. Margins of 20 % with respect to L_{max} cover eventually arising additional needs due to losses and short-time transient output currents.

2.2.2 Optimization for Minimum Conduction Losses

This section describes an optimized modulation strategy, which does not confine $D_{p,\{A,B,C\}}$ to 2/3, as shown in **Fig. 2.17**, and, in addition, uses optimized values for $D_{s,\{A,B,C\}}$. The proposed modulation strategy facilitates considerable loss reductions in case of substantially different power levels at the output ports.

The presented derivations are based on the Fundamental Frequency Analysis (FFA), to achieve simplified expressions for the output power levels,

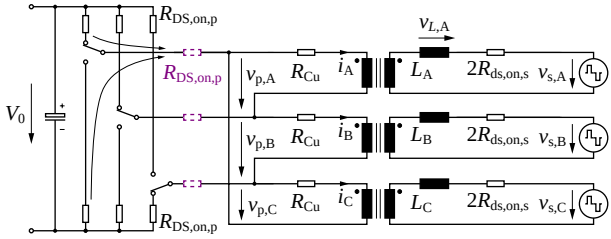


Fig. 2.18: Considered loss resistances required to model the conduction losses. For each half-bridge, either the low-side or high-side switch is conducting, resulting in an equivalent resistance in series to the bridge output that equals the respective MOSFET on-state resistance. For the secondary-side bridges this results in an equivalent resistance of $2R_{\mathrm{ds,on,s}}$ since each full-bridge incorporates two half-bridges.

$P_{\{\mathrm{A,B,C}\}}$, and the RMS values of the primary-side referred transformer currents, $I_{\{\mathrm{A,B,C}\}}$, and still maintain reasonable accuracies [198]. By way of example,

$$I_{\mathrm{A(1)}} = \frac{\sqrt{V_{\mathrm{p,A(1)}}^2 + n_{\mathrm{A}}^2 V_{\mathrm{s,A(1)}}^2 - 2V_{\mathrm{p,A(1)}} n_{\mathrm{A}} V_{\mathrm{s,A(1)}} \cos(\varphi_{\mathrm{A}})}}{2\pi f_{\mathrm{s}} n_{\mathrm{A}}^2 L_{\mathrm{A}}}, \tag{2.29}$$

$$P_{\mathrm{A(1)}} = \frac{V_{\mathrm{p,A(1)}} V_{\mathrm{s,A(1)}} \sin(\varphi_{\mathrm{A}})}{2\pi f_{\mathrm{s}} n_{\mathrm{A}} L_{\mathrm{A}}}, \tag{2.30}$$

$$V_{\mathrm{p,A(1)}} = V_0 \frac{2\sqrt{2}}{\pi} \sin\left(\frac{\pi}{2} D_{\mathrm{p,A}}\right) \quad \forall\, D_{\mathrm{p,A}} \in [0,1], \text{ and} \tag{2.31}$$

$$V_{\mathrm{s,A(1)}} = V_{\mathrm{A}} \frac{2\sqrt{2}}{\pi} \sin\left(\frac{\pi}{2} D_{\mathrm{s,A}}\right) \quad \forall\, D_{\mathrm{s,A}} \in [0,1] \tag{2.32}$$

are obtained for phase A, for the fundamental frequency components of $i_{\mathrm{A}}(t)$, the power P_{A}, $v_{\mathrm{p,A}}(t)$, and $v_{\mathrm{s,A}}(t)$, cf. **Fig. 2.13**, and similar expressions result for phases B and C; the index (1) denotes the fundamental frequency component, $I_{\mathrm{A(1)}}$, $V_{\mathrm{p,A(1)}}$, and $V_{\mathrm{s,A(1)}}$ are RMS values.

From the transformer RMS currents $I_{\{\mathrm{A,B,C}\}(1)}$ the conduction losses are calculated, with the according circuit arrangement of the involved loss resistances depicted in **Fig. 2.18**. The conduction losses are composed from the on-state resistances of the primary and secondary-side MOSFETs, $R_{\mathrm{ds,on,p}}$ and $R_{\mathrm{ds,on,s}}$, and the winding resistances of the transformers, R_{Cu}, where six

identical MOSFETs for the primary-side three-phase two-level inverter and identical transformers and secondary-side MOSFETs for each secondary-side full-bridge are assumed, resulting in identical resistance values for all three ports. This allows to express the conduction losses P_c by

$$\begin{aligned} P_\mathrm{c} =& R_\mathrm{s}\left(I_{\mathrm{A(1)}}^2 + I_{\mathrm{B(1)}}^2 + I_{\mathrm{C(1)}}^2\right) + \\ & 2R_{\mathrm{ds,on,p}}\left(I_{\mathrm{A(1)}}^2 + I_{\mathrm{B(1)}}^2 + I_{\mathrm{C(1)}}^2\right) - \\ & 2R_{\mathrm{ds,on,p}}\left(I_{\mathrm{A(1)}}I_{\mathrm{B(1)}}\cos\left(\Delta\varphi_{\mathrm{AB}}\right) + I_{\mathrm{B(1)}}I_{\mathrm{C(1)}}\cos\left(\Delta\varphi_{\mathrm{BC}}\right) + I_{\mathrm{C(1)}}I_{\mathrm{A(1)}}\cos\left(\Delta\varphi_{\mathrm{CA}}\right)\right). \end{aligned} \tag{2.33}$$

In the above expression, $\Delta\varphi_{ij} = \varphi_i - \varphi_j$, $i, j = \{\mathrm{A}, \mathrm{B}, \mathrm{C}\}$ refers to the fundamental frequency phase displacement of the transformer currents i_i and i_j and

$$R_\mathrm{s} = R_\mathrm{Cu} + 2n^2\, R_{\mathrm{ds,on,s}} \tag{2.34}$$

denotes the sum of the primary-referred on-state resistance of the secondary-side full-bridges and the winding resistance of the transformer.

For the optimization procedure described in the following, it is assumed that the conduction losses are dominated by the summed resistances of the transformer windings and the secondary-side MOSFET on-state resistances[3], R_s. Consequently, this allows to approximate the conduction losses in (2.33) by neglecting the on-state resistance of the primary-side MOSFETs, resulting in

$$P_\mathrm{c} = R_\mathrm{s}\left(I_{\mathrm{A(1)}}^2 + I_{\mathrm{B(1)}}^2 + I_{\mathrm{C(1)}}^2\right). \tag{2.35}$$

The introduced approximation significantly simplifies the optimization procedure since the trigonometric cross-coupling terms between the currents are eliminated, thereby allowing an independent optimization of the secondary-side duty cycles that enables the two-step optimization procedure presented below. Since according to (2.35), minimizing the conduction losses corresponds to a minimization of the squared sum of the RMS currents, the above equation allows to omit the loss resistance R_s, resulting in the cost function

$$f_\mathrm{cost} = I_{\mathrm{A(1)}}^2 + I_{\mathrm{B(1)}}^2 + I_{\mathrm{C(1)}}^2, \tag{2.36}$$

that represents the basis for the derivation of a modulation strategy that minimizes the conduction losses and enables the calculation of optimal duty cycles, $D_{\mathrm{p},\{\mathrm{A,B,C}\},\mathrm{opt}}$ and $D_{\mathrm{s},\{\mathrm{A,B,C}\},\mathrm{opt}}$.

[3] E.g. for the hardware prototype presented in **Section 2.2.4** , R_Cu and $R_{\mathrm{ds,on,s}}$ account for 95 % of the total resistance.

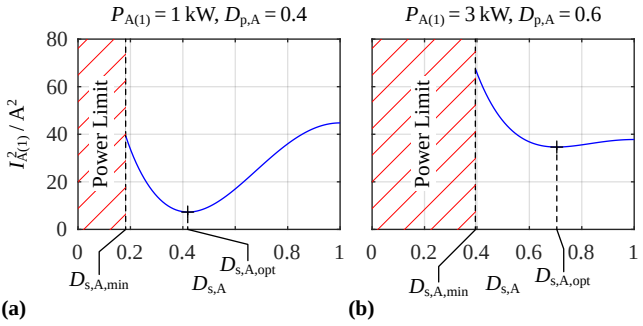


Fig. 2.19: Squares of the RMS values of the primary-side transformer current of phase A for input and output port DC voltages according to **Tab. 2.2**, $n_A = 7$, $L_A = 2.7\,\mu\mathrm{H}$, varying values of $D_{s,A}$, and different power levels and primary-side duty cycles: **(a)** $P_{A(1)} = 1\,\mathrm{kW}$, $D_{p,A} = 0.4$, and **(b)** $P_{A(1)} = 3\,\mathrm{kW}$, $D_{p,A} = 0.6$. The required output power cannot be provided for $D_{s,A} < D_{s,A,min}$. Minima in $I^2_{A(1)}$ result for: **(a)** $D_{s,A} = 0.42$ and **(b)** $D_{s,A} = 0.71$.

In a first step, the secondary-side duty cycles are optimized, since the secondary-side full-bridges can be operated independently of each other. In this regard, **Fig. 2.19** illustrates the characteristic of $I^2_{A(1)}$ against $D_{s,A}$ for $0 < D_{s,A} \leq 1$ for two different primary-side duty cycles and power levels, i.e, $P_{A(1)} = 1\,\mathrm{kW}$, $D_{p,A} = 0.4$ in **Fig. 2.19a** and $P_{A(1)} = 3\,\mathrm{kW}$, $D_{p,A} = 0.6$ in **Fig. 2.19b**. With respect to the depicted minima of $I^2_{A(1)}$, **Figs. 2.19a** and **2.19b** reveal optimal duty cycles of $D_{s,A,opt} = 0.42$ and $D_{s,A,opt} = 0.71$, respectively. The corresponding calculation, thus, needs to evaluate

$$\frac{\mathrm{d}I^2_{k(1)}}{\mathrm{d}D_{s,k}} = 0, \qquad k \in \{A, B, C\}, \tag{2.37}$$

which yields

$$\sin\left(\frac{\pi}{2} D_{s,k,opt}\right) = \frac{\sqrt{16V_0^4 \sin^4\left(\frac{\pi}{2} D_{p,k}\right) + \pi^6 f_s^2 n_k^4 L_k^2 P^2_{k(1)}}}{4V_0 n_k V_k \sin\left(\frac{\pi}{2} D_{p,k}\right)}. \tag{2.38}$$

The calculation of optimal primary-side duty cycles involves all converter phases, due to the couplings of the primary-side duty cycles according to (2.24).

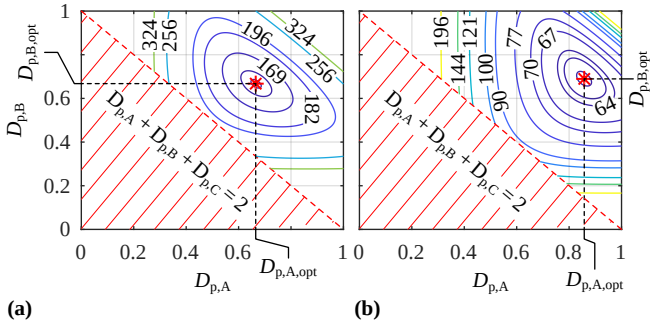


Fig. 2.20: Results determined for f_{cost}, cf. (2.36), for input and output voltages according to **Tab. 2.2**, $n_{\{\text{A,B,C}\}} = 7$, $L_{\{\text{A,B,C}\}} = 2.7\,\mu\text{H}$, different primary-side duty cycles, $D_{\text{p,A}}$ and $D_{\text{p,B}}$ ($D_{\text{p,C}} = 2 - D_{\text{p,A}} - D_{\text{p,B}}$), optimal duty cycle values for the secondary-side full-bridges, and different output power levels: **(a)** $P_{\text{A(1)}} = P_{\text{B(1)}} = P_{\text{C(1)}} = 4\,\text{kW}$, **(b)** $P_{\text{A(1)}} = 4\,\text{kW}$, $P_{\text{B(1)}} = 2\,\text{kW}$, $P_{\text{C(1)}} = 1\,\text{kW}$. Optimal primary-side duty cycles of $D_{\text{p,A}} = D_{\text{p,B}} = D_{\text{p,C}} = 0.67$ and $D_{\text{p,A}} = 0.86$, $D_{\text{p,B}} = 0.69$, $D_{\text{p,C}} = 0.45$ result for the two load scenarios, respectively. Operation in the hatched region is not possible because this would imply $D_{\text{p,C}} > 1$ according to (2.24).

For this reason, the complete expression (2.36) needs to be taken into account. **Fig. 2.20** illustrates the results computed for f_{cost} for $0 \leq D_{\text{p,A}} \leq 1$, $0 \leq D_{\text{p,B}} \leq 1$, optimized secondary-side duty cycles (see above), and for two different load scenarios: a symmetrical load case with $P_{\text{A(1)}} = P_{\text{B(1)}} = P_{\text{C(1)}} = 4\,\text{kW}$ in **Fig. 2.20a** and an asymmetrical load scenario in **Fig. 2.20b** with $P_{\text{A(1)}} = 4\,\text{kW}$, $P_{\text{B(1)}} = 2\,\text{kW}$, $P_{\text{C(1)}} = 1\,\text{kW}$. The hatched area in **Fig. 2.20** denotes combinations of unallowed values for $D_{\text{p,A}}$ and $D_{\text{p,B}}$, which would violate (2.24). Due to the operation with different power levels at the output ports, the optimal primary-side duty cycles that minimize the cost function in **Fig. 2.20b** are $D_{\text{p,A,opt}} = 0.86$, $D_{\text{p,B,opt}} = 0.69$ and $D_{\text{p,C,opt}} = 0.45$, i.e., different from 2/3, whereas optimal operation in the symmetrical case is achieved for $D_{\text{p,A,opt}} = D_{\text{p,B,opt}} = D_{\text{p,C,opt}} = 2/3$. The mathematical description of the optimization illustrated in **Fig. 2.20** is

$$\frac{\mathrm{d}f_{\text{cost}}}{\mathrm{d}D_{\text{p,A}}} = 0 \wedge \frac{\mathrm{d}f_{\text{cost}}}{\mathrm{d}D_{\text{p,B}}} = 0. \tag{2.39}$$

However, no closed-form analytical solution has been found for (2.39). Hence, a numerical solver is used to determine the optimal duty cycle values. With known duty cycles and output power levels, the corresponding phase shifts,

$\varphi_{\{A,B,C\},opt}$, are determined according to (2.30), which, for phase k, $k \in \{A, B, C\}$, is

$$\varphi_{k,opt} = \arcsin\left[\frac{\pi^3 f_s\, n_k L_k\, P_{k(1)}}{4V_0 V_k\, \sin\left(\frac{\pi}{2} D_{p,k,opt}\right)\, \sin\left(\frac{\pi}{2} D_{s,k,opt}\right)}\right]. \tag{2.40}$$

Discussion and ZVS

This section evaluates the optimized modulation strategy for the I3DAB converter specified and designed in **Section 2.2.1** for 24 characteristic operating points that result from the combinations of the selected output power levels listed below:

$$\begin{aligned} P_{A(1)} &= 4.0\,\mathrm{kW}, \\ P_{B(1)} &= [\,0.0,\, 2.0,\, 4.0\,] \times 1\,\mathrm{kW}, \\ P_{C(1)} &= [\,0.0,\, 0.1,\, 0.25,\, 0.5,\, 1.0,\, 2.0,\, 3.0,\, 4.0\,] \times 1\,\mathrm{kW}. \end{aligned} \tag{2.41}$$

To begin with, **Fig. 2.21** depicts the control variables, $D_{p,\{A,B,C\}}$, $D_{s,\{A,B,C\}}$, and $\varphi_{\{A,B,C\}}$, for the conventional modulation strategy presented in [172], which uses $D_{p,\{A,B,C\}} = 2/3$ for all operating points and confines the ranges for $D_{s,\{A,B,C\}}$ to values between 2/3 and 1, according to (2.25). With $D_{p,\{A,B,C\}} = 2/3$, the conventional modulation strategy facilitates decoupled control of output power and port voltage of each phase, however, excludes a great range of potential options for improved converter operation. **Fig. 2.22** presents the control variables determined with the developed optimized modulation strategy and reveals the expected change of the primary-side duty cycles for changing output power levels. The major findings drawn from **Fig. 2.22** are summarized below:

- An increase of the output power of a certain converter phase leads to an increase of the corresponding primary-side duty cycle, e.g., $D_{p,C}$ for increasing $P_{C(1)}$ in **Fig. 2.22**, and, due to (2.24), a decrease of one or both of the remaining primary-side duty cycles.
- The primary-side duty cycles are distributed according to the corresponding power levels, i.e., the largest primary-side duty cycle results for the converter phase with the highest output power and the smallest duty cycle for the phase with the lowest output power.
- In comparison to the conventional modulation strategy, the linear relationship between $D_{s,\{A,B,C\}}$ and $\varphi_{s,\{A,B,C\}}$ does not apply anymore and the full range of $0 \leq D_{s,\{A,B,C\}} \leq 1$ is utilized.

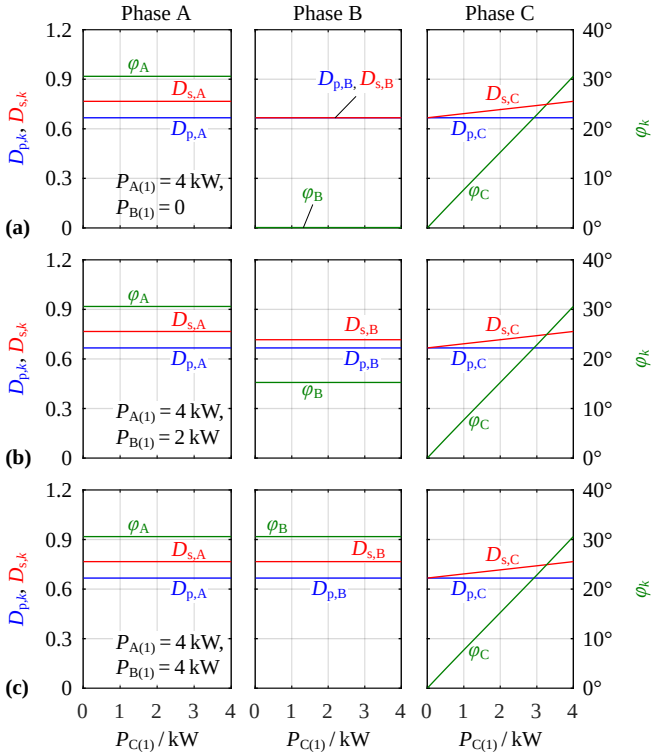


Fig. 2.21: Control parameters calculated with the conventional modulation scheme proposed in [172] for $P_{A(1)} = 4\,kW$, $0 < P_{C(1)} < 4\,kW$, and different power levels at the output port of phase B: **(a)** $P_{B(1)} = 0$, **(b)** $P_{B(1)} = 2\,kW$, **(c)** $P_{B(1)} = 4\,kW$. All primary-side duty cycles are fixed to $D_{p,\{A,B,C\}} = 2/3$. The values of $D_{s,\{A,B,C\}}$ and $\varphi_{\{A,B,C\}}$ are determined by the according power flow, where a linear relationship between $D_{s,\{A,B,C\}}$ and $\varphi_{\{A,B,C\}}$ according to (2.25) is considered.

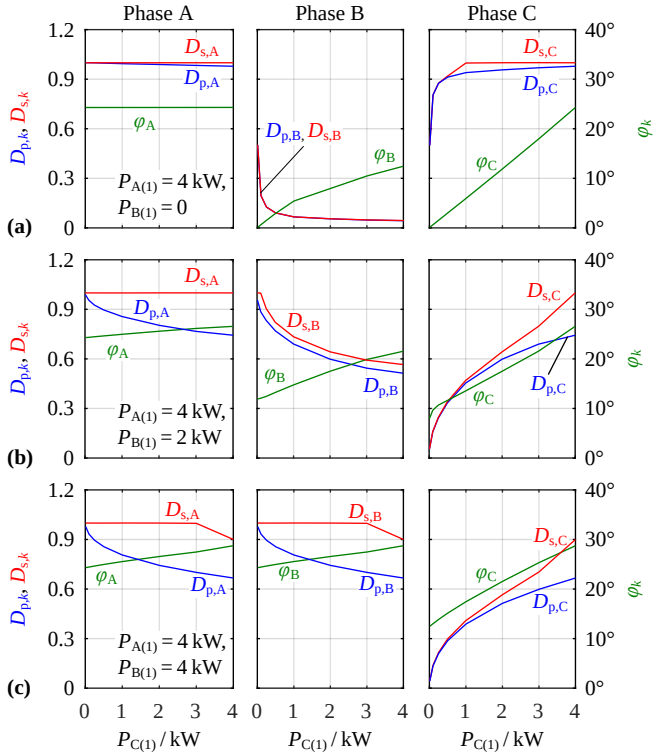


Fig. 2.22: Control parameters for minimum total RMS transformer current (proposed optimized modulation), $P_{A(1)} = 4\,\mathrm{kW}$, $0 < P_{C(1)} < 4\,\mathrm{kW}$, and different power levels at the output port of phase B: **(a)** $P_{B(1)} = 0$, **(b)** $P_{B(1)} = 2\,\mathrm{kW}$, **(c)** $P_{B(1)} = 4\,\mathrm{kW}$. The primary-side duty cycles are distributed according to the corresponding power levels where increasing power levels correspond to increasing duty cycles of the according phase.

The optimized modulation strategy achieves a reduction of the value of the cost function by up to 23 %, which is detailed in the course of the verification presented in **Section 2.2.3**. However, both the conventional and the optimized modulation strategy are found to lose ZVS at the primary side for operating points with substantially different power levels of the three converter ports, e.g., one half-bridge of the three-phase inverter loses ZVS for $P_{\mathrm{A}(1)} = 3\,\mathrm{kW}$, $P_{\mathrm{B}(1)} = 3\,\mathrm{kW}$, and $P_{\mathrm{C}(1)} = 1\,\mathrm{kW}$. Reduced magnetizing inductances of the HF transformers can be utilized to gain ZVS again and the value of the required magnetizing inductance is used as a Figure of Merit for evaluating the modulation strategies with regard to their suitabilities for operation with ZVS, i.e., a larger allowable magnetizing inductance denotes a modulation strategy that is more suitable with respect to ZVS. The calculation of maximum allowable magnetizing inductances for 512 different operating points, created from all combinations of $P_{\{\mathrm{A,B,C}\}(1)} = [\,0.0,\ 0.1,\ 0.25,\ 0.5,\ 1.0,\ 2.0,\ 3.0,\ 4.0\,] \times 1\,\mathrm{kW}$, returns maximum magnetizing inductances of

$$\begin{aligned} L_{\mathrm{mag,conv}} &< 1.47\,\mathrm{mH}\ \text{and} \\ L_{\mathrm{mag,opt}} &< 4.59\,\mathrm{mH} \end{aligned} \tag{2.42}$$

for the three HF transformers and the conventional and optimized modulation strategies, respectively.[4] According to this result, the optimized modulation strategy is far more robust with respect to ZVS operation than the conventional modulation. On a final note, it is worth to mention that both investigated modulation strategies feature complete four-port operation, i.e., bidirectional operation of the three converter phases and converter operation with different output port voltages, which is only limited by the maximum output power levels, the requirement of positive port voltages, and the additional limitations imposed by the converter hardware (e.g., thermal limitations).

2.2.3 Verification by Circuit Simulations

The results obtained from the optimization described in **Section 2.2.2** are verified by means of numerical circuit simulation. For this purpose, two characteristic load scenarios with different output power levels are chosen:

- Scenario I: $P_{\mathrm{A}(1)} = 4\,\mathrm{kW}$, $P_{\mathrm{B}(1)} = P_{\mathrm{C}(1)} = 0$;

[4] $L_{\mathrm{mag,conv}}$ and $L_{\mathrm{mag,opt}}$ are determined based on the assumption that zero instantaneous current enables ZVS. However, a practical implementation of ZVS requires increased magnetizing currents at the switching instants. Thus, the magnetizing inductances need to be reduced, accordingly.

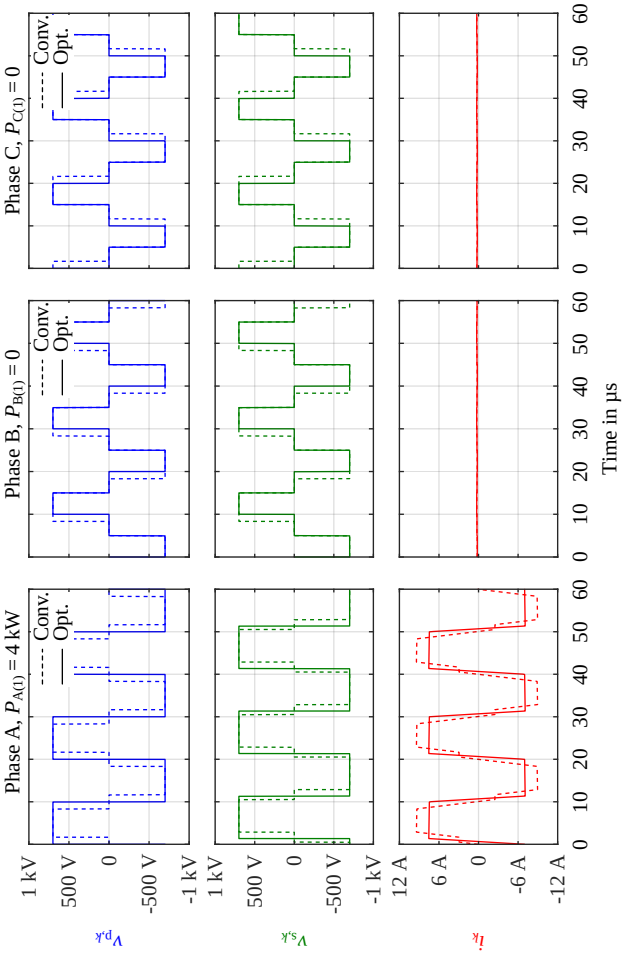


Fig. 2.23: Simulated voltage and current waveforms for $P_{A(1)} = 4\,\text{kW}$, $P_{B(1)} = 0$, and $P_{C(1)} = 0$. Only one port (phase A) delivers output power, therefore, the according primary-side duty cycle is set to the maximum value in order to minimize the RMS current. Due to additional harmonic components which are neglected in the FFA, higher output powers than expected result, leading to total output power levels of $P_A = 4.4\,\text{kW}$ and $P_B = P_C = 0$. The values of the cost function, cf. (2.36), are $56\,\text{A}^2$ and $40\,\text{A}^2$ for conventional and optimized modulation strategies, respectively.

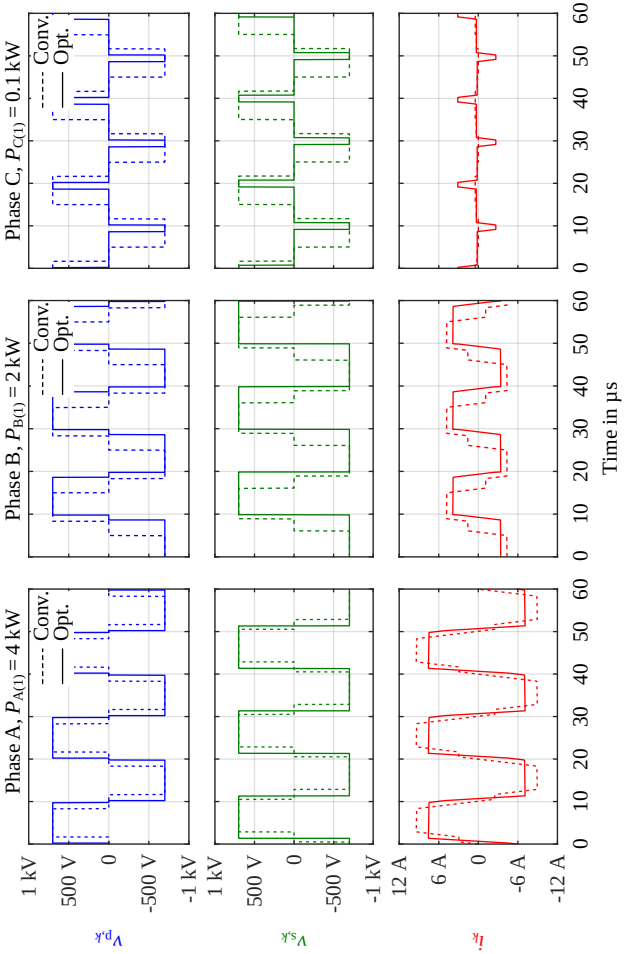


Fig. 2.24: Simulated voltage and current waveforms for $P_{A(1)} = 4\,kW$, $P_{B(1)} = 2\,kW$ and $P_{C(1)} = 0.1\,kW$. Due to additional harmonic components, increased output power levels of $P_A = 4.4\,kW$, $P_B = 2.2\,kW$, and $P_C = 0.3\,kW$ result. Similar to the results of **Fig. 2.23**, increased primary-side duty cycles are used for the phases that are subject to high loads (phases B and C). The values of the cost function, cf. (2.36), are 70 A^2 and 49 A^2 for conventional and optimized modulation strategies, respectively.

- Scenario II: $P_{A(1)} = 4\,\mathrm{kW}$, $P_{B(1)} = 2\,\mathrm{kW}$, $P_{C(1)} = 0.1\,\mathrm{kW}$.

Fig. 2.23 and **Fig. 2.24** depict the simulated waveforms corresponding to the two load scenarios, respectively, and for conventional and optimized modulation strategies. Comparing the primary-side voltage waveforms for both modulation strategies it is clearly visible that for the optimized modulation strategy the active duty cycles applied to the primary sides of the transformers deviate between the phases. In the first load scenario, depicted in **Fig. 2.23**, the primary-side duty cycle of the only port delivering output power (phase A) is set to the maximum value of 1. Due to the larger voltage time area applied to the transformer, the corresponding phase current amplitude can be reduced when compared to the conventional modulation. By reason of (2.24), the remaining phases are operated with a primary-side duty cycle of $D_{p,B} = D_{p,C} = 0.5$. Power flow for all phases is controlled via their corresponding secondary-side duty cycles and the phase shifts between primary and secondary sides, which are chosen according to (2.38) and (2.40). In the second load scenario, depicted in **Fig. 2.24**, the RMS currents of phases A and B are reduced by maximizing the primary-side duty cycles of the corresponding phase voltages, which is similar to the results obtained for scenario I, cf. **Fig. 2.23**. As a consequence, this leads to a reduction of $D_{p,C}$, resulting in a small active on-time of phase C as the according output power approaches zero. The optimized primary-side duty cycles, thus, allow for low losses in phase C and, at the same time, feature $D_{p,A} \approx 1$ and $D_{p,B} \approx 1$, which enables a reduction of the RMS currents in the remaining phases. The optimized modulation strategy reduces the values of the cost function, f_{cost}, defined with (2.36), from 56 A^2 and 70 A^2 to 40 A^2 and 49 A^2 for load scenarios I and II, respectively.

Fig. 2.25 presents the values of f_{cost} for both modulation strategies and for the 24 operating points defined with (2.41), cf. **Section 2.2.2**. The value of f_{cost} is proportional to the total conduction losses of the converter system and is, thus, a suitable measure for comparison. From the presented graphs it becomes evident that calculated and simulated values of fundamental frequency components exactly match. Compared to the conventional modulation scheme, the optimized modulation strategy achieves reductions of the total conduction losses of up to 23 % (e.g., at $P_{A(1)} = 4\,\mathrm{kW}$, $P_{B(1)} = 4\,\mathrm{kW}$, and $P_{C(1)} = 0$). As expected, the optimized control of the primary-side voltages is especially favorable for cases where large deviations between the three output power levels occur. The results of **Fig. 2.25**, however, only take the fundamental frequency components into consideration and neglect higher order harmonics in the waveforms. The additional contributions of higher

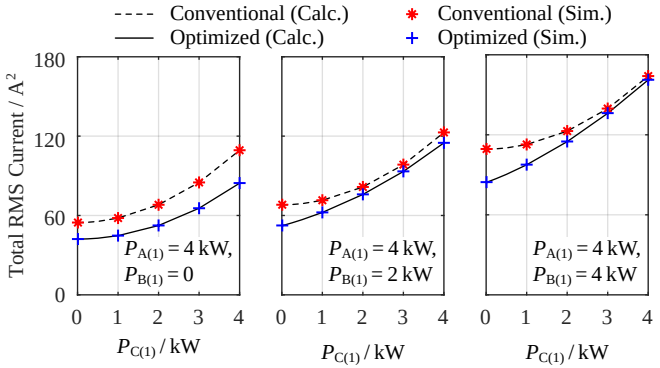


Fig. 2.25: Comparison of the calculated and simulated RMS transformer currents for both modulation strategies. Only the fundamental frequency components of current and power are considered. The simulated results precisely match the calculated values obtained from the optimization. Based on these results, reductions of the conduction losses by up to 23 % are estimated (e.g., at $P_{A(1)} = 4\,\text{kW}$, $P_{B(1)} = 4\,\text{kW}$, and $P_{C(1)} = 0$).

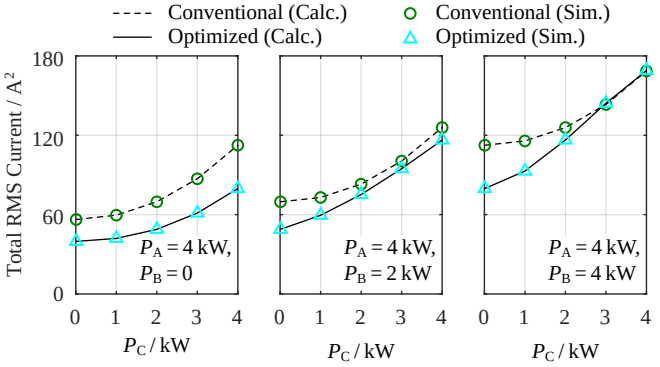


Fig. 2.26: Simulation results for the conventional and the optimized modulation scheme with all spectral components being taken into account. The simulation results prove that the predicted reduction in conduction losses is still achieved when higher order harmonic components are considered, thereby justifying the presented FFA-based optimization. The optimized modulation strategy reduces conduction losses by up to 30 % (e.g., at $P_A = 4\,\text{kW}$, $P_B = 4\,\text{kW}$, and $P_C = 0$).

Tab. 2.3: I3DAB prototype measurement conditions. Dashed identifiers refer to quantities that have been transformed to the high-voltage (HV) side of the transformers.

Input voltage (HV)	V_0	700 V
Output voltage (LV)	$V_{\mathrm{A,B,C}}$	95 V
Nominal load current (per LV port)	I_{nom}	25 A
Rated power (per LV port)	P_{nom}	2.4 kW
Switching frequency	f_{s}	50 kHz
Total DAB inductance (transformer leakage + L_{ext}, referred to LV side)	$L_{\mathrm{A,B,C}}$	3.3 µH
Total DAB inductance (transformer leakage + L_{ext}, referred to HV side)	$L'_{\mathrm{A,B,C}}$	180 µH
Transformer leakage inductance (referred to HV side)	L_{σ}	30 µH
Transformer magnetizing inductance (referred to HV side)	L_{mag}	1.1 mH
External series inductance (referred to HV side)	L'_{ext}	150 µH
Transformer turns ratio	$n_{\mathrm{A,B,C}}$	37 : 5

order harmonics increase the power levels and the RMS currents in all converter components. In order to compensate the deviations and precisely meet the desired output power levels, the values of $P_{\mathrm{A(1)}}$, $P_{\mathrm{B(1)}}$, and $P_{\mathrm{C(1)}}$, which denote the input parameters for the computation of duty cycles and phase angles, are slightly reduced. **Fig. 2.26** presents the corresponding results, which include all frequency components in RMS currents and power levels. The obtained results confirm the effectiveness of the optimized modulation scheme also when taking higher order harmonic components into account, with the conduction losses being reduced by up to 30 % (e.g., at $P_{\mathrm{A}} = 4\,\mathrm{kW}$, $P_{\mathrm{B}} = 4\,\mathrm{kW}$, and $P_{\mathrm{C}} = 0$). A direct comparison of **Figs. 2.25** and **2.26** reveals only minor differences between the results obtained with FFA and the detailed results that include all harmonic components, which justifies the presented optimization procedure.

2.2.4 Experimental Verification

In order to verify the theoretical considerations stated before, a scaled demonstrator system was constructed and experimentally tested. The according specifications for the prototype system were slightly adapted and are summarized in **Tab. 2.3**, where a reduced nominal power of 2.4 kW was used to meet the current measuring range of the available *Yokogawa WT3000* power

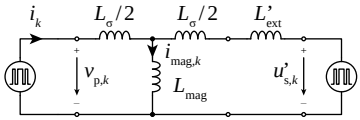


Fig. 2.27: Inductive network between primary and secondary converter bridge for each port, referred to the HV side of the transformer. The network consists of the equivalent circuit of the transformer and an external inductance L_{ext} which is physically located on the secondary side. Dashed identifiers refer to quantities that have been transformed to the HV side of the transformer.

analyzer. Since the required series inductance could not be entirely integrated into the leakage inductance of the transformer, an additional external inductor was used on each of the LV sides, resulting in a total series inductance of $L_{\text{A,B,C}} = 3.3\,\mu\text{H}$. The according equivalent circuit of the resulting inductive network is illustrated in **Fig. 2.27**, where it has to be mentioned that due to the asymmetric series inductances on the primary- and secondary- side of the transformer (i.e., left and right of the magnetizing inductance L_{mag}), almost the entire magnetizing current is flowing via the HV side bridge as long as the voltage ratio between both bridges corresponds to the transformer's turns ratio.

Measurements of the waveforms of each of the transformer's primary voltages $v_{\text{p},k}$, secondary voltages $v_{\text{s},k}$ and primary currents i_k for conventional as well as optimized modulation are presented in **Fig. 2.28** and **Fig. 2.29** for two exemplary operating points with $P_{\text{A}} = 2.4\,\text{kW}$, $P_{\text{B}} = 2.4\,\text{kW}$, $P_{\text{C}} = 2.4\,\text{kW}$ and $P_{\text{A}} = 2.4\,\text{kW}$, $P_{\text{B}} = 2.4\,\text{kW}$, $P_{\text{C}} = 200\,\text{W}$, respectively. In case of symmetrical loading of the three converter ports, illustrated in **Fig. 2.28**, no visible difference between the two modulation strategies can be recognized since almost the same modulation parameters result for both cases. However, it can be clearly recognized (for conventional as well as optimized modulation) that although the ratio between primary- and secondary-side voltages equals the transformer's turns ratio, the transformer current does not stay at a constant value during the interval where both full-bridges apply a positive (or negative) voltage to the transformers as it would be expected from the simulations. The resulting difference Δi, highlighted in **Fig. 2.28** on the example of port A, results from the magnetizing current that was neglected in the theoretical analysis of the modulation schemes. Due to the aforementioned asymmetry in the inductances, the magnetizing current is supplied almost entirely from the primary (i.e., HV) side of the converter, with negligible

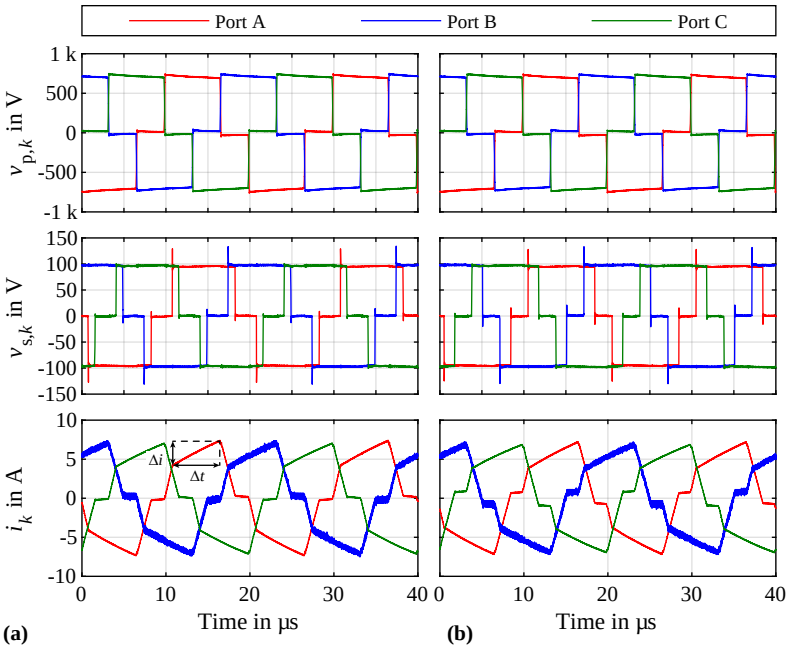


Fig. 2.28: Primary-side voltages $v_{p,k}$, primary transformer currents i_k and secondary-side voltages $v_{s,k}$ for **(a)** conventional and **(b)** optimized modulation under equal loading conditions with $P_A = 2.4\,\text{kW}$, $P_B = 2.4\,\text{kW}$, $P_C = 2.4\,\text{kW}$. Since the output load is equal for all three converter ports, the waveforms for both modulation schemes are almost identical. Although the ratio between primary- and secondary-side voltages equals the transformer's turns ratio, the transformer currents do not stay at a constant value during the interval $\Delta t = 5.5\,\mu\text{s}$ (indicated on the example of transformer current i_A in **(a)**), where both full-bridges apply a positive (or negative) voltage to the transformers as it would be expected from the simulations. The observed deviation from a constant value is caused by the magnetizing currents of the transformers and linearly increases with time due to the constant voltage being applied to the transformer's magnetizing inductances, with a maximum deviation of $\Delta i = 3.5\,\text{A}$ being reached towards the end of the interval.

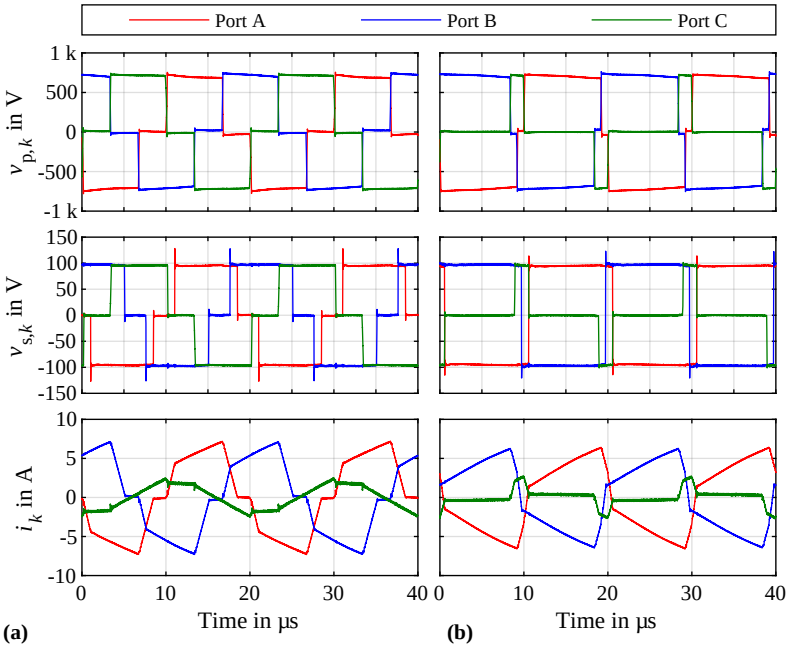


Fig. 2.29: Primary-side voltages $v_{p,k}$, primary transformer currents i_k and secondary-side voltages $v_{s,k}$ for **(a)** conventional and **(b)** optimized modulation under unequal loading conditions with $P_A = 2.4\,\text{kW}$, $P_B = 2.4\,\text{kW}$, $P_C = 200\,\text{W}$. The voltage time area applied to the three transformers is equal under conventional modulation. For optimized modulation, an asymmetry of the applied voltages results, where the voltage time area applied to the transformer of port C, which exhibits the smallest power flow, is heavily reduced, thereby enabling an according increase of the voltage time integral for the remaining ports. This leads to a reduction of the total RMS value of the currents in the system.

contribution from the LV side of the transformer. Therefore, according to the schematic depicted in **Fig. 2.27**, the magnetizing currents $i_{\mathrm{mag},k}$ can be calculated by integration of their respective primary-side voltage $v_{\mathrm{p},k}$,

$$i_{\mathrm{mag},k} = \int \frac{v_{\mathrm{p},k}}{L_{\mathrm{mag}}} \mathrm{d}t, \tag{2.43}$$

where the voltage drop over the stray inductance $L_\sigma/2$ connected in series between L_{mag} and $v_{\mathrm{p},k}$ was neglected since

$$L_{\mathrm{mag}} \gg \frac{L_\sigma}{2} \tag{2.44}$$

applies. Consequently, for the indicated interval $\Delta t = 5.5\,\mu\mathrm{s}$, Δi is determined according to

$$\Delta i = \int_{\Delta t} \frac{v_{\mathrm{p},k}}{L_{\mathrm{mag}}} \mathrm{d}t = \frac{v_{\mathrm{p},k}}{L_{\mathrm{mag}}} \Delta t = 3.5\,\mathrm{A}, \tag{2.45}$$

which corresponds to the value found in **Fig. 2.28**.

Contrary to the symmetric case, in case of asymmetric loading, illustrated in **Fig. 2.29**, it is recognized that the primary-side duty cycles are not symmetric if the optimized modulation parameters are utilized. As expected, the duty cycles of the port with the lowest load (port C) are significantly reduced compared to the remaining ports loaded with nominal power and also compared to what would result from the conventional modulation scheme. This results in an according increase of the duty cycles of the remaining converter ports, thereby allowing for the intended reduction of the respective transformer RMS currents. Due to the low power flow, the transformer current of port C is dominated by the magnetizing current.

In **Fig. 2.30** the measured quadratic sum of the three primary-side transformer RMS current, i.e., the cost function

$$f_{\mathrm{cost}} = I_{\mathrm{A}}^2 + I_{\mathrm{B}}^2 + I_{\mathrm{C}}^2 \tag{2.46}$$

is plotted, with $I_{\{\mathrm{A,B,C}\}}$ being the measured primary-side RMS currents of the three transformers including all harmonic components, i.e., not limited to the base frequency component. In addition, the according results from the theoretical analysis according to **Section 2.2.3** are depicted, again including all harmonic components, where the calculations were adapted to account for the voltage and inductance values utilized for the hardware prototype. It is clearly recognizable from the measured data points that the optimized

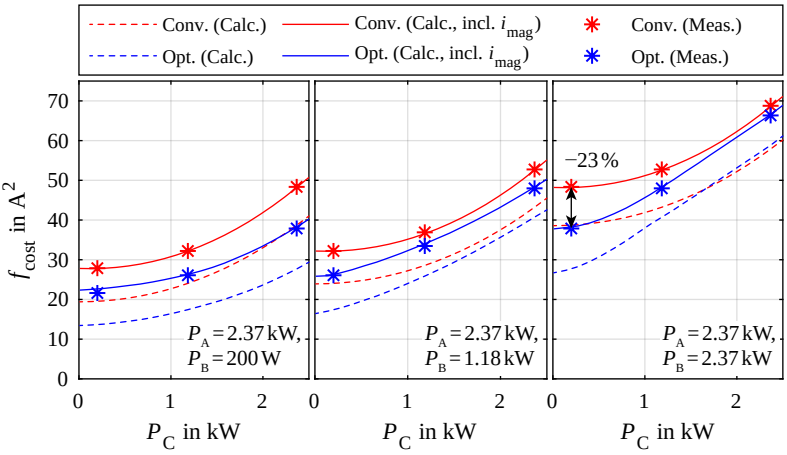


Fig. 2.30: Comparison between measured and calculated cost function values for three given combinations of P_A and P_B. A deviation between measured and calculated (dashed lines) values is observed, which is caused by the magnetizing current that was neglected in the calculation. If the magnetizing current is included in the determination of the cost function, the predicted results (solid lines) accurately match the obtained measurements. A reduction of the cost function by 23 % is obtained for heavily asymmetric operating conditions (e.g., $P_A = 2.4\,\text{kW}$, $P_B = 2.4\,\text{kW}$, $P_C = 200\,\text{W}$).

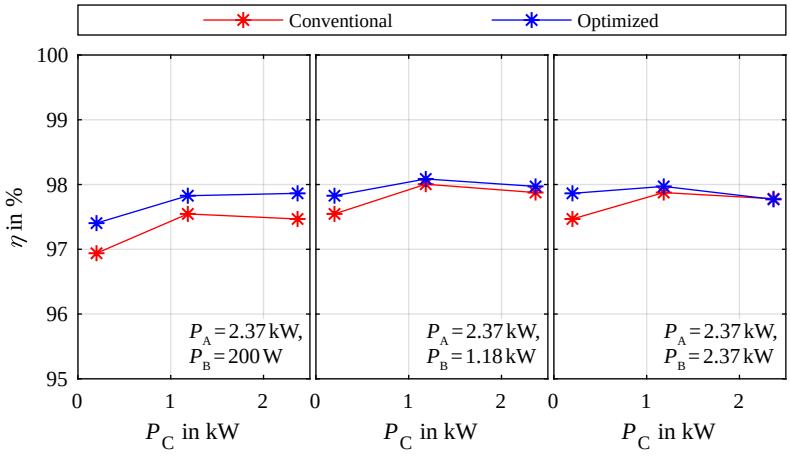


Fig. 2.31: Measured efficiencies of the converter for three given combinations of P_A and P_B. Depending on the operating point, an efficiency improvement of up to 0.5 % is obtained.

modulation scheme leads to a reduction of the cost function f_{cost}, however, the measured values are generally higher than what would result from the calculations. The observed difference results from the contribution of the magnetizing current to the total transformer RMS current, which was neglected in the calculations from **Section 2.2.3**. For this reason, an adapted calculation of the cost function that accounts for the magnetizing current in the determination of the transformer RMS currents is included in **Fig. 2.30**, which presents an almost ideal accordance between measured cost function and numerical calculation and confirms the expected cost function reduction of the optimized modulation scheme.

In addition to f_{cost}, also the efficiency of the converter was measured, with the results presented in **Fig. 2.31**. As expected, the optimized modulation scheme leads to an efficiency improvement especially in asymmetric load scenarios, with improvements of up to 0.5 % for certain operating points. The improvement in efficiency is smaller than what would be expected from the cost function alone, which is caused by additional loss contributions such as transformer core losses and switching losses.

2.2.5 Conclusion

A new modulation strategy for the I3DAB converter, which results from the integration of three conventional DABs, is presented in this chapter, which minimizes the conduction losses occurring in the power converter. Based on fundamental frequency analysis, the operating behavior of the converter is described and available degrees of freedom for converter optimization are identified. The investigated modulation strategy adapts the primary-side duty cycles in accordance to the output power levels, to achieve reduced RMS currents in the power semiconductors and the windings of the HF transformers. Compared to the conventional modulation strategy, it is found that reductions of the total conduction losses are especially feasible if the output power levels provided by the different output ports are subject to large differences. Furthermore, investigations with respect to ZVS reveal that the I3DAB converter may lose ZVS in case of unequal load conditions for both, conventional and optimized modulation strategies. However, ZVS can be regained by reducing the magnetizing inductance of the HF transformers. An exemplary I3DAB converter system serves for the purpose of evaluation. It provides input and output port DC voltages of 700 V and 100 V, respectively, and power levels of up to 4 kW at each output port, i.e., a total power of 12 kW. Depending on the considered operating point, the optimized modulation strategy is found to enable reductions of the total conduction losses by up to 23 %, which is successfully verified by means of numerical circuit simulations. With regard to ZVS, calculated results for 512 different operating points render the optimized modulation scheme more advantageous with respect to ZVS robustness, due to a significantly higher allowable value of the magnetizing inductance (4.59 mH instead of 1.47 mH) needed to ensure ZVS for all operating points.

The obtained findings are further verified by experiments with a scaled-down laboratory prototype system with a nominal power of 2.4 kW per port, where measurements reveal noticeable differences between the predicted and measured cost function values that originate from the magnetizing current that was neglected in the theoretical analysis. However, the proposed modulation scheme still enables a significant reduction of the conduction losses compared to the conventional modulation, with a reduction of the sum of the squared RMS currents of up to 23 % for certain asymmetric operating points. The reduction of the conduction losses results in according efficiency improvements of up to 0.5 %, e.g., from 97 % to 97.5 % for the example of a heavily asymmetric operating point with $P_A = 2.4\,\mathrm{kW}$, $P_B = 200\,\mathrm{W}$ and $P_C = 200\,\mathrm{W}$.

3

UH-PBW Amplifier Stage

This chapter discusses the design of the cascaded H-bridge amplifier stage which was selected for the implementation of the UH-PBW amplifier system based on the topology considerations in **Chapter 1**. The amplifier stage consists of several full-bridge converter cells and an according output filter to attenuate the switching frequency harmonics, which are highlighted in the overview of the entire converter in **Fig. 3.1**. Furthermore, a power supply for the converter is required, where the LF isolation approach introduced in **Section 1.2.2** was selected to supply the CHB cells. It has to be noted that the investigated system is a single-phase power source serving as a base case since a potential three-phase implementation can be composed from three identical single-phase systems. According design specifications of the single-phase amplifier are listed in **Tab. 3.1**.

Tab. 3.1: UH-PBW amplifier specifications.

Nominal AC output power	$P_{\mathrm{nom,AC}}$	10 kW
Nominal DC output power	$P_{\mathrm{nom,DC}}$	20 kW
Nominal peak output voltage (AC)	$\hat{v}_{\mathrm{out,nom}}$	325 V
Maximum peak output voltage (AC)	$\hat{v}_{\mathrm{out,max}}$	470 V
Maximum output voltage (DC)	$V_{\mathrm{max,DC}}$	500 V
Nominal (maximum) output current (DC/AC peak)	$\hat{i}_{\mathrm{out,nom}}$	61.5 A
Full-power bandwidth	$f_{\mathrm{out,max}}$	0 to > 50 kHz
Maximum RMS switching noise	$V_{\mathrm{noise,max}}$	10 mV

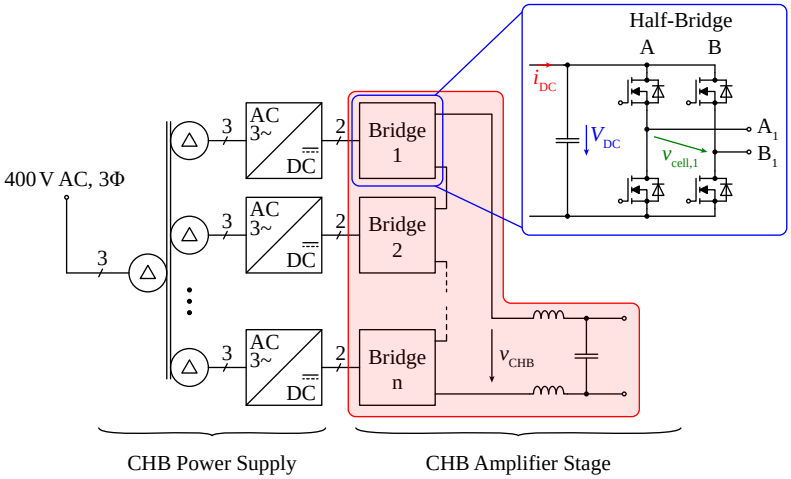


Fig. 3.1: System overview of the UH-PBW amplifier system employing the CHB topology (see **Section 1.1.3**). The amplifier stage consists of a switching stage incorporating several stacked full-bridge inverter cells and an output filter to attenuate the switching frequency harmonics in the output signal.

Regarding the specifications, it has to be noted that no lower output frequency limit is specified, which implies that for potentially arbitrarily low output signal frequencies the converter has to deliver the AC peak power for an unlimited duration of time. For this reason, the continuous output power rating which the converter has to be able to handle corresponds to the AC peak power level, i.e., twice the nominal average AC power (assuming unity power factor as a base case). As a consequence, a maximum continuous output current of 61.5 A results from the maximum power level of 20 kW at the nominal peak voltage of 325 V. Furthermore, **Tab. 3.1** specifies a maximum peak output voltage of 470 V, which originates from a potential application as a grid emulating system with a nominal phase voltage amplitude of 325 V, where the emulation of a 20 % grid overvoltage and an additional 20 % of margin were considered.

Regarding the output voltage quality, an improved criterion was introduced in the above specification, where the total RMS value of the switching noise including all switching frequency harmonics is limited (instead of using a simple peak-to-peak ripple criterion as in **Section 1.2.1**).

The design of the amplifier stage is split into two main subsystems. **Section 3.1** presents the design of the full-bridge inverter stages and according common-mode (CM) filtering measures required to suppress CM currents between the cells. In **Section 3.2** the design of the output filter is conducted, including a performance optimization of the differential-mode (DM) filter stage. In addition, details about the hardware realization of the prototype system are given in **Section 3.3**.

3.1 Cascaded H-Bridge Switching Stage

3.1.1 Inverter Stage Design

The design of the inverter stage of the CHB system starts with the identification of a suitable number of converter cells N_{cell} and the selection of their device switching frequency f_{s} as these are the key parameters which directly determine the achievable output performance of the system. For the modulation of the CHB converter Phase-Shifted Carrier PWM (PSPWM) [65] is used, i.e., each of the full-bridge inverters is modulated with regular unipolar PWM modulation [65] using a single triangular carrier and the individual carriers of all cells are phase-shifted by $^{180^\circ}/_{N_{\text{cell}}}$ with respect to each other. This results in the characteristic multi-level output voltage waveform v_{CHB} of the stack

with the number of voltage levels given by

$$N_{\text{level}} = 2N_{\text{cell}} + 1 \tag{3.1}$$

and an effective switching frequency that results from the multiplication of the semiconductor switching frequency by the number of half-bridges according to

$$f_{\text{s,eff}} = N_{\text{cell}} \cdot 2f_{\text{s}}, \tag{3.2}$$

which is on of the key reasons why the CHB topology was selected for the intended application. **Fig. 3.2** presents an illustration of the resulting waveforms for this modulation scheme considering an exemplary CHB with three full-bridge converter cells.

As already briefly illustrated in **Section 1.2.1**, a relation between the number of cells N_{cell} and the switching frequency of the half-bridges f_{s} can then be derived by combining the constraints originating from the output filter's reactive power demand and the required output voltage quality: on the one hand, the size of the filter components is limited by their reactive power consumption which rises with increasing output signal frequency $f_{\text{out,max}}$. On the other hand sufficient filter attenuation at the effective switching frequency $f_{\text{s,eff}}$ is required such that the desired output voltage quality can be achieved for a given number of voltage levels. This is accomplished by either selecting a sufficiently high switching frequency f_{s} of the half-bridges or by increasing the number of cells N_{cell}, where increasing the number of cells not only increases $f_{\text{s,eff}}$ and N_{level} directly, but also reduces the cell's DC-link voltage according to

$$V_{\text{DC,cell}} = \frac{V_{\text{DC,tot}}}{N_{\text{cell}}}, \tag{3.3}$$

where $V_{\text{DC,tot}}$ is the total summed DC-link voltage of all cells that is selected based on the required maximum output voltage of the converter plus some margin. A reduced cell DC-link voltage allows to use semiconductors with a smaller blocking voltage rating, which usually exhibit a better Figure of Merit and as a consequence allow the half-bridges to be operated at a higher switching frequency f_{s}, thereby further increasing $f_{\text{s,eff}}$. Since the maximum switching frequency is limited by the semiconductors used, i.e., their blocking voltage rating, whereas increasing the number of cells implies a higher hardware effort as more cells and semiconductors have to be controlled, a reasonable tradeoff between N_{cell} and f_{s} has to be identified.

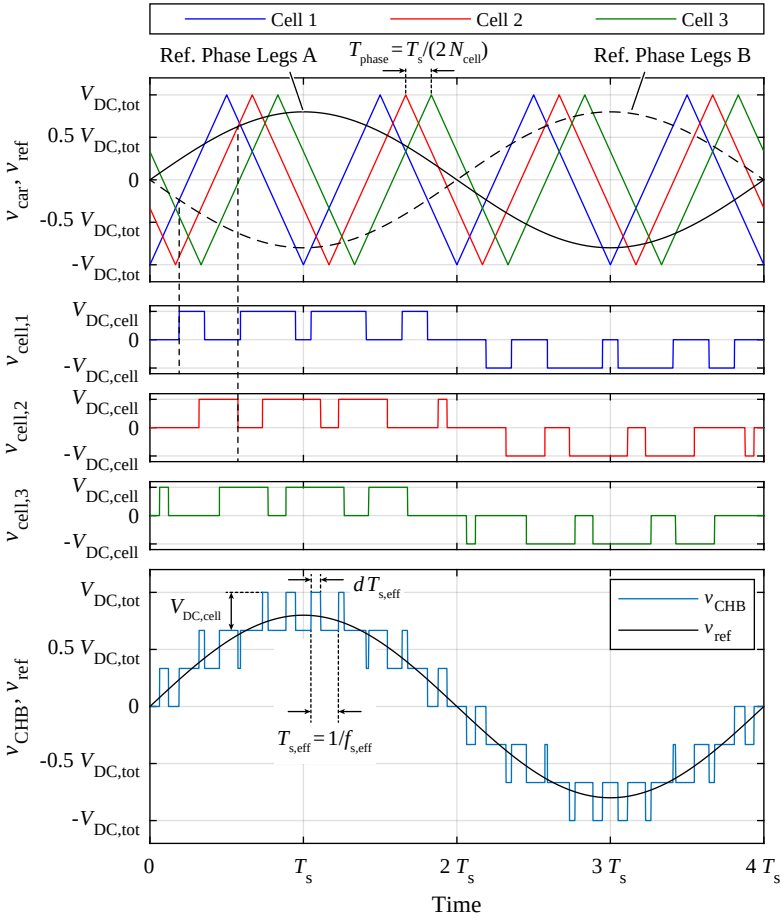


Fig. 3.2: PSPWM modulation scheme for an exemplary CHB converter consisting of $N_{cell} = 3$ converter cells and a sinusoidal reference signal. The output voltages of the individual full-bridge inverters ($v_{cell,1}$ to $v_{cell,3}$, cf. **Fig. 3.1**) are generated by a regular unipolar modulation scheme [65], with half-bridge A ("positive" half-bridge) of all cells controlled by the reference signal v_{ref} and half-bridge B ("negative" half-bridge) of all cells controlled by the inverted reference signal $-v_{ref}$. The triangular carrier signals $v_{car,1}$ to $v_{car,3}$ of the cells are phase-shifted by $T_{phase} = T_s/(2N_{cell})$, with T_s being the carrier period. As a consequence, the multi-level output voltage v_{CHB} results from the series connection of the full-bridge inverters at the stack output. The output voltage exhibits an effective switching frequency of $f_{s,eff} = 2N_{cell}f_s$ since the interleaving of the PWM carriers results in a cancellation of all lower frequency PWM harmonics.

In the following, two different cases are considered involving either a single-stage or a two-stage LC filter at the converter output (cf. **Fig. 3.3**). In both cases, the first stage filter inductor and capacitor are referred to as L_1 and C_1, respectively, whereas in case of the two-stage filter, the component ratios $k = {}^{L_2}/_{L_1}$ and $m = {}^{C_2}/_{C_1}$ are used in the following (instead of the second stage elements L_2 and C_2). This allows the characteristic frequency ω_0 to be defined as

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{3.4}$$

for both filter structures. The according corner frequencies can then be expressed by

$$\begin{aligned} \omega_c &= \omega_0 && \text{(single-stage filter)}, \\ \omega_{c,1} &= \omega_0 \cdot a_1, \quad \omega_{c,2} = \omega_0 \cdot a_2 && \text{(two-stage filter)}, \end{aligned} \tag{3.5}$$

where the factors a_1 and a_2 in case of the two-stage filter are given by the component ratios m and k according to

$$\begin{aligned} a_1 &= \frac{1}{\sqrt{2}} \sqrt{1 + \frac{1}{k} + \frac{1}{km} - \frac{\sqrt{-4km + (1+m+km)^2}}{km}}, \\ a_2 &= \frac{1}{\sqrt{2}} \sqrt{1 + \frac{1}{k} + \frac{1}{km} + \frac{\sqrt{-4km + (1+m+km)^2}}{km}}. \end{aligned} \tag{3.6}$$

In both cases it is assumed that the effective switching frequency of the converter is sufficiently above all corner frequencies, which allows the filter attenuation at an angular frequency ω in the stopband to be described by its asymptotic approximation (i.e., a constant slope with -40 dB/dec per stage is assumed), resulting in an approximation for the attenuation A_{filt}:

$$\begin{aligned} A_{\text{filt,single}}(\omega) &= \frac{\omega^2}{{\omega_c}^2} = \omega^2 L_1 C_1 && \text{(single-stage filter)}, \\ A_{\text{filt,two}}(\omega) &= \frac{\omega^2}{{\omega_{c,1}}^2} \frac{\omega^2}{{\omega_{c,2}}^2} = \omega^4 \left(\frac{L_1 C_1}{a_1 a_2} \right)^2 && \text{(two-stage filter)}. \end{aligned} \tag{3.7}$$

In addition, it has to be mentioned that the procedure described in the following to determine the required number of cells and their switching frequency only takes the reactive power demand of the filter and the output voltage quality into account. However, additional dynamic criteria are introduced later

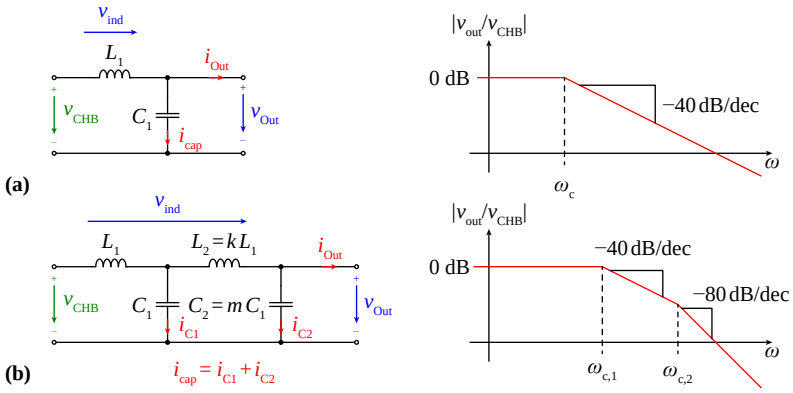


Fig. 3.3: (a) Single-stage and **(b)** two-stage LC filter structures and their transfer functions (asymptotic approximation) in the frequency domain.

which add further constraints on the design of the output filter. Therefore, the maximum achievable output frequency obtained from the final filter design (see **Section 3.2**) will be lower than the design value used in the following.

Determination of N_{cell} and f_s

As already mentioned above, the design constraints for N_{cell} and f_s originate from the required filter attenuation, which in turn is limited by the maximum reactive power demand of the filter components. For this reason, the according expressions for the maximum inductive filter voltage drop $\hat{v}_{\text{ind,max}}$ and the maximum capacitive filter current $\hat{i}_{\text{cap,max}}$ of the output filter stage (cf. **Fig. 3.3**) are required in a first step. In case of the maximum inductive voltage drop, this results in

$$\begin{aligned} \hat{v}_{\text{ind,max}} &= 2\pi f_{\text{out,max}} L_1 \, \hat{i}_{\text{out,nom}} && \text{(single-stage filter)}, \\ \hat{v}_{\text{ind,max}} &= 2\pi f_{\text{out,max}} L_1 (1+k) \, \hat{i}_{\text{out,nom}} && \text{(two-stage filter)}, \end{aligned} \tag{3.8}$$

where, in order to simplify the expressions, only the load current was considered, i.e., the calculation of $\hat{v}_{\text{ind,max}}$ neglects the current flowing into the filter capacitors C_1 and C_2. This is justified since the capacitive current demand is later limited to a fraction of the load current. Furthermore, in case of a unity power factor load, which is assumed as base case, these currents exhibit a phase shift of 90° against v_{out}, thereby implying a minor contribution of

the capacitive current to the total current flowing through the filter inductor since both components would have to be added geometrically. Similarly, the maximum capacitive filter current can be estimated by

$$\begin{aligned} \hat{i}_{\mathrm{cap,max}} &= 2\pi f_{\mathrm{out,max}} C_1 \hat{v}_{\mathrm{out,max}} && \text{(single-stage filter)}, \\ \hat{i}_{\mathrm{cap,max}} &= 2\pi f_{\mathrm{out,max}} C_1 (1+m) \hat{v}_{\mathrm{out,max}} && \text{(two-stage filter)}, \end{aligned} \tag{3.9}$$

where in case of the two-stage filter the voltage drop over L_2 is neglected, i.e., the output voltage v_{out} is assumed to be applied to C_1 and C_2 directly.

According limitations of these quantities are then expressed as ratios p and q of the maximum output voltage and output current of the converter, respectively, which results in the following inequalities:

$$\begin{aligned} \hat{v}_{\mathrm{ind,max}} &= 2\pi f_{\mathrm{out,max}} L_1 \hat{i}_{\mathrm{out,nom}} &&< p\,\hat{v}_{\mathrm{out,max}} \\ \hat{i}_{\mathrm{cap,max}} &= 2\pi f_{\mathrm{out,max}} C_1 \hat{v}_{\mathrm{out,max}} &&< q\,\hat{i}_{\mathrm{out,nom}} \end{aligned} \quad \text{(single-stage filter)},$$

$$\begin{aligned} \hat{v}_{\mathrm{ind,max}} &= 2\pi f_{\mathrm{out,max}} L_1 (1+k) \hat{i}_{\mathrm{out,nom}} &&< p\,\hat{v}_{\mathrm{out,max}} \\ \hat{i}_{\mathrm{cap,max}} &= 2\pi f_{\mathrm{out,max}} C_1 (1+m) \hat{v}_{\mathrm{out,max}} &&< q\,\hat{i}_{\mathrm{out,nom}} \end{aligned} \quad \text{(two-stage filter)}. \tag{3.10}$$

Rearranging of the above expressions to p and q and multiplication results in an lower bound for the characteristic frequency ω_0 of the filter as a function of the maximum output frequency $f_{\mathrm{out,max}}$:

$$\begin{aligned} \omega_0^2 &= \frac{1}{L_1 C_1} > \frac{\omega_{\mathrm{out,max}}^2}{pq} && \text{(single-stage filter)}, \\ \omega_0^2 &= \frac{1}{L_1 C_1} > \frac{\omega_{\mathrm{out,max}}^2}{pq}(1+k)(1+m) && \text{(two-stage filter)}, \end{aligned} \tag{3.11}$$

with $\omega_{\mathrm{out,max}} = 2\pi f_{\mathrm{out,max}}$ being the maximum angular frequency of the output voltage.

In a second step the required attenuation of the filter is determined in order to meet the desired signal quality of the output voltage. The according calculations are simplified by approximating the noise spectrum with a single noise component V_{noise} at the effective switching frequency $f_{\mathrm{s,eff}}$, containing the entire noise energy of all switching harmonics including their sidebands, instead of a distributed spectrum. Consequently, the required filter attenuation $A_{\mathrm{filt,min}}$ at $f_{\mathrm{s,eff}}$ is then estimated by the effective noise component V_{noise}

according to

$$A_{\text{filt,min}}(f_{\text{s,eff}}) = \frac{V_{\text{noise}}(f_{\text{s,eff}})}{\frac{1}{2}V_{\text{noise,max}}(f_{\text{s,eff}})}, \tag{3.12}$$

with the noise limit $V_{\text{noise,max}}$ taken from **Tab. 3.1** and an additional factor of $1/2$ since half of the noise voltage margin will be required to account for CM noise when designing the CM filter.

Since the effective noise voltage V_{noise} is approximated by the total high-frequency RMS noise of the filter input voltage, it can be calculated from the RMS value of the filter input voltage v_{CHB} with the desired output signal v_{out} (assumed as purely sinusoidal) subtracted

$$V_{\text{noise}} = \sqrt{V_{\text{CHB}}^2 - V_{\text{out}}^2} = \sqrt{\frac{1}{T_{\text{out}}}\int_0^{T_{\text{out}}} [v_{\text{CHB}}(t') - v_{\text{out}}(t')]^2 \mathrm{d}t'}, \tag{3.13}$$

where V_{CHB} and V_{out} are the according RMS values of v_{CHB} and v_{out}, respectively, and T_{out} denotes the period of the output signal. The integral in (3.13) can be reformulated by using the local RMS value

$$V_{\text{noise}}(t) = \sqrt{\frac{1}{T_{\text{eff}}}\int_t^{t+T_{\text{eff}}} [v_{\text{CHB}}(t') - v_{\text{out}}(t')]^2 \mathrm{d}t'} \tag{3.14}$$

which is defined as the RMS value over an effective switching frequency period $T_{\text{eff}} = 1/f_{\text{s,eff}}$ instead of the entire signal period T_{out} and therefore varies over the output signal period. Due to the high ratio between signal frequency $f_{\text{out}} = 1/T_{\text{out}}$ and effective switching frequency, the desired signal v_{out} is assumed to be constant during T_{eff}. Accordingly, the expression for $V_{\text{noise}}(t)$ results in the RMS value of a zero-mean rectangular signal

$$V_{\text{noise}}(t) = \frac{V_{\text{DC,tot}}}{N_{\text{cell}}}\sqrt{d(t)(1-d(t))} \tag{3.15}$$

with a peak-to-peak amplitude of $V_{\text{DC,tot}}/N_{\text{cell}}$ and a local duty cycle of $d(t)$ (cf. **Fig. 3.2**). Combining the equations leads to an approximation for the noise

voltage

$$\begin{aligned} V_{\text{noise}} &= \sqrt{\frac{1}{T_{\text{out}}}\int_0^{T_{\text{out}}} [v_{\text{CHB}}(t') - v_{\text{out}}(t')]^2 \,\mathrm{d}t'} \\ &= \sqrt{\frac{1}{T_{\text{out}}}\int_0^{T_{\text{out}}} V_{\text{noise}}^2(t')\mathrm{d}t'} \\ &= \sqrt{\frac{1}{T_{\text{out}}}\int_0^{T_{\text{out}}} \left[\frac{V_{\text{DC,tot}}}{N_{\text{cell}}}\sqrt{d(t)(1-d(t))}\right]^2 \mathrm{d}t} \\ &< \frac{V_{\text{DC,tot}}}{N_{\text{cell}}}\sqrt{\frac{1}{T_{\text{out}}}\int_0^{T_{\text{out}}} \left[\frac{1}{2}\right]^2 \mathrm{d}t} \\ &= \frac{V_{\text{DC,tot}}}{N_{\text{cell}}}\frac{1}{2}, \end{aligned} \tag{3.16}$$

where $d(t) = 0.5$ was used for the local RMS voltage by means of a worst case approximation. Consequently, the required filter attenuation at $f_{\text{s,eff}}$ can be determined by

$$A_{\text{filt,min}}(f_{\text{s,eff}}) = \frac{V_{\text{noise}}(f_{\text{s,eff}})}{\frac{1}{2}V_{\text{noise,max}}(f_{\text{s,eff}})} = \frac{\frac{V_{\text{DC,tot}}}{N_{\text{cell}}}}{V_{\text{noise,max}}}. \tag{3.17}$$

By combining (3.17) and (3.7), conditions for the required filter attenuation at $\omega_{\text{eff}} = 2\pi f_{\text{s,eff}}$ are obtained for both filter structures

$$\begin{aligned} A_{\text{filt,single}}(\omega_{\text{eff}}) &= {\omega_{\text{eff}}}^2 L_1 C_1 > \frac{V_{\text{DC,tot}}}{V_{\text{noise,max}}\, N_{\text{cell}}} \qquad \text{(single-stage filter)}, \\ A_{\text{filt,two}}(\omega_{\text{eff}}) &= {\omega_{\text{eff}}}^4 \left(\frac{L_1 C_1}{a_1 a_2}\right)^2 > \frac{V_{\text{DC,tot}}}{V_{\text{noise,max}}\, N_{\text{cell}}} \qquad \text{(two-stage filter)}, \end{aligned} \tag{3.18}$$

which by using $f_{\text{s,eff}} = 2N_{\text{cell}} f_{\text{s}}$ translate to

$$\begin{aligned} f_{\text{s}}^2 &> \frac{V_{\text{DC,tot}}}{16\pi^2 N_{\text{cell}}^3 V_{\text{noise,max}}}\frac{1}{L_1 C_1} \qquad \text{(single-stage filter)}, \\ f_{\text{s}}^4 &> \frac{V_{\text{DC,tot}}}{256\pi^4 N_{\text{cell}}^5 V_{\text{noise,max}}}\left(\frac{a_1 a_2}{L_1 C_1}\right)^2 \qquad \text{(two-stage filter)}. \end{aligned} \tag{3.19}$$

Finally, inserting the characteristic frequency limits from (3.11) leads to the minimum required device switching frequency as a function of the number of cells

$$f_\mathrm{s} > f_\mathrm{out,max}\sqrt{\frac{V_\mathrm{DC,tot}}{4N_\mathrm{cell}^3 V_\mathrm{noise,max} pq}} \qquad \text{(single-stage filter)},$$
$$f_\mathrm{s} > f_\mathrm{out,max}\sqrt[4]{\frac{V_\mathrm{DC,tot}}{16N_\mathrm{cell}^5 V_\mathrm{noise,max}}\left(\frac{a_1 a_2(1+k)(1+m)}{pq}\right)^2} \qquad \text{(two-stage filter)}. \tag{3.20}$$

By choosing suitable values for the maximum relative inductive filter voltage and capacitive filter currents of $p = 2/3$ and $q = 1/2$, respectively, the required switching frequencies can be determined, which is shown in **Fig. 3.4** together with the resulting DC-link voltage $V_\mathrm{DC,cell}$ of each cell for $f_\mathrm{out,max} = 100\,\mathrm{kHz}$ and a total DC-link voltage of $V_\mathrm{DC,tot} = 600\,\mathrm{V}$. The total DC-link voltage is determined by the maximum DC output voltage of 500 V and an additional modulation reserve of 20 %. This also guarantees sufficient voltage reserve in case of AC modulation for all operating points, since the required voltage reserve can be estimated from the geometric sum of the output voltage and the voltage drop over the filter inductor v_ind

$$\sqrt{\hat{v}_\mathrm{out}^2 + \hat{v}_\mathrm{ind}^2} < \sqrt{\hat{v}_\mathrm{out,max}^2 + \hat{v}_\mathrm{ind,max}^2} < 600\,\mathrm{V}, \tag{3.21}$$

where again unity power factor for the load is assumed as a reference load case and the filter capacitor current is neglected. In case of the two-stage filter, the component ratios were selected to $k = m = 1$ as a base case, although the filter optimization in **Section 3.2** later deviates from these values.

From **Fig. 3.4** a suitable N_cell and f_s have to be selected, where the main design aspect is the achievable switching frequency of the semiconductors that depends on the DC-link voltage as well as the semiconductor technology used. Due to the resulting voltage and frequency ranges, IGBTs as well as silicon carbide (SiC) MOSFETs are not suitable, as the resulting operating voltages are significantly below 400 V. Gallium nitride (GaN) devices would represent a suitable option and usually outperform silicon (Si) MOSFETs for the voltages at the case at hand [199]. However, since GaN devices were only commercially available for less than ten years at the point in time where this decision had to be made (e.g., the first commercially available GaN power switch with a blocking voltage of 600 V was mentioned in 2012 [200]), industrial experience regarding reliability, lifetime, failure rates and second source availability was

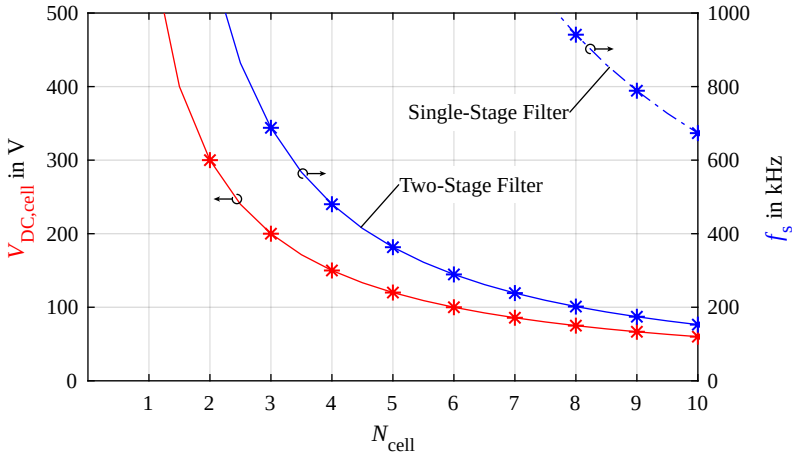


Fig. 3.4: Required cell DC-link voltage and half-bridge switching frequency depending on the number of cells in order to guarantee the desired output voltage quality as well as the reactive power limitations of the filter. A two-stage filter is selected since an excessively high number of cells or extremely high switching frequencies would result for a single-stage filter.

limited, which is an important aspect for a potential commercial application. For this reason and since the obtained voltage and switching frequency values are also considered feasible with Si MOSFETs, it was decided to use Si devices for the implementation of the inverter.

From **Fig. 3.4** it can be recognized that for the case of a single-stage filter a very high number of cells $N_{cell} \gtrapprox 10$ would be needed to bring the required device switching frequency in achievable ranges, i.e., $f_s < 1\,\text{MHz}$ (e.g., $f_s > 788\,\text{kHz}$ and $V_{DC,cell} = 67\,\text{V}$ result for $N_{cell} = 9$). Consequently, a single-stage filter is considered unsuitable and a two-stage filter is selected for the filter design. In case of a two-stage filter, reasonable values for N_{cell} are identified as $N_{cell} \geq 5$ since $N_{cell} = 4$ would still imply $f_s = 480\,\text{kHz}$, which is considered infeasible at $V_{DC,cell} = 150\,\text{V}$. [1] Furthermore, the curve starts to flatten above $N_{cell} = 7$ (e.g., less than 15 % reduction of f_s when changing from 8 to 9 cells), which allows to identify suitable values for N_{cell} to lie between $N_{cell} = 5$ and $N_{cell} = 7$. The selection of N_{cell} is further influenced

[1] With the loss model introduced later in this section, losses of 30 W per MOSFET are calculated on an exemplary case of 6 parallel connected BSZ900N20NS3 transistors. This is already at the limit of what their package can dissipate for a case temperature of 80 °C.

Type	Series	$R_{ds,on}$ (max., $T_j = 25\,°C$)	Identifier
BSC093N15NS5	OptiMOS 5	9.3 mΩ	1
BSC110N15NS5	OptiMOS 5	11 mΩ	2
BSC160N15NS5	OptiMOS 5	16 mΩ	3
IPB044N15N5	OptiMOS 5	4.4 mΩ	4
IPB060N15N5	OptiMOS 5	6.0 mΩ	5
IPT059N15N3	OptiMOS 3	5.9 mΩ	6
BSB165N15NZ3	OptiMOS 3	16.5 mΩ	7
IPT111N20NFD	OptiMOS 3	11.1 mΩ	8
IRF7779L2PbF	StrongIRFET	11 mΩ	9

Tab. 3.2: Considered MOSFETs for the inverter half-bridges. All devices are 150 V devices from Infineon.

by the available breakdown voltages of the MOSFETs, where manufacturers offer 100 V, 120 V, 150 V, 200 V devices. Including a typical margin of ≈ 75 % between DC-link and breakdown voltage, this would still imply 200 V devices to be required for $N_{cell} = 5$ (same devices as for $N_{cell} = 4$), whereas in case of 6 cells 150 V devices can be used that feature lower conduction and switching losses. For this reason, a six-cell system with a switching frequency of $f_s = 300\,kHz$ (rounded up from 289 kHz) was finally selected.

Inverter Half-Bridge Design

With the device switching frequency and the cell's DC-link voltage given, the design of the cell's inverter bridge-legs can be conducted, where the key design aspect is the dissipation of the losses that are expected to be dominated by the switching losses. For the design of the bridge-legs, several MOSFETs from *Infineon* listed in **Tab. 3.2** with a blocking voltage rating of 150 V are compared. Due to the required current, parallel connection of several devices is required, where the number of parallel devices N_{par} represents an additional degree of freedom. The configuration of the bridge (device type, N_{par}) is then chosen such that a suitable tradeoff between the total bridge losses, the losses per device (corresponding to cooling effort) and the number of required devices is achieved. **Tab. 3.3** summarizes the operating conditions considered for the inverter half-bridge design. Note that the loss calculations are simplified by neglecting the switching frequency

Parameter		Value
DC-link voltage	$V_{\mathrm{DC,cell}}$	100 V
Max. output current (DC, RMS)	$I_{\mathrm{b,max}}$	61.5 A
Max. output current (peak)	$\hat{i}_{\mathrm{b,max}}$	65 A
Switching frequency	f_{s}	300 kHz
Max. ambient temperature	T_{amb}	55 °C

Tab. 3.3: Half-bridge design specifications.

ripple of the output current. The peak output current $\hat{i}_{\mathrm{b,max}}$ of the bridge results from the geometric sum of load current and capacitive filter current in case of unity power factor load according to

$$\hat{i}_{\mathrm{b}} = \sqrt{i_{\mathrm{out}}^2 + i_{\mathrm{cap}}^2} = \sqrt{\left(\frac{2P_{\mathrm{nom,AC}}}{\hat{v}_{\mathrm{out}}}\right)^2 + \left(q\hat{i}_{\mathrm{nom,max}}\frac{\hat{v}_{\mathrm{out}}}{\hat{v}_{\mathrm{out,max}}}\right)^2}, \tag{3.22}$$

with the according maximum of $\hat{i}_{\mathrm{b,max}} = 65\,\mathrm{A}$ reached at $\hat{v}_{\mathrm{out}} = 325\,\mathrm{V}$. However, the worst-case operating point regarding the bridge losses results for DC operation with the maximum rated (see **Tab. 1.1**) output current of $I_{\mathrm{b,max}} = 61.5\,\mathrm{A}$.

In order to calculate the maximum losses occurring in the bridge, the according expressions for the conduction and switching losses have to be determined considering worst-case conditions. The worst case is achieved for the rated maximum DC output current of I_{b}=$I_{\mathrm{b,max}} = 61.5\,\mathrm{A}$ and a modulation index of $M = {}^{v_{\mathrm{out}}}/_{V_{\mathrm{DC,tot}}} = 54\,\%$, corresponding to the maximum DC output power of $P_{\mathrm{nom,DC}} = 20\,\mathrm{kW}$ that is achieved at 325 V DC output voltage. The conduction losses for a single device in case of N_{par} parallel connected MOSFETs can then be directly calculated according to

$$P_{\mathrm{cond,dev}} = R_{\mathrm{ds,on,max}}\left(\frac{I_{\mathrm{b,max}}}{N_{\mathrm{par}}}\right)^2 D, \tag{3.23}$$

with the on-state resistance $R_{\mathrm{ds,on,max}}$ taken from the datasheet at the maximum junction temperature $T_{\mathrm{j}} = 150\,^{\circ}\mathrm{C}$, and D being the relative on time, given by the modulation index according to

$$D = \frac{1+M}{2}. \tag{3.24}$$

Similarly, for the total half-bridge the conduction losses are given by

$$P_{\text{cond,tot}} = \frac{R_{\text{ds,on,max}}}{N_{\text{par}}} I_{\text{b,max}}^2. \tag{3.25}$$

Contrary to the conduction losses, accurate modeling of the switching losses is more challenging and according models are relatively complex since they depend on parasitic elements and device parameters [201], which are often not available or specified. For this reason, a simplified approach presented in [202] is utilized, which estimates the hard-switching losses of a single MOSFET to

$$P_{\text{sw,dev}} = f_{\text{s}} V_{\text{DC,cell}} \left(Q_{\text{oss}} + Q_{\text{rr}} \left(\frac{I_{\text{b}}}{N_{\text{par}}} \right) \right). \tag{3.26}$$

The expression in (3.26) depends on two charges Q_{oss} and Q_{rr}. Q_{oss} refers to the charge stored in the (nonlinear) drain-source capacitance C_{oss} and is obtained by numerical integration of the C_{oss} curve given in the datasheet according to

$$Q_{\text{oss}} = \int_0^{V_{\text{DC,cell}}} C_{\text{oss}}(v) \mathrm{d}v. \tag{3.27}$$

Q_{rr} denotes the reverse recovery charge of the MOSFET body diode. Its value is obtained from the device datasheet by assuming a linear relation between Q_{rr} and the switched current i_{sw} as a simplifying approximation, which allows rescaling of the datasheet value $Q_{\text{rr,datasheet}}$ given at a current $i_{\text{Qrr,datasheet}}$ according to

$$Q_{\text{rr}}(i_{\text{sw}}) = Q_{\text{rr,datasheet}} \frac{i_{\text{sw}}}{i_{\text{Qrr,datasheet}}} \tag{3.28}$$

and justifies the above stated $1/N_{\text{par}}$ dependency. Note that in a half-bridge either the low-side (LS) or the high-side (HS) switch (depending on the output current direction) incurs the total hard-switching losses while the switching losses of its respective counterpart are negligible since it acts as synchronous rectifier that only switches at zero voltage. Again, the worst case losses result for the maximum DC output current of the bridge, i.e., $I_{\text{b}} = I_{\text{b,max}}$. Based on (3.26), the switching losses of the total half-bridge, i.e., all devices combined, are given by

$$P_{\text{sw,tot}} = f_{\text{s}} V_{\text{DC,cell}} \left(N_{\text{par}} Q_{\text{oss}} + Q_{\text{rr}}(I_{\text{b}}) \right) = k_{\text{sw,0}} + k_{\text{sw,1}} I_{\text{b}}, \tag{3.29}$$

where the assumption of a linear relation between the switching losses $P_{\mathrm{sw,tot}}$ and the output current I_{b} was also found by the experimental data of [199] for a similar device.

It has to be noted that the switching losses are expected to be considerably higher than what the estimations in (3.26) and (3.29) suggest. The current-independent switching loss component originating from Q_{oss} (also referred to as zero-current switching (ZCS) losses) is expected to provide relatively accurate results, however, the reverse recovery charge Q_{rr} taken from the MOSFET's datasheets is specified for a current slope of $\mathrm{d}i/\mathrm{d}t = 100\,\mathrm{A/\mu s}$ and a junction temperature of $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$, while real operating conditions imply significantly higher values for these quantities, thereby increasing Q_{rr}. Furthermore, the model does not account for the overlap losses [203] which result from the overlap of load current and switch voltage during the switching transient. However, (3.29) is still useful for a comparison of different devices.

The results of the loss calculation are shown in **Fig. 3.5** for the total bridge losses $P_{\mathrm{tot}} = P_{\mathrm{cond,tot}} + P_{\mathrm{sw,tot}}$ and in **Fig. 3.6** for the maximum losses per MOSFET $P_{\mathrm{dev}} = P_{\mathrm{cond,dev}} + P_{\mathrm{sw,dev}}$ considering the devices listed in **Tab. 3.2** and different numbers of parallel devices. It is recognized that especially the three *BSC* devices feature low switching losses in general and low total losses for higher N_{par} values. For this reason and due to the large potential uncertainty associated with the estimation of the switching losses, only the three *BSC* devices are considered in the further design process. In addition, a total bridge loss minimum of ca. 31 W exists, which is achieved for different combinations of devices and N_{par}.

In order to verify the calculations, a prototype of the half-bridge containing six *BSC160N15NS5* devices (device identifier 3 in **Fig. 3.5** and **Fig. 3.6**) connected in parallel (which were selected due to their lower switching losses compared to the *BSC093N15NS5* and *BSC110N15NS5* devices while also keeping N_{par} limited to simplify the PCB layout), was constructed and the total losses were measured calorimetrically. The calorimetric measurements are conducted by placing the entire half-bridge prototype in a thermally isolated chamber which has its temperature controlled to a fixed temperature of 35 °C by a cooling system [204]. The heat flow that has to be extracted from the chamber to keep the temperature constant is measured and corresponds to the total heat energy generated in the chamber, which originates from the losses of the half-bridge and the power consumption of its auxiliary systems such as gate drives and cooling fans. By subtracting the power demand of gate drives and fans, which can be determined from their respective DC power

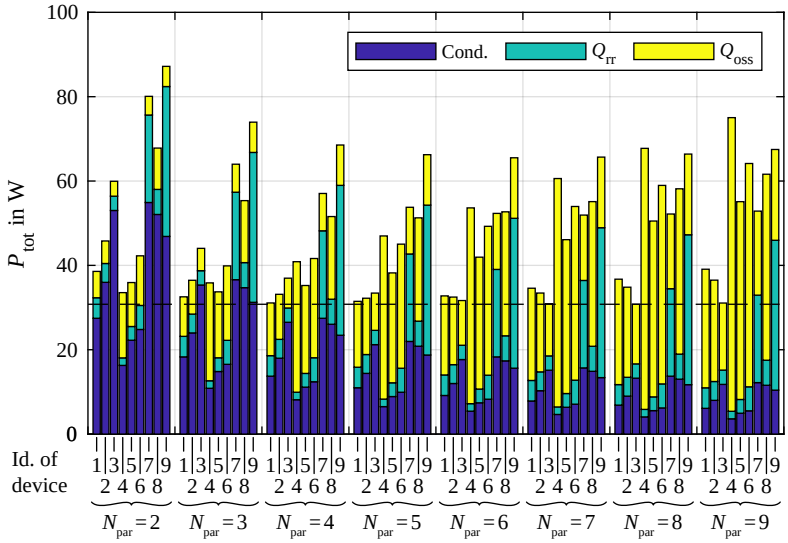


Fig. 3.5: Total half-bridge losses for different MOSFET types, depending on the number of paralleled devices. The losses are split into conduction losses (labeled "Cond.") and the two switching loss contributions originating from the parasitic capacitance of the MOSFET (labeled "Q_{oss}") and the reverse recovery charge (labeled "Q_{rr}"). A loss minimum of 31 W is found, which is reached by several combinations of devices and N_{par}.

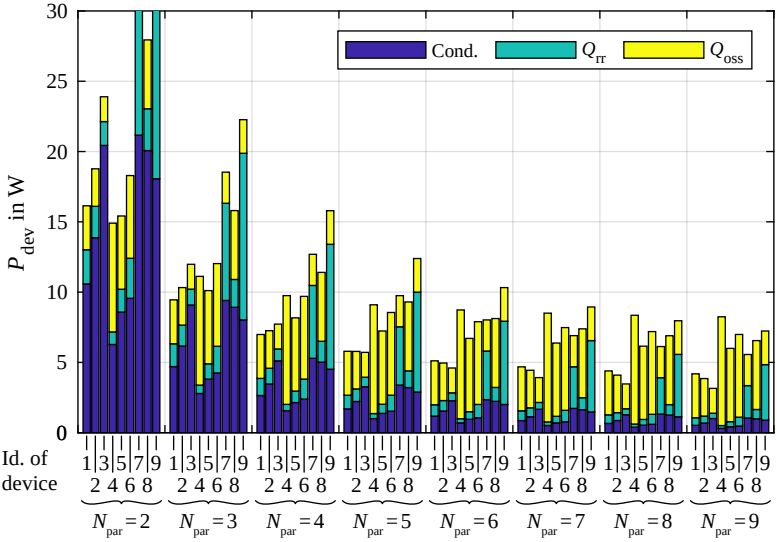


Fig. 3.6: Losses per single device for different MOSFET types, depending on the number of paralleled devices. The losses are split into conduction losses (labeled "Cond.") and the two switching loss contributions originating from the parasitic capacitance of the MOSFET (labeled "Q_{oss}") and the reverse recovery charge (labeled "Q_{rr}")

Load current	Total Losses	Auxiliary (Gate drive, fans)	Bridge Losses	Conduction Losses	Switching Losses
30 A	41.9 W	6.5 W	35.4 W	2.7 W	32.7 W
59.5 A	74.5 W	7.1 W	67.4 W	10.8 W	56.6 W

Tab. 3.4: Calorimetric measurement results of the prototype half-bridge for two different DC operating points with half-bridge load currents of $I_\mathrm{b} = 30\,\mathrm{A}$ and $I_\mathrm{b} = 59.5\,\mathrm{A}$, respectively. The tested half-bridge contains six *BSC160N15NS5* devices and was operated with a DC-link voltage of 100 V, a switching frequency of 300 kHz and a duty cycle of 54 %.

consumption, the total bridge losses P_tot can be calculated. From the total bridge losses, the switching losses $P_\mathrm{sw,tot}$ can be determined by subtracting the calculated conduction losses according to

$$P_\mathrm{sw,tot} = P_\mathrm{tot} - I_\mathrm{b}^2\, R_\mathrm{ds,on}, \tag{3.30}$$

where the temperature to evaluate the on-state resistance $R_\mathrm{ds,on}$ was approximated by measuring the surface temperature of the MOSFET packages and adding an estimate of 30 °C to account for the temperature difference between junction and case. This method provides reasonably accurate results compared to an electric measurement of the switch voltage and current overlap, which suffers from the inductance introduced by the current probe in the commutation loop and potential errors originating from time delay differences between voltage and current measurement [205, 206].

The results of the calorimetric loss measurements are summarized in **Tab. 3.4** for two operating points with different output currents, where for both cases a DC-link voltage of 100 V and a switching frequency of 300 kHz was used. Assuming a linear relation for the switching losses,

$$P_\mathrm{sw} = k_\mathrm{sw,0} + k_\mathrm{sw,1}\, I_\mathrm{b}, \tag{3.31}$$

according to (3.29), the measured coefficients $k_\mathrm{sw,0,meas} = 8.4\,\mathrm{W}$ and $k_\mathrm{sw,1,meas} = 0.81\,\mathrm{W/A}$ can be determined from the measured loss data and compared to the expectations from (3.29), which result to $k_\mathrm{sw,0} = 10.6\,\mathrm{W}$ and $k_\mathrm{sw,1} = 55\,\mathrm{mW/A}$ for a datasheet value of $Q_\mathrm{rr}\,(28\,\mathrm{A}) = 51.4\,\mathrm{nC}$ and $Q_\mathrm{oss} = 59\,\mathrm{nC}$ obtained from the numerical integration of the C_oss curve in [207]. It is found that the constant part, corresponding to the Q_oss losses meets the expectations, whereas the current coefficient substantially deviates by a factor of 13. In total, the losses per device are found to be 2.6 times higher

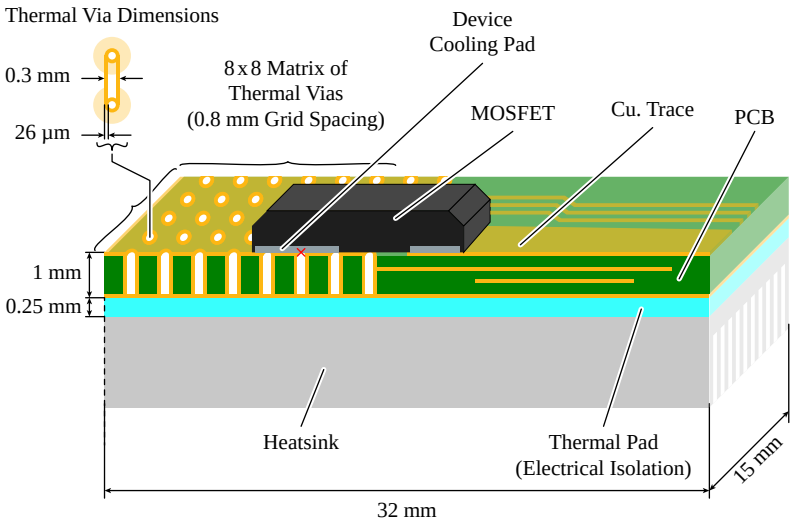


Fig. 3.7: Mechanical arrangement considered for the thermal simulation of the PCB area in the vicinity of a single MOSFET. In order to reduce the thermal resistance through the PCB a matrix of 64 thermal vias is installed in the PCB. The MOSFET is simulated as a heat source with a loss power of 15 W. Besides the PCB, the thermal path between MOSFET and heatsink incorporates a thermal pad for electrical isolation which exhibits a thermal conductivity of 6 W/(m K) [208]. Similarly, a thermal conductivity of 0.3 W/(m K) is estimated for the PCB [209, 210]. In case of the heatsink a constant temperature of 50 °C for the heatsink baseplate is assumed in the simulation.

than what was predicted in a first step for the worst case operating point with a DC output current of $I_{\mathrm{b,max}} = 61.5\,\mathrm{A}$, which results in $P_{\mathrm{dev}} = 12\,\mathrm{W}$ instead of $P_{\mathrm{dev}} = 4.6\,\mathrm{W}$ of total losses for a single device.

With the measured switching loss coefficients, the final bridge for the inverter can be designed, where rescaling the measured loss coefficients by N_{par} according to (3.26) also allows to determine the losses for different numbers of paralleled devices N_{par}. The limiting design aspect is the maximum losses per device that can be dissipated. Since all considered MOSFETs are bottom-cooled devices, cooling has to be accomplished through the PCB with thermal vias. The exact thermal resistance through the PCB is difficult to estimate as the heat distribution inside the PCB and the surrounding structures cannot be easily determined. For this reason, a thermal FEM simulation was conducted to determine the thermal resistance from MOSFET case to heatsink

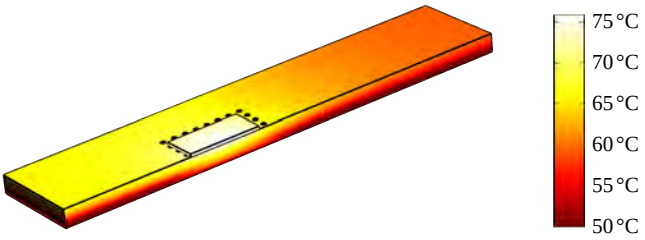


Fig. 3.8: Thermal simulation results of the PCB area around a single MOSFET. A temperature difference of 26 °C between heatsink baseplate and thermal hotspot on the MOSFET solder pad (marked in red in **Fig. 3.7**) is obtained, which, for the considered loss power of 15 W, results in an according thermal resistance of 1.73 K/W.

through the PCB for the arrangement with 64 thermal vias illustrated in **Fig. 3.7**. The according simulation results are illustrated in **Fig. 3.8**, where assuming a heatsink temperature of 50 °C and a loss power of 15 W, the simulation reveals a hotspot temperature of 76 °C, corresponding to a thermal resistance between MOSFET cooling pad and heatsink of $R_{\mathrm{th,PCB}} = 1.73\,\mathrm{K/W}$.

Based on the above result, an arrangement of five parallel *BSC160N15NS5* was finally selected, resulting in a maximum of $P_{\mathrm{dev}} = 14.6\,\mathrm{W}$ per device and $P_{\mathrm{tot}} = 78\,\mathrm{W}$ for each half-bridge. As a consequence, the thermal resistance $R_{\mathrm{th,hs}}$ of the required heatsink for two half-bridges follows from the maximum allowable junction temperature

$$T_{\mathrm{j}} = T_{\mathrm{amb}} + R_{\mathrm{th,hs}} 2P_{\mathrm{tot}} + \left(R_{\mathrm{th,PCB}} + R_{\mathrm{th,FET}}\right) P_{\mathrm{FET}} \tag{3.32}$$

of the devices, with $R_{\mathrm{th,FET}} = 1.3\,\mathrm{K/W}$ being the MOSFET internal thermal resistance from junction to case given by the datasheet. From (3.32) the required thermal resistance of the heatsink is determined to $R_{\mathrm{th,hs}} = 0.17\,\mathrm{K/W}$ in order to keep the junction temperature $T_{\mathrm{j}} < 125\,^{\circ}\mathrm{C}$ (25 °C below the absolute maximum rating) for an ambient temperature of $T_{\mathrm{amb}} = 55\,^{\circ}\mathrm{C}$.

3.1.2 Impact of Parasitic Capacitances

From **Fig. 3.1** it becomes clear that in general the voltage between a cell's reference potential (i.e., its DC-link midpoint) and ground changes with every switching action of any of the cells. Because in a physical realization there are inevitably parasitic stray capacitances between a cell's reference potential and ground, these voltage changes give rise to corresponding current flows to charge or discharge these parasitic capacitances, which could contribute

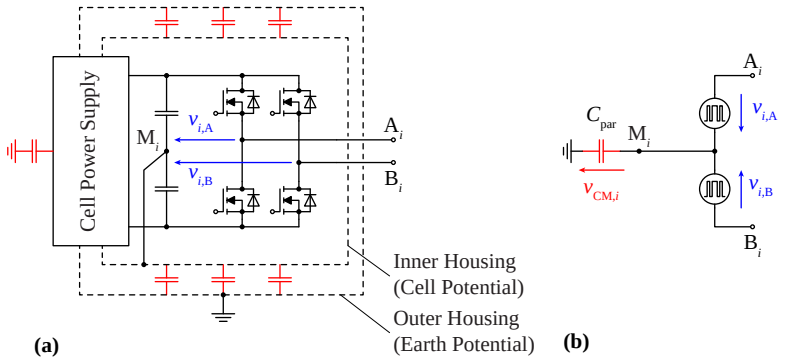


Fig. 3.9: (a) CM capacitances of a single cell. Each cell incorporates two mechanical enclosures: an inner housing connected to the cell's DC-link potential and an outer housing connected to ground. The parasitic CM capacitances originate from the capacitance between the two housings as well as the parasitic capacitances of the cell power supply and communication circuitry. **(b)** According equivalent circuit, where the parasitic capacitances are lumped together into a single equivalent capacitance C_{par}.

to switching losses as they flow during the switching transitions (being a consequence of the transitions' $\mathrm{d}v/\mathrm{d}t$), or lead to disturbances of the control and communication systems. Furthermore, these parasitic elements could form resonant networks with other parasitic elements (e.g., the parasitic inductances of the PCB power tracks) that lead to high-frequency oscillations within the system. In order to mitigate these effects, suitable countermeasures are required to suppress these parasitic current paths.

The origin of the parasitic capacitances is illustrated in more detail in **Fig. 3.9a** for a single cell. In the physical realization of the converter each cell contains two different housings: an inner housing which is connected to the cell's DC-link midpoint as well as an outer housing on earth potential. This structure is chosen to provide shielding for the cell interior components by preventing the capacitive leakage currents from flowing over undefined paths inside the cell (e.g., sensitive signaling components, analog measurement circuits, etc.) and guaranteeing predefined and identical conditions for all cells. Additional parasitic paths originate from the parasitic capacitance of the isolated power supply (i.e., the parasitic capacitance between primary-side

and secondary-side windings of the according transformer) as well as the parasitic capacitance of the digital isolators used to isolate the communication signals between cell and outer controller. These parasitic capacitances can be summarized to a single lumped capacitance C_{par}, where an estimation of $C_{\text{par}} = 500\,\text{pF}$ was considered for the parasitic capacitance of the mains-side transformer and the cell housing (cf. **Section 3.3**). The resulting equivalent circuit can then be simplified to the schematic given in **Fig. 3.9b**, where also the half-bridges have been replaced by their according ideal voltage sources $v_{i,\text{A}}$ and $v_{i,\text{B}}$ for cell number i. The cell's reference potential against earth is then given as the voltage $v_{\text{CM},i}$ across C_{par}.

From the above model for a single cell, the resulting equivalent circuit for the entire stack can be derived, which is presented in **Fig. 3.10a**. From there it can be recognized that the CM capacitances represent a capacitive load on the switch node of each half-bridge that has to be charged and discharged every time a cell switches. This is shown in **Fig. 3.10b** on the example of a switching action initiated by half-bridge 5A that has to charge the parasitic capacitances via the highlighted capacitive current path in the stack. This is considered undesirable since the capacitive loading could negatively influence the switching behavior of the inverter bridges by increasing the switching losses. The impact of the parasitic capacitances has already been described in literature in [156, 211], where suitable countermeasures to mitigate these effects are suggested by installing CMCs at the inverter output terminals as illustrated in **Fig. 3.11**. Consequently, the design approach described in [156] is used to dimension suitable CM filter elements, which consist of a CMC $L_{\text{CM,c}}$ with a parallel connected damping resistor $R_{\text{CM,c}}$ as illustrated in **Fig. 3.11** for a single cell and in **Fig. 3.12** for the entire cell stack. It has to be noted that in [156], solid grounding of one of the output terminals is assumed (cf. **Fig. 3.12**). This is considered a worst case approximation for the case at hand since in case of the UH-PBW, both stack outputs N and P are actually connected to an output filter, which contains a separate CMC itself (see **Section 3.2.2**). The CMC of the output filter would introduce an additional impedance in the path that limits the CM currents flowing via the output terminals, which is neglected for the design of the cell-level CM filter elements $L_{\text{CM,c}}$, $R_{\text{CM,c}}$. The design of the output CM filter (of which the neglected CMC is part of) is not covered here but discussed separately in **Section 3.2.2**. Following the cited design procedure from [156], $L_{\text{CM,c}} = 125\,\mu\text{H}$ and $R_{\text{CM,c}} = 250\,\Omega$ are determined for the value of the parasitic capacitance C_{par} stated above.

In order to verify that the stacking of the cells (with the designed CMCs) indeed does not deteriorate the switching behavior of the cells or infer with the

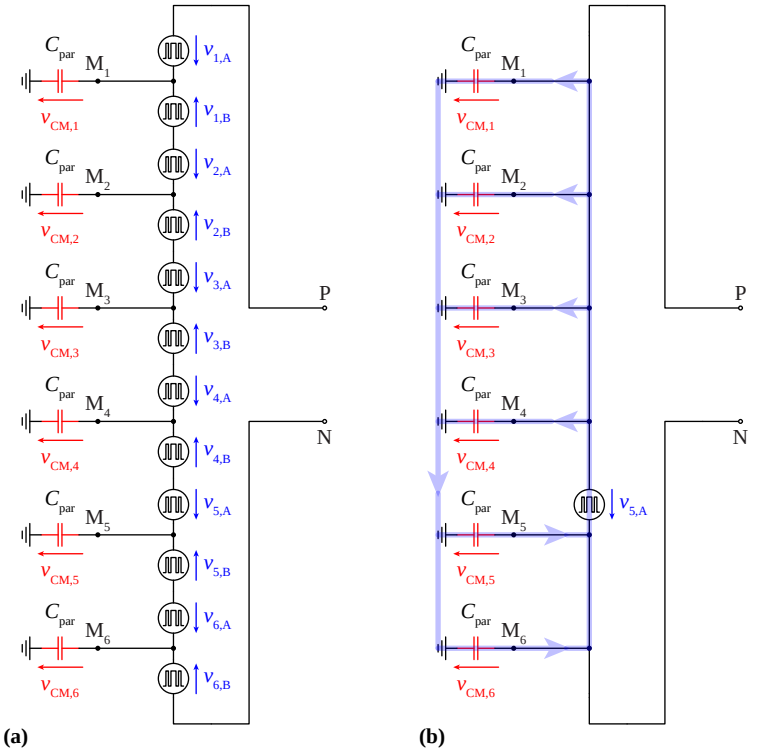


Fig. 3.10: **(a)** CM equivalent circuit for the entire cell stack with the output filter neglected. The parasitic capacitances represent capacitive loads for the inverter half-bridges illustrated as voltage sources. **(b)** Resulting CM current paths in case of a switching transition of half-bridge 5A.

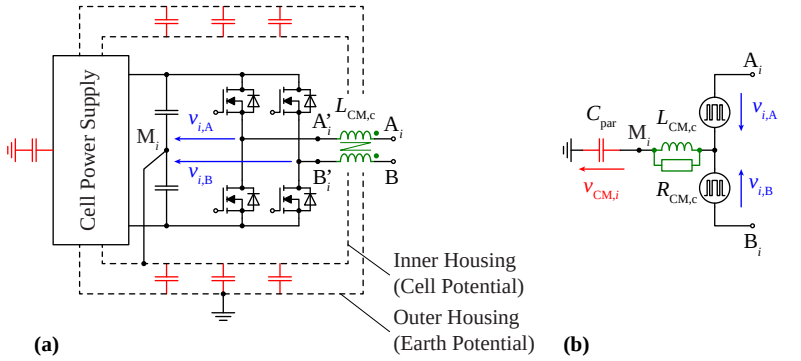


Fig. 3.11: (a) In order to suppress the CM currents resulting from the parasitic CM capacitances, the common-mode choke (CMC) $L_{\mathrm{CM,c}}$ is introduced at the cell's inverter output. **(b)** According simplified equivalent circuit including a damping resistor $R_{\mathrm{CM,c}}$ to avoid resonance phenomena between C_{par} and $L_{\mathrm{CM,c}}$.

communication system, measurements were carried out, where an increasing number of cells were stacked with only the output filter (i.e., no external load) connected to the cell stack. The power consumption of one cell was measured to verify whether the losses in the semiconductors increase with higher number of stacked cells. In addition, the output voltage of one of the full-bridges was monitored and the switching behavior for different numbers of cells was compared. **Fig. 3.13** illustrates the measurement setup. The filter components of the output filter are given by the preliminary filter board component values stated in **Section 3.3**, however, an additional 90 µH inductor was placed between stack terminal P and and the filter due to the reduced switching frequency resulting from the incomplete number of cells. The cells were operated with a time-independent and fixed modulation index of 75 %, resulting in an average output voltage of 75 V per cell. The total output voltage at the filter output therefore depends on the number of cells used in the experiment. Furthermore, it has to be noted that in order to guarantee access to the several measuring points with the measuring probes, parts of the housings had to be removed during the measurements, which alters the parasitic capacitances of the respective cells. This resulted in the following four scenarios:

- One cell: the stack was operated only with cell 1 (partial housing) as a reference case.

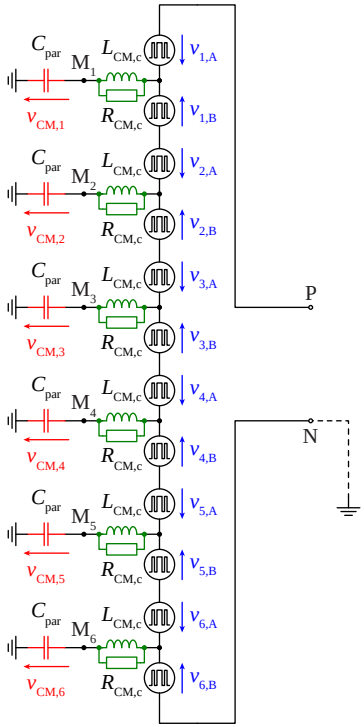


Fig. 3.12: Simplified CM equivalent circuit for the entire cell stack if the CMCs in the cell's outputs are included. For the dimensioning of the CMCs, the approach described in [156] is employed, where a solid grounding of one of the phase stack terminals is assumed (indicated by the dashed grounding of terminal N). Note that this is a worst case approximation for the case at hand.

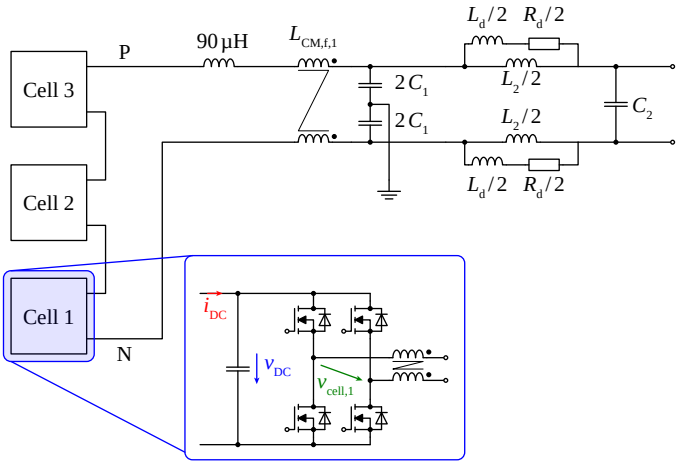


Fig. 3.13: Measurement setup used to characterize the impact of stacking cells (and hence increasing the parasitic CM capacitances to ground) on the switching behavior. The DC-link voltage v_{DC} and current i_{DC} as well as the bridge output voltage $v_{cell,1}$ of cell 1 are measured and compared for different numbers of stacked cells.

- Two cells (I): the stack was operated with cell 1 (partial housing) and cell 2 (partial housing).
- Two cells (II): the stack was operated with cell 1 (partial housing) and 3 (complete housing).
- Three cells: operation with cell 1 and 2 (partial housing) as well as cell 3 (complete housing).

Measurements with a higher number of cells were not carried out since it is expected that further stacking of additional cells will not change the investigated behavior significantly, as the relative increase in CM capacitance per added cell becomes smaller for higher number of cells.

In all four scenarios, the DC-link voltage v_{DC} as well as the DC-link input current i_{DC} of cell 1 were measured with an oscilloscope and the according power consumption was calculated. This is not expected to provide accurate absolute values for the bridge's power consumption but should still allow to detect differences in power consumption between operation with different numbers of cells. The power measurements did not reveal any deviation in power consumption of the monitored bridge that could indicate an increase in switching losses between the different scenarios. Furthermore, the bridge voltage $v_{\mathrm{cell},1}$ of cell 1 was measured with a *TIVHo8 IsoVu* Probe from *Tektronix* [212] that enables isolated voltage measurements with sufficiently high bandwidth and very high CM rejection to be able to evaluate and compare the switching transients for different cases. The results of the measurements are presented in **Fig. 3.14** for both (rising and falling) switching transitions of $v_{\mathrm{cell},1}$. It can be recognized that there is no significant deviation in the switching behavior between the different cases (e.g., no changes in the transition's $\mathrm{d}v/\mathrm{d}t$), which would indicate a problematic increase in switch node capacitance. In addition, the shown experiments also allowed to verify proper functioning of the digital communication system between the cells and the external main control system, thereby proving that no relevant CM currents are flowing over the signal paths that could disturb the communication.

3.1.3 Interlock Delay Distortion

Interlock delay distortion is a well-known phenomenon in switched-mode power converters [213–217], which originates from the non-zero rise and

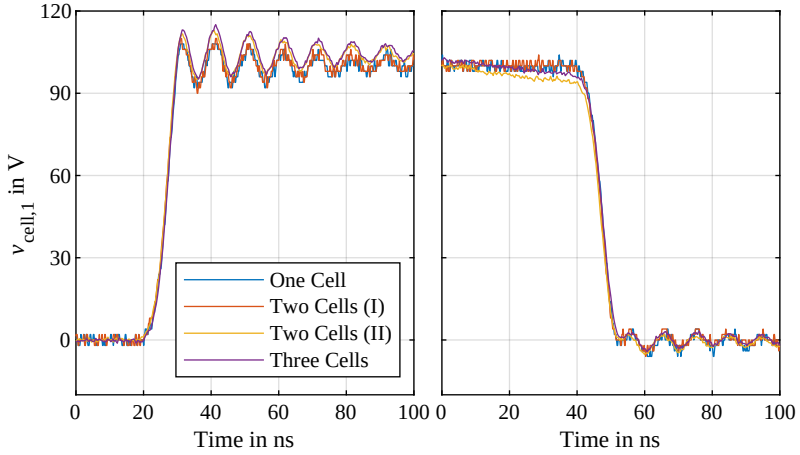


Fig. 3.14: Rising and falling switching transients of cell 1 for different numbers of stacked cells.

fall times of the semiconductors and the interlock delay time[2] introduced between turn-off and turn-on of the two switches of a half-bridge switching transient. This time interval, during which both semiconductors of the bridge are turned off, is required to prevent the two switches from conducting simultaneously, which would result in a short circuit of the DC-link (shoot-through). During the interlock interval, referred to as t_{intl}, the load current of the bridge commutates into the body diode or the parasitic capacitances of the MOSFETs and therefore the resulting output voltage of the bridge depends on the sign and the magnitude of the load current as well as the direction (rising vs. falling) of the transition. As a consequence, the interlock time causes nonlinear current-dependent distortions of the output voltage since the voltage-time area applied to the filter is modulated by the current.

This effect is illustrated in more detail on the example of a rising and a falling transition in **Fig. 3.15** and **Fig. 3.16** (assuming linear capacitances of the MOSFETs), respectively, where the current paths, gate signals and switch node voltage for a regular half-bridge during each transition are shown. For both cases it is assumed that during the transition the bridge output current i_{sw} stays constant, which is justified by the filter inductor connected to the bridge

[2] The interlock delay time is often referred to as *dead time* in literature. However, this term is not used in this thesis to avoid confusion with the transport delay times in dynamic systems that are often referred to by the same term.

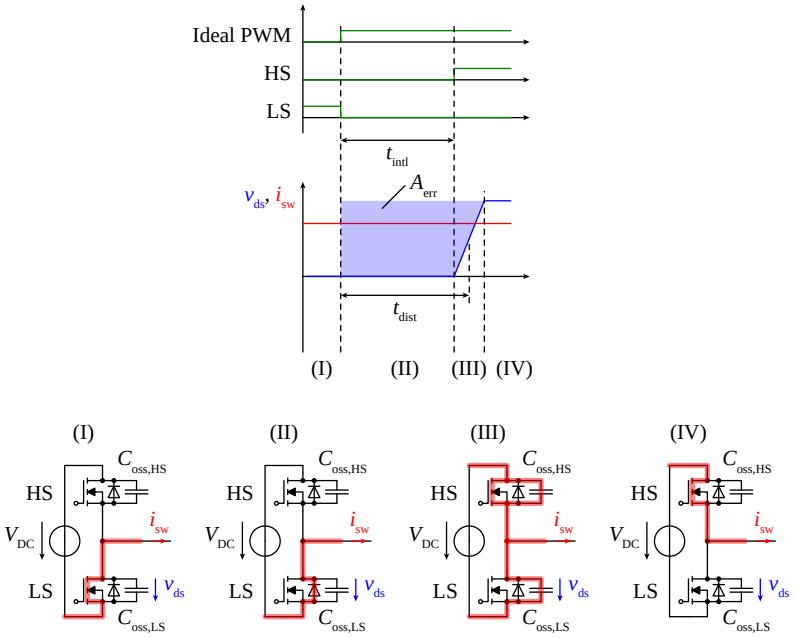


Fig. 3.15: Idealized waveforms and current paths during commutation for a rising switching transition of a half-bridge. For the considered current direction ($i_{sw} > 0$), a hard-switching transition results, i.e., during the interlock interval (II) the output current commutates into the body diode of the LS switch and the output voltage of the bridge does not change until the interlock delay time t_{intl} has expired. Afterwards, the HS switch is turned on, resulting in a rapid charge and discharge of the parasitic capacitances implying a fast and almost current independent $\mathrm{d}v/\mathrm{d}t$ of the transition (III) until the new switching stage of the half-bridge is reached (IV).

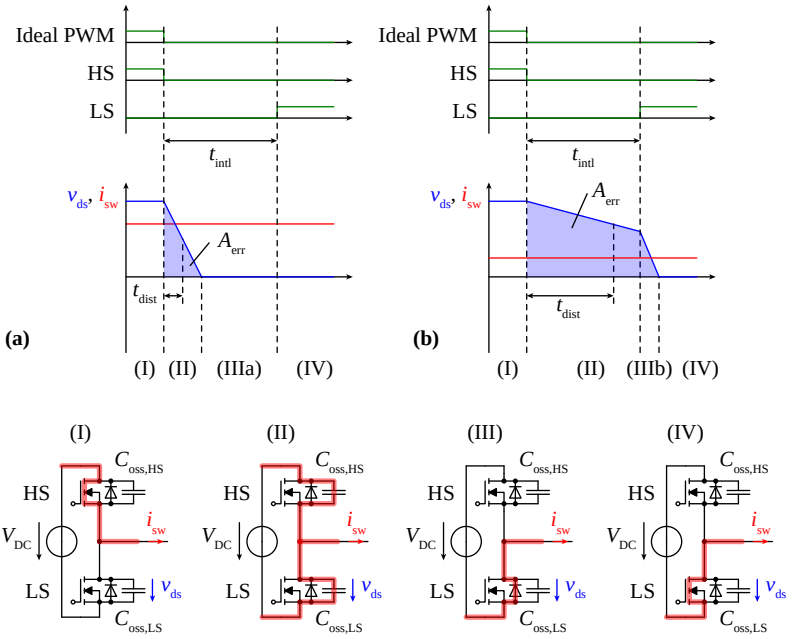


Fig. 3.16: Idealized waveforms and current paths during commutation for a falling switching transition of a half-bridge for **(a)** soft-switching and **(b)** partial hard-switching. Contrary to the hard-switching case before, the bridge current cannot flow over the body diode of the HS switch once the HS switch is turned off due to the considered current direction ($i_{sw} > 0$) and is forced to commutate into the parasitic capacitances of the switches instead (II). The switch node voltage starts to change immediately after the HS switch starts to block, with the dv/dt of the transition determined by the load current magnitude and the parasitic capacitances. Depending on the magnitude of the load current and the duration of t_{intl}, either soft-switching or partial hard-switching is achieved. In case of soft-switching, the dv/dt is sufficiently fast to complete the switching transition before the interlock interval expires. The load current then commutates into the LS body diode for the reminder of the interlock interval (IIIa) until the LS switch is turned and the bridge reaches its new state (IV). In case of partial hard-switching, the LS switch is turned on before the switch node potential has changed to zero, resulting in a hard commutation with reduced charges stored in the parasitic capacitances (IIIb) until the final half-bridge state is reached (IV).

output and the short transition time compared to the switching frequency. Furthermore, only positive load current is considered since in case of negative load currents the same effects are observed if the transition directions are exchanged (falling vs. rising transition).

In **Fig. 3.15** a rising transition with positive output current ($i_{\mathrm{sw}} > 0$) is shown, starting with the turn-off of the LS switch, which leads to the load current commutating into the according LS body diode. During the interlock interval the bridge maintains this state and the output voltage is negative given by the forward voltage drop of the diode. Once the complete interlock time has expired, the HS switch is turned on, which leads to discharging of $C_{\mathrm{oss,HS}}$ and charging of $C_{\mathrm{oss,LS}}$ and changes the switch node potential to the positive DC-link potential. The $\mathrm{d}v/\mathrm{d}t$ of this transition has only a weak dependence on the load current and is mostly determined by the semiconductors, gate drives and parasitic elements in the commutation path. This transition is also referred to as hard-switched transition. In order to quantize the deviation between ideal and real PWM transition, the error voltage-time integral A_{err} (highlighted in blue in **Fig. 3.15** and **Fig. 3.16**) is introduced, which in case of hard-switching can be approximated by $A_{\mathrm{err}} \approx V_{\mathrm{DC}}\, t_{\mathrm{intl}}$.

Similarly, **Fig. 3.16** illustrates a falling transition, again for positive output current ($i_{\mathrm{sw}} > 0$), initiated by the turn-off of the HS switch. Contrary to the hard-switched transition described above, the according HS body diode does not offer a suitable path due to the sign of the current and therefore, the current commutates into the parasitic capacitances of the switches and starts charging and discharging the capacitances $C_{\mathrm{oss,HS}}$ and $C_{\mathrm{oss,LS}}$, respectively. As a consequence, the output voltage starts to change already during the interlock interval. The $\mathrm{d}v/\mathrm{d}t$ of the transition is determined by the load current and the parasitic capacitances, with higher currents resulting in faster transition speeds, although the resulting $\mathrm{d}v/\mathrm{d}t$ values are typically slower compared to the hard-switching case. Once the output voltage has reached the forward voltage of the LS body diode, the body diode takes over the current, thereby clamping the output potential to the negative DC-link until the interlock time has expired and the LS switch is turned on. This type of transition, where the turn-on of the switch occurs at zero voltage, is referred to as soft-switching (zero-voltage switching, ZVS). Since the bridge voltage already starts to change during the interlock interval, the resulting error voltage-time area A_{err} for soft-switching is smaller than what is obtained for hard-switching and significantly depends on the load current. Furthermore, a third scenario has to be considered for low current magnitudes in case of soft-switching, which is also shown in **Fig. 3.16** and referred to as partial hard-switching. In

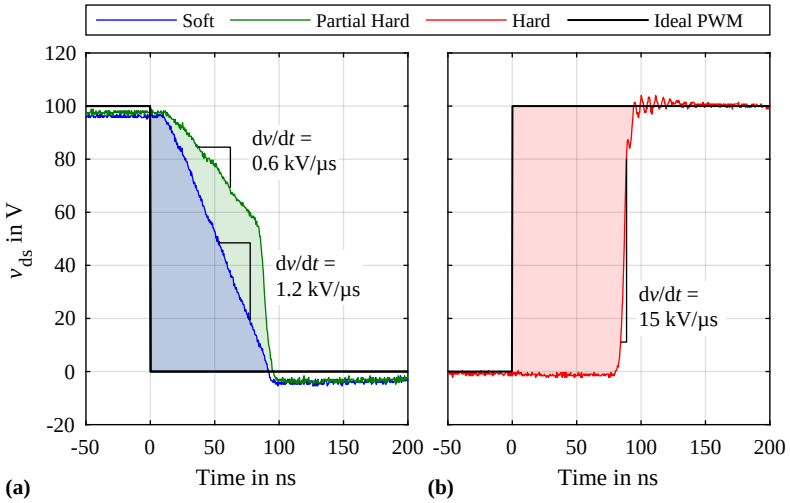


Fig. 3.17: Measurements results for the half-bridge output voltage v_{ds} for the three different types of switching transitions. A positive bridge output current sign ($i_{sw} > 0$) was used for all cases. For a falling transition this results in soft commutation (blue curve) for $i_{sw} = 8.5\,A$ and partial hard commutation (green curve) for $i_{sw} = 4\,A$, presented in **(a)**. Consequently, in **(b)** a rising transition for $i_{sw} = 7.1\,A$ is given, resulting in a hard commutation. In case of the falling transition the current dependency of the dv/dt during the interlock interval of the transition is clearly recognizable. Furthermore, a significantly higher dv/dt compared to soft-switching is observed in case of hard commutation.

this case the interlock interval is too short for the current to complete the charging process, resulting in a partial change of potential during the interlock interval and a hard commutation afterwards. Exemplary measurements of these transitions are presented in **Fig. 3.17** for the final version of the inverter bridge designed in **Section 3.1.1**.

In order to characterize the deviation of the bridge output voltage from the ideal PWM signal for each transition, a distortion delay time is defined based on the error voltage-time integral A_{err} according to

$$t_{dist} = \frac{A_{err}(i_{sw})}{V_{DC}}, \tag{3.33}$$

which represents the (current dependent) delay time between the ideal PWM transition and an equivalent rectangular transition that introduces the same

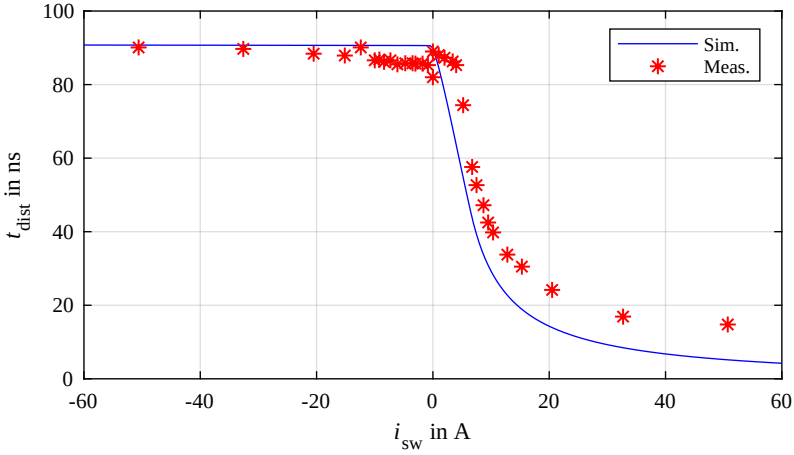


Fig. 3.18: Measured equivalent delay time (distortion delay time) for a falling switching transition, depending on the bridge-leg output current. The equivalent delay time is almost current independent for negative bridge output currents which result in hard-switching. For positive output current, the current dependency of the distortion delay time is clearly visible, with higher currents resulting in faster transitions and according shorter delay times. For a rising switching transition of the bridge-leg, the same curve but with reversed x-axis results. The measurements are compared to a circuit simulation with the data of the nonlinear output capacitance of the MOSFETs taken from the datasheet.

error voltage-time area as the real transition. This distortion delay time t_{dist} was measured for the final version of the inverter bridge designed in **Section 3.1.1** with the results presented in **Fig. 3.18** for a falling transition, which implies hard-switching for negative and soft-switching for positive output currents. Furthermore, the measurements are compared to the results of a circuit simulation including the nonlinear parasitic capacitances from the MOSFET datasheet with an additional linear switch node capacitance of 1 nF to account for the parasitics of the PCB layout. It can be recognized that for negative currents (hard-switching) the delay time is almost independent of the switched current and identical to the interlock interval of $t_{\text{intl}} = 90$ ns used to operate the bridge. For soft-switching the distortion delay heavily reduces with increasing load current as the charging process of the parasitic capacitances becomes faster at higher currents.

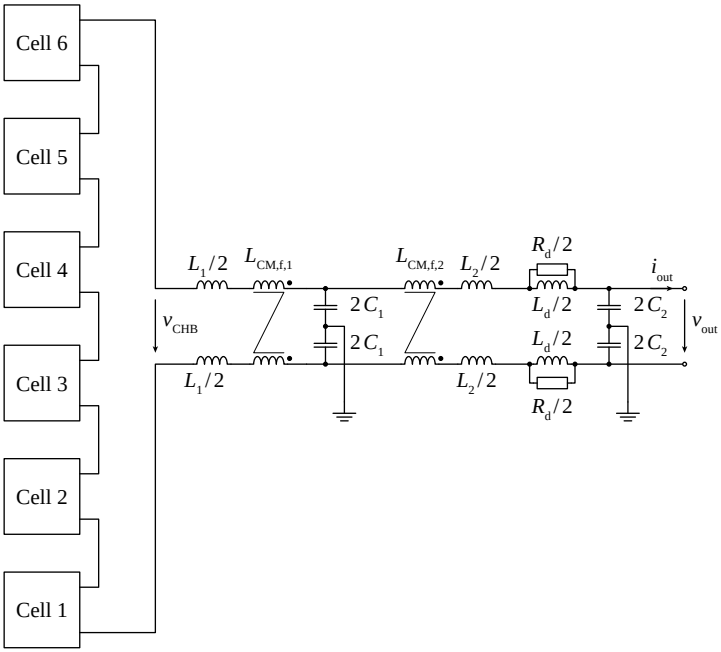


Fig. 3.19: Output filter structure for the UH-PBW system. A two-stage LC filter is used for both, the DM filter as well as the CM filter, where the filter capacitors C_1 and C_2 are used for both parts.

The data from **Fig. 3.18** is used to implement a compensation scheme that largely eliminates the current dependency of the bridge delay time by introducing an additional compensation delay time. Details about this compensation scheme are provided in **Section 4.5.2**.

3.2 Output Filter Design

Apart from the switching stage, a key element of the UH-PBW amplifier is the output filter which is required to filter out the switching frequency harmonics from the stack output voltage. Generally, such a filter incorporates a DM and a CM filter stage, where typically single- or multi-stage LC filter structures are employed for both parts. Since in **Section 3.1.1** it was already

demonstrated that a single-stage filter is not able to guarantee the required attenuation while still being able to fulfill the reactive power limitations, a two-stage filter structure was selected for DM filtering and the same filter structure is also chosen for the CM filter part. This results in the filter structure shown in **Fig. 3.19**, where the filter capacitors C_1 and C_2 are used for both, the DM as well as the CM filter stage. The goal of the filter design is then to determine suitable filter component values for the filter capacitors C_1 and C_2, the DM filter inductors L_1 and L_2 and the CM inductors $L_{\mathrm{CM,f},1}$ and $L_{\mathrm{CM,f},2}$. Additionally, a damping network L_d, R_d is required to suppress oscillations at the higher of the two resonance frequencies which the two-stage DM filter exhibits. In case of the first filter stage, active damping [218, 219] by the current controller can be achieved, i.e., no damping network is required.

Since the DM filter has a significant influence on the dynamics of the converter, the main goal of the filter design is to find the smallest possible filter elements which just guarantee the required attenuation as this reduces the reactive power consumption and enables fast dynamics of the output voltage control loop. However, an additional criterion limiting the maximum allowed output voltage dip in case of a load step is introduced in this section, which imposes additional restriction on the design of the DM filter elements. For this reason, the maximum achievable output frequency of the system resulting from the filter design described below is lower than the design frequency of $f_{\mathrm{out,max}} = 100\,\mathrm{kHz}$ initially stated in **Section 3.1.1**.

The design of the output filter is split into two sections: in **Section 3.2.1** the design of the DM filter stage is presented, where an adapted procedure based on the design-space optimization described in [96] is applied in order to maximize the achievable bandwidth of the converter. In addition, the design of the CM filter is given in **Section 3.2.2**. Since the CM filter stage has no influence on the achievable dynamics of the system, only a single attenuation criterion is applied for the design of the CM filter, however, a suitable model to determine the CM voltage on the converter output has to be derived first.

3.2.1 Differential-Mode Filter

Fig. 3.20 illustrates the DM filter structure, which originates from the schematic presented in **Fig. 3.19** by removing the CMCs and combining the series connection of the filter capacitors into a single DM capacitance, thereby resulting in a two-stage LC filter with four reactive filter elements L_1, L_2, C_1 and C_2 that have to be determined. The damping network L_d and R_d is neglected during the filter design, except for the voltage dip criterion

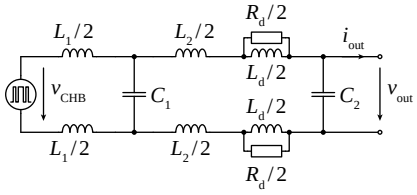


Fig. 3.20: DM filter structure. The filter inductors L_1 and L_2 are symmetrically distributed between both converter terminals such that identical conditions for both output terminals result.

introduced below, and subsequently dimensioned on the basis of the obtained filter components. For this reason, a four dimensional parameter space (L_1, L_2, C_1, C_2) results from which the optimal values of the filter components have to be determined.

For the design of the DM filter, the approach described in [96] is used with some modifications, similarly to the filter design presented in [220]. This approach is based on a filter optimization within a two dimensional L_1-C_1 plane where in a first step fixed component ratios

$$k = \frac{L_2}{L_1}, \quad m = \frac{C_2}{C_1} \tag{3.34}$$

are assumed that define the second stage elements. Within this plane, several limiting curves originating from the required output specifications of the system can be illustrated as boundaries that restrict the valid L_1-C_1 combinations to a limited area. An example of such a so-called *design space* is presented in **Fig. 3.21**, with the range of valid filter components highlighted in red. From this region, the optimal design is then identified, where in [96] an efficiency vs. power density Pareto optimization was carried out. In this work however, the filter enabling the highest possible large-signal output frequency without exceeding the reactive power demand limits is selected as optimum design rather than focusing on filter volume or losses. The component ratios k and m are then iterated through a certain range in a second step to identify the overall optimal design.

Tab. 3.5 summarizes the filter requirements, with the resulting design limitations and their implication on the design space listed below.

- **Output voltage quality:** As already stated in **Section 3.1.1** a limit for the total RMS noise voltage at the output of $V_{\text{noise,max}} = 10\,\text{mV}$

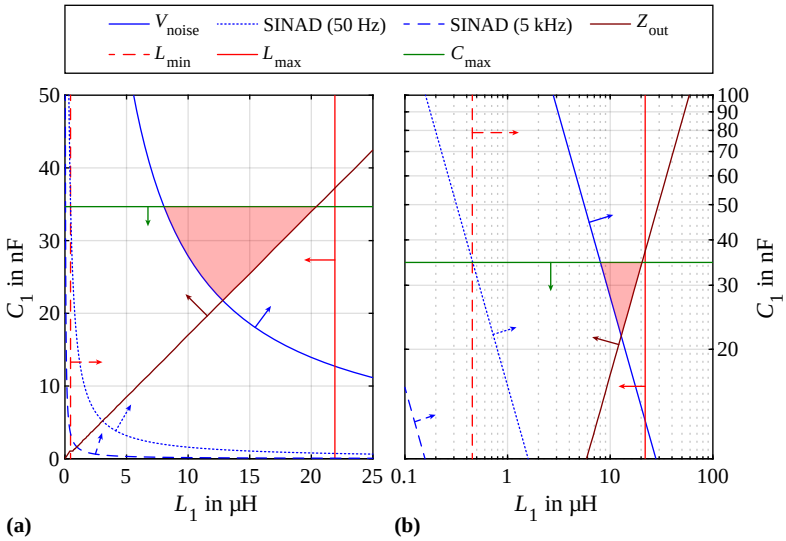


Fig. 3.21: Exemplary design space with **(a)** linear axes and **(b)** logarithmic axes for $k = 0.1$, $m = 5$. The arrows indicate on which side of the respective boundary curve a valid design has to be located. For the limitations of the maximum inductive voltage drop and the maximum capacitive filter current, which result in upper limits for L_1 and C_1, an exemplary maximum output frequency of $f_{out,max} = 50\,\text{kHz}$ was considered. Valid designs fulfilling all constraints are located in the area highlighted in red.

Design Constraint	Limit	Conditions
Total RMS switch noise	$< 10\,\text{mV}$	No-load, $\hat{v}_{\text{out}} = 325\,\text{V}$
SINAD ($f_{\text{out}} = 50\,\text{Hz}$)	$> 54\,\text{dB}$	No-load, $\hat{v}_{\text{out}} = 325\,\text{V}$
SINAD ($f_{\text{out}} = 5\,\text{kHz}$)	$> 34\,\text{dB}$	No-load, $\hat{v}_{\text{out}} = 325\,\text{V}$
Transient output voltage dip	$\Delta v_{\text{out}} < 50\,\text{V}$	Step amplitude $\Delta i_{\text{out}} = 15.4\,\text{A}$
Inductor current ripple	$\Delta i_{\text{pp,L1}} < 25\,\% \hat{i}_{\text{out,nom}} = 15.4\,\text{A}$	
Reactive inductor voltage drop	$\hat{v}_{\text{L,max}} < \sqrt{\hat{v}^2_{\text{CHB,max}} - \hat{v}^2_{\text{out,max}}} = 323\,\text{V}$	$\hat{i}_{\text{out}} = 42.6\,\text{A}$ ($P_{\text{nom}} = 10\,\text{kW}$ at $\hat{v}_{\text{out}} = 470\,\text{V}$)
Reactive capacitor current	$\hat{i}_{\text{C,max}} < \frac{1}{2}\hat{i}_{\text{out,nom}} = 30.8\,\text{A}$	$\hat{v}_{\text{out}} = 470\,\text{V}$

Tab. 3.5: Summary of the performance specifications used to design the DM filter.

is requested. Since the switching frequency and the number of cells are already determined, (3.18) can be used directly to determine the minimum required L_1C_1 product:

$$L_1C_1 > \sqrt{\frac{V_{\text{DC,tot}}}{N_{\text{cell}} V_{\text{noise,max}} \omega^4_{\text{eff}}} (a_1 a_2)^2} \tag{3.35}$$

$$= \sqrt{\frac{V_{\text{DC,tot}}}{N_{\text{cell}} V_{\text{noise,max}} \omega^4_{\text{eff}}} \frac{1}{km}}. \tag{3.36}$$

The factors a_1 and a_2 in the above expression are the frequency factors that relate the corner frequencies of the two-stage filter to its characteristic frequency $\omega_0 = 1/(L_1C_1)$, which are directly determined from the component ratios k and m according to (3.6). The resulting boundary curve represents a hyperbola illustrated in blue in the exemplary design space in **Fig. 3.21**, where valid designs have to be located on the upper right side of the curve, i.e., towards higher L_1 and C_1 values.

Similarly, the two signal-to-noise-and-distortion (SINAD) ratio criteria for $f_{\text{out}} = 50\,\text{Hz}$ and $f_{\text{out}} = 5\,\text{kHz}$ imply a minimum filter attenuation which is determined numerically by using a binary search algorithm to

find a suitable L_1C_1 product such that the quantity

$$\text{SINAD} = \frac{V_{\text{out,RMS}}}{\sqrt{V_{\text{out,RMS}}^2 - V_{\text{out,base}}^2}} \tag{3.37}$$

fulfills the requested limitations, with $V_{\text{out,RMS}}$ and $V_{\text{out,base}}$ representing the total RMS value and the fundamental component's RMS value of the filtered output voltage, respectively. The respective quantities are calculated from a Fourier transform of a single base frequency period of the ideal unfiltered CHB waveform, where each of the harmonics is attenuated according to the asymptotic approximation of the filter transfer function (cf. **Fig. 3.3**), assuming a −40 dB/dec attenuation per corner frequency given by (3.5) and (3.6) to approximate the transfer function of the output filter. Again, the according limitations represent hyperbolas illustrated in the L_1C_1 plane as blue dashed and dotted curves, respectively. However, these limits are less strict than the RMS noise voltage criterion mentioned before and therefore have no influence on the resulting design.

- **Output impedance:** In order to characterize the output impedance of the system, a load current step with amplitude $\Delta i_{\text{out}} = 15.4\,\text{A}$ (25 % of the rated peak current $\hat{i}_{\text{out,nom}} = 61.5\,\text{A}$) is considered at the converter output, which would result in an output voltage dip Δv_{out} that has to be compensated by the controller. An accurate description of the resulting voltage dip would require a complete dynamic model of the converter including the control system as it is carried out in **Chapter 4**. This would also require the values of the according control gains, which, however, are determined based on the values of the filter elements. For this reason and also to reduce the computational effort during the filter dimensioning, a simplified approach is utilized to approximate the occurring transient voltage dip, where the controller's reaction is idealized/approximated by a step voltage source that applies a voltage of $\Delta v_{\text{CHB}} = 300\,\text{V}$ (half of the DC-link voltage) to the filter input at the same time instance where the load current step occurs, i.e., neglecting the system delay times. The according circuit model is illustrated in **Fig. 3.22** together with the according voltage waveforms for an exemplary case, where (contrary to the analysis of the remaining design space constraints) the damping element L_d, R_d is included in the determination of the voltage dip since otherwise the resulting oscillations of the undamped filter would introduce massive deviations.

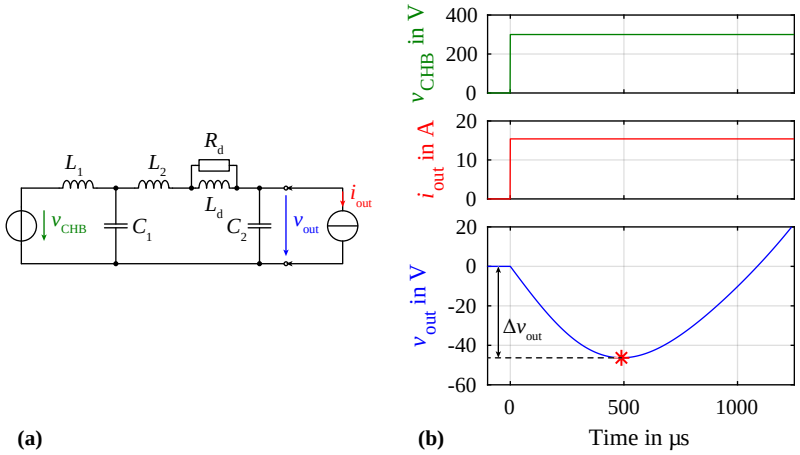


Fig. 3.22: Modeling of the transient output voltage dip in case of a load step. **(a)** Schematic diagram of the simulation model. **(b)** Exemplary output voltage waveform for $L_1 = 9\,\mu\text{H}$, $C_1 = 50\,\text{nF}$, $k = 0.1$, $m = 2$. Although the output voltage heavily overshoots in this model after recovering from the load step as the controller's reaction is simplified by a step voltage source, i.e., omitting the further compensatory action of the control system, the model allows the description of the resulting voltage dip Δv_{out}. Contrary to the remaining design space constraints, the damping element L_d, R_d is included in the calculation of the output impedance boundary. The according parameters are calculated according to (3.47).

The occurring maximum voltage dip is then calculated from the step response, where it has to be considered that this model can only be used for an approximation of the first time interval until the voltage starts to recover. Afterwards, the assumption of a constant filter input voltage is not valid anymore since the controller would continue to react and stabilize the output voltage, whereas in the simplified model a severe overshoot would result and the filter would start to oscillate since the subsequent reaction of the controller is omitted.

The stated approach allows to numerically determine the minimum required capacitance C_1 for a given value of the filter inductance L_1 such that the voltage dip Δv_{out} does not exceed the defined limit of 50 V. Larger filter capacitances lead to a reduction of the transient voltage dip as they can provide more charge to the converter output. The respective boundary in the design space is illustrated as a brown

line in **Fig. 3.21**, with valid filter parameters located above this line (i.e., towards higher capacitance values).

- **Inductor current ripple:** The peak-to-peak current ripple $\Delta i_{\mathrm{pp,L1}}$ in the first stage filter inductor L_1 is limited to $25\,\%\,\hat{i}_{\mathrm{out,nom}} = 15.4\,\mathrm{A}$ in order to avoid excessive peak currents in the inverter stage and increased high-frequency losses in the filter inductor. The according expression is given as [57]

$$\Delta i_{\mathrm{pp,L1}} = \frac{V_{\mathrm{DC,tot}}}{8 L_1 f_{\mathrm{s}} N_{\mathrm{cell}}^2}. \tag{3.38}$$

  Rearranging directly results in a minimum inductance value of

$$L_1 > \frac{V_{\mathrm{DC,tot}}}{8 f_{\mathrm{s}} N_{\mathrm{cell}}^2 \Delta i_{\mathrm{pp,L1}}} = 454\,\mathrm{nH} \tag{3.39}$$

  indicated by the red dashed boundary in **Fig. 3.21**.

- **Inductive voltage drop:** The maximum large-signal output frequency of the converter is mainly limited by the reactive power demand of the filter elements, i.e., the voltage drop over the filter inductor and the reactive current consumption of the filter capacitors. For this reason, two according constraints are introduced, where the first criterion refers to the maximum voltage drop over the filter inductors that is limited by the total DC-link voltage of the system. Assuming unity power factor on the converter output as a reference case, the inductive voltage drop is estimated to

$$\hat{v}_{\mathrm{L,max}} = \sqrt{\hat{v}_{\mathrm{CHB,max}}^2 - \hat{v}_{\mathrm{out,max}}^2} = 2\pi f_{\mathrm{out,max}} L_1 (1 + k)\, \hat{i}_{\mathrm{out,vmax}}, \tag{3.40}$$

  where the reactive current in the filter capacitors is neglected such that the phasor diagram from **Fig. 3.23** can be applied. The quantities $\hat{v}_{\mathrm{CHB,max}}$, $\hat{v}_{\mathrm{out,max}}$, $\hat{i}_{\mathrm{out,vmax}}$ and $f_{\mathrm{out,max}}$ refer to the maximum filter input voltage, the maximum load voltage and the according load current at nominal power as well as the maximum large-signal output frequency, respectively, where values of $\hat{v}_{\mathrm{CHB,max}} = 95\,\% V_{\mathrm{DC,tot}} = 570\,\mathrm{V}$ (providing a 5 % margin), $\hat{v}_{\mathrm{out,max}} = 470\,\mathrm{V}$, $\hat{i}_{\mathrm{out,vmax}} = 42.6\,\mathrm{A}$ apply; note that the considered output current is lower than the nominal output current $\hat{i}_{\mathrm{iout,nom}}$) due to operation at the maximum output voltage. From the

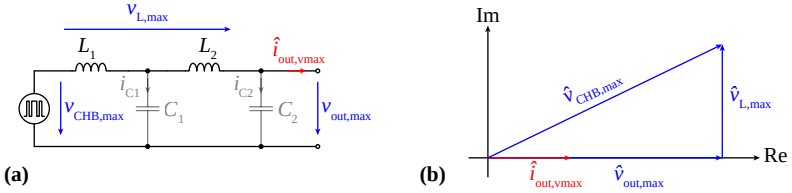


Fig. 3.23: Phasor diagram used to determine the maximum voltage drop over the filter inductances. The filter capacitor currents i_{C_1} and i_{C_2} are neglected, furthermore, a unity power factor load at the output is assumed as reference case.

above expression $\hat{v}_{\mathrm{L,max}} = 323\,\mathrm{V}$ is obtained. Rearranging results in an upper limit for the filter inductor value

$$L_1 < \frac{\sqrt{\hat{v}^2_{\mathrm{CHB,max}} - \hat{v}^2_{\mathrm{out,max}}}}{2\pi f_{\mathrm{out,max}}\,(1+k)\,\hat{i}_{\mathrm{out,vmax}}} = \frac{\hat{v}_{\mathrm{L,max}}}{2\pi f_{\mathrm{out,max}}\,(1+k)\,\hat{i}_{\mathrm{out,vmax}}}, \quad (3.41)$$

indicated by the red line in **Fig. 3.21** for an exemplary output frequency of $f_{\mathrm{out,max}} = 50\,\mathrm{kHz}$. It has to be noted that the introduced boundary still depends on the maximum output frequency, which later allows to choose the filter components in such a way that $f_{\mathrm{out,max}}$ is maximized.

- **Capacitive current demand:** Similar to the limitation of the inductive voltage drop, an upper limit for the filter capacitance is introduced to avoid excessive reactive currents to flow in the system. The reactive current demand is estimated as

$$\hat{i}_{\mathrm{C,max}} = \hat{v}_{\mathrm{out,max}} 2\pi f_{\mathrm{out,max}}\,(1+m)\,C_1, \quad (3.42)$$

where the voltage drop across the second stage filter inductor is neglected. Introducing a limit of 50 % of the nominal load current $\hat{i}_{\mathrm{out,nom}} = 61.5\,\mathrm{A}$ results in

$$C_1 < \frac{\hat{i}_{\mathrm{out,nom}}}{2\hat{v}_{\mathrm{out,max}} 2\pi f_{\mathrm{out,max}}\,(1+m)}, \quad (3.43)$$

with the according boundary in **Fig. 3.21** given as a green line for a maximum large-signal output frequency of $f_{\mathrm{out,max}} = 50\,\mathrm{kHz}$. Also in this case, the boundary depends on the value of $f_{\mathrm{out,max}}$.

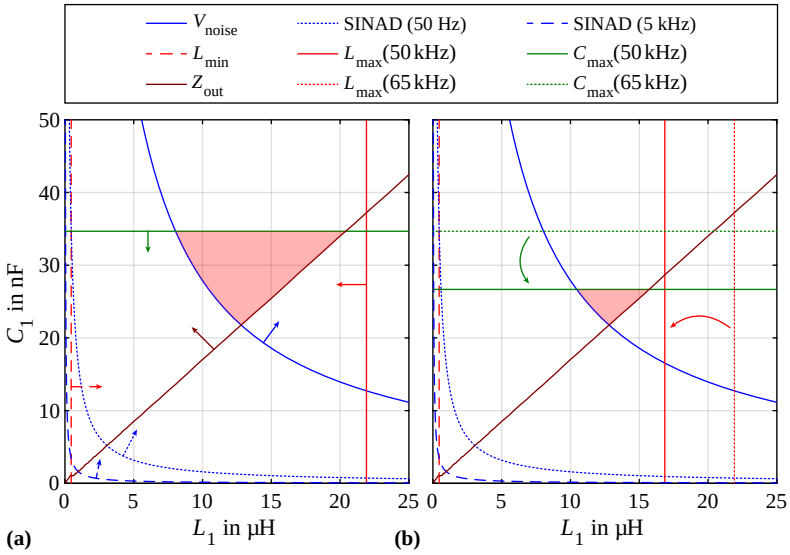


Fig. 3.24: Exemplary design space for $k = 0.1$, $m = 5$ and two different maximum output frequency values of **(a)** $f_{out,max} = 50\,kHz$ and **(b)** $f_{out,max} = 65\,kHz$. Increasing $f_{out,max}$ results in stricter design space limitations, where the maximum achievable output frequency for a given k and m is given by the value that shrinks the design space to a single point.

Considering the introduced constraints, a region of valid combinations of the filter elements L_1 and C_1 referred to as *design space* can be determined, which is highlighted as red area in **Fig. 3.21** for a given set of component ratios k and m. From this region, suitable values for L_1 and C_1 have to be selected, where it has to be considered that the two constraints belonging to the reactive power demand depend on the maximum large-signal output frequency $f_{out,max}$. From the according equations (3.41) and (3.43) it can be recognized that with increasing $f_{out,max}$ these constraints become more strict, i.e., higher values of $f_{out,max}$ shrink the design space. Consequently, this degree of freedom is utilized to determine the filter components such that the highest possible output frequency is achieved, which is accomplished by increasing the value of $f_{out,max}$ until the design space shrinks to a single point (cf. **Fig. 3.24**). The first stage filter elements L_1 and C_1 are then given by the coordinates (i.e., L_1 and C_1) of this point, whereas the second stage elements follow from $L_2 = kL_1$ and $C_2 = mC_1$.

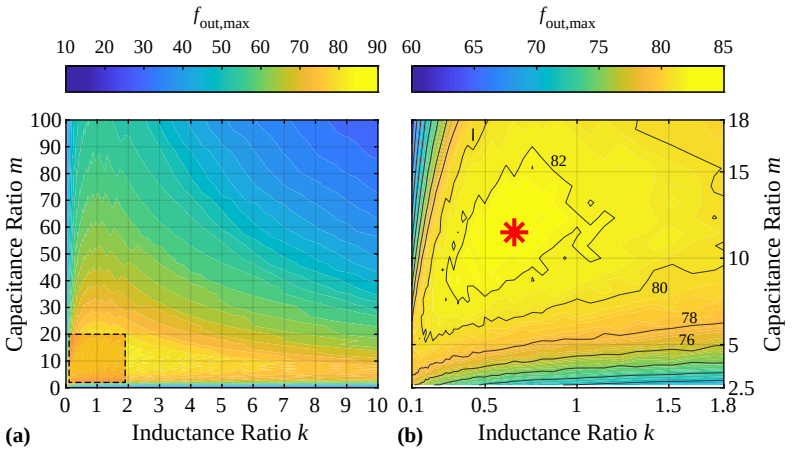


Fig. 3.25: Achievable large-signal output frequency $f_{\text{out,max}}$ as a function of the component ratios k and m. **(a)** Overview, **(b)** detailed view at the highlighted area.

With the above approach, optimal filter elements as well as a maximum large-signal output frequency are found for each combination of k and m. Discretizing k and m according to

$$k = 0.01 \cdot 10^{\frac{i}{33}}, \quad 0 \leq i \leq 99, \quad i \in \mathbb{N}, \tag{3.44}$$

$$m = 0.1 \cdot 10^{\frac{i}{33}}, \quad 0 \leq i \leq 99, \quad i \in \mathbb{N}, \tag{3.45}$$

and iterating over all possible combinations then allows to determine the overall achievable $f_{\text{out,max}}$ as a function of the component ratios, which is shown in **Fig. 3.25**.

From **Fig. 3.25** it can be recognized that the achievable maximum output frequency exhibits a maximum of ca. 80 kHz, where it has to be mentioned that the obtained maximum is flat, i.e., insensitive to the exact values of k and m since a larger number of different designs with k values ranging from 0.28 to 1 and m values from 7.5 to 16.3 allow output frequencies of > 82 kHz. The overall optimal design maximizing the output frequency can be determined to $k = 0.658$ and $m = 11.5$, enabling an output frequency of up to 83 kHz. **Fig. 3.26** presents the according design space, with the component values and the obtained performance qualifiers summarized in **Tab. 3.6**.

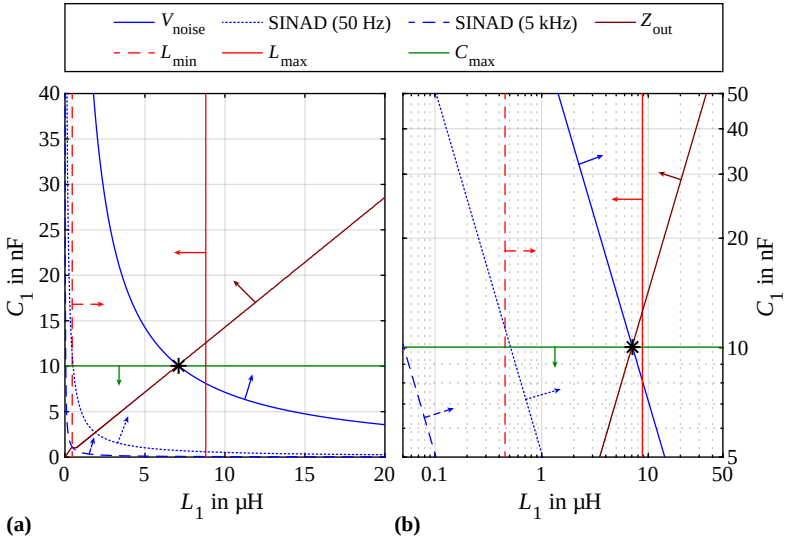


Fig. 3.26: Design space with **(a)** linear axes and **(b)** logarithmic axes for component ratios that maximize the converter's maximum large-signal frequency, $k = 0.658$ and $m = 11.5$.

Component	Value
L_1	7.1 µH
L_2	4.7 µH
C_1	10 nF
C_2	115 nF
L_d	9.3 µH
R_d	2.6 Ω
$f_{out,max}$	83 kHz

Tab. 3.6: Filter component values.

In a last step, the damping network of the filter is designed according to the expressions given in [96]:

$$a = \frac{L_\mathrm{d}}{L_2}, \tag{3.46}$$

$$R_\mathrm{d} = \sqrt{\frac{L_2}{C_2}} \cdot \frac{2a}{\sqrt{2a^2 + 6a + 4}}, \tag{3.47}$$

where a ratio between second stage filter inductor and damping inductor of $a = 2$ is suggested, resulting in an optimal damping resistor value of $R_\mathrm{d} = 2.6\,\Omega$.

Regarding the implementation of the DM output filter it has to be noted that the output path of the inverter stages already contains a certain DM inductance, which is formed by the leakage inductances of the cells' CMCs $L_{\mathrm{CM,c}}$ (cf. **Section 3.1.2**) that lie in the output terminals of the cells' inverter bridges. Additionally, the output filter also contains a first stage CMC ($L_{\mathrm{CM,f,1}}$ in the filter schematic presented in **Fig. 3.19**), which introduces additional leakage that acts as DM filter inductance. Consequently, since the value of L_1 is comparably small and falls into the range of the summed leakage inductances of the CMCs, the first stage DM inductor L_1 can be implemented by the leakage inductance of the involved CMCs rather than a single distinct component. The same holds true for the implementation of the second stage filter inductor L_2, which can be integrated into the leakage inductance of the second stage CMC $L_{\mathrm{CM,f,2}}$ (cf. **Fig. 3.19**). Details about the implementation of the DM filter inductors, including a schematic providing an overview over all the involved leakage inductances, are given in **Section 3.3.2**.

3.2.2 Common-Mode Filter

Since the CM output filter has no direct influence on the dynamic performance of the system, its design is based solely on the required attenuation to fulfill the RMS switch noise voltage criterion (see **Tab. 3.1**). Again, it has to be considered that in a first step half of the RMS noise voltage limit of 10 mV is required for the DM filter. Therefore, a total RMS noise voltage limit of 5 mV has to be considered for the CM noise at the output. For the design of the CM filter, a CM equivalent circuit of the converter has to be derived first, which allows to determine the occurring CM noise at the converter output. Based on the CM equivalent model the CM filter components can then be determined such that the required filter attenuation is obtained.

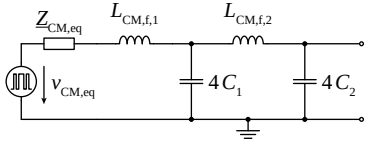


Fig. 3.27: CM filter structure. A two-stage CM filter is used where the CM capacitors are already given by the DM capacitances.

CM Equivalent Model

The CM model of the converter can be separated into the output filter and an equivalent noise source that originates from the cell stack. The according schematic is depicted in **Fig. 3.27** with the filter schematic originating from the CM equivalent of the total filter schematic in **Fig. 3.19** while neglecting the DM filter inductors L_1 and L_2 and the according damping elements L_d, R_d. It has to be noted that the CM filter capacitances are already determined by the DM filter capacitances since they are implemented by splitting the DM capacitors into a series connection of two components with twice the required value and connecting their midpoint to ground (cf. **Fig. 3.19**). Therefore, only the two CM filter inductors $L_{\mathrm{CM,f,1}}$ and $L_{\mathrm{CM,f,2}}$ have to be determined.

The CM equivalent model of the cell stack is based on the CM model introduced in **Section 3.1.2**, which is presented again in **Fig. 3.28**. It consists of the inverter bridges modeled by the voltage sources $v_{1,\mathrm{A}}$ to $v_{6,\mathrm{B}}$ as well as the lumped parasitic cell capacitances C_par and the cell CM filter elements $L_{\mathrm{CM,c}}$ and $R_{\mathrm{CM,c}}$ that are designed in **Section 3.1.2** to suppress the CM currents between the cells. Calculating the CM voltage at the stack output defined as

$$v_{\mathrm{CM,CHB}} = \frac{v_\mathrm{N} + v_\mathrm{P}}{2} \tag{3.48}$$

is accomplished by introducing an auxiliary potential v_H between the stack midpoint H and ground. The total CM voltage can then be calculated from the sum of the midpoint potential v_H and the CM voltage between stack midpoint and stack output, $v_{\mathrm{CM,H}}$, according to

$$v_{\mathrm{CM,CHB}} = v_\mathrm{H} + v_{\mathrm{CM,H}}, \tag{3.49}$$

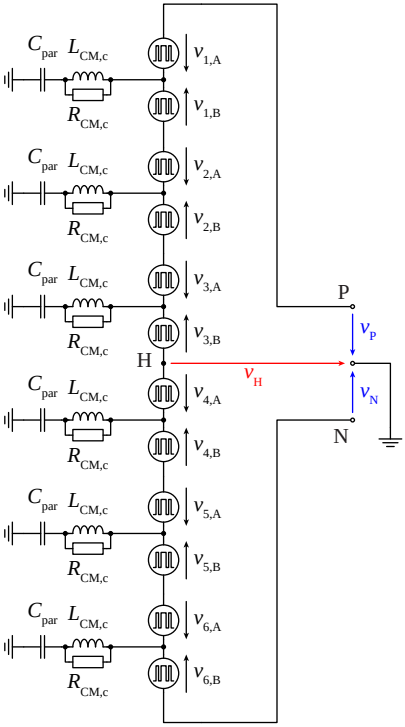


Fig. 3.28: Derivation of the CM equivalent circuit of the cell stack, based on the CM model introduced in **Section 3.1.2**. The total CM voltage can be determined by introducing the auxiliary potential v_H between the stack midpoint H and ground.

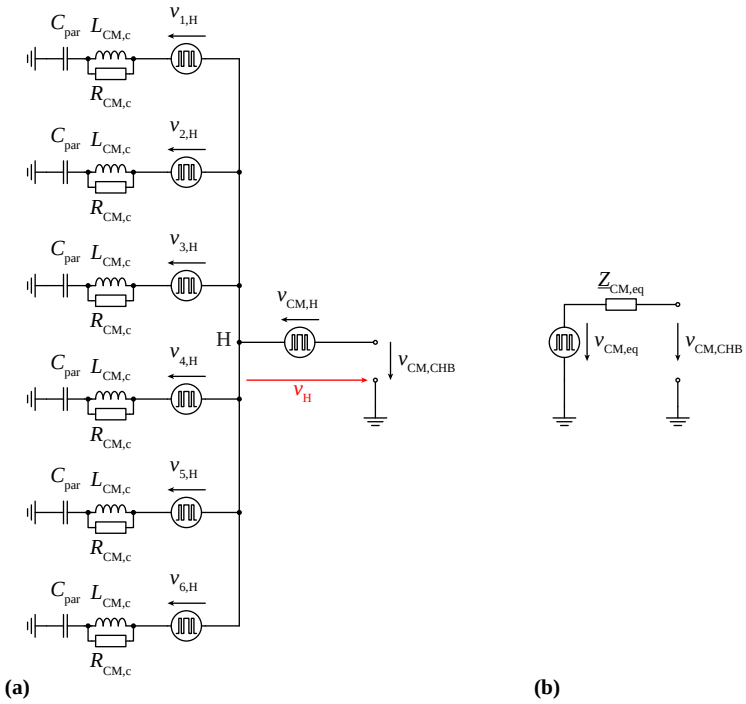


Fig. 3.29: (a) Simplified CM equivalent circuit diagram resulting from the combination of the different half-bridge voltages and **(b)** according Thévenin equivalent model, which is achieved by applying the superposition principle to the simplified CM schematic.

where $v_{\mathrm{CM,H}}$ follows from the half-bridge voltages according to

$$v_{\mathrm{CM,H}} = \frac{1}{2} \cdot \big(v_{6,\mathrm{B}} - v_{6,\mathrm{A}} + v_{5,\mathrm{B}} - v_{5,\mathrm{A}} + v_{4,\mathrm{B}} - v_{4,\mathrm{A}} - v_{3,\mathrm{B}} + v_{3,\mathrm{A}} - v_{2,\mathrm{B}} + v_{2,\mathrm{A}} - v_{1,\mathrm{B}} + v_{1,\mathrm{A}}\big) \,. \tag{3.50}$$

This allows to simplify the schematic from **Fig. 3.28** into the equivalent model in **Fig. 3.29**, where the half-bridge voltages $v_{1,\mathrm{A}}$ to $v_{6,\mathrm{B}}$ have been combined into the equivalent sources $v_{1,\mathrm{H}}$ to $v_{6,\mathrm{H}}$ in order to simplify the circuit. The respective expressions for these equivalent sources follow directly

from Kirchhoff's voltage law:

$$\begin{aligned} v_{1,\mathrm{H}} &= v_{3,\mathrm{B}} - v_{3,\mathrm{A}} + v_{2,\mathrm{B}} - v_{2,\mathrm{A}} + v_{1,\mathrm{B}} \\ v_{2,\mathrm{H}} &= v_{3,\mathrm{B}} - v_{3,\mathrm{A}} + v_{2,\mathrm{B}} \\ v_{3,\mathrm{H}} &= v_{3,\mathrm{B}} \\ v_{4,\mathrm{H}} &= v_{4,\mathrm{A}} \\ v_{5,\mathrm{H}} &= v_{4,\mathrm{A}} - v_{4,\mathrm{B}} + v_{5,\mathrm{A}} \\ v_{6,\mathrm{H}} &= v_{4,\mathrm{A}} - v_{4,\mathrm{B}} + v_{5,\mathrm{A}} - v_{5,\mathrm{B}} + v_{6,\mathrm{A}} \end{aligned} \tag{3.51}$$

The resulting circuit can finally be translated into a Thévenin equivalent model by applying the superposition principle, which results in the equivalent schematic in **Fig. 3.29b** with the inner impedance

$$\underline{Z}_{\mathrm{CM,eq}} = \frac{1}{6}\left(\frac{1}{sC_{\mathrm{par}}} + \frac{sL_{\mathrm{CM,c}}\,R_{\mathrm{CM,c}}}{sL_{\mathrm{CM,c}} + R_{\mathrm{CM,c}}}\right), \tag{3.52}$$

and an equivalent voltage

$$\begin{aligned} v_{\mathrm{CM,eq}} = \\ &\frac{1}{6}\left(-v_{5,\mathrm{A}} + v_{4,\mathrm{B}} + v_{3,\mathrm{A}} - v_{2,\mathrm{B}}\right) + \\ &\frac{1}{3}\left(-v_{6,\mathrm{A}} + v_{5,\mathrm{B}} + v_{2,\mathrm{A}} - v_{1,\mathrm{B}}\right) + \\ &\frac{1}{2}\left(v_{1,\mathrm{A}} + v_{6,\mathrm{B}}\right). \end{aligned} \tag{3.53}$$

Fig. 3.30 presents the frequency spectrum of the unfiltered CM voltage $v_{\mathrm{CM,eq}}$, where a sinusoidal signal with an RMS value of 230 V and a frequency of 50 Hz was assumed as a modulation reference for the cell stack.

CM Filter Dimensioning

With the unfiltered CM voltage given, the required filter attenuation can be determined such that the CM noise at the filter output remains within the required limits. In order to simplify the calculations, the same approach as in **Section 3.1.1** is used, i.e., the CM noise voltage spectrum is approximated by a single frequency component $V_{\mathrm{CM,eq,RMS}}$ at the lowest occurring frequency containing the entire signal energy instead of the real spectrum. The required attenuation $A_{\mathrm{CM}}(f_{\mathrm{s}})$ at the first harmonic frequency $f_{\mathrm{s}} = 300\,\mathrm{kHz}$ is then

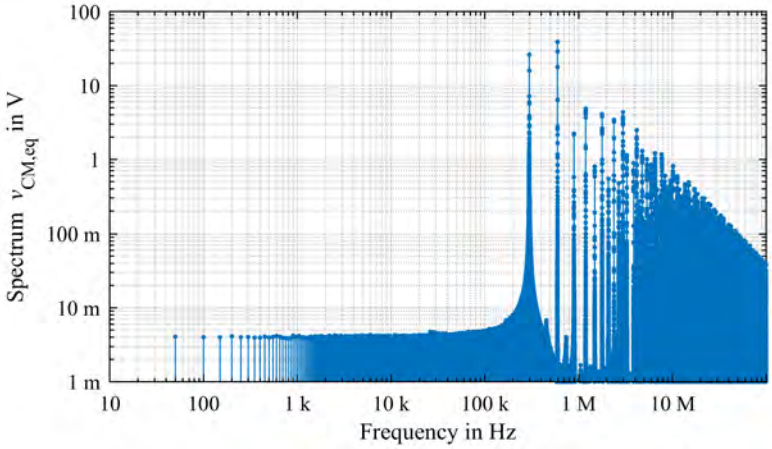


Fig. 3.30: Frequency spectrum of the unfiltered CM voltage $v_{CM,eq}$ for a 325 V amplitude, 50 Hz sinusoidal output waveform.

calculated according to

$$A_{CM}(f_s) = \frac{V_{CM,eq,RMS}}{\frac{1}{2}V_{noise,max}(f_s)} = 79.5\,\text{dB}, \tag{3.54}$$

where an equivalent noise voltage of $V_{CM,eq,RMS} = 47\,\text{V}$ was numerically calculated from the equivalent noise source in **Section 3.2.2** for an unloaded operating point with $\hat{v}_{out} = 325\,\text{V}$ (cf. **Fig. 3.30**). The additional factor of ½ in the denominator is required since only half of the noise voltage is assumed to originate from the CM noise (the other half of the noise originates from the DM noise).

With the filter capacitances given and neglecting the CM impedance $\underline{Z}_{CM,eq}$, the CM filter inductors can again be determined from the required attenuation of a two-stage filter given by (3.7), resulting in

$$L_{CM,f,1} = \sqrt{\frac{A_{CM}(f_s)\,(a_1 a_2)^2}{(2\pi f_s)^4\,(4C_1)^2}}. \tag{3.55}$$

However, the frequency factors a_1 and a_2 that relate the corner frequencies of the two-stage filter to its characteristic frequency according to (3.6) have to be determined first. This requires the selection of a suitable inductance

ratio $k_{\mathrm{CM}} = {}^{L_{\mathrm{CM,f,2}}}/_{L_{\mathrm{CM,f,1}}}$ between the CM inductances. A suitable inductance ratio for the CM inductance values can be found by considering the following relations between the leakage inductances $L_{\sigma,i}$ (corresponding to the DM inductance) and the main inductances $L_{\mathrm{m},i}$ (representing the CM inductance) of the two filter coils:

$$\begin{aligned} L_{\sigma,i} &= \frac{(2N_i)^2}{R_{\mathrm{m,DM},i}}, \\ L_{\mathrm{m},i} &= \frac{N_i^2}{R_{\mathrm{m,CM},i}}, \end{aligned} \qquad \text{for } i = \{1,2\}, \tag{3.56}$$

where N_i denotes the number of turns for each of the two identical windings of the i-th inductor and $R_{\mathrm{m,DM},i}$ and $R_{\mathrm{m,CM},i}$ represent the according magnetic reluctances of the leakage and main magnetic flux paths, respectively. Considering similar core geometries and winding techniques for the two inductors, it can be assumed that the ratio between leakage and main reluctance for each component is approximately the same, i.e.,

$$\frac{R_{\mathrm{m,DM},1}}{R_{\mathrm{m,CM},1}} = \frac{R_{\mathrm{m,DM},2}}{R_{\mathrm{m,CM},2}} \implies \frac{R_{\mathrm{m,DM},1}}{R_{\mathrm{m,DM},2}} = \frac{R_{\mathrm{m,CM},1}}{R_{\mathrm{m,CM},2}} \tag{3.57}$$

applies and consequently

$$k = \frac{L_{\sigma,2}}{L_{\sigma,1}} = \frac{\frac{(2N_2)^2}{R_{\mathrm{m,DM},2}}}{\frac{(2N_1)^2}{R_{\mathrm{m,DM},1}}} = \frac{\frac{N_2^2}{R_{\mathrm{m,CM},2}}}{\frac{N_1^2}{R_{\mathrm{m,CM},1}}} = \frac{L_{\mathrm{m},2}}{L_{\mathrm{m},1}} = k_{\mathrm{CM}}. \tag{3.58}$$

For this reason, $k_{\mathrm{CM}} = k = 0.658$ is selected. The values for the filter inductors then follow from (3.55) to $L_{\mathrm{CM,f,1}} = 250\,\mu\mathrm{H}$ and $L_{\mathrm{CM,f,2}} = k_{\mathrm{CM}} L_{\mathrm{CM,f,1}} = 164\,\mu\mathrm{H}$.

3.3 Hardware Realization of Cell and Phase Stack

This section provides the description of the hardware realization of the converter cell as well as the entire phase stack that was constructed in order to verify the theoretical design considerations. In **Section 3.3.1** a description of the CHB converter cell is presented, whereas **Section 3.3.2** describes the hardware implementation of the CHB phase stack. Details about the implementation of the control system are discussed later in **Chapter 4.5**.

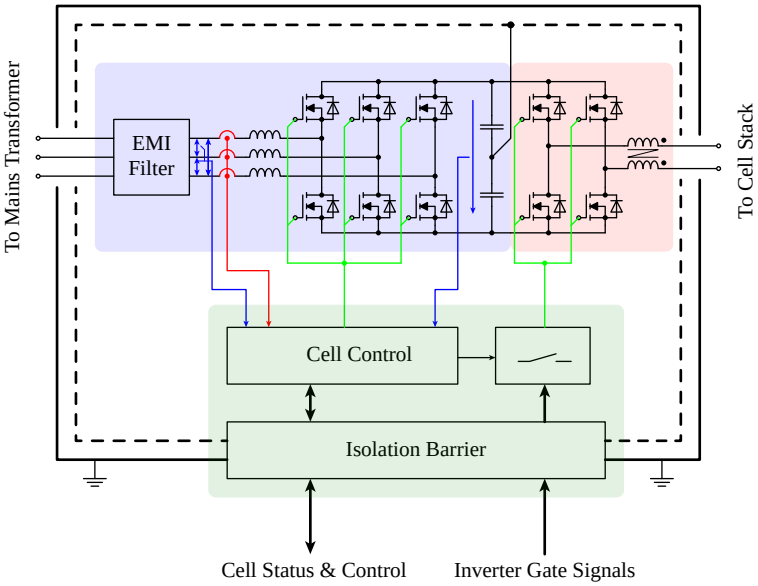


Fig. 3.31: Schematic overview of a converter cell.

3.3.1 CHB Converter Cell

Fig. 3.31 presents the schematic overview of a single CHB cell. For the power supply of the cells, the LF isolation approach suggested in **Section 2** was selected, i.e., each of the cells contains a three-phase boost-type PFC rectifier connected to the secondary winding system of a 50 Hz transformer that provides galvanic isolation and steps down the voltage. For the design of the DC-link capacitor, the approach described in **Section 2.1** is applied, resulting in a DC-link capacitance of 100 mF for the 100 V DC-link of each cell, where a grid impedance of 15 mΩ + j15 mΩ (referred to as "strong grid" in **Section 2.1**) was considered. However, due to constructive reasons, a smaller DC-link capacitor of 77 mF per cell was finally implemented in the prototype and the analysis from **Section 2.1** is used to implement a power derating for certain low output frequencies in order to guarantee compliance with the IEC 61000 standard. This is considered acceptable since the derating only affects converter operation within a very small output frequency interval between 3.1 Hz and 4.8 Hz, which can be recognized from the resulting derating curve in **Fig. 3.32**. Besides the DC-link capacitor, the design of the PFC rectifier follows state-of-the-art design guidelines with *dq* control being used for control of the rectifier.

Control of the PFC rectifier is established by a local cell controller containing a *Xilinx Zynq 7000 XC7Z020* SoC [221] for data processing, which, besides controlling the PFC rectifier operation, implements monitoring and supervision features of the cell and handles the communication with a superordinate external central control unit. Since PFC rectifier control is independent of the central controller, the cell is able to perform a black start from the grid as the PFC rectifier's three-phase bridge operates as diode rectifier during start up, which charges the DC-link to a sufficiently high voltage to allow the cell controller to operate. Contrary to the PFC rectifier, the inverter stages of the cells are not controlled by the local cell controllers but receive their gate signals directly from the central control unit. The local cell controller has no influence on the inverter control, except in fault conditions (e.g., overtemperature, grid overcurrent of the PFC rectifier, supply voltage failure, etc.) where it deactivates the entire inverter bridge.

Besides the inverter gate signals, a communication interface between cell and central control to exchange status and supervision information is required, which is implemented via an Serial Peripherial Interface (SPI) with the cells being configured as slaves. A direct communication channel between the cells themselves is not required. Since the local cell controller is referred

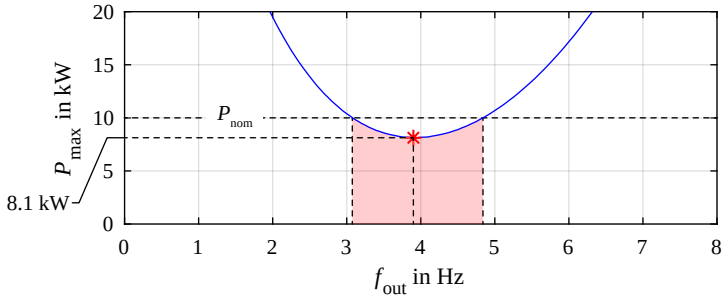


Fig. 3.32: Maximum allowed output power P_{max} of the converter as a function of the output frequency f_{out} if compliance with the IEC 61000 grid standard has to be ensured. Due to the limited DC-link capacitance of 77 mF per cell implemented in the converter prototype, a derating of the available output power below the nominal value of $P_{nom} = 10\,kW$ is required for frequencies between 3.1 Hz and 4.8 Hz in order to guarantee compliance with IEC 61000 for these operating points. The affected frequency interval is highlighted in red, with a minimum value of the available output power of $P_{max} = 8.1\,kW$ being reached for an output frequency of $f_{out} = 3.9\,Hz$. A DC-link capacitance of 100 mF for each cell would be required if compliant operation with the full nominal power also for the derated frequency interval would have to be ensured.

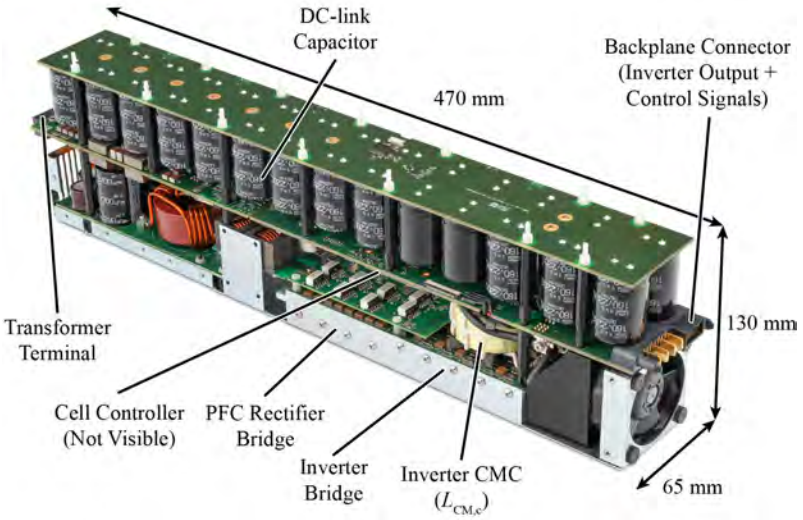


Fig. 3.33: Single converter cell with both housings removed. A large portion of the volume is occupied by the DC-link capacitors required to comply with the IEC 61000 grid regulations.

to its respective DC-link midpoint, whereas the central control unit lies on earth potential, all communication signals have to pass an isolation barrier.

As already mentioned in **Section 3.1.2**, each cell has two housings connected to different potentials, namely the inner housing connected to the cell's DC-link midpoint and the outer housing connected to earth. Pictures of the cell are given in **Fig. 3.33** with most of the housing components removed and in **Fig. 3.34**, where the two cell housings and the according isolation air gap are clearly visible. The mechanical dimensions of the inner housing are $l = 470\,\text{mm}$, $w = 128\,\text{mm}$ and $h = 67\,\text{mm}$ for length, width and height, respectively. With a distance between inner and outer housing of ca. $d = 5\,\text{mm}$, a parasitic capacitance of

$$C_{\text{cell}} = \frac{A_{\text{surf}}\epsilon_0}{d} = 360\,\text{pF} \tag{3.59}$$

results, where ϵ_0 is the vacuum permittivity and $A_{\text{surf}} = 20\,\text{dm}^2$ denotes the surface area of the inner cell housing. Together with the specified parasitic capacitance of the transformer of 120 pF this justifies the estimation of the total parasitic CM capacitance stated in **Section 3.1.2**.

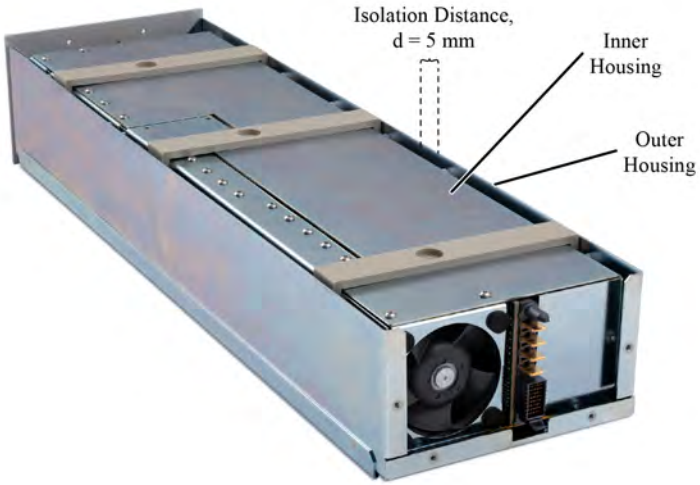


Fig. 3.34: Single converter cell with the inner housing installed but the top-side of the outer housing removed. The isolation air gap of 5 mm between the two mechanical enclosures is clearly visible.

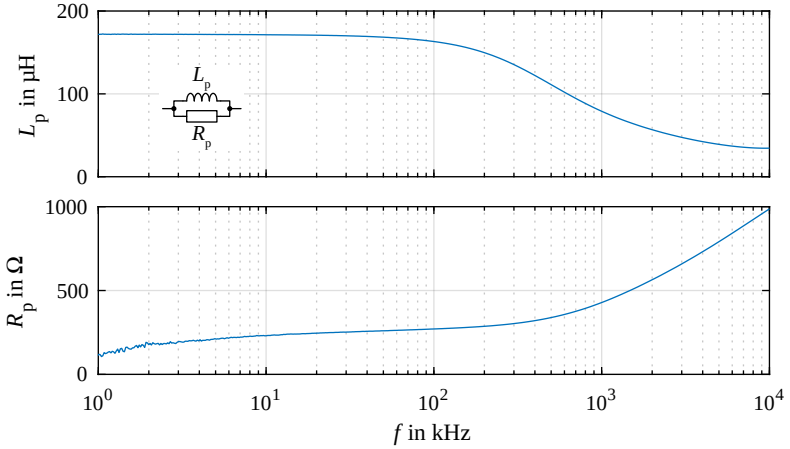


Fig. 3.35: Measured inductance and parallel resistance of the cell CMC if the component is modeled as a parallel combination of an inductance L_p and a parallel resistance R_p. A main inductance of 170 µH is found, which decreases with increasing frequency.

Special attention has to be paid to the implementation of the cells' CMCs since their leakage inductance is used for the implementation of the first stage filter inductor L_1 (cf. **Section 3.2.1**). A *T60004-L2050-W583-51* core from *Vacuumschmelze* with $N = 4$ turns for each winding was used to implement the CMCs, resulting in an expected main inductance value of $L_{CM,c} = A_L N^2 = 160\,\mu H$ for $A_L = 10\,\mu H$ given in the according core datasheet [222] at 100 kHz. A measurement of this inductance is shown in **Fig. 3.35** where the component is modeled as a parallel combination of an inductor L_p with a parallel resistance R_p that models the losses occurring in the inductor. The measurement reveals a slightly higher value of ca. 170 µH that starts to reduce for frequencies above ca. 150 kHz due to characteristic properties of the employed *VITROPERM 500F* nanocrystalline core material [223]. Due to these properties, the inductor exhibits a more and more resistive characteristic instead of an inductive behavior for increasing frequency, which allows to omit the damping resistors $R_{CM,c}$ intended to eliminate resonances of the CMC since the losses of the core material provide sufficient damping. This is recognized from the measured parallel resistance

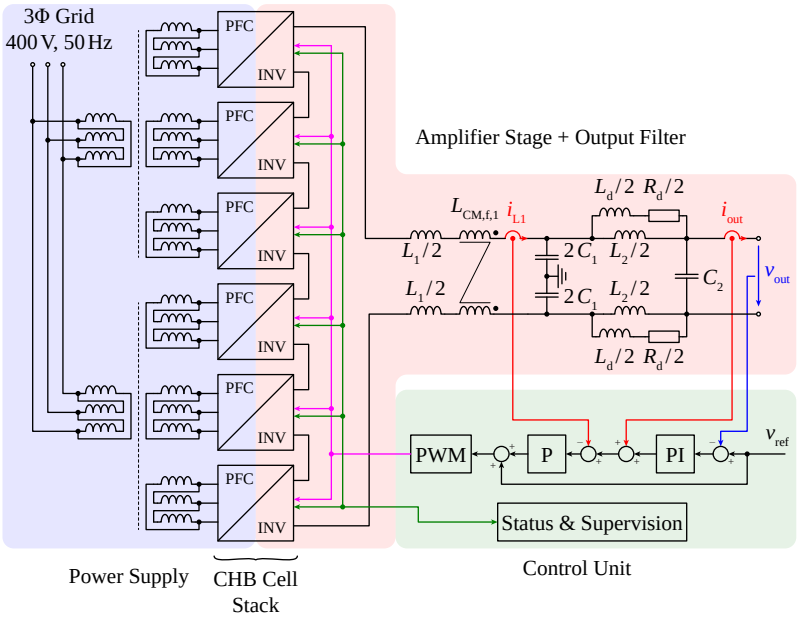


Fig. 3.36: Schematic overview over the entire UH-PBW amplifier system.

of 360 Ω in the vicinity of the resonance frequency

$$f_{\mathrm{CM,res}} = \frac{1}{2\pi\sqrt{L_{\mathrm{CM,c}} C_{\mathrm{par}}}} = 637\,\mathrm{kHz} \tag{3.60}$$

given by the resonant tank formed from the cells' parasitic ground capacitance $C_{\mathrm{par}} = 500\,\mathrm{pF}$ and $L_{\mathrm{CM,c}}$, which is close to the value of $R_{\mathrm{CM,c}} = 250\,\Omega$ dimensioned in **Section 3.1.2**.

Similarly to the CM inductance, the leakage inductance of the constructed CMC was measured, where a leakage inductance of $L_\sigma = 1.4\,\mu\mathrm{H}$ was found. Consequently, for a series connection of 6 cells a total inductance of 8.4 µH results that is used as part of the first stage filter inductor L_1.

3.3.2 CHB Phase Stack

The schematic overview of the entire system is repeated in **Fig. 3.36**. Besides the converter cells the UH-PBW amplifier system consists of a central control

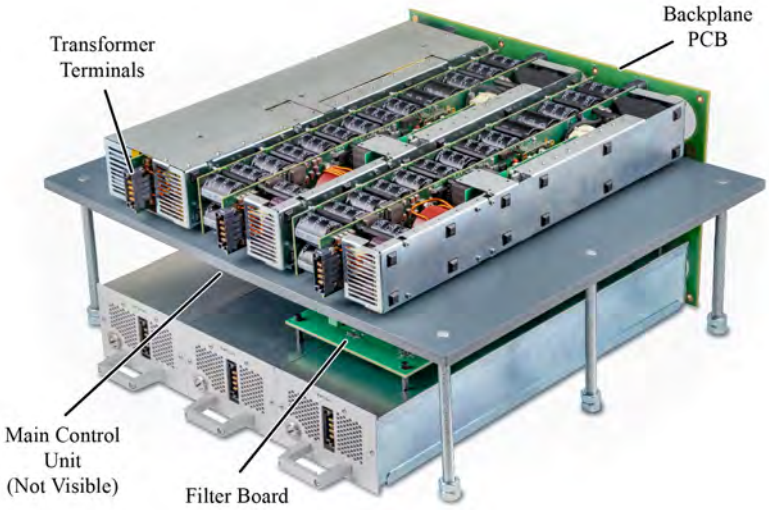


Fig. 3.37: Front view of the CHB phase stack. The lower three cells are mounted in their respective housings while the outer housings of the upper three cells were removed. In between the upper and lower three cells of the phase stack, the output filter and the central control unit are located.

unit that executes the controller and the output filter board that incorporates the output filter as well as the voltage and current sensors. Furthermore, these entities are connected via a backplane PCB that contains the signal communication lines and the power traces that connect the cells and the output filter. For all communication lines, Low Voltage Differential Signaling (LVDS) is used to improve noise immunity. In addition, two multi-winding transformers with three secondary three-phase winding systems each are used to supply the cell's PFC interface. Pictures of the prototype system are presented in **Fig. 3.37** and **Fig. 3.38**. Details about the implementation of the central control unit are provided in **Chapter 4.5**.

Regarding the output filter it has to be mentioned that a preliminary version of the filter board was utilized for the prototype system which deviated from the optimum filter design presented in **Section 3.2**. The preliminary version did not contain the dimensioned CM filter but instead incorporated a single-stage CM filter. Furthermore, a different (k, m) combination from **Fig. 3.25** and a different filter damping element was used. **Fig. 3.39** provides

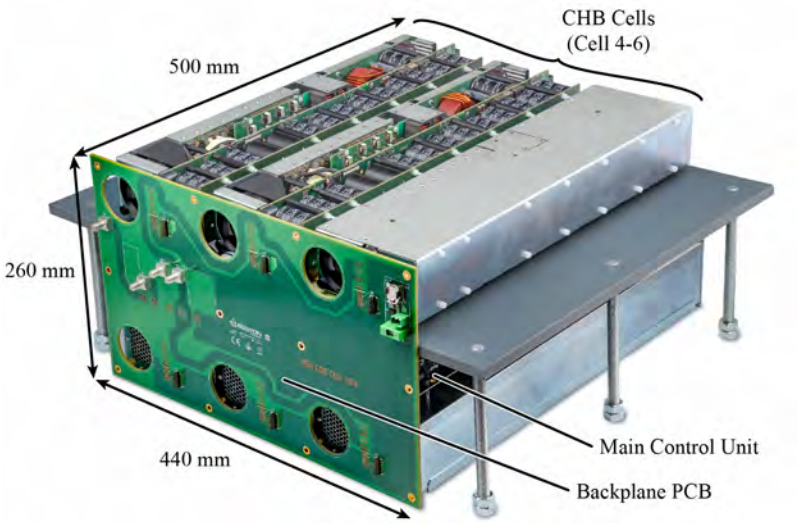
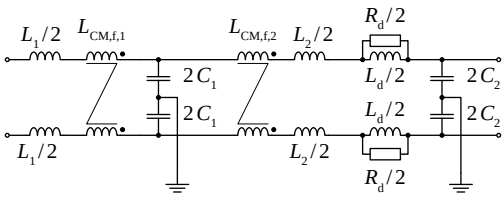
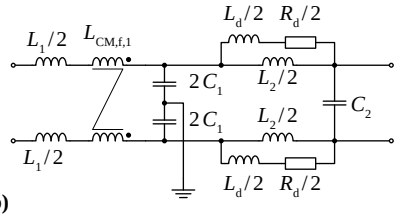


Fig. 3.38: Back view of the CHB phase stack. A backplane PCB containing the power routing as well as the communication lines is utilized to connect the cells of the phase stack.



(a)

L_1 = 7.1 µH
L_2 = 4.7 µH
C_1 = 10 nF
C_2 = 115 nF
L_d = 9.4 µH
R_d = 2.6 Ω
$L_{CM,f,1}$ = 250 µH
$L_{CM,f,2}$ = 164 µH
$f_{out,max}$ = 83 kHz



(b)

L_1 = 10 µH
L_2 = 930 nH
C_1 = 50 nF
C_2 = 86 nF
L_d = 2 µH
R_d = 7.5 Ω
$L_{CM,f,1}$ = 370 µH
$L_{CM,f,2}$ = N/A
$f_{out,max}$ = 77 kHz

Fig. 3.39: Differences between **(a)** the filter designed according to **Section 3.2** and **(b)** the preliminary filter used in the prototype converter. Besides the deviations in the component values, the implemented filter does not contain the CM filter inductance $L_{\mathrm{CM,f,2}}$. Furthermore, a different damping network L_d, R_d was implemented.

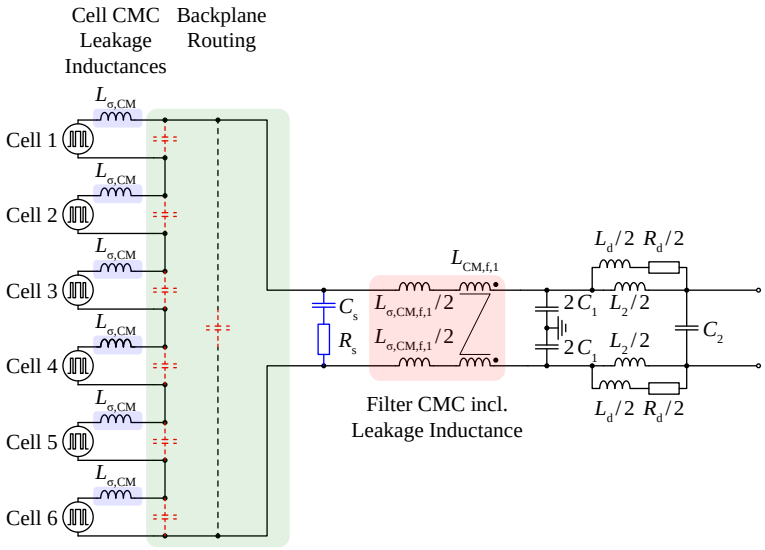


Fig. 3.40: Electrical interconnection of the leakage inductances of the CMCs of the cells and of the filter CMC used as differential-mode inductance. The parasitic capacitances of the backplane power traces form resonant networks with the leakage inductances of the CMCs that lead to resonance of the filter input voltage. In order to suppress these oscillations, the snubber circuit C_s, R_s was installed.

a comparison between the designed and the preliminary filter version and their respective component values. Due to deviating component values and the missing CM filter stage the CM noise floor of the output voltage was higher than what was requested in **Section 3.2** and the prototype exhibited a slightly reduced output bandwidth.

As mentioned in **Section 3.3.1**, the first stage DM filter inductor L_1 is implemented by the leakage inductances of the CMCs in the cells and the output filter. For the first stage CMC of the output filter a commercial component is used, featuring a leakage inductance of 2.1 µH. Together with the combined leakage inductance of the cell's CMCs, a total DM inductance of 10.5 µH results, which corresponds to the required value from **Fig. 3.39**, i.e., no distinct filter inductor for L_1 is required.

Fig. 3.40 provides a more detailed overview of the involved inductances and their respective electrical interconnection, along with a simplified illustration of the parasitic capacitances of the backplane power traces. During

commissioning it was found that the distributed filter inductances (formed by the CMC's leakage inductances) form resonant circuits together with the distributed parasitic capacitances of the backplane power traces. These are excited by the switching actions of the inverter bridges. For this reason, an RC snubber element with $R_s = 75\,\Omega$ and $C_s = 2\,\text{nF}$ was placed on the backplane close to the filter terminals in order to attenuate the observed oscillations, although it has to be mentioned that the utilized snubber was not able to fully eliminate the occurring resonances. The influence of the snubber circuit on the converter dynamics can be neglected as the capacitance C_s of the snubber element is negligible compared to the filter capacitor value.

4

Control System Design and Optimization

4.1 Introduction

Considering typical applications of the UH-PBW amplifier, such as P-HIL simulations or grid emulation, the amplifier is usually embedded in a larger test setup where a setpoint voltage is provided from a superordinate application (cf. **Fig. 1.12** in **Section 1.2**). The task of the control system discussed in the following is to provide accurate tracking of this reference signal and to ensure proper reaction of the converter to external disturbances (e.g., load variations) such that the desired output voltage of the converter is obtained. Consequently, the system that has to be controlled by the controller consists of the output filter including the connected load and the cells' inverter stages, where the controller determines the setpoint voltage for the PWM modulator that generates the gate signals for the cells' bridge-legs. Furthermore, the dynamics of the measurement acquisition and the execution delay times of the control algorithm have to be considered in the controller design since these significantly influence the dynamic behavior of the closed-loop system. Only digital controller implementations are considered in the following since both, the modulator as well as the control system, are implemented on a digital platform that consists of an FPGA and an according high-speed analog front-end to digitize the measured quantities.

Regarding the employed control structure, a large variety of different topologies can be found in literature. Following a similar categorization as [48], *linear* and *nonlinear* controllers can be distinguished [224]. The most prominent examples for linear controllers are regular PID control loops

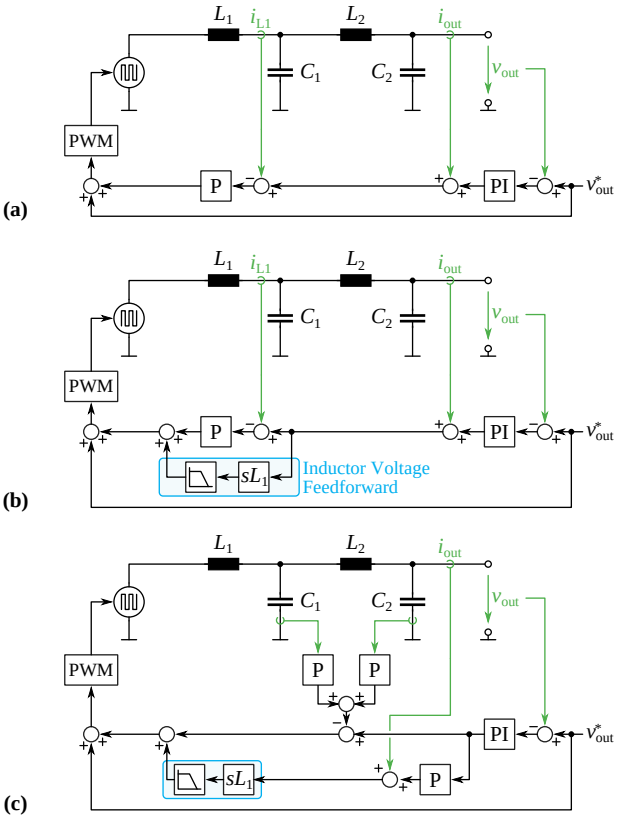


Fig. 4.1: Examples of linear cascaded control structures applicable for the UH-PBW amplifier, as already presented in [56] and **Fig. 1.16** of this thesis. **(a)** Outer PI voltage controller with inner P current controller and two feedforward (load current and reference voltage feedforward) paths. **(b)** Same control structure as **(a)** but extended by an additional inductor current feedforward path suggested in [53]. **(c)** Outer PI voltage controller combining capacitor current feedback suggested in [97] and including optional inductor voltage feedforward from [53].

[225–227] and according cascaded control structures based on several nested PID control loops. These are widely used for power converters [228, 229] in general due to their simplicity and were also suggested in [53, 97] for a similar high-bandwidth application. Several examples of these cascaded control structures reported in literature are depicted in **Fig. 4.1**, which are based on an outer PI voltage controller and incorporate different forms of inner current control loops and additional feedback and/or feedforward paths.

Another prominent example of a linear control structure used for the control of an inverter is deadbeat control [230, 231], which refers to a control strategy solely applicable for discrete-time systems. Deadbeat control aims to eliminate the error between reference and actual output signal within the minimum possible number of time steps [232]. However, the design of a deadbeat controller requires precise characterization of the controlled system, resulting in a high sensitivity to parameter deviations [232, 233]. This makes it particularly challenging to determine a suitable controller if different types of connected loads have to be considered that alter the dynamics of the controlled system.

A further example of a linear controller includes linear state-feedback control [224, 226, 234] which in the general case, however, requires knowledge of all states of the system under control either by measurement or by estimation, thereby increasing the implementation effort since additional senors or state estimators are required. In addition, several control concepts using linear controllers in rotating coordinate frames (e.g., *dq* control) [235, 236], repetitive control [237, 238] and resonant controllers [239, 240] are reported in literature. However, these are rendered unsuitable for the intended application since the output frequency of the amplifier is not a priori known and moreover, the output voltage waveform is not necessarily a sinusoidal signal.

Besides linear control concepts, various nonlinear control techniques exist. A detailed overview on nonlinear control strategies for inverters is beyond the scope of this thesis, noticeable examples include hysteresis control [241, 242], model predictive control [243–245], feedback linearization [246, 247], fuzzy control [248, 249] or adaptive control schemes [250–252]. Model predictive control has gained more and more interest in research in recent years but was rendered unsuitable due to the short execution times of the controller required for a high-bandwidth application. Generally, nonlinear controllers are significantly more difficult to design and optimize since the well established analytical tools to characterize the dynamic behavior of a system in the Laplace domain are restricted to linear systems. This heavily complicates the analysis of the resulting system behavior and makes investigations on

the closed-loop characteristic (e.g., regarding stability for different load cases) significantly more challenging. Furthermore, a nonlinear controller also implies a general nonlinear behavior of the closed-loop system of the amplifier. Since in many intended applications the converter will be a subsystem of a larger controlled system, e.g., in a P-HIL simulator where the setpoint for the amplifier is subject to a control loop itself, the introduced nonlinearity of this component is undesirable since the above mentioned complications are also subject to the dynamics of the superordinate system which then faces similar complications. For this reason, a linear control structure was selected for the UH-PBW amplifier, where the multi-loop control structure depicted in **Fig. 4.1a** incorporating an inner P current controller and an outer PI voltage controller was chosen for the implementation. The selected structure contains two feedforward paths for the load current and the reference voltage, which in [97] were reported to improve the dynamic performance of the controller.

With the control structure given, the main aspect of the control design is then to find suitable control gains which optimize the achievable dynamic performance of the converter while considering different types of connected loads. In order to accomplish this, suitable performance indices to quantify the dynamic properties of the closed-loop system under different loading conditions are introduced first. Based on these performance metrics, a multi-objective Pareto optimization is employed to find an optimal set of control parameters, where a reasonable tradeoff between different performance indices and load cases has to be identified.

This chapter is structured as follows: in **Section 4.2**, a simplified design approach using several simplifying approximations is used to determine the gains of the controllers. However, since this procedure is based on the phase margin criterion, which is only applicable for stable control plants, it cannot be applied to the general case including constant power loads, which introduce unstable poles in the filter transfer function. For this reason, a more detailed model of the converter is derived and used for a multi-objective Pareto optimization of the control parameters in **Section 4.3**, which determines an optimal set of control gains for different realization options of the PWM modulator. In **Section 4.4**, a verification of the dynamic behavior by means of circuit simulations is conducted. The simulations reveal that the PWM modulator may introduce unexpected nonlinear effects during transients, which cannot be described by the linear model, and different strategies to mitigate these effects are briefly investigated. Finally, **Section 4.5** provides additional details about the implementation of the control system on a high performance FPGA.

4.2 Simplified Control Design

In this section a simplified procedure to determine the control gains of the cascaded control structure illustrated in **Fig. 4.1a** is provided. The approach is based on decoupling the cascaded controller into two largely independent control loops: an outer voltage control loop which provides a reference current value $i_{\mathrm{L1,ref}}$ to an inner current control loop controlling the filter current i_{L1} in the filter inductor L_1. The control gains are then selected such that certain phase margin values are obtained for the two control loops. In order to decouple the system into two independent parts and simplify the resulting expressions, the following approximations of the converter dynamics are made:

- The two-stage LC filter is approximated by a single-stage LC filter by lumping the capacitance values of C_1 and C_2 into a single capacitance $C_{\mathrm{eq}} = C_1 + C_2$ and neglecting the inductance L_2 and the damping network L_{d}, R_{d} since the inductance of the filter inductor L_2 is small compared to L_1.
- Since the dynamics of the output voltage v_{out} are assumed to be slow compared to the dynamics of the inductor current i_{L1}, the change in capacitor voltage v_{out} can be neglected for the dynamics of the inner current control loop. For this reason, the plant which is controlled by the P current controller only consists of the filter inductor L_1 with the voltage on the filter capacitor being neglected concerning dynamics.
- The time delays introduced by various dynamic elements at several locations in the control loop are approximated by a lumped delay time T_{sum}. This accounts for the execution times of the digital implementation of the controllers, the conversion time of the measuring ADCs and the delays occurring in the power hardware (gate drive/signal path delays, switching times of power MOSFETs and interlock delay times).
- Both feedforward paths (reference voltage feedforward, load current feedforward) are neglected.
- The dynamics introduced by the measurements (voltage measurement, current sensors) are neglected.
- No-load conditions are assumed, i.e., the plant to be controlled only consists of the filter without any load connected to the output of the converter.

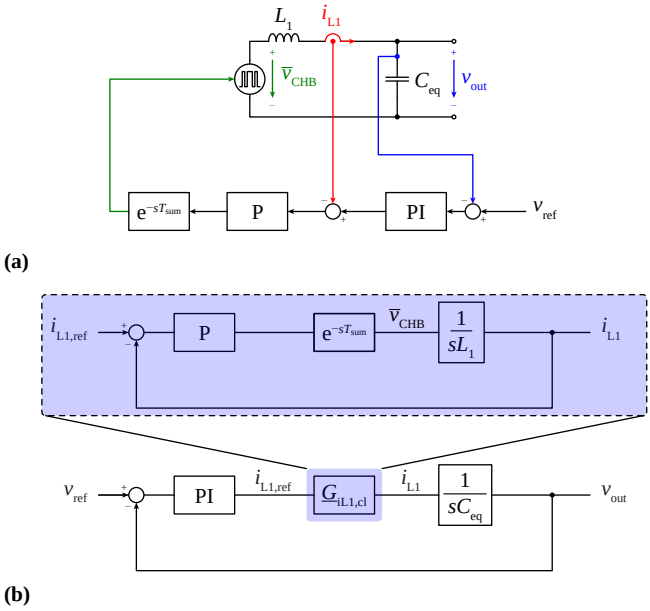


Fig. 4.2: (a) Simplified control structure. The two-stage LC output filter is approximated by a single-stage filter with equivalent capacitance $C_{\text{eq}} = C_1 + C_2$ and no-load conditions are assumed. Furthermore, the dynamics of the voltage and current measurements and both feedforward paths are neglected and the distributed delays occurring in the system are summarized into a single lumped transport delay T_{sum}. **(b)** According control block diagram consisting of an inner current control loop and an outer voltage control loop. In order to decouple both loops, the dynamic behavior of the capacitor voltage is assumed to be significantly slower than the dynamic of the filter current i_{L1}, allowing to neglect the capacitor voltage for the design of the current controller.

The resulting control block diagram following from these simplifications is depicted in **Fig. 4.2**. The inner current control loop consists of a P controller which controls the plant containing the lumped transport delay T_{sum} and the filter inductor L_1. The current controller sets the current flowing from the filter inductor into the output capacitor, consequently the outer voltage control loop incorporates the closed-loop current controller as a subsystem together with its according PI controller and the filter capacitor. For T_{sum} an estimation of 50 ns ADC conversion delay, 150 ns delay in the switching stage and 100 ns for controller execution in the FPGA is made, resulting in a total value of $T_{\text{sum}} = 300$ ns. Modeling is done entirely in the Laplace domain (s-domain) rather than in the z-domain since a natural sampling modulator (exhibiting no modulator delay [164]) is assumed. Furthermore, later the controllers in the FPGA including the ADCs will be implemented as pipelined structures and operate with a sampling frequency of 125 MHz, which calculate a new modulator reference sample every FPGA clock cycle. For this reason, the quantization time step is given by the FPGA clock period, which is short enough for the system to be treated as time-continuous. Details about the implementation can be found in **Section 4.5**.

4.2.1 Current Controller Dimensioning

The control design starts with determining the gain of the P current controller, $K_{\text{p,iL1}}$, where a phase margin of $PM_{\text{iL1}} = 40°$ is used as a design criterion. The according open-loop transfer function is given by

$$\underline{G}_{\text{iL1,ol}}(s) = K_{\text{p,iL1}}\, \mathrm{e}^{-s\, T_{\text{sum}}} \frac{1}{sL_1}, \tag{4.1}$$

with the according expression for the open-loop gain and phase resulting to

$$|\underline{G}_{\text{iL1,ol}}(s)| = \frac{K_{\text{p,iL1}}}{\omega\, L_1}, \quad \angle \underline{G}_{\text{iL1,ol}}(s) = -\frac{\pi}{2} - \omega\, T_{\text{sum}}, \tag{4.2}$$

where $\omega = 2\pi f$ denotes the angular frequency. From the above expression it is recognized that the phase of $\underline{G}_{\text{iL1,ol}}(s)$ is independent of the control gain $K_{\text{p,iL1}}$. The frequency $f_{0\text{dB,i}}$ for which the transfer function has to reach unity is therefore given directly by the point where the open-loop phase reaches $PM_{\text{iL1}} - 180° = -140°$, which for the case at hand results in $f_{0\text{dB,i}} = 463$ kHz. Setting $|\underline{G}_{\text{iL1,ol}}(s)|$ to unity at this frequency then allows to determine the gain of the controller to $K_{\text{p,iL1}} = 30\,\text{V/A}$.

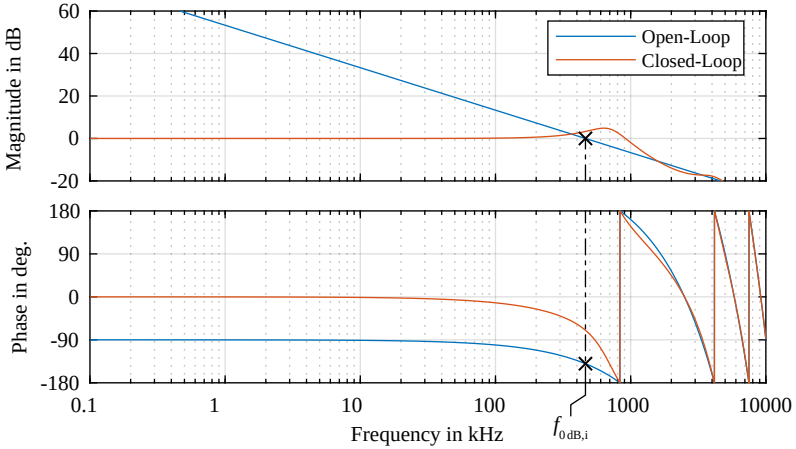


Fig. 4.3: Open- and closed-loop Bode plot of the inner current controller. A phase margin of 40° is obtained for $K_{\mathrm{p,iL1}} = 30\,\mathrm{V/A}$ at a frequency of $f_{0\mathrm{dB,i}} = 463\,\mathrm{kHz}$.

The according closed-loop transfer function of the current controller results to

$$\underline{G}_{\mathrm{iL1,cl}}(s) = \frac{i_{\mathrm{L1}}}{i_{\mathrm{L1,ref}}} = \frac{K_{\mathrm{p,iL1}}\,\mathrm{e}^{-sT_{\mathrm{sum}}}}{sL_1 + K_{\mathrm{p,iL1}}\,\mathrm{e}^{-sT_{\mathrm{sum}}}}. \tag{4.3}$$

with the open- and closed-loop transfer function of the current controller depicted in **Fig. 4.3**.

4.2.2 Voltage Controller Dimensioning

A similar approach is used to determine the control parameters ($K_{\mathrm{p,vout}}$ and $T_{\mathrm{i,vout}}$) for the outer voltage controller, where a larger phase margin of $PM_{\mathrm{vout}} = 60°$ is demanded to guarantee a sufficiently small step response overshoot. With the transfer function of the PI controller

$$\underline{G}_{\mathrm{PI,vout}}(s) = K_{\mathrm{p,vout}} \cdot \frac{1 + s\,T_{\mathrm{i,vout}}}{s\,T_{\mathrm{i,vout}}} \tag{4.4}$$

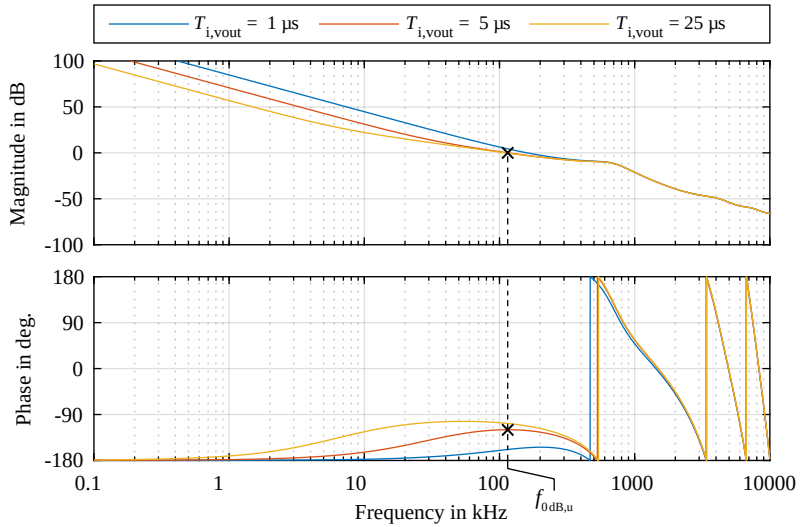


Fig. 4.4: Open-loop Bode plot of the outer voltage controller for $K_{p,vout} = 94.4\,mA/V$ and different values of $T_{i,vout}$. Increasing the integrator time constant $T_{i,vout}$ increases the phase maximum at the cost of slower reaction times of the PI controller's I-component. For a phase margin of $PM_{vout} = 60°$, a time constant of $T_{i,vout} = 5\,\mu s$ at a frequency of $f_{0dB,v} = 115\,kHz$ results.

the expression for the voltage controller's open-loop transfer function directly follows to

$$\underline{G}_{vout,ol}(s) = \underline{G}_{PI,vout}(s)\,\underline{G}_{iL1,cl}(s)\,\frac{1}{sC_{eq}} = \tag{4.5}$$

$$K_{p,vout}\,\frac{1 + s\,T_{i,vout}}{s\,T_{i,vout}} \cdot \frac{1}{sC_{eq}} \cdot \frac{K_{p,iL1}\,e^{-s\,T_{sum}}}{sL_1 + K_{p,iL1}\,e^{-s\,T_{sum}}}. \tag{4.6}$$

There are two parameters to determine in case of the voltage control loop with only the integrator time constant $T_{i,vout}$ having an influence on the open-loop phase. The open-loop phase exhibits a maximum since its value starts at $-180°$ for low frequencies due to the integrating behavior of the capacitor and the I-component of the controller and increases with frequency when the I-component reduces, before dropping once the phase lag of the closed-loop current control loop starts to dominate. This is illustrated in **Fig. 4.4** where the open-loop Bode plot of the voltage control loop is presented for

three different $T_{\mathrm{i,vout}}$ values. Increasing the integrator time constant $T_{\mathrm{i,vout}}$ increases the phase maximum as the I-gain starts do reduce faster already at lower frequency values. Since smaller $T_{\mathrm{i,vout}}$ values are usually favorable as this implies faster integrator actions, $T_{\mathrm{i,vout}}$ is selected to the minimum possible value such that the resulting maximum phase value just guarantees the required phase margin. For a phase margin of $PM_{\mathrm{vout}} = 60°$, a value of $T_{\mathrm{i,vout}} = 5\,\mu\mathrm{s}$ results, leading to a maximum open-loop phase of 120° at $f_{0\mathrm{dB,v}} = 115\,\mathrm{kHz}$. The proportional gain $K_{\mathrm{p,vout}}$ then again follows from requiring unity gain at this frequency, where a value of $K_{\mathrm{p,vout}} = 94.4\,\mathrm{mA/V}$ is found for the case at hand.

4.2.3 Simplified Controller Design Results

Fig. 4.5 presents the resulting closed-loop transfer function of the voltage control loop, together with the according reference step response. Furthermore the results are also compared to the more elaborated model derived in **Section 4.3**. Differences between the two models are especially recognizable at the beginning of the step response as well as for the higher frequency regions of the frequency response.

Although the decoupled model provides some useful insight into the overall system dynamics, there are certain drawbacks which render this approach insufficient for the control design of the UH-PBW amplifier system. Besides the deviations visible in the comparison between the models in **Fig. 4.5**, which are introduced by the simplifications used to decouple the control loops, this is especially caused by the fact that the Bode stability criterion is not applicable in case of active (constant-power) loads which are usually described by a negative small-signal resistance introducing an unstable pole (i.e., a pole in the right half of the s-plane) in the system to be controlled. Furthermore, it is generally not possible to link the requested phase margin values used to determine the control gains in a comprehensible way to more specific and experimentally accessible qualifiers (e.g., overshoot, settling times or bandwidth, amongst others). For this reason, a more elaborated procedure is described in the following section.

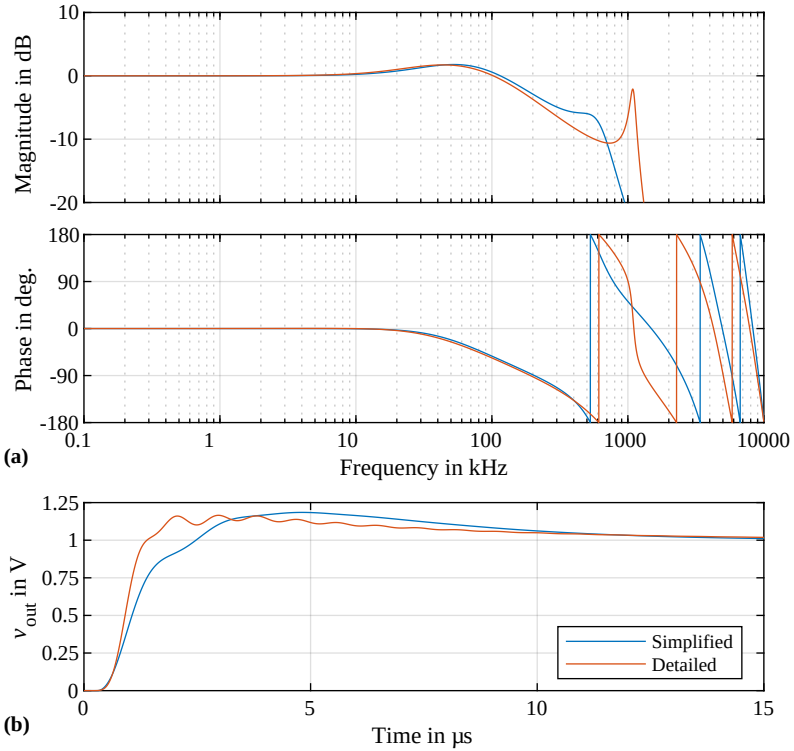


Fig. 4.5: Comparison between simplified and detailed dynamic model. **(a)** Closed-loop Bode plot of the outer voltage controller, **(b)** reference step response.

4.3 Control Optimization Assuming Ideal Modulator

In order to overcome the limitations described in **Section 4.2**, a more elaborated approach based on a numerical controller optimization, similar to the analysis conducted in [97, 253], is presented in this section. The optimization is based on a grid search iteration over all suitable control parameter combinations and selecting the optimal result based on a Pareto optimization of certain selected qualifiers. Additionally, a more accurate description of the dynamic system is introduced first which also considers different load cases in order to avoid the simplifications stated before.

4.3.1 System Modeling

In order to avoid the deviations introduced by the simplifications in **Section 4.2** and to improve the accuracy of the results, a more detailed dynamic model of the control system is required, which is presented in **Fig. 4.6**. Contrary to the section above, the entire two-stage filter is now considered, as well as the load current and reference feedforward paths. In addition, the current and voltage measurements are accounted for by their respective ADC conversion delays and an additional first-order low-pass filter, with the respective transfer functions given by

$$\underline{G}_{\mathrm{m},k} = \frac{1}{1+\frac{s}{\omega_{\mathrm{m},k}}} \cdot \mathrm{e}^{-sT_\mathrm{m}}, \quad k = \{\mathrm{vout}, \mathrm{iout}, \mathrm{iL1}\}, \tag{4.7}$$

where $\omega_{\mathrm{m,iout}} = \omega_{\mathrm{m,iL1}} = 10\,\mathrm{MHz}$, $\omega_{\mathrm{vout}} = 1\,\mathrm{MHz}$ and $T_\mathrm{m} = 50\,\mathrm{ns}$ are assumed for their respective hardware implementations. Additional delay times of $T_\mathrm{P} = T_\mathrm{PI} = 50\,\mathrm{ns}$ arise from the respective pipeline delays of the P and PI controller implementations (cf. **Section 4.5**).

Furthermore, the control structure has been extended by a first-order reference prefilter with transfer function

$$\underline{G}_\mathrm{pre} = \frac{1}{1+sT_\mathrm{pre}}, \tag{4.8}$$

located at the input of the PI output voltage controller. The time constant T_pre of this prefilter introduces an additional degree of freedom, which also has to be considered in the optimization.

Two additional inputs i_load and v_dist have been introduced to model external disturbances. The model input i_load describes disturbances caused by the

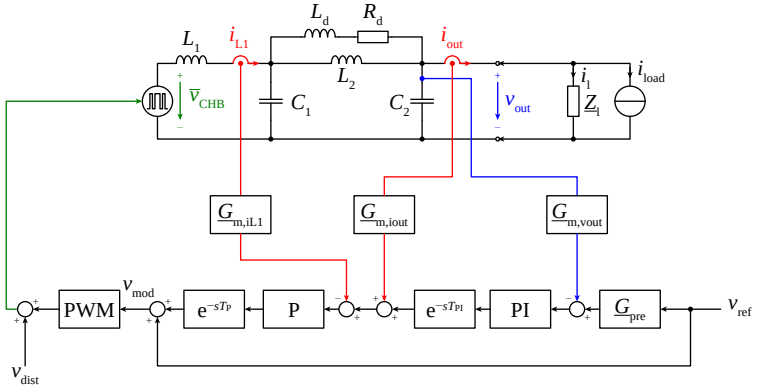


Fig. 4.6: Detailed control model containing the transfer functions of the measurement circuits and the different transport delays distributed between various entities. A first-order low-pass prefilter $\underline{G}_{pre}$ is added into the reference signal of the PI voltage controller, with its according time constant representing an additional degree of freedom for the control parameter optimization. Converter loading is considered by including the load impedance $\underline{Z}_l$, furthermore, two disturbance inputs i_{load} and v_{dist} are added to model external disturbances.

load, such as load steps, by a constant current source connected to the output of the converter, whereas v_{dist} refers to disturbances occurring in the switching stage, e.g., deviations in DC-link voltages or distortions introduced by the interlock delay times of the inverter bridges. These disturbance inputs are later used to introduce according disturbance transfer functions which allow the expression of certain performance metrics that describe the disturbance rejection of the closed-loop control system.

PWM and Power Stage Modeling

The dynamics of the PWM stage including the multi-carrier PWM modulator that generates the gate signals from its respective reference voltage v_{mod} are dominated by its respective transport delay T_{PWM}, which can be separated into a modulator delay and the delay of the power stage switching hardware. For the power stage, a delay time of $T_{\mathrm{FET}} = 150\,\mathrm{ns}$ is assumed, which accounts for the delay time of the inverter bridges and their interlock delay time of 90 ns (cf. **Section 4.5.2**) and additional 60 ns resulting from cumulated transport delay times introduced by several elements in the signal transmission path (e.g., gate drives, digital isolators to overcome potential barriers, LVDS transceivers). Regarding the modulator, two different cases are considered in this chapter, depending on the strategy to update the reference value during each switching frequency period, which is illustrated in **Fig. 4.7**. The two options are referred to in literature [65] as *natural sampling* and *uniform sampling* modulation. In **Fig. 4.7a**, natural sampling of the modulator reference is described. In this case the reference which is compared to the carrier is allowed to continuously change during the switching period and no explicit sampling takes place, which allows immediate reaction of the modulator to a changing reference and eliminates any modulator delay. However, it has to be ensured that each PWM signal switches only once per half-period in order to avoid multiple switching events which would increase the switching frequency (and thereby the switching losses) of the semiconductors. This is accomplished by an additional locking mechanism which locks the state of each half-bridge after a switching event until their carrier reaches top or bottom again. The locking mechanism and its implications on the PWM output signals of the modulator are described in more details in **Section 4.4**.

An alternative is given by uniform sampling illustrated in **Fig. 4.7b**, where the modulator reference is sampled independently by each half-bridge when their respective carrier reaches top or bottom. This inherently avoids the possibility of the reference crossing the carrier more than once per half-period. However, the sampling process introduces an additional sampling delay of

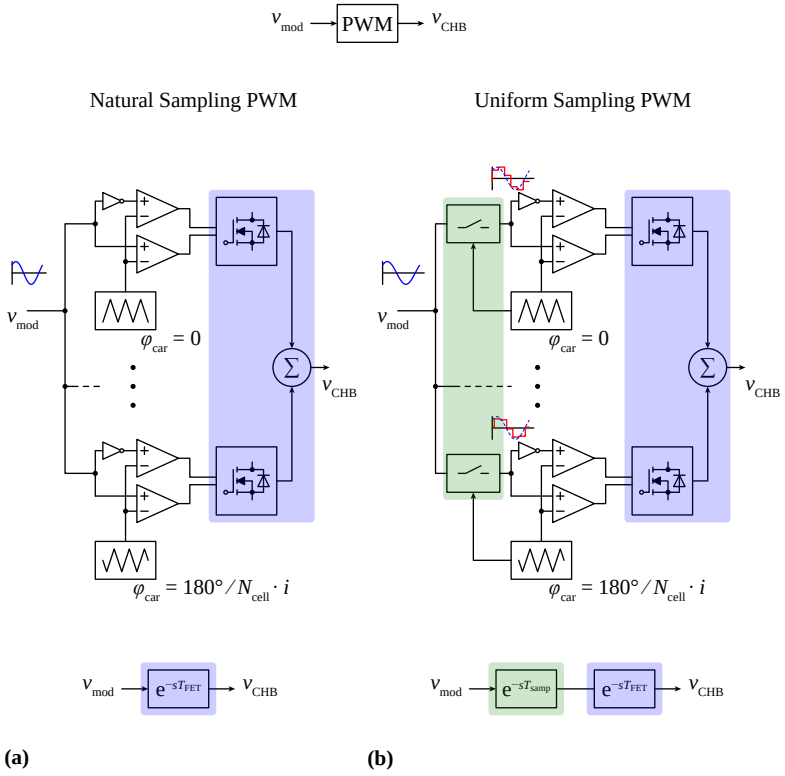


Fig. 4.7: Different possibilities of modulator reference update. **(a)** In case of natural sampling the modulator reference v_{mod} is directly compared to the carrier signal and no explicit sampling takes place. In case of uniform sampling **(b)** a sample-and-hold element is introduced before the comparators of each half-bridge, which samples the modulator reference when the respective triangular carrier reaches top or bottom. The sample-and-hold element introduces a significant delay of $T_{\text{samp}} = 840\,\text{ns}$ (for a sampling frequency of $f_s = 300\,\text{kHz}$) into the modulator. Note that the introduction of the necessary interlock delay time is not explicitly shown in **(a)** but accounted for in the power stage delay time $T_{\text{FET}} = 150\,\text{ns}$.

Tab. 4.1: Converter specifications (repeated as part of **Tab. 3.1**).

Nominal AC power	$P_{\mathrm{nom,AC}}$	10 kW
Nominal DC power	$P_{\mathrm{nom,DC}}$	20 kW
Nominal peak output voltage	$\hat{v}_{\mathrm{out,nom}}$	325 V
Nominal RMS output voltage	$V_{\mathrm{out,nom}}$	230 V
Nominal peak output current	$\hat{i}_{\mathrm{out,nom}}$	61.5 A

$T_{\mathrm{samp}} = \frac{1}{4 f_{\mathrm{s}}}$ with $f_{\mathrm{s}} = 300\,\mathrm{kHz}$ being the switching frequency of each half-bridge. The resulting modulator delay of 840 ns heavily increases the total delay occurring in the system.

Load Models and Considered Load Cases

The load connected to the converter has significant influence on the dynamic model and the resulting closed-loop system dynamics. Consequently, an according load impedance $\underline{Z}_{\mathrm{l}}$ connected to the output of the converter is included in the dynamic model in order to model converter loading. Three exemplary reference scenarios are considered in this optimization:

Passive Load A purely ohmic load is considered in this scenario, where the value of this load resistor is chosen such that the load consumes nominal power at rated voltage. For the according values which are repeated in **Tab. 4.1**, this results in a purely ohmic resistance of $\underline{Z}_{\mathrm{l}} = 5.29\,\Omega$.

No Load The converter operates without load connected to the output, i.e., the terminals are left open. Due to the linear nature of the system, this scenario also corresponds to the case of a constant current load where a current independent of the output voltage flows into the load. A 10 MΩ parallel resistance is used in the numerical calculations as an approximation to guarantee numerical stability.

Active (Constant Power) Load A load consuming a constant power $P_{\mathrm{nom,DC}}$, independent of the output voltage, is considered in this case. The voltage-current-characteristic of such a load in case of DC operation is described by

$$i_{\mathrm{l}} = \frac{P_{\mathrm{nom,DC}}}{v_{\mathrm{out}}} \tag{4.9}$$

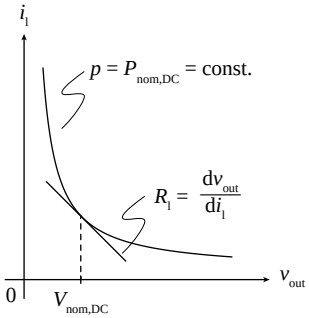


Fig. 4.8: Load characteristic of a constant power load. The linearization of the load characteristic implies a negative small-signal resistance as linear equivalent model.

and illustrated in **Fig. 4.8**. Since this load characteristic is nonlinear, it has to be linearized around a selected operating point, which results in a negative small-signal resistance typically used to describe these loads [254, 255] according to

$$R_l = \frac{dv_{out}}{di_l} = -\frac{V_{nom,DC}^2}{P_{nom,DC}}, \tag{4.10}$$

where a DC output voltage of $V_{nom,DC} = \hat{v}_{out,nom}$ corresponding to the nominal peak output voltage is considered as operating point. Consequently a negative, ohmic small-signal resistance of $\underline{Z}_l = R_l = -5.29\,\Omega$ follows for the nominal values given in **Tab. 4.1** (i.e., a constant-power load consuming nominal power).

A negative small-signal resistance introduces an unstable pole in the open-loop filter transfer function (without the controller involved) which destabilizes the system. For this reason, it is expected that the appearance of active loads degrades the achievable dynamic performance as the available set of valid control parameters may face stricter limitations to guarantee stability.

4.3.2 Optimization Algorithm, Boundary Conditions and Performance Qualifiers

The optimization algorithm is based on a grid search iteration over a certain range of control parameter combinations and selecting the most suitable

result from all possible combinations. For this reason, a set of performance qualifiers, which allow to assess the dynamic performance of different results, is required. These performance metrics are based on three transfer functions $\underline{G}_{\text{ref}}$, $\underline{G}_{\text{load}}$ and $\underline{G}_{\text{dist}}$ where the reference transfer function,

$$\underline{G}_{\text{ref}} = \frac{\hat{v}_{\text{out}}}{\hat{v}_{\text{ref}}}, \tag{4.11}$$

relates the reference input to the output voltage, the load transfer function,

$$\underline{G}_{\text{load}} = \frac{\hat{v}_{\text{out}}}{\hat{i}_{\text{load}}} = -\underline{Z}_{\text{out}}, \tag{4.12}$$

describes the dependency between output voltage and load current (also referred to as the converter's negative output impedance $\underline{Z}_{\text{out}}$) and

$$\underline{G}_{\text{dist}} = \frac{\hat{v}_{\text{out}}}{\hat{v}_{\text{dist}}} \tag{4.13}$$

corresponds to the transfer function from a disturbance injected in the switching stage. The latter is used to model disturbances which originate in the modulator itself, e.g., distortions due to interlock delays or deviations in the cell's DC-link voltages.

The following list defines the qualifiers used in this optimization, many of which have already been introduced with similar or identical definitions in literature [97, 253]:

- One of the most important performance metrics for a high performance power source is its small-signal −3 dB bandwidth, which is defined as the lowest frequency for which the reference transfer function $\underline{G}_{\text{ref}}$ drops below −3 dB. Since the achievable bandwidth depends on the load connected to the system, the obtained bandwidths in case of the passive load scenario, referred to as $f_{\text{bw,l}}$, are taken as a reference case to compare different sets of control parameters.

- In order to characterize the controller's reaction on disturbances, the maximum voltage dip v_{dip} caused by a load current step with an amplitude of 1 A, where the unloaded load scenario is taken as reference case, is considered. This is illustrated in **Fig. 4.9** where the typical waveform of the output voltage in case of a load step together with the definition of v_{dip} is presented.

- Furthermore, two quantities referred to as *error integrals* are introduced according to

$$E_{\mathrm{ref},k} = \int_0^{T_{\mathrm{set,ref},k}} t\,|v_{\mathrm{out}} - v_{\mathrm{ref}}|\,\mathrm{d}t, \tag{4.14}$$

$$E_{\mathrm{load},k} = \int_0^{T_{\mathrm{set,load},k}} t\,|v_{\mathrm{out}} - v_{\mathrm{ref}}|\,\mathrm{d}t, \tag{4.15}$$

which quantify the time-weighted absolute value of the deviation between output voltage and reference after a reference step or a load current step, respectively (cf. **Fig. 4.9**). They are also referred to in literature as "integral of time-weighted absolute error (ITAE)" and suggested as cost functions for control optimizations [53, 225]. The index $k = \{\text{passive, no-load, active}\}$ denotes the considered load case. The integration boundaries in the above expressions are given by the settling times $T_{\mathrm{set,ref},k}$ and $T_{\mathrm{set,load},k}$, which are defined as the time the controller requires to stabilize the output voltage within a band of ±0.5 % around the desired reference value after the corresponding reference step or load step. In case of $T_{\mathrm{set,ref},k}$ this definition is independent of the reference step amplitude due to the linearity of the system. In case of a load step, the settling time depends on the load current step amplitude and the reference voltage. For the case at hand, a reference voltage of $10\,\% \cdot \hat{v}_{\mathrm{out,nom}} = 32.5\,\mathrm{V}$ and a load step of $1/2 \cdot \hat{i}_{\mathrm{out,nom}} = 30.8\,\mathrm{A}$ was selected, where the comparably low reference voltage was selected such that the limitation of the $T_{\mathrm{set,load},k}$ introduced later ensures a tight control of the output voltage during load transients also for operation with low reference voltages. $T_{\mathrm{set,load},k}$ is then again defined as the time it takes the controller to stabilize the voltage within ±0.5 % around the reference. The same conditions (i.e., the same reference and load step amplitude) are also applied to evaluate the disturbance error integrals $E_{\mathrm{load},k}$ and (same reference amplitude) $E_{\mathrm{ref},k}$. **Fig. 4.9** illustrates the integration areas together with the according settling times for both step responses.

Since the aforementioned integrals also depend on the considered load of the system, the average value over the three reference load cases is

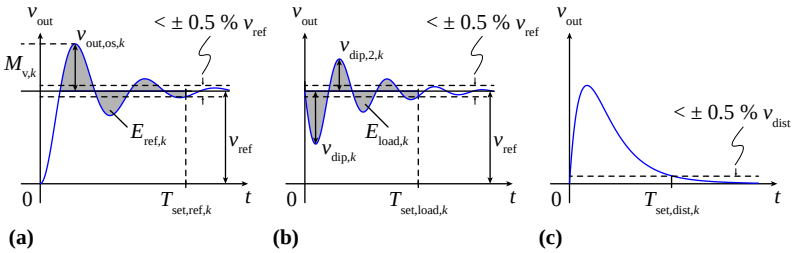


Fig. 4.9: Characteristic step responses for **(a)** the reference transfer function $\underline{G}_{\text{ref}}$, **(b)** the load disturbance transfer function $\underline{G}_{\text{load}}$ and **(c)** the disturbance transfer function $\underline{G}_{\text{dist}}$. The according settling times are defined as the time the controller requires to stabilize the output voltage within a band of $\pm 0.5\,\%$ around the desired value for the respective input. In case of $T_{\text{set,ref},k}$, this definition is independent of the input v_{ref}, whereas in case of $T_{\text{set,load},k}$, a reference of $v_{\text{ref}} = 32.5\,\text{V}$ and a load step amplitude of $i_{\text{load}} = 30.8\,\text{A}$ is assumed. Similarly, the settling time $T_{\text{set,dist},k}$ is defined as the time it takes the controller to suppress a step in the disturbance voltage v_{dist} to less than $0.5\,\%$ of its value considering $v_{\text{ref}} = 0$ (although this definition is again independent of the reference input due to the linearity of the system). The relevant integration area for the error integrals $E_{\text{ref},k}$ and $E_{\text{load},k}$ is highlighted in gray. The index $k = \{\text{passive, no-load, active}\}$ denotes the considered load case as the dynamic properties of the converter depend on the converter load.

introduced as a superordinate performance metric:

$$E_{\mathrm{ref}} = \frac{1}{3}\left(E_{\mathrm{ref,passive}} + E_{\mathrm{ref,no\text{-}load}} + E_{\mathrm{ref,active}}\right), \tag{4.16}$$

$$E_{\mathrm{load}} = \frac{1}{3}\left(E_{\mathrm{load,passive}} + E_{\mathrm{load,no\text{-}load}} + E_{\mathrm{load,active}}\right), \tag{4.17}$$

which is used to assess the combined dynamic performance of the control system over all considered load cases.

In addition, certain boundary conditions are applied which are used to immediately sort out unreasonable designs from the design space. Besides being a stable system, all valid designs have to fulfill the following conditions for all considered load cases:

- For a reference step, a maximum relative overshoot $M_{\mathrm{v},k}$

$$M_{\mathrm{v},k} = \frac{v_{\mathrm{out,os},k}}{v_{\mathrm{ref}}} \tag{4.18}$$

with $v_{\mathrm{out,os},k}$ being the peak voltage following a reference step and v_{ref} being the reference step amplitude (cf. **Fig. 4.9a**) is limited to $M_{\mathrm{v},k} < 10\,\%$ to avoid excessive overvoltage at the converter output during transients.

- A similar criterion is defined for the load current step response and illustrated in **Fig. 4.9**, where the ratio

$$M_{\mathrm{i},k} = \left|\frac{v_{\mathrm{dip},2,k}}{v_{\mathrm{dip},k}}\right| \tag{4.19}$$

between the highest overshoot following a load step and the initial voltage dip is limited to $M_{\mathrm{i},k} < 20\,\%$ to avoid excessive overshoot in case of a load transient.

- The settling times $T_{\mathrm{set,ref},k}$ and $T_{\mathrm{set,load},k}$ are limited to $T_{\mathrm{set,ref},k} < 100\,\mu\mathrm{s}$ and $T_{\mathrm{set,load},k} < 100\,\mu\mathrm{s}$.

- The settling times $T_{\mathrm{set,dist},k}$ (cf. **Fig. 4.9c**) are limited to $T_{\mathrm{set,dist},k} < 200\,\mu\mathrm{s}$ for all three load cases, where $T_{\mathrm{set,dist},k}$ is defined as the settling time of the disturbance transfer function $\underline{G}_{\mathrm{dist}}$, i.e., the time it takes the control to eliminate a step in the disturbance voltage to less than $0.5\,\%$ of its value at the system output.

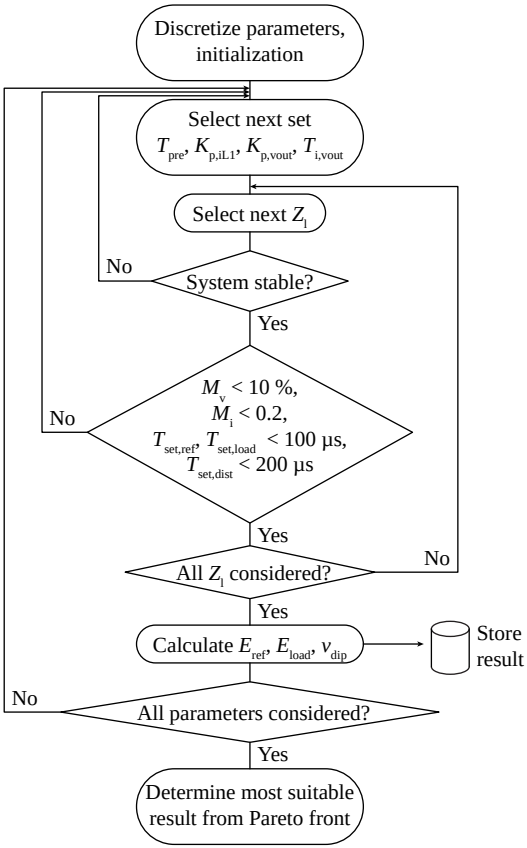


Fig. 4.10: Grid search algorithm implemented to determine an optimal set of control parameters.

Control parameter sets which violate one of the listed constraints for any of the considered load scenarios are considered invalid and excluded from the optimization.

A flowchart of the employed grid search optimization algorithm is presented in **Fig. 4.10**. The procedure starts with the discretization of the parameter ranges of the four control parameters T_{pre}, $K_{\mathrm{p,iL1}}$, $K_{\mathrm{p,vout}}$ and $T_{\mathrm{i,vout}}$, where the following discrete values were used:

$$T_{\mathrm{pre}} = \left\{0\,, 50\,\mathrm{ns} \cdot 10^{\frac{2i}{39}}\right\} \quad 0 \leq i \leq 39, \quad i \in \mathbb{N}, \tag{4.20}$$

$$K_{\mathrm{p,iL1}} = 0.5\,\mathrm{V/A} \cdot 10^{\frac{\log_{10}(80)\,i}{99}}, \quad 0 \leq i \leq 99, \quad i \in \mathbb{N}, \tag{4.21}$$

$$K_{\mathrm{p,vout}} = 0.1\,\mathrm{mA/V} \cdot 10^{\frac{\log_{10}(1500)\,i}{149}}, \quad 0 \leq i \leq 149, \quad i \in \mathbb{N}, \tag{4.22}$$

$$T_{\mathrm{i,vout}} = 100\,\mathrm{ns} \cdot 10^{\frac{3i}{29}}, \quad 0 \leq i \leq 29, \quad i \in \mathbb{N}. \tag{4.23}$$

These originate from a logarithmic distribution of the control parameters between 0 and 5 µs for T_{pre}, 0.5 V/A and 40 V/A for $K_{\mathrm{p,iL1}}$, 0.1 mA/V and 150 mA/V for $K_{\mathrm{p,vout}}$ and 0.1 µs and 100 µs for $T_{\mathrm{i,vout}}$. After initialization the algorithm iterates through all possible combinations of the four control parameters. For each combination, an inner loop over the considered load cases is carried out to verify whether the resulting system is stable and whether the boundary conditions stated above are met. If these conditions are fulfilled, the program calculates the performance qualifiers listed above and then continues with the next parameter set. Once all possible combinations of parameters have been considered, the program terminates.

Since two different possibilities regarding the implementation of the modulator are considered, the algorithm was executed twice, once with natural sampling and once with uniform sampling being considered for the PWM modulator. The output of the algorithm is a large set of possible control system parameter combinations for each case, from which the optimal design has to be selected. To accomplish this, a Pareto approach is introduced in the next section which allows to assess the tradeoffs between different performance metrics and ultimately to identify the most suitable design.

4.3.3 Optimization Results

The results generated by the grid search algorithm described in the section before are analyzed using Pareto plots, which allow to visualize different design tradeoffs between performance qualifiers and to identify performance boundaries and according Pareto-optimal designs. Furthermore, the influence

of the modulation strategy can be investigated by comparing the resulting performance spaces obtained for natural and uniform sampling PWM modulation.

However, as a first result it is found that the resulting performance space for uniform sampling modulation is empty, i.e., the algorithm was not able to find any valid design. This is also the case if all boundary conditions from **Section 4.3.2**, except stability, are omitted, which indicates that with the large delay introduced by the reference sampling in the modulator it is not possible to stabilize the unstable pole introduced by a constant power load in the filter transfer function. Since it is expected that the active load scenario heavily shrinks the design space, the algorithm was also executed with only the passive and no load cases considered, i.e., for a system which is not intended to operate with active loads. Although the procedure finds designs which are stable in this case, all of these control sets violate the remaining boundary conditions, mainly the applied overshoot limitations for $M_{\mathrm{v},k}$ and $M_{\mathrm{i},k}$. Similar results were also obtained if the delay compensation mechanism introduced in **Section 4.3.4** was considered in an attempt to mitigate the impact of the system's transport delay times. For this reason, uniform sampling modulation is considered infeasible for the intended high performance application, regardless of whether a delay predictor is used or not.

The obtained performance spaces for natural sampling modulation are illustrated in **Fig. 4.11**, where each data point corresponds to a control system characterized by the resulting loaded bandwidth $f_{\mathrm{bw,l}}$ and its average reference error integral E_{ref}. Different colors are used to either indicate the according average load step error integral E_{load} in **Fig. 4.11a** or the maximum voltage dip v_{dip} in **Fig. 4.11b**.

From **Fig. 4.11** it can be recognized that the reference error integral E_{ref} exhibits a minimum value at a design bandwidth $f_{\mathrm{bw,l,e_{min}}} = 36\,\mathrm{kHz}$ which separates the performance space into two regions $f_{\mathrm{bw,l}} < f_{\mathrm{bw,l,e_{min}}}$ and $f_{\mathrm{bw,l}} > f_{\mathrm{bw,l,e_{min}}}$. For $f_{\mathrm{bw,l}} < f_{\mathrm{bw,l,e_{min}}}$ the minimum possible reference error integral E_{ref} reduces with increasing bandwidth since the higher bandwidth enables a faster response of the system in reaching the desired output voltage, thereby reducing the error voltage time area present at the output. On the lower side, i.e., towards smaller E_{ref} values, this region is limited by the M_{i} constraint (ratio between overshoot following a load step and initial voltage dip) which results from the observation that in general, designs with a small bandwidth exhibit large prefilter time constants T_{pre} and low $K_{\mathrm{p,vout}}$ gains, thereby enabling higher $K_{\mathrm{p,iL1}}$ gains while still maintaining acceptable

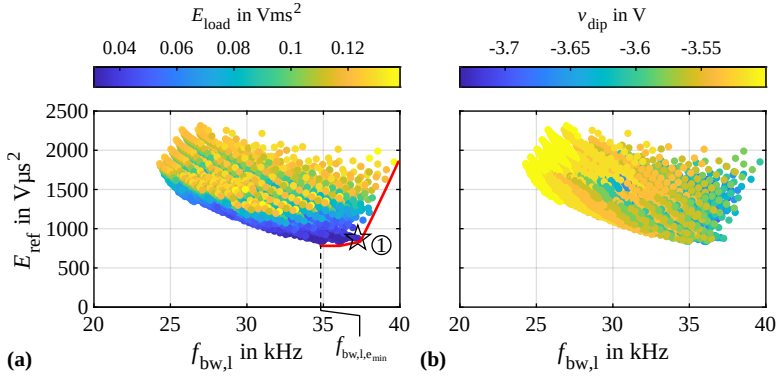


Fig. 4.11: Results of the grid search algorithm illustrated as $f_{\mathrm{bw,l}}$-E_{ref} Pareto plots with **(a)** the value of the error integral E_{load} and **(b)** the maximum voltage dip v_{dip} given on the color scale. Suitable designs can be identified on the Pareto front indicated in red in **(a)**, i.e., for high bandwidths and low error integrals E_{ref} and E_{load}, with the selected design being labeled as ①. The voltage dip v_{dip} exhibits only a weak dependency on the control parameters for the considered valid designs.

$M_{\mathrm{v},k}$ overshoot values until the $M_{\mathrm{i},k}$ limit is reached. For bandwidths above $f_{\mathrm{bw,l,e_{min}}}$ an increase of the minimum achievable E_{ref} with increasing control bandwidth is observed, which results from the higher overshoot values $M_{\mathrm{v},k}$ and according longer settling time values that these designs exhibit due to the higher bandwidth up to the point where the designs are excluded due to violating the $M_{\mathrm{v},k}$ overshoot limits. This introduces the Pareto boundary clearly recognizable at the lower right edge of the performance space as the aim is to maximize bandwidth and minimize error integrals at the same time. Similar effects are also recognized for the disturbance error integral E_{load} which is illustrated on the color scale of **Fig. 4.11a**. In addition, the maximum voltage dip v_{dip} is presented in **Fig. 4.11b**. It is found that the dependency of v_{dip} from the control parameters is only minor as maximum and minimum values of v_{dip} differ by only $\approx 7\,\%$ over the entire performance space. This indicates that the maximum voltage dip is mainly determined by the filter elements alone.

On the upper side of the performance space, i.e., for higher E_{ref} values, the performance space is limited by the settling times as well as the $M_{\mathrm{v},k}$ and $M_{\mathrm{i},k}$ boundaries. Designs located there represent non-optimal controllers since they represent systems which exhibit higher error integrals than what

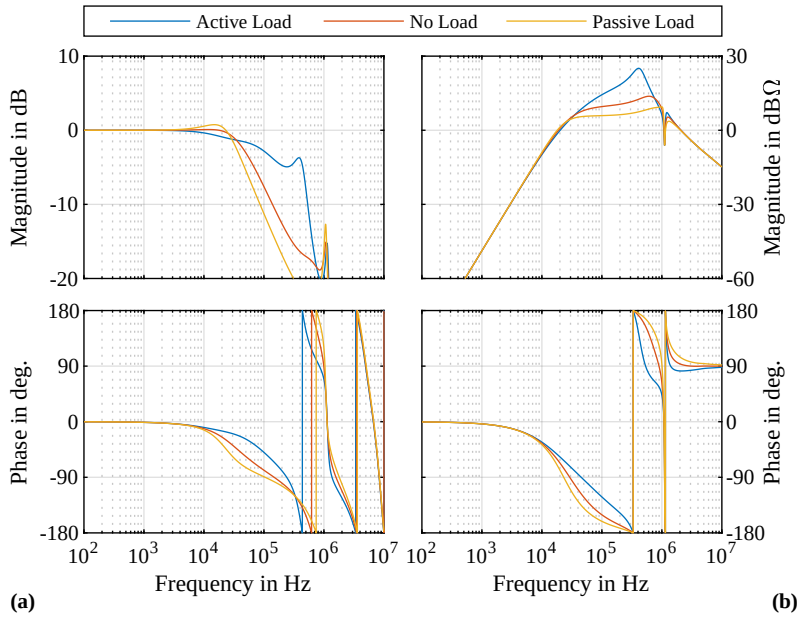


Fig. 4.12: Bode plots of the **(a)** reference transfer function and **(b)** the load disturbance transfer function for for the control parameters listed in **Tab. 4.2**, corresponding to design ① in **Fig. 4.11**.

could be obtained for the same bandwidth or that combine several undesirable properties (e.g., excessive overshoot with low bandwidth).

From the Pareto front the most suitable controller can finally be selected, where a reasonable tradeoff between error integrals and loaded bandwidth has to be identified. For the case at hand, the data point labeled as ① and highlighted in **Fig. 4.11a** featuring a loaded bandwidth of $f_{\mathrm{bw,l}} = 37\,\mathrm{kHz}$ was considered a reasonable compromise since due to the steep slope of the Pareto boundary, designs located at higher $f_{\mathrm{bw,l}}$ values only enable minor improvements in bandwidth while exhibiting considerably higher error integrals; e.g., the design maximizing the bandwidth only provides an increase in bandwidth of ca. 2.2 kHz (less than 10 %) while the according error integral E_{ref} doubles. The resulting control parameters are summarized in **Tab. 4.2**, with the according Bode plots and step responses of the corresponding system given in **Fig. 4.12** and **Fig. 4.13**, respectively.

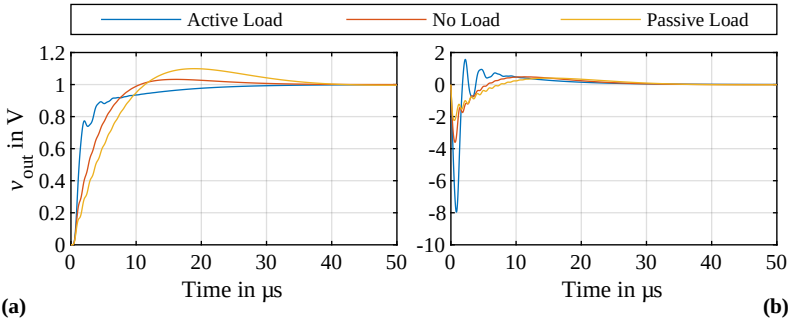


Fig. 4.13: (a) Reference step response and **(b)** load step response of the system for the control parameters listed in **Tab. 4.2**, corresponding to design ① in **Fig. 4.11**.

Parameter	Value
T_{pre}	3.12 µs
$K_{\text{p,iL1}}$	28.1 V/A
$K_{\text{p,vout}}$	9.6 mA/V
$T_{\text{i,vout}}$	2.2 µs
$f_{\text{bw,l}}$	37 kHz
E_{ref}	878 V µs^2
E_{load}	0.035 V ms^2
v_{dip}	−3.6 V

Tab. 4.2: Optimal control parameters and key performance metrics identified from the Pareto front in **Fig. 4.11**, corresponding to design ①.

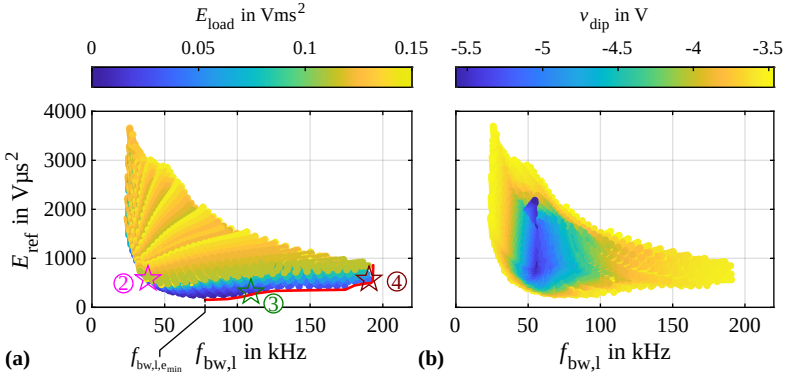


Fig. 4.14: Results of the grid search algorithm if no active loads are considered, illustrated as $f_{bw,l}$-E_{ref} Pareto plots with **(a)** the value of the error integral E_{load} and **(b)** the maximum voltage dip v_{dip} given on the color scale. Similarly to the results with active loads included, suitable designs can be identified on the Pareto front indicated in red in **(a)**, i.e., for high bandwidths and low error integrals E_{ref} and E_{load}. Three designs highlighted as ②, ③ and ④ are considered as examples to further illustrate this dependency in **Fig. 4.15**. Since the increase of E_{ref} with bandwidth is only minor, the design marked as ④ maximizing the control bandwidth is selected as optimal design. In case of the maximum voltage dip v_{dip}, similar values as in the case where active loads were also considered are obtained for designs located on the Pareto front. Designs with higher voltage dips of up to −5.5 V are also found in this scenario, which, however, are located further away from the Pareto front and therefore are not relevant for the selection of an optimal controller. It has to be noted that in the respective area where designs with higher voltage dip values are found (blue region in **(b)**), also many designs featuring similar v_{dip} values as the designs located on the Pareto front are found. However, these are masked by the data points with higher values of the voltage dip and are therefore not visible in **(b)**.

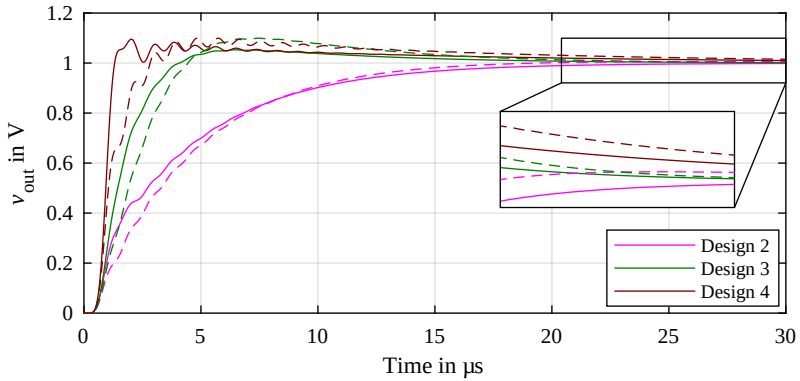


Fig. 4.15: Comparison of the step responses for the designs ②, ③ and ④ highlighted in **Fig. 4.14**. Solid lines: unloaded case, dashed lines: passive load with nominal value according to Tab 4.1. The higher value of the error integral E_{ref} of design ④ over design ③ originates from the higher settling times.

In order to investigate the restrictions which are introduced by demanding the system to operate with active loads, the optimization was also executed without considering constant power loads, i.e., only the passive and no-load scenarios were kept. The according results are presented in **Fig. 4.14a** and **4.14b**. While the basic relations described for the case including active loads are still valid, it can be recognized that the achieved bandwidth $f_{\mathrm{bw,1}}$ of the system is heavily increased by more than a factor of four which mainly results from the significantly higher $K_{\mathrm{p,vout}}$ obtained in this scenario. Again, the performance space exhibits a minimum E_{ref} at a system bandwidth $f_{\mathrm{bw,1,e_{min}}} = 77\,\mathrm{kHz}$ up to which an increase in bandwidth enables a reduction in error integral E_{ref}. A further bandwidth increase above this point leads to an increase in E_{ref} as this is accompanied by higher overshoot and longer settling time values, although this increase is only minor compared to the results from **Fig. 4.11**. This is illustrated in **Fig. 4.15**, where the reference step response plots for the three control designs ②, ③ and ④ highlighted in **Fig 4.14** are compared. Regarding the maximum voltage dip v_{dip}, it is found that designs located on the Pareto front exhibit similar values of ca. $-3.5\,\mathrm{V}$ as in the case where active loads are also considered. Contrary to the case where active loads were included, designs with higher voltage dips of up to $-5.5\,\mathrm{V}$ are also found in this scenario, which, however, are located further away from the Pareto front in **Fig. 4.14b** and therefore are not relevant for

Parameter	Value
T_{pre}	80 ns
$K_{\mathrm{p,iL1}}$	32.1 V/A
$K_{\mathrm{p,vout}}$	106 mA/V
$T_{\mathrm{i,vout}}$	11.7 µs
$f_{\mathrm{bw,l}}$	191 kHz
E_{ref}	567 V µs^2
E_{load}	0.04 V ms^2
v_{dip}	−3.53 V

Tab. 4.3: Optimal control parameters and key performance metrics identified from the Pareto front in **Fig. 4.14** (no active loads considered), corresponding to design ④.

the selection of an optimal controller. Similar to the scenario above, a suitable controller is selected from the Pareto front in **Fig. 4.14**, where in this case design ④ almost maximizing the bandwidth is considered appropriate as the error integrals exhibit only a minor increase with frequency. **Fig. 4.16** and **Fig. 4.17** present the Bode and step response plots for the resulting system. The according control gains are listed in **Tab. 4.3**, together with additional values of certain performance qualifiers.

For the hardware implementation of the amplifier system, the control parameters from **Tab. 4.3**, corresponding to the optimization without active loads considered, were finally selected, mainly since the much higher bandwidth enables to verify that the CHB topology is capable of generating such high frequency waveforms at a high power level. Furthermore, this also heavily simplifies experimental verification as no active load is required for verification. Since constant power loads are usually power converters with their own control system, experimental verification would require a load converter with a significantly higher bandwidth than the investigated system in order to verify active load operation over the entire bandwidth.

4.3.4 Delay Compensation

Since the transport delay times of the system are expected to have a significant influence on the achievable performance of the controller, which is already indicted by the observation that with the uniform sampling modulator no valid control design could be found, the implementation of a delay predictor

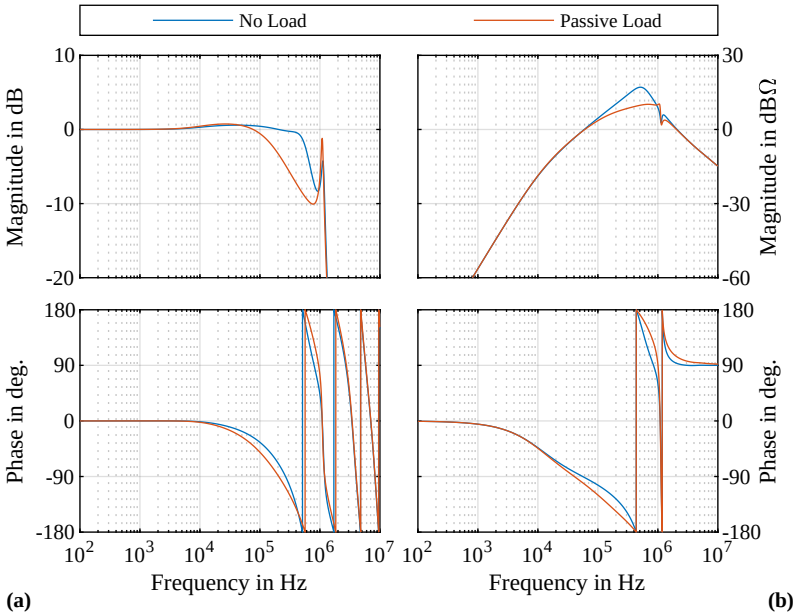


Fig. 4.16: Bode plots of the **(a)** reference transfer function and **(b)** load disturbance transfer function for the control parameters listed in Tab 4.3, corresponding to design ④ in **Fig. 4.14**. A peak in the reference transfer function at 1 MHz can be observed, which corresponds to the upper corner frequency of the output filter and suggests to improve the damping element L_d, R_d (cf. **Fig. 3.20**) in order to provide a better attenuation of this resonance frequency.

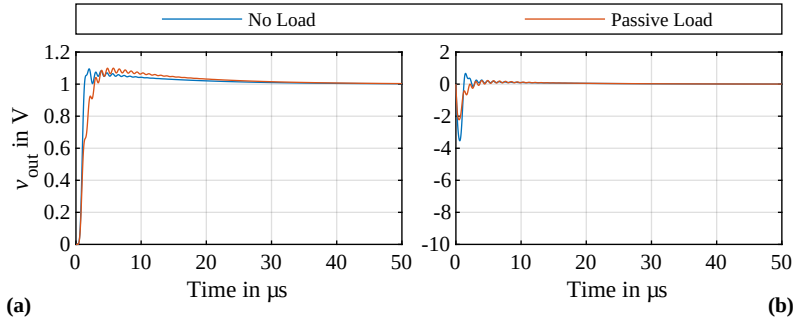


Fig. 4.17: (a) Reference step response and **(b)** load step response of the converter for the control parameters listed in **Tab. 4.3**, corresponding to design ④ in **Fig. 4.14**.

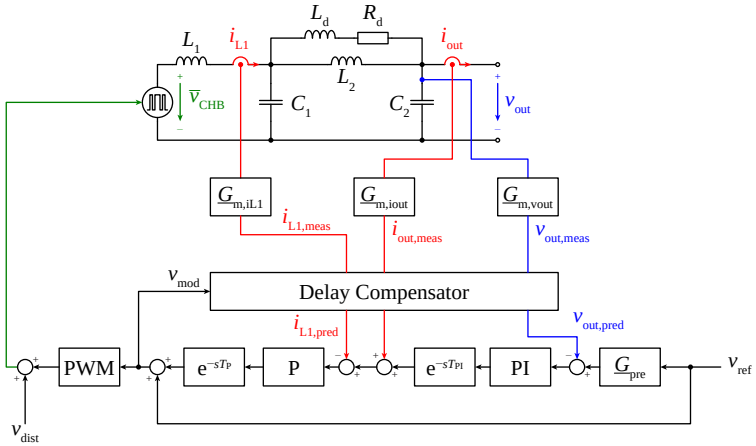


Fig. 4.18: Resulting control block diagram if delay compensation according to [97] is included in the controller. The delay compensator implements a discretized model of the filter's differential equations to predict the values of the measured filter current i_{L1} and the output voltage v_{out}.

suggested in [97] based on the approach in [256] was considered, which is briefly described in the following. **Fig. 4.18** illustrates the arrangement of this compensator unit, which is introduced after the digitization of the measurements and before the measured quantities are fed into the actual controller. The prediction algorithm is based on a discretized model of the filter differential equations and attempts to calculate the resulting inductor current i_{L1} and output voltage v_{out} ahead in time, i.e., to predict the actual values of these quantities present in the system once the entire delay times in the control loop have passed. In this way, the controller's reaction is based on an estimation of the respective quantities present in the system at the time instance where the controller's response becomes physically active on the filter input instead of the measured data samples that represent delayed data once the controller's reaction has propagated through the system. It has to be noted that prediction is only possible for the filter quantities i_{L1} and v_{out} since prediction of the load current i_{L1} would require additional information about the connected load in order to implement a load model.

The derivation of the according equations for the delay compensator can be found in [48] and results in the following linear relations between

Tab. 4.4: Coefficients of the delay compensator.

$k_{c,1}$	$\frac{T_{pred,i}}{L_1}$
$k_{c,2}$	$-\frac{T_{pred,i}}{L_1}$
$k_{c,3}$	$1-\frac{T_{pred,i}^2}{4L_1(C_1+C_2)}$
$k_{c,4}$	$\frac{T_{pred,i}^2}{4L_1(C_1+C_2)}$
$k_{c,5}$	$\frac{T_{pred,v}^2}{4L_1(C_1+C_2)}$
$k_{c,6}$	$1-\frac{T_{pred,v}^2}{4L_1(C_1+C_2)}$
$k_{c,7}$	$\frac{T_{pred,v}}{C_1+C_2}$
$k_{c,8}$	$-\frac{T_{pred,v}}{C_1+C_2}$

the measured samples $v_{out,meas}$, $i_{L1,meas}$ and $i_{out,meas}$ and the predicted values $v_{out,pred}$, $i_{L1,pred}$:

$$\begin{aligned} i_{L1,pred} &= k_{c,1}\, v_{mod} + k_{c,2}\, v_{out,meas} + k_{c,3}\, i_{L1,meas} + k_{c,4}\, i_{out,meas}, \\ v_{out,pred} &= k_{c,5}\, v_{mod} + k_{c,6}\, v_{out,meas} + k_{c,7}\, i_{L1,meas} + k_{c,8}\, i_{out,meas}, \end{aligned} \tag{4.24}$$

with the according coefficients listed in **Tab. 4.4** and v_{mod} being the setpoint voltage of the modulator which is fed back from the output of the controller to the delay compensator. The prediction horizon T_{pred} is determined by the sum of the delay times in the according control loop and differs between voltage and current predictor:

$$T_{pred,i} = T_m + T_{PWM} + T_P \tag{4.25}$$

$$T_{pred,v} = T_m + T_{PWM} + T_P + T_{PI} \tag{4.26}$$

since for the current control loop only the inner P current controller has to be considered while the voltage control loop also contains the outer PI voltage controller.

According results of the grid search algorithm of the control parameters for the system with uniform sampling PWM modulation including delay compensation again result in empty performance spaces, i.e., the delay compensator is not able to sufficiently improve the dynamics of the system. In case of natural sampling modulation, the resulting Pareto plots given in **Fig. 4.19** are obtained if the scenario without active loads being considered is taken as an exemplary case. From **Fig. 4.19** it can be recognized that if the compensation mechanism is included the Pareto front moves towards smaller values of

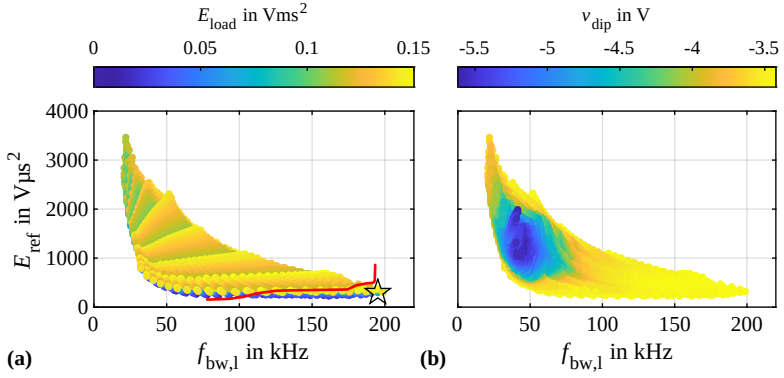


Fig. 4.19: Results of the grid search algorithm if delay compensation is used, again with the load step error integral E_{load} **(a)** and the voltage dip v_{dip} **(b)** indicated on the color axis. No active loading of the converter is considered. The Pareto front from **Fig. 4.14a** is included in **(a)** for comparison, indicating that a small improvement regarding the reference error integral E_{ref} is obtained. The achieved maximum bandwidth is almost the same in both cases.

the reference error integrals E_{ref} compared to the case without compensation, while only a minor performance increase in bandwidth is obtained as the achieved bandwidths are almost identical. Additionally, the designs providing higher bandwidths than what was accomplished without the compensator generally exhibit higher load disturbance error integral values E_{load}. Furthermore, it was found that if active loads are also considered for converter loading, the achievable bandwidth was reduced, i.e., the delay compensator degrades the achievable output bandwidth.

An additional aspect that has to be considered if the delay compensator is used results from the fact that the voltage controller's reaction is based on the predicted value instead of the measured value alone. As a consequence, steady-state deviations occurring in the converter hardware, e.g., the offset errors of the current sensors, can lead to DC offset errors of the converter output voltage despite the integrating behavior of the output voltage controller usually intended to eliminate these deviations. This is illustrated on the exemplary case of unloaded converter operation with a DC setpoint voltage of $v_{ref} = 0\,\mathrm{V}$, where an offset error in the load current sensor of $\Delta i_{err} = 100\,\mathrm{mA}$ is assumed. Since steady-state operation with DC is considered, the integrating behavior of the PI voltage controller forces the respective input of

the controller, which corresponds to the deviation between v_{ref} and $v_{\mathrm{out,pred}}$, to zero, i.e., $v_{\mathrm{ref}} = v_{\mathrm{out,pred}} = 0$. Considering (4.24) and the fact that during unloaded DC operation the filter current i_{L1} as well as the load current i_{out} are zero, this results in

$$0 = v_{\mathrm{out,pred}} = k_{\mathrm{c},5}\, v_{\mathrm{mod}} + k_{\mathrm{c},6}\, v_{\mathrm{out}} + k_{\mathrm{c},8}\, \Delta i_{\mathrm{err}}. \tag{4.27}$$

Furthermore, $v_{\mathrm{out}} = v_{\mathrm{mod}}$ holds since the modulator delay as well as the filter transfer function approach unity for DC operation. Consequently, the above equation can be rearranged to

$$v_{\mathrm{out}} = -\frac{k_{\mathrm{c},8}\, \Delta i_{\mathrm{err}}}{k_{\mathrm{c},5} + k_{\mathrm{c},6}} = -k_{\mathrm{c},8}\, \Delta i_{\mathrm{err}} = -217\,\mathrm{mV}, \tag{4.28}$$

i.e., the offset error of the current sensor results in an offset voltage error at the converter output despite the integrating behavior of the output voltage controller. Although the resulting offset voltage for the considered example is comparably small, the above example indicates that the delay compensation mechanism degrades the system's reaction to disturbances.

A more detailed investigation on the influence of the delay compensation on the performance of the converter and how to overcome the stated difficulties exceeds the scope of this optimization and is subject to future work. For the hardware implementation of the prototype system, the delay compensator was not further considered, mainly due to the additional implementation effort and since, depending on the considered load cases, only a minor increase or even a reduction of the maximum bandwidth is achieved while increasing the sensitivity of the system to steady-state deviations.

4.4 Impact of Continuous Locking Modulator

4.4.1 Modulator Locking Mechanism

So far it was assumed that the PWM modulator of the converter behaves in a linear manner, i.e., the PWM stage could be described by a linear equivalent voltage source which only exhibits a transport delay T_{PWM}. This enables the usual design methods for linear control systems to be applied as it is expected that the frequency components fed into the modulator input are reflected at the modulator output without any distortion as long as their frequency is sufficiently lower than the switching frequency of the carriers. However, in a real world implementation the modulator introduces significant nonlinear

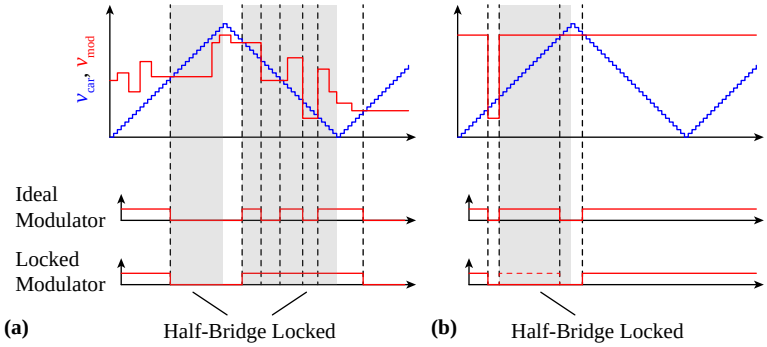


Fig. 4.20: Modulator locking illustrated on the example of a single half-bridge with carrier v_{car} and two different modulator reference signals v_{mod}. In **(a)**, a waveform crossing the carrier at several time instances is presented. The locking mechanism prevents any change in the output signal after the first carrier crossing of the reference until the carrier reaches its top or bottom value, where the bridge is unlocked again. **(b)** Example of a short input pulse being heavily distorted into a pulse with a considerably longer duration by the locking mechanism.

behavior which is immediately seen from the additional switching frequency components which appear at the power stage output. Besides the switching frequency components, the locking mechanism implemented to prevent multiple switching of the PWM stage within a single carrier period (which could otherwise occur for natural sampling) introduces an additional nonlinear effect which significantly affects the dynamic behavior of the converter.

The locking mechanism of the natural sampled PWM modulator is illustrated in **Fig. 4.20** on the example of a single half-bridge of the CHB converter. Since no explicit sampling of the modulator reference is applied in case of the natural sampled modulator, the reference value can continuously change during the PWM period and could cross the carrier more than once, where in an ideal modulator each of these transitions would imply a switching event of the respective half-bridge. As a consequence, the additional switching transitions would increase the switching frequency of the respective half-bridge above the carrier frequency, which has to be avoided since increasing the switching frequency causes the switching losses in the PWM stage to increase. This is particularly crucial if high frequency sensor noise is coupled into the control system and fed into the modulator. For this reason, a lock-

ing mechanism is implemented that stores the current bridge state of each half-bridge for the remainder of the PWM half-period once the according carrier crosses the reference. The half-bridge stays in locked state (i.e., it keeps its switching state) until the PWM half-period has expired, which is indicated by the respective PWM carrier reaching its top or bottom value, thereby releasing the half-bridge from the locked state and reestablishing regular PWM operation again.

Since during steady-state sinusoidal operation the reference signal is expected to vary considerably slower than the carrier and no multiple carrier crossings should occur, the half-bridge locking should not interfere with the dynamic behavior of the system in steady state. More precisely, multiple carrier crossings of the modulator can only occur, if the slew rate of the reference signal exceeds the slew rate of the carrier. For a sinusoidal modulator reference with amplitude $\hat{v}_{\mathrm{mod}}$ and angular frequency ω_{mod}, this translates into the following condition to avoid multiple carrier crossings:

$$\frac{2\,V_{\mathrm{DC,tot}}}{\frac{1}{2f_{\mathrm{s}}}} = 4V_{\mathrm{DC,tot}}f_{\mathrm{s}} > \hat{v}_{\mathrm{mod}}\omega_{\mathrm{mod}}, \tag{4.29}$$

where the slew rate of the carrier follows from the maximum voltage range (negative to positive) of the modulator of $2V_{\mathrm{DC,tot}}$ which the carrier crosses during half of the PWM carrier period $1/f_{\mathrm{s}}$. For the selected switching frequency of $f_{\mathrm{s}} = 300\,\mathrm{kHz}$ this condition results in a maximum modulator frequency of $f_{\mathrm{mod}} = 195\,\mathrm{kHz}$ if a full-scale sinusoidal signal with an amplitude of $\hat{v}_{\mathrm{mod}} = V_{\mathrm{DC,tot}} = 600\,\mathrm{V}$ is considered at the modulator input.

However, in **Fig. 4.20b** it is shown on the example of a short input pulse that the mechanism can lead to significant distortion of the reference during transients. This has a considerable impact on the reference step response of the system, where short transients exhibiting significantly faster slew rates than the above limits may occur.

4.4.2 Impact on Converter Step Response

The effect of the half-bridge locking mechanism on the reference step response can be investigated with circuit simulations which accurately account for the modulator implementation. In **Fig. 4.21** a series of simulated step responses is plotted for two amplitudes of $v_{\mathrm{ref}} = 20\,\mathrm{V}$ and $v_{\mathrm{ref}} = 100\,\mathrm{V}$ in **Fig. 4.21a** and **b**, respectively. Each series consists of a set of five reference step simulations which only vary regarding the start time of the reference step relative to the carrier of cell 1 reaching zero, with the definition of the start time $\Delta t_{\mathrm{start},k}$ given

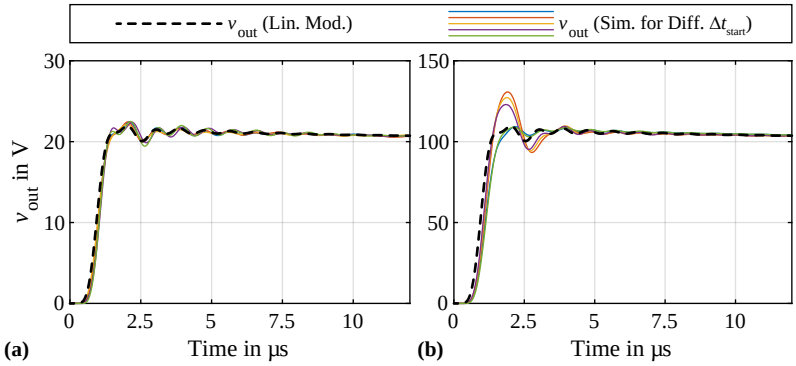


Fig. 4.21: Series of step response simulations for different start times $\Delta t_{\text{start},k}$ after carrier zero and **(a)** $v_{\text{ref}} = 20\,\text{V}$ and **(b)** $v_{\text{ref}} = 100\,\text{V}$. Excessive overshoot is found due to modulator locking for $v_{\text{ref}} = 100\,\text{V}$, which cannot be described by the linear dynamic model from **Section 4.3**. Due to the nonlinearity of this effect, no deviation is detected for $v_{\text{ref}} = 20\,\text{V}$ in these examples. Dashed: expected step response from the linear dynamic model. Colored lines: step responses obtained from simulations for different $\Delta t_{\text{start},k}$ values.

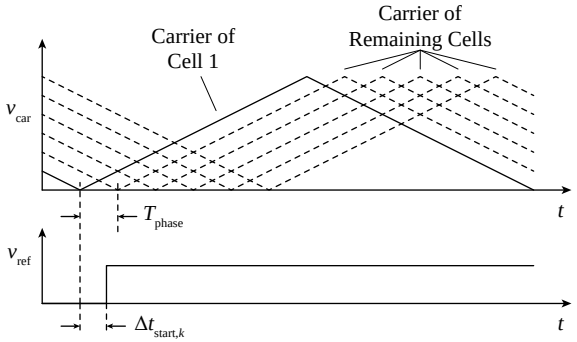


Fig. 4.22: Definition of the start time $\Delta t_{\text{start},k}$ of the reference step simulations relative to the carrier of cell 1.

in **Fig. 4.22**. The according values which were chosen for the simulations are

$$\Delta t_{\text{start},k} = [0, 56\,\text{ns}, 112\,\text{ns}, 168\,\text{ns}, 224\,\text{ns}], \tag{4.30}$$

$$\tag{4.31}$$

where the step size between two different values corresponds to a fifth of the time period $T_{\text{phase}} = 280\,\text{ns}$ of two subsequent carriers reaching zero after which the behavior of the modulator will periodically repeat.

While for the $v_{\text{ref}} = 20\,\text{V}$ case the simulated system shows exactly the dynamic behavior expected from the linear model, several cases with significantly higher overshoot are observed in case of the $v_{\text{ref}} = 100\,\text{V}$ step. This overshoot is caused by the half-bridges getting locked by the occurring transients of the modulator voltage, which prevents the controller from an appropriate reaction to stabilize the voltage until the locked half-bridges are released again when their respective carrier reaches top or bottom. Since the duration for which the bridges remain in the locked state depends on how soon their carrier reaches top or bottom after the transient occurred, the behavior exhibits a dependence on the start time $\Delta t_{\text{start},k}$ of the reference step. Furthermore, the obtained behavior depends on the amplitude of the reference step as higher reference voltages result in higher modulator reference values that are more likely to trigger the locking effect of one or several half-bridges.

Due to its nonlinear and time dependent behavior, a mathematical description of this effect is very difficult to achieve, in particular it is not possible to account for the increased overshoot in the linear model from **Section 4.3.1**. However, it is expected that especially no-load conditions and controllers which feature a high bandwidth are prone to exhibiting increased overshoot during reference steps as high bandwidths usually correspond to higher slew rates which could interfere with the half-bridge locking mechanism and passive loads tend to damp the resulting overshoot. For this reason the data set obtained from the optimization was extended by a set of circuit simulations in order to find a control system which allows reference steps with an amplitude of at least 100 V without triggering the described overshoot phenomenon. For each valid control design corresponding to a data point in the performance space in **Fig. 4.14** the above stated set of five circuit simulations was performed where a 100 V reference step was simulated for five different start times $\Delta t_{\text{start},k}$. For each control design then the maximum relative overshot over these five simulations, given as

$$M_{\text{v,sim}} = \max_k M_{\text{v,sim},k}, \tag{4.32}$$

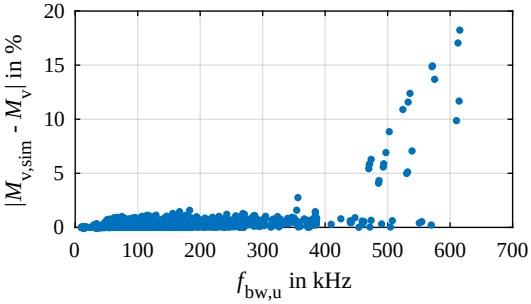


Fig. 4.23: Difference in overshoot between linear model from **Section 4.3** and circuit simulation. High bandwidths $f_{bw,u}$ (unloaded output) correlate with increased risk of triggering the locking effect, leading to excessive overshoot on the converter output.

is determined and compared to the overshoot M_v following from the linear model. The according results are presented in **Fig. 4.23** where the maximum difference between calculated and simulated overshoot is plotted as a function of the −3 dB control bandwidth under unloaded conditions, $f_{bw,u}$. From **Fig. 4.23** is found that excessive overshoot only occurs for control designs which feature bandwidths $f_{bw,u} > 350\,\text{kHz}$ (unloaded output) while only minor deviations $< 2\,\%$ are observed for slower controllers, which originate from the switching frequency ripple of the simulated output voltage. Control designs with bandwidths above this frequency that exhibit no severe overshoot were found too, however, a clear relation between utilized control parameters and the occurrence of elevated overshoot for these controllers could not be identified. For this reason, an additional boundary condition was introduced that limits the unloaded bandwidth of the control system, where a threshold of $f_{bw,u} < 300\,\text{kHz}$ was selected to provide a suitable margin.

The resulting Pareto performance space after applying this additional boundary condition is presented in **Fig. 4.24a** and **b**, with the excluded designs highlighted in red in **Fig. 4.24a**. Since the bandwidth under loaded and unloaded conditions are strongly related to each other, the eliminated designs are located towards high bandwidths in the performance space and limit the achievable performance. From the remaining designs, again the most suitable controller has to be determined for the implementation, where finally the design maximizing the achievable bandwidth on the Pareto front was selected. The according control parameters and performance metrics are given in **Tab. 4.5**. According Bode and step response plots are given in **Fig. 4.25** and **Fig. 4.27**. Furthermore, the simulated step response series for

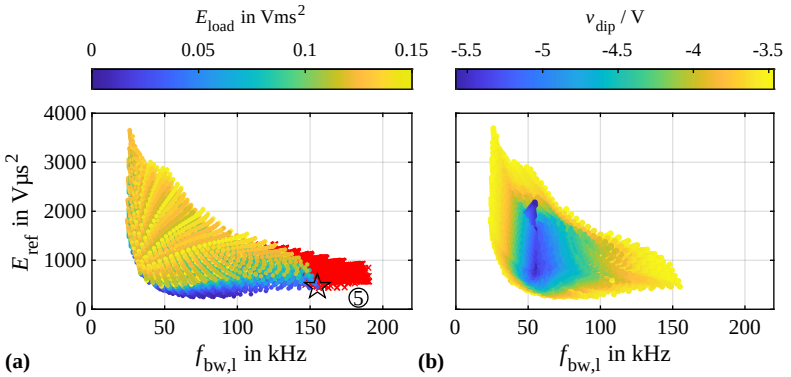


Fig. 4.24: Results of the grid search algorithm if no active loads are considered (see **Fig. 4.11**), again with the load step error integral E_{load} **(a)** and the voltage dip v_{dip} **(b)** indicated on the color axis. Designs exhibiting $f_{bw,u} > 300\,\text{kHz}$ were excluded (indicated by red markers in **(a)**). Due to the bandwidth limitation, the Pareto front is confined, resulting in a different optimal design labeled as ⑤ in **(a)**.

Parameter	Value
T_{pre}	530 ns
$K_{p,iL1}$	32 V/A
$K_{p,vout}$	106 mA/V
$T_{i,vout}$	9.24 µs
$f_{bw,l}$	155 kHz
E_{ref}	455 V µs^2
E_{load}	0.028 V ms^2
v_{dip}	−3.53 V

Tab. 4.5: Control parameters and key performance metrics of the controller used for hardware implementation, corresponding to design ⑤ in **Fig. 4.24**.

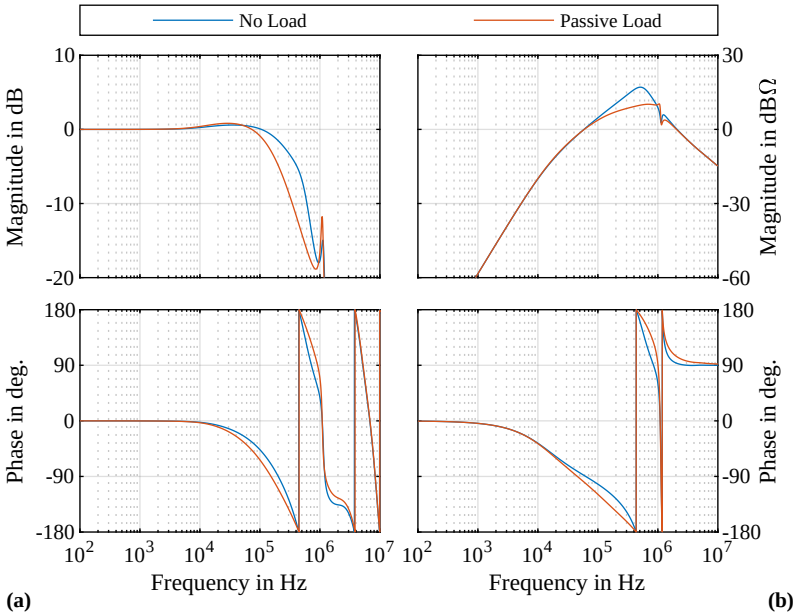


Fig. 4.25: Bode plots of the **(a)** reference transfer function and **(b)** load disturbance transfer function for the control parameters listed in Tab 4.5, corresponding to design ⑤ in **Fig. 4.24**.

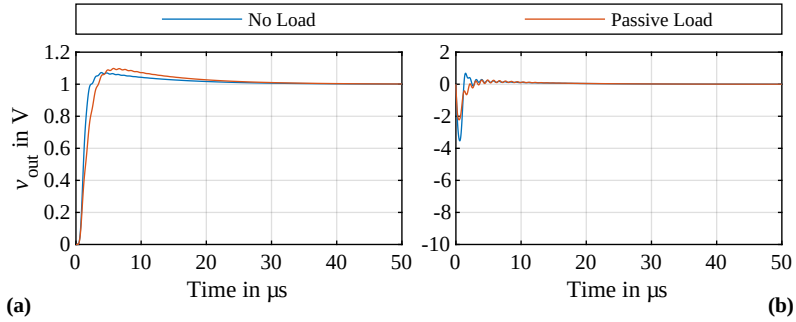


Fig. 4.26: (a) Reference and **(b)** load step response of the converter for the control parameters listed in **Tab. 4.5**, corresponding to design ⑤ in **Fig. 4.24**.

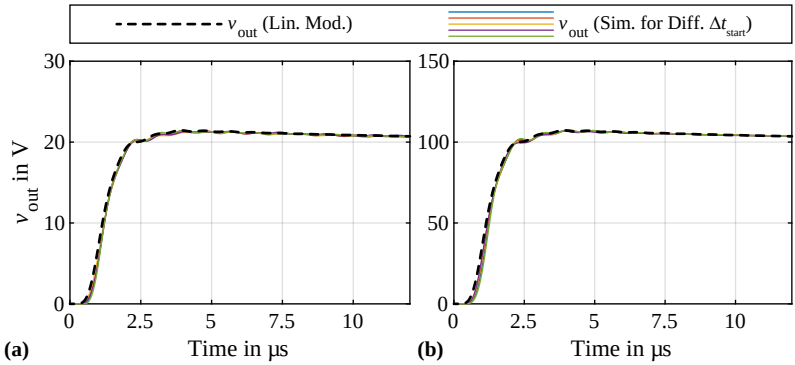


Fig. 4.27: Series of step response simulations for different start times $\Delta t_{\text{start},k}$ after carrier zero and **(a)** $v_{\text{ref}} = 20\,\text{V}$ and **(b)** $v_{\text{ref}} = 100\,\text{V}$. The overshoot observed for the original design (i.e., without considering the impact of the locking modulator) is eliminated and the simulated behavior matches the expectations from the linear dynamic model. Dashed line: expected step response from the linear dynamic model. Colored lines: step responses obtained from simulations for different $\Delta t_{\text{start},k}$ values.

this control set is illustrated in **Fig. 4.27**, where it can be verified that the increased overshoot effect was eliminated by the bandwidth reduction.

It has to be mentioned that due to the nonlinear nature of the locking modulator, the observed increase in overshoot may occur again at higher reference step amplitudes as the circuit simulations used to determine the bandwidth limit only account for steps of 100 V, although the selected approach clearly demonstrates that a relation between control bandwidth and modulator locking exists. For this reason, additional concepts to eliminate disturbances originating from the modulator implementation are presented in the next section.

4.4.3 Alternative Concepts to Eliminate the Impact of the Locking Modulator

Two additional concepts to eliminate the impact of the half-bridge locking of the modulator are briefly illustrated in the following. The first approach is based on limiting the slew rate of the reference signal while the second solution allows an increase in switching frequency for a limited time interval.

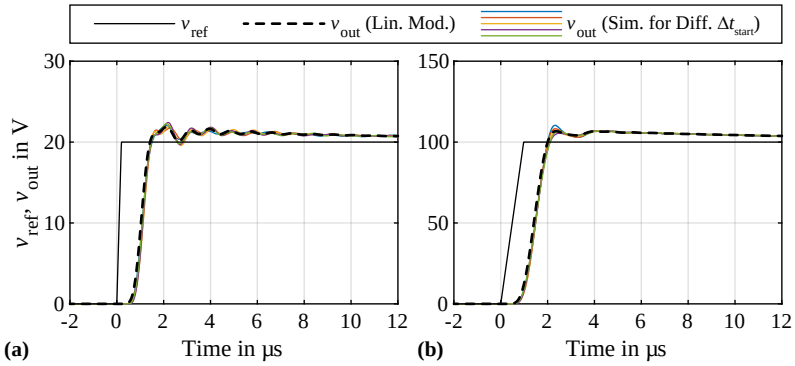


Fig. 4.28: Series of step response simulations for different start times $\Delta t_{\text{start},k}$ after carrier zero and **(a)** $v_{\text{ref}} = 20\,\text{V}$ and **(b)** $v_{\text{ref}} = 100\,\text{V}$, where the control parameters from **Tab. 4.3**, corresponding to the original controller design ④ were used. By limiting the slew rate of the reference signal, the overshoot originating from modulator locking is eliminated. Solid line: slew rate-limited (102 V/µs) reference signal. Dashed line: expected step response from the linear dynamic model. Colored lines: step responses obtained from simulations for different $\Delta t_{\text{start},k}$ values.

Slew Rate Limitation

Since distortion of the modulator signal caused by the locking effect is only occurring if the slew rate of the modulator input signals exceeds the slew rate of the carrier, the basic idea behind this solution is to limit the slew rate of the reference voltage v_{ref} as this is expected to have a similar impact on the modulator input. This can be verified in **Fig. 4.28**, where the step response series already introduced in the section before is repeated for a slew rate-limited reference voltage and the control parameters from **Tab. 4.3** corresponding to control design ④ (i.e., without the bandwidth restriction introduced in **Section 4.4**). The slew rate limit SL_{max} of the reference signal was determined such that a sinusoidal signal with an RMS value of 230 V and a frequency of 50 kHz experiences no distortion, which results in a maximum required slew rate of

$$SL_{\text{max}} = 2\pi\, 50\,\text{kHz}\, 230\,\text{V}\sqrt{2} = 102\,\text{V/µs}. \tag{4.33}$$

With the slew rate limited reference the excessive overshoot introduced by the modulator locking is eliminated and the system exhibits the dynamic behavior predicted by the linear model. However, a potential drawback of

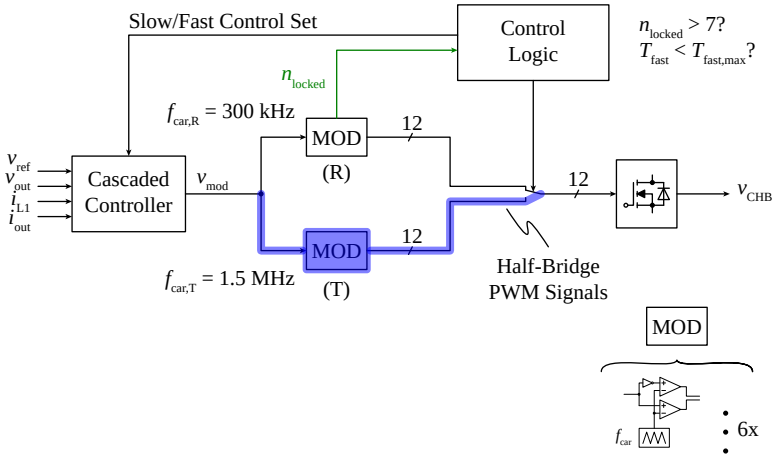


Fig. 4.29: Block diagram of an advanced modulator structure allowing a temporary increase of the switching frequency. Besides the regular PWM modulator (R) operating at the half-bridge switching frequency of $f_s = 300\,\text{kHz}$, an additional PWM modulator (T) operating at a higher switching frequency of $f_s = 1.5\,\text{MHz}$ is installed and both modulators receive the same input signal. A control logic is used to detect locking operation of the regular modulator and switches the PWM signals of the half-bridges to the transient modulator, thereby enabling a faster dynamic response. Since operation of the half-bridges with a higher switching frequency causes excessive losses, usage of the transient modulator is only applicable for short transients.

this approach is that the slew rate limiting element required at the reference input of the control system introduces its own nonlinear characteristic into the closed loop system behavior as signals featuring higher slew rates are distorted by the input limiter.

Temporary Increase in Switching Frequency

The solutions suggested so far aim at limiting the dynamics of the modulator reference signal in order to avoid the distortions introduced by the locked half-bridges. In contrast, the following approach is based on an improvement of the dynamics of the modulator, which is accomplished by an increase of its switching frequency that has two advantageous effects: On the one hand,

a higher switching frequency implies a higher slew rate of the carrier signals, thereby increasing the slew rate threshold of the modulator reference which has to be exceeded to trigger the locking mechanism leading to nonlinear behavior. On the other hand, the time required for a half-bridge to recover from its locked state considerably reduces as this time interval is limited by one half of the PWM period, which reduces the maximum error in voltage-time area applied to the filter input by a locked half-bridge. However, an increased switching frequency inevitably leads to increased switching losses and for this reason, the suggested approach is only capable of covering short transients during which the thermal capacity of the power stage is able to absorb the additional losses. If this thermal budget is used up, a certain cool down interval is required, which allows the switches to dissipate the excess losses, during which the converter is not able to react with the same dynamic response. During this cool down phase the converter is operated with a different set of control parameters in order to account for the limited dynamics and to avoid triggering the modulator overshoot.

Fig. 4.29 presents a block diagram of how a temporary increase in switching frequency can be implemented. Instead of a single conventional PWM modulator with a fixed frequency, two independent modulators with different carrier frequencies are used, which receive the same reference input from the output of the cascaded controller. The carrier frequency of the transient modulator (labeled "(T)"), is chosen as an integer multiple of the regular carrier frequency of the regular modulator (labeled "(R)") and selected to $f_{\mathrm{car,T}} = 5\, f_{\mathrm{car}} = 1.5\,\mathrm{MHz}$. Furthermore, a control logic is required which detects whether the regular modulator enters locked operation (i.e., whether it introduces nonlinear distortion due to locked half-bridges) and switches between the modulator output signals that are used to control the half-bridges.

An important aspect is to find a suitable condition for the control logic to identify locked operation of the modulator. Simply detecting whether the reference crosses the carrier more than once per half-period is considered insufficient as noise could lead to multiple crossings in the vicinity of a regular (slow) transition. A suitable indicator for this is found by considering the total number of locked half-bridges n_{locked}, which during regular operation cycles between 5, 6 and 7 in case of a modulator with six carriers (i.e., twelve half-bridges). This is illustrated in **Fig. 4.30a** at the example of a DC reference signal with a modulation index of $m = 0.4$, where it can be recognized that each carrier reaching top or bottom, thereby freeing its two respective half-bridges, is followed by two successive carrier transitions causing two half-bridges to enter the locked state until the pattern is repeated periodically.

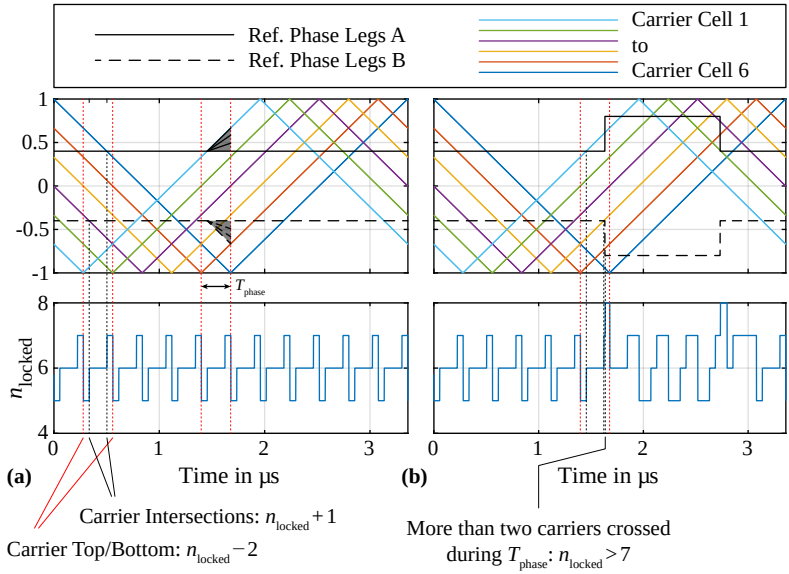


Fig. 4.30: Number of locked half-bridges during **(a)** regular operation with a DC reference and **(b)** in case of a reference step transient. Each time one of the six carriers reaches its top or bottom value its respective half-bridges are unlocked again, thereby reducing the number of locked half-bridges n_{locked} by two. Unless the slew rate of the modulator reference does not exceed the slew rate of the carriers (indicated by the shaded area in **(a)** for the example of a continuously increasing reference) only two carrier intersections of the reference signals can occur during the interval T_{phase} between two consecutive carriers reaching top or bottom. For this reason, during normal operation the number of half-bridges which are in the locked state, n_{locked}, cycles between 5, 6 and 7 for the exemplary case of a modulator incorporating six carriers (i.e., twelve half-bridges). In **(b)** the slew rate of the reference step signal exceeds the carrier slew rate, resulting in more than two carrier intersections during a T_{phase} interval and thus n_{locked} exceeding 7. See **Fig. 3.2** for the definition of phase leg A and B and their respective modulator reference signals for the used PSPWM modulation scheme.

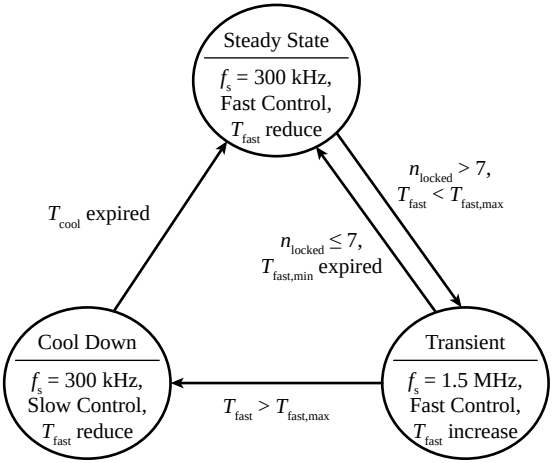


Fig. 4.31: State diagram of the control logic enabling a temporary increase in switching frequency. A thermal duration timer T_{fast} is used to account for the additional loss power dissipation occurring in the semiconductors operated at f_s. If the maximum duration for which the bridges are allowed to operate at a higher switching frequency is exceeded, the control logic enters a cool down state during which the switching frequency of the half-bridges is limited to the regular operating frequency of f_s = 300 kHz. During this interval, the control parameters of the cascaded controller have to be adapted since the modulator is not able to react to transients with the same dynamic response and would exhibit locking distortion with according overshoot.

As long as the slew rate of the modulator reference does not exceed the slew rate of the carrier, only two carrier intersections occur during each interval T_{phase} of two consecutive carriers reaching top or bottom. Locked operation of the modulator can therefore be detected if the number of locked half-bridges exceeds 7, which is illustrated in **Fig. 4.30b** on the example of a step change in the modulation index from 0.4 to 0.8. The reference step leads to more than two carrier intersections between two consecutive carriers reaching top or bottom and as a consequence, the number of locked half-bridges n_{locked} exceeds a value of 7.

The state diagram of the control logic is depicted in **Fig. 4.31**. Converter operation starts from the steady-state operation state with the 300 kHz modulator and the set of high performance control parameters being used. If the modulator enters locked operation, the control logic switches to transient

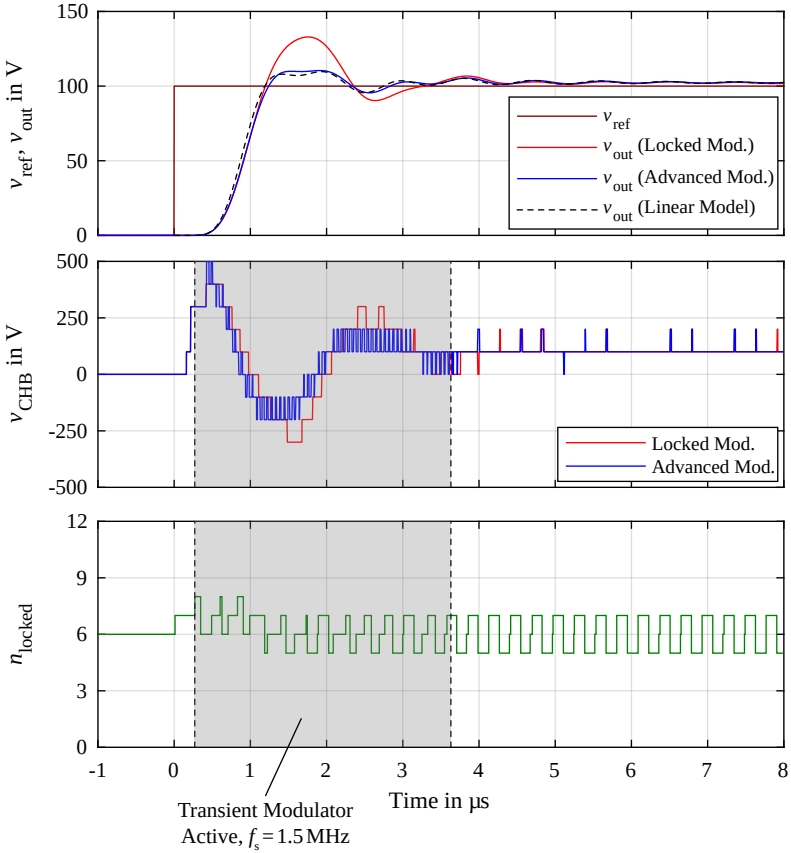


Fig. 4.32: Comparison of the resulting waveforms for a reference step with $v_{ref} = 100\,V$ for the regular locking modulator and the suggested advanced modulator structure from **Fig. 4.29**. The overshoot occurring from the locking effect of the regular modulator is eliminated by the temporary increase of the switching frequency during the highlighted interval. The increased switching frequency is clearly recognizable in the waveforms of the filter input voltage v_{CHB}.

state, where the PWM signals from the 1.5 MHz modulator are utilized, and starts to increase the thermal duration timer T_{fast}. Transient operation is kept for a minimum duration of $T_{\text{fast,min}}$, afterwards the system changes back to regular operation as soon as the regular modulator recovers from locked operation. During steady-state operation, the thermal counter T_{fast} is slowly reduced again as the cooling system dissipates the excess losses. If the regular modulator stays in locked operation for too long and T_{fast} exceeds its maximum duration $T_{\text{fast,max}}$, given by the thermal capacity of the semiconductors, the system is forced into a cool down state with a switching frequency of 300 kHz to avoid overheating of the MOSFETs. During the cool down phase the modulator is not able to react to fast transients and would exhibit the overshoot observed in **Section 4.4.2**. For this reason, the control parameters have to be adapted to a set with reduced performance (e.g., the ones found in **Section 4.4.2**), until the according duration T_{cool} of the cool down state has expired and the control logic changes to the regular state again.

Circuit simulations were used to verify proper operation of the suggested scheme, with the resulting waveforms for a 100 V reference step response provided in **Fig. 4.32** and compared to the case where an overshoot caused by modulator locking is observed. The simulation proves that the temporary increase in switching frequency successfully eliminates the excessive overshoot introduced by a fixed frequency modulator and leads to the dynamic response expected from the linear model.

4.5 Control Hardware Implementation

4.5.1 Digital Control Architecture

The control system of the entire UH-PBW amplifier not only involves the cascaded controller required to control the inverter stage, but also has to perform several additional tasks, mainly the control of the six PFC rectifiers but also various monitoring and supervision functionalities. However, many of these tasks can be performed locally on the cells, e.g., PFC control. For this reason, the control system was implemented as a distributed architecture consisting of several processing units, which can be divided into a single central controller and six local cell controllers. **Fig. 4.33** presents an overview of the implemented control architecture. Details about the cells' local control unit are provided in **Chapter 3.3**; its main task is the control of the cell's PFC stage since PFC operation of each cell is independent of the remaining cells and the operation of the inverter bridges.

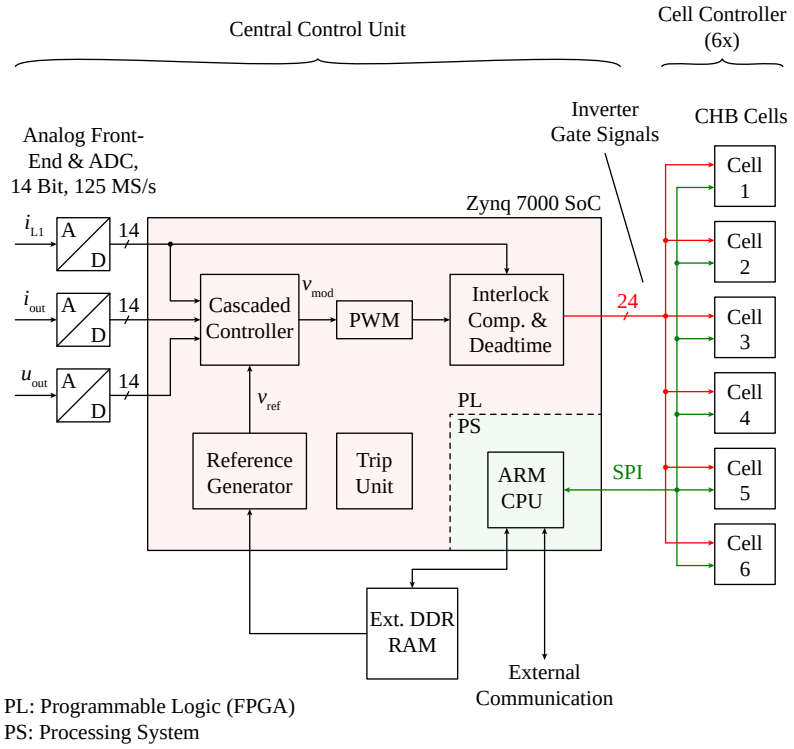


Fig. 4.33: Overview of the control system of the UH-PBW amplifier, implemented as a distributed architecture consisting of a central controller and six local cell controllers.

Contrary to the operation of the PFC rectifier, the inverter stages are exclusively controlled by the central control unit, which contains the entire output voltage control loop from the high speed ADCs and their according analog front-end to the generation of the gate signals. Again a *Zynq 7000* SoC is used for data processing, where the cascaded controller is implemented as a pipelined structure in the FPGA part of the SoC in order to minimize the execution delay times of the control loop. Massive oversampling with a sampling rate of 125 MS/s is used for the entire signal path, allowing the controller to be treated as time-continuous due to the short sampling time period and enabling a pipeline execution delay of 50 ns for each (inner current and outer voltage) controller. For AD conversion of the measured quantities, *LTC2255* devices from *Analog Devices* [257] are used, which were mainly selected due to their short conversion delay time of $T_\mathrm{m} = 50\,\mathrm{ns}$ compared to similar devices. It has to be noted that no filtering of the measured currents is performed as this would significantly limit the bandwidth of the measurements. In particular this implies that the switching frequency ripple of the inductor current is also present at the input of the cascaded controller. This was already successfully practiced in [167].

Further tasks of the central controller include various protection and monitoring features (e.g., overcurrent and overvoltage trips), execution of the interlock distortion compensation mechanism as well as handling of the cell communication and providing a user interface for the user to control the system. In addition, a reference voltage v_ref is required for the controller, which is generated by a reference generator core that streams the reference data samples stored in the DDR memory of the control unit into the cascaded controller.

Special attention has to be paid to the current measurements, for which isolated current sensors that provide a sufficiently high bandwidth while also covering DC currents are difficult to find. The bandwidth of commercial magnetic current sensors providing a sufficient current range $> 65\,\mathrm{A}$ that also allow to measure DC signals are usually limited to $< 300\,\mathrm{kHz}$, which is not enough for the intended application as a significantly higher bandwidth than the operating bandwidth of the controller is required.[1] For this reason, a custom current sensor based on the combination of a commercial component covering the low frequency range with a current transformer that measures the high frequency components is employed, which enables measuring band-

[1] Shunt measurements are not considered a reasonable option as additional analog signal isolation would be required before AD conversion. Digital signal isolation, featuring either serial or parallel data transmission, was considered unfeasible due to the introduced transmission delay or the high number of required signal isolators, respectively.

widths of ≈ 10 MHz. A detailed explanation of this principle can be found in [168].

4.5.2 Interlock Delay Compensation

In **Section 3.1.3** it was demonstrated that the interlock delay time required to safely operate the inverter half-bridges introduces current-dependent deviations of the inverter output voltage, which can degrade the signal quality of the amplifier. These deviations can be modeled as current dependent delay times between ideal PWM signal and physical switching transition of each half-bridge, which result in a distortion of the voltage time area applied to the filter input since these delay times differ between rising and falling switching transients, thereby altering the duration of the PWM pulses.

In order to mitigate these deviations, different approaches are described in literature, e.g., the addition of a compensation voltage on the modulator reference as in [258–260] or the dynamic adaption of the interlock delay time or additional variable time delays in the PWM signals as in [261, 262]. The mechanism implemented for the converter in this work is based on an additional delay unit, which introduces a variable delay time that depends on the load current of the inverter bridges that corresponds to the first stage filter current i_{L1}. **Fig. 4.34** presents the according block diagram.

The compensation mechanism consists of an additional edge delay block, which is located before the interlock delay generation unit that generates the high-side (HS) and low-side (LS) gate signals from the ideal PWM signal coming from the modulator. This edge delay unit introduces an adaptive delay time t_{c} of the PWM signal, where t_{c} is chosen in such a way that the total delay

$$t_{\mathrm{sum}} = t_{\mathrm{c}} + t_{\mathrm{dist}} \tag{4.34}$$

of compensation delay and the physical equivalent delay t_{dist} caused by the half-bridge is constant for each switching transition. Consequently, the adaptive delay time value depends on the instantaneous filter current i_{L1} as well as the switching direction of the transition (rising or falling) and is obtained from a look-up table containing the compensation values determined by

$$t_{\mathrm{c}} = \max_{i_{\mathrm{L1}}} \left[t_{\mathrm{dist}} \left(i_{\mathrm{L1}} \right) \right] - t_{\mathrm{dist}}(i_{\mathrm{L1}}), \tag{4.35}$$

with the according switching edge delay time values t_{dist} taken from the circuit simulation introduced in **Section 3.1.3**. From the equation above

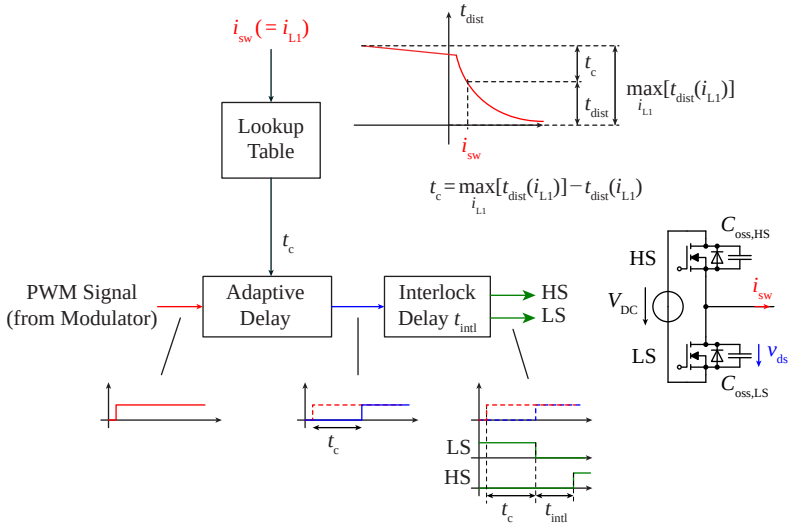


Fig. 4.34: Block diagram of the interlock delay compensation mechanism.

$t_{sum} = \max_{i_{L1}}[t_{dist}]$ follows, which, from the measured data in **Fig. 3.18** in **Section 3.1.3**, can be determined to $t_{sum} = 90\,\text{ns}$ and corresponds to the transport delay time of the inverter stage used in **Section 4.3.1**.

According waveforms of this compensation are illustrated in **Fig. 4.35** on the example of a falling transition for hard- as well as soft-switching, i.e., for different load current signs of the half-bridge. Without the compensation mechanism, different delay times of the half-bridge result that alter the duration of the PWM pulse. By introducing a suitable compensation delay time t_c, the total delay between ideal PWM signal and physical PWM transition on the bridge output is kept constant, thereby eliminating the current dependent distortion of the PWM pulse.

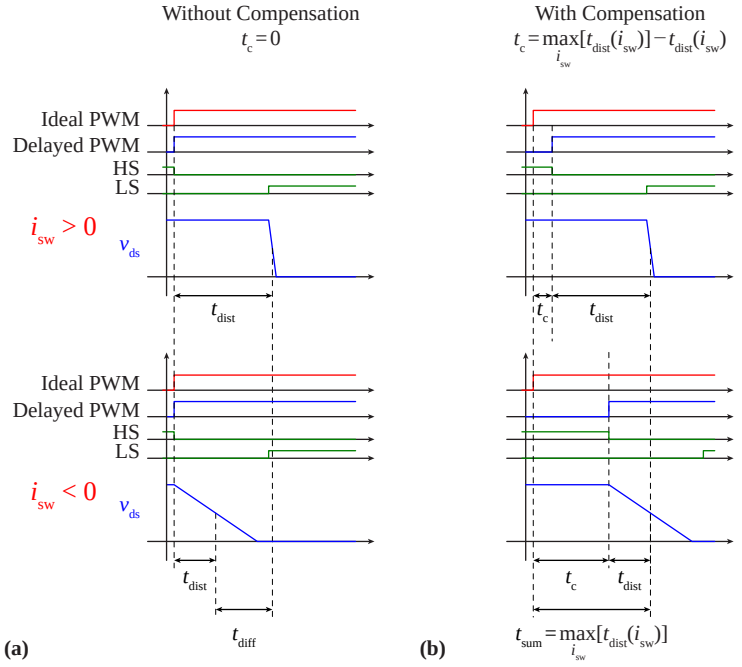


Fig. 4.35: Exemplary waveforms of interlock delay compensation unit **(a)** without compensation and **(b)** with compensation mechanism for a falling transition and two different load current directions. Without compensation, the delay time between ideal PWM signal and physical transition corresponds to the physical delay time t_{dist} of the half-bridge, which depends on the sign and magnitude of the load current. The resulting deviation between the two exemplary transitions is indicated by the difference of their respective delay times t_{diff}. By introducing a compensation delay time t_{c} in the PWM signal, the sum of compensation delay and physical delay time, t_{sum}, is kept constant, thereby eliminating the current dependency of the PWM delay times that distort the duration of the PWM pulses. Note that t_{dist} represents the delay time of an idealized rectangular PWM transition that has the same voltage-time integral as the v_{ds} waveform that exhibits a finite (load current-dependent) slope (see **Section 3.1.3**).

5
Experimental Verification

This chapter presents the measurement results which were obtained from the constructed prototype converter. In order to characterize the behavior of the system, different types of steady-state and transient measurements were conducted and compared to the results from the dynamic model and circuit simulations. **Fig. 5.1** illustrates the according measurement setup, where the main quantities being measured by an oscilloscope are the first stage filter inductor current i_{L1}, the load current i_{out} and the output voltage v_{out}. Furthermore, a so-called *Integrated Logic Analyzer (ILA)* [263] core from *Xilinx* was included in the main control FPGA, which allows to monitor the reference setpoint voltage with the full sampling rate of 125 MS/s. In order to synchronize the external oscilloscope with the FPGA-internal ILA, a trigger unit was implemented in addition, generating a common trigger impulse that triggers the ILA as well as the external oscilloscope via an IO pin of the FPGA. Since the ILA and the oscilloscope are synchronized via a common trigger, proper phase alignment between both measurements is guaranteed.

Due to the high signal frequencies and the large physical dimensions of the experimental setup, care has to be taken to avoid large parasitic inductances of the cabling connections between converter and load. In addition, the inductance of the load resistor itself has to be considered. For the load resistor several (depending on the required load resistance) parallel connected *LPS1100H47R0J* devices from *Vishay* [264] with a resistance of 47 Ω were used, which exhibit a negligible parasitic inductance of less than 50 nH. For the cabling between converter and load, manually twisted two-wire conductors with minimum possible length were used, where an inductance measurement revealed a cabling inductance of 1 µH.

The experimental setup further incorporates a load switch in order to conduct load step measurements, consisting of a bidirectional semiconductor

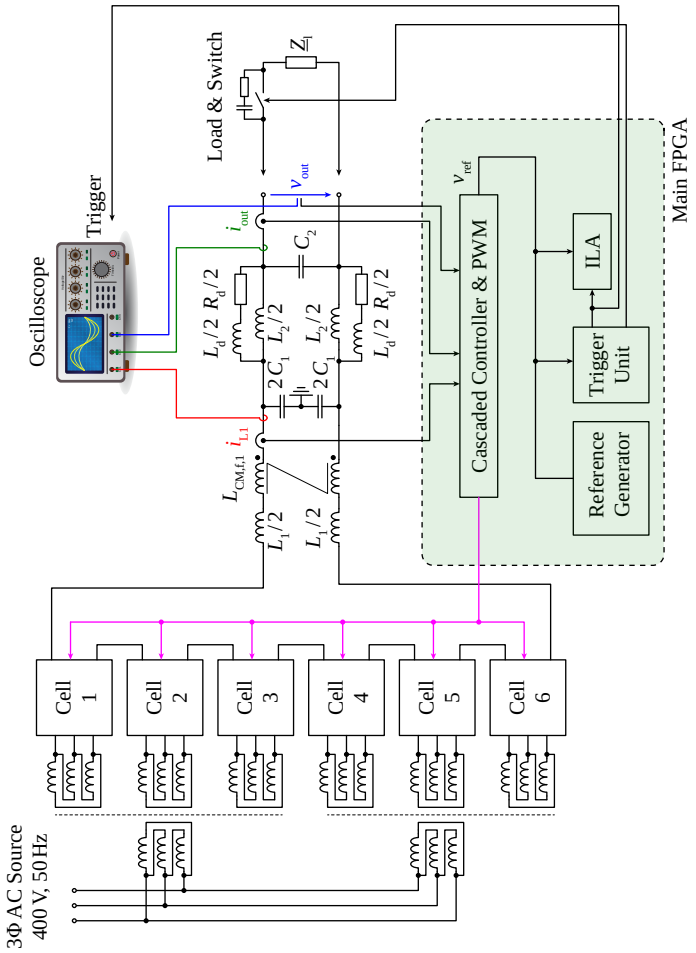


Fig. 5.1: Measurement setup for the experimental characterization of the UH-PBW prototype converter. An additional unit for the generation of the reference signal and a trigger generator are implemented in the FPGA in order to guarantee synchronized triggering of the oscilloscope and the in-FPGA ILA that records the reference signal. The trigger generator is also used to trigger the load switch in case of load step measurements.

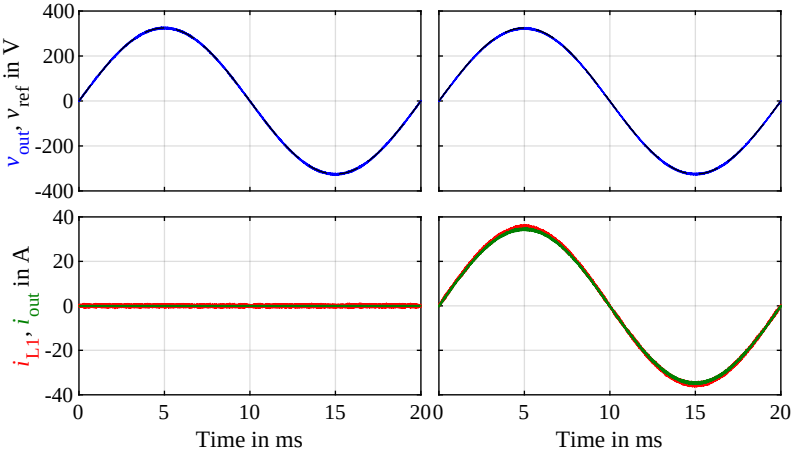


Fig. 5.2: Operation with a sinusoidal reference with $\hat{v}_{ref} = 325\,V$ and a frequency of 50 Hz. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

switch (two SiC MOSFETs connected in anti-series with a common source pin) and an according RC snubber element. The according control signal is also generated by the trigger unit inside the FPGA.

The first set of measurements presented in the following incorporates steady-state sine waveforms where unloaded as well as loaded operation at various output frequencies are compared. These results allow to derive the transfer characteristic of the system in the form of a Bode plot as well as the output impedance of the converter. In addition, the transient behavior of the converter is demonstrated by the measured reference step and load step responses. Finally, some arbitrary signals including sine waveforms with a third harmonic component or triangular waveforms are presented.

5.1 Steady-State System Characterization

5.1.1 Steady-State Sine Waveforms

Fig. 5.2 to **Fig. 5.6** present the waveforms obtained for a sinusoidal reference signal with an amplitude of $\hat{v}_{ref} = 325\,V$ (230 V RMS) for five distinct frequencies of 50 Hz, 1 kHz, 20 kHz, 80 kHz and 150 kHz, respectively. All five measurements were carried out for unloaded as well as loaded operation,

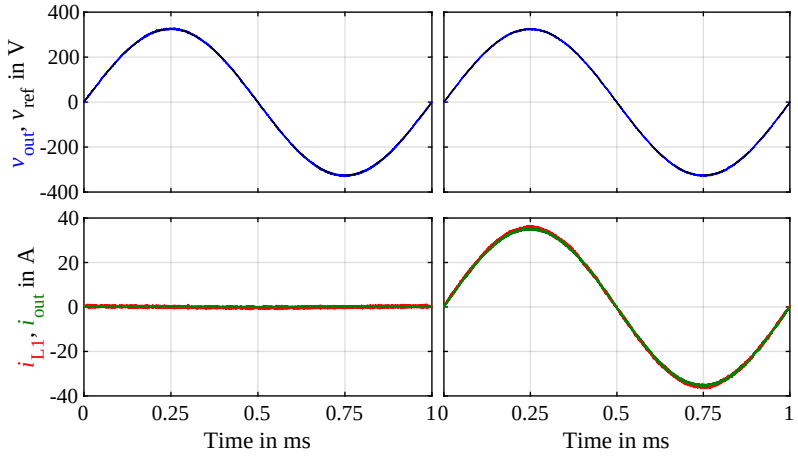


Fig. 5.3: Operation with a sinusoidal reference with $\hat{v}_{ref} = 325\,\mathrm{V}$ and a frequency of 1 kHz. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

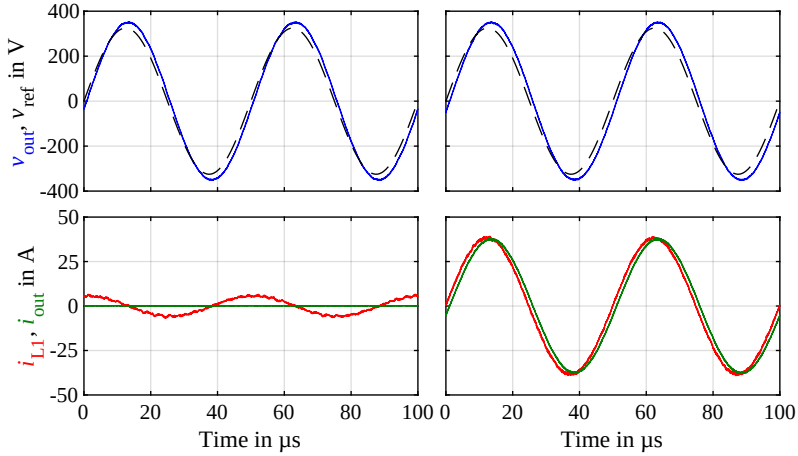


Fig. 5.4: Operation with a sinusoidal reference with $\hat{v}_{ref} = 325\,\mathrm{V}$ and a frequency of 20 kHz. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

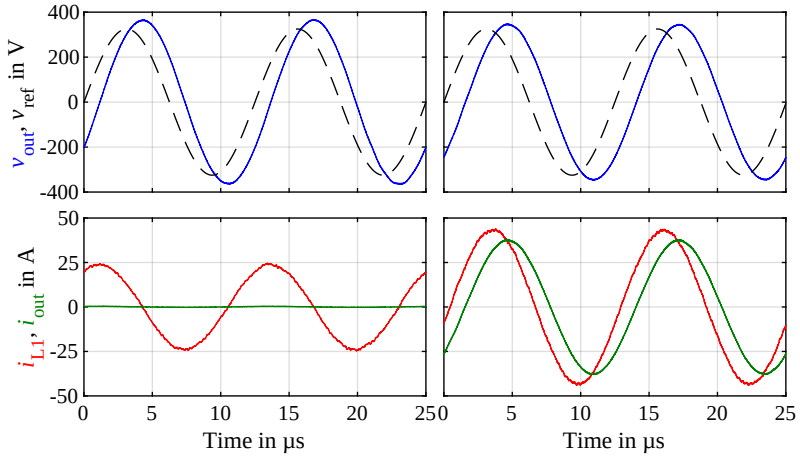


Fig. 5.5: Operation with a sinusoidal reference with $\hat{v}_{ref} = 325\,V$ and a frequency of 80 kHz. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

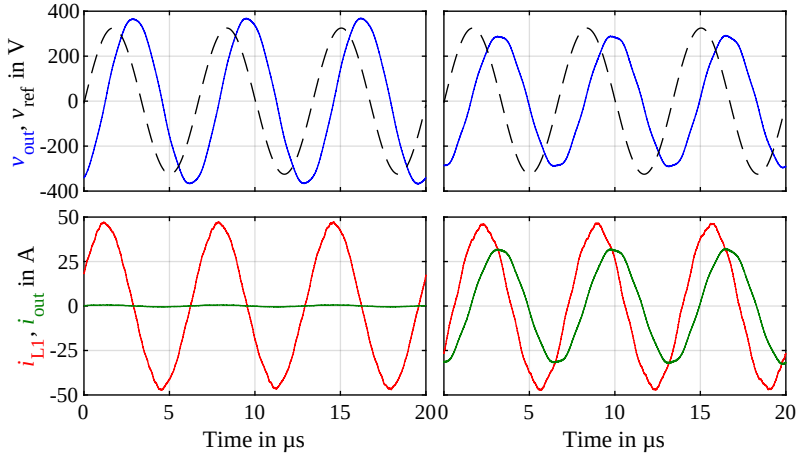


Fig. 5.6: Operation with a sinusoidal reference with $\hat{v}_{ref} = 325\,V$ and a frequency of 150 kHz. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

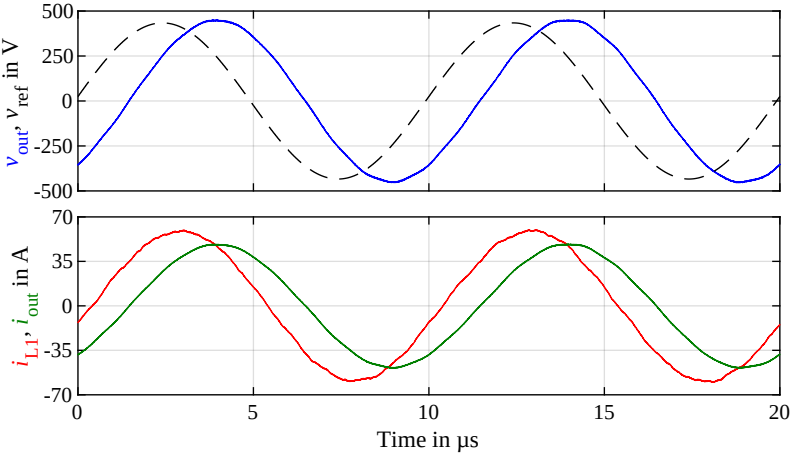


Fig. 5.7: Operation with a sinusoidal reference with $\hat{v}_{ref} = 434\,\text{V}$ and a frequency of 100 kHz. A power of 10 kW is delivered to a 9.4 Ω ohmic load with 1 µH parasitic series inductance.

where a 9.4 Ω load with a parasitic series inductance of 1 µH was used, resulting in a peak current of 34.6 A and a power of 5.6 kW for 325 V nominal voltage amplitude. Besides the waveforms of the reference v_{ref} and the output voltage v_{out}, the results also include the first stage filter current i_{L1} as well as the load current i_{out}. Furthermore, **Fig. 5.7** presents operation at a reference amplitude of $\hat{v}_{ref} = 434\,\text{V}$ at a frequency of 100 kHz, resulting in nominal output power of 10 kW for the considered 9.4 Ω load.

From the plots it can be recognized how the converter reproduces the desired signals, where for frequencies > 1 kHz a noticeable phase shift and a deviation in amplitude with respect to the reference signal is observed. Also, the reduction in output voltage between unloaded and loaded operation increases with increasing frequency, suggesting an increase in output impedance for higher operating frequencies.

In addition, the measurements demonstrate the significant capacitive current consumption of the output filter for high frequencies, which becomes evident from the i_{L1} filter current waveform reaching peak values of 25 A and 47 A for no-load conditions at 80 kHz and 150 kHz, respectively. The current ripple in the first stage filter inductor current i_{L1} is barely recognizable in the presented measurements since the employed first stage filter inductor $L_1 = 10.2\,\mu\text{H}$ is considerably larger than the lower limit of 450 nH given by

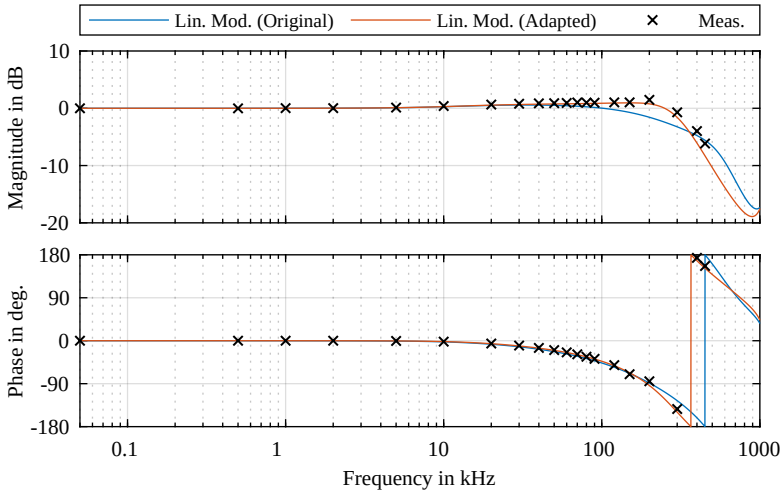


Fig. 5.8: Measured transfer characteristic of the unloaded system. For frequencies below 200 kHz, a reference amplitude of 325 V is used for the measurement, for higher frequencies the reference amplitude is reduced to 32.5 V to avoid the reactive filter current exceeding the current limit. An accurate matching between measurements (black markers) and the original dynamic model from **Chapter 4** is obtained for frequencies below ca. 50 kHz. For higher frequencies, noticeable deviations of the transfer characteristic are found, which originate from the additional dynamics of the voltage measurement circuitry and the deviating filter inductor value. If the dynamic model is adapted by accounting for these influences, an accurate matching between measurements and adapted dynamic model over the entire operating range is obtained.

the inductor current ripple criterion in **Section 3.2.1**. It has to be mentioned that the output frequencies of 100 kHz and 150 kHz are significantly higher than the maximum achievable output frequency of $f_{\mathrm{out,max}} = 77$ kHz stated in the filter realization in **Section 3.3**. This is feasible since, due to the reduced power of 5.6 kW, lower load currents result that allow higher capacitive reactive currents to be delivered by the switching stage. Furthermore, the maximum output frequency $f_{\mathrm{out,max}}$ is given for the maximum output voltage of 470 V, whereas lower (nominal) output voltage values were used during these measurements, thereby reducing the resulting capacitor currents.

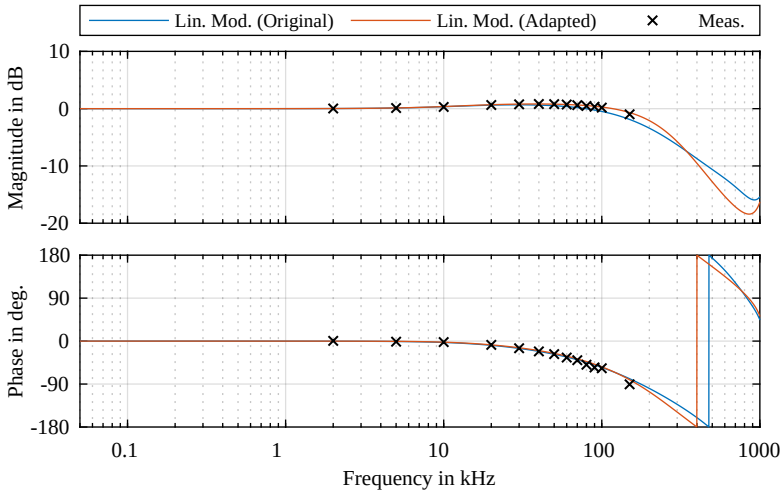


Fig. 5.9: Bode plot of the loaded system (9.4 Ω load with additional 1 µH parasitic inductance in series). Similarly to unloaded operation, an accurate matching between measurements (black markers) and the original dynamic model from **Chapter 4** is obtained for frequencies below ca. 50 kHz while noticeable deviations due to the additional dynamics of the voltage measurement circuitry and the deviating filter inductor value occur for higher frequencies. Again, these deviations are eliminated if an adapted dynamic model that considers these additional dynamics is used.

5.1.2 Transfer Characteristic and Output Impedance

In order to obtain the transfer characteristics in the frequency domain, the sine measurements presented in the section before were repeated for a wide set of different signal frequencies. Phase and amplitude were measured with respect to the reference signal and plotted in a Bode plot given in **Fig. 5.8** for unloaded operation and **Fig. 5.9** for loaded operation, where the same 9.4 Ω, 1 µH load as for the sine measurements presented in **Section 5.1.1** was used. Furthermore, the obtained transfer characteristic is compared to the results of the dynamic model from **Section 4.4**, which is illustrated by the blue curve in the presented Bode diagrams. However, while the results present a good accordance between linear model and measured results for frequencies below ca. 50 kHz, noticeable deviations are found for higher frequencies. These deviations are caused by the following differences between dynamic model and actual hardware realization, which resulted from practical realization issues that arose during the commissioning process of the converter:

- During commissioning it was found that the voltage measurement circuitry sensing the output voltage is subject to severe disturbances due to the switching actions of the inverter stages. In order to reject these disturbances, digital filtering of the voltage measurement was established inside the FPGA, where a second-order IIR Butterworth filter with a corner frequency of 5 MHz and a pipeline latency of two clock cycles at 125 MS/s was implemented to attenuate the switching noise. This filter had a noticeable influence on the transfer function of the closed-loop control system due to the introduced phase lag in the feedback path.

- Additionally, the analog front-end of the voltage measurement driving the ADC consisting of an *LTC6363* fully differential amplifier from *Analog Devices* was originally dimensioned to exhibit a first-order low-pass filter characteristic with a corner frequency of 1 MHz. However, a measurement of the transfer characteristic of the sensing circuit revealed a second-order behavior with an additional pole at 1.2 MHz, resulting in a faster reduction in phase with frequency, as illustrated in **Fig. 5.10**, thereby further increasing the phase lag of the voltage measurement. Circuit simulations revealed that the additional pole can be attributed to parasitic capacitances of the PCB layout of the voltage divider which is composed of several SMD components in order to handle the high voltage.

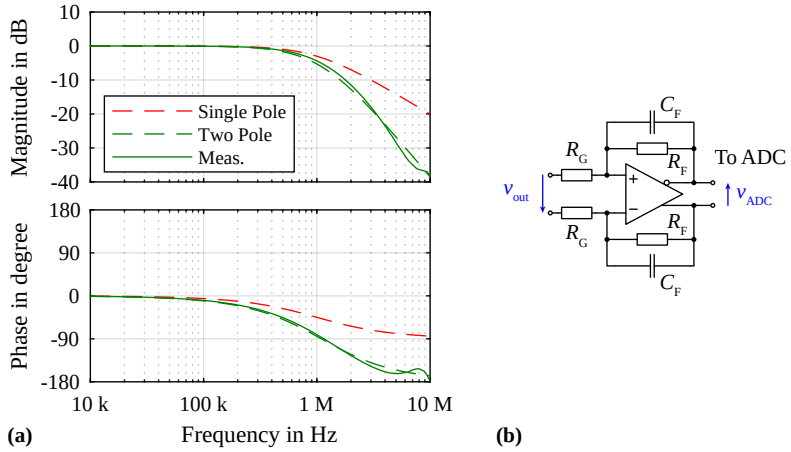


Fig. 5.10: (a) Bode plot of the analog front-end of the voltage measurement feeding the *LTC2255* ADC from *Analog Devices* used for the voltage measurement. Instead of the first-order behavior expected from the according schematic of the analog front-end illustrated in **(b)**, the measurement reveals a second-order system with two corner frequencies at 1 MHz and 1.2 MHz.

- The leakage inductances of the cells' CMCs were found to exhibit a larger value than what was expected from the initial prototype CMC designed and characterized in **Section 3.3.1**. Instead of a leakage inductance of 1.4 µH found for the prototype component in **Section 3.3.1**, a higher value of 1.7 µH was found by an additional measurement of the finalized CMCs in the constructed system. The higher inductance of the six cell CMCs resulted in a total inductance value of 12 µH instead of 10.2 µH for the first stage filter inductance L_1.

Taking into account the above aspects, the dynamic model introduced in **Section 4.4** can be updated while keeping the control parameters at the values given in **Tab. 4.5**, resulting in the orange curve in the Bode plots shown in **Fig. 5.8** and **Fig. 5.9** which proves a very good accordance between measurement results and dynamic model. However, it has to be mentioned that since the control parameters were originally designed for the ideal system in **Section 4.4**, the dynamics of the prototype system will slightly deviate from the expectations following from the Pareto optimization of the control parameters.

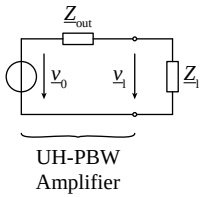


Fig. 5.11: Thévenin equivalent circuit of the converter. The phasors $\underline{v}_0$ and $\underline{v}_l$ are obtained from the unloaded and loaded sine voltage measurements, respectively. $\underline{Z}_l$ denotes the impedance of the used 9.4 Ω, 1 µH load.

From the measurement results illustrated in **Fig. 5.8** and **Fig. 5.9**, also the output impedance of the converter can be estimated, which corresponds to the negative load-disturbance transfer function, i.e., $\underline{Z}_{\text{out}} = -\underline{G}_{\text{load}}$ (cf. **Section 4.3.2**). Considering the Thévenin equivalent circuit of the converter according to **Fig. 5.11**, the output impedance can be determined according to

$$\underline{Z}_{\text{out}} = \frac{\underline{v}_0 - \underline{v}_l}{\underline{v}_l} \cdot \underline{Z}_l. \tag{5.1}$$

In the above expression $\underline{v}_0$ and $\underline{v}_l$ represent the output voltage phasors during loaded and unloaded operation, respectively, which are obtained from the measurements of the transfer characteristic presented before. $\underline{Z}_l$ refers to the according load impedance, where for the conducted experiments, $\underline{Z}_l = 9.4\,\Omega + \mathrm{j}\omega\,1\,\mu\mathrm{H}$ applies. The results for the output impedance are presented in **Fig. 5.12** together with the expectations from the original and updated dynamic models. While the difference between the two models is minor, the measurements exhibit a noticeable deviation for lower frequencies, particularly regarding the phase. These deviations are a consequence of the limited measurement accuracy of the output voltage measurement, where, due to the subtraction of the two output voltage measurements of both load scenarios in (5.1), small deviations in the measured voltage already result in large errors of the obtained impedance. This can be demonstrated on the exemplary measurement at an output frequency of 2 kHz, where the following measurements were taken:

$$\underline{v}_0 = 326\,\mathrm{V}\angle 0°, \quad \underline{v}_l = 326.1\,\mathrm{V}\angle 0.485° \Rightarrow \tag{5.2}$$

$$\underline{Z}_{\text{out}} = 79.61\,\mathrm{m\Omega}\angle -92.24°. \tag{5.3}$$

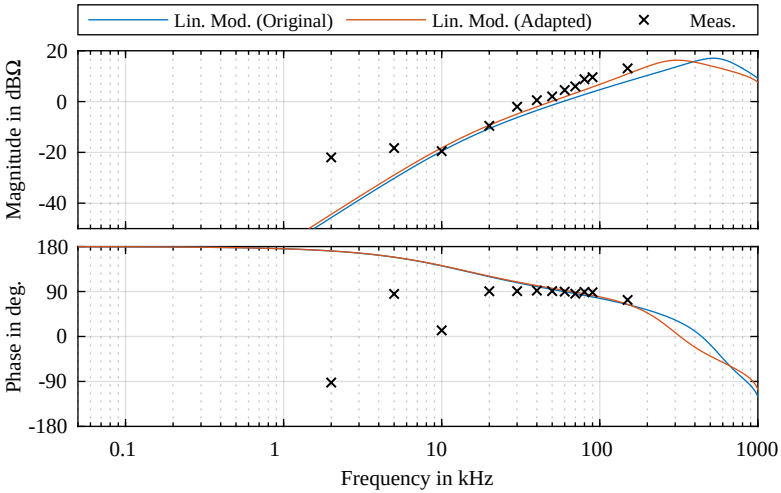


Fig. 5.12: Output impedance of the converter. Blue: original dynamic model used to dimension the controller in **Chapter 4**. Orange: improved dynamic model obtained when accounting for additional dynamics introduced by the voltage measurement circuitry and the adapted filter inductor value. Black markers: measurements. Measured values were calculated according to (5.1) with the data of **Fig. 5.8** and **Fig. 5.9** used to determine the impedance. Since the voltage differences between loaded and unloaded operation are small (especially in case of low signal frequencies), measurement errors result in comparably large deviations of the resulting impedance values.

Assuming a deviation in the measured angle of $\underline{v}_1$ of $\Delta\phi = -0.5°$ and a relative amplitude error ϵ of $\epsilon = -0.1\,\%$ results in

$$\underline{v}_0 = 326\,\mathrm{V}\angle 0°, \quad \underline{v}_l = (1+\epsilon)\,326.1\,\mathrm{V}\angle\,(0.485° + \Delta\phi) \Rightarrow \tag{5.4}$$

$$\underline{Z}_{\mathrm{out}} = 6.97\,\mathrm{m\Omega}\angle 20.75°, \tag{5.5}$$

i.e., a change in results by more than a factor of ten in impedance and a change in phase difference of 113°. Since the voltage difference between unloaded and loaded operation increases with frequency, thereby reducing the influence of the errors of the measurement, also the observed deviations between measured and calculated output impedance are reduced with increasing operating frequency.

5.2 Transient Behavior

The transient behavior of the converter is characterized by two types of step responses. The reference step response provides insight in the system's transient behavior to reference tracking, while the load step response characterizes the system's transient response to output disturbances.

5.2.1 Reference Step Responses

Fig. 5.13 presents a reference step response of the converter from 0 V to 100 V at unloaded as well as loaded condition, where the same 9.4 Ω load with 1 µH parasitic series inductance as for the measurements before was used. The measurements reveal an overshoot of 18 % and 11 % for unloaded and loaded operation, respectively, with according rise times (measured from 10 % to 90 % of the reference voltage) of 1 µs and 1.4 µs. Furthermore, the measurements are compared to the calculated step response following from the updated dynamic model (i.e., including the deviations mentioned in **Section 5.1.2**), presenting a very good accordance between measurement and linear model.

Since the observed overshoot for both load cases is higher than the limit of 10 % introduced in **Chapter 4**, which is caused by the differences between dynamic model and hardware realization listed in **Section 5.1.2**, the step response measurements were repeated for an additional set of control parameters given in **Tab. 5.1**, which exhibits a lower error integral and a reduced bandwidth compared to the originally selected parameters in **Section 4.4**. The according results are shown in **Fig. 5.14**, together with the expectations from the linear model. Due to the reduced control gains, smaller overshoots

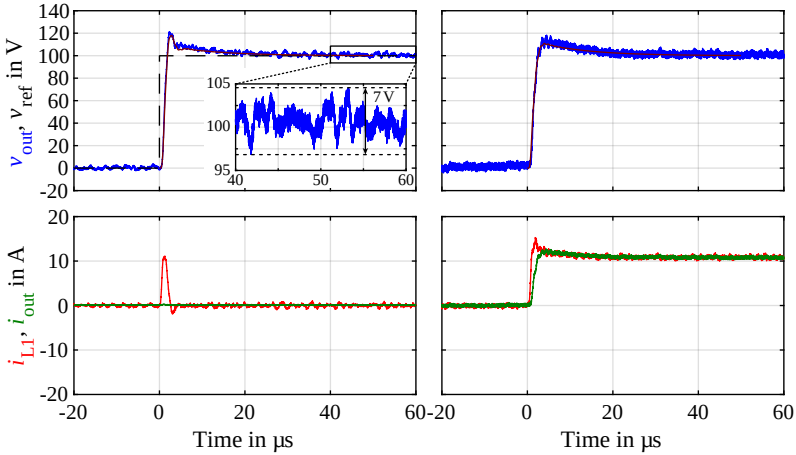


Fig. 5.13: Reference step response for $v_{ref} = 100\,\mathrm{V}$. Left: unloaded, right: $9.4\,\Omega$ ohmic load with $1\,\mu\mathrm{H}$ parasitic series inductance. Peak-to-peak noise voltage levels of 7 V are found in the noise floor of the output voltage for the unloaded reference step once the transient has settled, which are caused by the voltage measurement implementation issues discussed in **Section 5.3**. Blue: measured output voltage, brown: output voltage resulting from linear model.

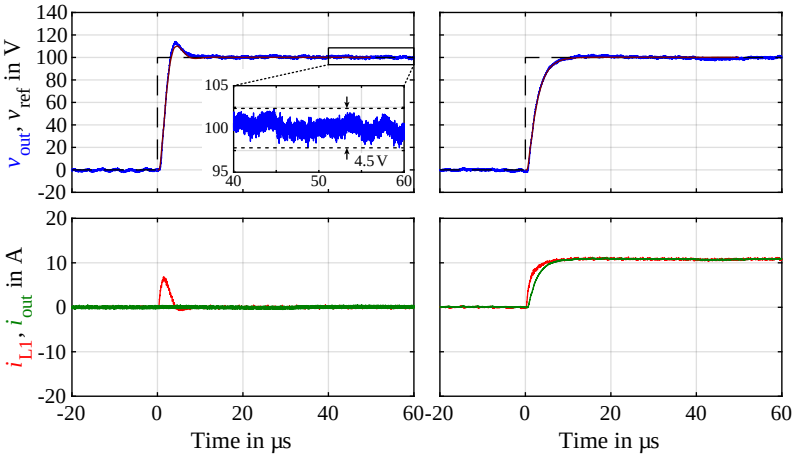


Fig. 5.14: Reference step response for $v_{ref} = 100\,\mathrm{V}$ with the adapted set of control parameters listed in **Tab.5.1**. Left: unloaded, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance. Compared to the step response in **Fig. 5.13**, the output voltage exhibits a significantly reduced noise floor with peak-to-peak noise voltage levels of 4.5 V. This is a consequence of the smaller control gains that are used, which reduce the noise voltage occurring in the voltage measurement that is coupled into the control loop (cf. **Section 5.3**). Blue: measured output voltage, brown: output voltage resulting from linear model.

Parameter	Value
T_{pre}	0 ns
$K_{\text{p,iL1}_{\text{L1}}}$	10.5 V/A
$K_{\text{p,vout}}$	4 mA/V
$T_{\text{i,vout}}$	90 µs
E_{ref}	254 V µs^2
E_{load}	1.12 V ms^2
V_{dip}	−5.77 V
$f_{\text{bw,l}}$	48 kHz

Tab. 5.1: Alternative set of control parameters used for additional step response measurements; related key performance metrics are also given.

of 10 % and 0 % result for unloaded and loaded operation, respectively, at the cost of a reduced bandwidth which also manifests in the increased rise times of 2 µs (unloaded measurement) and 4.8 µs (loaded measurement). Again, a good matching between dynamic model and measurement is found.

5.2.2 Load Step Responses

The results of the load step response are shown in **Fig. 5.15**. Again, two tests were performed where in both cases a 15.6 Ω load is connected to the output of the converter at time zero, which for the reference voltage of 100 V results in a current step at the output of 6.4 A. The two scenarios differ by the initial operating conditions, where in the first case the converter is initially unloaded, resulting in a load step from zero to 640 W at the reference voltage of 100 V, while in the second scenario the converter is initially operated with a 23.5 Ω load before an additional load with 15.6 Ω is connected to its output, thereby resulting in a final resistance of 9.4 Ω and an according step in power of from 425 W to 1.1 kW for the same reference voltage. Again, the measurements are compared to the results expected from the linear model, where a good agreement between calculation and measurements is revealed. Voltage dips of 23 V and 21 V are found for the two cases in **Fig 5.15**. Although the dynamic model in **Chapter 4** considers a current source instead of a switched ohmic load for a load step, the obtained results closely match the expected value of the voltage dip of $v_{\text{dip}} = 3.5\,\text{V/A}$ expected from the linear model since the output impedance of the converter is significantly lower than the considered

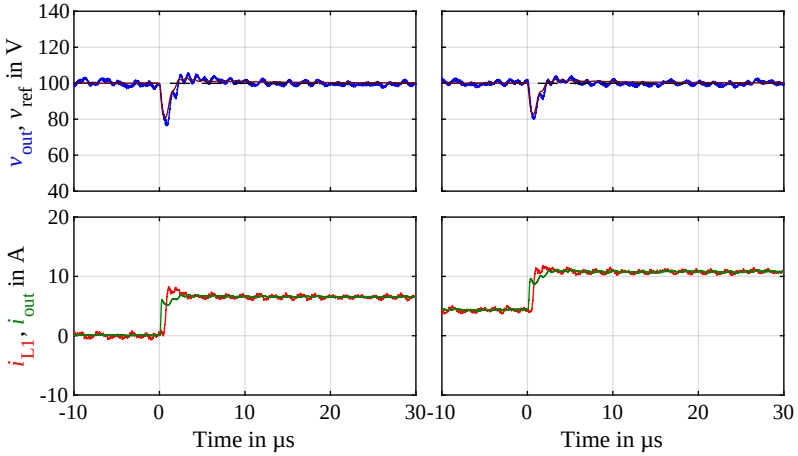


Fig. 5.15: Load step response for a DC voltage of 100 V. Left: step from unloaded operation to a 15.7 Ω load with 1 µH parasitic series inductance connected at time zero. Right: the converter is initially operated with a steady-state load of 23.5 Ω with a parasitic series inductance of 1 µH. At time zero, an additional 15.7 Ω resistive load is connected in parallel, resulting in a load impedance of 9.4 Ω with a parasitic series inductance of 1 µH. Note that the parasitic series inductance does not change between the two states since it is almost entirely given by the cable connection from the converter to the load while the load resistors including the load switch are implemented on a common PCB that introduces only negligible inductance. Blue: measured output voltage, brown: output voltage resulting from linear model.

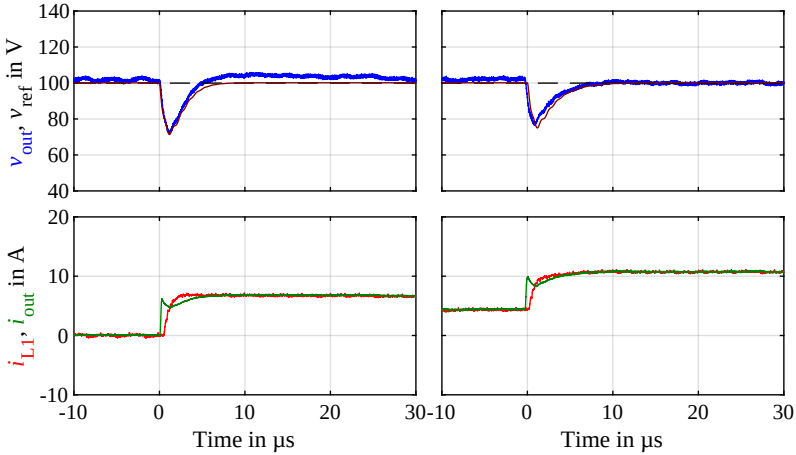


Fig. 5.16: Load step response for a DC voltage of 100 V with the adapted set of control parameters listed in **Tab.5.1**. Left: step from unloaded operation to a 15.7 Ω load with 1 µH parasitic series inductance connected at time zero. Right: the converter is initially operated with a steady-state load of 23.5 Ω with a parasitic series inductance of 1 µH. At time zero, an additional 15.7 Ω resistive load is connected in parallel, resulting in a load impedance of 9.4 Ω with a parasitic series inductance of 1 µH. Note that the parasitic series inductance does not change between the two states since it is almost entirely given by the cable connection from the converter to the load while the load resistors including the load switch are implemented on a common PCB that introduces only negligible inductance. Blue: measured output voltage, brown: output voltage resulting from linear model.

load resistance. Similar to the reference step response discussed above, also the load step measurements were repeated for the adapted control parameters listed in **Tab. 5.1**. The according results are shown in **Fig. 5.16** and reveal significantly slower dynamics and larger output voltage dips of 30 V and 27 V, respectively, for both cases due to the reduced control bandwidth. Again, the measurement results reveal a close agreement with the expectations from the dynamic model.

In addition, also the reaction of the converter to a load step in case of a sinusoidal output signal from unloaded operation to a 15.7 Ω load was measured, with the results shown in **Fig. 5.17** for a 325 V, 10 kHz sinusoidal reference and different phase angles at which the load step occurs. The observed current flowing before the load switch is closed and after reopening

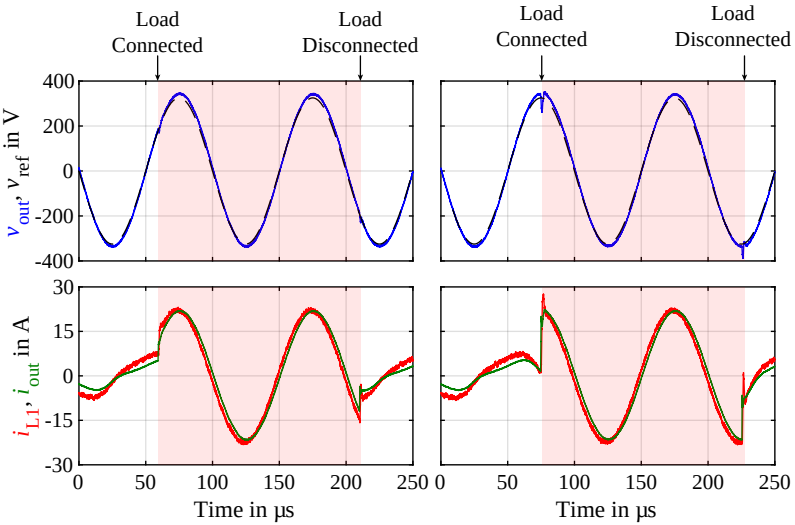


Fig. 5.17: Load step response for a 15.7 Ω load and a sine voltage of 325 V amplitude at 10 kHz. Two measurements are shown for two different switching times relative to the angle of the reference signal. The current flowing before and after the time period where the load is connected (highlighted in red) is caused by the RC snubber element installed over the load switch terminals. This current exhibits considerable nonlinear distortion introduced by the nonlinear behavior of the ceramic capacitor used for the snubber.

the load switch results from the RC snubber circuit connected across the terminals of the load switch (cf. beginning of this chapter) and exhibits significant nonlinearity due to the employed nonlinear ceramic capacitor.

5.3 Output Voltage Quality

During commissioning of the system it was found that the output voltage of the converter exhibits a considerable amount of noise, e.g., peak-to-peak values of 7 V can be recognized in the reference response waveforms from **Fig. 5.15** after the system has settled to the steady-state reference value. The observed noise levels significantly exceed the 10 mV noise voltage limit stated in **Chapter 3** and can be attributed to the following two noise sources:

- As already mentioned in **Section 5.1.2**, the implemented measurement front-end of the output voltage measurement suffers from insufficient noise immunity, which results in severe disturbances of the measured voltage caused by the switching actions of the inverter cells' bridges. Although digital filtering massively reduces the occurring distortion, a significant noise floor remains which is fed into the feedback loop of the voltage controller and degrades the output voltage quality of the converter since the controller acts on the distorted measurement. The according distortion of the output voltage becomes more prominent for higher values of the control gains $K_{\mathrm{p,iL1}}$ and $K_{\mathrm{p,vout}}$, which can be recognized by comparing the noise floor in the load step responses of **Fig. 5.15** and **Fig. 5.16**. Since the used control gains are significantly lower for the measurement in **Fig. 5.16**, the according output voltage exhibits a significantly reduced noise floor.

- Additionally, it was found that the CM currents flowing via the parasitic capacitances C_{par} of the cells (cf. **Section 3.1.2**) introduce distortion of the converter's output voltage due to the stray inductances of the cells' CMCs being utilized to realize the first stage filter inductor (according to **Section 3.3** the first stage filter inductor L_1 is not implemented as a distinct component but realized by the stray inductances of the incorporated CMCs). As a consequence, the CM currents flowing via the parasitic cell capacitances introduce according voltage drops across these stray inductances. This effect is illustrated in **Fig. 5.18** on the example of a switching action of half-bridge A of cell 5, with the according voltage drop across the cells' CMCs caused by the CM current appearing as a DM noise voltage at the filter input. Since the base

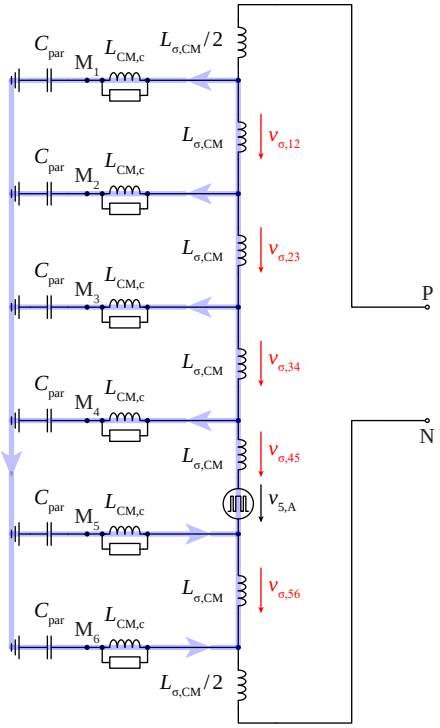


Fig. 5.18: Exemplary switching action of cell 5 in the CHB stack introducing a CM current via the cell's parasitic capacitances. Since the leakage inductances $L_{\sigma,\mathrm{CM}}$ of the cell's CMCs are used for the implementation of the first stage filter inductor L_1, the according voltage drops $v_{\sigma,12}$ to $v_{\sigma,56}$ caused by the CM currents appear as a DM noise voltage at the stack output. Note that only the CM current paths via the parasitic cell capacitances are shown in the above schematic, while the additional CM path via the output filter is omitted for simplicity.

frequency of this disturbance corresponds to the half-bridge switching frequency of $f_s = 300\,\text{kHz}$, the respective noise voltage exceeds the bandwidth of the control system where proper compensation action of the voltage controller could mitigate the effect. At the same time the filter attenuation at 300 kHz is not high enough to sufficiently attenuate the occurring noise voltage. Consequently, the introduced disturbance adds an additional noise contribution to the output voltage of the converter.

Due to the aforementioned influences the converter prototype was not able to guarantee the output voltage criteria introduced in **Section 3.2**, particularly the 10 mV maximum RMS noise voltage limit. Measurements of the output voltage quality were conducted with a *Rohde und Schwarz UPV Audio Analyzer* [265] in order to measure the signal-to-noise-and-distortion (SINAD) figures (cf. **Section 3.2**) of the converter. SINAD values of 54.8 dB and 51.3 dB for unloaded operation with a 325 V sinusoidal reference and frequencies of 50 Hz and 5 kHz, respectively, were found. Furthermore, in case of loaded operation with a 5.6 kW ohmic load according values of 54.4 dB (at 50 Hz) and 48.8 dB (at 5 kHz) were obtained for the same reference signals. Although these numbers would theoretically fulfill the SINAD criteria stated in **Section 3.2**, it has to be mentioned that the employed spectrum analyzer exhibits a measurement bandwidth of 250 kHz, i.e., the device is not able to measure distortions at the half-bridge switching frequency of 300 kHz and its harmonics. A more precise characterization of the prototype converter including the cell switching frequency harmonics would be required, however, the aforementioned influences that degrade the signal quality of the output voltage would have to be addressed first. Regarding the voltage measurement, this would required a redesign of the analog front-end of the measurement system in order to establish proper suppression of the switching noise. In addition, a reduction of the voltage drop across the CMCs's leakage inductances caused by the CM currents could be achieved by reducing of the respective stray inductances of the cell's CMCs and implementing the filter inductor L_1 as a distinct component outside the cells.

5.4 Arbitrary Signal Generation

Several additional test waveforms were generated in order to demonstrate the performance of the system, with the results described below. For the

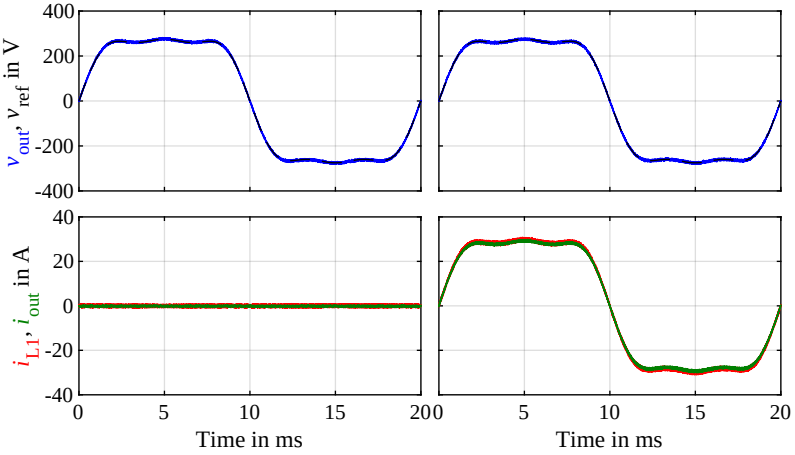


Fig. 5.19: Superposition of three sinusoidal signals (325 V at 50 Hz, 75 V at 150 Hz, 25 V at 250 Hz) used as reference input. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

following examples, again unloaded and loaded operation are shown, with a 9.4 Ω load with a parasitic series inductance of 1 µH being used in all cases.

Fig. 5.19 presents a sinusoidal 325 V amplitude, 50 Hz base frequency signal with a 75 V third harmonic and a 25 V fifth harmonic component superimposed, which could serve as an example for a grid emulation application when emulating low-frequency grid disturbances.

A similar example, however, with significantly higher frequencies is provided in **Fig. 5.20** for a 325 V amplitude, 8 kHz base signal with a 75 V third harmonic added to the reference. Additionally, **Fig. 5.21** presents measurement results for a 300 V amplitude, 10 kHz sinusoidal base frequency signal with a 100 V fourth harmonic included.

Further tests were carried out with two triangular waveforms. In **Fig. 5.22** a 325 V, 10 kHz triangular signal is shown, resulting in a load power of 3.6 kW for the considered load. Finally, **Fig. 5.23** presents a similar measurement for a 300 V, 60 kHz triangular reference, corresponding to 3 kW of load power for loaded operation.

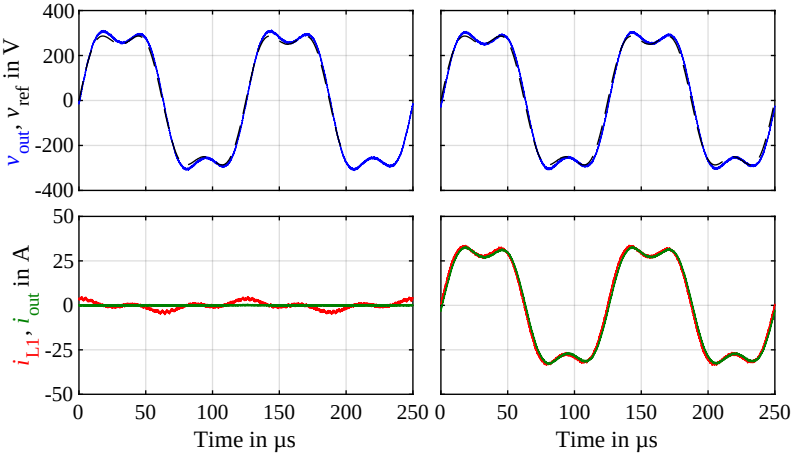


Fig. 5.20: Superposition of two sinusoidal signals (325 V at 8 kHz, 75 V at 24 kHz) used as reference input. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

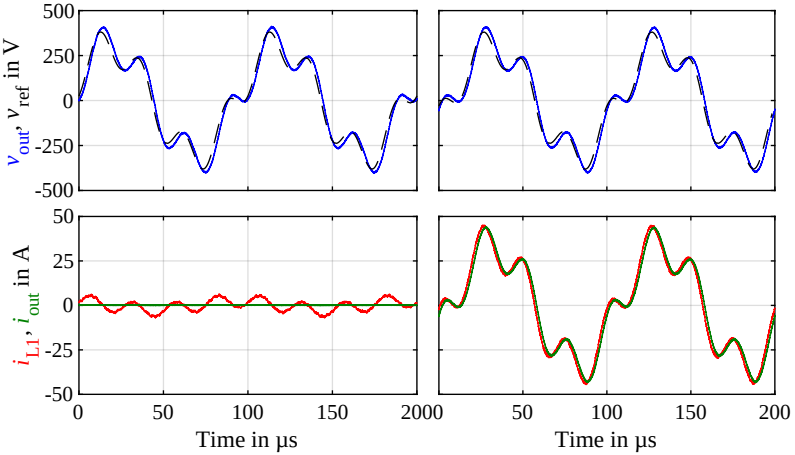


Fig. 5.21: Superposition of two sinusoidal signals (300 V at 10 Hz, 100 V at 40 kHz) used as reference input. Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

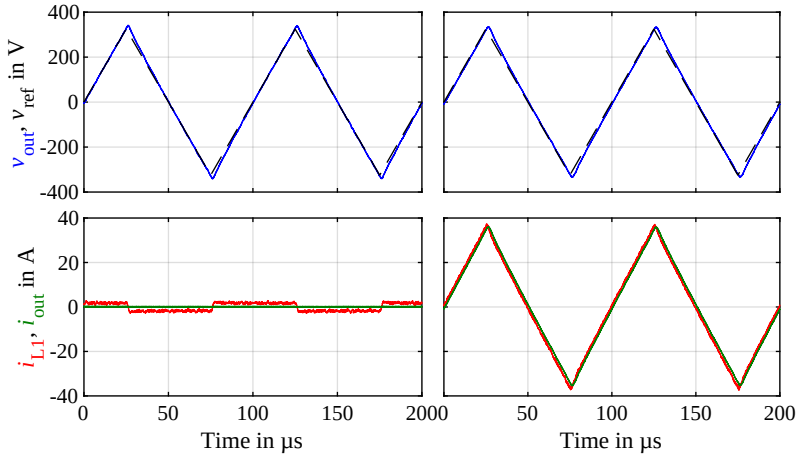


Fig. 5.22: Triangular reference signal (325 V amplitude, 10 kHz). Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

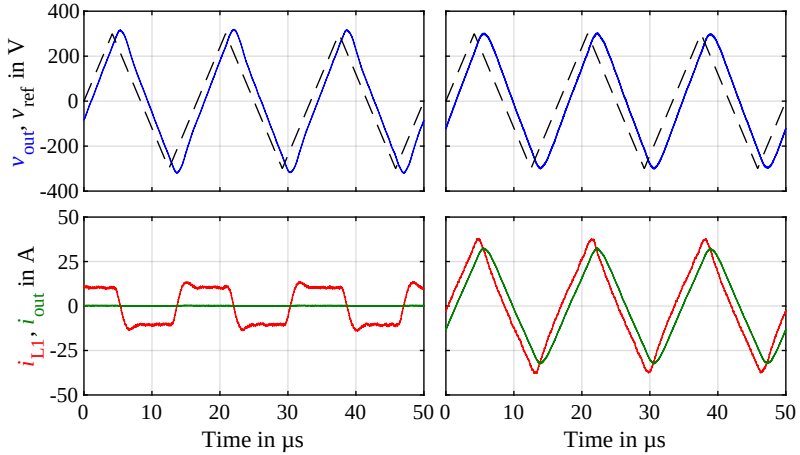


Fig. 5.23: Triangular reference signal (300 V amplitude, 60 kHz). Left: no load, right: 9.4 Ω ohmic load with 1 µH parasitic series inductance.

6

Conclusions and Outlook

High-bandwidth power amplifiers are key components in P-HIL testing facilities used for commissioning, testing and experimental characterization of power electronic converters and devices, where they are used to emulate the behavior of grids, loads or other electrical appliances, thereby serving as physical interface between a simulation model and the real-world device-under-test. Due to the continuously increasing frequencies of the involved dynamic phenomena that have to be covered by these systems, also the bandwidth of the test environment has to adapt accordingly, which reflects in ever-rising performance requirements for the involved amplifiers with targeted output bandwidths in excess of 50 kHz to 100 kHz for output phase voltages of typically 230 V RMS and power levels of several kilowatts and above.

State-of-the-art solutions that are able to fulfill these requirements usually employ linear amplifier structures as these allow to combine very high bandwidths with low output impedances, featuring very good dynamic performance. However, analog amplifiers inevitably suffer from high losses and accordingly low efficiencies. Conventional switched-mode solutions on the other hand do not reach the targeted output bandwidths due to their limited switching frequencies, which require the installation of output filters with low corner frequencies to filter out the switching frequency harmonics. This limits the achievable output bandwidths to significantly lower values than what is achieved by their linear counterparts.

For this reason, in order to overcome the limitations of currently available systems, this thesis focuses on the scientific investigation and development of a switched-mode four-quadrant high-bandwidth power amplifier intended as a test source for P-HIL simulation environments, aiming for large-signal output frequencies of up to 100 kHz and a maximum output power of 10 kW

per phase at a nominal RMS output voltage of 230 V. In the following, the key results of this thesis are summarized and an outlook on further research vectors is provided.

6.1 Results and Conclusions

This thesis starts with a review of different amplifier topologies that are described in the literature, including purely switched-mode solutions, analog amplifiers and hybrid converter topologies that incorporate a combination of either a linear amplifier and a switched-mode stage or of two different (a slow-switching and a fast-switching) digital amplifier stages. Purely switched-mode topologies are preferred over analog amplifiers due to the inherently high losses of analog solutions, which also cannot be entirely avoided in hybrid systems incorporating analog subsystems. On the other hand, digital hybrid systems are considered unfavorable due to their relatively high complexity that originates from the combination of different switched-mode stages. Since even with today's modern WBG devices the necessary switching frequencies required for standard digital amplifiers using the conventional half-bridge topology cannot be achieved, parallel- or series-interleaved multi-level concepts are identified as most suitable for the implementation of a high-bandwidth power amplifier, as both concepts feature high efficiencies and, due to the involved interleaving, high *effective* switching frequencies, thereby enabling high bandwidths over the full output voltage and power range. Considering an equal number of half-bridges and identical switching frequencies of the incorporated semiconductor devices, both (parallel- as well as series-interleaved) concepts provide equal characteristics regarding their switched multi-level output voltages, since the same effective switching frequency and the same number of voltage levels are obtained. However, a further advantage of the series-interleaved topology over parallel-interleaved systems originates from the fact that with series-interleaving the operating voltage of the employed power semiconductors reduces with increasing number of interleaved converter cells, thus allowing to use MOSFETs with lower blocking voltages that enable lower losses and/or higher switching frequencies of the half-bridges. For this reason, a series-interleaved CHB topology was selected for the implementation of the high-bandwidth power amplifier investigated in this work.

The entire design process of a 230 V/10 kW single-phase UH-PBW amplifier featuring a CHB topology is then covered, where the key objectives include the power supply of the CHB cells and its behavior on the grid, the

dimensioning of the CHB switching stage and its output filter and the design of a suitable high performance control system.

Regarding the power supply structure of the amplifier, two independent aspects of a power supply for a generic UH-PBW amplifier were investigated. In a first step, the operating behavior of the converter if operated with low-frequency (i.e., $\ll 50\,\mathrm{Hz}$) single-phase loads is analyzed. It is found that the pulsating power demand of the connected load leads to distortions of the amplifier's grid currents, which is a consequence of the single-phase power pulsation that propagates from the output to the mains side of the system. However, the tolerable LF harmonics of the grid current are limited by grid standards, such as the IEC 61000 flicker and harmonic limits. For this reason, either sufficient decoupling between grid and load power has to be provided, implying a sufficiently large DC-link capacitor to buffer the pulsating power, or the output power has to be derated for certain low output frequencies. This results in a design constraint for the DC-link capacitance and/or a derating profile for the output power of the system, where for the investigated converter employing the CHB topology, a DC-link capacitance of 77 mF for the 100 V DC-link of each converter cell was determined. The resulting system enables operation with the maximum output power over almost the entire output frequency range, where a derating to 80 % of the output power is accepted for a limited output frequency interval from 3.1 Hz to 4.8 Hz in order to guarantee full compliance with the IEC 61000-3-11 and IEC 61000-3-12 harmonic and flicker limitations for all operating points.

In a second step, an advanced multi-port DAB converter structure is investigated as a potential solution for the implementation of a power supply of a CHB converter, aiming for a component count reduction of the isolated DC-DC converters required to supply the CHB cells. The considered structure is obtained from the Integration of Three Dual-Active Bridge (I3DAB) converters into a multi-port topology featuring one common input and three individual output ports, where the primary-side full-bridges of the individual DABs are combined into a common three-phase two-level inverter. On the example of a $3 \times 4\,\mathrm{kW}$ system with input and output voltages of 700 V and $3 \times 100\,\mathrm{V}$, respectively, it is demonstrated that in case of asymmetric loading scenarios of the converter previously unused degrees of freedom in the modulation of the primary-side bridge can be utilized to reduce the conduction losses occurring in the system. This results in the development of a novel modulation scheme that improves the part-load efficiency of the I3DAB, where a reduction of the conduction losses of up to 23 % is predicted. The obtained theoretical findings are experimentally verified by a scaled-down demonstrator

system with a nominal power of $3 \times 2.4\,\mathrm{kW}$. From the experiments an overall good accordance between theoretical analysis and experiments is obtained, although it is found that the magnetizing currents of the transformers that were neglected in the theoretical evaluation introduce minor deviations in the cost function representing the conduction losses. Regarding efficiency, the experimental results reveal improvements of up to 0.5 %, e.g., from 97.5 % to 98 % for asymmetric loading of the three converter ports with 2.4 kW, 200 W and 200 W, respectively.

Considering the design of the CHB amplifier stage, a key objective was to identify the relationship between fundamental design parameters of the CHB inverters, which are the required number of CHB cells, the switching frequency of the inverter bridges and their DC-link voltage and the system's performance, in particular the maximum output frequency. It is shown that a relation between these design parameters can be derived from the maximum large-signal output bandwidth and the required output voltage quality as well as the maximum acceptable reactive power demand of the output filter elements. Considering an upper limitation of the maximum achievable switching frequency of the used silicon MOSFETs due to the occurring switching losses, these relations are then used to determine the key design parameters of the CHB phase stack, where for the investigated 230 V/10 kW UH-PBW amplifier a system consisting of six converter cells with a DC-link voltage of 100 V and a switching frequency of 300 kHz of each half-bridge results. Based on this, the inverter bridges of the CHB cells and the two-stage output filter are then dimensioned, where in case of the output filter a procedure based on a filter design space optimization is employed. The design space optimization allows to determine the optimum filter component values such that the maximum achievable large-signal output bandwidth of the converter for a given switching frequency and number of cells is reached. A maximum output frequency of 83 kHz can be guaranteed over the entire operating range (i.e., up to the maximum peak output voltage of 470 V), enabling output frequencies in excess of 100 kHz if only the nominal peak output of 325 V voltage is considered.

Additionally, the control system of the converter is designed, where a cascaded control structure incorporating an inner current control loop and an outer voltage control loop was selected for the implementation. A multi-objective Pareto optimization approach is employed to determine optimal control gains and to investigate the influence of different load scenarios on the achievable performance. Regarding the implementation of the control system the main focus lies on the minimization of the delay times in the

control loop, thereby suggesting the use of naturally sampled PWM to avoid the sampling delay of the modulator. However, it is found that the half-bridge locking mechanism required to avoid multiple reference crossings of the PWM carrier that would result in an increase of the half-bridge switching frequency above the PWM frequency introduces nonlinear effects that may result in considerably increased overshoot of the output voltage during transients. Therefore, different approaches to mitigate these effects are suggested, with possible solutions including a reduction of the control bandwidth, a slew rate limitation of the reference voltage or the implementation of an advanced PWM modulator that allows for a temporary increase of the switching frequency during transients. For the hardware implementation of the system, an adapted set of control parameters is chosen, resulting in a closed-loop small-signal bandwidth of 155 kHz for operation with nominal ohmic load.

In order to verify the predicted dynamic performance obtained from the theoretical models, a 10 kW single-phase demonstrator system was constructed, featuring a CHB topology with six cells and enabling an effective switching frequency of 3.6 MHz. Each of the cells is operated with a DC-link voltage of 100 V and a switching frequency of 300 kHz. The demonstrator achieves a large-signal bandwidth of 100 kHz under full-load operation, which is verified by an extensive set of measurements that reveal an accurate matching of the dynamic behavior between the linear system model and measurement results, thereby proving that the CHB topology is a well suited option for the implementation of a UH-PBW amplifier.

6.2 Future Research Vectors and Outlook

With the continuously increasing switching frequencies of today's modern power electronic systems and the according faster system dynamics there is a constant need for power amplifiers that feature ever higher output bandwidths. For this reason, the development of high-bandwidth power amplifiers is expected to stay an active field of research, with the key objective of further increasing the achievable bandwidth of these systems.

Considering purely switched-mode topologies due to their superior efficiency over systems involving linear amplifiers, this inevitably requires an increase of the effective switching frequencies and/or the number of voltage levels. A straight-forward approach to accomplish this would be the usage of WBG semiconductor devices that allow for considerably higher switching frequencies of the employed power transistors. This would also justify a re-evaluation of the topology selection presented in this work, since with

the massively increased switching frequencies, simpler converter topologies are also able to meet higher performance requirements, thereby offering the possibility to reduce the complexity as well as possibly the costs of the system compared to an equivalent CHB converter.

At this point, it has to be recognized that independent of the involved topology, further increasing the effective switching frequency of the converter implies frequencies in the range of several tens of megahertz at power levels of several tens of kilowatts and according voltage and current levels. This implies additional challenges regarding the influence of parasitic elements inevitably present in all sorts of electrical components, e.g., the parasitic capacitances and inductances of filter elements, busbars or connectors that connect the CHB cells or HF eddy current losses caused by the magnetic stray field of current-carrying conductors in the vicinity of other conductive parts (e.g., mechanical assembly components). Particularly in the light of a possible industrial implementation, an interesting question would be which additional technical limitations of the effective switching frequency caused by the parasitic elements would arise and how these could be overcome. Concerning the CHB topology this raises the question whether the high degree of modularity offered by the topology which, however, requires a comparably high number of physically distributed connections that are subject to currents and voltages at the effective switching frequency, is still advantageous or whether other topologies that feature a higher degree of integration and thereby a smaller physical size may be beneficial in order to reduce the parasitic elements.

The above mentioned aspects regarding the impact of parasitic elements are not restricted to the internal circuitry of the converter operated at the effective switching frequency. With increasing output bandwidth similar influences also arise for the load systems connected to the amplifier, including the cabling in between as well as safety equipment such as fuses, circuit breakers or contactors. Although the involved frequencies present at the output of the amplifier are significantly lower than the effective switching frequency, as these components are subject to the filtered output signal, it has to be recognized that the physical dimensions of the assemblies connected to the output of the amplifier are generally much larger than the internal structures of the converter, resulting in considerably higher values of the according parasitic elements. A prominent example would be the voltage drop over the parasitic inductance of the cabling connection between amplifier and load, for which advanced control schemes involving an additional external voltage measurement on the load side represent possible solutions to mitigate

this effect [170]. Similarly, the magnetic stray fields of electrical connections may introduce excessive eddy current losses in cables or connector systems, therefore requiring the development of suitable cabling and terminations that are capable of covering the targeted frequency range.

Another interesting aspect in terms of the power hardware is the large DC-link capacitance required to suppress distortions of the grid currents caused by LF single-phase loads. Due to the high volume occupied by this capacitance, the question arises whether a reduction of this capacitance is possible while still being able to comply with the IEC 61000 flicker and harmonic limitations, with a promising concept being power pulsation buffering described in [190] for the elimination of the electrolytic capacitors of a single-phase AC to DC power supply.

Other research vectors refer to the employed control structures and their respective implementation on the control hardware, where interesting questions would be to what extent the control bandwidth of the system could be increased by using more sophisticated control strategies and which control architectures would be suitable to accomplish this. However, possible improvements achieved by advanced control strategies might be limited by the execution times of the respective algorithms. For this reason, a careful tradeoff between computation time and possible improvements is essential, where the continuously growing computational power of modern digital signal processing platforms might offer new opportunities to cover numerically intense algorithms. In this regard, also a deeper investigation of the effects of the delay compensation scheme cited in this work would be desirable. Additionally, an aspect which was not investigated in this thesis involves the quantization noise caused by the limited resolution of the digital PWM modulator that is a consequence of the maximum clock frequency of the employed FPGA. Since the quantization step size of a digital PWM modulator is directly proportional to the ratio of PWM carrier and FPGA clock frequency, higher half-bridge switching frequencies (e.g., due to using WBG devices) imply coarser PWM quantization step sizes, thereby increasing the quantization noise. For this reason, noise reduction techniques, e.g., noise shaping [266], might be required.

Finally, it has to be recognized that the high-bandwidth power amplifier developed in this thesis exhibits a voltage-source characteristic, whereas in P-HIL applications also current-source characteristics or the emulation of a predefined impedance over a wide frequency range is desirable. For this reason, a detailed investigation on the extension of the control structure to allow operation as a current source or the emulation of impedances [170] over

a wide frequency range would be an interesting subject for future scientific work.

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Education

2017 – 2022	Doctorate, ETH Zurich Power Electronic Systems Laboratory (PES)
2014 – 2016	MSc ETH (with distinction), ETH Zurich Information Technology and Electrical Engineering
2011 – 2014	BSc ETH, ETH Zurich Information Technology and Electrical Engineering
2002 – 2010	High School, Bundesgymnasium Lustenau, Lustenau, Austria

Work Experience

2016 – 2021	Research Assistant, ETH Zurich Power Electronic Systems Laboratory (PES)
2012 – 2016	Teaching Assistant (Digital Circuits, Mathematics III: Partial Differential Equations, Electromagnetic Fields and Waves, Electrical Engineering I), ETH Zurich