A Novel Control Concept for Operating a Two-Stage D-Rectifier-Based Telecommunications Power Supply Module under Heavily Unbalanced Mains Voltage Conditions

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Abstract – In this paper a novel control concept for a unity power factor three-phase AC/DC two-stage telecommunications power supply system is proposed. The system is formed by an input-side delta-connection of three single-phase modules with parallel connected DC outputs. The control concept features output voltage control, module load sharing and mains voltage proportional guidance of the input currents and does allow to continue in operation also in case of heavily unbalanced mains voltage condition like given for missing mains phase or in case of an earth-fault of a mains phase or for a short circuit between two mains phases.

1 Introduction

High power telecommunications power supply modules are typically designed for a rated output power of $P_{O,max}$ = 48V · 200A = 10kW and do show a two-stage topology where a front-end three-phase unity power factor rectifier supplies a DC/DC converter output stage.

For the realization of a three-phase unity power factor rectifier in [1] the topology depicted in **Fig.1** has been proposed which is characterized by an input-side delta-connection of three single-phase rectifier modules (Δ-Rectifier). Single-phase unity power factor rectifier modules are highly developed and well known in the industry. Furthermore, the Δ-Rectifier shows the advantage of high modularity, which does facilitate manufacturing and according to [1] does provide a very low RMS value of the mains current ripple. Also it is characterized by a low voltage stress on the power transistors and the free-wheeling diodes and/or a low realization effort. Therefore, the realization effort of the power circuit which is very much comparable to a direct-three-phase rectifier system realization, i.e. the Vienna Rectifier, [2].

In this paper a novel concept for controlling a three-phase telecommunications power supply employing a -Rectifier as input stage is proposed. The control concept does tolerate heavy mains voltage unbalance and/or two-phase operation as described in more detail in **section 2**. In **section 3** the system behavior will be analyzed for symmetric and heavily unbalanced mains voltage conditions including two-phase operation (missing mains phase) and for assuming an earth fault (short circuit between one phase and the neutral) by digital simulation.

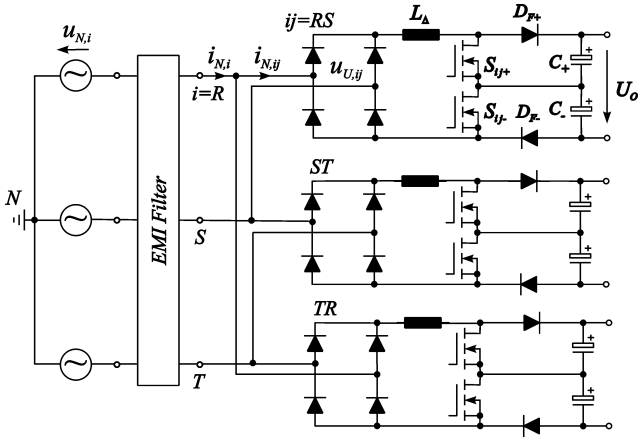

Fig.1: Basic structure of the power circuit of a three-phase boost-type unity power factor rectifier formed by input-side delta-connection of three single-phase three-level power factor corrected rectifier modules (three-level *D-Rectifier*).

2 System Control

Figure 2 shows the proposed structure of the control of a three-phase Δ-Rectifier-based telecommunication power supply module, which is able to handle heavily unbalanced mains voltage conditions.

The cascaded system control is organized in a multi-layer structure as also employed in power electronic building blocks (PEBB) [3]. Corresponding to the dominant time constants there are four layers:

- Hardware manager: transistor gate-drive, current sensors, fast protection (<1µs);
- Topology manager: current control, hardware interfaces, communication backbone, synchronization and power management of the line-to-line modules (<100µs);
- Application manager: mains frequency current shaping, conventional protection, output voltage control (<10ms);

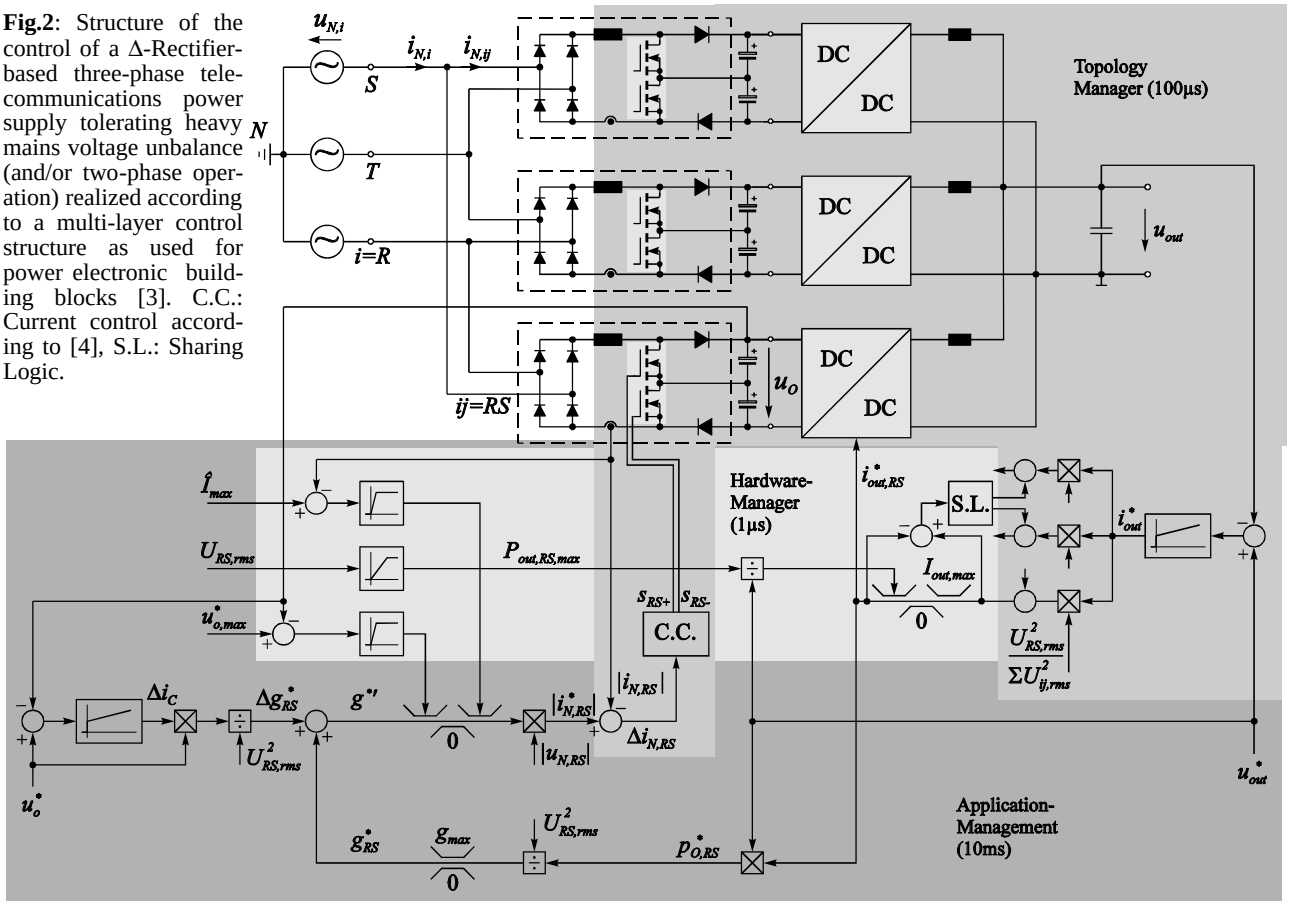

Fig.2: Structure of the control of a Δ-Rectifier-based three-phase telecommunications power supply tolerating heavy mains voltage unbalance (and/or two-phase operation) realized according to a multi-layer control structure as used for power electronic building blocks [3]. C.C.: Current control according to [4], S.L.: Sharing Logic.

- System manager: communication to central supervising unit, power management.

The switching functions s_{ij+} and s_{ij-} of each line-to-line module of the power supply are generated by an inner average current mode control [4]. The inner line-to-line current control loops do employ current reference values $i_{N,ij}$*, *ij = RS, ST, TR*, which are generated by multiplying a reference conductance *g*'* with the actual absolute values of the line-to-line voltages $|u_{N,ij}|$. The conductance *g*'* is defined by the DC/DC converter output voltage control and by the module output voltage controller Δg_{ij}^* (both realized as PI-type controllers with anti-windup), i.e. $g^{*\prime} = g^* + \Delta g_{ij}$. Highly dynamic limiting of *g*'* is provided in order not to exceed the maximum allowable peak current stress $\hat{I}_{max}$ of the power semiconductors and/or a maximum level $u_{o,max}$ (as defined by the voltage rating of the electrolytic capacitors and by blocking capability of the power semiconductors) of the rectifier module output voltage in case of, e.g. a load dump or in case of the return of a missing mains phase. The reference conductance g_{ij}^* which corresponds to the mains-side reference input conductance for the line-to-line rectifier modules, in order to fulfill the output power requirement, is derived from each DC/DC converter output power reference value $p^*_{o,ij} = i_{out,ij}^* u_{out}^*$ by a division by the square of the input line-to-line voltage rms value. The limitation of g_{ij}^* to g_{max} is with reference to the line-to-line mains voltage in order not to exceed $\hat{I}_{max}$ in the stationary case.

A special issue of the realization of a three-phase unit by combination of three line-to-line modules is the division of the output voltage controller output (total output current/power reference value) into reference values of the output currents $i_{out,ij}^*$ of the DC/DC converters connected to the individual line-to-line modules. The calculation of $i_{out,ij}^*$ is performed by multipliers considering the squares of the normalized input line-to-line voltages. The multipliers are shown in Fig.2 on the left-hand-side of the output voltage controller. This load sharing strategy ensures an ohmic mains behavior of the three-phase converter input. However, for a mains voltage unbalance this sharing strategy does limit the maximum output power level already at slight input voltage unbalance conditions, because there is one DC/DC converter running into its output current limit. An improved strategy does distribute the excessive power demand in this case to the DC/DC converters which are not running already at their power and/or current limit. However, one has to take into account that this strategy does not allow to keep the symmetric ohmic mains condition.

A symmetric ohmic mains behavior is only one possibility of a load sharing strategy. In case the system is not operating at the power limit the sharing of the output power does provide a degree of freedom which could be used for operating the system in the point of maximum total efficiency or at a point where all current, voltage and temperature stresses do lead to the maximum reliability of

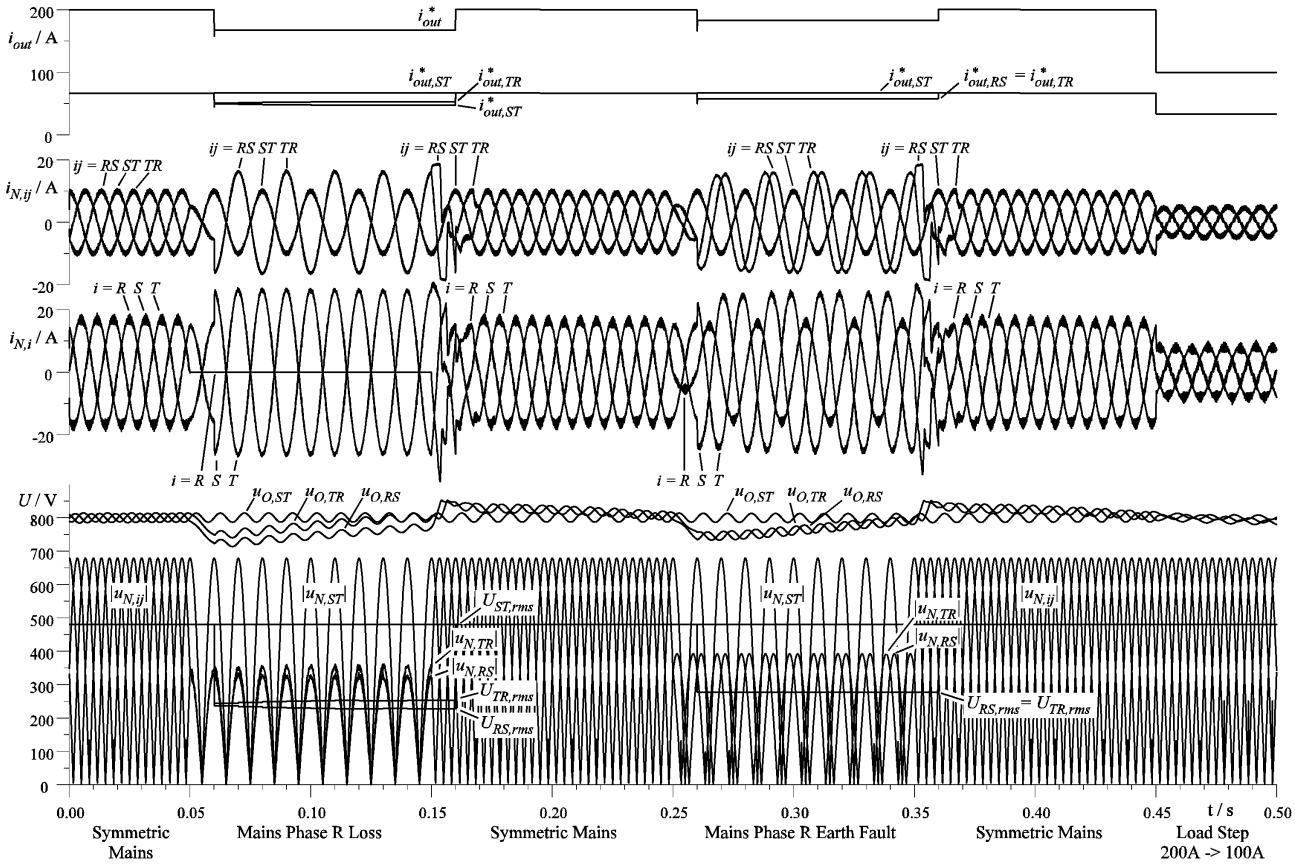

Fig.3: Time behavior of the total output reference current i_{out}*, the individual output currents $i_{out,ij}$* (*ij=RS, ST, TR*), the line-to-line currents $i_{N,ij}$ (*ij=RS, ST, TR*), the phase currents $i_{N,i}$ (*i=R, S, T*), the individual rail voltages $u_{O,ij}$ (*ij=RS, ST, TR*), the absolute values of the line-to-line voltages $|u_{N,ij}|$ (*ij=RS, ST, TR*) and the rms values of the line-to-line voltages $U_{ij,rms}$ (*ij=RS, ST, TR*) for symmetric mains conditions, mains phase R loss, mains phase R earth fault and a load step i_{out} = 200A -> 100A.

the system, i.e. the "mean time between failure" (MTBF) rate is at a maximum.

The output current reference values $i_{out,ij}^*$ are limited according to the maximum admissible output current $I_{out,max}$ of the DC/DC converters as defined by the system design and are decreased in case the rectifier module input rms voltage $U_{ij,rms}$ goes under the minimum level of the defined input voltage range according to the converter dimensioning.

3 Digital Simulation

The results of the digital simulation of the control for a system with a nominal output power of $P_O = u_{out}\ i_{out}$ = 50V * 200A = 10kW operating at balanced and unbalanced three-phase mains (480V_{rms} line-to-line voltage) are shown in **Fig.3**. The converter is designed for a input line-to-line voltage range of $U_{ij,rms}$ = 320 … 530V and does decrease the output power linearly to P_O = 0W @ $U_{ij,rms}$ = 0V. The digital simulation does analyze the following mains and load conditions:

0 … 50ms: symmetric mains.

50 … 150ms: two-phase supply (mains phase loss).

150 … 250ms: return of the missing mains phase.

250 … 350ms: earth fault of a mains phase.

350 … 450ms: removal of the earth fault (return to the symmetric case).

450 … 500ms: load step i_{out} = 200A → 100A with symmetric mains conditions.

Figure 4 shows the time slot of t = 40ms … 80ms of Fig.3 with increased time resolution. At t = 50ms the loss of the mains phase R does occur. The calculation of the rms values of the mains line-to-line voltages does require a minimum calculation time of $t_{C,rms}$ = 10ms what results in a temporarily false value of the conductances g_{ij}* and Δg_{ij}* (*ij* = *RS* and *TR*). These wrong values do cause a significant drop of the rail voltages $u_{O,RS}$ and $u_{O,TR}$ during the time period t = 50 … 60ms. As soon as the rms values are calculated correctly the rapid fall of the rail voltages is stopped due to the step-like increased values of the line-to-line currents $i_{N,RS}$ and $i_{N,TR}$. The individual rail voltage controllers, which are realized as of anti-windup proportional-integral-(PI)-type, do compensate this excessive drop.

The module connected between phases *S* and *T* is not influenced by the loss of phase *R*. The circuit simulated in the case at hand does distribute the excessive power demand of module *ij* = *ST* to the remaining modules *ij* = *RS*, *TR* in equal shares. The converter system is then able to handle an output power of P_O = 8.33kW what corresponds to 83.3% of the rated power of the system for a mains voltage of 480V_{rms} line-to-line.

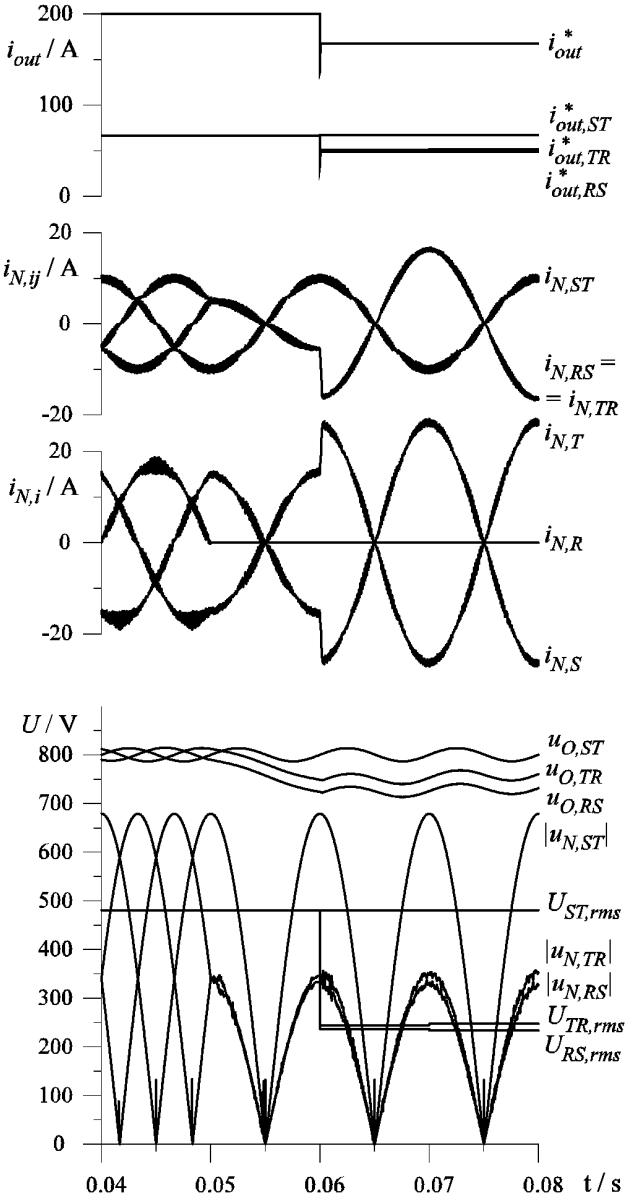

Fig.4: Section of the overall time behavior shown in Fig.3 around the instant in time where the mains phase R loss does occur (t = 50ms). Special attention has to be paid to the measurement of the rms values of the mains voltages which is delayed by 10ms in order to perform the rms value calculation.

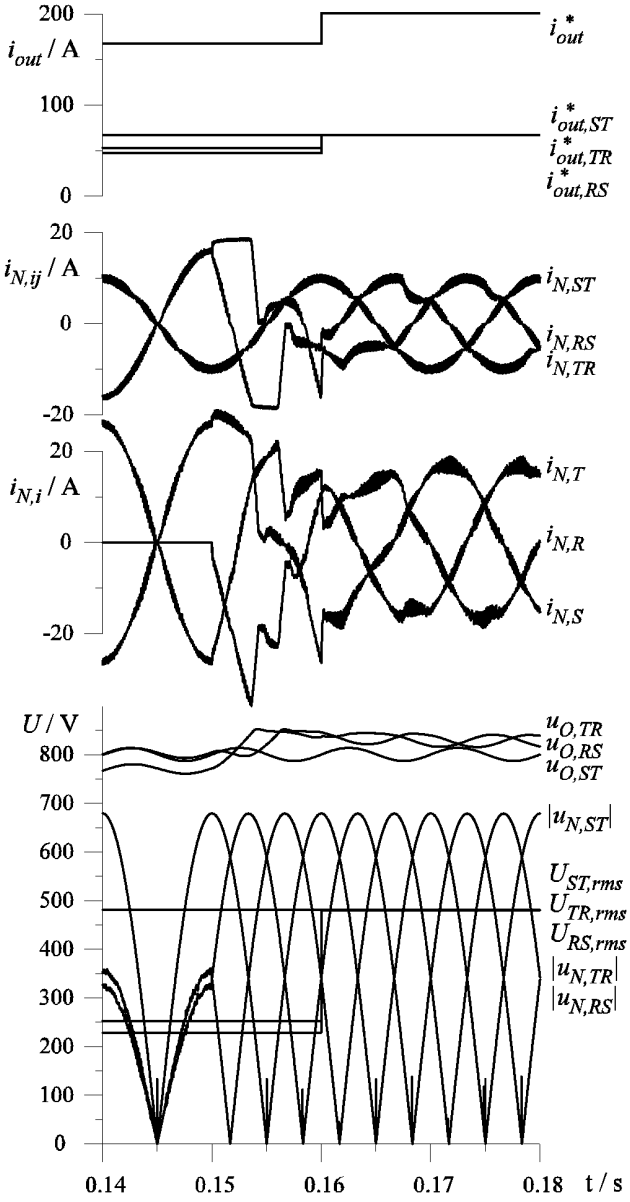

Fig.5: Section of the overall time behavior shown in Fig.3 around the instant in time where the mains phase R does return (t = 150ms). Special attention has to be paid to the current limit of the line-to-line currents $i_{N,RS}$ and $i_{N,TR}$ and to the rail voltage limit of $u_{O,RS}$ and $u_{O,TR}$ where the actual rms value of the line-to-line voltage temporarily is calculated incorrectly.

A detailed view on the return of the missing phase R at t = 150ms is given in **Fig.5**. The line-to-line currents $i_{N,RS}$ and $i_{N,TR}$ do increase very rapidly because of the large values of the conductances g_{ij}* and Δg_{ij}* (ij = RS and TR) which were previously necessary to fulfill the output power demand at low rms values $U_{RS,rms}$ and $U_{TR,rms}$ of the resulting line-to-line voltages. The line-to-line currents are limited by the current limit function according to Fig.2 to a value of $\hat{I}_{max}$ = 19A. The excessive line-to-line current values do cause an overshoot of the rail voltages $u_{O,RS}$ and $u_{O,TR}$ what activates the overvoltage limit function approximately at t = 153ms … 160ms. The discontinuity of the mains voltage is completely handled by the converter system within a time span of 30ms (t = 180ms). The nominal output power of P_O = 10kW is available 10ms after the return of the missing phase R.

The behavior for an earth fault of phase R (cf. **Fig.6**) is very much comparable to the case of a phase loss shown in Fig.4. The main difference is the exact input voltage definition of the influenced line-to-line modules in contrast to the series connection of the line-to-line modules in the case of a phase loss. Again the delayed calculation of the rms values $U_{RS,rms}$ and $U_{TR,rms}$ of the input voltages does cause a drop of the DC link capacitor voltages within the time interval t = 250 … 260ms. The output power available in the case of an earth fault is P_O = 9.16kW and/or 91.6% of the rated output power.

The removal of the earth fault (cf. **Fig.7**) is comparable to the returning of a missing phase shown in Fig.5. The converter system first is running into the current limit and then into the rail voltage limit.

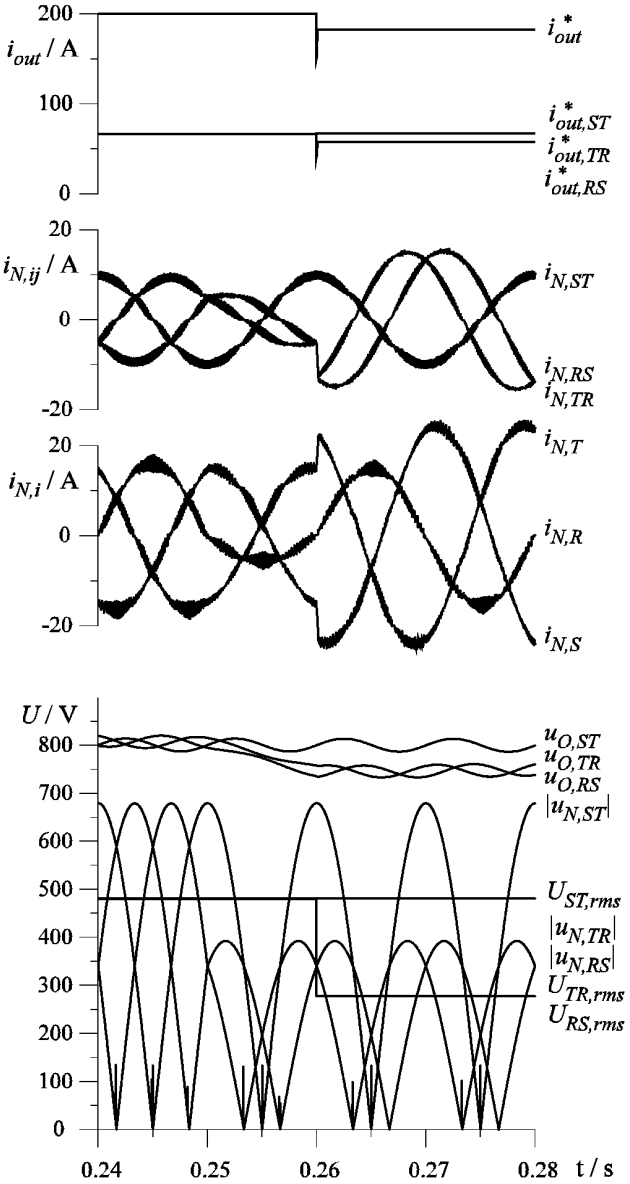

Fig.6: Section of the time behavior shown in Fig.3 around the instant in time where the mains phase R earth fault does occur (t = 250ms). Special attention again has to be paid for the calculation of the rms values of the mains line-to-line voltages which does cause a delay of 10ms in the conductance calculation.

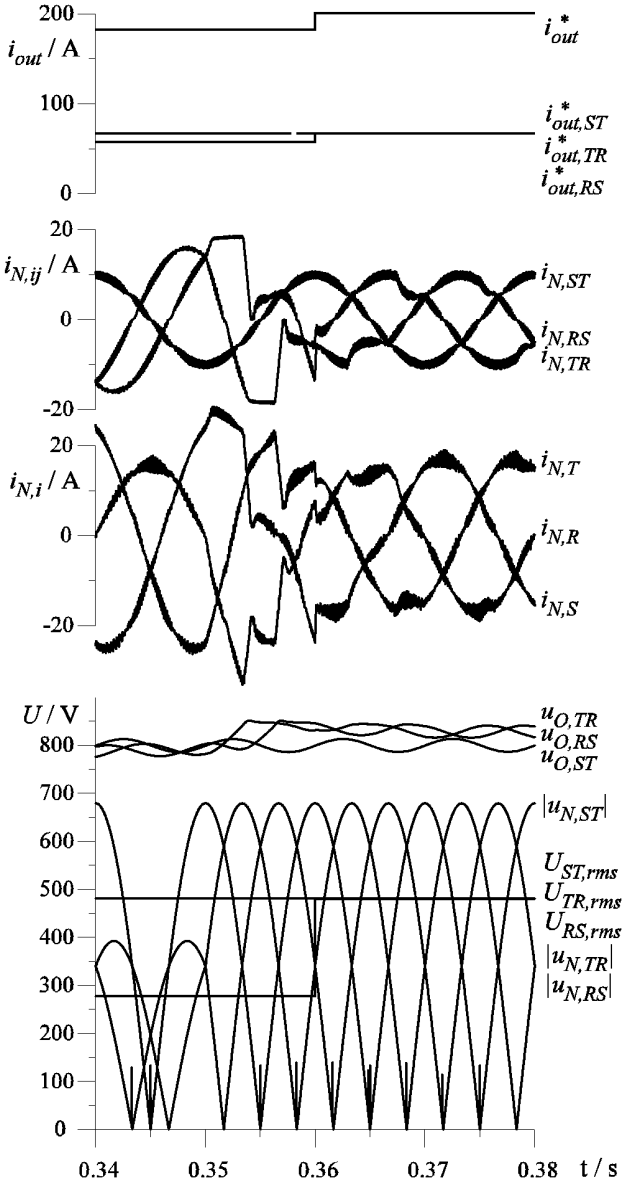

Fig.7: Section of the time behavior shown in Fig.3 around the instant in time where the mains phase R earth fault is removed (t = 350ms). Special attention has to be paid to the current limit of the line-to-line currents $i_{N,RS}$ and $i_{N,TR}$ and the rail voltage limit of $u_{O,RS}$ and $u_{O,TR}$ where the actual rms value of the line-to-line voltage is not yet calculated correctly.

The stationary case is reached again after approximately 30ms at t = 380ms.

A load dump at t = 450ms (cf. Fig.3) is completely handled by the output power pre-control path $p_{O,ij}$ (ij = *RS*, *ST*, *TR*) according to Fig.2 and therefore needs not to be investigated in more detail.

4 Conclusion

As this paper shows the Δ-Rectifier is an interesting alternative to competing rectifier concepts especially under consideration of mains voltage unbalances. The converter system does incorporate a degree of freedom in the input conductance value calculation which does allow to have an increased output power level for unbalanced mains conditions as compared to direct three-phase rectifier systems. The dynamic performance of the Δ-Rectifier at mains voltage discontinuities could be further improved by a faster determination of the mains condition based on the absolute value of the mains voltage space vector what will be a topic of the future research at ETH Zurich besides a practical verification of the simulation results given in this paper.

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