ETH zürich

4.8 MHz GaN Class-D Power Amplifier and Measurement Systems for Next Generation Power Electronics

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Infineon TechTalk

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Next Generation Power Electronics (NGPE)

- Transition to a Net Zero Emissions Society relies on highly efficient power conversion/processing technologies
- Lower functional volume and faster dynamics required

▼ High-Speed Drive ▼ PV/Wind Inverter ▼ SST ▼ EV Drivetrain ▼ EV Charger





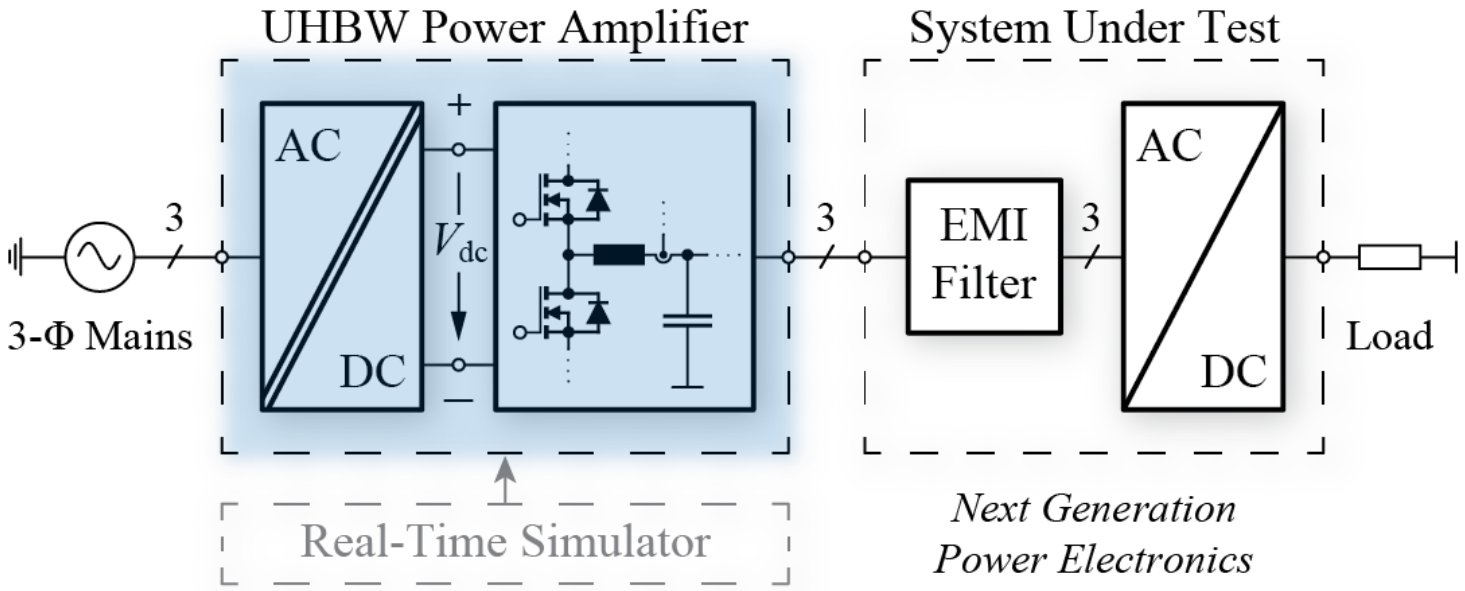
→ Realized with increased switching frequencies

Outline

- Challenges resulting from increased switching frequencies up to the multi-MHz range

- Converter Design and Testing

- Measurement Technology
  - I-Measurement
  - Isolated V-Measurement

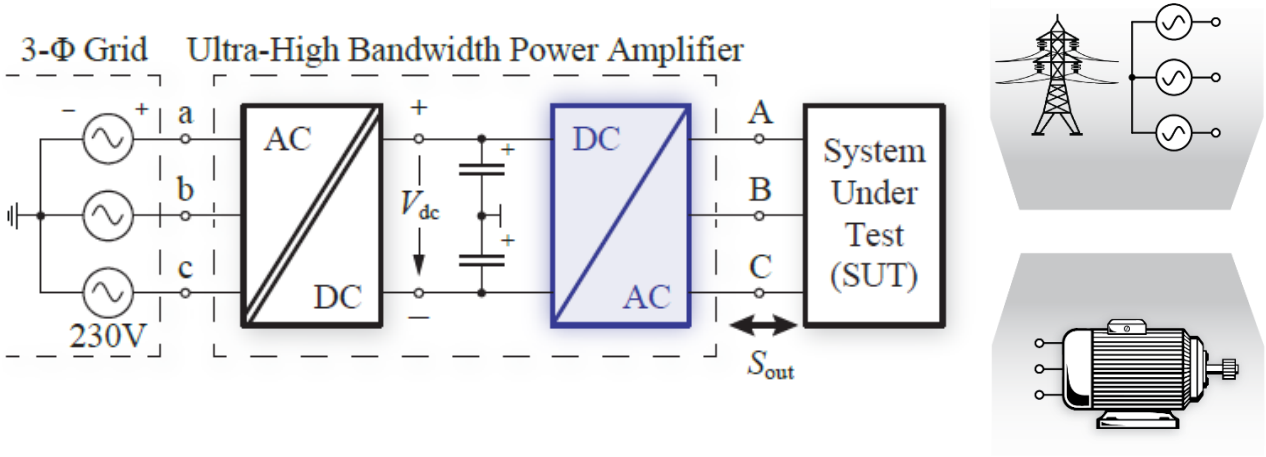


100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier

Very High Power Density Converter Systems with Multi-MHz Switching Frequencies

UHBWPA: Applications + Specifications

- P-HIL → Three-phase Ultra-High Bandwidth Power Amplifier (UHBWPA)
- Focus on single-phase module of DC/AC stage



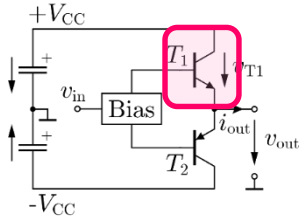
▼ UHBWPA Specifications

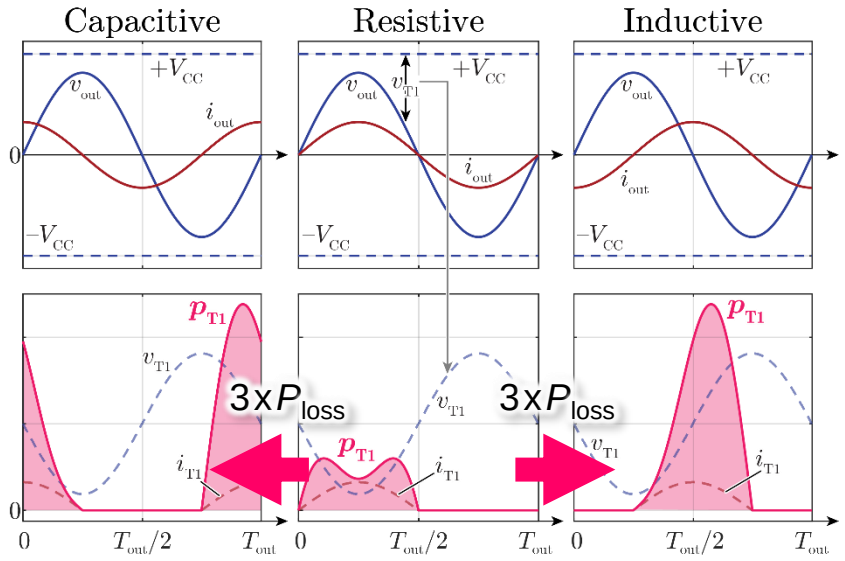
Parameter		Value
Peak Output Voltage per Phase	$V_{out,pk}$	0 . . . 350 V
Output Frequency	f_{out}	dc. . . 100 kHz
Output Power per Phase	S_{out}	0 . . . 10 kVA
DC Link Voltage	V_{dc}	800 V
Effective Switching Frequency	$f_{sw,eff}$	4.8 MHz
System Efficiency (Nom. Op. Pt.)	η	95 %

→ Fast dynamics (100 kHz) and high efficiency (95 %) at nominal power of 10 kW per phase

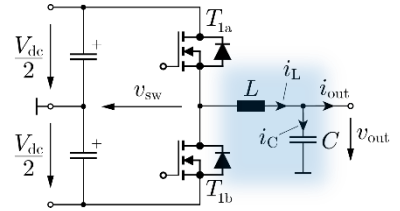
UHBWPA: Linear vs. Switch-Mode

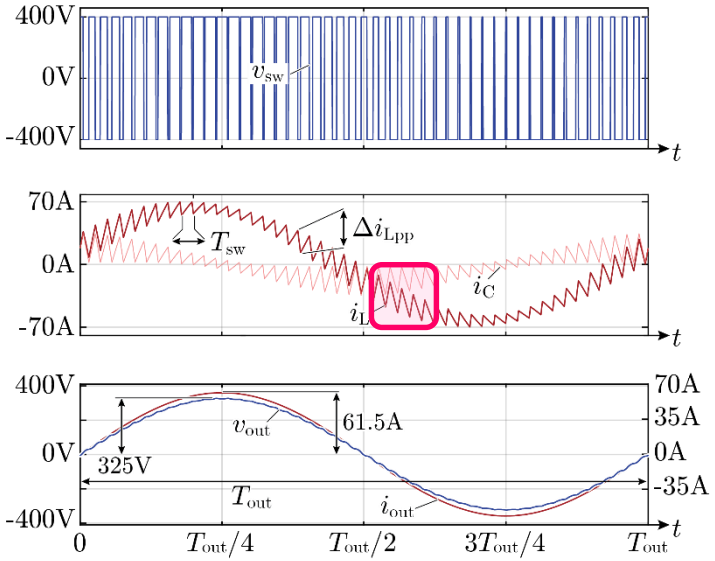
▼ Linear UHBWPA





▼ Switch-Mode UHBWPA



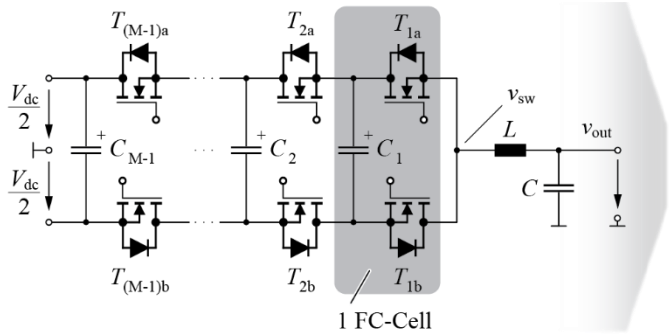


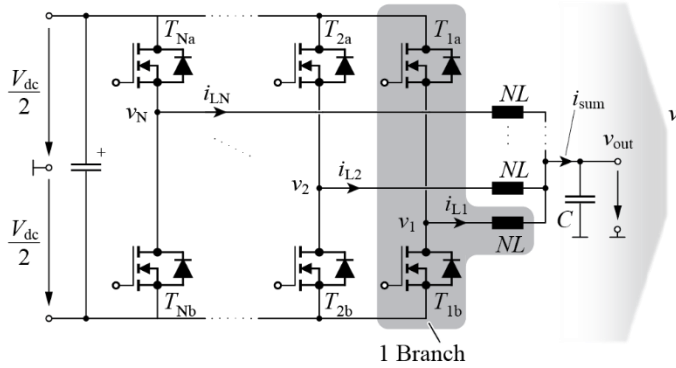
→ Switch-mode for higher efficiency → 100 kHz BW needs ≈5 MHz sw. frequency (1-stage filter)

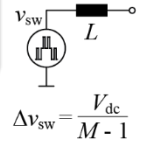
→ Advanced topology to increase f_{sw} with minimal losses and to reduce ripple with minimal volume

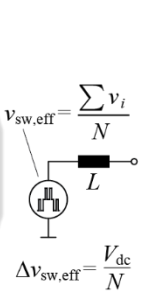
Advanced Circuit Topology

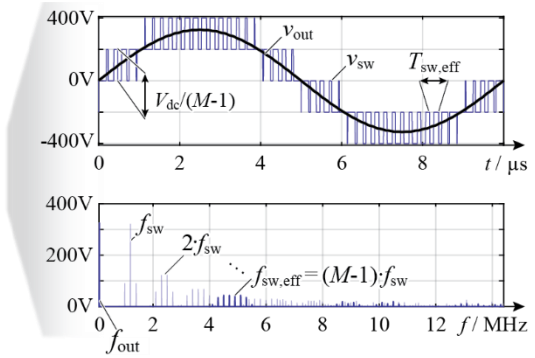
- Series & Parallel interleaving
- Multi-level switch-node voltage + very high effective switching frequency

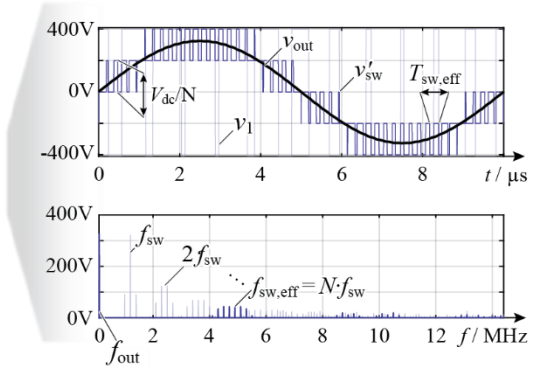


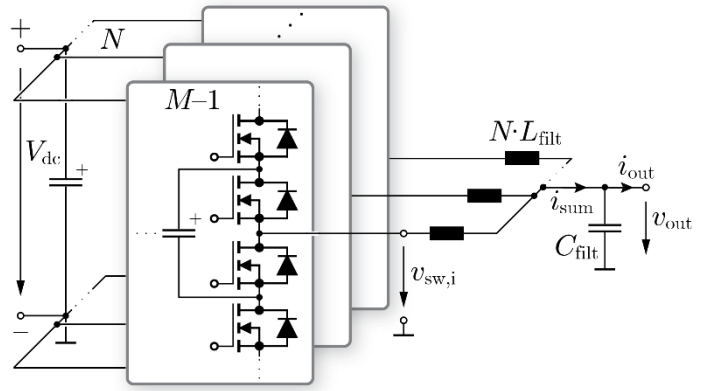












$$\Delta v_{sw,eff} = V_{dc} / ((M-1) \cdot N)$$

$$f_{sw,eff} = (M-1) \cdot N \cdot f_{sw}$$

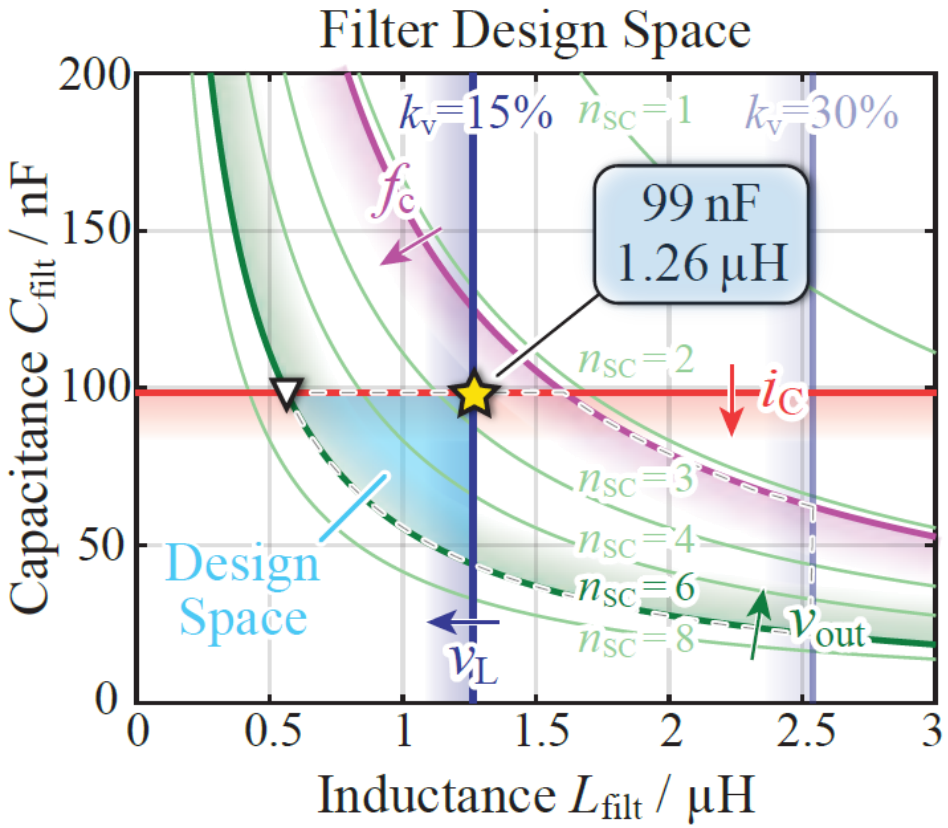
→ Find best combination of series (*M*) and parallel (*N*) interleaving

Output Filter Design

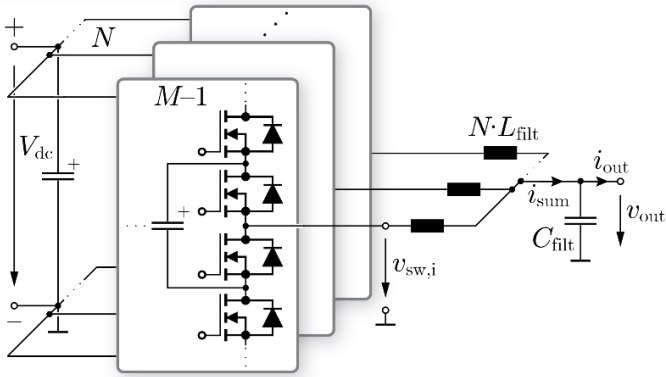
- Nominal operating point
  - 230 V_{rms}, 10 kW, 100 kHz
- Fixed $f_{sw,eff}$ = 4.8 MHz
- Filter design space
  - Max. BW → min. f_c
  - 1% max. output volt. ripple
  - 15% max. ind. volt. drop
  - 30% max. cap. current

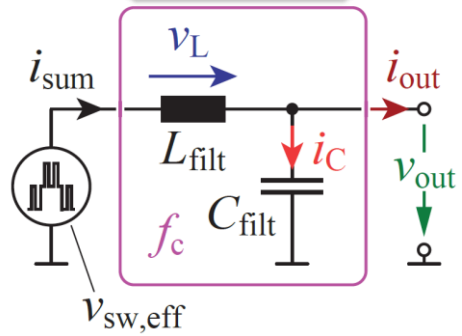
★ L_{filt} = 1.26 µH, C_{filt} = 99 nF
  - → $L_{br} = N \cdot L_{filt}$ = 3.8 µH

▽ L_{filt} = 0.6 µH, C_{filt} = 99 nF
  - Volume minimal filter



$f_{sw,eff}$ = 4.8 MHz

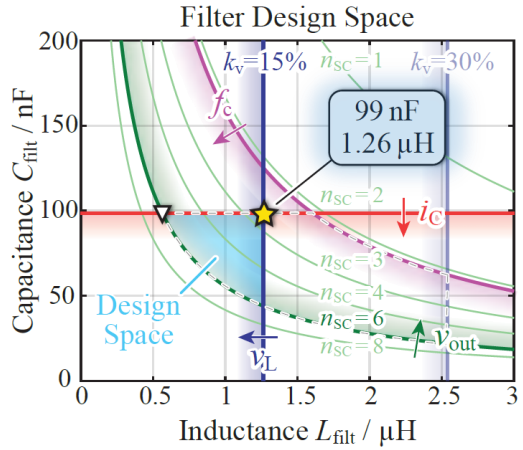


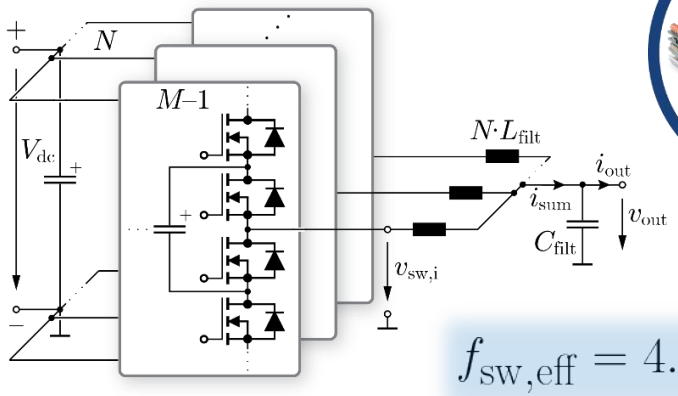


→ Find best combination of series (*M*) and parallel (*N*) interleaving with given output filter and $f_{sw,eff}$

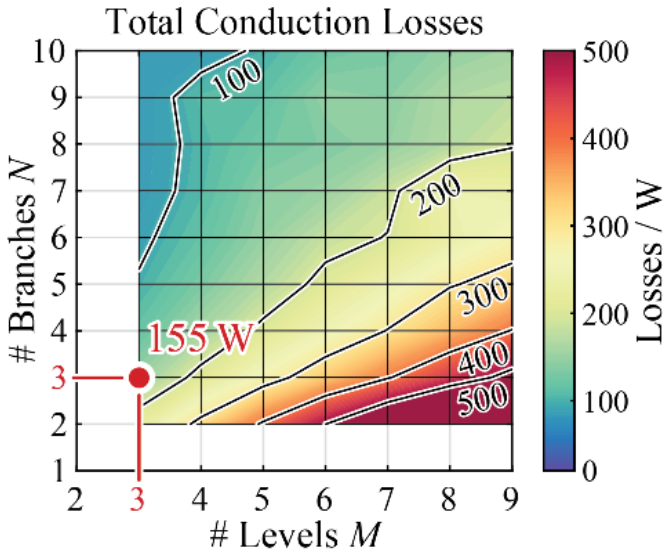
Optimal Design Selection

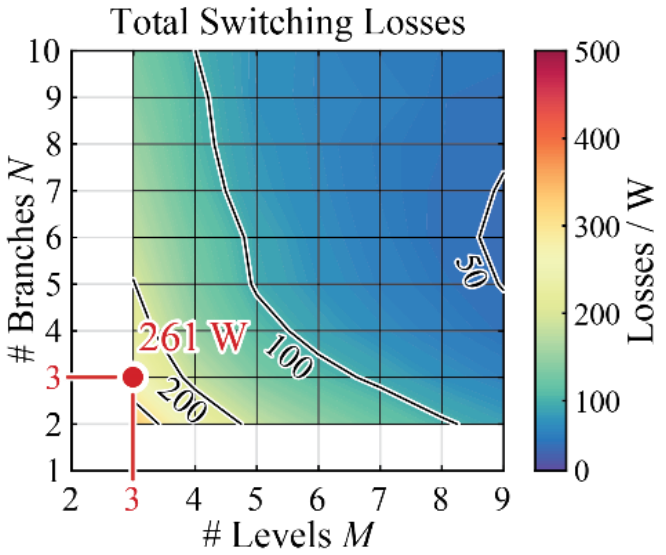
- Filter design space
  - L_{filt} = 1.26 µH, C_{filt} = 99 nF
- Nominal operating point
  - 230 V_{rms}, 10 kW, 100 kHz
- 70 mΩ / 600 V GaN HEMT
  (IGOT60R070D1)

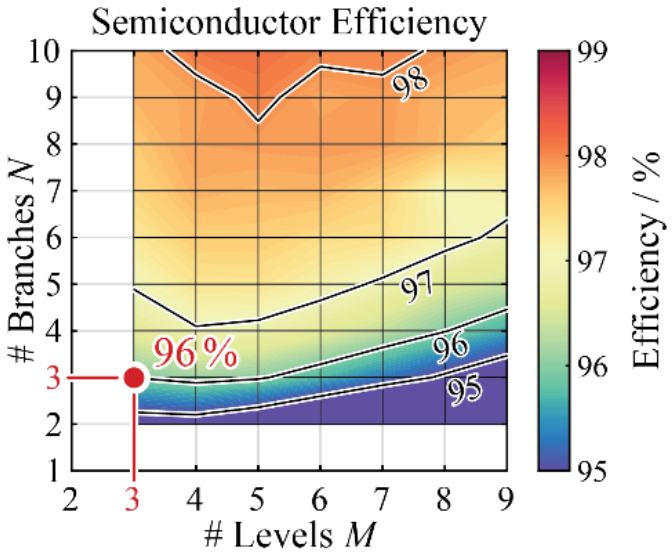




$f_{sw,eff} = 4.8\,\text{MHz}$



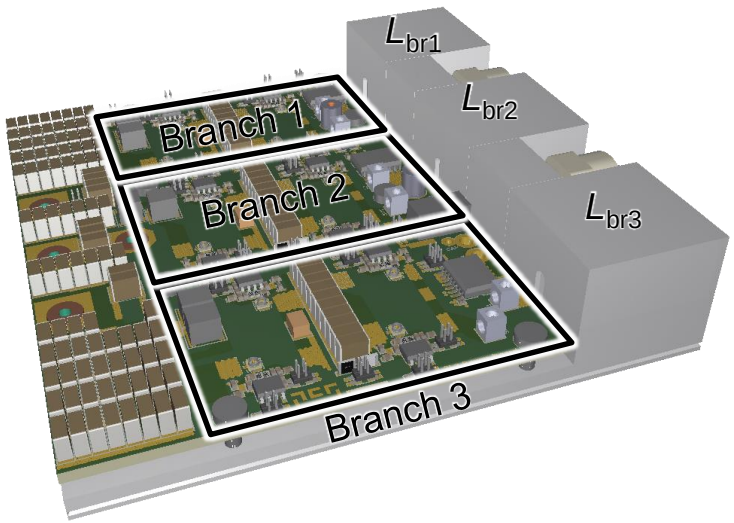




→ Selection of $M=3$ / $N=3$ considering efficiency / filter volume / design complexity trade-off

Hardware Demonstrator – CAD

- $M=3$ / $N=3$ hardware single-phase 10 kW demonstrator
- $f_{sw,eff}$ = 4.8 MHz (800 kHz per device)
- Modular layout of $N=3$ branches

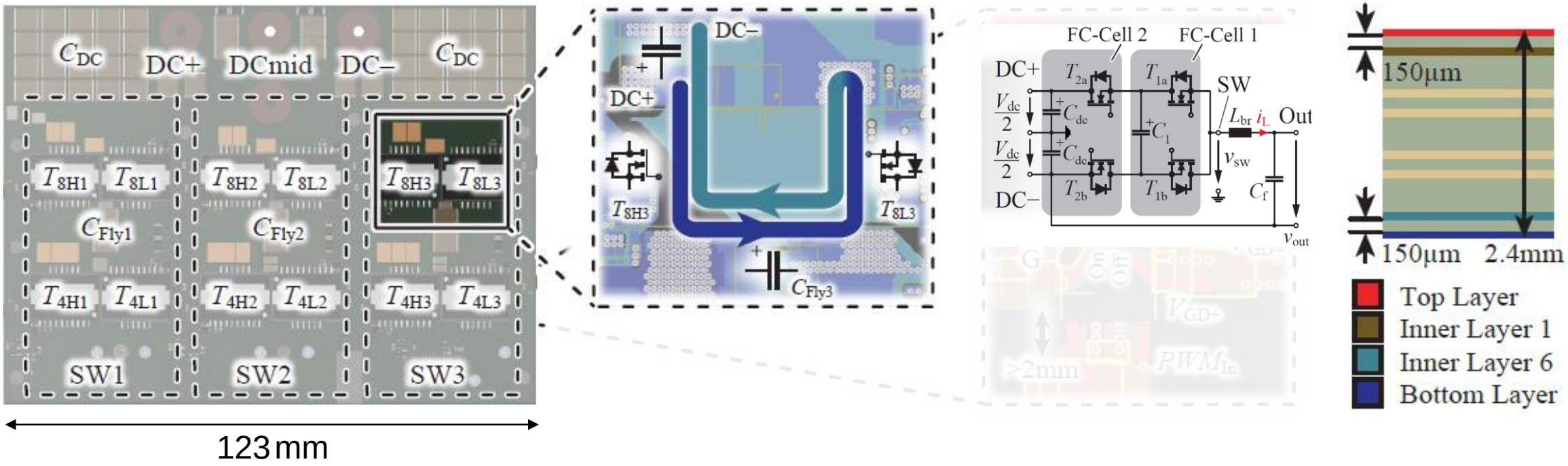


Power PCB — Measurement PCB — Control PCB

→ Three vertically stacked PCBs to maximize power density and signal integrity

Power PCB – Power Commutation Loop

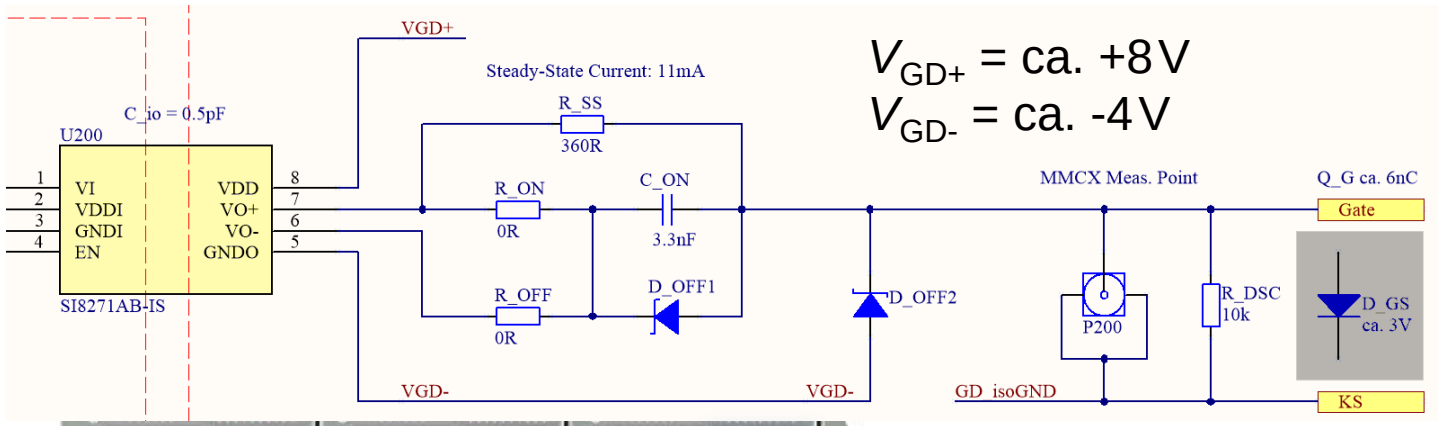
- Top-side cooled power semiconductors placed on bottom-side
- Minimum power commutation loop → Coplanar arrangement on two adjacent layers
  → Exemplary shown for T_{8H3} and T_{8L3}

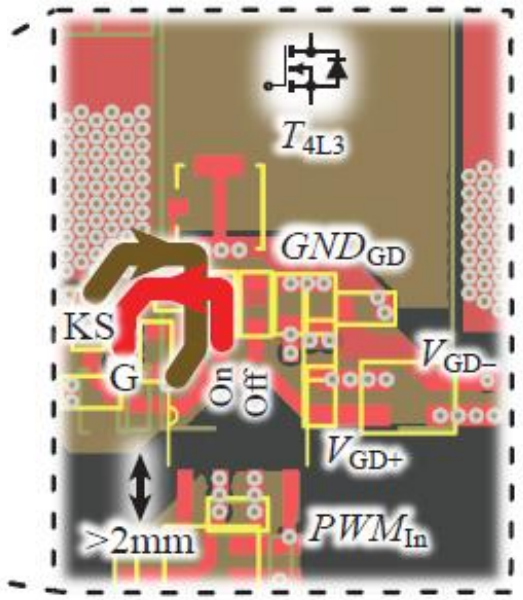


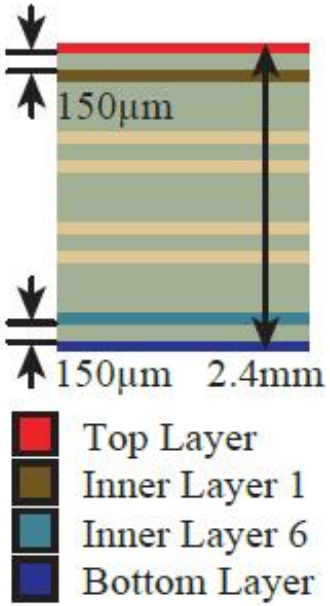
→ Power loop inductance <2.2 nH (outer sw. cell) / <1.5 nH (inner sw. cell) (device: $L_{DS,int}$≈3.5 nH)

Power PCB – Gate Commutation Loop

- Gate-Drivers placed on top-side (adjacent to each switch)
- Minimum turn-on/off commutation loop → Coplanar arrangement on two adjacent layers
  → Exemplary shown for T_{4L3}





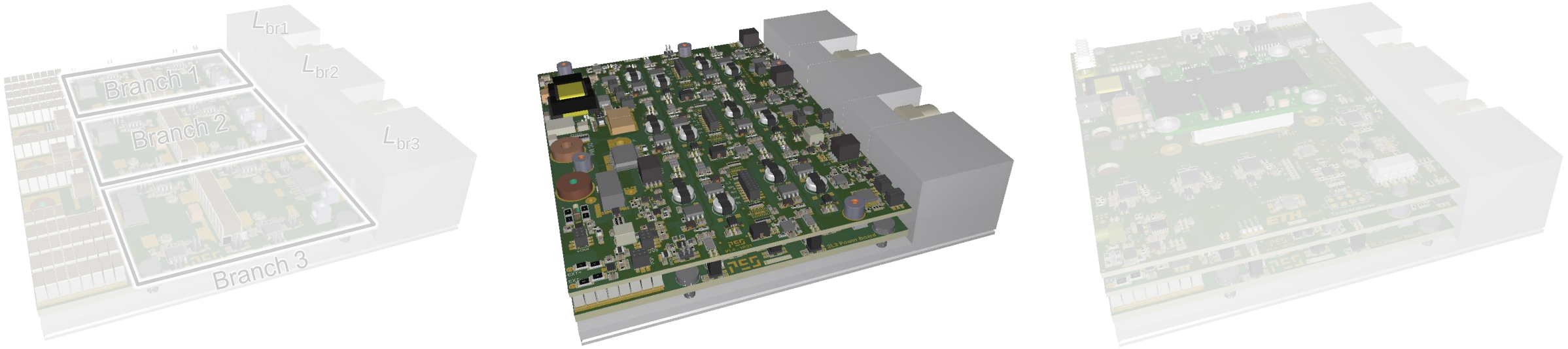


→ Gate loop inductance ≈3 nH (on-path) / ≈4 nH (off-path) (device: $L_{GS,int}$≈7 nH (!))

→ No parasitic turn-on

Hardware Demonstrator – CAD

- $M=3$ / $N=3$ hardware single-phase 10 kW demonstrator
- $f_{sw,eff}$ = 4.8 MHz (800 kHz per device)
- Modular layout of $N=3$ branches



Power PCB — Measurement PCB — Control PCB

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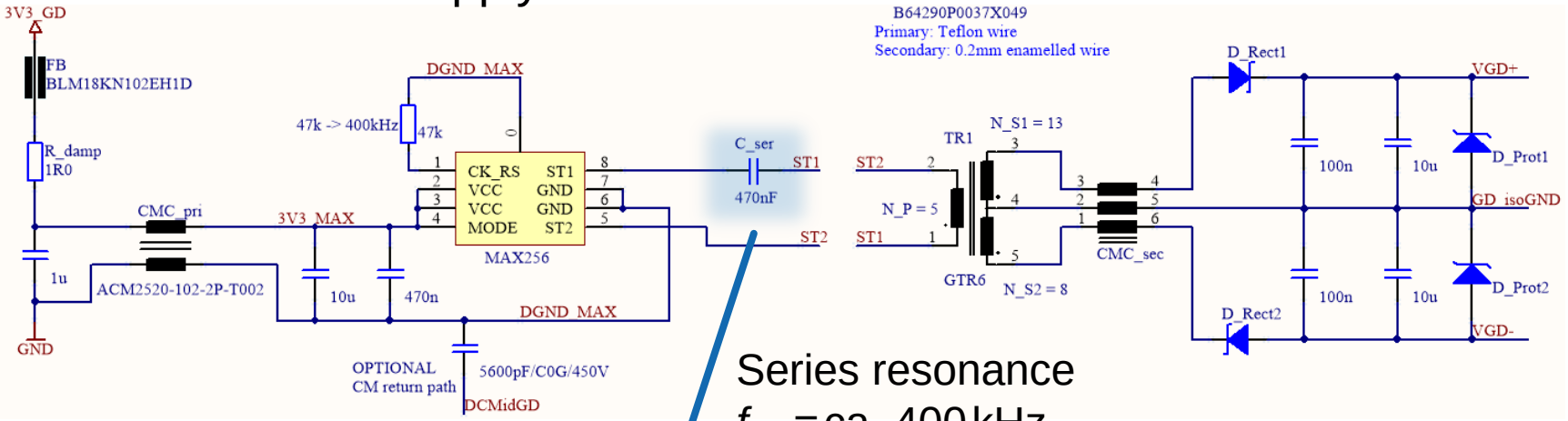
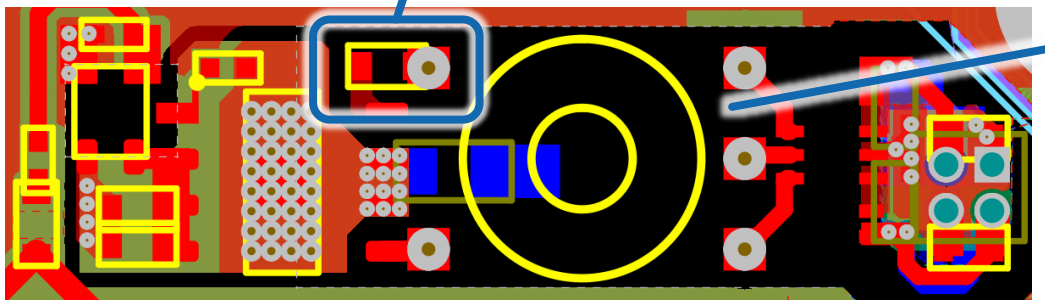
Measurement PCB – Isolated GD Supplies

- Individual isolated GD supply for each switch



V_{GD+} = ca. +8 V
V_{GD-} = ca. -4 V

Series resonance
f_{res} = ca. 400 kHz



Ultra-low coupling-*C*
C_{ps} = ca. 1 pF

→ No overlap between primary and secondary + Low-C transformer → High dv/dt immunity

Hardware Demonstrator – CAD

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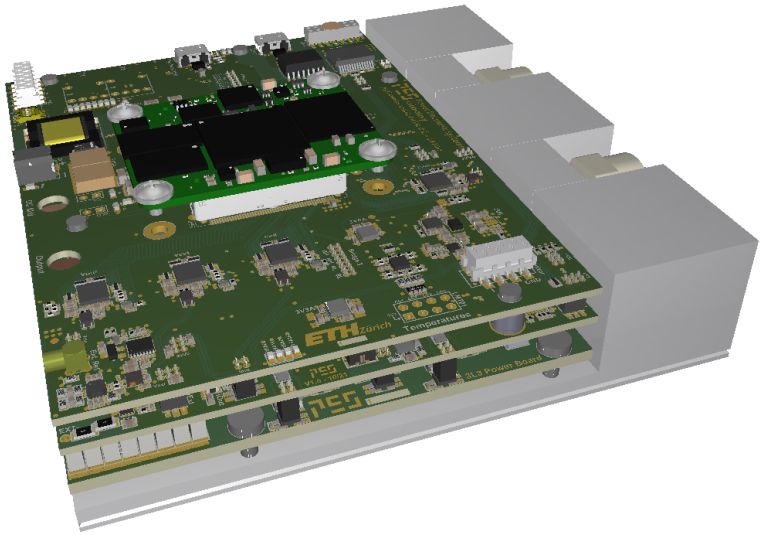

Power PCB — Measurement PCB — Control PCB

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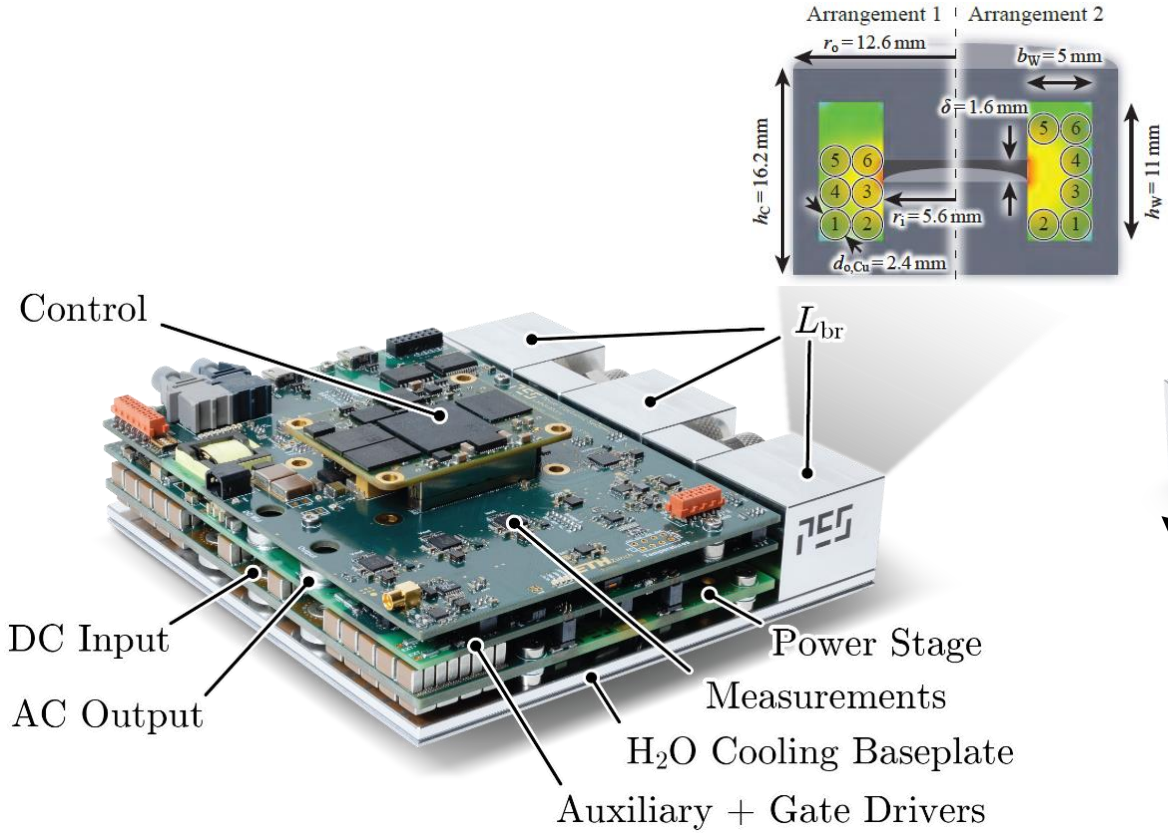
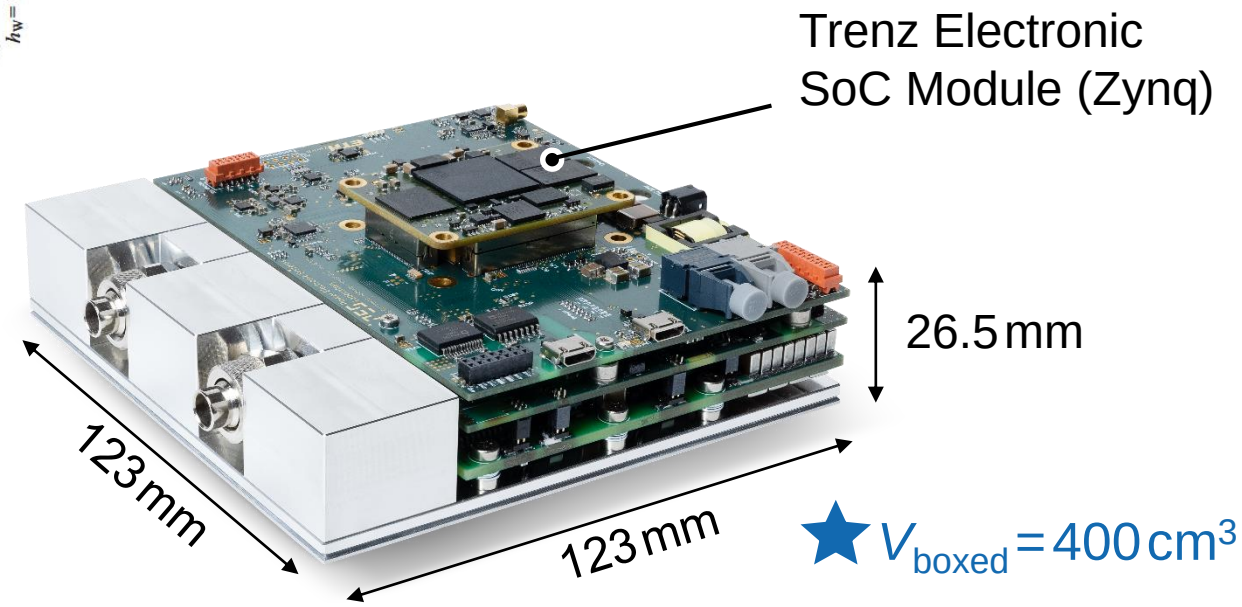
Hardware Demonstrator

- $M=3$ / $N=3$ hardware single-phase 10 kW demonstrator

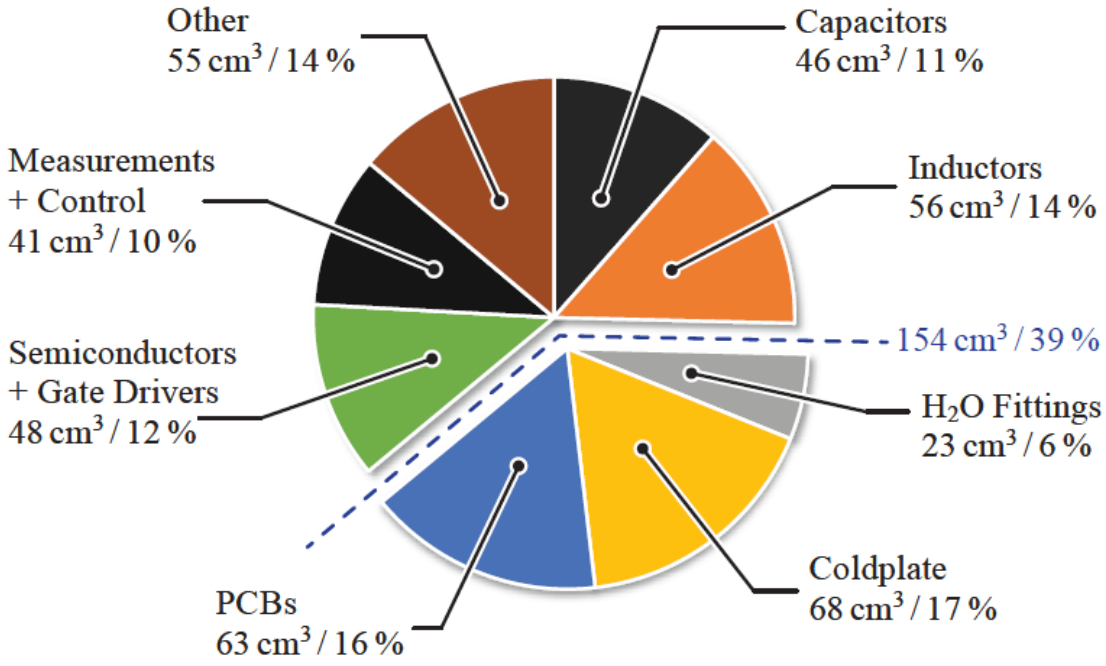


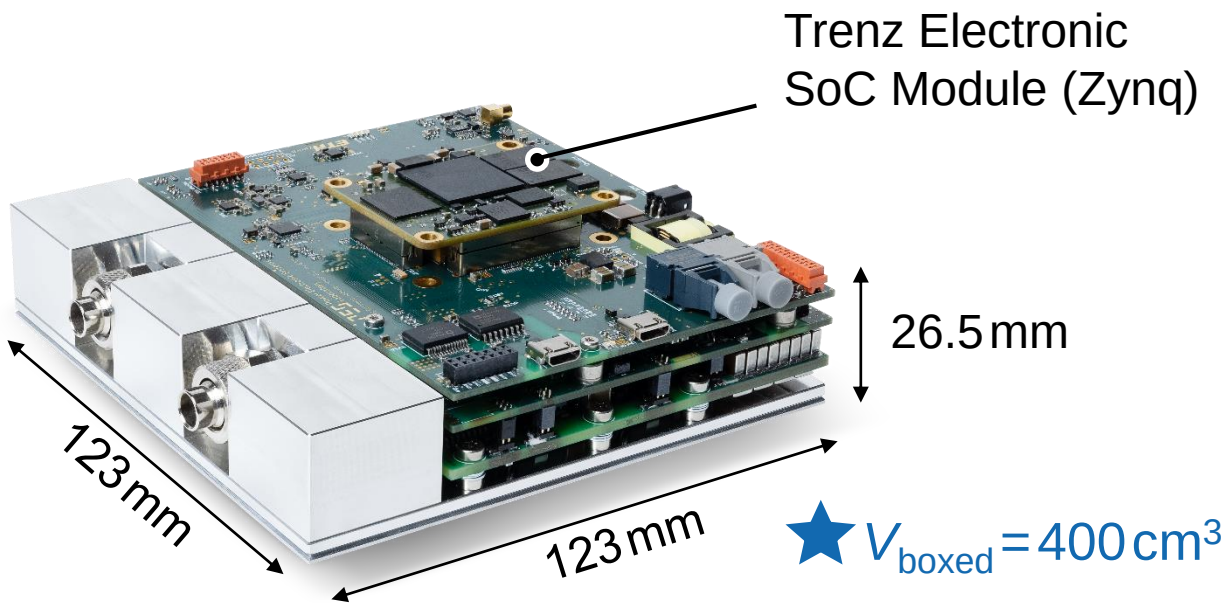


→ 25 kW/dm³ (410 W/in³) power density

Hardware Demonstrator – Volume Breakdown

- $M=3$ / $N=3$ hardware single-phase 10 kW demonstrator



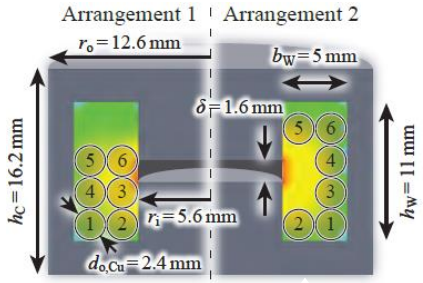


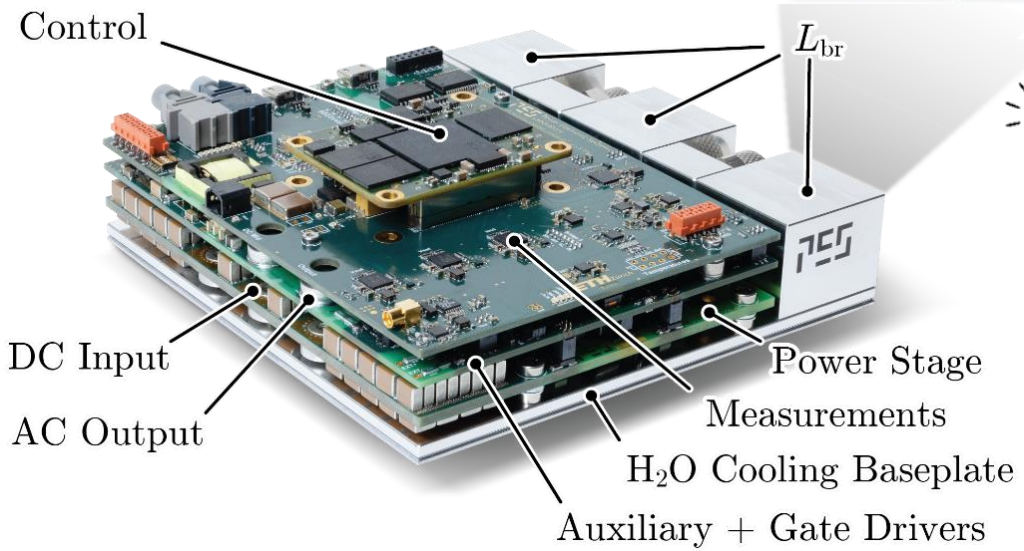
→ Almost 40% of volume occupied by mechanical parts

Hardware Demonstrator – Inductor

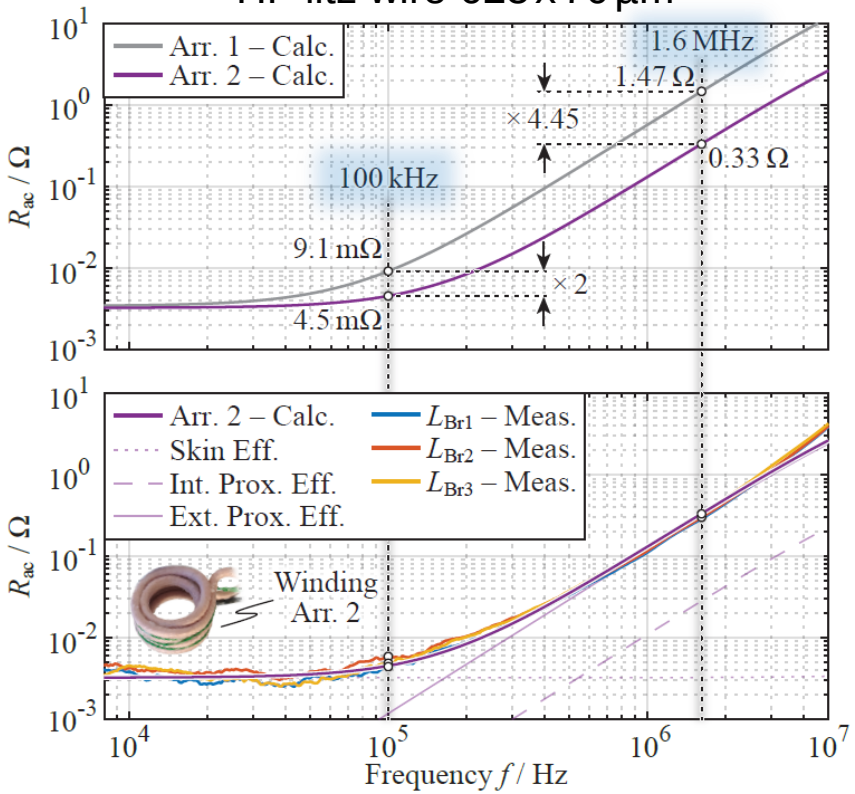
- *M*=3 / *N*=3 hardware single-phase 10 kW demonstrator

Ferroxcube 3F46





HF litz wire 625 x 70 µm



Weighted Losses:

Arr. 1: ca. 31.3 W

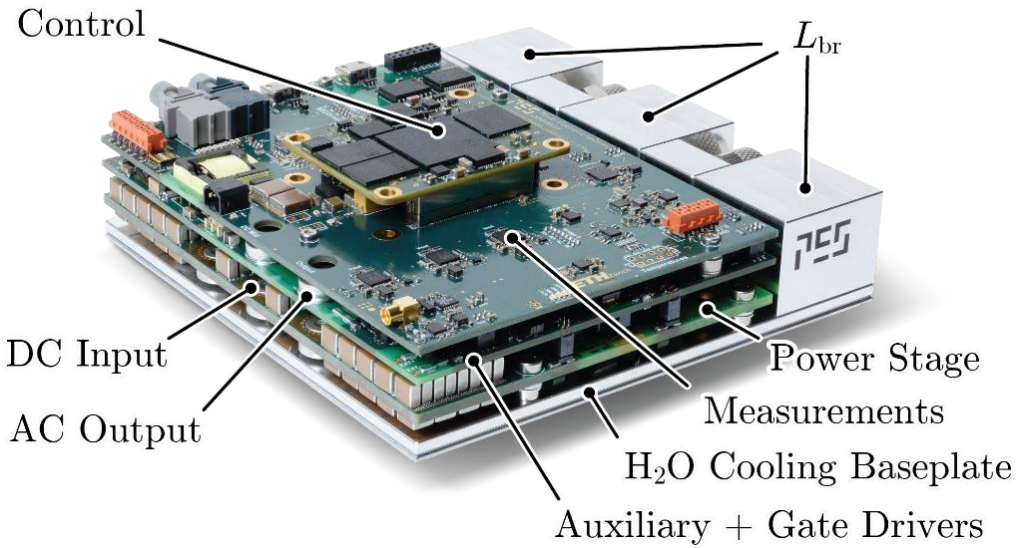
***Arr. 2:* ca. 7.7 W**

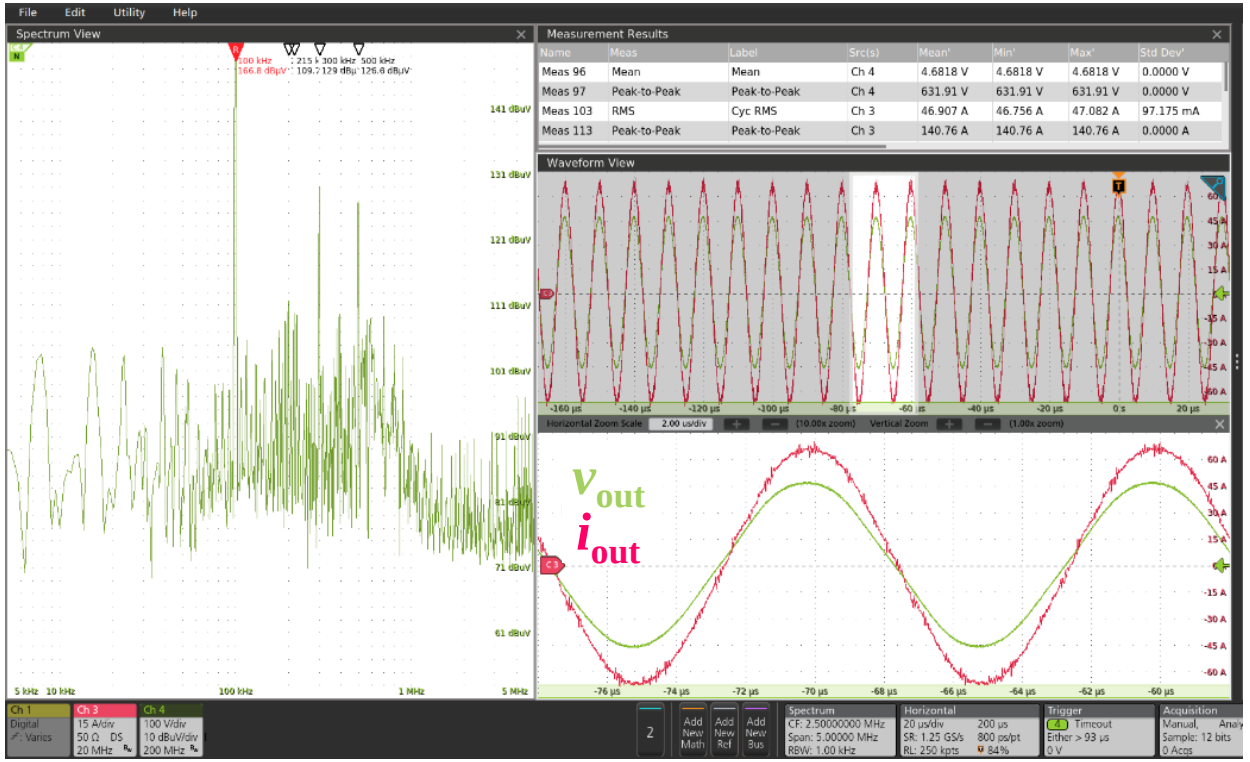
	R_{dc} mΩ	$R_{ac,100k}$ mΩ	$R_{ac,1.6M}$ Ω
Arr. 1	*3.40*	*9.14*	*1.47*
Arr. 2	*3.20*	*4.53*	*0.33*
L_{br1}	3.15	4.41	0.28
L_{br2}	3.46	5.84	0.30
L_{br3}	3.25	4.83	0.33

→ Pot core branch inductor → No ext. fringing field → No eddy-current losses in metallic enclosure

Experimental Verification

- Operation with sinusoidal reference at 100 kHz and 10 kW (full-load) output power (230 Vrms, 43.5 Arms)
- Open-loop operation
- 24 ns interlocking time



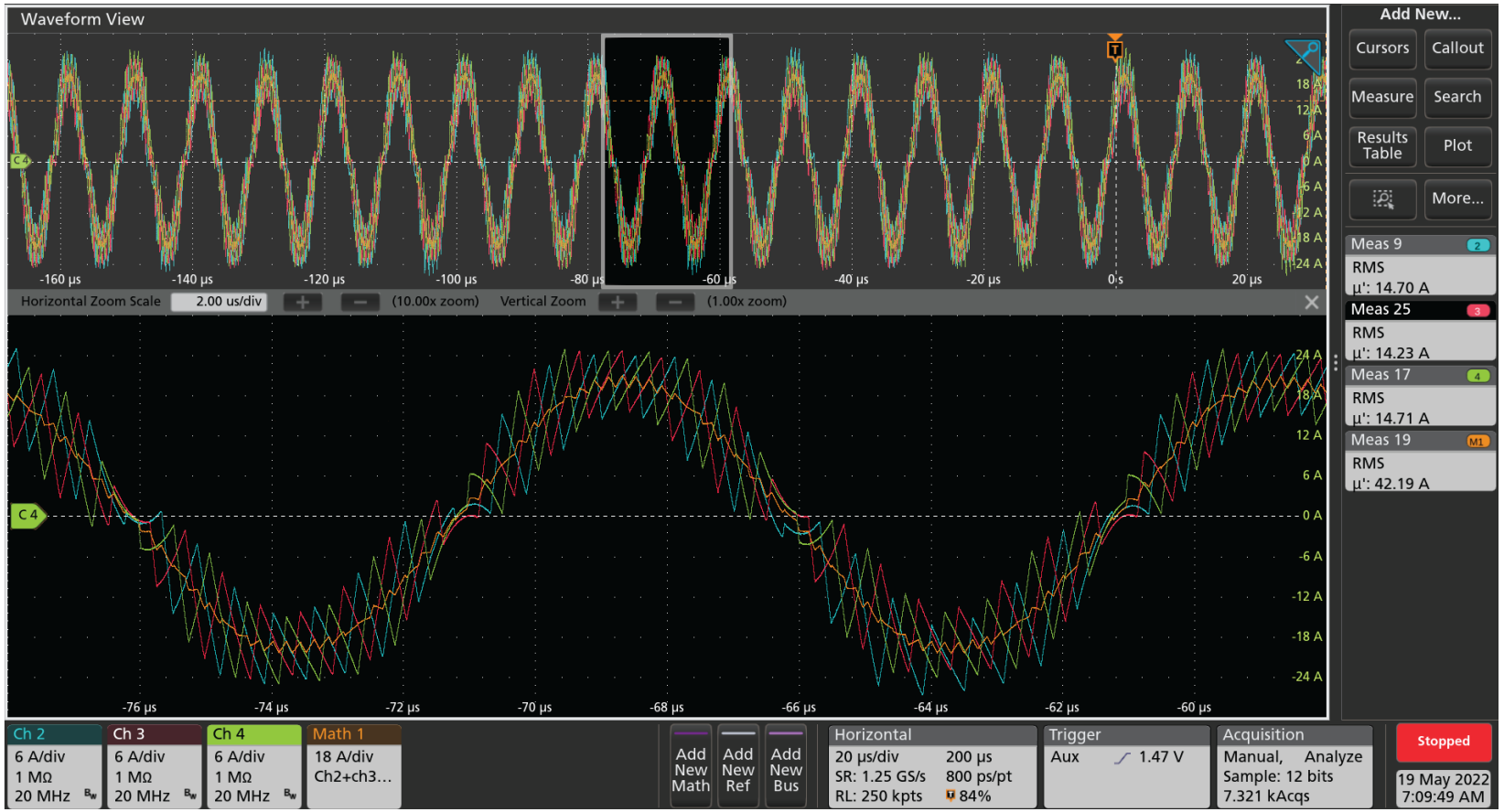


→ ≈40 dB attenuation of 3rd and 5th harmonic

Experimental Verification

- Operation with sinusoidal reference at 100 kHz and 10 kW (full-load) output power

i_{L1} 6 A/div
i_{L2} 6 A/div
i_{L3} 6 A/div
i_{sum} 18 A/div

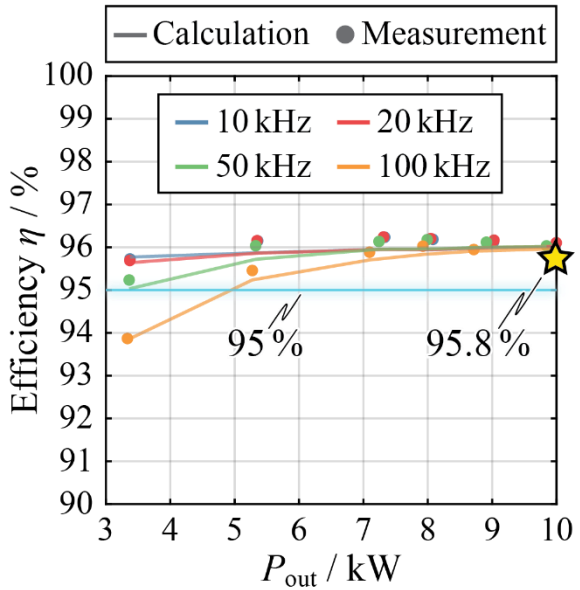


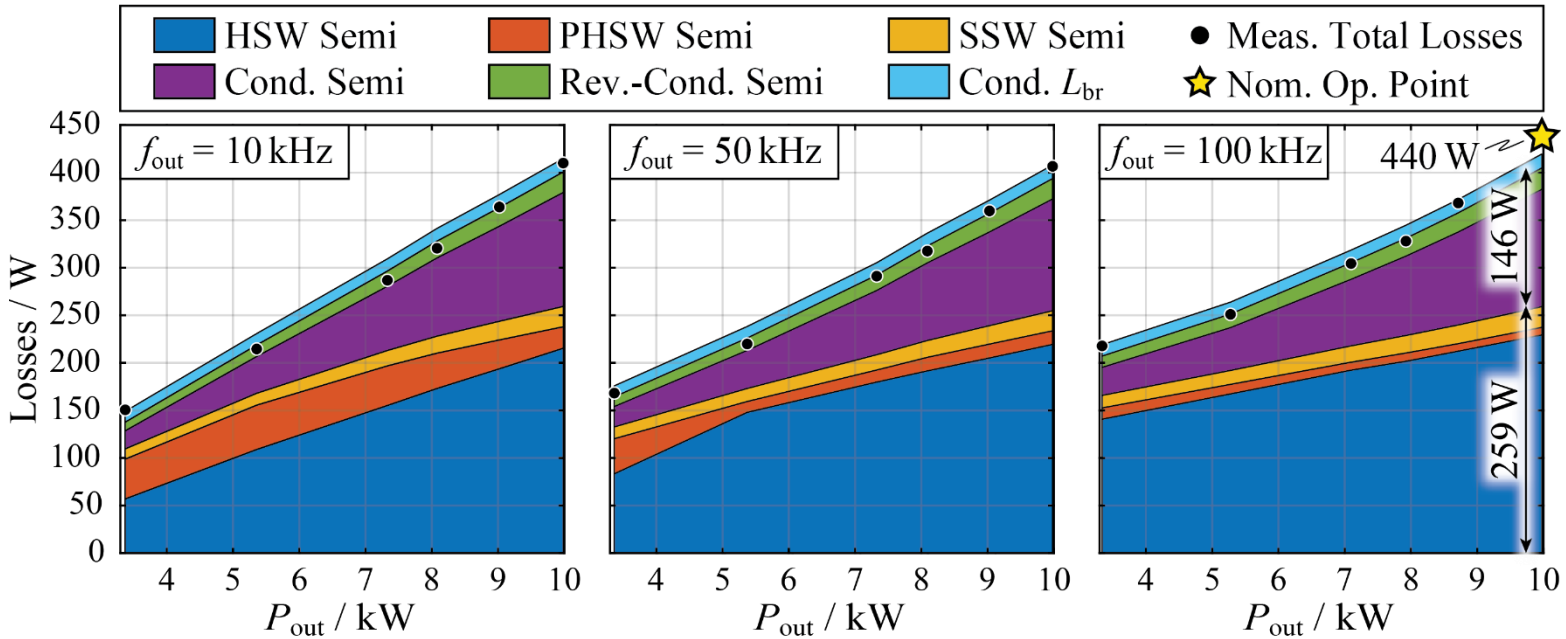
→ Adequate current balancing without active symmetry control

Experimental Verification: Efficiency

- $M=3$ / $N=3$ hardware demonstrator → $f_{sw,eff}$ = 4.8 MHz
- Open-loop operation with V_{out} = 230 V_{rms}
- 24 ns interlocking time

Low-inductive load resistor (2 kW)



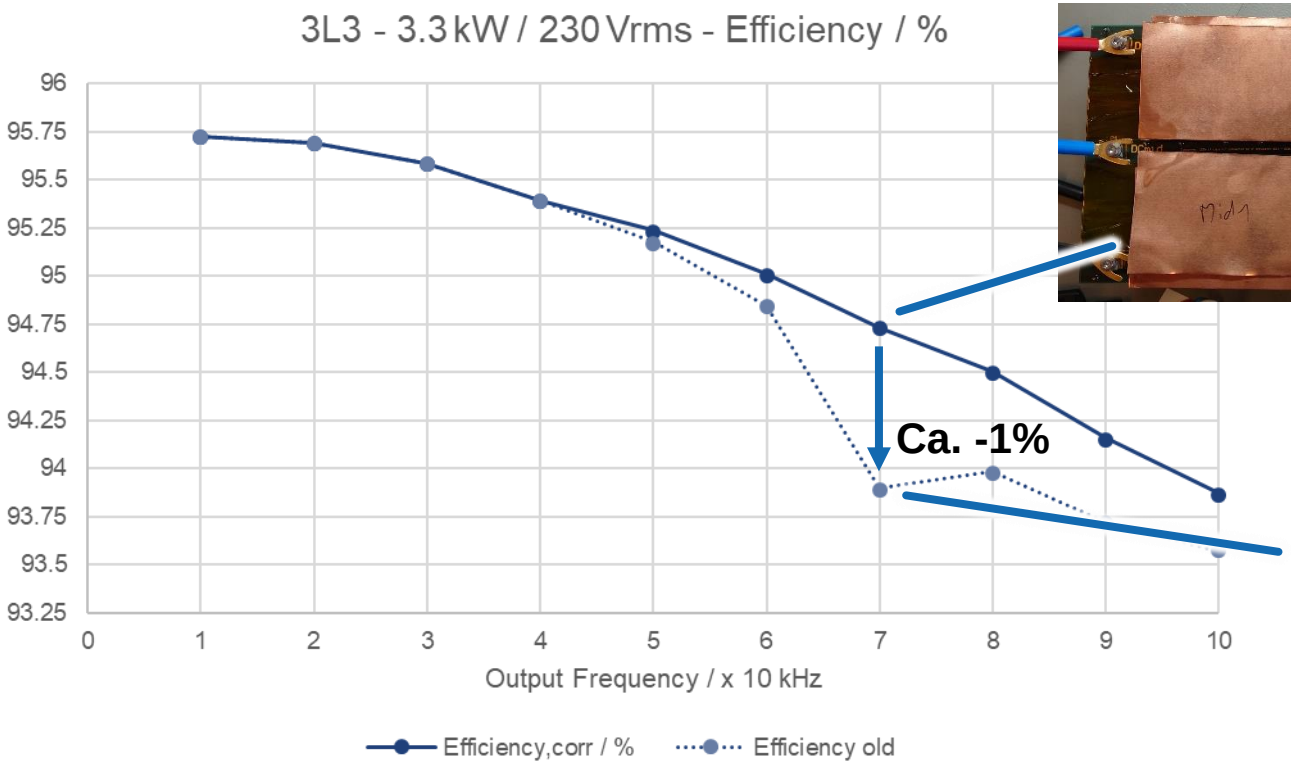


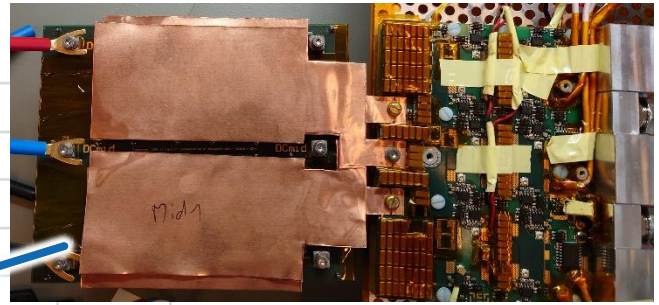
→ η = 95.8 % @ 100 kHz, 10 kW (nom. op. point)

→ Losses dominated by (hard-) switching losses

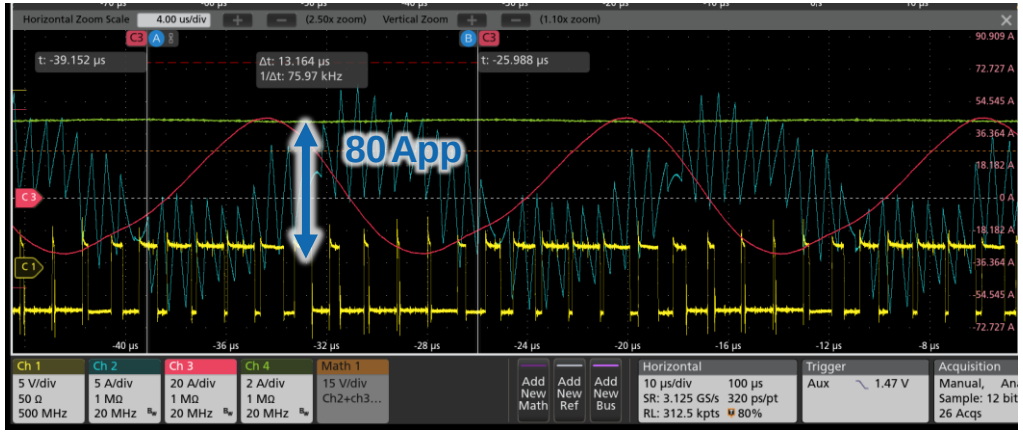
Experimental Verification: Efficiency

- Impact of output frequency and input capacitor connection @ P_{out} = 3.3 kW





Low-inductive connection of external DC-link capacitors (< 30 nH)

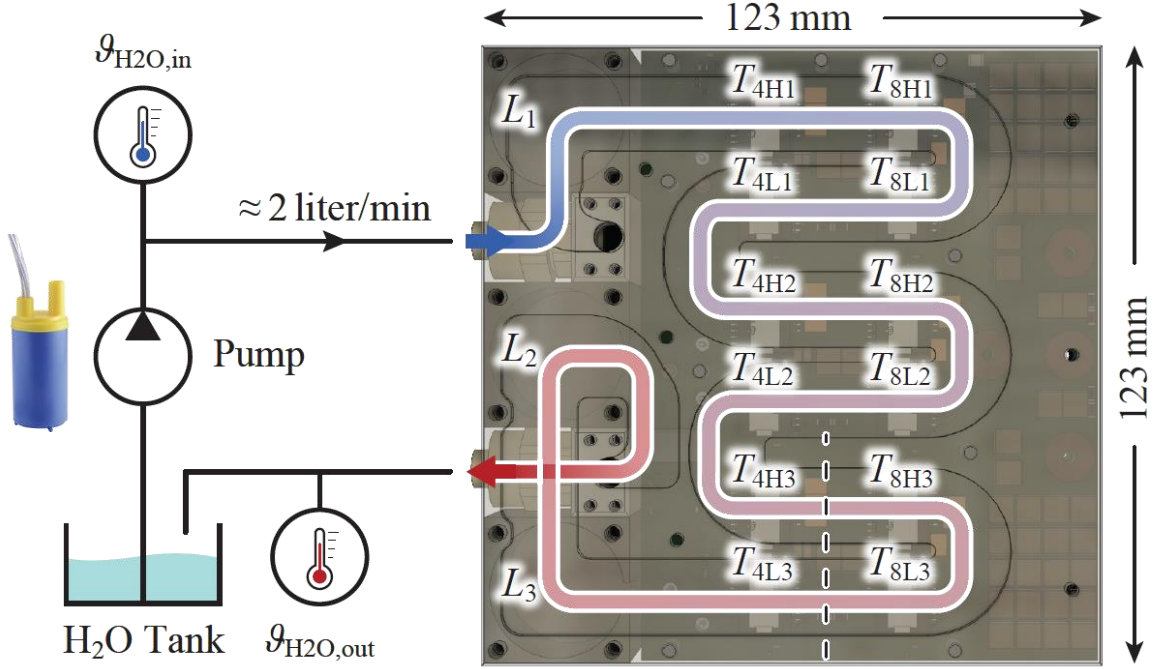


→ Significant drop at 70 kHz (-1%) → ca. 80 App oscillation between 3L3 and Film-C DC-link bank

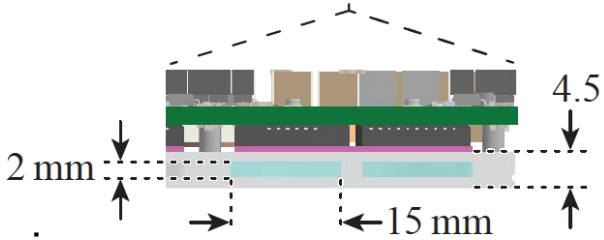
→ Low-inductive connection to mitigate resonance

Thermal Management

- 4.5 mm thin Al coldplate
- Direct cooling of power semiconductors + inductors
  - 12 V / 14 W Pump
  - Volume Flow ≈ 2 l/min
  - 10 l H_2O Tank → "open-circuit" (No Heat Exchanger)
  - 15 mm x 2 mm Channel



TG6050 TIM
6 W/(m·K), 1 mm

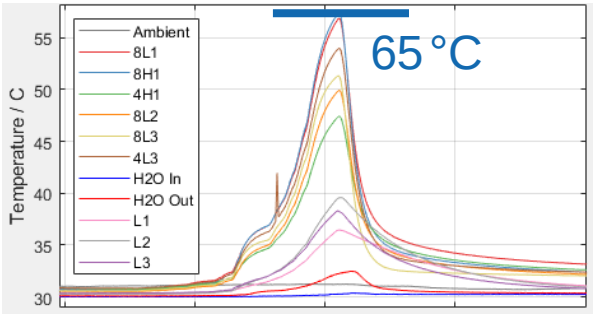


→ Loss estimation: $P_{loss,est} = c_{P,H2O} \cdot \rho_{H2O} \cdot \dot{V} \cdot \Delta\vartheta_{H2O}$

→ $P_{loss,est}$ = 150 W for $\Delta\vartheta_{H2O} = \vartheta_{H2O,out} - \vartheta_{H2O,in}$ = 1 K, $\dot{V}$ = 2 l/min

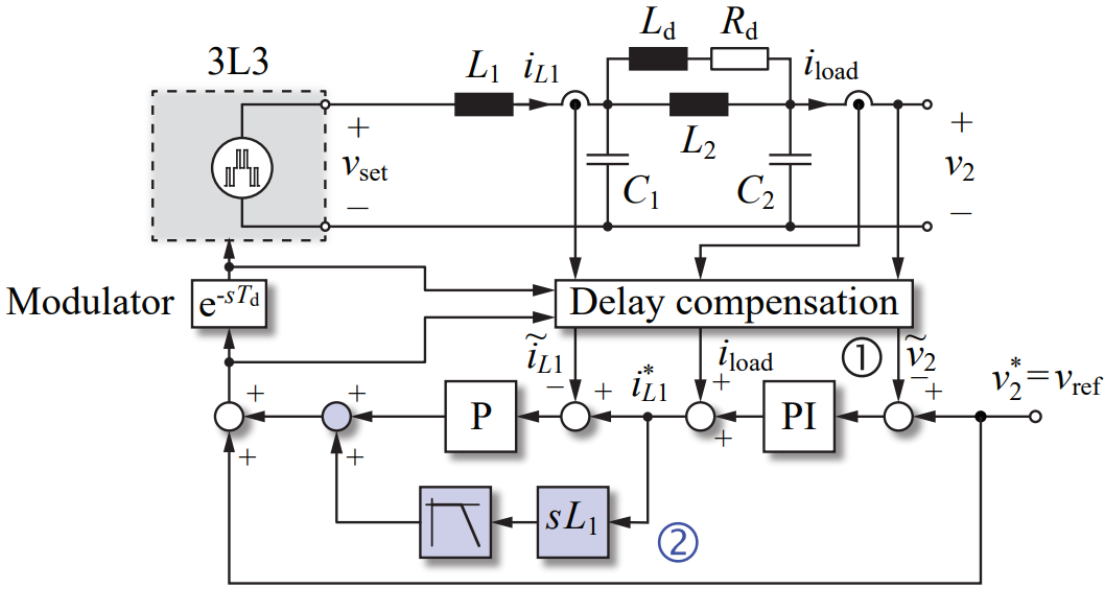
→ $\vartheta_{Case,Switch}$ < 65°C → $\vartheta_{J,Switch}$ < 100°C (estimated with $R_{th,j-c}$ = 1 K/W, P_{switch} = 34 W)

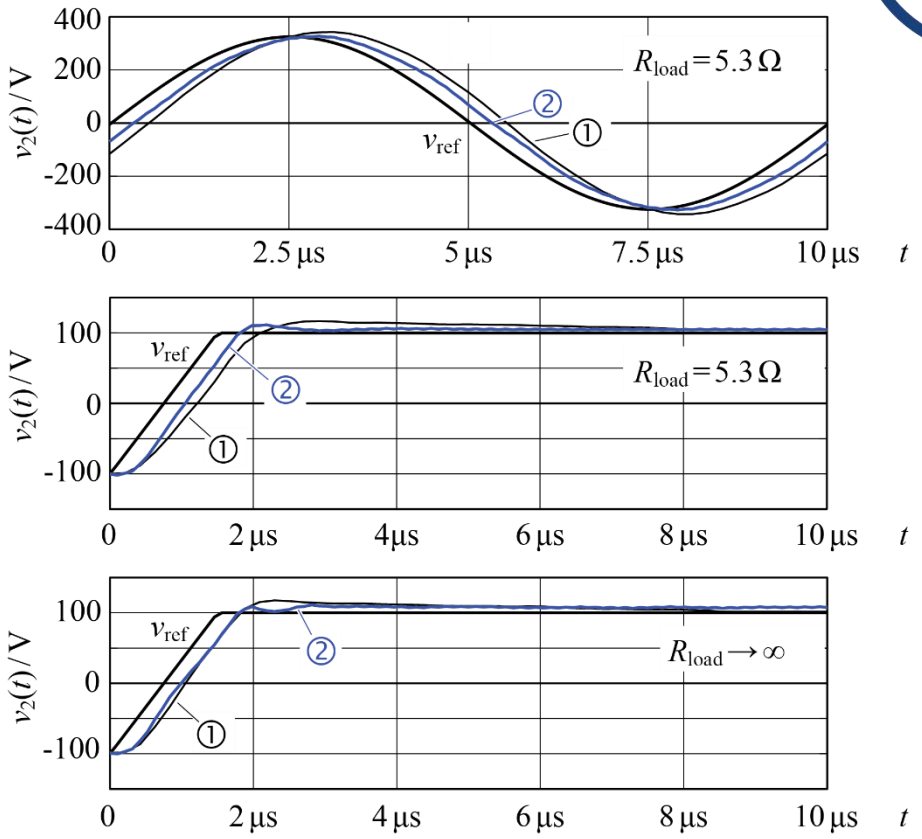
→ Room for improvement with better TIM + alternative package (?)



Outline: Output Voltage Control

- Cascaded current and voltage control
- v_{ref}, i_{load} and inductor voltage feedforward

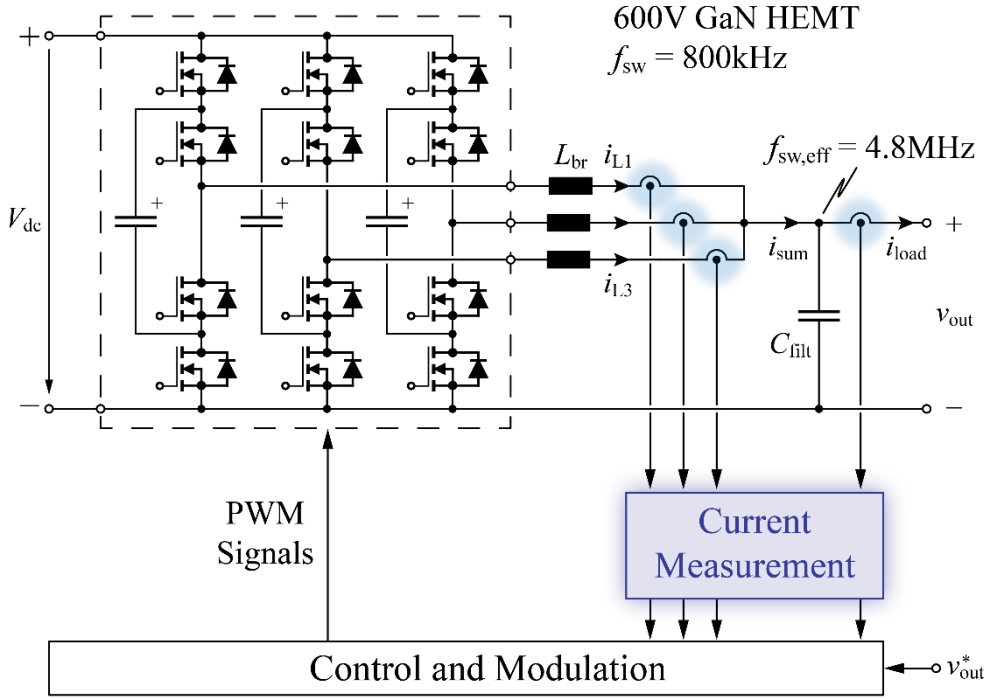




→ >300 kHz closed-loop control BW possible

→ Minimal loop delay crucial for ultra-fast control

F. Krismer, et *al.*, "Optimized Cascaded Controller Design for a 10 kW / 100 kHz Large Signal Bandwidth AC Power Source," IEEE Energy Conversion Congress and Exposition (ECCE USA), Detroit, MI, USA, Oct. 11-15, 2020.

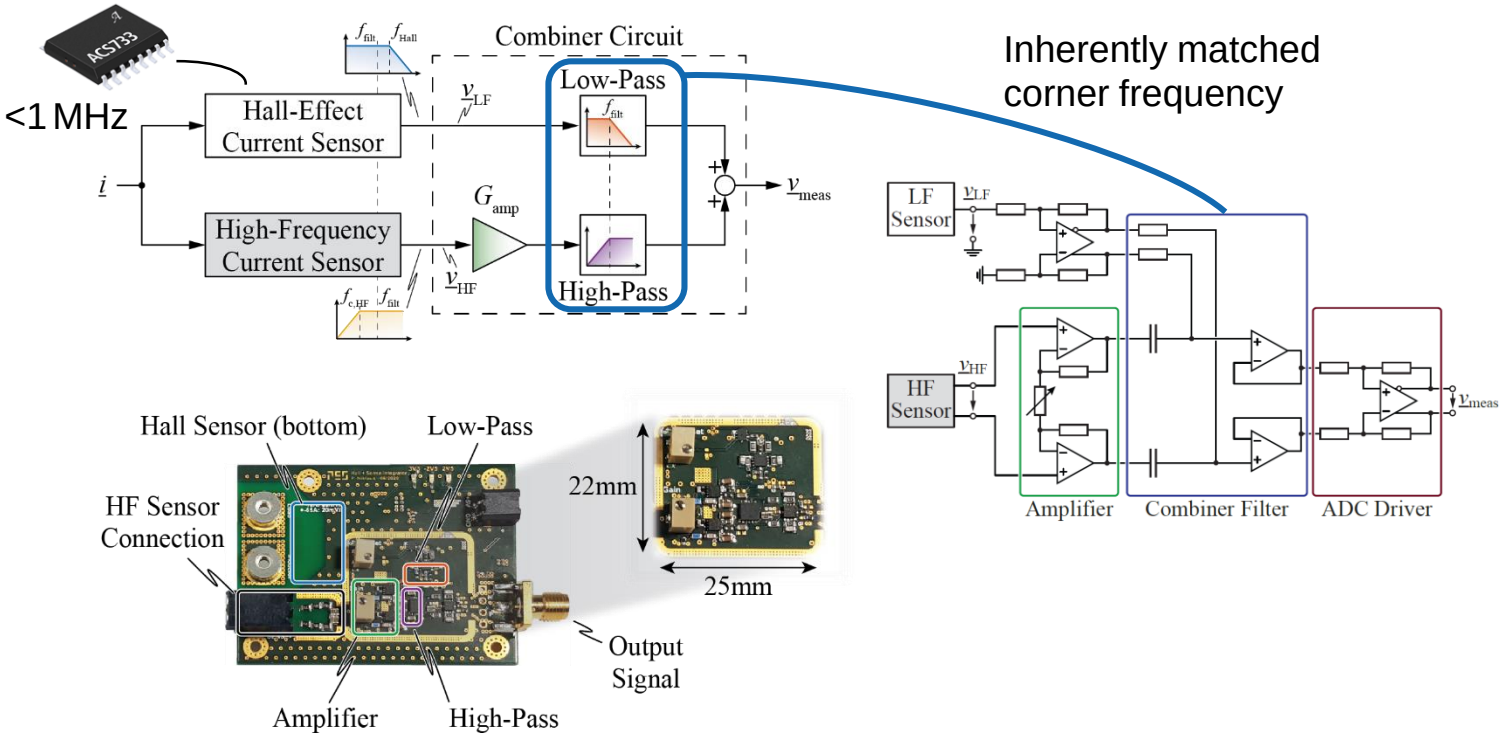


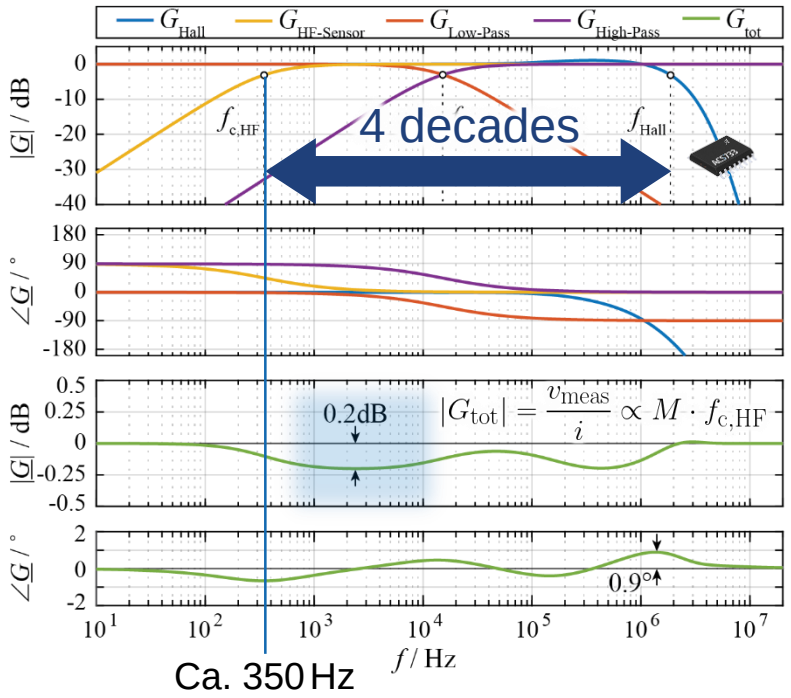
High-Frequency DC-Coupled Current Measurement Sensors

Bandwidth Extension of Commercial Hall-Effect Current Sensors to >10 MHz

LF + HF Sensor Combination

- Minimal error in the transition / combiner region
- Active combiner circuit

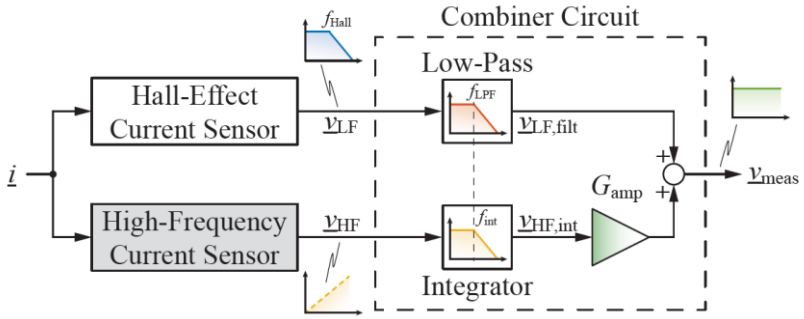


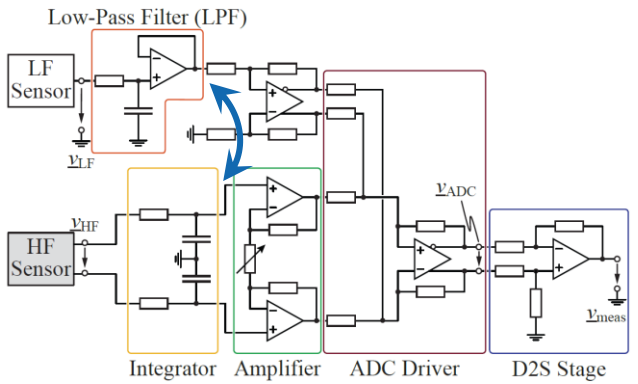


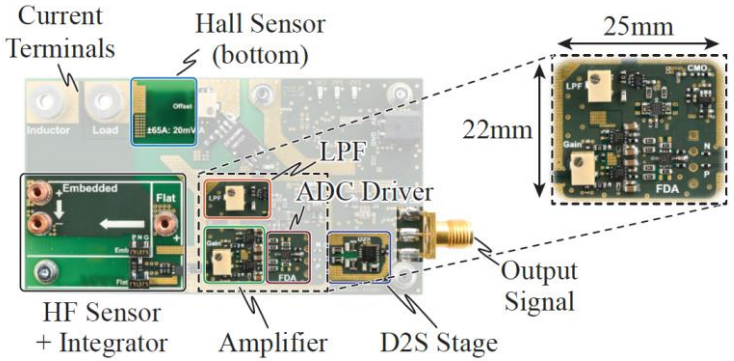
→ 4 decades overlap required → Possible with lower sensor response overlap range?

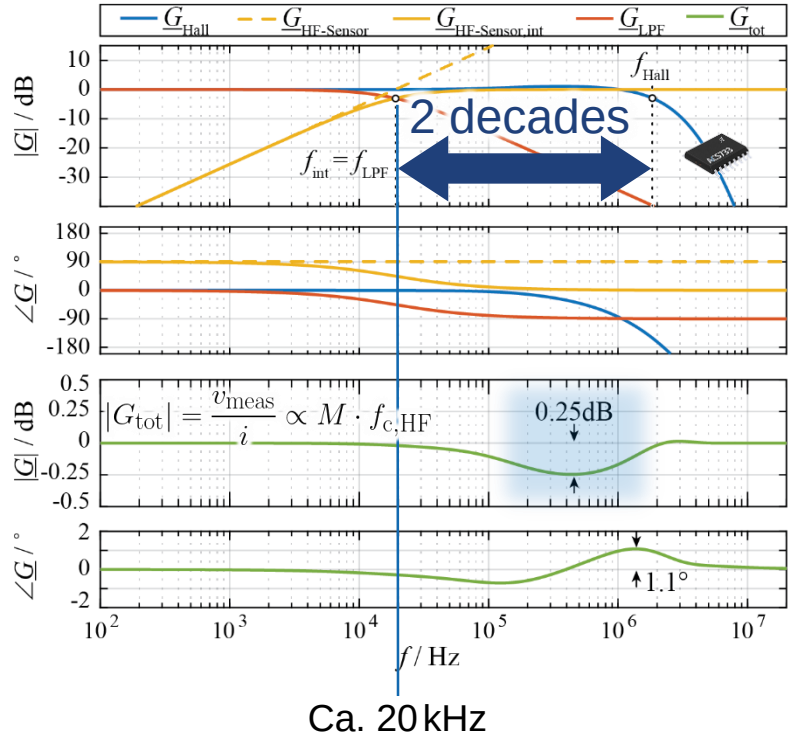
LF + HF Sensor Combination

- Inherent well-defined high-pass response of HF sensor
- Manual matching of crossover frequency







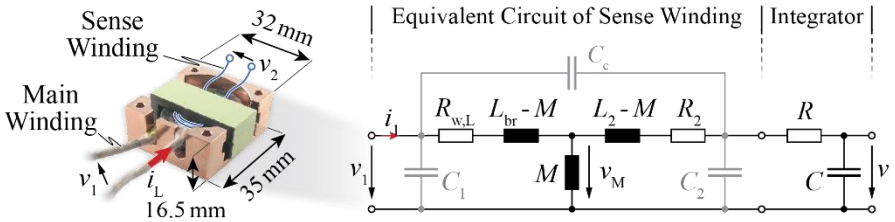


→ Only 2 decades overlap required → Find suitable HF sensors

Investigated HF Sensors

- Max. BW and minimal volume

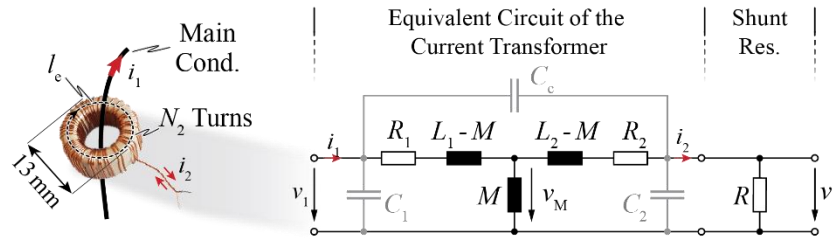
▼ Isolated Inductive Voltage Sensing



→ No add. volume!

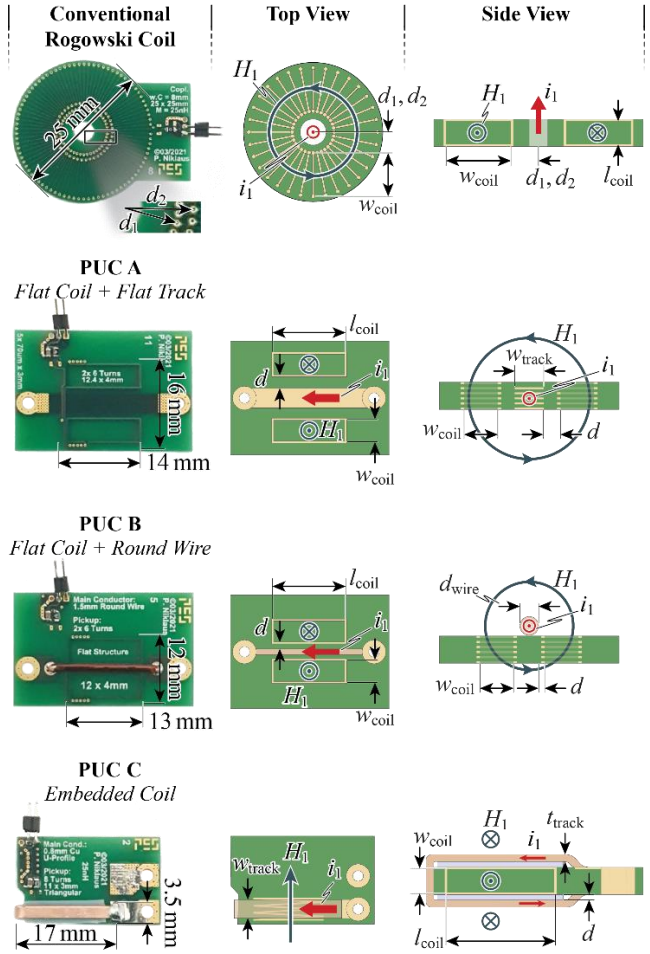
$$v = i_1 \cdot \frac{sM}{1 + sRC}$$

▼ Current Transformer



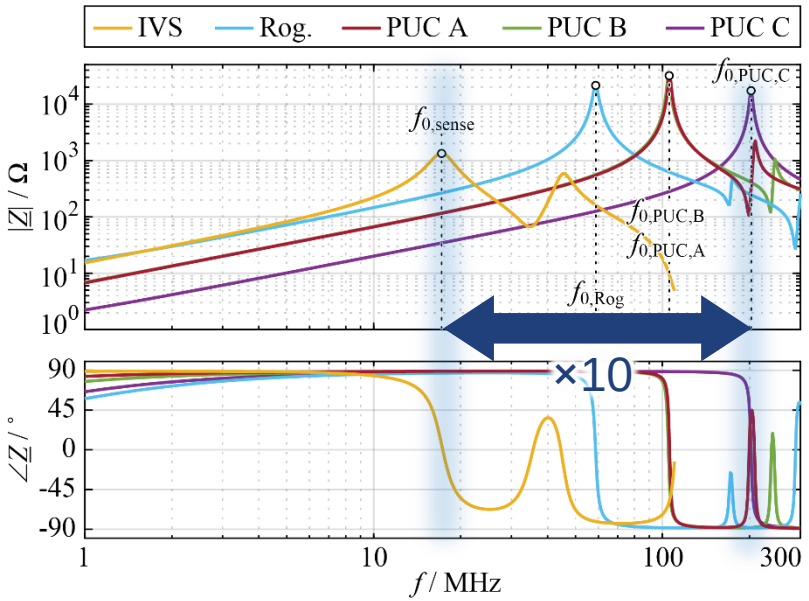
→ Higher BW

$$v = i_1 \cdot R \cdot \frac{sM/(R + R_2)}{1 + sL_2/(R + R_2)}$$



◀ Pickup Coils

→ Highest BW + linear

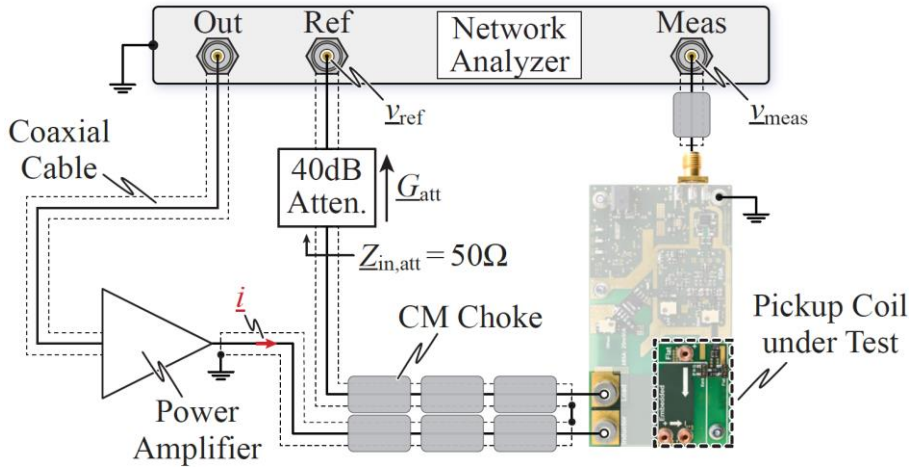


→ Which sensor offers best performance?

Experimental Verification – Frequency Response

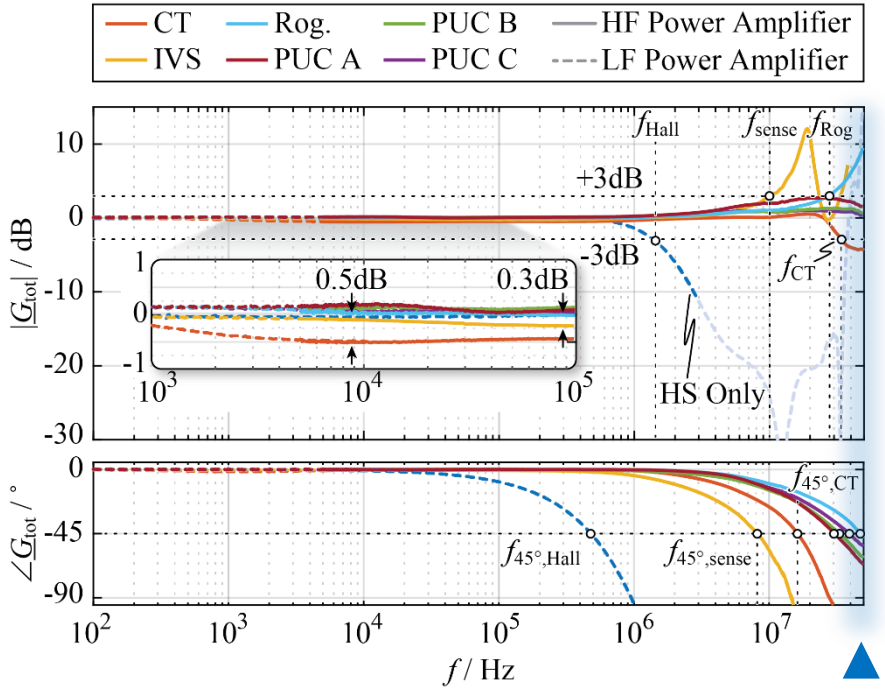
- All sensors tested in-circuit

▼ Setup Frequency Response



$$\underline{G}_{meas} = \frac{\underline{v}_{meas}}{\underline{v}_{ref}} = \frac{\underline{v}_{meas}}{\underline{i} \cdot \underline{Z}_{in,att} \cdot \underline{G}_{att}} = \frac{\underline{G}_{tot}}{\underline{Z}_{in,att} \cdot \underline{G}_{att}}$$

▼ Frequency Domain



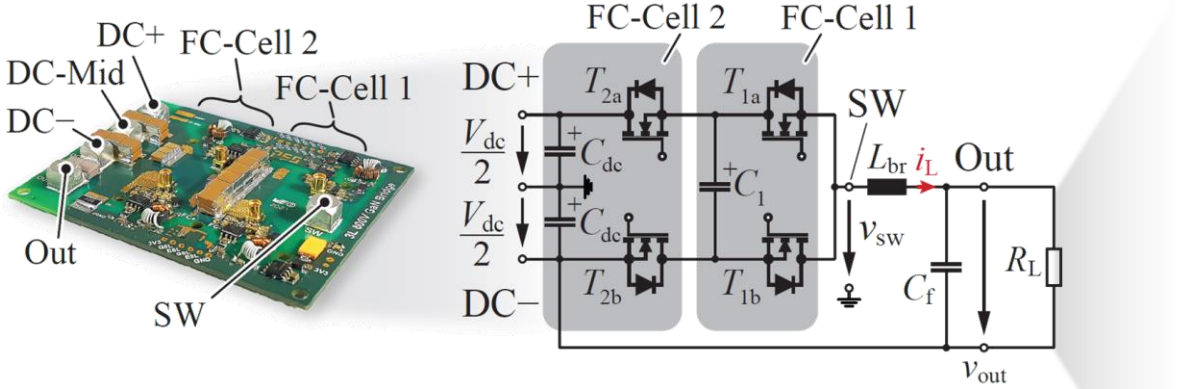
▲ >50 MHz

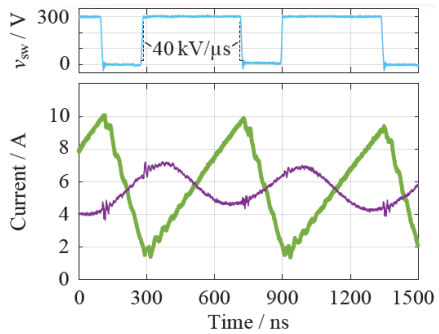
→ 10 MHz BW fulfilled with all sensors

→ PUC C with highest BW and smallest form factor

Experimental Verification – Time Domain Behavior

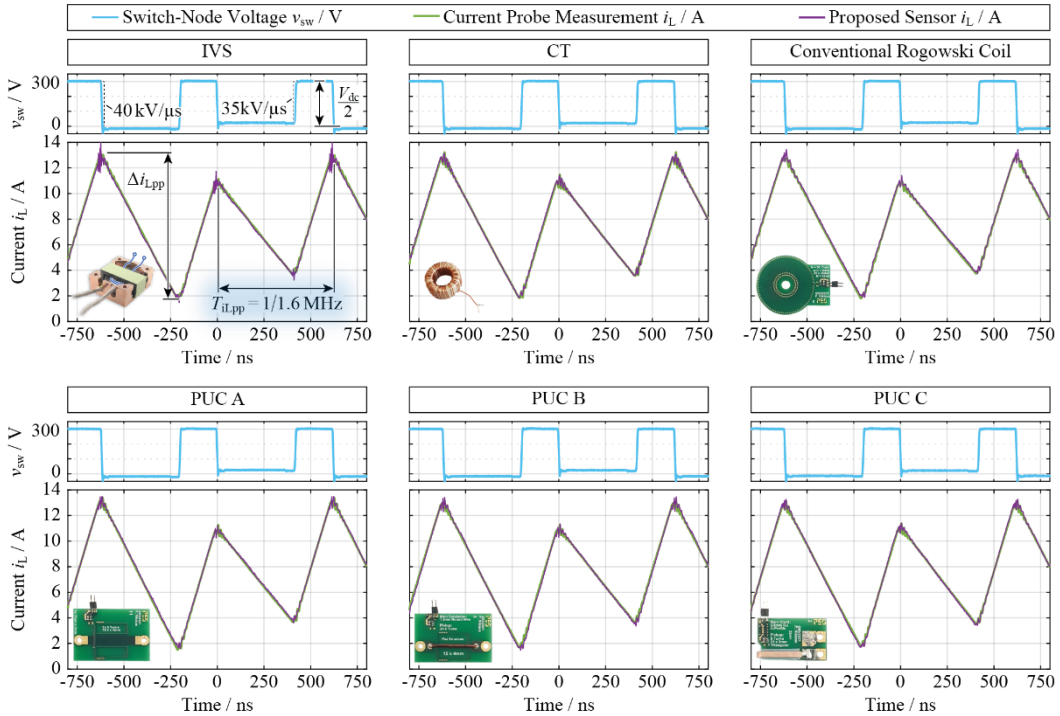
- All sensors tested in-circuit





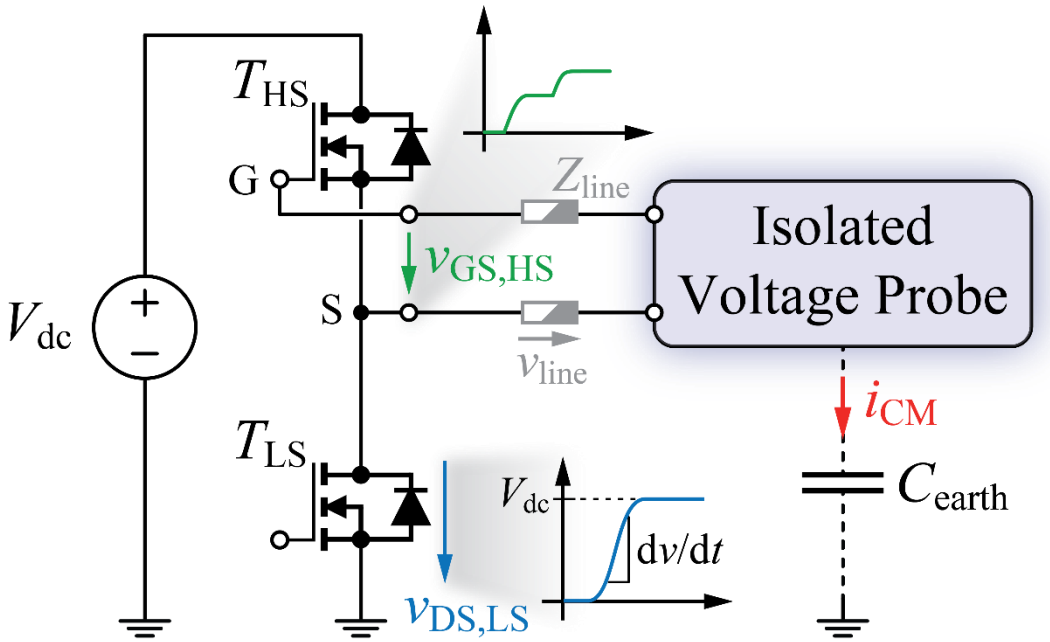
Hall sensor only

▼ Time Domain – Sensors after *L*



→ Accurate tracking of triangular current

→ PUC C with highest BW and smallest form factor

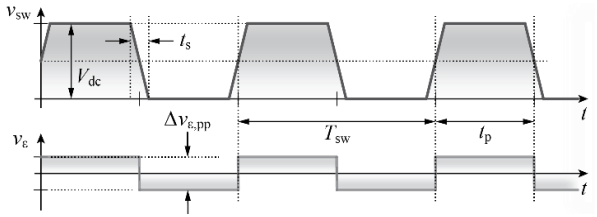


High-Bandwidth Isolated Voltage Measurements with Very High Common Mode Rejection Ratio

Accurate Measurements during Fast Voltage Transients

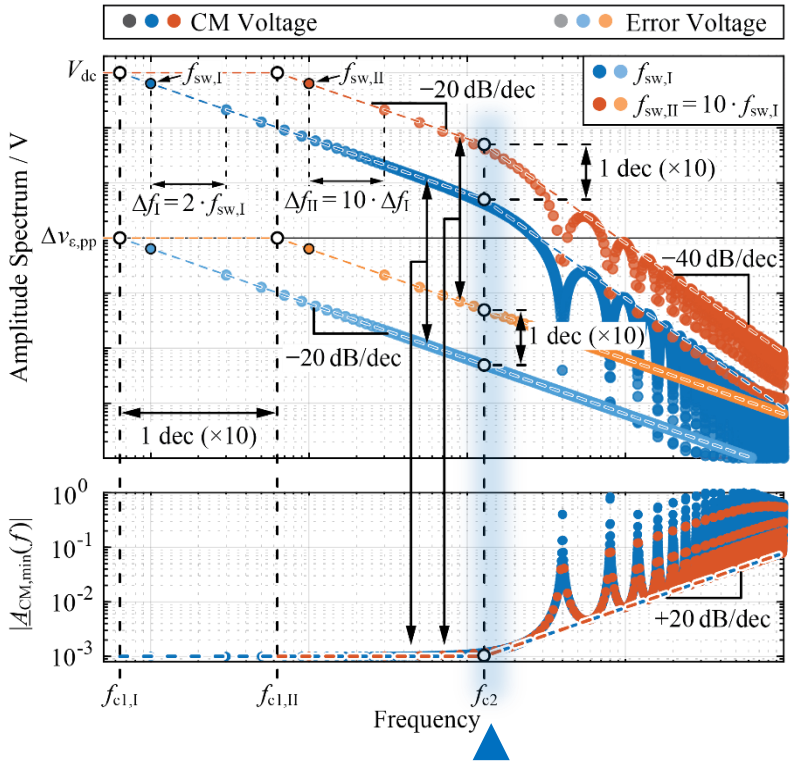
Modeling of Required CMRR

- Spectral envelope of trapezoidal CM voltage
- Rectangular error voltage

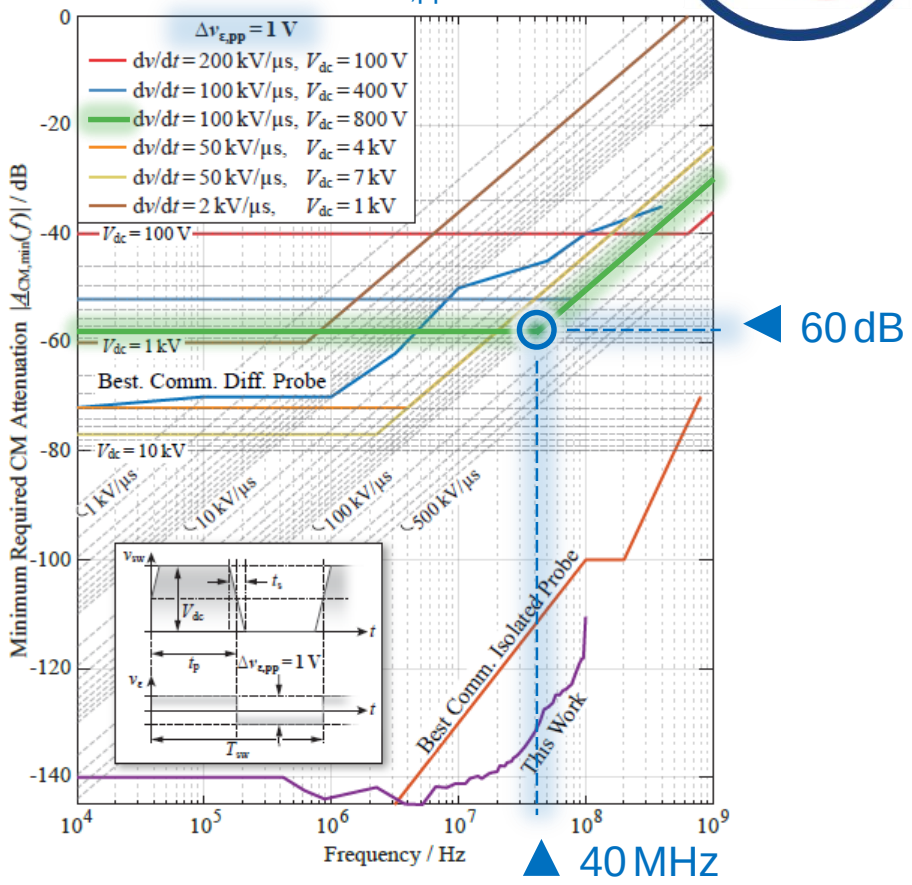


$$f_{c1} = \frac{1}{\pi \cdot t_p} = \frac{f_{sw}}{\pi \cdot D}$$

$$f_{c2} = \frac{1}{\pi \cdot t_s} = \frac{dv/dt}{\pi \cdot V_{dc}}$$



For $\Delta v_{\varepsilon,pp} = 1\,V$



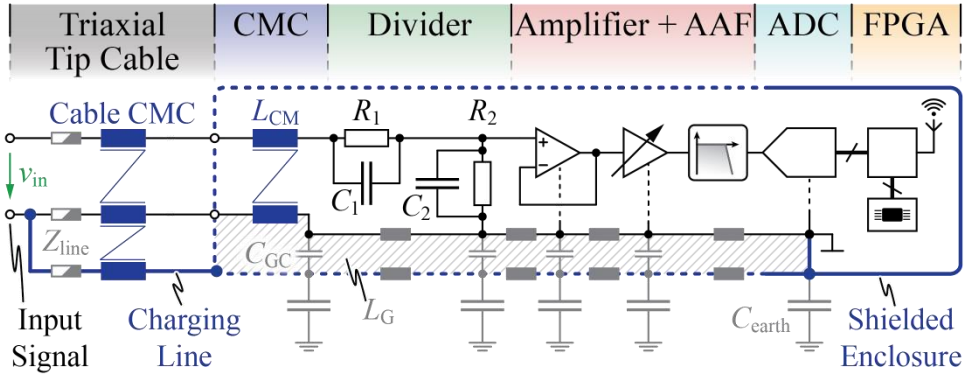
60 dB

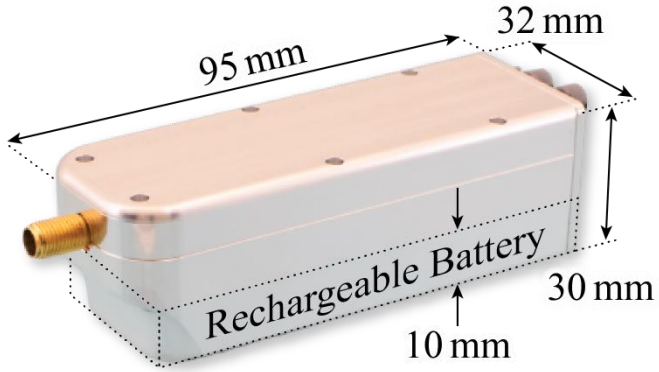
40 MHz

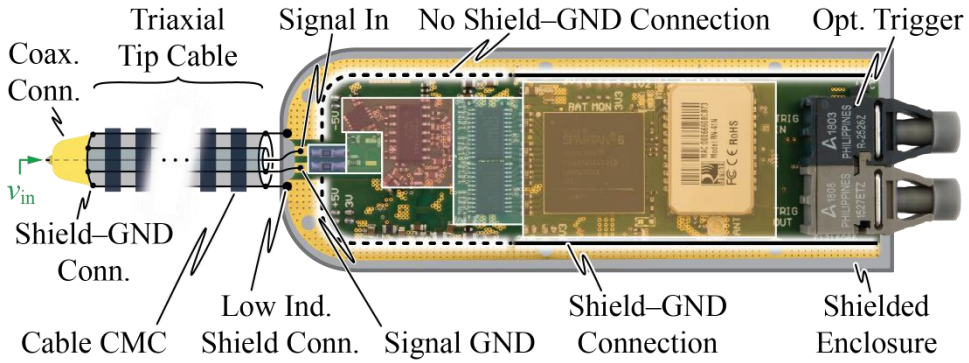
→ Only V_{dc} + dv/dt determine CMRR requirement and NOT switching frequency

Isolated Voltage Measurement System

- Small and decoupled C_{earth} → Low CM current i_{CM}
- Several measures to limit/redirect i_{CM}





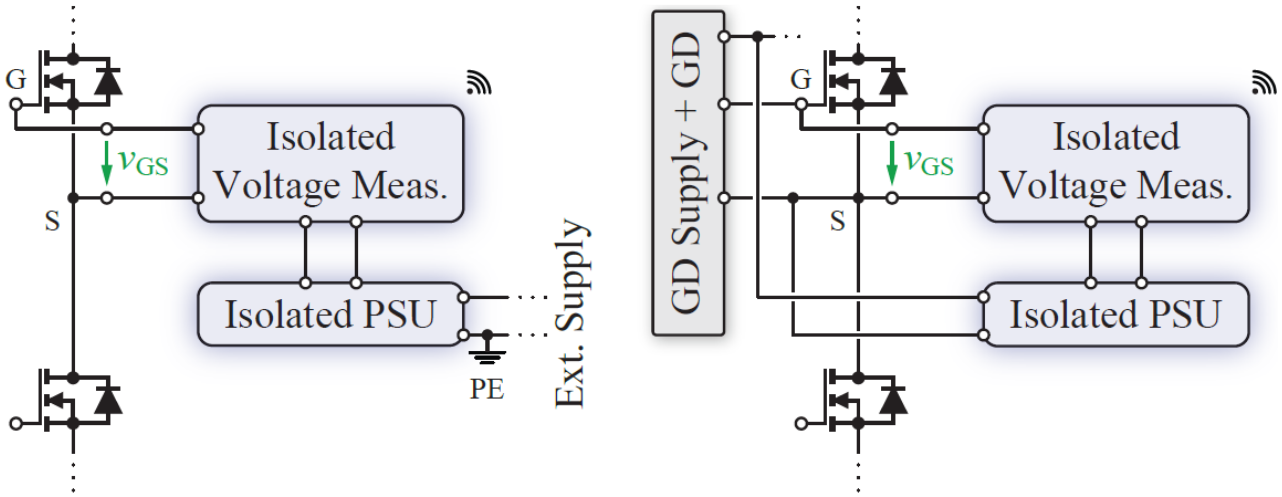


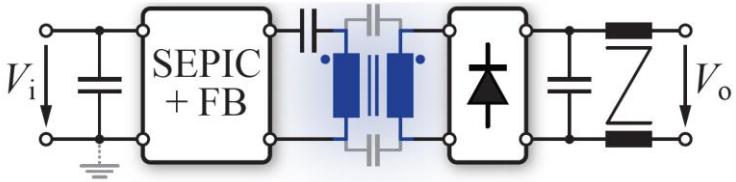
Parameter	Value
Input Voltage Range	±1 ... ±75 V
Bandwidth	130 MHz
Sampling Rate	400 MSPS
Vertical Resolution	8 Bit
CMRR @ 100 MHz	>108 dB

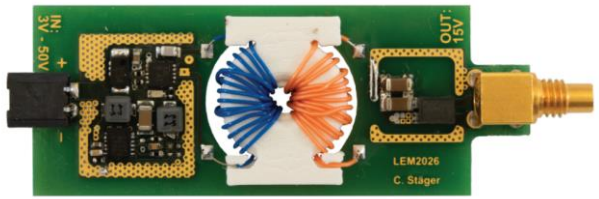
→ Fully independent of other equipment (no oscilloscope etc. required)

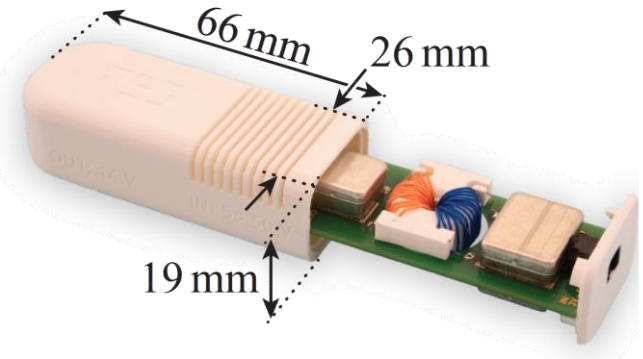
Isolated Voltage Measurement System

- Battery operation (ca. 2 h for power cons. of 2 W)
- Low-C isolated power supply
- Wide input voltage range (5 – 50 V), 5 W output power





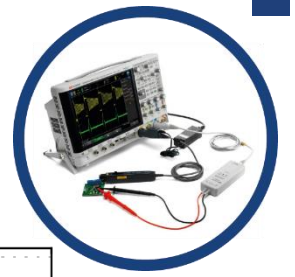




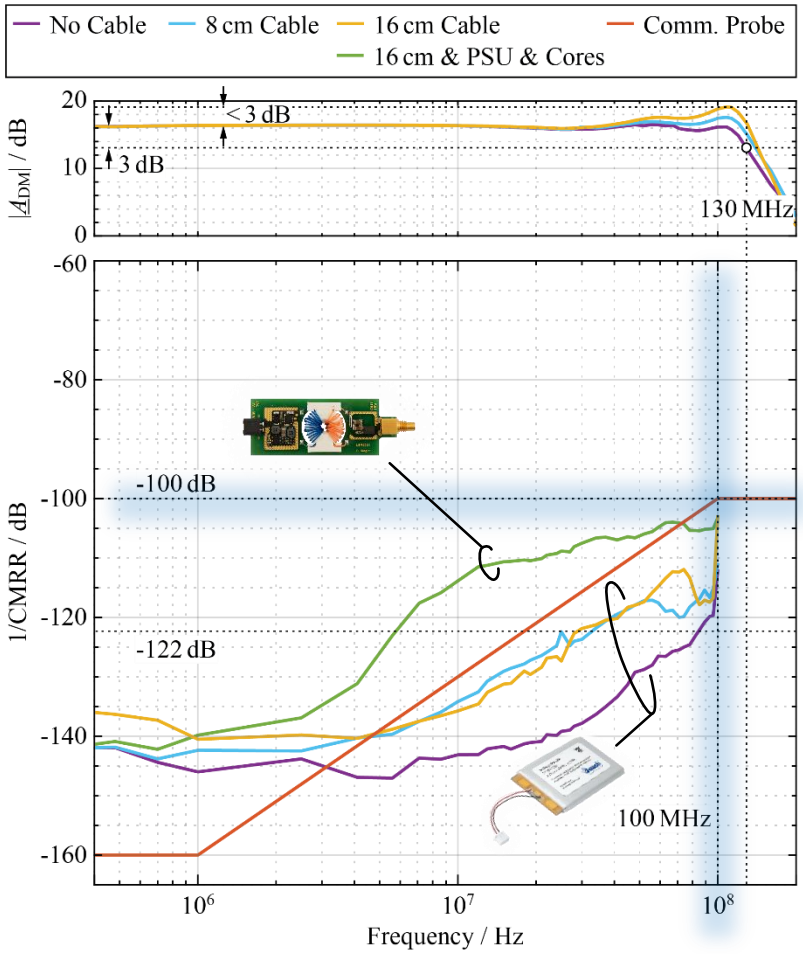
→ Coupling capacitance < 2 pF, isolation > 1 kV (tested)

→ Unlimited operating time

Experimental Verification



◀ Freq. Dom.

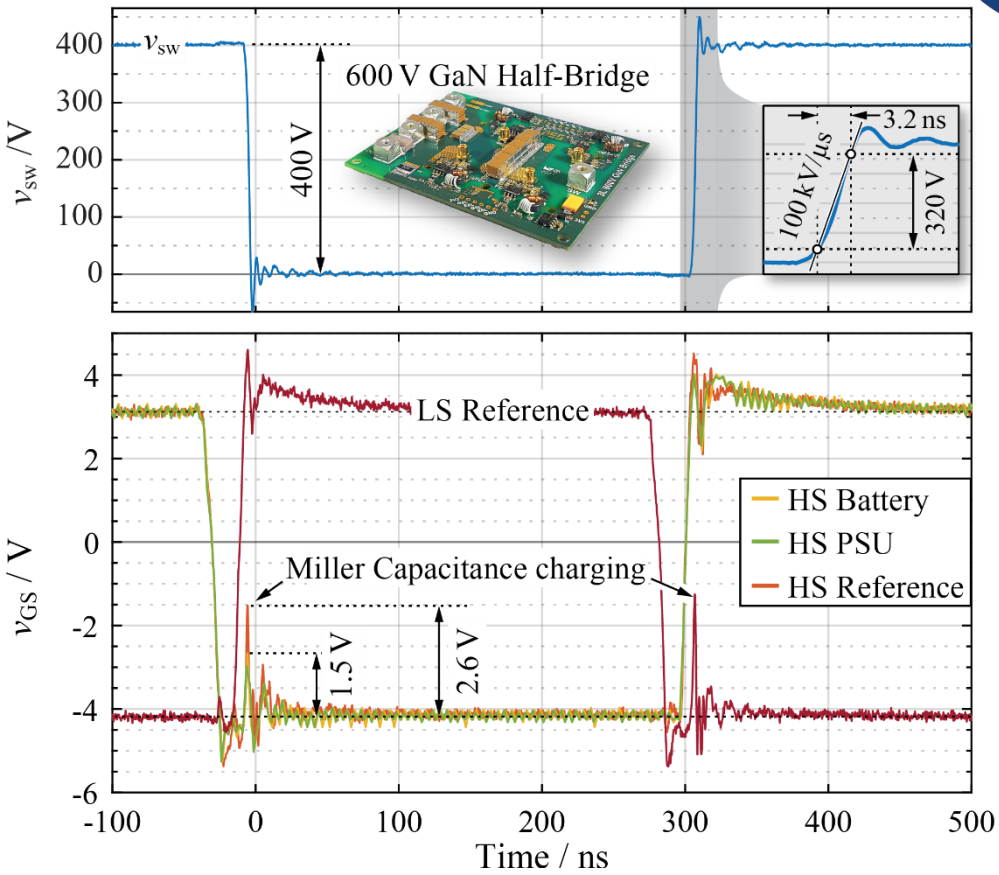


◀ 100 dB

◀ 100 MHz

→ >100 dB CMRR @ 100 MHz, 130 MHz BW

▼ Time Domain



→ Accurate tracking of $v_{GS,HS}$, no CM distortion

Conclusions / Summary

- Test and verification of Next Generation Power Electronics

▼ 3L3 UHBPA

- Part of P-HIL test env.
- Topological evaluation
- Hardware demonstrator with 25 kW/dm^3 power density
- 95.8 % efficiency @ 230 V_{rms}, 10 kW, 100 kHz

▼ I-Sensor

- Hall sensor BW extension to >50 MHz
- Diff. HF sensors compared
- Superior CMRR
- Compact design

▼ V-Sensor

- Isolated V-measurement
- Fluctuating ref. potential
- Isolated measurement system realized
- 130 MHz BW + 100 dB CMRR @ 100 MHz

→ Several challenges related to very high switching frequency converters addressed

Power Electronic Systems Laboratory

Thank you!

► Slides

Further Reading:

► P. S. Niklaus, J. W. Kolar, and D. Bortis, “100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier with 4.8 MHz Switching Frequency,” *IEEE Transactions on Power Electronics*, Vol. 38, No. 2, pp. 2307-2326, February 2023.
DOI: https://doi.org/10.1109/TPEL.2022.3213930

► F. Krismer, V. Behrunani, P. S. Niklaus, and J. W. Kolar, “Optimized Cascaded Controller Design for a 10 kW / 100 kHz Large Signal Bandwidth AC Power Source,” in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, October 11-15, 2020
DOI: https://doi.org/10.1109/ECCE44975.2020.9236149

► P. S. Niklaus, D. Bortis, and J. W. Kolar, “Beyond 50 MHz Bandwidth Extension of Commercial DC-Current Measurement Sensors with Ultra-Compact PCB Integrated Pickup Coils,” *IEEE Transactions on Industry Applications*, Vol. 58, No. 4, pp. 5026-5041, August 2022.
DOI: https://doi.org/10.1109/TIA.2022.3164865

► P. S. Niklaus, R. Bonetti, C. Stäger, J. W. Kolar, and D. Bortis, “High-Bandwidth Isolated Voltage Measurements with Very High Common Mode Rejection Ratio for WBG Power Converters,” *IEEE Open Journal of Power Electronics*, Vol. 3, pp. 651-664, September 2022.