Analysis of Active Ripple Current Compensators Employing Multi-Cell Switch-Mode Amplifier Topologies

Hans Ertl, Johann W. Kolar*, Gerald Morauf, Franz C. Zach

Technical University Vienna
Dept. of Electrical Drives and Machines
Power Electronics Section

Gusshausstrasse 27/372, A-1040 Vienna

phone: +43-1-58801-37235 fax: +43-1-58801-37297
email: j.ertl@tuwien.ac.at

* Swiss Federal Institute of Technology Zurich
Power Electronics and
Electrometrology Laboratory

ETH Zentrum, ETL 22 CH-8092 Zurich

phone: +41-1-632 28 34 fax: +41-1-6321212
email: kolar@lem.ee.ethz.ch

Abstract – In this paper an active ripple current compensator for improving the EMC behavior of mains connected PWM converters is analyzed. The proposed compensation system is formed by a multi-level multi-cell switch-mode amplifier connected in parallel to the pulse width modulated main converter which neutralizes the switching frequency current components of the main converter in order to significantly improve the mains voltage quality at the point of common coupling of the total system. With the proposed active system the application of bulky and expensive EMC filters which further show remarkable additional losses can be avoided to a large extent. The paper describes the operating and control principle, analyzes the compensation behavior as well as the control required for covering the losses of the compensator. Furthermore, guidelines for dimensioning and realization of the transducer required to determine the ripple of the main converter and considerations to realize this sensor/filter-device using a modified (air gapped) current transformer are given. Finally, an easy to implement circuit scheme to perform the required interleaved mode modulation of the multi-cell switch-mode amplifier is presented and analyzed.

1. INTRODUCTION

Medium power alternative energy systems such as photo voltaic plants or variable frequency wind or hydro turbines in general are connected to the public mains by pulse width modulated (PWM) DC voltage link IGBT converters [1]. Furthermore, applications of such grid-connected converters (**Fig.1**) for active three-phase rectification with sinusoidal input currents or for static var compensation have been known for many years [2]. However, due to the comparatively low switching frequency of these converters (usually lying in the region $f_{S,main} \approx 5\ldots10$ kHz, dependent on the power level) in order to maximize the efficiency, significant additional filtering effort is necessary to limit the switching frequency voltage components at the point of common coupling (PCC) to comply with the relevant EMC regulations. For filtering in most cases LCL type structures are used (Fig.1) where L_F "stabilizes" the dependency of the filter characteristic on the mains impedance and an additional dissipative damper path R_D/C_D is required to achieve proper dynamic behavior. However, this passive filter significantly contributes to the costs and to the power density of the total system, especially if very good suppression of the switching frequency components is required. Furthermore, additional losses essentially caused by R_D and by the equivalent series resistance (ESR) of L_F appear. The R_D-losses could be avoided if the filter damping is realized actively by adequate control of the IGBT converter [3,4]; however, with this method the filter damping is not given if the converter is in off-state and/or for higher order mains harmonics.

To avoid the drawbacks of the passive filtering as described before active systems have been proposed

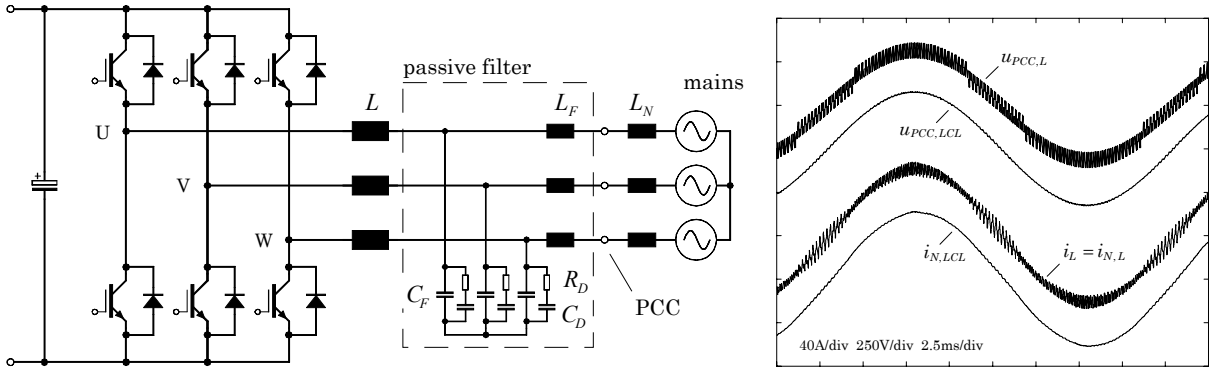

Fig.1: Circuit scheme and input current/voltage waveforms of a grid-connected PWM converter without (L) and with (LCL) additional passive input filter; parameters $P \approx 30$kW, $L = 1$mH, $L_F = 500\mu$H, $C_F = C_D = 10\mu$F, $R_D = 4.7\Omega$, $f_{S,main} = 5$kHz.

where an additional converter system operating at high switching frequency compensates the ripple current components of the main converter. The application of this principle is known in the lower power area for switch-mode (class-D) amplifiers [5] but also at high power levels for improving the input current of traction locomotives. E.g., the current ripple of the main input converter (realized using self-commutated thyristor technology) of the ÖBB Rh 1014 is compensated by her IGBT auxiliary supply converters [6].

However, an effective ripple compensation of such systems can be achieved only if the switching frequency of the compensation stage is sufficiently high as compared to the switching frequency of the main converter. Consequently, if the main converter itself is based on IGBT technology, the compensation stage would have to operate at very high switching frequencies if the unit is realized using conventional class-D amplifier technologies. This drawback, however, can be efficiently bypassed using class-D amplifier topologies proposed originally for testing applications [7].

2. RIPPLE COMPENSATOR – BASIC CONCEPT

According to **Fig.2**, the proposed ripple compensator is formed by two switch-mode current sources connected in line-to-line configuration to the PCC. Due to the assumed pure three-phase system (i.e., no connection of the DC link center point to the neutral line of the mains) the application of only two compensation sources inherently results in a ripple cancellation of all three phases originated by $i_{N,R} + i_{N,S} + i_{N,T} = 0$. The ripple of the mains converter is detected by a current transducer with a subsequent high-pass filter $H(s)$. As described in section 4, this current transducer can be realized advantageously using an air-gapped current transformer. Besides the

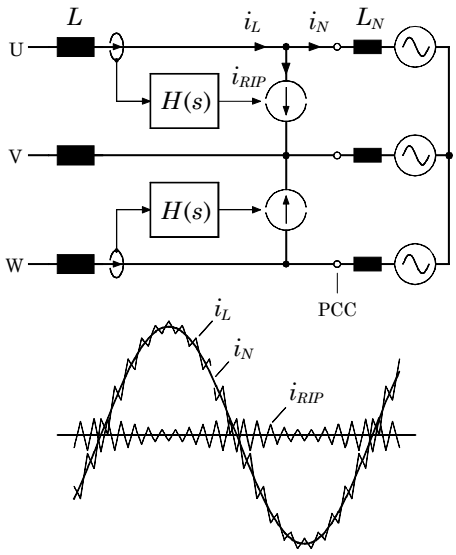

Fig.2: Basic topology and current waveforms of a three-phase active ripple compensator based on two line-to-line switch-mode current sources.

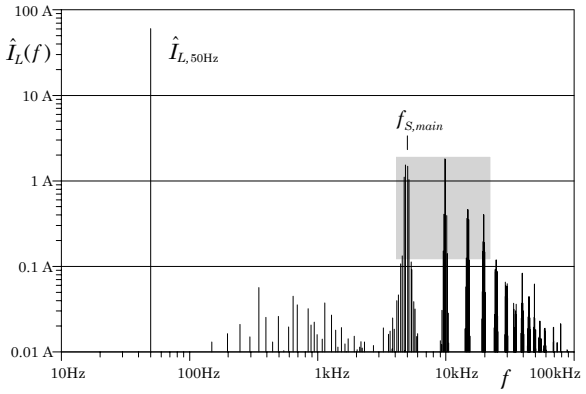

Fig.3: Spectrum of the output inductor current of a 30kW grid-connected IGBT converter (cf. Fig.1).

fact that in this case the secondary winding only has to be dimensioned regarding the ripple current component the lower cut-off frequency of the transformer already acts as a first stage of the high-pass filter.

It should be noted that for the idealized case no average power flow to or from the current source results. For optimal compensation, a pure sinusoidal line frequency voltage appears at the PCC and therefore also across the ripple current compensator. On the other hand, the current flowing through the compensator only shows switching frequency components, i.e., no cross correlation between current and voltage is existent and consequently an idealized compensator would not need a separate power supply. A real compensation system only has to cover its own losses (conduction and switching losses of the power stage as well as the power consumption of the driver stages and the control circuitry). As will be discussed in section 6, these losses can be balanced by the system itself if the compensator is equipped with a "resistor emulation" (i.e., a current component proportional to the appearing voltage). The value of the resistor to be emulated is provided by the DC link voltage control of the compensator.

The main problem of all ripple current compensators is the required bandwidth to cancel the harmonics of the main converter. If, according to **Fig.3**, e.g., the harmonics of the IGBT converter shown in Fig.1 shall be reduced to 0.1A resulting in a ≈55dB signal-to-noise ratio (50Hz-fundamental current to the residual switching frequency components), the compensator stage has to operate perfectly up to 20kHz as indicated by the shaded rectangle of Fig.3. Consequently, the ripple compensation stage has to meet audio amplifier quality levels, whereas on the other hand it has to be designed regarding the full line-to-line voltage (including transient overvoltages which may appear at the PCC) of the mains. Due to the basic fact of all class-D power amplifier systems that their effective switching frequency at least has to be 5...10-times the bandwidth which shall be achieved, the compensation current sources would have to operate at switching frequencies of 100...200kHz! Therefore, according to the

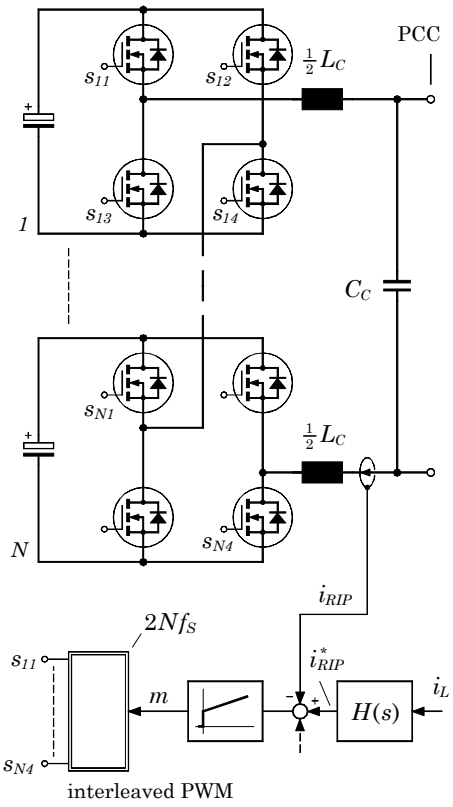

Fig.4: Power circuit and control structure for a multi-cell ripple current compensator.

required high DC link voltage of the compensator (which would have to be higher than the peak value of the line-to-line voltage of the mains, i.e., $U_D \approx 600\mathrm{V_{DC}}$ for a $400\mathrm{V_{RMS}}$ low-voltage mains) conventional hard-switched half-bridge switch-mode amplifier topologies would not be applicable efficiently. It should be noted that due to mains overvoltages semiconductor devices of at least 1000V blocking capability would be necessary. However, such MOSFETs show rather high on-state losses. Furthermore, also the switching losses would be substantial, even in case the internal diode of the MOSFET is blocked off by a serial diode and an explicit fast free-wheeling diode is used.

To avoid the problems discussed before, therefore, the application of a multi-cell class-D amplifier topology (as described in [7] for testing applications) is proposed here for realizing the power stages of the compensator. As indicated by **Fig.4**, the whole current source is formed by multiple (N) full-bridge switching cells which are connected in series regarding their output voltage. In case the individual cells are operated in an interleaved PWM mode the "effective" (regarding the dynamic behavior) switching frequency results to N-times the operating frequency of a single cell, i.e., $2N$-times the switching frequency f_S of the MOSFETs. Furthermore, simultaneously a significantly improved output voltage behavior of the compensator itself is achieved due to the fact that a single switching instant contributes only a voltage step of $1/N$-th of the total effective DC link voltage U_D of the system. Therefore, the total voltage ripple appearing at the output of the multi-cell topology is significantly reduced as compared to a single-cell (N=1) structure of equal transistor switching frequency. Furthermore, the multi-cell topology gives an additional benefit because the comparatively low DC link voltage of a single cell (e.g., typically $U_{DC}/N = 150\mathrm{V}$ for a compensator consisting of N=6 cells) allows the application of modern low-voltage MOSFET devices resulting in the fact that the cells can be operated at increased switching frequencies f_S. Originated by the interleaved PWM mode, the maximum output current/voltage ripple amplitude of multi-cell amplifiers as derived in [7] calculate to

$$\Delta i_{\max} = \frac{U_D}{8 f_S L_C} \cdot \frac{1}{N^2} \quad \Delta u_{\max} = \frac{U_D}{128 f_S^2 L_C C_C} \cdot \frac{1}{N^3} \quad (1)$$

and therefore is reduced remarkably for N=4...6-cell systems. The control of the system is performed in a manner that the signal gained from the high-pass filter $H(s)$ now acts as a reference value i^*_{RIP} for an, e.g., PI-type current controller (cf. Fig.4). The output of this controller gives the modulation index m (i.e., the duty cycle) of the interleaved PWM generator. However, an additional reference value would be required for DC link voltage control (cf. section 6). It should be noted that the output filter L_C, C_C of the multi-cell stage has to be dimensioned regarding the effective switching frequency $2Nf_S$ (e.g., 240kHz for $N = 6$ and a MOSFET operating frequency of $f_S = 20\,\mathrm{kHz}$) and hence these filter components are very small.

3. Ripple Signal Filter

In the following, the selection and dimensioning of the ripple signal filter $H(s)$ shall be analyzed. The total transfer function $G_C(s)$ of the compensator based on Fig.2 with $i_N = i_L - i_{RIP}$ is calculated to be

$$G_C(s) = \frac{I_N}{I_L} = 1 - \frac{I_{RIP}}{I_L} = 1 - \frac{H(s) I_L}{I_L} = 1 - H(s). \quad (2)$$

Thus, $H(s)$ has to be selected such that $G_C(s)$ results in a low-pass filter of higher order. To achieve an optimized ripple current rejection it would be obvious to choose a filter response with steep frequency roll-off, e.g., Chebychev or at least Butterworth response for $G_C(s)$. However, these filter characteristics show significant ringing (overshoot) which may be excited by load variations of the main converter. Consequently, a 3rd-order low-pass filter with an aperiodic damping characteristic given by

$$G_C(s) = \frac{1}{(1+sT_0)^3} = \frac{1}{1+3sT_0+3s^2T_0^2+s^3T_0^3} \quad (3)$$

has been chosen to optimize the transient behavior of the compensator. Using Eq.(2) this results in

$$H(s) = \frac{3sT_0+3s^2T_0^2+s^3T_0^3}{1+3sT_0+3s^2T_0^2+s^3T_0^3} \quad (4)$$

as transfer function which has to be implemented for the high-pass filter. Remark: This transfer function does not represent a "classical" 3rd-order high-pass which is characterized by the fact its numerator exclusively shows s^3-terms. If a classical high-pass would be used for $H(s)$, the compensator transfer characteristic $G_C(s)$ would only show a 1st-order roll-off at higher frequencies!

Now Eq.(4) can be divided according to $H(s) = H_1(s) \cdot H_2(s)$ into a series connection of a 1st-order high-pass $H_1(s) = sT_0/(1+sT_0)$ and a residual 2nd-order filter

$$H_2(s) = \frac{3 + 3sT_0 + s^2T_0^2}{1 + 2sT_0 + s^2T_0^2} \qquad (5)$$

which is of importance because $H_1(s)$ finally shall be realized by the intrinsic high-pass characteristic of the current transformer (cf. **Fig.5 (a)**) which senses the ripple of the main converter. Figure 5 (a) also gives a suggestion for implementing the filter part $H_2(s)$ using a passive LC structure. The calculation of this circuit (not given here for the sake of brevity), shows that its transfer function equals to Eq.(5) if the components are selected according to: $L_0C_0 = T_0^2$, $R_X = \frac{3}{2}Z_0$ and $R_Y = \frac{1}{2}Z_0$ with $Z_0^2 = L_0/C_0$. However, as is shown by the dimensioning, the application of this circuit is not very practical due to the influence of the ESR of the filter inductor L_0. If, e.g., $T_0 = 100\mu s$ is chosen, resulting in a filter cut-off frequency of $f_0 = 1/(2\pi T_0) = 1.6$kHz, the relationships given above are valid for $L_0 = 10$mH, $C_0 = 1\mu$F, $R_X = 150\Omega$, $R_Y = 50\Omega$. The ESR of L_0 is limited to values which are small compared to R_X; however, this in general would not be the case if small PCB inductors are applied (e.g., a 10mH size 2220-SMD coil shows a resistive component of ≥100Ω; furthermore its accuracy is usually only about ±10%). Therefore, alternatively, an active signal filter circuit is used to implement $H_2(s)$ (cf. **Fig.5 (b)**). This MI/DF bi-quad structure [8] requires only 3 standard OP-amplifiers, 3 capacitors of identical value and 7 resistors for realization. The dimensioning $R_0C_0' = T_0$ gives the required transfer function of Eq.(5).

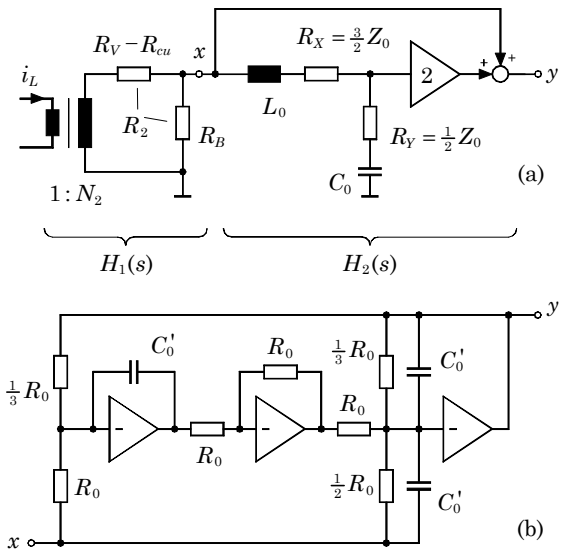

Fig.5: Ripple signal filter $H(s)$; (a) structure diagram, $H_1(s)$ realized by i_L-sensor; (b) bi-quad implementation of $H_2(s)$.

The simulation diagrams given in **Fig.6** demonstrate the excellent system performance if the passive filter of Fig.1 is replaced by the proposed compensation scheme using the previously described ripple signal filter ($T_0 = 100\mu s$). For $t \le t_1$ the ripple compensation is disabled for demonstration purposes. At time instant t_3 the load condition of the main converter is reduced to about 60%. Due to the dimensioning of the ripple signal filter (aperiodic damping) a fast but smooth response of the compensator is achieved.

However, the examination of the mains current spectrum (Fig.7 compared to Fig.3) indicates that the ripple suppression is not as perfect as might be expected, especially for the region of 5...10kHz. The reason for this is, as a more detailed analysis shows, not caused by the ripple signal filter and by the amplifier bandwidth but results here from a not optimized damping of the output filter (L_C, C_C in Fig.4) of the multi-cell stage.

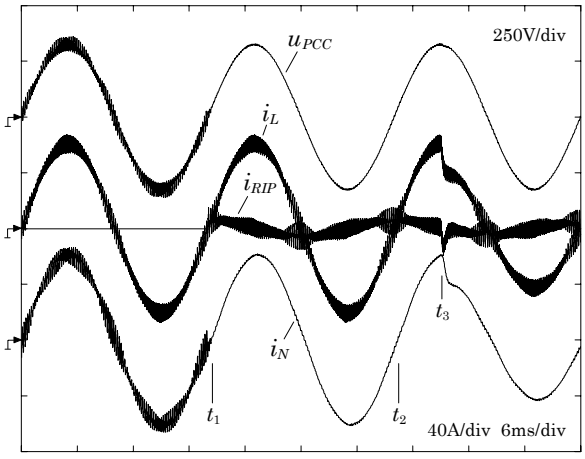

Fig.6: Operating behavior: $t \le t_1$: compensator disabled; $t \ge t_1$: compensator enabled; t_3: load step of main converter (ripple compensation also given during transients).

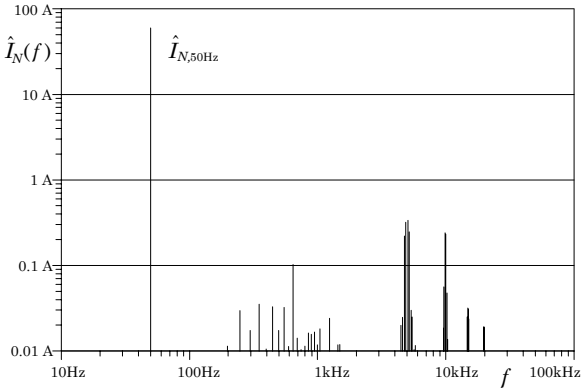

Fig.7: Spectrum of mains current i_N for [t_1,t_2] of Fig.6.

4. RIPPLE CURRENT TRANSDUCER

Due to the fact that the compensator only needs information about the ripple it is near at hand to use a current transducer which does not sense the total current of the main converter but measures particularly the switching frequency components. This results in a more compact sensing device as compared to the application of, e.g., bulky DC or line-frequency AC current transformers. In [9] a very interesting method of using a Rogowski coil as ripple current transducer has been proposed. The linear system presented in [9] aims for suppressing the switching frequency noise of a 125kHz SMPS and, therefore, is focused at high-frequency signals. The usage of a Rogowski coil transducer for a lower frequency region as being relevant for the compensator presented here would require a rather high number of turns in order to get good sensitivity based on the increased coil inductance. Consequently, the basic Rogowski principle shall be modified by increasing the inductance using an air-gapped core. The output voltage of the coil at no-load ($i_2 = 0$) follows $u = L_{coil} \cdot di_1/dt$ and has to be integrated to give a current-proportional signal. However, this can be performed by the transducer itself if the coil is terminated by a resistor ($i_2 \neq 0$). The resulting system now, however, can also be seen as a conventional current transformer where the air-gap determines the lower cut-off frequency and takes charge of the low-frequency primary current components as has been already mentioned in section 1.

For realizing the transducer a E25/13/7 N27 ferrite core has been chosen. According to Ampere's law and using an air-gap of $l = 0.5$ mm, the single-turn primary winding gives an induction value of $\mu_0/l = 2.5\,\mathrm{mT/A}$. Therefore, avoiding core saturation current levels of up to 100A would be allowed. Using the Al - value specified by the data sheet ($Al = 0.15\,\mu\mathrm{H}$) a secondary winding of $N_2 = 200$ turns of 0.25mm∅ wire (i.e., 1:200 current transforming ratio) results in a coil (magnetizing) inductance of $L_m = Al \cdot N_2^2 = 6000\,\mu\mathrm{H}$. As described in the previous section, the high-pass characteristic of the current transformer shall be used to implement the filter stage $H_1(s) = sT_0/(1+sT_0)$. Using $T_0 = L_m / R_2$ gives $R_2 = 60\,\Omega$ for the total resistance at the secondary side to achieve $T_0 = 100\,\mu\mathrm{s}$ as defined by the ripple signal filter. Considering $R_{cu} \approx 4\,\Omega$, the split-up of R_2 according to Fig.5 (a) into $R_V = 36\,\Omega$ (series resistor for adjusting T_0) and a burden resistor $R_B = 20\,\Omega$ gives a total transducer sensitivity of 0.1V/A. It shall be noted that due to the lower cut-off frequency of the current transformer ($f_0 = 1/(2\pi T_0) = 1.6\,\mathrm{kHz}$), the secondary winding does not show remarkable line frequency current components which reduces the necessary cross-section of the wire.

The measurement results of **Fig.8 (a)** confirm that L_m (and therefore consequently T_0) shows no significant variations for the relevant current region 0...60A. According to the measured frequency characteristic (cf. Fig.8 (b)), the transducer can be used up to 1MHz and shows a dynamic response (cf. **Fig.9**) being well suited for the described active ripple compensator. It has to be pointed out especially that the proposed ripple current sensor is a small and reliable device which can be manufactured using only low-cost standard components.

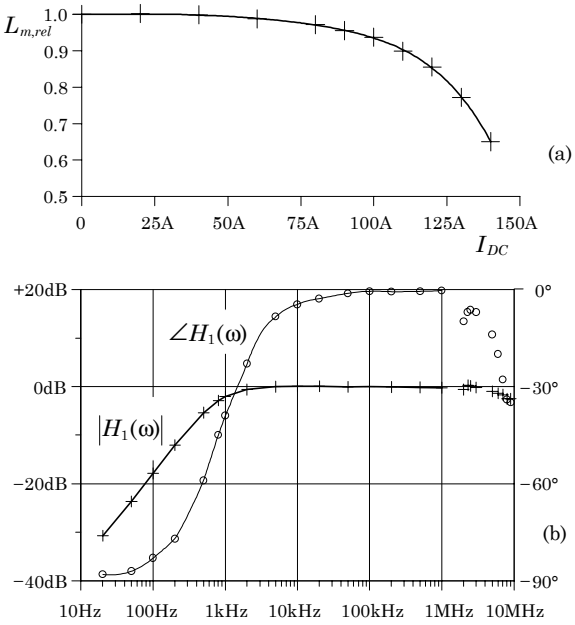

Fig.8: (a): Normalized transducer inductance L_m in dependency on low-frequency and/or DC biases; (b) frequency response (shown for a T_0 = 300µs transducer).

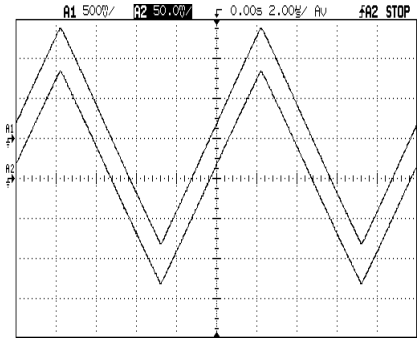

Fig.9: Transient response of the transducer: Measurement of a 100kHz triangle current (2µs/div); top trace: primary current 0.5A/div; bottom trace: burden voltage (R_B = 20 Ω), 50mV/div (i.e. current scale: 100mV/A).

5. INTERLEAVED PWM MULTI-CELL CONTROL

As described in section 2, the multi-cell class-D topology becomes very attractive if it is operated in an interleaved PWM mode. For a series connection of, e.g., $N = 6$ interleaved full-bridge stages, an effective output switching frequency appears being 12 times the switching frequency of the MOSFETs. Nevertheless, the effort to realize the interleaved PWM generator might be seen as an essential drawback of such

systems. As is shown, however, by the implementation given here, the whole current control of the compensator including the PWM generation requires comparatively few low-cost standard components. Similar to the solution given in [7] the interleaved pulse width modulator is based on phase shifted triangular carrier signals. However, these signals here are not generated by analog integrators but alternatively using simple RC low-pass stages (cf. **Fig.10**) starting from phase shifted square-wave (logic) signals u_{sq} which originate from a digital multiphase counter CTR. Consequently, these carrier signals show noticeable exponential shape and it is expected, that the linearity of the modulator would by far not be as perfect as for using purely triangular signals. As a detailed calculation omitted here shows, the transfer characteristic of this simple RC based modulator (normalized average output voltage u in dependency on the input modulation index m) results to

$$u(m) = \ln\frac{1+km}{1-km} \Big/ \ln\frac{1+k}{1-k} \qquad m = -1 \ldots +1 \quad (6)$$

with k being the peak-to-peak amplitude of the carrier signal referenced to the square-wave signal (i.e., $k = u_{tri,pp}/u_{sq,pp}$). Surprisingly, this characteristic for typical values $k = 0.5$ (i.e., $\tau = RC \approx T/4$) shows good linearity (cf. Fig.11). This is caused by the fact that the influence of the non-linearity of the carrier signals partially is compensated by the two half-periods of the signal. It has to be noted additionally that the modulator is part of the feedback loop which controls the compensation current i_{RIP}, hence modulator errors are also reduced by the loop gain. For $k = 0.5$, however, the modulator gain remains constant within $-10\%/+20\%$ (Fig.11).

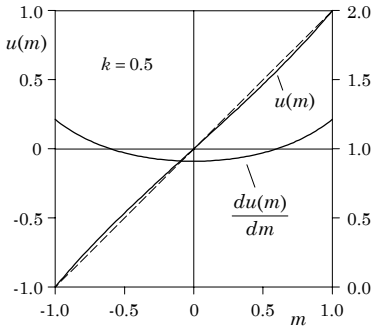

Fig.11: Normalized transfer characteristic $u(m)$ and gain $du(m)/dm$ of the pulse width modulator of Fig.10 given for $k = 0.5$.

As shown in Fig.10, the $2N$ driver signals gained from the PWM comparators have to be isolated by optocouplers for providing the necessary isolation between the individual floating power cells (cf. power circuit shown in Fig.4). The driving of the MOSFETs itself advantageously can be performed by integrated driver ICs (e.g., IR2110 etc.). To improve the transient behavior of the current control loop a feedforward of the compensator output voltage (u_{PCC} in Fig.10) is implemented.

Figure 12 demonstrates the high dynamic performance of the compensator current control. Here, a system with an effective switching frequency of ≈ 250kHz (i.e., $f_S \approx 20$ kHz MOSFET switching frequency) is analyzed. The gain of the PI-type controller has been chosen such that the bandwidth of the loop results to ≈50kHz (i.e., $2Nf_S/5$) and comes close to the theoretically possible maximum value of $2Nf_S/\pi$. This can be seen by the fact that the maximum slope of m comes close to the slope of the carrier signal u_{tri} (cf. circled area of Fig.12). The system shows a

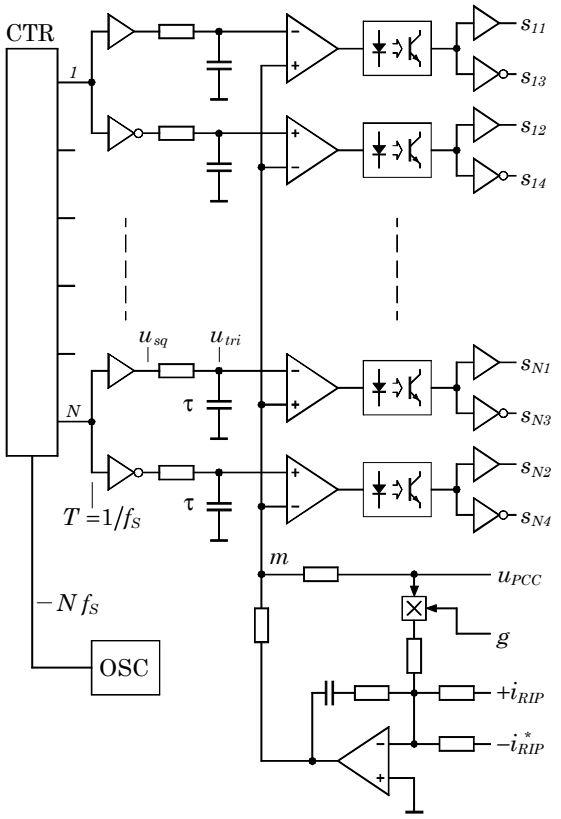

Fig.10: Schematic circuit diagram of the interleaved PWM generator and of the compensator current control.

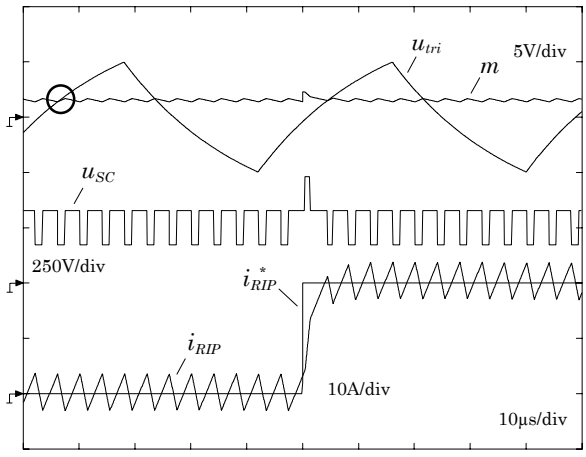

Fig.12: Modulator operation and transient response of the proposed current control. Here, u_{SC} denotes the total (multi-level) output voltage of all switching cells.

very fast transient response within a few micro seconds. The high effective switching frequency in connection with the multi-level characteristic makes possible to choose a very low output inductance (here $L_C = 20\,\mu\text{H}$ is used, cf. Fig.4). Furthermore, it should be kept in mind that i_{RIP} originally denotes the 5kHz-ripple of the main converter; the 250kHz-ripple component of i_{RIP} shown in Fig.12 would have to be suppressed by the high-frequency output filter L_C, C_C of Fig.4.

6. Loss Balancing – Power Supply

As already discussed in section 2 the idealized principle of a ripple compensator shows no average power flow. Theoretically no DC link power supply is required and the DC link capacitor has to be dimensioned only regarding the apparent switching frequency ripple currents. However, in a real system the losses of the compensator components have to be covered. Furthermore, it should be noted that the ripple signal filter, despite of a high-pass characteristic does not suppress the line-frequency current components of the main converter perfectly. Consequently, in connection with the line-frequency voltage at the PCC an average power flow may result, depending on the load state of the main converter. For stationary operation the compensator has to control this power flow to cover its own losses in order to guarantee a stable DC link voltage. Due to the four-quadrant characteristic of the topology this can be performed easily using the mentioned "resistor emulation" concept which shall be explained briefly. As shown in Fig.10, a line-frequency current component $g \cdot u_{PPC}$ is added to the current reference value. Thus, g acts as a "control conductance" which is defined by the output of a superimposed DC link voltage control. Because all stages are operated using equal modulation index m the individual DC link voltages are equal for an idealized system. Small un-symmetries which cannot be avoided in case of real systems can be balanced if the DC voltage links are equipped with small bias-resistor/voltage limitation networks.

7. Conclusions

The application of multi-cell multi-level amplifier topologies gives a very interesting possibility for realizing ripple current compensators for medium power grid-connected converters. Due to the lower DC link voltages of multi-cell topologies power MOSFET devices can be applied which result in higher switching frequencies. Furthermore, using interleaved PWM control, a high effective switching frequency is given resulting in a very good dynamic response of the unit which is necessary in order to achieve a good compensation performance. Using special control techniques, the system is able to cover its losses from the power terminals and no significant additional power supply is required.

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