A Novel Hysteresis Current Control for Three-Phase Three-Level PWM Rectifiers

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Abstract - **A novel hysteresis current control concept for three-phase three-level PWM rectifiers is presented. The proposed control is based on a virtual connection of the output center point and the mains star point and achieves a decoupling of the three phases. This control technique, besides having the advantages of a classical hysteresis control, provides a more regular switching of the power transistors and an intrinsic stability of the output center point voltage, and allows a full utilization of the modulation range. The novel control concept is discussed and compared to conventional current control techniques. Furthermore, the current control is digitally implemented and experimental results for controlling a Vienna Rectifier are presented.**

I. Introduction

For three-phase, three-level rectifier systems (cf. **Fig. 1**) a control of the input phase currents and of the output voltage has to be provided. Furthermore, a balancing of the partial output voltages and/or a control of the output voltage center point potential (cf. *M* in Fig. 1) has to be implemented. In general there are two categories of current controllers used for three-level rectifier control, conventional carrier-based controllers (CCC, which are usually denominated as average current mode control for single phase systems) and the conventional hysteresis control (CHC) [1-2].

The CCC employs in each phase a P-type controller, a PWM triangular carrier and a comparator to generate the gate drive signal of the corresponding transistor. The main advantages of the carrier-based method are a fixed frequency, which simplifies the EMI filter design and the natural center point stability. However, the CCC requires a control–oriented modeling of the system [3] and a mains voltage pre-control signal in order to insure a sinusoidal input current shape with low control error [4]. In addition, the CCC has a relatively low dynamic performance and requires additional control effort to compensate for non-idealities such as differences in the switch delay times.

In contrast, the CHC derives the transistor gate drive signal from a direct comparison of the actual line current and the current reference. This technique is easier to implement than a carrier-based controller and does not require any control system analysis. The CHC also shows high dynamics and is highly robust. However, it is characterized by the disadvantage of a non-constant switching frequency and/or irregular switching. The actual switching frequency depends on the input inductance of the PWM mains side inductors, on the width of the hysteresis band and on the operating conditions, such as the input and output voltage levels. Furthermore, the CHC has no natural stability of the output center point voltage [8].

Therefore, both control methods present advantages and drawbacks. For three-phase *two-level* PWM rectifier systems with CHC additional circuitry has been proposed to limit the maximum switching frequency [5, 6], or to keep it even constant [7, 9-11]. In particular, [9] proposes a hysteresis control method for two-level PWM inverters that eliminates the interaction between the phases thus allowing a phase-locked loop control of the modulation frequency of the switches.

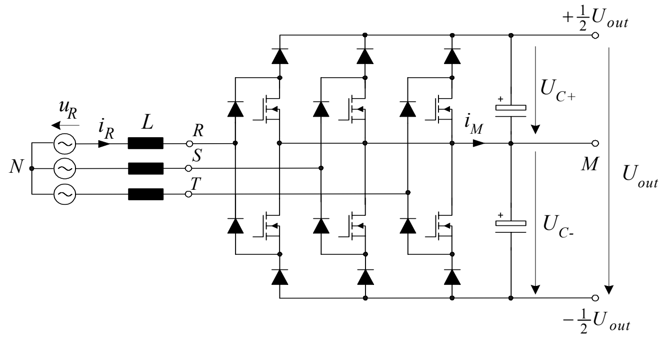

Fig. 1. Basic power circuit structure of a three-phase, three-level rectifier.

An analogous approach would be interesting for three-phase *three-level* rectifiers (cf. Fig. 1). This paper proposes such control concept, which decouples the three phases by extending the actual phase currents by a zero sequence current component and results in a virtual connection of the mains star point *N* and of the output center point *M*. Accordingly, the proposed current control is named Decoupling Hysteresis Control (DHC). The decoupling provides a more regular switching and a natural stability of the output center point. Furthermore, the advantages of the conventional hysteresis control such as excellent dynamic performance, low complexity of implementation, and direct compensation of non-idealities (e.g. of gate drive and switching delay times and power semiconductor on-state voltage drops) are maintained.

In **Section II** the basic conventional control concepts, i.e. CHC and CCC are briefly described. In **Section III** the principle of operation of the DHC is discussed and a comparison to the CHC and CCC is given. Finally, **Section IV** presents experimental results, obtained from employing a digital signal processor (DSP) implementation of the DHC for a three-phase three-level Vienna Rectifier.

II. Conventional Input Current Control

A. Conventional Hysteresis Current Control

For three-phase, three-level PWM rectifier systems the CHC, shown in **Fig. 2**, is implemented independently for each phase. Each current controller directly generates the switching signal, s_i' (1), where *i* indicates the phase *R*, *S* or *T*. For the case of positive input current, if the error between the phase current, i_i, and the reference sinusoidal current, i_i^*, exceeds the upper hysteresis limit $+h$, the power transistor of the corresponding phase is turned off, causing i_i to decrease. Once i_i reaches the lower hysteresis limit $-h$, the power transistor is turn on again, the phase current increases and the cycle repeats.

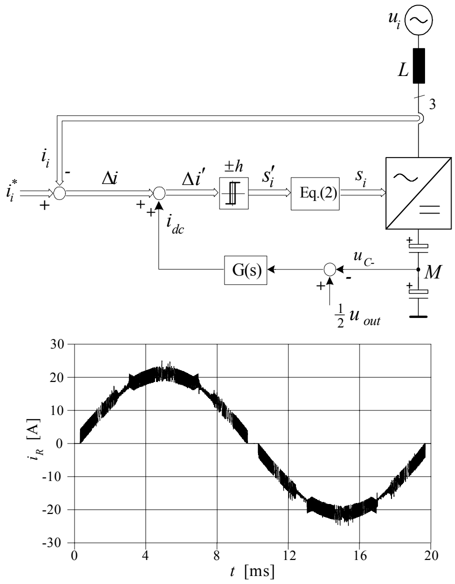

Fig. 2. Block diagram and simulated rectifier input phase current for conventional hysteresis current control (CHC). Simulation parameters are defined in Section III D.

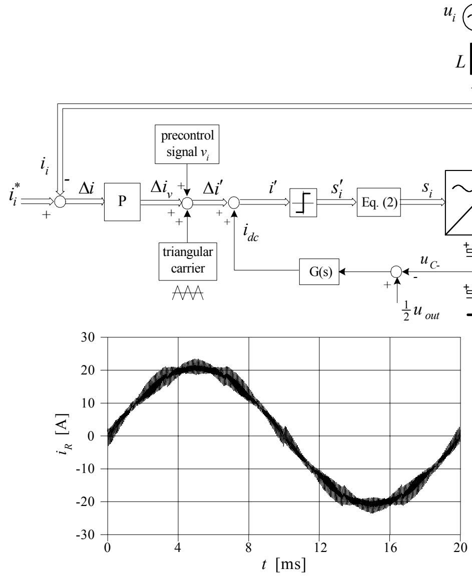

Fig. 3. Block diagram and simulated rectifier input phase current for conventional carrier-based current control (CCC). Simulation parameters are defined in Section III D.

$$s_i' = \begin{cases} 0 & if \quad i_i > i_i^* + h \\ 1 & if \quad i_i < i_i^* - h \end{cases} . \tag{1}$$

The final switching decision, s_i, is determined considering the direction of the mains phase current [8] or the sign of the corresponding reference current i_i^* as given in (2) or of the related mains phase voltage u_i ($i_i^* \sim u_i$)

$$s_i = \begin{cases} s_i' & if \quad i_i^* \geq 0 \\ NOT\, s_i' & if \quad i_i^* < 0 \end{cases} . \tag{2}$$

In Fig. 2 this is considered in the block labeled with Eq.(2).

The resulting input current waveform (cf. Fig. 2) exhibits time intervals where no switching occurs. This clearly indicates a mutual influence of the phase current control circuits. Furthermore, as shown in [8] the rectifier output center point is not naturally stable and therefore must be actively controlled. This could be achieved in the simplest case by a P-type control (block G(s) in Fig.2) which generates an offset, i_{dc}, of the phase current reference values in case an output center point voltage shift

$$\Delta U_M = \frac{1}{2}(U_{C+} - U_{C-}) \tag{3}$$

occurs (U_{C+} and U_{C-} are the upper and the lower output partial voltage).

The CHC has among its advantages, simplicity of implementation, robustness, and excellent dynamics but results in irregular switching and is characterized by a dependency of the average switching frequency on the mains voltage and output voltage ratio, the absolute mains voltage level, the input inductor value and the width of the hysteresis band amplitude.

B. Conventional Carrier-based Current Control

For CCC, the switching decision s_i', is the result of a comparison of the dynamically weighted current error (in the simplest case only a P-type control is employed) with a triangular carrier signal, as shown in **Fig. 3**. The use of a triangular carrier results in a constant switching frequency.

As with the hysteresis control, the final switching decision, s_i, depends on the sign of the corresponding mains phase current reference value.

In order to ensure a low current control error and/or a sinusoidal input current shape also for P-type control, a mains voltage pre-control signal, v_i, is added to the current controller output. The time behavior of the pre-control signal can be derived from an analysis of the input voltage formation [4] resulting in

$$v_i' = \begin{cases} \hat{I}_{CS}\left(\dfrac{4u_i}{U_{out}} - 1\right) & if \; i_i \geq 0 \\ \hat{I}_{CS}\left(\dfrac{4u_i}{U_{out}} + 1\right) & if \; i_i < 0 \end{cases} \tag{4}$$

($\hat{I}_{CS}$ represents the amplitude of the triangular carrier signal) which then is extended by a third harmonic, $v_i = v_i' + u_3$ ($u_3 = \frac{1}{2}$ (max $\{u_R, u_S, u_T\}$ + min $\{u_R, u_S, u_T\}$)) in order to allow a full utilization of the modulation range.

As the output voltage center point of the rectifier for CCC is naturally stable [8], theoretically no output voltage center point control would have to be provided. However, in a practical realization an asymmetry of the partial output voltages can occur due to non-idealities such as different switching and gate drive delay times of the phases. Therefore, a control of the center point voltage is implemented following the same concept as for the CHC.

For the switching state sequence of the CCC a subsequent rectifier switching state is achieved by changing always only the switching state of one phase. Compared to that the switching of the CHC is highly irregular, what results in a higher average switching frequency for equal input current ripple rms value (cf. Fig. 9).

III. DECOUPLING HYSTERESIS CONTROL

A. Principle of Operation

The basic concept of the proposed control can be clearly shown based on an equivalent circuit of the AC part of the three-phase PWM rectifier depicted in **Fig. 4**.

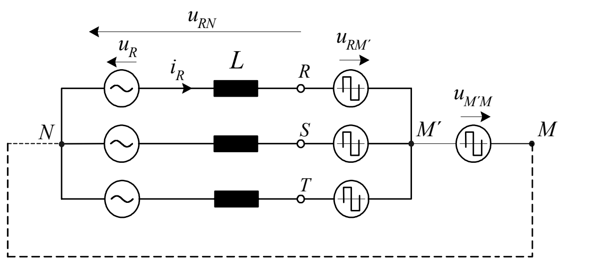

Fig. 4. Equivalent circuit of the AC part of a three-phase PWM rectifier (dashed line shows a virtual connection of N and M established by the control).

The shape of the input phase current i_i, (index i indicates phase R, S or T) is defined by the voltage across the input inductors $u_{L,i}$

$$\begin{cases} L\dfrac{di_R}{dt} = u_{L,R} = u_R - u_{RN} \\ L\dfrac{di_S}{dt} = u_{L,S} = u_S - u_{SN} \\ L\dfrac{di_T}{dt} = u_{L,T} = u_T - u_{TN} \end{cases} \tag{5}$$

where u_i is the mains phase voltage and u_{iN} denotes the rectifier input voltage referred to the mains star point N.

As the mains star point, N, and the rectifier output center point, M, are not connected we have for the rectifier input voltage

$$\begin{cases} u_{RN} = u_{RM} + u_{MN} \\ u_{SN} = u_{SM} + u_{MN} \\ u_{TN} = u_{TM} + u_{MN} \end{cases}, \tag{6}$$

where u_{iM} are the rectifier input voltages referred to M, and u_{MN} is the zero sequence voltage occurring between the mains star point and output center point. Furthermore, the sum of the phase currents is forced to zero

$$i_R + i_S + i_T = 0\,. \tag{7}$$

In addition for a symmetric mains

$$u_R + u_S + u_T = 0 \tag{8}$$

is valid. Taking (7) and (8) into account, it follows from (5) and (6)

$$u_{MN} = -\frac{1}{3}(u_{RM} + u_{SM} + u_{TM}) \tag{9}$$

which corresponds to a mutual coupling of the three phases.

In case M and N would be connected ($u_{MN} = 0$), and/or

$$u_{iN} = u_{iM}, \tag{10}$$

the current in each phase would only be dependent on the respective rectifier phase and mains phase voltage and a zero sequence current driven by u_{MN} would flow in the center point to neutral connection.

For the proposed DHC, the connection of N and M is virtually established (shown by a dashed line in **Fig. 4**) by adding a zero sequence current i_0 to the actual phase current ($i_i' = i_i + i_0$, cf. **Fig. 5**) where i_0 is generated by the integration of the measured zero sequence voltage u_{MN}

$$i_0 = \frac{1}{L}\int_T u_{MN}\,dt \tag{11}$$

(L denotes the phase inductance). Therefore, the controller processes the same error signal as for an actual connection of N and M. Accordingly, a decoupling of the three phases is realized.

In **Fig. 6**(a) the simulated time behavior of the virtual phase current i_i' and of the corresponding actual phase i_i is shown. The control error $\Delta i_i' = i_i^* - i_i'$ processed by the hysteresis controller is depicted in Fig. 6(c), the switching frequency ripple of the actual phase current is shown in Fig. 6(d).

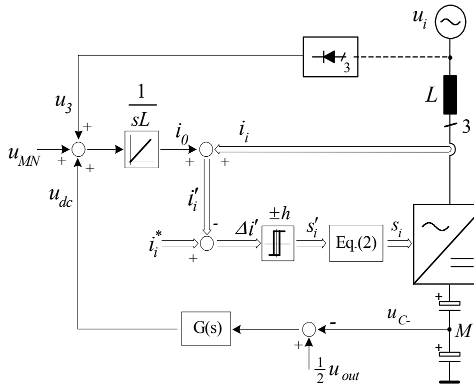

Fig. 5. Control structure of the proposed current controller. The relation of s_i' and s_i is like for the CHC (cf. (1)-(2)), [15].

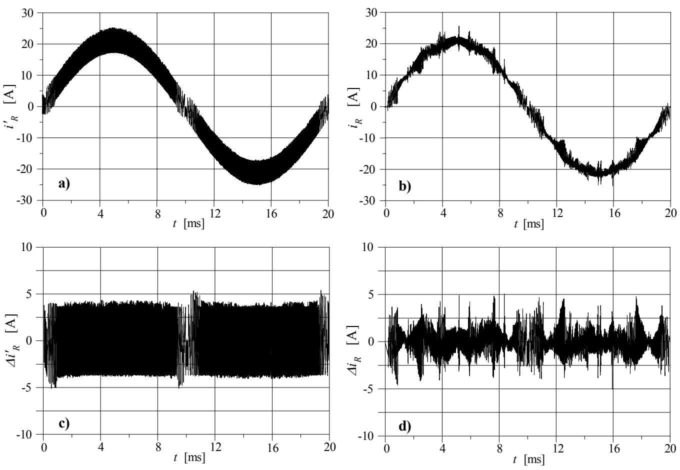

Fig. 6. Simulated time behavior of $i_R' = i_R + i_0$ (cf. Fig.5) **(a)** and of the actual mains current i_R **(c)** within one mains period in case of DHC. The respective current ripples are shown in **(b)** and **(d)**. Simulation parameters are defined in Section III D.

B. Extension of the Modulation Range

The modulation index, M, is defined as

$$M = \frac{\hat{U}_i}{\frac{1}{2}U_{out}} \tag{12}$$

where $\hat{U}_i$ is the amplitude of the fundamental of the rectifier input voltage and U_{out} denominates the rectifier output voltage. The virtual connection of M and N would allow the formation of the rectifier input phase voltage amplitude only up to $U_{out}/2$. In order to extend the linear modulation range to its actual maximum, $M_{max} = 2/\sqrt{3}$, an additional zero sequence signal u_3, having three times the fundamental frequency, has to be added to the zero sequence voltage u_{MN}.

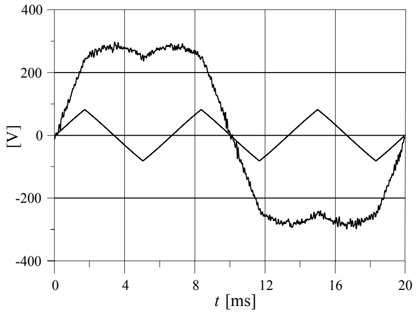

Fig. 7. Simulated time behaviour of the local average value of a rectifier input phase voltage u_{iM} (with reference to M) and time behavior of u_3 injected into the control loop. The resulting shape of $u_{iM,avg}$ is identical to third harmonic injection of CCC [13] and therefore allows a full utilization of the linear modulation range.

In practice this voltage can be obtained from the output voltage of a three phase diode bridge [13], or, mathematically using

$$u_3 = \tfrac{1}{2}\,max\,\{u_R, u_S, u_T\} + \tfrac{1}{2}\,min\,\{u_R, u_S, u_T\}\ . \tag{13}$$

The difference of u_3 and u_{MN} is integrated and added to the current control error in the same fashion as u_{MN} in (11). As the actual input current is still controlled to a sinusoidal shape, this leads to the formation of a third harmonic and/or zero sequence component of the rectifier input voltage which cancels u_3 at the input of the integrating element $1/sL$ (cf. Fig.5). This is verified by digital simulation in **Fig. 7**.

C. Output Partial Voltages Balancing

As a detailed analysis shows, the proposed current control results is the natural stability of the rectifier output center point M and/or exhibits a self balancing of the output capacitor voltages U_{C+} and U_{C-}.

In **Fig. 8**(a) the dependency of the midpoint current (global) average I_M on the output center potential shift ΔU_M defined in (3) is depicted for CHC (dashed line, for a proof of the instability of M in case of CHC see [8]) and for the proposed DHC (bold solid line). Furthermore, an approximation of the characteristic of the DHC (thin line) is included which could be analytically derived as follows.

If one assumes the three phases to be decoupled, each single phase circuit can be considered as conventional single-phase boost converter where the total midpoint current i_M of the three-phase system can be calculated as

$$i_M = i_{MR} + i_{MS} + i_{MT}\ . \tag{14}$$

For each boost converter the output current i_{Mi} is related to the respective input current i_i by the duty cycle d_i

$$i_{Mi} = d_i \cdot i_i \tag{15}$$

where d_i is defined by

$$d_i = \begin{cases} 1 - \dfrac{|u_i|}{U_{C+} + \Delta U_M} & if\ \ u_i, i_i \geq 0 \\ 1 - \dfrac{|u_i|}{U_{C+} - \Delta U_M} & if\ \ u_i, i_i < 0 \end{cases} \tag{16}$$

This clearly shows that, e.g. $\Delta U_M > 0$ ($U_{C+} > U_{C-}$) results for $u_i > 0$ in a reduction and for $u_i \leq 0$ in an increase of the corresponding power transistor turn-on time. Accordingly, in the average over the half period $u_i > 0$ a lower share of the phase current $i_i > 0$ is switched to the output center point M than drawn from M within $u_i \leq 0$ ($i_i \leq 0$).

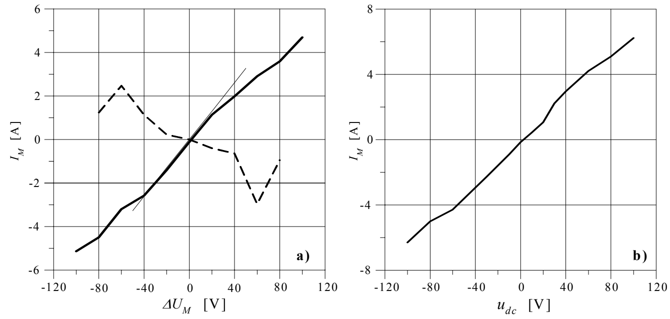

Fig. 8. **(a)** Natural stability of the output center point for DHC (bold line) and instability for CHC (dotted line, [8]); analytically derived characteristic of the DHC shown by thin line. **(b)** Center point control characteristic for DHC.

This results in a positive global average value of the center point current $I_M > 0$, charging C_- and discharging C_+ what finally decreases ΔU_M. The corresponding characteristic is depicted in Fig. 8(a).

Analogous to CHC (cf. Fig. 2(a)) a zero sequence voltage u_{dc} can be used for DHC to implement a feedback control of the midpoint current average value I_M and/or of the midpoint potential shift ΔU_M, as shown in Fig. 5. The corresponding control characteristic, i.e. the dependency of I_M on u_{dc} is represented in Fig. 8(b).

D. Average Switching Frequency, Input Current Ripple and Conducted EMI

The average switching frequency f_{avg} can be calculated starting from the time distribution of the switching state changes $\tilde{s}_i$, where $\tilde{s}_i = 1$ for each change of switching state. The local switching frequency is then provided by the number of occurrences of $\tilde{s}_i$ within a sliding time window Δt centered in t_{loc}, $0 \leq t_{loc} \leq T/2$, and given by

$$f_{loc} = \frac{1}{2\Delta t} \sum_i \left. \tilde{s}_i \right|_{\Delta t}\ . \tag{17}$$

Fig. 9 shows the switching frequency distribution derived for a window of Δt = 300 μs according to (17), in case of CHC, CCC, and DHC. In this latter case, the switching frequency is nearly constant whereas for CHC a highly irregular switching occurs.

The parameters of the simulations in this paper have been set to obtain the same current ripple rms value, Δi_{rms} = 1.27 A, for the three control concepts. The parameters are:

L = 450 μH,
U_{out} = 800V
$\hat{U}_i$ = 327 V
$\hat{I}$ = 21 A
M = 0.81.

The hysteresis band for the CHC is h = 2 A, while it is h' = 3.6 A for DHC, and the switching frequency for the CCC is f = 14.5 kHz. Besides the switching losses, the rms input current ripple level is also related to the average switching frequency. The current ripple level is directly dependent on the modulation index M, the input inductance value and on the hysteresis band amplitude (excluding CCC). In the case of the CCC, it also depends on the carrier waveform shape [4]. For the three controllers under study, the dependence of the current ripple ΔI_{rms} on the modulation index M is compared in Fig. 9(d) for a constant average switching frequency equal to 26 kHz. This shows

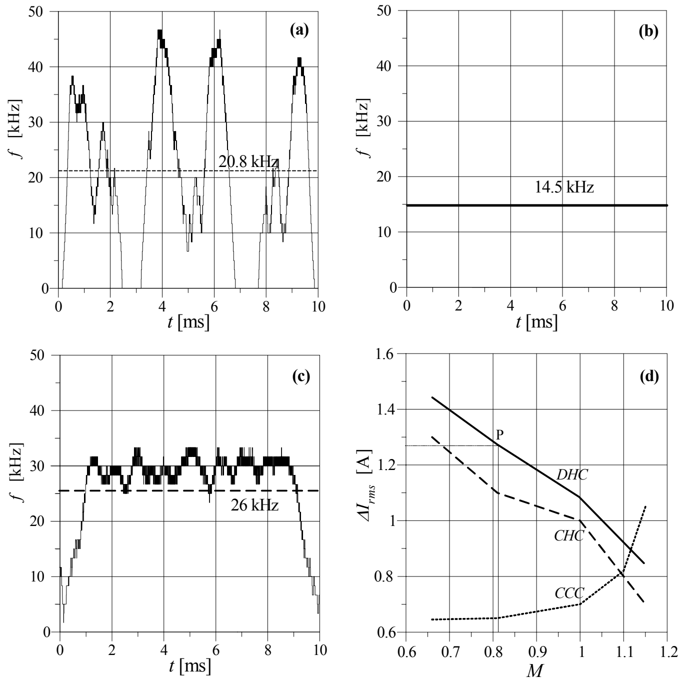

Fig. 9. Time behavior of the switching frequency distributions within a half mains period in case of CHC **(a)**, CCC **(b)** and DHC **(c)**. **(d)** Dependency of the input current ripple rms value ΔI_{rms} on the modulation index M for CHC (dashed line), CCC (dotted line) and DHC (solid line) for constant average switching frequency f_P = 26 kHz and operating parameters according to Section III D. Point P in **(d)** refers to the operating point of **(c)**.

that the DHC has an increased rms current ripple than the CHC, although the DHC has a more uniform switching frequency than the CHC. While the CHC and DHC show a decreasing current ripple for an increasing M, in order to keep the average switching constant, the current ripple for the CCC is increasing.

Fig. 10 shows the simulated frequency spectra of the differential mode voltage measured by a LISN at the mains side of the rectifier operated with CHC, CCC and DHC respectively. While the spectrum of the CCC exhibits the typical prominent harmonic amplitudes around the carrier frequency and its harmonics, the spectrum of the DHC, although very similar to the one of a CHC, is actually more spread and has the best EMI performance of the three controllers.

E. Dynamic Behavior

It is stated in the literature that a hysteresis current controller has an excellent dynamic behavior [9-11]. To analyze the dynamics of the input phase currents when the DHC is implemented, a sequence of step changes in the reference current are simulated. The results presented in Fig. 11 are for a step decrease (21 A to 5A) and a step increase (5A to 30 A) in the peak value of reference current. The input phase current waveforms show that there is an almost instantaneous change in the input current to the new reference level. This shows the excellent dynamics performance capable of the DHC.

IV. Experimental Analysis

A. Input Inductors Dimensioning

The appropriate dimensioning of the inductive components is an important issue to obtain high power density and low specific weight of the converter. A ferrite core inductor and an iron-power core one have been dimensioned and compared. The basis for the comparison is that they result in the same current ripple Δi_{rms} = 1.27 A for M = 0.81 and output voltage U_{out} = 800 V.

The ferrite core inductor has been designed to have a constant inductance value of L_{lin}=450 µH. It has been realized with an E65-core of ferrite grade N27, with B_{sat} = 0.3 T, 54 turns (copper diameter d_c = 2.3 mm), operating at maximum rectifier input current $\hat{I} = 25$A corresponding to modulation index M= 0.66 which defines the worst-case operating condition. The total volume of the linear inductor is V_{lin}=192 cm^3. In comparison, a nonlinear inductor realized with an iron powder core, MICROMETALS T200-26B, 68 turns, toroidal thickness t = 35 mm and diameter d = 61 mm, resulting in an inductance value of L_{nonlin}= 750 µH at 0 A and in a volume V_{nonlin}= 102 cm^3.

Therefore, the volume of the input inductors can be reduced by about 50% when employing non-linear iron powder inductors instead of ferrite core ones, when they result in the same current ripple. Iron power core inductors have been employed in the converter used for the experimental validation of the proposed current controller, and they do not affect the modulation and the performance of the converter compared to the use of linear input inductors.

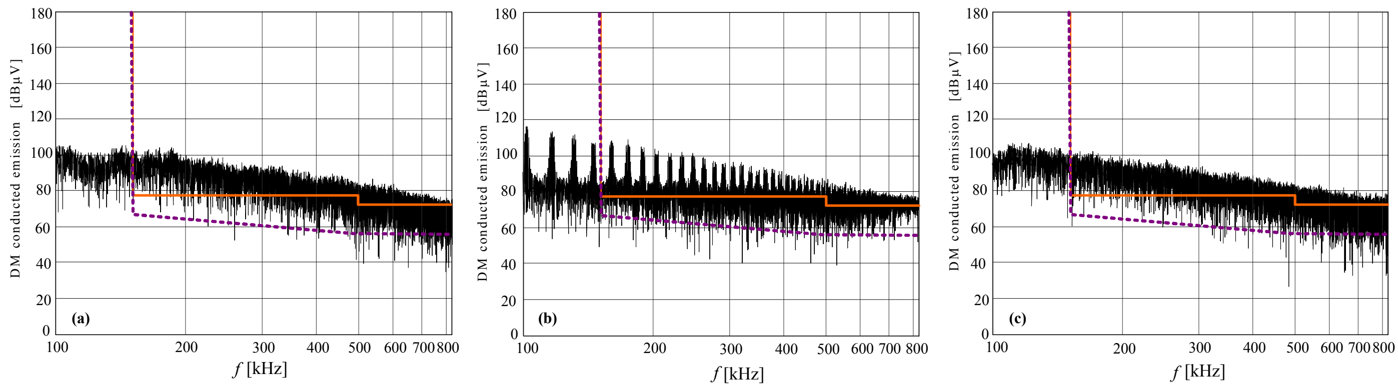

Fig. 10. Simulated frequency spectrum of the differential mode (DM) conducted noise which would be measured at the output of a LISN placed at the mains side of the rectifier. CHC **(a)**, CCC **(b)** and DHC **(c)**. In addition, the limits according to CISPR 16 for Class A (solid line) and Class B (dashed line) are indicated. For the spectra shown the most unfavorable points occur at 170 kHz **(a)**, 159.5 kHz **(b)** and 150 kHz **(c)** and the required attenuations for Class B are 89 dB, 84 dB and 80 dB respectively.

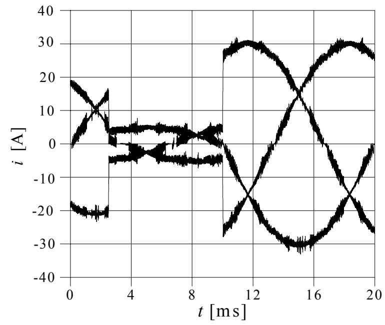

Fig. 11. Dynamic behaviour of the input currents for the DHC for a sequence of reference current amplitudes of 21 A, 5 A, 30 A.

B. Practical Implementation

The experimental evaluation of the DHC is achieved by using a three-phase, three-level Vienna Rectifier (VR). The VR is connected to a three-phase 200 V rms line-to-line, 50 Hz voltage source and operated with an output voltage of 350 V dc at an output power of approximately 2 kW. Non-linear, iron powder core, input inductors are used that have an inductance of 750 μH at 0A and reduces to approximately 300 μH at full load.

The current controller is implemented digitally using an Analog Devices ADSP21991 DSP, which is a 16-bit, 160MHz processor. The DSP is interfaced to the VR via a measurement and fault printed circuit board. Seven analog signals (2 line currents, 3 phase voltages and the 2 DC voltages) are sampled at 250 kHz using the internal 14-bit ADC. During the ADC conversion time of 425 ns for the two current signals, the algorithm calculates the midpoint to neutral voltage using derived phase to midpoint voltages that are based on the switch state, current direction and instantaneous capacitor voltages. The midpoint to neutral voltage is integrated and summed to the current reference. The DSP digitally implements the hysteresis current controller using the measured phase currents and reference current signals. All three switches are updated simultaneously at the end of the calculations. The calculation time is 2.5 μs, which represents a processor loading of 62.5%. The calculation of the reference current and third harmonic signals is made using the measured input phase voltages and is updated at a rate of 10 kHz.

C. Measurement Results

The operation of the proposed current controller has been experimentally verified. **Fig. 12**(a) shows the input phase voltage (115 V rms) and the input inductor current (6.5 A rms) generated by the CHC and DHC. For the DHC the switching can be seen to be occurring for majority of the input current waveform compared to the CHC where there are times in which no switching occurs due to the interaction of the phases. Fig. 12(b) shows the zoomed in version of Fig. 12(a) and additionally the gate to source voltage of the R-phase switch. It can be clearly seen from the gate drive signal that there is no switching occurring at the peak of the fundamental current for the CHC compared with the DHC in which there is more regular switching occurring. The current waveforms also show that the input current has excursions which go outside the hysteresis band (h = 0.5A). This is because of the discrete implementation of the current controller in which the switching can be delayed by up one sampling period plus the computation delay time. The level of current excursion is then dependent on the instantaneous di/dt of the input rectifier current [14].

The DHC also has the stated advantage in that it provides inherent stability of the centre point voltage (balancing of each of the capacitor's voltage). This operation can be seen in Fig. 12(c) where the top two traces are the upper and lower capacitor voltages for the CHC and the bottom two traces are the capacitor voltages for DHC. In the DHC case it can be seen that the capacitor voltages are balanced and regular, while in the CHC case the capacitor voltages are continuously varying and are irregular. Therefore these waveforms prove that the center point voltage is inherently stable using the DHC.

V. Conclusions

This paper has proposed a control concept for three-level three-phase rectifiers based on the hysteresis method, which takes advantage of the decoupling of the three phases by employing a virtual connection of the mains star point and the output center point in the control loop. The basic idea is to modify the control signal, by adding an additional current, in order to eliminate the phase interaction at the control level.

This new decoupled hysteresis controller produces a more regular switching frequency than that from a conventional hysteresis controller while retaining its advantages. In addition, the output center point voltage is intrinsically stable and the modulation range can be extended by adding a third harmonic signal to the current control error. The modified control strategy has been verified through simulation and experimental implementation in a DSP controlled Vienna Rectifier.

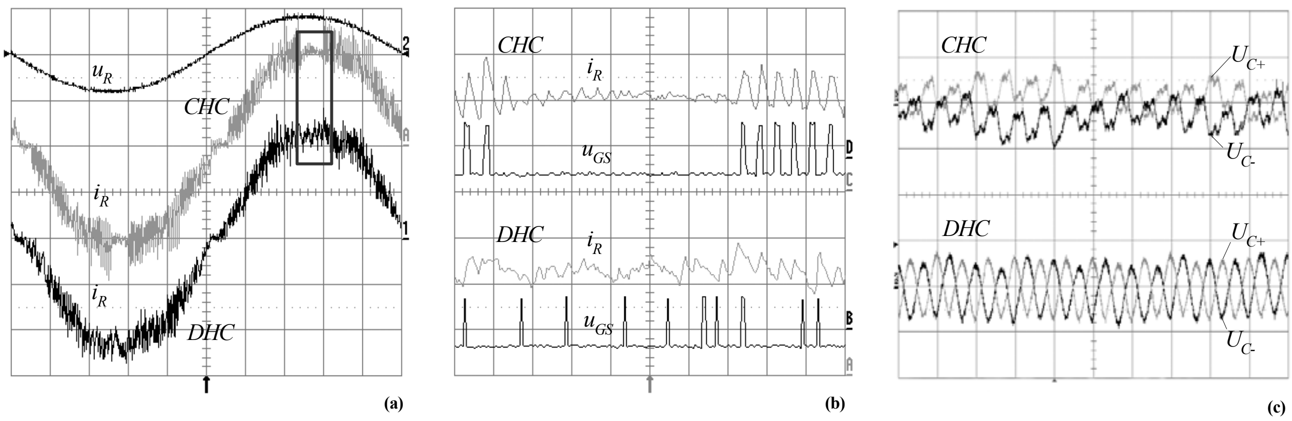

Fig. 12. **(a)** Input phase voltage u_R (100V/div) and input inductor current, i_R, for CHC and DHC (4A/div) **(b)** zoomed version of i_R (4A/div) and gate drive voltage (20V/div) for CHC and DHC **(c)** center point voltage controllability with top two traces are the upper & lower capacitor voltages for the CHC, while the bottom two traces are the capacitor voltages for DHC (All traces are AC coupled 5V/div).

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