New Wide Input Voltage Range Three-Phase Unity Power Factor Rectifier Formed by Integration of a Three-Switch Buck-Derived Front-End and a DC/DC Boost Converter Output Stage

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Abstract – A new three-phase unity power factor rectifier with a three-switch buck-derived input stage and a DC/DC boost converter output stage is presented. This system has a wide input voltage range and a continuous sinusoidal time behavior of the input currents lying in phase with the input voltages which is also guaranteed in case of a failure in one phase of the mains. The input currents are controlled using a switching state sequence showing minimum switching losses. A multi-loop system control is realized by an outer output voltage controller and an inner-loop buck+boost inductor current controller. Furthermore active damping of the input filter resonance is provided. For increasing the output power of the system a parallel connection of two interleaved units is proposed. There, a low input current ripple is achieved, and the cut-off frequency of the input filter can be shifted to higher frequencies (resulting in improved control dynamics and a more compact design downsizing of the inductors and of the input filter).

1 Introduction

The rectifier input stage of three-phase telecommunications power supply modules with sinusoidal input current usually is realized by a buck- or a boost-derived converter system [1]-[4]. Accordingly, the input voltage of the DC/DC converter output stage of the module being fed by the rectifier shows a lower or upper limit which is defined by the amplitude of the mains line-to-line voltage. Therefore, designing the power supply module for world-wide applicability, i.e. for a mains voltage range of nominal $208 \ldots 480\,\mathrm{V_{rms}}$ line-to-line, results in a high blocking voltage and high current stress and/or low utilization of the power semiconductors and power components (cf. Sections A and B in [5]) and/or translates in a relatively low efficiency of the energy conversion and high realization costs of the rectifier stage.

For solving this basic problem a combination of a buck and a boost rectifier topology (**Fig. 1**(a)) has been proposed in [5], [6] which gives the possibility of controlling the input voltage of the DC/DC converter to 400 V within the entire input voltage range mentioned. This results in an advantageous design of the power semiconductors of the rectifier stage and allows the application of a DC/DC converter technology being well-known from systems with single-phase AC supply. Furthermore, an auxiliary start-up circuit as required for rectifier systems with boost-characteristic can be omitted, and in contrast to standard buck-type systems a sinusoidal input current shape can be guaranteed also in case of a failure of one phase of the mains. However, owing to employing three single-phase units for the realization of the three-phase system the rectifier circuit proposed in [5], [6] shows a high complexity, i.e. comprises in total six turn-off power semiconductors and driver stages, three inductors and three output capacitors and requires special means for achieving a synchronized operation and equal distribution of the total output power to the individual units.

In this paper based on [7]-[10] a novel direct three-phase realization of the rectifier stage as depicted in Fig. 1(b) is proposed which shows a significantly lower complexity while main-

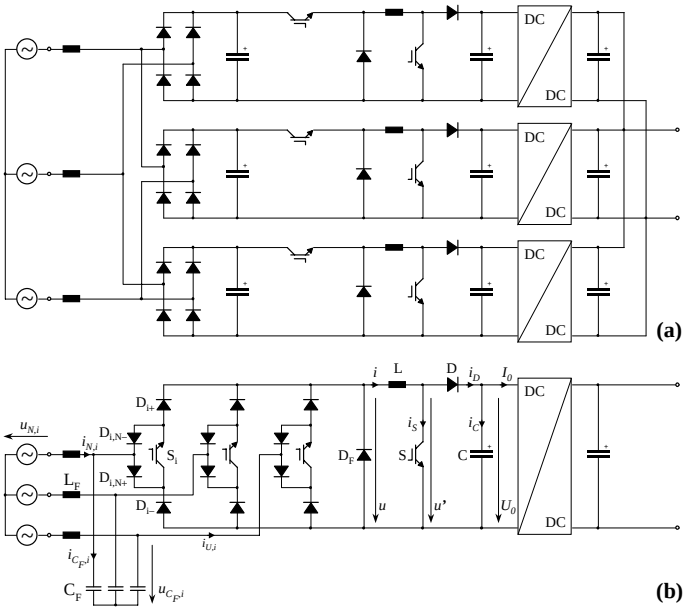

Fig. 1: Basic structure of the power circuit of a telecommunications rectifier module employing a conventional three-phase buck+boost power factor corrector **(a)** and proposed novel circuit topology **(b)** as rectifier input stage.

taining the basic advantages of the combination of single phase systems.

In **section 2** the basic principle of operation of the novel system is described. Analyzing the conduction states of the system the current space vectors being available for the formation of the input phase currents $i_{U,i}$ are calculated. A simple modulation scheme is proposed which guarantees a sinusoidal shape of the mains currents $i_{N,i}$ (switching-frequency harmonics of the discontinuous rectifier input currents $i_{U,i}$ are suppressed by a low-pass input filter) and minimum converter switching losses. Guidelines for the dimensioning of the power semiconductors and the buck+boost inductor are given and the possibility of minimizing the current ripple by synchronizing the switching of the buck input stage and the boost output stage is discussed. Furthermore, the optimum output voltage level and/or the optimum operating point for changing between buck and boost operation in order to achieve maximum system efficiency for a given mains voltage range is calculated.

The design of a multi-loop control of the rectifier, i.e. an outer output voltage control defining the reference values of an inner-loop boost-inductor current control is discussed in **section 3**. There, also an active damping of the input filter is provided.

In **section 4** the proposed control concept is verified by digital simulations, and finally, in **section 5** the possibility of a phase-shifted parallel operation of two systems for minimizing the filter requirement, which is the main topic of research being currently under progress, is described briefly.

2 Basic Principle of Operation

In the following, the basic principle of the stationary system operation is explained. Based on the investigation of the system conduction states the related input current space vectors are calculated, and a switching state sequence with regard to minimum switching losses is proposed. Furthermore, the current stresses on the power components are calculated analytically and the operating range of the buck stage in combination with the boost stage is determined, and a dimensioning example is given.

2.1 Assumptions

For the sake of simplicity we assume for the further considerations:

- a purely sinusoidal shape of the filter capacitor voltage, $u_{C_F,i} \approx u_{N,i}$ (identical to the mains voltage),

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\omega_N t), \\ u_{N,S} &= \hat{U}_N \cos(\omega_N t - \frac{2\pi}{3}), \\ u_{N,T} &= \hat{U}_N \cos(\omega_N t + \frac{2\pi}{3}), \end{aligned} \tag{1}$$

  and/or a mains voltage space vector

$$\underline{u}_N = \hat{U}_N \exp(\jmath\,\varphi_N), \tag{2}$$

  ($\varphi_N = \omega_N t$, ω_N denotes the mains angular frequency), and

- a constant inductor current I, a constant output current I_0 and a constant output voltage U_0.

Furthermore we will neglect

- the fundamental voltage drop $\jmath\omega_N L_F\,\underline{i}_N$ across the input filter inductors L_F, and
- the mains current ripple and the reactive current due to the filter capacitors C_F; i.e. consider the mains current to be approximately equal to the fundamental of the rectifier input current, $i_{N,i} \approx i_{U,(1),i}$.

Remark: The space vector related to a triple of phase quantities is calculated according to the defining equation (shown for the example of the mains phase voltages)

$$\underline{u}_N = \frac{2}{3}\left(u_{N,R} + \underline{a}u_{N,S} + \underline{a}^2 u_{N,T}\right) \qquad \underline{a} = \exp(\jmath\frac{2\pi}{3}). \tag{3}$$

In summary, for an ideally sinusoidal shape of the mains phase voltage we would like to form a fundamental of the rectifier input current lying in phase with the mains phase voltage ($\varphi_U \approx \varphi_N$)

$$\underline{i}^*_{U,(1)} = \hat{I}_{U,(1)} \exp(\jmath\varphi_U) \approx \underline{i}_N \tag{4}$$

where the index (1) denotes the fundamental component, the switching frequency components are largely suppressed by the input filter (L_F, C_F in Fig. 1(b)).

2.2 Conduction States and Current Space Vectors

Due to the phase symmetry of the converter structure and the symmetry of the mains voltage system a detailed analysis of the systems behavior can be constrained to a $\frac{\pi}{3}$-wide interval of the mains period. In the case at hand, a combination of the mains phase voltages $u_{N,R} > 0 > u_{N,S} > u_{N,T}$ being valid within the angle interval $\varphi_U \in (0; \frac{\pi}{3})$ (cf. **Fig. 2**, interval 1) is considered.

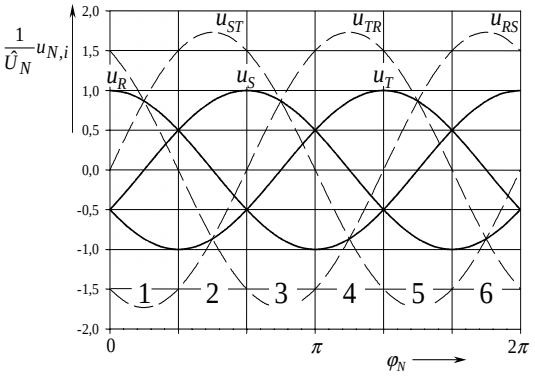

Fig. 2: Mains phase voltages and intervals being defined by different relations of the instantaneous mains phase voltage values. The interval $\varphi_N \approx \varphi_U \in (0; \frac{\pi}{3})$ considered for the analysis of the system behavior in this paper is pointed out by a dotted area.

For the denomination of the switching states of the power transistors S_i, $i = R, S, T$, and S switching functions s_i and s are used in the following, where $s_i, s = 0$ denotes the off-state, and $s_i, s = 1$ denotes the on-state. The characterization of the

s_R	s_S	s_T	$i_{U,R}$	$i_{U,S}$	$i_{U,T}$	$\underline{i}_{U,j}$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	$+I$	$-I$	$\frac{2}{\sqrt{3}}\jmath I$
1	0	0	0	0	0	0
1	0	1	$+I$	0	$-I$	$\frac{2}{\sqrt{3}} I e^{\jmath\frac{\pi}{6}}$
1	1	0	$+I$	$-I$	0	$\frac{2}{\sqrt{3}} I e^{-\jmath\frac{\pi}{6}}$
1	1	1	$+I$	0	$-I$	$\frac{2}{\sqrt{3}} I e^{\jmath\frac{\pi}{6}}$

Tab. 1: Switching states j, corresponding input phase currents $i_{U,i}$ and current space vectors $\underline{i}_{U,j}$ for $\varphi_U \in (0; \frac{\pi}{3})$.

switching state of the buck input stage is defined by the combination $j = (s_R s_S s_T)$ of the phase switching functions. The conduction states of the buck input stage are shown in **Fig. 3**, **Fig. 4** shows the related space vectors according to **Tab. 1**.

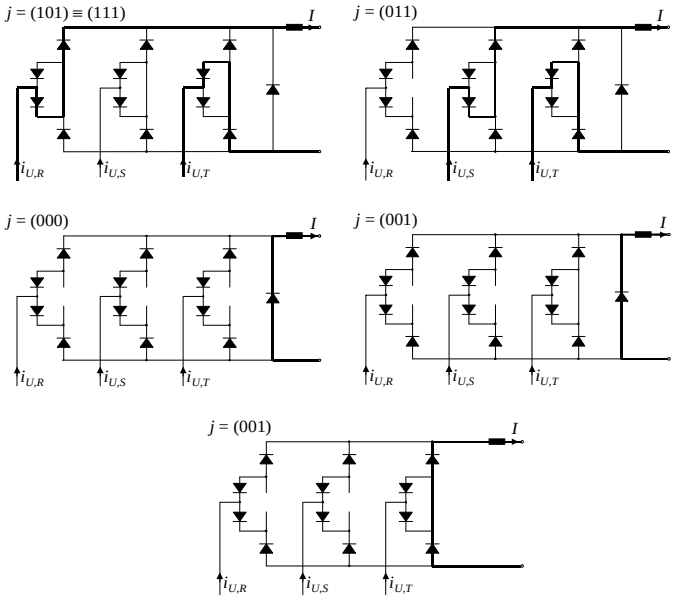

Fig. 3: Conduction states of the buck stage according to Tab. 1 (valid for $u_{N,R} > 0 > u_{N,S} > u_{N,T}$). The current flow is indicated by a bold line, and the power transistors are not explicitely shown for the sake of clearness.

For $s_i = 1$, $i = R, S, T$, the bridge leg i corresponds to a bridge leg of a conventional diode bridge (cf. **Fig. 5**), therefore, the current path for the different switching states can be identified easily. E.g., for $s_R = 0$, $s_S = 1$ and $s_T = 1$ there results a positive current $+I$ in phase S and a negative current $-I$ in phase T due to $u_{N,S} > u_{N,T}$, and according to Eq. (3) an input current space vector $\underline{i}_{U,(011)} = \frac{2}{\sqrt{3}}\jmath I$ is formed at the input. If all power transistors S_i, $i = R, S, T$, are in the on-state, $j = (111)$, the system corresponds to a three-phase diode bridge, due to $u_{N,R} > u_{N,S} > u_{N,T}$ there follows $i_{U,R} = +I$ and $i_{U,T} = -I$. In this case, the generated input current space vector $\underline{i}_{U,(111)} = \frac{2}{\sqrt{3}} I \exp\left(\jmath\frac{\pi}{6}\right)$ is equal to the space vector $\underline{i}_{U,(101)}$ (cf. Tab. 1). Since no difference in the input phase

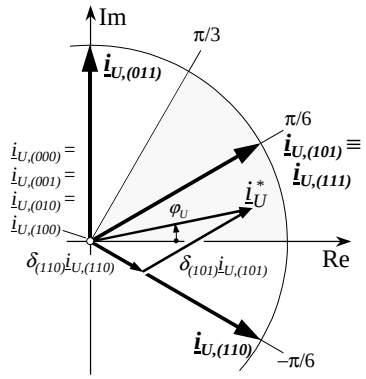

Fig. 4: Input current space vectors $\underline{i}_{U,j}$ according to Tab. 1 (valid for $u_{N,R} > 0 > u_{N,S} > u_{N,T}$ and/or for $\varphi_U \in (0; \frac{\pi}{3})$), and approximation of the reference value of the input current $\underline{i}_U^*$ via neighboring current space vectors.

current behavior is given, the switching state $j = (101)$ or $j = (111)$ can be used for achieving $i_{U,R} = +I$, $i_{U,S} = 0$ and $i_{U,T} = -I$. The complete set of space vectors associated with the switching states j of the rectifier system valid within the considered angle interval $\varphi_U \in (0; \frac{\pi}{3})$ is shown in Fig. 4.

Remark: If no free-wheeling diode D_F is provided, a free-wheeling path over one bridge leg has to be ensured (e.g., switching state $j = (100)$), hence the switching state $j = (000)$ must not be assumed. If an explicit free-wheeling diode D_F exists, the free-wheeling of the inductor current will always lead via this diode, also if the power transistors of a bridge leg is in the on-state (e.g., switching state $j = (100)$), because of the higher forward voltage drops of the power semiconductor devices in one bridge leg (cf. Fig. 3). For the sake of safety, and to guarantee a free-wheeling path also if a switching failure occurs a system structure with explicit free-wheeling diode D_F will be considered. A further advantage of the system structure with explicit free-wheeling diode is a decrease of the conducting losses of the diodes D_{i+} and D_{i-} (cf. section 2.4.1, **Fig. 7**(a) and (b)), as a disadvantage the higher realization effort has to be mentioned.

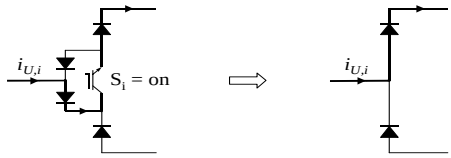

Fig. 5: The basic function of a bridge leg of the buck input stage with power-transistor S_i in on-state corresponds to a bridge leg of a conventional diode bridge. The current path for positive input current $i_{U,i} > 0$ is indicated by a bold line.

2.3 Control of the Input Current

For the formation of a given reference value $\underline{i}_U^*$ of the input current and/or of a related mains current $\underline{i}_N \approx \underline{i}_U^*$ only the space vectors lying in immediate neighborhood of $\underline{i}_U^*$ are incorporated into the switching state sequence in order to achieve a deviation as small as possible between reference and actual space vectors. In general, the switching sequence valid within

Seq.	j_1	j_2	j_3	j_4	j_5	j_6	$S_{cl.}$
1.1	(111)	(110)	(100)	(100)	(110)	(111)	S_R
1.2	(111)	(110)	(010)	(010)	(110)	(111)	S_S
1.3	(111)	(110)	(000)	(000)	(110)	(111)	–
2.1	(110)	(100)	(101)	(101)	(100)	(110)	S_R
2.2	(110)	(000)	(101)	(101)	(000)	(110)	–
3.1	(100)	(110)	(111)	(100)	(110)	(111)	S_R

Tab. 2: Switching state sequences available for two subsequent pulse half periods valid within $\varphi_U \in (0; \frac{\pi}{6})$, $S_{cl.}$ denotes the clamped power transistor.

one pulse (half) period has to be arranged in such a manner that a minimum number of switching transitions of the power transistors and/or minimum switching losses occur.

For $\varphi_U \in (0; \frac{\pi}{6})$ the space vectors $i_{U,(101)} \equiv i_{U,(111)}$, $i_{U,(110)}$ and $i_{U,(FW)}$ [1], and for $\varphi_U \in (\frac{\pi}{6}; \frac{\pi}{3})$ the space vectors $i_{U,(101)} \equiv i_{U,(111)}$, $i_{U,(011)}$ and $i_{U,(FW)}$ are employed.

There are several possibilities to arrange the switching states within one pulse (half) period. The switching states can either be arranged symmetrically (cf. **Tab. 2**, sequences 1.x and 2.x) or asymmetrically (cf. Tab. 2, sequence 3.1) to the middle of the pulse period. Besides that, the free-wheeling state can either be placed in the middle of a pulse half period (cf. sequences 2.x) or at the beginning and/or at the end of a pulse half period, respectively (cf. sequences 1.x). Furthermore, one has the possibility to clamp one power transistor within a $\frac{\pi}{3}$-wide interval (sequences 1.1, 1.2, 2.1, 3.1) or to use the switching state $j = (000)$ as free-wheeling state (sequence 1.3, 2.2). These switching state sequences presented here show no difference regarding to the number of switching transitions, but different switching losses as derived in the following.

2.3.1 Switching Losses

For the sake of simplicity we assume (i) the switching energy loss w to be proportional to the switched voltage $u(t)$ (the proportional relationship is represented by a constant of proportionality k), and (ii) a constant switched current I (as impressed by the inductor L). For the energy loss of one power transistor S_i occuring at a switching action from the on-state to the off-state one receives (cf. [11])

$$w_{\text{on-off},S_i} = k_{\text{on-off}}\, u_{\text{on-off}}(t)\, I, \tag{5}$$

and for the switching energy loss at a switching action from the off-state to the on-state

$$w_{\text{off-on},S_i} = k_{\text{off-on}}\, u_{\text{off-on}}(t)\, I. \tag{6}$$

The average value of the global switching energy loss (related to a mains period T_N) can then be calculated from the sum of the local switching energy losses (related to a pulse period T_P) of all power transistors S_i incorporated into the switching actions via

$$W = \frac{1}{T_N} \int_0^{T_N} \left(\sum_i w_{\text{on-off},S_i}(t) + \sum_i w_{\text{off-on},S_i}(t) \right) \mathrm{d}t; \tag{7}$$

[1] $j = (FW)$ denotes the free-wheeling state, $(FW) = (100), (010), (001), (000)$.

Seq.	P
1.x	$\frac{3\sqrt{3}}{\pi}\, f_P k\, I\, \hat{U}_N$
2.x	$\frac{9}{\pi}\, f_P k\, I\, \hat{U}_N$
3.1	$\frac{6\sqrt{3}}{\pi}\, f_P k\, I\, \hat{U}_N$

Tab. 3: Average value of the switching power losses for the switching states sequences given in Tab. 2.

due to the symmetry of the feeding AC mains and the rectifier system the integration can be constrained to an interval $\varphi_U \in (0; \frac{\pi}{6})$ (cf. Eq. (9)).

Investigating e.g. sequence 1.1 (cf. Tab. 2) we have: At the transition from the switching state $j = (111)$ to $j = (110)$ the power transistor S_T has to be switched off at a voltage $u_{C_F,ST}$. At the following transition $j = (110) \rightarrow j = (100)$ the power transistor S_S has to be switched off at a voltage $u_{C_F,RS}$. In the subsequent pulse half period the power transistors S_S, S_T have to be switched on again at the same voltages, but in reverse order. If $k_{\text{on-off}} + k_{\text{off-on}} = k$ is assumed for the sake of simplicity, the switching energy loss within a pulse period can then be calculated as

$$\begin{aligned} w_{\text{on-off}}(t) + w_{\text{off-on}}(t) &= k\, I\, (u_{C_F,ST}(t) + u_{C_F,RS}(t)) = \\ &= k\, I\, u_{C_F,RT}(t). \end{aligned} \tag{8}$$

Based on Eq. 8 one receives for the average value of the global switching power loss within one mains period

$$P = W\, f_P = \frac{1}{\frac{\pi}{6}} \int_0^{\frac{\pi}{6}} k\, f_P\, I\, u_{C_F,RT}(\varphi_U)\, \mathrm{d}\varphi_U \approx \frac{3\sqrt{3}}{\pi} k\, f_P\, I\, \hat{U}_N. \tag{9}$$

If the switching state $j = (000)$ is incorporated in the switching state sequence instead of $j = (100)$, there is no change in switching energy loss, because the additional switching operation of the power transistor S_R occurs with zero current.

The switching power losses for the other switching sequences shown in Tab. 2 can be calculated in an analogous way, the results are shown in **Tab. 3**, **Fig. 6** shows the behavior of the normalized switching energy losses within one mains period.

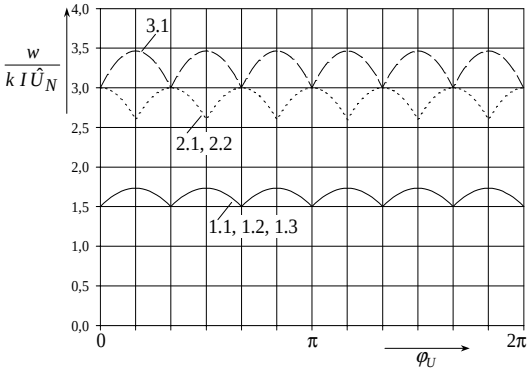

Fig. 6: Normalized switching energy losses for the switching state sequences given in Tab. 2.

With respect to Tab. 3 and/or Fig. 6 one can see immediately that the switching state sequences with the free-wheeling state lying at the beginning and/or at the end of one pulse half period, respectively, are advantageous over other switching sequences regarding the switching energy loss. If the power transistor of one bridge leg shall be clamped within a $\frac{\pi}{3}$-wide interval one can either choose the power transistor of the phase i, with the phase voltage $u_{N,i}$ having the maximum absolute value, i.e. phase $i = R$ for $\varphi_U \in (0; \frac{\pi}{6})$ in sequence 1.1 (cf. Fig 2), or the phase i with the phase voltage lying in between the others, i.e. phase S for $\varphi_U \in (0; \frac{\pi}{6})$ in sequence 1.2.

2.4 Current Stress on the Power Components

2.4.1 Power Semiconductors

In the following the current average and rms values are calculated as required for the calculations of the on-state losses of the semiconductor devices (cf. [11]). The analytical results are achieved by analyzing the current flow in one bridge leg within one pulse half period and the relative on-times of the current space vectors in dependency on the angle φ_U and the modulation index M of the buck input stage,

$$M = \frac{\hat{I}_N}{I}, \qquad M \in [0; 1]\,. \tag{10}$$

Due to the symmetry of the feeding AC mains and due to the identical structure of the bridge legs of the buck input stage the results are valid for all bridge legs, but one has to separately calculate the component stresses for the system structures with and without free-wheeling diode D_F. The resulting characteristic values of the power semiconductor currents are compiled in Fig. 7.

Diodes $D_{N,i+}$ and $D_{N,i-}$
The diodes $D_{N,i+}$ and $D_{N,i-}$ do not take part in the free-wheeling action in any way, for that reason the results with and without free-wheeling diode are the same,

$$I_{D_{N,i},\mathrm{avg}} = \frac{1}{\pi}\hat{I}_N, \qquad I_{D_{N,i},\mathrm{rms}} = \frac{1}{\sqrt{M\,\pi}}\hat{I}_N. \tag{11}$$

Diodes D_{i+} and D_{i-}
If an explicit free-wheeling diode D_F is provided, the current stress on the diodes D_i equals the current stress on the diodes $D_{N,i}$ (cf. Eq. (11)). If the bridge leg is part of the free-wheeling path, i.e., if no explicit free-wheeling diode is provided, one receives a higher current stress for the diodes D_i:

$$I_{D_i,\mathrm{avg}} = \frac{1}{3M}\hat{I}_N, \qquad I_{D_i,\mathrm{rms}} = \frac{1}{\sqrt{3}\,M}\hat{I}_N. \tag{12}$$

Power Transistors S_i
The power transistors are in on-state, if either the diodes $D_{N,i+}$ and D_{i+} or the diodes $D_{N,i-}$ and D_{i-} are conducting. Therefore, the current stress on the power transistors can be calculated easily by adding up the results for $D_{N,i}$ and D_i. With an explicit free-wheeling diode D_F there results

$$I_{T_i,\mathrm{avg}} = \frac{2}{\pi}\hat{I}_N, \qquad I_{T_i,\mathrm{rms}} = \frac{2}{\sqrt{M\,\pi}}\hat{I}_N, \tag{13}$$

without free-wheeling diode one receives

$$I_{T_i,\mathrm{avg}} = \left(\frac{1}{3\,M} + \frac{1}{\pi}\right)\hat{I}_N, \quad I_{T_i,\mathrm{rms}} = \sqrt{\frac{1}{3\,M^2} + \frac{1}{M\,\pi}}\,\hat{I}_N. \tag{14}$$

Free-Wheeling Diode D_F
The current stress on the free-wheeling diode corresponds to the difference of the current stresses on the diodes $D_{i,-}$ with (cf. Eq. (11)) and without free-wheeling diode (cf. Eq. (12)),

$$I_{D\,F,\mathrm{avg}} = \left(\frac{1}{M} - \frac{3}{\pi}\right)\hat{I}_N, \quad I_{D\,F,\mathrm{rms}} = \sqrt{\frac{1}{M^2} - \frac{3}{M\pi}}\,\hat{I}_N. \tag{15}$$

Boost Diode D and Boost Power Transistor S
For a constant output current I_0 (as assumed here), the current stresses on the boost semiconductor devices depend only on the modulation index δ of the boost converter,

$$I_{D,\mathrm{avg}} = I_0, \qquad I_{D,\mathrm{rms}} = I_0\frac{1}{\sqrt{1-\delta}},$$
$$I_{S,\mathrm{avg}} = I_0\frac{\delta}{1-\delta}, \qquad I_{S,\mathrm{rms}} = I_0\frac{\sqrt{\delta}}{1-\delta}, \tag{16}$$

with

$$\delta = 1 - \frac{U}{U_0}. \tag{17}$$

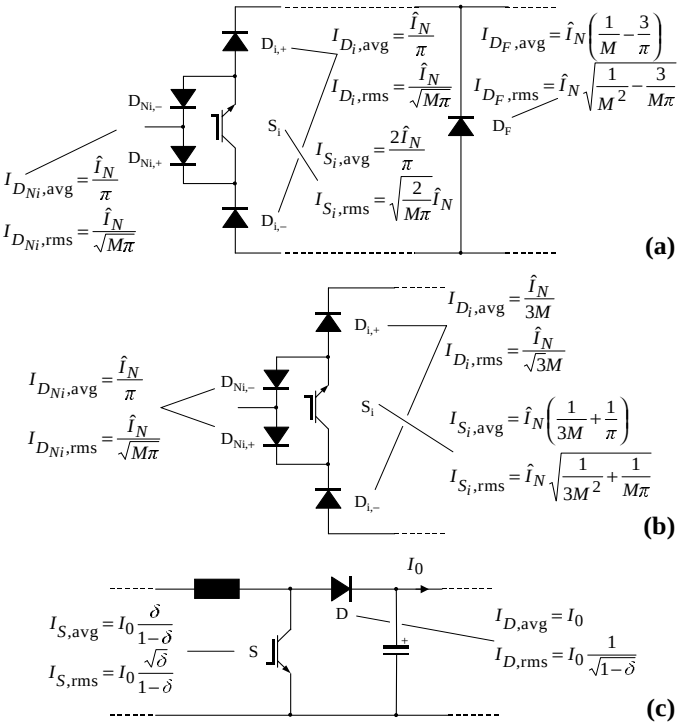

Fig. 7: Compilation of the results of the analytical calculation of average and rms values of the power semiconductor currents in dependency on the mains current amplitude $\hat{I}_N$ and on the modulation depths of the converters (M: buck input stage; δ: boost converter). Buck stage **(a)** with and **(b)** without free-wheeling diode D_F, **(c)** boost converter.

2.4.2 Output Capacitor

The maximum current stress on the capacitor C at the output of the boost converter occurs at minimum input voltage, i.e. at maximum modulation index δ of the boost converter. If the output current I_0 is assumed constant the rms-value of the capacitor current can be calculated using

$$I_{C,\mathrm{rms}} \approx I_0 \sqrt{\frac{\delta}{1-\delta}}. \tag{18}$$

2.4.3 Input Filter Capacitor

With regard to minimum capacitor voltage ripple it is advantageous to select a large capacitance value. But, an upper limit is given by the reactive power, which has to be limited to, e.g., $Q_{C_F} = (0,05 \ldots 0,1)\ P_N$ in order to achieve a displacement factor $\cos\varphi \approx 1$ of the mains current,

$$C_F < \frac{(0,05 \ldots 0,1)\ P_N}{3\,\omega_N\,U_N^2}. \tag{19}$$

Besides that, the cut-off frequency of the input filter ω_F has to lie sufficiently above the frequencies of low frequency distortions of the mains voltage to avoid an excitation of the input filter,

$$\omega_F = \frac{1}{\sqrt{(L_N + L_F)C_F}} > (5; 7; 11; \ldots)\,\omega_N, \tag{20}$$

where L_N denotes the inner mains inductance, and L_F denotes the inductance value of the filter inductor.

2.5 Buck+Boost Inductor

For obtaining a low value of the current ripple Δi of the inductor current I, one has to choose a sufficiently large inductance value of the buck+boost inductor L under consideration of the voltage appearing across the inductor. Advantageously, there the switching actions of the buck input stage and the boost converter are coordinated in such a manner that the voltage drop across the inductor and thereby also the current ripple is minimized.

The relevant operating point concerning the dimensioning of the buck+boost inductor is the upper limit of the input voltage range, i.e. minimum buck stage modulation index $M_{\min}$. The inductance value can be calculated (based on an equivalent DC/DC converter system, which is not discussed here for the sake of brevity) by

$$L = U_0 \frac{1 - \frac{\pi}{2\sqrt{3}}\,M_{\min}}{f_P} \frac{1}{\Delta i}. \tag{21}$$

2.6 Buck and Boost Operating Range

At low input voltage the boost converter is operating, and the modulation index of the buck input stage is defined to be $M_{\max} = 0.90$ in order to have a margin of 10 % available for control and active damping (cf. section 3). Therefore, considering that the average values of input and output power are identical,

$$\frac{3}{2}\hat{U}_N\hat{I}_N = U\,I, \tag{22}$$

and Eq. (10), at a mains phase voltage

$$U_{N,\mathrm{rms}} = \frac{\sqrt{2}}{3\,M_{\max}}U \tag{23}$$

the output voltage U of the buck input stage equals the output voltage U_0 of the boost converter. For further increasing input voltage level the boost converter is deactivated (i.e., $\delta = 0$), and the modulation index of the buck input stage is set according to Eqs. (10) and (22)

$$M = \frac{\sqrt{2}}{3}\frac{U}{U_{N,\mathrm{rms}}}. \tag{24}$$

Figure 8 gives an overview over the behavior of the system parameters according to Eqs. (10), (23) and (17) for the operating parameters given in section 2.7.

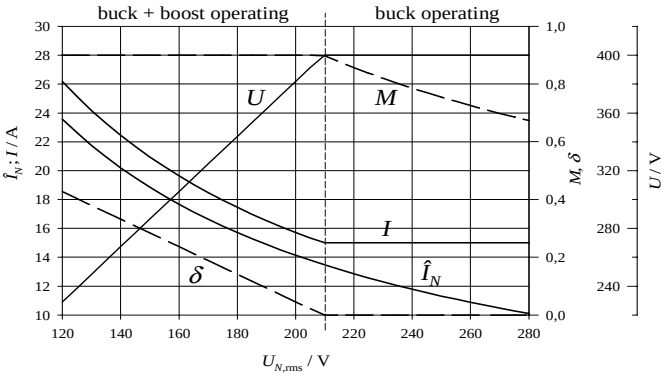

Fig. 8: Dependency of characterizing system parameters for system operating parameters specified in section 2.7 on the input voltage.

2.7 Dimensioning Example

With regard to a low mains phase currents ripple and a less complex and low-cost system manufacturing using standard semiconductor devices and small packages (e.g. TO220, TO247) it is advantageous to realize a rated output power of e.g. 10 kW by parallel connection of two systems rated for 5 kW (cf. section 5). A prototype of the proposed system for 5 kW having the following operating parameters is currently under construction at the Department of Electrical Drives and Machines of the Technical University Vienna:

$$\begin{aligned} P_N &= 5\,\mathrm{kW}\,(6\,\mathrm{kW}) \\ U_{N,\mathrm{rms}} &= 120\,\mathrm{V} \ldots 280\,\mathrm{V} \\ U_0 &= 400\,\mathrm{V} \\ f_N &= 50\,\mathrm{Hz} \\ f_P &= 30\,\mathrm{kHz}. \end{aligned}$$

In the following, the range of the current stresses on the power semiconductor devices (cf. Eqs. (11) – (16)), the required inductance value of the buck+boost inductor, and the dimensioning of the capacitors are given for the specified operating

$I_{\rm avg}, I_{\rm rms}$ / A	120 V	...	210 V	...	280 V
$I_{D_{(N),i},\rm avg}$	7.5	...	4.5	...	3.2
$I_{D_{(N),i},\rm rms}$	14.0	...	8.0	...	6.9
$I_{S_i,\rm avg}$	15.0	...	8.6	...	6.4
$I_{S_i,\rm rms}$	19.8	...	11.3	...	9.8
$I_{D_F,\rm avg}$	3.7	...	2.1	...	5.4
$I_{D_F,\rm rms}$	9.8	...	5.7	...	9.0
$I_{D,\rm avg}$	15.0	...	15.0	...	15.0
$I_{D,\rm rms}$	19.8	...	15.0	...	15.0
$I_{S,\rm avg}$	11.2	...	0	...	0
$I_{S,\rm rms}$	17.1	...	0	...	0

Tab. 4: Current stresses on the semiconductor devices for different input voltage levels. For input voltages higher than 210 V the boost converter is deactivated.

parameters. For obtaining an overload capability of 20 % the system is rated for $P = 6\,\mathrm{kW}$.

If a current ripple $\frac{\Delta i_{\max}}{I} = 20\%$, i.e. 3 A at $I = 15\,\mathrm{A}$, is not to be exceeded, one receives for the required inductance value with $M_{min} = 0.673$ (cf. Eqs. (21) and (24))

$$L \approx 1.7\,\mathrm{mH}. \tag{25}$$

The output capacitor C has to be selected according to the current stress reaching a maximum value at minimum input voltage, i.e. maximum modulation index of the boost converter $\delta = 0.43$, (cf. Eqs. (17) and (18))

$$I_{C,\rm rms} \approx 13.0\,\mathrm{A}. \tag{26}$$

With Eq. (19) one can give the following guideline for the dimensioning of the filter capacitor,

$$C_F < \frac{(0.05\ldots0.1)\cdot 6000\,\mathrm{W}}{3\cdot 2\pi\,50\,\mathrm{Hz}\cdot(280\,\mathrm{V})^2} = (4\ldots8)\,\mu\mathrm{F}, \tag{27}$$

with $L_N \approx L_F = 100\,\mu\mathrm{H}$ the resulting cut-off filter frequency (cf. Eq. (20)),

$$f_F = \frac{1}{2\pi}\,\frac{1}{\sqrt{200\,\mu\mathrm{H}\,(4\ldots8)\,\mu\mathrm{F}}} = (4\ldots5.6)\,\mathrm{kHz}, \tag{28}$$

lies significantly above the critical frequency range occupied by low frequency distortions of the mains voltage.

The current stresses on the semiconductor devices resulting for minimum and maximum input voltage are compiled in **Tab. 4**.

3 Multi-Loop System Control

The block diagram of the system control with output voltage controller as master control and current controller for the DC-side inductor current as slave control is shown in **Fig. 9**.
The reference value of the output capacitor charging current i_C^* is set by the output voltage controller $F(s)$ in dependency on the control error of the output voltage $u_0^* - u_0$ (i_0 considers a load current feedforward). Considering the balance of output power of the buck input stage and of the boost converter

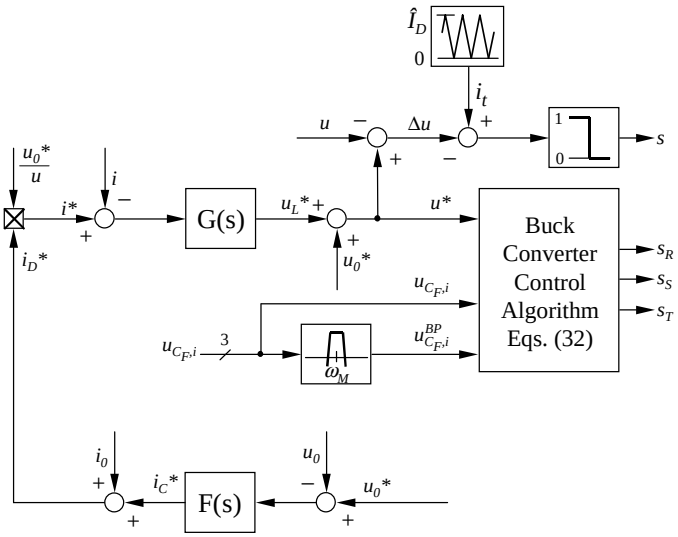

Fig. 9: Block diagram of the control structure.

$u\,i = i_D^*\,u_0^*$ the buck+boost inductor current has to be proportional to the local average value of the boost converter output current i_D (weighting factor $\frac{u_0^*}{u}$). The current controller $G(s)$ sets the reference value of the voltage u_L^* across the buck+boost inductor, by adding the output voltage reference value u_0^* one receives the reference value for the output voltage u^* of the buck input stage. If this reference value u^* lies below the maximum output voltage u of the buck stage (i.e., $\Delta u > 0$), the boost converter has to be activated: The voltage u_L^* appearing across the buck+boost inductor is set according to the current i^* required for a given output power. If the difference $u - u_0$ between the output voltage of the buck stage and the system output voltage is not sufficiently large to achieve the voltage u_L required for impressing i^*, the potential at the boost side of the inductor has to be reduced by switching the boost power transistor S with proper δ, whereby the voltage appearing across the buck+boost inductor increases to u_L^*. To guarantee a synchronized operation of buck and boost converter, a triangular carrier wave having pulse frequency f_P is provided. There the activation of the boost converter can be achieved automatically by comparing Δu to i_t in case a triangular carrier having an offset of $\frac{1}{2}\hat{I}_D$ is employed.

Based on the following requirements

- resistive fundamental mains behavior, cf. Eq. (29),
- average value of the line-to-line input voltages switched to the output of the buck stage being equal to the reference value u^*, cf. Eq. (30) (valid for $\varphi_U \in (0; \frac{\pi}{6})$), and
- sum of the relative on-times of the switching states within one pulse period has to equal to 1, cf. Eq. (31) (valid for $\varphi_U \in (0; \frac{\pi}{6})$), i.e.

$$\underline{i}_{U,(1)} \propto \underline{u}_{C_F} \tag{29}$$

$$\delta_{(101)}\,u_{C_F,RT} + \delta_{(110)}\,u_{C_F,RS} = U \tag{30}$$

$$\delta_{(101)} + \delta_{(110)} + \delta_{(FW)} = 1 \tag{31}$$

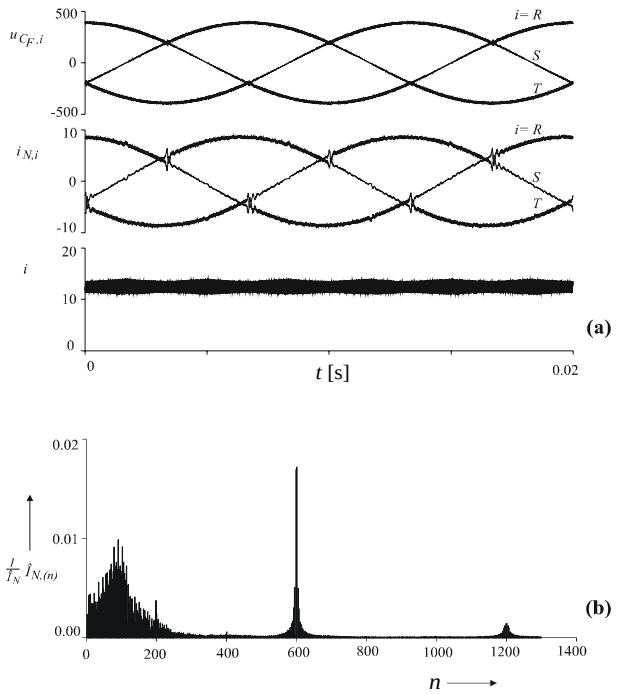

Fig. 10: Digital simulation of the time behavior of the input filter capacitor voltages $u_{C_F,i}$, $i = R, S, T$, of the mains phase currents $i_{N,i}$, and of the output current i of the buck stage. The normalized spectrum of the mains current is shown in **(b)**, fundamental component $\hat{I}_N$ suppressed (n denotes the ordinal number of the harmonics with reference to the mains frequency $f_N = 50\,\mathrm{Hz}$).

and incorporating the reference value u^* of the output voltage of the buck input stage, and the instantaneous values of the input filter capacitor voltage fundamentals $u_{C_F,(1),i}$, $i = R, S, T$, the switching functions are generated according to Eqs. (32) (given for an angle interval $\varphi_U \in (0; \frac{\pi}{6})$, where the actual angle interval is determined considering the relation of the instantaneous input capacitor voltage values $u_{C_F,i}$).

$$\begin{aligned}
\delta_{(101)} &= \frac{1}{3}\frac{u^*}{|\underline{u}_{C_F}|^2}\left(u^{BP}_{C_F,R} + u^{BP}_{C_F,S} - u^{BP}_{C_F,T}\right) + \Delta\delta_{(101)} \\
\delta_{(110)} &= \frac{1}{3}\frac{u^*}{|\underline{u}_{C_F}|^2}\left(u^{BP}_{C_F,R} - u^{BP}_{C_F,S} + u^{BP}_{C_F,T}\right) + \Delta\delta_{(110)} \\
\delta_{(FW)} &= 1 - \frac{2}{3}\frac{u^*}{|\underline{u}_{C_F}|^2}u^{BP}_{C_F,R} + \Delta\delta_{(FW)}, \qquad (32)
\end{aligned}$$

$u^{BP}_{C_F,i}$ denote the bandpass filtered input capacitor voltages $u_{C_F,i}$. The band-pass filter is employed for deriving the fundamentals $u_{C_F,(1),i} \approx u^{BP}_{C_F,i}$ of the voltages $u_{C_F,i}$ without phase displacement (filter mid-band frequency $\omega_M = 2\pi\,50\,\mathrm{Hz}$); $\Delta\delta_j$ is a correction value according to the active damping,

$$\Delta\delta_j = \frac{u^{HP}_{C_F,i}}{I}\,g_D, \qquad (33)$$

where g_D represents the damping conductance. The input filter capacitor voltages $u_{C_F,i}$ are high-pass filtered, $u^{HP}_{C_F,i}$ for calculating $\Delta\delta_j$ in order to restrict the damping to frequencies in the vicinity of the input filter resonance frequency (cut-off frequency $\omega_{HP} \approx \omega_F$).

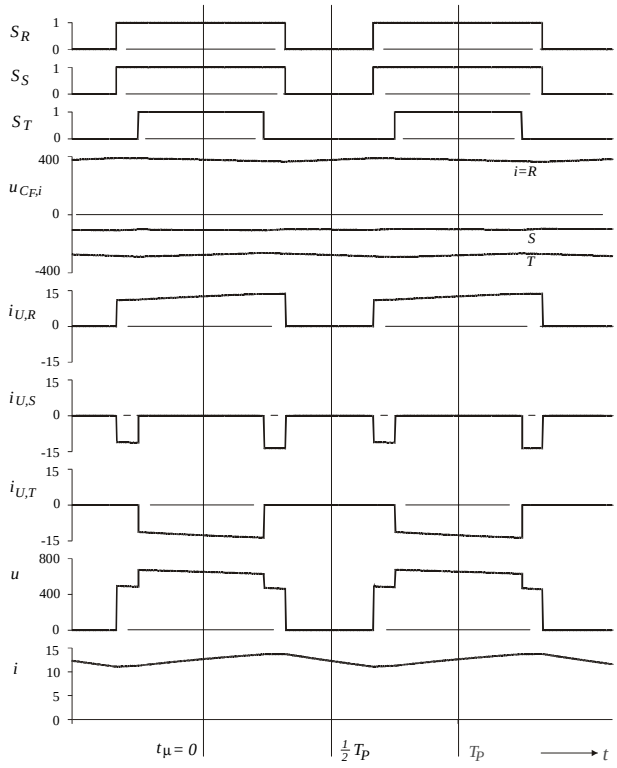

Fig. 11: Digital simulation of the local time behavior of the control signals s_i, of the input filter capacitor voltages $u_{C_F,i}$, of the input currents $i_{U,i}$, of the buck stage output voltage u and of the inductor current i, valid for $\varphi_U \in (0; \frac{\pi}{6})$. t_μ denotes the local time being counted within a pulse period T_P.

4 Digital Simulation

By the results of a digital simulation (shown in **Figs. 10** and **11**) the applicability of the proposed control concept is demonstrated clearly. The operating parameters are set according to section 2.7, for the input voltage $U_{N,\mathrm{rms}} = 280\,\mathrm{V}$ is assumed.

5 Parallel Connection of Two Systems

By providing phase-shifted operation of two systems connected in parallel, the following advantages over a single system of higher power are achieved:

- input currents show a more continuous shape,
- cancellation of current harmonics having pulse frequency, i.e first current harmonic occuring at double pulse frequency $2f_P$, and therefore
- cut-off frequency of the input filter can be shifted to higher frequencies, and/or reduction of the input filter size and increasing dynamics of the output voltage control.

However, a symmetrical distribution of the current to the parallel systems has to be ensured. In the following, the current space vectors available at a parallel operation of two systems and the possibility for an actively symmetrization of the individual currents are briefly investigated.

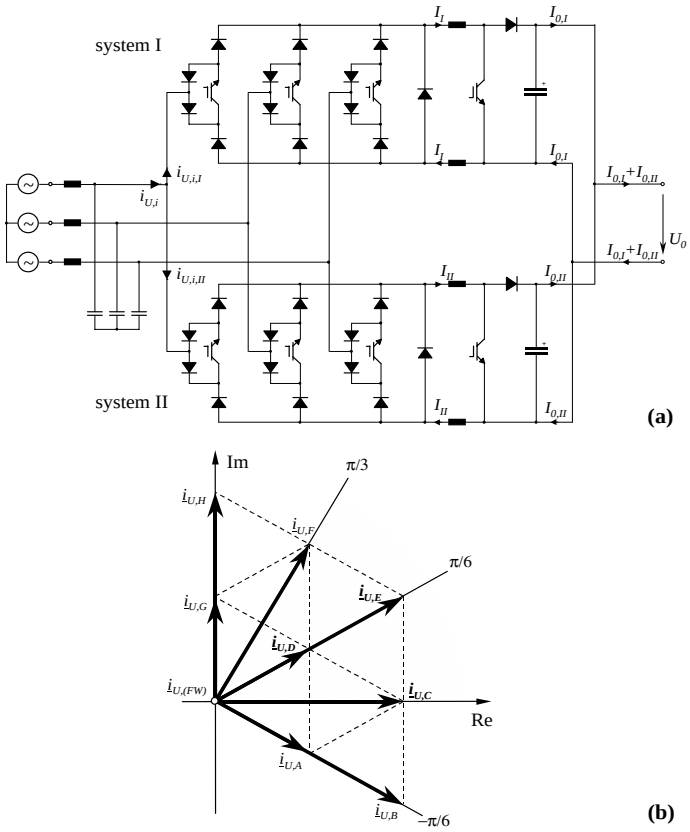

Fig. 12: Parallel connection of two single systems **(a)**, and input current space vectors available for current formation in an angle interval $\varphi_U \in (0; \frac{\pi}{3})$ (cf. **(b)**).

5.1 System Structure and Current Space Vectors

The current space vector formed at the input side of the parallel connection of two single systems I and II (cf. **Fig. 12**(a)) can be obtained easily by the sum of the current space vectors generated by the individual systems. The space vectors available within an angle interval $\varphi_U \in (0; \frac{\pi}{3})$ are compiled in **Tab. 5**, space vectors showing a redundancy of switching states concerning current formation (i.e. by different single-system input currents $i_{U,i,I}$ and $i_{U,i,II}$ the same total current space vector $\underline{i}_U$ is formed at the input side) are marked with an asterisk (*).

5.2 Current Symmetrization

In order to achieve a symmetric distribution of the current to the individual systems the redundant current space vectors (cf. Tab. 5) are applied in the switching state sequence. There are two possibilities to obtain this symmetrization: (i) one system is in active state (a current space vector $\underline{i}_U \neq 0$ is formed at the input of the system) and the other system in free-wheeling state, e.g.,

$$\begin{aligned} j_I = (101) \qquad & \underline{i}_{(101),I} = \frac{2}{\sqrt{3}}\, I_I \, \exp\left(\jmath\frac{\pi}{6}\right) \\ j_{II} = (100) \qquad & \underline{i}_{(100),II} = 0, \end{aligned} \tag{34}$$

*	$\underline{i}_{U,A} = \frac{2}{\sqrt{3}} I \exp\left(-\jmath\frac{\pi}{6}\right)$		$\underline{i}_{U,E} = \frac{4}{\sqrt{3}} I \exp\left(\jmath\frac{\pi}{6}\right)$
	$\underline{i}_{U,B} = \frac{4}{\sqrt{3}} I \exp\left(-\jmath\frac{\pi}{6}\right)$	*	$\underline{i}_{U,F} = 2\, I \exp\left(\jmath\frac{\pi}{3}\right)$
*	$\underline{i}_{U,C} = 2\, I$	*	$\underline{i}_{U,G} = \frac{2}{\sqrt{3}} I \exp\left(\jmath\frac{\pi}{2}\right)$
*	$\underline{i}_{U,D} = \frac{2}{\sqrt{3}} I \exp\left(\jmath\frac{\pi}{6}\right)$		$\underline{i}_{U,H} = \frac{4}{\sqrt{3}} I \exp\left(\jmath\frac{\pi}{2}\right)$

Tab. 5: Current space vectors for parallel operation of two systems valid in the angle interval $\varphi_U \in (0; \frac{\pi}{3})$.

(cf. Tab. 1) or (ii) both systems are in active state, e.g.,

$$\begin{aligned} j_I = (110) \qquad & \underline{i}_{(110),I} = \frac{2}{\sqrt{3}}\, I_I \, \exp\left(-\jmath\frac{\pi}{6}\right) \\ j_{II} = (011) \qquad & \underline{i}_{(011),II} = \frac{2}{\sqrt{3}}\, \jmath\, I_{II}. \end{aligned} \tag{35}$$

If $I_I = I_{II} = I$ (as assumed for current symmetrization) in both cases the total current space vector (cf. Fig. 12(b))

$$\underline{i}_{U,j_I,j_{II}} = \underline{i}_{U,j_I} + \underline{i}_{U,j_{II}} = \frac{2}{\sqrt{3}}\, I \, \exp\left(\jmath\frac{\pi}{6}\right) = \underline{i}_{U,D} \tag{36}$$

is formed at the input side of the parallel systems.

A closer theoretical investigation and experimental analysis of the systems behavior for parallel operation will be given in a future paper.

6 Conclusions

In this paper a novel wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage (cf. Fig. 1(b)) has been proposed showing the following

Advantages:

+ simple structure of the power and the control circuit especially in comparison to the conventional topology of a three-phase buck+boost converter shown in Fig. 1(a),
+ sinusoidal mains phase currents lying in phase with the mains phase voltage,
+ the input current of the rectifier system can be controlled advantageously providing a switching states sequence causing minimum switching losses,
+ the output voltage level of 400V allows the connection to DC/DC converters known from single-phase power factor correction and available in the market, furthermore
+ due to the boost converter a sinusoidal mains phase current shape can be guaranteed also in case of a failure of one phase of the mains,
+ an auxiliary start-up circuit can be omitted,
+ high efficiency up to 97 %, and
+ high power density ($\approx 1\,\mathrm{kW/dm^3}$, and $\approx 1.25\,\mathrm{kW/kg}$),
+ by parallel connection of two or more systems the input current ripple can be decreased and the input filter as well as the buck+boost inductor can be downsized.

Disadvantage in comparison to the conventional structure (cf. Fig. 1(a)):

- lower redundancy in case of a failure of one phase of the mains; for the system shown in Fig. 1(a); in case of a loss of one phase the full rated output power is available (cf. Fig. 5 in [6]), whereas in case of a failure of one phase at the proposed system the power has to be reduced by a factor $\sqrt{3}$.

Future research of the Power Electronics Group of the Technical University Vienna will be aiming for

- an evaluation of the proposed system by comparison with a wide input voltage range three-phase boost-type (VIENNA) rectifier [12] having an output voltage of 800 V (for converting this voltage to 48 V two 400 V DC/DC converters of half rated power have to be connected in series, for the proposed system two DC/DC converters of half rated power have to be connected in parallel, therefore, the comparison of the systems can be limited to the rectifier input stage),
- the experimental investigation of a 5 kW-prototype; according to the current state of development the laboratory system shows overall dimensions of $(34 \times 16 \times 10)\,\mathrm{cm} \doteq (13.4 \times 6.3 \times 3.9)\,\mathrm{in}$, an efficiency of $\eta \approx 95\%$ at $U_{N,\min} = 120\,\mathrm{V}$ and of $\eta \approx 97\,\%$ at $U_{N,\max} = 280\,\mathrm{V}$; the control is realized in purely analog fashion,
- optimizing the power density according to experimental tests (minimizing the inductance of the DC/DC inductor which currently has a significant share of the total volume of the passive power components), and
- the parallel connection of two systems controlled by a digital signal processor.

The results of this research efforts will be presented at a future conference.

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