ETH zürich

Advanced 3-Φ SiC/GaN PWM Inverter Concepts for Future VSD Applications

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Outline

- *Introduction*
- *SiC/GaN Application Challenges*
- *VSI with Output Filters*
- *Double-Bridge VSI Topologies*

Coffee Break 4:00 – 4:30 p.m.

- *Buck+Boost VSI & CSI Topologies/Control*
- *Multi-Level & Quasi-Three-Level VSI*
- *Ultra-Compact & Motor Integr. VSI*

- *Conclusions*

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3-Φ Variable Speed Drive Inverter Systems

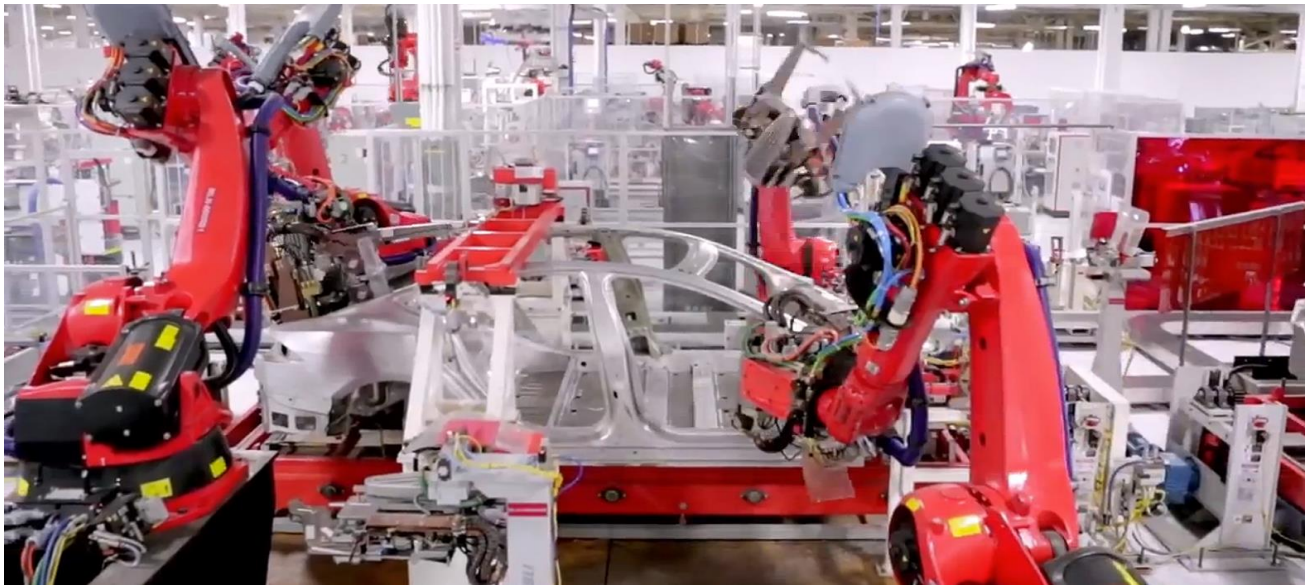
State-of-the-Art
Future Requirements

▶ *Variable Speed Drive (VSD) Systems*

- Industry Automation / Robotics
- Material Machining / Processing – Drilling, Milling, etc.
- Pumps / Fans / Compressors
- Transportation
- etc., etc.

.... Everywhere !

Source: TESLA MOTORS

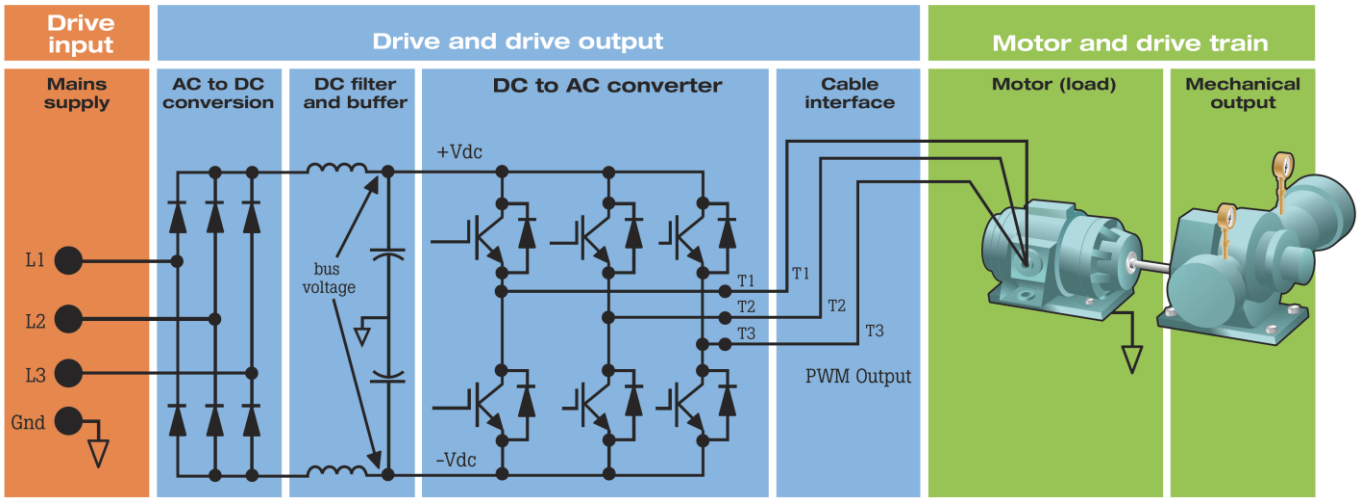


- *60% of El. Energy Used in Industry Consumed by VSDs*

▶ VSD State-of-the-Art

- *Mains Interface / 3-Φ PWM Inverter / Cable / Motor — All Separated*
  - → *Large Installation Space / $$$*
  - → *Complicated / Expert Installation / $$$*
- *Conducted EMI / Radiated EMI / Bearing Currents / Reflections on Long Motor Cables*
  - → *Shielded Motor Cables / $$$*
  - → *Inverter Output Filters (Add. Vol.) / $$$*

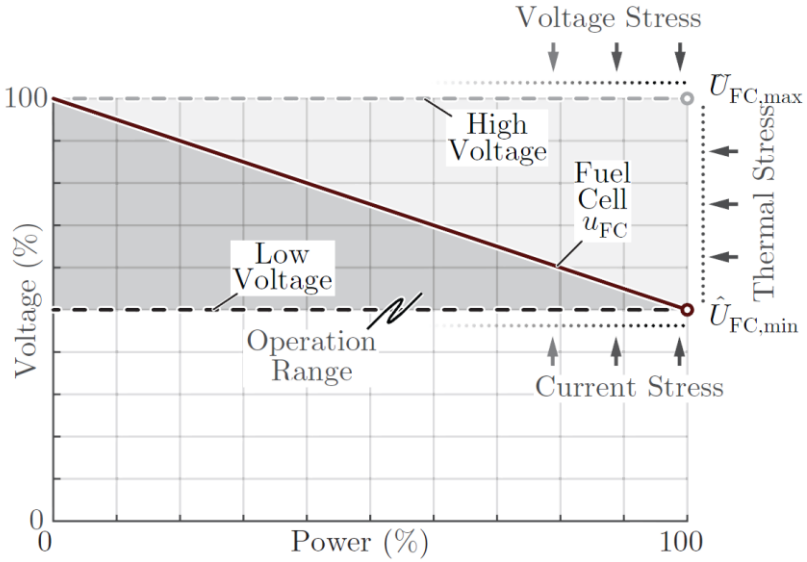
Source: FLUKE



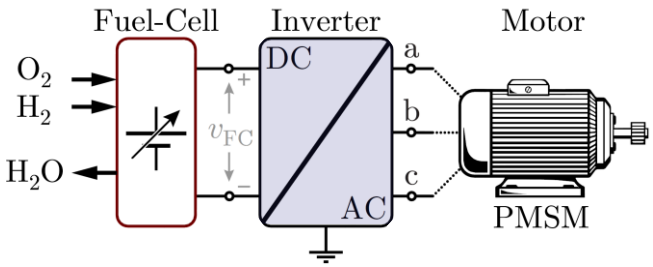
- *High Performance @ High Level of Complexity / High Costs (!)*

Future Requirements (1)

- *"Non-Expert" Install. / Low-Cost Motors* → *"Sinus-Inverter" OR Integrated Inv.*
- *Wide Applicability / Wide Voltage & Speed Range* → *Matching of Supply & Motor Voltage*
- *High Availability*



Source: magazine.fev.com

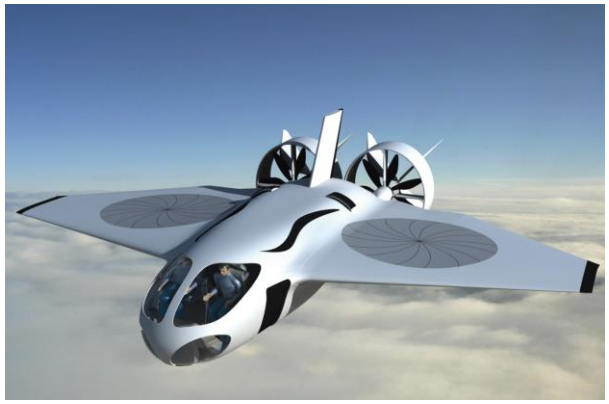


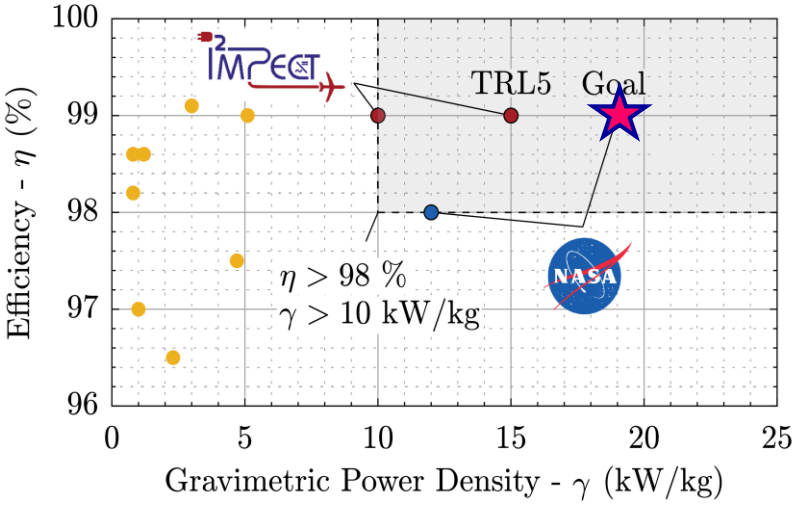
- *Single-Stage Energy Conversion* → *No Add. Converter for Voltage Adaption*

Future Requirements (2)

- Red. Inverter Volume / Weight → Matching of Low Volume of High-Speed Motors
- Lower Cooling Requirement → Low Inverter Losses & Low HF Motor Losses
- High-Speed Machines → High Output Frequencies

Source: Georgia Tech





→ Main "Enablers" — SiC/GaN Power Semiconductors & Adv. Inverter Topologies

Enabling Technologies & Challenges

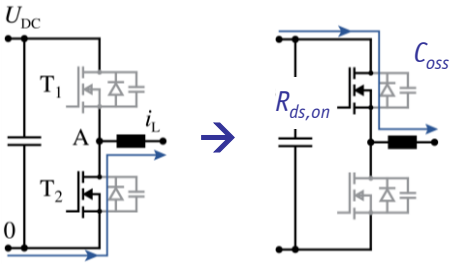
WBG Semiconductors
Advanced Inverter Topologies

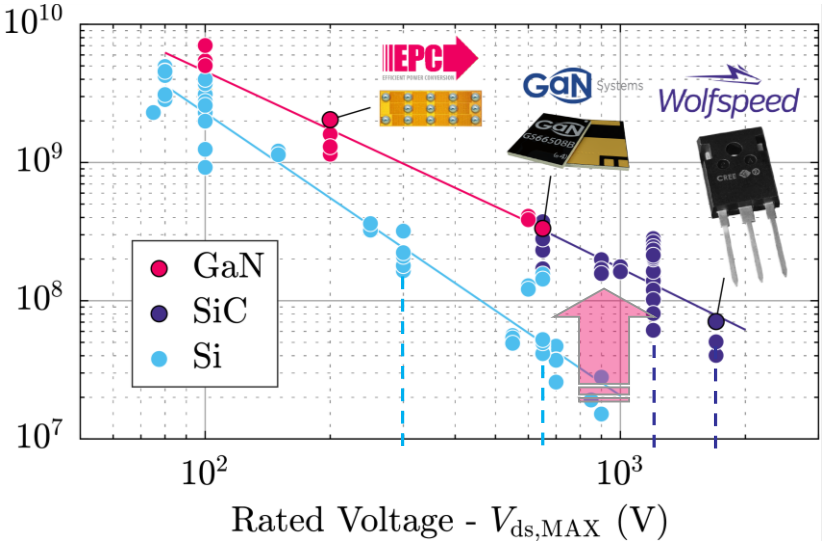
Source:
www.terencemauri.com

▶ SiC/GaN

- *Very Low On-State Resistance* → *Low (Partial Load) Conduction Losses*
- *Very Low Switching Losses* → *High Switching Frequencies*
- *Small Chip Area* → *Compact Realization*

$$\text{FOM} = \frac{1}{R_{\text{ds,on}} Q_{\text{oss}}}$$



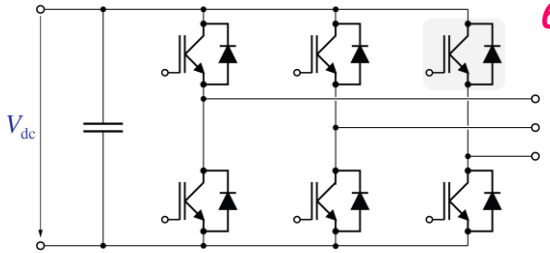


→ *Challenges in Packaging / Thermal Management / Gate Drive / PCB Layout*
→ *Extremely High Sw. Speed (dv/dt)* → *Motor Insul. Stress / Reflections / Bearing Curr. / EMI*

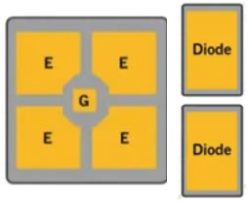
Si vs. SiC

- *Si-IGBT / Diode* → *Turn-Off Tail Current & Diode Reverse Recovery Current*
- *SiC-MOSFET* → *Massive Loss Reduction @ Part Load BUT Higher R_{th}*

6x Si-IGBT
6x Si-Diode



9.5mm x 10.4mm
2x 3.4mm x 5.8mm
(100%)

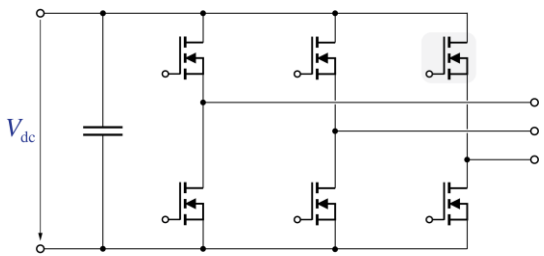


Source: ATZ elektronik

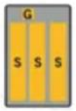
1200V 100A
Die Size: 98.8mm² + 39.4mm²

Source: Infineon

6x SiC-MOSFET



4.0mm x 6.4mm
(37%)



1200V 100A
Die Size: 25.6mm²

Source: Cree

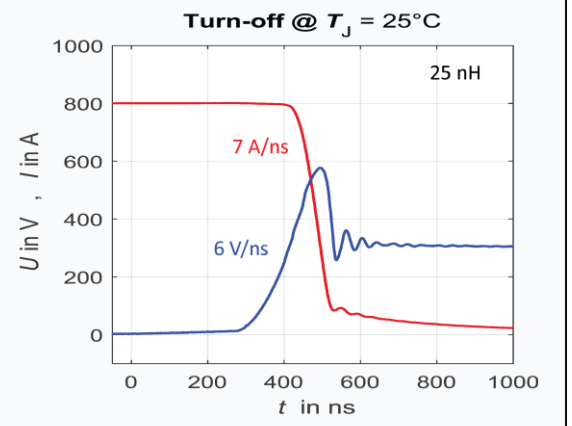
→ *Space Saving of >30% on Module Level (!)*

Si vs. SiC

- *Si-IGBT → dv/dt = 2...6 kV/us (Inverter for Var. Speed Drives / IEC 61800-3)*
- *SiC-MOSFETs → dv/dt = 20...60 kV/us*

Source: M. Bakran / ECPE 2019

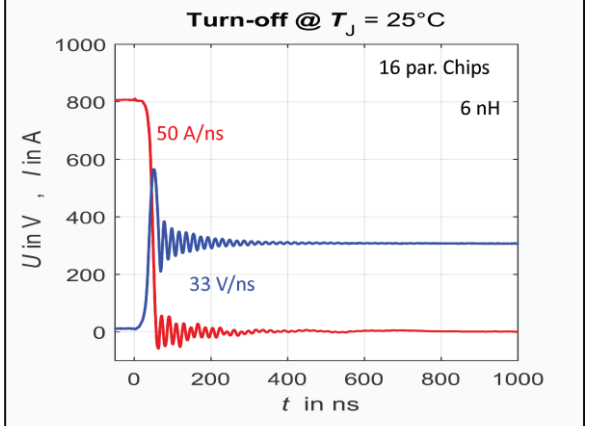
Si-IGBT / Hybrid-Pack 2



E_{off} = 45900 µJ

-> 8 kV/µs at 400V

SiC-MOSFET / (scaled for low inductance)



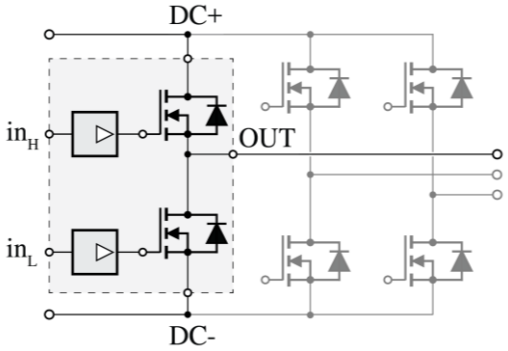
E_{off} = 4672 µJ

-> 44 kV/µs at 400 V

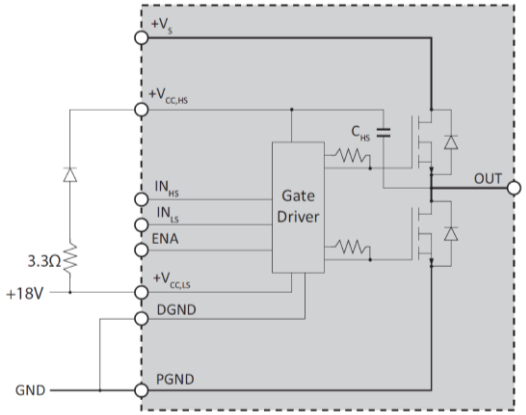
→ *Extremely High dv/dt → Motor Insul. Stress / Reflections / Bearing Curr. / EMI*

▶ SiC System in Package

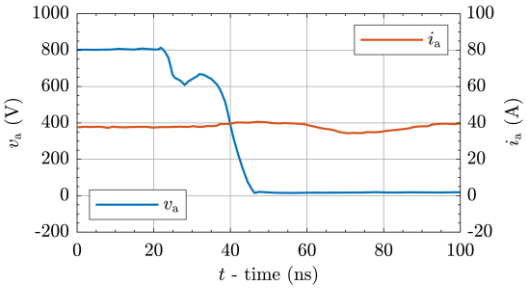
- *Integrated SiC Switching Cell — Bridge Leg + Intellig. Gate Drivers (Bootstrap HS Supply)*
- *1200V / 35mΩ, 31mm x 29.5mm*



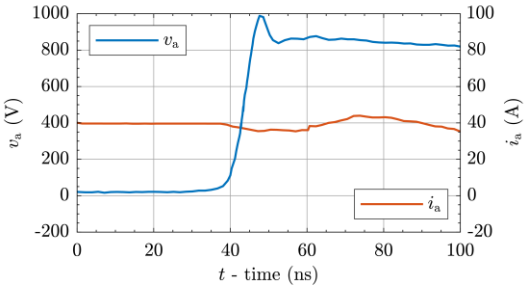
Source: A. Bhalla / PSD 2019



Turn On: 85V/ns

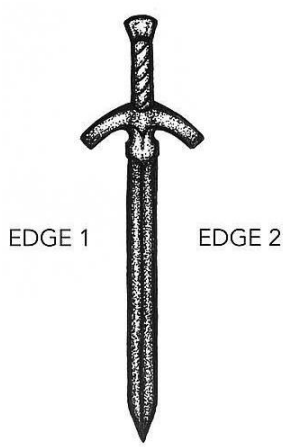


Turn Off: 140V/ns



→ *Extremely High dv/dt* → *Motor Insul. Stress / Reflections / Bearing Curr. / EMI*

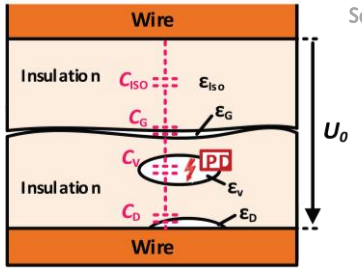
GaN/SiC VSD Application Challenges



Idea: F.C. Lee

▶ PD Motor Insulation Destruction (1)

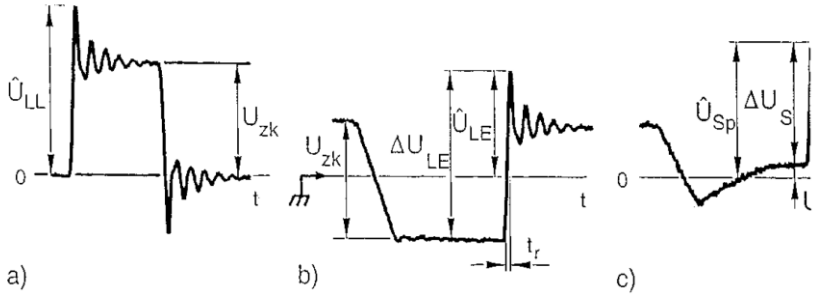
- *High dv/dt* → *Uneven Wdg. Voltage Distribution / Reflections — High Voltage Peaks*
- *Voltage Peaks* → *Local Insul. Breakdown e.g. in Air-Filled Voids = Partial Discharge (PD)*
- *PD* → *Grad. Destroys Insul. (Impinging Electrons, Ozone Chem. Attack)*



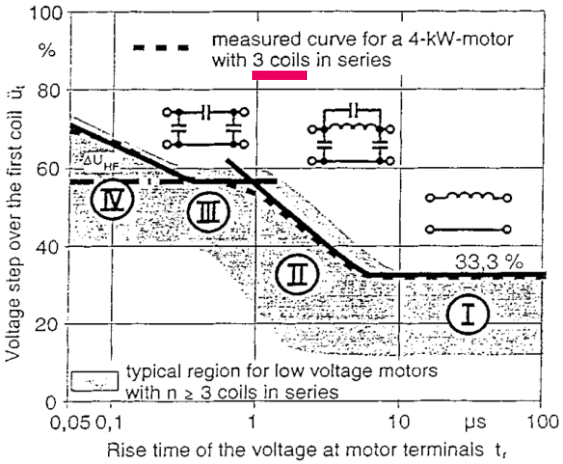
Source: Bakran / ECPE 2019

Inverter Motor Voltages

(a) Line-to-Line
(b) Line-to-Earth
(c) Across First Coil



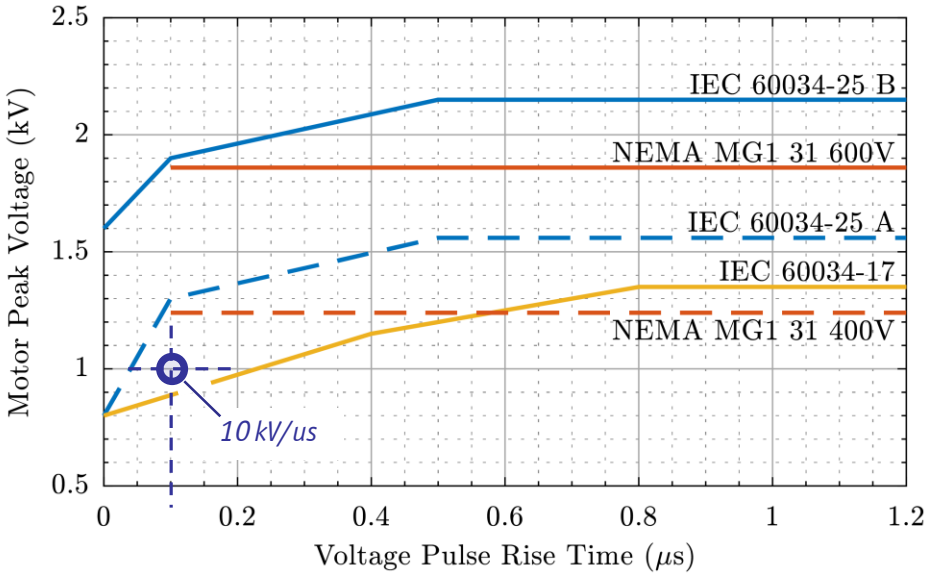
Source: Kaufhold et al. 2000



- *Preventing PD* → *Ampl. of Voltage Peaks < PD Inception Voltage (PDIV)*
- *PDIV Parameters* → *Temp. / Humidity / Pressure / Insul. Thick. / Type / Wire Diameter etc.*

PD Motor Insulation Destruction (2)

- *dv/dt-Limits Specified by Standards*
- *National Electrical Manufact. Association (NEMA, Motors Manufact. in USA)*
- *Intern. Electrotechn. Commission (IEC)*



NEMA MG1 Part 31 - 400V & 600V

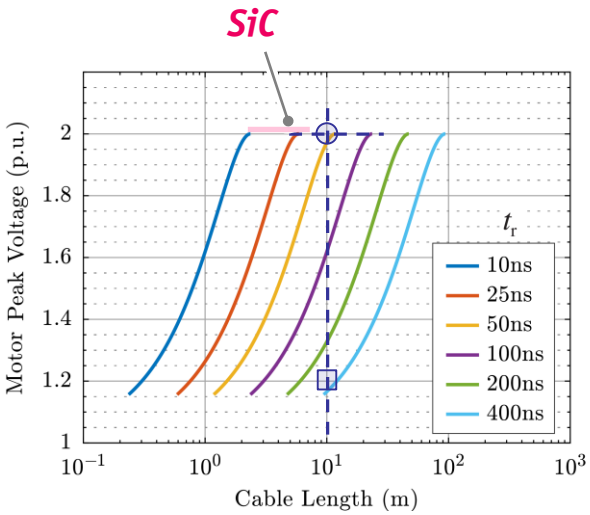
IEC 60034-17 - Cage Induction Motors
IEC 60034-25 - 500V (A) & 690V (B)
IEC 60034-27 - PD Measurements

...

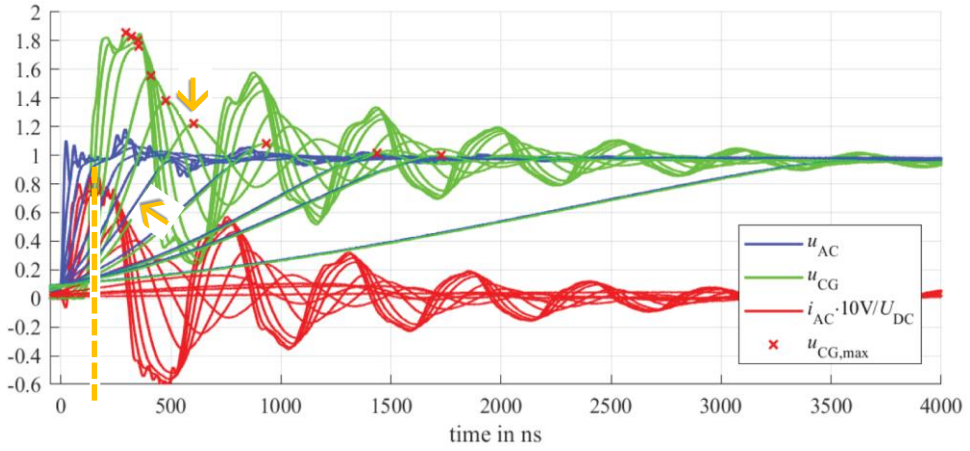
- *Ensuring the Limits → dv/dt-Filtering OR Full-Sinewave Filtering*
- *Relevance of dv/dt-Limits, e.g. for Single-Tooth Windings Under Discussion*

Surge Voltage Reflections

- *Short Rise Time of Inverter Output Voltage*
- *Impedance Mismatch of Cable & Motor → Reflect. @ Motor Terminals / High Insul. Stress*
- *Long Motor Cable $l_c \geq \frac{1}{2}\, t_r\, v$*



Source: Bakran / ECPE 2019

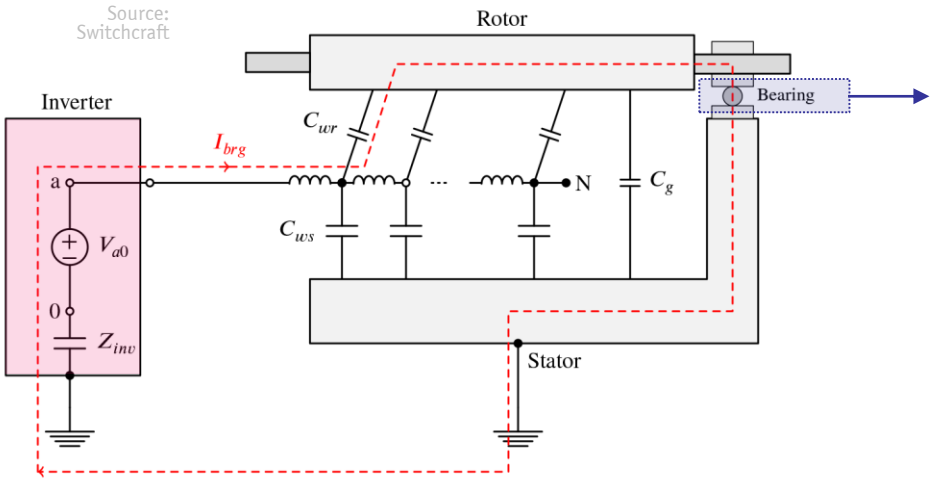


→ *dv/dt-Filtering OR Sinewave Filtering / Termination & Matching Networks etc.*

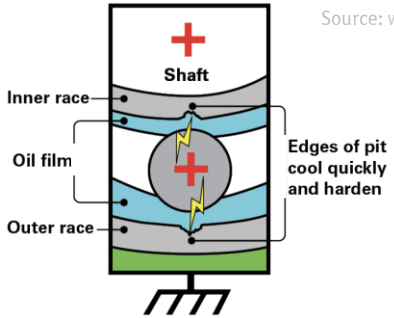
Motor Bearing Currents

- Switching Frequency CM Inverter Output Voltage → Motor Shaft Voltage
- Electrical Discharge in the Bearing ("EDM")

Source: Switchcraft



Source: www.est-aegis.com



Source: BOSCH

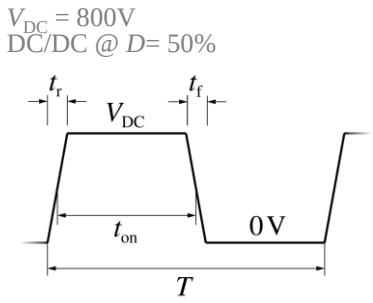
→ Cond. Grease / Ceram. Bearings / Shaft Grndg Brushes / dv/dt- OR Full-Sinewave Filters

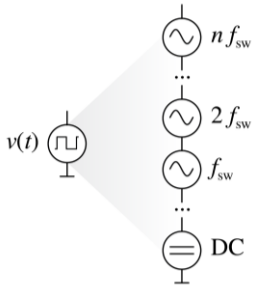
▶ SiC vs. Si Inverter EMI Spectrum

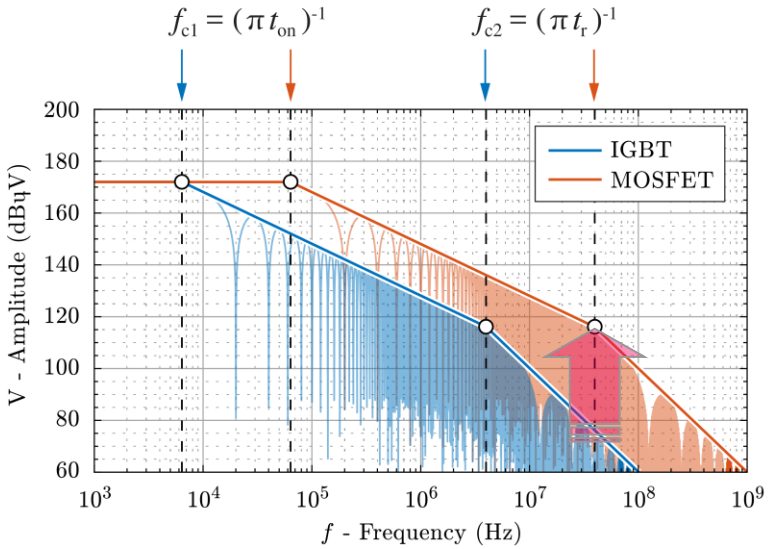
- SiC Enables Higher dv/dt → Factor 10
- SiC Enables Higher Switching Frequencies → Factor 10
- EMI Envelope Shifted to Higher Frequencies

Source/Idea: M. Schutten / GE

f_S= 10kHz & 5 kV/us for (Si IGBT)
f_S= 100kHz & 50 kV/us for (SiC MOSFET)





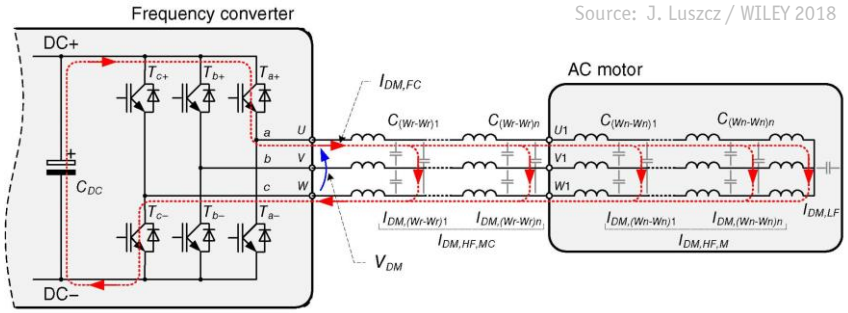


→ Higher Influence of Filter Component Parasitics and Couplings
→ dv/dt-Filtering OR Full Sinewave Filtering, Shielded Motor Cables

▶ DM & CM Conducted / Radiated EMI

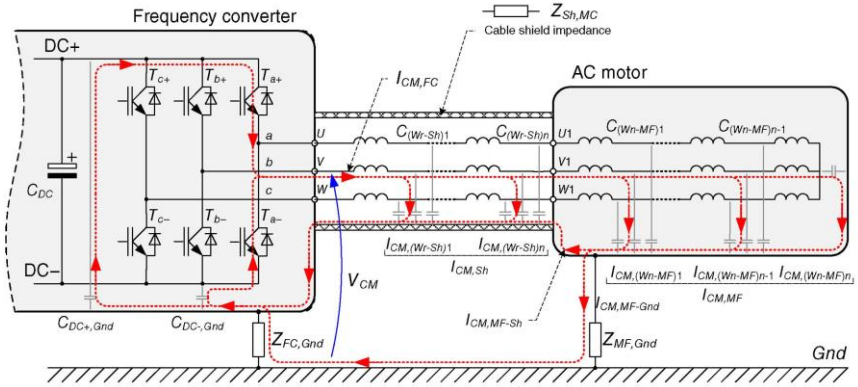
- *DM Conducted EMI Pathway*

Source: J. Luszcz / WILEY 2018



- *CM Conducted EMI Pathway (Motor Side)*

Source: J. Luszcz / WILEY 2018



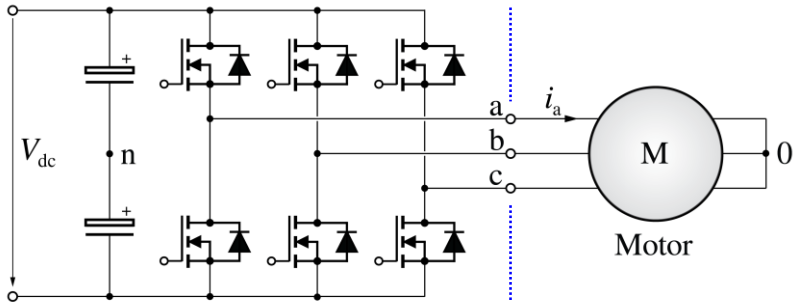
- *EMI Standards (Cond. & Rad.) → Shielded Motor Cables OR Full-Sinewave Filtering*

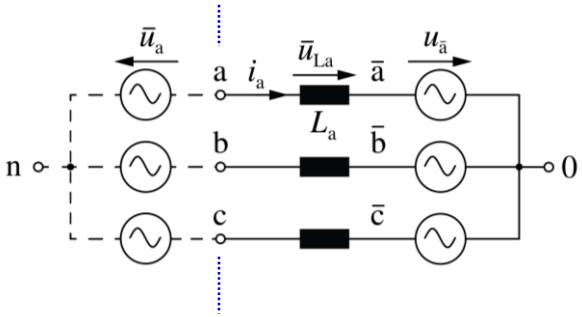
3-Φ Pulse-Width Modulated Inverter Basics

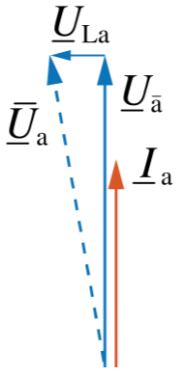
Motor Current Control
DM/CM Equivalent Circuit
CM/DM Filtering

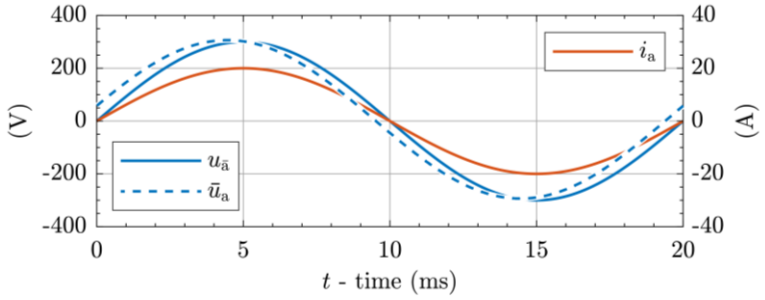
Impression of Sinusoidal Motor Current

- *Pulse-Width Modulation of Inverter Output Voltage*



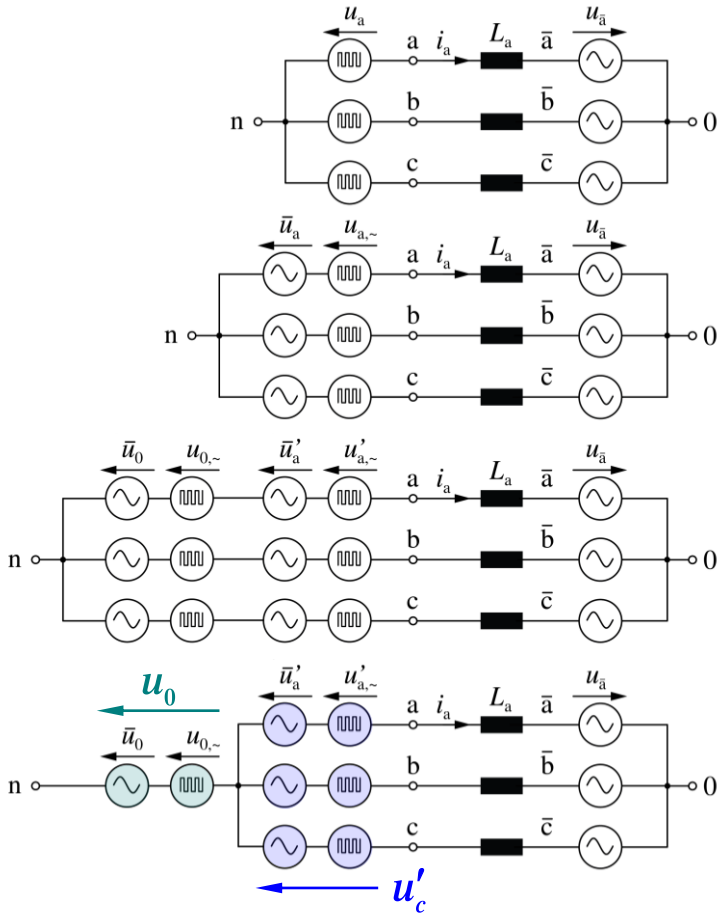






- *Difference of Inverter Voltage u_a and Inner Motor Voltage $u_{\bar{a}}$ Defines Phase Current i_a*

Equivalent Circuit (1)



$$u_a = \bar{u}_a + u_{a\sim}$$
$$u_b = \bar{u}_b + u_{b\sim}$$
$$u_c = \bar{u}_c + u_{c\sim}$$

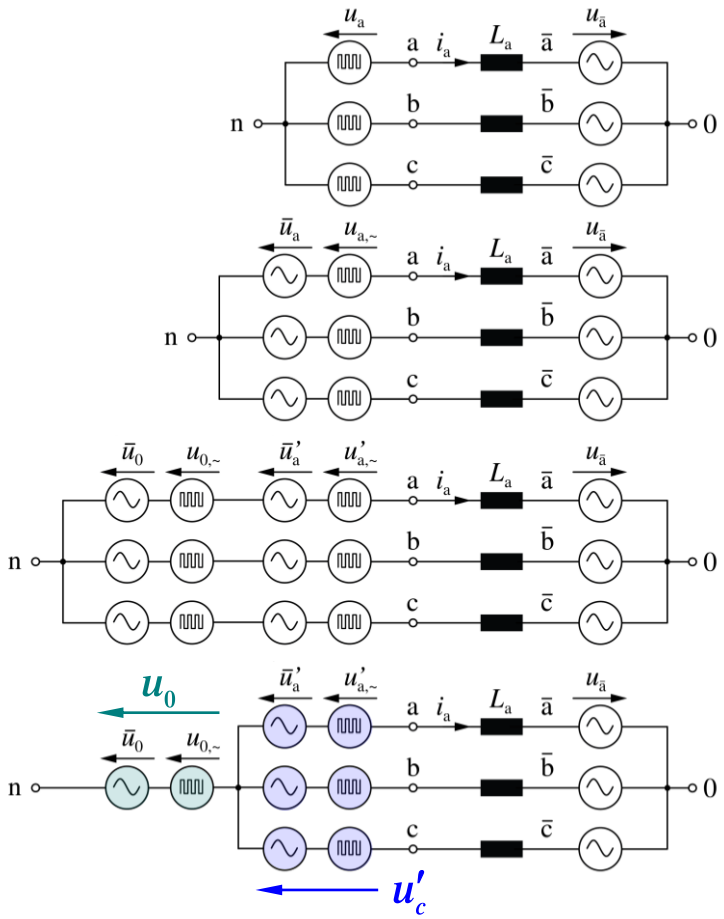
$$u_a = u_a' + u_0 \qquad u_a' + u_b' + u_c' = 0$$
$$u_b = u_b' + u_0$$
$$u_c = u_c' + u_0$$

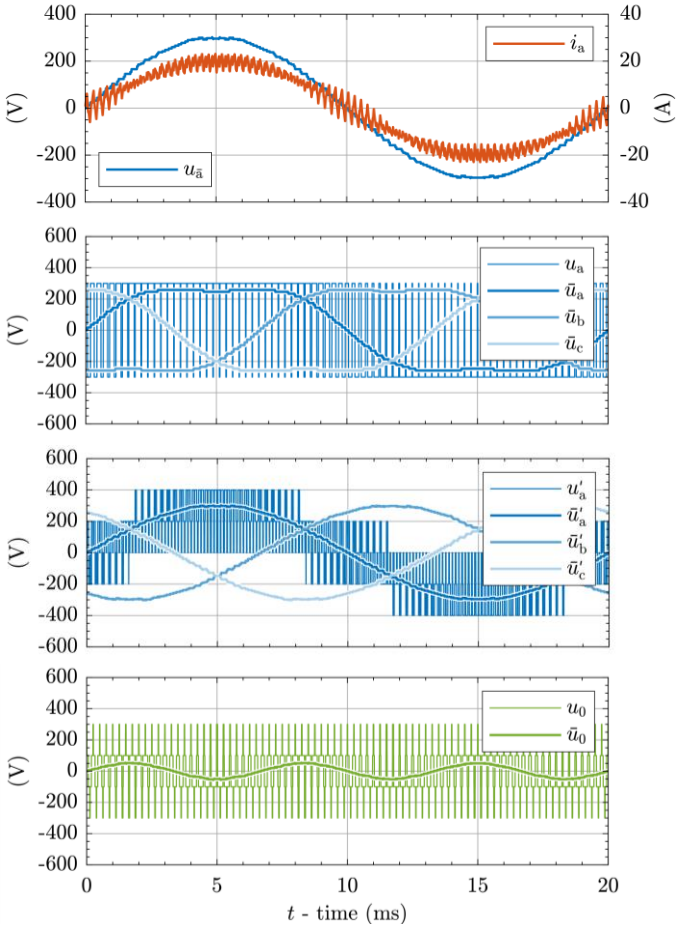
$$u_0 = \tfrac{1}{3}(u_a + u_b + u_c)$$

$$u_a = \bar{u}_a + u_{a\sim}$$
$$u_0 = \bar{u}_0 + u_{0\sim}$$

- *Active Voltage Component* u_a'
- *Inactive CM Zero Sequence Voltage* u_0
- *Low-Frequ. & Sw.-Frequ. Components*

Equivalent Circuit (2)



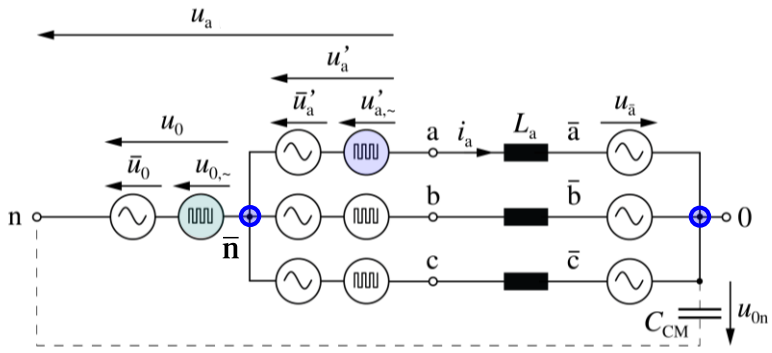


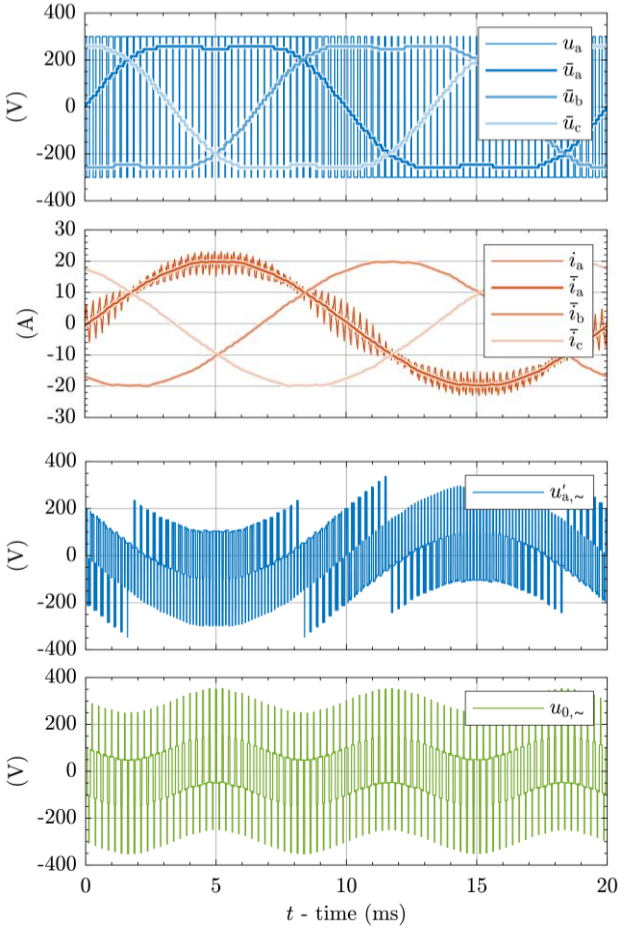
Equivalent Circuit (3)

- Sw.-Frequ. Active / DM Voltage
- Sw.-Frequ. Inactive / CM Voltage

$$u_0 = u_{n0} \quad \rightarrow \quad u_{\bar{n}0} \equiv 0$$

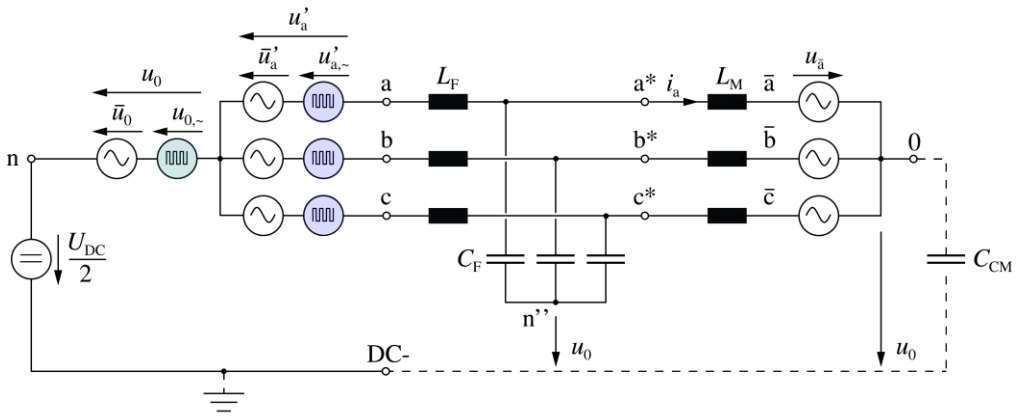
$$\begin{aligned} u_0 + u'_a &= L\frac{di_a}{dt} + u_a + u_{0n} \\ u_0 + u'_b &= L\frac{di_b}{dt} + u_b + u_{0n} \\ u_0 + u'_c &= L\frac{di_c}{dt} + u_c + u_{0n} \\ \hline 3u_0 + 0 &= \quad 0 \quad + 0 \quad + 3u_{0n} \end{aligned}$$

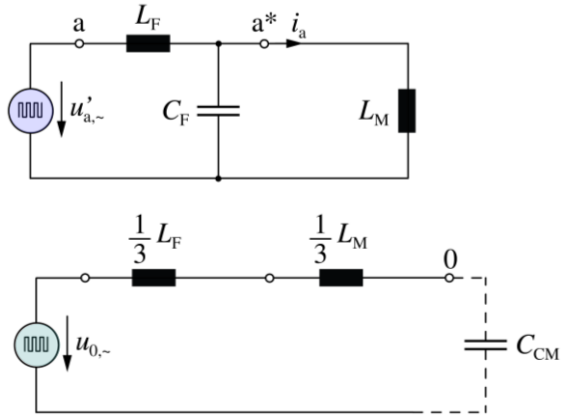




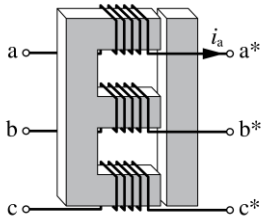
DM / CM Filtering

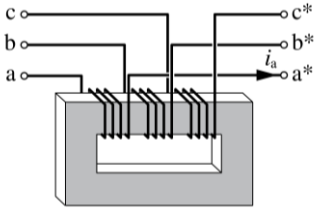
DM & CM Equivalent Circuit

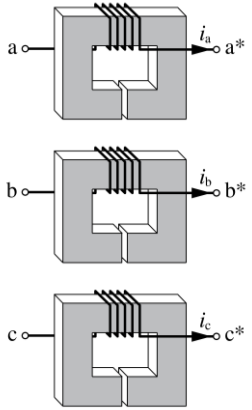




Filter Inductor Types







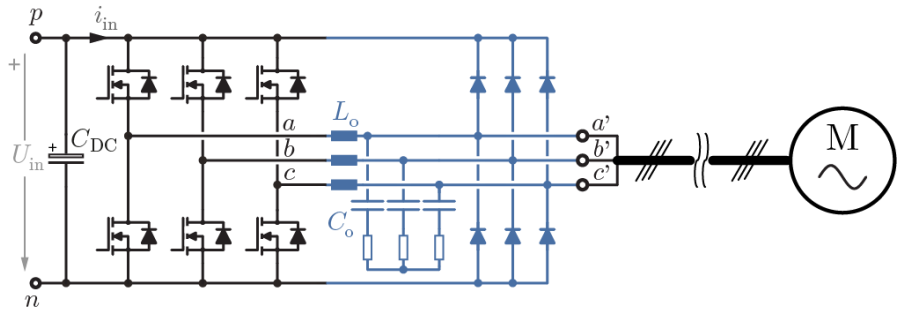
→ DM Inductor / CM Inductor / Phase Inductors

Inverter Output Filters

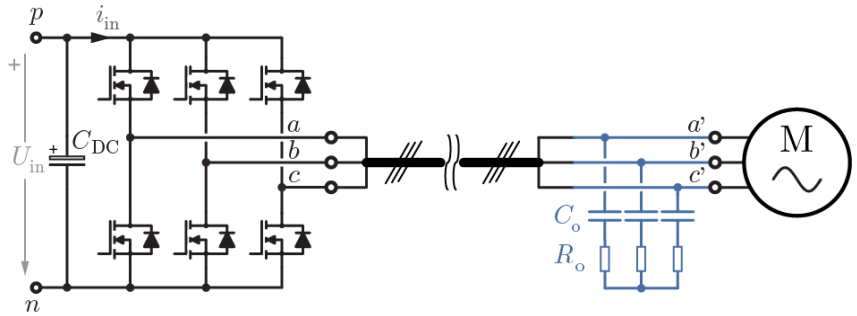
dv/dt-Filters
Motor Cable Termination
Staggered Switching
Active CM-Filtering

Passive dv/dt-Filter & Cable Termination

- $f_C > f_S$ → Reduction of High dv/dt of Inverter Output Voltage to 3...5kV/us



- Termination of Cable with Characteristic Impedance & Damping

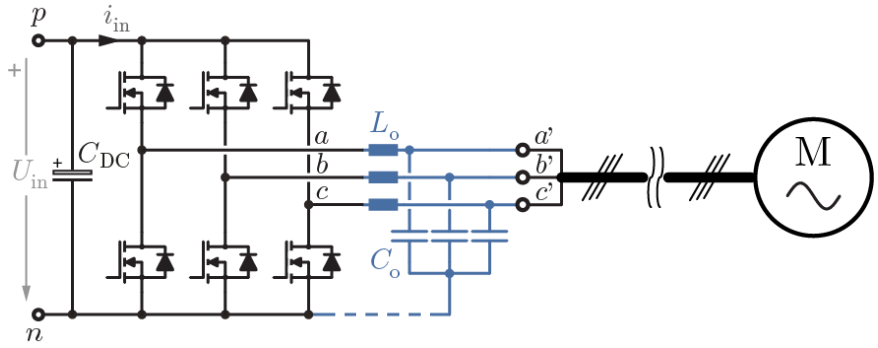


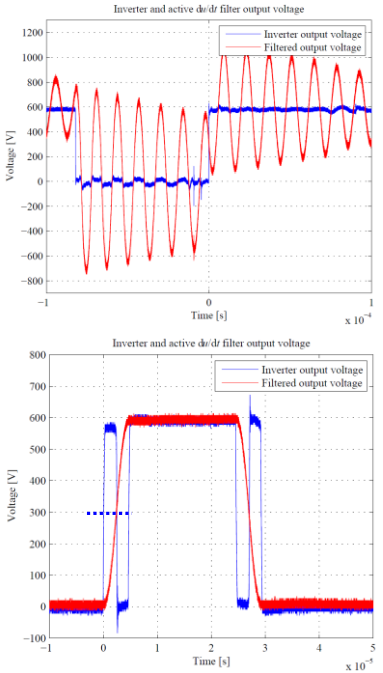
- Limited Applicability @ High Output / Sw. Frequencies (Losses) → Sinewave Filter

Active dv/dt-Filtering

- Active Control of the dv/dt-Filter Transient Behavior → 2-Step Transition
- Influence of Motor Current → Adaption of Sw. Scheme
- Connection to DC- Optional

Source: PhD Thesis, J.P. Ström
Lappeenranta Univ., 2009 / VACON

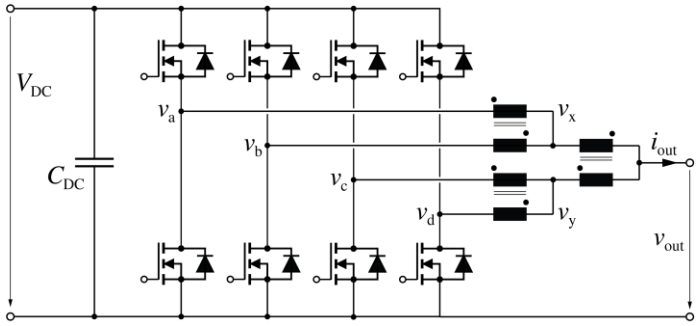


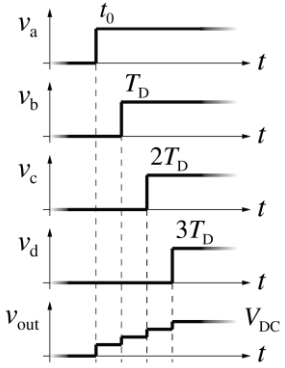


- Ideally No Damping Resistors
- Increase of Sw. Losses → Low Sw. Frequ. OR High Sw. Speed Semiconductors

Staggered/Resonant Switching

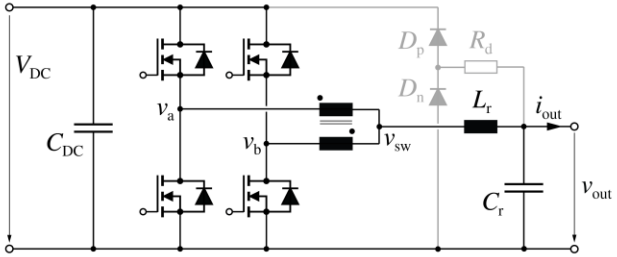
- *Staggered Sw. Parallel Bridge-Legs → Non-Resonant Multi-Step Transistion*

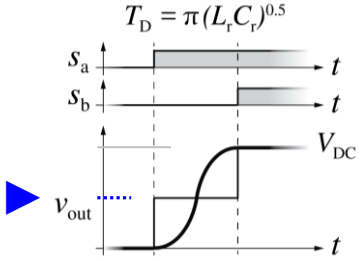




Source: J. Ertl et al. PCIM Europe 2017

- *2-Step Switching / Resonant Transition (cf. Active dv/dt-Filter)*



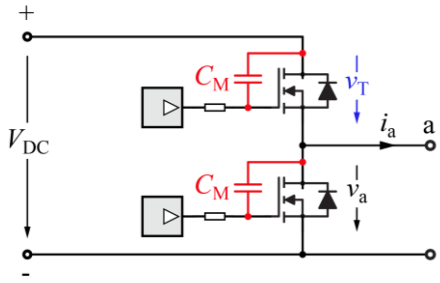


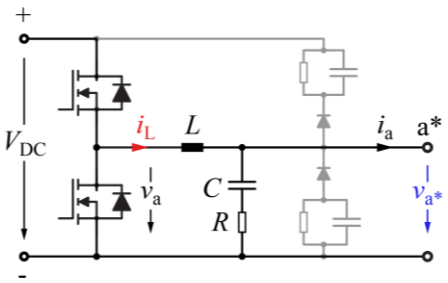
Source: J. Ertl et al. PCIM Europe 2018

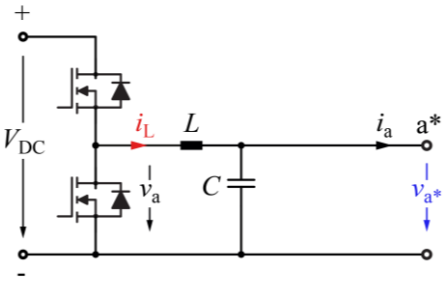
- *Adv. for High Power / Output Curr. Syst. Employing Parallel Bridge-Legs & Local Comm. Cap.*

Comparison of dv/dt-Filtering Techniques (1)

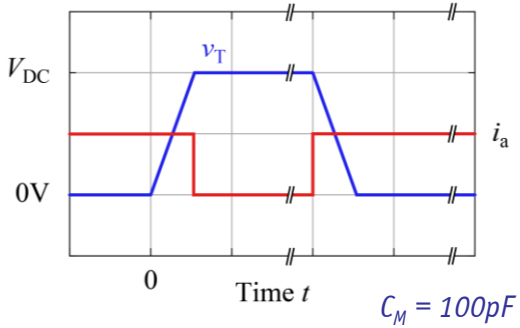
- **Active Concepts**
  1. Miller Capacitor
  2. Gate Curr. Control
- **Passive Concepts**
  1. LCR-Filter
  2. Clamped LC-Filter
- **Hybrid Concepts**
  1. LC-Filter
  2. Multi-Step Switching



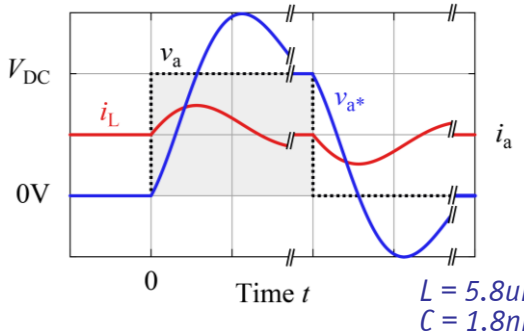




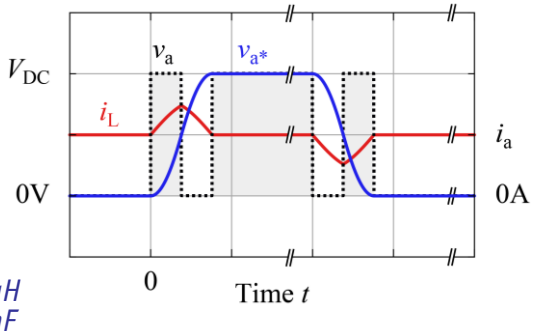
- **Output Voltage Waveforms – V_{DC} = 800V, P_{out} = 10kW**



C_M = 100pF



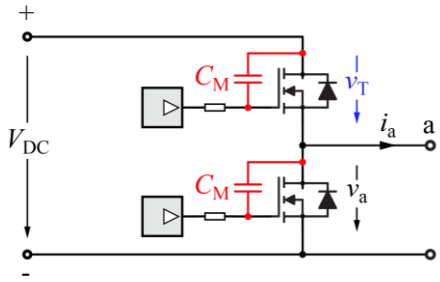
L = 5.8uH
C = 1.8nF
R = 28Ω

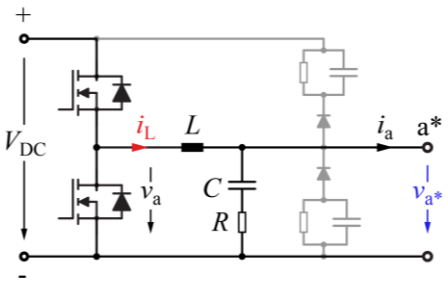


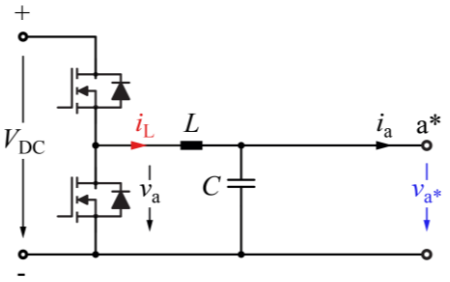
L = 6.2uH
C = 1.3nF

Comparison of dv/dt-Filtering Techniques (2)

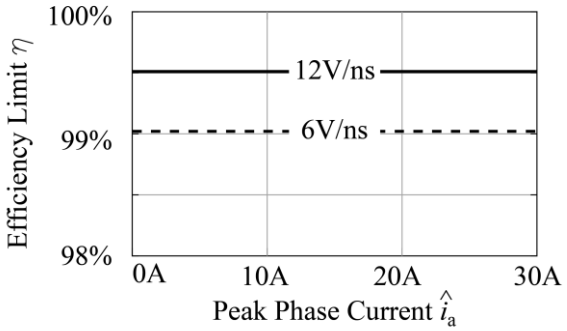
- **Active Concepts**
  1. Miller Capacitor
  2. Gate Curr. Control
- **Passive Concepts**
  1. LCR-Filter
  2. Clamped LC-Filter
- **Hybrid Concepts**
  1. LC-Filter
  2. Multi-Step Switching

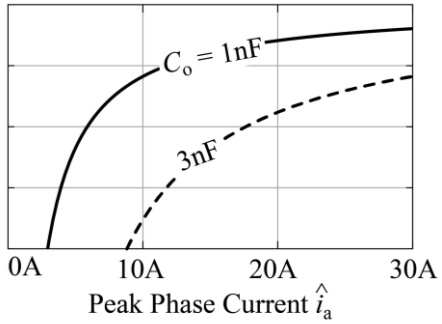


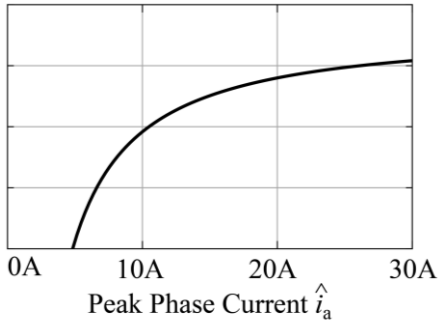




- **Losses – V_{DC} = 800V, P_{out} = 10kW, f_{sw} = 20kHz, 1200V SiC-MOSFETs (16mΩ)**

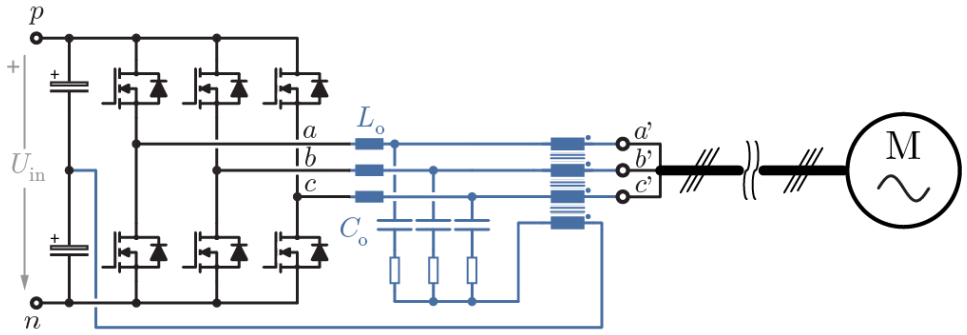






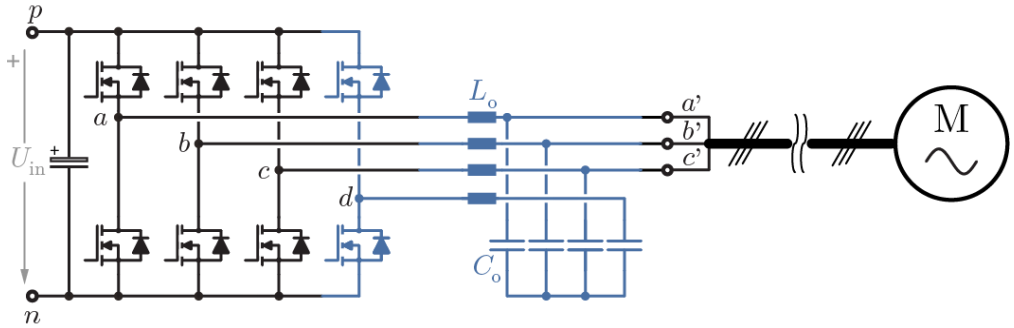
Active CM Voltage Filters (1)

- *Series Compensation of CM-Voltage & DM dv/dt-Filtering*



Source: X. Chen et al., 2007

- *Aux. Bridge-Leg → Zero CM-Voltage for Active Inv. Sw. States & DM dv/dt-Filtering*



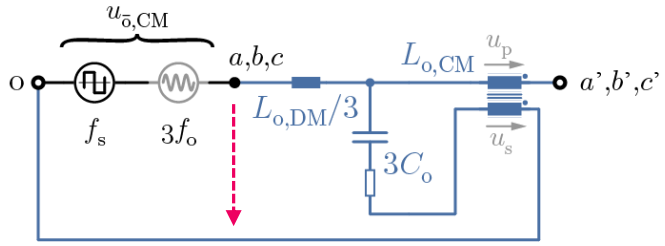
Source: T.A. Lipo et al., 1999

- *Residual CM-Volt. Due to CM-Transf. & Sw. Imperfections / Complexity & Missing Zero State*

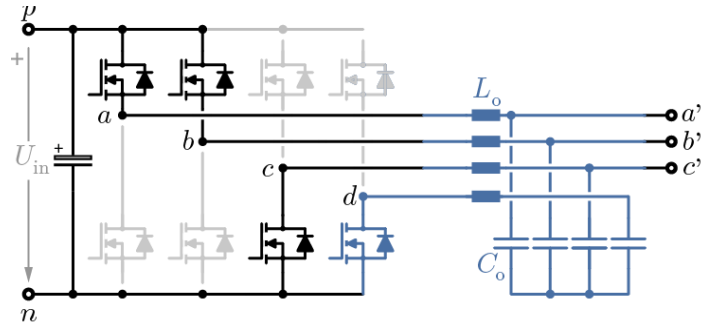
Active CM Voltage Filters (2)

- *Series Compensation of CM-Voltage & DM dv/dt-Filtering*

Source: X. Chen et al., 2007



- *Aux. Bridge-Leg → Zero CM-Voltage for Active Inv. Sw. States & DM dv/dt-Filtering*



Source: T.A. Lipo et al., 1999

- *Residual CM-Volt. Due to CM-Transf. & Sw. Imperfections / Complexity & Missing Zero State*

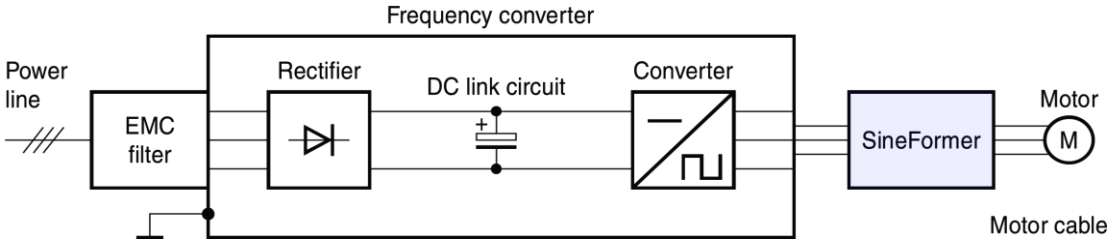
Inverter Systems with Full-Sinewave Output Filters

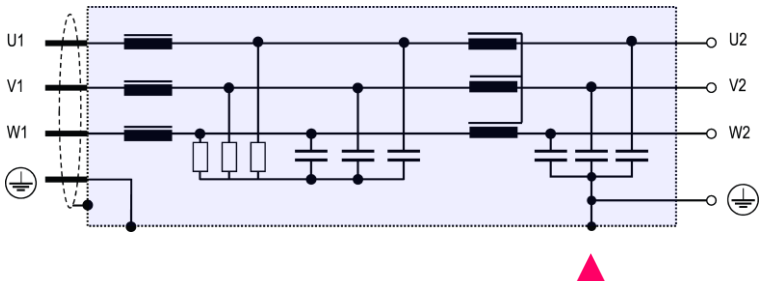
Filter Topology
TCM Inverter Operation
GaN vs. Si VSD Performance
Output Filter Control
Adv. Modulation

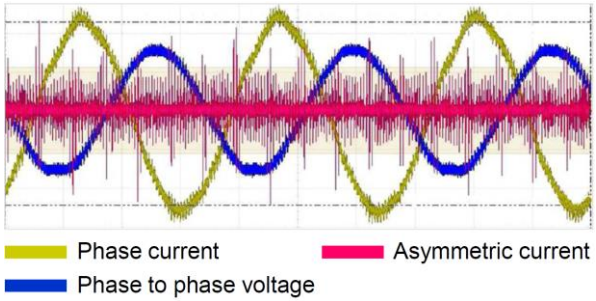
"SineFormer" Output Filter

- $f_C << f_S$ DM and CM (!) Output Filter Stage → Sin. Output Voltage / No Sw. Frequ. CM Voltage
- No Shielded Motor Cables Required
- Reduction of Mains-Side EMI

Source: TDK







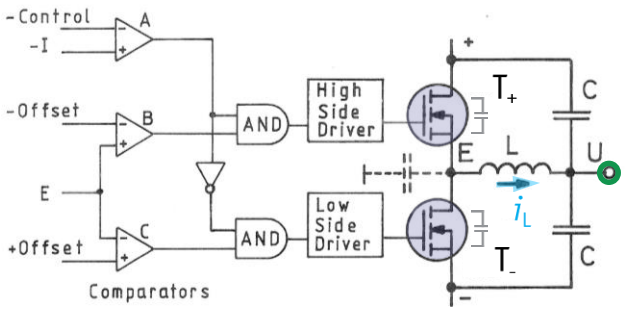
- Large Weight & Volume → ≈2 kVA/dm³ (f_S= 4...8 kHz, f_0= 0...100 Hz)
- Filter Cap. Starpoint Connected to PE Not to DC- (Allows Retrofitting)

Full-Sinewave Filtering

NFO® Sinus

▶ Full-Sinewave Filtering @ ZVS/TCM Operation

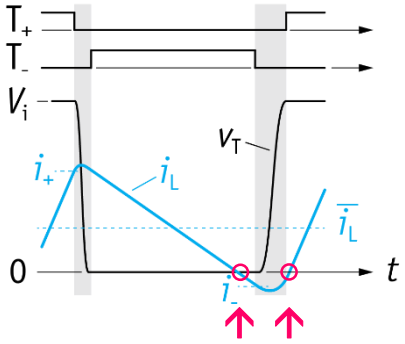
- *ZVS of Inverter Bridge-Legs (No Use of the Intrinsic Diodes of Si MOSFETs)*
- *High Sw. Frequency & TCM → Low Filter Inductor Volume*



Source: Joensson

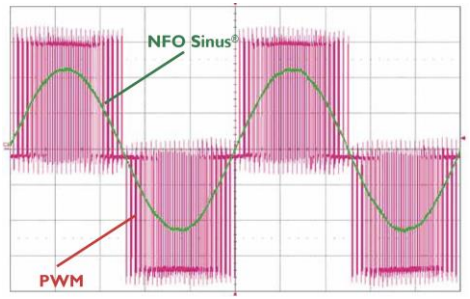
PCIM'88
(POWER CONVERSION)
CONFERENCE
DECEMBER 8-10, 1988
TOKYO, JAPAN

← 1988 !



Source: NFO Sinus

NFO Sinus® is available in size 0.37 kW up to 22 kW



- *Widely Varying Switching Frequency → Voltage Headroom and/or Multiple Bridge-Legs*
- *Rel. High Current Stress on the Power Transistors*

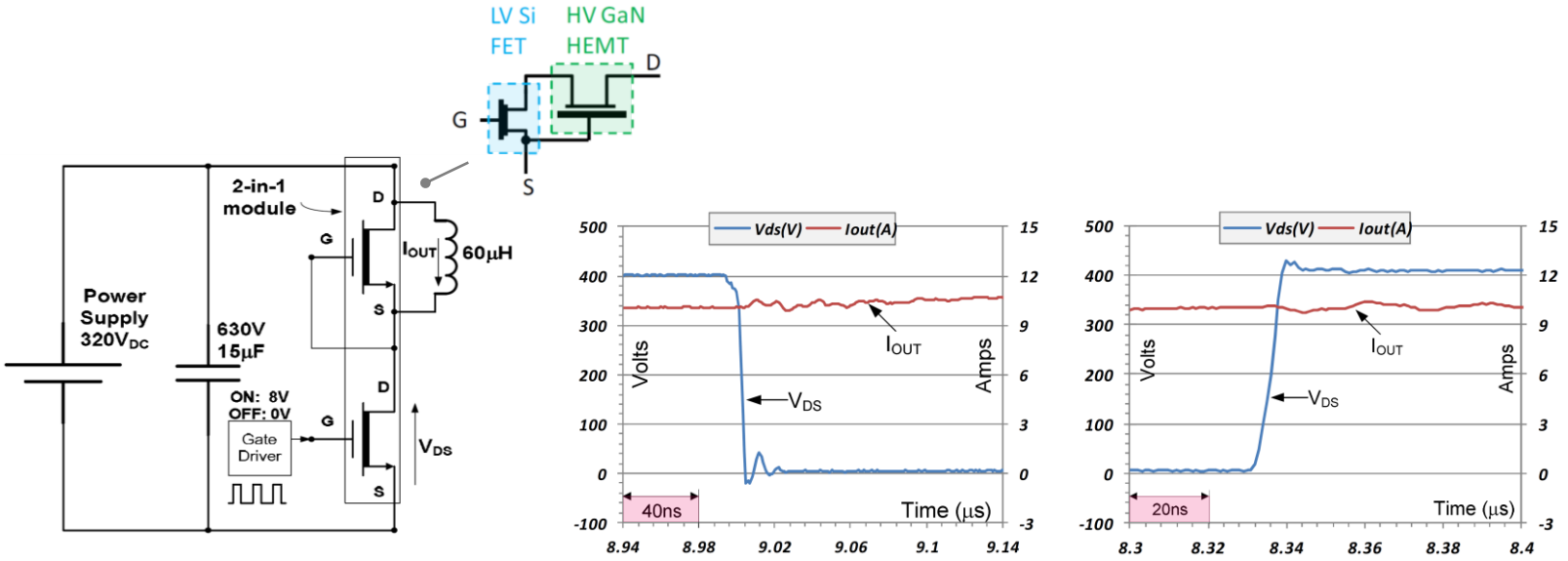
Full-Sinewave Filtering

YASKAWA

▶ 3-Φ 650V GaN Inverter System (1)

Source: YASKAWA

- *Transphorm 650V GaN HEMT/30V Si-MOSFET Cascode Switching Devices*
- *Measurement of Sw. Properties → Turn-On/Off 10A/400V*

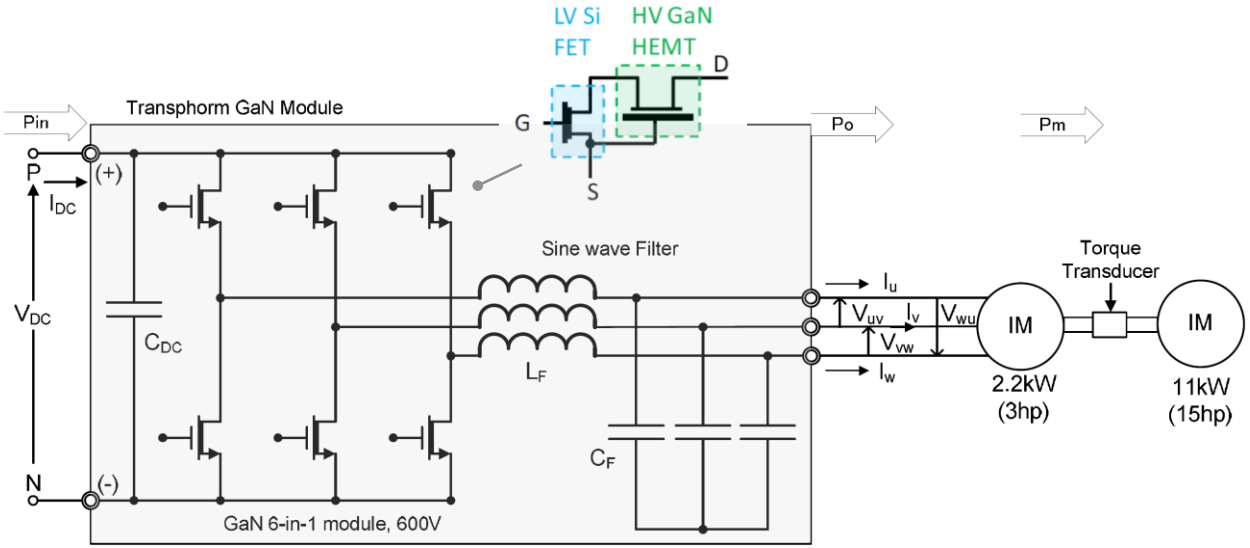


- *Factor 10 Lower On/Off Delay & Sw. Times Comp. to IGBTs*
- *Extremely Low Sw. Losses → Inverter Sw. Frequency f_S= 100kHz*

▶ 3-Φ 650V GaN Inverter System (2)

Source: YASKAWA

- *Transphorm 650V Normally-On GaN HEMT/30V Si-MOSFET Cascode 6-in-1 Power Module*
- *Sinewave LC Output Filter — Corner Frequency f_C= 34kHz (f_S= 100kHz)*
- *No Freewheeling Diodes*



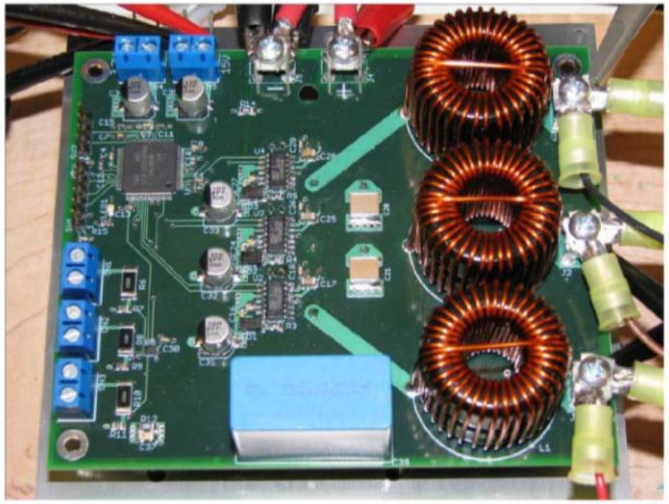
600V/14A

→ *Very Low Filter Volume Compared to Si-IGBT Drive Systems (f_C= 0.8kHz @ f_S ≈ 3kHz)*

▶ 3-Φ 650V GaN Inverter System (3)

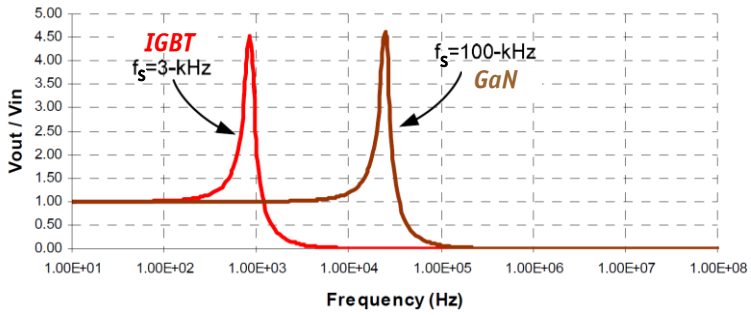
Source: YASKAWA

- Transphorm 650V Normally-On GaN HEMT/30V Si-MOSFET Cascode 6-in-1 Power Module
- Sinewave LC Output Filter — Corner Frequency f_C= 34kHz (f_S= 100kHz)
- No Freewheeling Diodes



L_F=220uH Iron Powder Core Filter Inductors, C_F=0.1uF

$f_C \approx 1/5\, f_S$

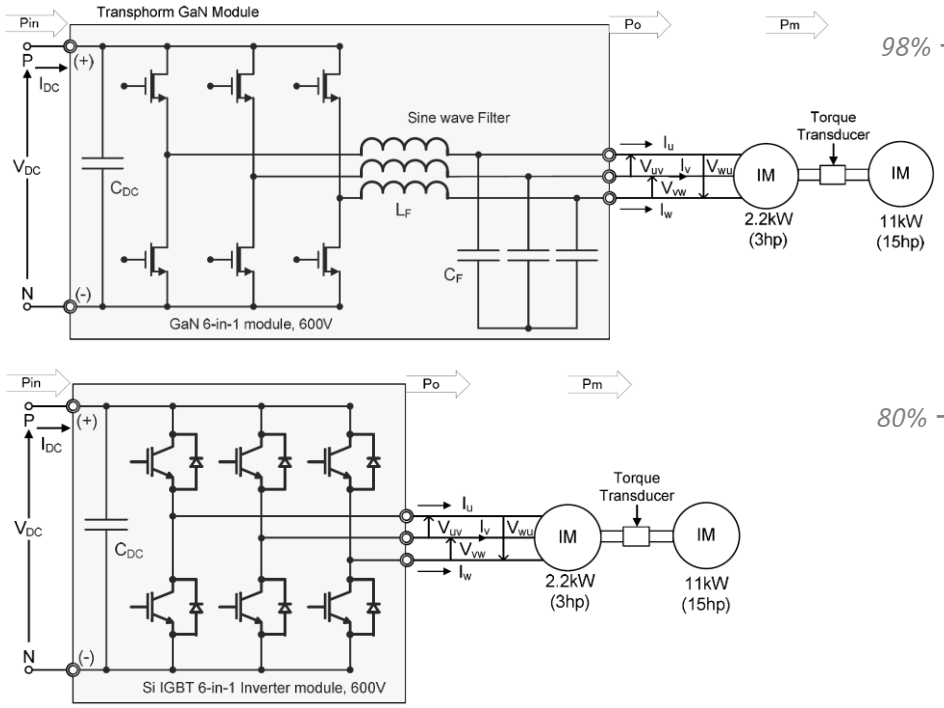


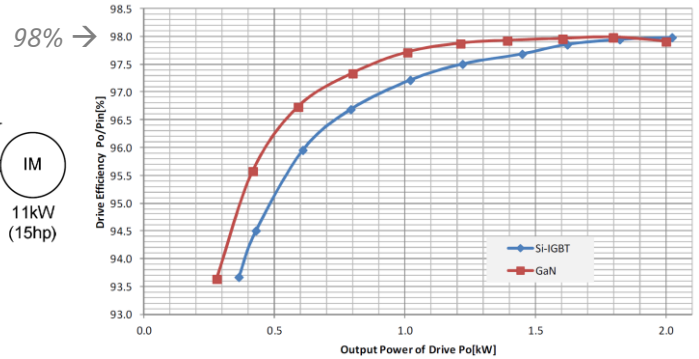
→ Very Low Filter Volume Compared to Si-IGBT Drive Systems (f_C= 0.8kHz @ $f_S \approx$ 3kHz)
→ Lower Size of DC Input Capacitor (-75% vs. IGBT) & -8dB Audible Noise @ 6krpm

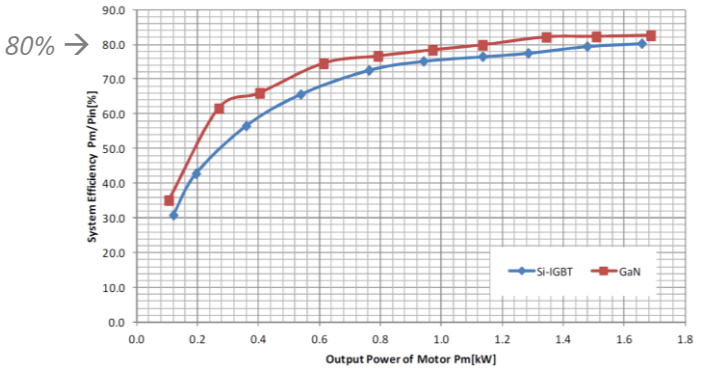
▶ 3-Φ 650V GaN Inverter System (4)

Source: YASKAWA

- *Comparison of GaN Inverter with LC-Filter to Si-IGBT System (No Filter, f_S=15kHz)*
- *Measurement of Inverter Stage & Overall Drive Losses @ 60Hz*





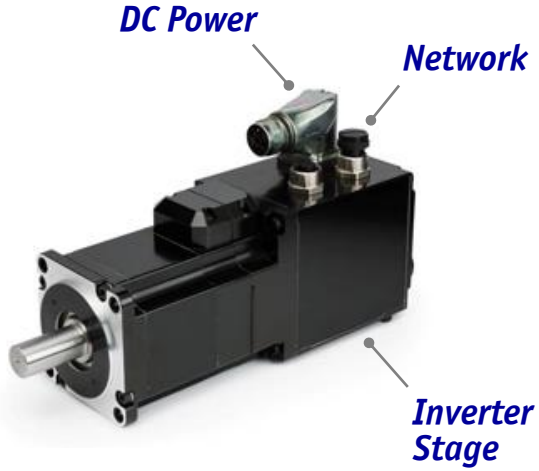


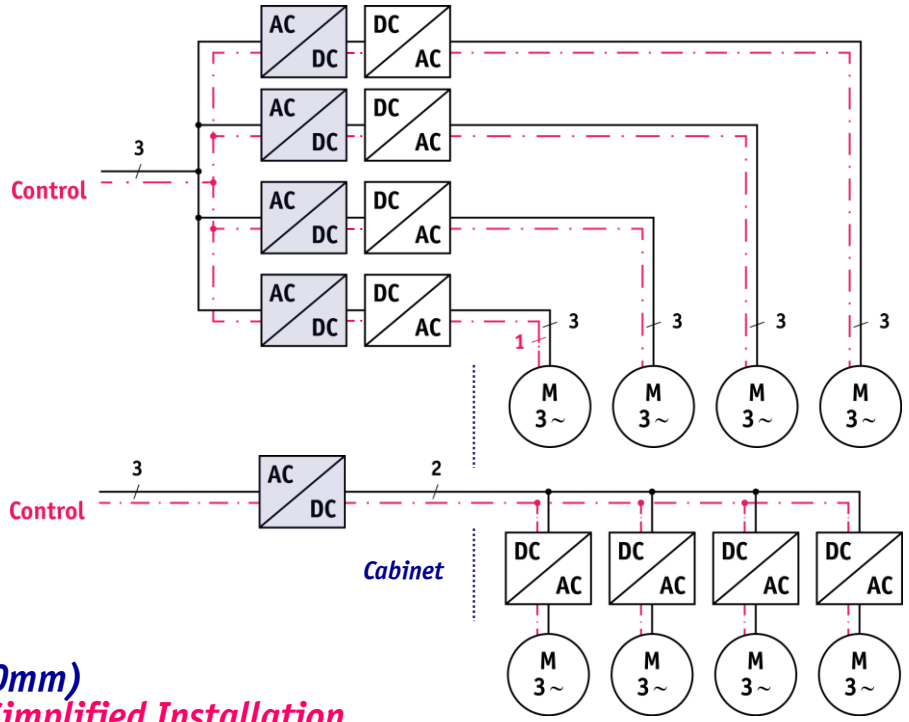
→ *2% Higher Efficiency of GaN System Despite LC-Filter (Saving in Motor Losses) !*

▶ 3-Φ 650V GaN Inverter System (5)

Source: YASKAWA

- *Sigma-7F Servo Drive — Motor Integration of DC/AC Stage (TO-220 GaN)*
- *Distributed DC-Link System — Single AC/DC Converter / Smaller Cabinet*
- *0.1 – 0.4kW / 270...324V Nominal DC-Link Voltage*





→ *Small Size (0.4 kW @ 70 x 70x 170mm)*
→ *Massive Saving in Cabling Effort / Simplified Installation*

Full-Sinewave Filtering

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▶ 2-Stage Full-Sinewave Output Filter (1)

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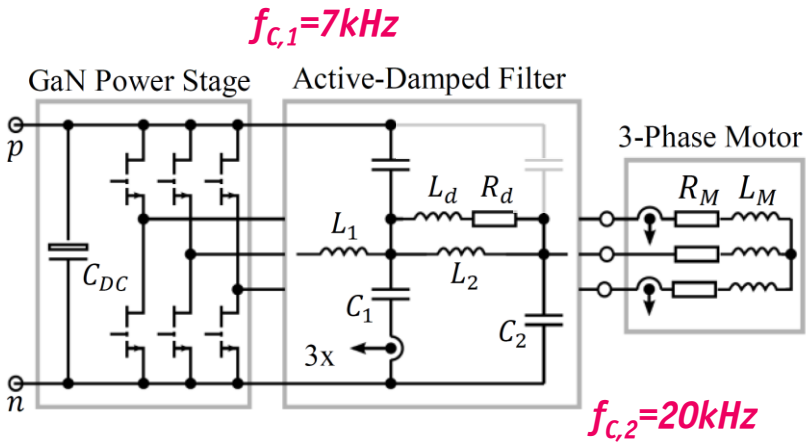
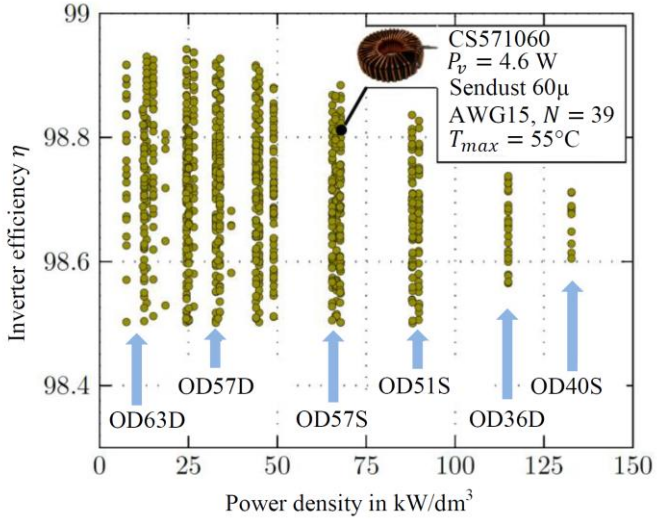
H. Ertl et al. (2018)

- *Sinewave Output & IEC/EN 55011 Class-A*
- *Low-Loss Active Damping of 1st Filter Stage — Neg. Cap. Current Feedback*
- *2kW / 400V DC-Link 3-Φ 650V GaN Inverter (I_M=5A), $f_{out,max}$ = 500Hz*
- *Sw. Frequency f_S= 100kHz*

Outer Diameter OD=35…65mm
S=Single/D=Two Stacked Cores
Solid Copper Wire AWG 13…20
Sendust, MPP, High-Flux, etc.





→ *Evaluation of Optimized Inductors — Soft Sat. Toroidal Iron Powder Cores*
→ *L_1=200uH (OD57S) / C_1=2.5uF / L_2=25uH (OD20S) / C_2=2.5uF / L_d=33uH / R_d=5.6Ω*

2-Stage Full-Sinewave Output Filter (2)

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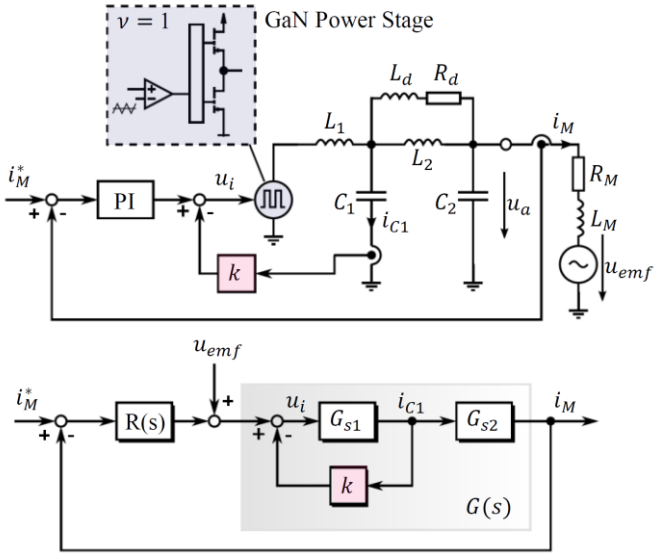
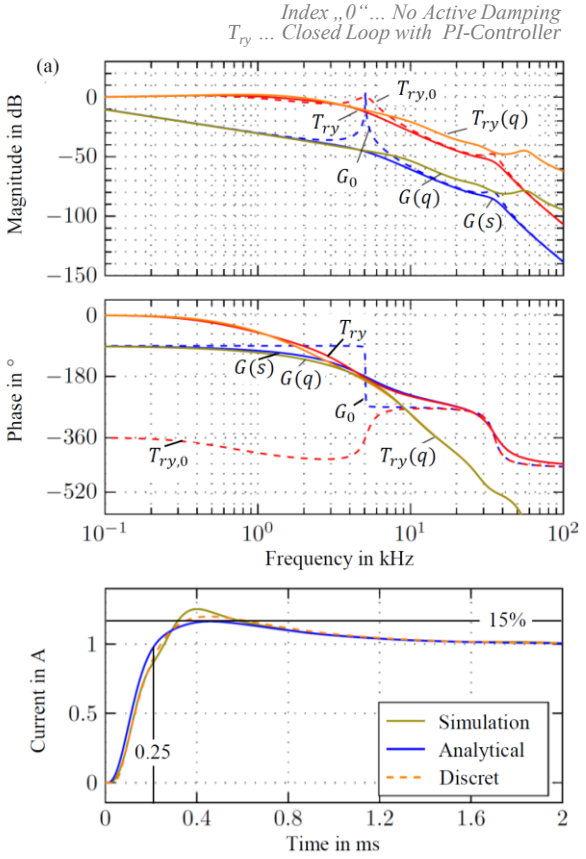
- Neg. Cap. Current Feedback Emulates "Loss-Free" Damping Resistor
- Passive Damping of 2nd Filter Stage
- PI-Type Current Control



→ Transfer Functions & Step Response



2-Stage Full-Sinewave Output Filter (3)

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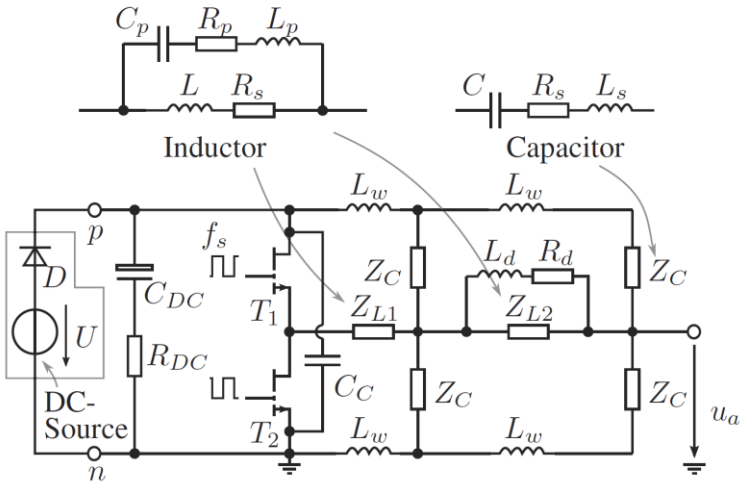
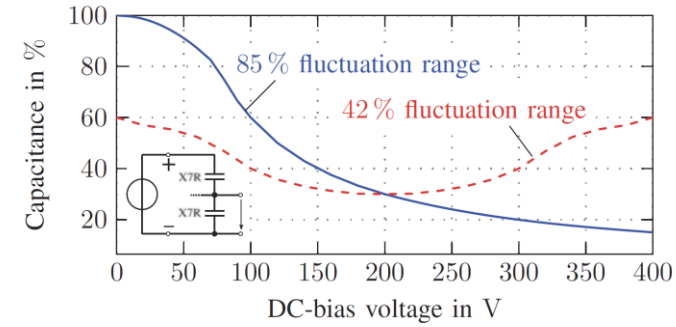
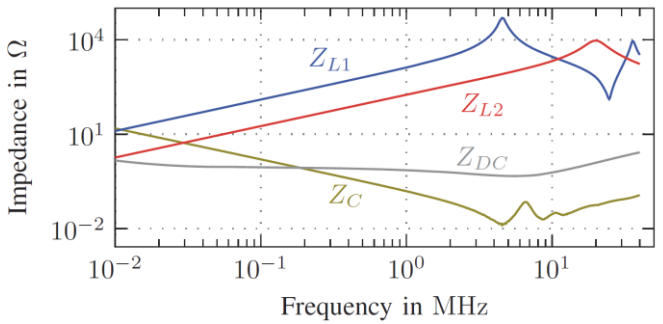
- *Nonlinearity of MMLC Caps (X7R, 330nF/500V) → Effect on i_C-Feedback*
- *Symmetric Connection of Filter Capacitors to +/-DC Reduces Nonlinearity*
- *1st Resonance of Filter Components @ ≈5MHz*







- *Impedances of Filter Components & DC-Link Capacitor (C_{DC} =120uF)*

▶ 2-Stage Full-Sinewave Output Filter (4)

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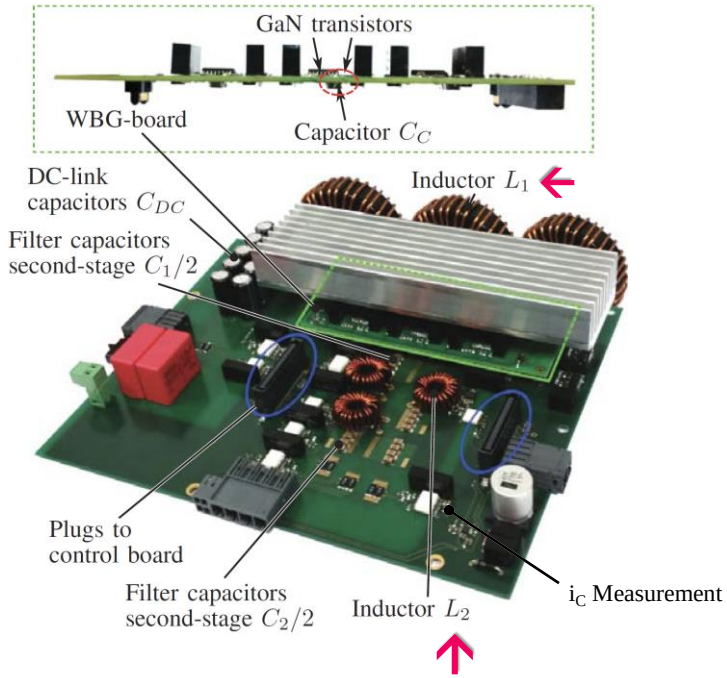
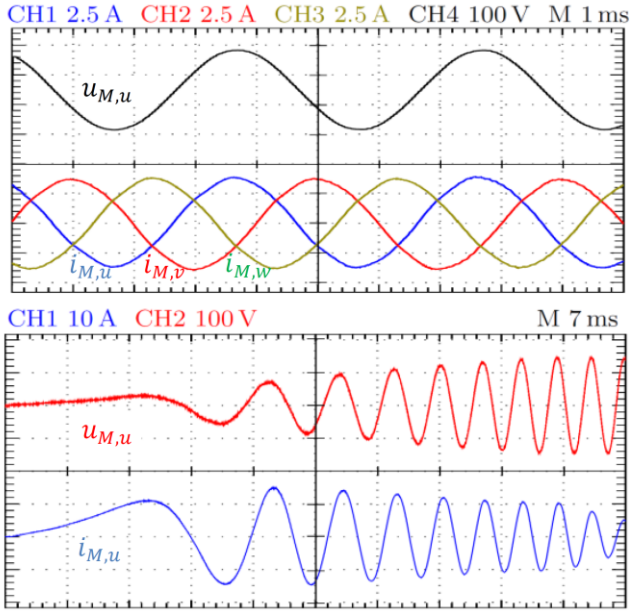
- *Exp. Verification — 650V E-Mode GaN Systems Transistors (50mΩ)*
- *Sw. Frequency f_S= 100kHz, Efficiency ≈98%*
- *200mm x 250mm*





- *Stationary Motor Phase Curr. /Voltage @ 2.5Nm & f_{out}=250Hz*
- *Speed Increase from Standstill to n = 3000rpm in 60ms*

▶ 2-Stage Full-Sinewave Output Filter (5)

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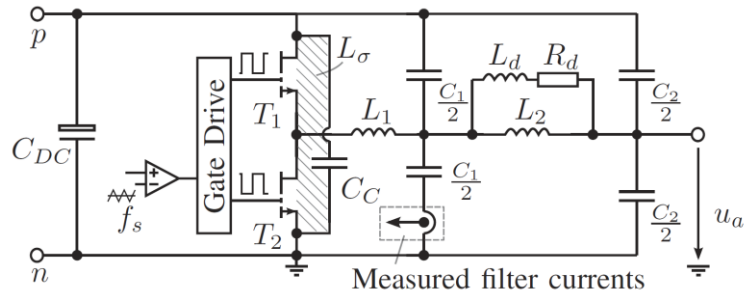
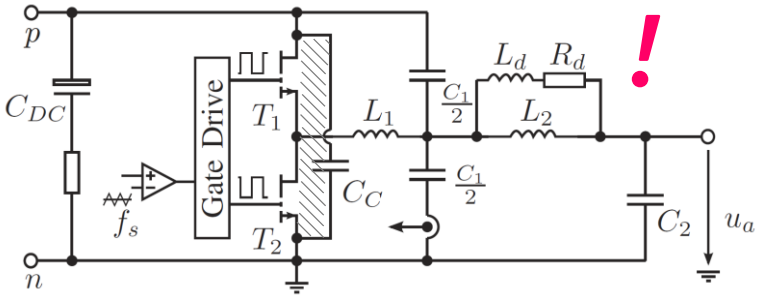
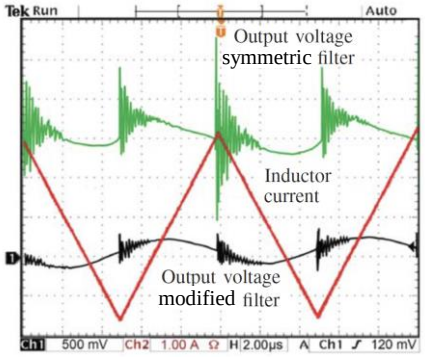
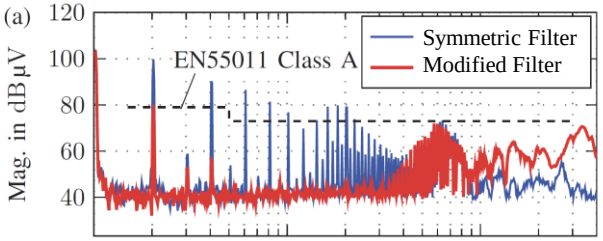
- *Modification of Output Filter Structure*
- *Elimination of Direct Cap. Coupling Between Output and Noisy (!) DC+ (Due to R_{DC})*
- *For Opt. i_C-Feedback C_1 Realized Using ≈Linear Kemet KC-Link*









- *Modified Filter → Compliance to EMI Standard EN55011 Class-A*

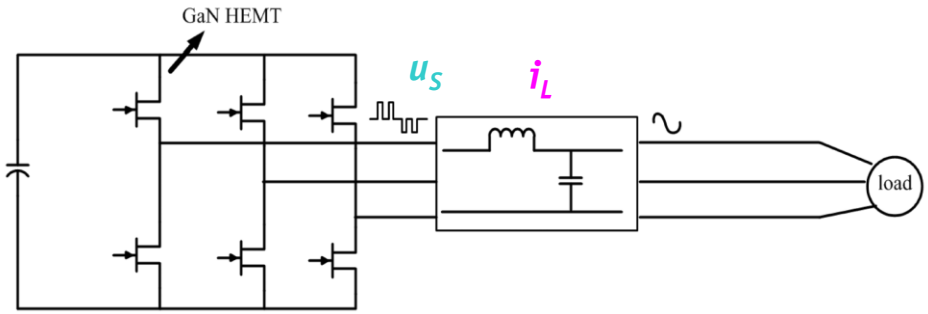
Full-Sinewave Filtering

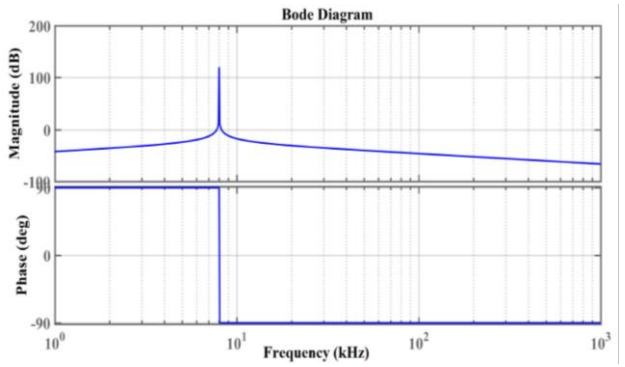
SIEMENS

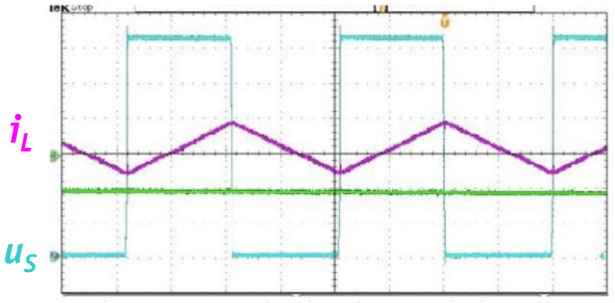
▶ 3-Φ 900V GaN Inverter System (1)

Source: SIEMENS

- 900V Normally-Off GaN in TO-220 Package (165mΩ)
- 650V DC-Link Voltage (!) / Sinewave Output Filter
- Filter Corner Frequ. f_C — Geom. Mean of f_S & $10f_{out,max}$
- Sw. Frequency f_S= 128kHz







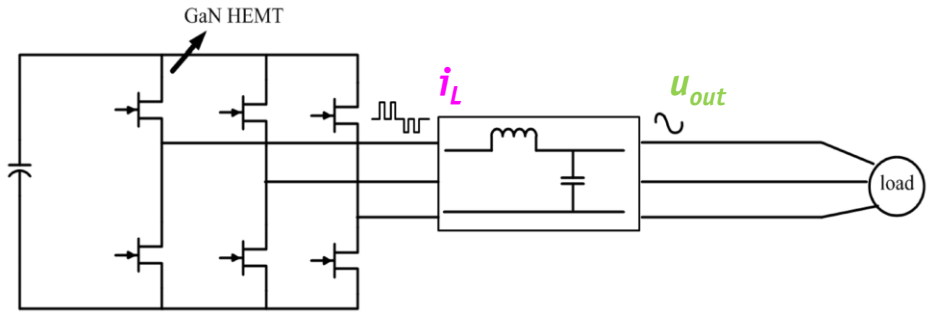
100V/div
2A/div

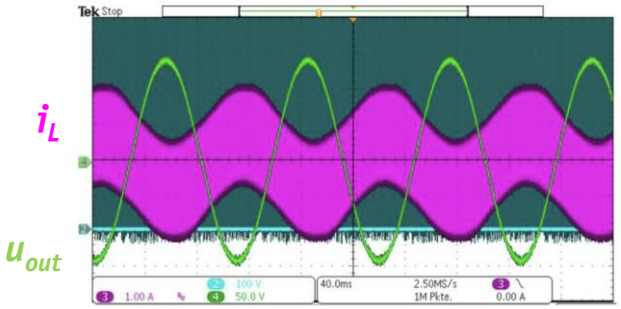
- Filter Corner Frequency f_C = 8kHz (L=320uH, $\Delta i_{L,max}$=50% @ 3kW)

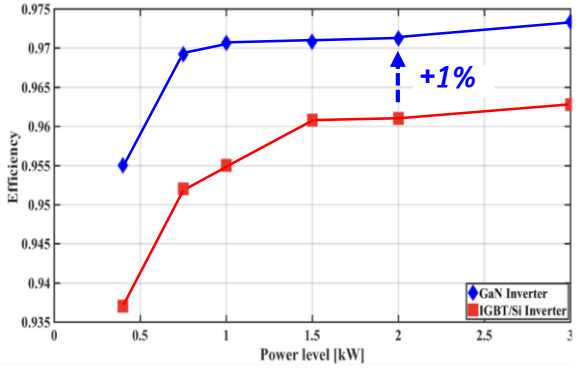
▶ 3-Φ 900V GaN Inverter System (2)

Source: SIEMENS

- 900V Normally-Off GaN in TO-220 Package (165mΩ)
- 650V DC-Link Voltage (!) / Sinewave Output Filter
- Filter Corner Frequ. f_C — Geom. Mean of f_S & $10f_{out,max}$
- Sw. Frequency f_S= 128kHz







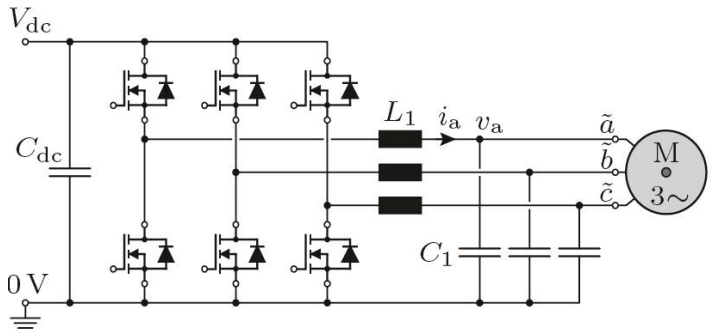
- GaN Inverter & Filter → 1% Higher Efficiency Comp. to Si-IGBT System (f_S= 16kHz, No Filter)

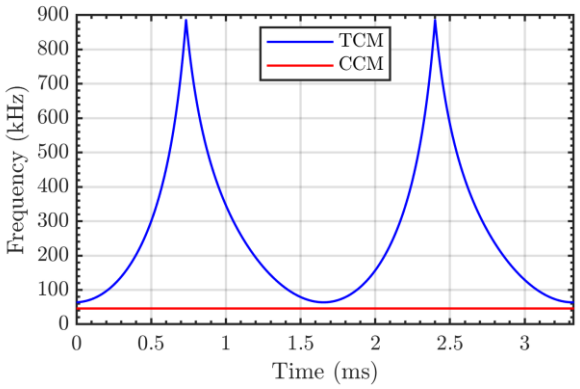
Full-Sinewave Filtering

Multi-Objective Optimization

Modulation Methods — CCM / TCM

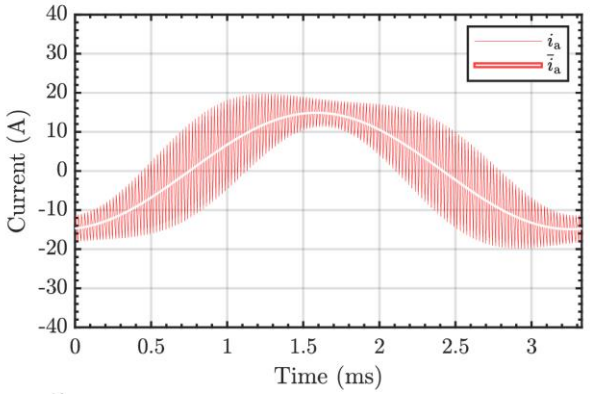
- Constant (CCM) vs. ZVS Variable (TCM) Sw. Frequency
- 7.5 kW 3-Φ 800 V_{dc} PWM Inverter w/ LC Output Filter



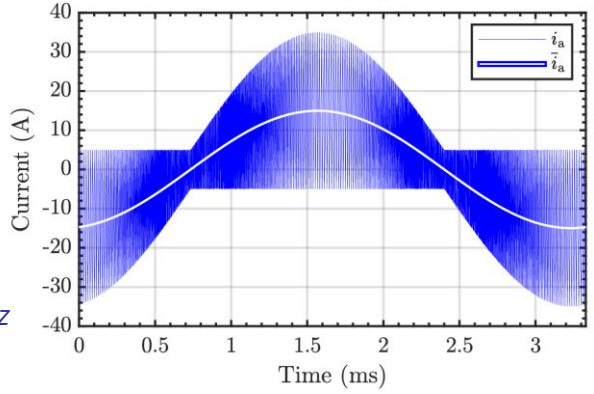


f_{sw} = 46 kHz

▶ CCM



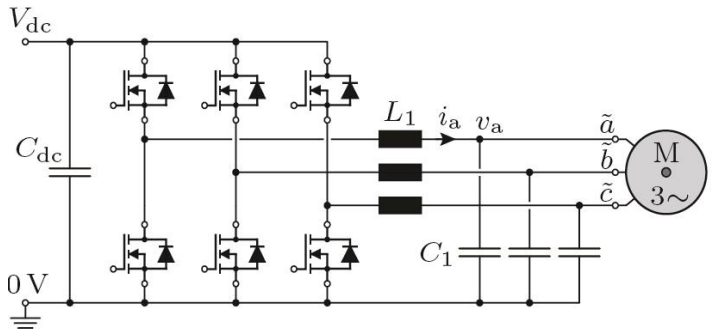
▶ TCM

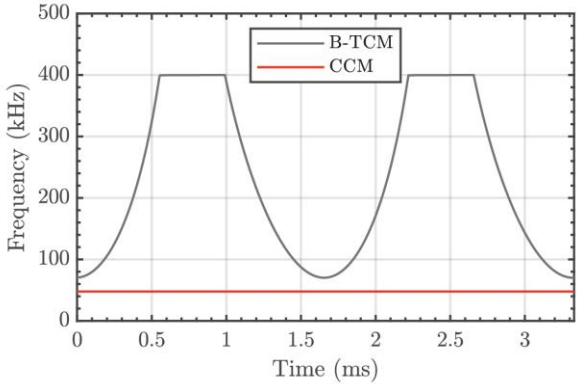


$f_{sw,min}$ = 64 kHz
$f_{sw,max}$ = 886 kHz

Modulation Methods — CCM / B-TCM

- Constant (CCM) vs. Bounded Var. Sw. Frequency (B-TCM)
- 7.5 kW 3-Φ 800 V_{dc} PWM Inverter w/ LC Output Filter

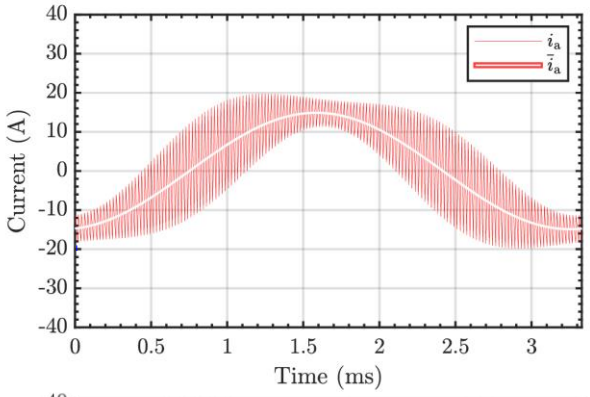




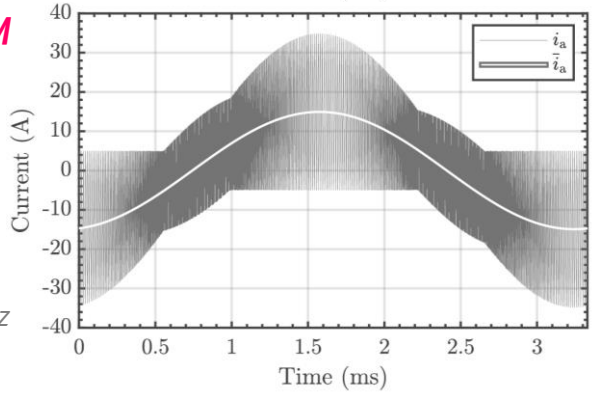
$f_{sw,min}$ = 70 kHz
$f_{sw,max}$ = 400 kHz

f_{sw} = 46 kHz

▶ CCM



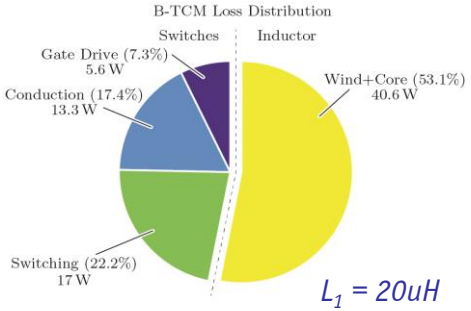
▶ B-TCM



▶ Pareto-Optimization of CCM/TCM/B-TCM (1)

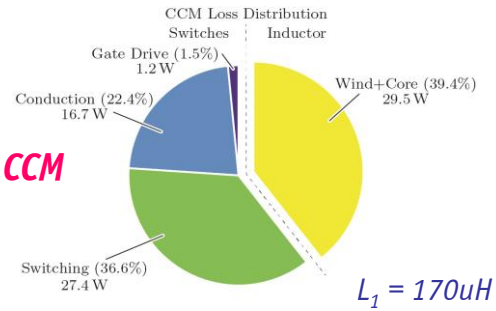
- 7.5kW 3-Φ 800V_{dc} PWM Inverter w/ LC Output Filter
- Loss Breakdown @ Efficiency = 99.0%

B-TCM



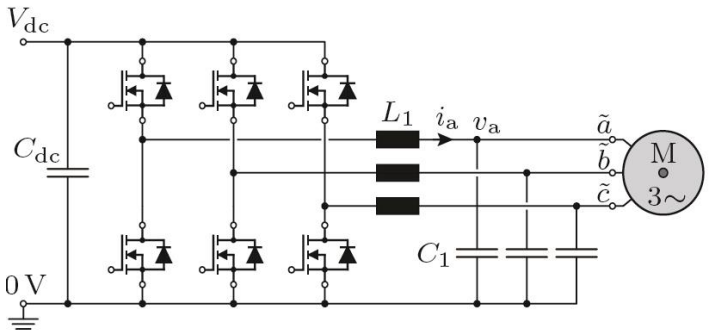
L_1 = 20uH

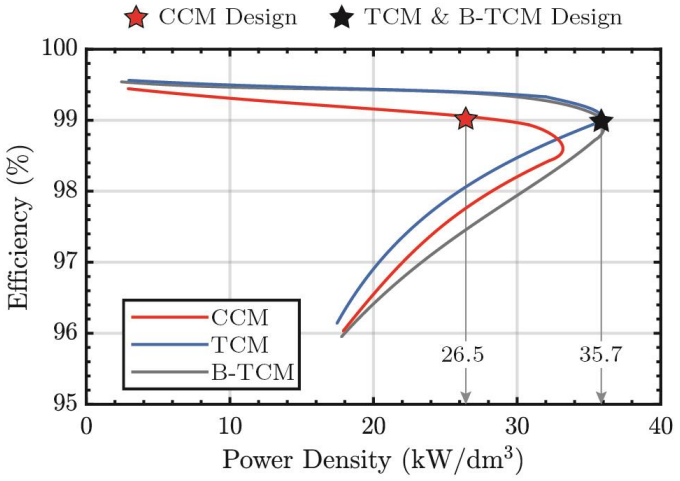
CCM



L_1 = 170uH

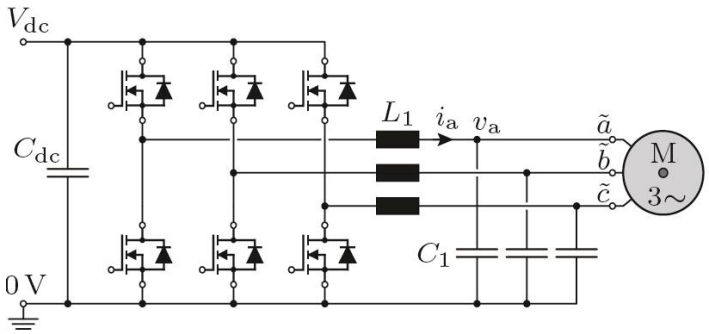
- +40% Power Density of B-TCM & TCM



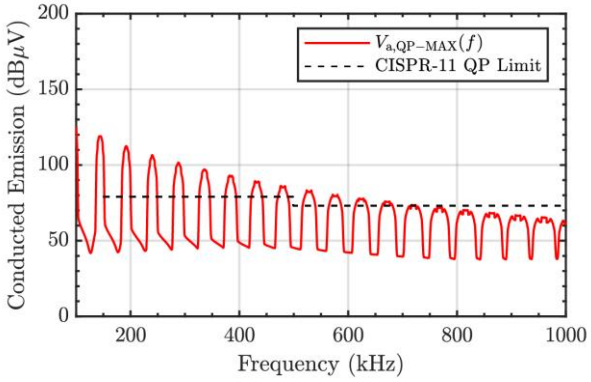


▶ Pareto-Optimization of CCM/TCM/B-TCM (2)

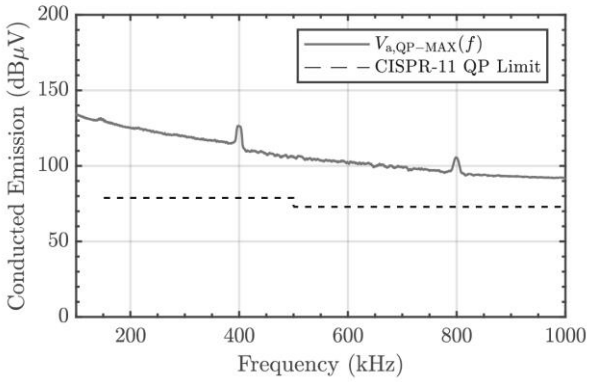
- 7.5 kW 3-Φ 800 V_{dc} PWM Inverter w/ LC Output Filter
- Req. 2nd Filter Stage Attenuation



▶ CCM

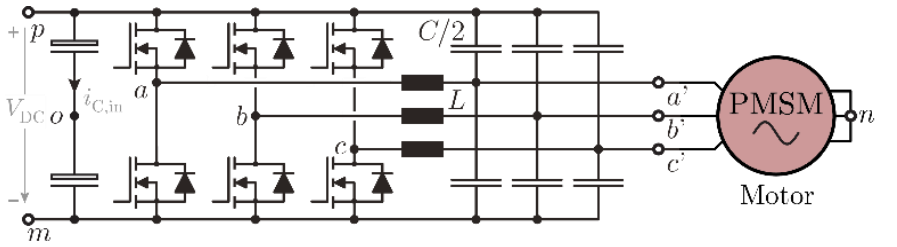


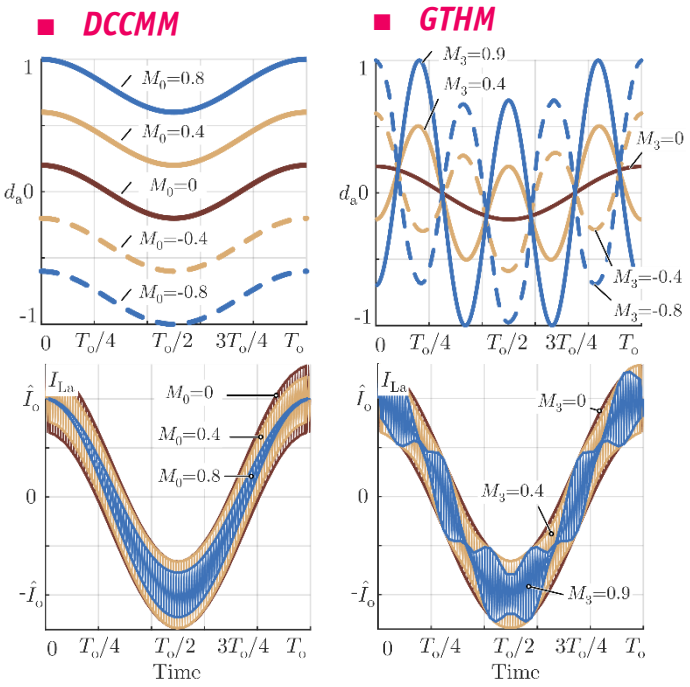
▶ B-TCM



Remark — Advanced 3rd Harmonic Injection (1)

- DC- Ref. LC-Filter → Max. Ind. Current Ripple @ d=0.5
- DCCMM — Max. DC-Offset M_0 Shifting Phase Voltages Towards d=0 OR d=1
- GTHM — Max. 3rd Harm. M_3 for Red. of Sw. Frequ. Harmonic Power

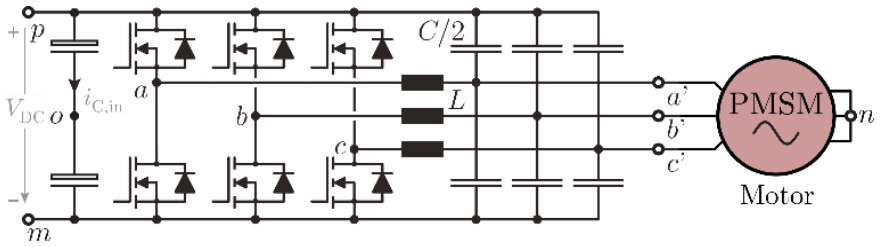




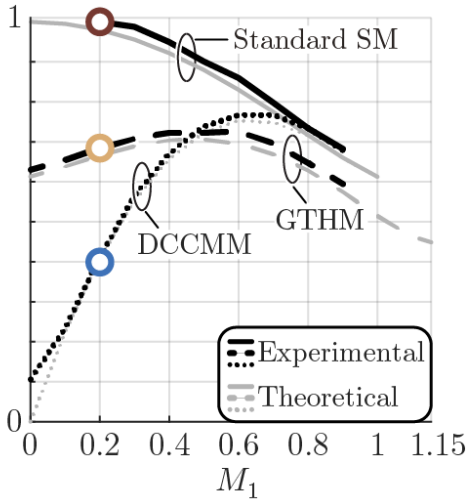
- GTHM → Add. Cap. Reactive Power — Critical @ High f_{out}
- DCCMM → Unequal Stress on the Power Semiconductors — Critical @ Low f_{out}

Remark — Advanced 3rd Harmonic Injection (2)

- Massive Red. of Current Ripple @ Lower Modulation Index
- DCCMM — Adv. for M = 0...0.5
- GTHM — Adv. for M = 0.5...1.0



$$F = \frac{\Delta I_{RMS}}{\Delta I_{RMS,max}}$$



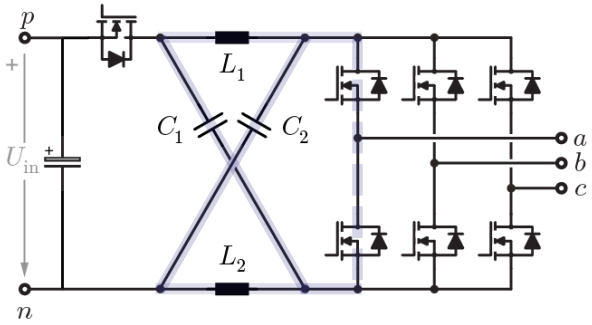
- GTHM → Add. Cap. Reactive Power — Critical @ High f_{out}
- DCCMM → Unequal Stress on the Power Semiconductors — Critical @ Low f_{out}

Buck+Boost Inverter

Z-Source Inverter etc.
VSI & DC/DC Front-End
Double-Bridge VSI
Phase-Modular Buck+Boost Inverter
CSI & DC/DC Front-End

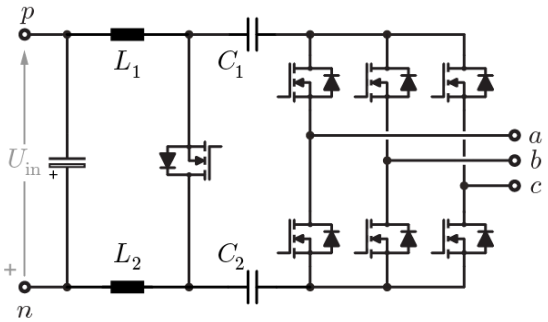
"Outside-the-Box" Topologies

- Z-Source Inverter → Shoot-Through States Utilized for Boost Function
- Higher Component Stress Eff. Limits Boost Operation to ≈120% U_{in}



Source: F.Z. Peng / 2003
J. Rabkowski / 2007

- 3-Φ Back-End DC/AC Cuk-Converter

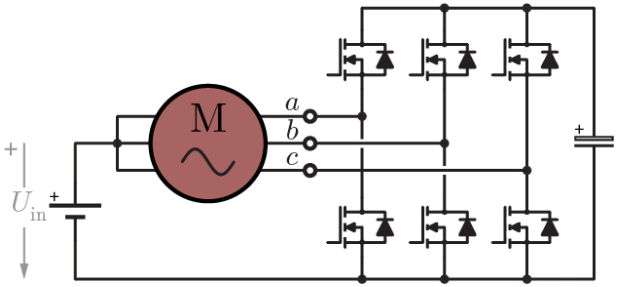


Source: T.A. Lipo et al. /2002 & K.D.T Ngo / 1984

- Integration Typ. Results in Higher Comp. Stresses & Complexity / Lower Performance

Boost Converter DC-Link Voltage Adaption

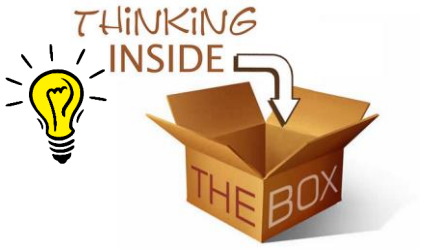
- *Inverter-Integr. DC/DC Boost Conv. → Higher DC-Link Voltage / Lower Motor Current*
- *Access to Motor Star-Point & Specific Motor Design Required*
- *No Add. Components*

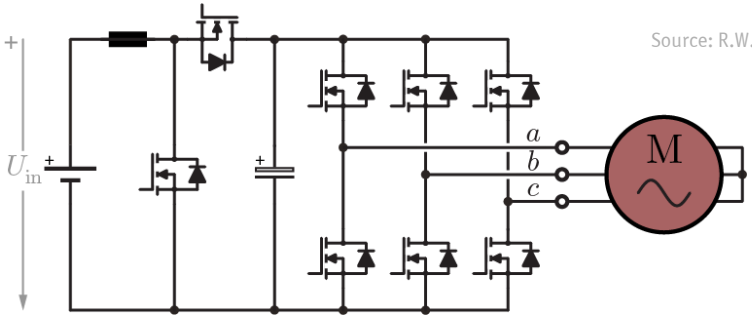


Source: J. Pforr et al. / 2009

- *Explicit Front-End DC/DC Boost Stage*

Source: www.rick-gerber.com



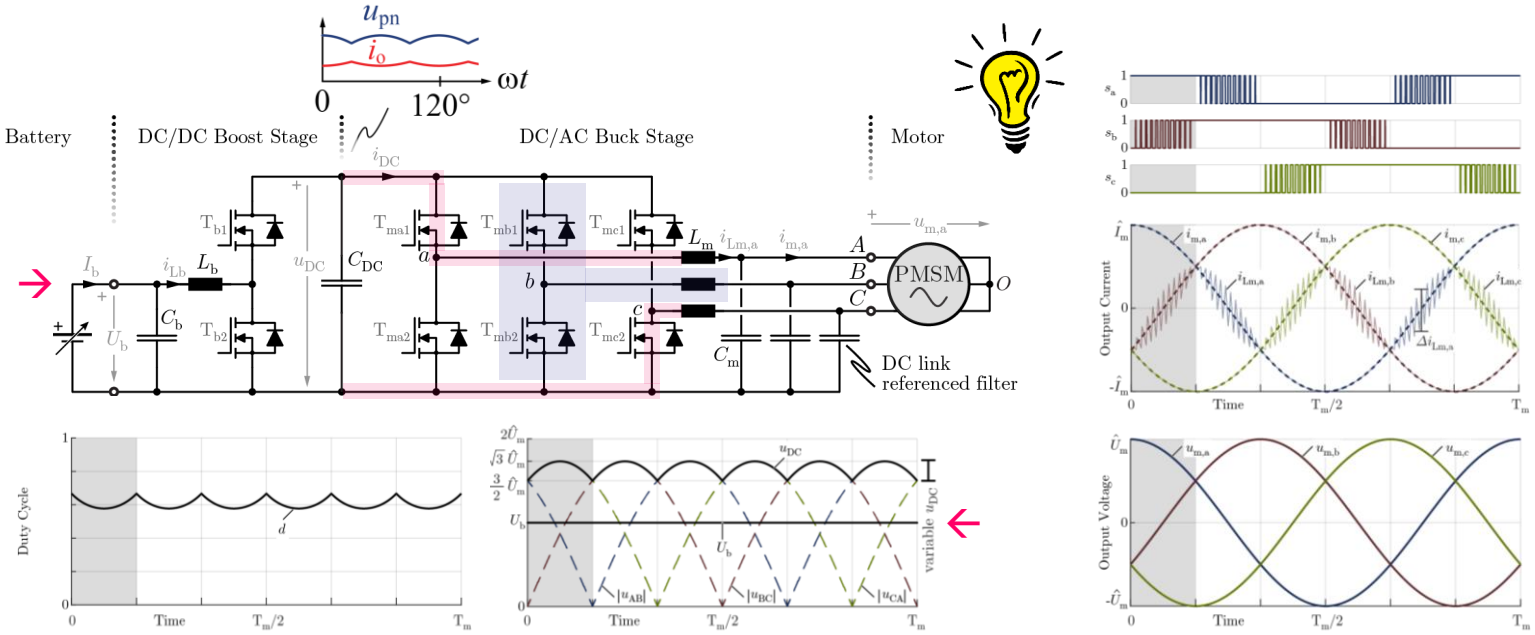


Source: R.W. Erickson et al. / 1986

→ *Analyze Coupling of the Control of Both Converter Stages → "Synergetic Control"*

▶ "Synergetic Control" of Boost-Buck Inverter (1)

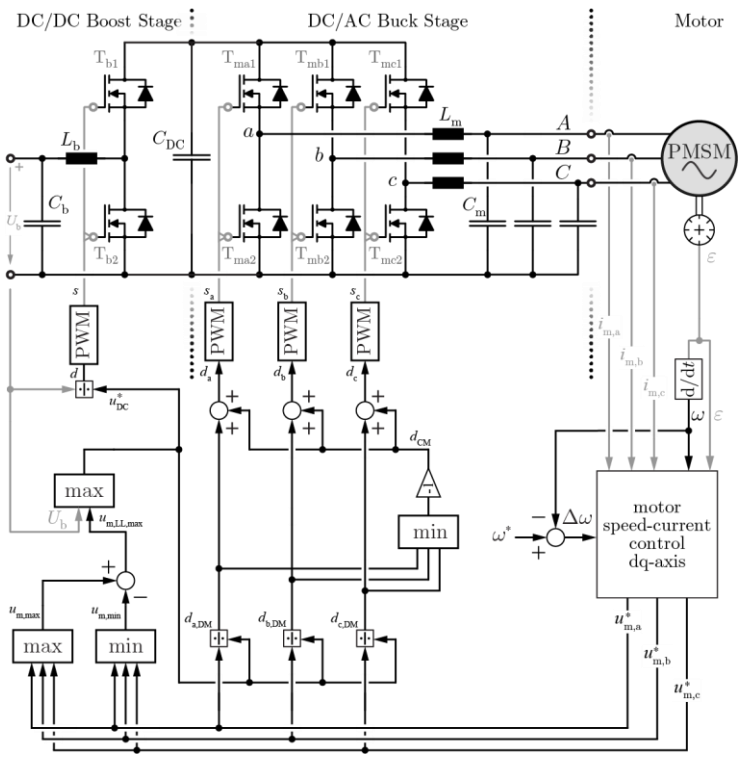
- DC/DC Boost Converter Used for 6-Pulse Shaping of DC-Link Voltage
- 2 (!) Inverter Phases Clamped (1/3 PWM) → Low Switching Losses / High Efficiency
- Conv. PWM Inverter / Clamped Boost-Stage Operation @ Low Speed

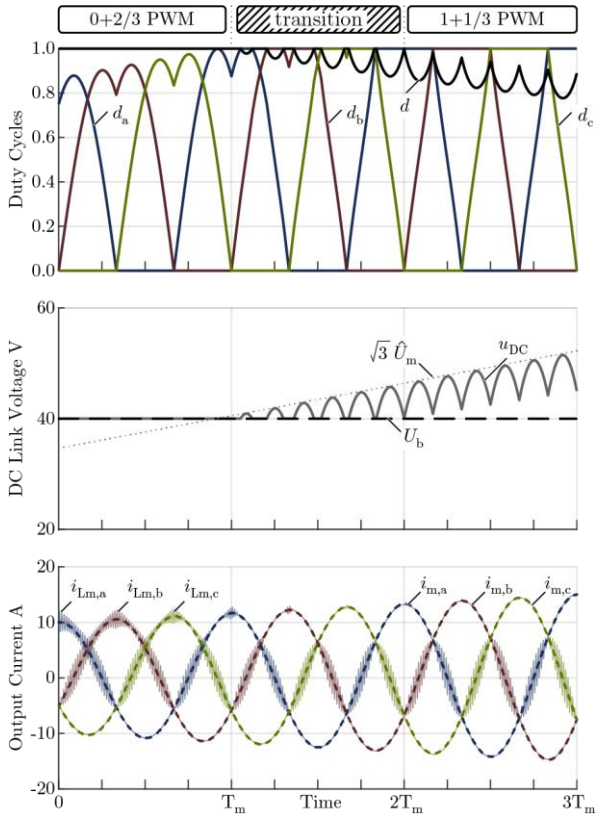


- Preferable for Low-Dynamics Drive Systems

▶ "Synergetic Control" of Boost-Buck Inverter (2)

■ Control Structure & Simulation Results





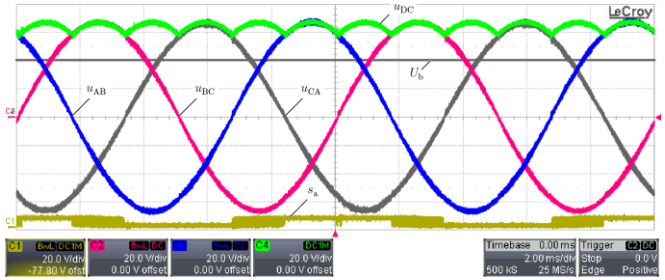
- **Seamless Transition** — Clamped Boost-Stage → Temporary → Full Boost-Stage Operation

▶ "Synergetic Control" of Boost-Buck Inverter (3)

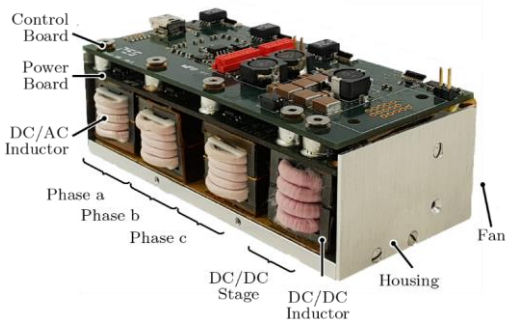
■ Experimental Verification

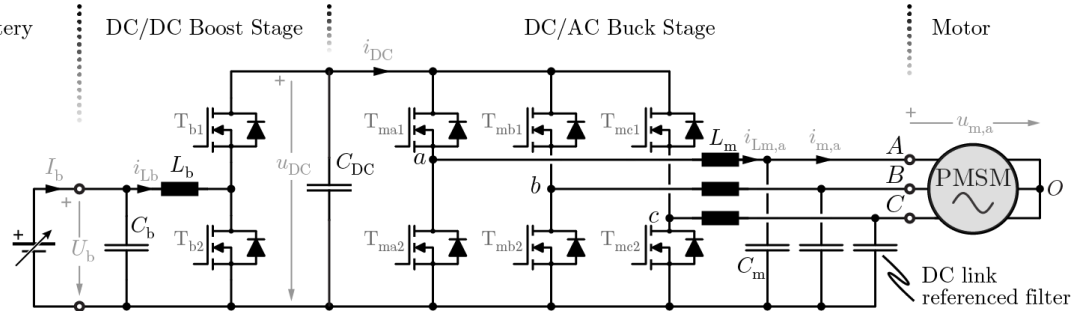
U_b = 40...60V
P = 500W
f_S = 300kHz (200V EPC GaN, 2 per Switch)
f_0 = 5kHz (max.)
M = 0...2 (for U_b=40V)

$$M = \frac{\hat{U}_\mathrm{m}}{\frac{1}{2}U_\mathrm{b}}$$



185cm³ / 11.3in³



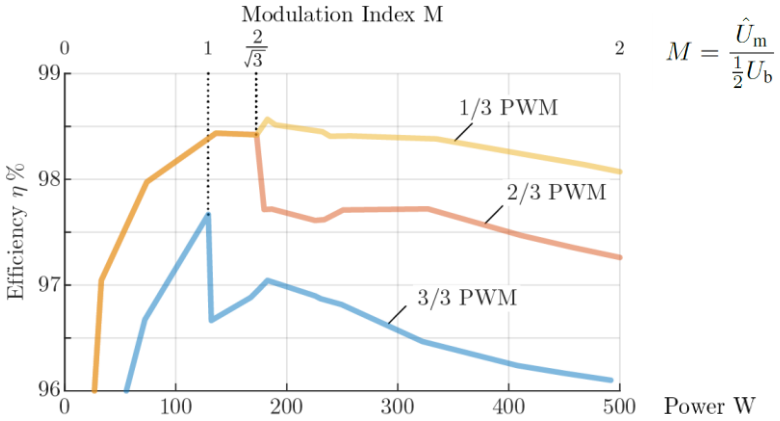


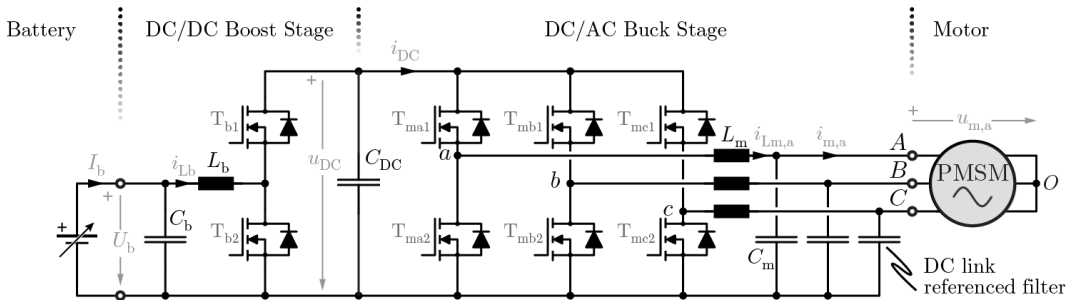
→ Comparison to Conv. U_{DC}=const. Operation (PWM of 2/3 Phases or 3/3 Phases)

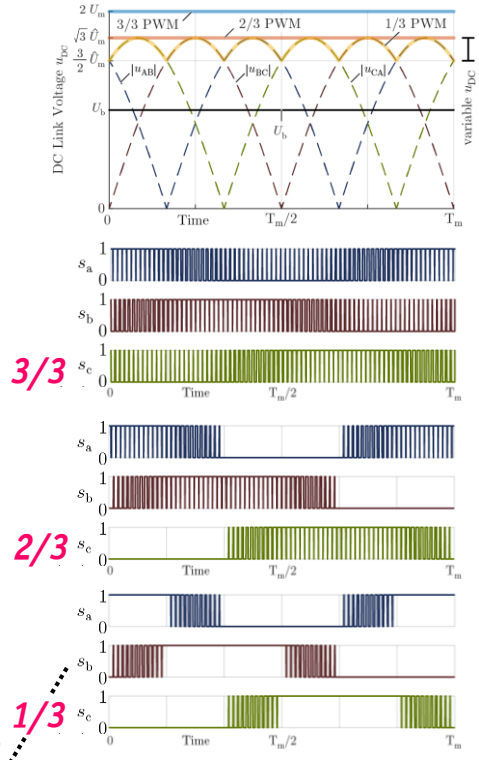
▶ "Synergetic Control" of Boost-Buck Inverter (4)

- *Experimental Verification*

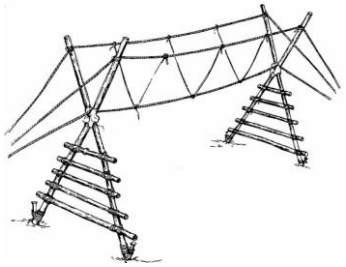
— *Const. DC-Link Voltage & PWM of 3/3 Phases or 2/3 Phases*
— *Synergetic Control = PWM of 1/3 Phases → Substantial Loss Saving (!)*





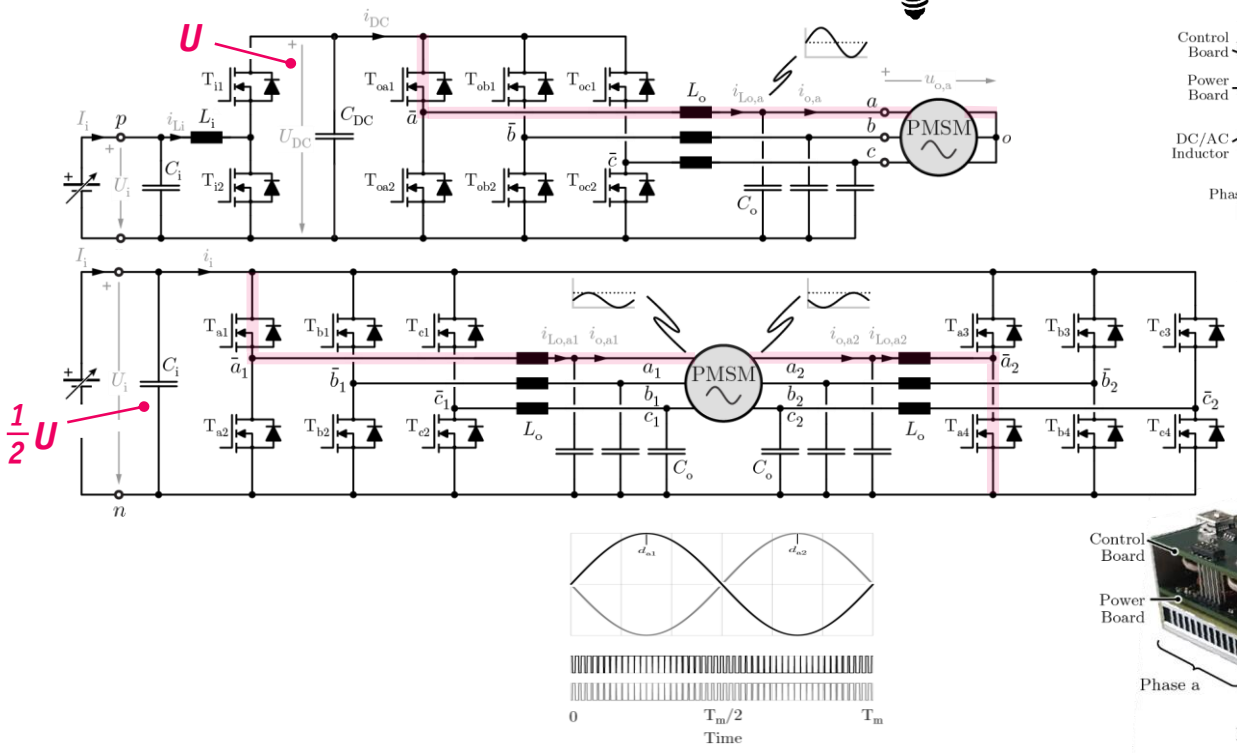


Double-Bridge Inverter

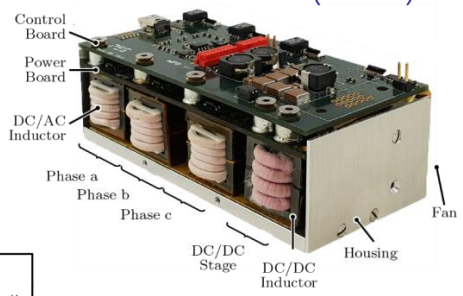


Double-Bridge Inverter (1)

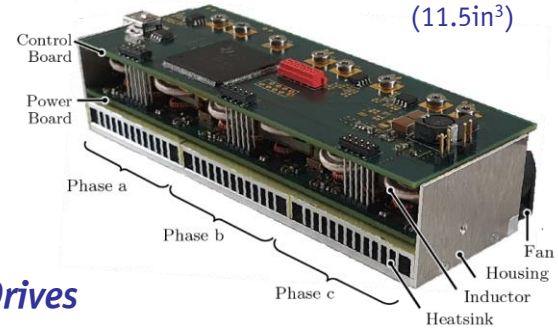
- *Alternative to Front-End DC/DC Converter*
- *Effectively Doubles the DC-Link Voltage (!)*



185cm³ (11.3in³)



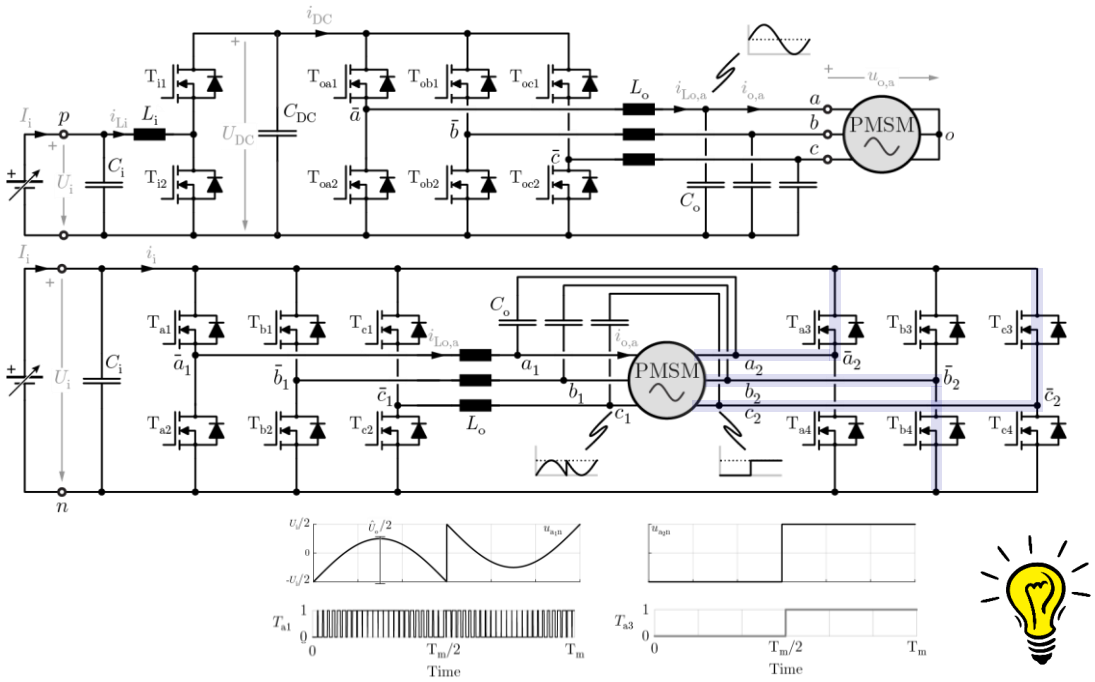
187cm³ (11.5in³)



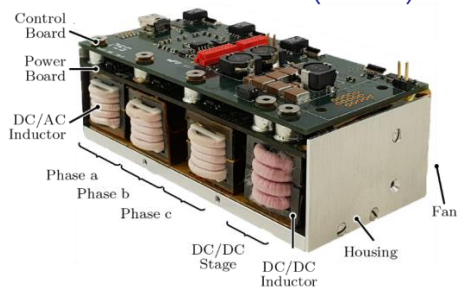
- *Requires Open Winding Motor & Higher Number of Gate Drives*

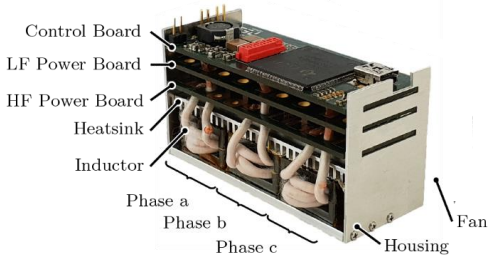
Double-Bridge Inverter (2)

- *2nd Bridge Switching with Output Frequ. → "Unfolder" Operation*
- *Avoids Volume and Losses of Boost Stage → Eff. Single-Stage Conversion*



185cm³ (11.3in³)



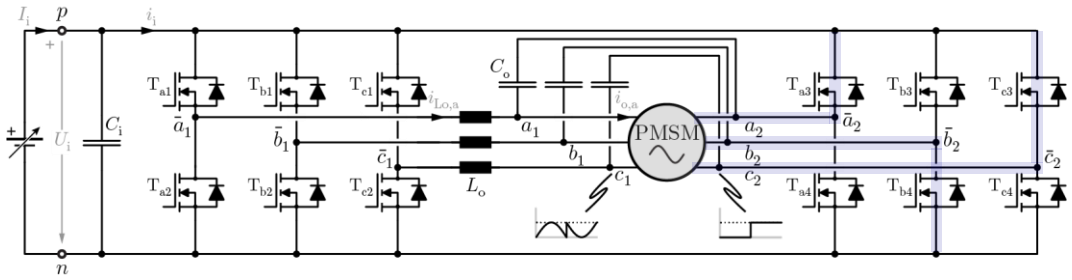


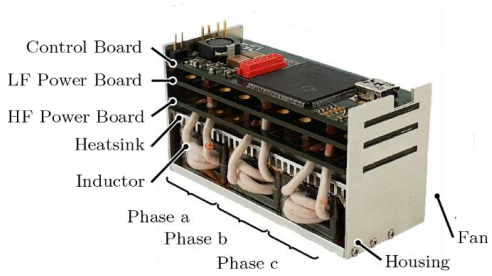
85cm³ (5.2in³)

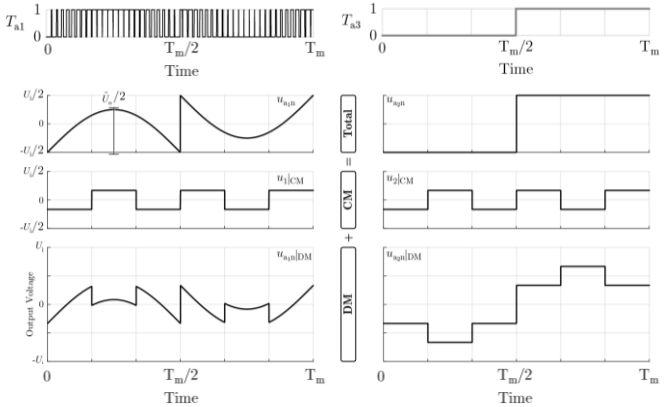
- *Only Three Inductive Components*
- *Requires Open Winding Motor & Higher Number of Gate Drives*

Double-Bridge Inverter (3)

- 2nd Bridge Switching with Output Frequ. → "Unfolder" Operation
- Avoids Volume and Losses of Boost Stage → Eff. Single-Stage Conversion





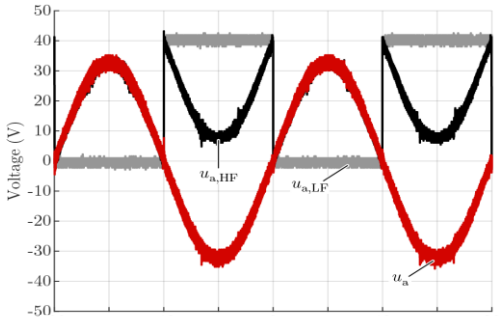


- 6-Pulse Operation of the 2nd Bridge → Motor CM Voltage (Bearing Currents)

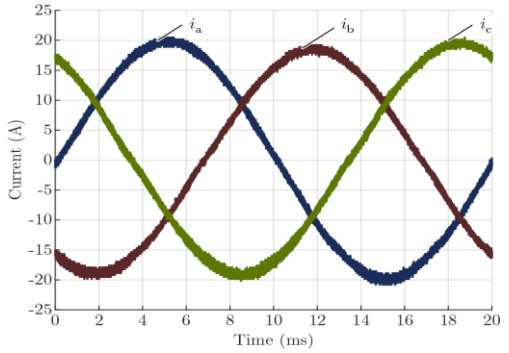
Double-Bridge Inverter (4)

- *Hardware Demonstrator*

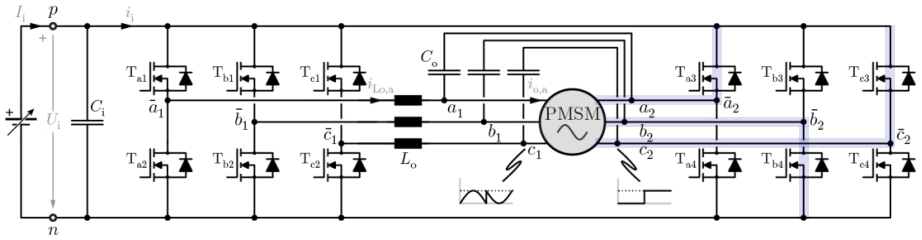
U_b = 40V
P = 1.0kW
f_S = 350kHz (200V EPC GaN, 2 per Switch)
f_0 = 5kHz



Voltages Phase a



Motor Phase Currents



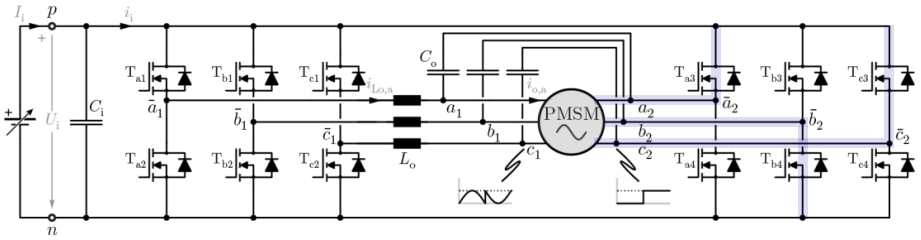
- *6 Winding Terminals → No Problem for Future Motor-Integrated Inverters*

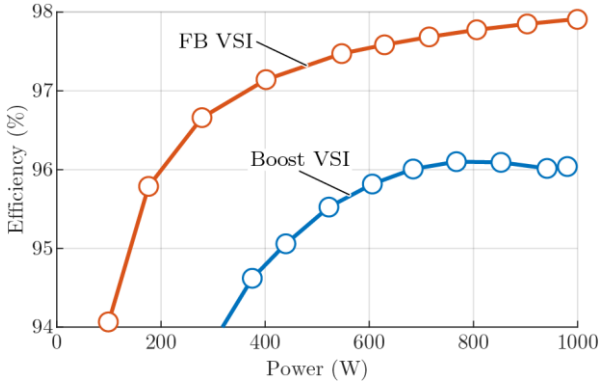
Double-Bridge Inverter (5)

- *Hardware Demonstrator*

U_b = 40V
P = 1.0kW
f_S = 350kHz (200V EPC GaN, 2 per Switch)
f_0 = 5kHz

190 W/in³





- *Single Sw. Stage → No Boost-Stage Losses*
- *6 Winding Terminals → No Problem for Future Motor-Integrated Inverters*

Phase-Modular Topologies

Boost+Buck Modules
Buck+Boost Modules

General Remarks

- *Usually DC-Link Voltage Midpoint Considered as AC Output Ref. Point*
- *Open Machine Starpoint → Introduce CM Voltage Shift → Neg. DC-Rail as Reference*

Source: Cuk (1982)

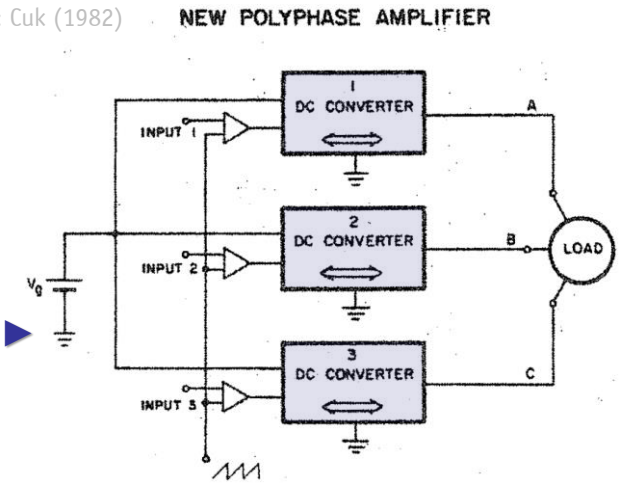


Fig. 7. New three-phase switching amplifier. Three bidirectional dc-dc converters, with their own modulators, driven by a set of three-phase sine waves, constitute three phase voltages around the differential load.

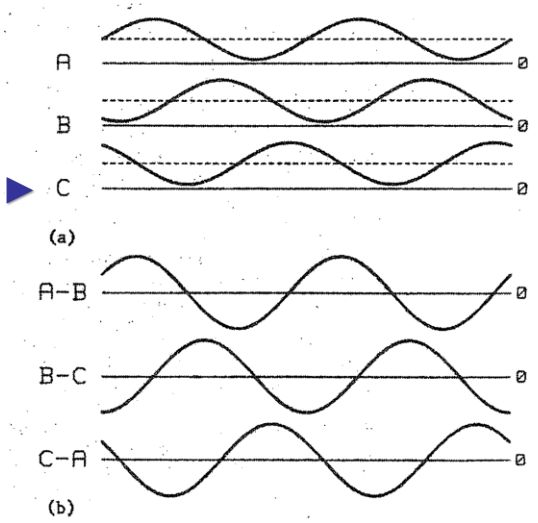
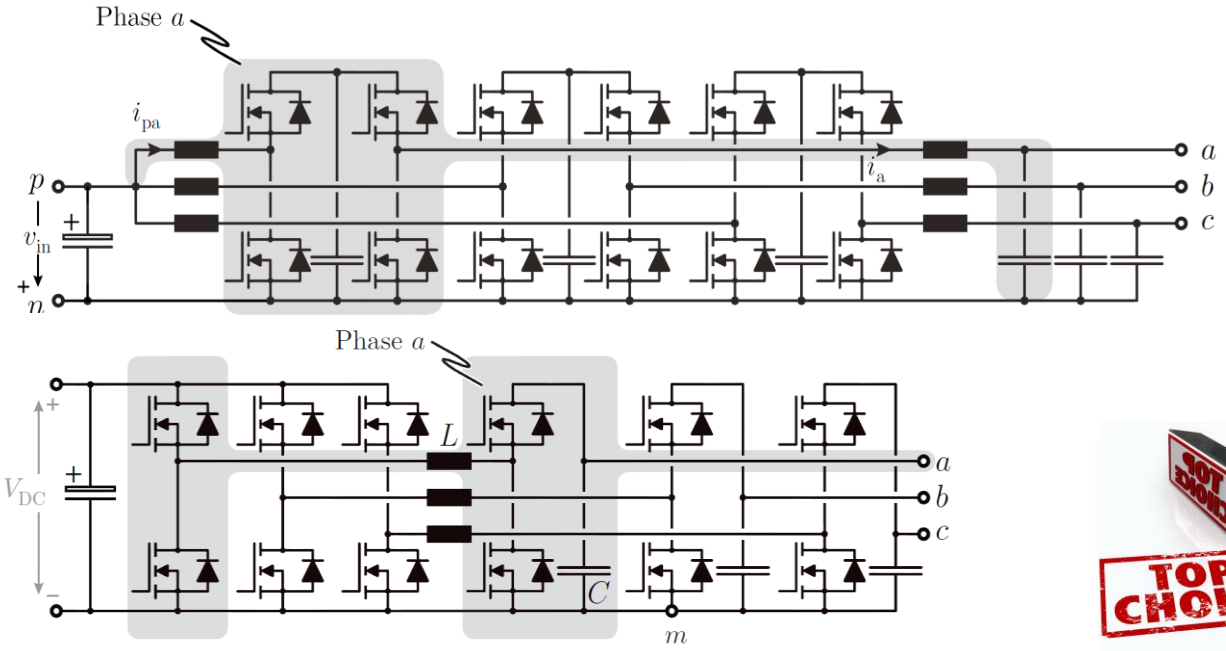


Fig. 8. (a) Line-to-ground and (b) line-to-line voltages generated by the new three phase power amplifier. The dc component of the line-to-ground voltages automatically disappears in line-to-line voltages which are pure ac.

→ *Realization of 3-Φ Inverter Using 3 x DC/DC Converter (Phase) Modules — S. Cuk/1982*

Phase-Modular Boost+Buck / Buck+Boost Inverter

- *Wide Voltage Conv. Range* → *Battery or Fuel-Cell Supply & Adaption to Motor Voltage*
- *Continuous Output Voltage* → *Explicit or Integr. LC Output Filter*

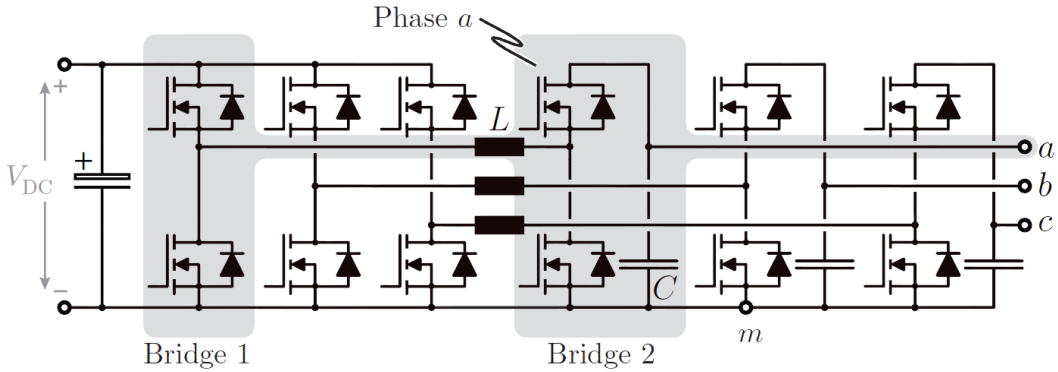


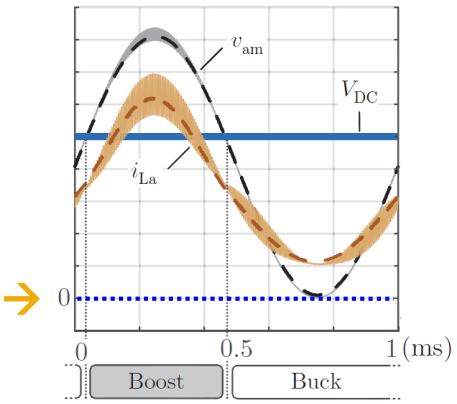
→ *Preference for Low Number of Ind. Components* → *Buck+Boost Concept — "Y-Inverter"*

Y-Inverter Lighthouse Project

- 3-Φ Continuous Output / Low EMI !
- Buck+Boost Operation / Wide Input &/or Output Range
- Standard Bridge-Legs / Building Blocks
- ZVS Operation / High Power Density

- No Shielded Cables / No Insul. Stress
- Industrial Drive
- 1.2kV SiC MOSFETs

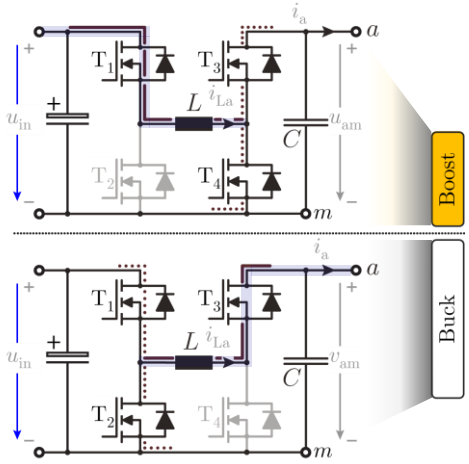


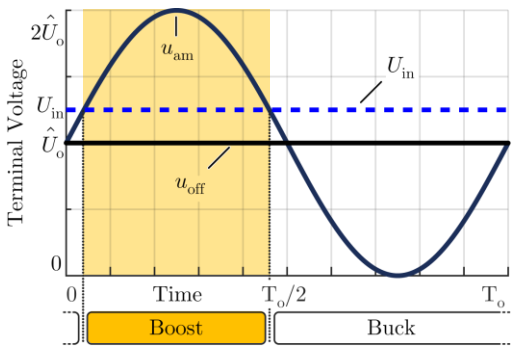


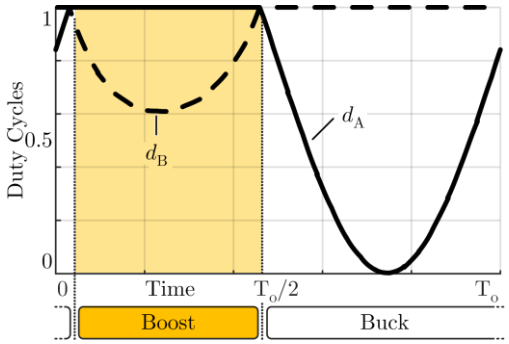
- *Project Scope* → Hardware Demonstrator / Exp. Analysis / Comparative Evaluation

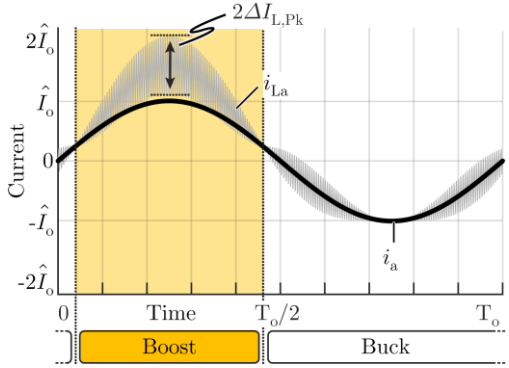
▶ Y-Inverter (1)

- *Operating Behavior*







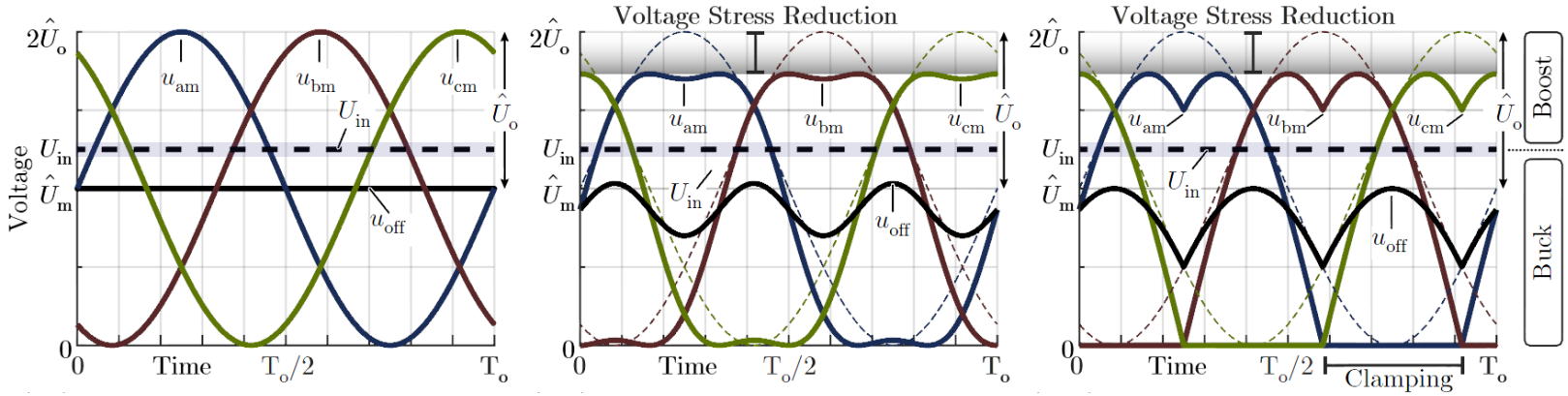


- $u_{am} < U_{in}$ → Buck Operation
- $u_{am} > U_{in}$ → Boost Operation
- Output Voltage Generation Referenced to DC Minus
- *Switch-Mode Operation of Only Buck OR Boost Stage*

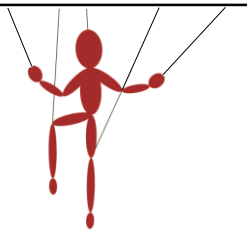
▶ Y-Inverter (2)

- Modulation Scheme

- Continuous Modulation → Opt. DC-Offset of Output Phase Voltages for Low Mod. Index
- Sin. Mod. w/o 3rd Harm. Inj. OR Phase Clamping (DPWM)

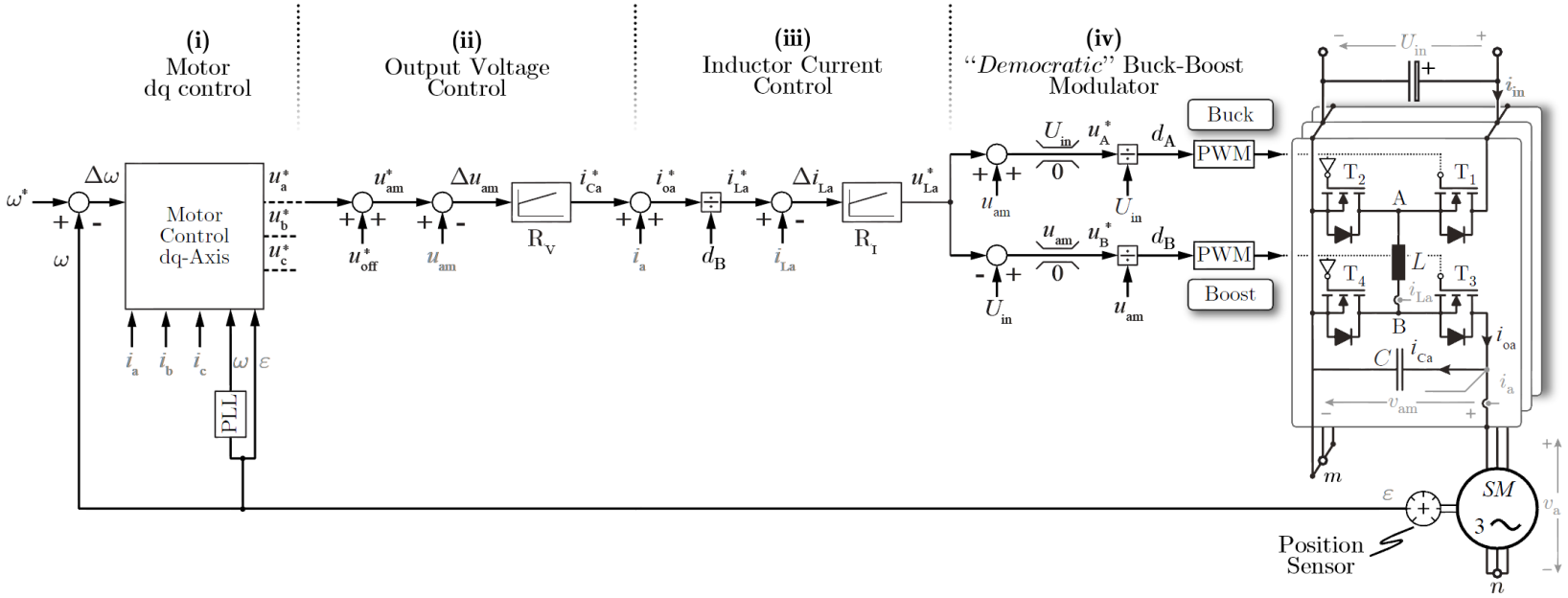


- DPWM → Min. DC-Link Voltage & Low Sw. Losses BUT Unsymm. Curr. Stress on Transistors



▶ Y-Inverter (3)

- *Control Structure*

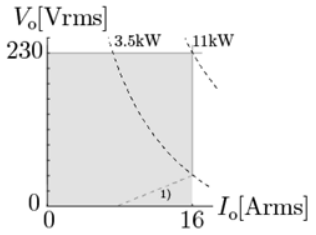


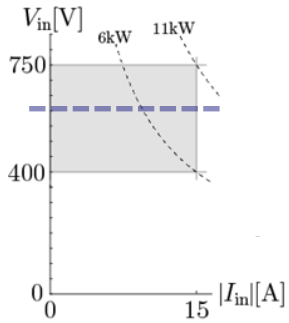
- *"Democratic Control" → Seamless Transition Between Buck & Boost Operation*

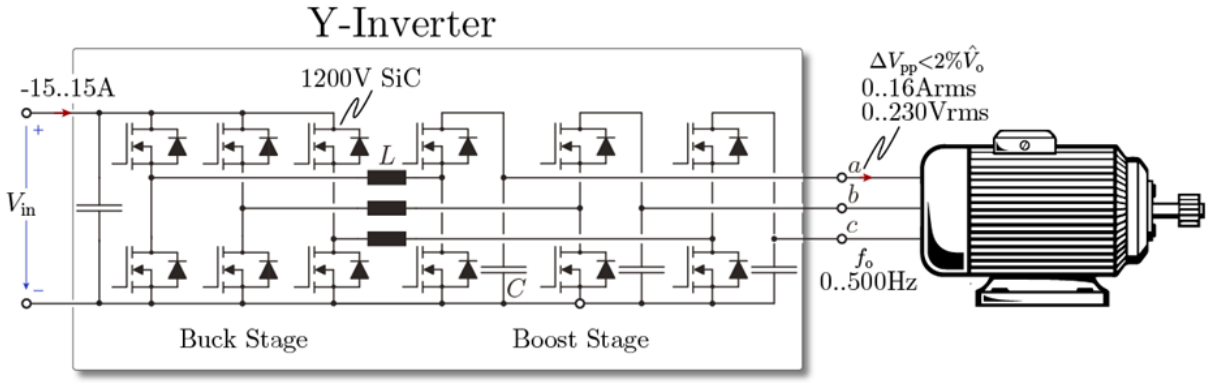
▶ Y-Inverter Prototype (1)

- *Demonstrator Specifications*

- Wide DC Input Voltage Range → 400...750V_{DC}
- Max. Input Current → ± 15A



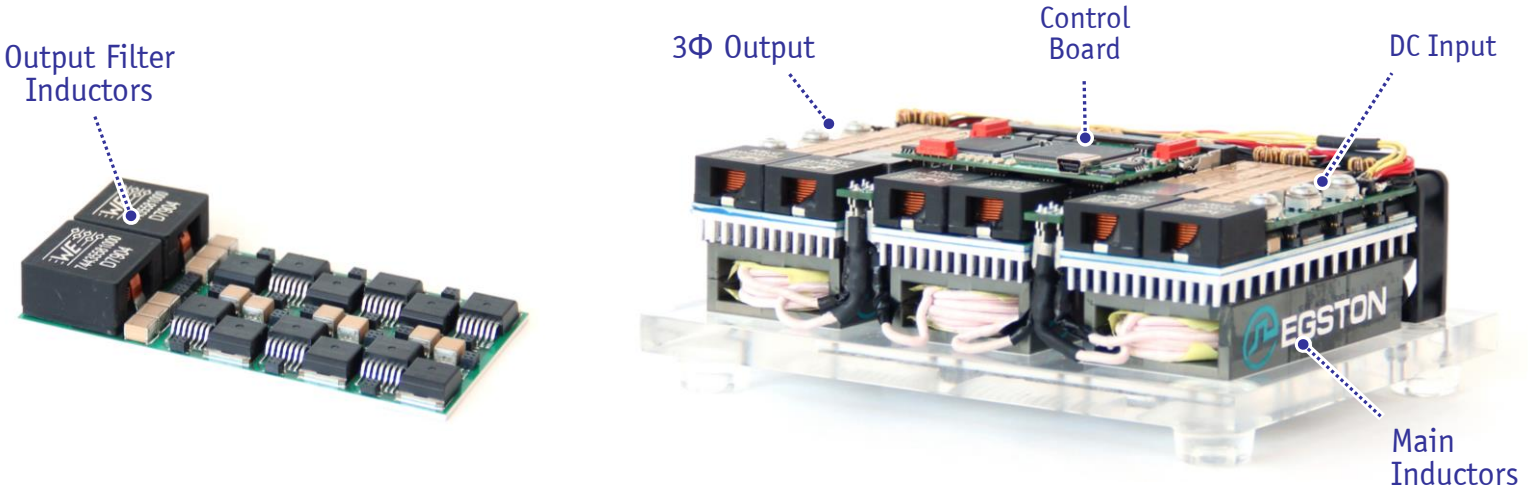




- Max. Output Power → 6...11 kW
- Output Frequency Range → 0...500Hz
- Output Voltage Ripple → 3.2V Peak @ Output of Add. LC-Filter

▶ *Y-Inverter Prototype (2)*

- DC Voltage Range 400...750V_{DC}
- Max. Input Current ± 15A
- Output Voltage 0...230V_{rms} (Phase)
- Output Frequency 0...500Hz
- Sw. Frequency 100kHz
- 3x SiC (75mΩ)/1200V per Switch
- IMS Carrying Buck/Boost-Stage Transistors & Comm. Caps & 2nd Filter Ind.



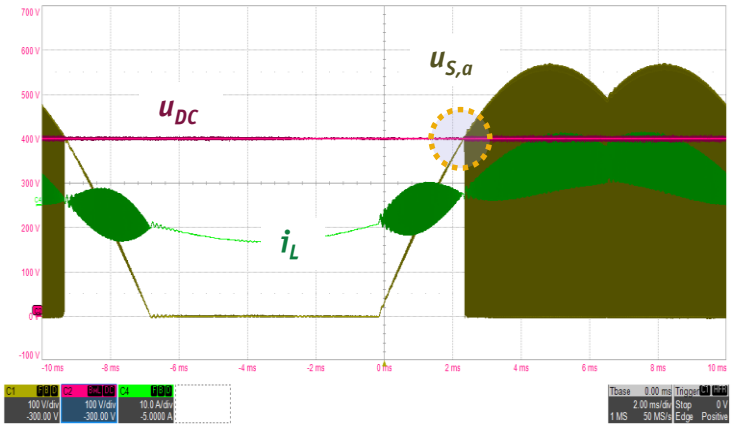
- Dimensions → 160 x 110 x 42 mm^3 (15kW/dm^3, 245W/in^3)

▶ Measurement Results (1)

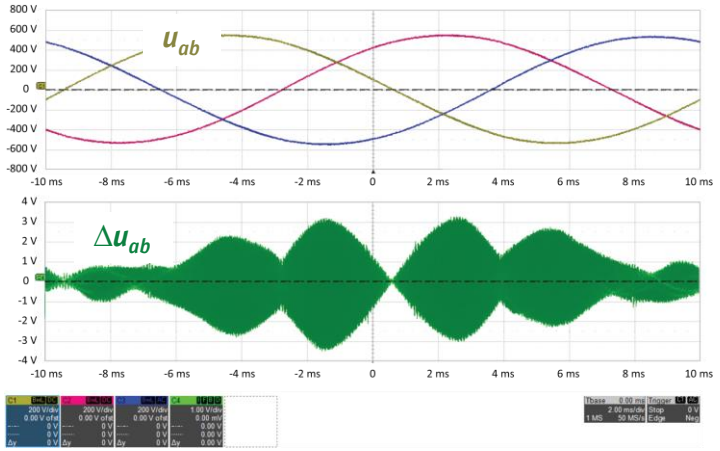
- *Stationary Operation*

U_{DC}= 400V
U_{AC}= $400V_{rms}$ (Motor Line-to-Line Voltage)
f_O = 50Hz
f_S = 100kHz / DPWM
P = 6.5kW

100V/div
10A/div



200V/div
1V/div



→ *Line-to-Line Output Voltage Ripple < 3.2V*

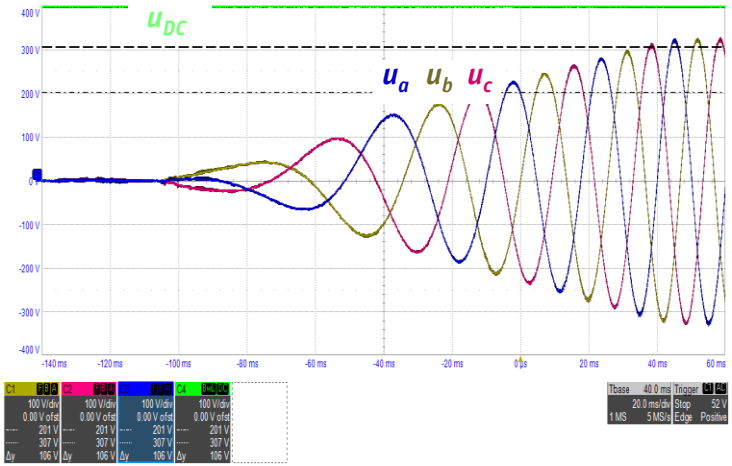
Measurement Results (2)

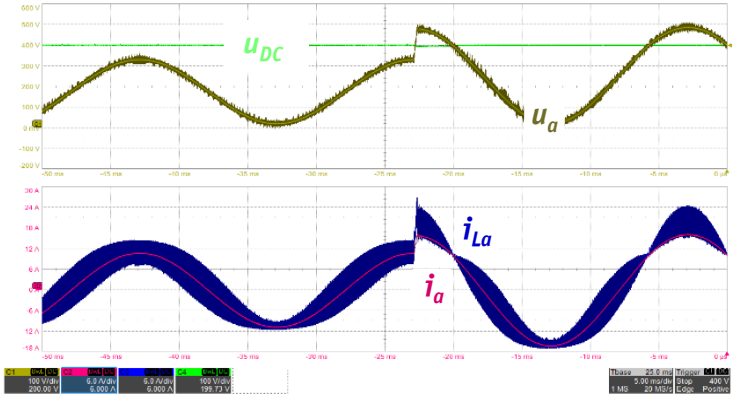
- *Transient Operation*

U_{DC}= 400V
U_{AC}= $400V_{rms}$ (Motor Line-to-Line Voltage)
f_O = 50Hz
f_S = 100kHz / DPWM
P = 6.5kW

100V/div
100V/div
6A/div
6A/div

100V/div

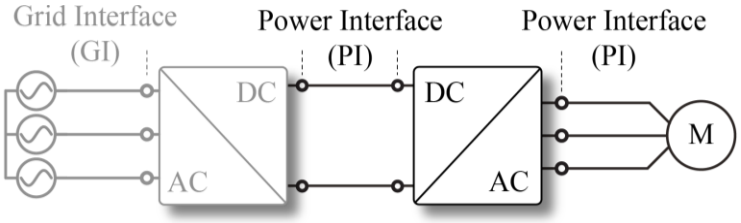


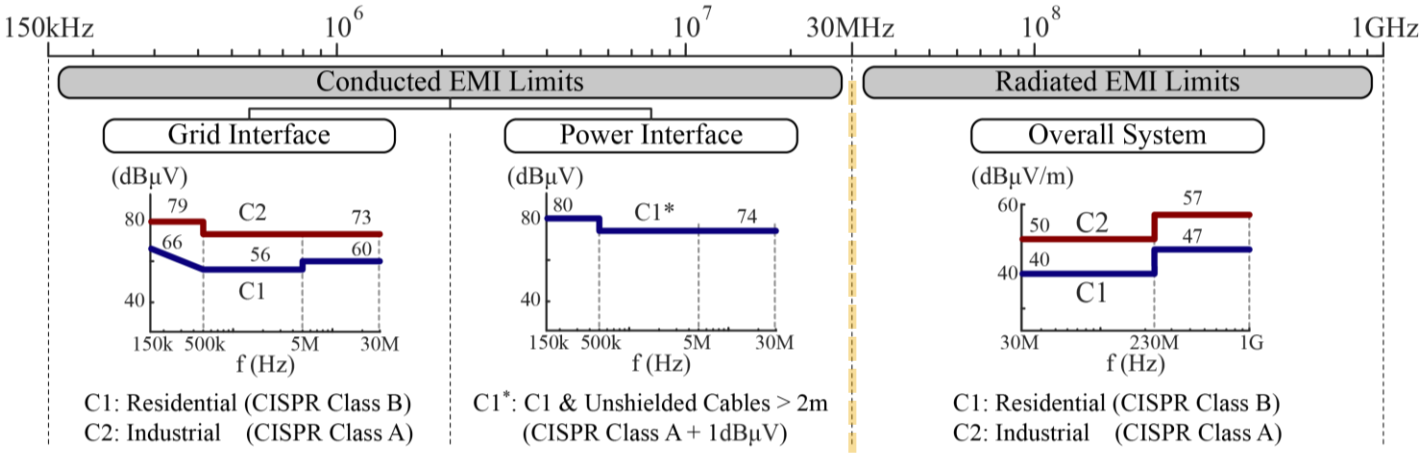


- *Dynamic Behavior V-f Control and Load-Step*

▶ EMI-Limits (VSD Product Standard)

- IEC 61800-3 → Product Standard for Variable-Speed Motor Drives
- EMI Emission Limits → Grid Interface (GI) and Power Interface (PI)
- Application → Residential (C1) or Industrial (C2)

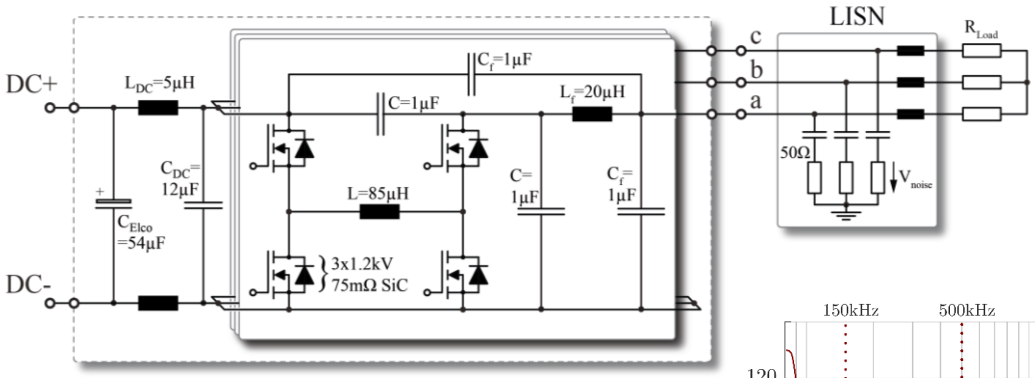


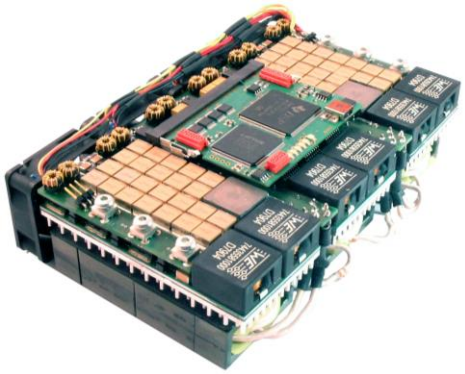


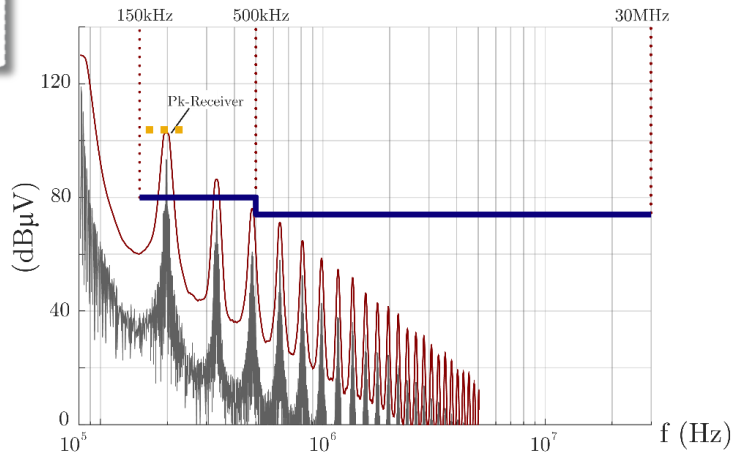
■ *EMI-Filter Design for Unshielded Cables > 2m and Resid. Applications (Cond. & Rad.)*

Conducted EMI-Filter Design (1)

- Calculation of Conducted EMI w/o EMI-Filter (@ f_{out} = 50Hz)



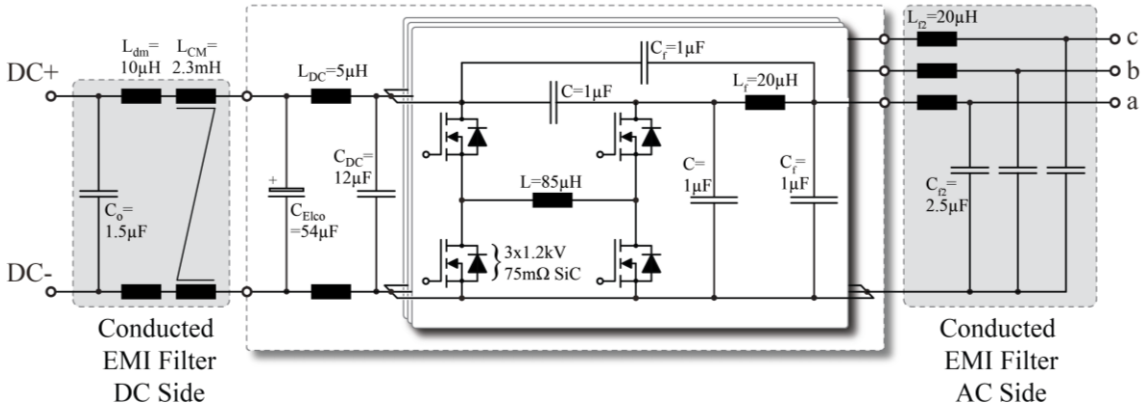


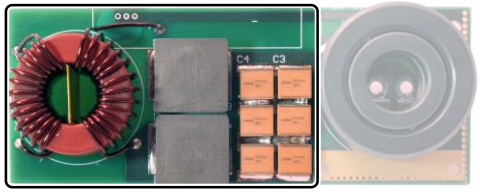


→ >30dB Attenuation @ 200kHz ($2f_s$) Needed
→ Additional Single-Stage EMI-Filter for Conducted EMI Compliance

▶ Conducted EMI-Filter Design (2)

- Separate Cond. DM & CM EMI-Filter on DC-Side & DC-Minus Ref. EMI-Filter on AC-Side





L_{CM} L_{DM} $C_{DM} = C_0$

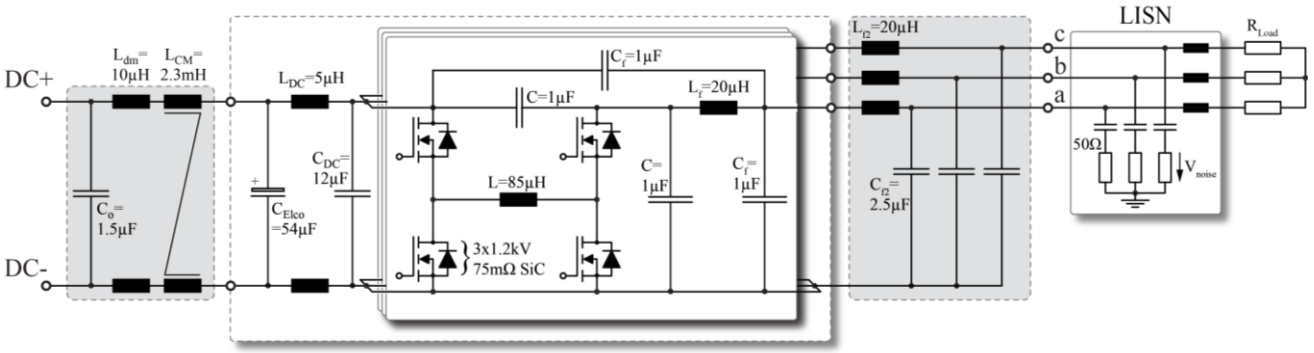
C_{f2} (on the back)

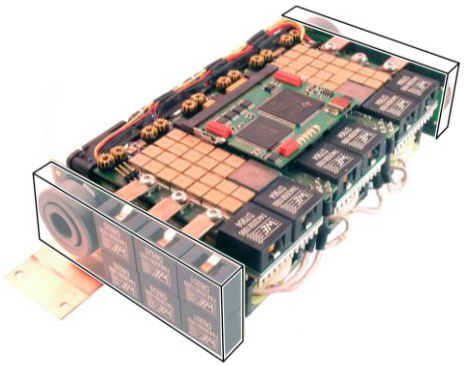
L_{f2}

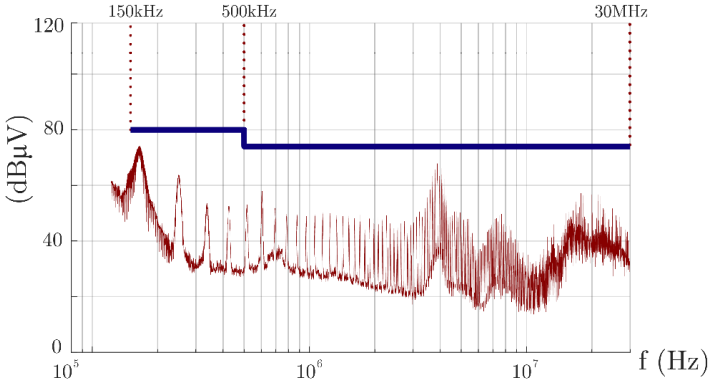
→ *Low Add. EMI Filter Volume — 74cm³ for Each Filter (incl. Toroid. Rad. EMI Filter)*
→ *Total Power Density Reduces — 15kW/dm³ (740cm³) → 12kW/dm³ (890cm³)*

Experimental Results - Conducted EMI

- Measurements of the Cond. EMI Noise on the AC-Side (QP, with 50Hz AC-LISN)



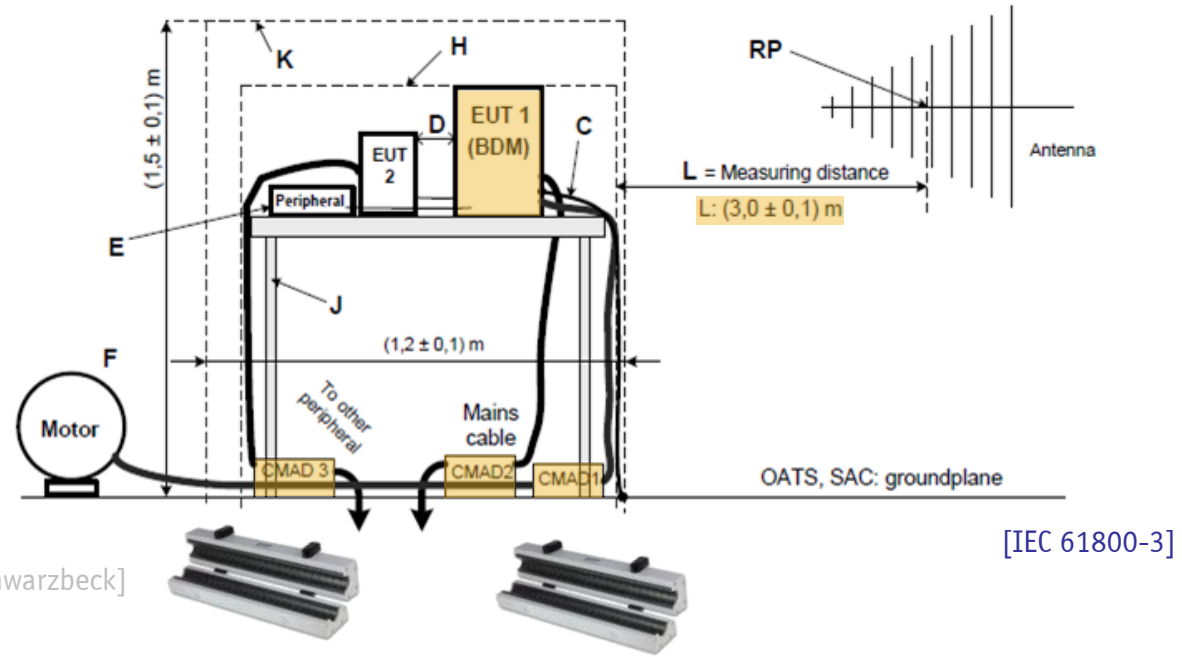




→ *Small 80uH CM-Ind. Added on AC-Side - (3cm³ of Add. Volume = 0.5% of Converter Vol.)*
→ *Conducted EMI with Unshielded Motor Cable Fulfilled*

▶ *Measurement of Radiated EMI-Noise (1)*

- Equipment Under Test (EUT) Placed on Wooden Table with Specified Arrangement
- CM Absorption Devices (CMAD) Terminate All Cables on AC- & DC-Side (Total $l_{cable} \approx 1.5$m)
- Measurement of Radiated Noise with Antenna in 3m Distance



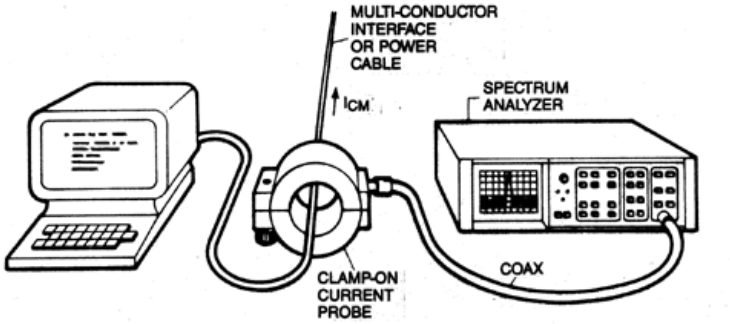
[IEC 61800-3]

[Schwarzbeck]

- *Either Open-Area Test Site (OATS) or Special Semi-Anechoic Chamber (SAC) Needed*
- *Alternative Pre-Compliance Measurement Method*

▶ Measurement of Radiated EMI-Noise (2)

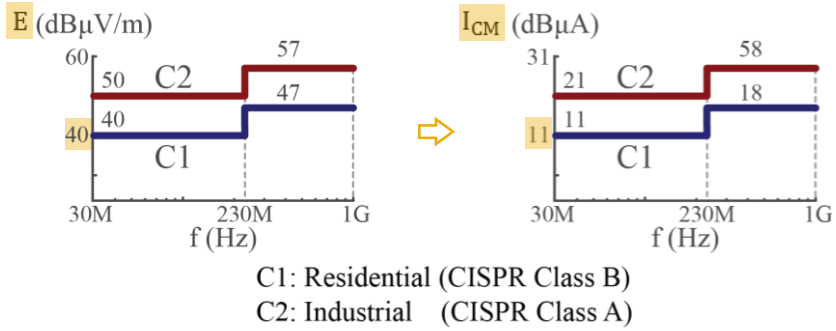
- CM-Currents NOT Returning IN THE CABLE are Dominant Source of Radiation
- Relation Between Radiated Electric Field and CM-Currents (!)



$$E = \begin{cases} \dfrac{\mu_0 \cdot f \cdot l_{cable} \cdot I_{cm}}{r} & \dfrac{\lambda}{4} \leq l_{cable} \\ \dfrac{\mu_0 \cdot \frac{c_0}{4} \cdot I_{cm}}{r} & \dfrac{\lambda}{4} > l_{cable} \end{cases}$$

[Electromagnetic Compatibility Engineering, H. Ott]

[Fischer FCC F-33-1]
up to 250MHz
Z_{nom} = 6.3Ω

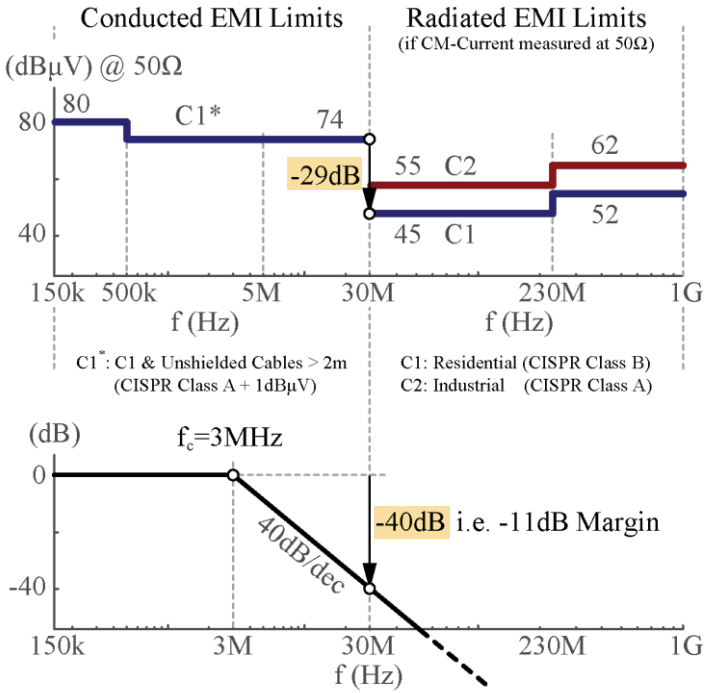


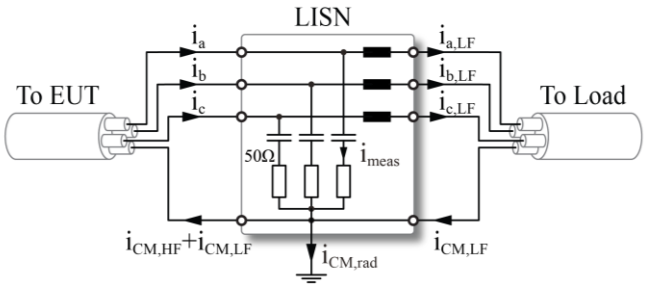
C1: Residential (CISPR Class B)
C2: Industrial (CISPR Class A)

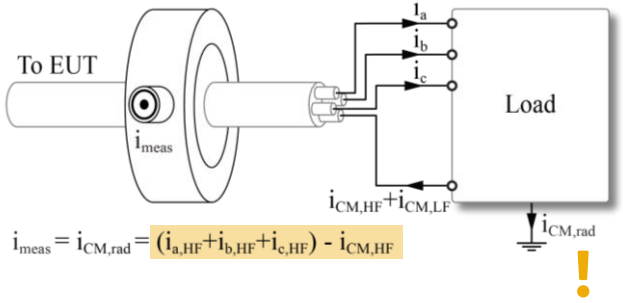
- *Max. Allow. El. Field Strength of 40dBuV/m → Max. CM-Current of 3.5uA (11dBuA)*
- *Current Probe Impedance of 6.3Ω (F-33-1) → Max. Noise Volt. of 26dBuV @ Test Receiver*

Radiated EMI-Filter Design (1)

- High Frequ. CM-Filter Needed to Limit Radiated EMI, i.e. CM-Currents < 3.5uA for f > 30MHz
- Radiated EMI @ 30MHz Still Measureable with LISN, i.e. 3.5uA @ 50Ω = 45dBµV



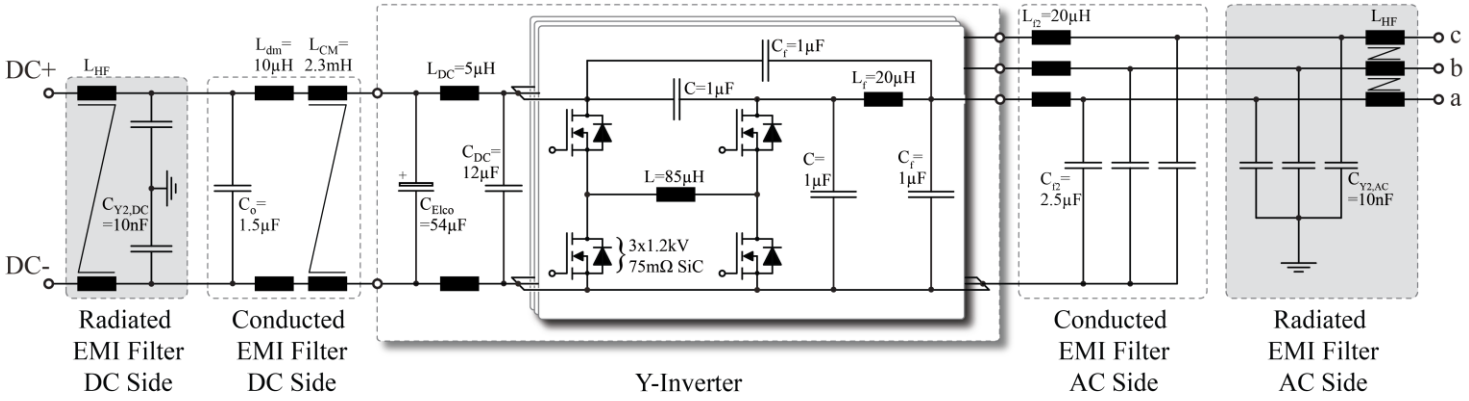


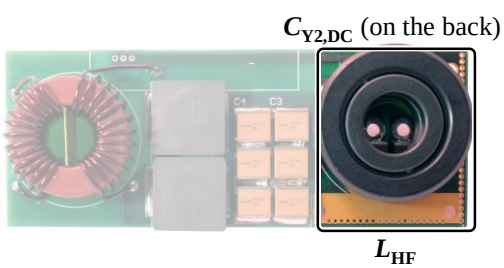


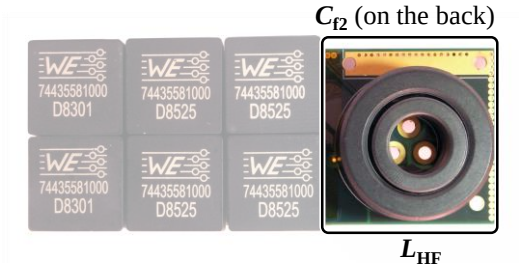
- *Assume Worst-Case CM-Noise of 74dBuV @ 30MHz* → *Attenuation of -29dB Needed*
- *Considering Additional Attenuation Margin* → *Cut-Off Freq. Below 3MHz*

Radiated EMI-Filter Design (2)

- Single-Stage HF CM-Filter on DC-Side and AC-Side
- Plug-On CM-Cores (NiZn-Ferrites) → Low Parasitics & Good HF-Att. up to 1GHz



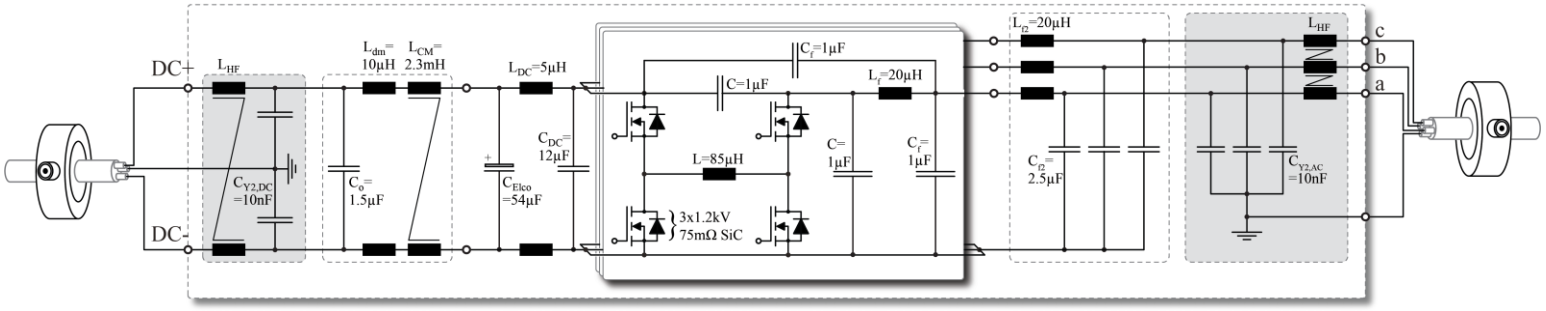


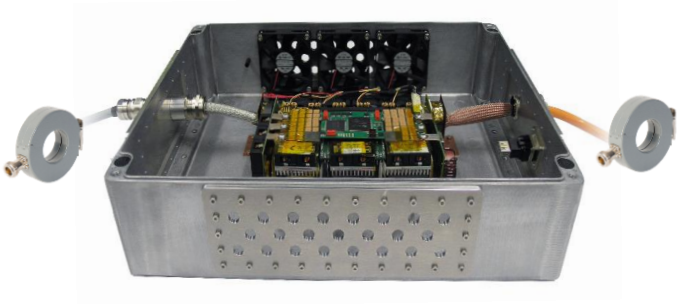


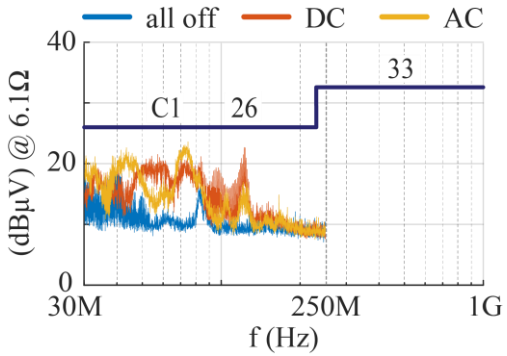
→ *Additional EMI Filter Volume Already Considered with Conducted EMI Filter*
→ *Total Power Density Slightly Reduces — 15kW/dm³ → 12kW/dm³*

▶ Experimental Results - Radiated EMI

- Y-Inverter Placed in Metallic Enclosure → Emulate Housing, but UNshielded Cables (!)
- Measurement Setup → According IEC 61800-3
- Alternative Measurement Principle → Conducted CM-Current Instead of Radiation





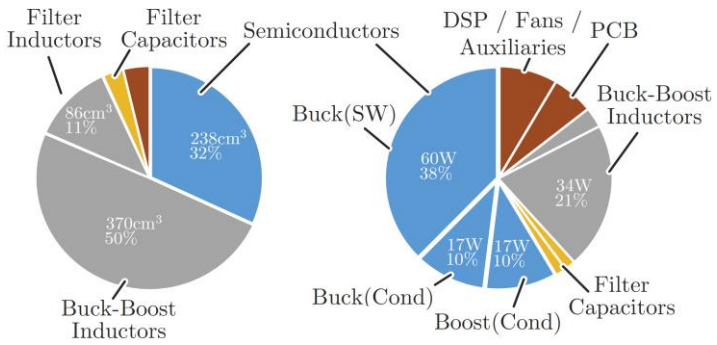


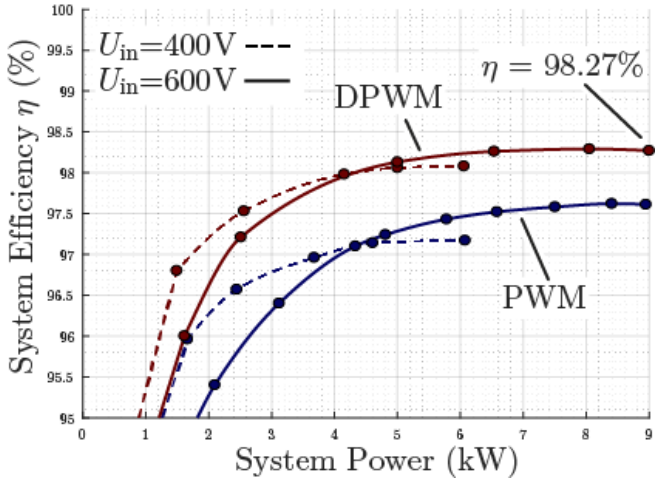
→ *Already Noticeable Noise Floor*
→ *HF-Emissions Well Below Equivalent EMI-Limit* → *Next Step: Verification Using Antenna*

▶ Efficiency Measurements

- *Dependency on Input Voltage & Output Power Level*

U_{DC}= 400V / 600V
U_{AC}= 230V_{rms} (Motor Phase-Voltage)
f_S = 100kHz

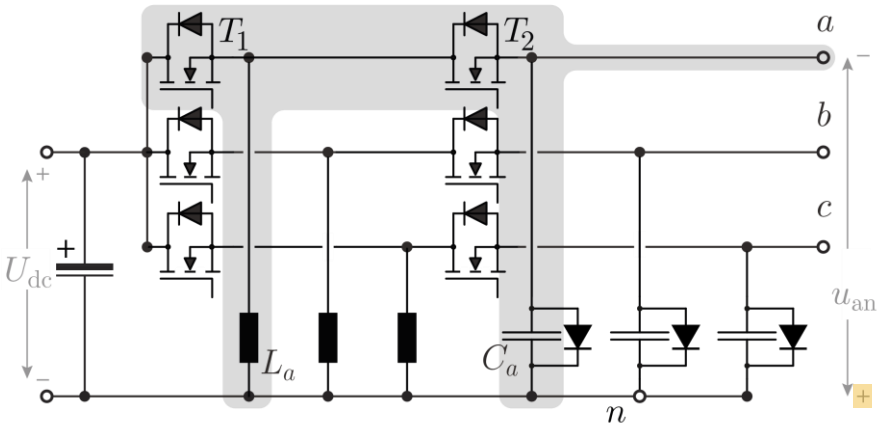




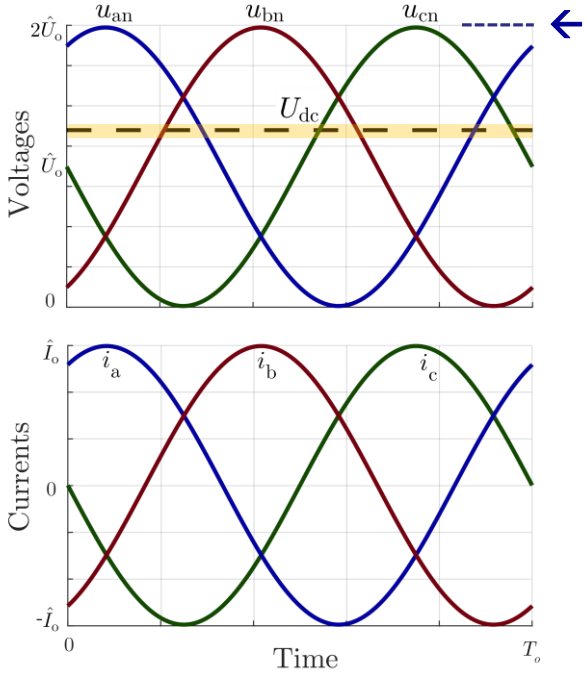
→ *Multi-Level Bridge-Leg Structure for Increase of Power Density @ Same Efficiency*

Alternative Topology (1)

- Phase Modules Based on 2-Switch Inverting Buck+Boost Topology
- Cont. Sinusoidal PWM OR Discontinuous PWM (DPWM)



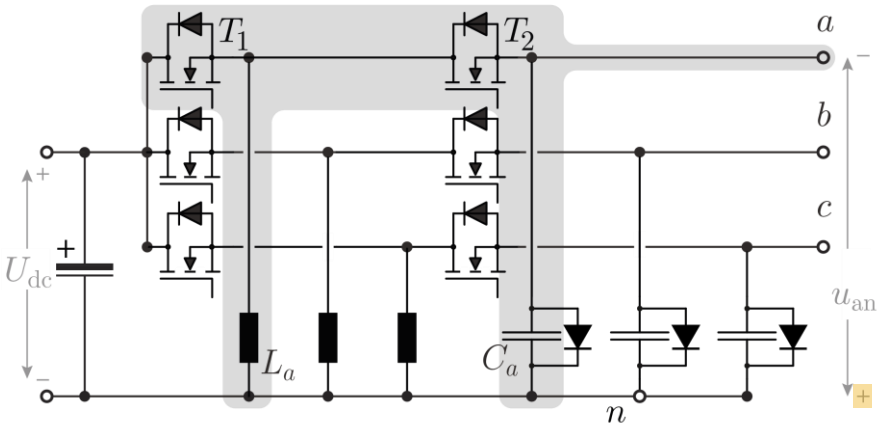
$$d_a = \frac{|u_{an}|}{|u_{an}| + U_{dc}}$$



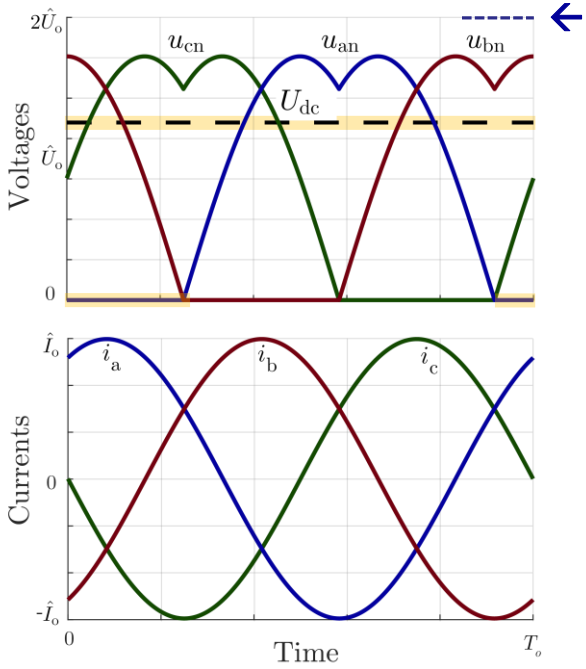
- Single-Stage Energy Conversion
- Lower # of Switches Comp. to Y-Inv. / Higher Comp. Stresses → Low Power Applications

Alternative Topology (2)

- Phase Modules Based on 2-Switch Inverting Buck+Boost Topology
- Freewheeling Diodes Preventing Oscillations @ DPWM Clamping



$$d_a = \frac{|u_{an}|}{|u_{an}| + U_{dc}}$$



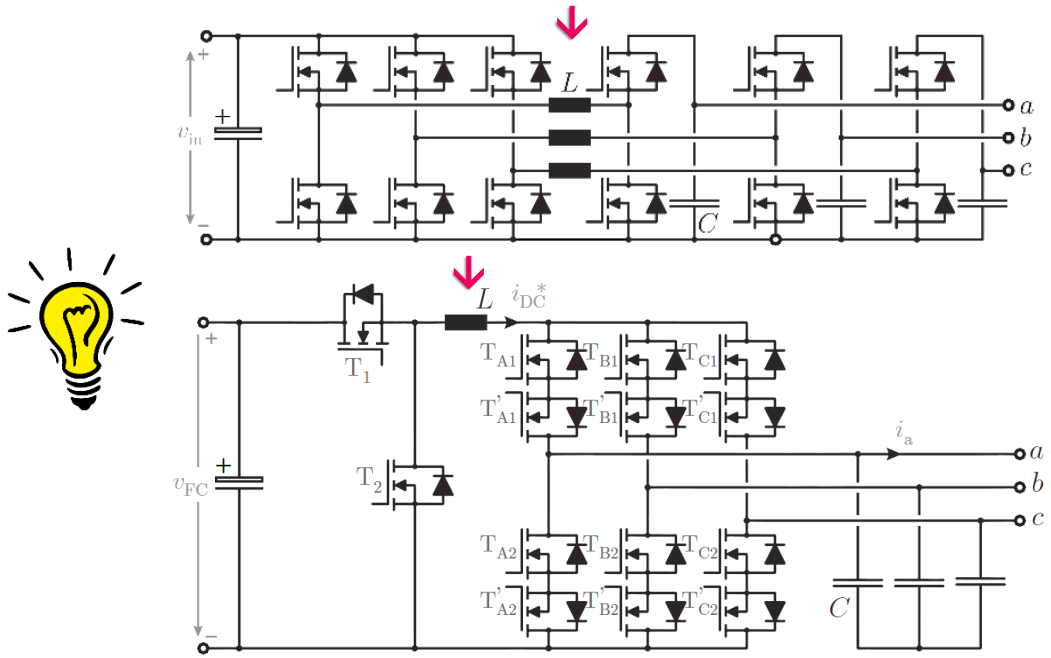
- Single-Stage Energy Conversion
- Discontinuous PWM → Reduced Switching Losses

DC/DC Buck-Stage & Current Source Inverter

Monolithic Bidir. GaN Switches
Synergetic Control

Current Source Inverter (CSI) Topologies

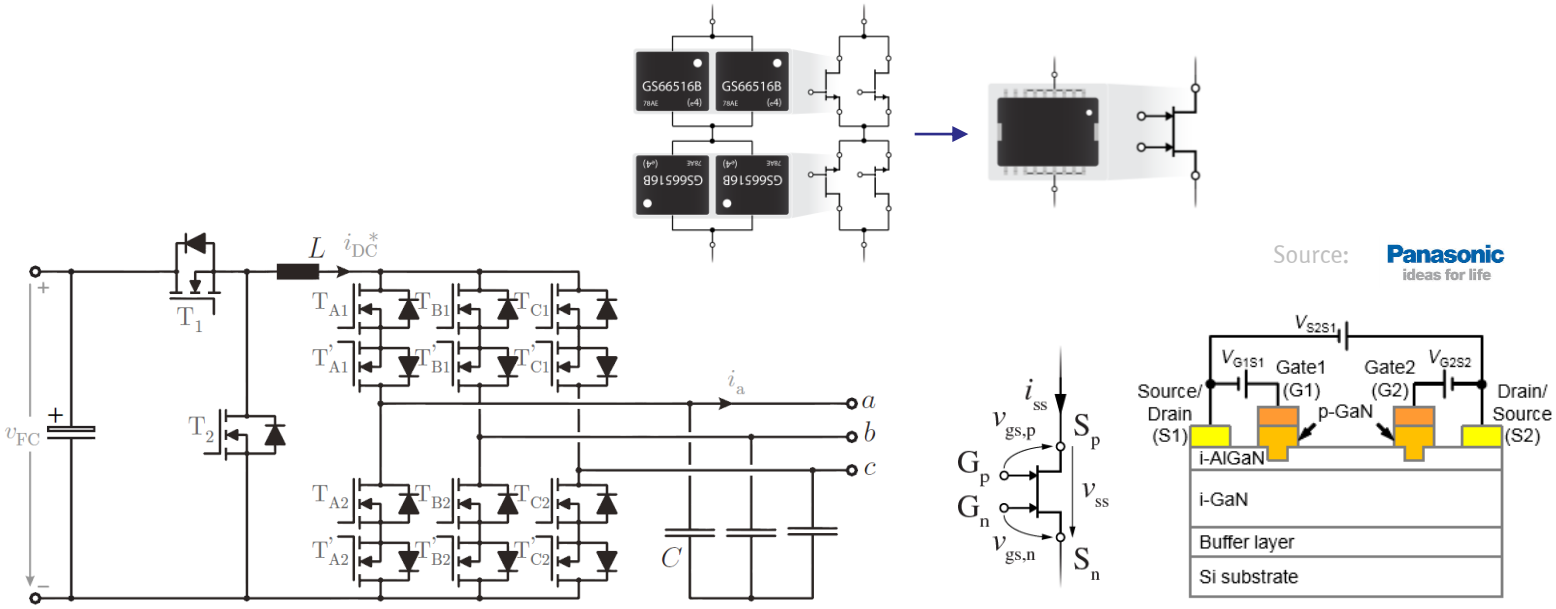
- *Phase Modular Concept → Y-Inverter (Buck-Stage / Current Link / Boost-Stage)*
- *3-Φ Integrated Concept → Buck-Stage & Current DC-Link Inverter*



→ *Low Number of Ind. Components & Utilization of Bidir. GaN Semicond. Technology*

▶ 3-Φ Integrated Buck-Boost CSI (1)

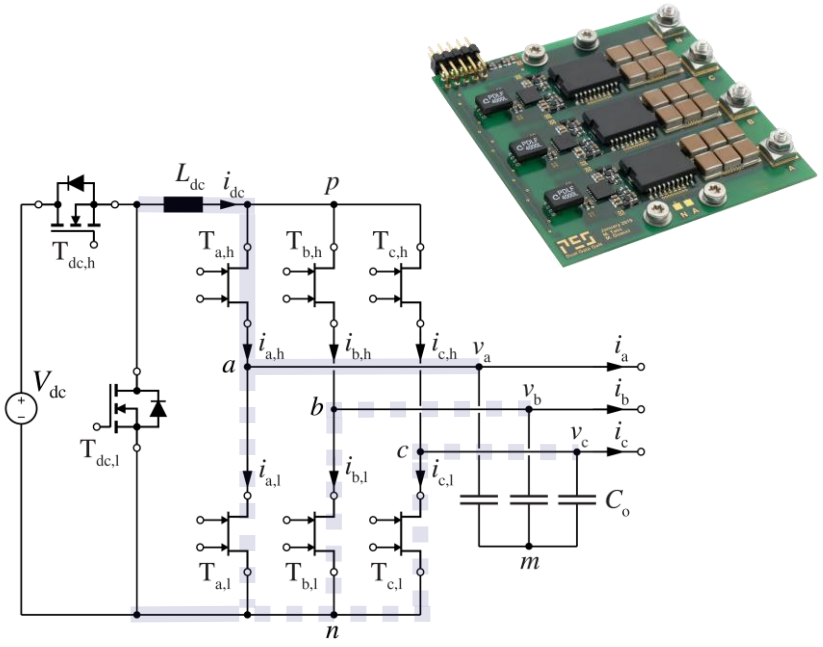
- Basic Topology Proposed in 1984 (Ph.D. Thesis of K.D.T. Ngo/CPES)
- Bidir./Bipolar Switches → Positive DC-Side Voltage for Both Directions of Power Flow

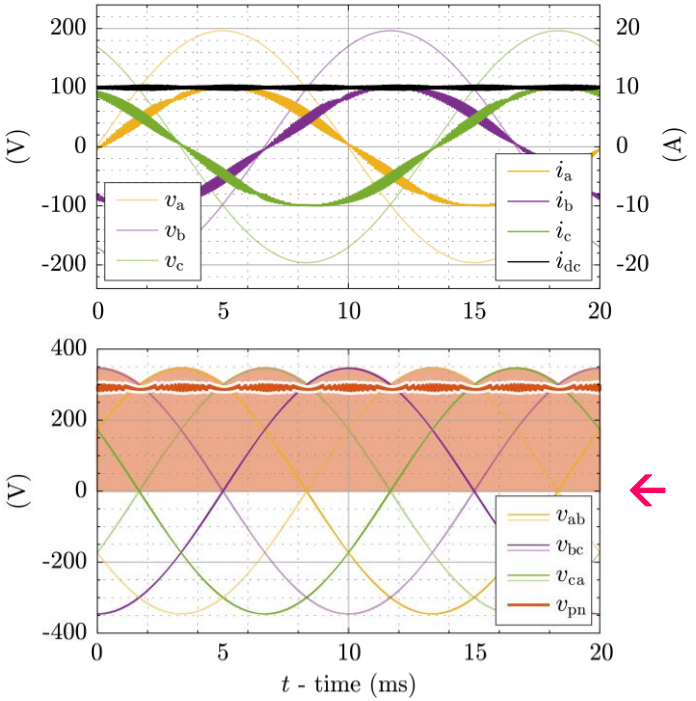


→ Monol. GaN Switches → Factor 4 Improvement in Chip Area Comp. to Discrete Realiz.
→ Also Beneficial for Matrix Converter Topologies

▶ 3-Φ Integrated Buck-Boost CSI (2)

- Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates / Full Controllability
- Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control

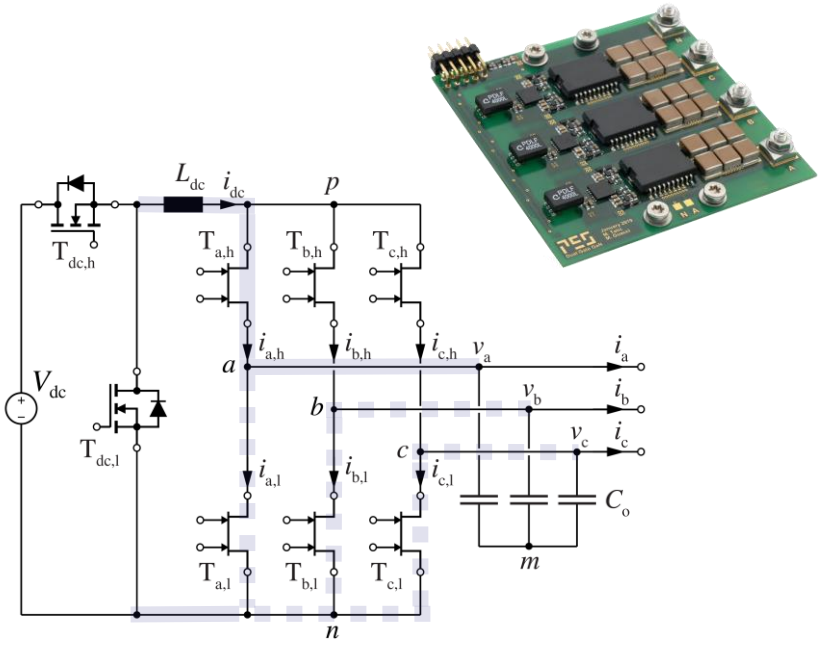


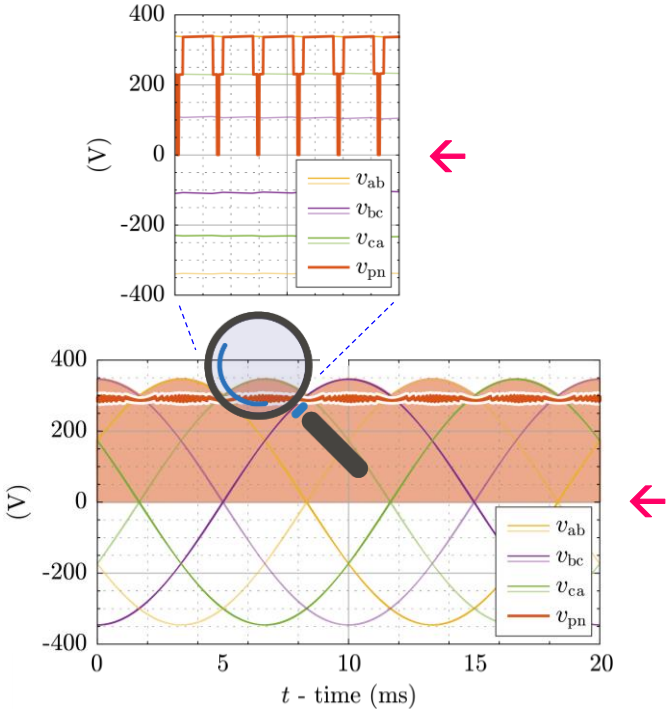


- Conventional Control of Inverter Stage → Switching of All 3 Phase Legs (3/3)

▶ 3-Φ Integrated Buck-Boost CSI (3)

- Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates / Full Controllability
- Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control

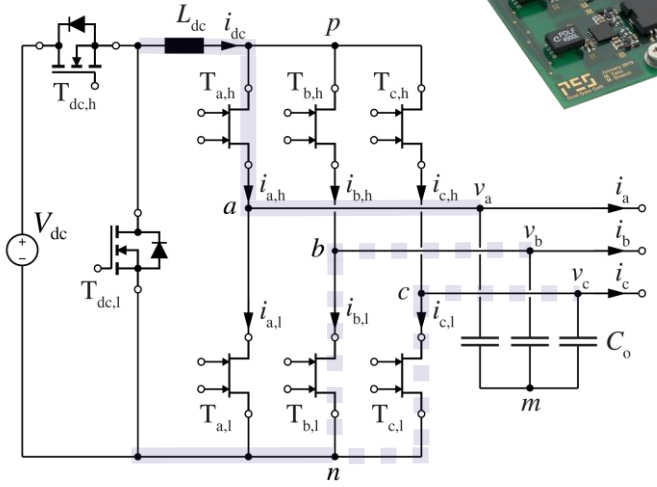


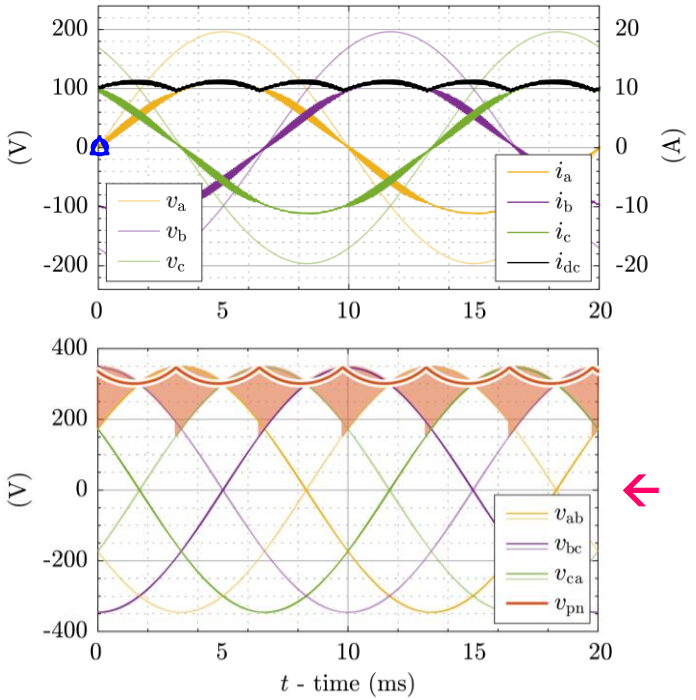


- Conventional Control of Inverter Stage → Rel. High CSI-Stage Sw. Losses

▶ 3-Φ Integrated Buck-Boost CSI (4)

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase*

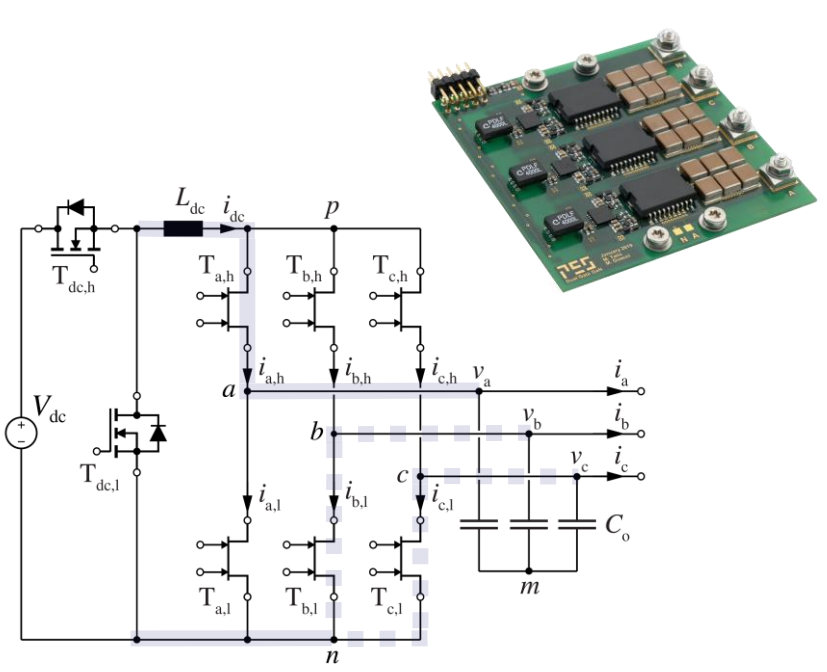


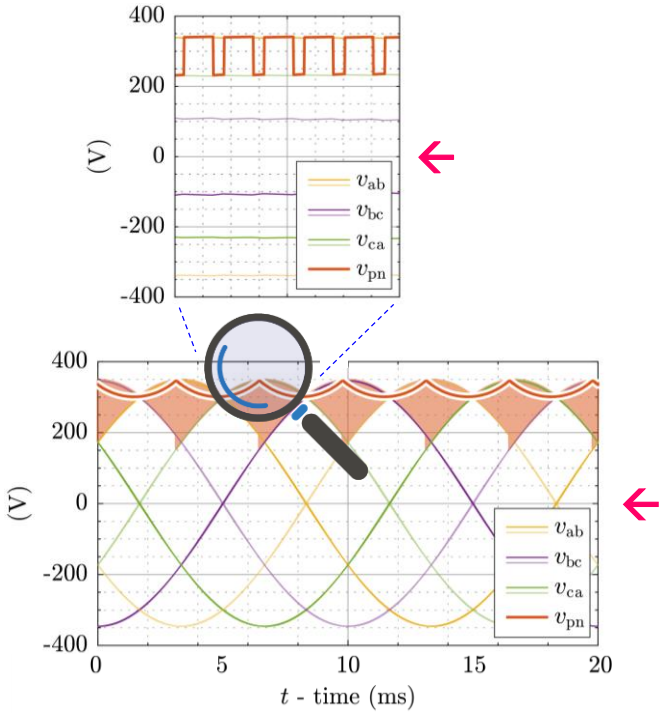


- *Switching of Only 2 of 3 Phase Legs → Significant Reduction of Sw. Losses*

▶ 3-Φ Integrated Buck-Boost CSI (5)

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase*

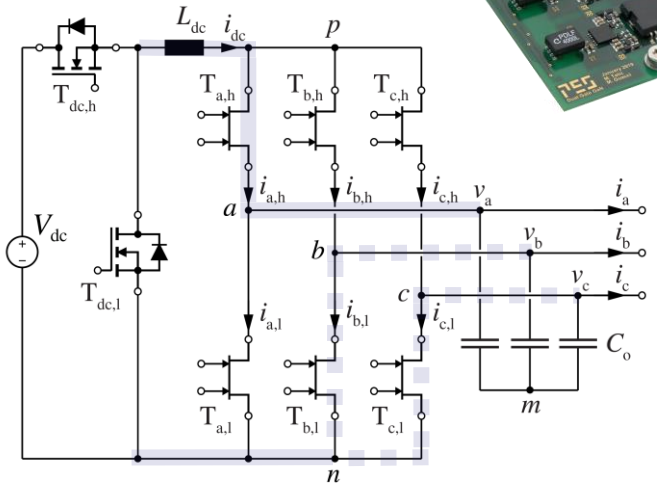


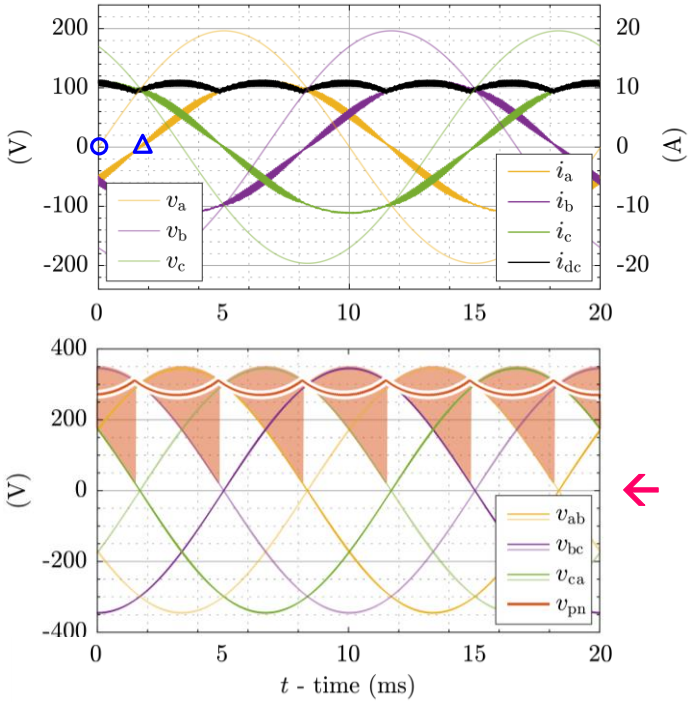


- *Switching of Only 2 of 3 Phase Legs → Significant Red. of Sw. Losses (≈ -86% for R-Load)*

▶ 3-Φ Integrated Buck-Boost CSI (6)

- "Synergetic" Control of Buck-Stage & CSI Stage
- 6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase

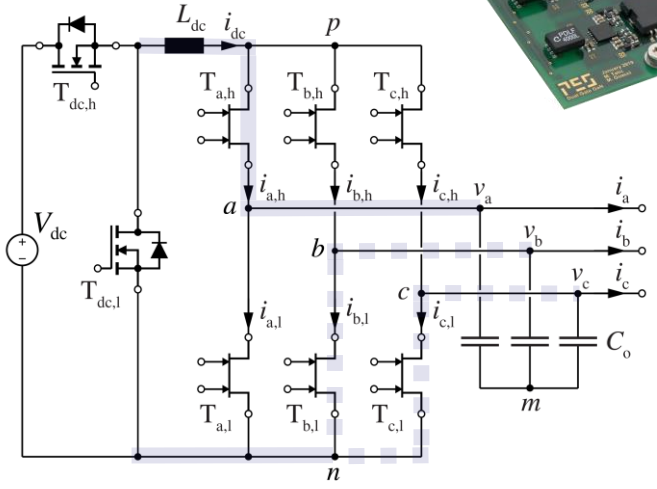


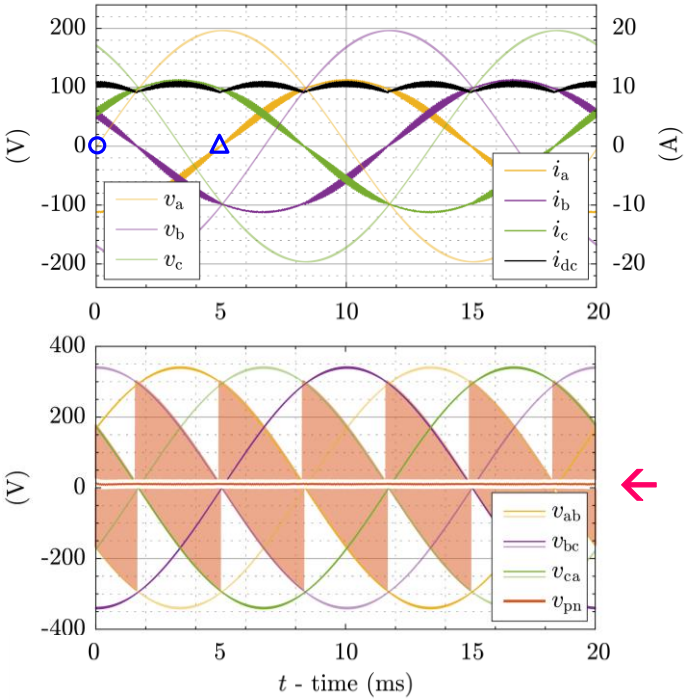


- Operation for 30° Phase Shift of AC-Side Voltage & Current

▶ 3-Φ Integrated Buck-Boost CSI (7)

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase*

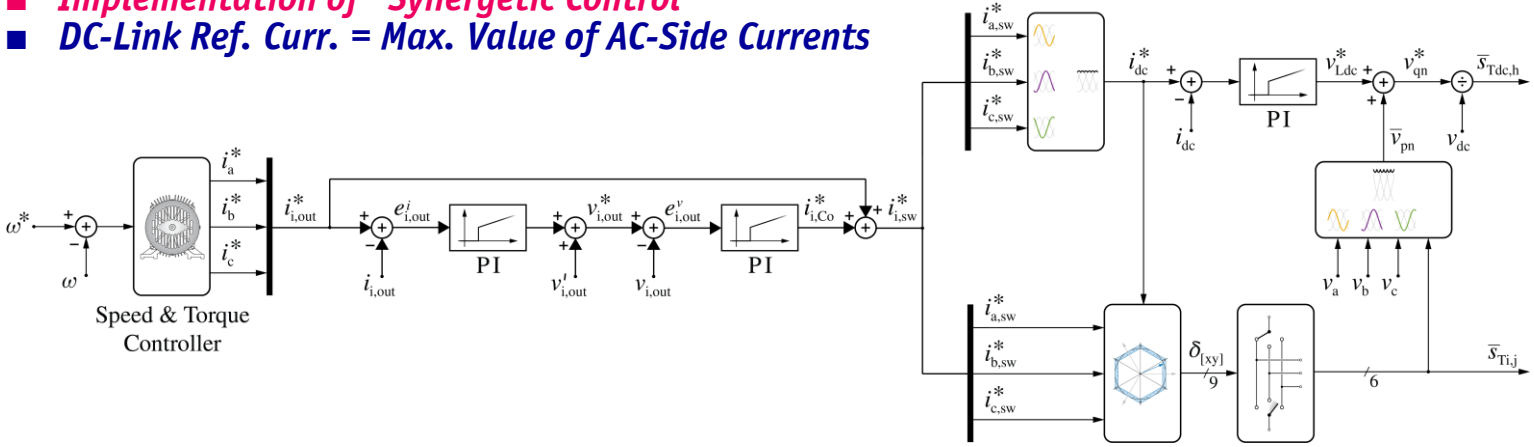




- *Operation for 90° Phase Shift (±90° — Limit Case for Buck-Stage Current Control)*

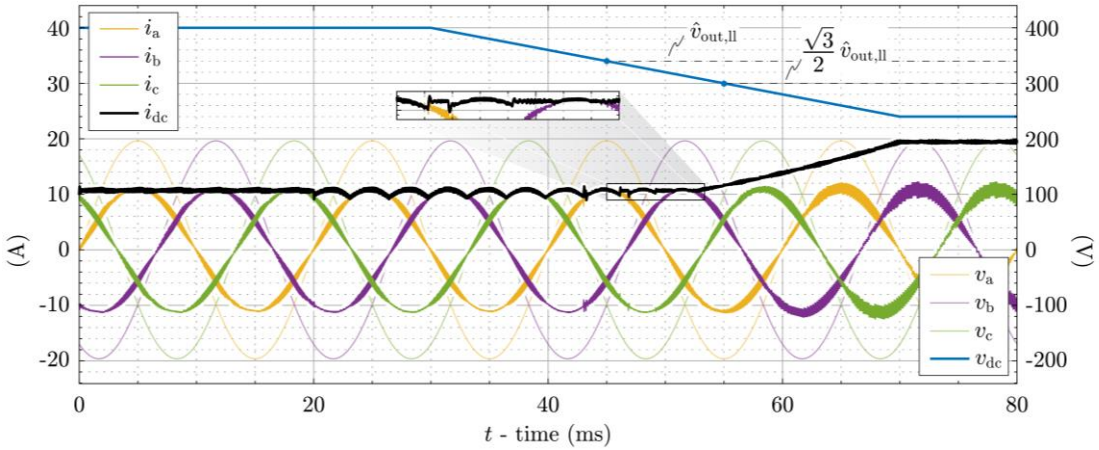
▶ 3-Φ Integrated Buck-Boost CSI (8)

- *Implementation of "Synergetic Control"*
- *DC-Link Ref. Curr. = Max. Value of AC-Side Currents*



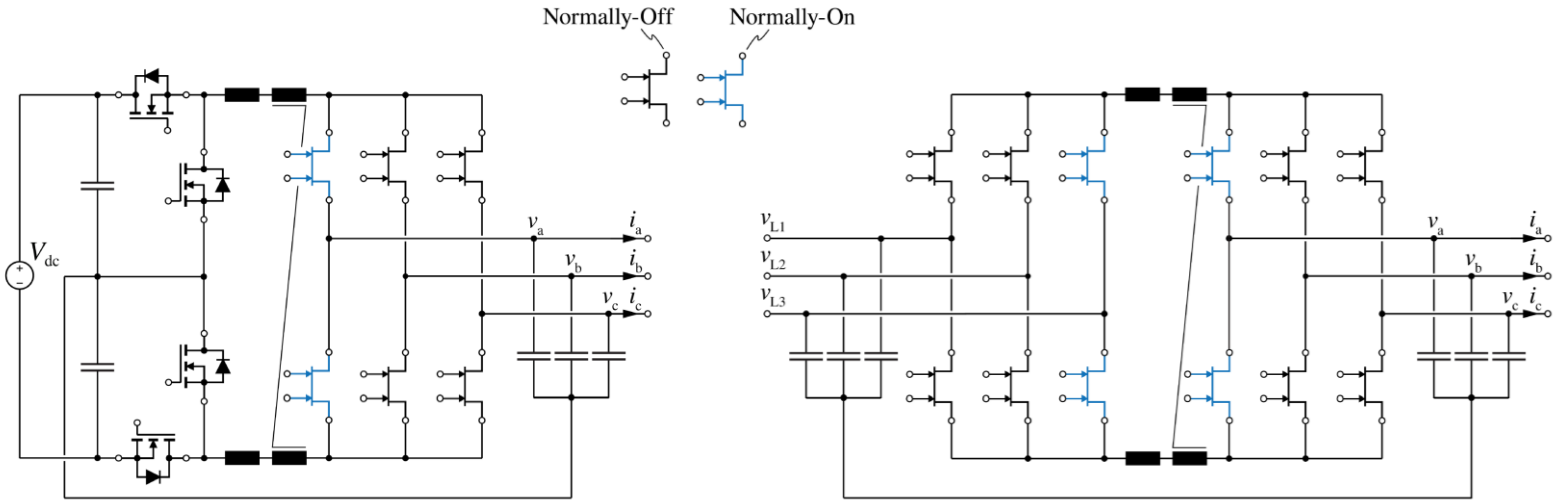
3/3 Mod. (i_{DC}=const.) →
2/3 Mod. (6-Pulse i_{DC}) →
Partial 2/3 Mod. →
Full-Boost Operation

- *Seamless Transition from Buck to Boost Operation*



Future Research

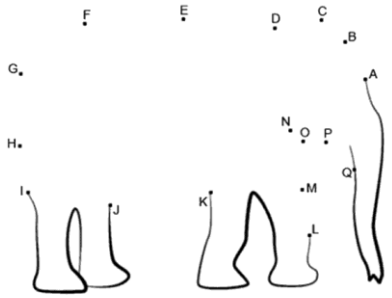
- *Advanced DC/AC Topologies incl. CM-Filtering*
- *Extension of 2/3-PWM to Bipolar DC-Link Voltage 3-Φ AC/AC Converter*
- *Multi-Objective Design & Comparative Evaluation*



- *Partial Use of "Normally-On" Switches for Freewheeling in Case of Auxiliary Power Loss*

Further Concepts

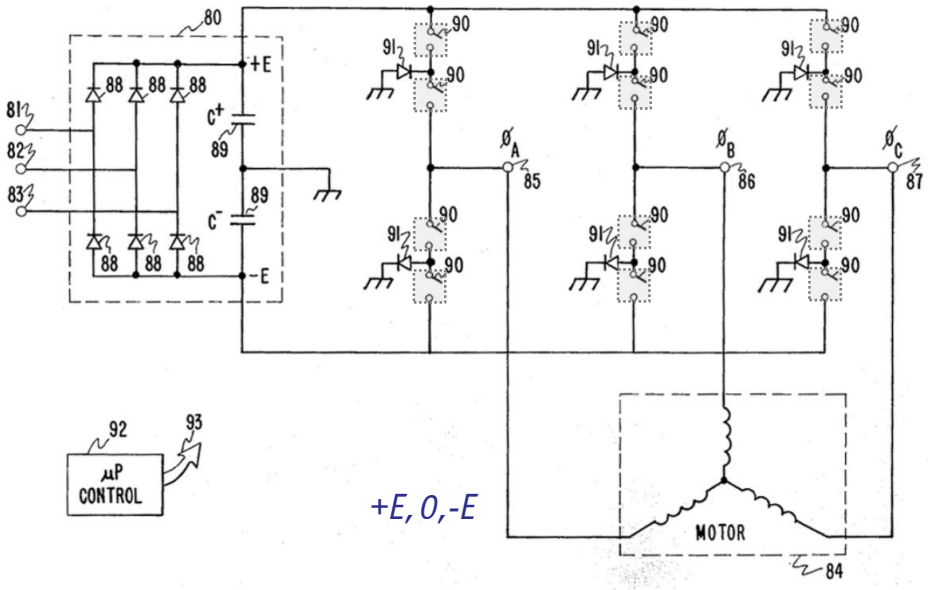
Simplified NPC 3-Level Inverter
Quasi-2-Level FCC



Hybrid Simplified NPC 3-Level Inverter (1)

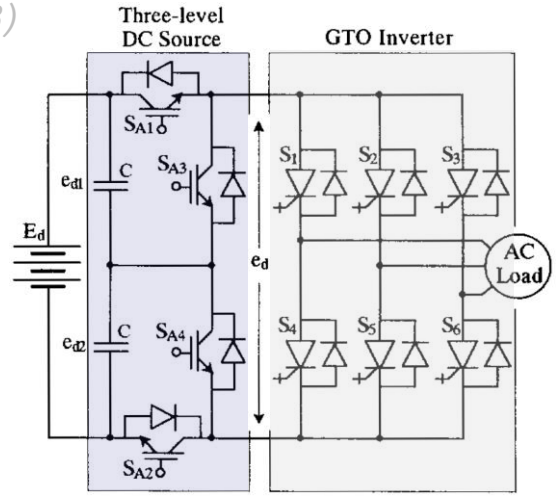
- *3-Level Neutral Point Clamped (3L-NPC) Topology Proposed in 1979 (!)*
- *Simplified NPC Configuration → Reduced Total # of Switches*
- *Fast/Slow & Low/High Voltage Semiconductors ("Hybrid")*

– *Baker (1979)*



+E, 0, -E

– *Rojas (1993)*



+E, e_{d1}, e_{d2}, 0

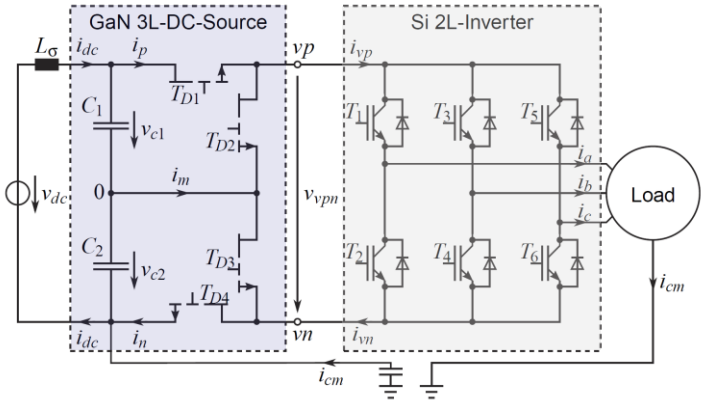
→ *Realization of the Simplified Concept Using 650V GaN HEMTs & 1200V Si IGBTs*

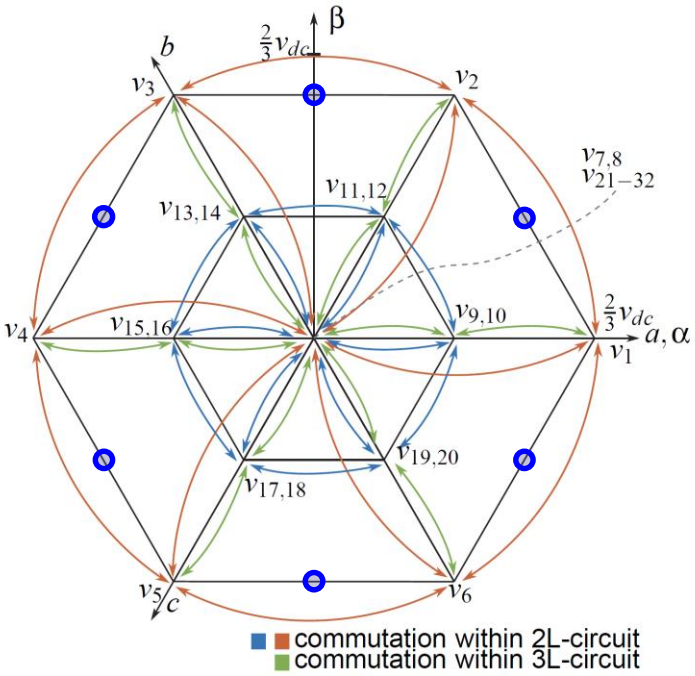
▶ Hybrid Simplified NPC 3-Level Inverter (2)

FAU FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

- *Application of Low Sw. & Cond. Loss 650V GaN Technology for 800V DC-Link*
- *Redundant Voltage Vectors Allow Control of Neutral Point Voltage*
- *Avg. Sw. Frequency of GaN HEMTs & Si IGBT → Factor 6*

- *Piepenbreier (2018)*





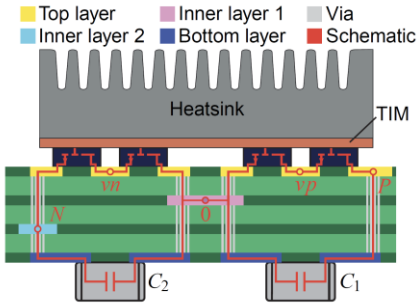
- *Missing Sw. States Comp. to Full 3L-NPC → 7 Instead of 9 Phase Voltage Levels*
- *Diff. Sw. Schemes → E.g. Commutation of 2L-Stage @ Full DC Voltage Can be Avoided*

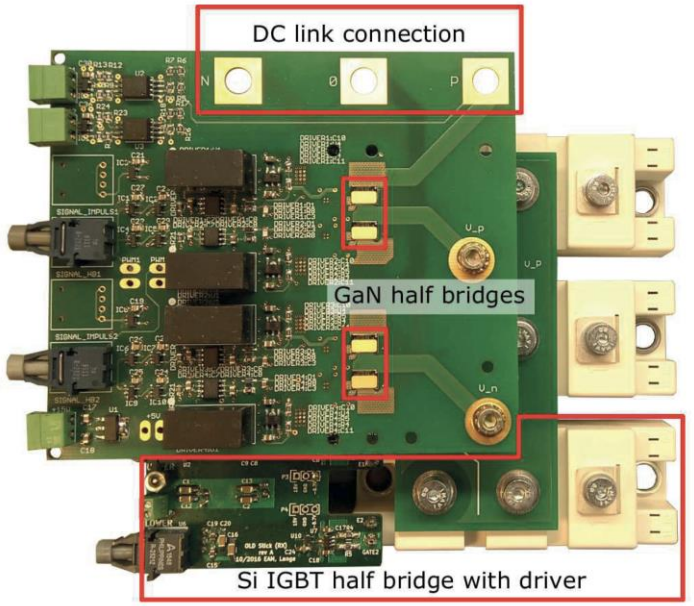
▶ Hybrid Simplified NPC 3-Level Inverter (3)

FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

- *Demonstrator Using Top-Cooled 650V SMD GaN Half-Bridges & 1200V Si-IGBT Modules*
- *Minimiz. of Commutation Loop by Close Placement of 2L-Inverter Stage & 3L-Source*
- *Vertical Commutation Loop of 3L Input Stage*

– *Piepenbreier (2018)*



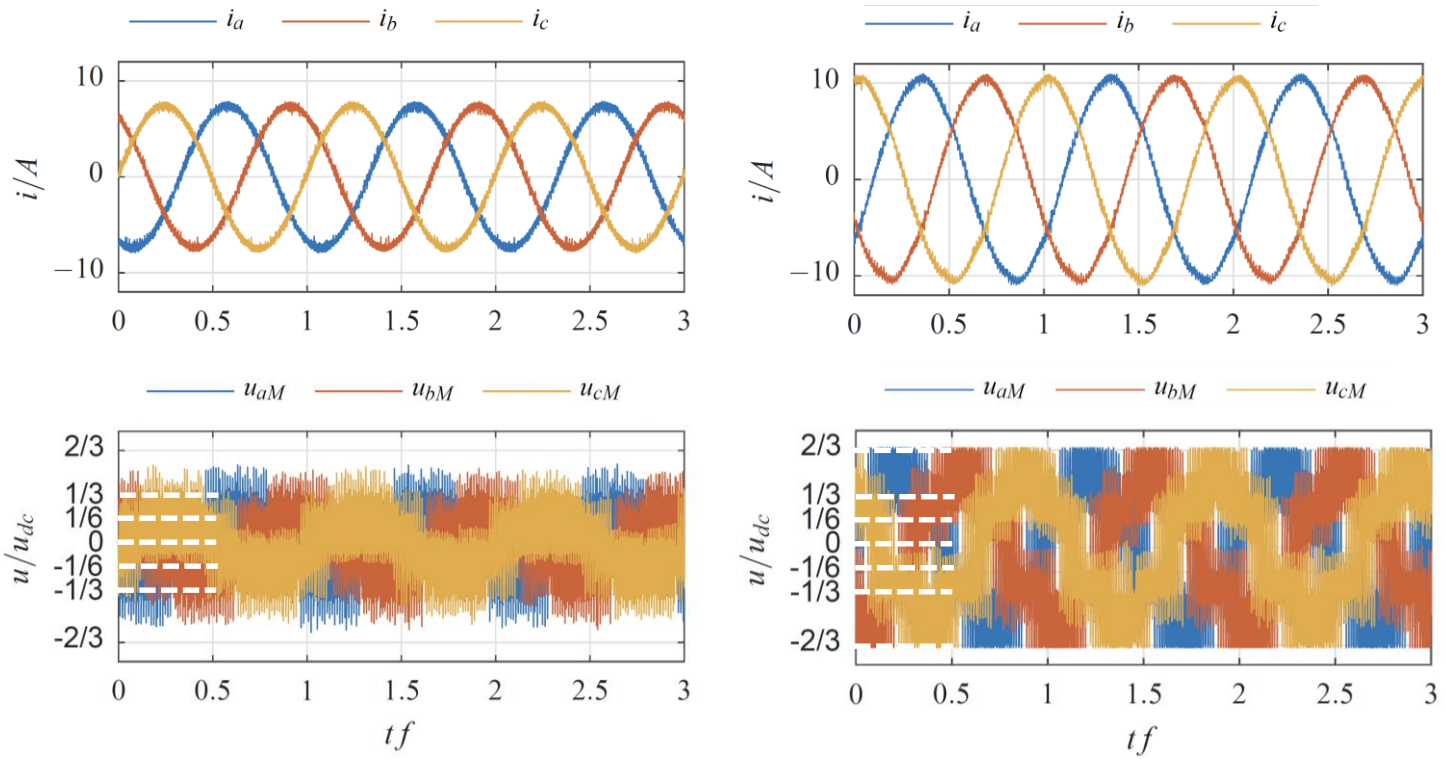


- *10kHz Sampling Frequ. → Avg. Sw. Frequencies: 20kHz (GaN) & 3.33kHz (IGBTs)*

▶ Hybrid Simplified NPC 3-Level Inverter (4)

FAU FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

■ *Experimental Results* → *Phase Currents & Phase Voltages* – Piepenbreier (2018)



● *Analysis for Different Modulation Depths — M=0.49 & M=0.92*

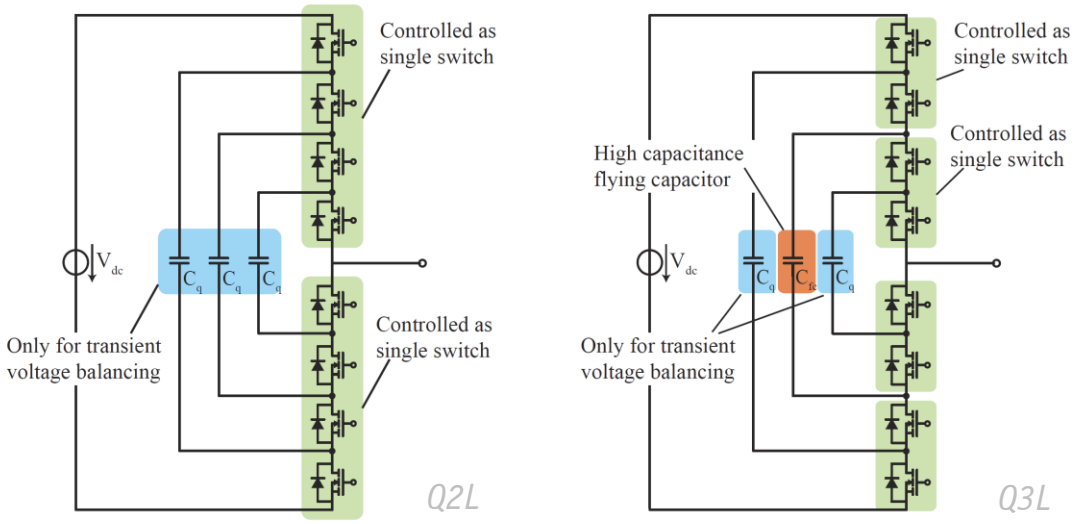
Quasi-2L/3L Flying Capacitor Inverter

Quasi-2L & Quasi-3L Inverters (1)

- *Operation of N-Level Topology in 2-Level or 3-Level Mode*
- *Intermediate Voltage Levels Only Used During Sw. Transients*
- *Applicability to All Types of Multi-Level Converters*

- *Schweizer (2017)*

ABB



- *Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages*
- *Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors*
- *Low Voltage/Low $R_{DS(on)}$/Low $ MOSFETs → High Efficiency / No Heatsinks / SMD Packages*

Quasi-2L & Quasi-3L Inverters (2)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

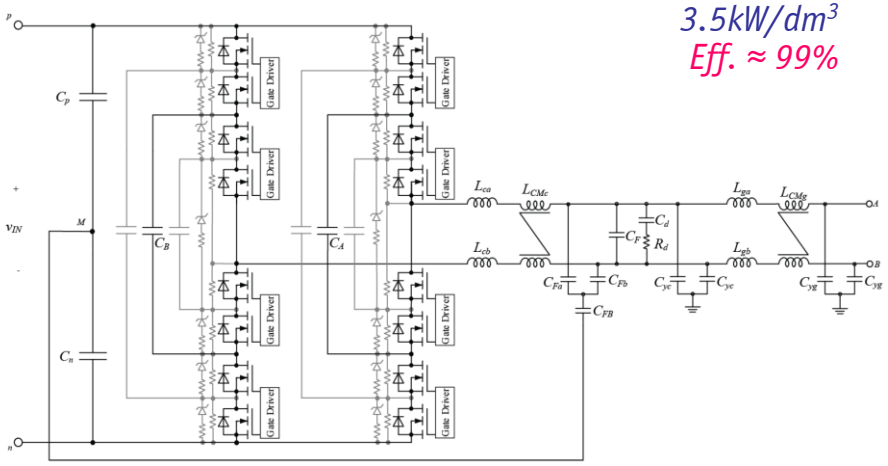
3.3kW @ 230V_{rms}/50Hz
Equiv. f_S= 48kHz

3.5kW/dm³
Eff. ≈ 99%

- Schweizer (2017)

ABB

SMD
150V Si-MOSFETs



- Reduced Average dv/dt → Lower EMI / Refection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/$R_{DS(on)}$/$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

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Eff. ≈ 99%

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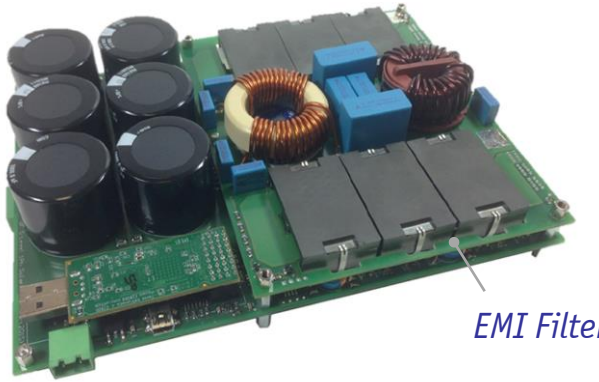
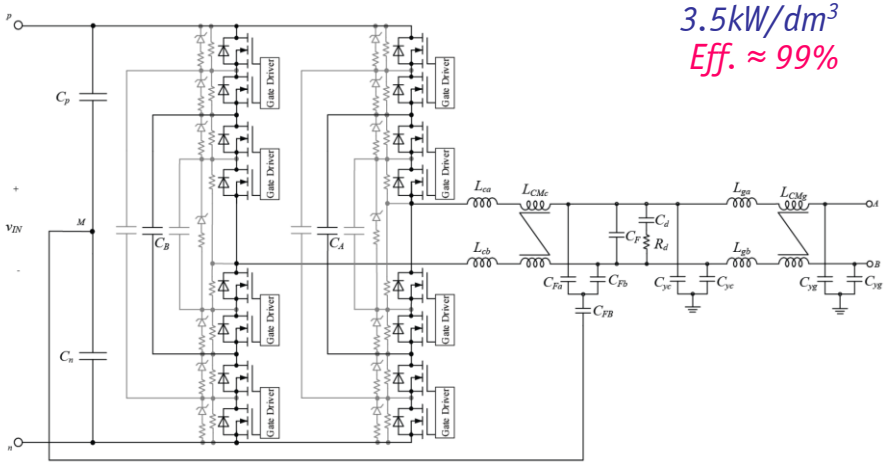
ABB



EMI Filter



- *Reduced Average dv/dt → Lower EMI / Refection Overvoltages*
- *Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors*
- *Low Voltage/$R_{DS(on)}$/$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages*

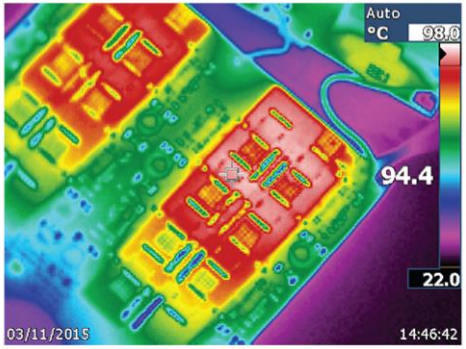
▶ Quasi-2L & Quasi-3L Inverters (2)

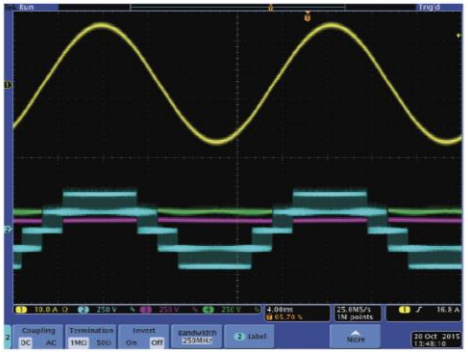
- Schweizer (2017)

ABB

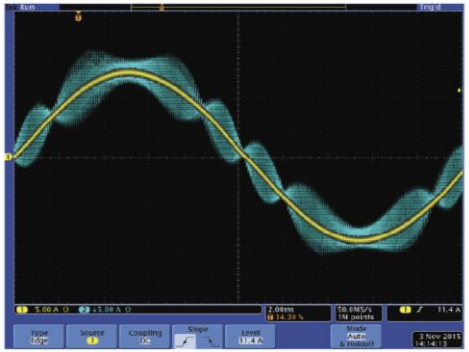
- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

Operation @ 3.2kW





- Conv. Output Voltage
- Sw. Stage Output Voltage
- Flying Cap. (FC) Voltage
- Q-FC Voltage (Uncntrl.)



- Output Current
- Conv. Side Current

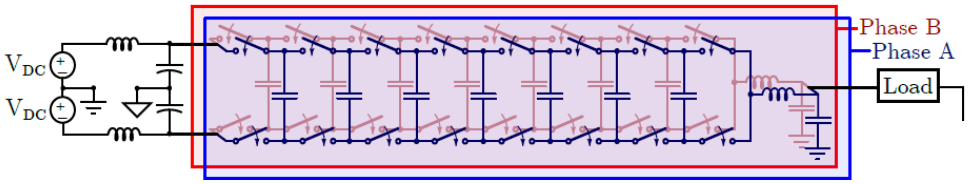
- Reduced Average dv/dt → Lower EMI / Refection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/$R_{DS(on)}$/$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

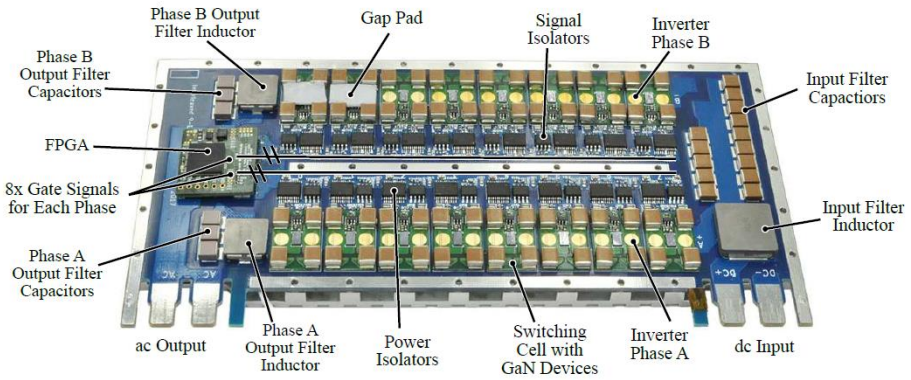
Ultra-Compact Modular Flying-Capacitor Inverter

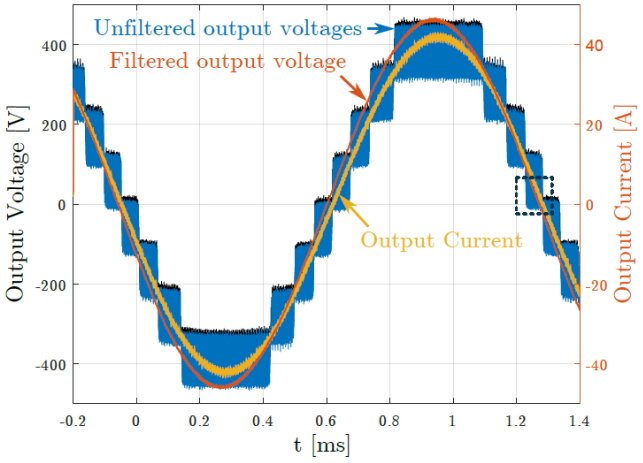
9-Level Flying Capacitor GaN Inverter (1)

ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

- *Rated Power 9.7kW*
- *DC-Link Voltage 1kV*
- *Output Filter → Sinusoidal Output Voltage*
- *Phase-Leg Modularity /Scalability*
- *Interleaving of 2 Bridge-Legs*
- *2-Side Forced-Air Cooling*







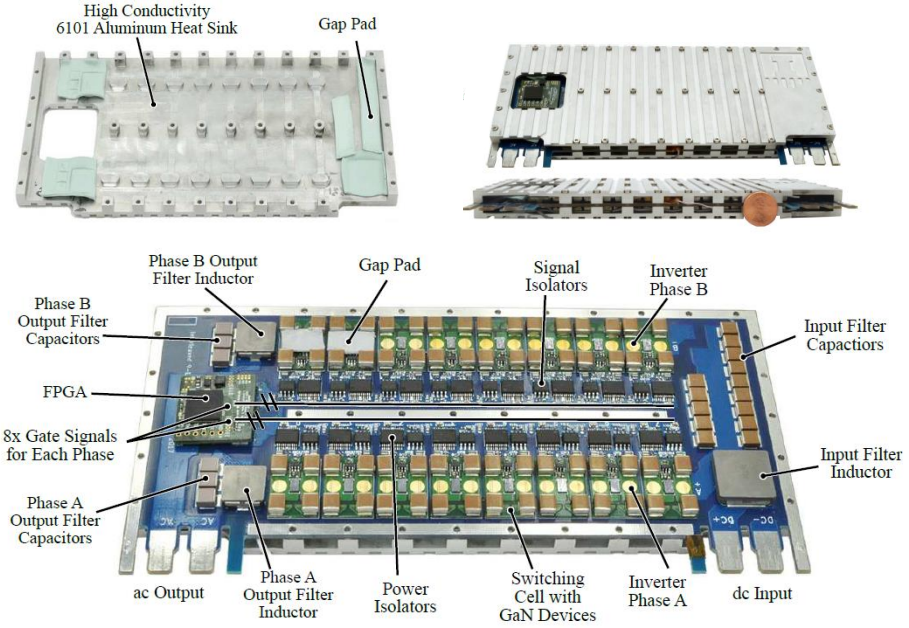
- *High Effective Sw. Frequ. (9x120 = 960kHz) → Very Small Output Filter*

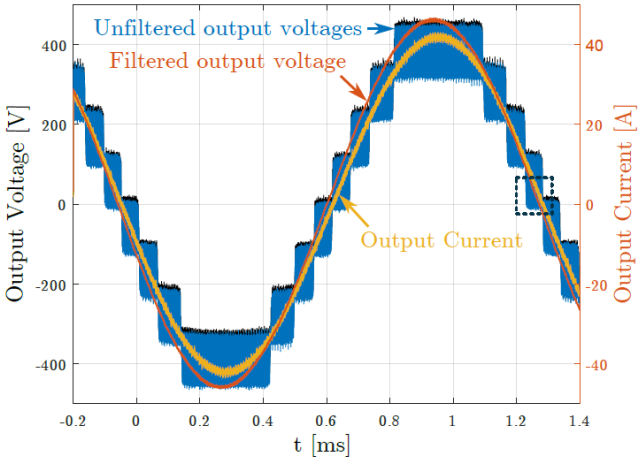
Source: R. Pilawa et al. (2018)

9-Level Flying Capacitor GaN Inverter (2)

- Rated Power 9.7kW
- DC-Link Voltage 1kV
- Peak Efficiency > 98.6%
- Specific Power 35kW/dm³
- 200x100x16mm³

17kW/kg





- High Effective Sw. Frequency (960kHz) → Very Small Output Filter

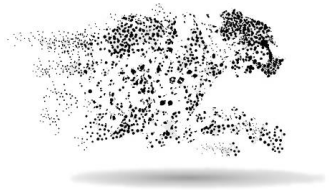
Source: R. Pilawa et al. (2018)

Ultra-Compact Power Module with Integrated Filter

650V GaN E-HEMT Technology

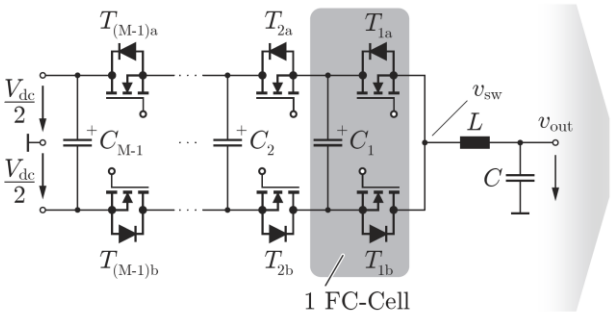
$f_{S,eff}$ = 4.8MHz

f_{out} = 100kHz

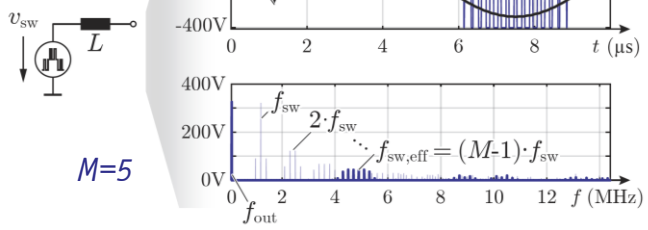


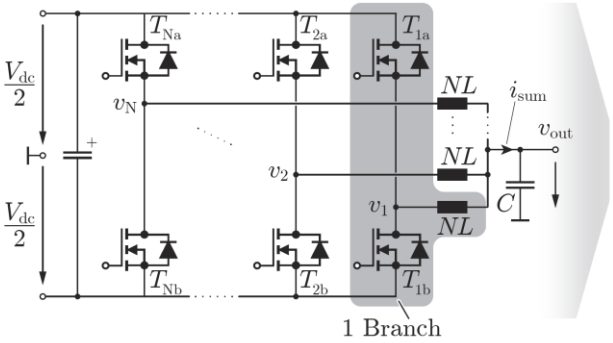
Integrated Filter GaN Half-Bridge Module (1)

- Minimization of Filter Volume by Series & Parallel Interleaving & Extreme Sw. Frequency
- Handling of DC Output Requires Flying Capacitor Approach for Series Interleaving

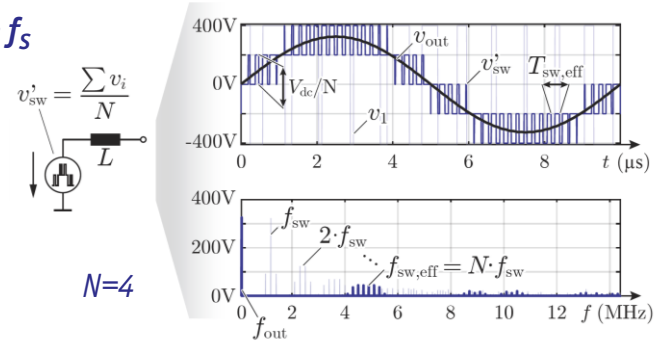


$f_{s,eff} = (M\text{-}1) \cdot f_s$





$f_{s,eff} = N \cdot f_s$

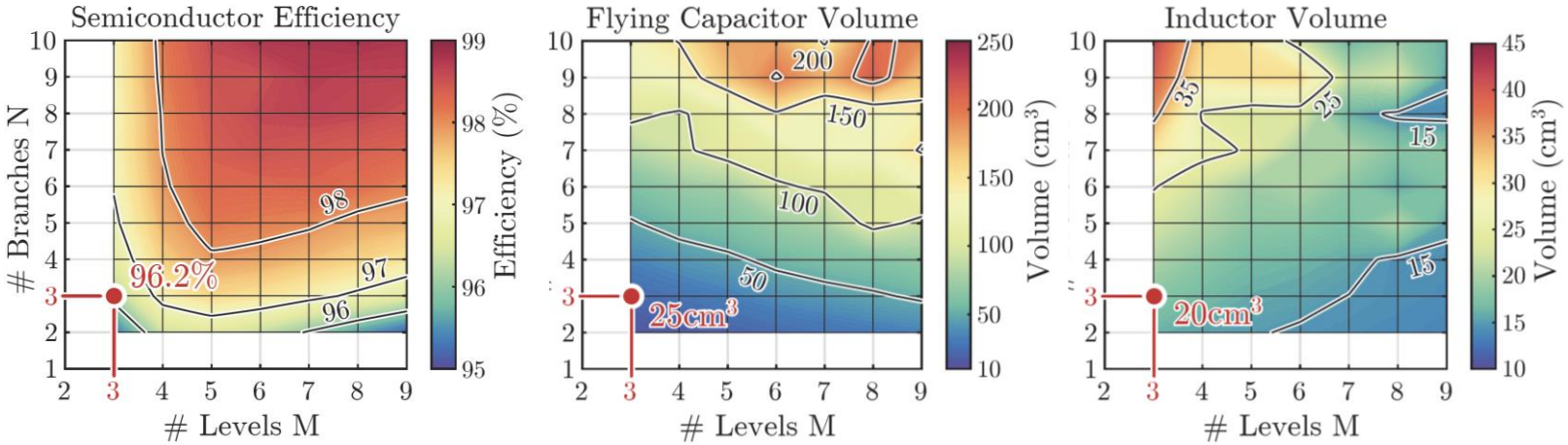


→ Target: Best Combination of Multiple Levels (M) & Parallel Branches (N)

▶ Integrated Filter GaN Half-Bridge Module (2)

- Analysis of Best Combination of Levels (M) & Parallel Branches (N)
- Application of GaN Semiconductor Technology
- U_{DC}=800V, P=10kW, $\Delta u_{out,pp}$= 1%, $f_{S,eff}$= 4.8MHz

@ C_{filt}= 90nF =const.



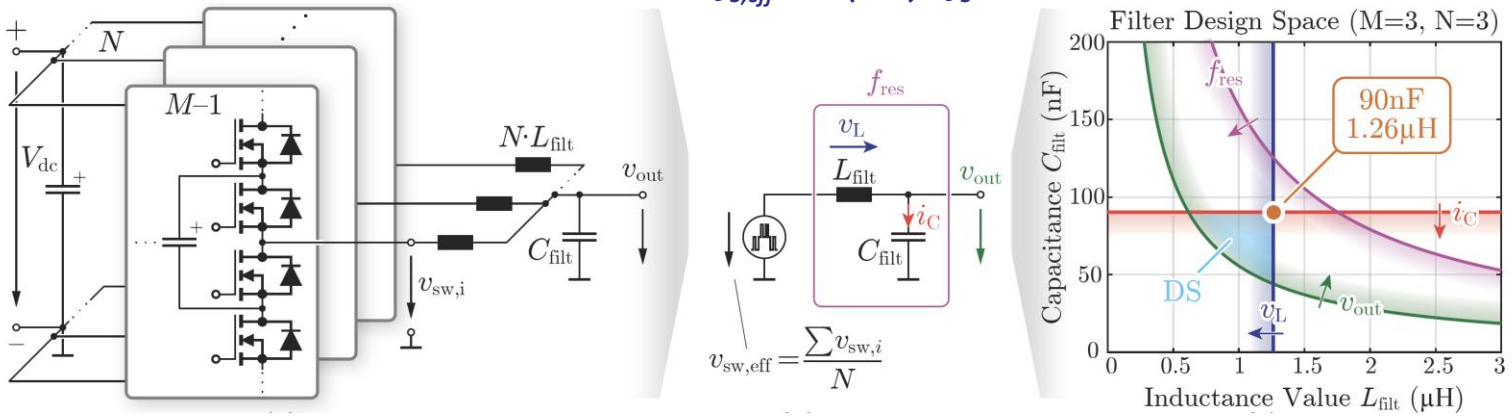
→ L_{filt}= 1.26uH Fixed in Order to Limit Branch Current Ripple for High N
→ Selection of M=3 / N=3 Considering Efficiency / Filter Volume Trade-Off

▶ Integrated Filter GaN Half-Bridge Module (3)

- Selection of M=3 / N=3 Considering Efficiency / Filter Volume Trade-Off
- $N \cdot L_{filt}$=3.3uH of Branch Inductance / C_{filt} = 90nF
- 650V GaN E-HEMT Technology
- $f_{S,eff}$= 4.8MHz

V_L < 15%
I_C <30%

$f_{S,eff} = N \cdot (M-1) \cdot f_S$



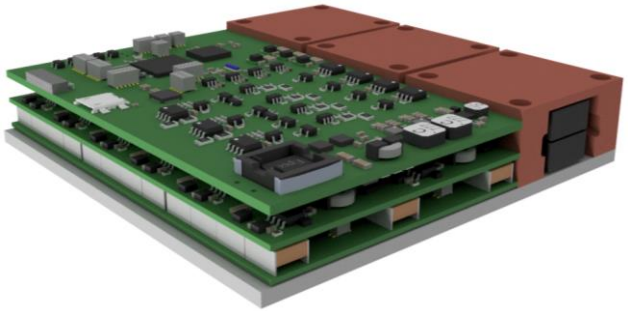
- Design for Max. Output Frequency of f_{out} = 100kHz (!) @ Full-Scale Voltage Swing

▶ Integrated Filter GaN Half-Bridge Module (4)

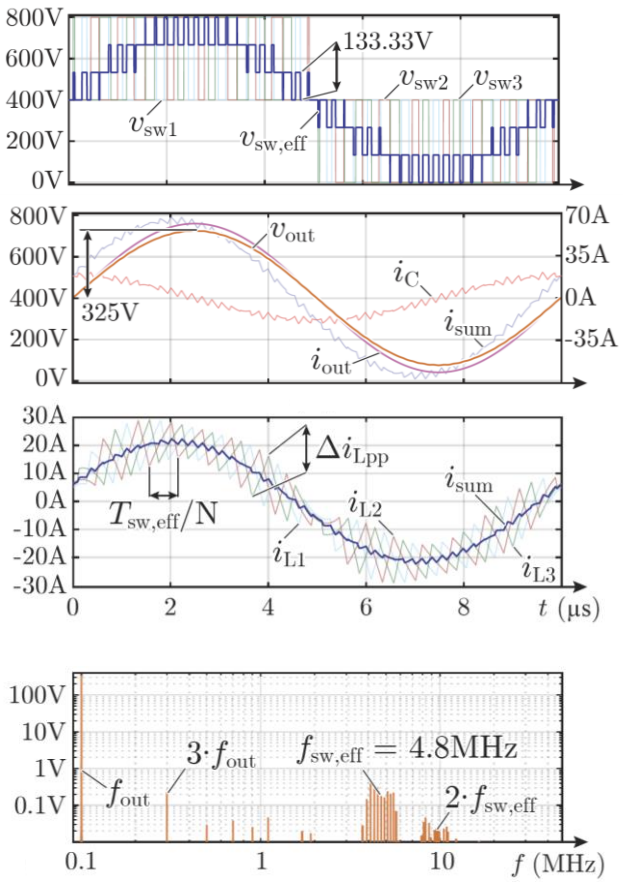
- **Demonstrator System**

— 650V GaN Power Semiconductors
— Volume of ≈180cm³ (incl. Control etc.)
— H_2O Cooling Through Baseplate

★ ≈ 50kW/dm³



- Operation @ f_{out}=100kHz ($f_{S,eff}$= 4.8MHz)

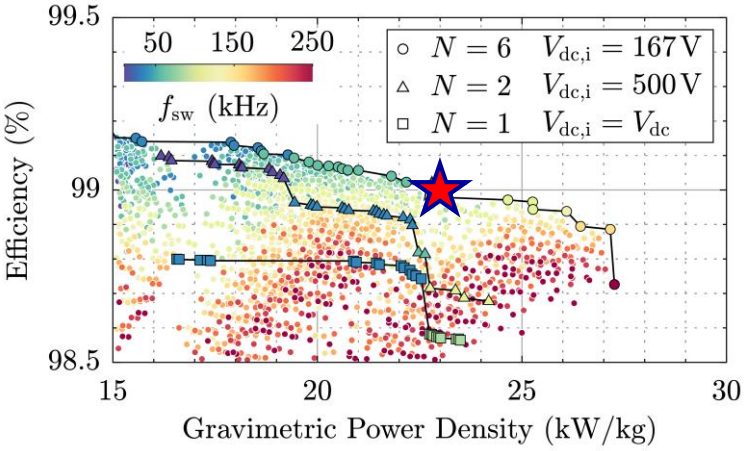


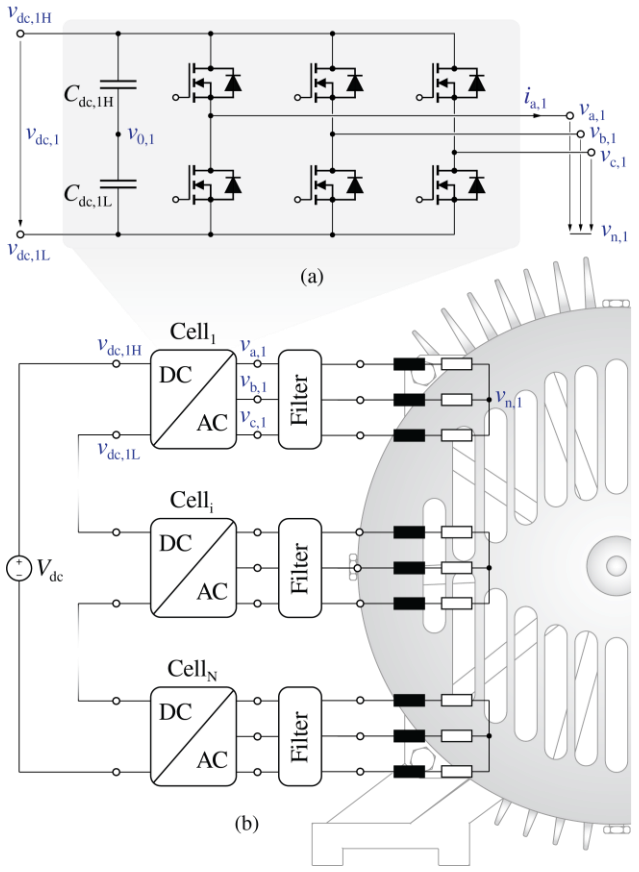
Motor-Integrated Modular Inverter

Motor-Integrated Modular Inverter

- Machine/Inverter Fault-Tolerant VSD
- Motor-Integr. Low-Voltage Inverter Modules
- Very-High Power Density / Efficiency
- Supply of 3-Φ Winding Sets / Low C Buffer Cap.

- Rated Power 45kW / f_{out} = 2kHz
- DC-Link Voltage 1 kV

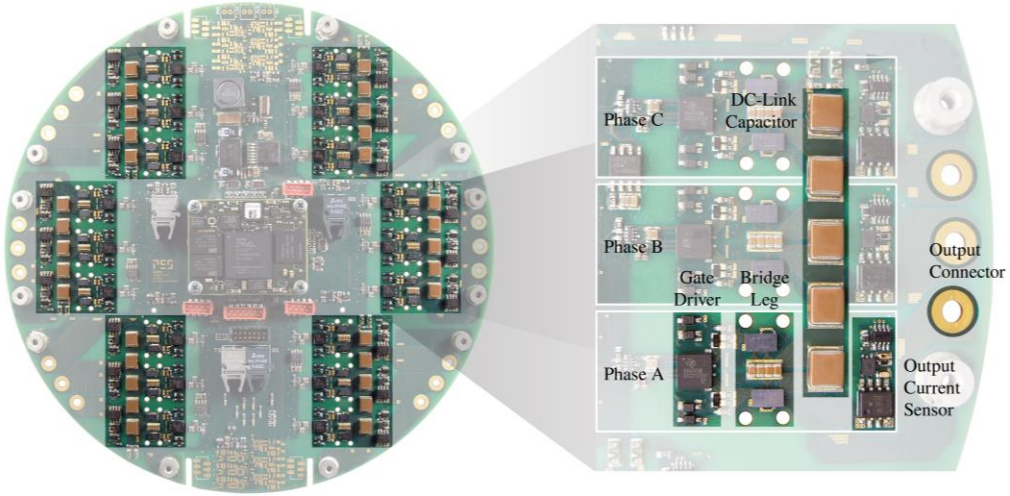


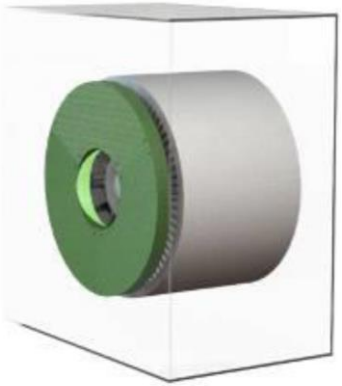


→ Evaluate Machine Concept (PMSM vs. SRM etc.) / Wdg Topologies / Filter Requ. / etc.

▶ Motor-Integrated Inverter Demonstrator

- Rated Power 9kW @ 3700rpm
- DC-Link Voltage 650V...720V
- 3-Φ Power Cells 5+1
- Outer Diameter 220mm





Source: Oak Ridge Nat. Lab

- Axial Stator Mount
- 200V GaN e-FETs
- Low-Capacitance DC-Links
- 45mm x 58mm / Cell

→ Main Challenge — Thermal Coupling/Decoupling of Motor & Inverter

Conclusions

Conclusions

- *Future Need for „SWISS Knife“-Type Systems*

— *Wide Input / Output Voltage Range*
— *Continuous / Sinusoidal Output Voltage*
— *Electromagnetically „Quiet“ - No Shielded Cables*
— *On-Line Monitoring / Industry 4.0*
— *“Plug & Play“ / Non-Expert Installation*
— *SMART Motors*

Source: UK Outdoor Store

- *Enabling Technologies*

— *SiC / GaN*
— *Adv. (Multi-Level) Topologies incl. PFC Rectifier*
— *“Synergetic” Control*
— *Monolithic Bidirectional GaN*
— *Intelligent Power Modules*
— *Integration of Switch / Gate Drive / Sensing / Monitoring*
— *Adv. Modeling / Simulation / Optimization*

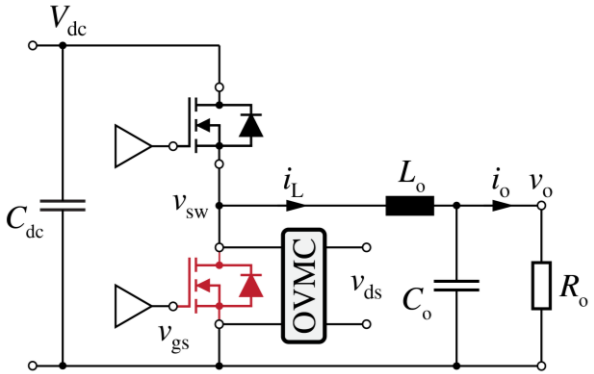
- *System Level → Integration of Storage, Distributed DC Bus Systems, etc.*

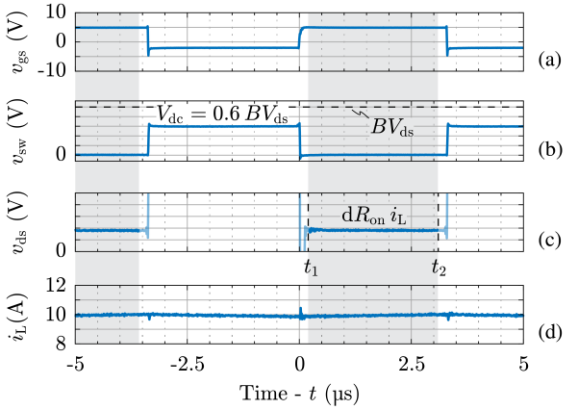
Accurate Measurement of SiC/GaN Power Semiconductor Characteristics

On-State Voltage
Switching Losses

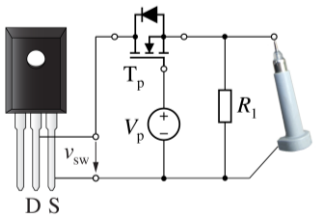
▶ On-State Voltage Measurement (1)

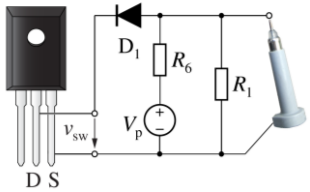
- Device / Load Current / Gate Voltage / Junction Temp. → On State-Resistance $R_{DS(on)}$

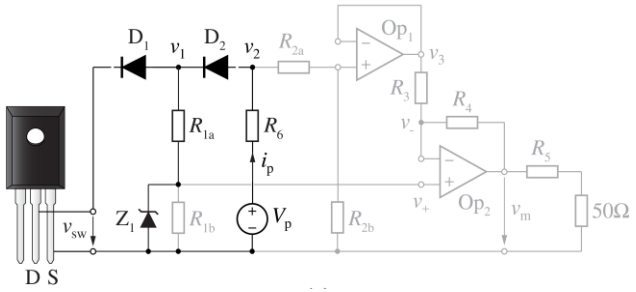




$$R_{DS(on)} = v_{DS(on)} / i_L$$



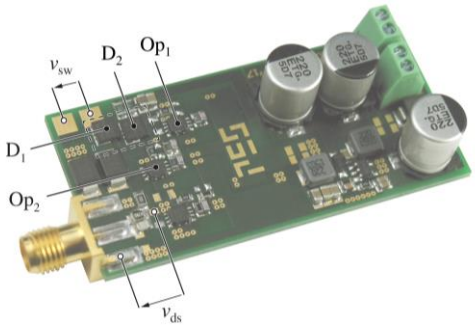


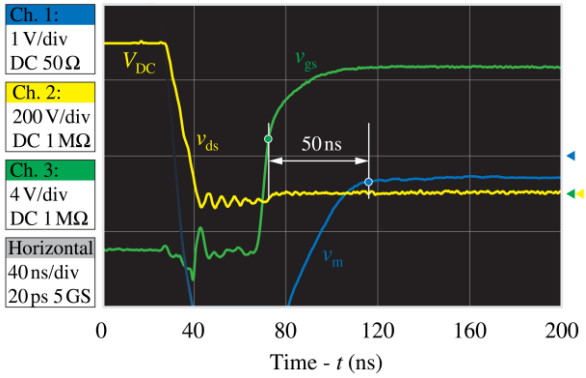


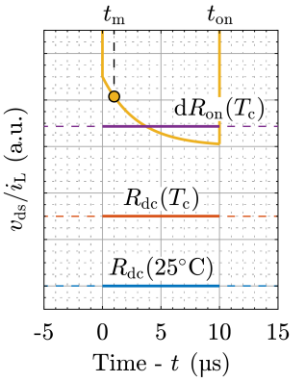
- Decoupling High Blocking Voltage and (Very) Low On-State Voltage (≈1V << BV_{DS})

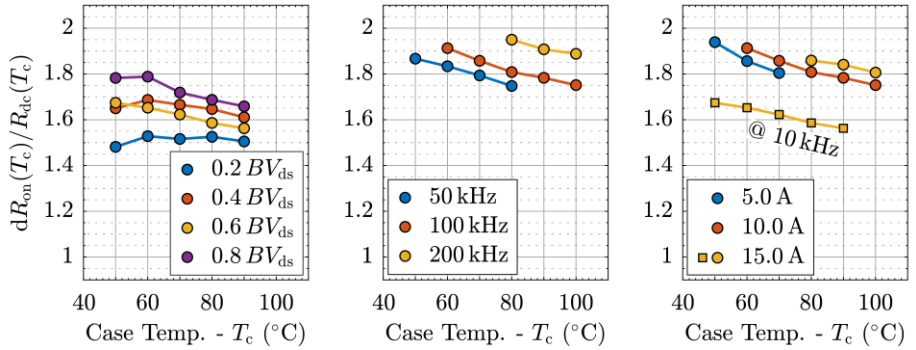
▶ On-State Voltage Measurement (2)

- **High Accuracy** → **Compensation of Decoupling Diode Forward Voltage**
- **Fast Dyn. Response** → **Valid Measurement 50ns After Turn-On**





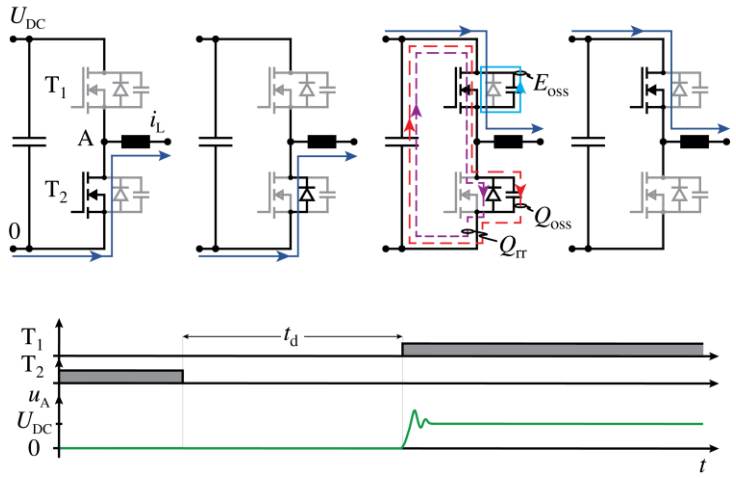




- **Example — Dyn. $R_{DS(on)}$ of GaN HEMTs → 2x $R_{DS(on)}$ @ 100kHz - 0.6BV_{DS}**

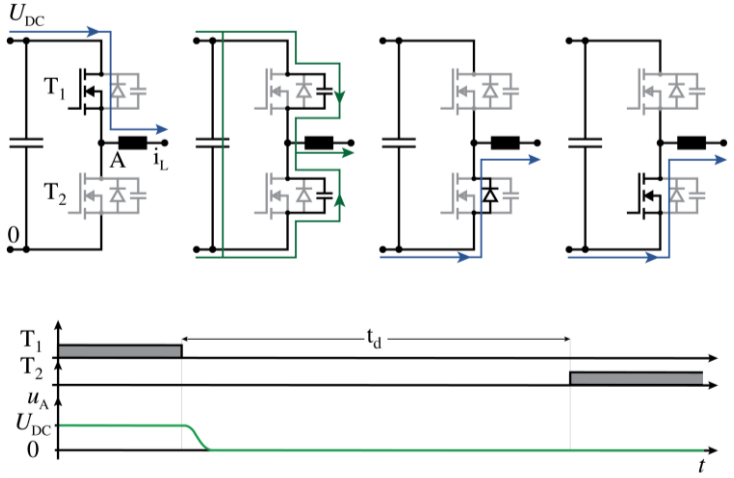
▶ Hard- & Soft-Switching Losses

■ Hard-Switching



→ $E_{sw} = Q_{oss}U_{DC} + k_1 I_{sw} + k_2 I_{sw}^2$

■ Soft-Switching (ZVS)

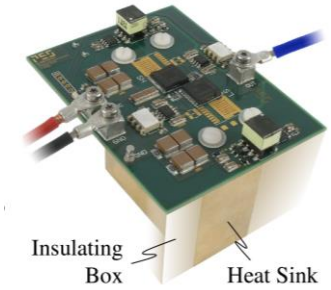


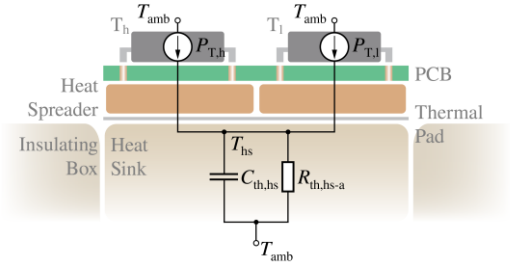
→ $E_{sw} \approx 0$

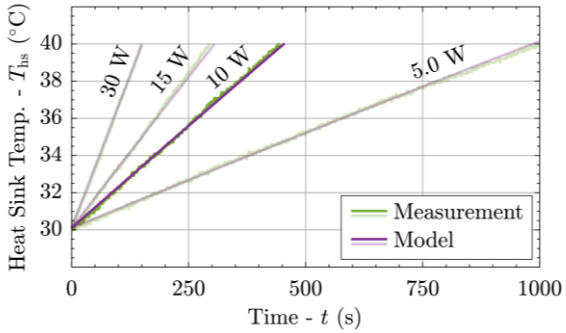
- *High Sw. Speeds → Overvoltage & Ringing / Probe Intrusiveness / etc.*
- *Low ZVS Losses → High Accuracy Only for Calorimetric / Direct Loss Measurement*

▶ Switching Loss Measurement

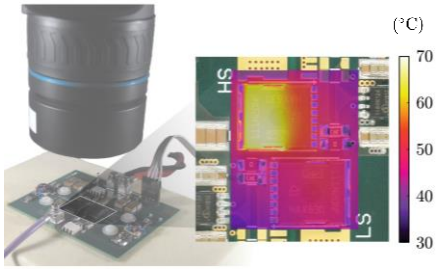
- *Heat-Sink Temp.-Based Transient Calorim. Method → 15 min / Measurement*

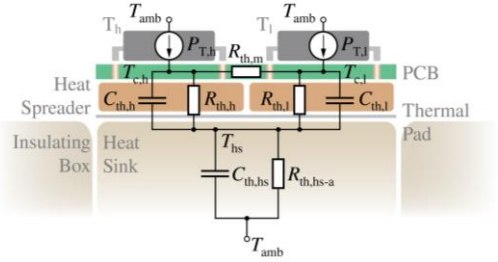


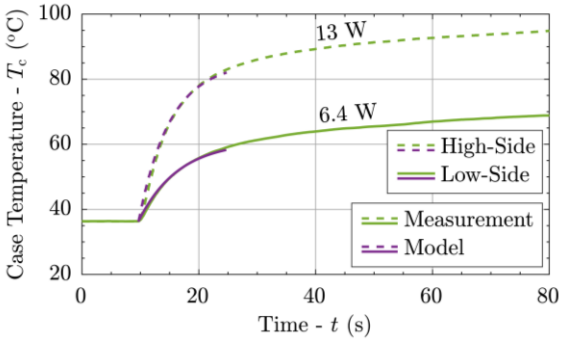




- *Case Temp.-Based Ultra-Fast Method → 15 sec / Measurement*

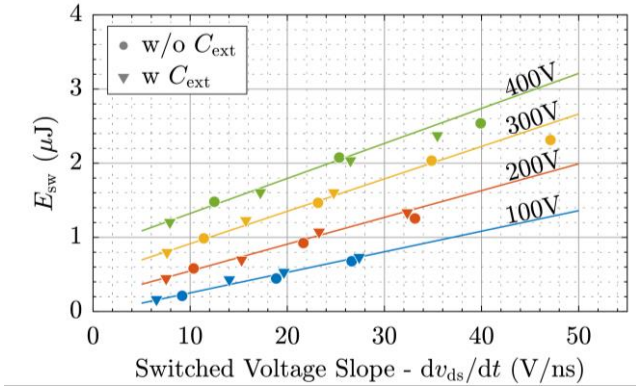


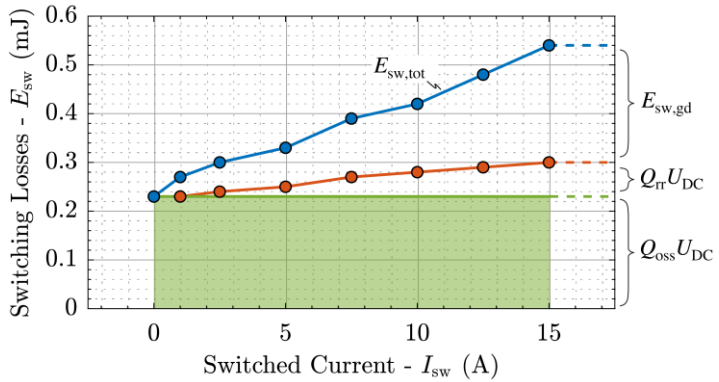




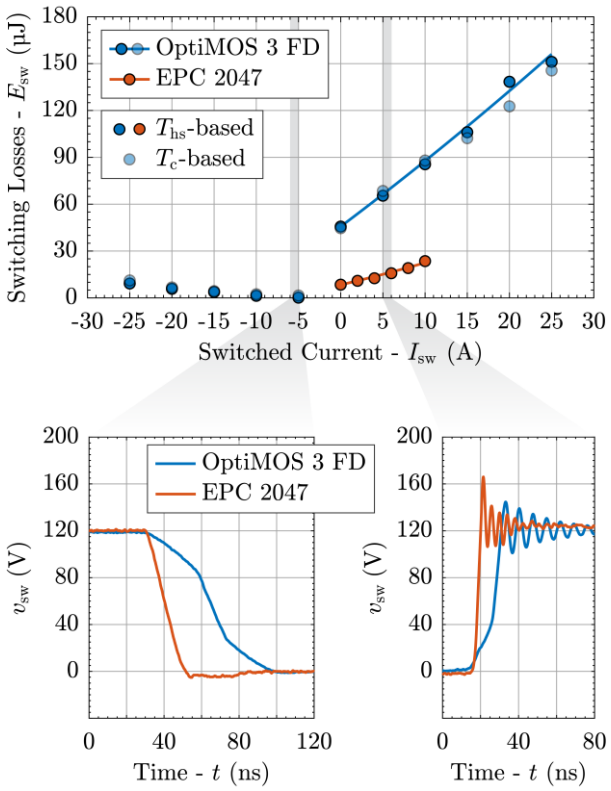
▶ Example Measurement Results

■ 650V GaN (ZVS)





■ 200V Si vs. GaN (Hard-Sw. & ZVS)

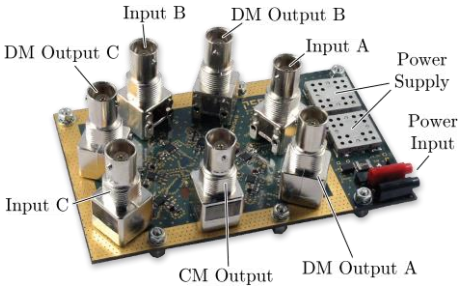


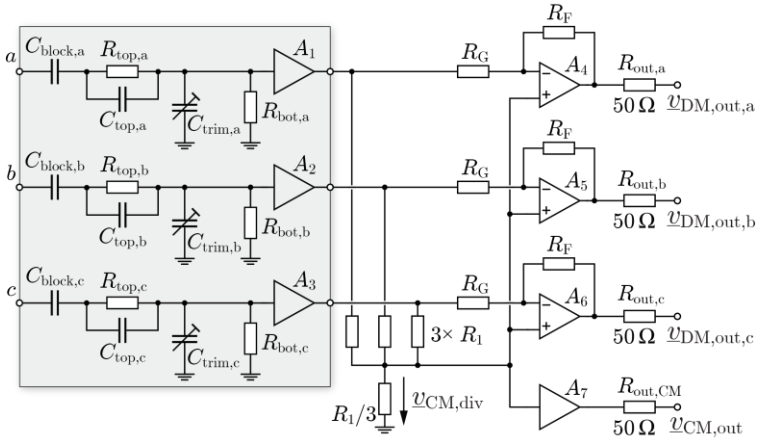
■ 1.2kV SiC (Hard-Sw.)

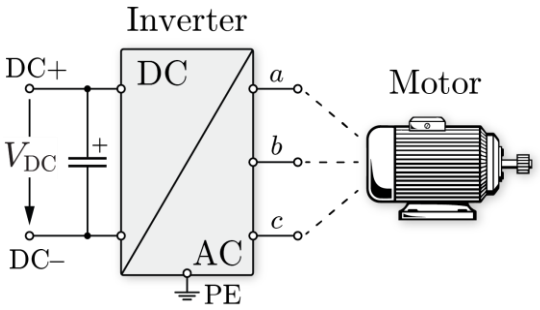
3-Φ DM/CM Conducted EMI Separation

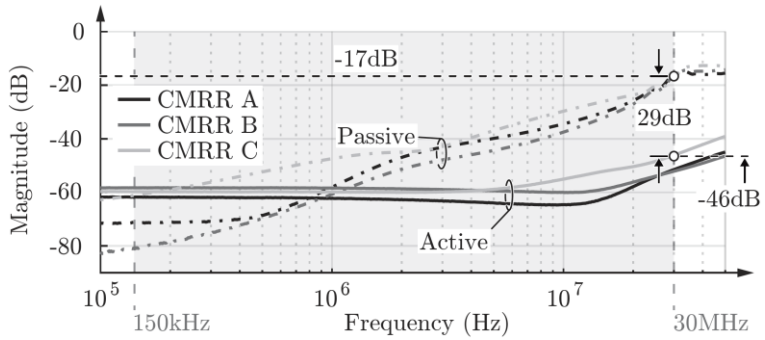
▶ 3-Φ DM/CM EMI Measurement & Separation

- *EMI Measurement @ Inverter Output*
- *DM/CM Splitting for Specific Filter Design*









- *Cap. Coupled Interface Circuit as Replacement for LISN (Var. Output Frequ.)*

Biographies of the Presenters

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Johann W. Kolar is a Fellow of the IEEE and has received his PhD degree (summa cum laude) from the Vienna University of Technology, Austria. He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, modulation and control concepts and has supervised 70+ Ph.D. students. He has published 880+ scientific papers in international journals and conference proceedings and has filed 190+ patents. He received numerous awards, incl. 29 IEEE Transactions and Conference Prize Paper Awards, the 2016 IEEE William E. Newell Power Electronics Award, and 2 ETH Zurich Golden Owl Awards for excellence in teaching. He has initiated and/or is the founder of 4 ETH Spin-off companies. The focus of his current research is on ultra-compact / ultra-efficient SiC and GaN converter systems, solid-state transformers, advanced three-phase inverter concepts for variable speed motor drives, ultra-high speed and bearingless motors / actuators, and design automation in power electronics/mechatronics.

Mattia Guacci (STM'16) received the B.Sc. degree (summa cum laude) and the M.Sc. degree (summa cum laude) in Electronic Engineering from the University of Udine, Italy in July 2013 and in October 2015, respectively. In 2014 he was with Metasystems SpA in Reggio nell'Emilia, Italy working on on-board battery chargers for electric vehicles. In November 2015 he joined the Power Electronic Systems (PES) Laboratory of the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland as a scientific assistant investigating compact, high-efficiency DC/AC power converters based on wide band-gap power semiconductors. In September 2016 he started his Ph.D. at PES focusing on advanced power electronics concepts for future aircraft and electric vehicle applications. Mattia Guacci has authored 10 scientific papers in refereed journals and conference proceedings and has filed 4 patents. He has received 1 IEEE Prize Paper Award.

Michael Antivachis (SM'16) received the B.Sc. degree in electrical engineering from the National Technical University of Athens (NTUA) in 2014 and the M.Sc. degree in energy science and technology from the Swiss Federal Institute of Technology (ETH) in 2016. Since June 2016 he is with the Power Electronic Systems Laboratory (PES) of ETH Zurich as a Ph.D. candidate. His research interests include high-speed motor drive systems for commercial applications, high power density inverter topologies employing wide-bandgap power devices and low EMI emission profile inverters.

Dominik Bortis received the M.Sc. and Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 he is heading the research group Advanced Mechatronic Systems at PES, which concentrates on ultra-high speed motors, magnetic bearings and bearingless drives, new linear-rotary actuator and machine concepts with integrated power electronics. Targeted applications include e.g. highly dynamic and precise positioning systems, medical and pharmaceutical systems, and future mobility concepts. Dr. Bortis has published 90+ scientific papers in international journals and conference proceedings. He has filed 32 patents and has received 6 IEEE Conference Prize Paper Awards.

Thank you!