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The Essence of Three-Phase PFC Rectifier Systems

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Definitions and Characteristics

• Passive Rectifier Systems	 Line Commutated Diode Bridge/Thyristor Bridge - Full/Half Controlled Low Frequency Output Capacitor for DC Voltage Smoothing Only Low Frequency Passive Components Employed for Current Shaping, No Active Current Control No Active Output Voltage Control
• Hybrid Rectifier Systems	 Low Frequency and Switching Frequency Passive Components and/or Mains Commutation (Diode/Thyristor Bridge - Full/Half Controlled) and/or Forced Commutation Partly Only Current Shaping/Control and/or Only Output Voltage Control Partly Featuring Purely Sinusoidal Mains Current
• Active Rectifier Systems	 Controlled Output Voltage Controlled (Sinusoidal) Input Current Only Forced Commutations / Switching Frequ. Passive Components
Phase-Modular Systems	 Phase Rectifier Modules of Identical Structure Phase Modules connected in Star or in Delta Formation of Three Independent Controlled DC Output Voltages
Direct Three-Phase Syst.	- Only One Common Output Voltage for All Phases

- Symmetrical Structure of the Phase Legs
 Phase (and/or Bridge-)Legs Connected either in Star or Delta







Diode Bridge Rectifier with Capacitive Smoothing



0.2

0

ĺ0

5

10

15

n

 $U_{LL} = 3 \times 400 V$ $f_N = 50 Hz$ $P_{out} = 2.5 kW (R=125 \Omega)$ $C = 1 mF; 40 \mu F$ $X_c/R = 0.025; 0.636$



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40

20

0

-20

-40

20

25

Current (A)

 $u_{\rm pn} (40 \mu F)$

15

Diode Bridge Rectifier / DC-Side Inductor and Output Capacitor



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Diode Bridge Rectifier / AC-Side Inductor and Output Capacitor



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Passive 3rd Harmonic Injection





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Passive 3rd Harmonic Injection



- Minimum THD of Phase Current for i_y = 1/2 I
 THD_{min} = 5 %





Auto-Transformer-Based-12-Pulse Rectifier Systems

■ AC-Side Interphase Transf. (Impr. DC Voltage)



DC-Side Interphase Transf. (Impr. DC Current)



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DC-Side Interphase Transformer can be omitted in Case of Full Transformer Isolation of Both Diode Bridges

Diode Bridge and DC-Side Electronic Inductor (EI)

- + Only Fract. of Output Power Processed+ High Efficiency and Power Density
- Not Output Voltage Control
- EMI Filtering Required

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Diode Bridge and DC-Side Electronic Inductor (EI)

Control Structure

• Current Control could Theoretically Emulate Infinite Inductance Value but Damping (Parallel Ohmic Component) has to be Provided for Preventing Oscillations

Diode Bridge and DC-Side Electronic Inductor (EI)

 $U_{LL} = 3 \times 400 V$ $P_0 = 5 kW$ $f_s = 70 kHz$ $C = 4 \times 330 \mu F / 100 V$

Diode Bridge and DC-Side EI or Electronic Capacitor MERS Concept (Magnetic Energy Recovery Switch)

Fundamental Frequency Equivalent Circuit

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0.25

12-Pulse Rectifier Employing Electr. Interphase Transformer (EIT)

- Switching Frequency DC-Side Inductors
 Proper Control of the EIT Allows to Achieve *Purely Sinusoidal* Mains Current !

Active 3rd Harmonic Injection <u>into All Phases</u>

- No Output Voltage Control
- Mains Current Close to Sinusoidal Shape

e.g.: $i_1 = I + 3/2 i_y$ $i_2 = I - 3/2 i_y$ CCL: $3i_y = i_1 - i_2$

Minnesota Rectifier

- Controlled Output Voltage
- Purely Sinusoidal Shape of Mains Current

Active 3rd Harmonic Injection into All Phases

• Current Control Implemention with Boost-Type DC/DC Converter (*Minnesota Rectifier*) or with Buck-Type Topology

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Active 3rd Harmonic Inj. Only <u>into One Phase</u> (I)

- + Purely Sinusoidal Mains Current (Only for Const. Power Load)
 + Low Current Stress on Active Semicond. / High Efficiency
- + Low Complexity

• T₊, T₋ Could be Replaced by Passive Network

 $i + \bar{i}_{T_+} = G \cdot u_{a0} = i_a$ Sinusoidal Mains Current:

 $=G\frac{u_a \cdot u_{ac} + u_b \cdot u_{bc}}{u_{ac}} = G\left(u_{a0} + u_{b0}\frac{u_{bc}}{u_{ac}}\right)$

 $i = \frac{P}{u_{ac}} = \frac{u_{ac} \cdot i_a + u_{bc} \cdot i_b}{u_{ac}}$

Condition: $i_{a} + i_{b} + i_{c} = 0$ 0

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- $i_v = -i_b$
- Local Avg. Ind. Voltage / Bridge Leg (T_+, T_-) Output Voltage:

- Current to be Inj. Into Phase b:

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- Bridge Leg Voltage Formation:

- Constant Power Load Current:

 $\bar{i}_{T_+} = k \cdot i_y = -k \cdot G \cdot u_{b0} = -G \cdot u_{b0} \frac{\cdots_{bc}}{u_{ac}}$

 $\overline{u}_{L} \approx 0$ and/or $\overline{u}_{20} = u_{b0}$

 $\overline{u}_{20} = u_{b0} = k \cdot u_{a0} + (1 - k)u_{c0}$

 $u_{b0} = k \cdot u_{ac} + u_{c0}$

- Bridge Leg Current Formation:

Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$

$$k = \frac{u_{bc}}{u_{ac}}$$

$$\frac{p}{1 - \frac{p}{1 - p$$

 $i_a = G \cdot u_{a0}$

 $i_b = G \cdot u_{b0}$

 $i = G_{i} \eta$

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► Active 3rd Harmonic Inj. Only <u>into One Phase</u> (II)

Boost-Type Topology

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- + Controlled Output Voltage
- + Purely Sinusoidal Mains Current
- Power Semiconductors Stressed with Line-to-Line and/or Full Output Voltage

- Proof of Sinusoidal Mains Current Shape for $\omega t \in \left| 0, \frac{\pi}{3} \right|$ (1)
- 4 Different Switching States:

$$T_{+} \text{ on, } T_{-} \text{ off }$$

$$k_{1}$$

$$T_{+} \text{ off, } T_{-} \text{ on }$$

$$k_{2}$$

$$T_{+} \text{ off, } T_{-} \text{ off }$$

$$k_{3} = (1 - k_{1} - k_{2})$$

3 Different States Regarding the Current Paths with Relative On-Times k_1 , k_2 , and k_3

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- $k_2 = \frac{u_{ab}}{U_{nn}}$ $k_1 \left(u_{bc} - U_{pn} \right) + k_2 u_{bc} + \left(1 - k_1 - k_2 \right) u_{bc} = 0$ $k_1 = \frac{u_{bc}}{U_{nn}}$ $\overline{i} = \frac{P}{U_{pn}} = \frac{u_{ab}i_a - u_{bc}i_c}{U_{pn}} = -k_1i_c + k_2i_a$ - Constant Power, Load Current: $\bar{i}_{T+} = k_1 i_v^* + (1 - k_1 - k_2) i_a^*$ Condition: $i_a^* + i_b^* + i_c^* = 0$ - Current Formation in T₊: $\overline{i}_{T+} + \overline{i}^* = i_a^*$ Sinusoidal Mains Current:

 $i_{v}^{*} = -i_{b}^{*}$

 $\overline{u}_{L,1}^* \approx 0 \qquad \overline{u}_{L,2}^* \approx 0$

 $k_1 u_{ab} + k_2 (u_{ab} - U_{pn}) + (1 - k_1 - k_2) u_{ab} = 0$

- Bridge Leg (T₊, T₋): Voltage Form.:
- Current to be Injected into b:
- Inductor Voltages:
- Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$ (2)

 $i_a^* = G \cdot u_{a0}$

 $i_b^* = G \cdot u_{b0}$

 $i_c^* = G \cdot u_{c0}$

► Active 3rd Harmonic Inj. Only <u>into One Phase</u> (III)

Buck-Type Topology

- + Controlled Output Voltage
- + Purely Sinusoidal Mains Current
- + Low Current Stress on the Inj. Current Distribution Power Transistors / High Eff.
- + Low Control Complexity
- Higher Number of Active Power Semiconductors than Active Buck-Type PWM Rect. (but Only T+, T_ Operated with Switching Frequency)

- Patent Pending
- Switches Distributing the Injected Current could be Replaced by Passive Network

P=10kW

-20

-30 L 0

5

10

15

20

t (ms)

25

30

35

40

 $T_{-} \} k_2$

Proof of Sinusoidal Mains Current Shape for
$$\omega t \in \left[0, \frac{\pi}{3}\right]$$

 $i_{1} = -i_{1}$

- Current Formation:

$$\begin{array}{ll} i_y &= -i_b & & \text{Duty Cycles:} & T_+ \} k_1 \\ k_1 I = i_a & k_2 I = -i_c & & & \\ i_y = -(1-k_1)I + (1-k_2)I = -i_b & & i_a = G \cdot u_{a0} \\ i_a + i_b + i_c = 0 & & & i_b = G \cdot u_{b0} \\ & & & i_c = G \cdot u_{c0} \end{array}$$

- Voltage Formation:

$$\begin{split} \overline{u}_L &\approx 0 \\ k_1 u_a + (1 - k_1) u_b - (k_2 u_c + (1 - k_2) u_b) &= u_{pn} \\ k_1 u_{ab} - k_2 u_{cb} &= u_{pn} \\ i_a u_{ab} + i_c u_{cb} &= u_{pn} I \\ i_a u_{ab} + i_c u_{cb} &= P \\ i_a u_{ab} + i_c u_{cb} &= P \\ \end{split}$$

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Diode Bridge Combined with DC/DC Boost Converter

 Other Diode Bridge Output Current Impressing DC/DC Converter Topologies (e.g. SEPIC, Cuk) result in Same Mains Current Shape

Half-Controlled Rectifier Bridge Boost Converter

- Sinusoidal Current Control Only in Sectors with 2 Positive Phase Voltages, e.g. in Sector B
- In other Sectors, Only One Phase Current could be Shaped, e.g. in Sector A
- + Controlled Output Voltage (U > √6 Û)
 + Low Complexity (e.g. Single Curr. Sensor)
 + Low Conduction Losses

- Block Shaped Mains Current

Half-Controlled Rectifier Bridge Boost-Type Converter

- Current Control Concepts
- **Option 1: All Switches Simultaneously Controlled with Same Duty-Cycle (Synchr. Modulation)**
- Option 2: Only Phase with most Positive Voltage is Modulated, Switch of Phase with most Neg. Voltage is Cont. Turned on for Lowering Conduction Losses in Case of Switch Implementation with MOSFETs. Middle Phase Switch is OFF; Results in Block Shaped Mains Current

Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

Impressed Diode Bridge Output Voltages

- + Output Voltage Controlled+ Sinusoidal Mains Current Shaping Possible
- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed

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Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

Experimental Results (Impressed Diode Bridge Output Voltages)

Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

Impressed Diode Bridge Output Currents

- + Sinusoidal Mains Current Shaping Possible
- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed
- ► Wide Varity of Further Topologies for Pulse Multiplication (e.g. 12p → 36p) which Process Only Part of Output Power but don't Provide Output Voltage Control

Half-Controlled Rectifier Bridge Buck-Type Converter

- + Controlled Output Voltage
- + Low Complexity
- + Low Conduction Losses
- Block Shaped Mains Current

• Topology Limits Input Current Shaping to Intervals with Positive Phase Voltage

Sector 1: Only i_a could be Controlled Sector 2: i_a and i_b could be Controlled

• Low Complexity Control: Only Current of Phase with most Positive Voltage Controlled; Switch of Phase with most Neg. Voltage Turned On Cont. for Providing a Free-Wheeling Path

Classification of Unidirectional Rectifier Systems





Phase-Modular Rectifier Topologies

Y-Rectifier





- Individual DC Output Voltages of the Phase Units
 Isolated DC/DC Converter Stages Required for Forming Single DC Output





► Y-Rectifier



• Basic AC-Side Behavior Analogous to Direct Three-Phase Three-Level Rectifier Systems



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► Y-Rectifier

Cond. States for $i_a>0$, $i_b<0$, $i_c<0$ in Dep. on Transistor Switching States ($S_a S_b S_c$)



Switching States (011) and (100)

- Redundant Concerning Formation of $u_{\bar{a}\bar{b}}, u_{\bar{b}\bar{c}}, u_{\bar{c}\bar{a}}$
- Inverse Concerning Charging of C_a and C_c (and C_b)



► Y-Rectifier

Equivalent Circuit and Voltage Formation



$$u_{\overline{a}} = \overline{u}_{\overline{a}} + u_{\overline{a},\sim}$$
$$u_{\overline{b}} = \overline{u}_{\overline{b}} + u_{\overline{b},\sim}$$
$$u_{\overline{c}} = \overline{u}_{\overline{c}} + u_{\overline{c}} \sim$$

$$u_{\overline{a}} = u'_{\overline{a}} + u_0 \qquad u'_{\overline{a}} + u'_{\overline{b}} + u'_{\overline{c}} = 0$$
$$u_{\overline{b}} = u'_{\overline{b}} + u_0$$
$$u_{\overline{c}} = u'_{\overline{c}} + u_0$$

$$\overrightarrow{u}_{\overline{a}} = \overline{u}'_{\overline{a}} + \overline{u}_{0}$$
$$u_{\overline{a},\sim} = u'_{\overline{a},\sim} + u_{0,\sim}$$

(shown at the Example of Phase a)



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► Y-Rectifier

Equivalent Circuit and Voltage Formation



• Voltage of the Star Point N' Defined by u₀ (CM-Voltage)



► Y-Rectifier

Modulation and Voltage Formation



• Addition of m_0 Increases Modulation Range from $\hat{U}_a = U$ to $\hat{U}_a = 2/\sqrt{3}U$

• Potential of Star Point N' Changes with LF (\overline{u}_0) and Switching Frequency ($u_{0,\sim}$)



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► Y-Rectifier

 Balancing of Phase-Module DC-Output Voltages by DC Component of u₀ (m
₀)



- \overline{m}_0 Only Changes the On-Time of Redundant Switching Stages, e.g. (100) and (011)
- No Influence on the AC-Side Current Formation- Allows Balancing of the Module Output Voltages Independent of Input Current Shaping



► Y-Rectifier

Control Structure / 2-out-of-3 Output Voltage Balancing





 $\frac{\pi}{3}$

ωt

► Y-Rectifier

Experimental Verification of Output Voltage Balancing

- Symm. Loading P_a = P_b = P_c = 1000 W
 Asymm. Loading P_a = 730 W, P_b = P_c = 1000 W

 $U_{\rm N} = 3 \times 230 \text{ V} (50 \text{ Hz})$ $P_{\rm o} = 3 \times 1 \text{ kW}$ $U_{o} = 400 V$ $f_{s} = 58 \text{ kHz}$ *L* = 2.8 mH (on AC-side) $C = 660 \, \mu F$



VDC.T

VDC.S

VDC.R

10

Input Phase Currents, Control Signal i_0 , Output Voltages





Symm. Loading

Asymm. Loading

i_{N,i}: 1 A/div

 V_{DC_i} : 100 V/div



• Δ -Rectifier



• Connection of Each Module to All Phases / Rated Power also Available for Phase Loss !



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\blacktriangleright Δ -Rectifier

Derivation of Equivalent Circuit / Circulating Current Component i₀



$$u_{\overline{a}b} = u'_{\overline{a}b} + u_0$$
$$u_{\overline{b}c} = u'_{\overline{b}c} + u_0$$
$$u_{\overline{c}a} = u'_{\overline{c}a} + u_0$$



Def.: $u'_{\overline{a}b} + u'_{\overline{b}c} + u'_{\overline{c}a} = 0$

- Mains Phase Current Formed by $u'_{\overline{a}b}$, $u'_{\overline{b}c}$, $u'_{\overline{c}a}$ and u_a , u_b , u_c
- Circulating Current *i*₀ Formed by *u*₀

$$u_0 = \frac{1}{3} \left(u_{\overline{a}b} + u_{\overline{b}c} + u_{\overline{c}a} \right)$$

 u₀ and/or i₀, which does not Appear in i_a, i_b and i_c, can be Maximized by Proper Synchron. of Module PWM Carrier Signals; Accordingly, Switching Frequency Components of u'_{ab}, u'_{bc} and u'_{ca} are Minimized







\blacktriangleright Δ -Rectifier

Y-Equivalent Circuit Describing Mains Current Formation

• Equiv. Conc. No-Load Voltage at Terminals a, b, c (No Circ. Current i_0 , i.e. No Voltage Drop across L_{Δ}

$$u_{ab} = u'_{\overline{a}b} = u_{\overline{a}'} - u_{\overline{b}'}$$
$$u_{bc} = u_{\overline{b}c} = u_{\overline{b}'} - u_{\overline{c}'}$$

• Equiv. Y-Voltage Syst. should not Contain Zero Sequ. Comp.



• Equiv. Concerning Input Impedance between any Terminals



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Circulating Current Max. / Minimization of Mains Current Ripple

 $U_{LL} = 3 \times 480 \text{ V} (50 \text{ Hz})$ $P_0 = 5 \text{ kW}$ $U_0 = 800 \text{ V}$ $f_s = 25 \text{ kHz}$ L = 2.1 mH (on AC-Side)

• For Proper Phase Shift of Module PWM Carrier Signals a Share of the Line-to-Line Current Ripple can be Confined into the Delta Connection.





\blacktriangleright Δ -Rectifier

Experimental Results

 $U_{LL} = 3 \times 480 \text{ V} (50 \text{ Hz})$ $P_0 = 5 \text{ kW}$ $U_0 = 800 \text{ V}$ $f_s = 25 \text{ kHz}$ L = 2.1 mH (on AC-Side)





 $i_{a^{\prime}}, i_{\bar{a}b^{\prime}}, i_{\bar{c}a}: 5 \text{ A/div}; \qquad i_{a}\text{-}i_{a,(1)}\text{, } i_{0}\text{: 2 A/div}$

- Formation of Input Phase Current $i_a = i_{\overline{a}b} i_{\overline{c}a}$
- Circulating Zero Sequence Current i_0



Coffee Break !





Classification of Unidirectional Rectifier Systems



Single-Switch + Boost-Type DCM Converter Topology

- + Low Complexity / Single Switch+ No PWM, Constant Duty Cycle Operation
- + No Current Measurement
- High Peak Current Stress
- Low Frequ. Distortion of Mains Currents / Dep. on U_{pn}/\hat{U}
- High EMI Filtering Effort



- Improvement of Mains Current Shape by 6th Harmonic Duty Cycle Modulation or Boundary Mode Operation
- Reduction of EMI Filtering Effort by Interleaving

 $U_{LL} = 3 \times 400 \text{ V} (50 \text{Hz})$ $P_0^{LL} = 2.5 \text{ kW}$ $U_0 = 800 \text{ V}$ **THD**_i = 13.7 %





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Two Interleaved Single-Switch Boost-Type DCM Converter Stages



- + Interleaving Reduces Switching Frequency Input Current Ripple
 + For Low Power Only One Unit Could be Operated Higher Efficiency
- Low Frequency Mains Current Distortion Still Remaining
 Relatively High Implementation Effort



Two-Switch Boost-Type DCM Converter Topology



Classification of Unidirectional Rectifier Systems



<u>Two-Level</u> CCM Boost-Type PFC Rectifier Systems

- Y-Switch Rectifier
 Δ-Switch Rectifier



► Y-Switch Rectifier



• Proper Control of Power Transistors Allows Formation of PWM Voltages at \overline{a} , \overline{b} , \overline{c} and/or Impression of Sinusoidal Mains Current



► **Δ-Switch Rectifier**



- Δ -Switch Rectifier Features Lower Conduction Losses Compared to Y-Switch System
- Active Switch Could be Implemented with Six-Switch Power Module









► **Δ-Switch Rectifier**

Equivalent Circuit / Mains Current Control

• Reference Voltages, i.e. the Output of the Phase Current Controllers Need to be Transformed into \triangle -Quantities



- Mains Currents Controlled in Phase with Mains Voltages u_a, u_b, u_c
- Voltage Formation at a, b, c is Determined by Switching State of $S_{\overline{a}\overline{b}\overline{a}}$, $S_{\overline{b}\overline{c}\overline{b}}$, $S_{\overline{c}\overline{a}\overline{c}}$ and AND Input Current Direction/Magnitude
- Always Only Switches Corresponding to Highest and Lowest Line-to-Line Voltage are Pulsed
- Switch of Middle Phase Turned Off Continuously



• Δ -Switch Rectifier

Modulation

 $U_{LL} = 115 V (400 Hz)$ $P_0 = 5 kW$ $U_0 = 400 V$ $f_S = 72 kHz$

Power Density: 2.35 kW/dm³







\blacktriangleright Δ -Switch Rectifier

Experimental Analysis

 $U_{LL} = 115 V (400Hz)$ $P_0 = 5 kW$ $U_0 = 400 V$ $f_S = 72 kHz$

Power Density: 2.35 kW/dm³





<u>Three-Level</u> Boost-Type CCM PFC Rectifier System

• Derivation of Circuit Topologies





Derivation of Three-Level Rectifier Topologies (1)



• Sinusoidal Mains Current Shaping Requires Independent Controllability of the Voltage Formation of the Phases



Derivation of Three-Level Rectifier Topologies (2)



 $+\frac{1}{2}U$ R $u_{\rm pn}$ $-\frac{1}{2}U$



- Three-Level Characteristics
- + Low Input Inductance Requ.

 $+\frac{1}{2}U$

- + Low Switching Losses,
- + Low EMI
- Higher Circuit Complexity
 Control of Output Voltage Center Point Required









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Three-Level PFC Rectifier Analysis

- Input Voltage Formation
- Modulation / Sinusoidal Input Current Shaping
- Output Center Point Formation
- Control
- Design Considerations
- EMI Filtering
- Digital Control
- Experimental Analysis





Input Voltage Formation



• Voltage Formation

$$u_{\overline{a}M} = (1 - s_a) \operatorname{sign}(i_a) \frac{U}{2}$$

is Determined by Phase Switching State AND Direction of Phase Current



 $s_a = 0$ $T_{a+}, T_{a-}: OFF$ $u_{\overline{a}M} = -\frac{1}{2}U$





 $s_a = 1$ $T_{a+}, T_{a-}: ON$ $u_{\overline{a}M} = 0$



Semiconductor Blocking Voltage Stress

Blocking Voltage Definition

- D_{F+} : Limited to U_+ via Parasitic Diode of T_{a+}
- D_{N+}: Not Dir. Def. by Circuit Structure
- D_N.: Not Dir. Def. by Circuit Structure
- *D*_{F-}: Limited to *U*₋ via Paras. Diode of *T*_{a-}
- T_{a+}: Limited to U₊ via D_{F+}
- Ta-: Limited to U_ via DF-



 $u_{\bar{a}M} = -\frac{1}{2}U$







 $s_a = 1$ $T_{a+}, T_{a-}: ON$ $u_{\overline{a}M} = 0$



Impression of Input Current Fund. (Ohmic Fund. Mains Behavior)





IPC/

PWM / Formation of \bar{u}_{a} , \bar{u}_{b} , \bar{u}_{c} / AC-Side Equiv. Circuit (1)

• Def. of Modulation Index:

$$M = \frac{\hat{U}_{\overline{a}}}{\frac{1}{2}U} \qquad \left(0 \dots \frac{2}{\sqrt{3}}\right)$$

• Zero-Sequence Signal to Achieve Ext. Mod. Range

$$u_{\overline{a}\,0} = u'_{\overline{a}} + u_{0} \qquad u'_{\overline{a}} + u'_{\overline{b}} + u'_{\overline{c}} = 0$$

$$u_{\overline{b}\,0} = u'_{\overline{b}} + u_{0} \qquad u_{0} = \frac{1}{3} \Big(u_{\overline{a}\,0} + u_{\overline{b}\,0} + u_{\overline{c}\,0} \Big)$$

• Generation of *u*₀, *i.e.* 3rd Harmonic Signal







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PWM / Formation of \bar{u}_{a} , \bar{u}_{b} , \bar{u}_{c} / AC-Side Equiv. Circuit (2)

$\overline{u}_a', \overline{u}_b', \overline{u}_c'$	Impression of Mains Current Fundamental in Combination with <i>u_a</i> , <i>u_b</i> , <i>u_c</i>	$u'_{\overline{a}} = u_{\overline{a}N'}$ $u'_{\overline{b}} = u_{\overline{b}N'}$ $u'_{\overline{c}} = u_{\overline{c}N'}$	$= \overline{u}_{\overline{a}}' + u_{\overline{a}}_{\sim}$ $= \overline{u}_{\overline{b}}' + u_{\overline{b}}_{\sim}$ $= \overline{u}_{\overline{c}}' + u_{\overline{c}}_{\sim}$
$\overline{u}_{a^{\sim}}^{\prime},\overline{u}_{b^{\sim}}^{\prime},\overline{u}_{c^{\sim}}^{\prime}$	Causing the Switching Frequ. Ripple of the Mains Currents and/or DM Filtering Requirement	Note:	$u_{NN'} = 0$
		$u_{\overline{a}0} = u'_{\overline{a}}$	+ <i>u</i> ₀
		$u_{\overline{b}0} = u_{\overline{b}}' + u_0$	
		$u_{\overline{c}0} = u_{\overline{c}}' + u_0$	
<u>u</u> 0	Low Frequency Zero Sequence Component for Extending the Modulation Range from $M = 01$ (Sinusoidal Modulation) to $M = 0\frac{2}{\sqrt{3}}$	u ₍	$u_0 = \overline{u}_0 + u_{0\sim}$
<i>u</i> _{0~}	Switching Frequency CM Voltage Fluctuation of the Output → Resulting in CM Current and/or CM Filtering Requirement		




• Time Behavior of the Components of Voltages $u_{\overline{a}}$, $u_{\overline{b}}$, $u_{\overline{c}}$



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Local Average Value of Center Point Current

• Derivation of Low-Frequency Component \overline{i}_M of Center Point Current Assuming a 3rd Harmonic Component of u_0 as Employed for Increasing the Modulation Range)

 $m_a = m'_a + m_0 = M_1 \cdot \cos(\omega t) + M_3 \cdot \cos(3\omega t)$ $m_b = m'_b + m_0 = M_1 \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$ $M_1 = \frac{U}{\frac{1}{2}U}$ $M_3 = \frac{U_0}{\frac{1}{2}U}$ $m_c = m'_c + m_0 = M_1 \cdot \cos\left(\omega t + \frac{2\pi}{3}\right) + M_3 \cdot \cos\left(3\omega t\right)$ $\alpha_a = 1 - m_a$ (relative on-time of T_{a+}) $\overline{i}_M = \alpha_a \cdot i_a + \alpha_b \cdot i_b + \alpha_c \cdot i_c$ $\alpha_b = 1 - m_b$ (relative on-time of T_{b+}) $=(1-m_a)\cdot i_a + (1-m_b)\cdot i_b + (1-m_c)\cdot i_c$ $\alpha_c = 1 - m_c$ (relative on-time of T_{c+}) RMS of \overline{i}_M minimal for $\frac{M_3}{M_4} \approx \frac{1}{4}$ • m_0 , i.e. PWM incl. 3rd Harm., Reduces \overline{i}_M and Extends the Modulation Range



Assumption: $i_a > 0, i_b < 0, i_c < 0$



Cond. States within a Pulse Period / Center Point Current Formation

- **Consider e.g.** $i_a > 0, i_b < 0, i_c < 0$
- Switching States (100), (011) are Forming Identical Voltages $u'_{\overline{a}}, u'_{\overline{b}}, u'_{\overline{c}}$ but Inverse Centre Point Currents i_M
- Control of i_M by Changing the Partitioning of Total On-Times of (100) and (011)







 i_M

System Control

- Control Structure
- Balancing of the Partial Output Voltages



Control Structure



- Output Voltage Control Mains Phase Current Control
- Control of Output Center Point Potential (Balancing of U₊, U₋)
- Control of i_a, i_b, i_c Relies on u_a, u_b, u_c
 Control of u_M Relies on u₀ (DC Component)
 No Cross Coupling of both Control Loops





Control of Potential *u*_M of Output Voltage Center Point

• Assumption: $i_a > 0$, $i_b < 0$, $i_c < 0$



• Control via DC Component of u_0 , i.e. by Adding m_0 to the Phase Modulation Signals i.e. by Inversely Changing the Rel. On-Times of (100) and (011), $\delta_{(100)}$ and $\delta_{(011)}$, without taking Influence on the Total On-Time $\delta_{(100)} + \delta_{(011)}$.



Control of Output Voltage Center Point Potential u_M



- Output Voltage Unbalance Results in Increasing On-Time of T_{a^+} and Decreasing Off-Times of T_{b^-} and T_{C^-} so that the Voltages $\overline{u'}_{\overline{a}}$, $\overline{u'}_{\overline{b}}$, $\overline{u'}_{\overline{c}}$ are Formed as in the Symmetric Case ($\Delta U = 0$) and/or the Mains Phase Currents Remain at Sinusoidal Shape
- Resulting \bar{i}_M Reduces ΔU , i.e. Self Stability Guaranteed





► Admissible Unbalance of Loading of U₊ and U₋



• System Tolerates Load Unbalance Dependent on the Voltage Transfer Ratio $(U_+ + U_-)/\hat{U}$ and/or the Value of The Modulation Index M

Design Guidelines

- Current Stress on the Components
 Transistor Selection
- Output Pre-Charging at Start-up



Current Stress on Power Semiconductors

6-Switch Circuit Topology



- Output Voltage > √3 Û_{max} (typ. 1.2 √3 Û_{max}); Û_{max}: Ampl. of Max. Mains Phase Voltage
 Required Blocking Capability of All Semiconductors: ½ U



Current Stress on Power Semiconductors

3-Switch Circuit Topology



- Output Voltage > $\sqrt{3} \hat{U}_{max}$ (typ. 1.2 $\sqrt{3} \hat{U}_{max}$); \hat{U}_{max} : Ampl. of Max. Mains Phase Voltage Required Blocking Capability of All Semiconductors: $\frac{1}{2}$ U



► Nonlin. C_{oss} of Superjunct. MOSFETs Causes Input Curr. Distortion



- Nonlinear Output Capacitance C_{oss} of MOSFET (CoolMOS) has to be Charged at Turn-off
- Large Turn-Off Delay for Low Currents (e.g. Delay of CoolMOS IPP60R099 (@ IDS = 1.3 A): 11% of Switching Cycle @ fs = 500 kHz
- Results in PWM Volt. and/or Input Curr. Distortion







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Pre-Charging of Output Capacitors / Start-Up Sequence

- Lower Mains Diode D_{N-} is Replaced by Thyristor
 Inrush Current is Limited by R_{pre}
 Switches are not Gated During Start-Up
 Start-up Sequence is Required





EMI Filtering

- DM Filtering
 CM Filtering





EMI Filtering Concept

- DM and CM Filter Stages
- Connection of Output Voltage Midpoint *M* to Artificial Mains Star-Point *N'*
- → No High-Frequency CM-Voltage at *M*
- → Capacitance of C_{FB} Not Limited by Safety Standards
- Parasitic Capacitances have to be Considered for CM-Filter Design







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DM Filter Design

• DM Equivalent Circuit

• Required DM Attenuation, e.g. for fs = 1 MHz (VR1000)



• DM Filter Structure





CM Filter Design

• CM Equivalent Circuit







• **Required CM Attenuation**



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EMI Filter Structure for VR1000 Rectifier System

• 3 Stage DM Filter

• 2 Filter Stages for CM Filter



3 x CM Inductors in Series to Implement Proposed Filter Concept
 Additional CM Filter Stage Required Due to Parasitic Capacitances





EMI Filter Design

- Analytical Approximation
 Volume / Efficiency Optimization



Considered System



Goal

Tasks

- \rightarrow Meet Conducted EMI Standards (e.g. CISPR 11, Class A or Class B)
- Find Needed Filter Attenuation
 Design Filter Accordingly



Calculate Required Filter Attenuation



DM Attenuation

→ Determine Filter Attenuation such that Test Receiver Output is Below EMI Limits at all Frequencies

Challenges

- → Determine Spectrum of VDM and VCM
- \rightarrow Computationally Intensive Test Receiver Modeling





CM and DM Voltage Formation / Time Behavior



Voltage *V*_a splitted into LF and High Frequency Components



Simplified Calculation of Required Filter Attenuation



- \rightarrow Model of Test Receiver is Omitted
- → Harmonic Power Concentrated only @ Switching Frequency → VDM,rms can be Calculated in Time Domain



Simplified Calculation of Required Filter Attenuation



- \rightarrow Model of Test Receiver is Omitted
- → Harmonic Power Concentrated only @ Switching Frequency f_P → $V_{DM,rms}$ can be Calculated in Time Domain

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Simplified Calculation of Required Filter Attenuation



 $A_{\text{filter}}(f_D)[dB\mu V] = V_{\text{est}}(f_D)[dB\mu V] - \text{Limit}(f_D)[dB\mu V] + \text{Margin}(f_D)[dB\mu V]$



Shown for DM Filter



Optimal Selection of Current Ripple Ratio k (f_P = const.)

→ High Ripple Current in L_{Boost} (→ high k) requires Large CLC-filter; in Return the L_{boost} is Small → Small Ripple Current in L_{Boost} (→ small k) requires Large L_{boost} ; in Return the CLC-filter is Small

Shown for DM Filter



- Optimal Selection of Switching Frequency f_P (k = const.)
- → High Switching Frequency requires Large CLC-filter; in Return the L_{boost} is Small → Low Switching Frequency requires Large L_{boost} ; in Return the CLC-filter is Small





Optimization Result for DM Filter of a Single-Phase Boost-Type PFC Rectifier





Optimization Result for DM Filter of a Single-Phase Boost-Type PFC Rectifier



Experimental Analysis

- Power Density / Efficiency Pareto Limit
 Experimental Analysis VR250



Experimental Analysis

■ Generation 1 – 4 of VIENNA Rectifier Systems

 Switching Frequency of f_s = 250 kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality THD_i







Demonstrator – VR250 (1)

• Specifications

 $U_{LL} = 3 \times 400 V$ $f_N = 50 Hz \dots 60 Hz \text{ or } 360 Hz \dots 800 Hz$ $P_0 = 10 kW$ $U_0 = 2 \times 400 V$ $f_s = 250 \text{ kHz}$

• Characteristics

η = 96.8 % THD_i = 1.6 % @ 800 Hz 10 kW/dm3 3.3 kg (≈3 kW/kg)

Dimensions: 195 x 120 x 42.7 mm³





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Demonstrator – VR250 (2)

• Specifications

 $U_{LL} = 3 \times 400 V$ $f_N = 50 Hz \dots 60 Hz \text{ or } 360 Hz \dots 800 Hz$ $P_o = 10 kW$ $U_o = 2 \times 400 V$ $f_s = 250 \text{ kHz}$

• Characteristics

η = 96.8 % THD_i = 1.6 % @ 800 Hz 10 kW/dm3 3.3 kg (≈3 kW/kg)

Dimensions: 195 x 120 x 42.7 mm³





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• Mains Behavior @ f_N = 50 Hz







Mains Behavior @ f_N = 400Hz / 800Hz







Demonstrator Performance (VR250)

• Input Current Quality @ f_N = 800 Hz



• Efficiency @ f_N = 800 Hz




Demonstrator (VR250) Control Behavior







Demonstrator (VR250) EMI Analysis



• DM Emissions







Evaluation of Boost-Type Systems

3rd Harmonic Inj. Rectifier ∆-Switch Rectifier Vienna-Rectifier Six-Switch Rectifier





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Boost-Type PFC Rectifiers

- 3rd Harmonic Inj. Type
 Diode Bridge Conduction Modulation





Boost-Type PFC Rectifiers

■ 3rd Harmonic Inj. Type → Limited Operating Range

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Boost-Type PFC Rectifiers

△-Switch Rectifier
 → System Complexity







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Vienna Rectifier vs. Six-Switch Rectifier



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Buck-Type CVM PFC Rectifier System

• Derivation of Circuit Topologies



Derivation of the Circuit Topology (1)

Insertion of Switches in Series to the Diodes



- + DC Current Distribution to Phases a, b, c
- can be Controlled + Control of Output Voltage $0 \le u \le \frac{3}{2}\hat{U}$

- Pulsating Input Currents / EMI Filtering Requ.
 Relatively High Conduction Losses



Derivation of the Circuit Topology (2)



• Insertion of 4Q-Switches on the AC-Side in Order to Enable Control of the DC Current Distribution to Phases *a*, *b*, *c*



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Derivation of the Circuit Topology (3)

Circuit Extensions



- Integration of Boost-Type Output Stage
- Wide Output Voltage Range, i.e. also $U > \frac{3}{2}\hat{U}$
- Sinusoidal Mains Current also in Case of Phase Loss

$C \perp_{\pm} u_{pn} \square R$ |u| $\perp C_a$ L L $C \stackrel{+}{=} u_{pn} \prod R$ $C \stackrel{+}{=} |u_{pn}| R$ n n $\perp C_{a}$ = C

L

■ Circuit Extensions Shown for 3-Switch Topology, but is also Applicable to 6-Switch Topology



Buck-Type PFC Rectifier Analysis

- Modulation
- Input Current Formation
 Output Voltage Formation
 Experimental Analysis



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Modulation Scheme

- Consider 60°-Wide Segment of the Mains Period; Suitable Switching States Denominated by (s_a, s_b, s_c)
- Clamping to Phase with Highest Absolute Voltage Value, i.e.
- Phase *a* for $\omega t \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right)$,
- Phase *c* for $\omega t \in \left(+\frac{\pi}{6}, +\frac{\pi}{2}\right)$ etc.
- Assumption: $\omega t \in \left(0, +\frac{\pi}{6}\right)$





(011)

 $^{\circ}a$

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• Clamping and "Staircase-Shaped" Link Voltage in Order to Minimize the Switching Losses





Input Current and Output Voltage Formation (1)



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Input Current and Output Voltage Formation (2)



- Output Voltage Formation:

$$\overline{u} = u_{ab} \cdot \alpha_b + u_{ac} \cdot \alpha_c$$

$$P_{\text{link}} = P_{\text{input}}$$

$$\overline{u} \cdot I = \frac{3}{2} \cdot \hat{U} \cdot \hat{I}^*$$

$$\overline{u} = \frac{3}{2} \cdot \hat{U} \cdot \frac{\hat{I}^*}{I} = \frac{3}{2} \cdot \hat{U} \cdot M$$

- Output Voltage is Formed by Segments of the Input Line-to-Line Voltages
- Output Voltage Shows Const. Local Average Value





Experimental Results

Ultra-Efficient Demonstrator System

 $U_{LL} = 3 \times 400 \text{ V} (50 \text{ Hz})$ $P_0 = 5 \text{ kW}$ $U_0 = 400 \text{ V}$ $f_s = 18 \text{ kHz}$ $L = 2 \times 0.65 \text{ mH}$

η = 98.8% (Calorimetric Measurement)







Experimental Results

Ultra-Efficient Demonstrator System

 $U_{LL} = 3 \times 400 \text{ V} (50 \text{ Hz})$ $P_0 = 5 \text{ kW}$ $U_0 = 400 \text{ V}$ $f_s = 18 \text{ kHz}$ $L = 2 \times 0.65 \text{ mH}$

η = 98.8% (Calorimetric Measurement)





Comparison of Buck-Type Systems

Six-Switch Rectifier SWISS-Rectifier



Buck-Type PFC Rectifiers





Buck-Type PFC Rectifiers







SWISS Rectifier vs. Six-Switch Rectifier





Summary of Unidirectional PFC Rectifier Systems

- Block Shaped Input Current Systems
- Sinusoidal Input Current Systems







Boost-Type

0

 $U > \sqrt{3} \hat{U}$

 $u_{\rm pn}$









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Sinusoidal Input Current Rectifier Systems (1)





Sinusoidal Input Current Rectifier Systems (2)





Bidirectional PFC Rectifier Systems

- Boost-Type Topologies
 Buck-Type Topologies





Boost-Type Topologies



Classification of Bidirectional Boost-Type Rectifier Systems



- Active NPC (ANPC) Converter
- Bridge-Leg Inductor (BLI) Converter



Derivation of Two-Level Boost-Type Topologies

• Output Operating Range







Derivation of Three-Level Boost-Type Topologies







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Comparison of Two-Level/Three-Level NPC Boost-Type Rectifier Systems



- Two-Level Converter Systems
- + State-of-the-Art Topology for LV Appl.
- + Simple, Robust, and Well-Known
- + Power Modules and Auxiliary Components Available from Several Manufacturers
- Limited Maximum Switching Frequency
- Large Volume of Input Inductors



- Two-Level \rightarrow Three-Level Converter Systems
- + Reduction of Device Blocking Voltage Stress
- + Lower Switching Losses
- + Reduction of Passive Component Volume
- Higher Conduction Losses
- Increased Complexity and Implementation Effort





Active Neutral Point Clamped (ANPC) Three-Level Boost-Type System



- + Active Distribution of the Switching Losses Possible
 + Better Utilization of the Installed Switching Power Devices
- Higher Implementation Effort Compared to NPC Topology





T-Type Three-Level Boost-Type Rectifier System



- + Semiconductor Losses for Low Switching Frequencies Lower than for NPC Topologies
- + Can be Implemented with Standard Six-Pack Module
- Requires Switches for 2 Different Blocking Voltage Levels





Three-Level Flying Capacitor (FC) Boost-Type Rectifier System



- + Lower Number of Components (per Voltage Level)
 + For Three-Level Topology only Two Output Terminals
- Volume of Flying CapacitorsNo Standard Industrial Topology





Three-Level Bridge-Leg Inductor (BLI) Boost-Type Rectifier System



- + Lower Number of Components (per Voltage Level)
 + For Three-Level Topology only Two Output Terminals

- Additional Volume due to Coupled Inductors
 Semiconductor Blocking Voltage Equal to DC Link Voltage




Pros and Cons of Three-Level vs. Two-Level Boost-Type Rectifier Systems

- + Losses are Distributed over Many Semicond.
 Devices; More Even Loading of the Chips →
 Potential for Chip Area Optimization for Pure Rectifier Operation
- + High Efficiency at High Switching Frequency
- + Lower Volume of Passive Components
- More Semiconductors
- More Gate Drive Units
- Increased Complexity
- Capacitor Voltage Balancing Required
- Increased Cost

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• Moderate Increase of the Component Count with the T-Type Topology

Consideration for 10kVA/400V_{AC} Rectifier Operation; Min. Chip Area, $T_{j,max}$ = 125°C

Multi-Level Topologies are Commonly Used for Medium Voltage Applications but Gain Steadily in Importance also for Low-Voltage Renewable Energy Applications



Buck-Type Topologies



Derivation of Unipolar Output Bidirectional Buck-Type Topologies

• Output Operating Range





• System also Features Boost-Type Operation





'n

 u_{pn} U $-I_{max}$ $+I_{max}$

Derivation of Unipolar Output Bidirectional Buck-Type Topologies





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Final Remarks

Performance Trends Multi-Objective Optimization



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Power Electronics Performance Trends

- Performance Indices
- Power Density [kW/dm³]
 Power per Unit Weight [kW/kg]
 Relative Costs [kW/\$]
- Relative Losses [%]
- Failure Rate [h-1]





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Technology Sensitivity Analysis Based on η-ρ-Pareto Front

Sensitivity to Technology Advancements Trade-off Analysis







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Converter Performance Evaluation Based on η - ρ - σ -Pareto Surface

▶ **σ**: kW/\$







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Converter Performance Evaluation Based on η - ρ - σ -Pareto Surface

Technology Node'





Thank You!



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Questions ?



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About the Instructors



Johann W. Kolar (F⁻10) received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel converter topologies and modulation/control concepts, e.g., the VIENNA Rectifier, the Swiss Rectifier, and the three-phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 450 scientific papers in international journals and conference proceedings and has filed more than 85 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for data centers, More-Electric-Aircraft and distributed renewable energy systems, and on Solid-State Transformers for Smart Microgrid Systems. Further main research areas are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC and GaN), micro power electronics and/or Power Supplies on Chip, multi-domain/scale modeling/simulation and multiobjective optimization, physical model-based lifetime prediction, pulsed power, and ultra-high speed and bearingless motors. He has been appointed an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, the IEEE IECON Best Paper Award of the IES PETC in 2009, the IEEE PELS Transaction Prize Paper Award 2009, the Best Paper Award of the IEEE/ASME Transactions on Mechatronics 2010, the IEEE PELS Transactions Prize Paper Award 2010, the Best Paper 1st Prize Award at the IEEE ECCE Asia 2011, and the 1st Place IEEE IAS Society Prize Paper Award 2011 and the IEEE IAS EMC Paper Award 2012. Furthermore, he received the ETH Zurich Golden Owl Award 2011 for Excellence in Teaching. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003.

He initiated and/or is the founder/co-founder of 4 spin-off companies targeting ultra-high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.



About the Instructors (Cont'd)



Jonas Mühlethaler (M'09) received his M.Sc. in 2008 and the Ph.D. degree in 2012, both in electrical engineering and both from the Swiss Federal Institute of Technology Zurich (ETHZ), Switzerland. During his master studies, he focused on power electronics and electrical machines. In his M.Sc. thesis, which he wrote at ABB Corporate Research in Sweden, he worked on compensating torque pulsation in Permanent Magnet Motors. In 2008 he joined the Power Electronic Systems Laboratory (PES), ETHZ, to work towards his Ph.D. degree. During the Ph.D. studies, which he finished in 2012, he worked on modeling and multi-objective optimization of inductive power components. Currently, he is working as a Postdoctoral Fellow at PES. Dr. Mühlethaler is the author of 13 conference and Transactions papers and a Member of the IEEE.

