ETH
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Comprehensive Evaluation of Three-Phase AC-AC PWM Converter Systems

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Outline

60 Min
- Review of AC-DC-AC Converters
- Derivation of Basic MC Topologies

15 Min
- 

50 Min
- MC Dimensioning
- Extended MC Topologies

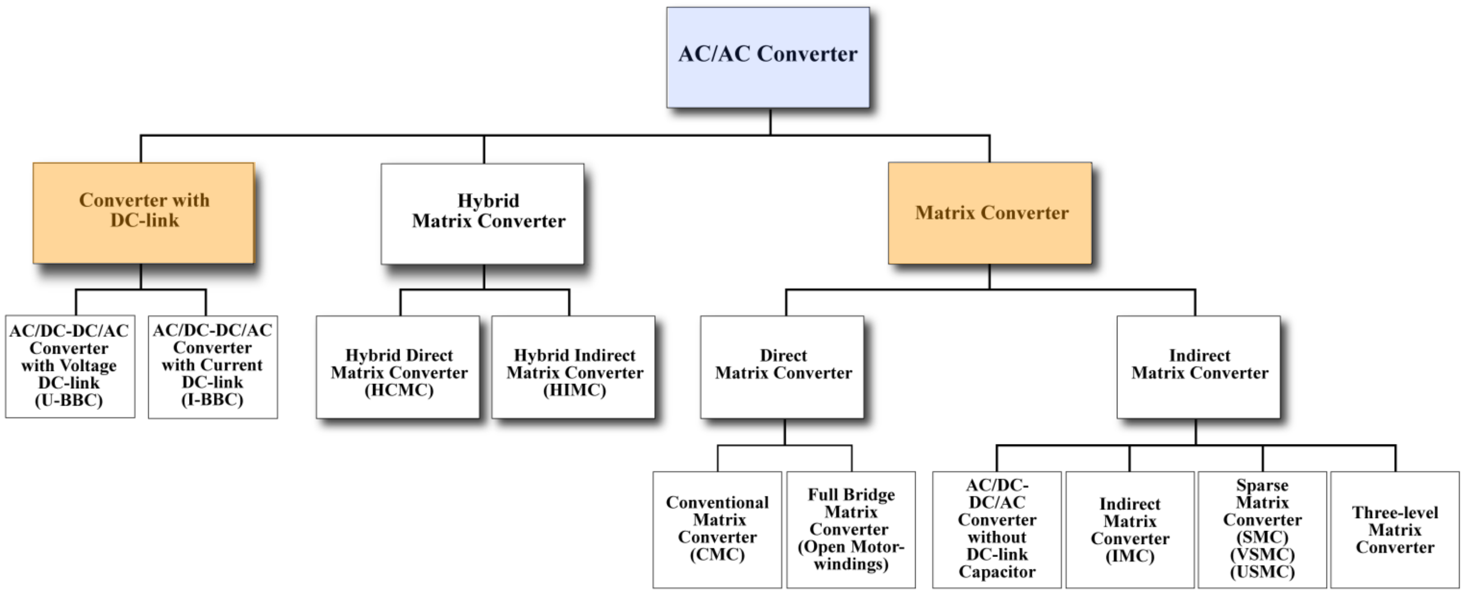
15 Min
- 

45 Min
- Methodology for Converter Comparisons
- Comparative Evaluation of AC-AC Converters

15 Min
- 

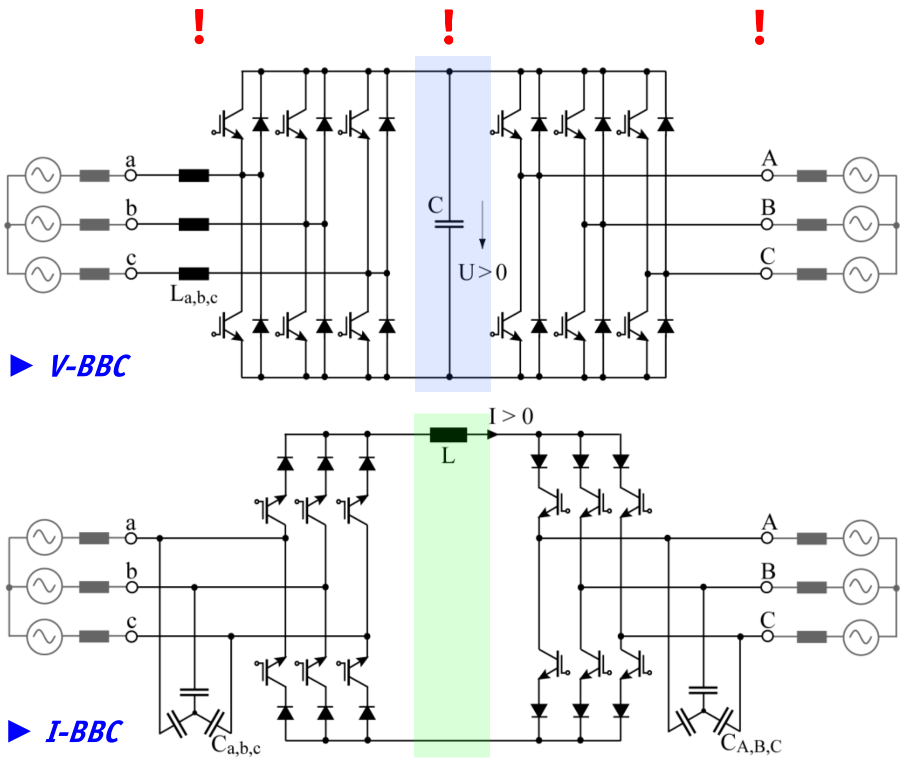
40 Min
- Multi-Domain Simulator Demonstration (GECKO) GeckoCIRCUITS
- Conclusions / Questions / Discussion

Classification of Three-Phase AC-AC Converters



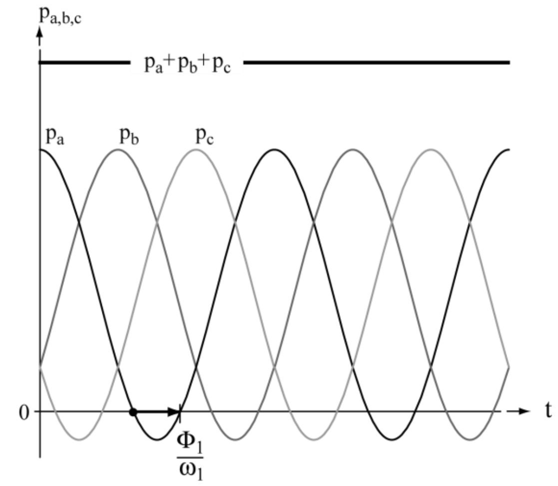
- *Converters with DC-link*
- *Hybrid Converters*
- *Indirect / Direct Matrix Converters*

DC-link AC-AC Converter Topologies



- ***V-BBC***
- ***I-BBC***

$$P = \frac{3}{2}\hat{U}_1 \cdot \hat{I}_1 \cos\Phi_1$$



Symmetric Three-Phase Mains

Phase Voltages

$$
\begin{aligned}
u_a &= \hat{U}_1 \cos(\omega_1 t) \\
u_b &= \hat{U}_1 \cos\left(\omega_1 \left(t - \frac{T}{3}\right)\right) \\
u_c &= \hat{U}_1 \cos\left(\omega_1 \left(t + \frac{T}{3}\right)\right)
\end{aligned}
$$

Phase Currents

$$
\begin{aligned}
i_a &= \hat{I}_1 \cos(\omega_1 t - \Phi_1) \\
i_b &= \hat{I}_1 \cos\left(\omega_1 \left(t - \frac{T}{3}\right) - \Phi_1\right) \\
i_c &= \hat{I}_1 \cos\left(\omega_1 \left(t + \frac{T}{3}\right) - \Phi_1\right)
\end{aligned}
$$

Instantaneous Power

$$
\begin{aligned}
p(t) = u_a i_a + u_b i_b + u_c i_c = \frac{P}{3}(1 + \cos 2\omega_1 t) & + \frac{Q}{3}\sin 2\omega_1 t \\
+ \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) & + \frac{Q}{3}\sin 2\omega_1 \left(t - \frac{T}{3}\right) \\
+ \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) & + \frac{Q}{3}\sin 2\omega_1 \left(t + \frac{T}{3}\right)
\end{aligned}
$$

$$
P = \frac{3}{2}\hat{U}_1 \cdot \hat{I}_1 \cos\Phi_1
$$

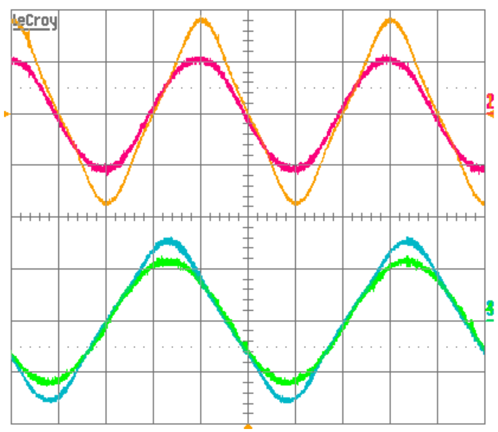
$$
Q = \frac{3}{2}\hat{U}_1 \cdot \hat{I}_1 \sin\Phi_1
$$

$$
\boxed{p(t)} = \frac{P}{3}(1 + \cos 2\omega_1 t) + \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) + \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) = \boxed{3\frac{P}{3} = P}
$$

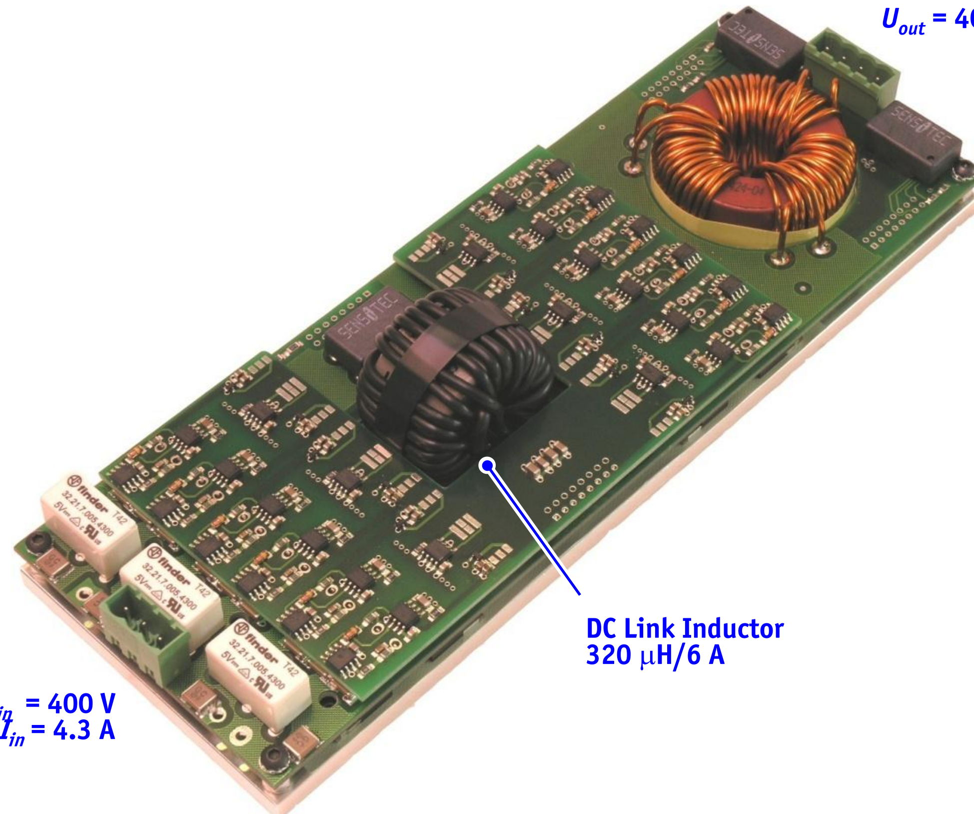
All-SiC JFET I-BBC Prototype

- P_{out} = 2.9 kVA
- f_S = 200 kHz
- 2.4 kVA / liter (42 W/in³)
- 230 x 80 x 65 mm³

200V/div
5A/div



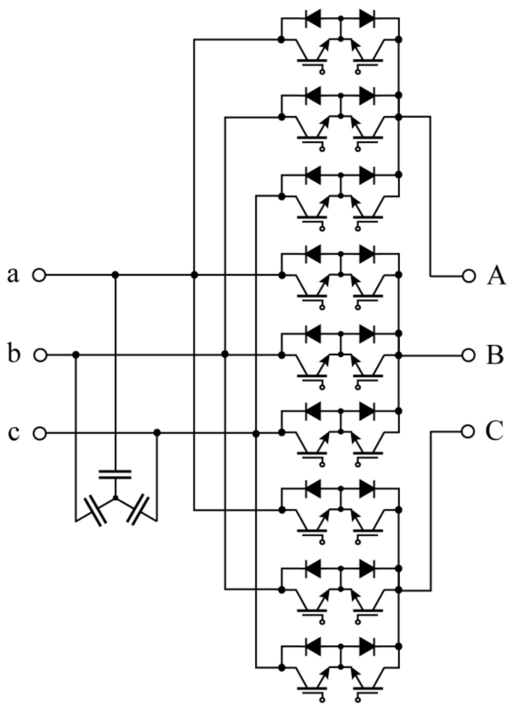
U_{out} = 400 V

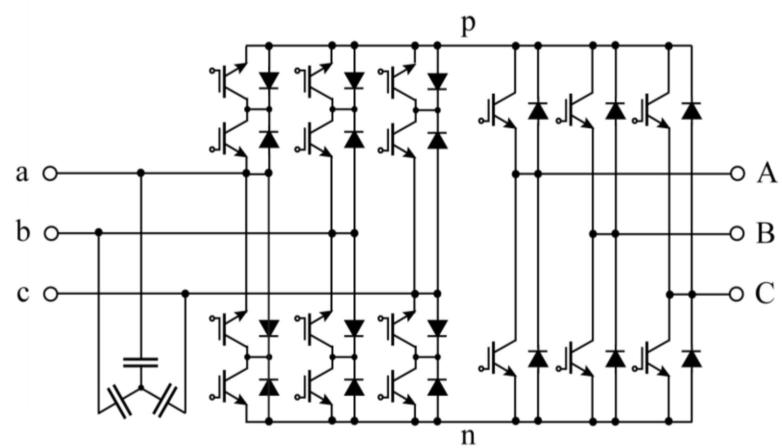


DC Link Inductor
320 µH/6 A

U_{in} = 400 V
I_{in} = 4.3 A

Basic Matrix Converter Topologies





$$\frac{Q}{3}\left(\sin 2\omega_1 t + \sin 2\omega_1\left(t-\frac{T}{3}\right) + \sin 2\omega_1\left(t+\frac{T}{3}\right)\right) \equiv 0$$

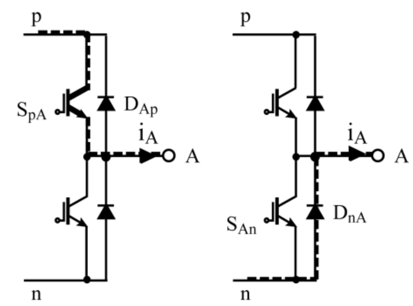
V-BBC

Voltage Space Vectors
Modulation
DC Link Current

VSI Space Vector Modulation (1)

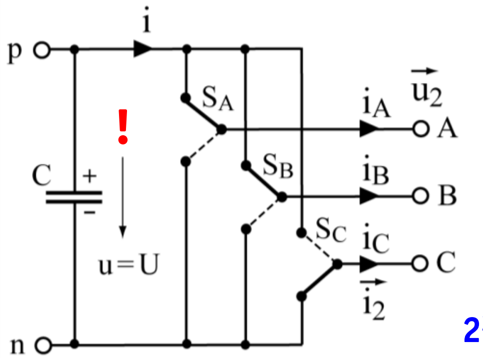
$$\vec{u}_{2,j} = \frac{2}{3}\left(u_{A,j} + \underline{a}u_{B,j} + \underline{a}^2 u_{C,j}\right)$$
$$u_{0,j} = \frac{1}{3}\left(u_{A,j} + u_{B,j} + u_{C,j}\right)$$

- Switching with Interlock Delay



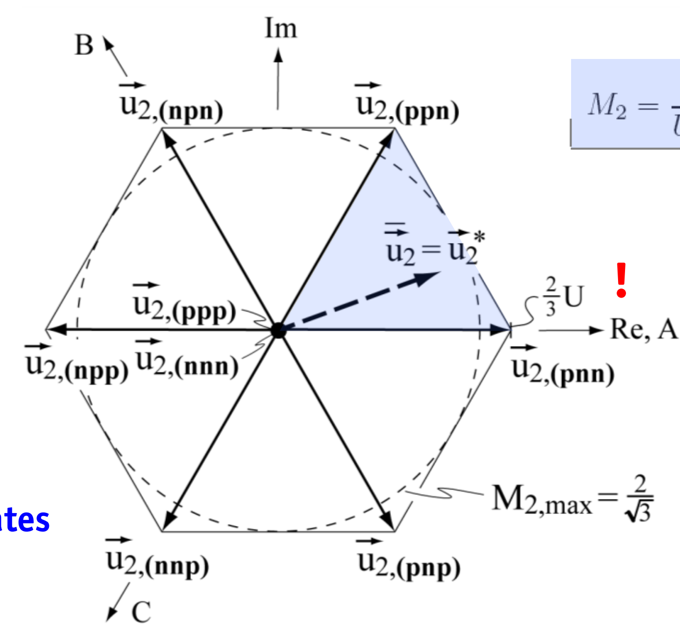
Output Voltage Reference Value

$$\boxed{\vec{u}_2^*} = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \boxed{\hat{U}_2^* e^{j\omega_2^* t}}$$



2^3 = 8 Switching States

$$\boxed{M_2 = \frac{\hat{U}_2^*}{U/2}}$$



VSI Space Vector Modulation (2)

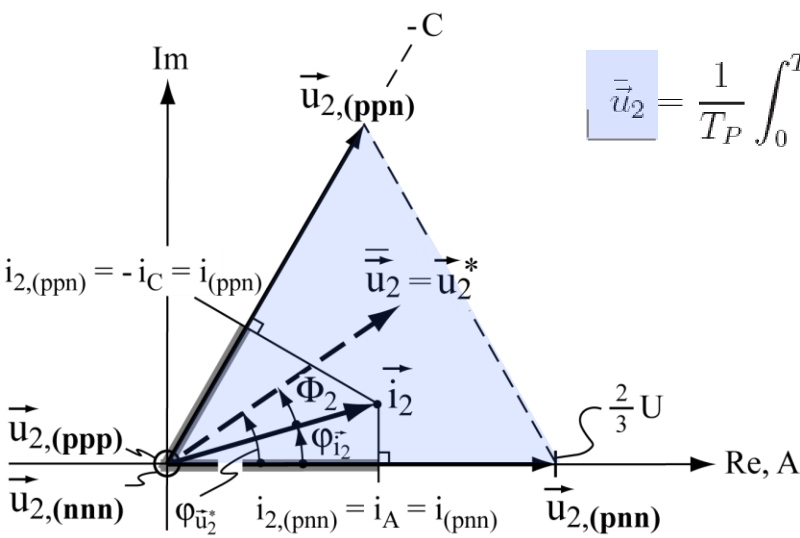
$$M_{2,\max} = \frac{\hat{U}^*_{2,\max}}{U/2} = \frac{2}{\sqrt{3}}$$

Switching State Sequence

$$\cdots \Big|_{t_\mu = 0} \quad (nnn) - (pnn) - (ppn) - (ppp) \Big|_{t_\mu = T_P/2}$$

$$(ppp) - (ppn) - (pnn) - (nnn) \Big|_{t_\mu = T_P} \quad \cdots$$

Formation of the Output Voltage



$$\bar{\vec{u}}_2 = \frac{1}{T_P}\int_0^{T_P} \vec{u}_{2,j}\,\mathrm{d}t_\mu = d_{(pnn)} \cdot \vec{u}_{2,(pnn)} + d_{(ppn)} \cdot \vec{u}_{2(ppn)}$$

$$= d_{(pnn)}\frac{2}{3}U + d_{(ppn)}\frac{2}{3}U\,\mathrm{e}^{j\pi/3}$$

$$= \vec{u}_2^*$$

Relative On-times

$$d_{(ppn)} = \frac{\sqrt{3}}{2}M_2 \sin\left(\varphi_{\vec{u}_2^*}\right)$$

$$d_{(pnn)} = \frac{\sqrt{3}}{2}M_2 \sin\left(\frac{\pi}{3} - \varphi_{\vec{u}_2^*}\right)$$

VSI Space Vector Modulation (3)

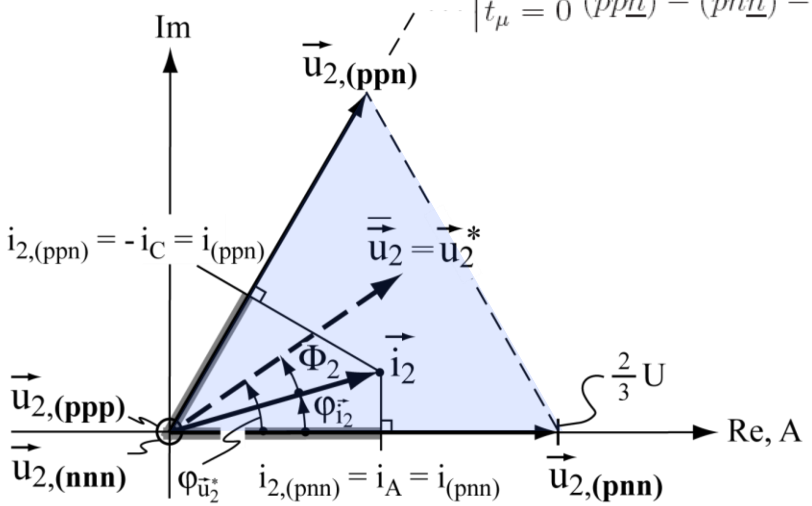
Freewheeling On-time

$$d_{(nnn)} + d_{(ppp)} = 1 - (d_{(ppn)} + d_{(pnn)})$$

Discontinuous Modulation

$$\Big| t_\mu = 0 \; (\underline{p}nn) - (\underline{p}pn) - (\underline{p}pp) \Big| t_\mu = T_P/2 \; (\underline{p}pp) - (\underline{p}pn) - (\underline{p}nn) \Big| t_\mu = T_P \cdots$$

$$\Big| t_\mu = 0 \; (pp\underline{n}) - (pn\underline{n}) - (nn\underline{n}) \Big| t_\mu = T_P/2 \; (nn\underline{n}) - (pn\underline{n}) - (pp\underline{n}) \Big| t_\mu = T_P \cdots$$



Space Vector Orientation

$$\frac{d_{(ppn)}}{d_{(pnn)}} = \frac{\sin\left(\varphi_{\vec{u}_2^*}\right)}{\sin\left(\frac{\pi}{3} - \varphi_{\vec{u}_2^*}\right)}$$

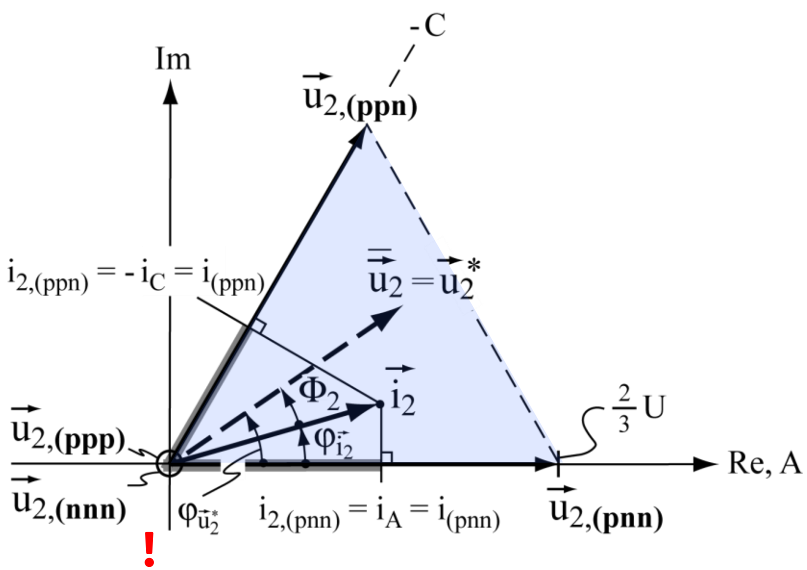
Modulation Limit

$$M_{2,\max} = \frac{\hat{U}^*_{2,\max}}{U/2} = \frac{2}{\sqrt{3}}$$

VSI Space Vector Modulation (4)

DC-link Current Shape

$$i_j = i_{2,j}$$



$$
\begin{aligned}
i_{(nnn)} &= \boxed{0} \\
i_{(nnp)} &= i_C \\
i_{(npn)} &= i_B \\
i_{(npp)} &= i_B + i_C = -i_A \\
i_{(pnn)} &= i_A \\
i_{(pnp)} &= i_A + i_C = -i_B \\
i_{(ppn)} &= i_A + i_B = -i_C \\
i_{(ppp)} &= \boxed{0}
\end{aligned}
$$

Local Average Value

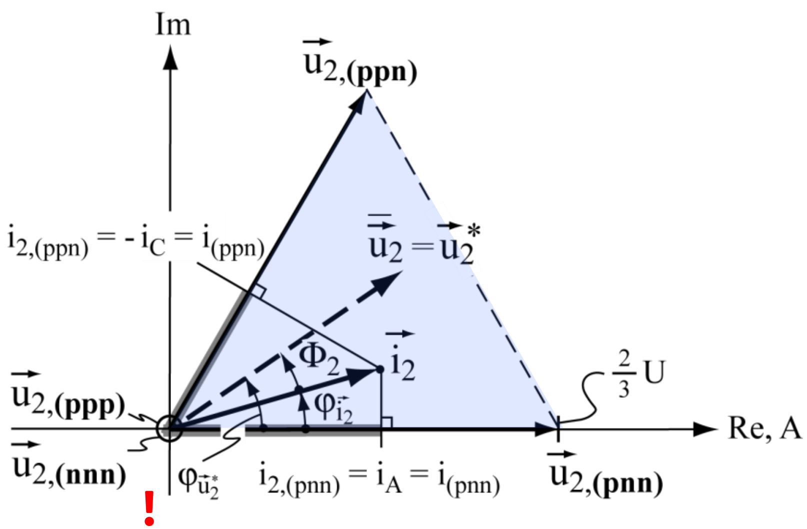
$$\bar{i} = \frac{1}{T_P} \int_0^{T_P} i_j \; \mathrm{d}t_\mu$$

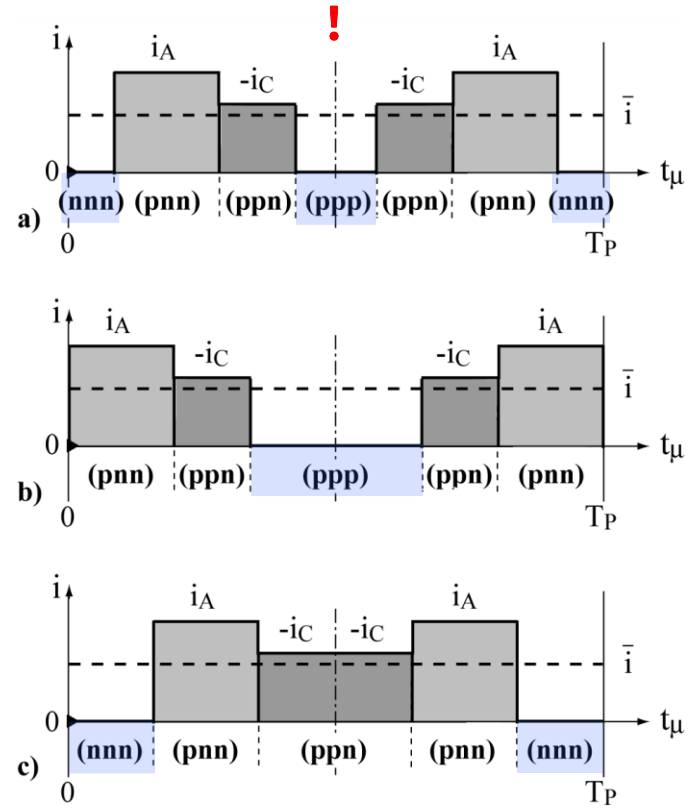
$$\bar{i} = -i_C d_{(ppn)} + i_A d_{(pnn)}$$

VSI Space Vector Modulation (5)

Local DC-link Current Shape

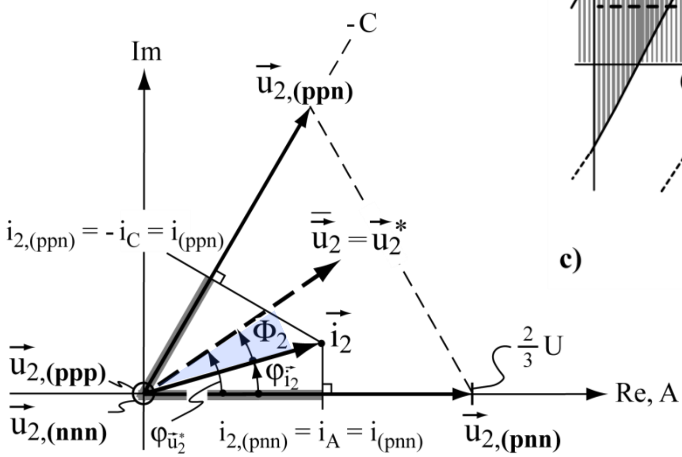
$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2$$

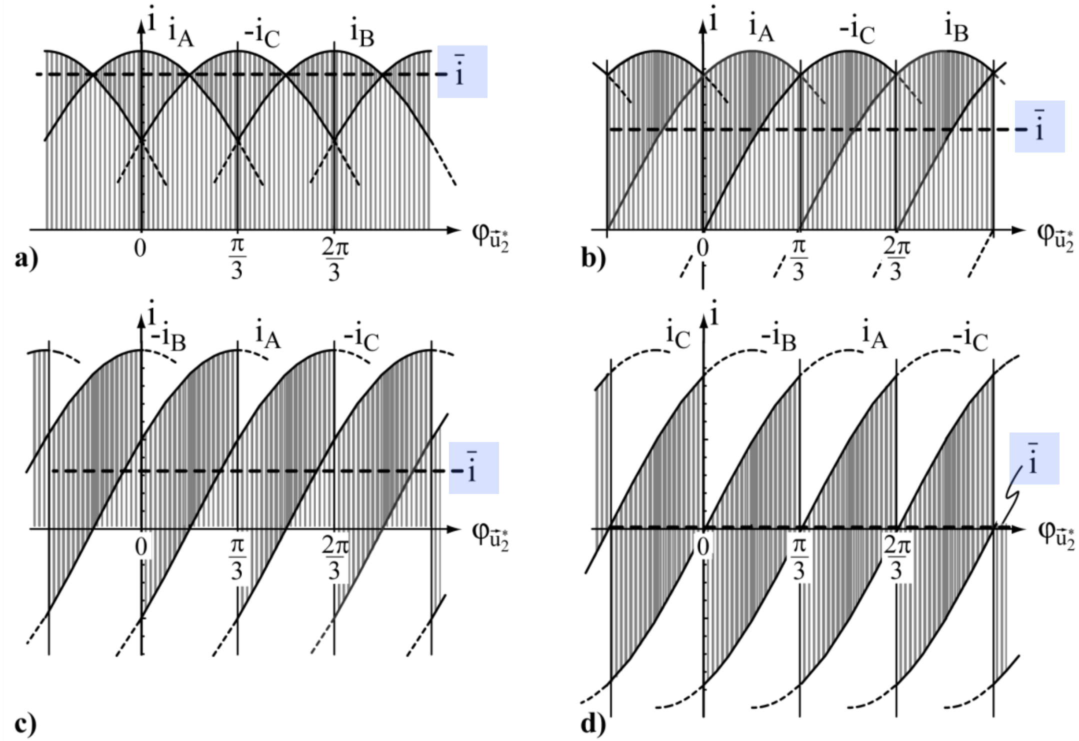




VSI DC-link Current Waveform

Influence of Output Voltage Phase Displacement Φ_2 on DC-link Current Waveform





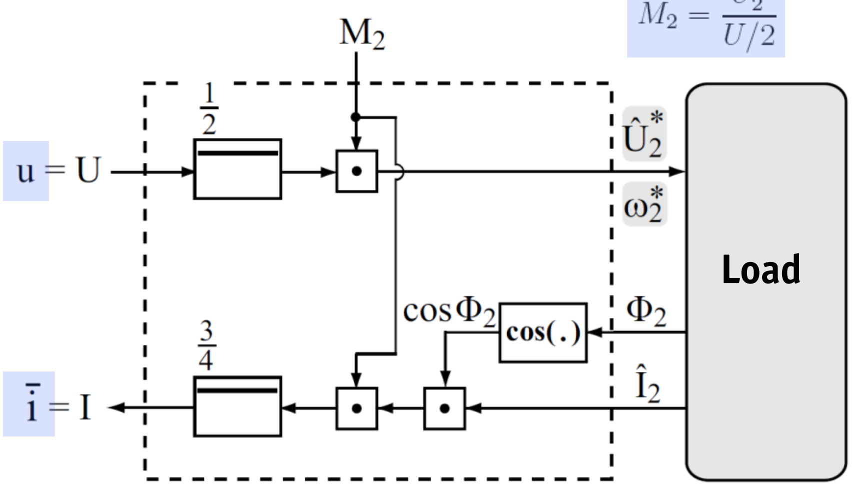
$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos\Phi_2$$

$$M_2 = 2/\sqrt{3}$$

VSI Functional Equivalent Circuit

Voltage Conversion

$M_2 = \frac{\hat{U}_2^*}{U/2}$



$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos\Phi_2$

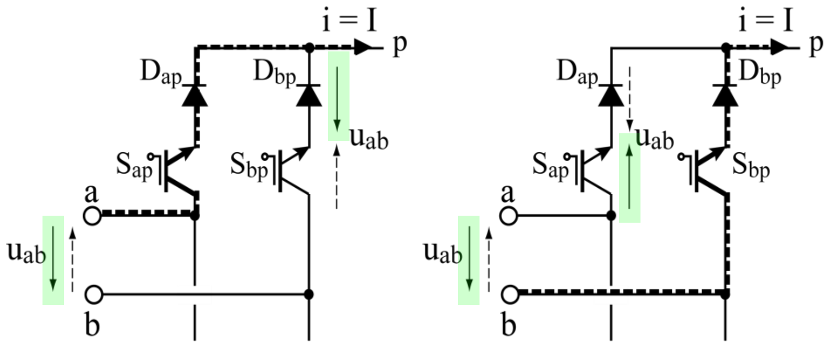
Current Conversion

I-BBC

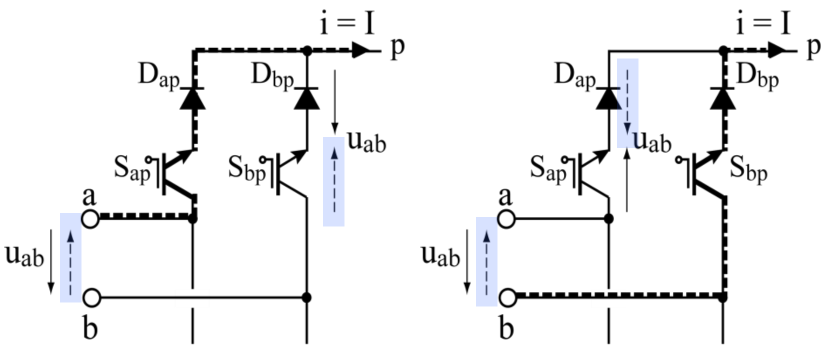
Current Space Vectors
Modulation
DC Link Voltage

CSR Commutation & Equivalent Circuit

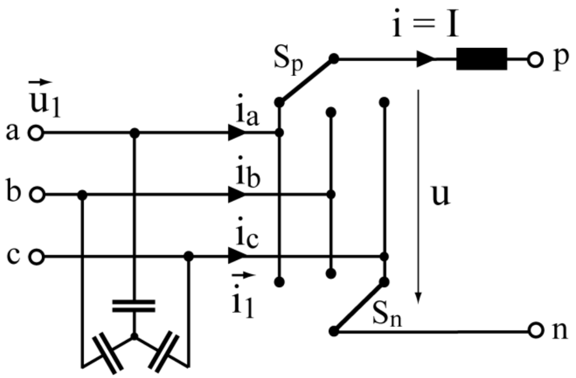
Forced Commutation



Natural Commutation



Equivalent Circuit



- $3^2 = 9$ Switching States
- Overlapping Switching

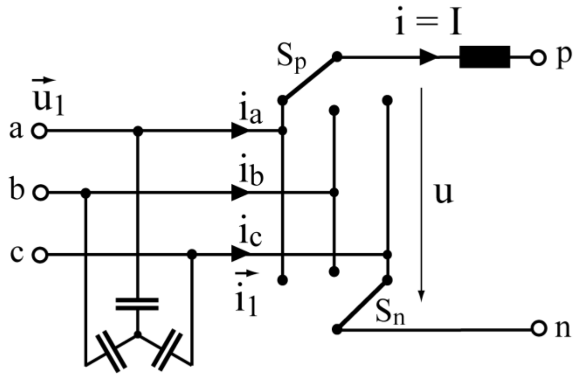
CSR Space Vector Modulation (1)

$$\vec{i}_k = \frac{2}{3}\left(i_{a,k} + \underline{a}\, i_{b,k} + \underline{a}^2\, i_{c,k}\right) \qquad \underline{a} = e^{j2\pi/3}$$

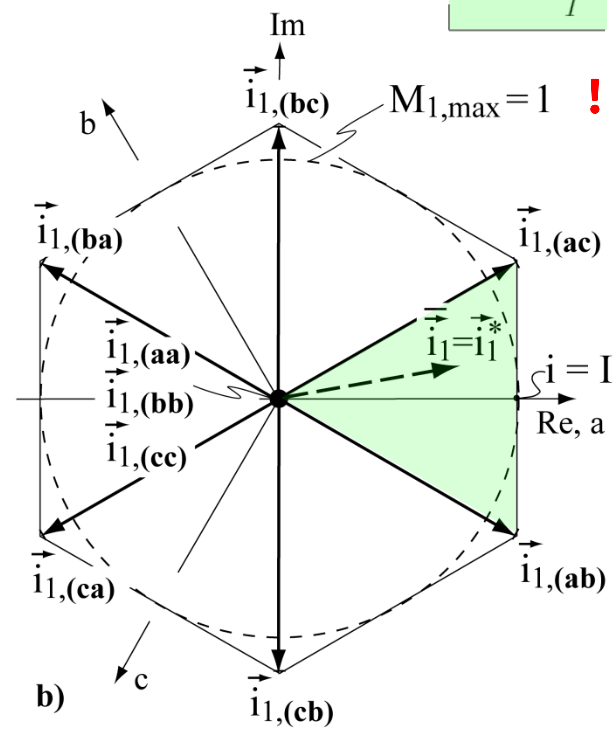
$$M_1 = \frac{\hat{I}_1^*}{I}$$

Input Current Reference Value

$$\vec{i}_1^* = \hat{I}_1^* e^{j\varphi_{\vec{i}_1^*}} = \hat{I}_1^* e^{j(\omega_1 t - \Phi_1^*)}$$



a)



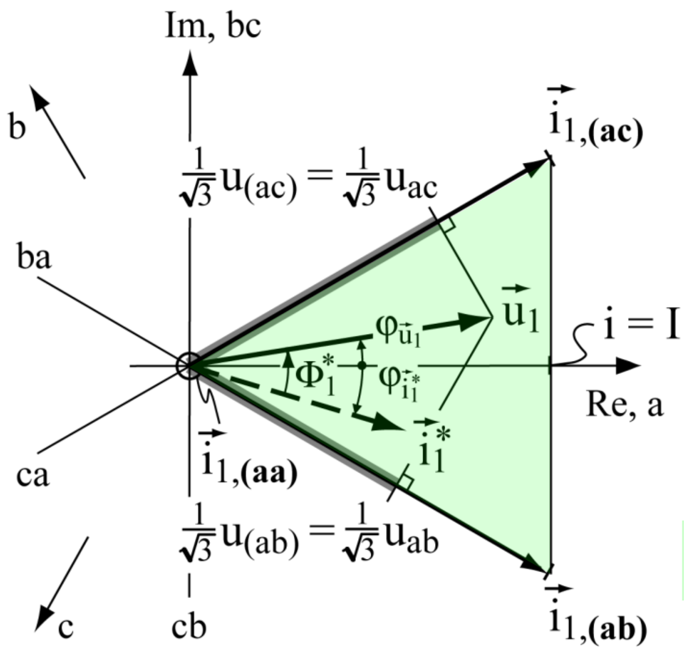
b)

CSR Space Vector Modulation (2)

Formation of the Input Current

$$|\vec{i}_{1,k}| = i_{1,k} = 2/\sqrt{3} \cdot I$$

$$\boxed{\vec{i}_1} = \frac{1}{T_P}\int_0^{T_P} \vec{i}_{1,k}\, \mathrm{d}t_\mu = \boxed{d_{(ac)} \cdot \vec{i}_{1,(ac)} + d_{(ab)} \cdot \vec{i}_{1,(ab)}} = \boxed{\vec{i}_1^{\,*}}$$



$$\boxed{\varphi_{\vec{i}_1^*}} = \boxed{\varphi_{\vec{u}_1} - \Phi_1^*}$$

Relative On-times

$$d_{(ac)} = M_1 \sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1^*}\right)$$

$$d_{(ab)} = M_1 \sin\left(\frac{\pi}{6} - \varphi_{\vec{i}_1^*}\right)$$

$$d_{(aa)} = 1 - \left(d_{(ac)} + d_{(ab)}\right)$$

Space Vector Orientation

$$\frac{d_{(ac)}}{d_{(ab)}} = \frac{\sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1^*}\right)}{\sin\left(\frac{\pi}{6} - \varphi_{\vec{i}_1^*}\right)}$$

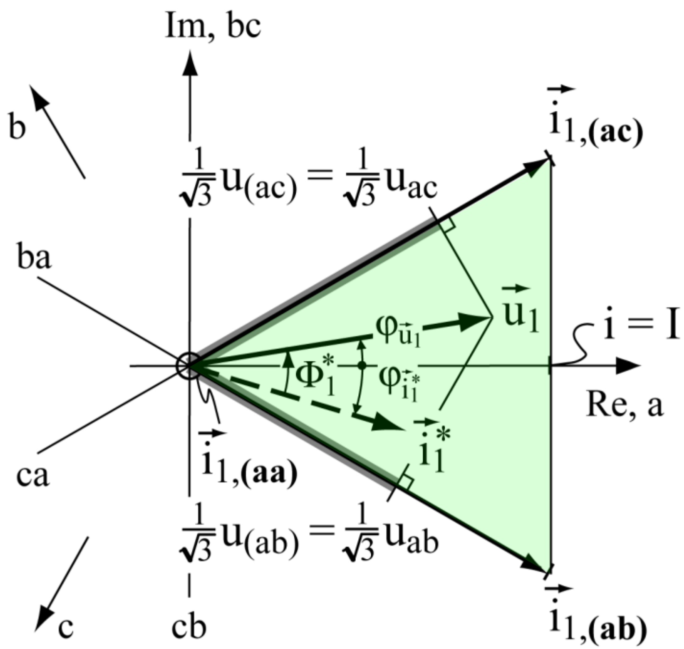
CSR Space Vector Modulation (3)

Switching State Sequence

$$\cdots \Big| t_\mu = 0 \quad (\underline{a}b)-(\underline{a}c)-(\underline{a}a) \Big| t_\mu = T_P/2 \quad (\underline{a}a)-(\underline{a}c)-(\underline{a}b) \Big| t_\mu = T_P \cdots$$

$$\cdots \Big| t_\mu = 0 \quad (\underline{a}c)-(\underline{a}b)-(\underline{a}a) \Big| t_\mu = T_P/2 \quad (\underline{a}a)-(\underline{a}b)-(\underline{a}c) \Big| t_\mu = T_P \cdots$$

$$\cdots \Big| t_\mu = 0 \quad (\underline{a}c)-(\underline{a}a)-(\underline{a}b) \Big| t_\mu = T_P/2 \quad (\underline{a}b)-(\underline{a}a)-(\underline{a}c) \Big| t_\mu = T_P \cdots$$



DC-link Voltage Formation

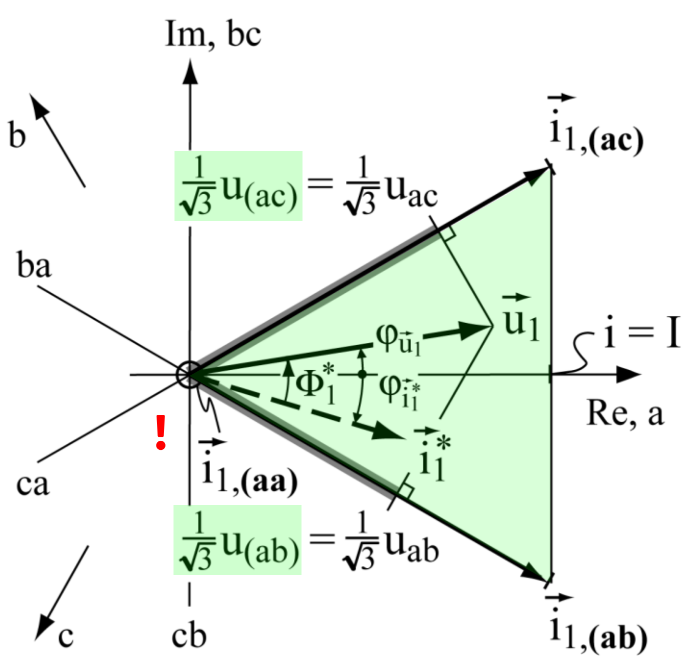
$$
\begin{aligned}
u_{(ab)} &= u_a - u_b = u_{ab} \\
u_{(ba)} &= u_b - u_a = u_{ba} = -u_{ab} \\
u_{(bc)} &= u_b - u_c = u_{bc} \\
u_{(cb)} &= u_c - u_b = u_{cb} = -u_{bc} \\
u_{(ca)} &= u_c - u_a = u_{ca} \\
u_{(ac)} &= u_a - u_c = u_{ac} = -u_{ca} \\
u_{(aa)} &= u_{(bb)} = u_{(cc)} = 0
\end{aligned}
$$

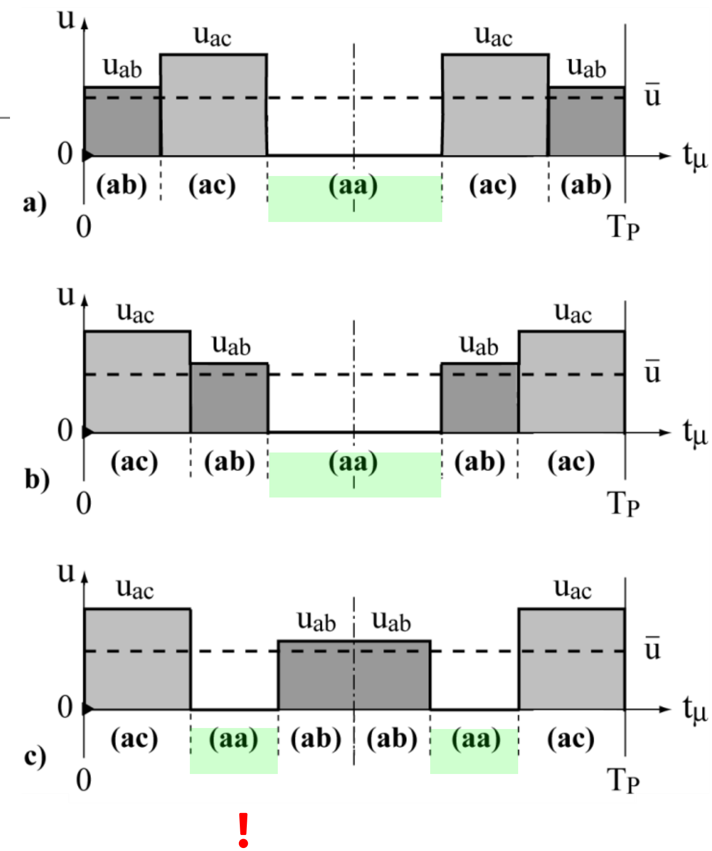
$$u_k = \sqrt{3} \cdot u_{1,k} \qquad \bar{u} = u_{ab} d_{(ab)} + u_{ac} d_{(ac)}$$

CSR Space Vector Modulation (4)

Local DC-link Voltage Shape

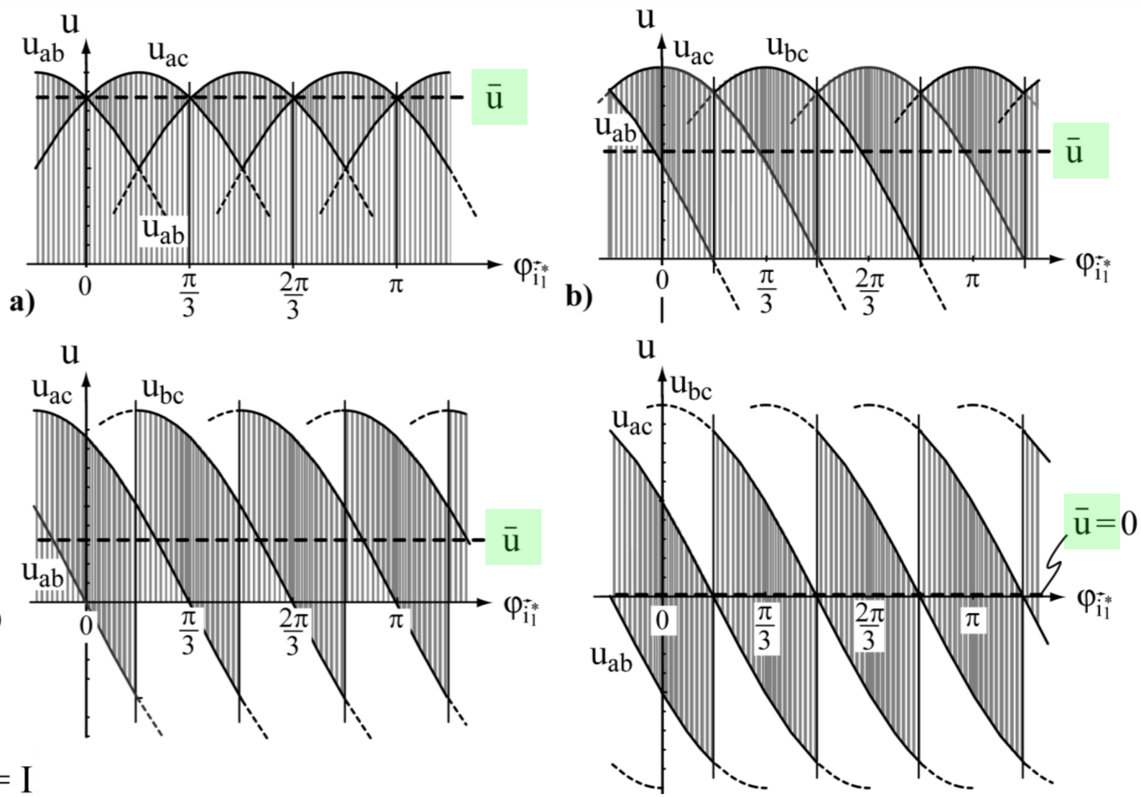
$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

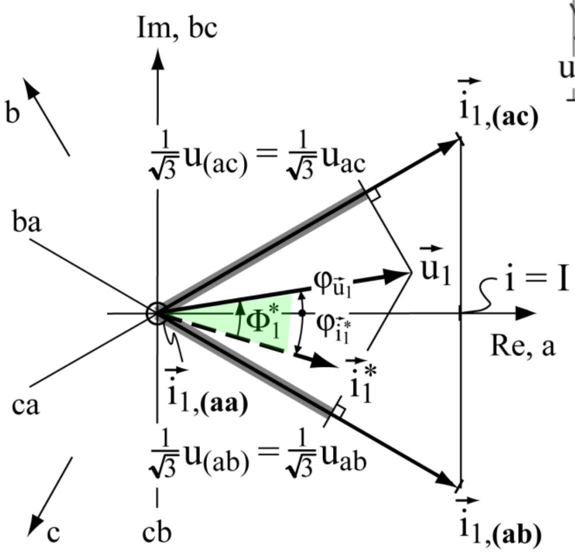




CSR DC-link Voltage Waveform

Influence of Input Current Phase Displacement Φ_1 on DC-link Voltage Waveform



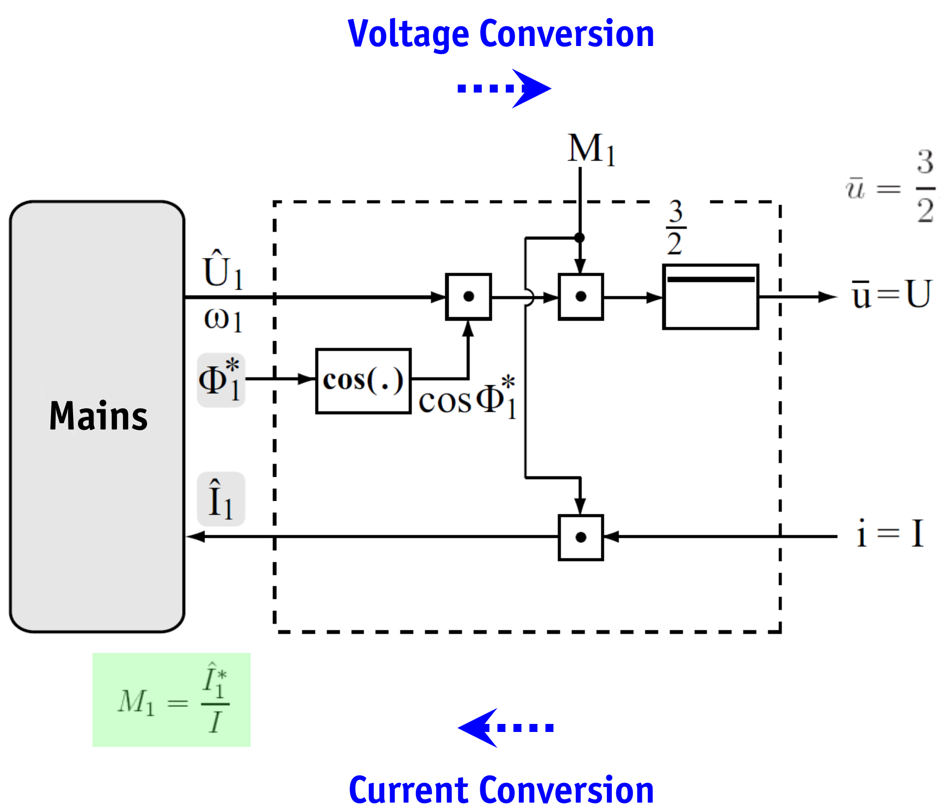


$$M_1 = \frac{\hat{I}_1^*}{I}$$

!

$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

CSR Functional Equivalent Circuit



$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

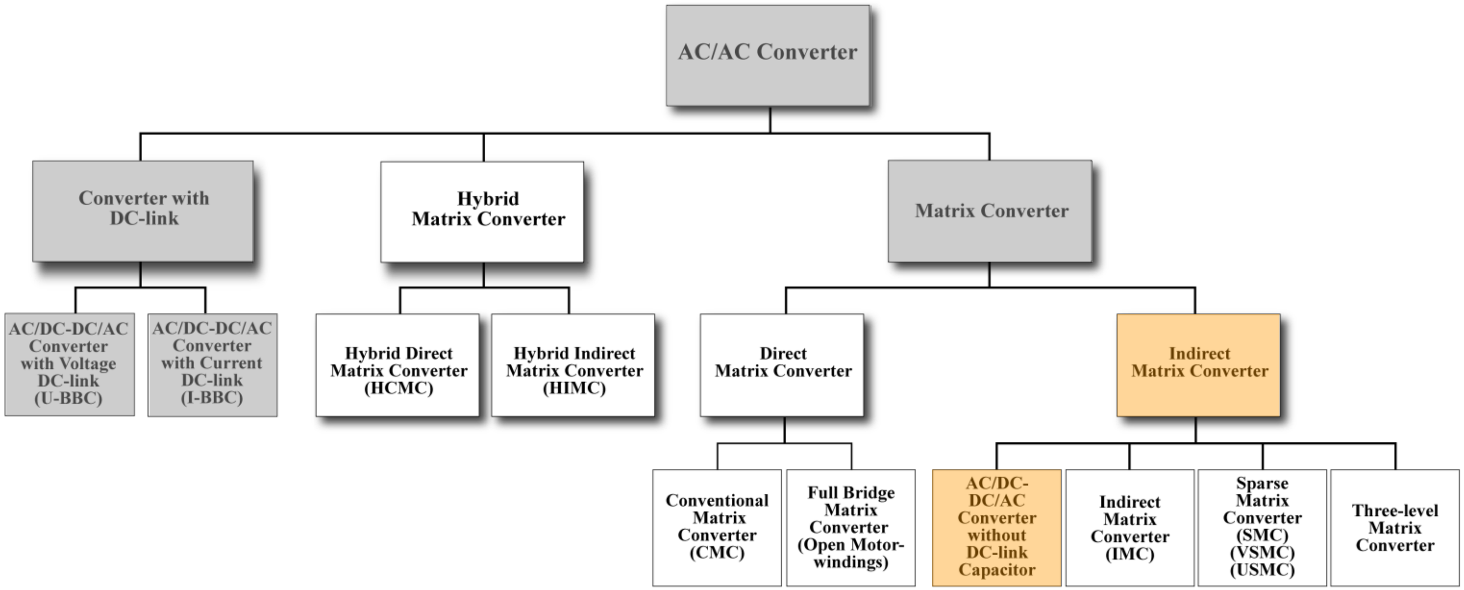
$$M_1 = \frac{\hat{I}_1^*}{I}$$

Derivation of MC Topologies

Fundamental Frequency Front End

F^3E

Classification of Three-Phase AC-AC Converters



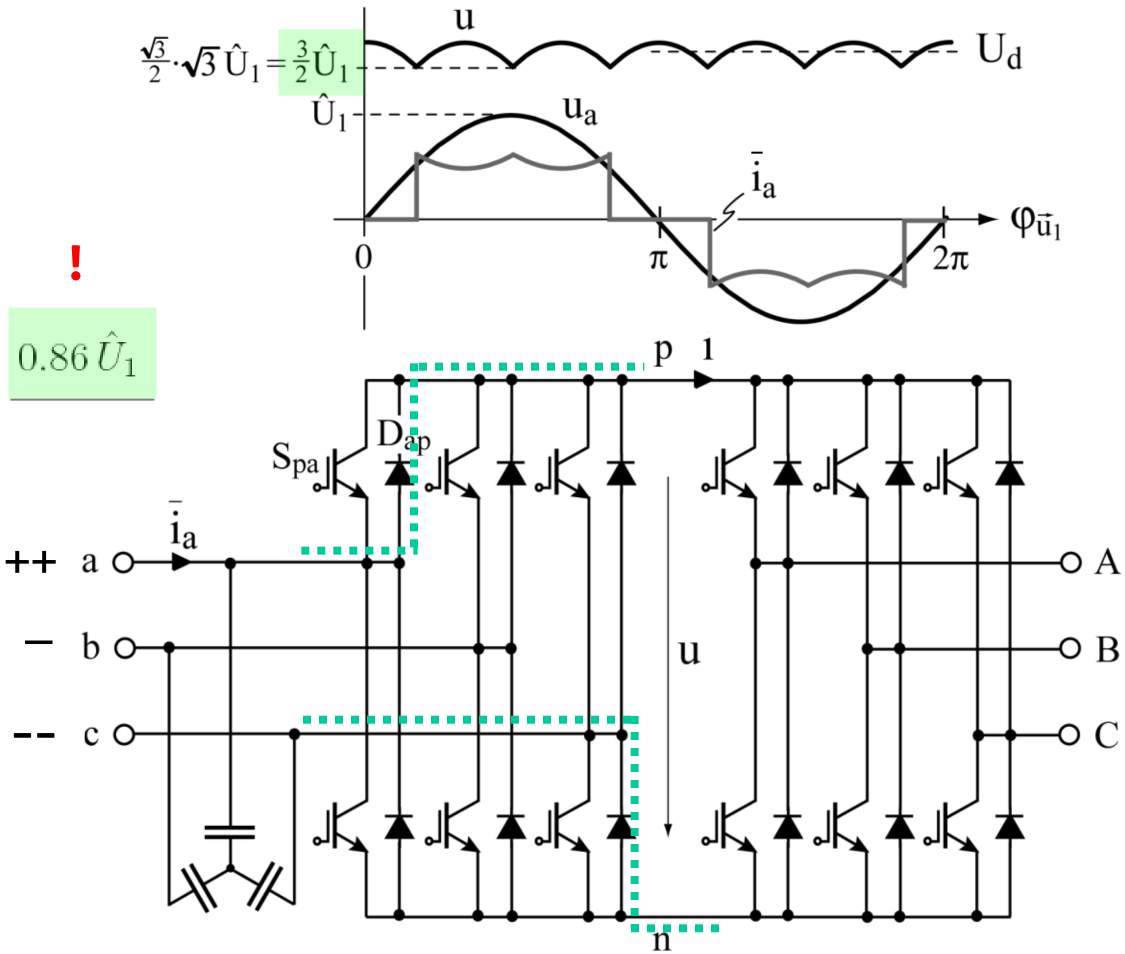
- *Converter without DC-link Capacitor*

F^3E Topology / Mains Behavior

$$u_{min} = \frac{3}{2}\hat{U}_1$$

!

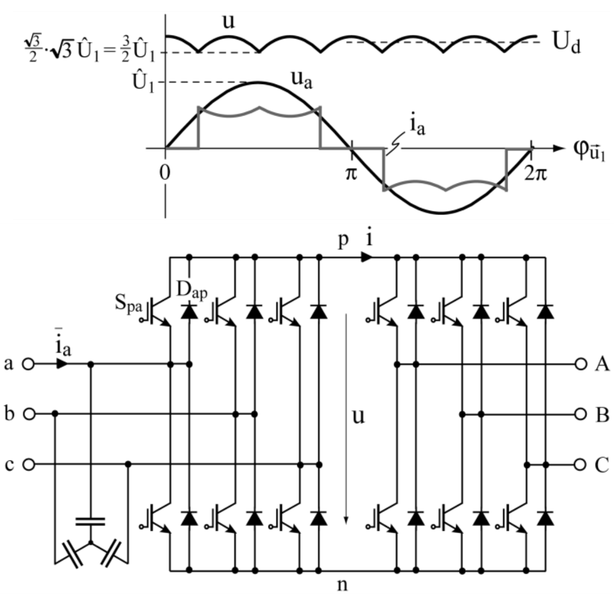
$$\hat{U}_2^* < \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \approx 0.86\,\hat{U}_1$$

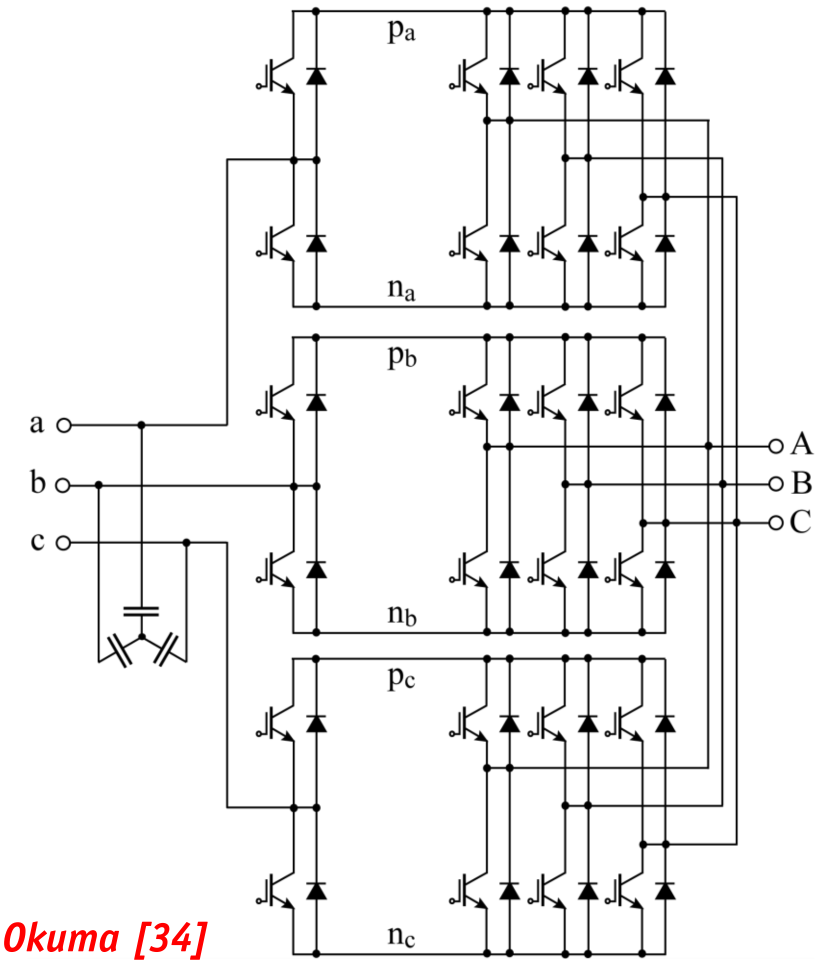


P. Ziogas [12]
T. Lipo [13, 18, 20]
B. Piepenbreier [15]

F^3E Topology Extension

▶ ***Sinusoidal Mains Current***



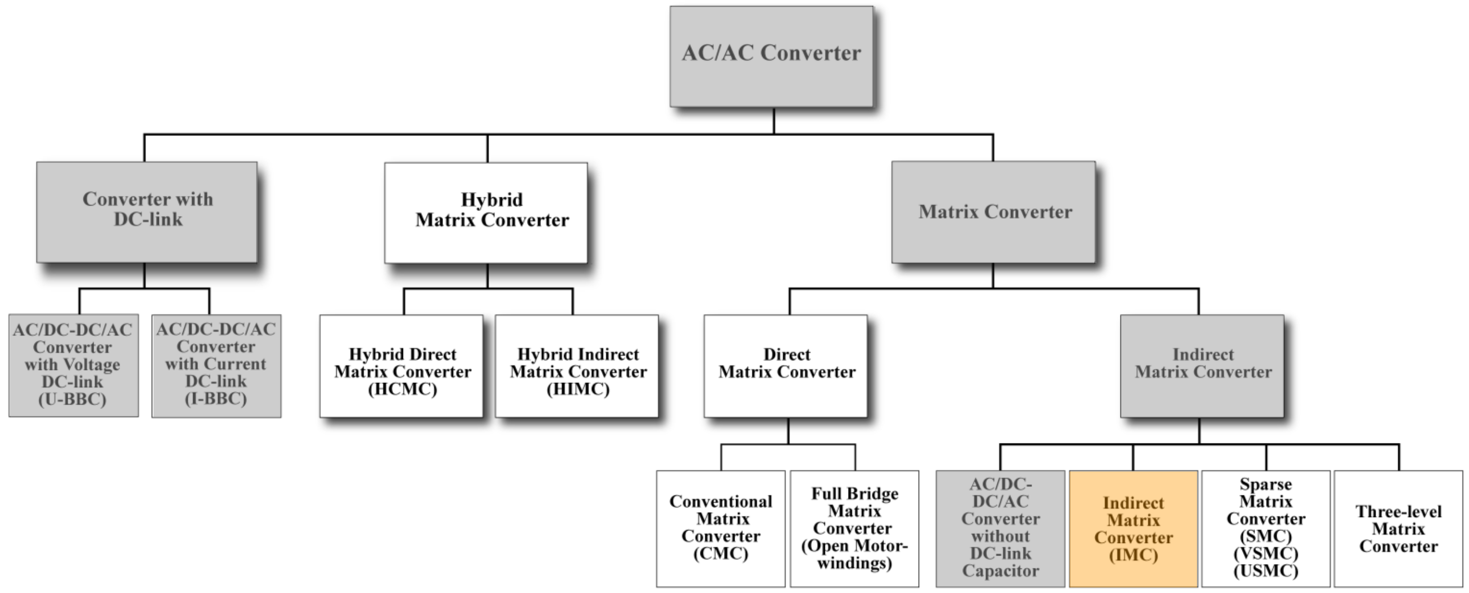


Y. Okuma [34]

Indirect Matrix Converter – IMC

Space Vectors
Modulation
Simulation
Experimental Results

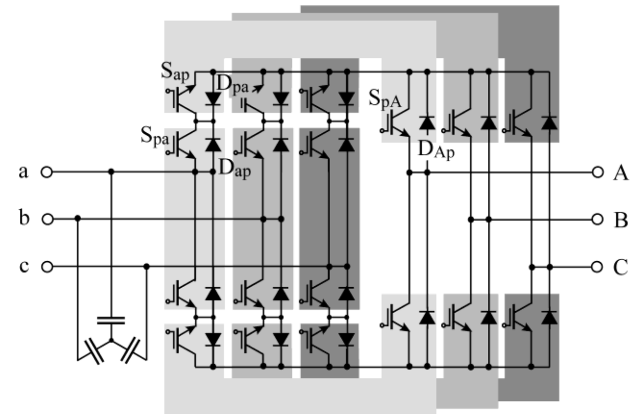
Classification of Three-Phase AC-AC Converters

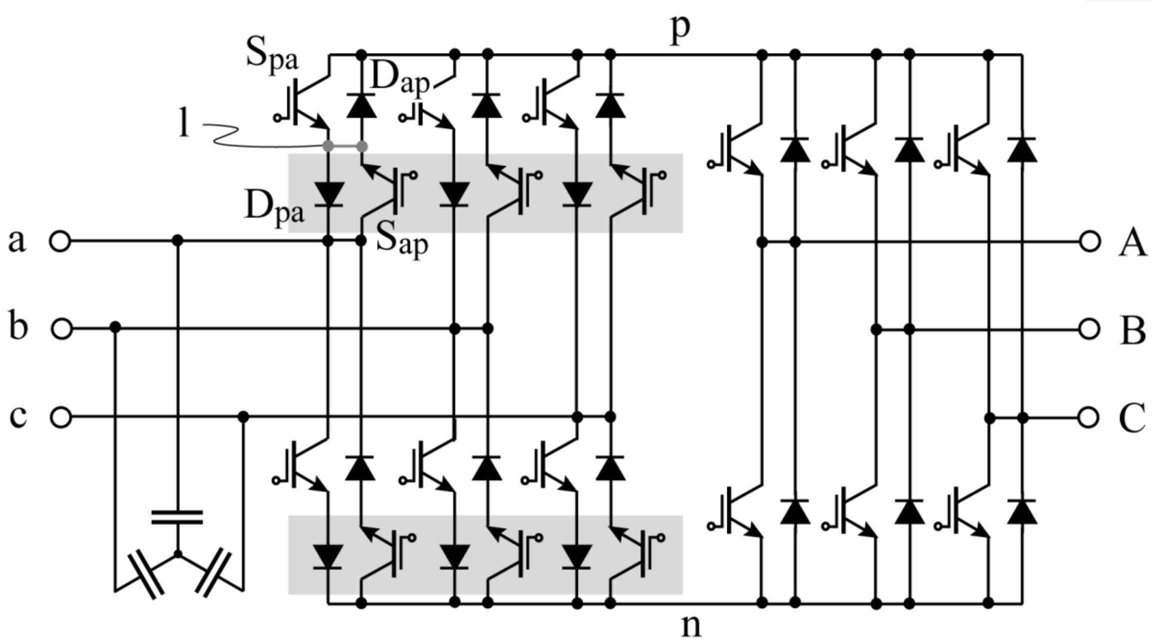


- *Indirect Matrix Converter*

IMC Topology Derivation

- ▶ *Extension of F^3E-Topology*
- ▶ *Bidirectional CSR Mains Interface* **!**

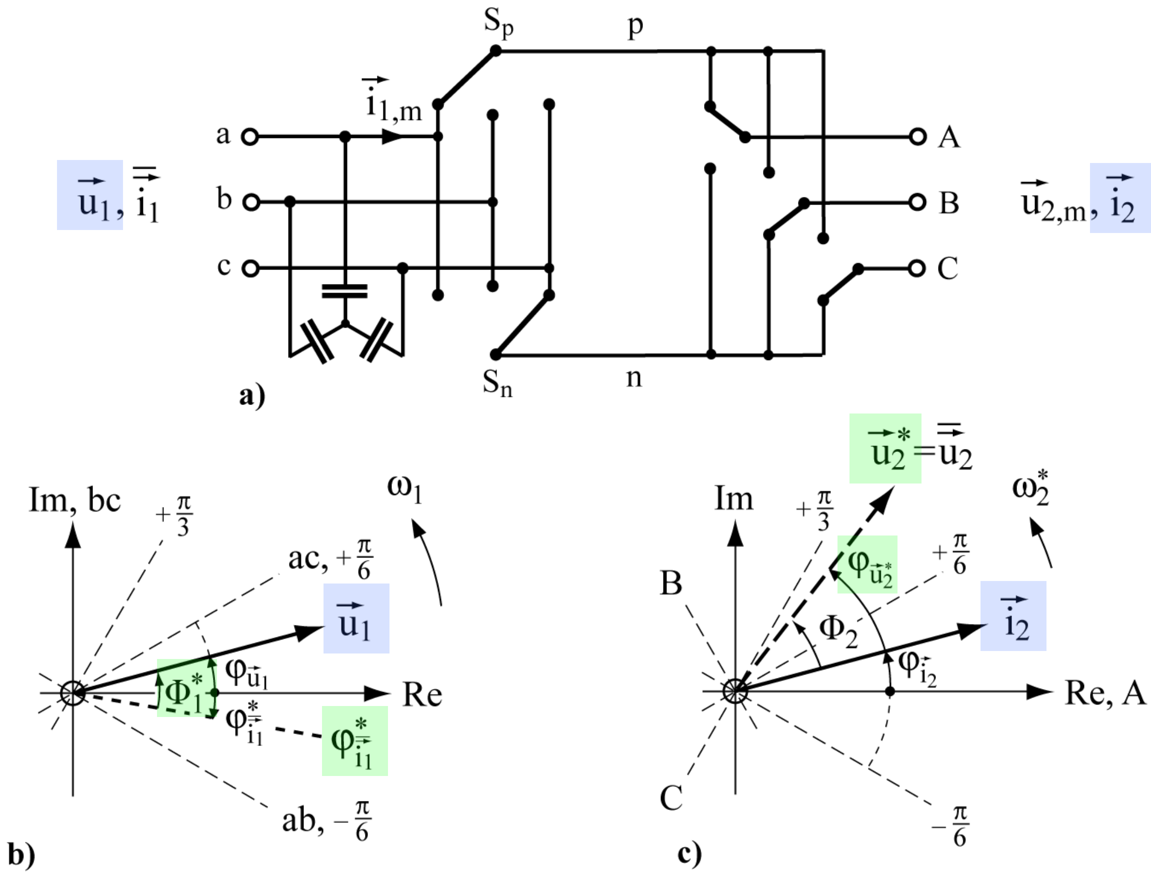




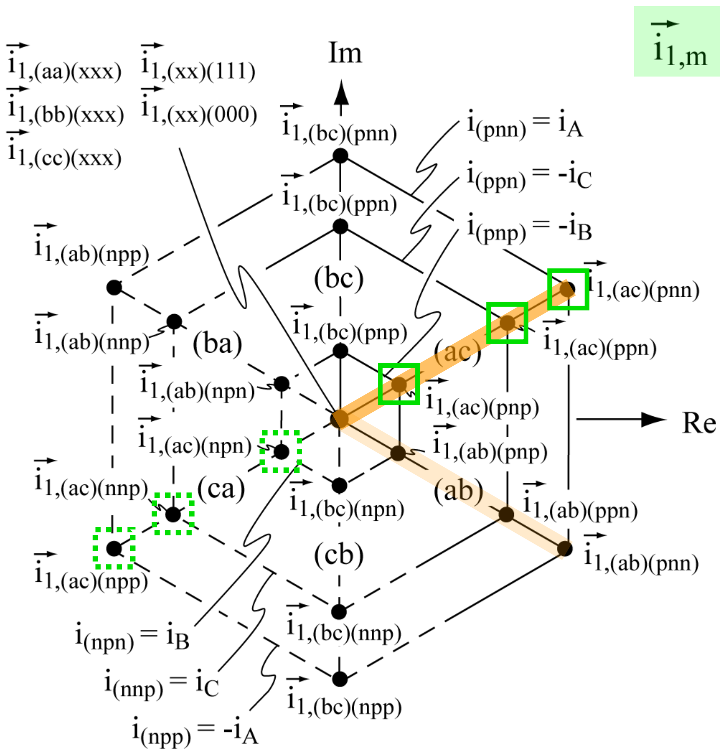
J. Holtz [16]
K. Shinohara [17]

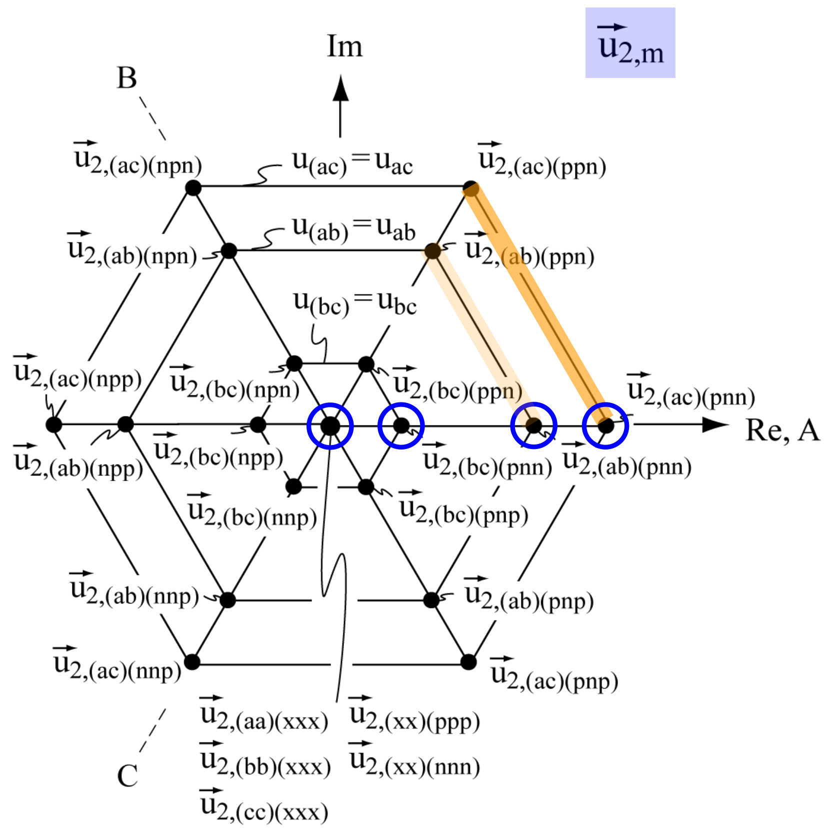
IMC Properties

▶ ***Positive DC-link Voltage Required*** !

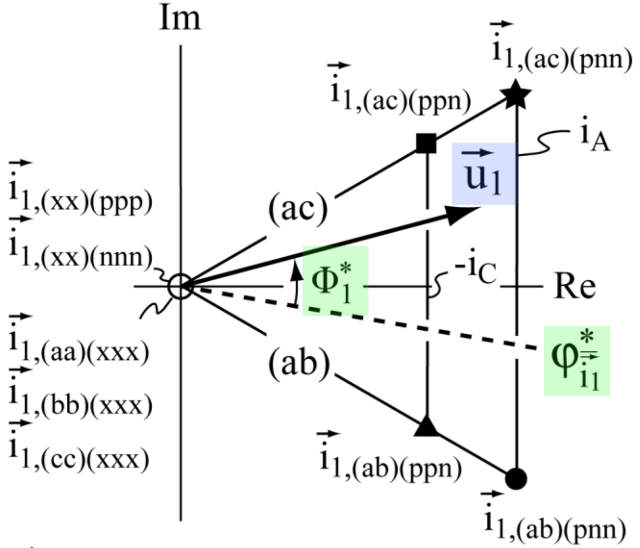


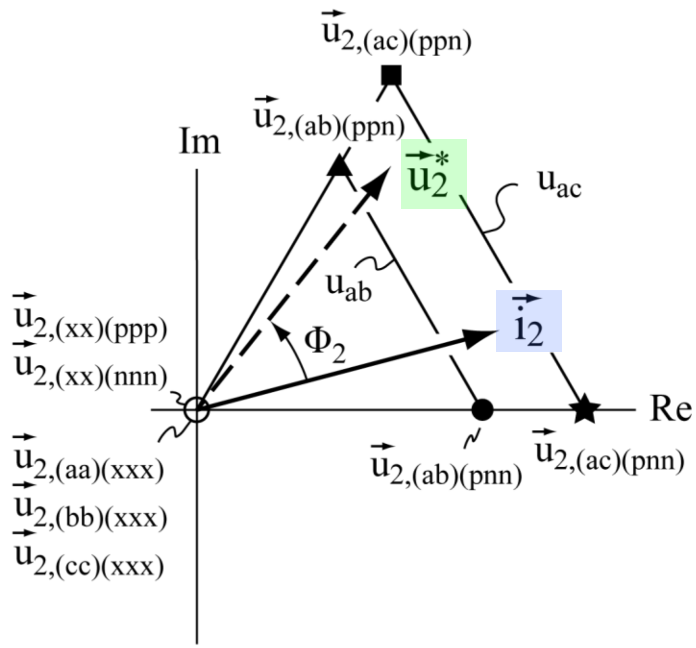
IMC Voltage and Current Space Vectors





IMC Space Vector Modulation (1)





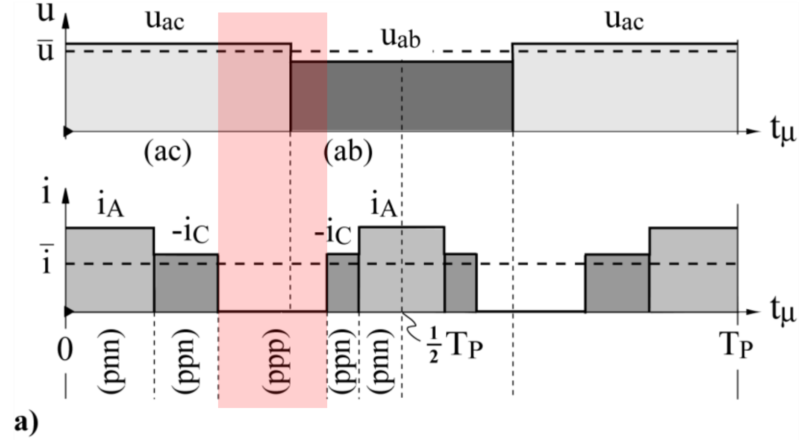
$$\vec{u}_1 = \hat{U}_1 e^{j\varphi_{\vec{u}_1}} = \hat{U}_1 e^{j\omega_1 t} \qquad \vec{i}_1 = \hat{I}_1 e^{j\varphi^*_{\vec{i}_1}}$$

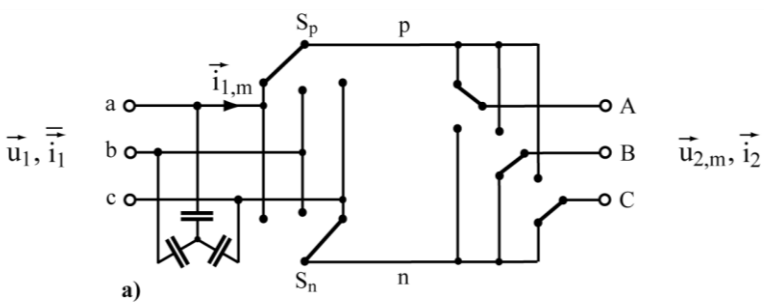
$$\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$$

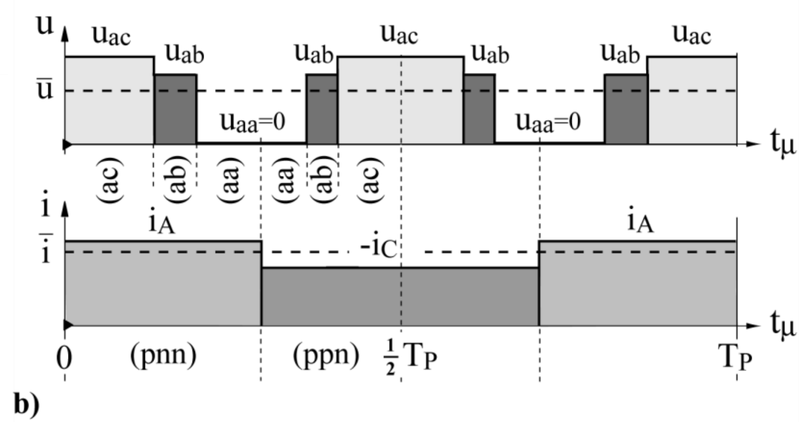
$$\vec{i}_2 = \hat{I}_2 e^{j\varphi_{\vec{i}_2}} = \hat{I}_2 e^{j\left(\varphi_{\vec{u}_2^*} - \Phi_2\right)}$$

IMC Space Vector Modulation (2)

- Zero Current Commutation !
- Zero Voltage Commutation

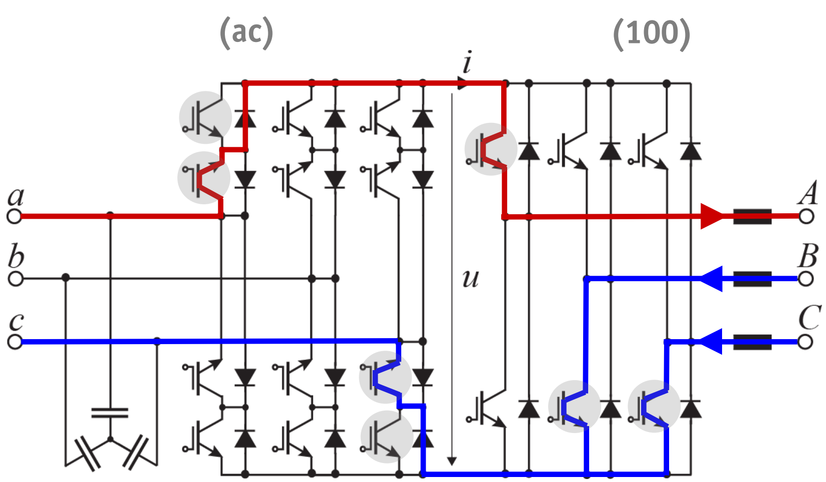


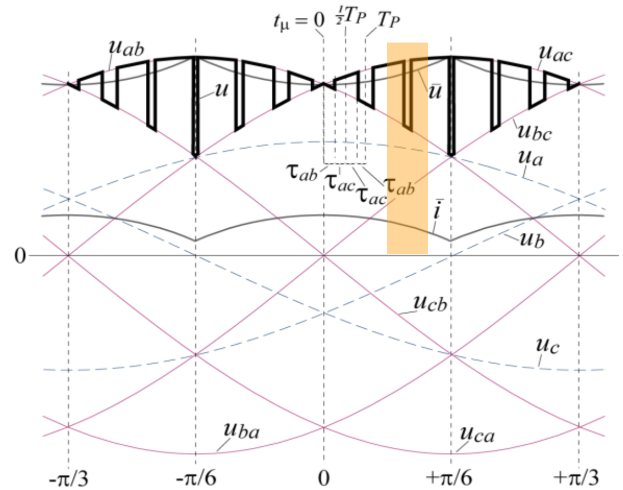


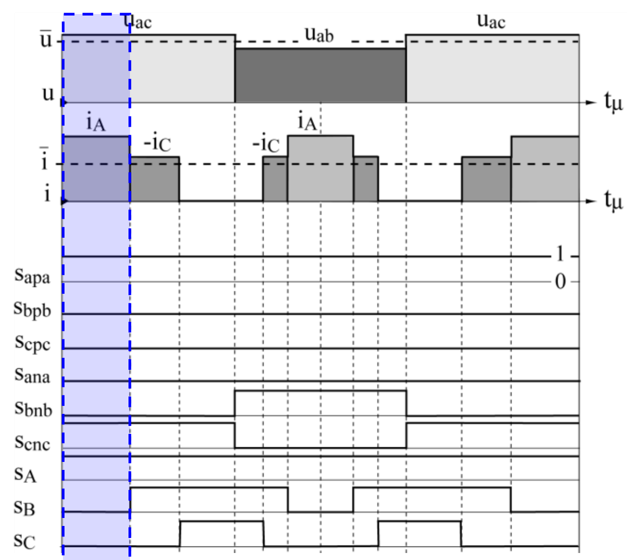


IMC Zero DC-link Current Commutation (1)

DC-link Voltage $u = u_{ac}$
DC-link Current $i = i_A$

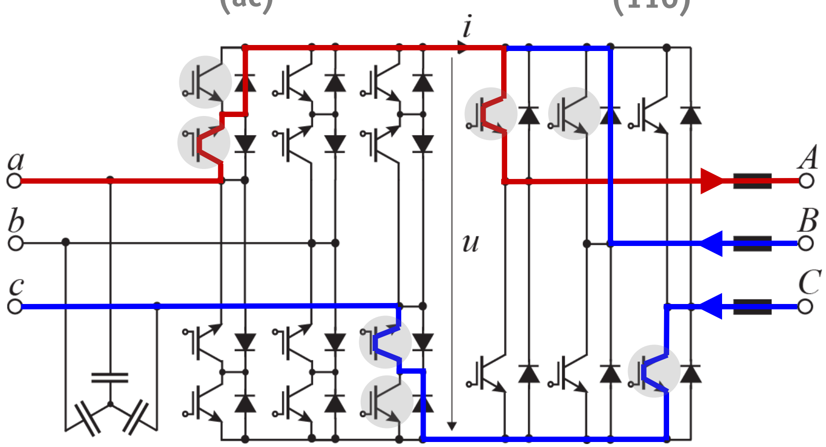


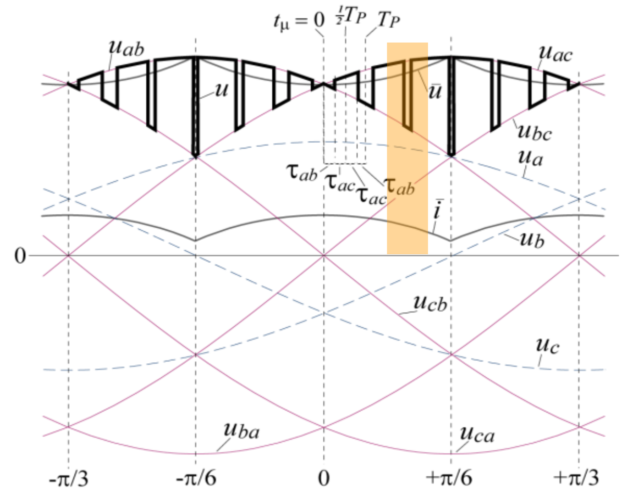




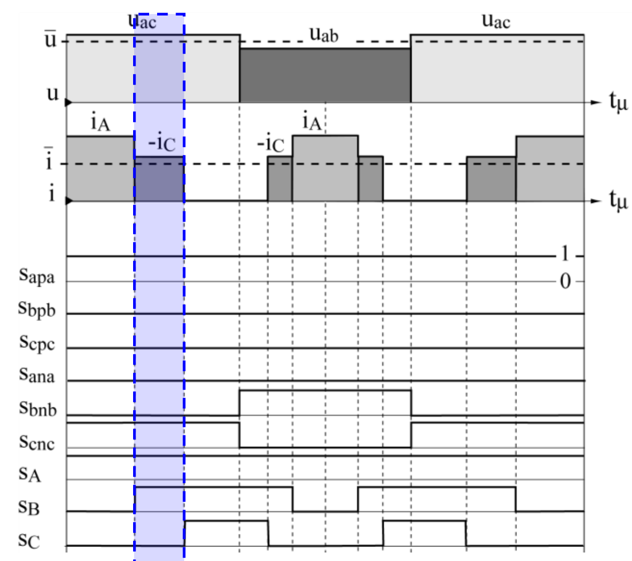
IMC Zero DC-link Current Commutation (2)

DC-link Voltage $u = u_{ac}$
DC-link Current $i = -i_C$





120° of Mains Period

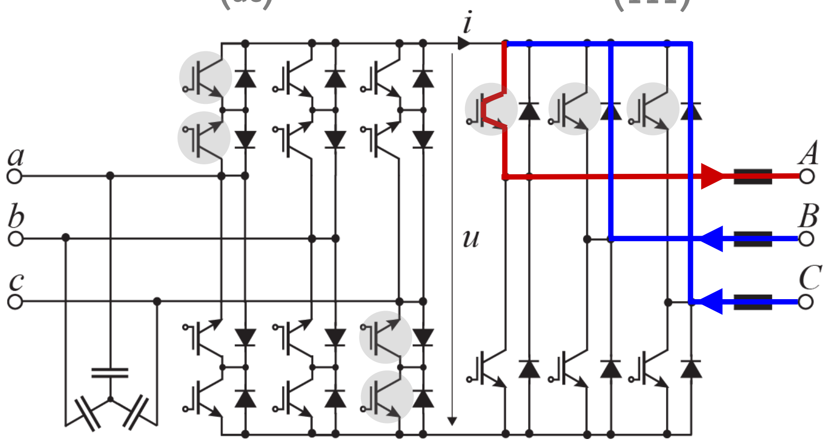


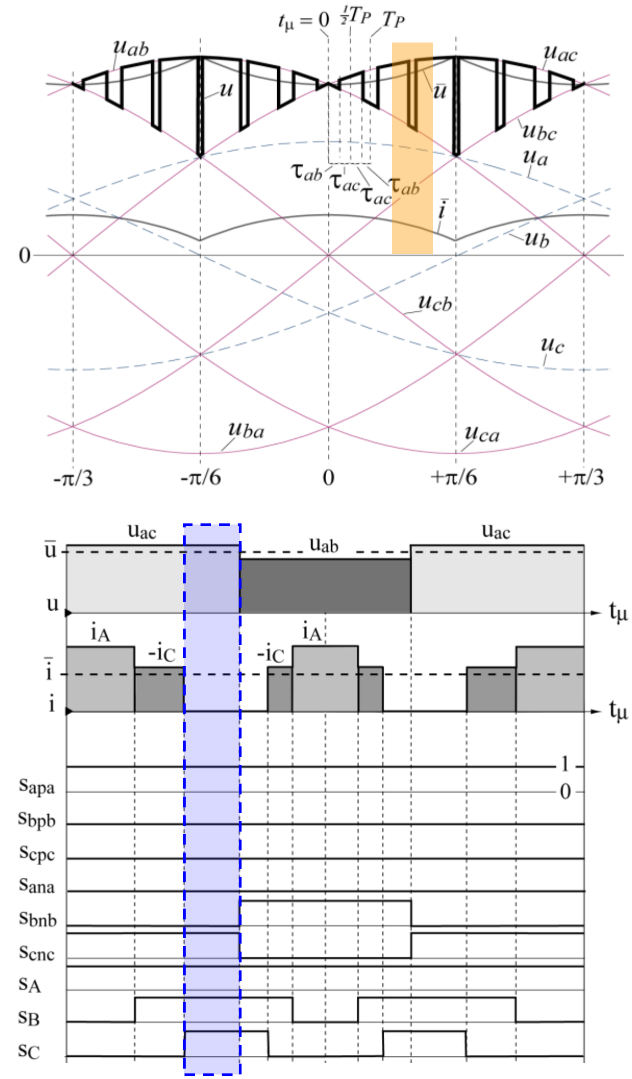
DC link Voltage & Current

PWM Pattern

IMC Zero DC-link Current Commutation (3)

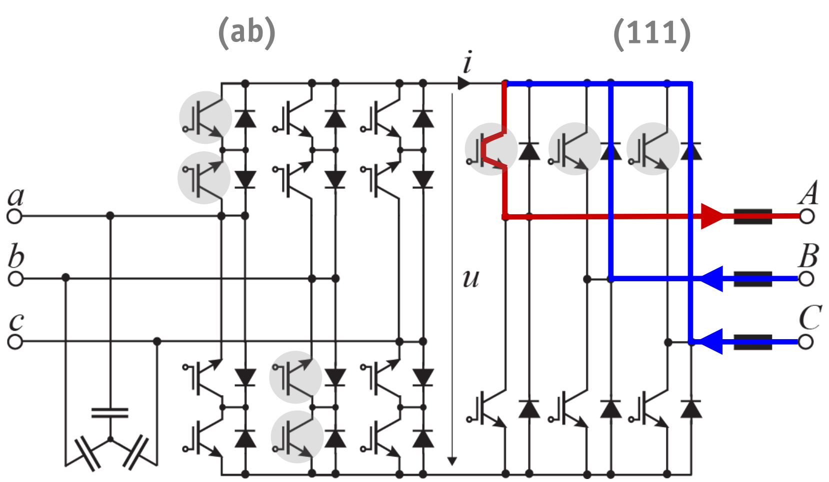
DC-link Voltage $u = u_{ac}$
DC-link Current $i = 0$

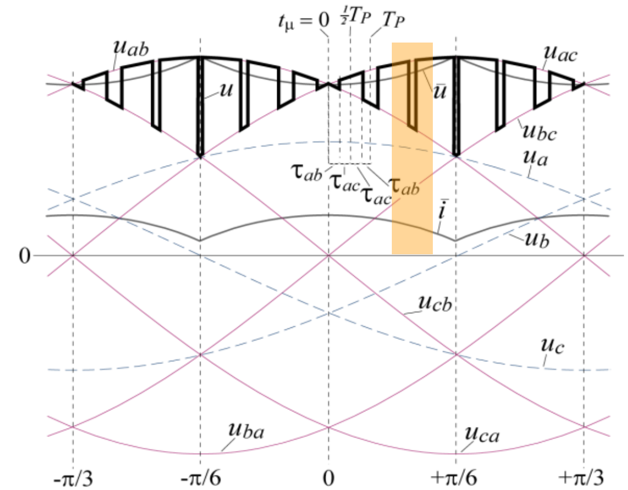




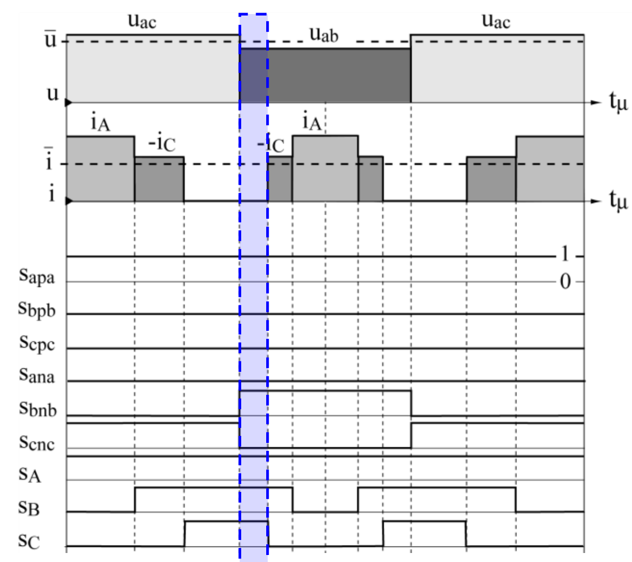
IMC Zero DC-link Current Commutation (4)

DC-link Voltage $u = u_{ab}$
DC-link Current $i = 0$





120°of Mains Period

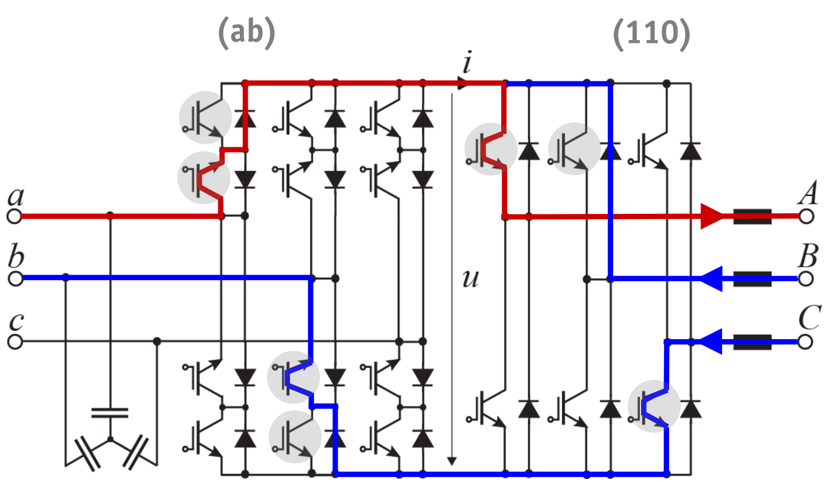


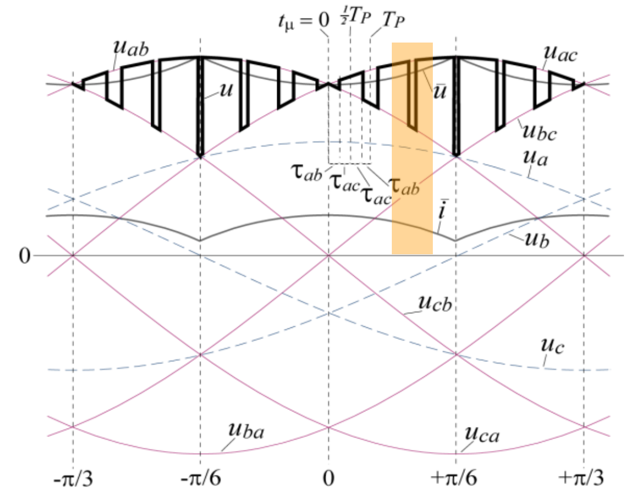
DC link Voltage & Current

PWM Pattern

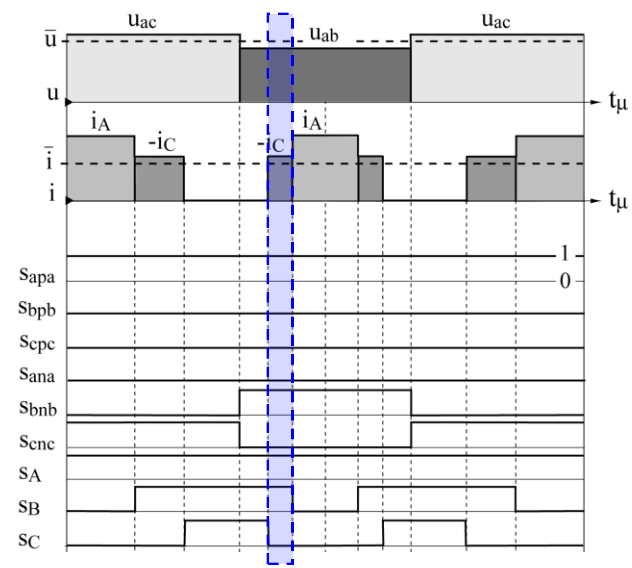
IMC Zero DC-link Current Commutation (5)

DC-link Voltage $u = u_{ab}$
DC-link Current $i = - i_C$





120°of Mains Period

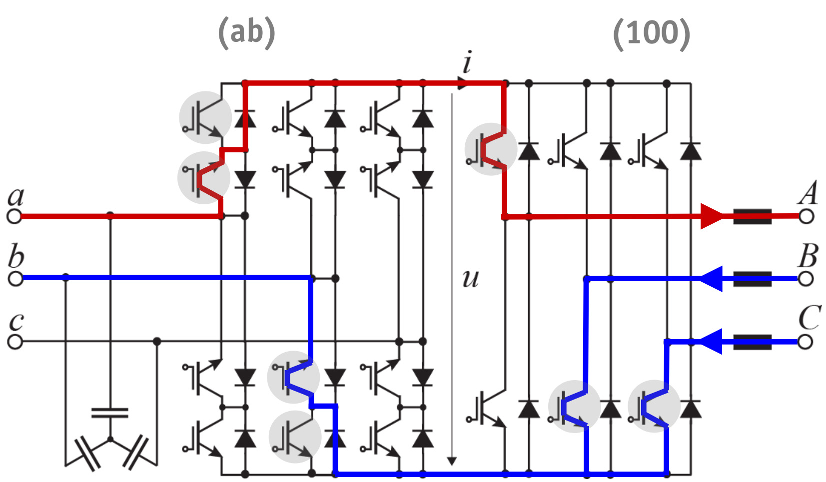


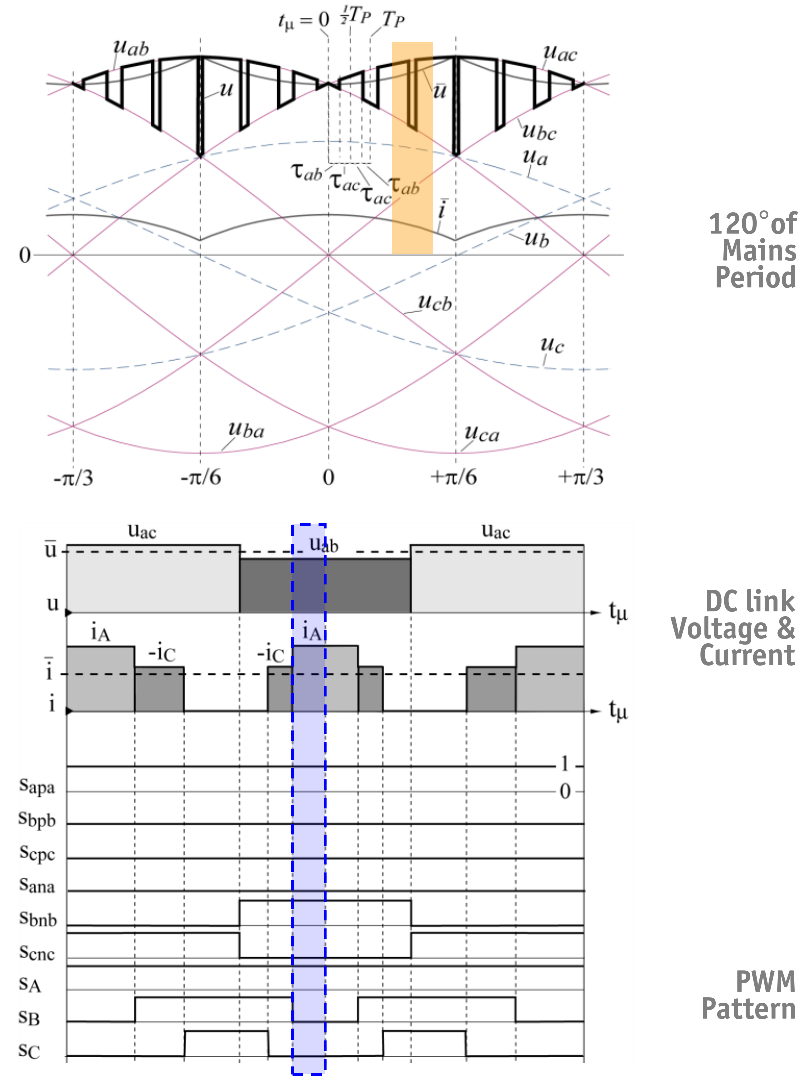
DC link Voltage & Current

PWM Pattern

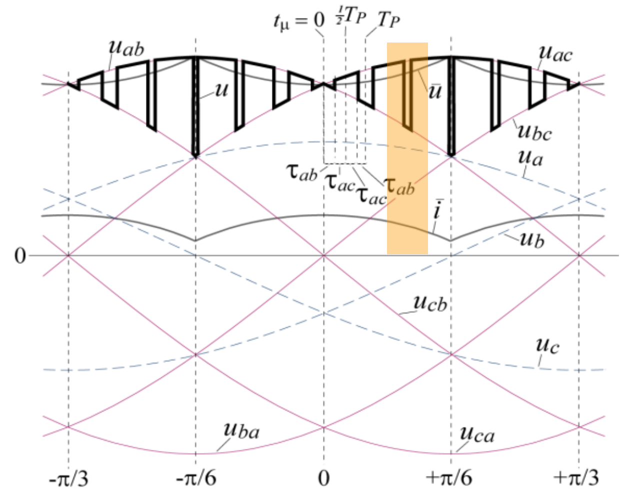
IMC Zero DC-link Current Commutation (6)

DC-link Voltage $u = u_{ab}$
DC-link Current $i = i_A$

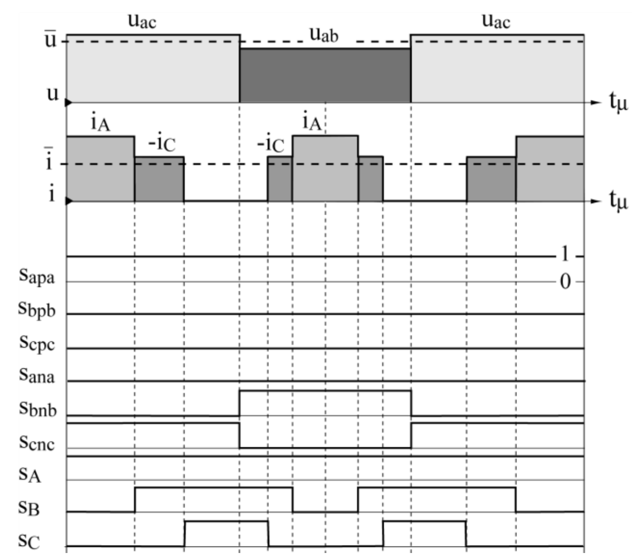




IMC Zero DC-link Current Commutation (7)



120° of Mains Period



DC link Voltage & Current

PWM Pattern

Summary

- **Simple and Robust** Modulation Scheme Independent of Commutation Voltage Polarity or Current Flow Direction
- **Negligible Rectifier Stage Switching Losses** Due to Zero Current Commutation

Coffee Break !

IMC Space Vector Modulation (3)

Output Voltage Ref. Value $\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$

Input Current Ref. Angle $\varphi^*_{\vec{i}_1}$ $\quad \vec{i}_1 = \hat{I}_1 e^{j\varphi^*_{\vec{i}_1}} \quad \varphi^*_{\vec{i}_1} = \varphi_{\vec{u}_1} - \Phi_1^*$

Mains Voltage $\vec{u}_1 = \hat{U}_1 e^{j\varphi_{\vec{u}_1}} = \hat{U}_1 e^{j\omega_1 t}$

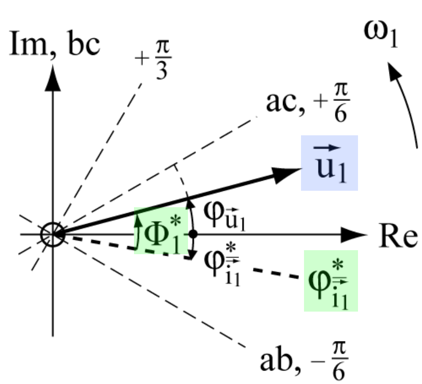
Load Behavior $\vec{i}_2 = \hat{I}_2 e^{j\varphi_{\vec{i}_2}} = \hat{I}_2 e^{j\left(\varphi_{\vec{u}_2^*} - \Phi_2\right)}$

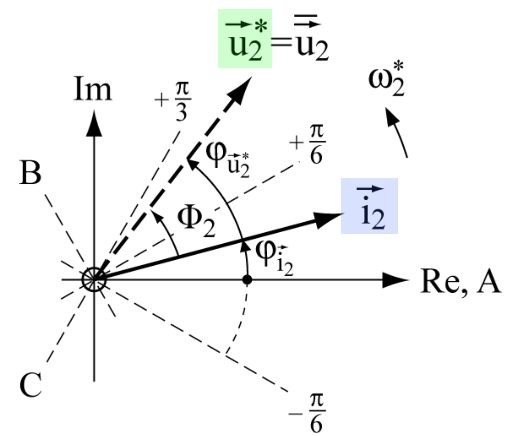
Assumptions

$$\varphi_{\vec{u}_1} \in \left[0, \frac{\pi}{6}\right]$$

$$\varphi_{\vec{u}_2^*} \in \left[0, \frac{\pi}{3}\right]$$

$$\varphi^*_{\vec{i}_1} \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$$





PWM Pattern is Specific for each Combination of Input Current and Output Voltage Sectors

Freewheeling Limited to Output Stage

$$d_{(ab)} + d_{(ac)} = 1$$

Input Current Formation

$$\bar{i}_a = \left(d_{(ab)} + d_{(ac)}\right) \bar{i} = \bar{i}$$

$$\bar{i}_b = -d_{(ab)} \bar{i}$$

$$\bar{i}_c = -d_{(ac)} \bar{i}$$

Desired Input Current

$$\bar{i}_a = \hat{I}_1 \cos \varphi^*_{\vec{i}_1}$$

$$\bar{i}_b = \hat{I}_1 \cos\left(\varphi^*_{\vec{i}_1} - \frac{2\pi}{3}\right)$$

$$\bar{i}_c = \hat{I}_1 \cos\left(\varphi^*_{\vec{i}_1} + \frac{2\pi}{3}\right)$$

Resulting Rectifier Stage Relative On-Times

$$\boxed{d_{(ab)} = \frac{\sin\left(\frac{\pi}{6} - \varphi^*_{\vec{i}_1}\right)}{\cos \varphi^*_{\vec{i}_1}}} \qquad \boxed{d_{(ac)} = \frac{\sin\left(\frac{\pi}{6} + \varphi^*_{\vec{i}_1}\right)}{\cos \varphi^*_{\vec{i}_1}}}$$

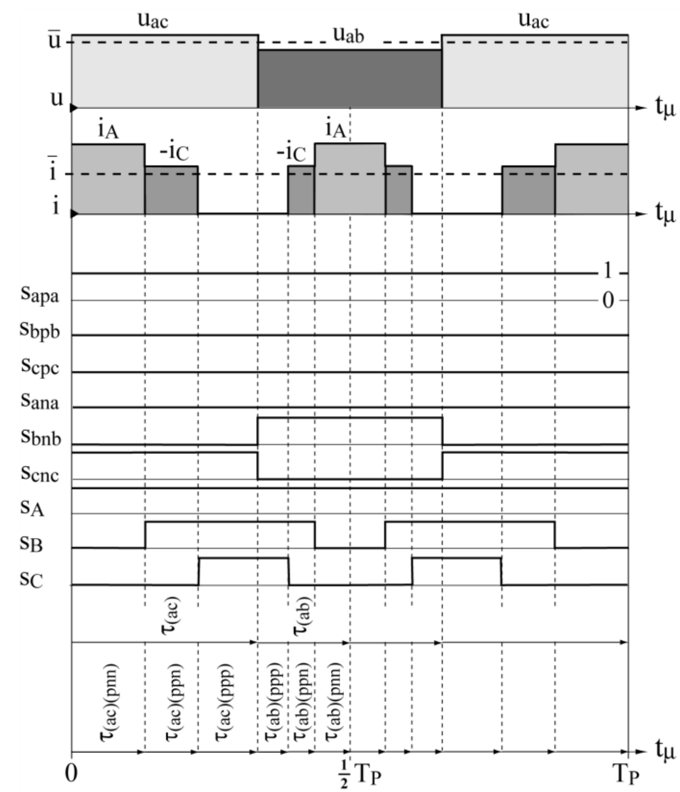
Absolute On-Times

$$\tau_{(ab)} = d_{(ab)} \frac{T_P}{2} \qquad \tau_{(ac)} = d_{(ac)} \frac{T_P}{2}$$

Mains Voltage

$$u_a = \hat{U}_1 \cos\left(\varphi_{\vec{u}_1}\right)$$
$$u_b = \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} - \frac{2\pi}{3}\right)$$
$$u_c = \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} + \frac{2\pi}{3}\right)$$

Switch Conducting the Largest Current is Clamped (over π/3-wide Interval)



Available DC Link Voltage Values

$$u_{(ac)} = u_{ac} = u_a - u_c = \sqrt{3} \cdot \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} - \frac{\pi}{6}\right)$$
$$u_{(ab)} = u_{ab} = u_a - u_b = \sqrt{3} \cdot \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} + \frac{\pi}{6}\right)$$

Select Identical Duty Cycles of Inverter Switching States (100), (110) in τ_{ac} and τ_{ab} for Maximum Modulation Range

$$\delta_{(ac)(pnn)} = \frac{\tau_{(ac)(pnn)}}{\tau_{(ac)}} = \delta_{(ab)(pnn)} = \frac{\tau_{(ab)(pnn)}}{\tau_{(ab)}} = \delta_{(pnn)}$$
$$\delta_{(ac)(ppn)} = \frac{\tau_{(ac)(ppn)}}{\tau_{(ac)}} = \delta_{(ab)(ppn)} = \frac{\tau_{(ab)(ppn)}}{\tau_{(ab)}} = \delta_{(ppn)}$$

Voltage Space Vectors Related to Active Inverter Switching States

$$\vec{u}_{2,(pnn)} = \frac{2}{3}u$$

$$\vec{u}_{2,(ppn)} = \frac{2}{3}u\,\mathrm{e}^{j\pi/3}$$

Output Voltage Formation

$$\begin{aligned}\bar{\vec{u}}_2 &= \frac{2/3}{T_P/2}\Big(\delta_{(ac)(pnn)}\tau_{(ac)}u_{ac} + \delta_{(ab)(pnn)}\tau_{(ab)}u_{ab} \\ &\qquad + \delta_{(ac)(ppn)}\tau_{(ac)}u_{ac}\mathrm{e}^{j\pi/3} + \delta_{(ab)(ppn)}\tau_{(ab)}u_{ab}\mathrm{e}^{j\pi/3}\Big) \\ &= \delta_{(pnn)}\frac{2}{3}\left(\frac{\tau_{(ac)}}{T_P/2}u_{ac} + \frac{\tau_{(ab)}}{T_P/2}u_{ab}\right) + \delta_{(ppn)}\frac{2}{3}\left(\frac{\tau_{(ac)}}{T_P/2}u_{ac} + \frac{\tau_{(ab)}}{T_P/2}u_{ab}\right)\mathrm{e}^{j\pi/3} \\ &= \delta_{(pnn)}\frac{2}{3}\left(d_{(ac)}u_{ac} + d_{(ab)}u_{ab}\right) + \delta_{(ppn)}\frac{2}{3}\left(d_{(ac)}u_{ac} + d_{(ab)}u_{ab}\right)\mathrm{e}^{j\pi/3}\end{aligned}$$

Local DC-link Voltage Average Value

$$\overline{u} = d_{(ac)}u_{ac} + d_{(ab)}u_{ab}$$

$$\bar{\vec{u}}_2 = \delta_{(pnn)}\frac{2}{3}\overline{u} + \delta_{(ppn)}\frac{2}{3}\overline{u}\,\mathrm{e}^{j\pi/3} \qquad \bar{\vec{u}}_2 = \vec{u}_2^{*}$$

Calculation of the Inverter Active Switching State On-Times can be directly based on $\bar{u}$!

DC-link Voltage Local Average Value

$$\overline{u} = \frac{3}{2}\cdot\hat{U}_1 \frac{\cos\left(\varphi_{\vec{u}_1} - \varphi^*_{\vec{i}_1}\right)}{\cos\left(\varphi^*_{\vec{i}_1}\right)} = \frac{3}{2}\cdot\hat{U}_1 \frac{\cos\left(\Phi^*_1\right)}{\cos\left(\varphi^*_{\vec{i}_1}\right)}$$

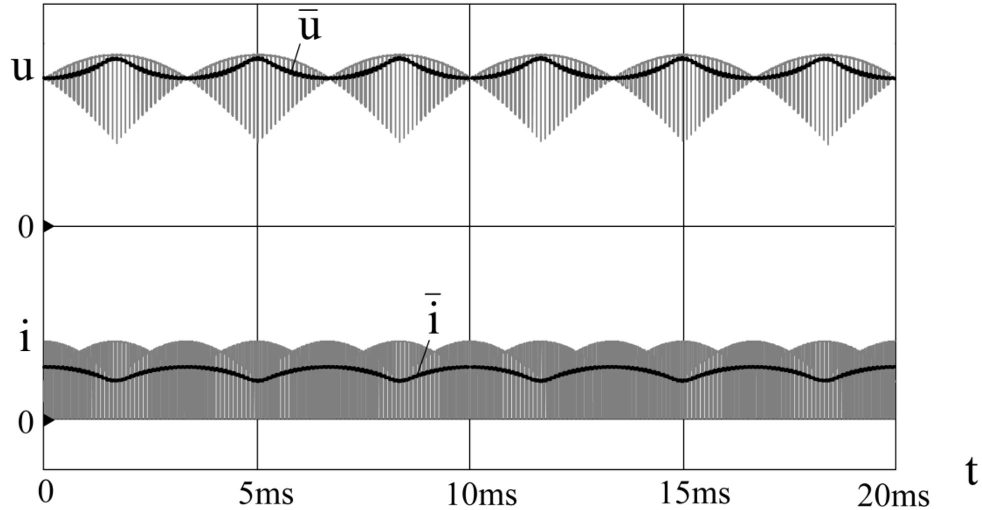
Minimum of DC-link Voltage Local Average Value

$$\overline{u}_{\min} = \frac{3}{2}\hat{U}_1 \cos\Phi^*_1$$

Resulting IMC Output Voltage Limit

$$\boxed{\hat{U}^*_{2,\max} \leq \frac{\sqrt{3}}{2}\cdot\hat{U}_1 \cos\Phi^*_1}$$

Simulation of DC-link Voltage and Current Time Behavior



Resulting Inverter Stage Relative On-Times

$$\delta_{(ppn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\overline{u}/2} \sin\left(\varphi_{\vec{u}_2^*}\right)$$

$$\delta_{(pnn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\overline{u}/2} \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right)$$

Resulting Inverter Stage Absolute On-Times

$$\tau_{(ac)(pnn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(pnn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{\hat{U}_1} \frac{1}{\cos \Phi_1^*} \sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1}^*\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right)$$

$$\tau_{(ac)(ppn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(ppn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{\hat{U}_1} \frac{1}{\cos \Phi_1^*} \sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1}^*\right) \sin\left(\varphi_{\vec{u}_2^*}\right)$$

DC-link Voltage Local Average Value

$$\bar{i}_{(ac)} = \frac{1}{\tau_{(ac)}}\left(i_A\delta_{(pnn)}\tau_{(ac)} - i_C\delta_{(ppn)}\tau_{(ac)}\right) = i_A\delta_{(pnn)} - i_C\delta_{(ppn)}$$

$$\bar{i}_{(ab)} = \frac{1}{\tau_{(ab)}}\left(i_A\delta_{(pnn)}\tau_{(ab)} - i_C\delta_{(ppn)}\tau_{(ab)}\right) = i_A\delta_{(pnn)} - i_C\delta_{(ppn)}$$

Equal DC-link Current Local Average Values for Inverter Active Switching States

$$\bar{i} = \bar{i}_{(ac)} = \bar{i}_{(ab)} = \hat{I}_2\frac{\hat{U}_2^*}{\hat{U}_1}\frac{\cos\Phi_2}{\cos\Phi_1^*}\cos\varphi^*_{\vec{i}_1}$$

Local Average Value of Input Current in *a*

$$\bar{i}_a = \bar{i} = \hat{I}_1\cos\varphi^*_{\vec{i}_1}$$

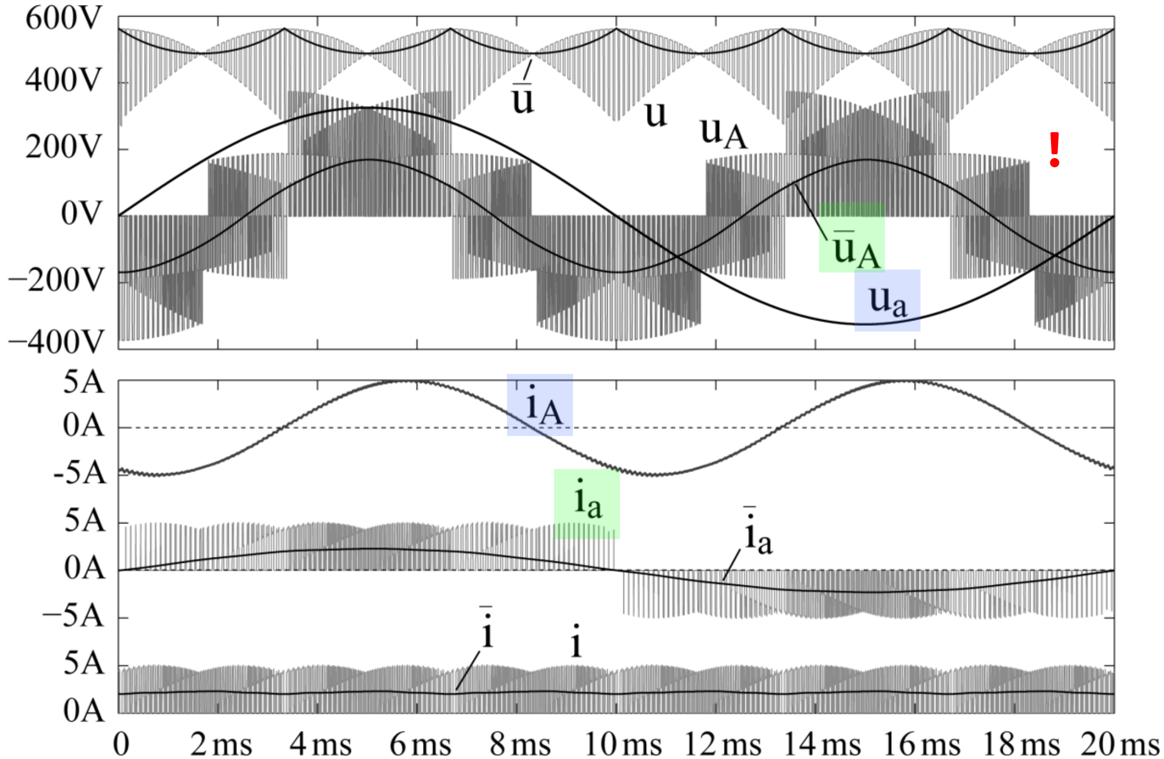
Resulting Input Phase Current Amplitude

$$\hat{I}_1 = \hat{I}_2\frac{\hat{U}_2^*}{\hat{U}_1}\frac{\cos\Phi_2}{\cos\Phi_1^*}$$

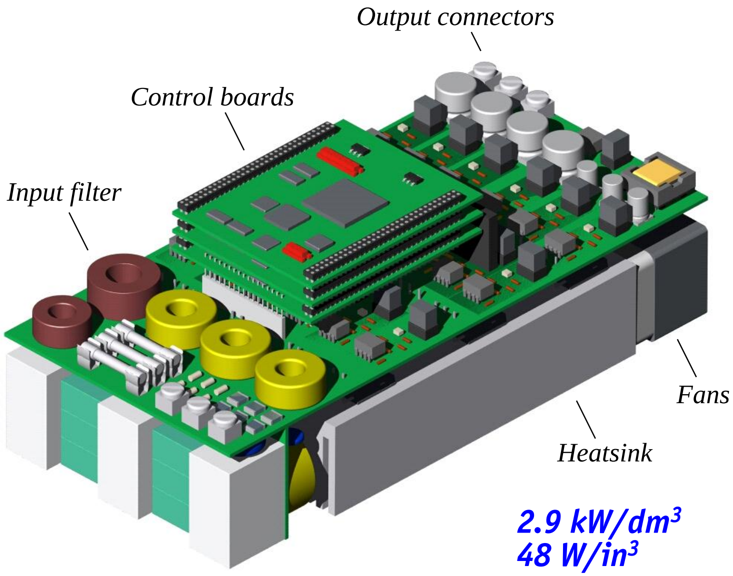
Power Balance of Input and Output Side

$$\bar{p} = P = \bar{u}\,\bar{i} = \frac{3}{2}\hat{U}_1\hat{I}_1\cos\Phi_1^* = \frac{3}{2}\hat{U}_2^*\hat{I}_2\cos\Phi_2$$

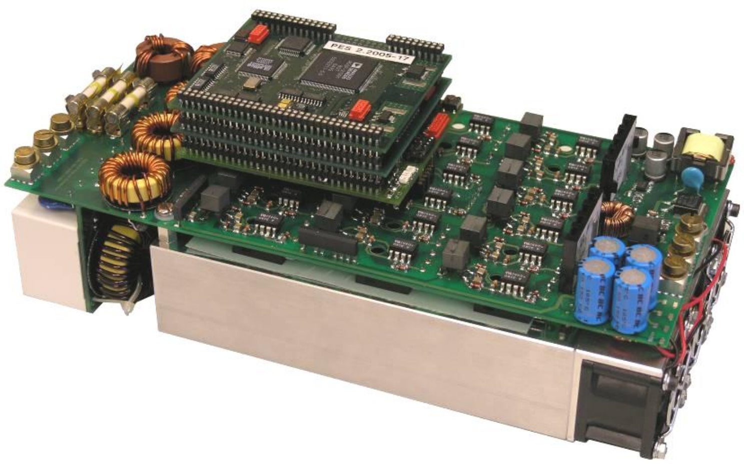
IMC Simulation Results



RB-IGBT IMC Experimental Results (1)



2.9 kW/dm^3
48 W/in^3



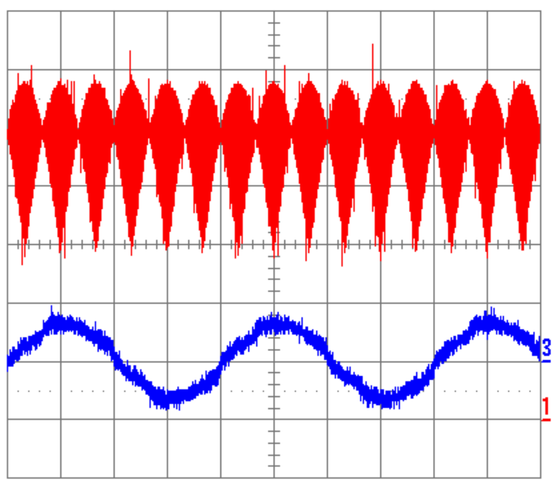
Input RMS voltage	*400V*
Output Power	*6.8 kVA*
Rectifier Switching Frequency	*12.5 kHz*
Inverter Switching Frequency	*25 kHz*

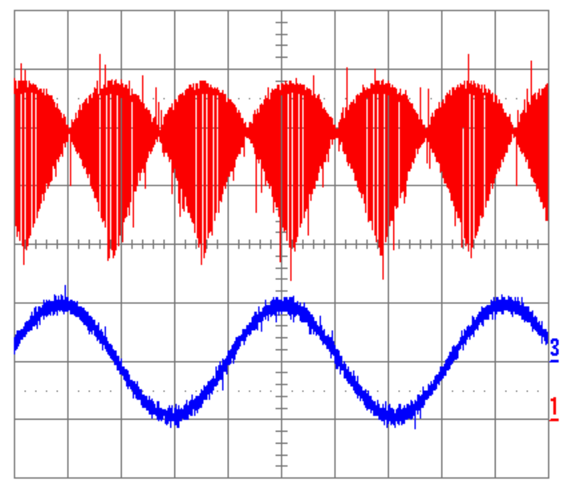
Efficiency 95%

RB-IGBT IMC Experimental Results (2)

U_{12} = 400V
P_{out} = 1.5 kW
f_{out} = 120 Hz
f_S = 12.5 kHz / 25kHz

DC Link Voltage





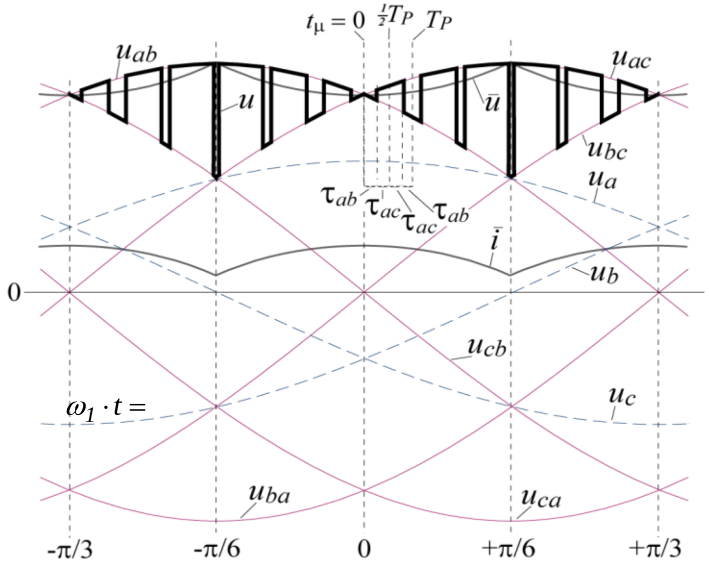
Input Current

Output Current

100 V/div
5A/div

Alternative Modulation Schemes (1)

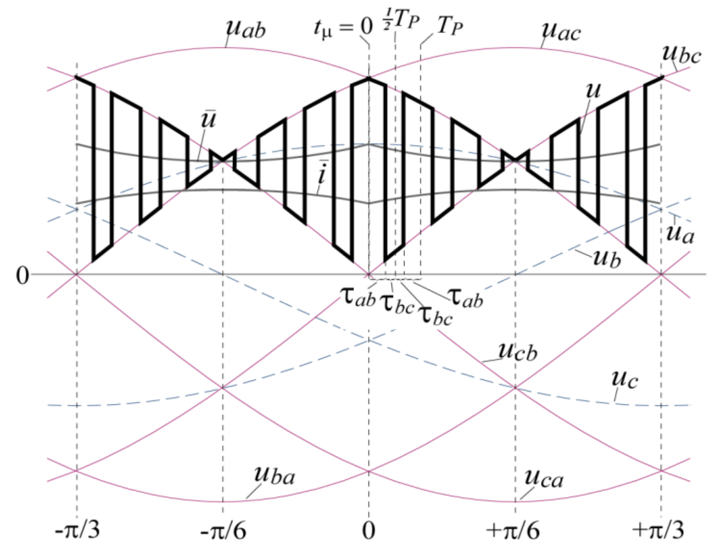
► Conventional Modulation (HV)



DC-link Voltage: *Largest and Medium Line-to-Line Mains Voltage*

$$\hat{U}_{2,max,I} = \frac{\sqrt{3}}{2}\hat{U}_1 \approx 0.86 \cdot \hat{U}_1 \quad !$$

► Low Output Voltage Modulation (LV)

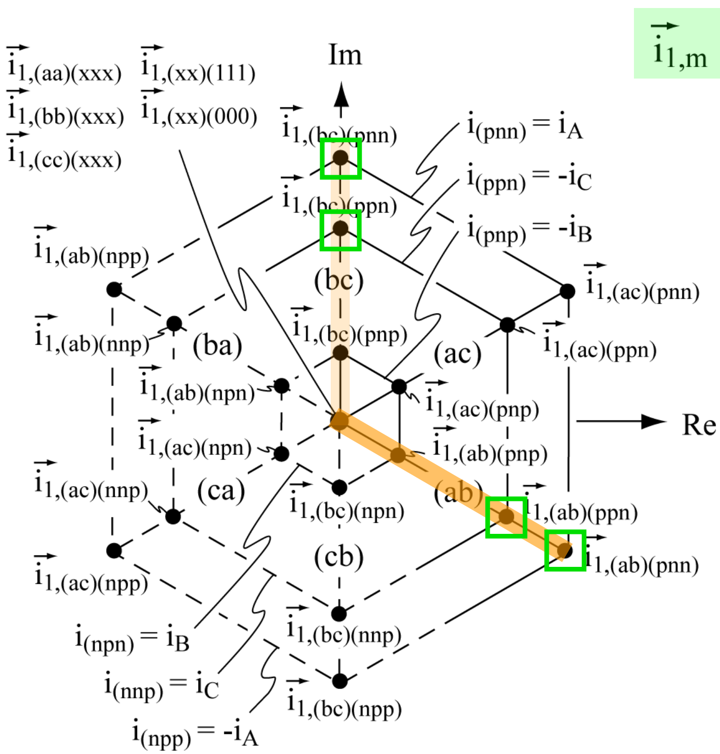


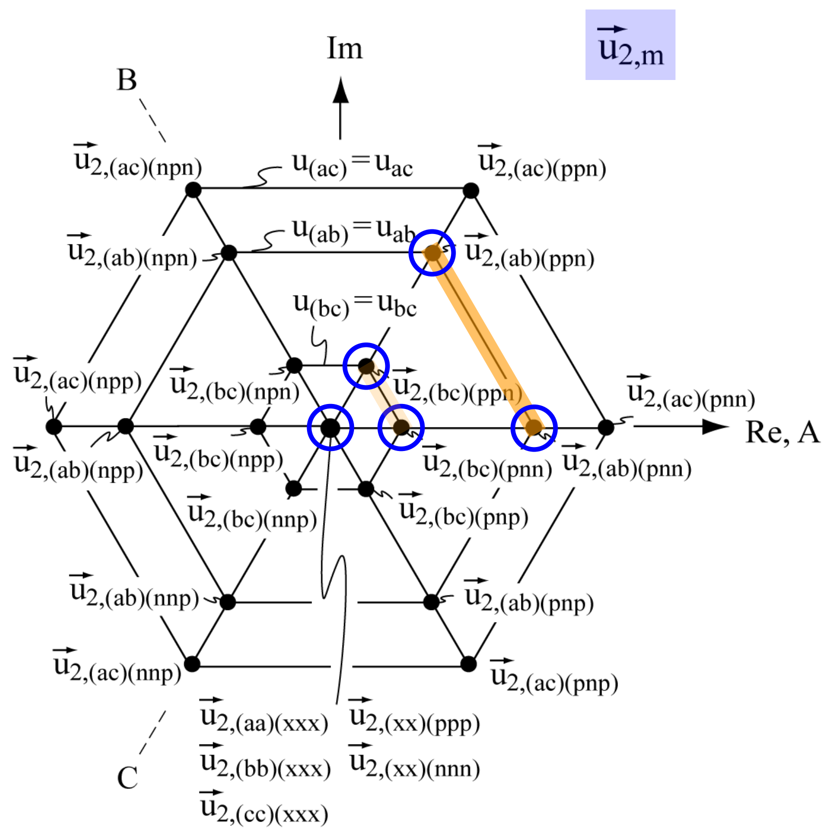
DC-link Voltage: *Medium and Smallest Line-to-Line Mains Voltage*

$$\hat{U}_{2,max,II} = \frac{1}{2}\hat{U}_1 = 0.5 \cdot \hat{U}_1 \quad !$$

Alternative Modulation Schemes (2)

▶ Low Output Voltage Modulation



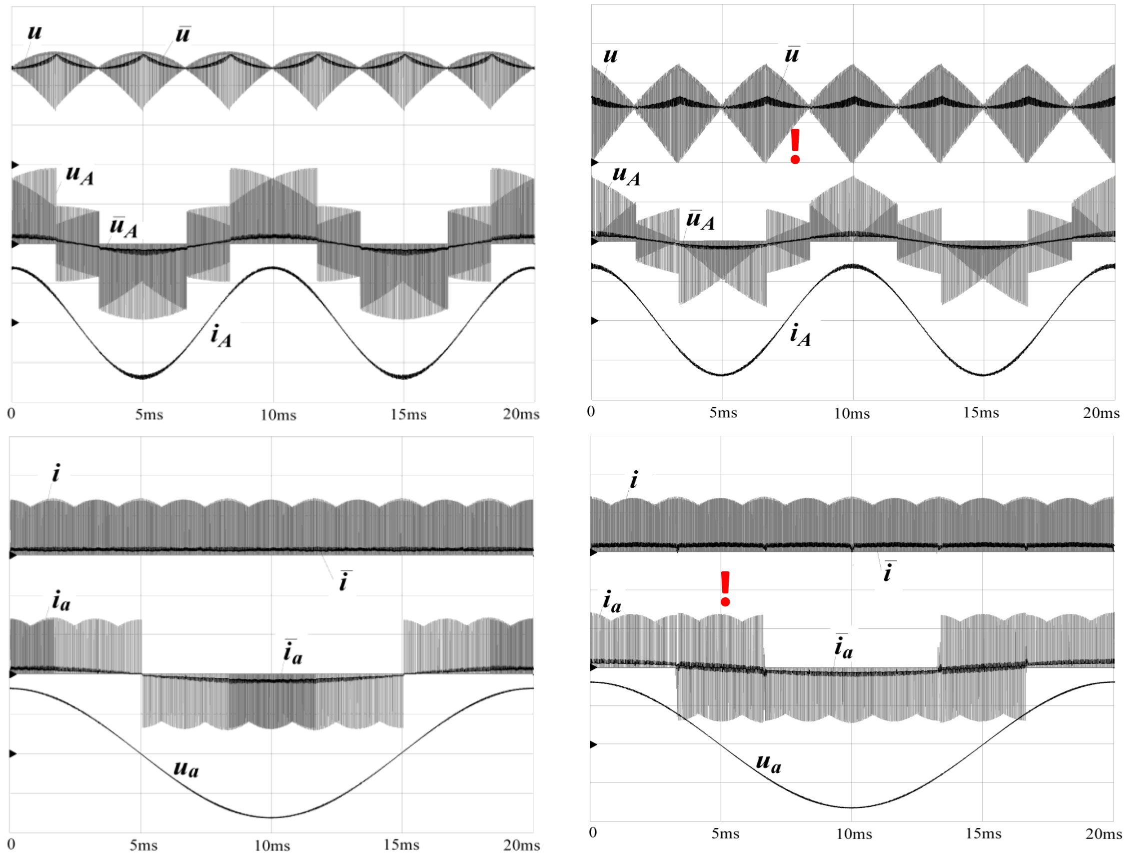


Alternative Modulation Schemes (3)

► LV vs. HV Modulation

Output Voltage Generation

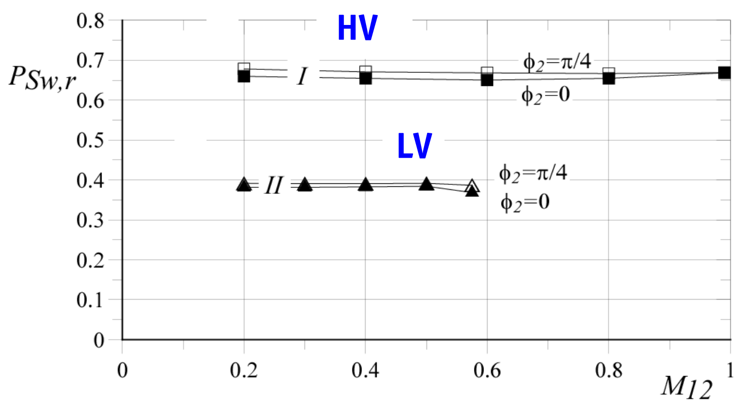
Input Current Generation



Alternative Modulation Schemes (4)

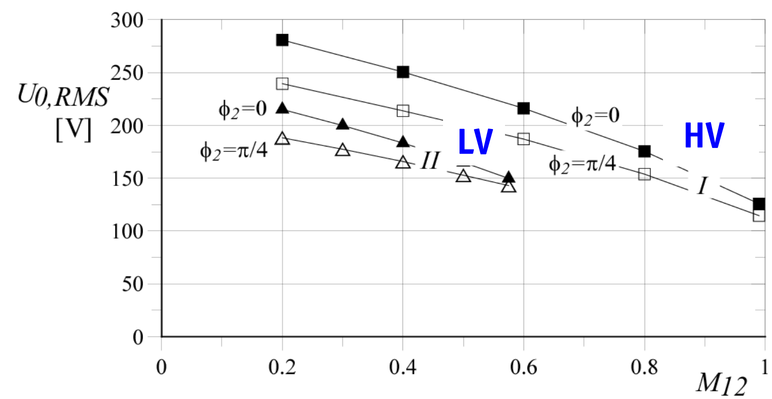
▶ **LV vs. HV Modulation**

Switching Losses



Reduction of Switching Losses to approx. 58%

Output Common Mode Voltage

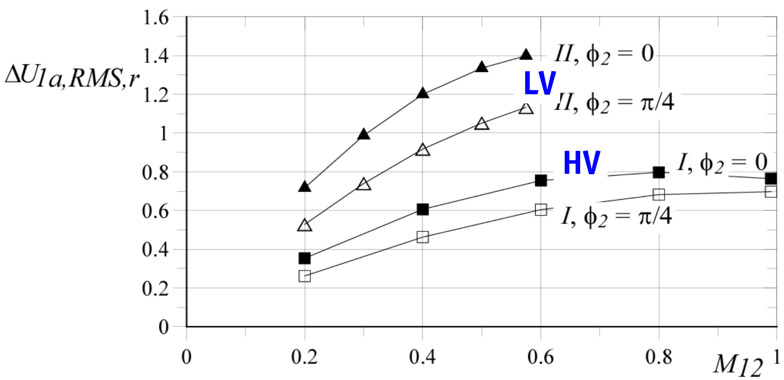


Output Common Mode Voltage reduced to approx. 75%

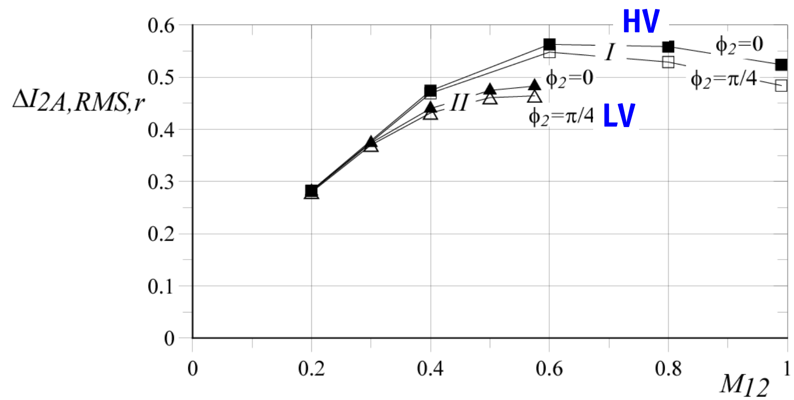
Alternative Modulation Schemes (5)

▶ LV vs. HV Modulation

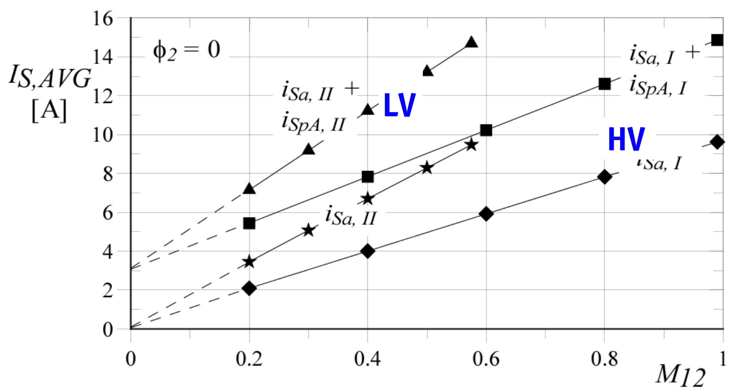
Input Voltage Ripple



Output Current Ripple



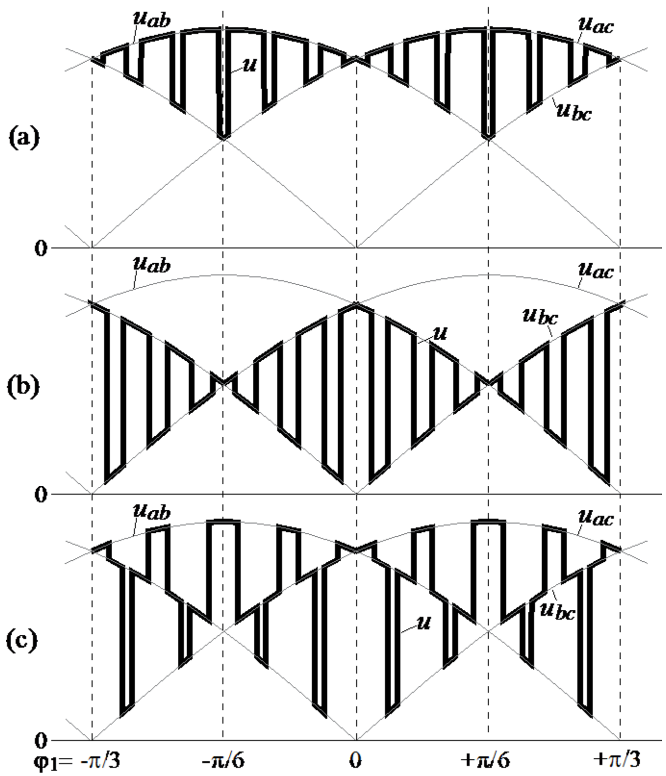
Current Stresses



- Input Voltage Ripple Doubles
- Output Current Ripple Slightly Reduced
- For given $\hat{U}_2$ (M_{12}) the Component Current Stress are Increasing (Conduction Losses)

Alternative Modulation Schemes (6)

▶ Three-Level Medium Voltage Modulation



High Output Voltage Modulation (HVM)

$$\hat{U}_2 = 0 \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

Low Output Voltage Modulation (LVM)

$$\hat{U}_2 = 0 \ldots \frac{1}{2} \cdot \hat{U}_1$$

Three-Level Modulation

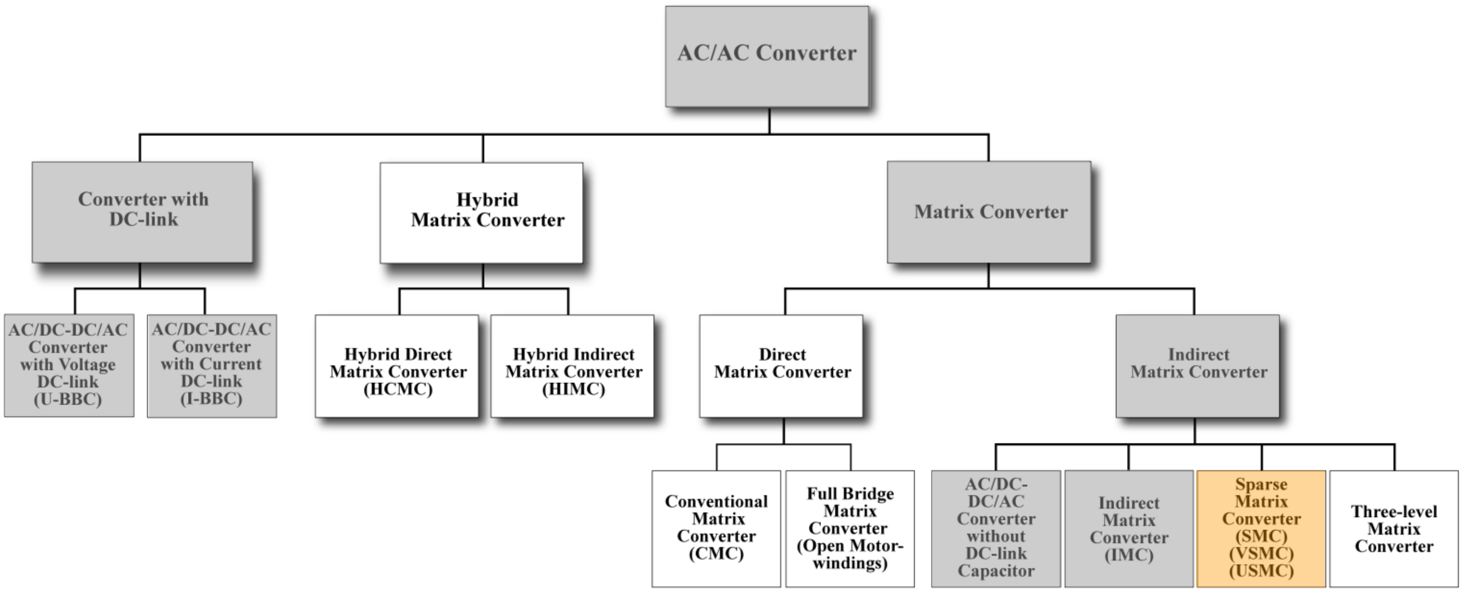
$$\hat{U}_2 = \frac{1}{2} \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

Weighted Combination of HVM and LVM

Sparse Matrix Converter - SMC

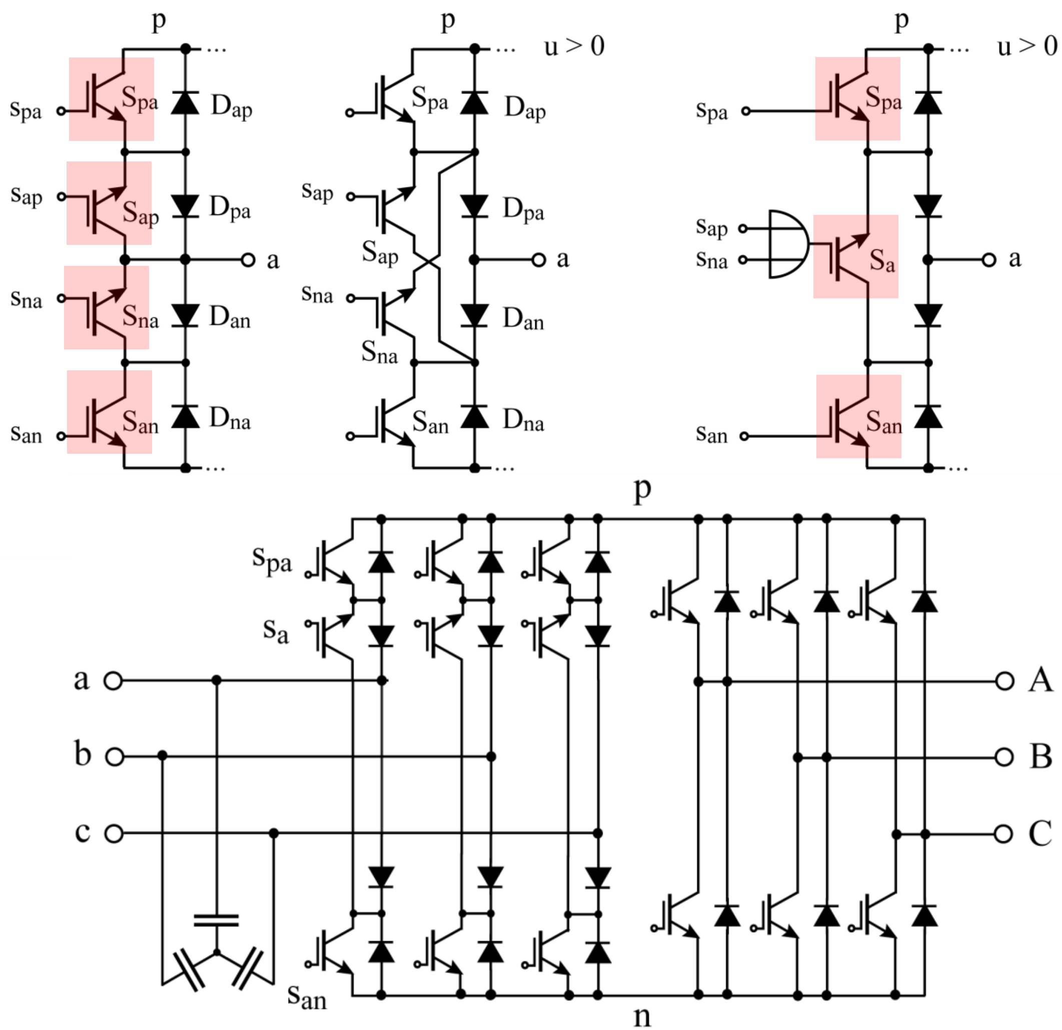
Topology Derivation
Bidirectional / Unidirectional Converter
Experimental Results

Classification of Three-Phase AC-AC Converters



- *Sparse Matrix Converter*

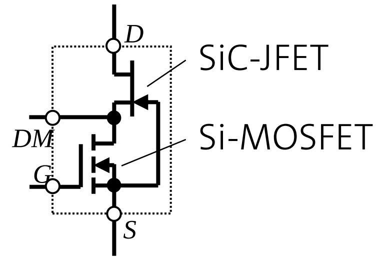
Sparse Matrix Converter



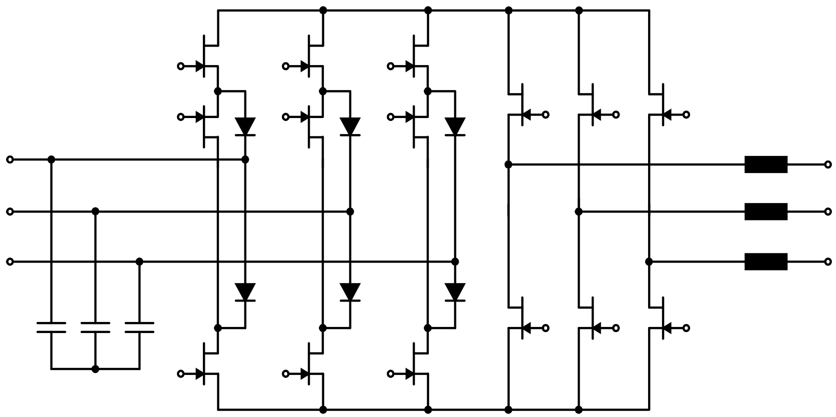
ETH Zurich

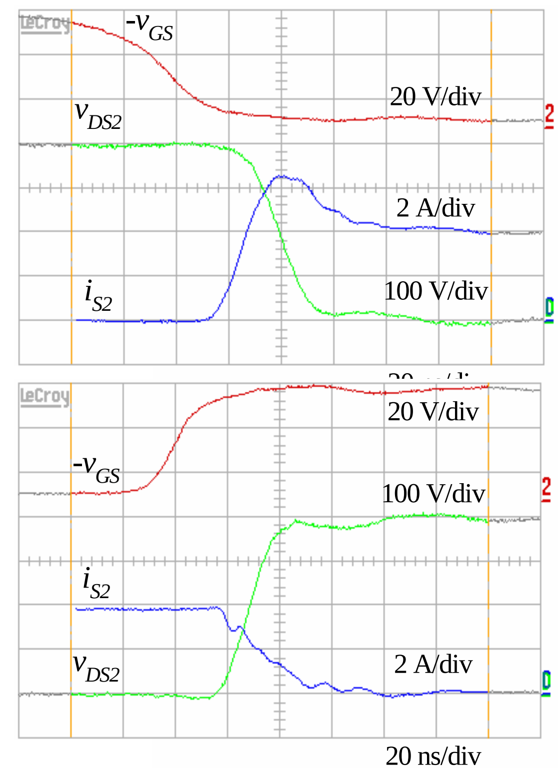
- *15 Transistors*
- *18 Diodes*

SiC Sparse Matrix Converter

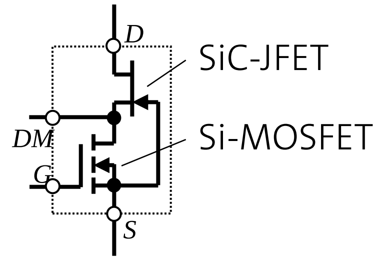


Switching Frequency **150kHz**
Output Power **2.5kW@10kW/dm³**

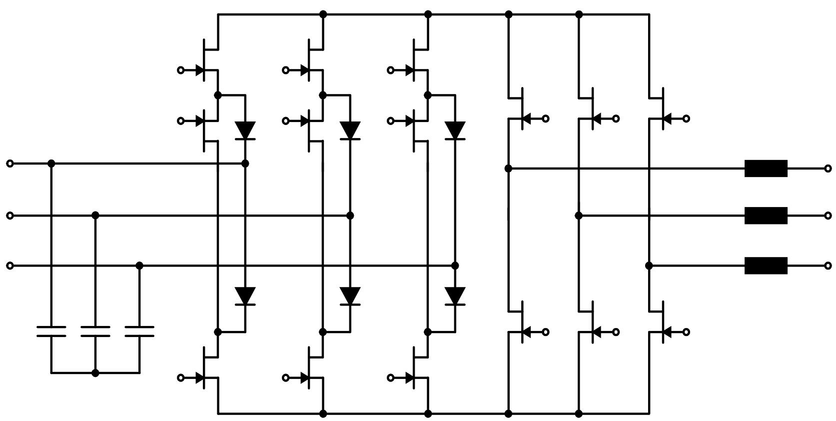




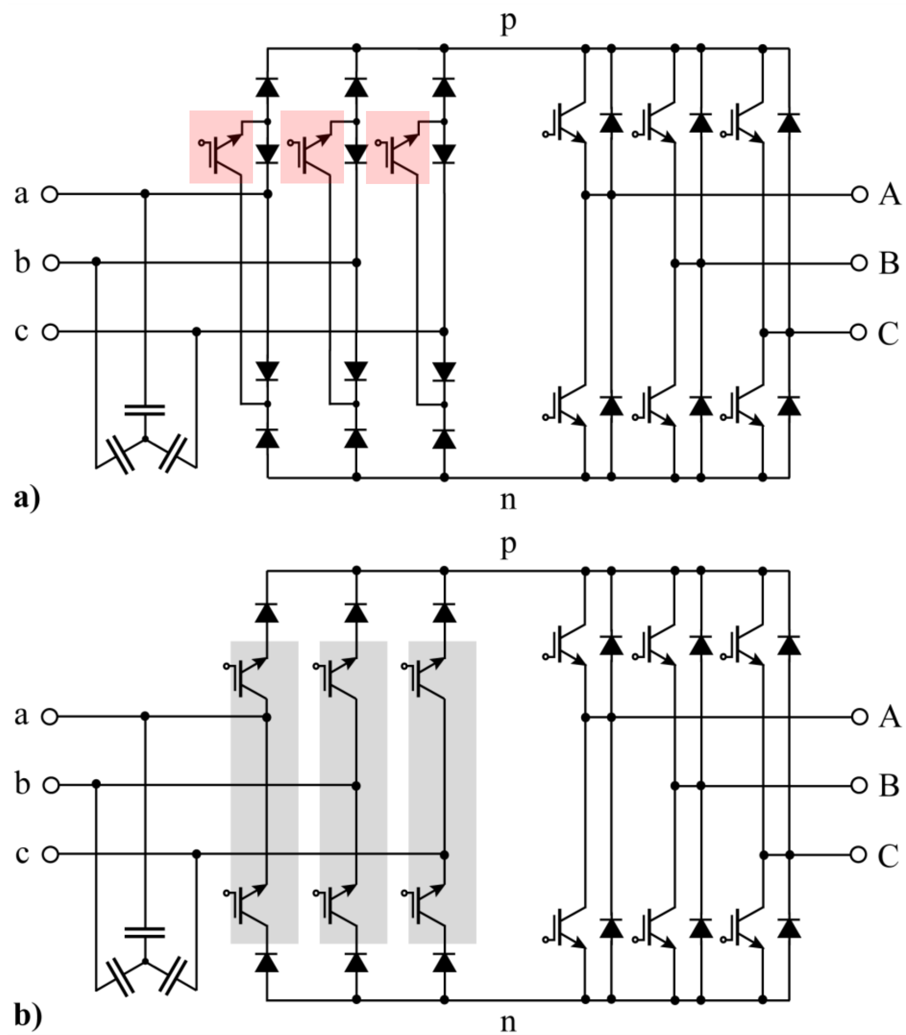
SiC Sparse Matrix Converter



Switching Frequency 150kHz
Output Power 2.5kW@10kW/dm^3



Ultra Sparse Matrix Converter



ETH Zurich
T. Lipo [13, 20]

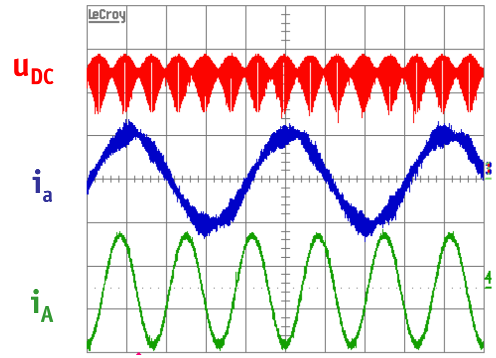
- *9 Transistors*
- *18 Diodes*

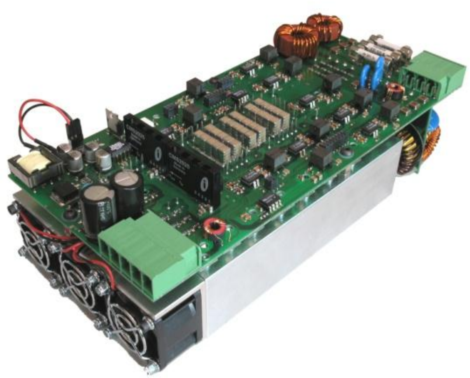
Ultra Sparse Matrix Converter

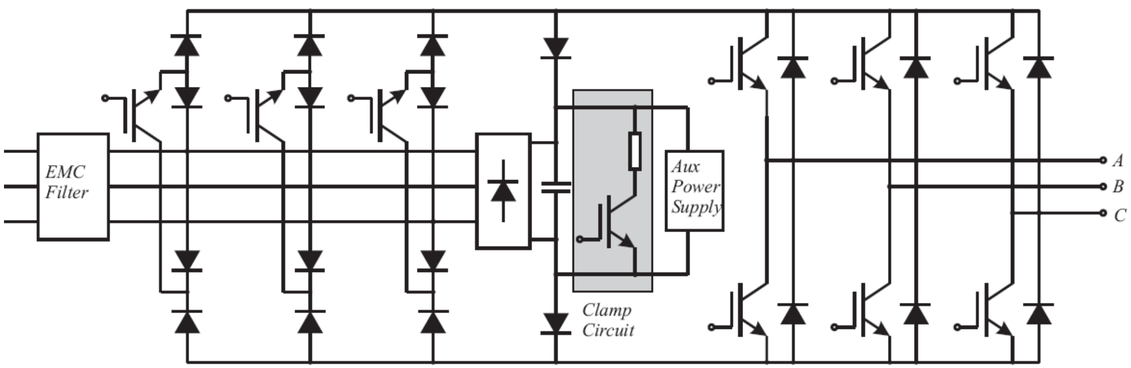
U_{in} = 3-Φ 400V/50Hz
U_{out} = 3-Φ 0...340V / 0...200Hz
P = 5.5kVA

f_S = 25kHz (Rect.) / 50kHz (Inv.)

200V/div
2A/div
5ms/div



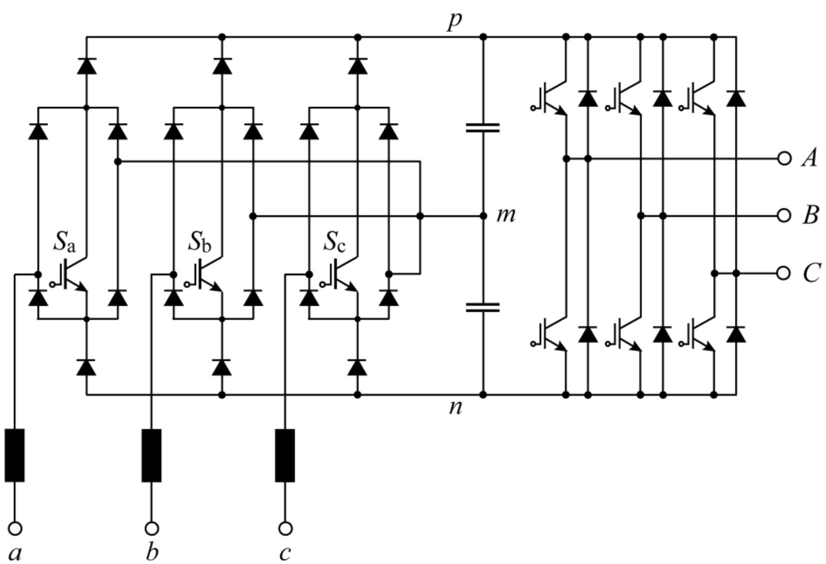




!

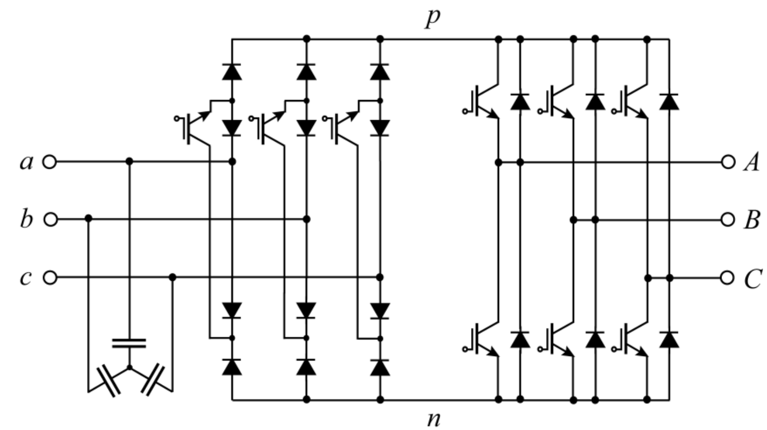
Unidirectional 9-Switch AC-AC Converters with PFC Input

VIENNA Rectifier with VSI (VR-VSI)



- With Intermediate Energy Storage
- 3-Level Input Stage
- Impressed Currents at Input Terminals (a,b,c)
- Additional DC-Link Chopper Required

Ultra Sparse Matrix Converter (USMC)



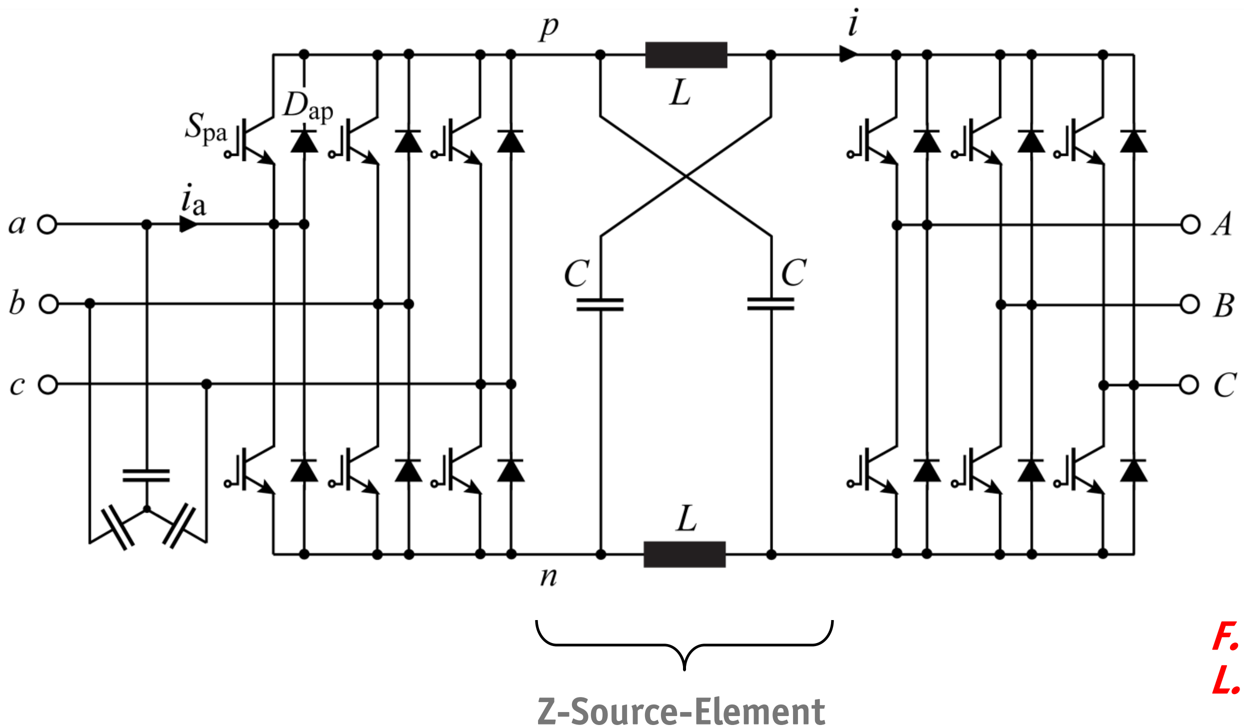
- Without Intermediate Energy Storage
- “Quasi” 3-Level Output
- Impressed Voltages at Input Terminals (*a*,*b*,*c*)
- Additional DC-Link Chopper/Clamp Required

Topologies with LC-Element in DC-Link

Z-Source Converter ZSC
T-Source Converter TSC

Z-Source Converter

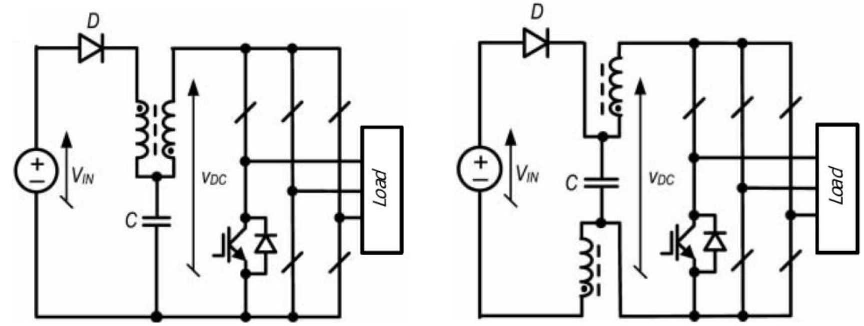
F³E-Topology with Z-Source-Element (LC-Element) in DC-Link



F. Z. Peng [45]
L. Sack [46]

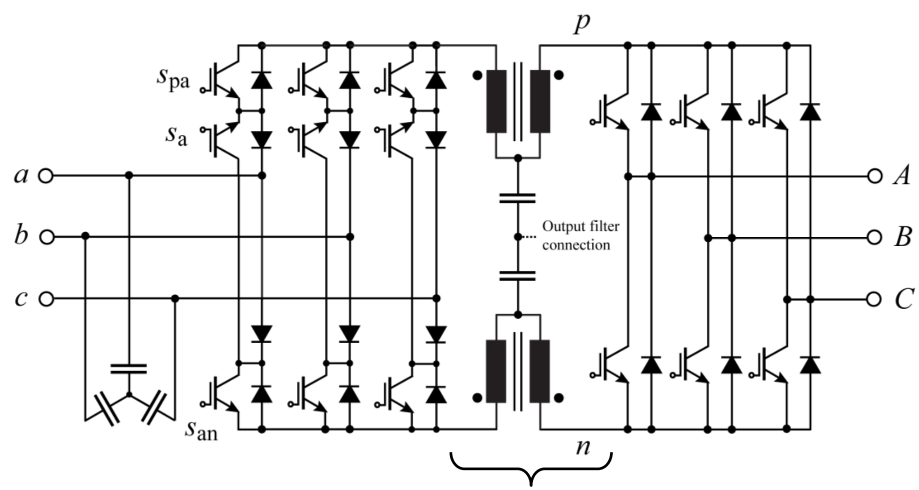
T-Source Converters

- Suggested 2-Level T-Source Inverter Topologies by Strzelecki et al. [46], 2009, and Trans-Z-Source Inverter by Quian et al. [48], 2010.



T-Source "Sparse Matrix Related" AC-AC Converter

- IMC-Based Modulation Scheme
- Output Voltage Boost Capability
- Low Input Stage Switching Losses
- High Blocking Voltage Require-ments of Output Side Switches
- Need for Low Leakage Transformer

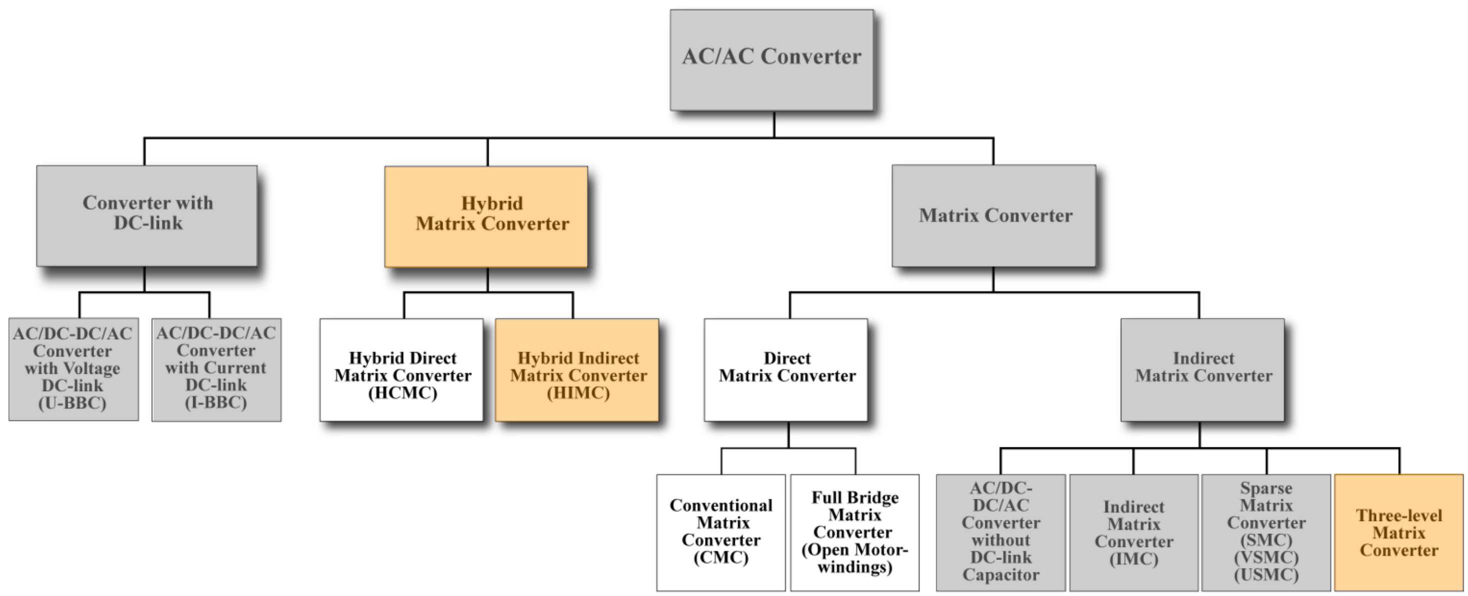


Double T-Source with HF Autotransformer

IMC - Extensions

- *Three-Level*
- *Hybrid*

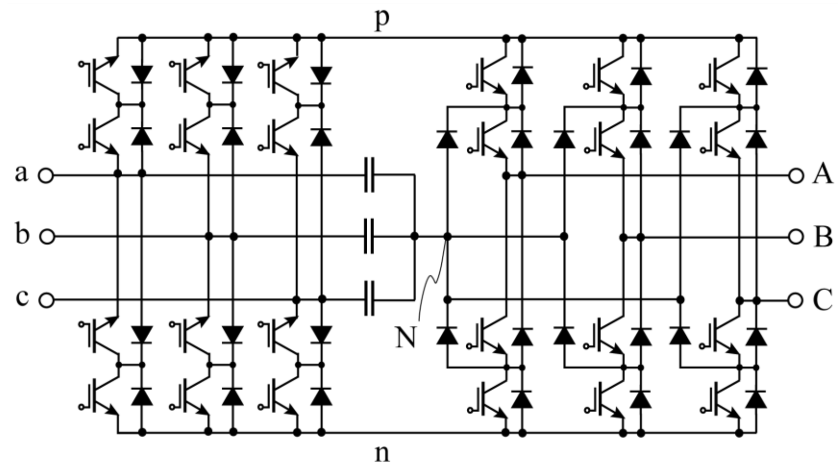
Classification of Three-Phase AC-AC Converters



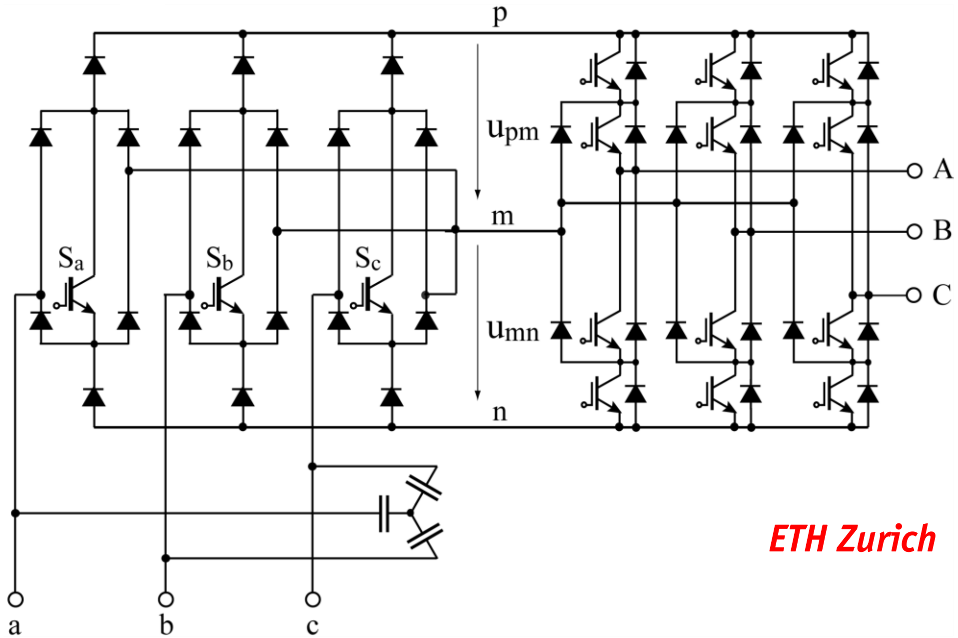
- *Three-Level IMC*
- *Hybrid IMC*

Three-Level Matrix Converter

▶ *Bidirectional Converter*

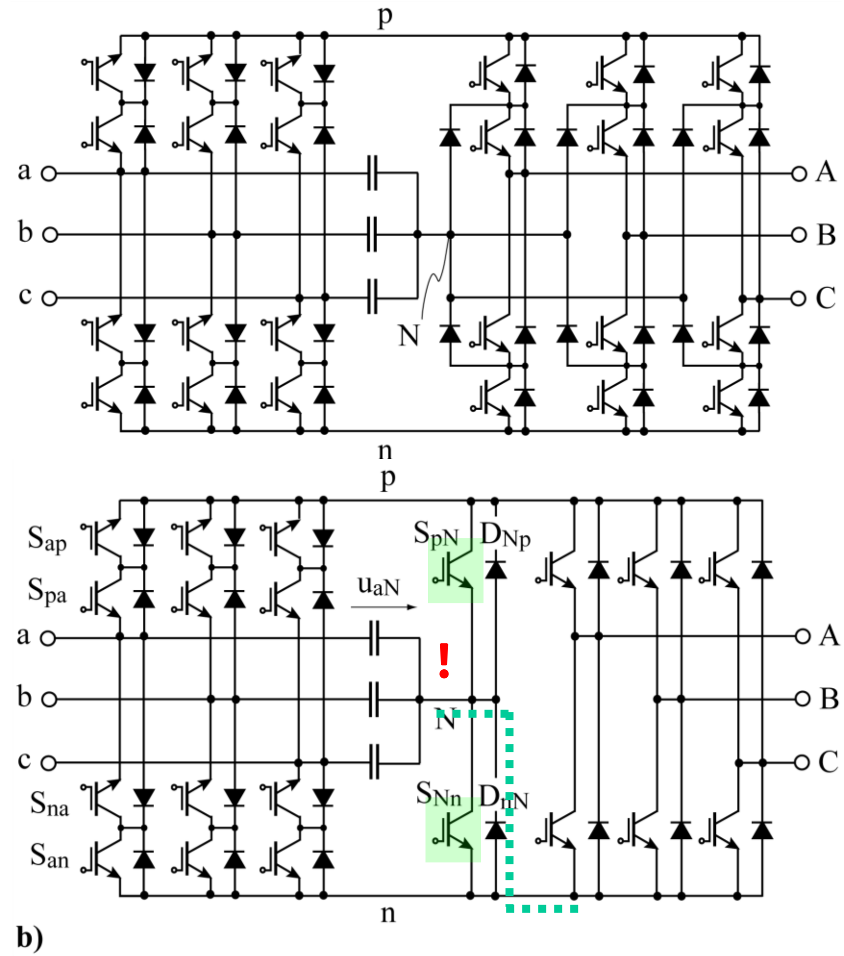


▶ *Unidirectional Converter*



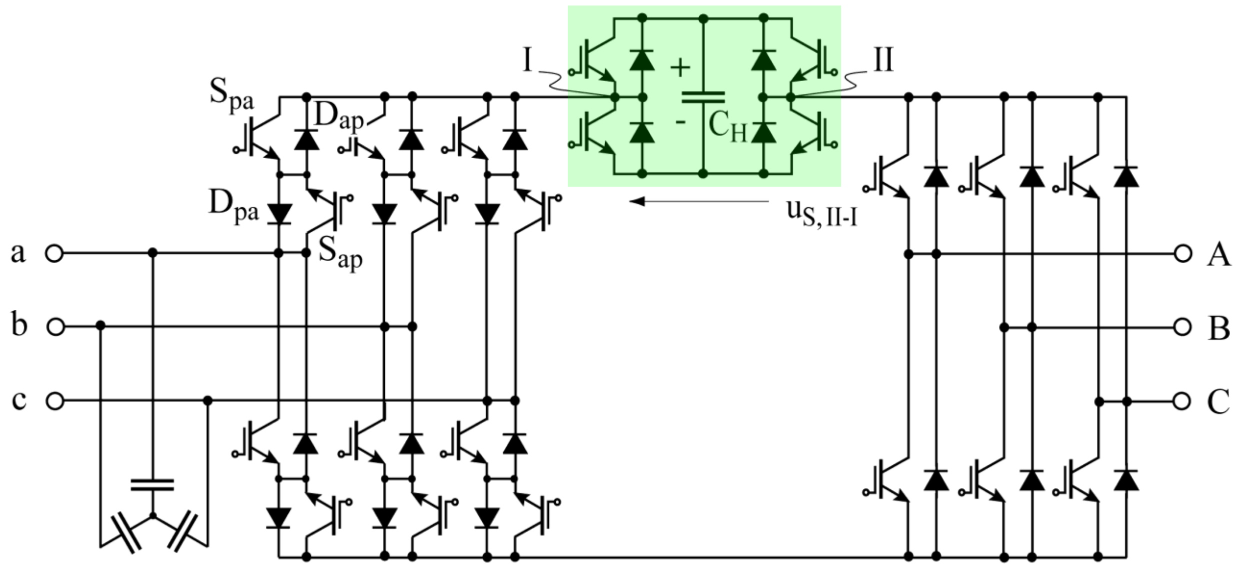
ETH Zurich

Three-Level Matrix Converter



Ch. Klumpner [23, 24]

Hybrid IMC

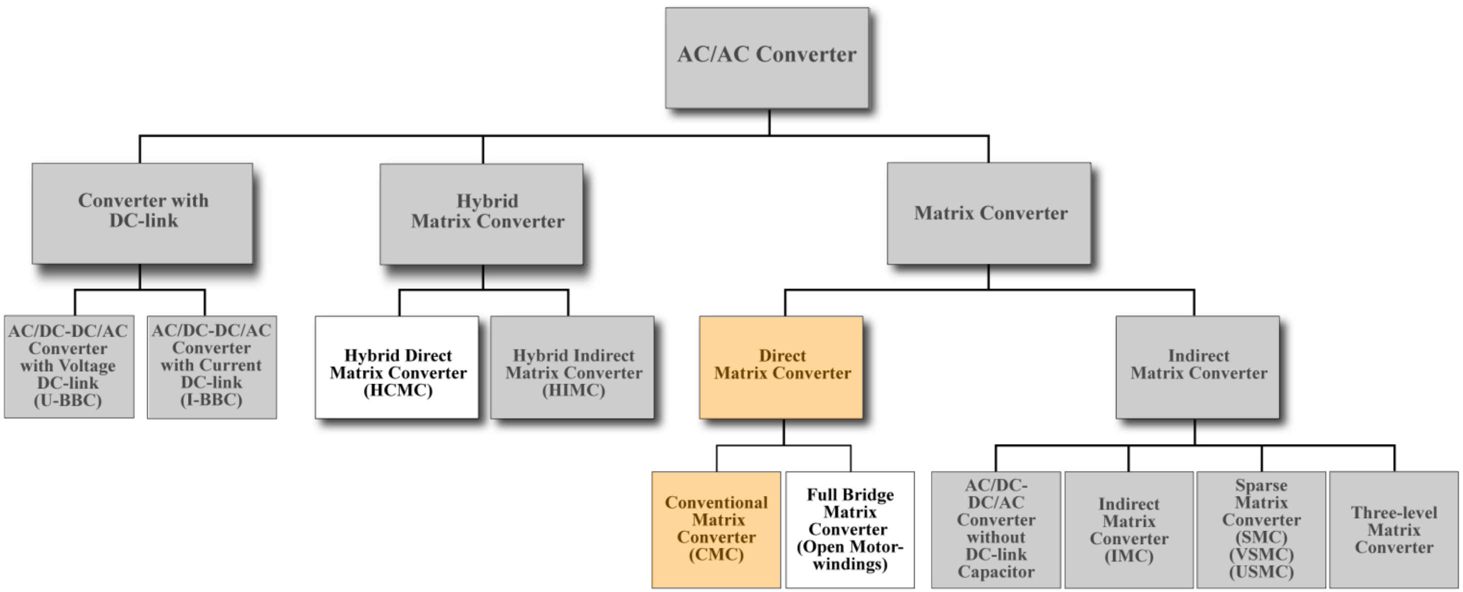


Ch. Klumpner [5, 6]

Conventional Matrix Converter - CMC

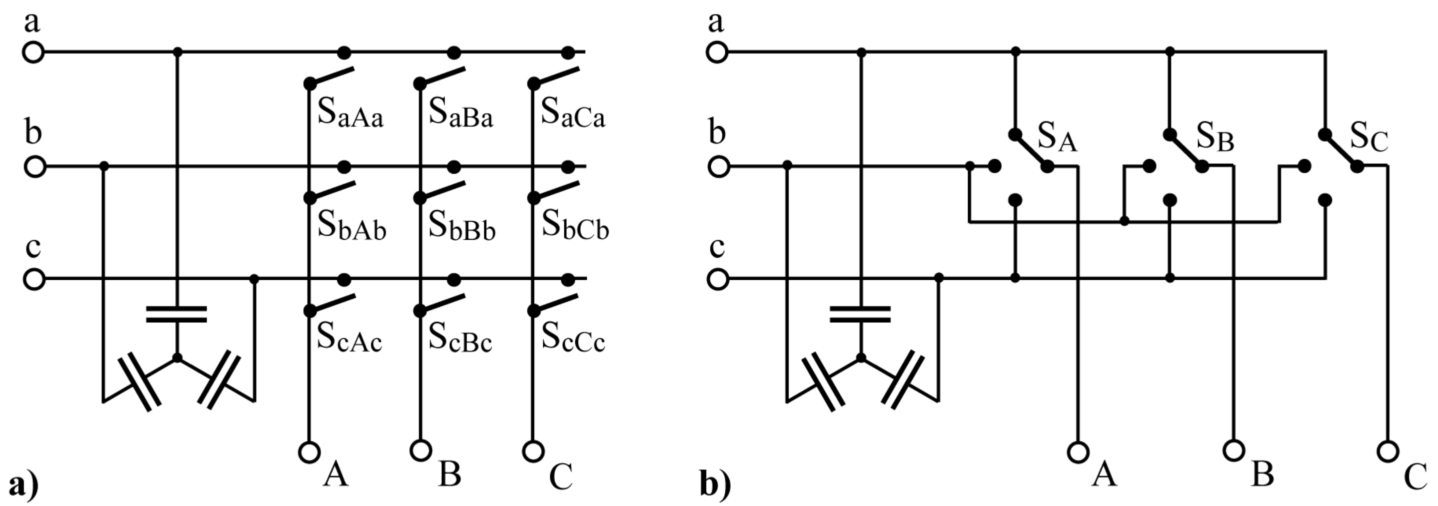
Modulation
Multi-Step Commutation

Classification of Three-Phase AC-AC Converters



- ***Conventional Matrix Converter***

Conventional Matrix Converter – CMC



► *Quasi Three-Level Characteristic*

CMC Classification of Switching States

Group I

Freewheeling States

$$(\mathrm{aaa}) \quad (\mathrm{bbb}) \quad (\mathrm{ccc})$$

Group II

Generating Stationary Output Voltage and Input Current Space Vectors

$$\left.\begin{matrix} (\mathrm{cca}) & (\mathrm{ccb}) & (\mathrm{aab}) \\ (\mathrm{aac}) & (\mathrm{bbc}) & (\mathrm{bba}) \end{matrix}\right\} u_{AB} = 0$$

$$\left.\begin{matrix} (\mathrm{acc}) & (\mathrm{bcc}) & (\mathrm{baa}) \\ (\mathrm{caa}) & (\mathrm{cbb}) & (\mathrm{abb}) \end{matrix}\right\} u_{BC} = 0$$

$$\left.\begin{matrix} (\mathrm{cac}) & (\mathrm{cbc}) & (\mathrm{aba}) \\ (\mathrm{aca}) & (\mathrm{bcb}) & (\mathrm{bab}) \end{matrix}\right\} u_{CA} = 0$$

Group III

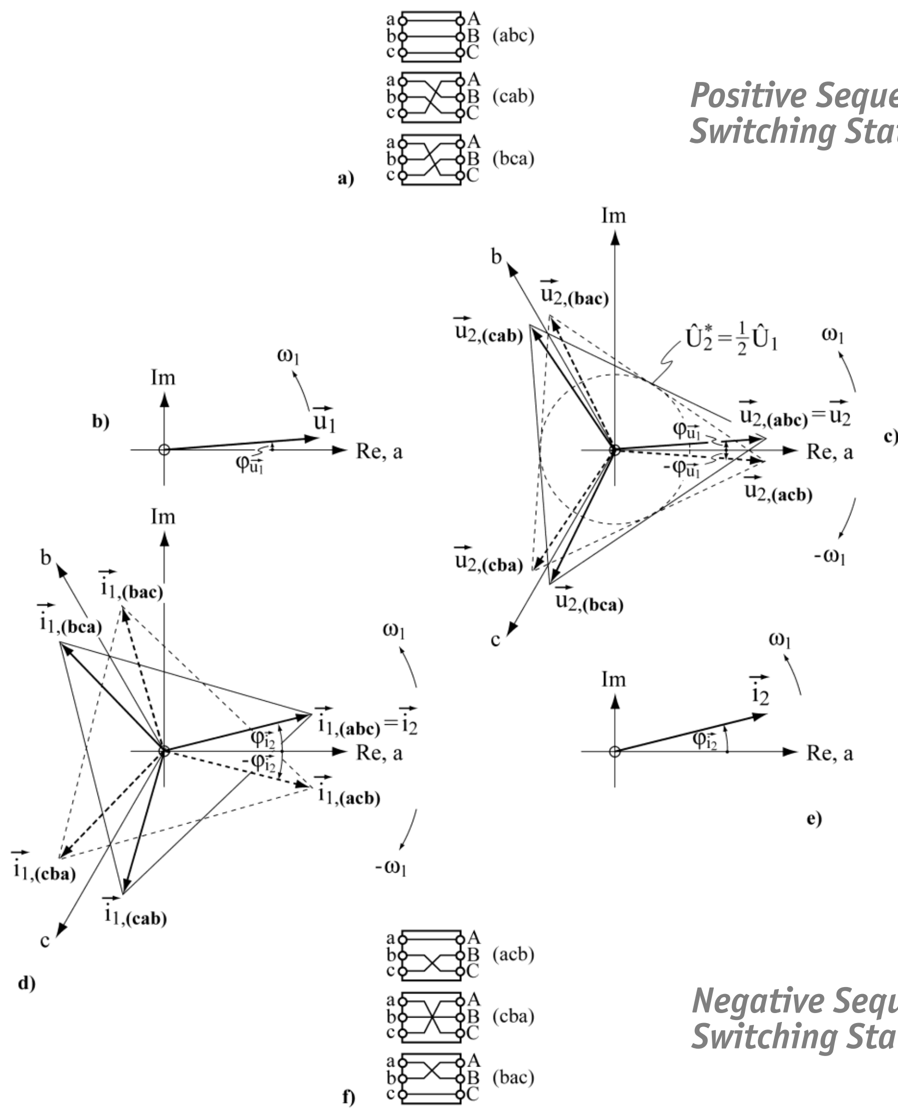
Generating Rotating Space Vectors

$(\mathrm{abc}) \quad (\mathrm{cab}) \quad (\mathrm{bca})$ *Positive Sequence*

$(\mathrm{acb}) \quad (\mathrm{cba}) \quad (\mathrm{bac})$ *Negative Sequence*

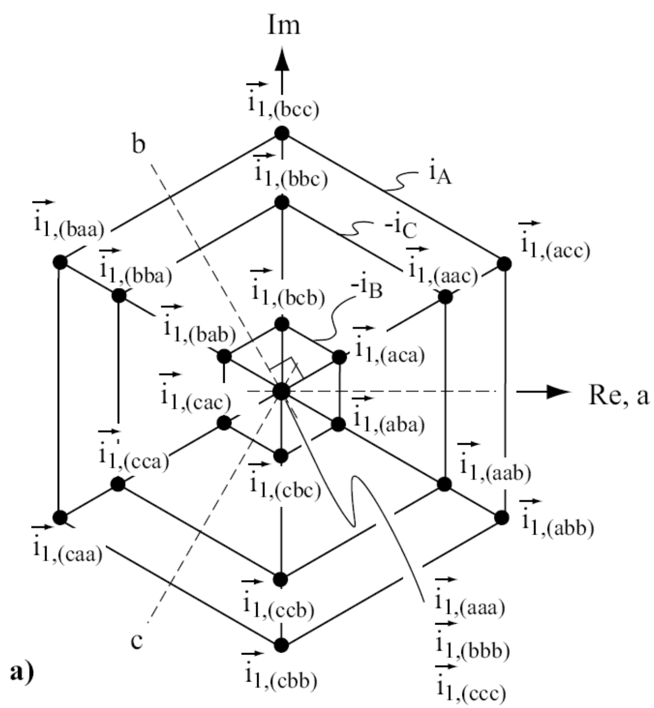
CMC Rotating Space Vectors

Positive Sequence Switching States

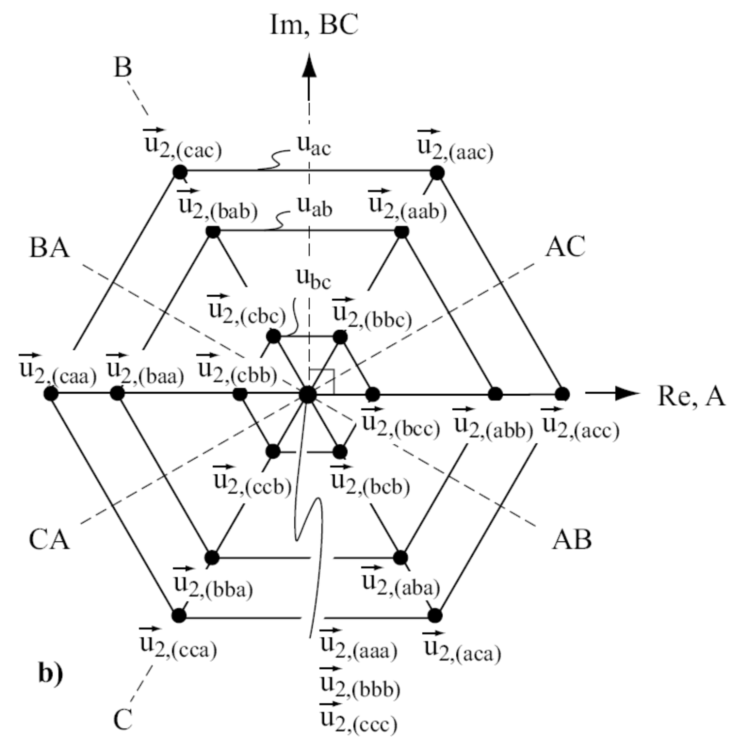


Negative Sequence Switching States

CMC Stationary Space Vectors



Input Current Space Vectors



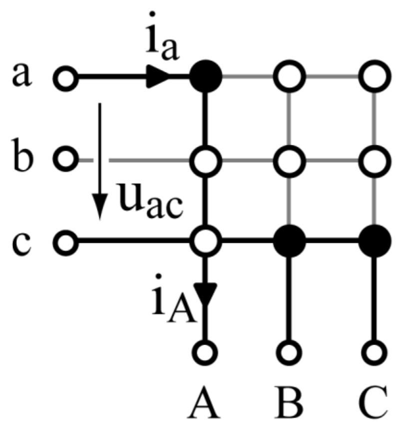
Output Voltage Space Vectors

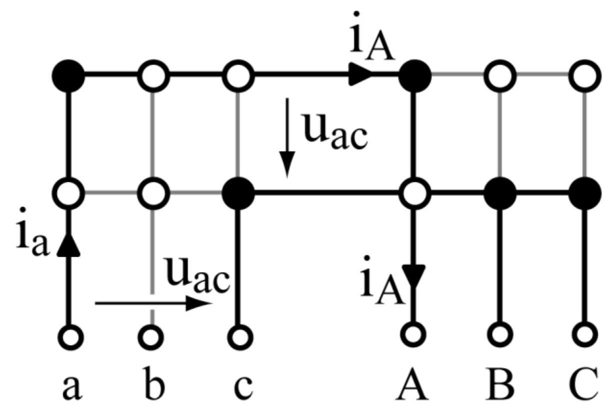
CMC/IMC Relation (1)

Correspondence of Switching States

$$\vec{u}_{2,(acc)} = \vec{u}_{2,(ac)(pnn)}$$

$$\vec{i}_{1,(acc)} = \vec{i}_{1,(ac)(pnn)}$$





▶ *Indirect Space Vector Modulation*

P. Ziogas [12]
L. Huber / D. Borojevic

CMC/IMC Relation (2)

Matrix Representation of Voltage and Current Conversion

- **CMC**

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} s_{aAa} & s_{bAb} & s_{cAc} \\ s_{aBa} & s_{bBb} & s_{cBc} \\ s_{aCa} & s_{bAb} & s_{cCc} \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix} = \underline{\underline{S}}_{CMC,U} \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \underline{\underline{S}}_{CMC,I} \begin{pmatrix} i_A \\ i_B \\ i_C \end{pmatrix}$$

$$\underline{\underline{S}}_{CMC,I} = \underline{\underline{S}}^T_{CMC,U}$$

- **IMC**

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} s_{pA} & s_{An} \\ s_{pB} & s_{Bn} \\ s_{pC} & s_{Cn} \end{pmatrix} \cdot \begin{pmatrix} u_p \\ u_n \end{pmatrix} = \underline{\underline{S}}_{WR,U} \begin{pmatrix} u_p \\ u_n \end{pmatrix}$$

$$\begin{pmatrix} u_p \\ u_n \end{pmatrix} = \begin{pmatrix} s_{apa} & s_{bpb} & s_{cpc} \\ s_{ana} & s_{bnb} & s_{cnc} \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix} = \underline{\underline{S}}_{GR,U} \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

$$\underline{\underline{S}}_{IMC,I} = \underline{\underline{S}}^T_{IMC,U}$$

CMC/IMC Relation (3)

$$\underline{\underline{S}}_{CMC,U} \equiv \underline{\underline{S}}_{IMC,U}$$

$$\underline{\underline{S}}_{IMC,U} = \underline{\underline{S}}_{WR,U}\,\underline{\underline{S}}_{GR,U} = \begin{pmatrix} s_{pA} & s_{An} \\ s_{pB} & s_{Bn} \\ s_{pC} & s_{Cn} \end{pmatrix} \cdot \begin{pmatrix} s_{apa} & s_{bpb} & s_{bpb} \\ s_{ana} & s_{bnb} & s_{cnc} \end{pmatrix}$$

$$\begin{pmatrix} s_{aAa} & s_{bAb} & s_{cAc} \\ s_{aBa} & s_{bBb} & s_{cBc} \\ s_{aCa} & s_{bCb} & s_{cCc} \end{pmatrix}$$

$$\equiv \begin{pmatrix} s_{apa}s_{pA} + s_{ana}s_{An} & s_{bpb}s_{pA} + s_{bnb}s_{An} & s_{cpc}s_{pA} + s_{cnc}s_{An} \\ s_{apa}s_{pB} + s_{ana}s_{Bn} & s_{bpb}s_{pB} + s_{bnb}s_{Bn} & s_{cpc}s_{pB} + s_{cnc}s_{Bn} \\ s_{apa}s_{pC} + s_{ana}s_{Cn} & s_{bpb}s_{pC} + s_{bnb}s_{Cn} & s_{cpc}s_{pC} + s_{cnc}s_{Cn} \end{pmatrix}$$

Example

$$\vec{u}_{2,(acc)} = \vec{u}_{2,(ac)(pnn)}$$

$$\vec{i}_{1,(acc)} = \vec{i}_{1,(ac)(pnn)}$$

$$\underline{\underline{S}}_{CMC,U} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \end{pmatrix}$$

CMC/IMC Relation (4)

$\varphi_{\vec{u}_2^*} \in [0, \pi/6]$

Correspondence of Switching States

- **IMC**

$$\cdots|_{t_\mu = 0} \quad (ac)(pnn) - (ac)(ppn) - (ac)(ppp) - (ab)(ppp) - (ab)(ppn) - (ab)(pnn)|_{t_\mu = T_P/2}$$
$$(ab)(pnn) - (ab)(ppn) - (ab)(ppp) - (ac)(ppp) - (ac)(ppn) - (ac)(pnn)|_{t_\mu = T_P} \quad \cdots$$

- **CMC**

$$\cdots|_{t_\mu = 0} \quad (acc) - (aac) - (aaa) - (aaa) - (aab) - (abb)|_{t_\mu = T_P/2}$$
$$(abb) - (aab) - (aaa) - (aaa) - (aac) - (acc)|_{t_\mu = T_P} \quad \cdots$$

$\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$

- **IMC**

$$\cdots|_{t_\mu = 0} \quad (ac)(ppn) - (ac)(pnn) - (ac)(nnn) - (ab)(nnn) - (ab)(pnn) - (ab)(ppn)|_{t_\mu = T_P/2}$$
$$(ab)(ppn) - (ab)(pnn) - (ab)(nnn) - (ac)(nnn) - (ac)(pnn) - (ac)(ppn)|_{t_\mu = T_P} \quad \cdots$$

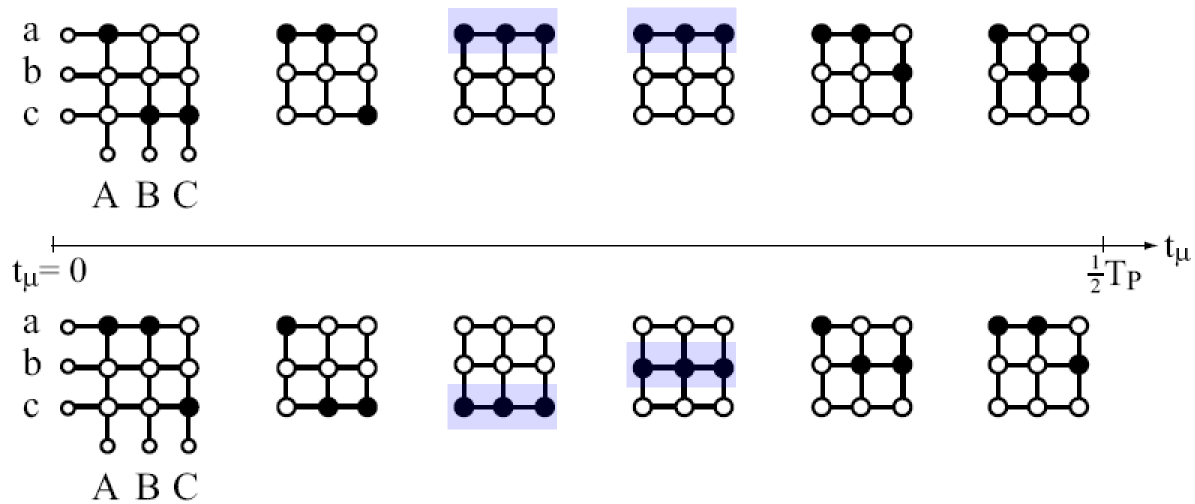
- **CMC**

$$\cdots|_{t_\mu = 0} \quad (aac) - (acc) - (ccc) - (bbb) - (abb) - (aab)|_{t_\mu = T_P/2}$$
$$(aab) - (abb) - (bbb) - (ccc) - (acc) - (aac)|_{t_\mu = T_P} \quad \cdots$$

CMC/IMC Relation (5)

$\varphi_{\vec{u}_2^*} \in [0, \pi/6]$

$\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$



$\varphi_{\vec{u}_2^*} \in [0, \pi/3]$

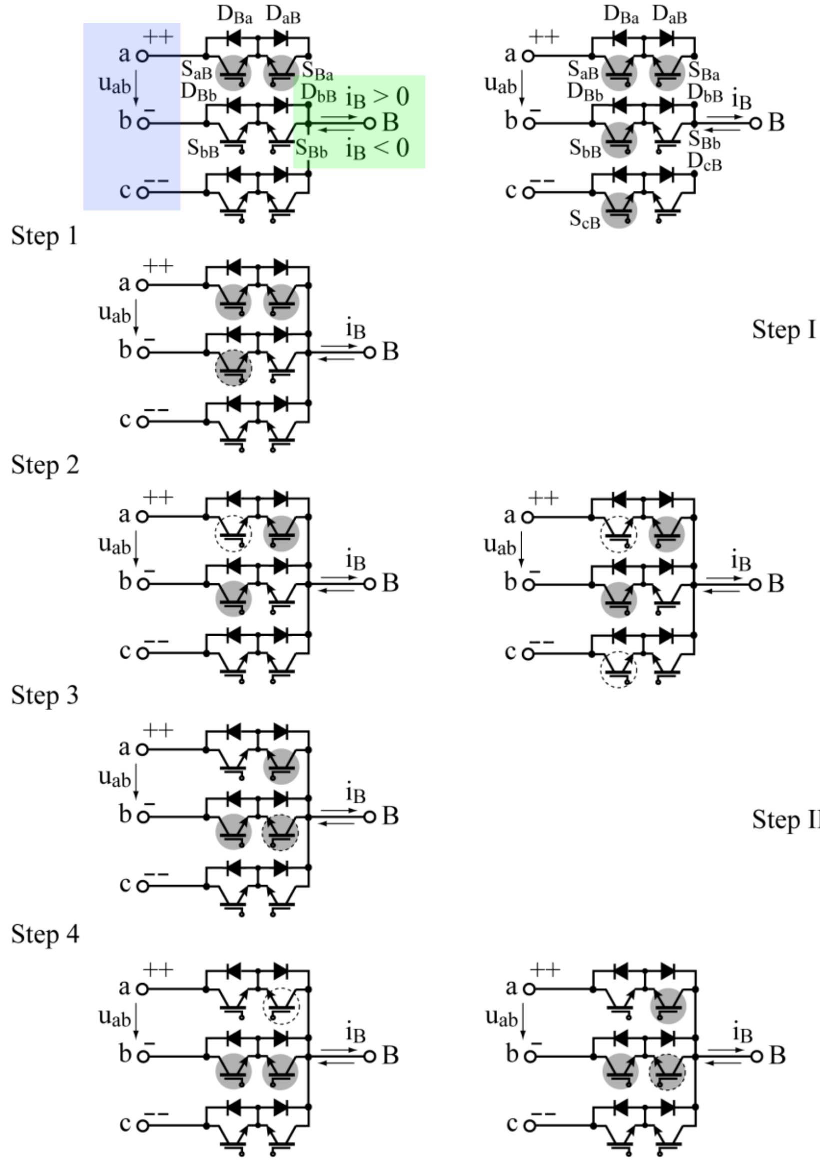
$$\ldots|_{t_\mu = 0} \quad (acc) - (aac) - (aaa) - (aaa) - (aab) - (abb)|_{t_\mu = T_P/2}$$

$$(abb) - (aab) - (aaa) - (aaa) - (aac) - (acc)|_{t_\mu = T_P} \quad \ldots$$

CMC Multi-Step Commutation

J. Oyama / T. Lipo
N. Burany
P. Wheeler
W. Hofmann

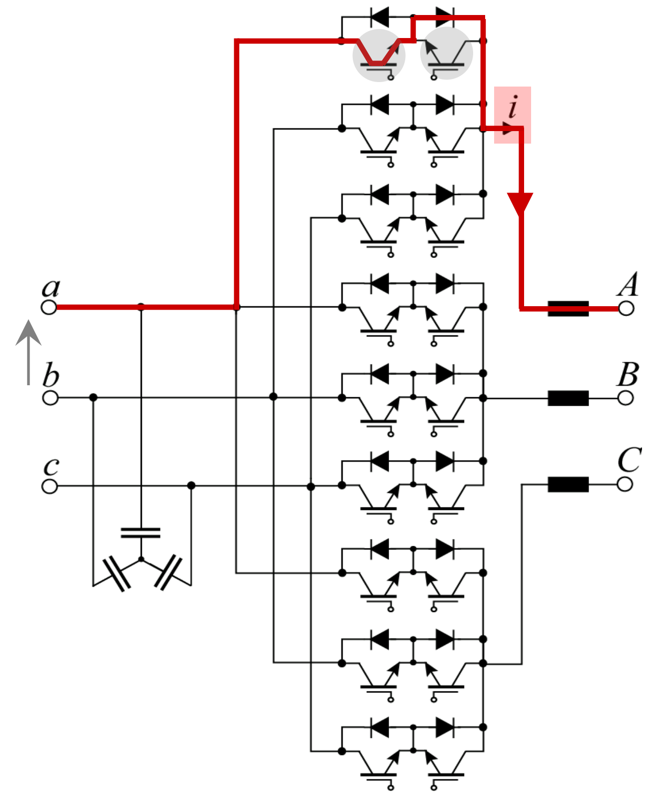
Example: *u*-Dependent Commutation



- ▶ *Four-Step Commutation*
- ▶ *Two-Step Commutation*

4-Step Commutation of CMC (1)

Example: *i*-Dependent Commutation

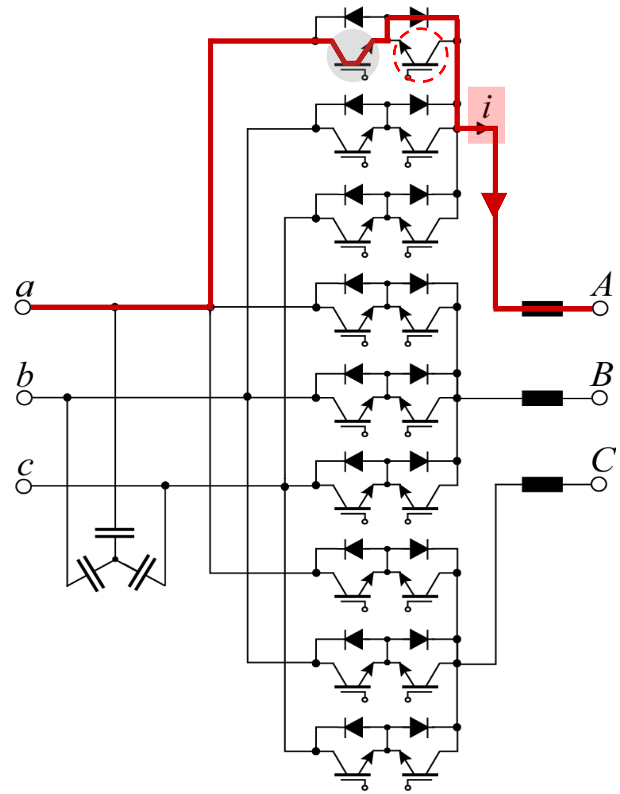


- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (2)

1st Step: Off



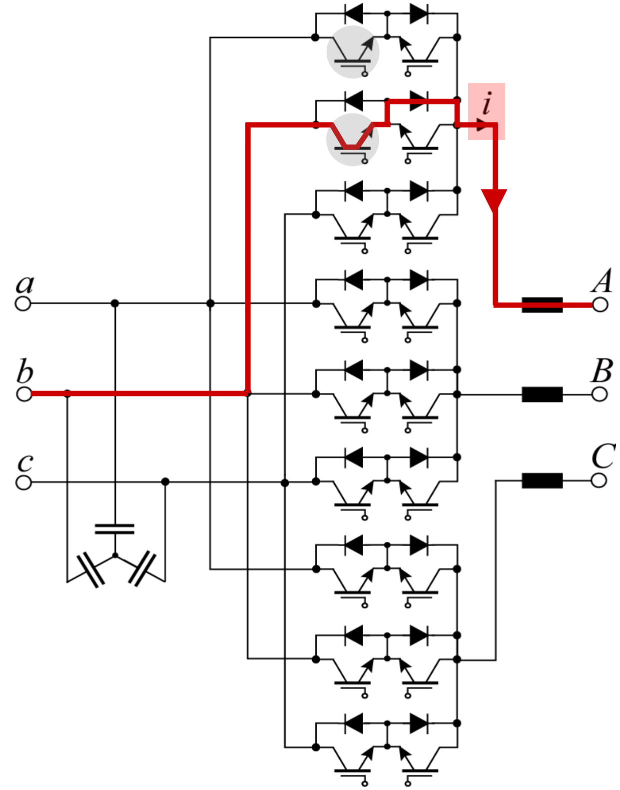
Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (3)

1st Step: Off
2nd Step: On



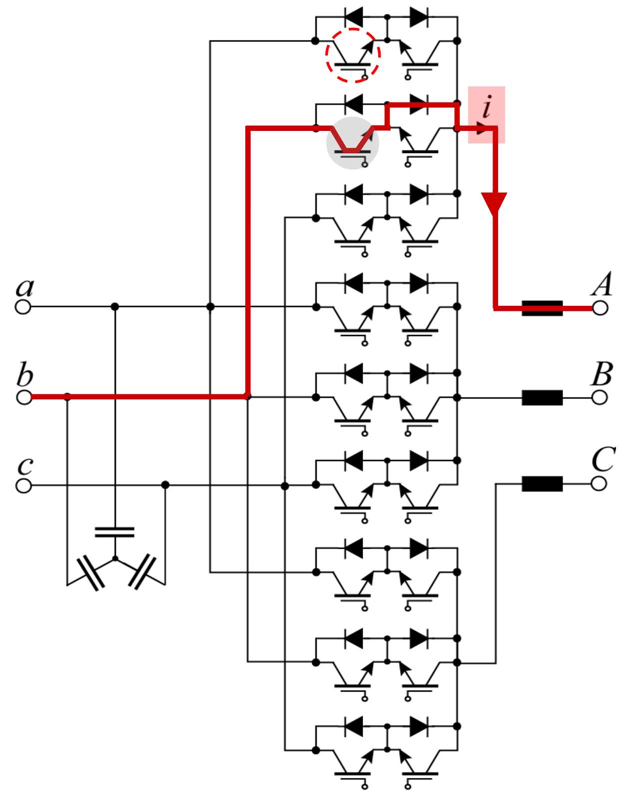
Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (4)

1st Step: Off
2nd Step: On
3rd Step: Off



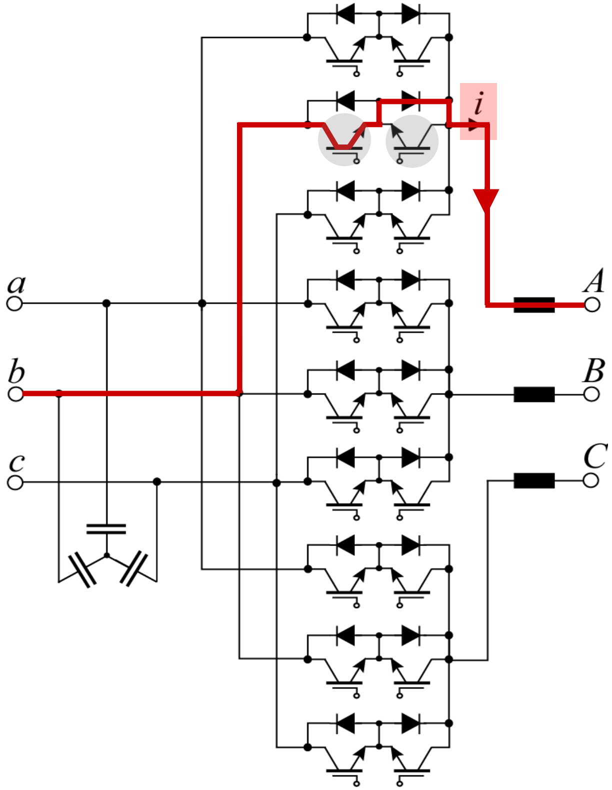
Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (5)

1st Step: Off
2nd Step: On
3rd Step: Off
4th Step: On



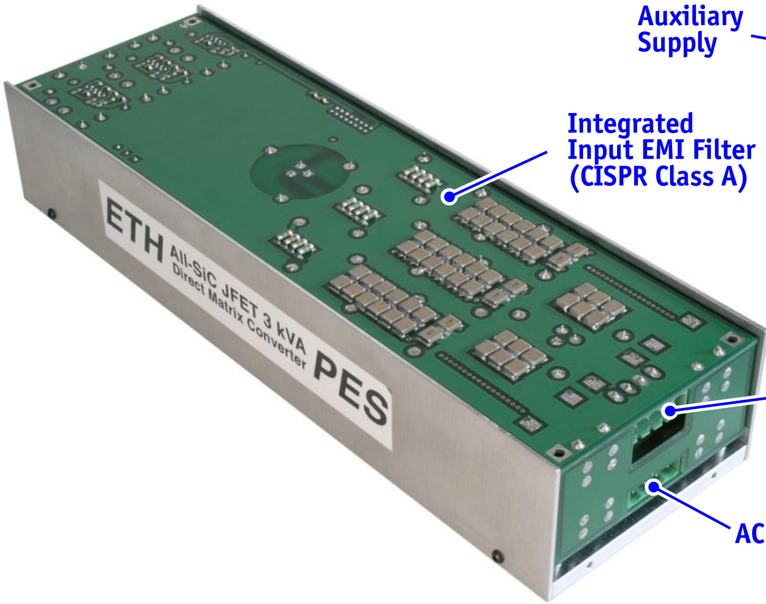
Sequence Depends on Direction of Output Current !

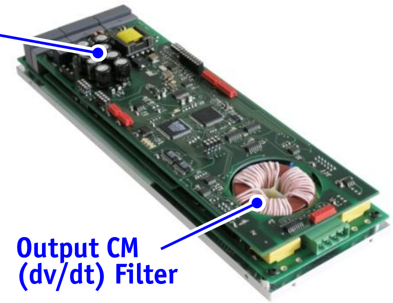
Constraints

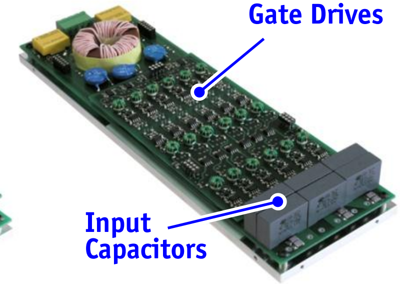
- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

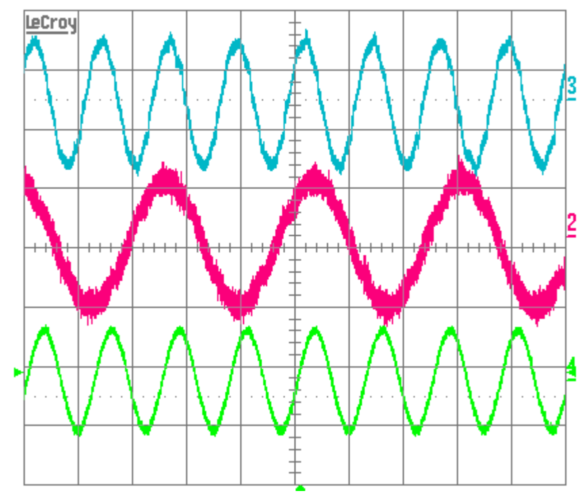
All-SiC JFET Conventional direct Matrix Converter







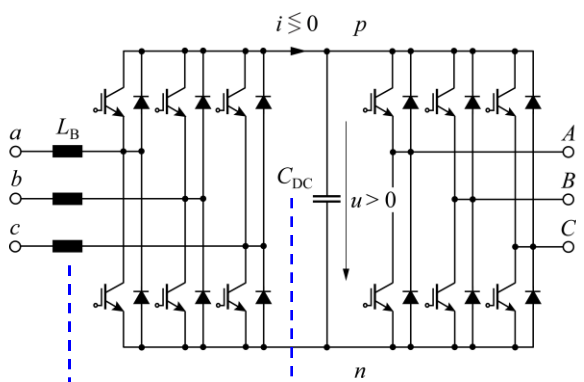
Measurements @ U_{in}= 115 V RMS, 400 Hz



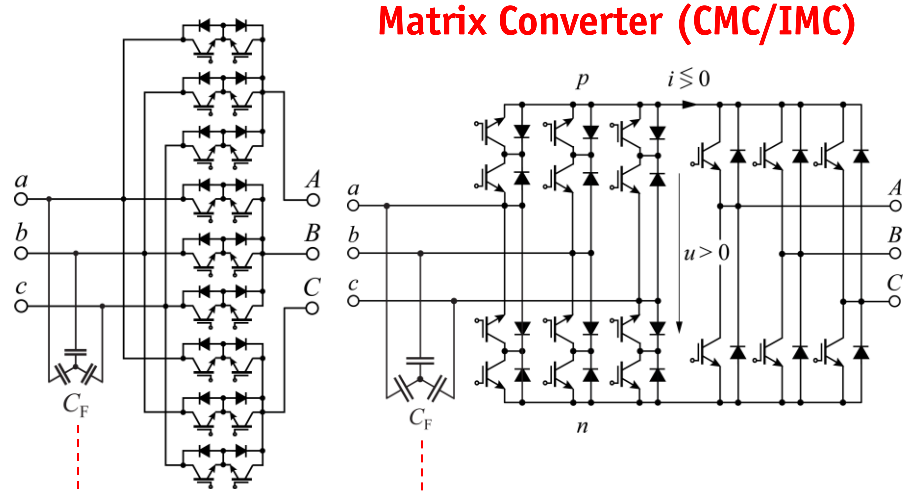
- P_{out} = 3 kVA, η = 93.1% (at 200 kHz)
- $f_{S,nom}$= 144 kHz ($f_{S,design}$= 200 kHz)
- 3 kVA/dm³ (50W/in³) with 1200 V/6 A SiC JFET
- ≈ 8 kVA/dm³ (135W/in³) with 1200 V/ 20 A SiC JFET
- 273 x 82 x 47mm³ = 1.05 dm³ (64 in³)

Control Properties of AC-AC Converters (1)

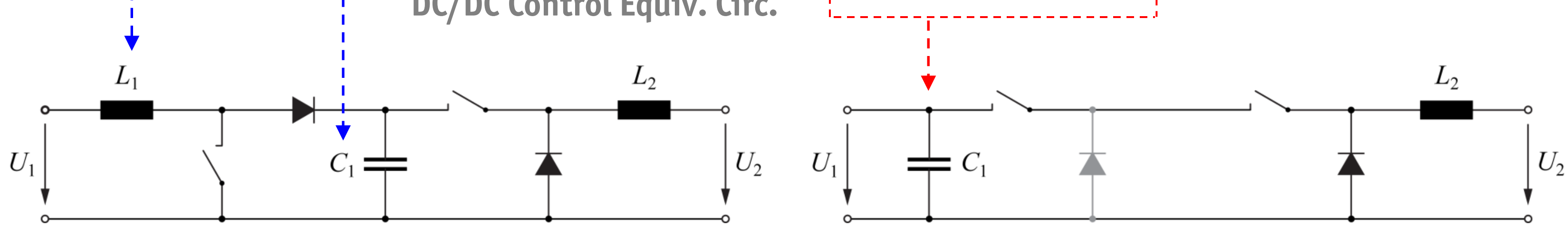
Voltage DC-Link B2B Conv. (V-BBC)



Matrix Converter (CMC/IMC)



DC/DC Control Equiv. Circ.



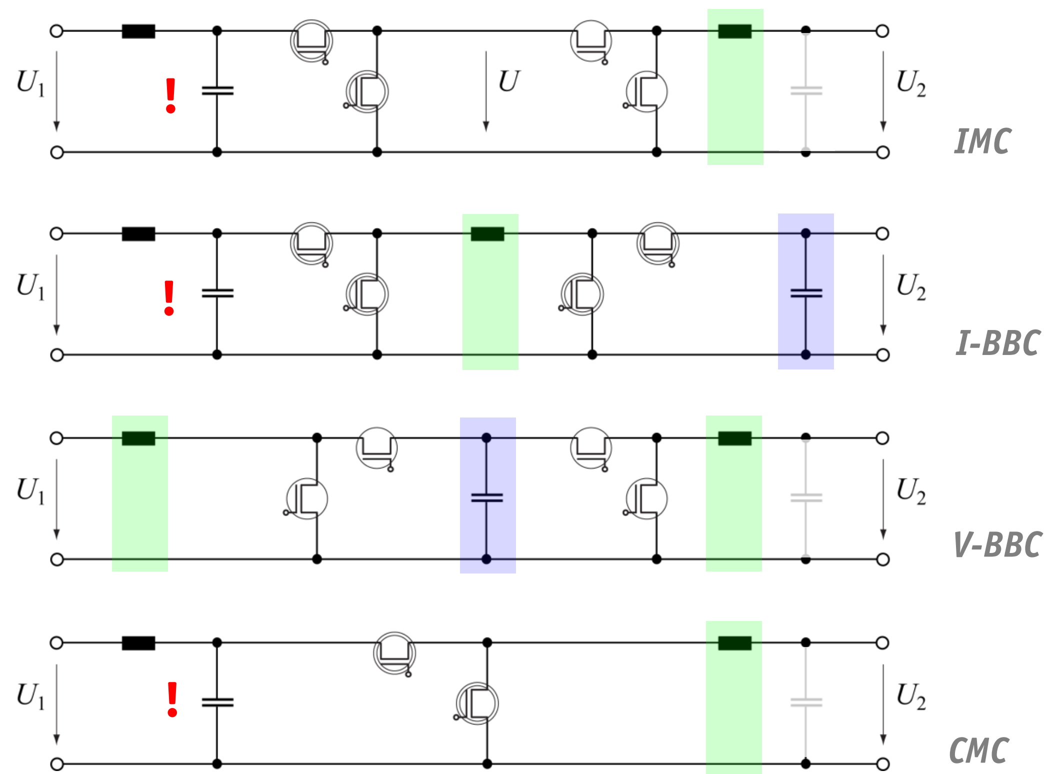
- ▶ **Boost-Buck-Type Converter**
- ▶ **Max. Output Voltage can be Maintained during Low Mains Condition**

- ▶ **Buck-Type Converter**
- ▶ **Maximum Output Voltage is Limited by Actual Input Voltage** $\hat{U}_2 = 0.866 \cdot \hat{U}_1$

Control Properties of AC-AC Converters (2)

DC-DC Equivalent Circuits

! ***Uncontrolled Input Filter***



Control Properties of AC-AC Converters (3)

■ Voltage DC-Link B2B Converter (V-BBC)

- ▶ Input Current (in Phase with Input Voltage)
- ▶ DC-Link Voltage

} 2 Cascaded Control Loops

- ▶ Output Current (Torque and Speed of the Motor)

} 2 Cascaded Control loops

■ Matrix Converter (CMC / IMC)

- ▶ Output Current (Torque and Speed of the Motor)

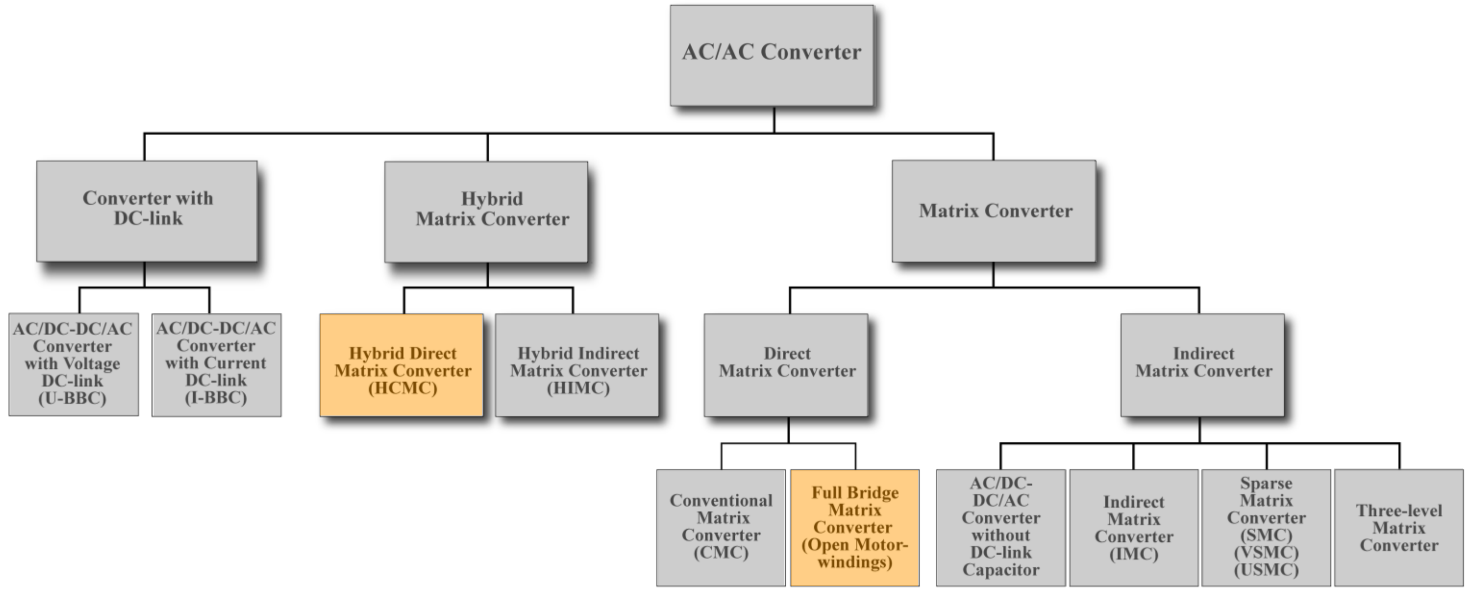
} 2 Cascaded Control Loops

- ▶ Optional: Input Current (Formation of Input Current still Depends on the Impressed Output Current)

CMC - Extensions

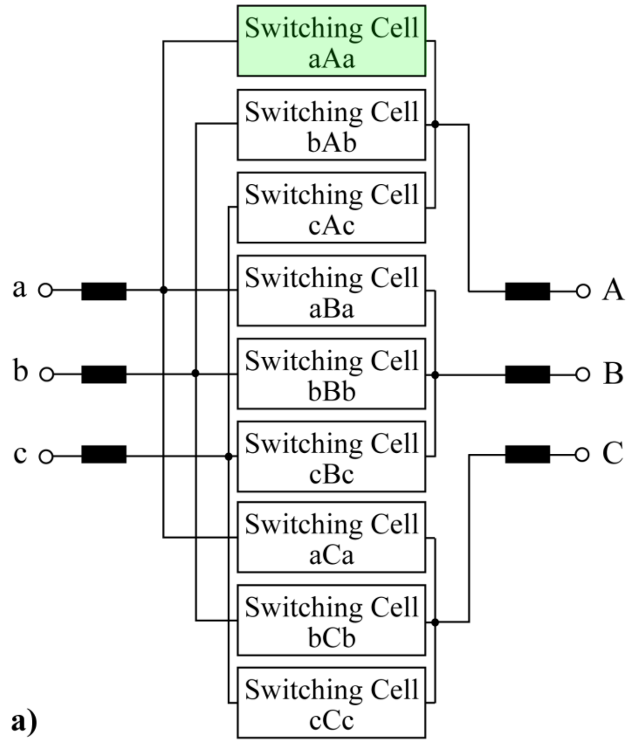
Multi-Level
Full-Bridge

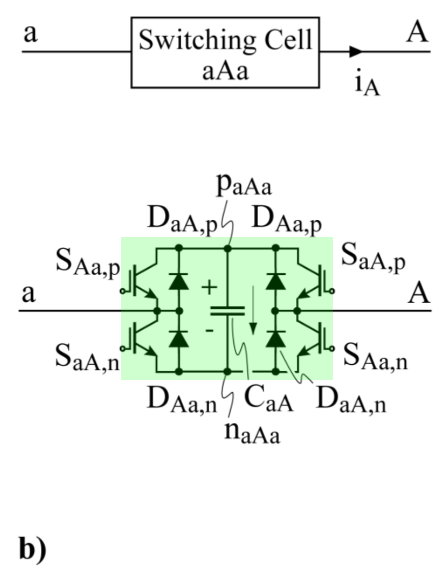
Classification of Three-Phase AC-AC Converters



- *Hybrid CMC*
- *Full-Bridge CMC*

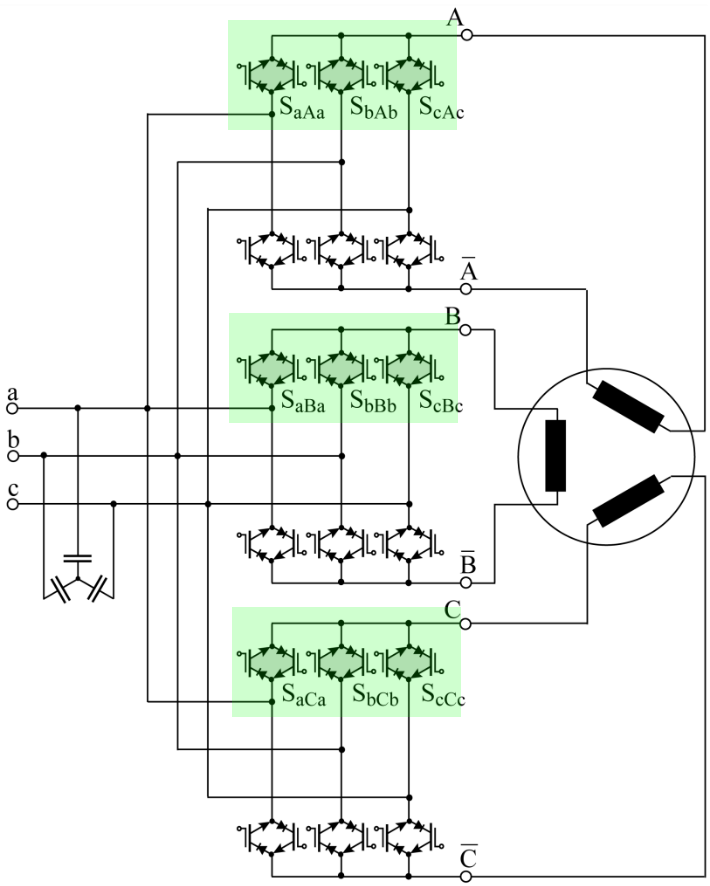
Hybrid CMC

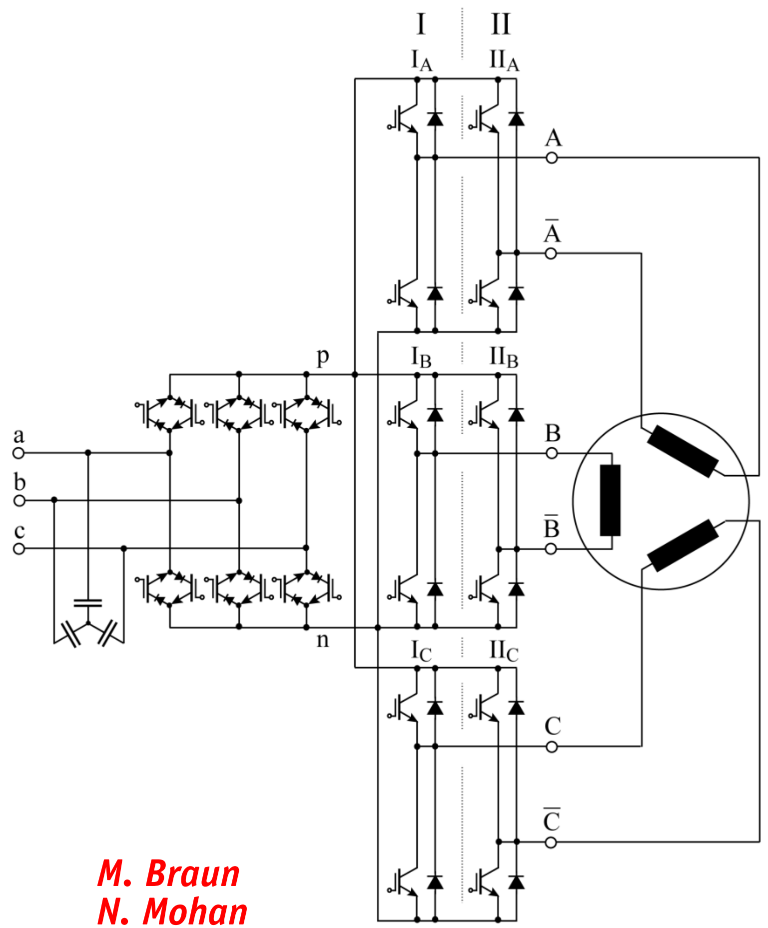




B. Erickson

Full-Bridge CMC / IMC





M. Braun
N. Mohan

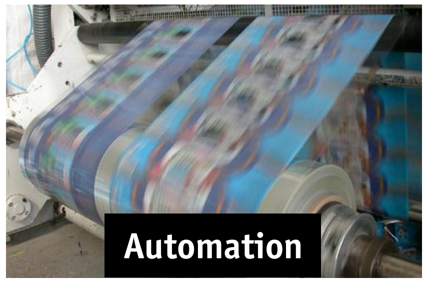
Coffee Break !

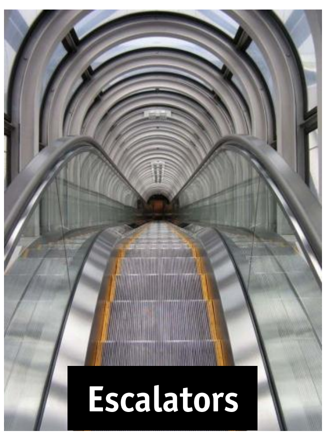
Comparative Evaluation

DC Link Converters
Matrix Converters

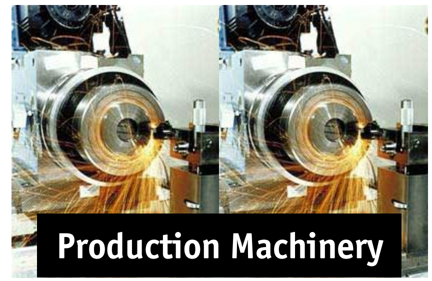
Application Areas of Three-Phase PWM Converters

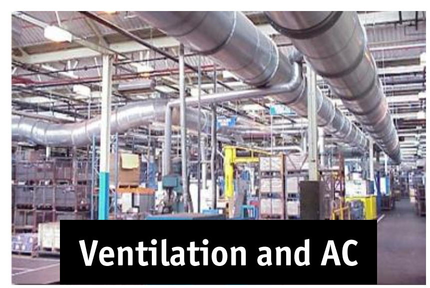
Bidirectional Power Flow





Unidirectional Power Flow



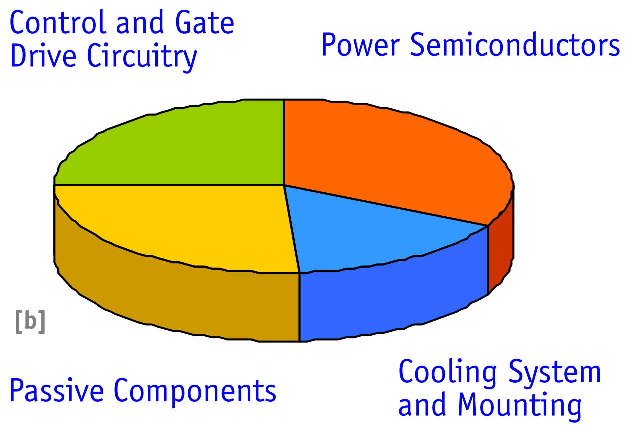


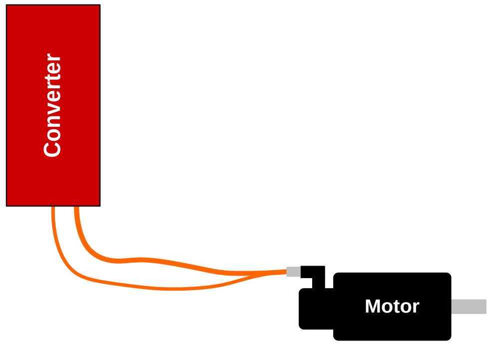
60% of Worldwide Ind. Energy Used by Electric Motor Drives! [a]

[a] "Study on Worldwide Energy Consumption", ECPE Workshop, 2008

Motivation

▶ Cost Allocation of VFD Converters





▶ Status Quo ⇒ Motivation

- **Holistic Converter System Comparisons are (still) Rarely Found**
- **Comprehensive Comparisons Involves a Multi-Domain Converter Design**
- **Voltage-Source-Type Converter Topologies are Widely Used**

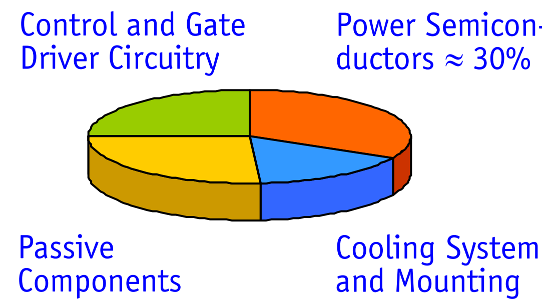
▶ Focus of the Investigation

- **Bidirectional Three-Phase AC/DC/AC and AC/AC Converters**
- **Low Voltage Drives**
- **Power Level from 1 kVA to few 10 kVA**

[b]: Based on “ECPE Roadmap on Power Electronics, 2008”

Comparative Evaluation – Virtual Converter Evaluation Platform

- **Define Application / Mission Profile**
  - ***M-n* Operating Rage (Continuous / Overload Requirement)**
  - **Torque at Standstill**
  - **Motor Type**
  - **etc.**



- **Compare Required Total Silicon Area (e.g. for $T_J < 150°C$, $T_C = 95°C$)**
  - **Guarantee Optimal Partitioning of Si Area between IGBTs and Diodes**

- **Semiconductor Type, Data**
- **Thermal Properties**
- **EMI Specifications**
- **Converter Type, Motor Type (Losses)**
- **Modulation Scheme**
- **etc.**

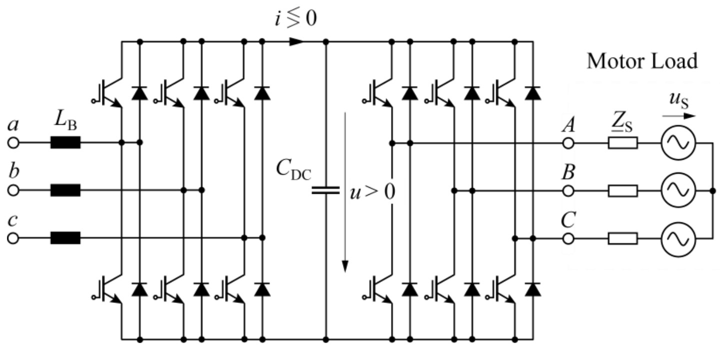
Inputs:
- ***M-n* Operating Range**
- Mission Profile
- etc.

Virtual Converter Evaluation Platform

Outputs:
- **Total Si Area – Figure-Of-Merit**
- **Operating Efficiency**
- Average Mission Efficiency
- Total Mission Energy Losses
- EMI Filter Volume
- Costs

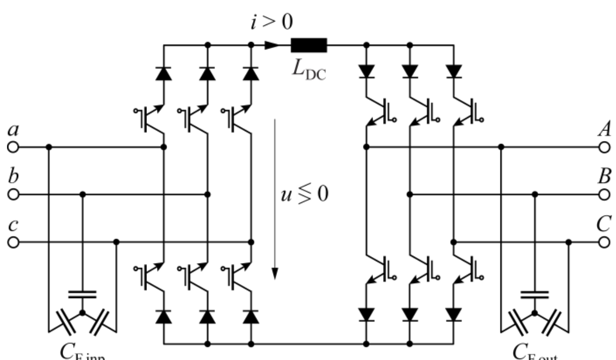
Considered Converter Topologies – V-BBC, I-BBC, IMC, and CMC

With Intermediate Energy Storage



VSR (Boost) VSI (Buck)

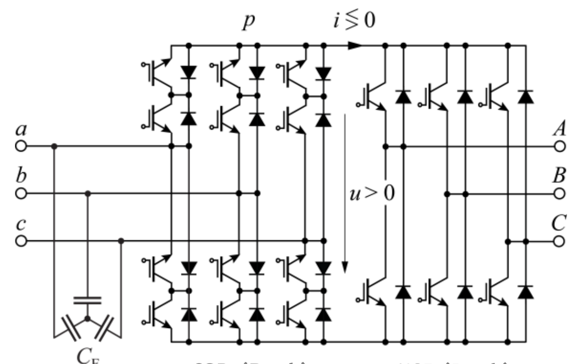
Voltage Source Back-to-Back Converter (V-BBC)
"State-of-the-Art" Converter System



CSR (Buck) CSI (Boost)

Current Source Back-to-Back Converter (I-BBC)

Without Intermediate Energy Storage

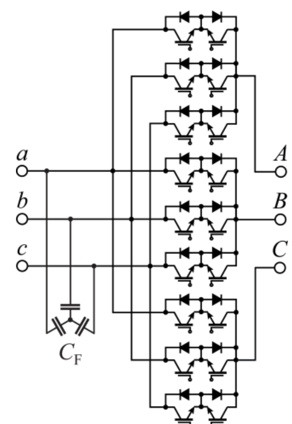


CSR (Buck) VSI (Buck)

$U_{2,max} = 0.866\ U_1$

Indirect Matrix Converter (IMC)

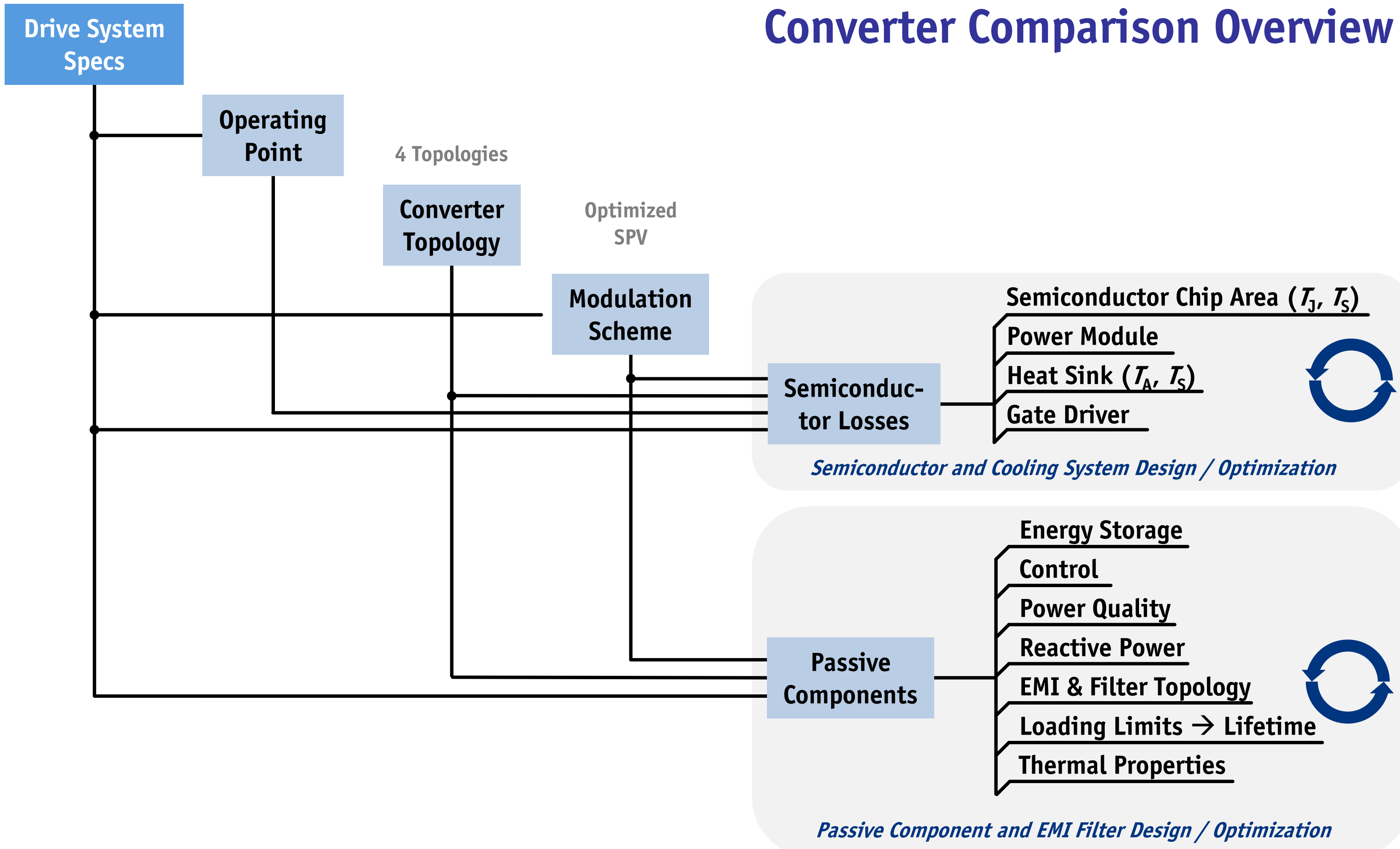
$U_{2,max} = 0.866\ U_1$



(Buck)

Conventional (Direct) Matrix Converter (CMC)

Converter Comparison Overview



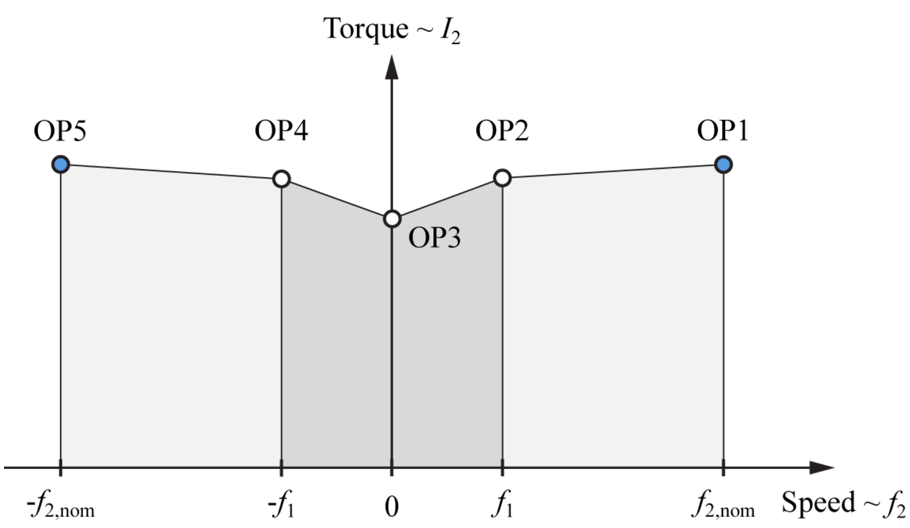
Comparative Evaluation (1) – Specifications and Operating Points

Main Converter Specifications

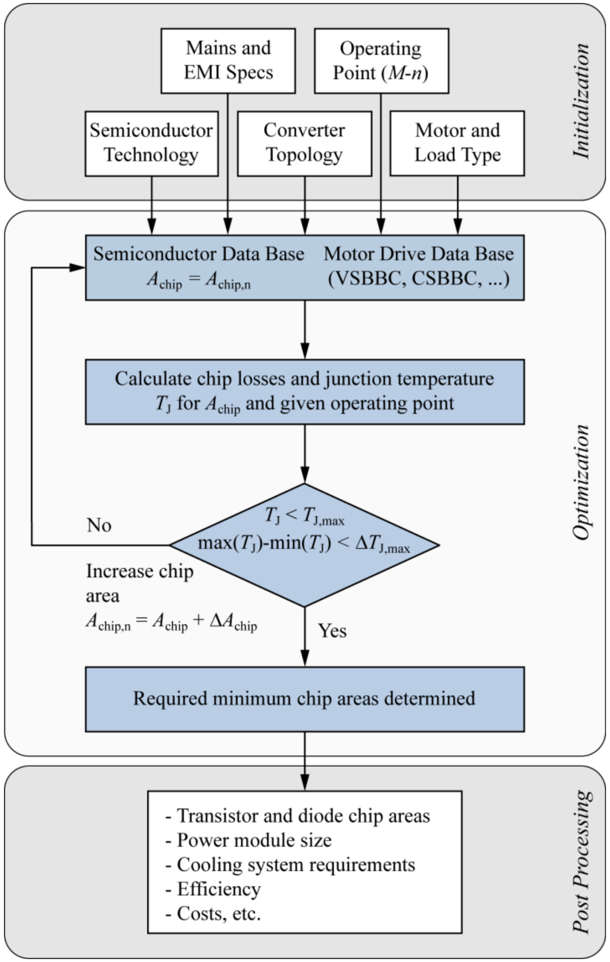
- 3 x 400 V / 50 Hz, 15 kVA
  f_{sw} = [8 ... 72] kHz
  U_{DC} = 700 V (VSBBC)
- PMSM, Matched to Converter
  (L_S in mH range, $\Phi_2 \approx 0°$)
- EMI Standard, CISPR 11
  QP Class B (66 dB at 150 kHz)
- Ambient Temperature T_A = 50°C
  Sink Temperature T_S = 95°C
  Max. Junction Temperature $T_{J,max}$ =150°C
  (for T_A = 20°C $\Rightarrow$ T_S = 65°C, $T_{J,max}$ = 20°C)

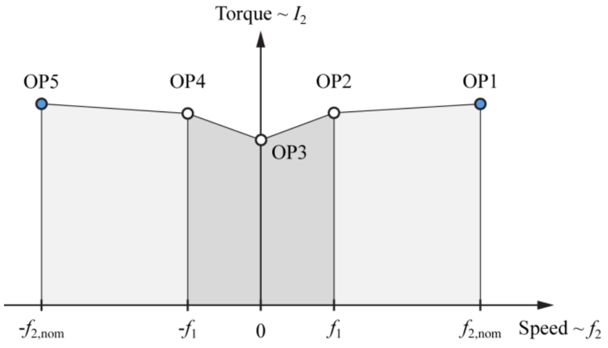
Torque Speed Plane

OP1/OP5 Nominal Motor/Generator Operation (90% $U_{2,max}$)
OP2/OP4 Motor/Generator Operation for $f_2 = f_1$
OP3 Motor Operation at Stand-still $f_2 = 0$

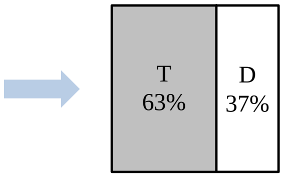


Comparative Evaluation (2) – Semicond. Area Based Comparison





▶ **Minimum Chip Area Required to Fulfill the Junction Temperature Limit $T_{J,max}$ (150°C)**



ETH Zurich [49]

Semiconductor and Cooling System Modeling

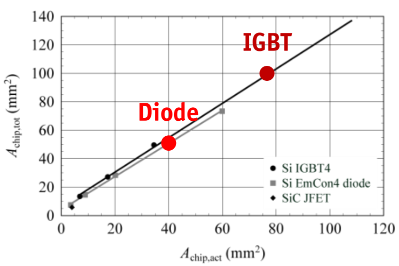
Semiconductor Database

- 1200 V Si IGBT4 and EmCon4 Diodes (Infineon)
- 1200 V normally-on SiC JFET (SiCED)

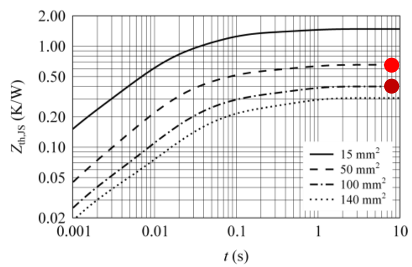
Component Level

System Level

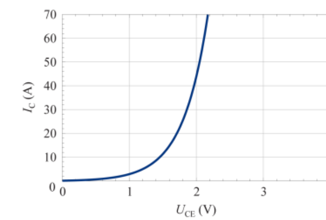
Scaling of Chip Area

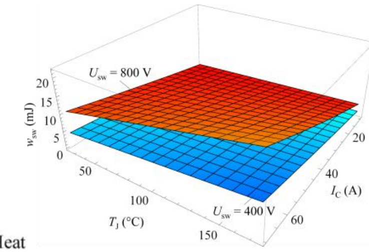


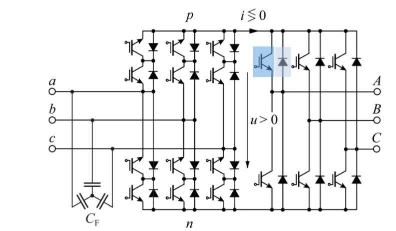
Transient Thermal Impedance

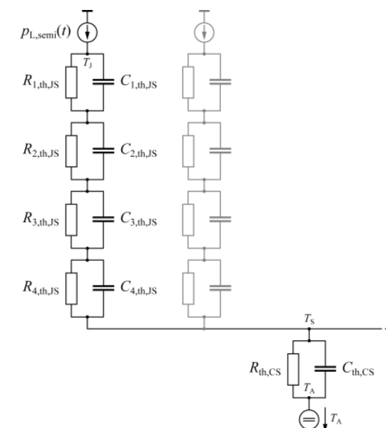


Losses as $f(A_{chip}, I, U, \text{and } T_J)$

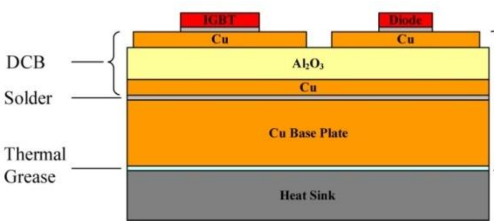


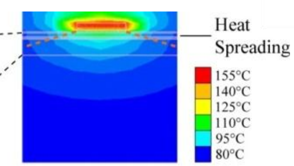




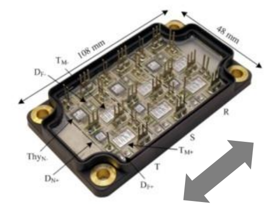


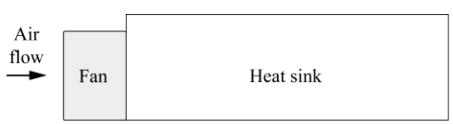
Cooling Performance

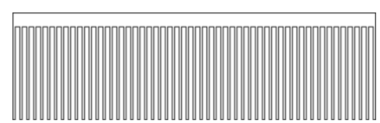




Simulation with
ICEPAK and GECKO

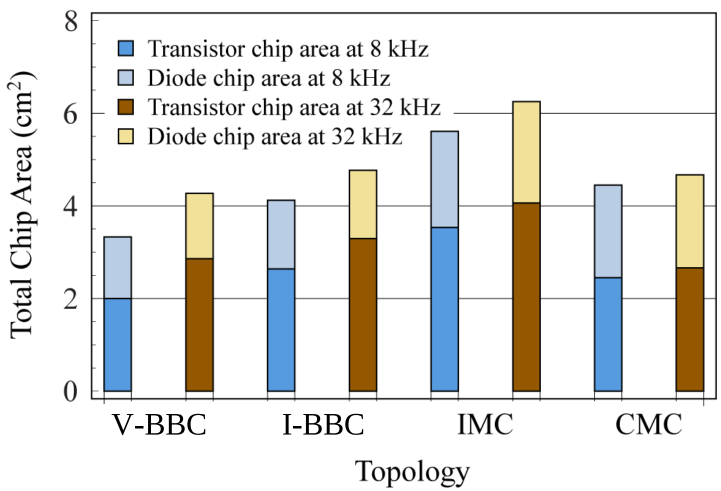




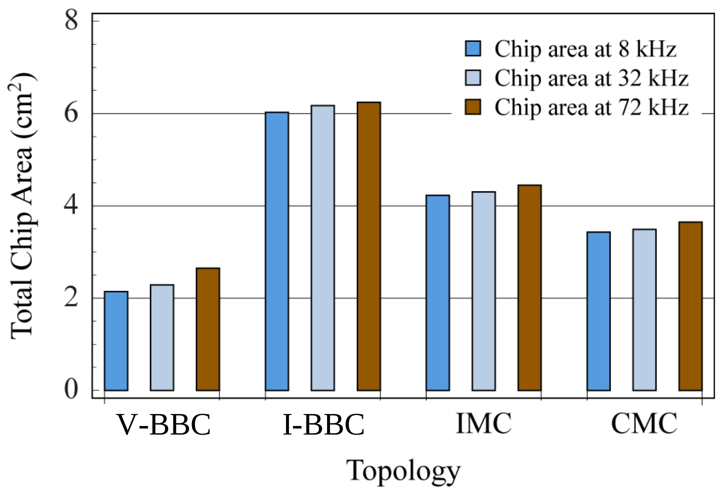


Comp. Evaluation (3) – Semiconductor Chip Areas (OP1 & OP5)

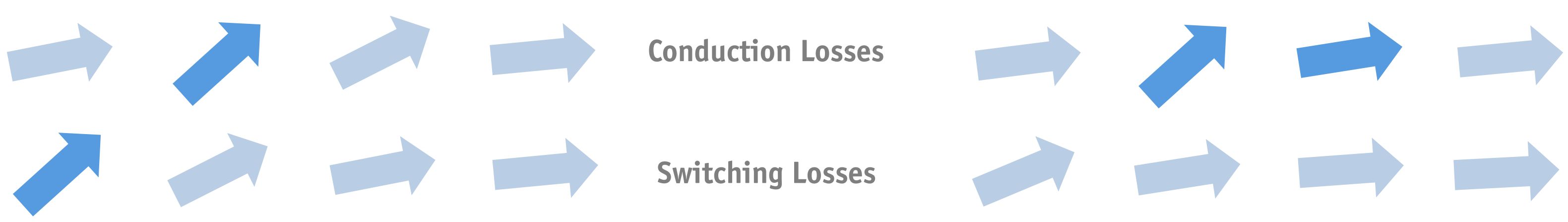
1200 V Si IGBT4 and EmCon4 Diodes



1200 V Normally-On SiC JFETs (SiCED)



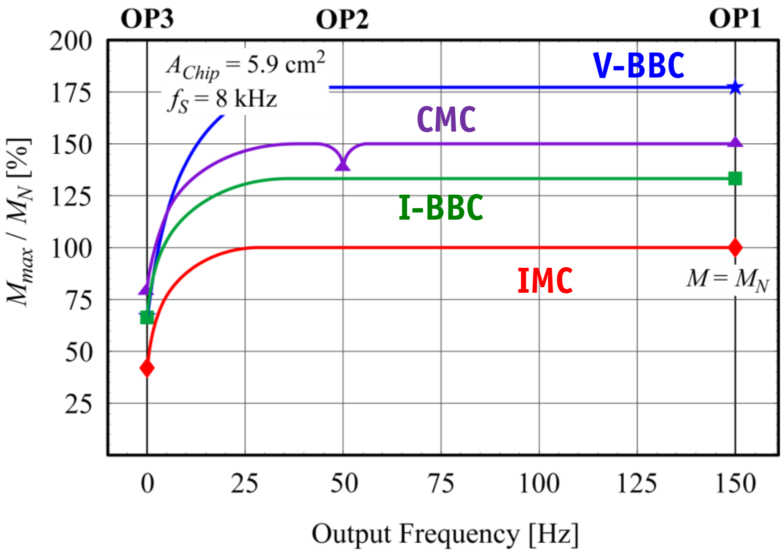
Resulting Sensitivities



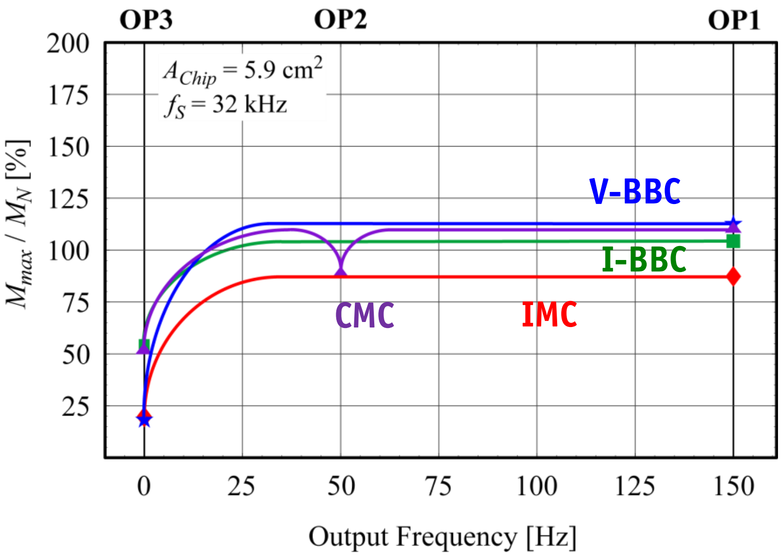
Comparative Evaluation (4) – Torque Envelope for Equal A_{chip}

► For OP1 (P_{2N} = 15 kVA) and OP3 (Stand-Still)

8 kHz: $A_{Chip} \approx 6\ cm^2$, Referenced to IMC



32 kHz: Available Chip Area $A_{Chip} \approx 6\ cm^2$



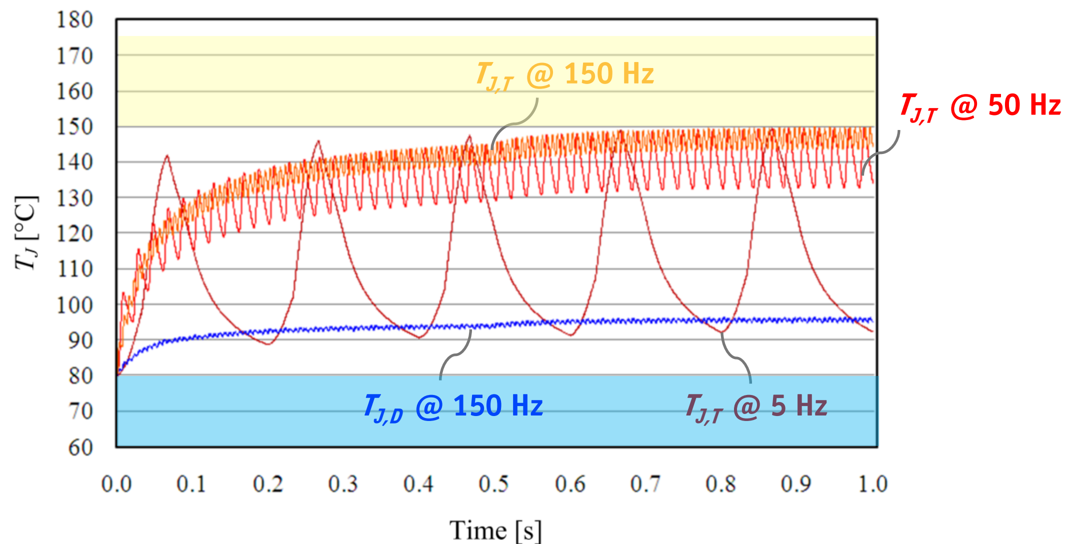
Note: Design at Thermal Limit – A More Conservative Design would be Applied for a Product!

Verification by Electro-Thermal Simulation Shown for IMC

Junction Temperatures OP1

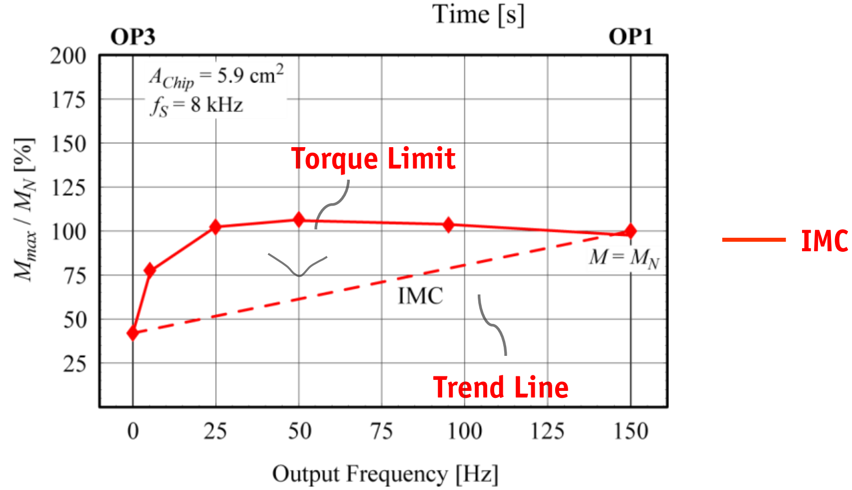
- Suggested Algorithm to Optimally Select the Semiconductor Chip Area Matches well at OP1 and OP3

Evaluated for OP1 @ 8 kHz



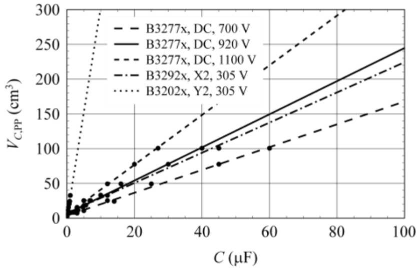
Torque at OP1 and OP3

- Suggested Algorithm allows for Accurate Torque Estimation at OP1 and OP3
- Torque Limit Line Requires a Thermal Impedance Model of the Module (R-C Network)

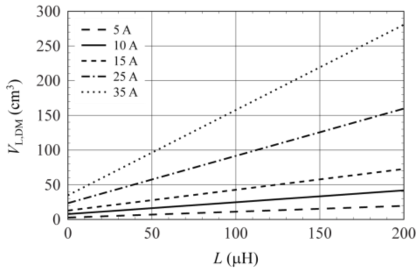


Passive Component and EMI Input Filter Modeling

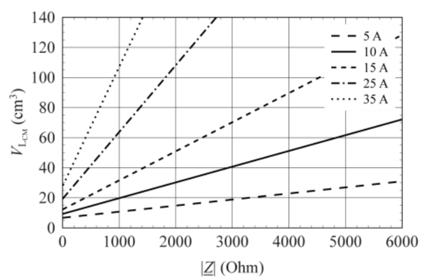
Component Level

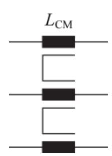


$I_{C,rms,max}$
$\mathrm{d}u/\mathrm{d}t\,|_{max}$
T_{op} = 70°C
MTTF data



$\Delta L_{0,Imax}$
$T_{op,max}$ = 100°C

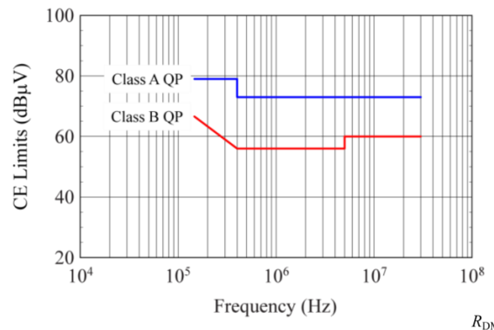




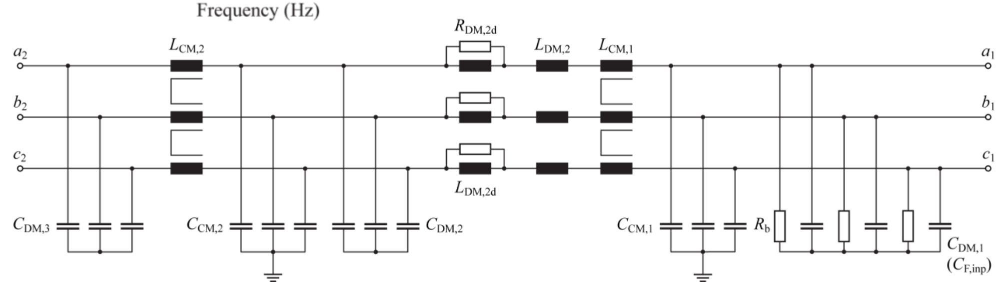
$T_{op,max}$ = 100°C

System Level

EMI Input Filter Topology



- CISPR 11 (Compliant to IEC/EN) EMI Standard for CE
- Filter Design Margin
  DM Design Margin: **6 dB**
  CM Design Margin: **8-10 dB**

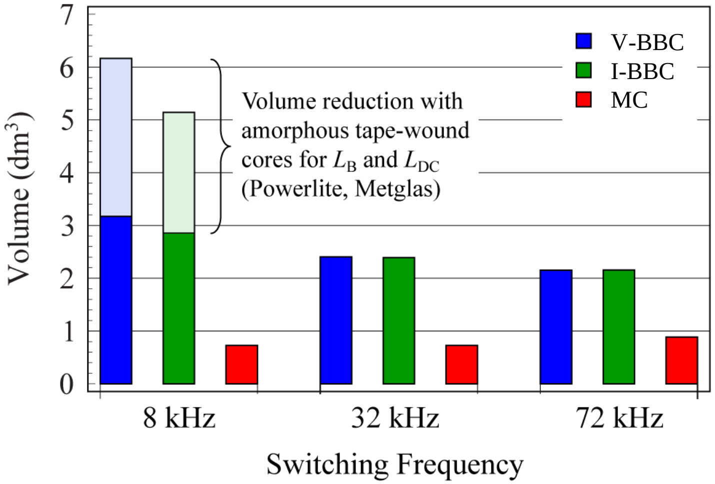


Design Criteria and Constraints

- Ripple-Based ($C_{F,inp}$, $C_{F,out}$, L_B)
- Reactive Power ($C_{F,inp}$)
- Control-Based (C_{DC}, L_{DC})
- Energy-Based (C_{DC}, L_{DC})

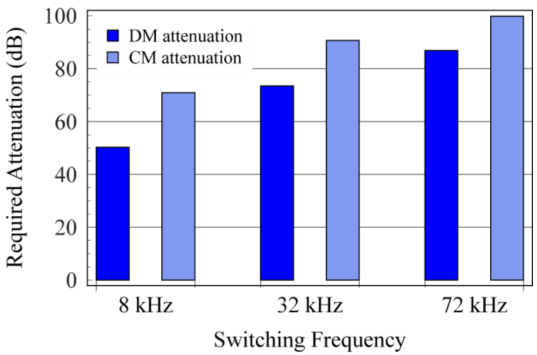
Comparative Evaluation (5) – Attenuation, Volume of Passives

Volume of Passive Components

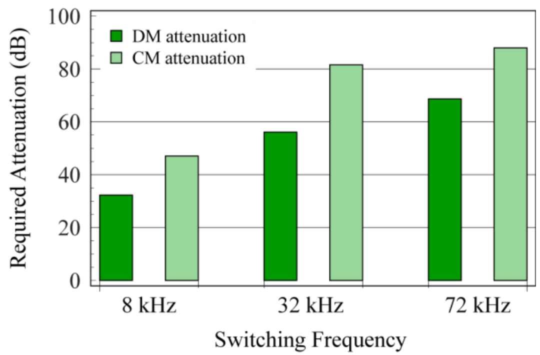


- V-BBC Requ. 15 dB More Atten.

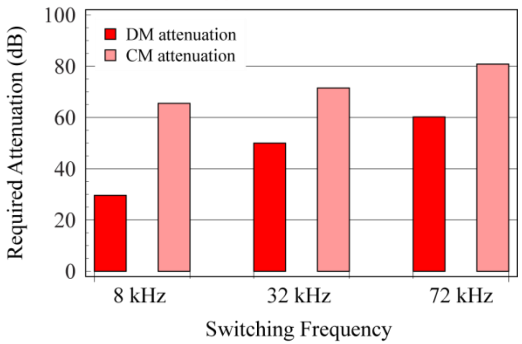
V-BBC



I-BBC

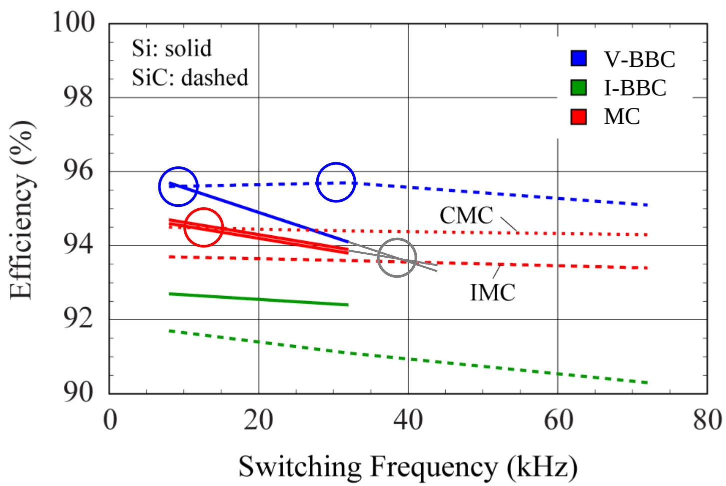


MC (IMC/CMC)

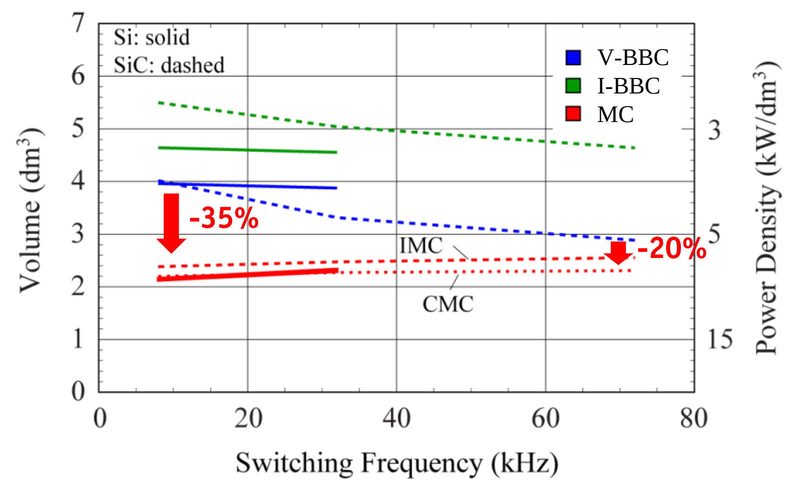


Comparative Evaluation (6) – Total Efficiency and Volume

Efficiency vs. Switching Frequency



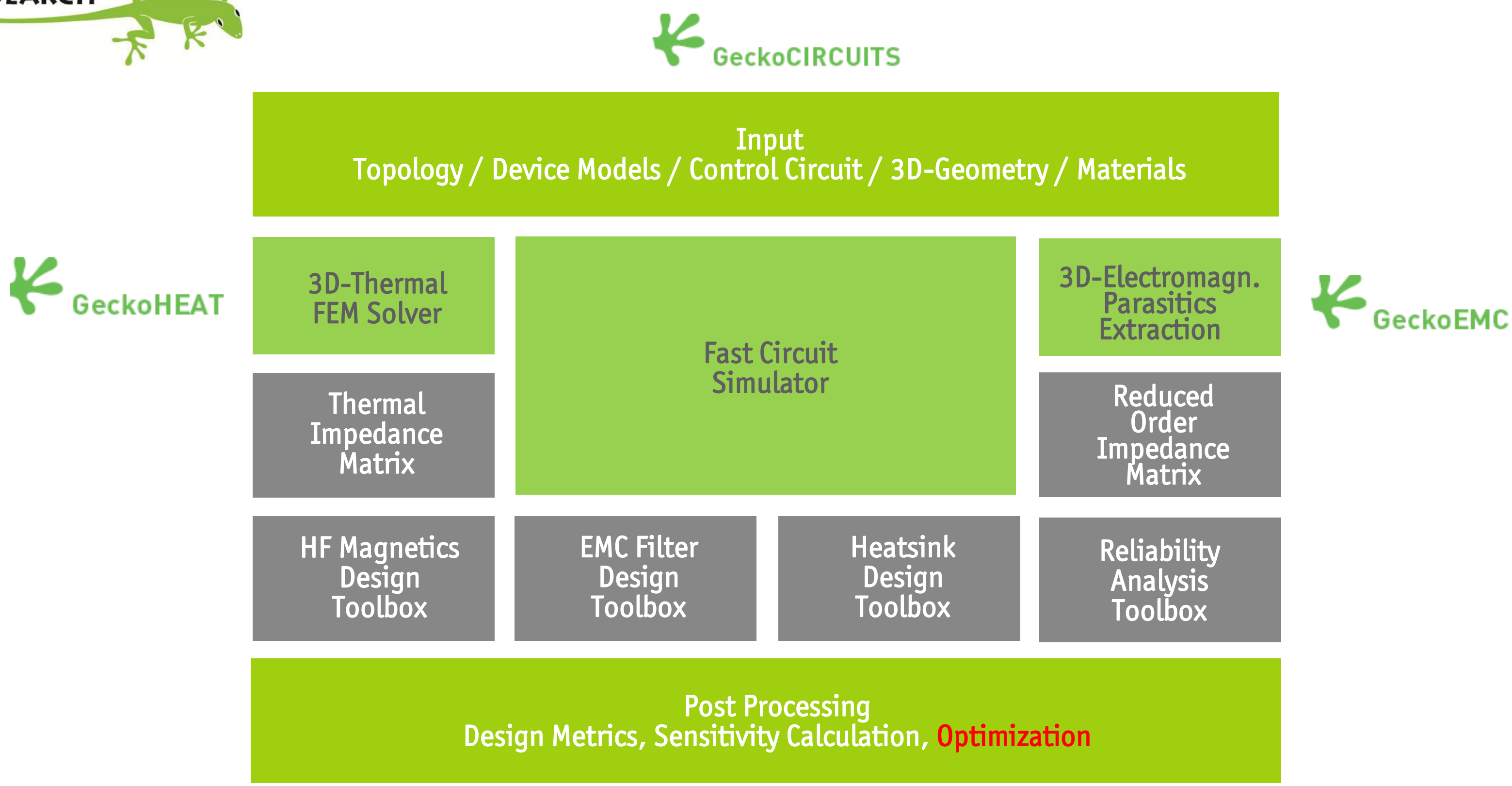
Volume vs. Switching Frequency



- ▶ V-BBC: Local Optimum at 35 kHz for SiC JFETs
- ▶ MC: Significant Volume Reduction

GECKO RESEARCH

Multi-Domain Simulation Software

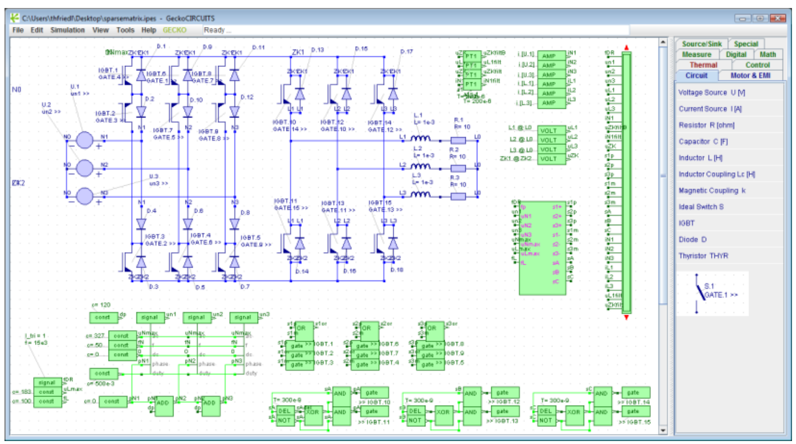


Device & Material Database
Control Toolbox
Optimization Toolbox

Overview of Gecko-Software Demonstration

- ***Gecko-CIRCUITs: Basic Functionality***

- ***Indirect Matrix Converter (IMC)***
  - *IMC Simulation with Controlled AC Machine*
  - *Specify Semiconductor Characteristics*
  - *Simulate Semiconductor Junction Temperature*
  - *etc.*



- ***Gecko EMC: Basic Functionality***

Further Information Regarding Gecko-Research

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Power Electronics Simulation - Gecko Research

- Specialized Software to meet demands of Power Electronics Engineers
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- Three tools working together: GeckoCICUITS, GeckoEMC, GeckoHEAT
- Multi-Domain approach and Optimization
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Power Electronic Converter Optimization

Let's assume you want to build a single-phase PFC rectifier with 230V input voltage, 400V output voltage and 3.2kW output power. You can optimize this rectifier for highest efficiency or for highest power density or for minimum cost or ...

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Gecko-Research Application Notes (1)

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AC/AC-Conversion for Highly Compact Drives - What Options Do I Have?

For operating a Permanent Magnet Synchronous Machine (PMSM), which allows a highly compact design, you have to supply three-phase voltage with controllable output frequency and controllable voltage amplitude. There are many different alternatives for the AC/AC converter. Here you will learn all options.

- Part I - An Overview of AC/AC-Converter Topologies

Overview of AC-AC Converters

How to Design a 10kW Three-Phase AC/DC Interface Step by Step

You need a rectifier with sinusoidal input currents (power factor correction) and controlled DC-voltage at the output side? In this report you will learn how to compare the well-known Bidirectional 3-Phase AC/DC PWM Converter with Impressed Output Voltage (VSR) with a Vienna Rectifier employing a simple but effective strategy.

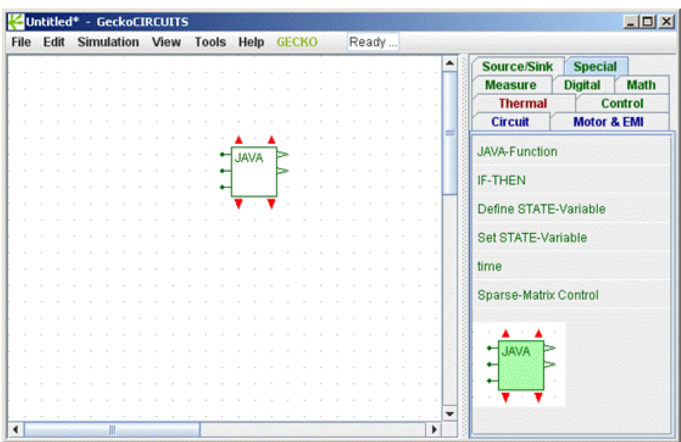
- Part I - How Can I Compare Topologies?
- Part II - Semiconductor Loss Calculation Demystified
- Part III - Do You Know the Junction Temperatures of Your Design? (coming soon)

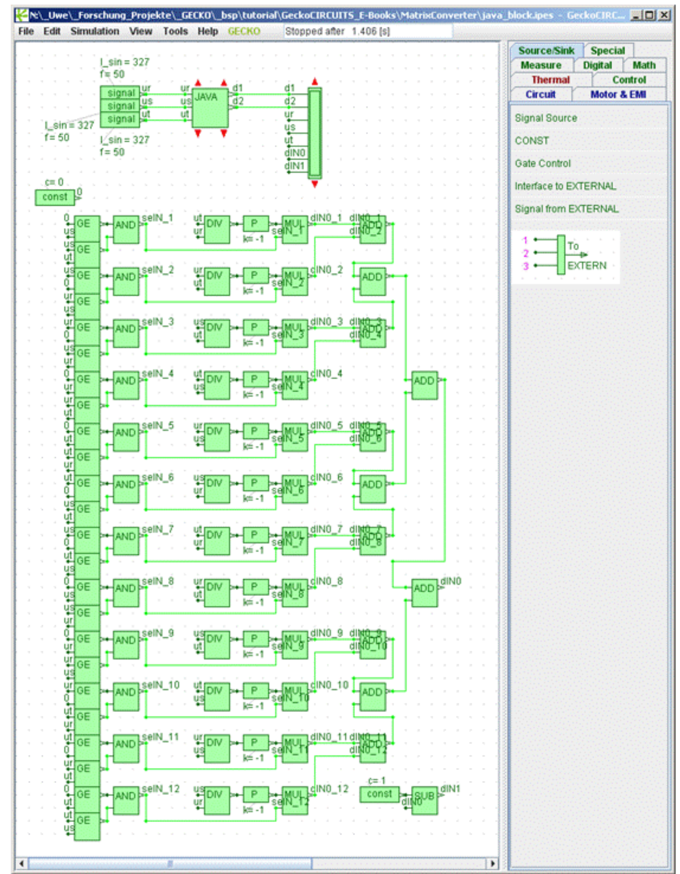
Gecko-Research Application Notes (2)

Useful Hints for e.g. How to Implement Sector Detection for SV Modulation

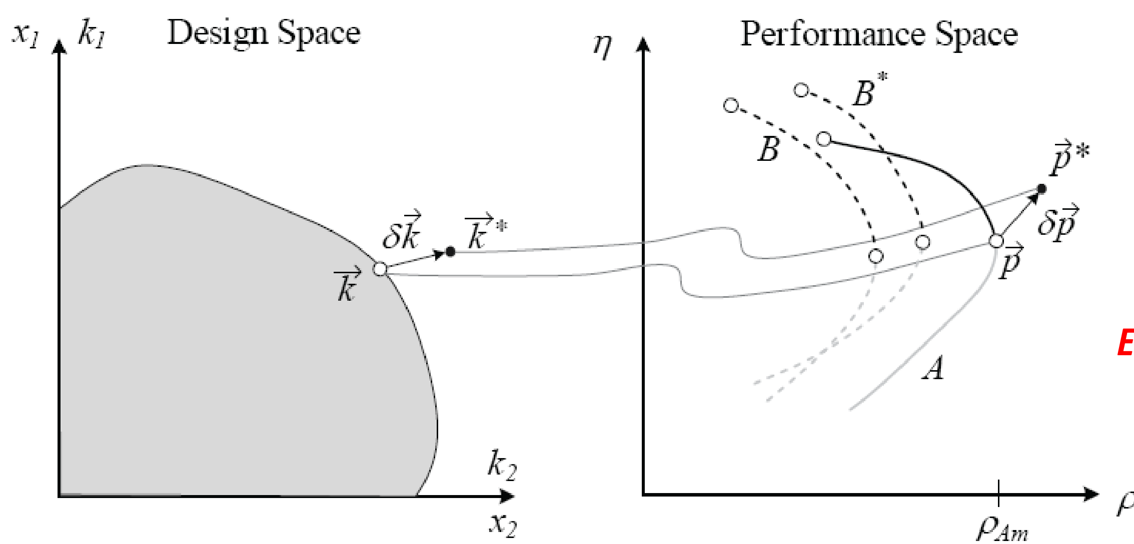
▶ JAVA Code Block

- Integration of Complex Control Code; Enhances Overview and Transparency
- Code can Virtually be Copied to DSP C-Code Generator (Minor Syntax Adaptations)





Power Electronics Converter Optimization



ETH Zurich [50]

Goal: Optimization Toolbox

- *Guided Step-by-Step Converter Design Procedure to Enable Optimal Utilization of Technological Base and Optimal Matching between Design Specifications and Final Performance*

Conclusions

Hype Cycle of Technologies

-Gartner Group

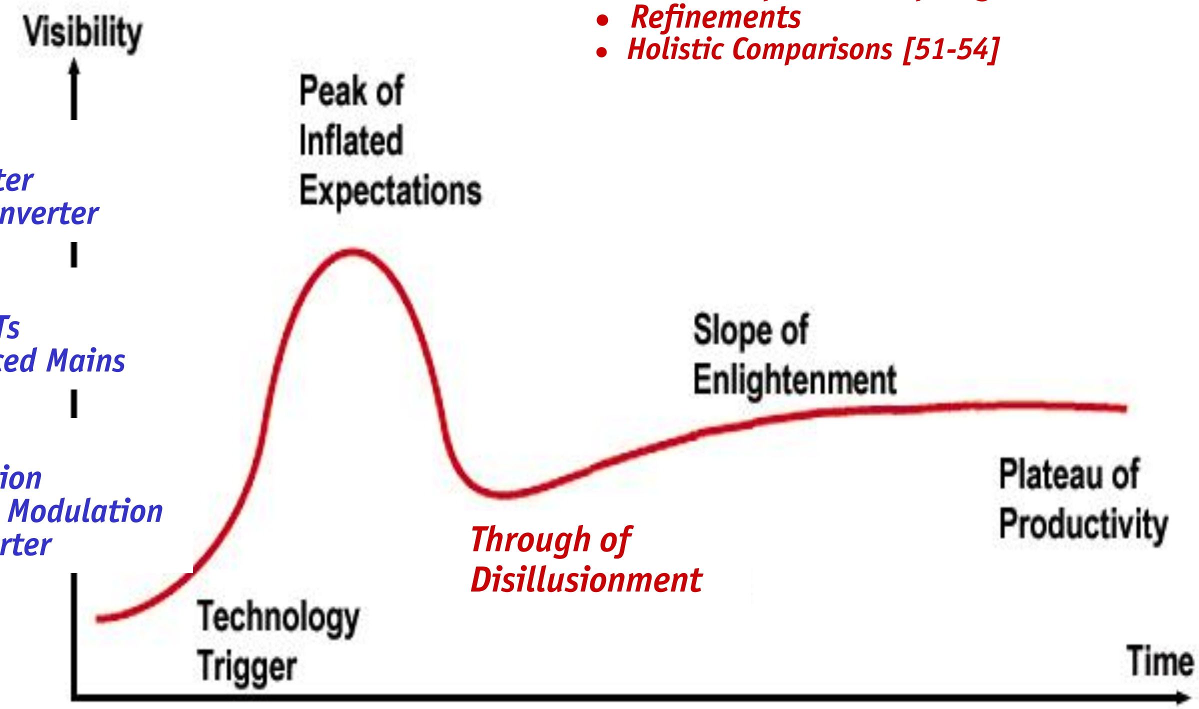
2005 –
- *Hybrid Matrix Converter*
- *More Complicated Topologies*
- *Refinements*
- *Holistic Comparisons [51-54]*

2000
- *Sparse Matrix Converter*
- *Three-Level Matrix Converter*

1995
- *Reverse Blocking IGBTs*
- *Handling of Unbalanced Mains*

1990
- *Multi-Step Commutation*
- *Indirect Space Vector Modulation*
- *Indirect Matrix Converter*

1970´s
- *Invention of Matrix Converter Topology*

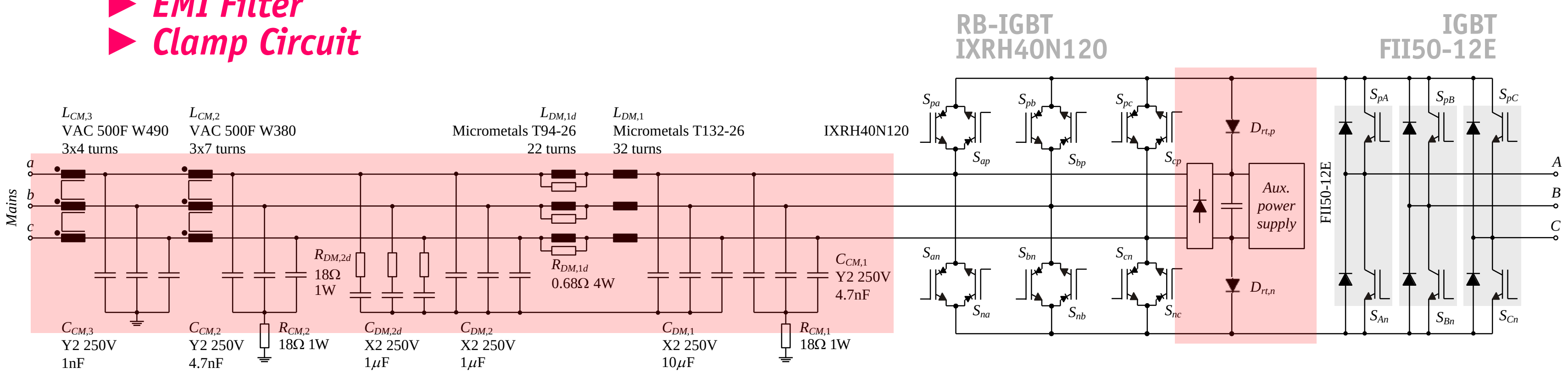


Conclusions (1)

- ***MC is NOT an All-SiC Solution***
  - *Industry Engineers Missing Experience*
  - *86% Voltage Limit / Application of Specific Motors / Silicon Area*
  - *Limited Fault Tolerance*
  - *Braking in Case of Mains Failure*
  - *Costs and Complexity Challenge*
  - *Voltage DC Link Converter could be implemented with Foil Capacitors*

- ***MC does NOT offer a Specific Advantage without Drawback***

- ***EMI Filter***
- ***Clamp Circuit***



Conclusions (2)

- *Research MUST Address Comprehensive System Evaluations*
  - *MC Promising for High Switching Frequency*
  - *Consider Specific Application Areas*
  - *Consider Life Cycle Costs*
  - *etc.*
- *V-BBC is a Tough Competitor*
- *F^3E Might Offer a Good Compromise*
- *Most Advantageous Converter Concept Depends on Application and on whether a CUSTOM Drive Design is Possible*
- *Integration of Multiple Functions (as for MC) Nearly ALWAYS Requires a Trade-off*

Thank You !

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About the Instructors

Johann W. Kolar (F´ 10) received his Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 350 scientific papers in international journals and conference proceedings and has filed 75 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for power supply of data centers, More-Electric-Aircraft and distributed renewable energy systems. Further main areas of research are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multi-domain/multi-scale modeling / simulation and multi-objective optimization, physical model based lifetime prediction, pulsed power, bearingless motors, and Power MEMS.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, and the IEEE IECON Best Paper Award of the IES PETC in 2009. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. He initiated and/or is the founder / co-founder of 4 Spin-off Companies targeting ultra high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.

Thomas Friedli (M'09) received his M.Sc. degree in electrical engineering and information technology (with distinction) and his Ph.D. from the Swiss Federal Institute of Technology (ETH) Zurich, in 2005 and 2010, respectively.

From 2003 to 2004 he worked as a trainee for Power-One in the R&D centre for telecom power supplies. His Ph.D. research from 2006 to 2009 involved the further development of current source and matrix converter topologies in collaboration with industry using silicon carbide JFETs and diodes and a comparative evaluation of three-phase ac-ac converter systems.

He received the 1st Prize Paper Award of the IEEE IAS IPCC in 2008 and the IEEE IAS Transactions Prize Paper Award in 2009.