Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

compel 2014

# Tutorial 2

# X-treme Efficiency Power Electronics

**J. W. Kolar**
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

compel 2014

# Deep Green Power Electronics

**J. W. Kolar**
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

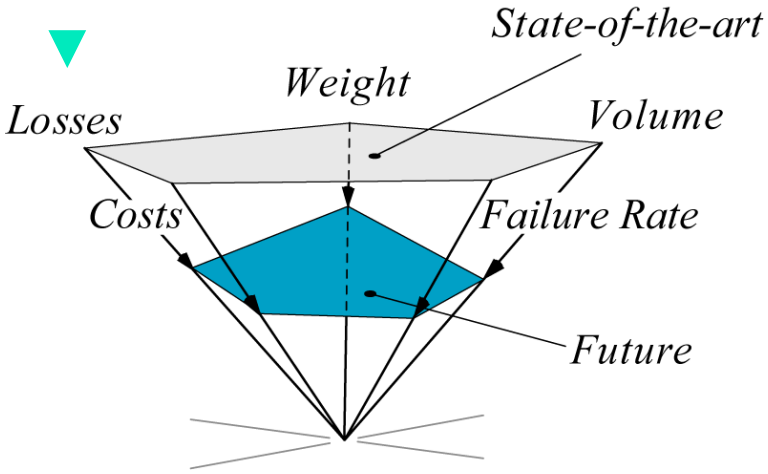
# Outline

- Trends of Efficiency Improvement
- Converter Loss Components
- Efficiency Improvement by
  - * Design
  - * Control
  - * Topology & Control
- Highly Accurate Efficiency Measurement
- $\eta > 99\%$ Converter Demonstrators
- Conclusions

# Power Electronics Performance Trends

- **Performance Indices**

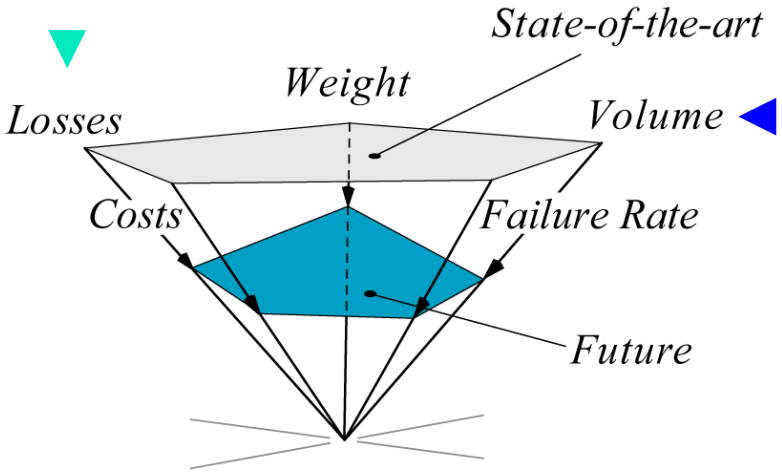
  - **Power Density [kW/dm³]**
  - **Power per Unit Weight [kW/kg]**
  - **Relative Costs [kW/$]**
  - **Relative Losses [%]**
  - **Failure Rate [h⁻¹]**



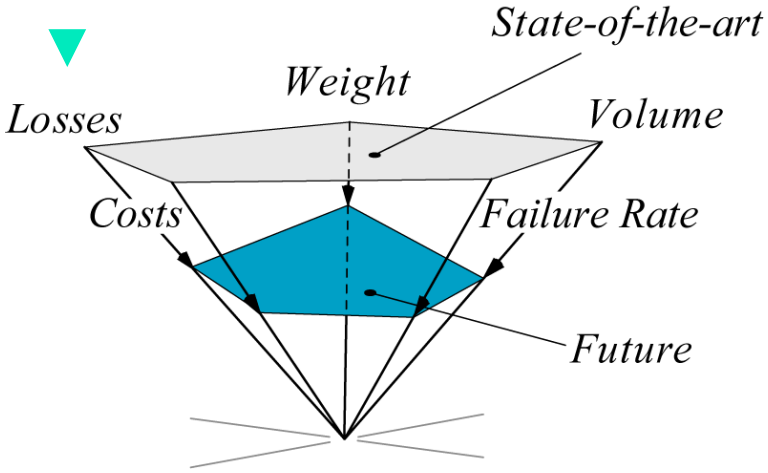
# Drivers for High Efficiency

< 2000 Increase of Power Density / Thermal Limitation / Max. Full Load Efficiency

> 2000 Mostly Voluntary Efficiency Requirements for Entire Power Range (100%, 50%, 20%)

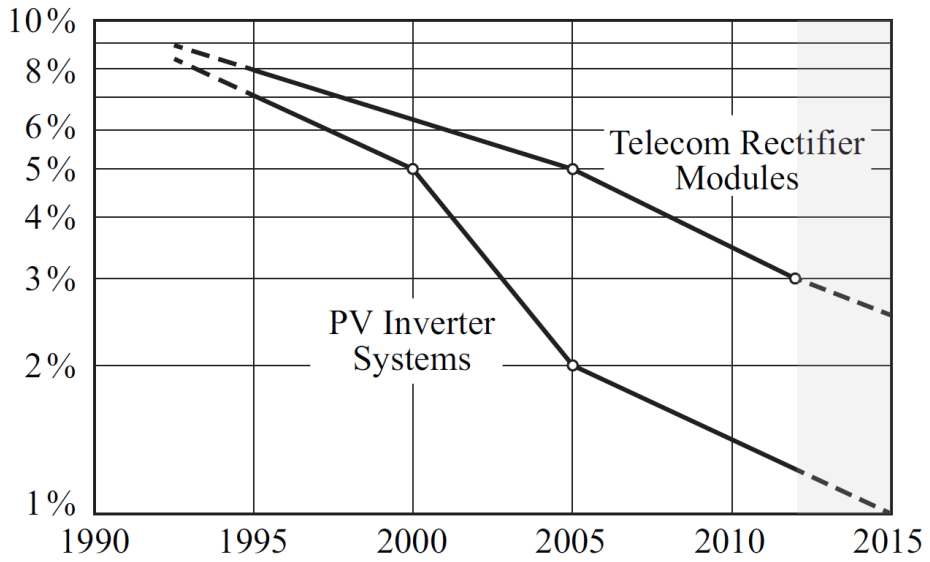


# Efficiency / Power Factor Limits (5%)...20%...100% Load

# General Efficiency Trends

Inefficiency (Losses)...

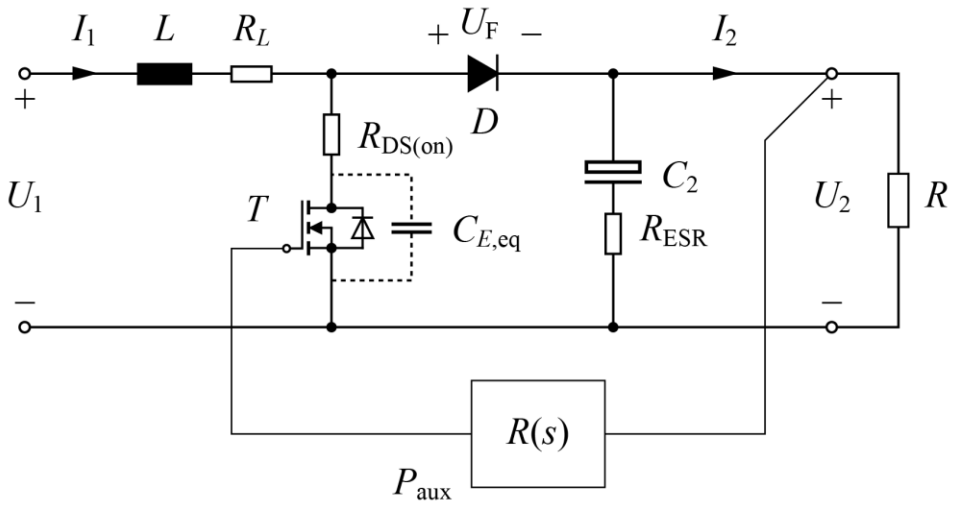



— PV Inverters: Typ. Loss Reduction of Factor 2 over 5 Years

# Efficiency Basics

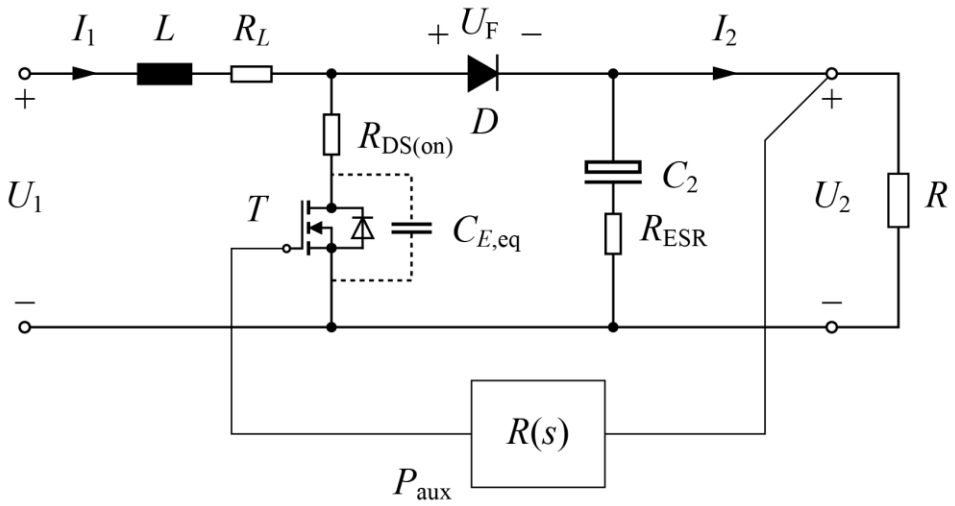
Converter Loss Components
Efficiency Maximum
Efficiency vs. Power Factor

# Non-Idealities of Converter Circuits




- $P_V = (P_{aux} + \frac{1}{2} C_{E,eq} U_2^2 f_P) + (U_F + k_P f_P) I_2 + (1-D)^{-2} (R_L + D R_{DS(on)} + D(1-D) ESR) I_2^2$

# Non-Idealities of Converter Circuits

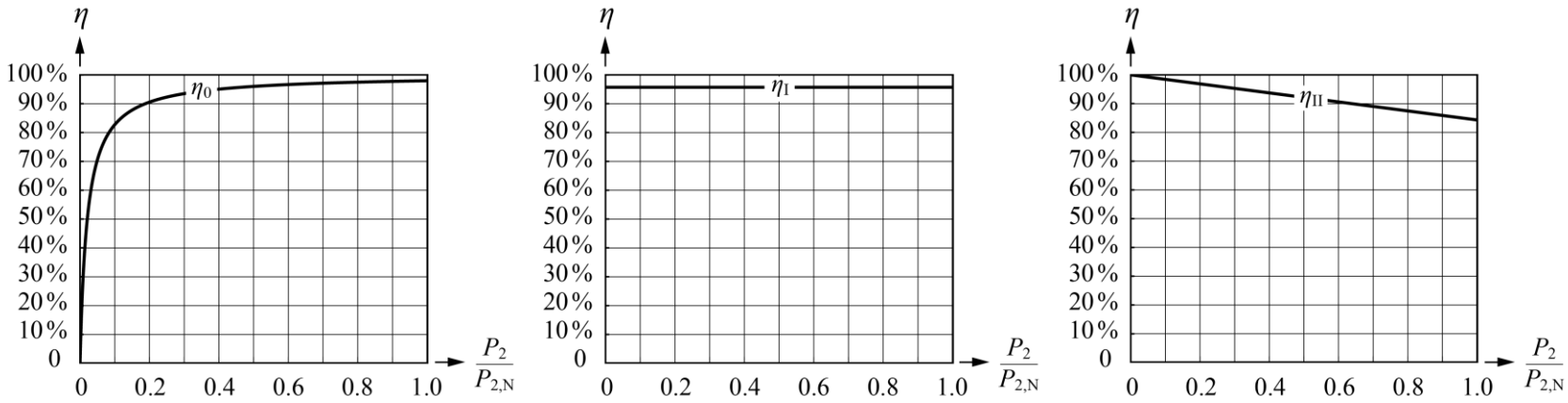



- $$P_V = P_{V,0} + P_{V,I} + P_{V,II} = k_0 + k_I P_2 + k_{II} P_2^2$$

# Influence of Loss Components on Efficiency Characteristic

$$\eta = \frac{P_2}{P_1} = \frac{1}{1 + \frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}$$

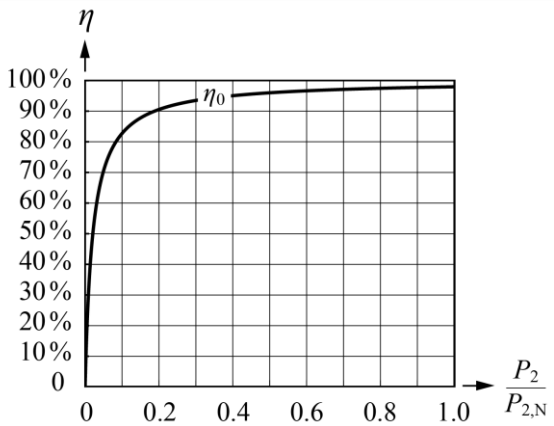
$$P_V = P_{V,0} + P_{V,I} + P_{V,II} = k_0 + k_I P_2 + k_{II} P_2^2$$



# Influence of Loss Components on Efficiency Characteristic

$$\eta = \frac{P_2}{P_1} = \frac{1}{1+\frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}$$

$$P_V = P_{V,0} + P_{V,I} + P_{V,II} = k_0 + k_I P_2 + k_{II} P_2^2$$



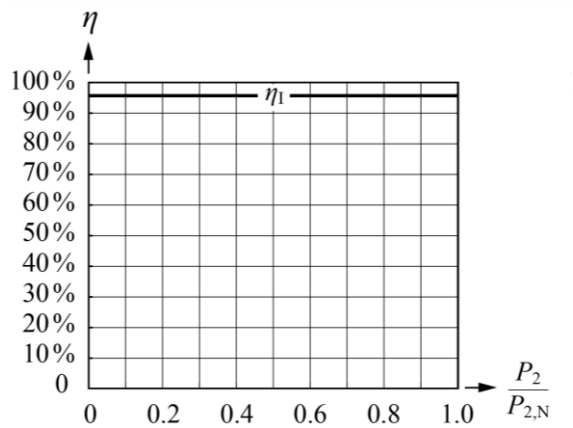

► **Only Constant Losses**

$$\eta_0 = \frac{1}{1+\frac{P_{V,0}}{P_2}} = \frac{1}{1+\frac{k_0}{P_2}} \approx 1 - \frac{k_0}{P_2}$$

# Influence of Loss Components on Efficiency Characteristic

$$\eta = \frac{P_2}{P_1} = \frac{1}{1+\frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}$$

$$P_V = P_{V,0} + P_{V,I} + P_{V,II} = k_0 + k_I P_2 + k_{II} P_2^2$$



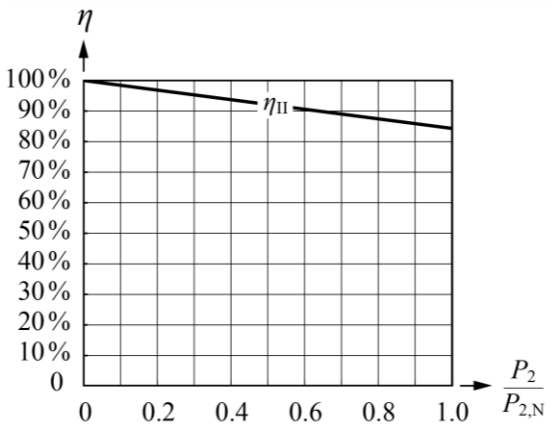

► **Only Power Proportional Losses**

$$\eta_I = \frac{1}{1+\frac{P_{V,I}}{P_2}} = \frac{1}{1+k_I} \approx 1 - k_I = const.$$

# Influence of Loss Components on Efficiency Characteristic

$$\eta = \frac{P_2}{P_1} = \frac{1}{1+\frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}$$

$$P_V = P_{V,0} + P_{V,I} + P_{V,II} = k_0 + k_I P_2 + k_{II} P_2^2$$

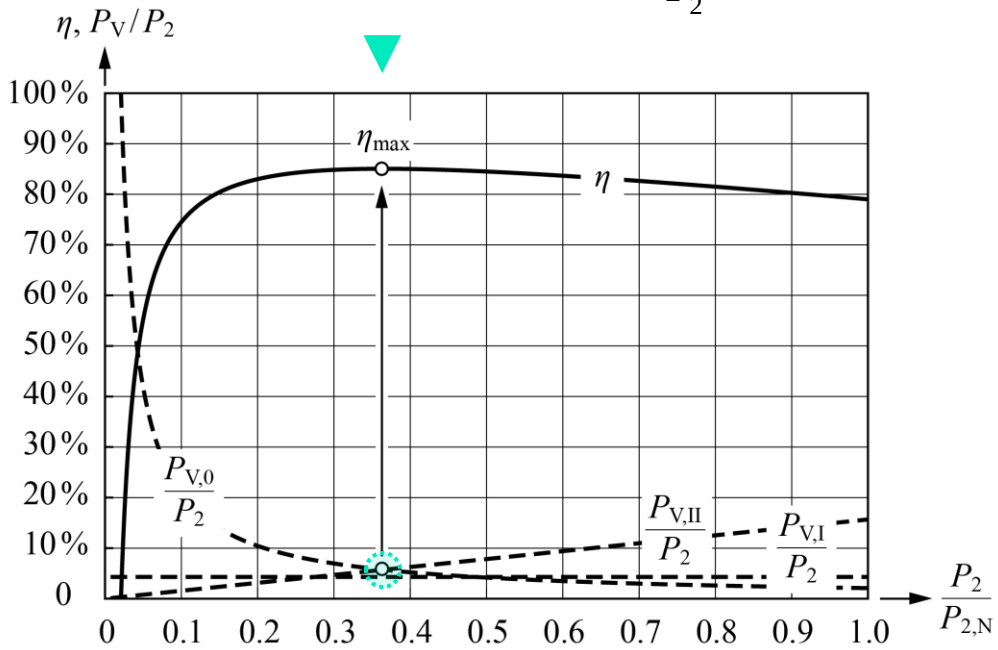



► **Quadratically Power Dependent Losses**

$$\eta_{II} = \frac{1}{1+\frac{P_{V,II}}{P_2}} = \frac{1}{1+k_{II}P_2} \approx 1 - k_{II}P_2$$

# Efficiency Maximum

$$\eta = \frac{P_2}{P_1} = \frac{1}{1 + \frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}$$

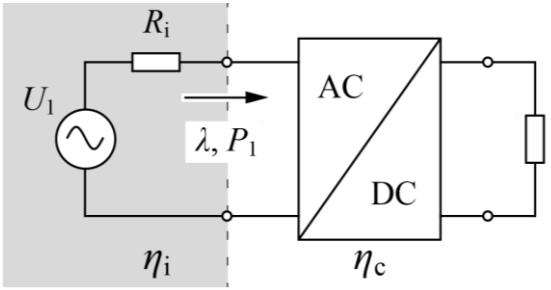



**@ Maximum:** **Equal Constant and Quadratic Losses**

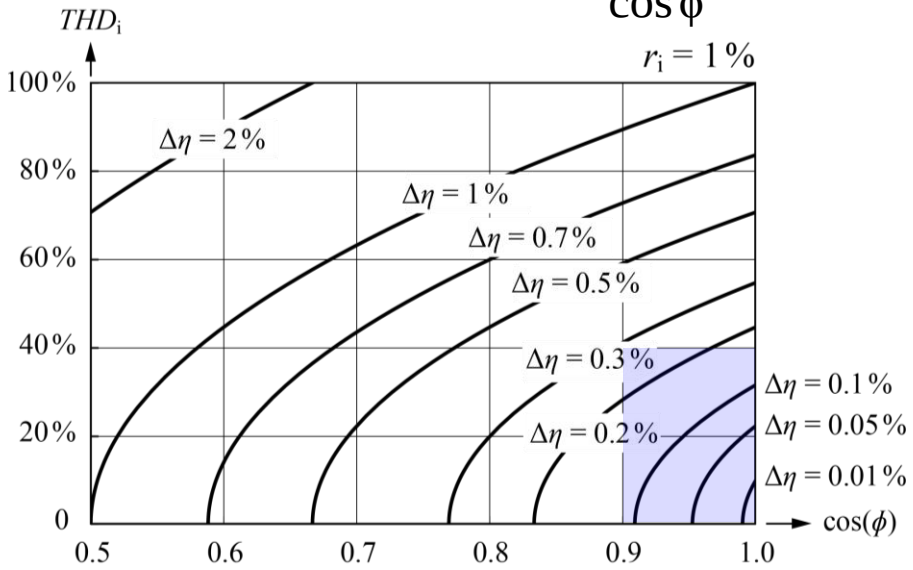
$$P_{V,II,\eta\max} = P_{V,0}$$

# Efficiency vs. Power Factor

$$\eta_i \approx 1 - \frac{P_{V,Ri}}{P_1} = 1 - \frac{I_1^2 R_i}{U_1 I_{1,(1)} \cos\phi}$$




$$\Delta\eta = r_i\left(1 - \frac{1 + THD_i^2}{\cos\phi}\right)$$




► **Sensible Compromise e.g. for Three-Phase Systems**

# Measures for Efficiency Improvement

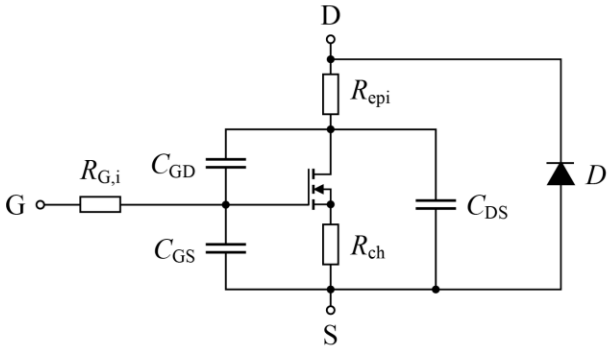
**Design**
- Power Semiconductors
- Inductive Components / EMI-Filter
- Auxiliaries

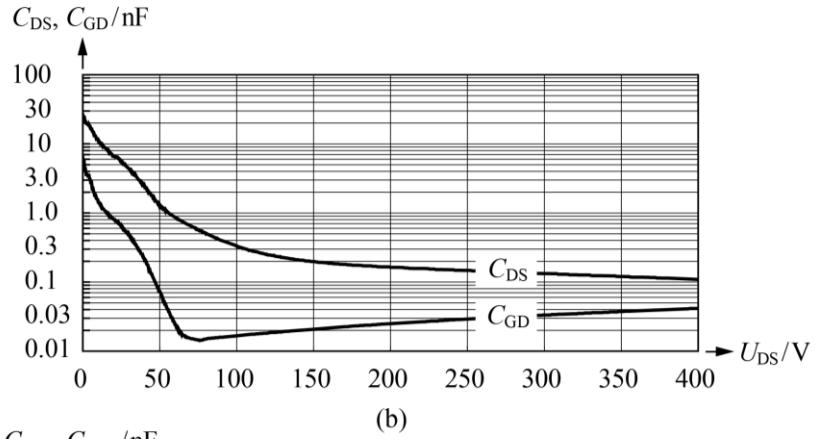
# Power Semiconductors

# Power Semiconductors

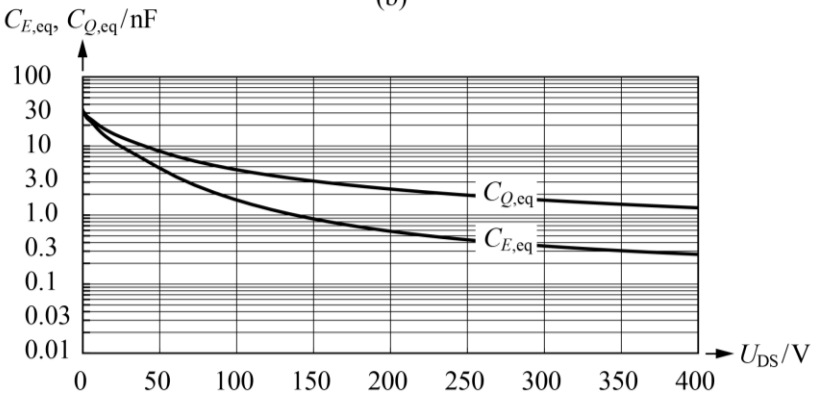
- On-State Losses
- Capacitive Switching Losses

$$C_{GS} = C_{iss} - C_{rss}$$
$$C_{GD} = C_{rss}$$
$$C_{DS} = C_{oss} - C_{rss}$$




(b)



# Power Semiconductors

- On-State Losses
- Capacitive Switching Losses

$$P_{V,T} = I_{DS,rms}^2 R_{DS(on)} + \frac{1}{2} C_{E,eq}(U_2) U_2^2 f_P$$

# Power Semiconductors

$$R_{DS(on)} = \frac{R^*_{DS(on)}}{A_{Si}}$$

$$C_{E,eq} = C^*_{E,eq} A_{Si}$$

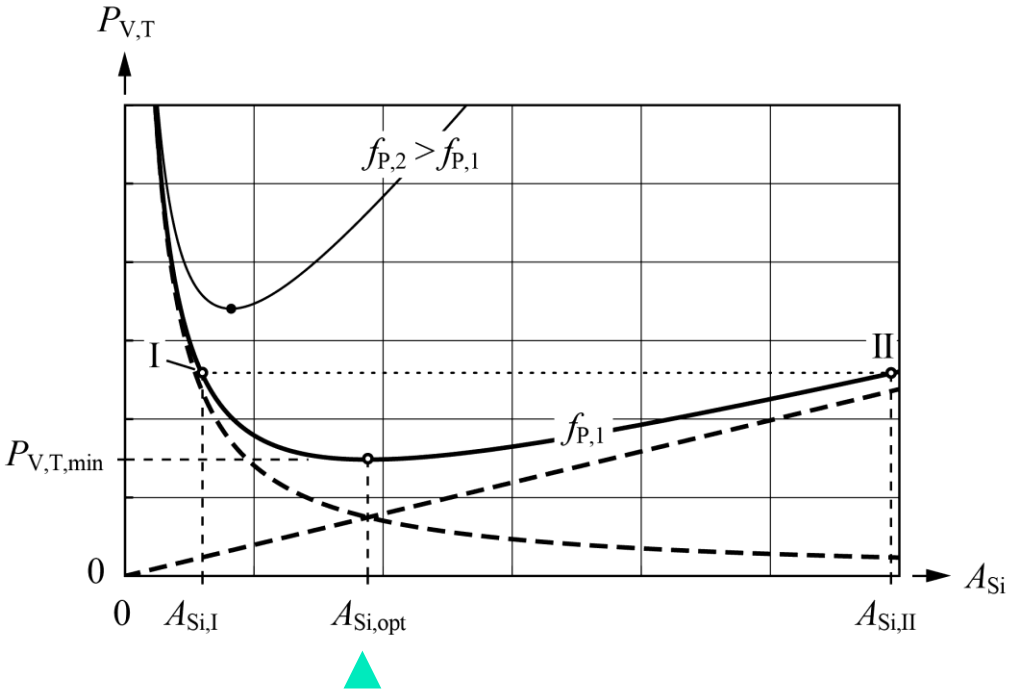
$$P_{V,T} = \gamma_C \frac{1}{A_{Si}} + \gamma_P A_{Si} f_P$$

▶ **Silicon Area Related Resistance / Capacitance**

# Power Semiconductors

$$R_{DS(on)} = \frac{R^*_{DS(on)}}{A_{Si}}$$

$$C_{E,eq} = C^*_{E,eq} A_{Si}$$

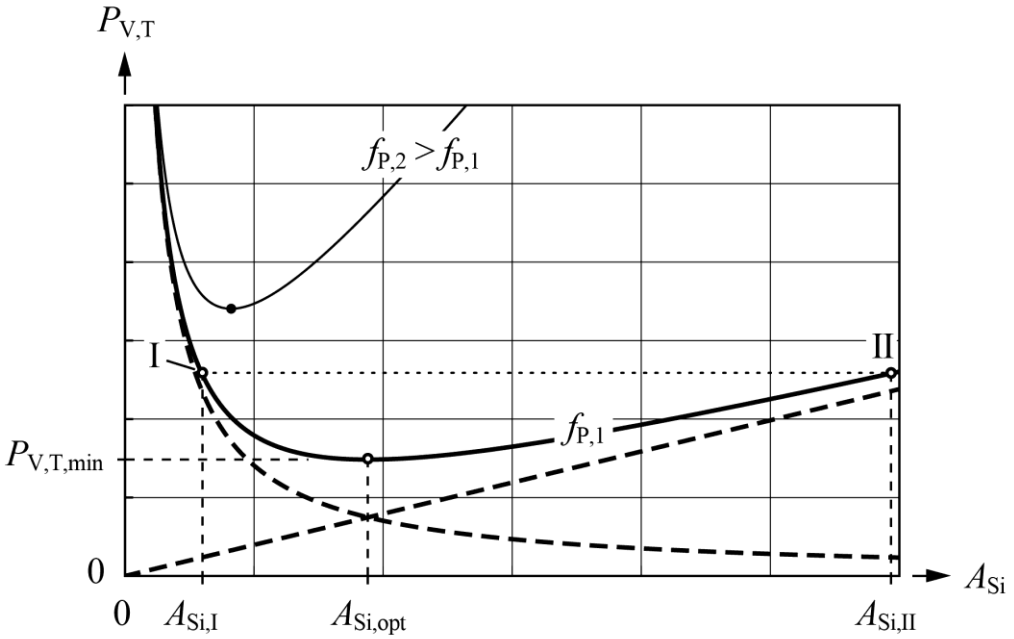



► **Optimum Silicon Area - Minimum Losses**

# Power Semiconductors - Efficiency Barrier

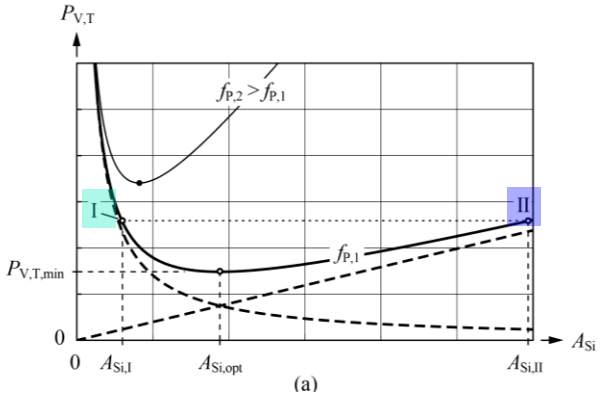
$$R_{DS(on)} = \frac{R^*_{DS(on)}}{A_{Si}}$$

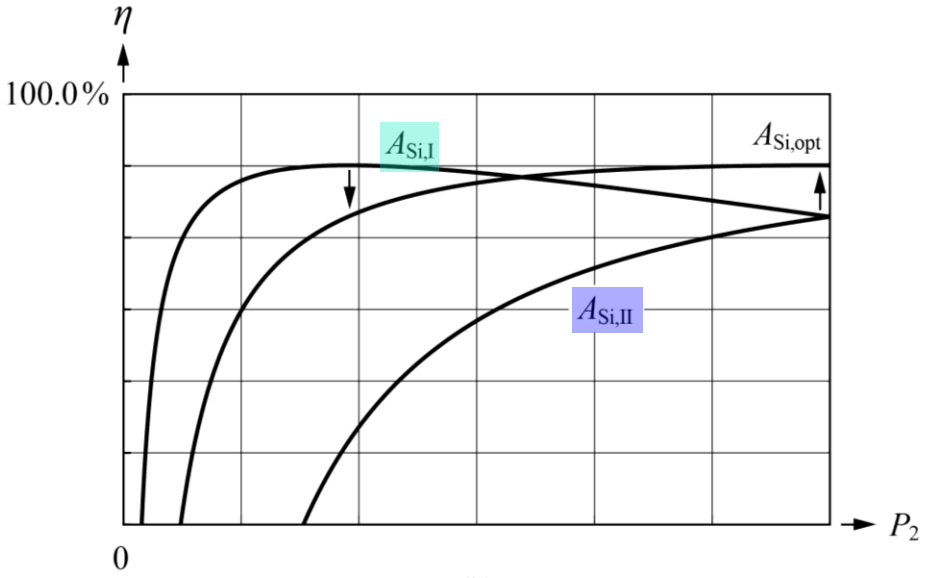
$$C_{E,eq} = C^*_{E,eq} A_{Si}$$




$$P_{V,T,\min} = 2\sqrt{\gamma_C \gamma_P}\sqrt{f_P} = \sqrt{2} I_{rms} U_2 \sqrt{f_P}\sqrt{R^*_{DS(on)} C^*_{E,eq}} \propto \frac{1}{FOM_\eta}$$

# Power Semiconductors




- Selection of $A_{Si} > A_{Si,opt}$ Leads to Lower Efficiency in Whole Operating Range

# Inductive Components / EMI Filter

# Inductive Components – Efficiency vs. Volume

- Iron Losses

$$\Delta B = \frac{L\Delta i}{NA_E} \propto \frac{U_d}{f_P A_E} \propto \frac{1}{A_E} \propto \frac{1}{l^2}$$

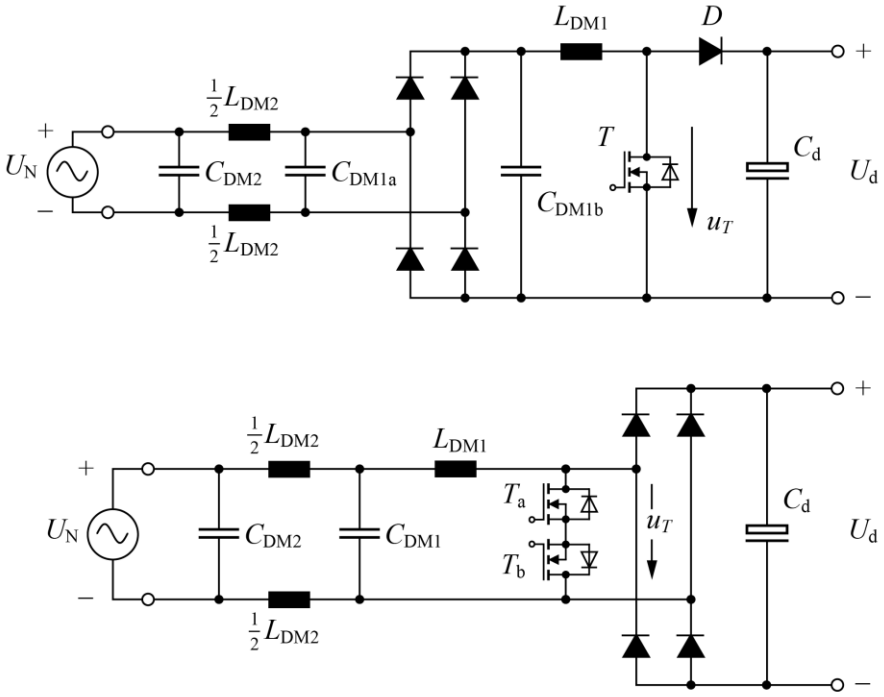
$$P_{V,E} \propto f_P^{\alpha} \Delta B^{\beta} V_E \propto \approx (\frac{1}{l^4}) l^3 \propto \frac{1}{l}$$

- Copper Losses

$$P_{V,W} = I_{rms}^2 R_W \propto \frac{l}{\kappa A_W} \propto \frac{l}{l^2} = \frac{1}{l}$$

► Iron and Copper Losses are Decreasing with Increasing Linear Dimensions

# Selection of the Switching Frequency

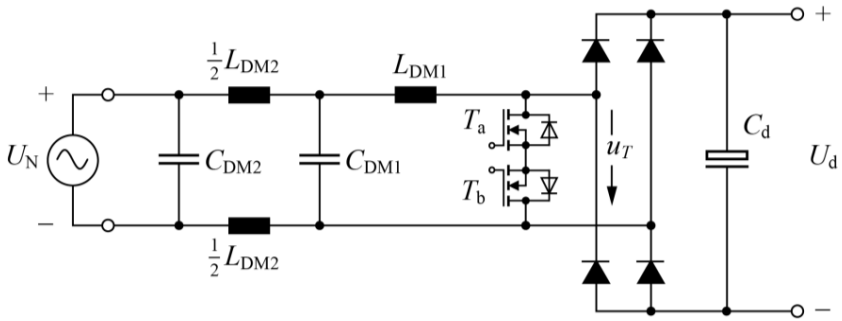


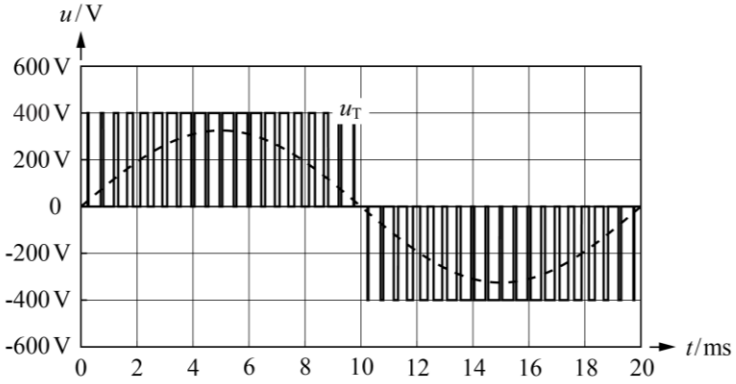

- **Example of Single-Phase PFC Rectifier Systems**

# Selection of the Switching Frequency

- Consider Boost Inductor as Part of EMI Filter
- Calculate Equivalent Noise Voltage @ Switching Frequency

$$M = \frac{\hat{U}_N}{U_d}$$



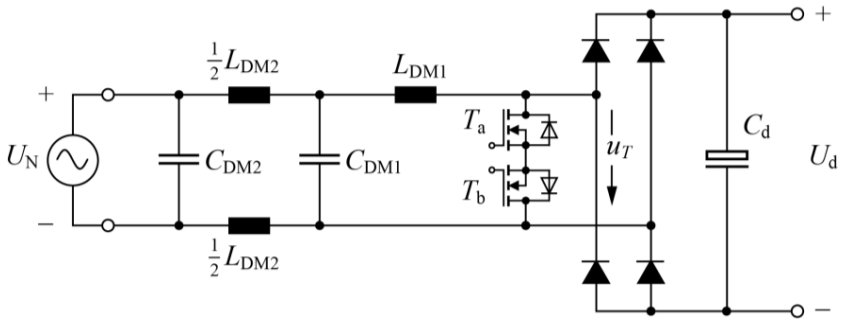

$$\hat{U}_{T,(n)} = U \quad \rightarrow \quad \hat{U}^2_{T,(n)} = U^2$$
$$\hat{U}_{T,(2n)} = \tfrac{1}{2}U \quad \rightarrow \quad \hat{U}^2_{T,(2n)} = \tfrac{1}{4}U^2$$

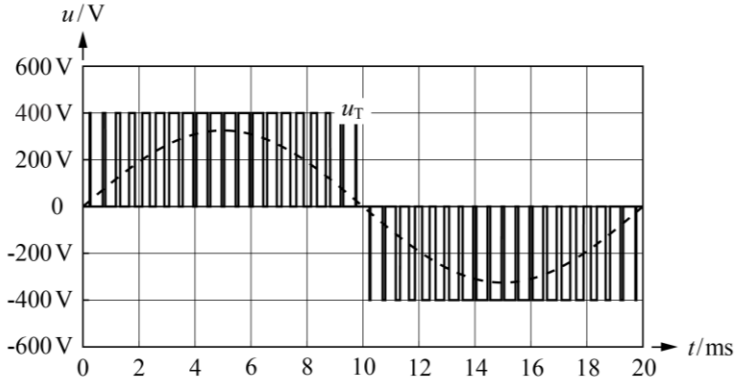
**Limited Influence of Higher Order Harmonics**

# Selection of the Switching Frequency

- Consider Boost Inductor as Part of EMI Filter
- Calculate Equivalent Noise Voltage @ Switching Frequency

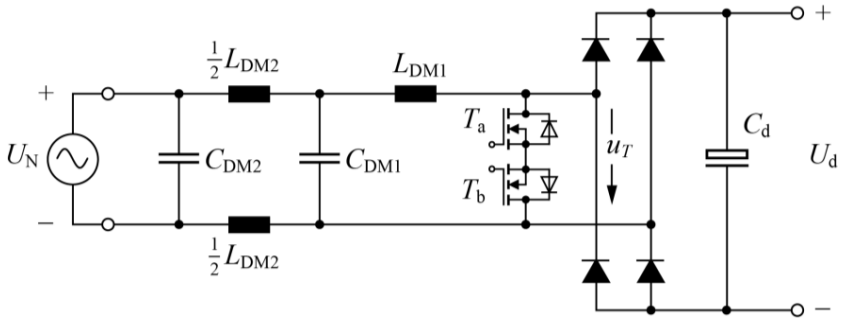
$$M = \frac{\hat{U}_N}{U_d}$$

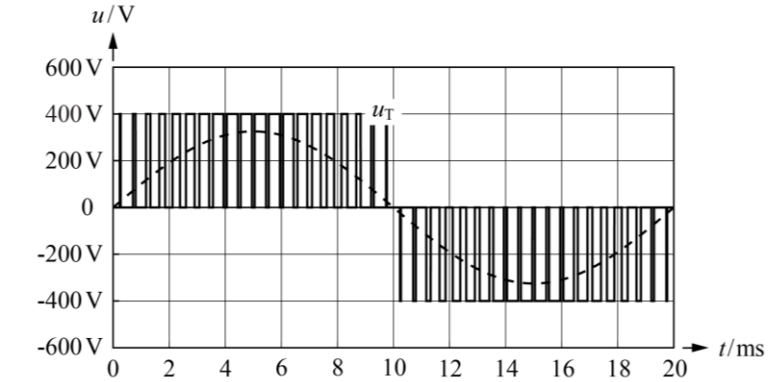


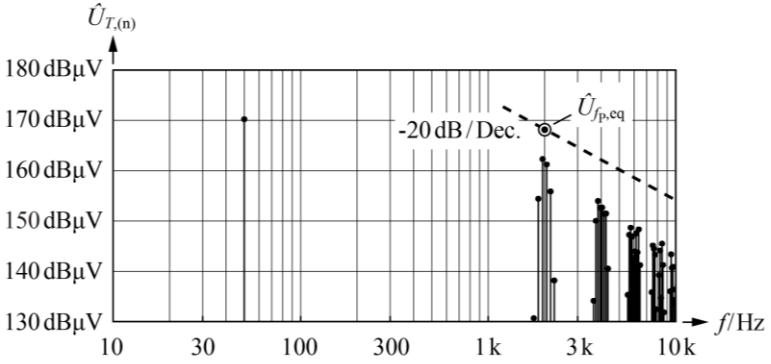




$$U_{f_P,eq,rms}^2 = U_{T,rms}^2 - U_{N,rms}^2 \quad \rightarrow \quad U_{f_P,eq,rms} = \sqrt{M\left(\frac{2}{\pi} - \frac{M}{2}\right)}\, U_d$$

# Selection of the Switching Frequency

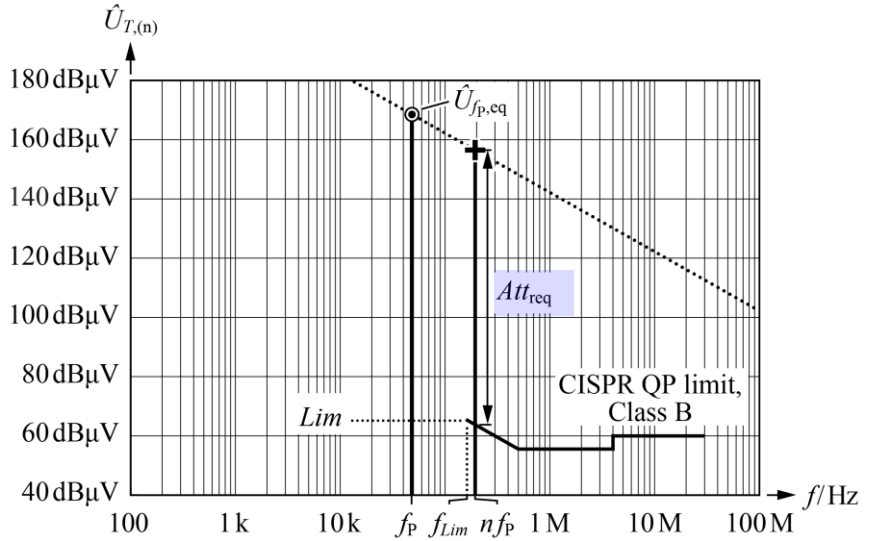


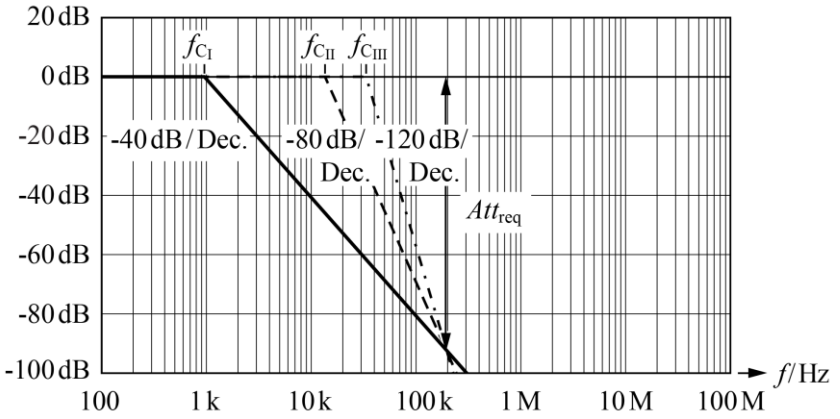




- **Equivalent Noise Voltage @ Switching Frequency**

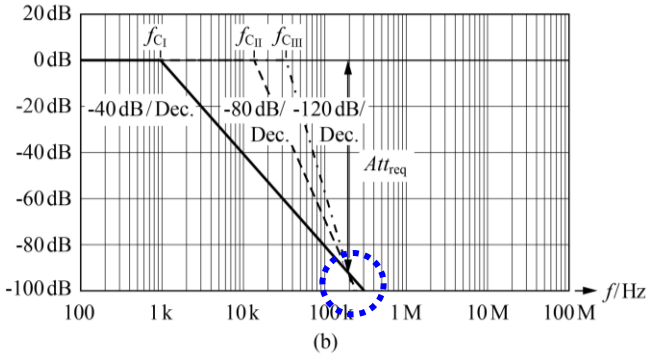
# Required EMI Filter Attenuation

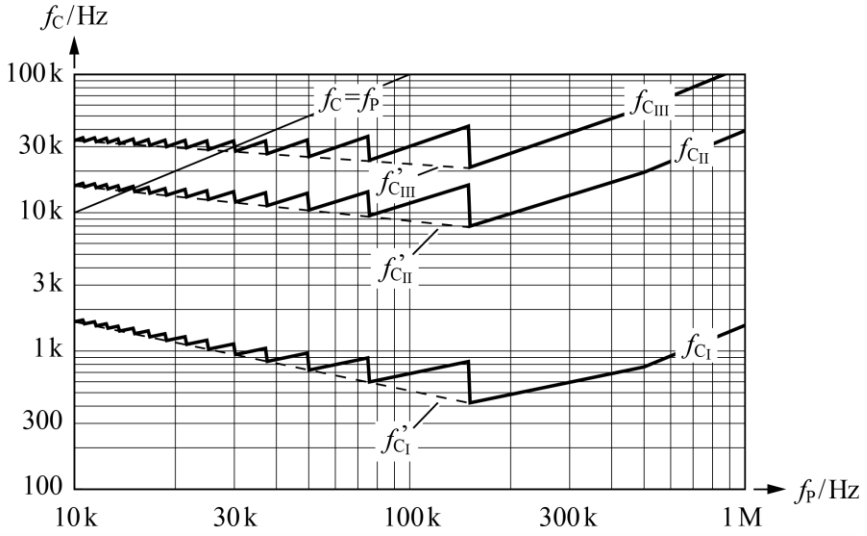



- **Higher Switching Frequency Increases Required Attenuation**

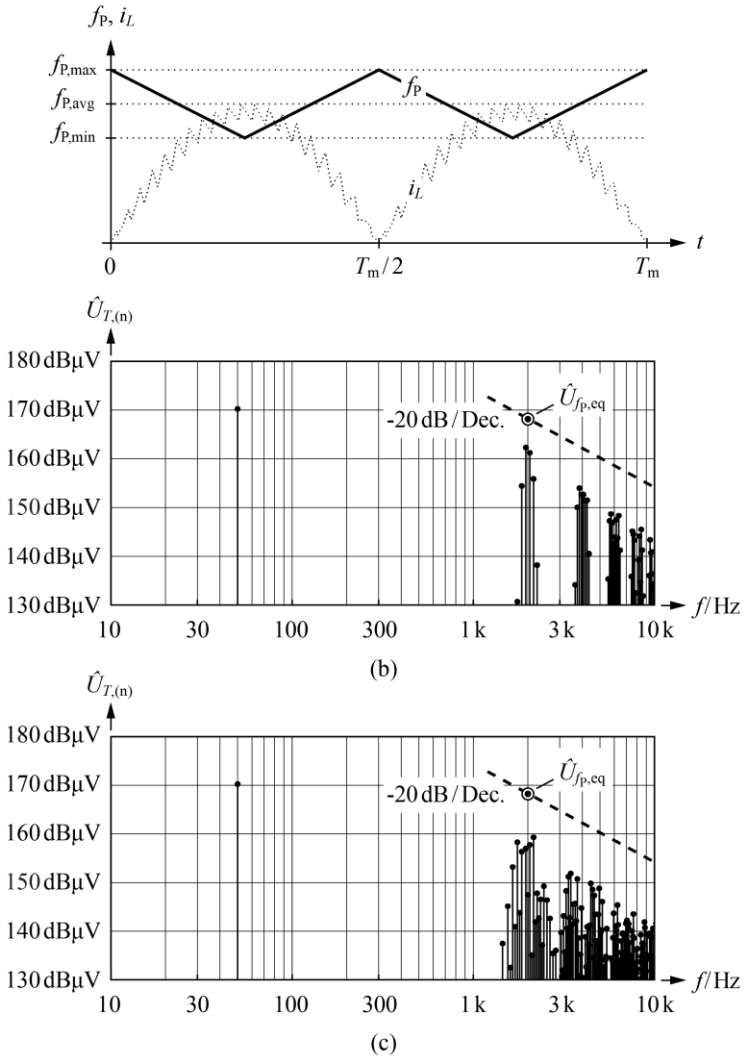
# Required EMI Filter Attenuation



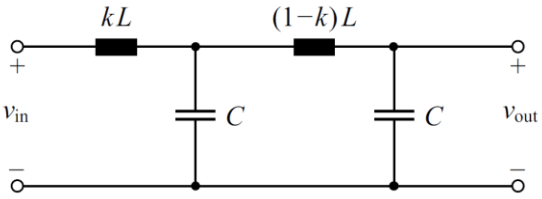

- **Higher Switching Frequency Increases Required Attenuation**

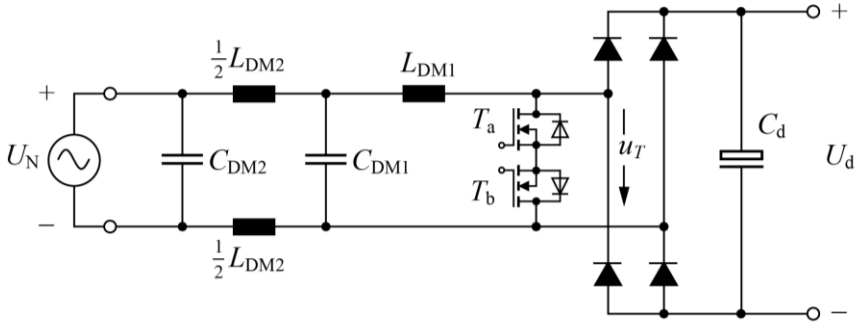
# Minimize Required EMI Filter Attenuation




- **Distribute Harmonic Power Equal over Frequency Range**

# EMI Filter Optimization



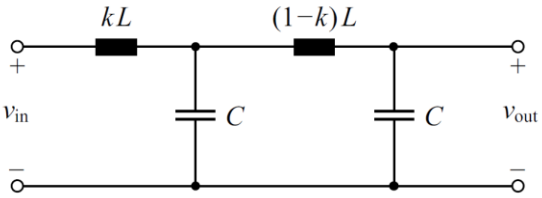



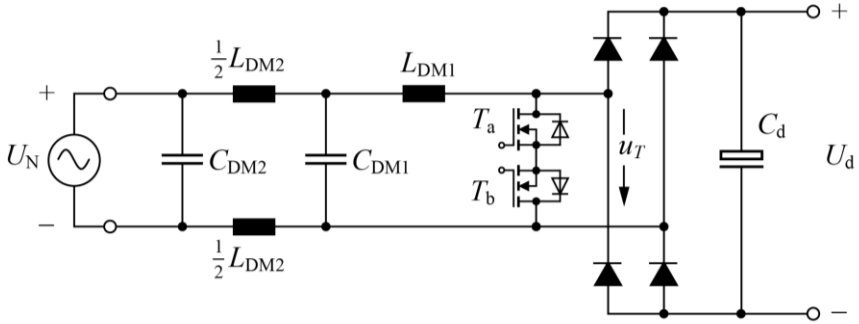

$$G_F \approx \frac{1}{\omega^4 k(1-k)L^2C^2}$$

$$k_{opt} = 0.5$$

► **Equal Partitioning of Total Inductance Provides Max. Attenuation**

# EMI Filter Optimization




$$V_C = \rho_C \tfrac{1}{2} C U^2 = k_C C$$
$$V_L = \rho_L \tfrac{1}{2} L I^2 = k_L L$$

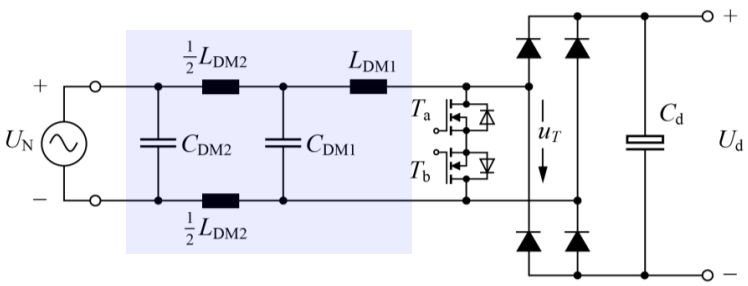
$$\rightarrow \quad V_C = rV, \quad V_L = (1-r)V \quad \rightarrow \quad LC = \frac{(1-r)}{k_L}\frac{r}{k_C}V^2 \rightarrow Max$$

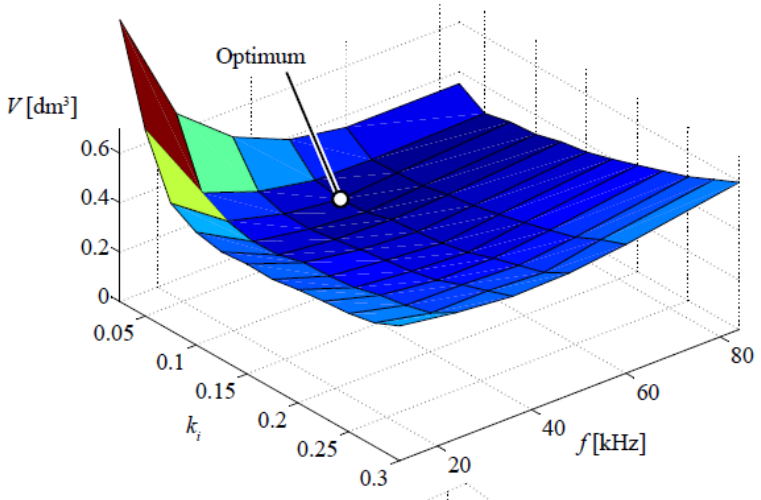
$$r_{opt} = 0.5$$

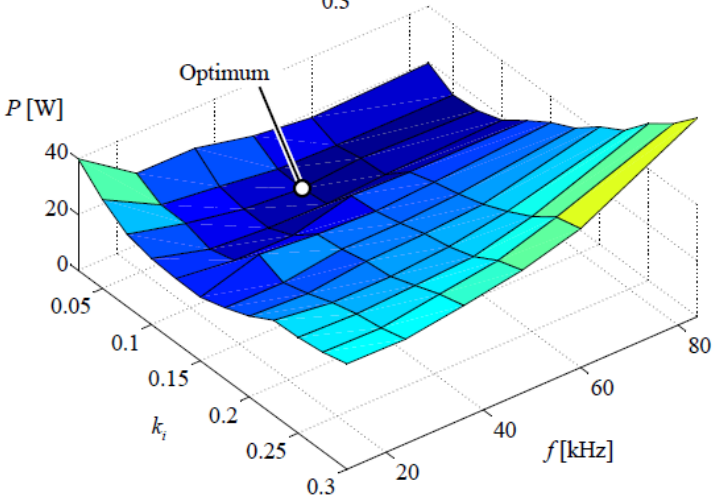
► **Equal Partitioning of Total Volume between *L* & *C* Provides Max. Attenuation**

# EMI Filter Optimization

- **Impact of Switching Frequency and Ripple Ratio on Volume**



# EMI Filter Optimization

## Impact of Switching Frequency and Ripple Ratio on Volume ($P_N$=1.5kW)

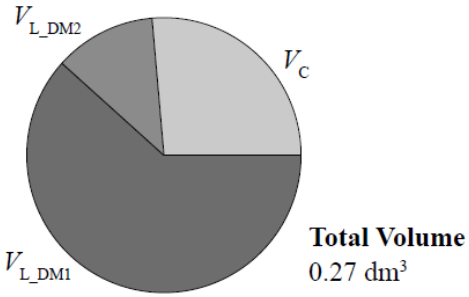
**Operating Point**

$f$ 48 kHz
$k_i$ 0.075
Attenuation 85 dB

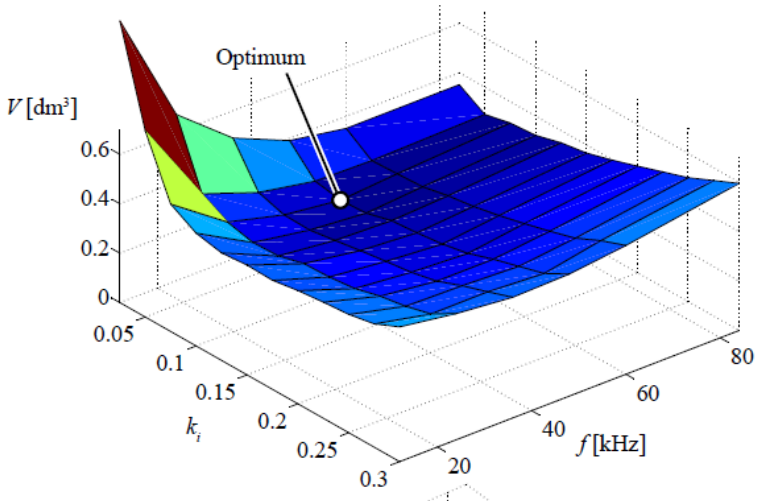
**Filter Values**

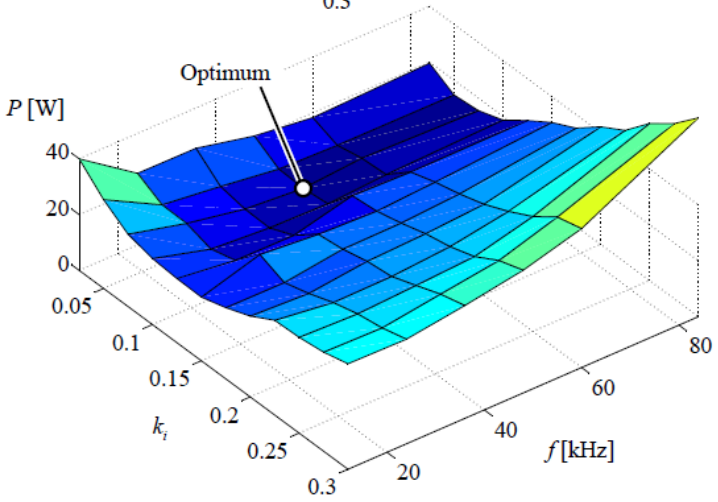
$L_{DM1}$ = 1.5 mH
$L_{DM2}$ = 204 µH
$C_{DM1}$ = $C_{DM2}$ = 6.4 µF

**Volume Partitioning**




**Total Volume**
0.27 dm³

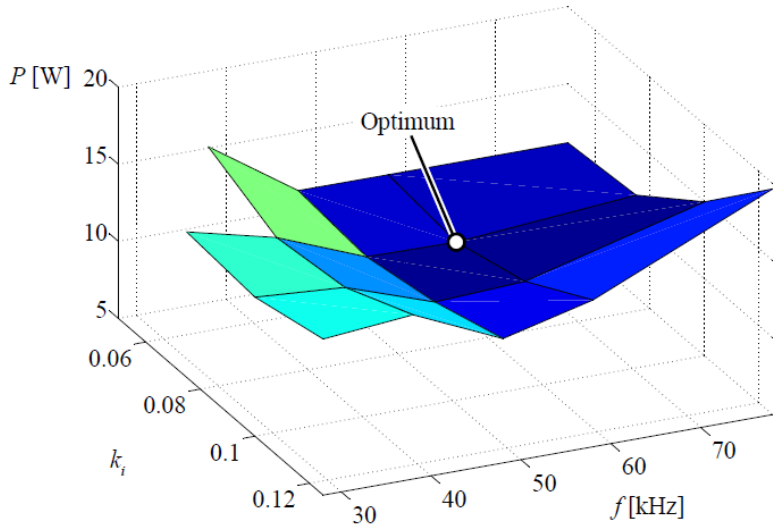


# EMI Filter Optimization

- **Optimization for Minimum Losses at Given Maximum Filter Volume**

$$V_{\max} = 0.4\text{dm}^3$$
$$k_i = 0.075$$
$$f_P = 58\text{kHz}$$



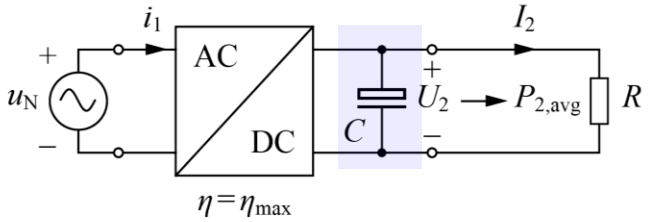

- **Optimum Values $k_i$ and $f_P$ are Close to Volume Optimal Design**

# Measures for Efficiency Improvement

**Control** - Intermittent Operation
- Interleaving

# Intermittent Operation

# Intermittent Operation

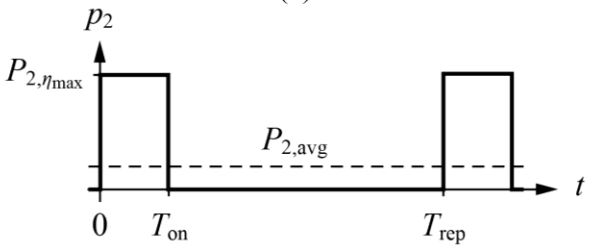



(a)

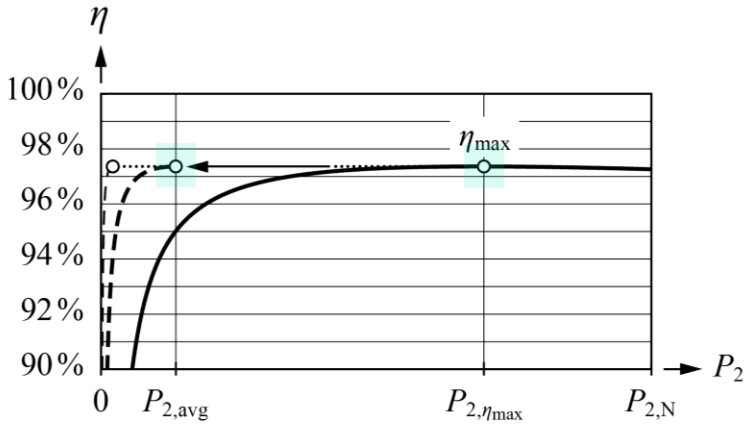
- **Operate Converter ONLY at Maximum Efficiency Power Level**
- **Adjust Delivered Power by Proper Selection of the Duty Cycle**

$$\frac{T_{on}}{T_{rep}} = \frac{P_{2,avg}}{P_{2,\eta max}}$$

$$\eta = \eta_{max}$$



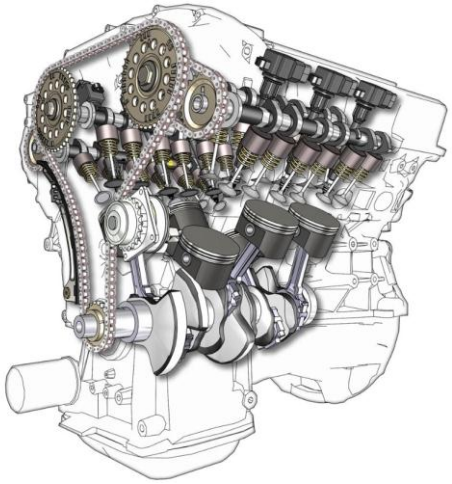

(b)




(c)

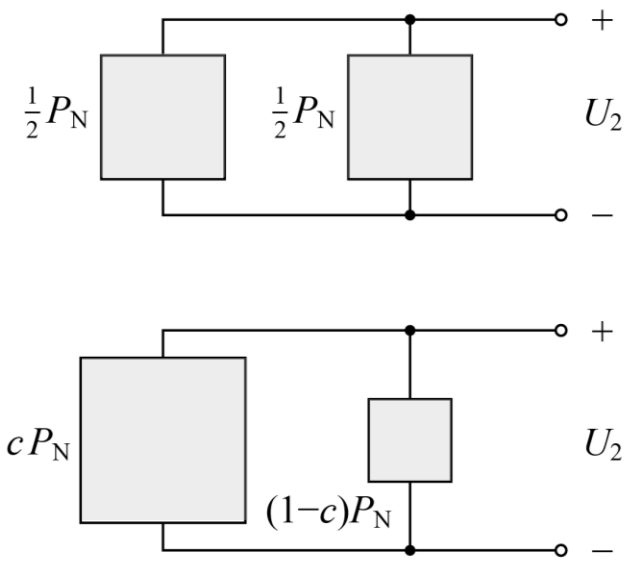
- **Energy Storage Requirement !**

# Parallel Interleaving



## Mechanical Version of "Parallel Interleaving"

# Parallel Operation of Multiple Sub-Systems



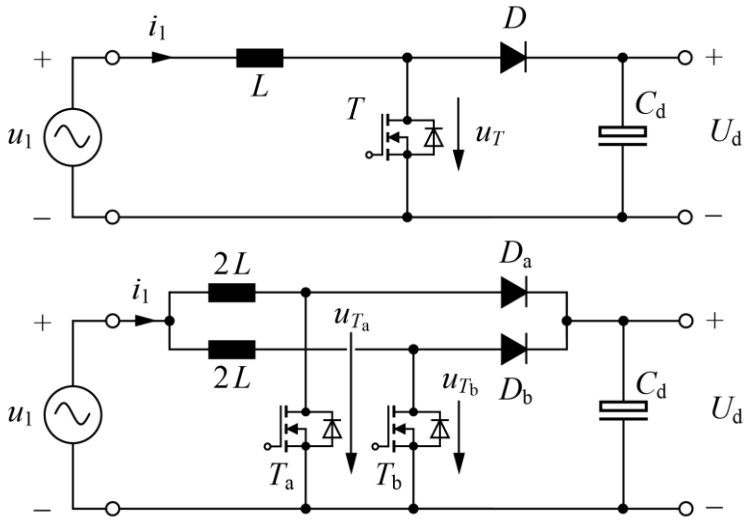

- Features Phase-Shedding (Equivalent to Adjustable Silicon Area!)
- Features Cancellation of Harmonics

# Parallel Operation of Multiple Sub-Systems

$$P_{2,a} = aP_2$$

$$P_{2,b} = (1-a)P_2$$

$$a_{opt} = 0.5$$

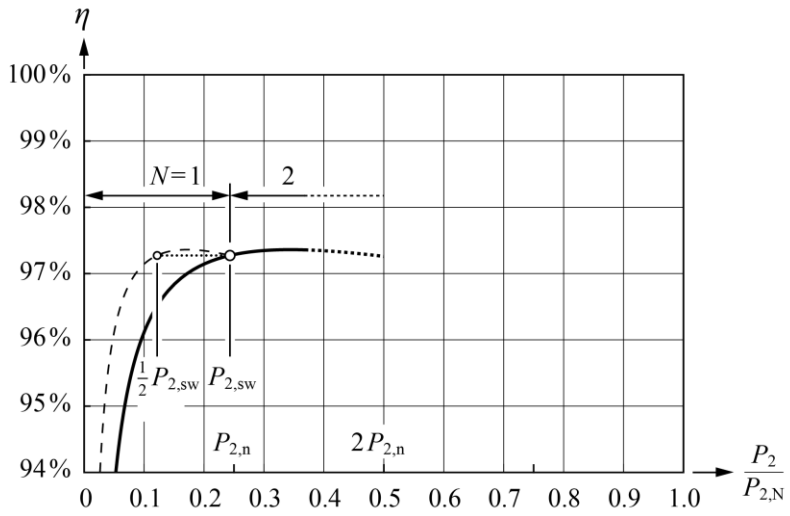


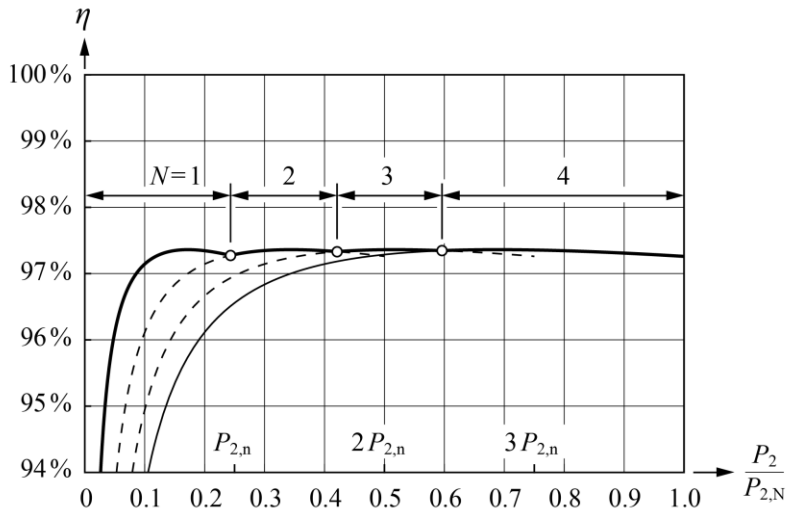

- **Equal Sharing of Total Power for Minimal Losses**

# Efficiency Optimum Phase-Shedding

## ► Maximization of Part-Load Efficiency

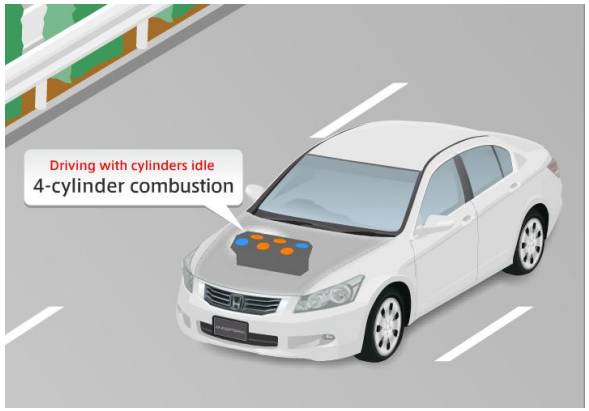
$$\eta\left\{\frac{1}{N}P_{2,sw}\right\} = \eta\left\{\frac{1}{N+1}P_{2,sw}\right\}$$

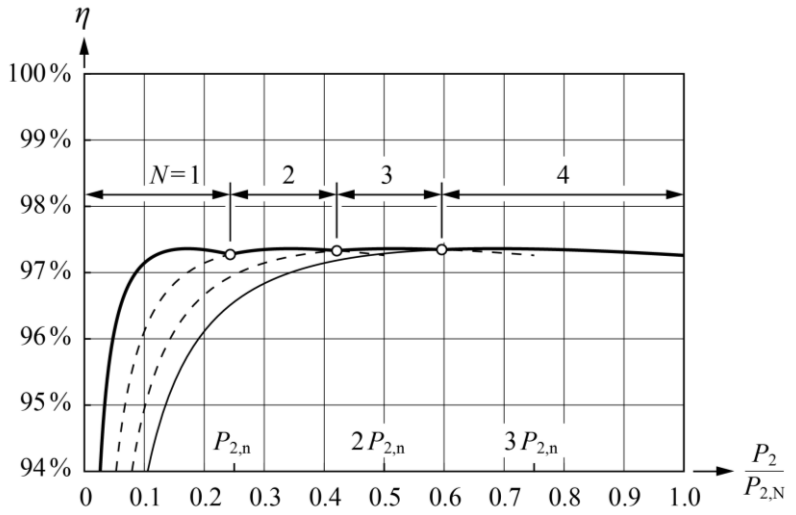


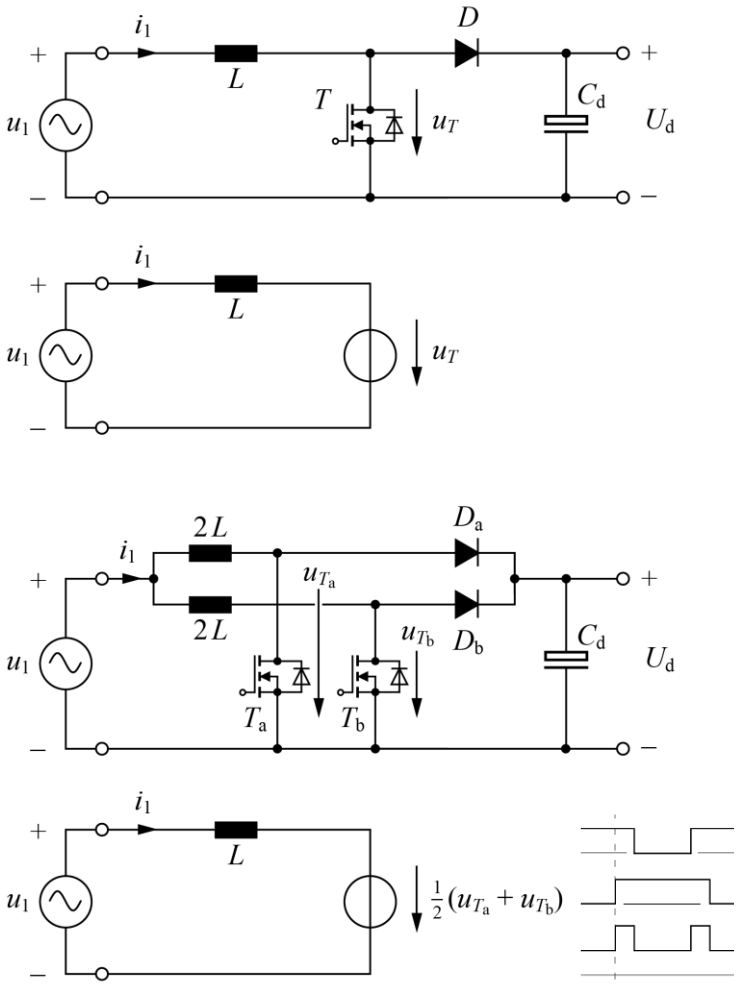
# Efficiency Optimum Phase-Shedding

- **Deactivation of "Cylinders"**



# Ripple Cancellation

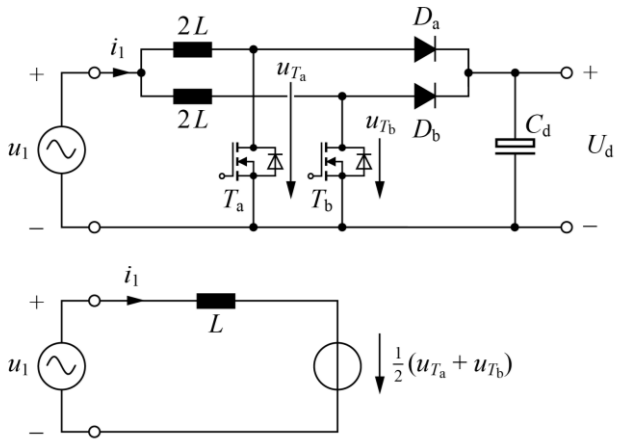


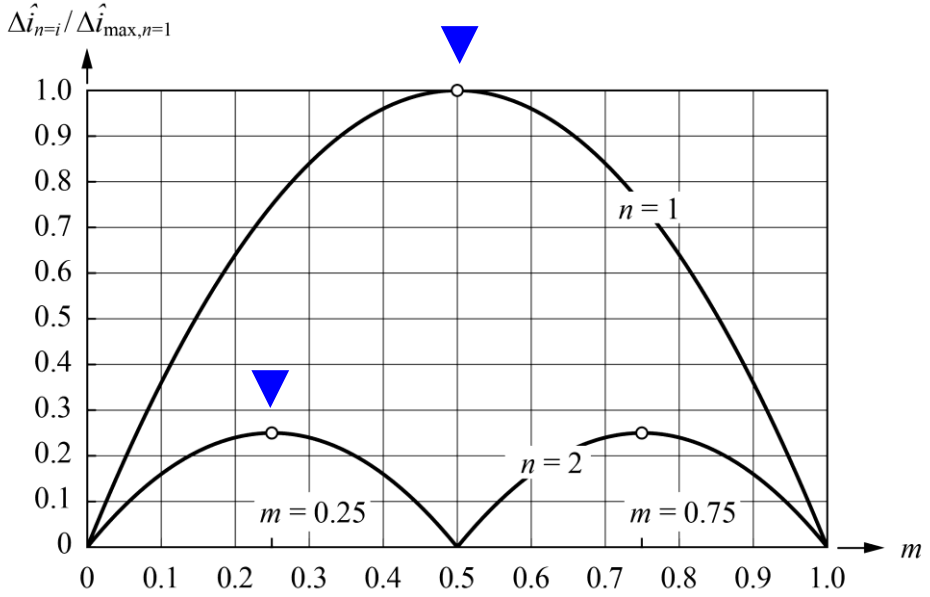

- Operation of $n$ =2 Systems 180° Out of Phase

# Ripple Cancellation

$$\Delta\hat{i}_{\max,n=1} = \frac{U_d}{8 f_P L} \rightarrow \Delta\hat{i}_{\max,n=2} = \frac{U_d}{32 f_P L}$$

**Doubling of Effective Switching Frequ. @ Same Switching Losses**



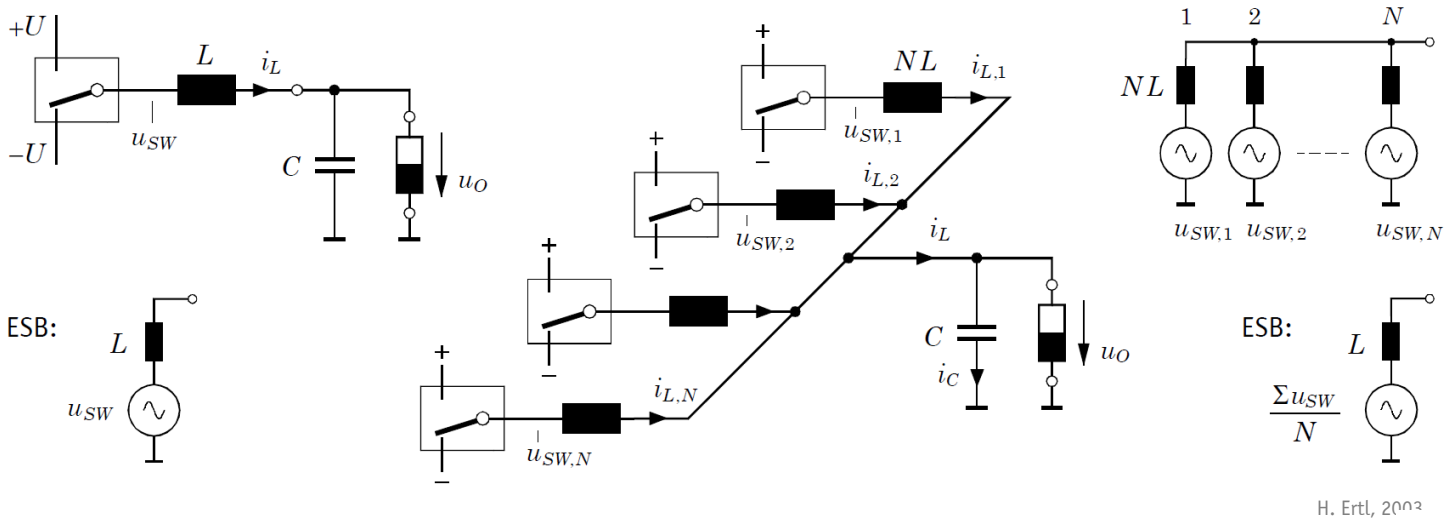

► **Possible Red. of Input Capacitance $C \rightarrow C/8$ –or– Inductance $2L \rightarrow L/4$**

# Scaling Laws of Parallel Interleaving

# ▶ Parallel Interleaving (Homogeneous Power)

- **Characteristics**

— Breaks the Frequency Barrier
— Breaks the Impedance Barrier
— Breaks Cost Barrier - Standardization
— High Part Load Efficiency




H. Ertl, 2003

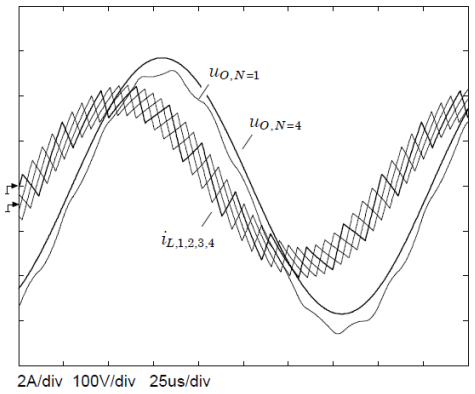
- **Fully Benefits from Digital IC Technology (Improving in Future)**
- **Redundancy → Allows Large Number of Units without Impairing Reliability**

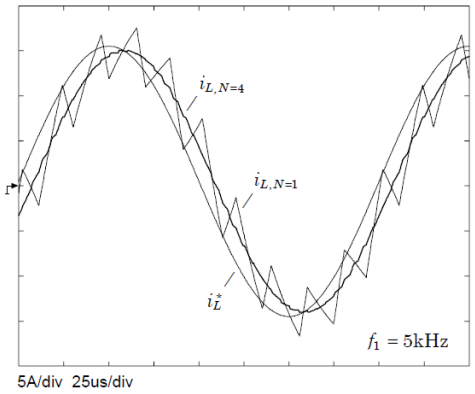
# ▶ Parallel Interleaving (Homogeneous Power)

— Multiplies Frequ. / Red. Ripple @ Same (!) Switching Losses & Incr. Control Dynamics

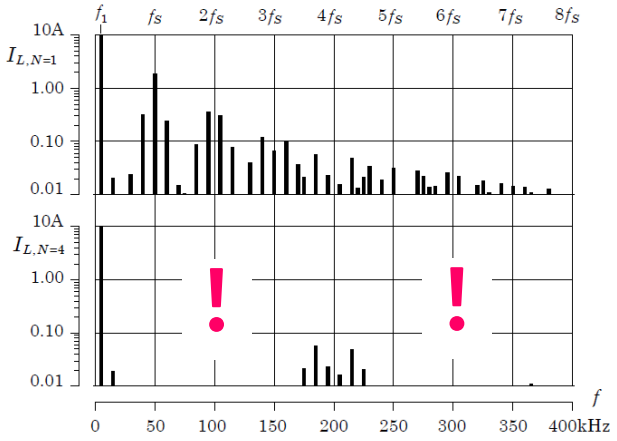
$$\Delta U_{\max,N} = \Delta U_{\max} \cdot \frac{1}{N^3}$$

$$\Delta I_{\max,N} = \frac{\Delta I_{\max}}{N^2}$$




H. Ertl, 2003

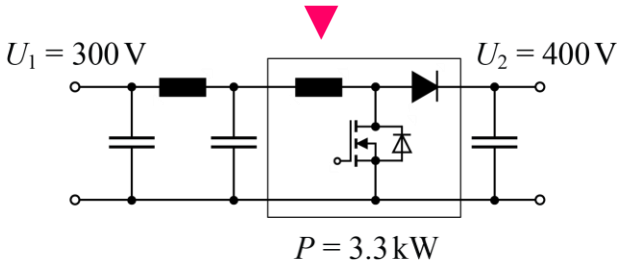


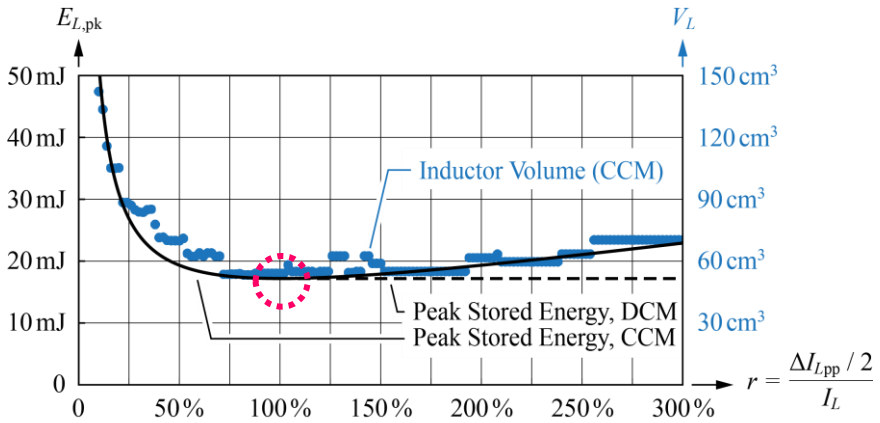

$N = 3$

- Fully Benefits from Digital IC Technology (Improving in Future)
- Redundancy → Allows Large Number of Units without Impairing Reliability

# ▶ Remark #1 Volume of Cell-Inductors

- **Harmonics Cancellation Allows Large ripple of Cell Currents**



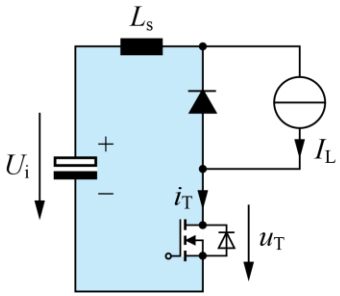

$300\,\mathrm{V} \rightarrow 400\,\mathrm{V}$ @ $3.3\,\mathrm{kW}, f_s = 48\,\mathrm{kHz}$

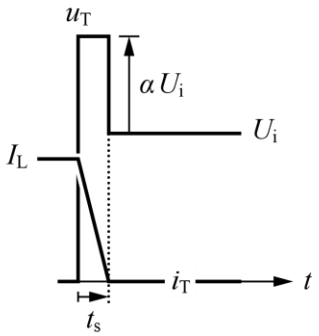
→ **Minimum Volume for 100% Current Ripple (DCM)**

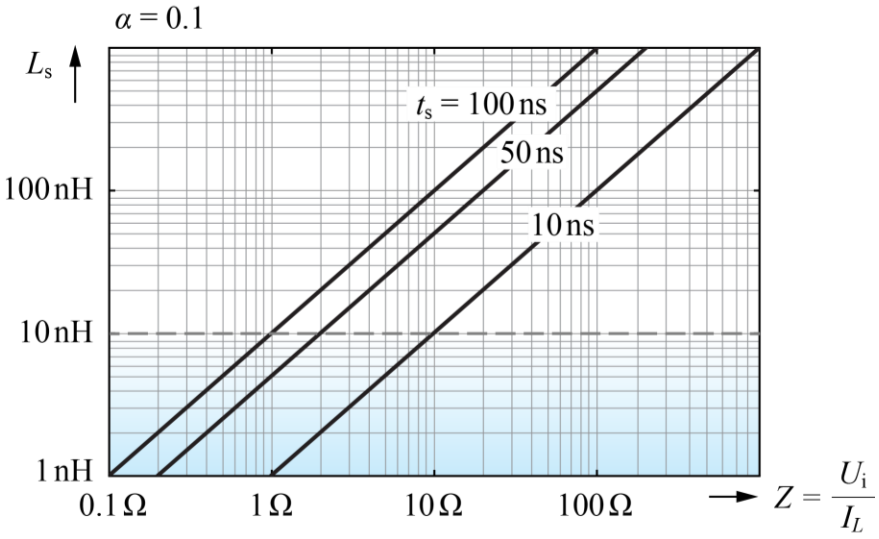
# ▶ Remark #2 Impedance Matching

- Allowed $L_s$ Directly Related to Switching Time $t_s$ →

$$L_s \le \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \frac{U_i}{I_L} \qquad Z$$

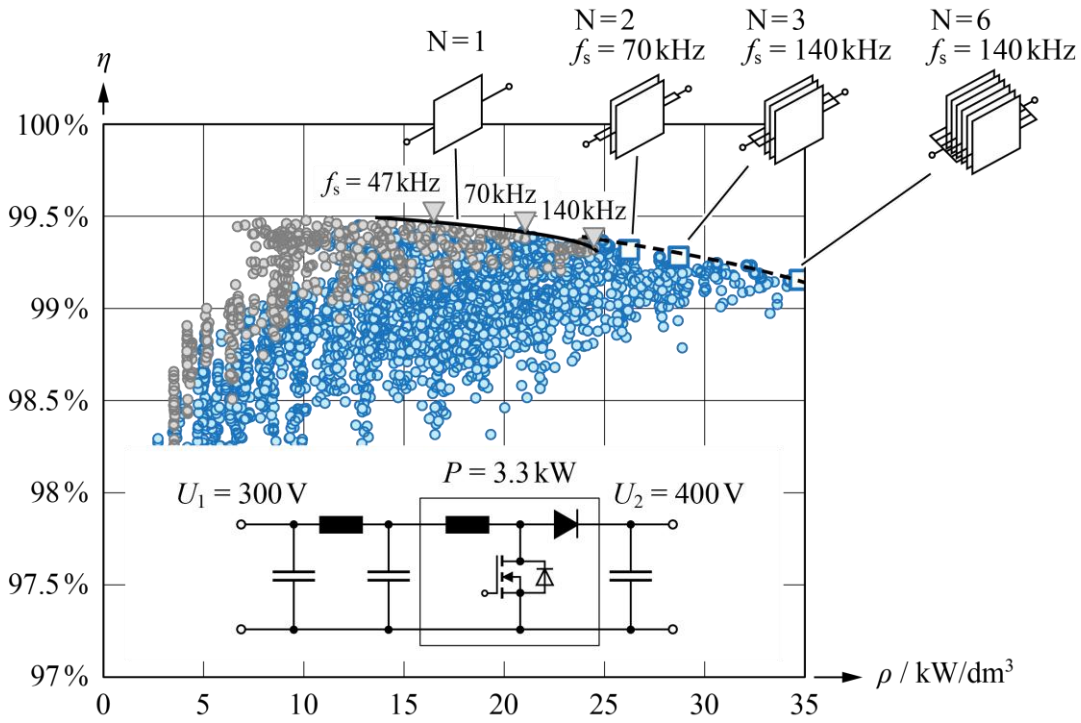



→ Parallel Interl. Allows to Split-Up Large Currents → Increase of $Z$ / Allows Faster Swtchg

# ▶ Remark #3 Efficiency/Power Density (Pareto) Limit

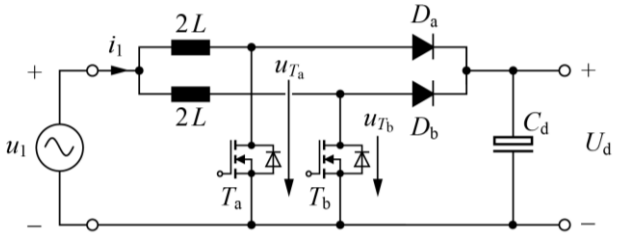


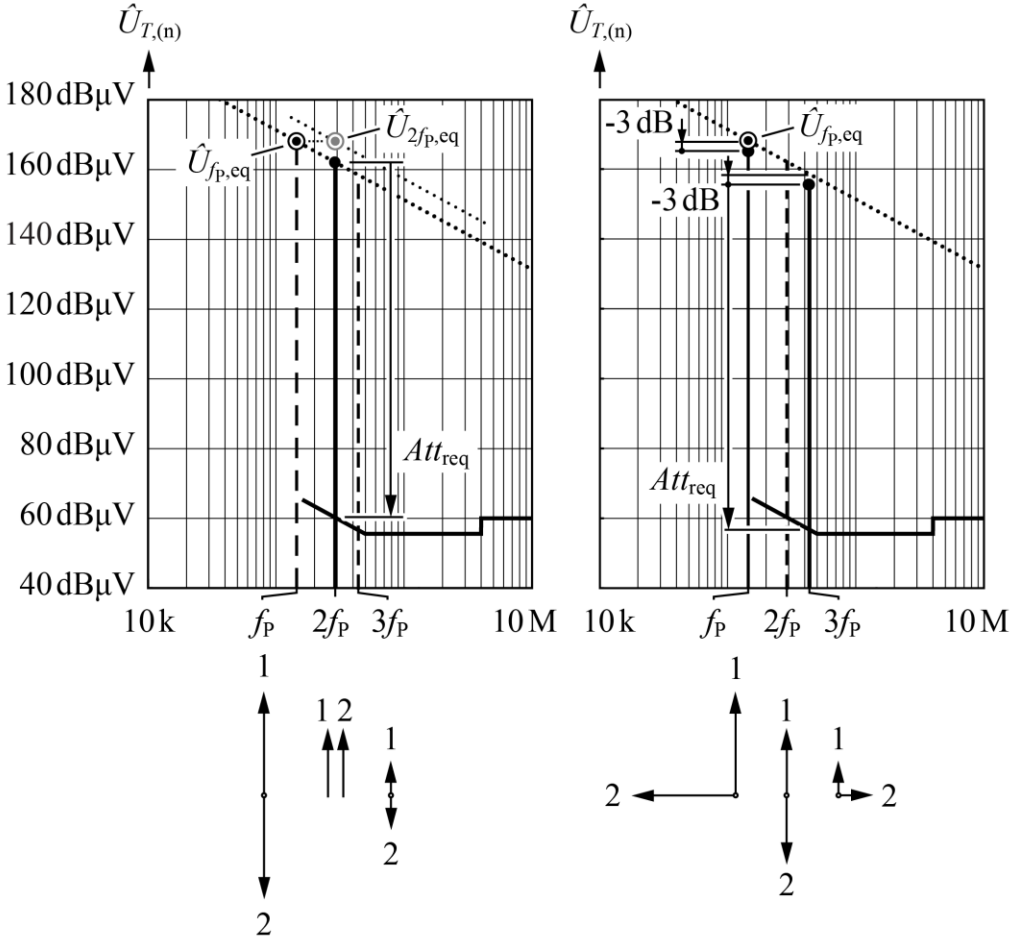

- **Parallel Interleaving - Shift of the Pareto Limit → Higher Power Densities**

# EMI Reduction due to Parallel Interleaving

# Reduction of EMI Filter Volume

- Symm. Interleaving – 180°
- Asymm. Interleaving – 90°



# Measures for Efficiency Improvement

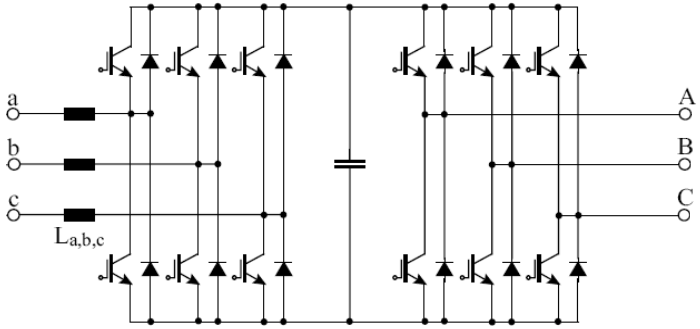
**Topology & Control**

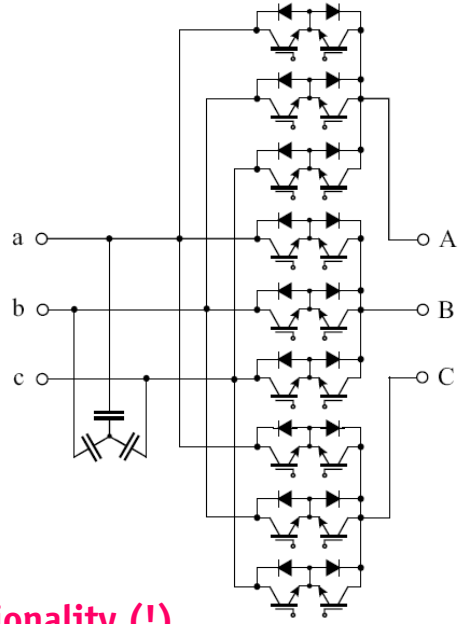
- Single-Stage vs. Two-Stage Conversion
- Synchronous Rectification
- Resonant Transition Mode Switching
- Interleaving

# Single-Stage vs. Two-Stage Conversion

# ▶ Single-Stage → Integration of Functions

— **Examples:**
* **Matrix Converters**
* **Multi-Functional Utilization (Machine as Inductor of DC/DC Conv.)**
* **etc.**

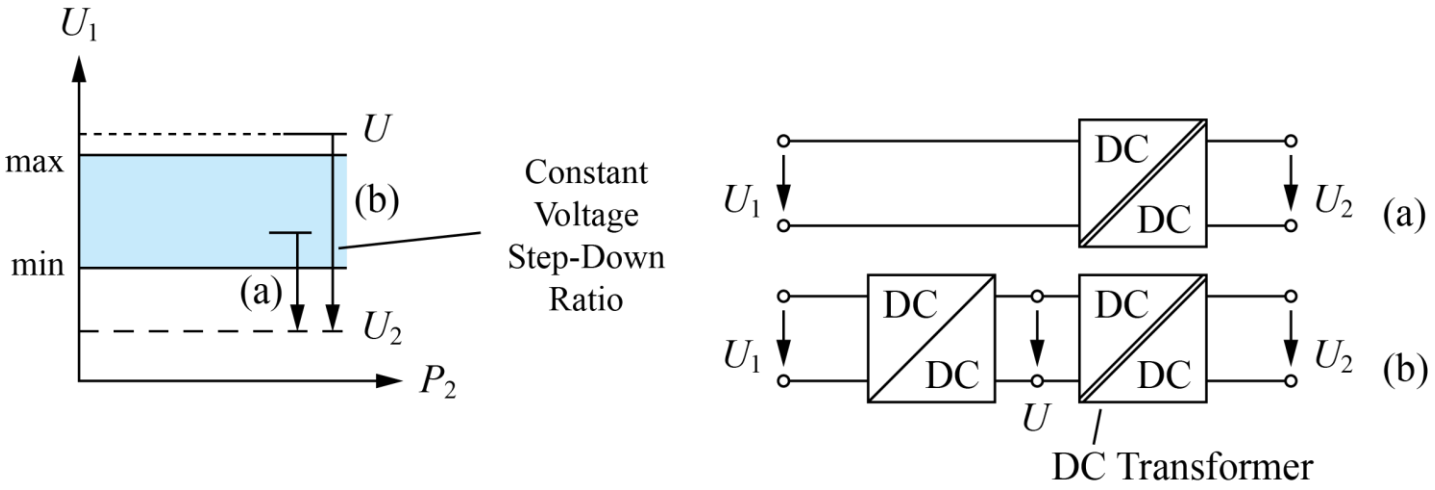



- **Integration Restricts Controllability / Overall Functionality (!)**
- **Typ. Lower Efficiency / Higher Control Compl. of Integr. Solution**
- **Basic Physical Properties remain Unchanged (e.g. Filtering Effort)**

# ▶ Two-Stage → Optimal Splitting of Functionality

- Highly Optimized Specific Functionality → High Performance for Specific Task
- Restriction of Functionality → Lower Costs

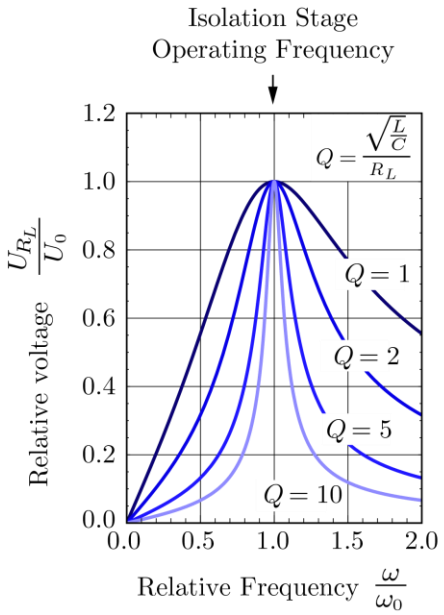


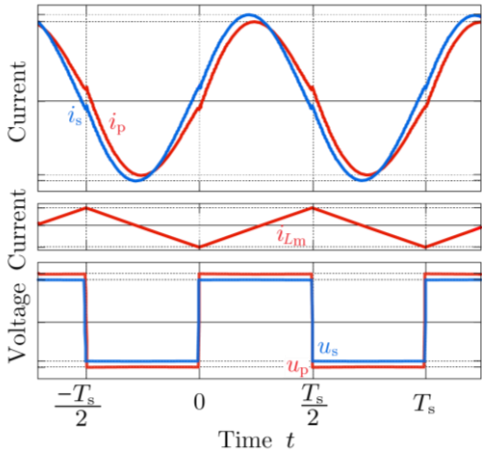

- Example of Wide Input Voltage Range Isolated DC/DC Converter

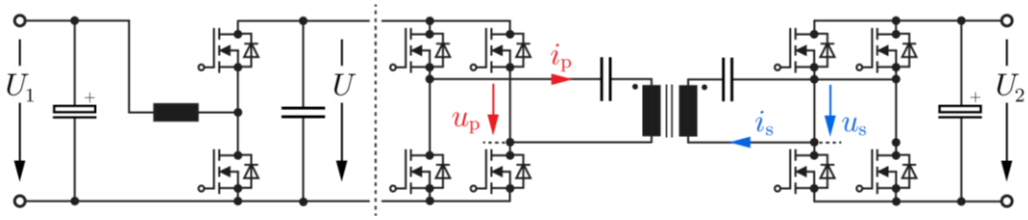
# ▶ Two-Stage → Optimal Splitting of Functionality

— **Example:** DC-Transformer → Isolation @ Constant (Load Ind.) Voltage Transfer Ratio

E.g. adopted by VICOR – "Sine Amplitude Converter" for Fact. Power Architecture → Very High Efficiency



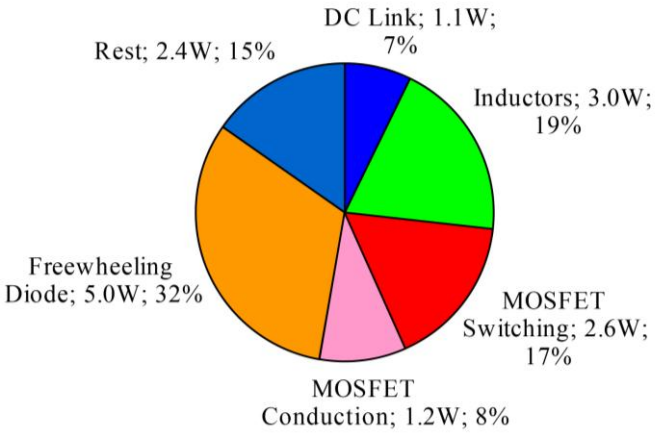



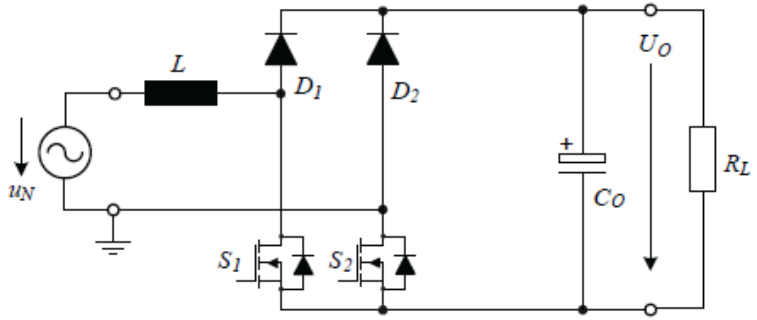

■ Resonant Frequ. ≈ Switching Frequ. → Input/Output Voltage Ratio = $N_1/N_2$

# Resonant Transition Mode

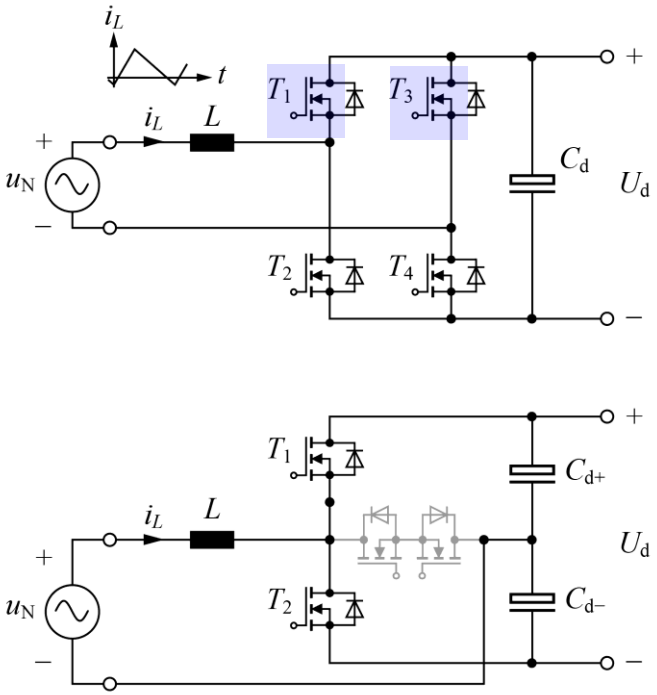
# Technological Limits of Hard-Switched CCM Converters

- On-State Voltage of Freewheeling Diodes ($U_F$)
- Capacitive Switching Losses of MOSFETs ($A_{Si,opt}$)



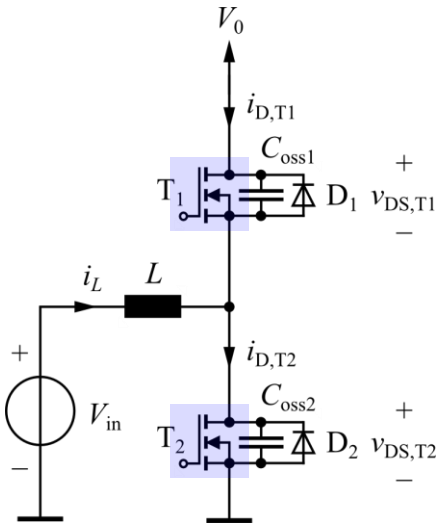
# Zero Voltage Switching – Triangular Current Mode (TCM) Operation

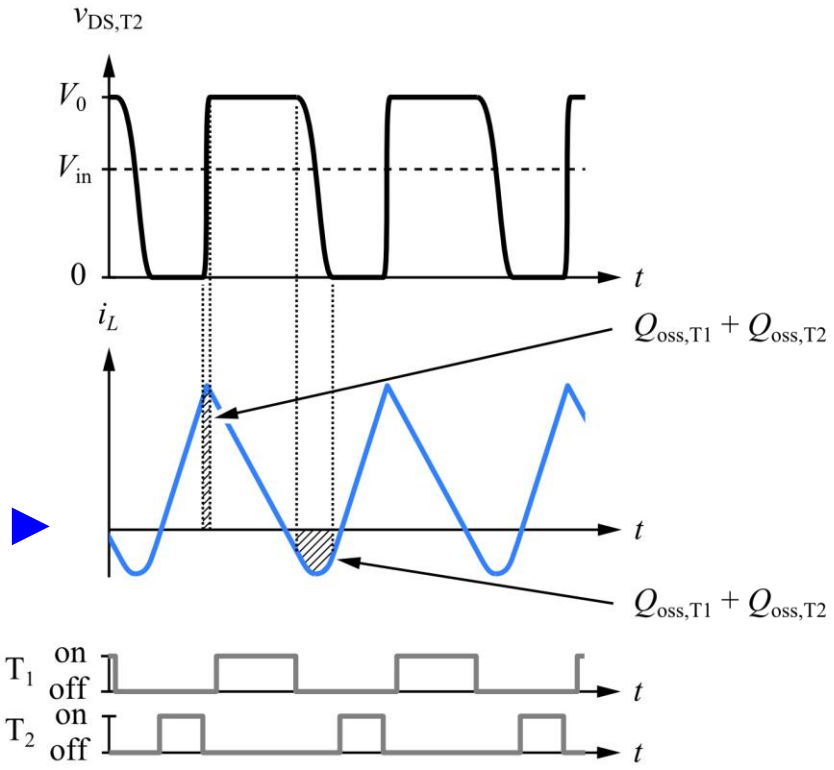



- Synchronous Rectification
- Negative Current Ensures ZVS

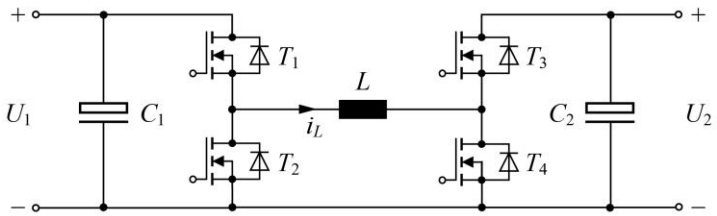
# Zero Voltage Switching – Triangular Current Mode (TCM) Operation

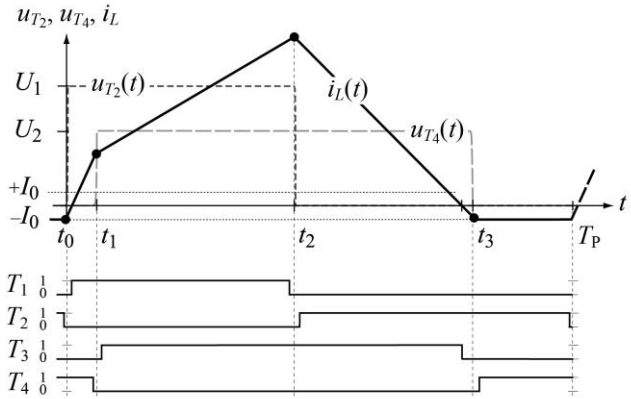
- Synchronous Rectification
- Negative Current Ensures ZVS



# 12kW TCM Buck+Boost DC/DC Converter




- **Overlapping Input and Output Voltage Ranges**

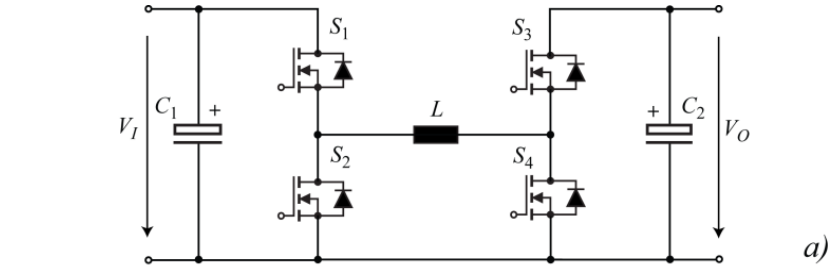
  $U_1$=150...450V
  $U_2$=150...450V

- **Max. Eff. = 99.3% @ 30kW/l**

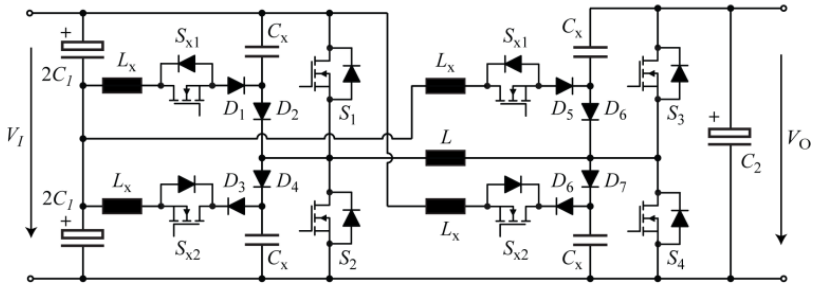
# "Snubbers" vs. TCM

— Non-Isolated Buck+Boost DC-DC Converter for Automotive Applications

99.3% Efficiency
30 kW/dm³

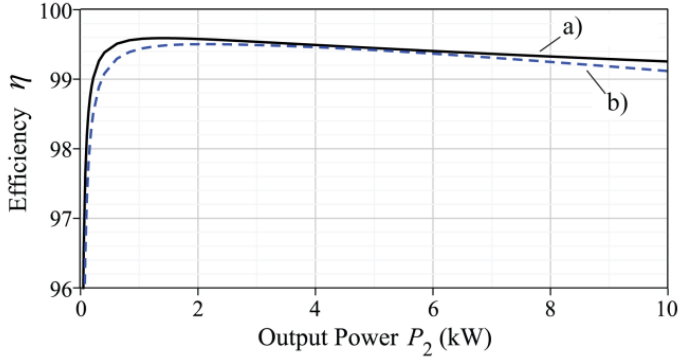



a)




b)

■ Instead of Adding Aux. Circuits
Change Operation of BASIC (!) Structure
"Natural" Performance Limit



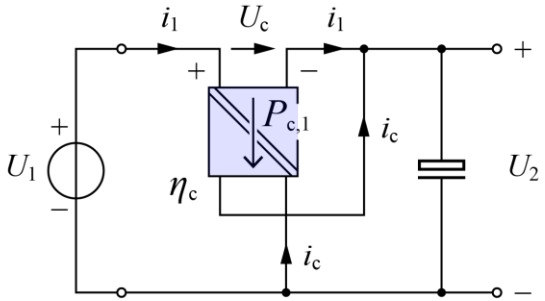
# Measures for Efficiency Improvement

**Further Concepts**

- Partial Power Conversion
- Ride-Through Boost Converter
- Series/Parallel Rearrangement

# Partial Power

# Partial Power Converter



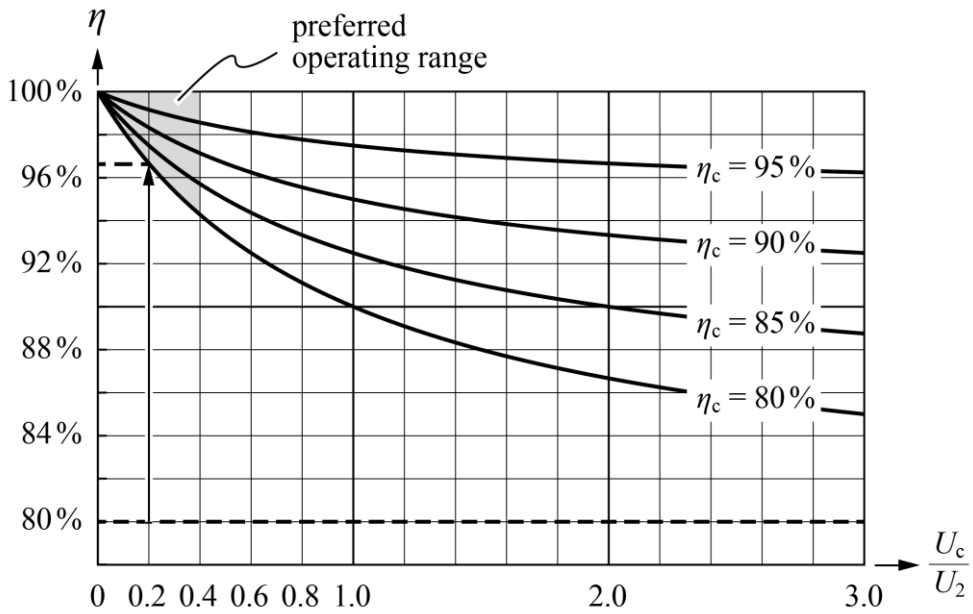

$$U_2 = U_1 - U_c$$

- **Reduces Rated Power of PPC**

$$p_c = \frac{P_{c,1}}{P_1} = \frac{\frac{U_c}{U_2}}{1+\frac{U_c}{U_2}}$$

- **Limited Influence of PPC Efficiency on Total Efficiency**

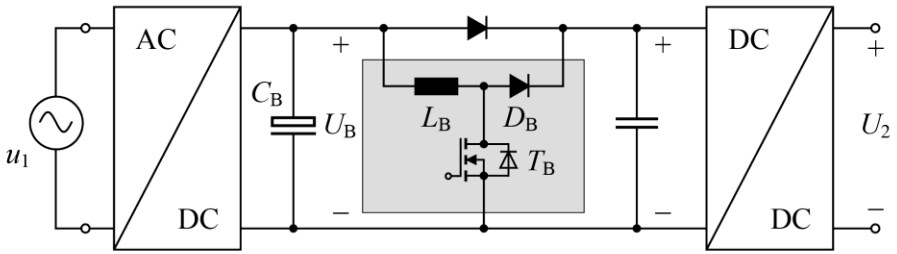
$$\eta = \frac{P_2}{P_1} = \frac{(1+\frac{U_c}{U_2}\eta_c)}{(1+\frac{U_c}{U_2})}$$



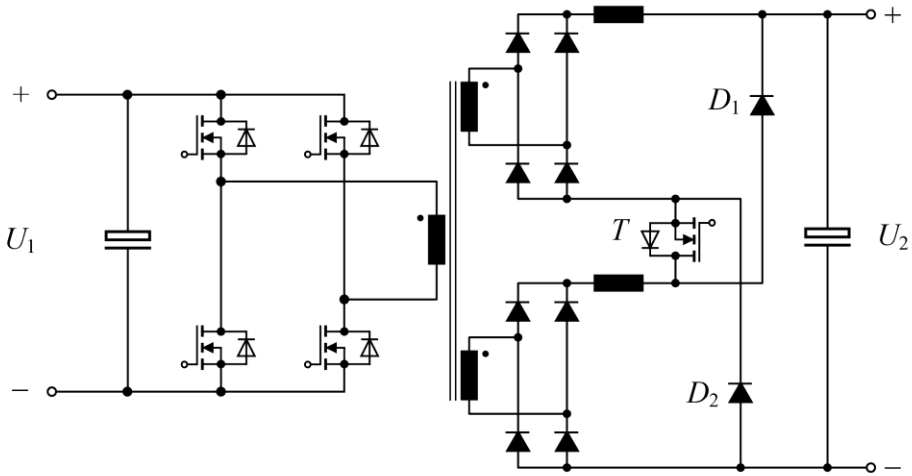
# Voltage / Topology Preconditioning

# ▶ Voltage / Topology Preconditioning

- ▶ Ride-Through Boost Converter




- ▶ Series-Parallel Reconfiguration (Voltage:2 AND Current x2 → Advantage Comp. to Multi-Level Conv.)

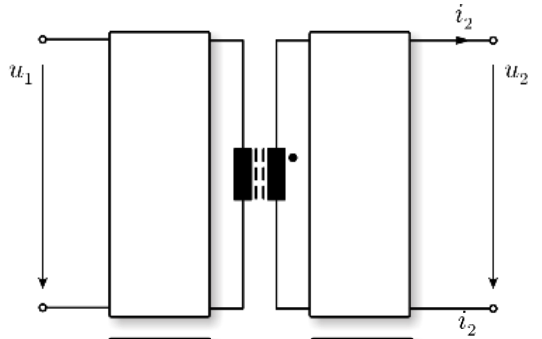



- ■ S/P Reconfiguration also Applicable for 3-Phase System (Star → Delta Rearrangement)

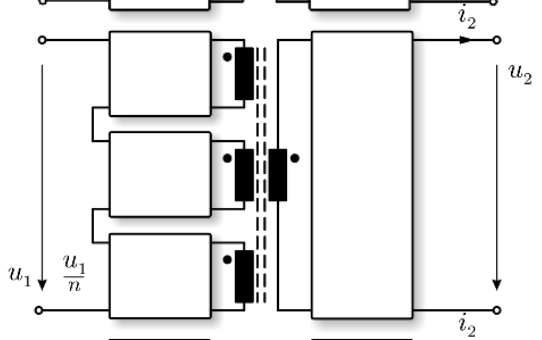
# Mixed Interleaving

- Numerous Combinations (ISOP, ISIS, IPOS, IPOP, etc.)

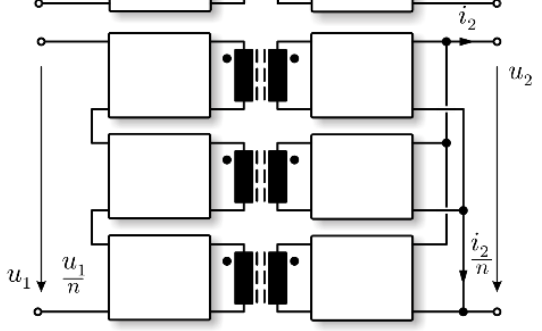
* Conventional




* Input Series




* ISOP = Input Series / Output Parallel Topology




- Low Inp. Voltage / Output Curr. Harmonics
- Low Input / Output Filter Requirement
- Impedance Matching

# Highly Accurate Efficiency Measurement

**Concepts**

- Power Analyzer
- Calorimeter

# Power Analyzer

# Maximum Admissible Power Measurement Error

- **Admissible Error of Loss Determination *NOT* Efficiency Determination**

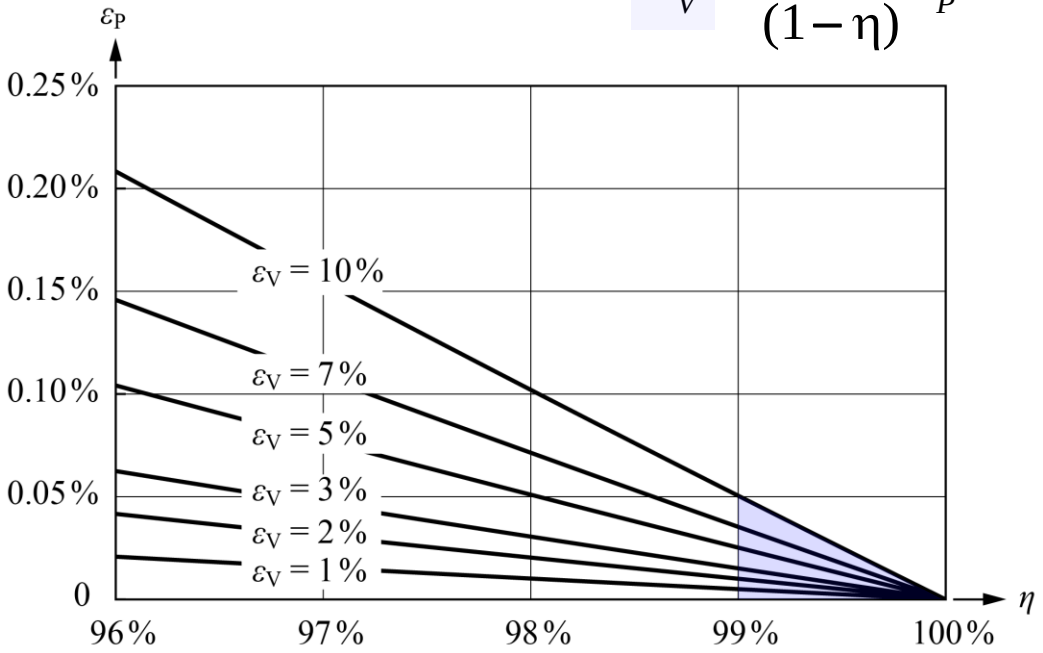
$$\eta = \frac{P_2}{P_1}$$

$$\varepsilon_\eta = 2\varepsilon_P$$

$$\eta = (1 - \frac{P_V}{P_1})$$

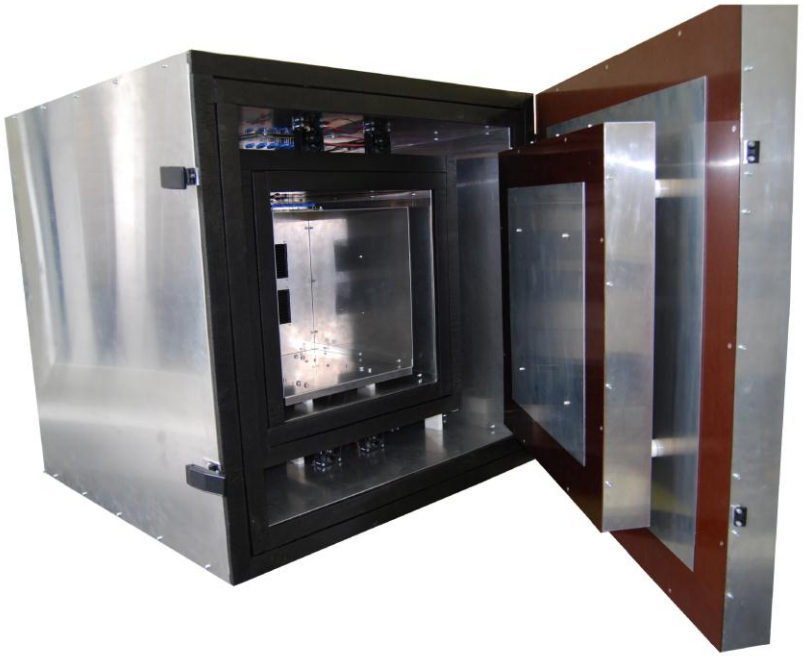
$$\varepsilon_\eta = \varepsilon_V \frac{(1-\eta)}{\eta}$$

$$\varepsilon_V = \frac{2\eta}{(1-\eta)} \varepsilon_P$$



# Calorimeter

# Two-Chamber Calorimeter



- Measurements up to 85°C Ambient Temp.
- Relative Error of Loss Measurements < 3.5%@10W
  < 1.0%@100W
  < 0.5%@200W

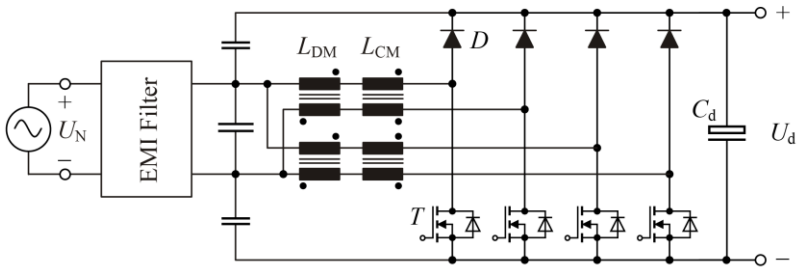
# Ultra-High Efficiency Converters

**Concepts @ 3.3kW**

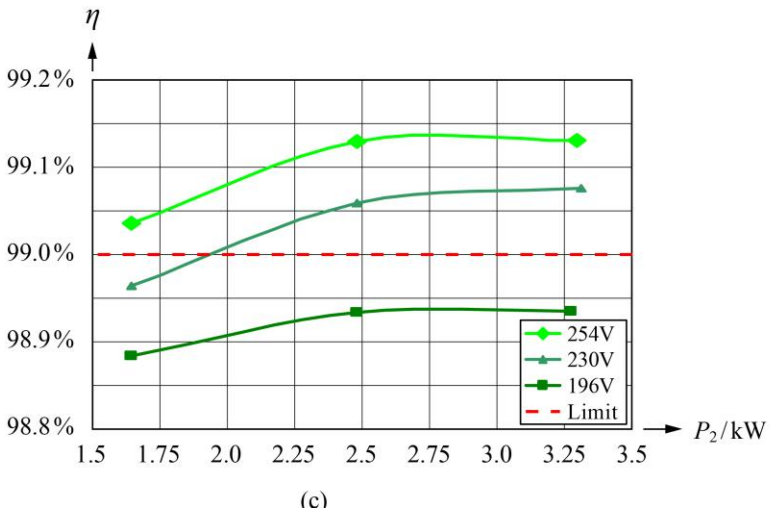
- 2x Interleaved CCM Bridgeless PFC Rectifier
- 6x Interleaved TCM PFC Rectifier
- Telecom Rectifier Module


Research Projects of ETH Zurich Partly Supported by the European Center for Power Electronics

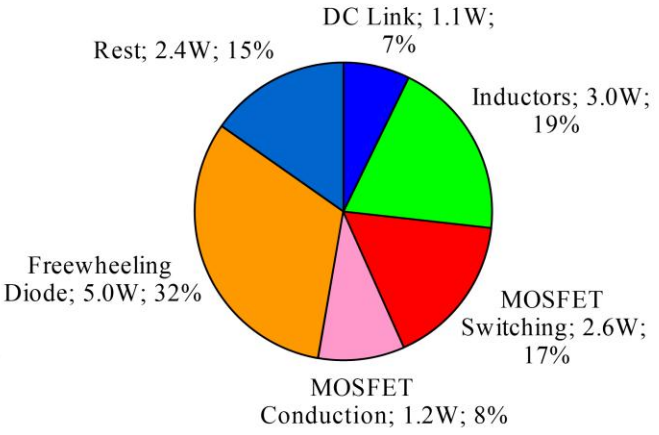
# 3.3kW CCM PFC Rectifier System




(b)

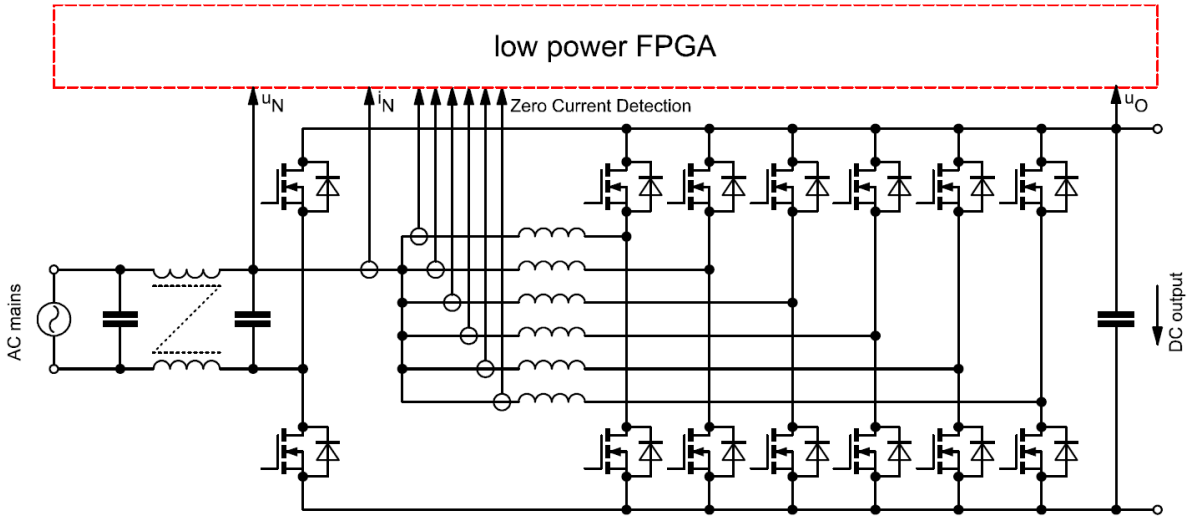



(c)



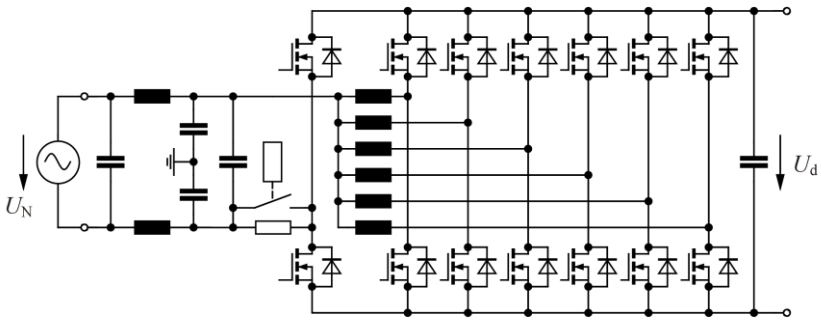
# 3.3kW TCM PFC Rectifier System

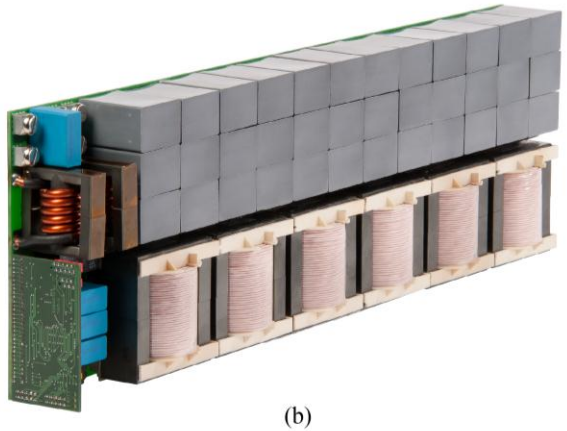
★ 99.36% @ 1.2kW/dm³



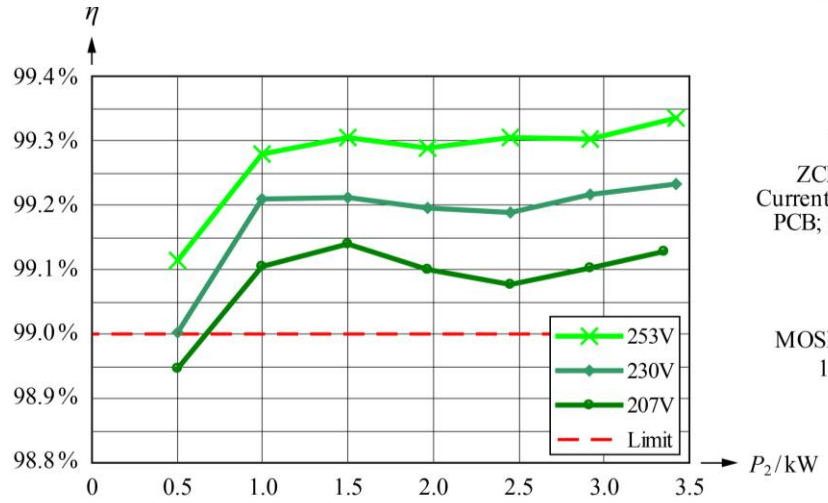

- Bidirectional – Supports V2G Concepts
- Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

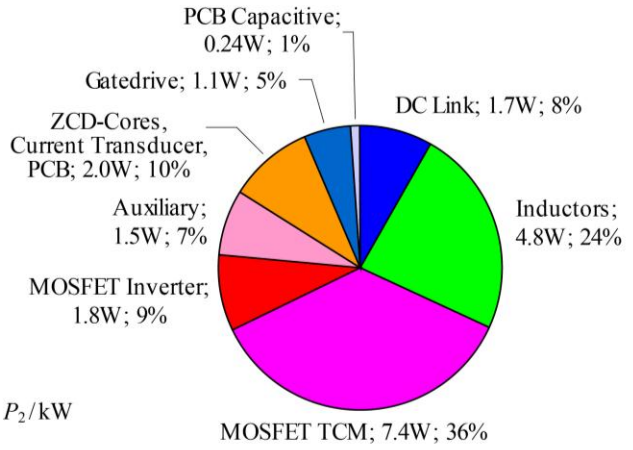
# 3.3kW TCM PFC Rectifier System



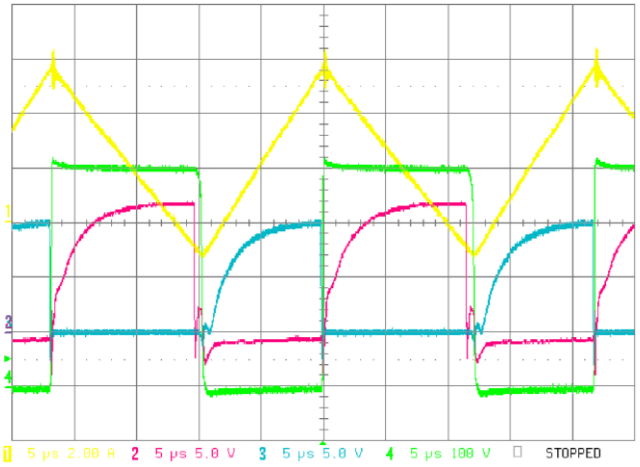
(b)

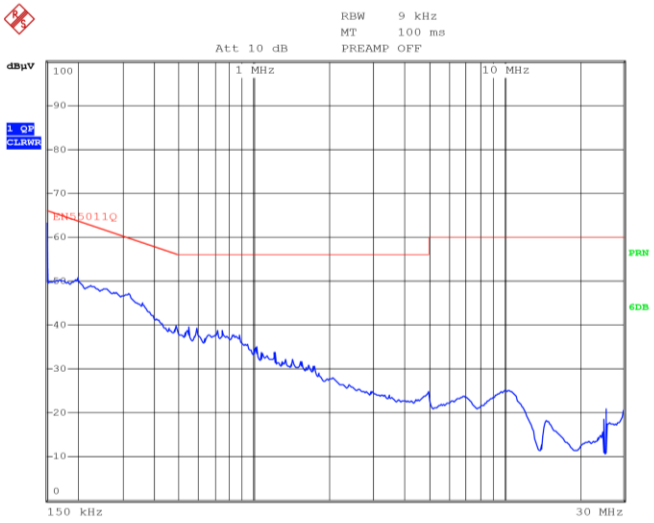


# 3.3kW TCM PFC Rectifier System

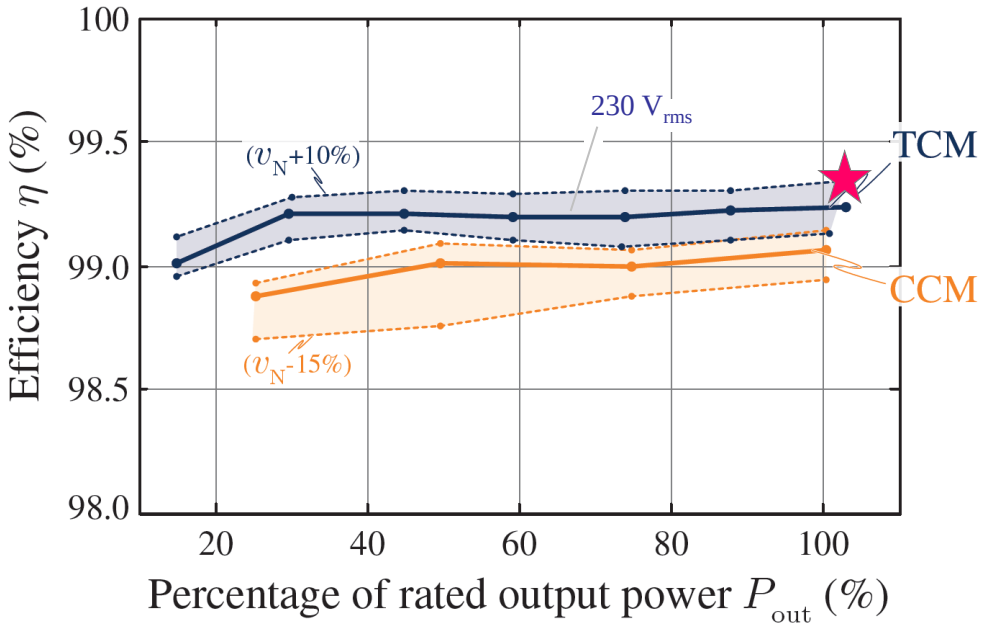
## ▶ Measurement Results



# 3.3kW TCM PFC Rectifier System

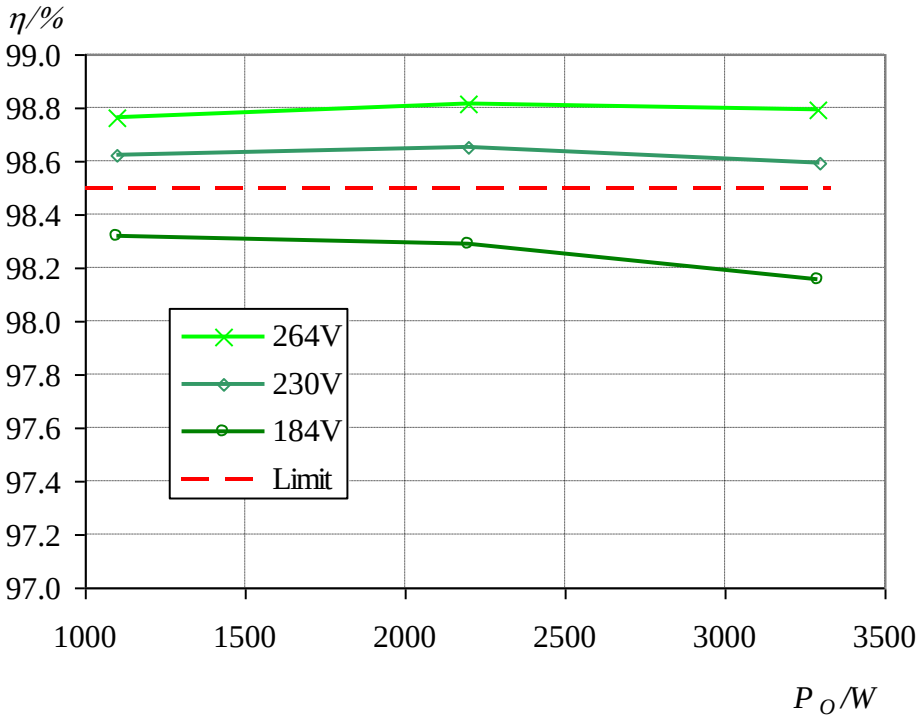
★ 99.36% @ 1.2kW/dm³




► Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

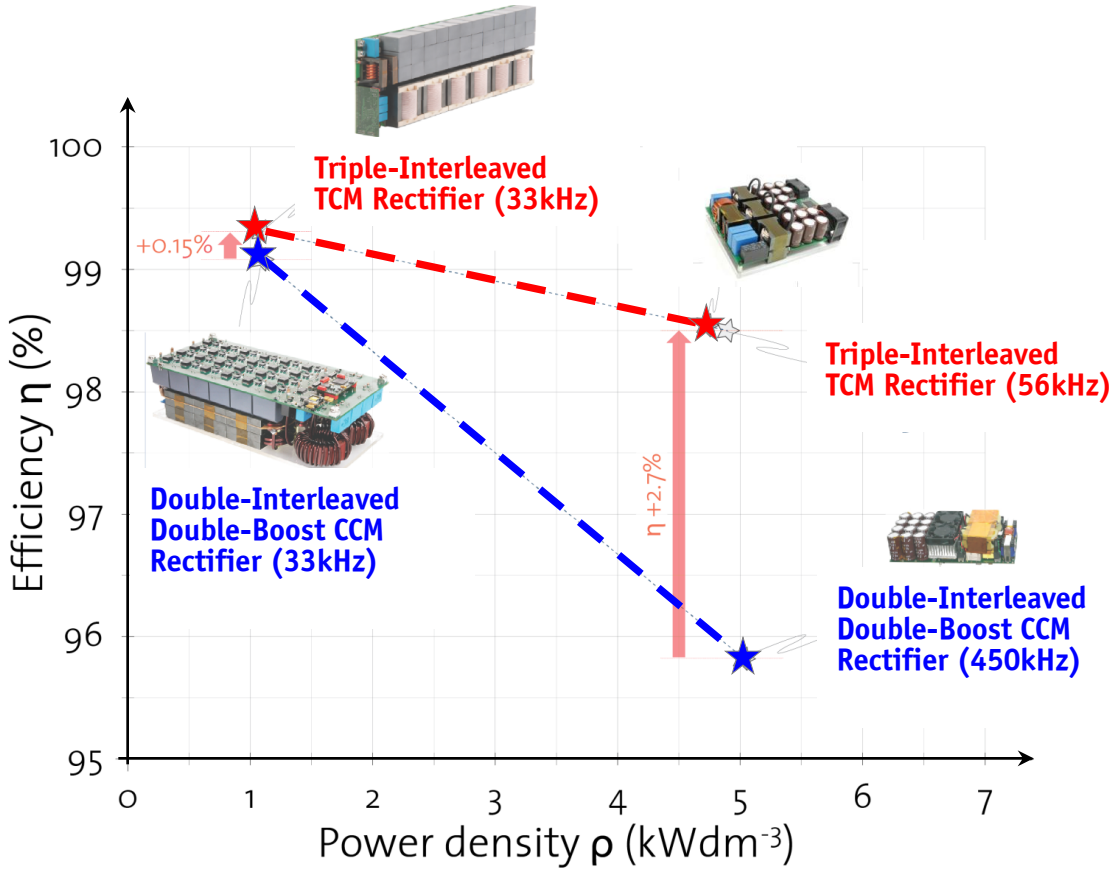
# Ultra-Compact/Efficient TCM PFC Rectifier System

- Input Voltage $184...264V_{AC}$
- Output Voltage $420V_{DC}$
- Rated Power $3.3kW$




★ 98.6% @ 4.5kW/dm³

# Converter Performance Evaluation Based on η-ρ-Pareto Front



# KEYS for Achieving the Performance Improvement

- Only Basic Topology Employed
- ZVS Achieved by Only Modifying Operation Mode
- Active ZVS
- Triangular Current Mode (TCM)
- Variable Switching Frequency
- No Diode On-State Voltage Drop
- Continuously Guided u, i Waveforms
- Interleaving
- Utilization of Low Superjunct. $R_{DS,(on)}$
- Utilization of Digital Signal Processing

… despite Using "Old" Si Technology

- Low Complexity
- No Aux. Circuits
- No (Low) Switching Losses
- No Direct Limit of # of Parallel Trans.
- Simple Symm. of Loading of Modules
- No Current Sensor (only i=0 Detection)
- Spread & Lower Ampl. EMI Noise
- Synchr. Rectification
- No Free Ringing → Low EMI Filter Vol.
- Low EMI Filter Vol. & Cap. Curr. Stress
- Low Cond. Losses despite TCM
- Low Control Effort despite 6x Interl.

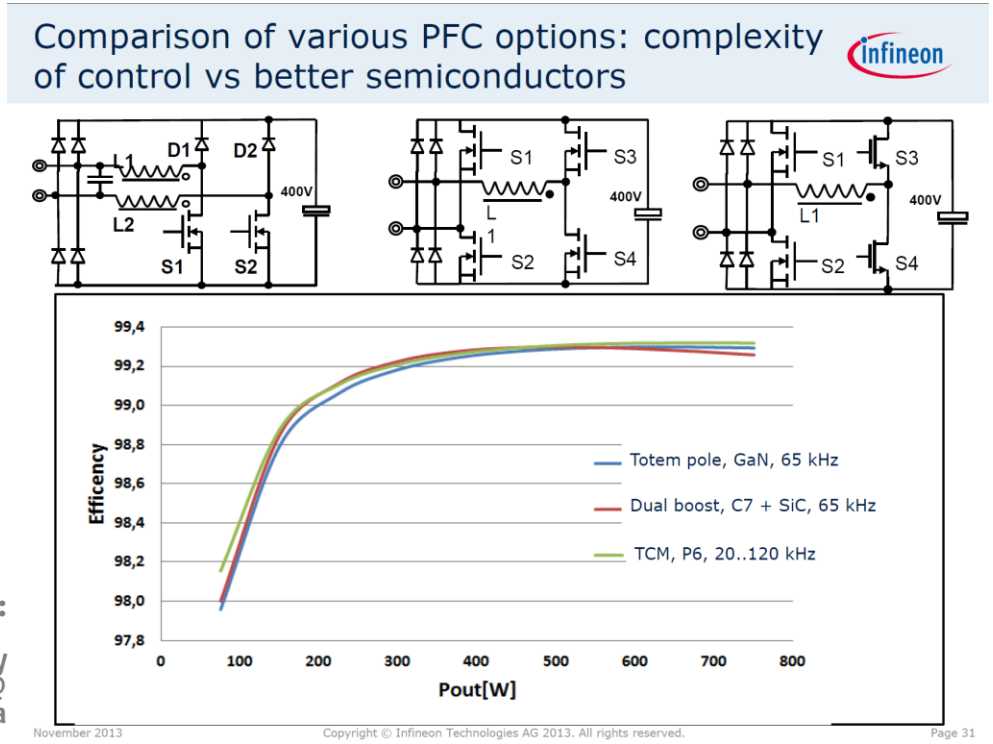
… the Basic Concept is Known since 1989 (!)

# Alternative Converter Concepts (?)

- Indication for a "Natural" Performance Limit

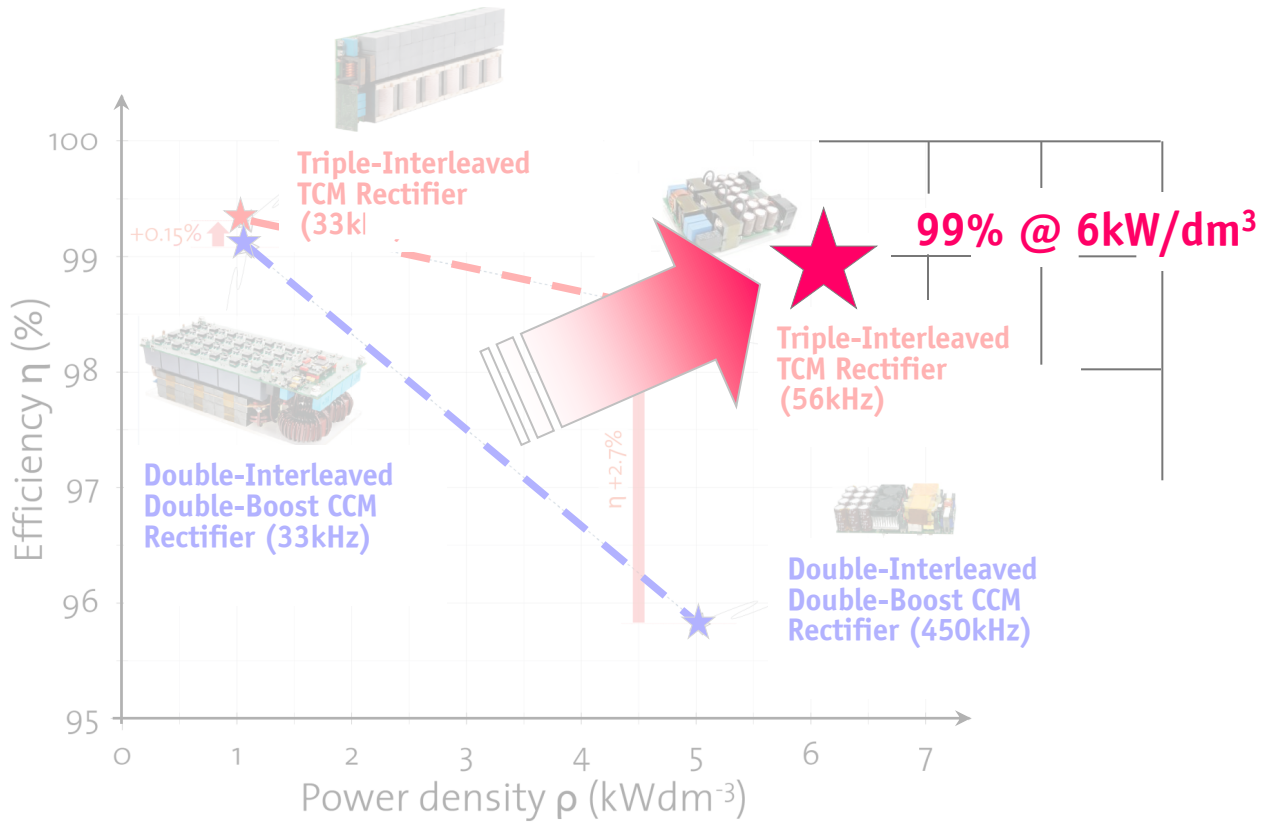
Source:

Dr. Gerald Deboy
Plenary Presentation @
IECON 2013, Vienna




- Minimum Performance Difference for Best Matching of Topology/Semicond./Modulation
- Only Use BASIC Topologies - Costs are THE Deciding Criteria (!)

# Is Another Step of Massive Improvement Possible ?



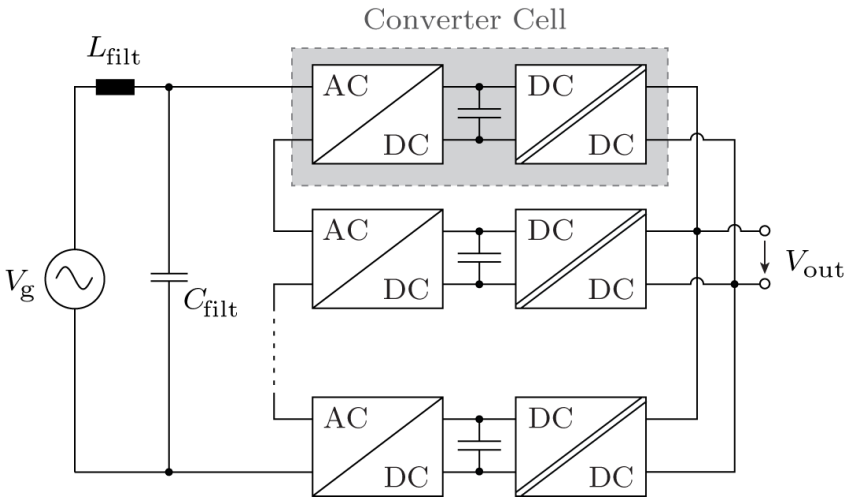
# Multi-Cell Approach

→ Series Interleaving

# Telecom Rectifier Employing Series Multi-Cell Approach

- **Specifications**

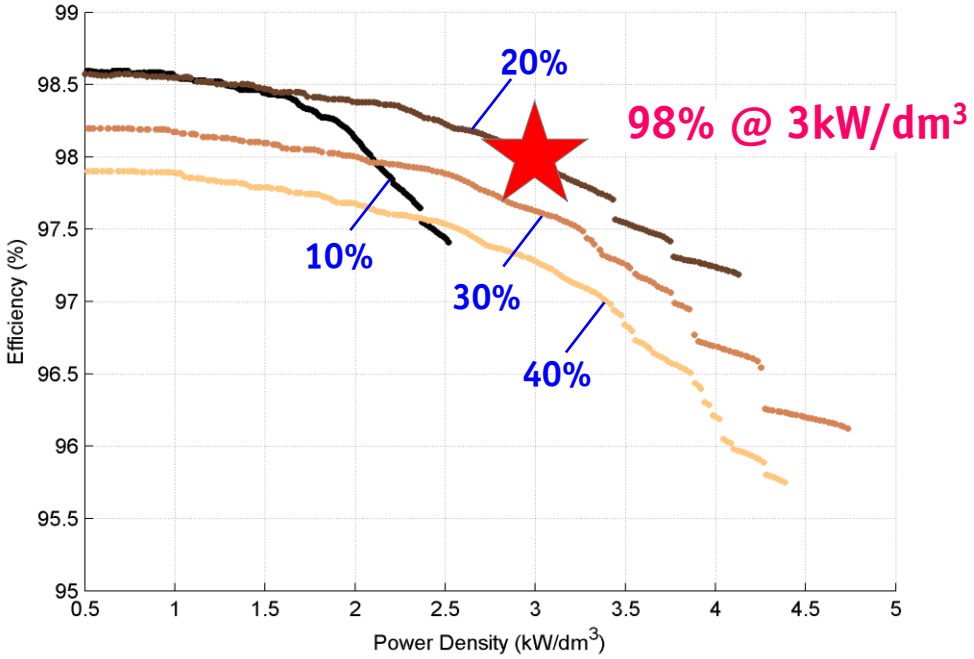
| | |
|---|---|
| Input Voltage | 230 $V_{rms}$ (180 $V_{rms}$ – 270 $V_{rms}$) |
| Nominal Output Voltage | 48 $V_{DC}$ |
| Output Voltage Range | 40-60 $V_{DC}$ |
| Rated Power | 3.3 kW |
| Target Efficiency | 98.5% |
| Target Power Density | 3 kW/dm$^3$ |
| Hold-Up Time | 10ms at Rated Power |
| Switching Frequency | ≥20 kHz (per Module) |
| EMI Standard | CISPR Class A and Class B |




- **Input Series Output Parallel (ISOP) Connection**

# First Optimization Results

- Calculation of Opt. Maximum Admissible DC-Link Voltage Drop during Hold-Up Time (10ms)
- Pareto-Optimal for $N = 6$ Cells (PFC Rectifier + Phase-Shift Full-Bridge)

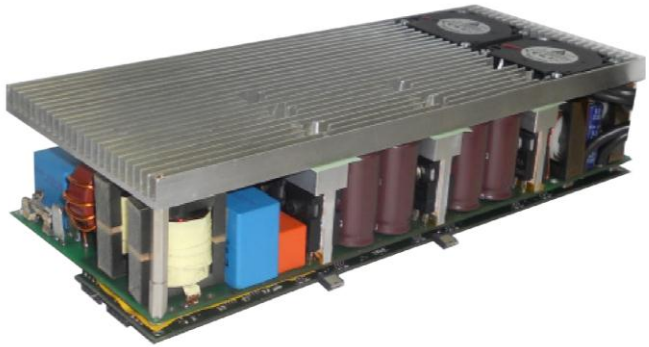


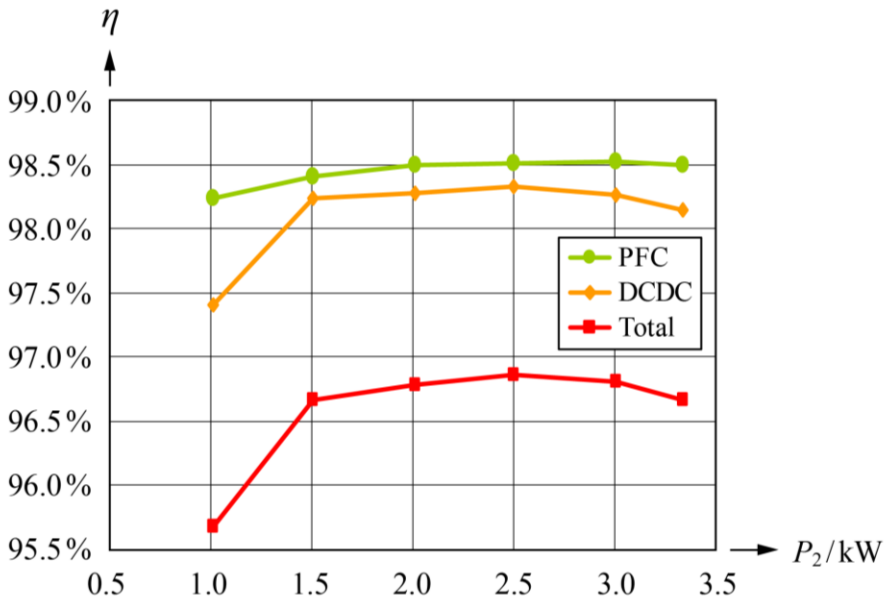

- Optimal Performance for 20% Hold-up DC-Link Voltage Drop

# "Conventional" 3.3kW Telecom Rectifier Module

- 3x Interleaved TCM PFC Rectifier Stages
- Full-Bridge Phase-Shift DC/DC Converter / Full Bridge Synchr. Rectifier

★ 96.8% @ 2.5kW/dm³

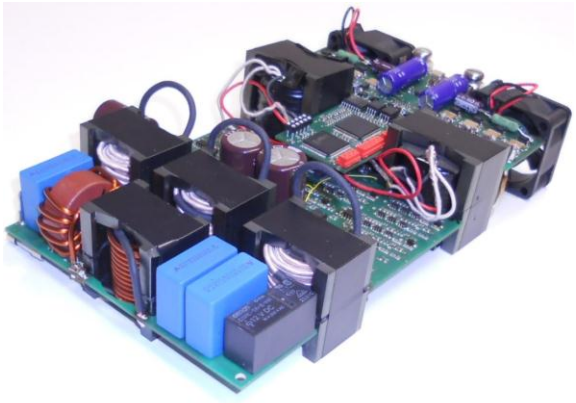


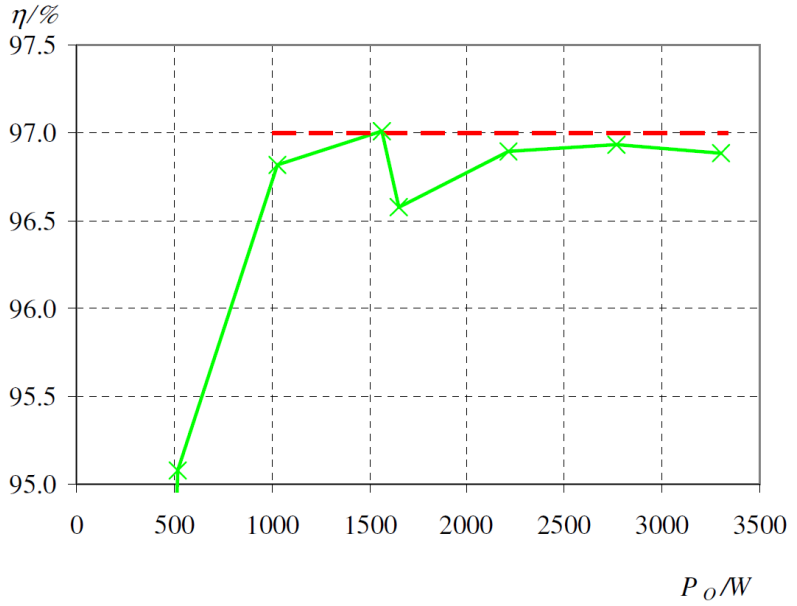


# Next Gen. "Conventional" 3.3kW Telecom Rectifier Module

- 3x Interleaved TCM PFC Rectifier Stages
- 2x Interleaved Full-Bridge Phase-Shift DC/DC Conv. / Full-Bridge Synchr. Rectifier

★ 97% @ 3.3kW/dm³





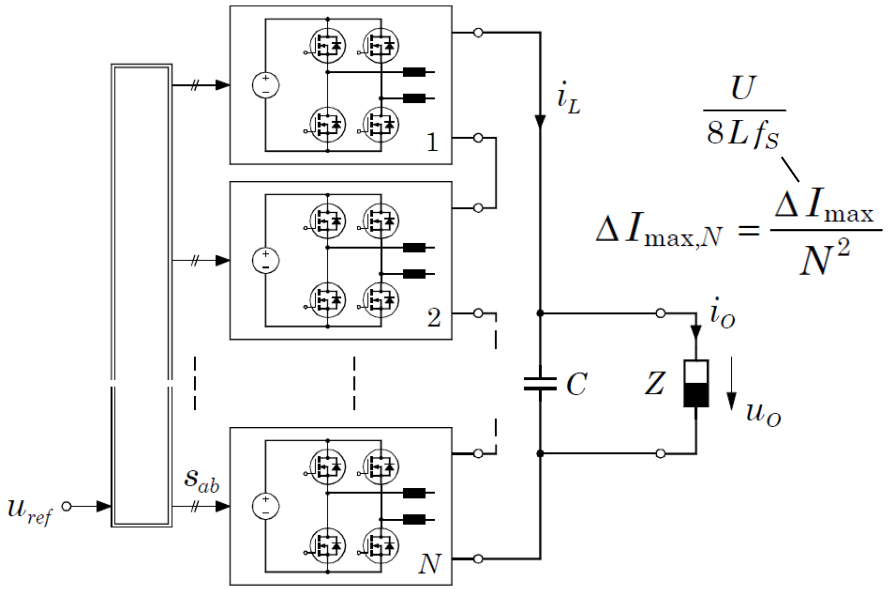
# Scaling Laws of Series Interleaving

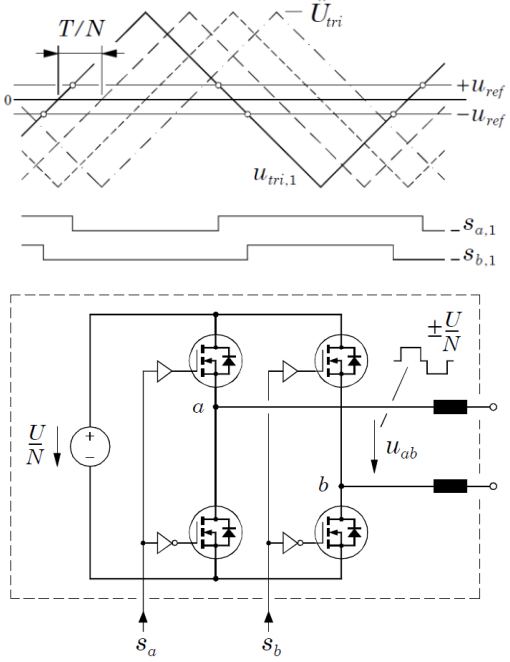
# Series Interleaving of Converter Cells

- **Characteristics**

$$\frac{\Delta U_{\max,N}}{U} = \frac{\pi^2}{32}\left[\frac{f_0}{f_S}\right]^2 \cdot \frac{1}{N^3}$$

— Breaks the Frequency Barrier
— Breaks the Silicon Limit 1+1=2 NOT 4 (!)
— Breaks Cost Barrier - Standardization
— Extends LV Technology to HV



# Series Interleaving of Converter Cells

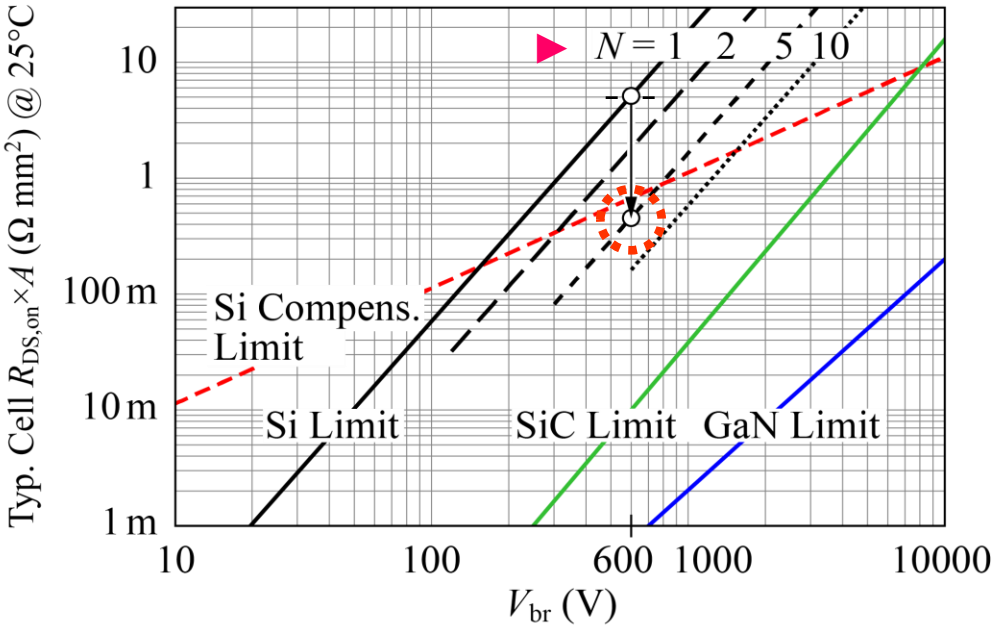
- **Series Interleaving of LV MOSFETs (LV Cells) Effectively *SHIFTS the Si-Limit* (!)**

Assumption:

Chip Area of each LV Chip Equal to the Chip Area of the HV Chip

- **Scaling of Specific On-State Resistance**

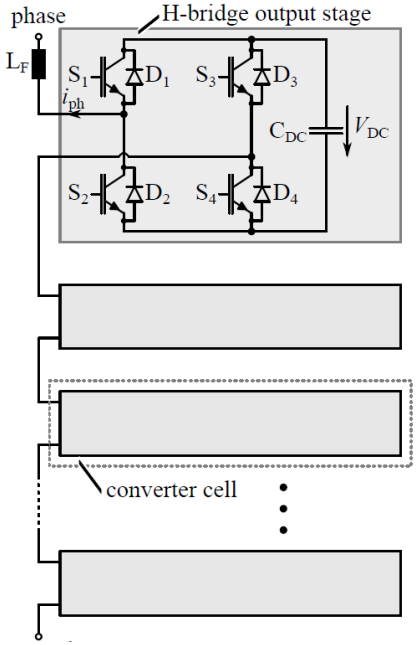
$$(R_{\mathrm{DS,on}} \times A)_{\mathrm{eff}} \approx \frac{1}{N^{1.5}} (R_{\mathrm{DS,on}} \times A)$$

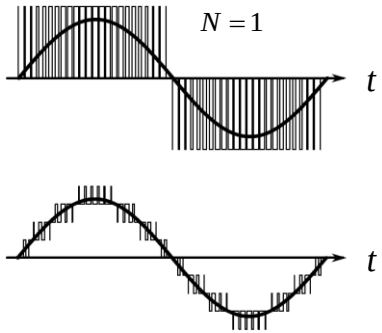


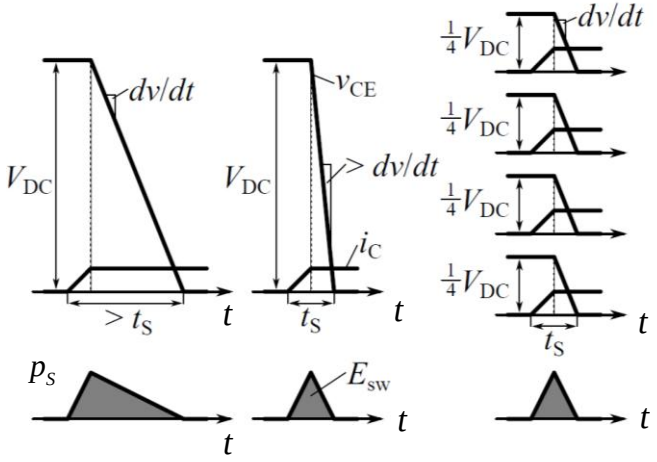

- **Excellent Opportunity for Extreme Efficiency Ultra-Compact Converters**

# Series Interleaving of Converter Cells

- Interleaved Series Connection Dramatically Reduces Switching Losses (or Harmonics)




– Scaling of Switching Losses for Equal $\Delta i/I$ and $dv/dt$

$$P_{S,N} \approx P_{S,N=1} \cdot \left( \frac{1}{2N^2} \cdots \frac{1}{N^3} \right)$$

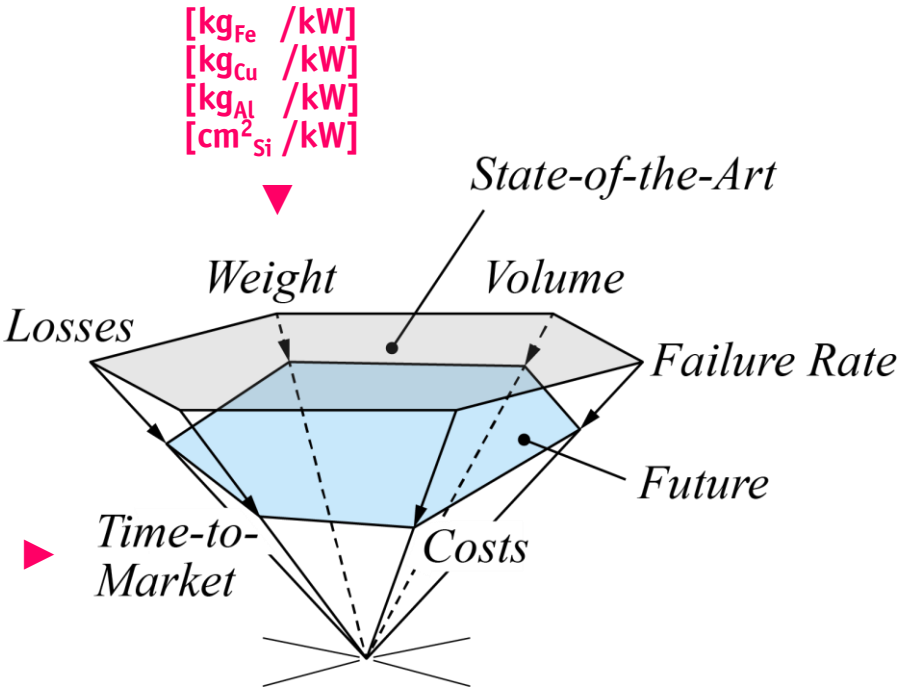
- Converter Cells Could Operate at VERY Low Switching Frequency (e.g. 5kHz)
- Minimization of Passives (Filter Components)

# Remarks on Performance Indices

→ Couplings & Limits

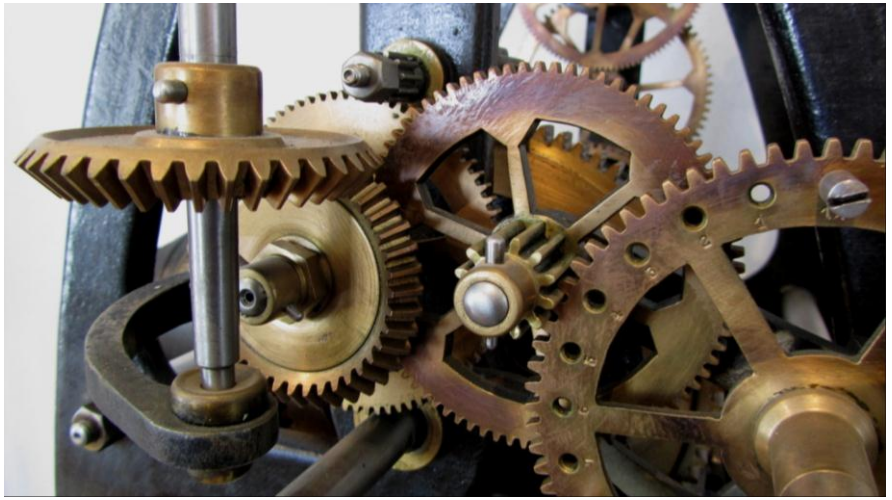
# Power Electronics Converters Performance Indices

- Performance Indices
  - Power Density [kW/dm$^3$]
  - Power per Unit Weight [kW/kg]
  - Relative Costs [kW/$]
  - Relative Losses [%]
  - Failure Rate [h$^{-1}$]



# ▶ Design Challenge

- Mutual Couplings of Performance Indices → Trade-Offs

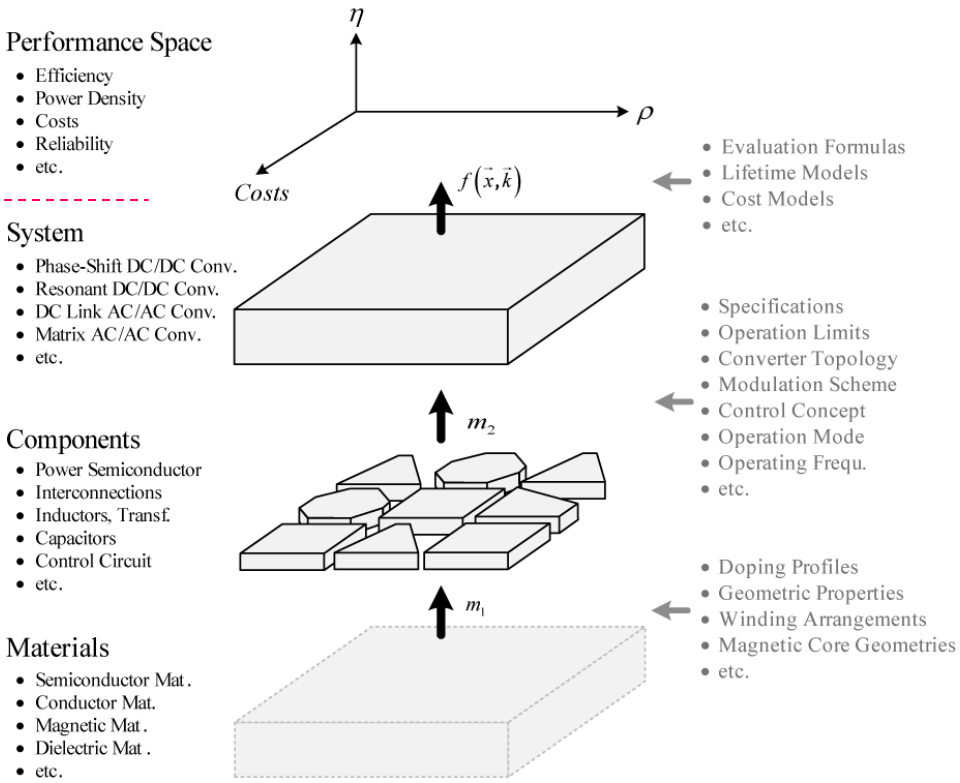


— For Optimized System Several Performance Indices Cannot be Improved Simultaneously

# Abstraction of Power Converter Design

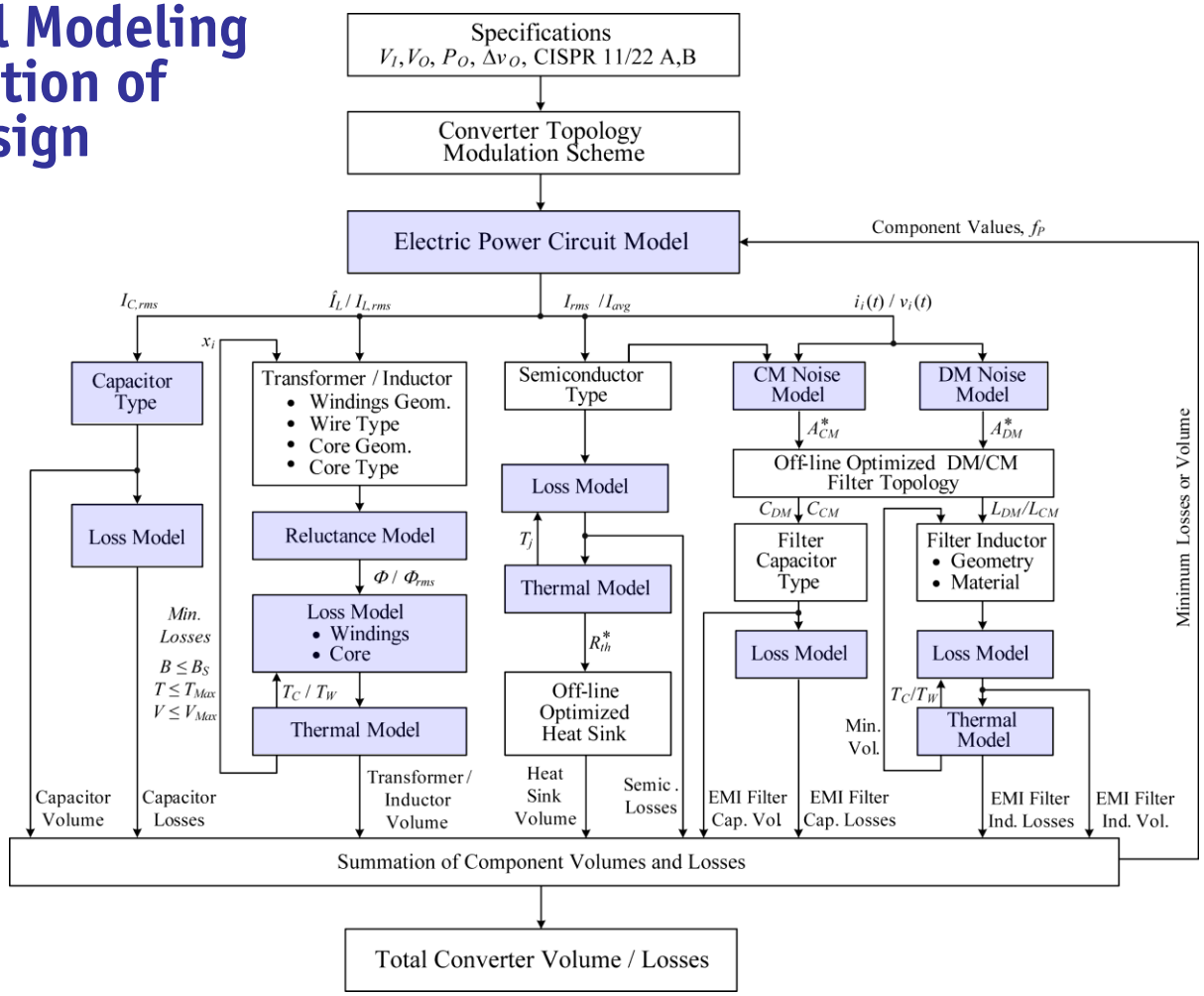
**Performance Space**

**Design Space**




- **Mapping of *Design Space* into System *Performance Space***

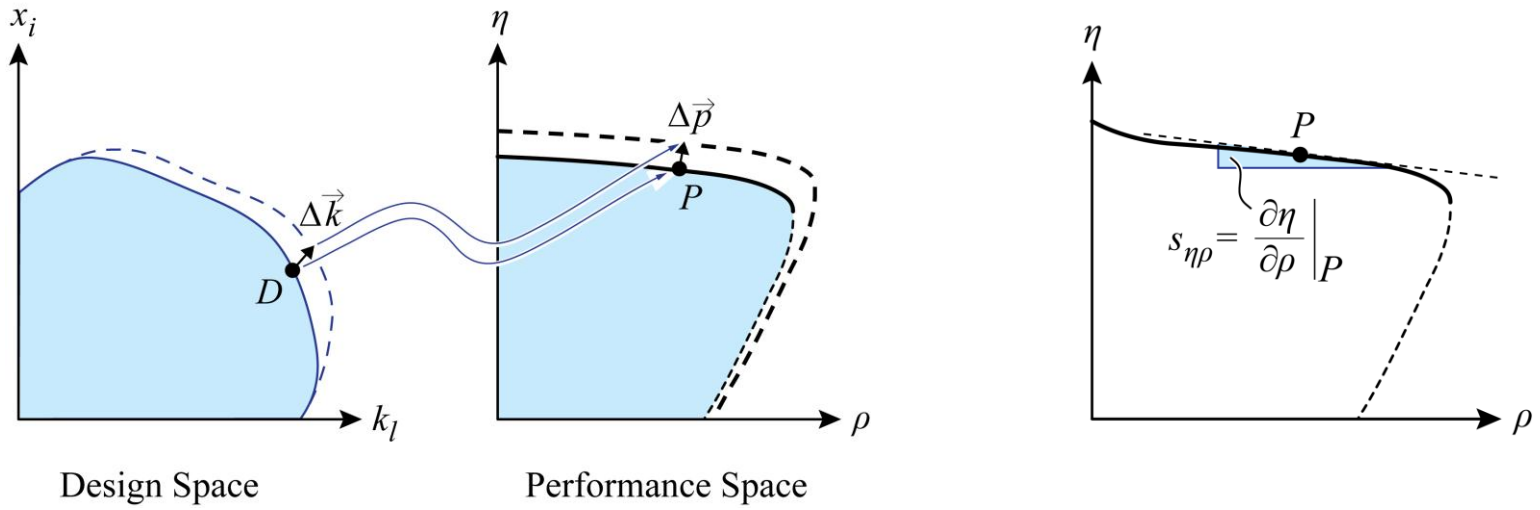
# Mathematical Modeling and Optimization of Converter Design



# Multi-Objective Optimization

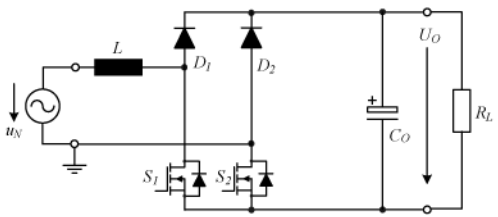
- Identifies Performance Limits → Pareto Front

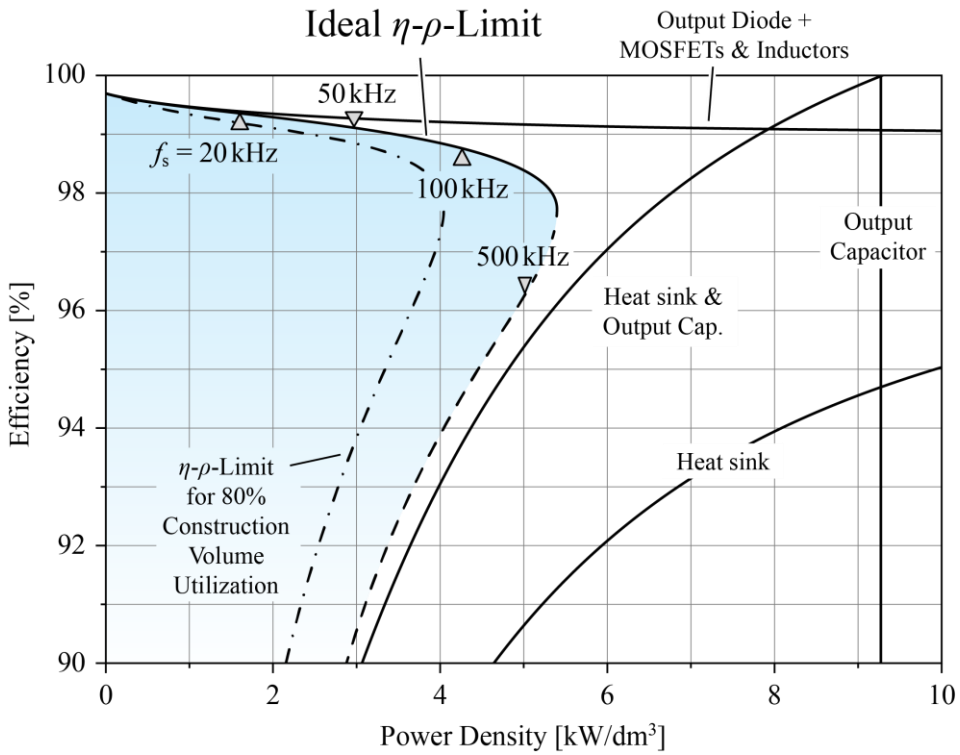
— Sensitivities to Technology Advancements (Example: η-ρ-Pareto Front)
— Trade-off Analysis



# ▶ Analysis of Performance Limits → Pareto Front

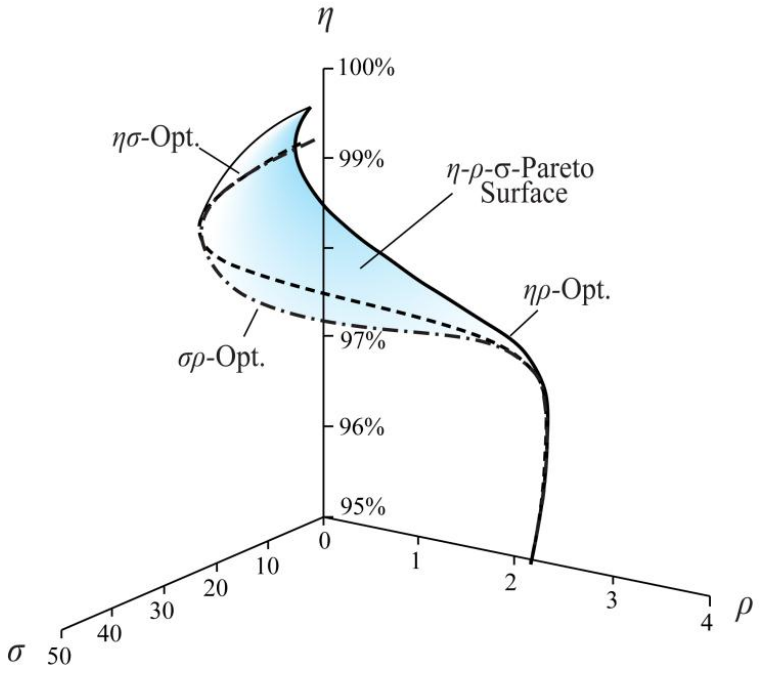
- **Clarifies Influence of Main Components and Operating Parameters**

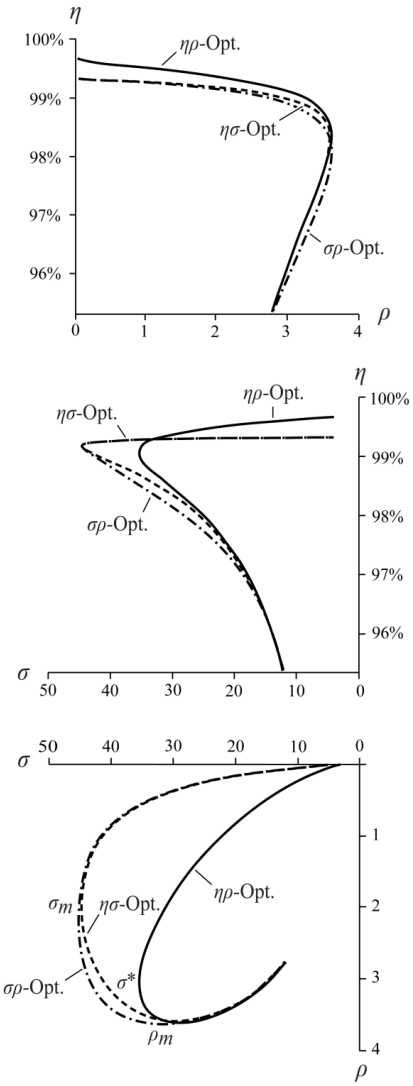


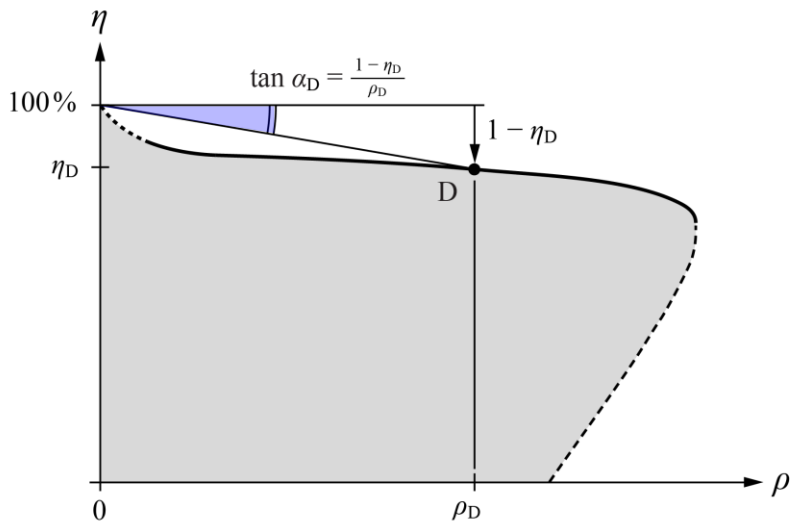
# ► η-ρ-σ-Pareto Surface

- **σ: kW/$**



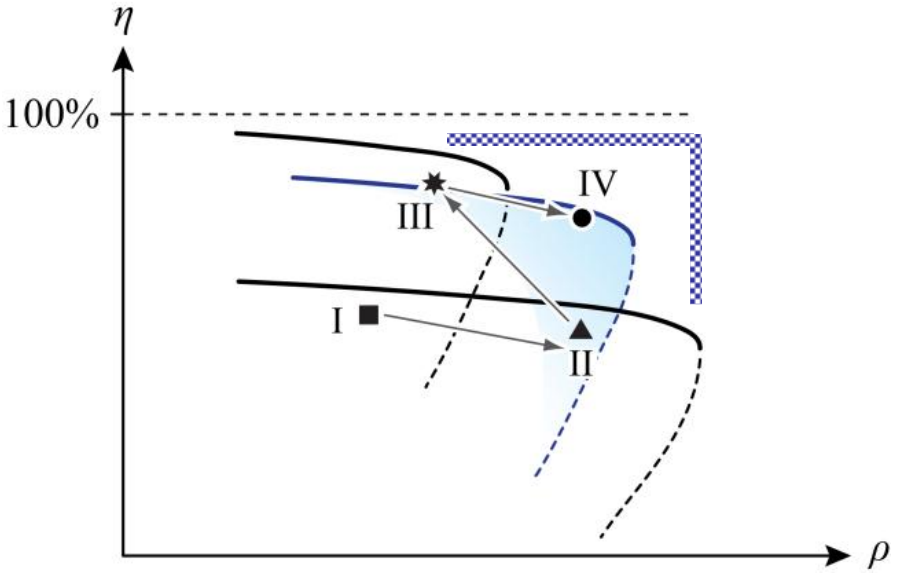
# Efficiency vs. Power Density




- **FOM = Ratio of Relative Losses and Power Density**

# Observation

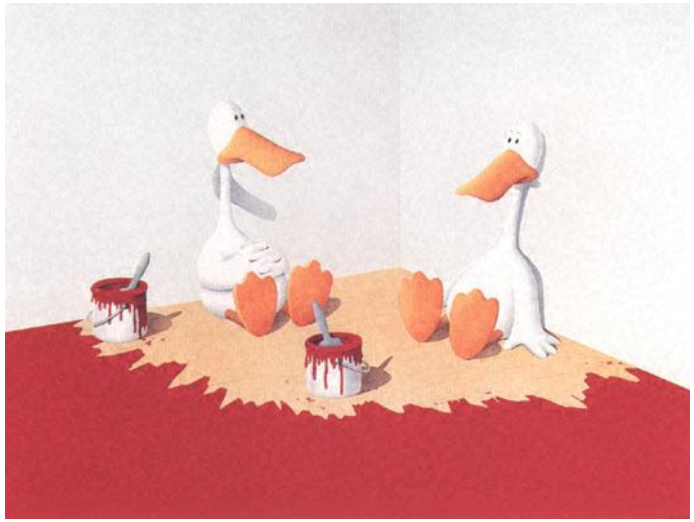
- **Very Limited Room for Further Performance Improvement !**



# Observation

► Very Limited Room for Further Performance Improvement !

Efficiency



Power Density

- General Challenge in Power Electronics
- Cost Models are Becoming Mandatory – Even for University Research(!)

# Conclusions

- No Magic New Topology
- Technological Limits (Magnetics!)

- Light-Load Efficiency → Ohmic Characteristics / ZVS / Interleaving !
- Modern Semiconductor Technology
- Modern Digital Control Technology

- System Oriented Analysis → Architecture & Energy Management
- Adv. Packaging & Thermal Manag. for High Eff. AND Power Density

# Questions

# References

**J. W. Kolar, F. Krismer, Y. Lobsiger, J. Mühlethaler, T. Nussbaumer, J. Miniböck**, *Extreme Efficiency Power Electronics*, Proc. of International Conf. of Integrated Power Electronics Systems (CIPS), Nuremberg, Germany, March 6-8, 2012.

**U. Badstuebner, J. Miniböck, J. W. Kolar,** *Experimental Verification of the Efficiency/Power-Density (n-p) Pareto Front of Single-Phase Double-Boost and TCM PFC Rectifier Systems*, Proc. of 28th IEEE Applied Power Electronics Conf. (APEC), Long Beach, California, USA, March 17-21, 2013.

# Acknowledgement

**F. Krismer**
**Y. Lobsiger**
**J. Mühlethaler**
**Th. Nussbaumer**
**J. Miniböck**
**M. Kasper**

# About the Instructor

**Johann W. Kolar (**F´10) received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel converter topologies and modulation/control concepts, e.g., the VIENNA Rectifier, the SWISS Rectifier, the Delta-Switch Rectifier, the isolated Y-Matrix AC/DC Converter and the three-phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 450 scientific papers at main international conferences, over 180 papers in international journals, and 2 book chapters. Furthermore, he has filed more than 110 patents. He was appointed Assoc. Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001, and was promoted to the rank of Full Prof. in 2004. Since 2001 he has supervised over 60 Ph.D. students and PostDocs.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for data centers, More-Electric-Aircraft and distributed renewable energy systems, and on Solid-State Transformers for Smart Microgrid Systems. Further main research areas are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC and GaN), micro power electronics and/or Power Supplies on Chip, multi-domain/scale modeling/simulation and multi-objective optimization, physical model-based lifetime prediction, pulsed power, and ultra-high speed and bearingless motors. He has been appointed an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011.

He received 9 IEEE Transactions Prize Paper Awards, 8 IEEE Conference Prize Paper Awards, the PCIM Europe Conference Prize Paper Award 2013 and the SEMIKRON Innovation Award 2014. Furthermore, he received the ETH Zurich Golden Owl Award 2011 for Excellence in Teaching and an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003.

He initiated and/or is the founder/co-founder of 4 spin-off companies targeting ultra-high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and from 2001 through 2013 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.