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Isolated Three-port Bidirectional DC-DC Converter

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Contents

Abstract

The demand for versatile electrical energy management systems that interface diverse energy sources, energy storage elements and loads, is increasing because of their potential applications in hybrid electric vehicles (HEVs) and fuel cell vehicles (FCVs), renewable energy generation systems and uninterruptible power supplies. The voltage levels and the voltage-current characteristics of the energy sources and storage elements are normally different from those of the loads. Therefore, a power electronics system to interface sources, storage elements and loads needs to be incorporated into energy management systems. The structure of such a system mostly includes an intermediate power bus and is configured using various two-port converters to interconnect the bus and the sources/loads. The main drawback of this structure is the complexity of the whole system, even if every two-port converter is simple and has the minimum number of power switches.

This thesis proposes and investigates a new multi-port converter, i.e., a single power processing stage with multiple power ports, which offers an opportunity to make the whole system simpler and more compact. Special attention is given to the converter employed in multiple voltage electrical systems in hybrid electric vehicles and fuel cell vehicles. Bidirectional power flow capability for the ports interconnecting storage elements and galvanic isolation between the sources and storage elements are key features of such a multi-port converter.

The isolated three-port bidirectional dc-dc converter, presented in this thesis, is composed of three full-bridge cells and a high-frequency transformer. Besides the conventional phase shift modulation technique managing the power flow between the ports, an additional duty cycle control is utilized to optimize the system behavior. This allows the system to

operate with minimum overall losses, no matter if the port voltage is a fixed value or varying in a wide range.

The dynamic analysis and the associated control strategy of the proposed converter are highly important for future industry applications. A two-input and two-output control-oriented model is developed by linearization of the static control-to-output characteristic of the converter based on a small-signal analysis. A decoupling network is applied to decompose the multi variable control system into a series of independent single-loop subsystems and to eliminate the loop interaction. Thus, the power flow from/to the ports can be controlled independently and simultaneously.

Finally, a laboratory prototype is built to verify the converter performances and the power management features.

Kurzfassung

Der Bedarf nach vielseitigen leistungselektronischen Systemen, die diverse Energiequellen, Speicherelemente und Verbraucher miteinander verbinden, wächst aufgrund der zahlreichen Einsatzmöglichkeiten stetig. Beispiele hierfür sind Anwendungen in Hybridautos und Brennstoffzellenfahrzeugen, die Energiegewinnung mit erneuerbaren Energiequellen und unterbrechungsfreie Stromversorgungen. Die Spannungs- und Stromcharakteristiken der Energiequellen sind typischerweise unterschiedlich von denen der Verbraucher, weshalb leistungselektronische Systeme für das Energiemanagement zwischen Energiequellen, Speicherelementen und Verbrauchern benötigt werden. Ein derartiges System umfasst heute im Wesentlichen einen Leistungsbus, der mittels mehrerer 2-Port-Konverter die Energiequellen und Verbraucher verbindet. Der hauptsächliche Nachteil dieser Struktur ist die Komplexität des Gesamtsystems, auch wenn die einzelnen 2-Port-Konverter einfach Topologie und eine minimale Anzahl an Leistungshalbleitern aufweisen.

In dieser Arbeit wird ein neuartiger Multi-Port-Konverter, d.h. eine Leistungsstufe mit mehreren Ein- und Ausgängen, vorgestellt und analysiert um das Gesamtsystem einfacher und kompakter zu gestalten. Besonderes Augenmerk wird dabei auf Konverter für die Kopplung von Systemen mit unterschiedlichen Spannungen gelegt, wie dies bei Anwendungen in Hybrid- und Brennstoffzellenfahrzeugen der Fall ist. Die Hauptmerkmale dieser Multi-Port-Konverter sind die bidirektionale Leistungscharakteristik jener Ports, welche Speicherelemente verbinden, und die galvanische Trennung zwischen den Energiequellen und den Speicherelementen.

Der in dieser Arbeit behandelte 3-Port-Konverter besteht aus bidirektionalen DC-DC Konvertern in Vollbrücken-Schaltung und nur einem

hochfrequent getakteten Transformator zur galvanischen Isolation. Neben der konventionellen Phasenverschiebungsmodulation zur Regelung des Leistungsflusses zwischen den Ports wird eine zusätzliche Regelung der Einschaltdauern der Leistungshalbleiter zur Optimierung des Systemverhaltens vorgeschlagen. Dies garantiert minimale Verlustleistung des Gesamtsystems unabhängig vom Spannungsbereich der angeschlossenen Lasten bzw. Quel

Ein weiterer Schwerpunkt der Arbeit ist die Analyse des dynamischen Verhaltens und des Regelverfahrens. Mit Hilfe einer Kleinsignalanalyse und Linearisierung der stationären Charakteristik des Konverters wird ein regelungstechnisches Modell mit zwei Ein- und Ausgängen entwickelt. Ein Entkopplungsnetzwerk zur Aufspaltung des Mehrgrössen-Regelsystems in einzelne unabhängige Regelkreise wird entworfen, womit der Leistungsfluss zwischen allen Ports gleichzeitig und unabhängig voneinander eingestellt werden kann.

Anhand von Messungen an einem Labor-Testsystem werden abschliessend die Funktionsfähigkeit der Leistungsregelung und eine hohe Performance des Konverters nachgewiesen.

Notation

X_{y_rms}	RMS value of x_y
X_y	Magnitude of x_y
$\hat{X}_y$	Amplitude of $\underline{x}_y$
$\Delta x_y(s)$	Laplace transform of $\Delta x_y(t)$
$\Delta x_y(t)$	Perturbation of the continuous-time signal $x_y(t)$
$\Delta x_y(z)$	Z-transform of $\Delta x_y[n]$
$\Delta x_y[n]$	Samples of $\Delta x_y(t)$, resulting in a discrete-time signal
$\Delta x_y^*(s)$	Laplace transform of $\Delta x_y^*(t)$
$\Delta x_y^*(t)$	$\Delta x_y(t) \sum_{n=-\infty}^{\infty} \delta(t - nT_{samp})$, resulting in a sampled continuous-time signal
$\underline{x}_y$	Fundamental phasor of x_y
$x_{y(n)}$	Approximation of x_y by replacing the exponential term with its n-order series
x_{y_Hi}	x_y associated with the MOSFET S_{Hi}
x_{y_Lo}	x_y associated with the MOSFET S_{Lo}
x_{y_avg}	Half-cycle-average value of x_y
x_{y_a}, x_{y_b}, x_{y_c}	x_y for the interval a, b and c

x_{y_peak}	Peak value of the steady-state waveform x_y
x_{y_ref}	Reference signal of x_y
x_{yr}	Transformer primary-referred value of x_y.

Symbols

α	Phase displacement of the voltage vector $\underline{u}_{1r}$ and the current vector $\underline{i}_{12r}$
δ_1-δ_3	Duty cycle of the full-bridge unit output voltage
δ_{fs}	Skin depth at the switching frequency f_s
ϕ_1-ϕ_2	Phase shift angle between the gate signals of the switches in two phase legs
B_{max}	Maximum flux density
C_f	Output filter capacitor
C_{gd}, C_{gs}, C_{ds}	Inter-electrode capacitances of the MOSFET
C_{oss}	Output capacitance of the MOSFET in the HV unit
C_{sb}	Capacitor in the RC snubber
D_1-D_{12}, D_{Hi}, D_{Lo}	Diode
d_1-d_3	On-duty ratio of the switch
d'_1-d'_3	Off-duty ratio of the switch
d_s	Diameter of a single strand of the litz wire
d_w	Overall diameter of the litz wire excluding the insulating layer
E_{sw}	Sum of the energy dissipation of two MOSFETs in the same phase leg during the commutation interval
f_{samp}	Sampling frequency, i.e., twice the switching frequency f_s
f_s	Switching frequency

G	Transfer function matrix of the three-port converter, including the elements G_{11}, G_{12}, G_{21} and G_{22}
G_{2I_A}, G_{3I_A}, G_{2V_A}	Transfer function of the anti-aliasing low-pass filters
G_{2I_D}, G_{3I_D}, G_{2V_D}	Transfer function of the digital low-pass filters
G_{2I_M}, G_{3I_M}	Transfer function from the port currents to the measured source/load currents
G_{2I_PI}, G_{3I_PI}, G_{2V_PI}	Transfer function of the current/voltage loops with the PI controllers
G_{2I}, G_{3I}, G_{2V}	Transfer function of the current/voltage loops without the controllers
G_{2V_M}	Transfer function from the measured port current to the measured port voltage
G_{AD}	Transfer function of the sample and hold unit in the A/D converter
G_{PI_2I}, G_{PI_3I}, G_{PI_2V}	PI controllers for the current/voltage loops
$G_{vd}(z)$	Control-to-output-voltage pulse transfer function in the discrete-time domain
$G_{vs}(s)$	Control-to-output-voltage transfer function in the continuous-time domain
H	Transfer function matrix of the decoupling network, including the elements H_{11}, H_{12}, H_{21} and H_{22}
h_f	Height of the single layer solid foil
i_{1M}-i_{3M}	Measured source/load current
i_1-i_3	Input/output current
i_{ch}	Channel current in the MOSFET
i_D	Current of the body diode of the MOSFET

i_d	Drain current of the MOSFET
i_{L1}-i_{L3}	Current flowing through the leakage inductance of the transformer L_1-L_3
i_{Lpd}, i_{Lps}, i_{Lpl}	Currents flowing through the parasitic inductances L_{pd}, L_{ps}, L_{pl}
i_{Ls}	Current flowing through the inductance L_s
i_o	Inductive load current in the test circuit for the MOSFET switching behavior analysis
i_{Rg}	Current flowing through the gate resistor R_g
L_{12}, L_{13}, L_{23}	Inductance, transformed from L_1-L_3
L_1-L_3	Leakage inductance of the transformer
L_m	Magnetizing inductance of the three-winding transformer
L_{p1}-L_{p3}	Inductors in the LC filters on the ports
L_{pd}, L_{ps}, L_{pl}	Parasitic inductances due to the device package and the interconnection layout
L_s	Sum of the leakage inductances in the two-port converter
l_t	Average length of one turn of the winding
n_1-n_2	Turns ratio of the ideal two-winding transformer
n_l	Number of layers of the winding
n_s	Number of strands of the litz wire
n_t, n_{t_1}, n_{t_2}	Number of turns of the winding, n_{t_1} and n_{t_2} indicating the number of turns of the winding on the HV bus (port 1) and the 42 V bus (port 2) sides
P_{12_f}, P_{23_f}, P_{13_f}	Fundamental component of the active power transferred from one port to the other port.

P_{12}, P_{23}, P_{13}	Active power transferred from one port to the other port
P_1-P_3	Active power transferred from/to the port, i.e., active power delivered by the source, consumed by the load or stored by the storage device
P_{cond}	Conduction losses of the MOSFET
P_{core}	Core losses of the magnetic component
P_{sw}	Switching losses of four MOSFETs in the same full-bridge unit
P_{wind}	Conduction losses of the winding
p_{ds}	Transient power losses of the MOSFET
R_{ac}, R_{ac_Litz}, R_{ac_Solid}	AC resistance of the winding, R_{ac_Litz} and R_{ac_Solid} indicating the AC resistances of the litz wire and solid foil winding, respectively
R_{dc}, R_{dc_Litz}, R_{dc_Solid}	DC resistance of the winding, R_{dc_Litz} and R_{dc_Solid} indicating the DC resistances of the litz wire and solid foil winding, respectively
R_{ds}	On-resistance of the MOSFET
R_g	Gate resistor
R_l	Load resistor
R_{sb}	Resistor in the RC snubber
R_s	Sum of the resistances in the two-port converter
S_1-S_{12}, S_{Hi}, S_{Lo}	Switch
T_1-T_2	Ideal two-winding transformer
T_a-T_d	Time interval for the switching state
T_r	Three-winding transformer

T_{samp}	Sampling cycle, i.e., half of the switching cycle T_s
T_s	Switching cycle
t_0-t_3	Time instant at the beginning of the switching state
t_{step}	Time step for the numerical calculation in the switching behavior analysis
t_s	Distance between the centers of two adjacent strands of a litz wire
t_w	Distance between the centers of two adjacent Litz wires of a winding
V_b	Forward voltage of the body diode of the MOSFET
V_{core}	Core volume
V_T	Threshold voltage of the MOSFET
v_{1M}-v_{3M}	Measured source/load voltage
v_1-v_3	Input/output port voltage
v_{ac1}-v_{ac3}	AC voltage imposed by the bridge unit
v_{gd}, v_{gs}, v_{ds}	Gate-drain, gate-source and drain-source voltages of a MOSFET
v_g	Gate supply voltage
v_{in}	Source voltage in the test circuit for the MOSFET switching behavior analysis
v_{L1}-v_{L3}	Voltage applied to the leakage inductance of the transformer L_1-L_3
v_{Ls}	Voltage applied to the inductance L_s
v_{sb}	Voltage across the capacitor C_{sb} in the RC snubber
w_f	Width of the single layer solid foil.

Acronyms

AC	Alternating Current
CCM	Continuous Conduction Mode
DAB	Dual-active-bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
EPA	Environmental Protection Agency
FC	Fuel Cell
FCV	Fuel Cell Vehicle
GTO	Gate Turn-off Thyristor
HB	Half Bridge, i.e., phase leg
HCA	Half Cycle Average
HEV	Hybrid Electric Vehicle
HV	High Voltage
ICE	Internal Combustion Engine
ICE+EG	Internal Combustion Engine plus Electric Generator
IGBT	Insulated-gate Bipolar Transistor
LC	Inductor Capacitor
LV	Low Voltage
MCT	MOS-controlled Thyristor
MOSFET	Metal Oxide Semiconductor Field-effect Transistor

PS	Phase-shift
PV	Photovoltaics
PWM	Pulse-width Modulation
RB	Reverse-blocking
RC	Resistor Capacitor
RMS	Root Mean Square
TDR	Total Device Rating
WWEA	World Wind Energy Association
ZVS	Zero-voltage Switching.

Chapter 1

Introduction

1.1 Introduction to Multi-port Converters

A power electronic system, as shown in Figure 1.1, usually consists of an energy source, a load, a switching converter and a control circuit. The key element is the switching converter, which efficiently processes the electric power from its available input form to the desired output form according to the signal generated by the controller [1]. The switching converter is also known as a two-port converter since it has two power ports, one connecting the source for power input and the other one connecting the load for power output.

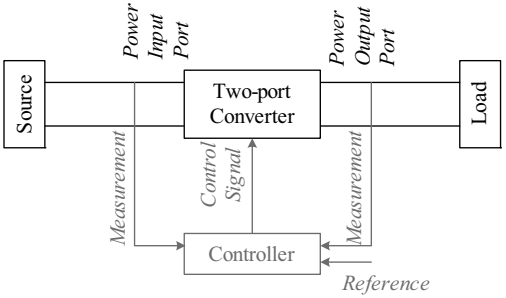


Figure 1.1: Block diagram of a power electronic system with a source and a load.

However, there are also some special cases, i.e. a system may accommodate multiple sources and/or multiple loads. The structure of such a system mostly includes an intermediate power bus and is configured using various two-port converters to interconnect the bus and the sources/loads, as illustrated in Figure 1.2. These two-port converters are controlled independently and a communication bus may be needed for the purpose of managing power flow. The main drawback of this structure is the complexity of the whole system, even if every two-port converter is simple and realized with the minimum number of power switches.

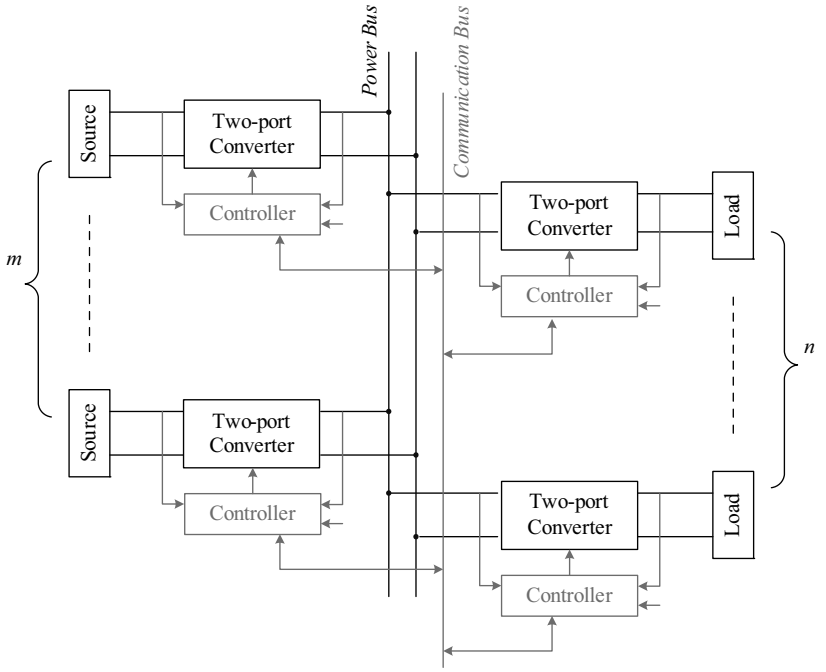


Figure 1.2: Block diagram of a power electronic system with various two-port converters.

A multi-port converter, i.e. a single power processing stage with multiple power ports, as illustrated in Figure 1.3, is emerging because it offers an opportunity to make the whole system simpler and more compact. This multi-port converter cannot only interface all sources/loads, and modify

the electrical energy form, but also manage the power flow between the sources and the loads.

The major advantage of the multi-port converter over various two-port converters with an intermediate power bus is that less power switches, less associated gate drivers and less passive components are needed since the partial redundant power processing units in the two-port converters are eliminated. Thus cost can be reduced, and higher power efficiency and higher power density can be achieved. Moreover, better dynamic performance can be obtained since the communication time between the different control circuits for the two-port converters does not exist any more due to the centralized control.

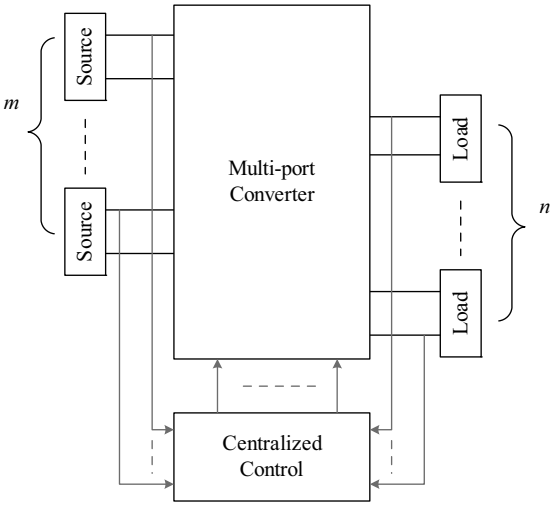


Figure 1.3: Block diagram of a power electronic system with a multi-port converter.

1.2 Application of Multi-port Converters

Demand for multi-port converters is increasing because of their potential application in renewable energy generation systems [2–10], hybrid electric vehicles (HEVs) and fuel cell vehicles (FCVs) [11], uninterruptible power supplies [12–14] and any other application with the requirement

to interface multiple sources/loads [15–30]. The motivation for employing multi-port converters, and the structure and basic function of the systems are discussed in following for three energy management applications: a renewable energy generation system, a propulsion system and a multiple voltage electrical system in HEVs and FCVs.

1.2.1 Renewable Energy Generation Systems

Nowadays, fossil fuels, including oil, natural gas and coal, are the main suppliers of energy. It is estimated that in 2006, 79 percent of global final energy consumption was through the use of fossil fuels, as shown in Figure 1.4 [31]. There are two issues which need to considered regarding fossil fuels. One is that fossil fuels are non-renewable resources. These resources were formed naturally over millions of years and cannot be produced, re-grown or regenerated as fast as they are consumed. The other is the impact on the natural environment. In the United States, more than 90 percent of greenhouse gas emissions originate from the combustion of fossil fuels [32]. The combustion of fossil fuels also produces other air pollutants, such as sulfur dioxide, nitrogen oxides and heavy metals.

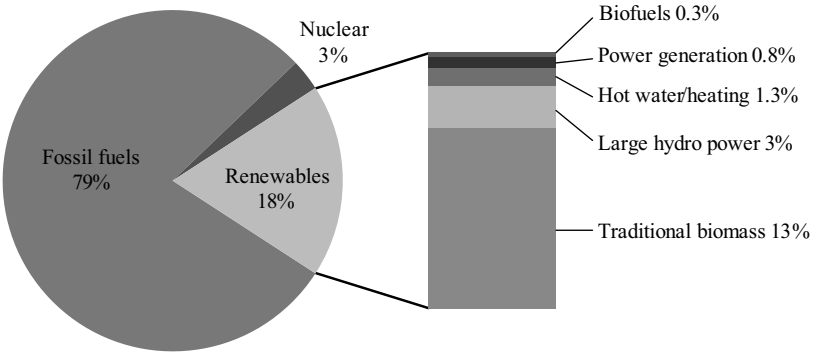


Figure 1.4: Global final energy consumption by energy type in 2006 [31].

Moreover, the day-by-day demand for energy is still increasing. The world energy consumption is projected to expand by 50 percent from 2005 to 2030 in the IEO 2008 reference, as a result of economic growth and expanding population in the world's developing countries [33].

The recognition of above mentioned factors drives mankind to actively look for solutions. Consequently, clean renewable energy, which can make deep cuts in fossil fuel use, and technologies for improving the efficiency in energy use, which can slow the energy demand growth, are of great interest.

Renewable resources, like biomass, sunlight and wind, are defined in [34] as "[...] virtually inexhaustible in duration but limited in the amount of energy that is available per unit of time [...]".

In 2006, renewable energy supplied about 18.4 percent of global electricity production [31]. There, modern technologies, which have been continuously growing in recent years, are:

- Wind power: the most competitive renewable energy technology [35]. In 1997, the installed capacity of wind-powered generators worldwide was about 7.5 GW. However, the sum of the global installations reached about 94 GW by the end of 2007, with 20 GW new installations [36];
- Solar PV: the world's fastest-growing renewable energy technology. Its existing world capacity by the end of 2007 was 10.5 GW, with a 36 percent annual average growth rate since 2002, according to the preliminary data [31];
- Small hydro power: one of the most cost-effective energy technologies to be considered for rural electrification. It has a relatively low environmental impact compared to a large hydro power since it does not interfere significantly with river flows, either being run-of-river or having a small reservoir. During 2006, the small hydro installations grew by 11 percent and the world total small hydro capacity was raised to 73 GW [31].

These modern power generation technologies are still gaining more momentum. For example, large scale wind farms are being developed both onshore and offshore. By 2010, the World Wind Energy Association (WWEA) expects 170 GW global capacity to be installed, implying that the overall capacity of 2010 is increased by a factor of two compared to that of 2007 [36].

However, the main disadvantage of these technologies is the uncontrollability of power production since natural sources vary in their availability. The detail is the following:

- Wind turbines convert the kinetic energy in wind into the electrical energy. The amount of electricity produced is dependent on the wind speed, more precisely on the cube of the wind speed. The wind power production fluctuates at different time scales: hourly, daily, seasonally. More challenging is that the wind turbines are not able to generate electricity when the wind speed is too low (less than about 2.5m/s) and the turbines need to be shut down to avoid the damage of equipments when the wind speed is too high (more than about 25m/s);

- Solar PV cells convert sunlight into electricity based on the photovoltaic effect. The amount of electricity produced relies on the radiation intensity and the angle at which the solar PV cells are radiated. The solar PV production varies throughout the day and through the seasons, and is affected by clouds and rain falls;

- Hydraulic turbines convert the gravitational energy of falling or flowing water into electricity. The amount of electricity produced is mainly determined by the water level and the speed and rate of the water flow. The small hydro power production has a seasonal variability.

Therefore, it would be difficult to operate a power system installed with only a single renewable generation unit due to the high uncertainty of the availability of the renewable source and the power difference between the supply profile and the demand pattern. An energy storage device needs to be incorporated into the system with the following benefits:

- compensation of the power mismatches between the souring and loading patterns: the energy storage device stores excess power when the load is light, and provides supplemental power when the load is heavy;

- reliable power supply to the load: the energy storage device can serve as a backup power source, which supplies sufficient power when the renewable source is not available;

- capture of maximum renewable energy: for example, maximum power point tracking can be performed and the additional power produced by the solar panel can be stored;

- avoidance of oversizing the renewable energy generation unit: the renewable energy generation unit can be sized according to the average power consumed by the load, The peak power requirement can be fulfilled by the power from the storage device in addition to the power of the renewable source.

An overview of the entire renewable energy generation system is illustrated in the Figure 1.5. Since different energy sources, storage devices and loads have different voltage levels and distinct voltage-current characteristics, they cannot directly be connected together. A multi-port converter [37–46], which utilizes a single power stage for interfacing sources and storage devices, and providing desired voltages/currents to loads, is a proper choice to achieve flexible, cost-effective, and more efficient power harvesting from a variety of renewable sources.

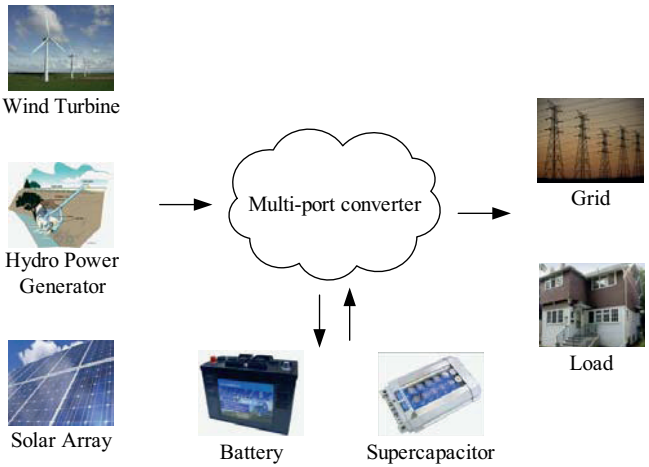


Figure 1.5: Multi-port converter utilization in renewable energy generation systems.

1.2.2 Propulsion Systems in Hybrid Electric Vehicles and Fuel Cell Vehicles

As is well known, research is ongoing to find a suitable alternative to conventional power train propulsion systems, which include an internal

combustion engine (ICE) and its associated subsystems. The conventional propulsion system has been in existence for over 100 years and it suffers from two problems, namely:

- Low efficiency: the energy distribution in a mid-size vehicle is shown in the Figure 1.6. Only 12.6 percent of the energy contained in gasoline is converted to traction, according to U.S. Urban Test Cycle [47]. The rest are losses: 62.4 percent is lost in the internal combustion engine; 17.2 percent is lost due to idling at stop lights or in traffic; 5.6 percent is lost in the transmission and other parts of the driveline.
- High emissions: a report from the U.S. Environmental Protection Agency (EPA) states that motor vehicles account for about 75 percent carbon monoxide emissions and are responsible for nearly one half of smog-forming volatile organic compounds, more than half of the nitrogen oxide emissions, and about half of the toxic air pollutant emissions in the United States [48].

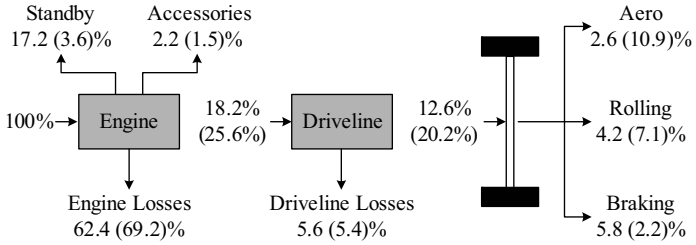


Figure 1.6: Energy distribution in a mid-size vehicle [47]. Note: numbers indicate urban energy distribution; numbers in parentheses indicate highway energy distribution.

Hybrid electric vehicles (HEVs), with an ICE that functions as primary power source and an energy storage system that functions as the secondary power source, appear to be one of the viable solutions [49–51]. The drive train efficiency in a HEV can potentially be improved to about 30-40 percent due to the optimization of the engine operation and recovery of kinetic energy during braking [52].

The hybrid propulsion system proposed in [53] is shown in Figure 1.7, which includes:

- an internal combustion engine plus electric generator (ICE+EG) system: it converts energy from gasoline or diesel to electric energy and is the main energy source, which is sized up to 60% of the maximum cruising power;

- a battery system: it is used to provide long-term power, such as driving the vehicle along when the ICE+EG system is stopped due to its poor efficiency, either if the vehicle is at a stop or at light load. The battery system feeds the 40% rest of the maximum cruising power;

- a supercapacitor storage: this kind of storage has an advantage over a battery system in terms of transient power capability. Consequently, a supercapacitor storage is employed to provide transient power for acceleration and to sink transient power from regenerative braking. The combination of a battery system with a supercapacitor can achieve a higher efficiency, a longer run-time and lower cost.

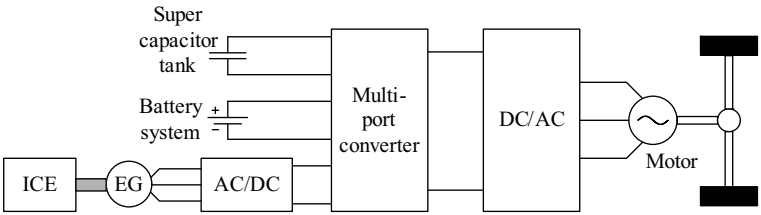


Figure 1.7: Hybrid propulsion system proposed in [53].

Fuel cells (FCs) utilize a chemical reaction to generate electricity with zero emissions if the fuel, e.g. hydrogen is obtained using renewable energy and very low emission if the hydrogen is derived from fossil fuels. Therefore, there is an increasing interest in using fuel cells for propulsion, i.e. replace the ICE system with the fuel cell system to drive the vehicle [54].

Energy storage devices, such as batteries and supercapacitors, should be combined with the FC stack to achieve the maximum efficiency of the FC system and to improve the slow response of FC in transitory situations.

In both hybrid vehicles and fuel cell vehicles, a multi-port converter [55–59], as illustrated in Figure 1.7, is a compact, efficient and reliable

solution to combine the power flowing from the on-board generation units and the storage devices and obtain a regulated bus DC voltage for the inverter.

1.2.3 Multiple Voltage Electrical Systems in Hybrid Electric Vehicles and Fuel Cell Vehicles

The present 14 V automotive electrical system has been in use for over four decades. Recently, the power demand of the electrical system has been significantly increasing since more and more electrical and electronic features are added to improve vehicle performance, fuel economy, emissions, passenger comfort, safety and convenience. By 2010, the estimated power demand can go up to about 5.5 kW for larger cars and about 3 kW for smaller cars [60].

The practical maximum allowed current in a vehicle is approximately 200 A, i.e. about 3 kW for a 14 V system since higher currents cause three problems, namely [61, 62]:

- increased size, weight and cost of wiring;
- higher ohmic losses in wiring harnesses, connections and components, causing a greater voltage variation at the load and reduced fuel economy;
- higher temperatures and the need for improved cooling.

Therefore, it is necessary for automotive manufacturers to consider a higher voltage for the electrical system, i.e. 42 V (3×14 V) is gaining acceptance internationally as the best compromise considering the predicted power demand and consumer safety requirements for an unprotected electrical system since 58 V DC, the maximum dynamic over voltage of the 42 V system, is still lower than 60 V DC, the maximum safe voltage to touch suggested by the medical research [63, 64].

Upgrading the voltage from 14 V to 42 V will enable many new systems throughout the vehicle (cf. Figure 1.8) [62, 64], e.g.

- in terms of fuel savings: electromagnetic valves, electric power steering, electric oil and water pumps;

- in terms of reducing emissions: electrically heating catalytic converter;
- in terms of comfort, convenience and safety: electrically heated seats, electrically heated steering wheel, active suspension, electric braking, electric de-icing, high-end sound.

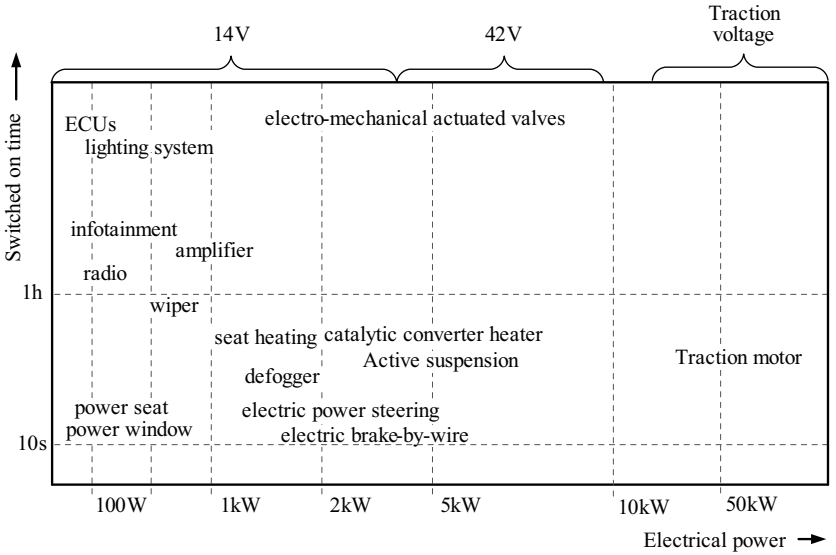


Figure 1.8: Power requirement for existing and prospective electrical systems in HEVs and FCVs [62].

It would take enormous resources for any automotive manufacturer to change the voltage of the electrical system from 14 V to 42 V in a single step due to the complexity of the present automotive industry. From a practical point of view, this conversion can only be phased gradually. During the transition it will be necessary to employ a dual low voltage system [64–67].

Additionally, a high voltage (HV) bus, ranging from 200 V to 500 V DC depending on the vehicle requirement, is required for the propulsion system in HEVs and in FCVs [68]. It means that the electrical system provides power not only for the vehicle ancillary loads but also for the

traction loads. Therefore, a multiple voltage (14 V/42 V/HV) electrical system will likely be employed in HEVs and FCVs, as shown in Figure 1.9 [69–73], where the 42 V starter/alternator is kept as a backup for the HV battery, although it could be eliminated in full hybrid vehicles. In this case, the energy from the 42 V starter/alternator can be used to charge the HV battery. On the other hand, the loads connected on the 14 V and 42 V sides can consume power from the traction generator in HEVs or the fuel cell in FCVs. A bidirectional multi-port converter, as shown in Figure 1.9, is needed to interface the three different voltage buses and to manage the power flow with low cost and high efficiency.

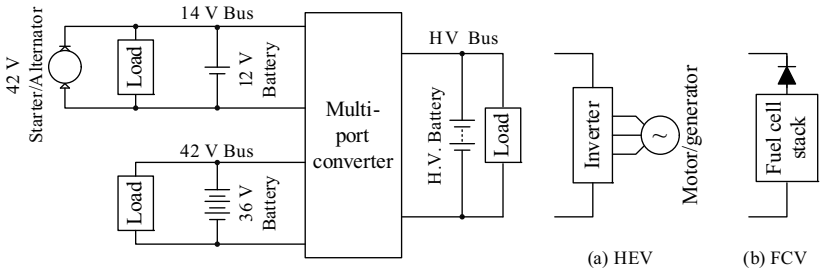


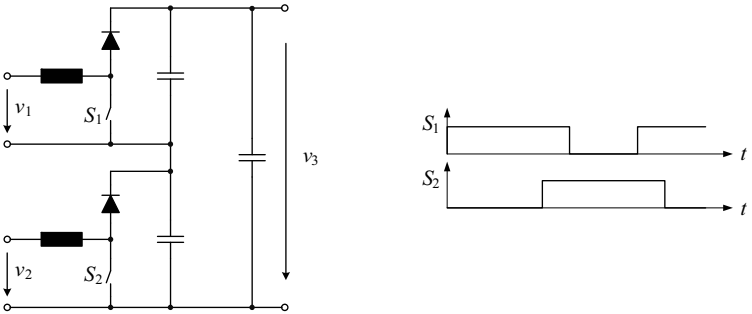
Figure 1.9: A multi-port converter interconnecting 14 V/42 V/HV bus in HEVs and FCVs.

1.3 State-of-the-art Multi-port Topologies

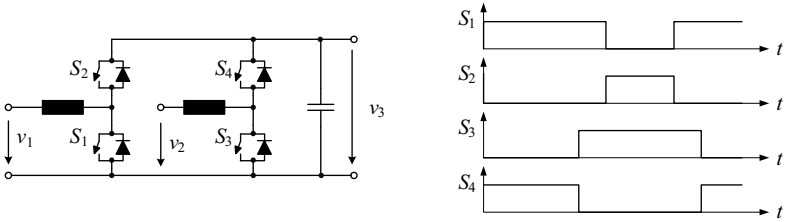
In recent years, multi-port DC-DC converters have drawn increasing research attention and many different topologies have been proposed. These topologies can be classified into three groups: non-isolated, partially isolated and fully isolated multi-port topologies. Different topologies of these groups along with their advantages, disadvantages and operation principles are explained in the following.

1.3.1 Non-isolated Multi-port Topologies

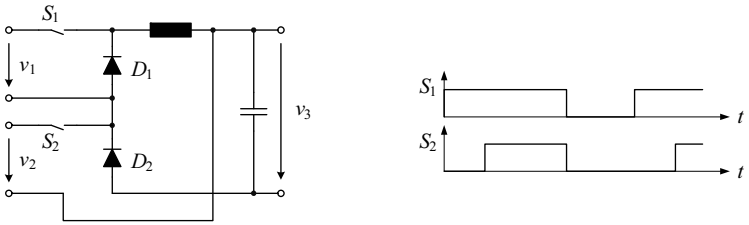
Non-isolated multi-port topologies, where all power ports share a common ground, are shown in Figure 1.10.



(a) Topology A1

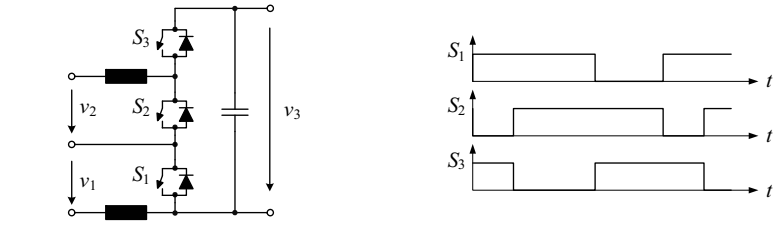


(b) Topology A2

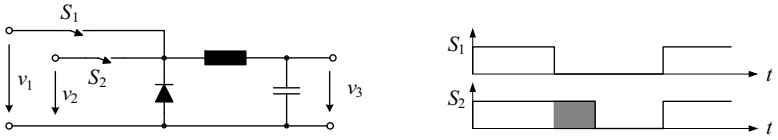


(c) Topology A3

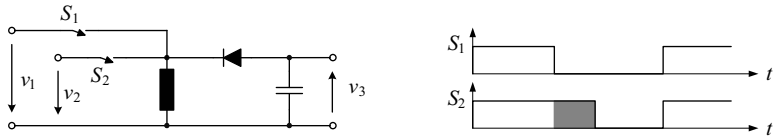
Figure 1.10: (a)-(f) Different non-isolated multi-port topologies and related gate signals of the switches.



(d) Topology A4



(e) Topology A5



(f) Topology A6

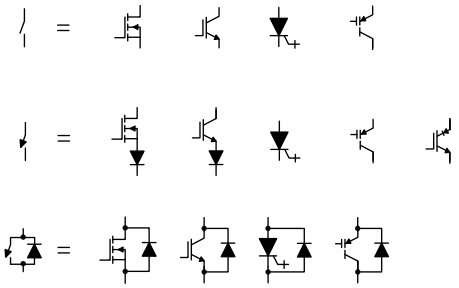


Figure 1.10: (a)-(f) Different non-isolated multi-port topologies and related gate signals of the switches (continued).

Table 1.1: Non-isolated multi-port topologies.

Name	Original topology	Connection method	Power flow	Voltage magnitude	Literature
A1	Boost	series	unidirectional	$V_1 + V_2 < V_3$	[2,3]
A2	Boost/buck	parallel	bidirectional	$V_1 < V_3$, $V_2 < V_3$	[7,53,55]
A3	Buck, buck-boost	partially series	unidirectional	$V_1 > V_3$ [a]	[21]
A4	Boost/buck	partially series	bidirectional	$V_1 + V_2 < V_3$	[58]
A5	Buck	partially parallel	unidirectional	$V_1 > V_3$, $V_2 > V_3$	[15]
A6	Buck-boost	partially parallel	unidirectional	-	[17,19]

[a] There is no voltage magnitude limit when the output power is drawn from both sources. But when only the energy from port 1 is available, the condition that V_1 is higher than V_3 needs to be observed.

F. Caricchi, F. Crescimbini et al. proposed a two-input topology in 1993 [2], referred as topology A1 (cf. Figure 1.10(a)). The topology is composed of two boost converters, whose outputs are connected in series. The amount of power drawn from the input power sources is regulated to the desired levels by adjusting the duty ratios of the switches S_1 and S_2. The peak-to-peak ripple of the output voltage v_3 can be reduced by properly choosing the time difference of the leading edges of two gate signals, as illustrated in Figure 1.10(a). One limit of this topology is that the sum of the magnitudes of two input voltages must be lower than that of the output voltage.

Several years later, the same research institute developed a similar topology in [53, 55], referred as topology A2 (cf. Figure 1.10(b)). This topology is also composed of two bidirectional boost/buck converters, whose outputs are connected in parallel and share the output capacitor. Moreover, each power port of topology A2 has the capability of bidirectional current flow due to the employment of standard inverter phase legs, where the switches are bidirectional-conducting, forward-blocking, i.e. normally a metal oxide semiconductor field-effect transistor (MOSFET) or insulated-gate bipolar transistor (IGBT) with anti-parallel diode. Topology A2 allows higher efficiency compared with topology A1 when the input/output voltages, v_1, v_2, and v_3 are of the same magnitude.

A double-input topology for high/low voltage sources was proposed by Y. Chen et al. in [21], referred as topology A3 (cf. Figure 1.10(c)). By removing port 1 and the switch S_1 and substituting the forward-biased diode D_1 with a short circuit, the remaining circuit of topology A3 can be recognized as a basic buck-boost converter. Similarly, by removing port 2 and the switch S_2 and replacing the diode D_2 with a short circuit, the remaining circuit is a buck converter. Therefore, topology A3 is a combination of a buck and a buck-boost converter, i.e. the circuit branch including the switch and the diode of the buck converter is in series with that of the buck-boost converter with a common LC low pass filter. The major advantage of the topology is that the magnitudes of the input voltages, i.e. V_1 and V_2, can be higher or lower than that of the regulated output voltage V_3 when the output power is drawn from both power sources. But when only energy from port 1 is available, topology A3 degenerates into a buck converter and V_1 must be higher than V_3 in order to transfer power to the load.

Interest in reducing switch count was presented by M. Marchesoni et

al. by introducing a three-switch bidirectional topology [58], referred as topology A4 (cf. Figure 1.10(d)). The topology is a basic bidirectional boost/buck topology unit but with an additional circuit branch including a power port, an inductor and a bidirectional-conducting switch placed in series with the original one, where only three controllable switches are needed against four switches in the conventional double boost/buck topology. In all eight possible switching configurations, only the configurations with one switch in the off state and the other two switches in the on state are adequate. Any two off-duty ratios of the switches can be used as control inputs to manage the power flow; the third duty ratio is determined by the condition $D_1' + D_2' + D_3' = 1$ in order to ensure a correct behavior of the topology, where D_1'-D_3' indicate the off-duty ratios of the switches S_1-S_3.

A two-input topology was developed by F. Rodriguez et al. in [15], referred as topology A5 (cf. Figure 1.10(e)). This topology is a basic buck topology unit but with an additional circuit branch including a power port and a switch placed in parallel with the original one. The switches in this topology are forward-conducting, bidirectional-blocking, which can be a gate turn-off thyristor (GTO), a MOSFET or IGBT in series with a diode, or a new developed reverse-blocking (RB) IGBT. In the continuous current mode (CCM), if any switch is turned on, the diode is blocking, but if all switches are turned off, the diode is conducting. If several switches are in the on state, the topology only captures power from the source with the highest voltage magnitude for which the respective switch is turned on. This reduces the effective duty ratio of the switch S_2 (marked by the shaded area in Figure 1.10(e)) in the duty cycle control scheme where the leading edge of each gate signal coincides, when V_1 is higher than V_2. The power rating is also limited since only one input/output is allowed to transfer energy to/from the common magnetic component at a time.

Another two-input topology was proposed by B. Dobbs et al. in [17], referred as topology A6 (cf. Figure 1.10(f)). This topology is based on a buck-boost topology unit providing either buck or boost transformation of the inputs, and its operation principles are similar to those of topology A5.

The pulse-width-modulation (PWM) controlled non-isolated multi-port topologies, whose features are summarized in Table 1.1, are mostly combinations of basic topology units, such as the buck, the boost, the buck-boost or the bidirectional boost/buck topology unit. These topolo-

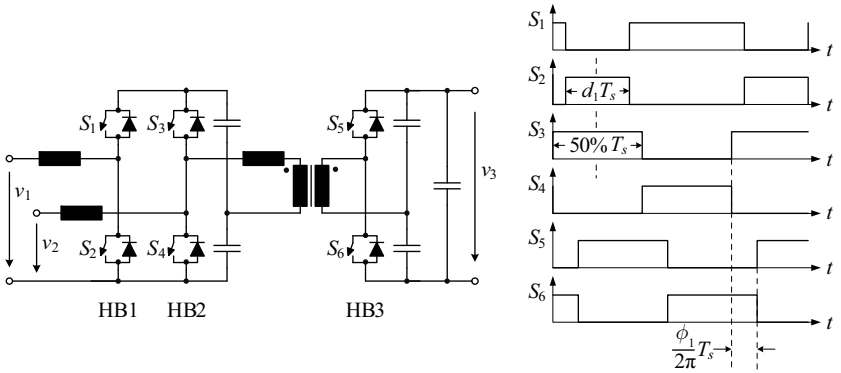
gies have a low parts count of switches, diodes and passive components. However, the need for one or more inductors for each topology results in high costs, a large volume and a slow dynamic response. Another disadvantage is that the topologies are characterized by hard switching.

1.3.2 Partially Isolated Multi-port Topologies

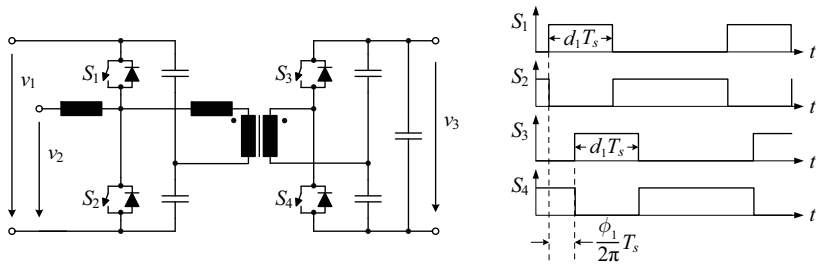
Partially isolated multi-port topologies, where some power ports share a common ground and these power ports are galvanically isolated from the remaining power ports for safety reasons and/or for matching different port voltage levels, are shown in Figure 1.11.

A partially isolated bidirectional multi-input topology was proposed by H. Tao et al. in [37], referred as topology B1 (cf. Figure 1.11(a)). The topology is the integration of a bidirectional boost/buck topology (including the boost/buck inductor for port 1 and the phase leg HB1) and a bidirectional boost-dual-half-bridge topology (including the boost/buck inductor for port 2, the phase legs HB2 and HB3, and the transformer) presented by F. Peng in [74]. This topology is based on the combination of a DC-link and magnetic-coupling, i.e. HB1 and HB2 are linked together by the DC-link capacitor leg and the isolation transformer links HB2 and HB3. HB1 is PWM controlled. HB2 and HB3 are operated in phase shift (PS) mode, i.e. the duty ratios of the switches in HB2 and HB3 are 50%, and the gate signals of the switches in HB3 are shifted by an angle ϕ_1 with respect to those of HB2. Moreover, the PWM carrier singal for HB1 is shifted by 180° compared to that for HB2, leading to a minimum current ripple for the DC-link capacitor leg. Therefore, a relatively small capacitance can be chosen. Thanks to the boost/buck inductors, the topology draws or injects smooth currents from or to the sources/storage devices. However, the switches in HB1 are soft-switched only if the current of the boost/buck indcutor for port 1 is bidirectional over one switching cycle. Otherwise, the diode-to-switch commutation fails and hard-switching occurs. The variations of the voltage levels of ports 2 and 3 impose a certain limitation on the zero-voltage switching (ZVS) operating region for the switches in HB2 and HB3. In [39], the switching conditions for the switches in HB1 *and* HB2 and HB3 are improved by introducing a variable hysteresis band control *and* an asymmetrical wave control, respectively.

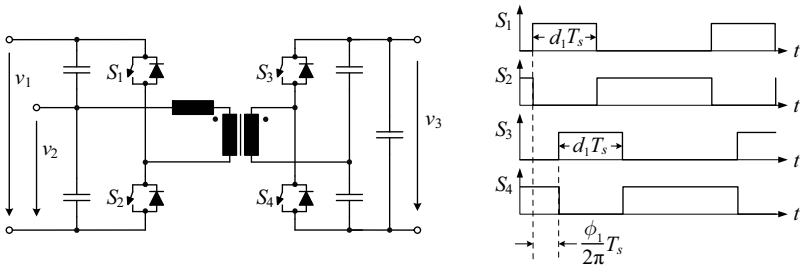
G. Su et al. presented a bidirectional triple-voltage topology in 2005 [69], referred as topology B2 (cf. Figure 1.11(b)). Similar to topology B1,



(a) Topology B1

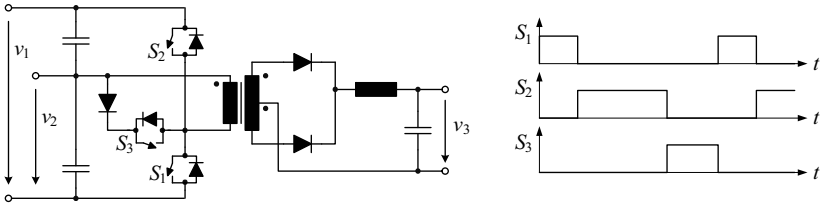


(b) Topology B2

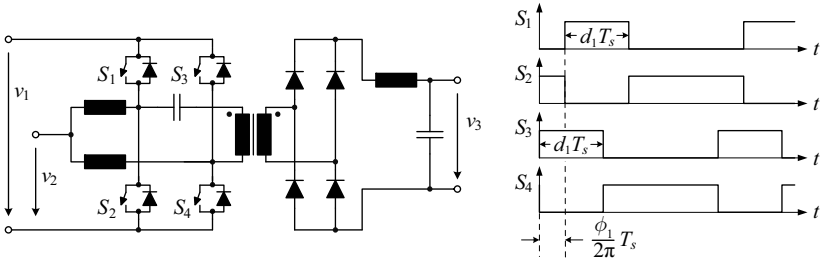


(c) Topology B3

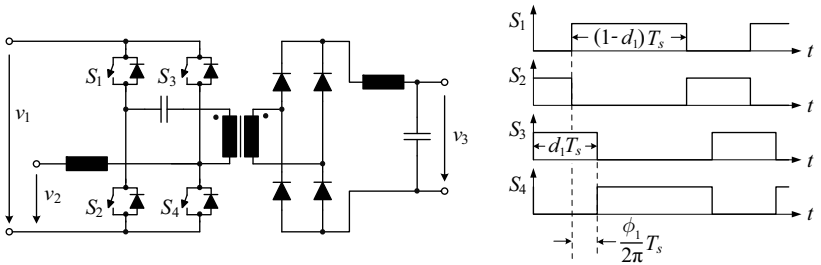
Figure 1.11: (a)-(f) Different partially isolated multi-port topologies and related gate signals of the switches.



(d) Topology B4



(e) Topology B5



(f) Topology B6

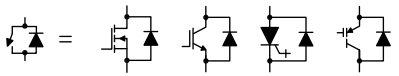


Figure 1.11: (a)-(f) Different partially isolated multi-port topologies and related gate signals of the switches (continued).

Table 1.2: Partially isolated multi-port topologies.

Name	Original topology	Control method	Power flow	DC magnetizing current	Literature
B1	Boost/buck, boost-dual-half-bridge	PS & PWM	bidirectional	No	[37, 39]
B2	Boost-dual-half-bridge	PS & PWM	bidirectional	No	[69]
B3	Dual-half-bridge	PS & PWM	bidirectional	Yes	[71]
B4	Half-bridge	PWM	one bidirectional port	Yes	[40]
B5	Two-phase boost/buck, phase-shift full-bridge	PS & PWM	two bidirectional ports	Yes	[38]
B6	Boost/buck, phase-shift full-bridge	PS & PWM	two bidirectional ports	Yes	[42]

this topology makes use of the combination of a DC-link and a magnetic-coupling to interface three voltage buses. However, the power port 1 of topology B2 is directly drawn out from the terminals of the DC-link capacitor leg, not from the boost/buck inductor for port 1 and the phase leg HB1 as configured in topology B1, resulting in smaller parts count. The power flow between the primary and the secondary side of the transformer is controlled by a shifted angle between the gate signals of $S_1 - S_2$ and those of $S_3 - S_4$. In addition, the duty ratios of the switches are adjusted to maintain the volt-seconds balance of the boost/buck inductor for port 2. With regard to the disadvantage, this topology has higher current stresses, higher conduction losses and switching losses, and smaller ZVS operating region compared to topology A1.

G. Su et al. proposed a reduced-complexity triple-voltage topology in 2007 [71], referred as topology B3 (cf. Figure 1.11(c)). This topology is derived from the bidirectional dual-half-bridge topology and the power port 2 is directly drawn out from the midpoint of the DC-link capacitor leg, eliminating the boost/buck inductor and the filter capacitor for port 2 in topology B2. The power management strategy is similar to that of topology B2. However, the average current of port 2 has to flow through the magnetizing inductance of the transformer since the DC current cannot flow through the capacitors, resulting in a DC flux bias of the transformer which lowers the utilization of the magnetic material. The average current of port 2 also has a small impact on the switching conditions of $S_1 - S_2$.

A tri-modal half-bridge topology was proposed by Al-Atrash et al. in [40], referred as topology B4 (cf. Figure 1.11(d)). This topology is essentially a modified version of the isolated half-bridge topology by adding a free-wheeling circuit branch consisting of a diode and a switch across the primary winding of the transformer. In a constant frequency PWM control scheme, a switching cycle is composed of three basic operation modes, where one and only one switch is turned on at a time. This switching sequence allows the main switches S_1 and S_2 to achieve zero-voltage switching by utilizing the energy of the leakage inductance of the transformer, although the free-wheeling switch S_3 is hard-switched. In addition, the magnetizing inductance of the transformer is used to store energy to interface the sources/storage devices of port 1 and 2, which needs to be considered in designing the transformer.

Furthermore, Al-Atrash et al. developed a soft-switched multi-port

topology in 2006 [38], referred as topology B5 (cf. Figure 1.11(e)). This topology is based on the integration of a two-phase boost/buck unit into the phase-shift full-bridge topology. Two power ports on the primary side of the transformer are bidirectional. The load port can be either unidirectional or bidirectional, depending on whether a diode rectifier or a synchronous rectification is employed. The power delivered to the load is regulated by the phase shift angle between two phase legs in the bridge and the energy flow in the boost/buck unit is controlled by the duty cycles of the switches. A DC magnetizing current appears in the primary side of the transformer in order to compensate the DC component of the primary-reflected load current. Moreover, the current-sharing control ensuring the current balance between two boost/buck inductors would be necessary in the practical circuit, although the duty cycles of two phase legs are required to be equal.

Later in 2007, Al-Atrash presented a similar topology in [42], referred as topology B6 (cf. Figure 1.11(f)). A single-phase boost/buck unit, not a two-phase arrangement as in topology B5, is integrated into the phase-shift full-bridge topology to form the multi-port topology. This allows two phase legs to operate at different duty cycles, i.e. the duty cycle of the leading leg is chosen to be complementary to that of the lagging one in order to increase the voltage gain of the full-bridge section and lower conduction losses compared to topology B5.

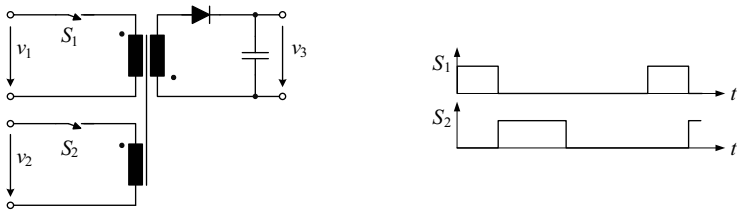
Partially isolated topologies, whose features are summarized in Table 1.2, are based on diverse isolated bridge topologies, such as the bidirectional boost-dual-half-bridge, the bidirectional dual-half-bridge, the half-bridge and the phase-shift full-bridge topology. These topologies can accommodate both a low-voltage input source/storage device and a high-voltage industry load by adjusting the corresponding winding turns ratio of the transformer; accordingly a stacking of many low-voltage cells to support higher voltage can be avoided that reduces costs and complexity. Moreover, the energy flow between two sources/storage devices of port 1 and 2 is controlled by the duty cycles of the switches, where the voltage level of port 1, i.e. V_1 must be higher than that of port 2, i.e. V_2. Furthermore, interleaving the topologies in multiple phases is an effective means to achieve higher power capabilities, and to reduce the port current ripples while their frequency multiplies, and to reduce or even eliminate the DC-link capacitor legs [22, 70, 72, 73, 75].

1.3.3 Fully Isolated Multi-port Topologies

Fully isolated multi-port topologies, where each power port has its own independent reference potential (ground) and the energy transfer between all ports is combined into a single magnetic device, i.e. the isolation transformer, are shown in Figure 1.12.

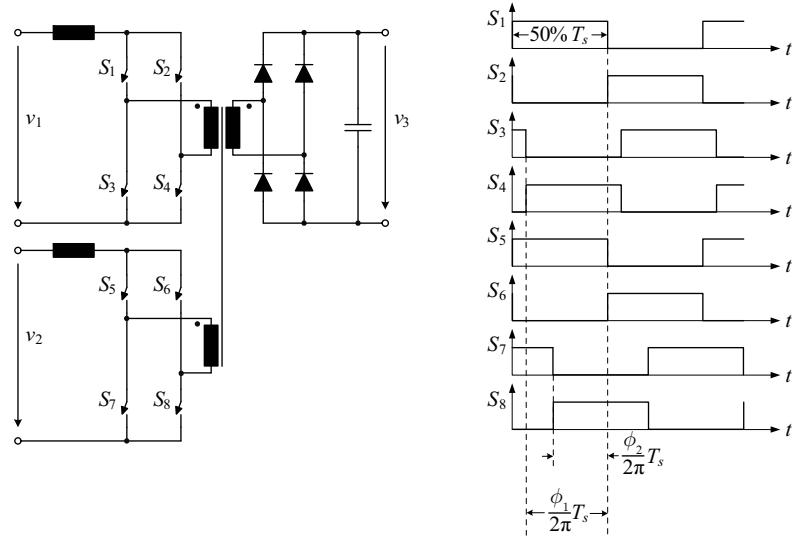
Matsuo et al. proposed a fully isolated two-input topology in [18], referred as topology C1 (cf. Figure 1.12(a)). This topology is essentially a variation of topology A6, i.e. the inductor in topology A6 is replaced by the transformer with a separate winding for each input/output. The operation principles, which are based on the time-sharing concept due to the clamped voltage across the winding of the transformer, are similar to those of topology A6. Hence, the power from the different sources cannot be transferred to the output simultaneously. The disadvantage that the switches S_1 and S_2 are hard-switched is improved in [8] by driving the switches alternately with a phase difference of 180°.

A two-input current-fed topology was developed by Y. Chen et al. in [4], referred as topology C2 (cf. Figure 1.12(b)). This topology is derived from the current-fed full-bridge topology by adding a current-source input-stage and the associated transformer winding. The energy from the input sources is combined by adding up the produced magnetic flux in the magnetic core of the coupled transformer. A phase-shifted PWM control instead of the conventional PWM scheme is used to avoid the transformer winding voltage-clamping problem. The inductor of each input transforms the voltage source into a current source, which implies that the voltage level of the voltage sources can be different. Due to the employment of

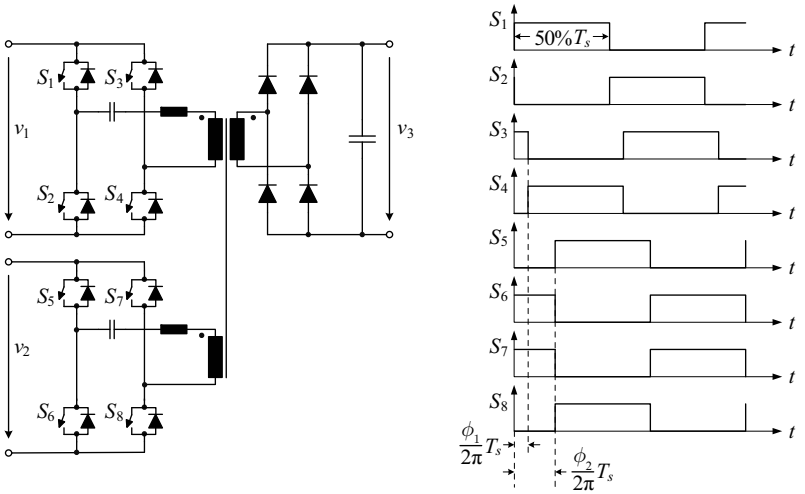


(a) Topology C1

Figure 1.12: (a)-(e) Different fully isolated multi-port topologies and related gate signals of the switches.

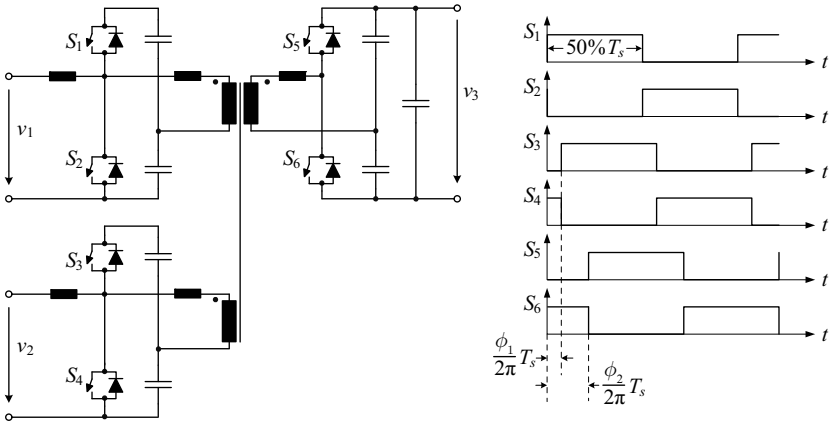


(b) Topology C2

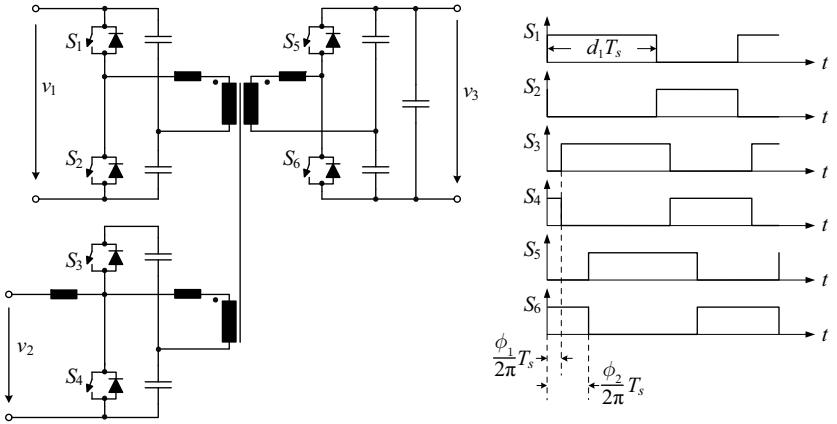


(c) Topology C3

Figure 1.12: (a)-(e) Different fully isolated multi-port topologies and related gate signals of the switches (continued).



(d) Topology C4



(e) Topology C5

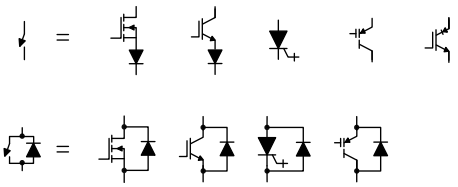


Figure 1.12: (a)-(e) Different fully isolated multi-port topologies and related gate signals of the switches (continued).

Table 1.3: Fully isolated multi-port topologies.

Name	Original topology	Control method	Power flow	DC magnetizing current	Literature
C1	Flyback	PWM	unidirectional	Yes	[8,18]
C2	Current-fed full-bridge	PS	unidirectional	No	[4]
C3	Series resonant	PS	two bidirectional ports	No	[30]
C4	Boost-dual-half-bridge	PS	bidirectional	No	[20]
C5	Boost-dual-half-bridge	PS & PWM	bidirectional	No	[43]

only forward-conducting and bidirectional-blocking switches, this topology has the capability to deliver power to the load from different sources simultaneously, but allows power flow only in one direction. The topology has other features such as the soft-switching accessibility.

A constant switching frequency series resonant multi-port topology was presented by H. Krishnaswami et al. in [30], referred as topology C3 (cf. Figure 1.12(c)). The topology is an extension of the series resonant topology, where two windings of the transformer are connected to full-bridge units through series resonant tank circuits. The phase shift angle between the fundamental components of the output voltages of the full-bridge units and the phase shift angle between two phase legs in one full-bridge are utilized to control the output voltage v_3 and the power drawn/delivered through port 1. The switches can achieve zero-voltage switching in a limited operation range depending on the load condition and the power distribution between ports 1 and 2 when the topology operates above the resonant frequency.

D. Liu et al. developed a multi-input bidirectional topology in [20], referred as topology C4 (cf. Figure 1.12(d)). This topology is viewed as an extension of the boost-dual-half-bridge topology. The leakage inductances of the three-winding transformer determine the power transfer in connection with the phase displacements between the square-wave output voltages of the bridges. The topology presents the natural bidirectional power flow property. Although the existence of the boost inductor reduces the port current ripple, it increases the system cost and size and limits the system bandwidth, thus slows the system dynamic response. For a wide voltage variation, the multi-port topology cannot operate optimally since there are high peak/RMS currents which lead to high conduction losses, and even the loss of soft-switching in some cases.

A triple-half-bridge bidirectional topology based on the boost-dual-half-bridge topology was proposed by H. Tao et al. in [76], referred as topology C5 (cf. Figure 1.12(e)). Similar to topology C4, the phase shift control manages the power flow between the inputs and outputs. Moreover, the operation of the topology is optimized by accommodating a source/storage device/load that has a dynamically changing voltage magnitude by a boost-half-bridge unit and by adjusting the duty ratios of the switches to keep the voltage levels of the capacitor legs constant. However, this topology can only be used in applications where only one source/storage device/load with a widely varying voltage level is inter-

connected since the same duty cycle is used in all half-bridge units and is the only variable that can compensate for the variation of the voltage level.

Fully isolated topologies, whose features are summarized in Table 1.3, are based on diverse isolated bridge topologies by adding an input-/output-stage circuit and associated transformer winding. The high-frequency transformer has multiple functions. It not only integrates and exchanges the energy through all power ports, but also provides full isolation between all sources/storage devices/loads. Different port voltage levels can be matched by suitable turns ratio of the transformer. For some topologies, the large leakage inductances, caused by the imperfect coupling of the windings which are arranged on the same core, can be used for delivering energy transfer, which results in higher power density and be more compact.

1.4 Main Objectives of the Research Work

Even though some multi-port topologies have been proposed, it is observed that only limited research has been conducted in the field of multi-port converters, since:

- Most of the research performed for multi-port converters has focused on the circuit topologies. Those topologies, which are reviewed in Section 1.3, have one or more disadvantages listed in the following:
  - Lack of bidirectional power flow capability, which does not allow to accommodate in the energy storage devices in the systems;
  - Requirement for the high-voltage storage devices formed by stacking many low-voltage cells with voltage balance circuits, which adds to the complexity of the system;
  - No galvanic isolation, which results in topologies not meeting safety requirements in many applications;
  - Need for one or more DC inductors, which increases cost and volume, and slows down the dynamic response;
  - Lack of the capability to transfer power from different sources to outputs simultaneously, which increases the current stresses

of the components and allows a utilization of systems only for low power applications;

- Presence of the DC magnetizing current in the transformer, which leads to a DC flux bias of the transformer, lowers the utilization of the magnetic material and increases the design difficulty of the transformer.

- Very few technical papers have specifically addressed the dynamic response of the converters to changes in the input voltage or in the load with the aim to keep the output voltage constant.

Besides, multi-port converters can find many applications with multiple sources/storage devices/loads. Among these applications, multiple voltage electrical systems in HEVs and FCVs are a typical example, where the multi-port converter interfacing HV/42 V/14 V buses should meet the following requirement:

- Bidirectional power flow capability for all three ports that interconnect voltage buses;
- Electric isolation between the 14 V/42 V buses and the HV bus;
- Low overall system losses in a wide operating range;
- Fast dynamic response in case the load changes;
- High power density.

The main objective of this work is to develop a novel power converter interconnecting multiple ports for multiple voltage electrical systems in HEVs and FCVs. This converter should have the following features:

- Multi-port interfacing capability. Power can flow from/to any port individually and simultaneously;
- Different voltage levels of the different ports adapted by the turns ratios of corresponding transformer windings;
- Electrical isolation between any two ports considering safety requirements;

- Safe start-up without any additional pre-charge circuit in order to minimize the realization effort and system complexity and ensure high power density.

The second main objective of the work is to develop a digital control system for multi-port converters. The control system should meet the following requirements:

- Control of the power transfer between the energy storage devices connected to two system ports. The voltages of the corresponding ports are assumed constant, accordingly the power transfer is controlled by controlling the charging/discharging currents.
- Voltage mode control for the port left without energy storage device. This ensures a constant output voltage independent of the load condition.

1.5 Publications

The results related to the dissertation have been published in international conferences and journals as listed below:

- C. Zhao, S. D. Round, J. W. Kolar, "Full-order averaging modelling of zero-voltage-switching phase-shift bidirectional DC-DC converters" *IET Power Electronics*, vol. 3, no. 3, pp. 400–410, 2010.
- C. Zhao, S. D. Round, J. W. Kolar, "An isolated three-port bidirectional DC-DC converter with decoupled power flow management" *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2443–2453, 2008.
- C. Zhao,S. Round, J. W. Kolar, "Buck and boost start-up operation of a three-port power supply for hybrid vehicle applications," in *Proceeding of IEEE Power Electronics Specialists Conference (PESC)*, pp. 1851–1857, 2005.
- C. Zhao, J. W. Kolar, "A novel three-phase three-port UPS employing a single high-frequency Isolation transformer," in *Proceeding of IEEE Power Electronics Specialists Conference (PESC)*, pp. 4135–4141, 2004.

Chapter 2

Steady-state Analysis of Three-port Converter

In this chapter, the description of the converter topology, the discussion of the operation principle and the analysis of the possibilities of power exchange between the ports are presented.

2.1 Description of the Proposed Converter Topology and the Operation Principle

2.1.1 Proposed Converter Topology

Figure 2.1 shows the proposed isolated three-port bidirectional topology for a multiple voltage electrical system in HEVs and FCVs, which is an extension of the dual-active-bridge (DAB) topology [77].

A traction motor, for example, can be connected to the HV bus (port 1) through an inverter. Energy storages devices, such as batteries and supercapacitors, can be interfaced with the two low voltage buses, i.e. the 42 V bus (port 2) and the 14 V bus (port 3). The HV, the 42 V and the 14 V buses are coupled via a three-winding transformer T_r and corresponding full-bridge units.

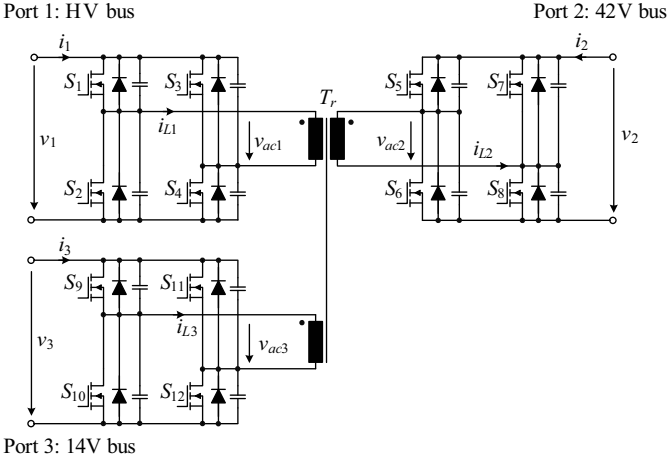


Figure 2.1: Proposed isolated three-port bidirectional converter topology, where high frequency linking of the full-bridge units is realized via a single transformer T_r.

The three-winding transformer T_r plays an important role in this topology. It has the following functions:

- It combines/delivers the energy from/to three voltage buses via magnetic coupling;
- It provides electrical isolation between the voltages buses;
- Different voltage levels of the buses can be matched by suitable turns ratios of the transformer windings.
- The leakage inductances of the transformer are utilized for delivering the energy transfer between the inputs and outputs.

The switches are implemented with MOSFETs. Since the MOSFET is a current-bidirectional two-quadrant switch, the current flowing in a full bridge unit can be bidirectional, i.e. this topology has bidirectional power flow capability. For example, the storage device connected to the 14 V bus can be charged by the energy generated by the motor functioning as a generator (on the HV bus side). On the other hand, it can also provide

power to the components interconnecting to the 42 V bus during start up when needed.

In addition, the leakage inductances of the transformer and the output capacitances of the MOSFETs are utilized to achieve the zero-voltage switching for the MOSFETs, reducing the switching losses and eliminating the body diode reverse recovery process and the potentially resulting over-voltage problem which could lead to breakdown and failure of the MOSFET. No extra active switches or passive components are required.

The zero-voltage switching of the MOSFETs, i.e. the diode-to-switch commutation mechanism, is explained in the following, assuming that a positive current flows through the bottom MOSFET, which is going to be turned off, and this current, which also flows through the transformer leakage inductance, remains constant during the commutation interval:

- Turn off: the conducting bottom MOSFET is turned off, and the positive current is diverted to the associated parasitic output capacitance and which therefore is charged;

- Turn on: at the same time, the diverted current discharges the parasitic output capacitance of the top MOSFET in the same phase leg. Once the capacitance is fully discharged, i.e. the drain-to-source voltage of the top MOSFET passes through zero, the body diode of the top MOSFET becomes forward-biased and the transformer leakage inductance current freewheels through the diode. The top MOSFET can then be forced on at zero voltage, i.e. without inducing turn-on switching losses.

The use of the full-bridge units instead of half-bridge units, which is employed in topology C4 [20] and C5 [76] (cf. Chapter 1), to build the three-port topology is justified as follows.

The cost of the active semiconductor devices is a large share of the overall costs and this suggests to evaluate different topologies by comparing their total device rating TDR, which is defined for a topology containing k switches as

$$TDR = \sum_{j=1}^{k} V_{ds\_j} I_{d\_rms\_j}, \tag{2.1}$$

where V_{ds_j} and $I_{d\_rms\_j}$ are the voltage stress of and the RMS value of the current flowing through a switch j, respectively.

The voltage buses in the multiple-voltage electrical system in HEVs and FCVs can be viewed as DC voltage sources. The voltage-source full-bridge unit, as illustrated in Figure 2.2(a), can selectively generate a a positive, negative or zero voltage using different combinations of the gate signals of the switches, i.e. $v_{ac1} = V_1$ when S_1 and S_4 are turned on, $v_{ac1} = -V_1$ when S_2 and S_3 are in the on-state and $v_{ac1} = 0$ when S_1 and S_3 or S_2 and S_4 are conducting, where V_1 denotes the DC magnitude of the voltage bus v_1. Therefore, each MOSFET in the full-bridge unit is subject to a voltage stress equal to the port voltage level V_1. I_{L1_rms} is the RMS value of the current i_{L1}. The RMS value of the current flowing through each MOSFET is $I_{L1\_rms}/\sqrt{2}$ since each MOSFET in the full-bridge unit conducts for half switching cycle. Therefore, the TDR of the full-bridge unit is

$$\begin{aligned} TDR_{FB} &= \sum_{j=1}^{4} V_{ds\_j} I_{d\_rms\_j} \\ &= 4V_1 \frac{I_{L1\_rms}}{\sqrt{2}} \\ &= 2\sqrt{2}\, V_1 I_{L1\_rms}. \end{aligned} \tag{2.2}$$

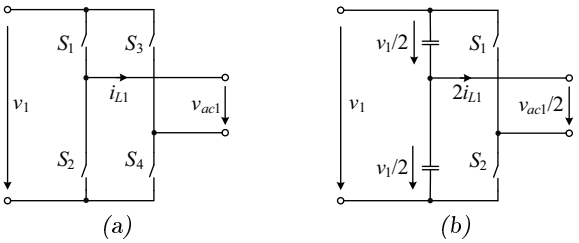


Figure 2.2: Circuit schematic of (a) full-bridge unit and (b) half-bridge unit.

For the half-bridge unit as illustrated in Figure 2.2(b), each MOSFET's voltage stress is still equal to the port voltage level V_1. The DC voltage across each capacitor in the DC-link capacitor leg is $V_1/2$. Therefore, the half-bridge unit generates the high-frequency voltage $v_{ac1}/2$. In

order to transfer same power, the current through the half-bridge unit is twice that through the full-bridge unit. Thus, the RMS value of the current flowing through each MOSFET in the half-bridge unit is equal to $2I_{L1\_rms}/\sqrt{2}$. The TDR of the half-bridge unit is

$$\begin{aligned} TDR_{HB} &= \sum_{j=1}^{2} V_{ds\_j} I_{d\_rms\_j} \\ &= 2V_1 \frac{2I_{L1\_rms}}{\sqrt{2}} \\ &= 2\sqrt{2}\, V_1 I_{L1\_rms}. \end{aligned} \tag{2.3}$$

Therefore, the total device rating is the same for the full-bridge unit and the half-bridge unit at the same output power. But the use of more semiconductor devices instead of passive components like bulky electrolytic capacitors, which is used in combination with high frequency polypropylene capacitors to form DC-link capacitors, allows the full-bridge unit to be more compact.

2.1.2 Modulation Technique

The modulation technique for the proposed topology can be described as follows:

- Each MOSFET operates at a fixed switching frequency and fixed 50% duty ratio. The gate signals of two MOSFETs in the same phase leg are complementary and the diagonal opposite MOSFETs in the same full-bridge unit are turned on and off simultaneously. The gate signals of the switches in the full-bridge unit of the transformer primary side (the HV side), for example, is illustrated in Figure 2.3(b). This voltage-source full bridge unit generates a high frequency square-wave voltage v_{ac1}. In order to simplify the analysis, we represent this full-bridge unit and the voltage bus by a high frequency voltage source, as shown in Figure 2.3(a). Similarly, we can simplify the other two full-bridge units and the associated voltage buses to two voltage sources. Thus the simplified equivalent circuit of the proposed topology (cf. Figure 2.1) can be obtained, as illustrated in Figure 2.4(a).

- The power flow between the voltage buses is controlled by shifting the patterns of the gate signals of the switches in the other two full-bridge units with respect to those in the full-bridge unit of the transformer primary side (the HV side), i.e. by shifting the high-frequency voltages v_{ac2} and v_{ac3} with respect to v_{ac1}, as shown in Figure 2.4(b). The phase shift angle of the voltages v_{ac1} and v_{ac2} is denoted as ϕ_1 in the following; accordingly, ϕ_2 denotes the phase displacement of v_{ac1} and v_{ac3}. There, ϕ_1 and/or ϕ_2 are defined as positive when v_{ac1} is leading v_{ac2} and/or v_{ac1} is leading v_{ac3}. The control range of ϕ_1 and ϕ_2 is from $-\pi$ to π.

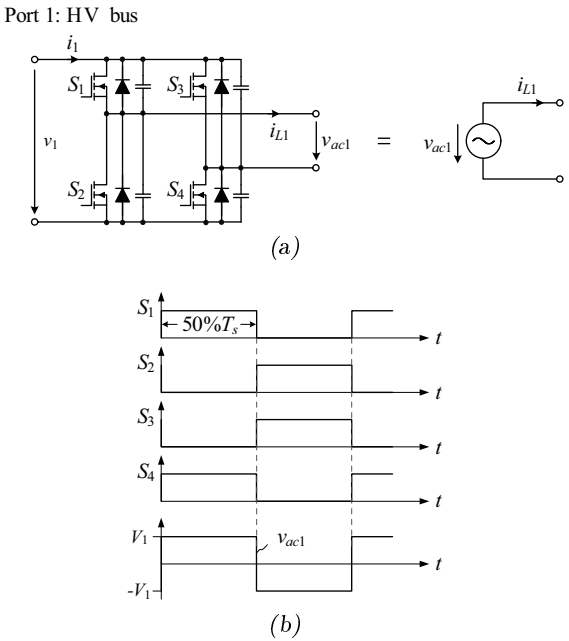


Figure 2.3: (a) High-frequency voltage source representing the full-bridge unit and the associated voltage bus; (b) Idealized gate signals waveforms and high-frequency voltage waveform v_{ac1}, which is determined by the pattern of the switch gate signals and the port voltage level V_1.

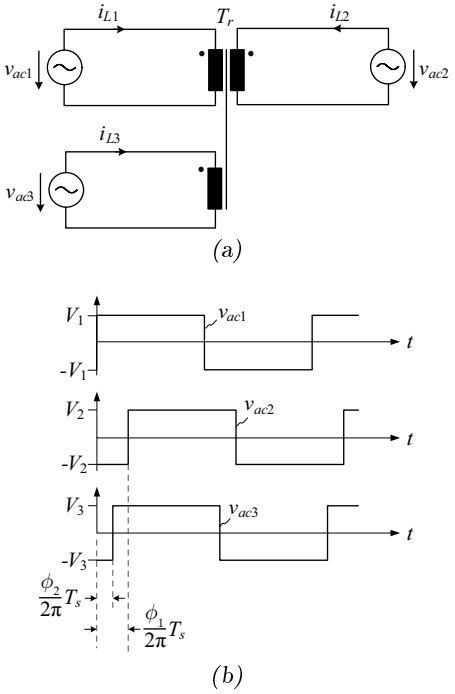


Figure 2.4: (a) Simplified equivalent circuit of the proposed topology (cf. Figure 2.1); (b) Idealized high-frequency voltages v_{ac1}, v_{ac2} and v_{ac3}, where ϕ_1 *and* ϕ_2 denote the phase displacement of v_{ac1} and v_{ac2} *and* v_{ac1} and v_{ac3}, respectively.

2.1.3 Equivalent Circuit of the Proposed Topology

The simplified equivalent circuit of the three-winding transformer T_r is shown in Figure 2.5 [79], where T_1 and T_2 are two ideal two-winding transformers with turns ratios $1 : n_1$ and $1 : n_2$, L_m is the effective magnetizing inductance, L_1, L_2, and L_3 are the leakage inductances.

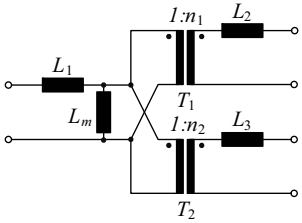


Figure 2.5: Simplified equivalent circuit of the three-winding transformer T_r [79].

The magnetizing inductance L_m of the transformer is usually much larger than the leakage inductances. Thus, the magnetizing inductance L_m can be neglected on a first step.

The resulting equivalent circuit of the proposed topology (cf. Figure 2.1) referred to the transformer primary side (the HV side) is shown in Figure 2.6, where the suffix $_r$ indicates that all voltages, currents and impedances are referred to the transformer primary side, i.e. $L_{1r} = L_1$, $i_{L1r} = i_{L1}$, $v_{L1r} = v_{L1}$, $v_{ac1r} = v_{ac1}$, $V_{1r} = V_1$, $L_{2r} = L_2/n_1^2$, $i_{L2r} = i_{L2}n_1$, $v_{L2r} = v_{L2}/n_1$, $v_{ac2r} = v_{ac2}/n_1$, $V_{2r} = V_2/n_1$, and $L_{3r} = L_3/n_2^2$, $i_{L3r} = i_{L3}n_2$, $v_{L3r} = v_{L3}/n_2$, $v_{ac3r} = v_{ac3}/n_2$, $V_{3r} = V_3/n_2$, V_2 and V_3 indicate the voltage levels of ports 2 and 3, v_{L1}-v_{L3} and i_{L1}-i_{L3} denote the voltages and currents of the leakage inductances L_1-L_3.

It is observed that the leakage inductances L_{1r}, L_{2r} and L_{3r} of the transformer are delivering the energy transfer between the high frequency voltage sources in combination with V_1-V_3 and ϕ_1 and ϕ_2.

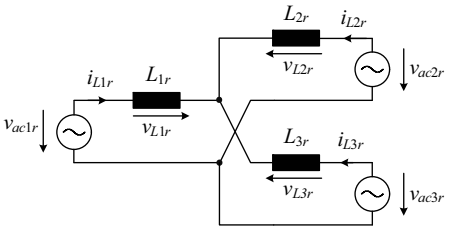


Figure 2.6: Simplified Y-type equivalent circuit of the proposed topology (cf. Figure 2.1) referred to the transformer primary side.

2.2 Power Transfer between the Ports

2.2.1 Power Transfer between Two Ports

When the third port is left open, the three-port circuit can be simplified to a two-port circuit, whose primary-referred equivalent circuit is shown in Figure 2.7, .

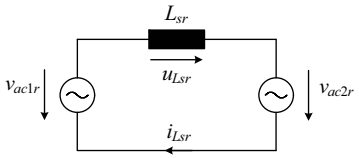


Figure 2.7: Simplified primary-referred equivalent circuit for studying the energy transfer between two ports when the third port is left open.

The energy transfer principle can be easily explained by studying the simplified primary-referred equivalent circuit (cf. Figure 2.7):

- The inductance L_{sr}, which is the sum of the primary and secondary leakage inductances, is utilized for delivering the energy transfer between the two voltage sources.
- The voltage sources generate two square-wave voltages v_{ac1r} and v_{ac2r} which are applied to the two sides of the inductance L_{sr}. The voltage difference voltage $v_{Lsr} = v_{ac1r}$ - v_{ac2r} determines the waveform of the inductance current i_{Lsr}.

- The inductance current i_{Lsr} is a pure AC current when the converter has reached a steady-state operation. The switching of the full-bridge unit on the primary and the secondary side translates this AC current into the port currents i_{1r} and i_{2r}.

2.2.2 Operating Characteristics of the Two-port Converter

In order to derive the operating characteristics of the two-port circuit, it is assumed that the switching is instantaneous, i.e. the current is diverted from one switch to the other switch of a phase leg instantaneously.

Analytical Expression of the Inductance Current $i_{Lsr}(t)$

The idealized voltage and current waveforms of the two-port circuit for the case of v_{ac1r} leading v_{ac2r} are shown in Figure 2.8.

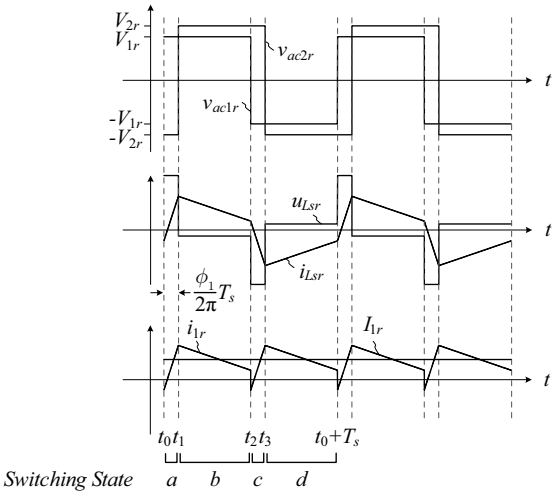


Figure 2.8: Idealized voltage and current waveforms of the two-port circuit for v_{ac1r} leading v_{ac2r}.

There are four switching states (a, b, c and d) in one switching cycle.

The inductance current i_{Lsr} is a function of time:

$$i_{Lsr}(t) = \frac{v_{ac1r}(t) - v_{ac2r}(t)}{L_{sr}}(t - t_i) + i_{Lsr}(t_i) \qquad t_i \leq t \leq t_j, \tag{2.4}$$

where t_i and t_j are the starting and ending time instants of each switching state, and $i_{Lsr}(t_i)$ is the initial current of each switching state.

From the Figure 2.8 and (2.4), the inductance current i_{Lsr} can be found to be:

- Switching state a: $t_0 \leq t \leq t_1$

$$i_{Lsr}(t) = \frac{V_{1r} + V_{2r}}{L_{sr}}(t - t_0) + i_{Lsr}(t_0), \tag{2.5}$$

  where $t_1 = t_0 + (\phi_1 T_s)/(2\pi)$ and T_s indicates the switching cycle;

- Switching state b: $t_1 \leq t \leq t_2$

$$i_{Lsr}(t) = \frac{V_{1r} - V_{2r}}{L_{sr}}(t - t_1) + i_{Lsr}(t_1), \tag{2.6}$$

  where $t_2 = t_0 + T_s/2$;

- Switching state c: $t_2 \leq t \leq t_3$

$$i_{Lsr}(t) = \frac{-V_{1r} - V_{2r}}{L_{sr}}(t - t_2) + i_{Lsr}(t_2), \tag{2.7}$$

  where $t_3 = t_2 + (\phi_1 T_s)/(2\pi)$;

- Switching state d: $t_3 \leq t \leq t_0 + T_s$

$$i_{Lsr}(t) = \frac{-V_{1r} + V_{2r}}{L_{sr}}(t - t_3) + i_{Lsr}(t_3). \tag{2.8}$$

Due to the odd symmetry of the waveform of i_{Lsr}

$$\begin{aligned} i_{Lsr}(t_0 + T_s/2) &= i_{Lsr}(t_2) = -i_{Lsr}(t_0) \\ i_{Lsr}(t_1 + T_s/2) &= i_{Lsr}(t_3) = -i_{Lsr}(t_1), \end{aligned} \tag{2.9}$$

we can solve for $i_{Lsr}(t_0)$, $i_{Lsr}(t_1)$, $i_{Lsr}(t_2)$ and $i_{Lsr}(t_3)$ from (2.5), (2.6)

and (2.9)

$$\begin{aligned} i_{Lsr}(t_0) = -i_{Lsr}(t_2) = -\frac{(V_{1r} - V_{2r})\pi + 2V_{2r}\phi_1}{4\pi f_s L_{sr}} \\ i_{Lsr}(t_1) = -i_{Lsr}(t_3) = \frac{(V_{2r} - V_{1r})\pi + 2V_{1r}\phi_1}{4\pi f_s L_{sr}}, \end{aligned} \tag{2.10}$$

where $f_s = 1/T_s$ denotes the switching frequency.

Substituting (2.10) into (2.5), (2.6), (2.7) and (2.8), we can obtain the complete analytical expression of the inductance current i_{Lsr}(t).

Direction and Amount of the Power Flow

The average active power P_{12} delivered from port 1 (v_{ac1r}) to port 2 (v_{ac2r}) via two phase-shift controlled full-bridge units within one switching cycle T_s can be derived based on the mathematical expression of i_{Lsr}(t)

$$\begin{aligned} P_{12} &= V_{1r} I_{1r} \\ &= V_{1r}(\frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{1r}(t)dt) \\ &= V_{1r}[\frac{2}{T_s}(\int_{t_0}^{t_1} i_{Lsr}(t)dt + \int_{t_1}^{t_2} i_{Lsr}(t)dt)] \\ &= \frac{\phi_1(\pi - \phi_1)V_{1r}V_{2r}}{2\pi^2 f_s L_{sr}}, \end{aligned} \tag{2.11}$$

where I_{1r} denotes the DC current magnitude of port 1 referred to the transformer primary side.

A similar analysis for the case where the square-wave voltage v_{ac2r} leads v_{ac1r}.

The general expression of the power P_{12} for both cases is

$$P_{12} = \frac{\phi_1(\pi - |\phi_1|)V_{1r}V_{2r}}{2\pi^2 f_s L_{sr}}. \tag{2.12}$$

According to (2.12), the power P_{12} as a function of the phase shift angle ϕ_1 is illustrated in Figure 2.9. The maximum power P_{12} of the two-

Table 2.1: Operating parameters of the power stage in the two-port converter.

Description	Parameter
Port 1 dc voltage	$V_1 = 14$ V
Port 2 dc voltage	$V_2 = 300$ V
Transformer turns ratio	$n_1 = 20$
Sum of leakage inductances	$L_{sr} = 160$ nH
Switching frequency	$f_s = 100$ kHz

port converter is found for $\phi_1 = \pi/2$. It is interesting to notice that the direction of the power flow P_{12} is determined by the sign of the phase shift angle ϕ_1, i.e. a positive value of the phase shift angle indicates that a power is delivered from port 1 (v_{ac1r}) to port 2 (v_{ac2r}) and a negative value denotes a power transfers from port 2 (v_{ac2r}) to port 1 (v_{ac1r}).

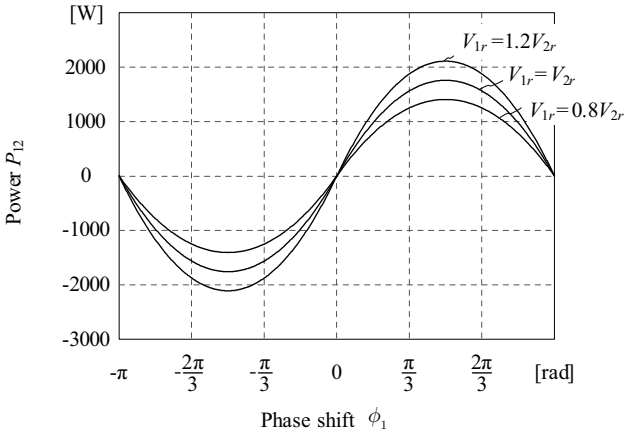


Figure 2.9: Power P_{12} versus phase shift angle ϕ_1 with parameters as given in Table 2.1.

This is also clear from the fundamental phasor diagram of the voltages and currents, which is depicted in Figure 2.10 (a) and (b), where $\underline{v}_{ac1r}$, $\underline{v}_{ac2r}$, $\underline{v}_{Lsr}$ and $\underline{i}_{Lsr}$ are the fundamental phasors of v_{ac1r}, v_{ac2r}, v_{Lsr} and i_{Lsr}, and α denotes the phase displacement of the phasors $\underline{v}_{ac1r}$ and $\underline{i}_{Lsr}$; $\underline{v}_{Lsr} = \underline{v}_{ac1r} - \underline{v}_{ac2r}$ and $\underline{i}_{Lsr}$ is oriented perpendicular to $\underline{v}_{Lsr}$.

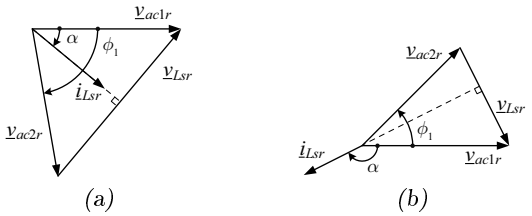


Figure 2.10: Fundamental phasor diagram of the voltages and currents of the two-port circuit (a) $\phi_1 > 0$ and (b) $\phi_1 < 0$.

The fundamental active power P_{12_f} is

$$P_{12\_f} = \frac{1}{2}\hat{U}_{1r}\hat{I}_{Lsr}\cos(\alpha), \tag{2.13}$$

where $\hat{U}_{1r} = 4V_{1r}/\pi$ and $\hat{I}_{Lsr}$ are the amplitudes of the voltage phasor $\underline{v}_{ac1r}$ and the current phasor $\underline{i}_{Lsr}$, respectively.

For $\phi_1 > 0$ (cf. Figure 2.10(a)), in case v_{ac1r} is leading v_{ac2r}, α is smaller than $\pi/2$. Therefore, we have $P_{12\_f} > 0$, the power flow is physically oriented from port 1 (v_{ac1r}) to port 2 (v_{ac2r}) and it reverses for $\phi_1 < 0$ since α then is larger than $\pi/2$ (cf. Figure 2.10(b)).

Optimization of the Ration of Voltage Levels V_{1r} and V_{2r}

Let's go back to the case where the square-wave voltage v_{ac1r} leads v_{ac2r}. According to (2.11), the phase shift angle ϕ_1 to deliver power P_{12} from port 1 to port 2 can be predicted as

$$\phi_1 = (\frac{\pi}{2} - \frac{\pi\sqrt{V_{1r}^2V_{2r}^2 - 8P_{12}V_{1r}V_{2r}f_sL_{sr}}}{2V_{1r}V_{2r}}). \tag{2.14}$$

Figure 2.11 shows the dependency of the phase shift angle ϕ_1 on the voltage level V_{1r}. It is observed that for transferring a constant amount of power required, the phase shift angle ϕ_1 decreases with voltage level V_{1r}.

Another quantity to be considered is the peak value of the inductance current (absolute value). Combining the initial current (2.10) of

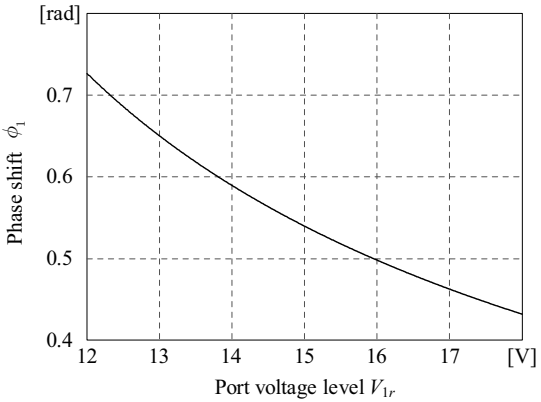


Figure 2.11: Dependency of the phase shift angle ϕ_1 on the voltage level V_{1r} for transferring a constant amount of power $P_{12} = 1$ kW; other parameters as given in Table 2.1.

each switching state and (2.14), the peak value i_{Lsr_peak} of the inductance current within one switching cycle can be calculated as a function of the voltage level V_{1r}, resulting in Figure 2.12. Accordingly, the optimal for relationship of the voltage levels would be $V_{1r} = V_{2r}$ where the peak value of the inductance current is minimal. This is important for improving the circuit efficiency because the power losses are closely related to the peak value of the inductance current i_{Lsr_peak}.

2.2.3 Direction and Amount of the Power Flow in the Three-port Converter

The Y-type primary-referred equivalent circuit depicted in Figure 2.6 can be transformed into a Δ-type equivalent circuit shown in the Figure 2.13, where $L_{12r} = L_k/L_{3r}$, $L_{13r} = L_k/L_{2r}$, $L_{23r} = L_k/L_{1r}$ and $L_k = L_{1r}L_{2r} + L_{1r}L_{3r} + L_{2r}L_{3r}$. It should be noted that the Δ-type and Y-type equivalent circuits are developed for different usage. The Δ-type equivalent circuit is suitable to analyze the power flow between three ports. On the other hand, the Y-type equivalent circuit is convenient for the switching-condition analysis and the losses calculation.

Now the resulting power flow of the three-port circuit can be deter-

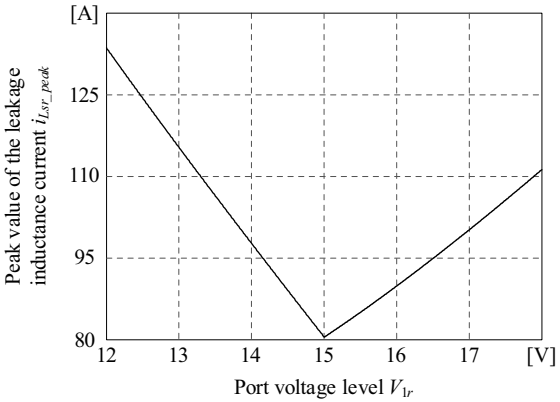


Figure 2.12: Peak value of the inductance current i_{Lsr_peak} within one switching cycle versus voltage level V_{1r} when transferring a constant power $P_{12} = 1$ kW; other parameters as given in Table 2.1.

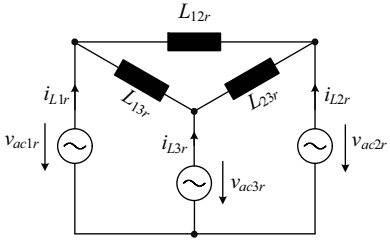


Figure 2.13: Δ-type primary-referred equivalent circuit of the proposed topology (cf. Figure 2.1).

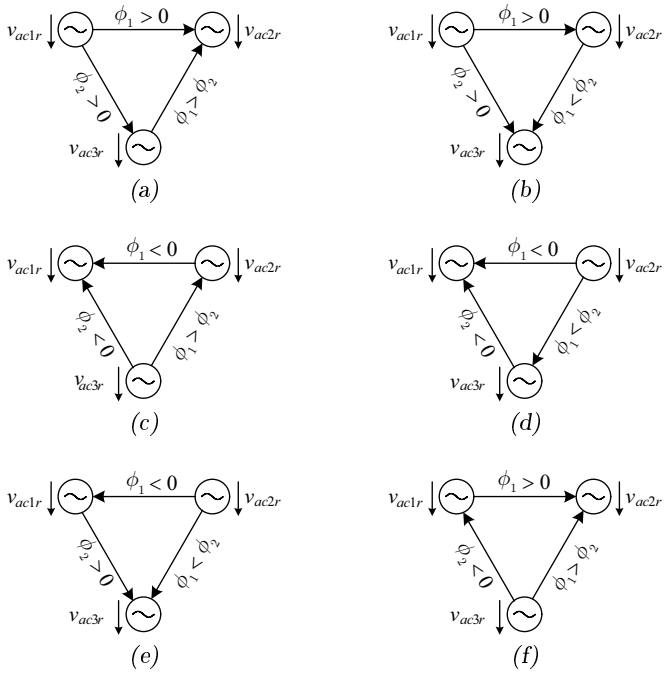


Figure 2.14: Equivalent circuit for studying the power flow between the three ports. The direction of power flow is only determined by the phase shift angles ϕ_1 and ϕ_2, not by the voltage levels V_{1r}, V_{2r} and V_{3r}.

mined by superposition of the power transfer of three two-port circuits v_{ac1r},v_{ac2r}, v_{ac1r},v_{ac3r}, and v_{ac2r},v_{ac3r}. For example, for $\phi_1 > 0$, $\phi_2 > 0$ and $\phi_1 > \phi_2$ (cf. Figure 2.14 (a)), the power flow is from port 1 (v_{ac1r}) to port 2 (v_{ac2r}), from port 1 (v_{ac1r}) to port 3 (v_{ac3r}), and from port 3 (v_{ac3r}) to port 2 (v_{ac2r}). Therefore, port 1 (v_{ac1r}) is acting as a source and port 2 (v_{ac2r}) is consuming power. Dependent on the relationship of ϕ_1 and ϕ_2, port 3 (v_{ac3r}) can be sinking or sourcing power or remain at zero power.

In summary, a power transfer is possible in any direction between any two ports and the direction is only determined by ϕ_1, ϕ_2, not by V_{1r}, V_{2r} and V_{3r} (cf. Figure 2.14).

According to (2.12), the power transferred from port 1 (v_{ac1r}) to port 2 (v_{ac2r}), from port 1 (v_{ac1r}) to port 3 (v_{ac3r}) and from port 2 (v_{ac2r}) to port 3 (v_{ac3r}), denoted as P_{12}, P_{13} and P_{23} in the following, is

$$\begin{aligned} P_{12} &= \frac{\phi_1(\pi - |\phi_1|)V_{1r}V_{2r}}{2\pi^2 f_s L_{12r}} \\ P_{13} &= \frac{\phi_2(\pi - |\phi_2|)V_{1r}V_{3r}}{2\pi^2 f_s L_{13r}} \\ P_{23} &= -\frac{(\phi_1 - \phi_2)(\pi - |\phi_1 - \phi_2|)V_{2r}V_{3r}}{2\pi^2 f_s L_{23r}}. \end{aligned} \tag{2.15}$$

Moreover, we have the active power transferred via the ports P_1, P_2 and P_3

$$\begin{aligned} P_1 &= P_{12} + P_{13} \\ P_2 &= P_{21} + P_{23} \\ &= -P_{12} + P_{23} \\ P_3 &= P_{31} + P_{32} \\ &= -P_{13} - P_{23}. \end{aligned} \tag{2.16}$$

The dependency of the input/output active power P_1, P_2 and P_3 on the the phase shift angles ϕ_1 and ϕ_2 is illustrated in Figure 2.15, where a positive power value indicates that the corresponding port acts as a source and a negative power value marks that the power is consumed by the corresponding port. It is observed that the maximum input power from port 1 P_1 is found when the phase shift angles ϕ_1 and ϕ_2 are both $\pi/2$,

i.e. when the partial power flows delivered from port 1 to ports 2 and 3, P_{12} and P_{13}, reach their maximum values.

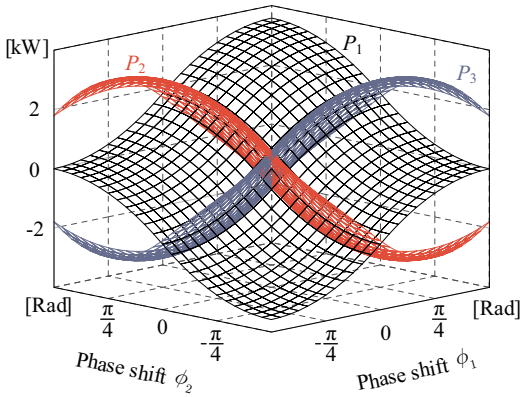


Figure 2.15: Dependency of the input/output active power, P_1, P_2 and P_3, on the phase shift angles ϕ_1 and ϕ_2; parameters as given in Table 2.2.

2.2.4 Three-port Converter with One Port at Zero Average Power

An important feature of the three-port converter is to directly supply power from one port, e.g. port 1, to another port, e.g. port 2, without charging or discharging the energy storage element located at the third port, e.g. port 3. This cannot be realized when the magnitude of v_{ac3r} is lower than that of v_{ac1r} and/or v_{ac2r} even if all power transistors of the port 3 full-bridge unit are remaining in the off-state as the anti-parallel free-wheeling diodes would be forced into conduction by v_{ac1r} and/or v_{ac2r}. Therefore, ϕ_1 and ϕ_2 must be selected properly in order to achieve $P_3 = 0$ and a given value of $P_1 = -P_2 = P$ (since the sum of the power of three ports has to be zero, $P_1 + P_2 + P_3 = 0$, if all losses are neglected).

From (2.16), now the relation of P_1, ϕ_1, and ϕ_2 can be derived under the side conditions $P_3 = 0$ and $P_1 = -P_2 = P$. Figure 2.16 shows an according example operating point; there are two solutions (ϕ_{11}, ϕ_{21}) and (ϕ_{12}, ϕ_{22}) for ϕ_1 and ϕ_2. As a set of higher phase shift angle values (ϕ_{12}, ϕ_{22}) results in a higher peak value of the leakage inductance current

and/or in higher conduction and switching losses, the lower phase shift angle values (ϕ_{11}, ϕ_{21}) are advantageously selected for the system control.

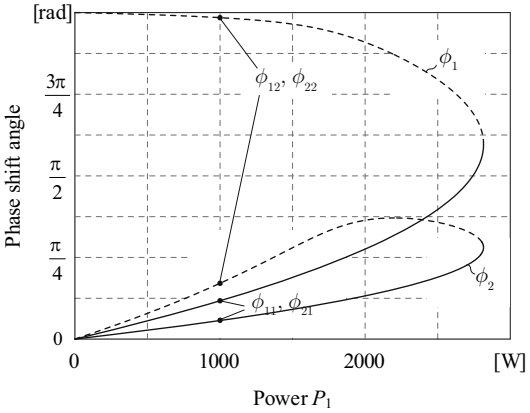


Figure 2.16: Phase shift angles ϕ_1 and ϕ_2 for achieving $P_1 = -P_2 = 1$ kW and $P_3 = 0$ W; parameters as given in Table 2.2.

2.3 Simulation Results

Digital simulations of the steady-state operation of the three-port converter under open-loop control of the phase shift angles have been implemented using SIMPLORER. There, the converter, whose circuit schematic is illustrated in Figure 2.1 (associated circuit parameters are given in Table 2.2), is connected to three different voltage sources.

Two operating points were studied: ($\phi_{1a} = 0.488$, $\phi_{2a} = 0.381$) and ($\phi_{1b} = 0.369$, $\phi_{2b} = 0.178$). Steady-state simulation waveforms for the operating point a and b are illustrated in Figure 2.17 and the Figure 2.18, respectively:

- the voltages of the phase leg outputs, v_{ac1}, v_{ac2} and v_{ac3};
- the leakage inductance current of each winding, i_{L1}, i_{L2} and i_{L3};
- the input/output port currents and their associated average values, i_1 and I_1, i_2 and I_2, i_3 and I_3.

Table 2.2: Circuit parameters of the three-port converter power stage.

Description	Parameter
Port 1 dc voltage	$V_1 = 300$ V
Port 2 dc voltage	$V_2 = 42$ V
Port 3 dc voltage	$V_3 = 14$ V
Transformer turns ratios	$n_1 = 3/20$
	$n_2 = 1/20$
Leakage inductances	$L_1 = 22$ μH
	$L_2 = 495$ nH
	$L_3 = 55$ nH
Switching frequency	$f_s = 100$ kHz

The resulting port power values for operating point a are $P_1 = 1.5$ kW, $P_2 =$ -1.0 kW, and $P_3 =$ -0.5 kW; for operating point b we have $P_1 = 1.0$ kW, $P_2 =$ -1.0 kW and $P_3 = 0$ kW. This verifies that with properly selected phase shift angle values a power transfer in any direction between the three ports is possible where any port also could remain at zero average power.

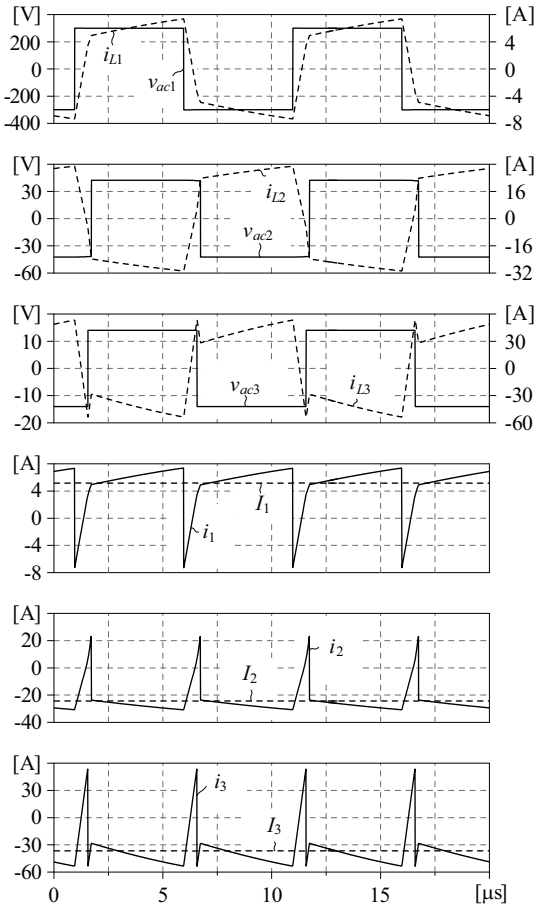


Figure 2.17: Steady-state simulation waveforms for operating point a (ϕ_{1a} = 0.488, ϕ_{2a} = 0.381), resulting in P_1 = 1.5 kW, P_2 = -1.0 kW and P_3 = -0.5 kW.

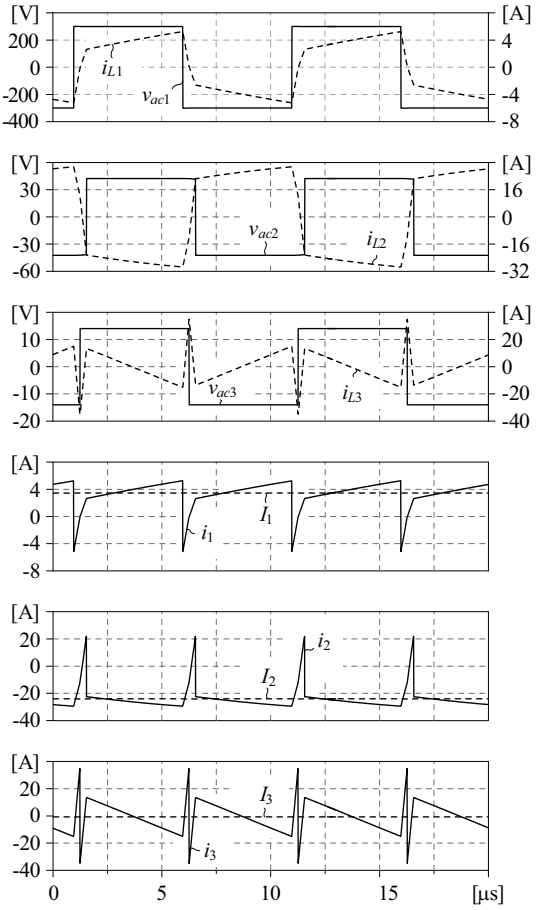


Figure 2.18: Steady-state simulation waveforms for operating point b (ϕ_{1b} = 0.369, ϕ_{2b} = 0.178), resulting in P_1 = 1.0 kW, P_2 = -1.0 kW and P_3 = 0 kW.

2.4 Summary

In this chapter, an isolated three-port bidirectional converter topology, which consists of three full-bridge units and a high frequency three-winding transformer, is proposed. This topology enables a power transfer from any port to the other two ports. In addition, the leakage inductances of the transformer and the output capacitances of the MOSFETs are utilized to achieve zero-voltage switching for the MOSFETs.

The steady-state analysis of the proposed topology is performed based on a derived Δ-type primary-referred equivalent circuit. There, by properly adjusting the phase shift angle values, an independent power flow control between any two ports can be achieved while the power flow to the third port is not affected.

Chapter 3

Optimization of the Three-port Converter Operating Point

3.1 Introduction

The transformer plays an important role in the proposed three-port converter. As mentioned in Section 2.1, one function is to match the different voltage levels of the ports by the suitable turns ratios. However, in case a port voltage varies in a wide range, the three-port converter can not always operate optimally since there are high peak/rms current values occur, which lead to high conduction losses, and even the loss of soft-switching in some cases.

Accordingly, an improved control method has been presented recently in [78], where the duty cycle of one port is adjusted according to its voltage level. However, soft-switching is lost immediately when more than one power source/storage element is involved. The idea in [76] is that a three-port converter composed of half-bridge cells instead of full-bridge cells operates with phase shift and pulsewidth modulation techniques. Again, this converter can only be used in applications where only one power source/storage element is interconnected since the same duty cycle

is used in all half-bridge cells and the duty cycle is the only variable which can compensate for the variation of the voltage level.

This chapter presents an optimization method, i.e. a new modulation technique, with the aim to achieve minimum overall system losses and/or high efficiency of the power transfer.

3.2 Introduction of Duty Cycle Control

In order to gain degrees of freedom for optimizing the operating behavior, a duty cycle variation of the full-bridge unit output voltages v_{ac1r}, v_{ac2r} and v_{ac3r} is introduced in addition to the phase shift control as shown in Figure 3.1. The control range of δ_1, δ_2 and δ_3 is from 0 to $\pi/2$.

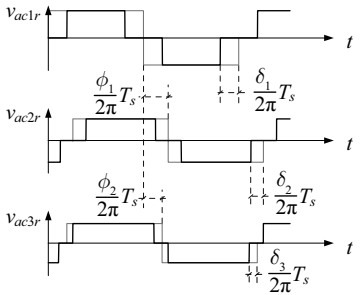


Figure 3.1: Definition of phase displacements and duty cycles of the full-bridge unit output voltages v_{ac1r}, v_{ac2r} and v_{ac3r}.

Here, each MOSFET still operates at a fixed switching frequency and keeps the 50% duty ratio. However, the diagonal opposite MOSFETs in the same full-bridge unit, e.g. S_1 and S_4, are not turned on and off simultaneously any more, as shown in Figure 3.2; but, the gate signal of the MOSFET S_4 is lagging the control signal of MOSFET S_1 by $\delta_1/\pi T_s$, resulting in a rectangular-wave output voltage v_{ac1r} with a time span of the positive/negative voltage pulse of $(1/2 - \delta_1/\pi)T_s$.

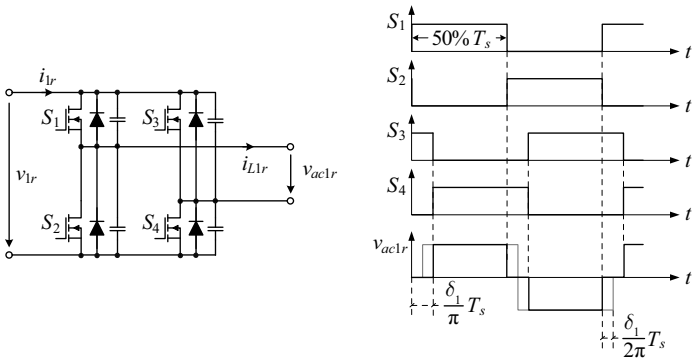


Figure 3.2: Idealized gate signals waveforms and high-frequency voltage waveform v_{ac1r} with a time span of the positive/negative voltage pulse $(1/2 - \delta_1/\pi)T_s$.

3.3 Avoiding Circulation of the Active Power inside the Converter

3.3.1 Fundamental Frequency Representation of the Power

For the sake of simplicity the further considerations are restricted to the fundamental components of the voltages, currents and corresponding active power values, i.e.

$$\begin{aligned} P_{12} &\approx P_{12\_f} \\ P_{23} &\approx P_{23\_f} \\ P_{13} &\approx P_{13\_f}. \end{aligned} \tag{3.1}$$

Furthermore, it is assumed that the leakage inductances L_1, L_2 and L_3 are identical, i.e.

$$L_{12r} = L_{13r} = L_{23r}. \tag{3.2}$$

The corresponding phasor diagram is shown in Figure 3.3 where $\underline{v}_{ac1r}$

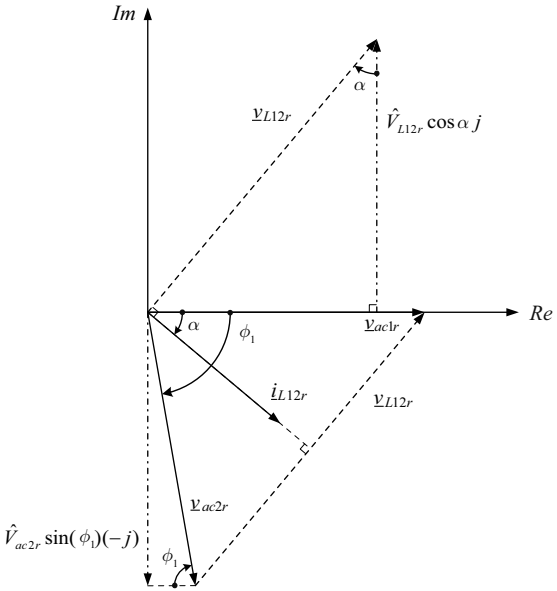


Figure 3.3: Phasor diagram for the converter voltages and currents.

defines the orientation of the real axis

$$\underline{v}_{ac1r} = \hat{V}_{ac1r} + 0j. \tag{3.3}$$

Considering the phase displacement ϕ_1 of v_{ac1r} and v_{ac2r}, i.e. of $\underline{v}_{ac1r}$ and $\underline{v}_{ac2r}$, $\underline{v}_{ac2r}$ can be expressed as

$$\underline{v}_{ac2r} = \hat{V}_{ac2r}\cos(\phi_1) - \hat{V}_{ac2r}\sin(\phi_1)j. \tag{3.4}$$

Accordingly, $\underline{v}_{L12r}$ formed by $\underline{v}_{ac1r}$ and $\underline{v}_{ac2r}$ is

$$\begin{aligned} \underline{v}_{L12r} &= \underline{v}_{ac1r} - \underline{v}_{ac2r} \\ &= \hat{V}_{ac1r} - \hat{V}_{ac2r}\cos(\phi_1) + \hat{V}_{ac2r}\sin(\phi_1)j. \end{aligned} \tag{3.5}$$

Introducing the phase displacement α of $\underline{v}_{ac1r}$ and $\underline{i}_{L12r}$, $\underline{v}_{L12r}$, which

is leading $\underline{i}_{L12r}$ by $\pi/2$, can be alternatively formulated as

$$\begin{aligned}\underline{v}_{L12r} &= \hat{V}_{L12r}\cos\left(\frac{\pi}{2}-\alpha\right)+\hat{V}_{L12r}\sin\left(\frac{\pi}{2}-\alpha\right)j \\ &= \hat{V}_{L12r}\sin(\alpha)+\hat{V}_{L12r}\cos(\alpha)j.\end{aligned} \tag{3.6}$$

Combining (3.5) and (3.6) results in

$$\hat{V}_{ac2r}\sin(\phi_1) = \hat{V}_{L12r}\cos(\alpha). \tag{3.7}$$

Considering (3.7), the power flow P_{12} now can be represented as

$$\begin{aligned}P_{12} \approx P_{12\_f} &= \frac{1}{2}\hat{V}_{ac1r}\hat{I}_{L12r}\cos(\alpha) \\ &= \frac{1}{2}\hat{V}_{ac1r}\frac{\hat{V}_{L12r}}{2\pi f_s L_{12r}}\cos(\alpha) \\ &= \frac{\hat{V}_{ac1r}}{4\pi f_s L_{12r}}\hat{V}_{L12r}\cos(\alpha) \\ &= \frac{\hat{V}_{ac1r}\hat{V}_{ac2r}\sin(\phi_1)}{4\pi f_s L_{12r}}.\end{aligned} \tag{3.8}$$

Furthermore, the full-bridge unit output voltages v_{ac1r} and v_{ac2r} (cf. Figure 3.1) are periodic time functions. The amplitudes of the fundamental frequency components of v_{ac1r} and v_{ac2r} can be derived using a Fourier series, i.e.

$$\begin{aligned}\hat{V}_{ac1r} &= \frac{4}{\pi}V_{1r}\cos(\delta_1) \\ \hat{V}_{ac2r} &= \frac{4}{\pi}V_{2r}\cos(\delta_2).\end{aligned} \tag{3.9}$$

Substituting (3.9) in (3.8), P_{12} can be represented as

$$P_{12} = \frac{4}{\pi^3 f_s L_{12r}}V_{1r}\cos(\delta_1)V_{2r}\cos(\delta_2)\sin(\phi_1). \tag{3.10}$$

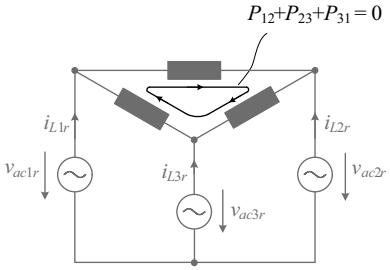


Figure 3.4: Zero active circulating power, i.e. $P_{12} + P_{23} + P_{31} = 0$.

Analogously, we have for P_{13} and P_{23}

$$\begin{aligned} P_{13} &= \frac{4}{\pi^3 f_s L_{13r}} V_{1r} \cos(\delta_1) V_{3r} \cos(\delta_3) \sin(\phi_2) \\ P_{23} &= \frac{4}{\pi^3 f_s L_{23r}} V_{2r} \cos(\delta_2) V_{3r} \cos(\delta_3) \sin(\phi_2 - \phi_1). \end{aligned} \tag{3.11}$$

3.3.2 Zero Circulating Active Power

For optimizing the operating point, i.e. for achieving minimum overall converter losses, a circulation of active power inside the three-port converter, which would not contribute to the active power of the ports, has to be prevented, i.e.

$$P_{12} + P_{23} + P_{31} = 0 \tag{3.12}$$

has to be ensured (cf. Figure 3.4).

Considering (2.16) with (3.12), we then have P_{12}, P_{23}, and P_{13} in dependency on P_2, P_3

$$\begin{aligned} P_{12} &= -\frac{2}{3}P_2 - \frac{1}{3}P_3 \\ P_{23} &= \frac{1}{3}P_2 - \frac{1}{3}P_3 \\ P_{13} &= -P_{31} = -\frac{1}{3}P_2 - \frac{2}{3}P_3. \end{aligned} \tag{3.13}$$

3.3.3 Operating Area

For controlling the converter, 5 degrees of freedom, i.e. the phase displacements ϕ_1 *and* ϕ_2 and the duty cycles δ_1, δ_2 *and* δ_3 are available. Defining the active power of two ports, e.g. P_2 and P_3 and ensuring zero circulating power means that the transfer of active power between the ports, i.e. P_{12}, P_{13} and P_{23}, is determined (cf. (3.13)), and only two degrees of freedom are remaining, i.e. the converter characteristics can be expressed in dependency on ϕ_1 and ϕ_2.

Referring to (3.10) and (3.11), the duty cycles δ_1, δ_2, and δ_3 now can be expressed as

$$\begin{aligned}
\delta_1 &= \begin{cases} \arccos(\Delta) & \text{if } (\phi_1 > \frac{\pi}{2}) \wedge (\phi_2 \leq \frac{\pi}{2}) \\ \pi - \arccos(\Delta) & \text{otherwise} \end{cases} \\
\delta_2 &= \arccos\left(\frac{\pi^3 f_s P_{12} L_{12r}}{4 V_{1r} V_{2r} \cos(\delta_1)\sin(\phi_1)}\right) \\
\delta_3 &= \arccos\left(\frac{\pi^3 f_s P_{13} L_{13r}}{4 V_{1r} V_{3r} \cos(\delta_1)\sin(\phi_2)}\right),
\end{aligned} \tag{3.14}$$

where

$$\Delta = \frac{\pi\sqrt{\pi f_s P_{12} P_{13} L_{12r}(\tan(\phi_2) - \tan(\phi_1))}}{2 V_{1r}\sqrt{P_{23}\tan(\phi_1)\tan(\phi_2)}}.$$

Taking into account that the argument of an inverse cosine function should remain within [-1, 1], (3.14) results in a restriction of the converter operating range and/or in a limit on the admissible range of ϕ_1 and ϕ_2. For example, there follows considering $\delta_1(\phi_1, \phi_2)$

$$-1 \leq \Delta \leq 1. \tag{3.15}$$

The corresponding range of ϕ_1, ϕ_2 is denoted as *Area* δ_1 in Figure 3.5. In analogy, *Area* δ_2 and *Area* δ_3 are resulting from $\delta_2(\phi_1, \phi_2)$ and $\delta_3(\phi_1, \phi_2)$. Considering all restrictions, the converter operation finally is restricted to *Area A* defined by the intersection of *Area* δ_1, *Area* δ_2 and *Area* δ_3.

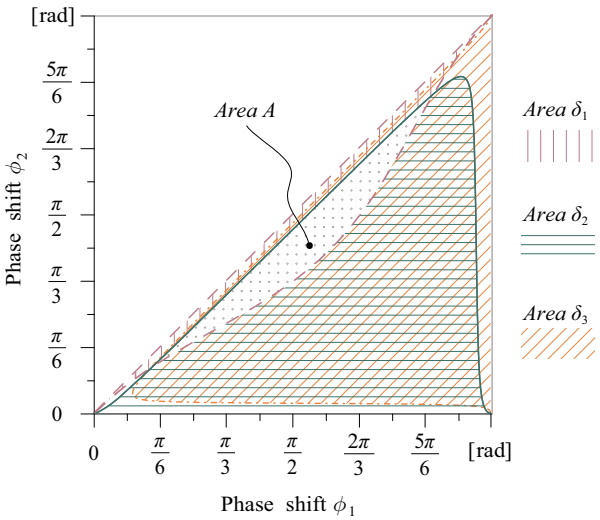


Figure 3.5: Operating area A, i.e. admissible range of phase shift angle ϕ_1 and phase shift angle ϕ_2, for P_1 = 1.5 kW, P_2 = -1.0 kW, P_3 = -0.5 kW, and zero circulating power; other parameters as given in Table 2.2.

3.4 Power Loss Analysis

In this section, the losses of the different components in the power stage are estimated. These losses can be categorized into two main parts: active components (MOSFETs) losses and magnetic components losses. Any other passive component losses, such as capacitor losses and PCB losses, are ignored.

3.4.1 MOSFET Losses

There are two main power loss mechanisms in MOSFETs: conduction losses and switching losses.

Conduction Losses

For MOSFETs, the conduction losses can be computed straightforward via

$$P_{cond} = I_{d\_rms}^2 \, R_{ds}, \tag{3.16}$$

where R_{ds} is the on-resistance of the MOSFET given in the datasheet. The RMS value of the current flowing through the MOSFET I_{d_rms} is $1/\sqrt{2}$ of that of the associated transformer winding since each MOSFET of the full-bridge unit conducts for half a switching cycle.

Switching Losses

Calculating the switching losses is more involved than calculating the conduction losses. The switching losses of the MOSFETs of a full-bridge unit are

$$P_{sw} = f_s \sum_{j=1}^{4} E_{sw\_j}, \tag{3.17}$$

where E_{sw_j} is the sum of the energy dissipations in two MOSFETs of a phase leg over the commutation interval j.

A typical test setup, comprising of a MOSFETs S_{Hi} and a MOSFET S_{Lo}, a DC voltage source and an inductive load, is simulated for analyzing the MOSFETs switching behavior.

The equivalent circuit of the test setup for the commutation interval when the current in S_{Lo} is diverted to the body diode D_{Hi} of S_{Hi} is depicted in Figure 3.6, where the suffixes $\_Hi$ and $\_Lo$ indicate that the association of elements to the upper MOSFET S_{Hi} or the lower one S_{Lo}:

- the current source with current i_{ch_Lo} representing the current in the MOSFET channel, which is determined by the instantaneous values of the gate-source voltage v_{gs_Lo} and the drain-source voltage

v_{ds_Lo} in [80]

$$i_{ch\_Lo} = \begin{cases} 0 & \text{for } v_{gs\_Lo\_e} < 0 \\ K(v_{gs\_Lo\_e})^2 & \text{for } \begin{matrix} v_{gs\_Lo\_e} > 0 \\ v_{ds\_Lo} > v_{gs\_Lo\_e} \end{matrix} \\ Kv_{ds\_Lo}[2v_{gs\_Lo\_e} - v_{ds\_Lo}] & \text{for } \begin{matrix} v_{gs\_Lo\_e} > 0 \\ v_{ds\_Lo} < v_{gs\_Lo\_e}, \end{matrix} \end{cases} \tag{3.18}$$

where $v_{gs\_Lo\_e} = v_{gs\_Lo} - V_T$, V_T is the threshold voltage and $K = \mu_{ns} C_{ox} Z/(2L)$ is a device parameter. The parameters K and V_T can be obtained by curve fitting (3.18) to the output characteristics given in the datasheet.

- the body diode D_{Hi}, whose reverse recovery characteristics are available in the datasheet;
- the non-linear inter-electrode capacitances, C_{gd_Hi}, C_{gs_Hi}, C_{ds_Hi}, C_{gd_Lo}, C_{gs_Lo} and C_{ds_Lo}, which are directly available in the datasheet;
- the parasitic inductances, L_{pd_Hi}, L_{ps_Hi}, L_{pl_Hi}, L_{pd_Lo} and L_{ps_Lo}, which can be estimated based on the dimensions of the device package and the layout of the interconnections.
- the small RC snubbers, R_{sb_Hi} and C_{sb_Hi}, R_{sb_Lo} and C_{sb_Lo}, which are needed to limit the rate of rise of drain-source voltages in order to reduce the peak power dissipation;
- the gate resistors R_{g_Hi} and R_{g_Lo};
- the gate supply with a voltage v_{g_Lo}, which is an ideal pulse voltage, stepping from V_G to 0 for turning off the switch;
- the inductive load with a current i_o and the DC source with a voltage v_{in}, which both can be considered as constant during the short switching interval and therefore are replaced with a constant current sourceI_o and a constant voltage source V_{in}, respectively.

The switching transient behaviors can be divided into two parts dependent on whether or not the body diode D_{Hi} conducts. If the diode does

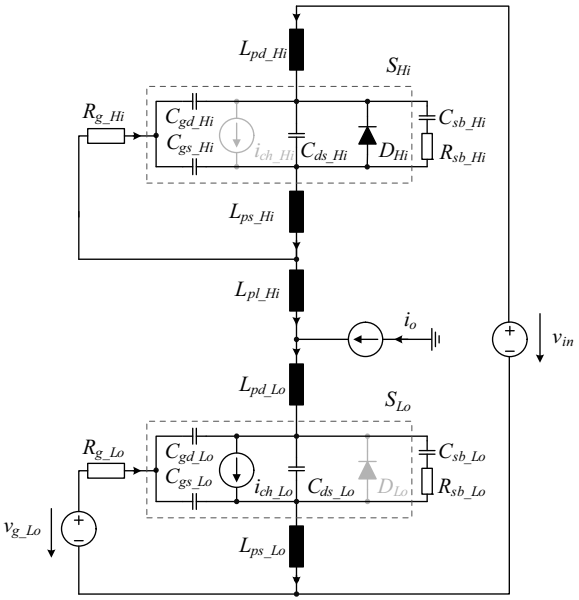


Figure 3.6: Equivalent circuit of the test setup within the commutation interval when the current in MOSFET S_{Lo} is diverted to the body diode D_{Hi}. The suffixes $\_Hi$ and $\_Lo$ denominate the components associated to the upper MOSFET S_{Hi} and the lower MOSFET S_{Lo}.

not conduct, i.e. the body diode current i_{D_Hi} remains zero, the circuit equations based on the equivalent circuit (cf. Figure 3.6) are expressed using a Laplace transform

$$i_{Rg\_Hi}(s) = s\,C_{gd\_Hi}\,v_{gd\_Hi}(s) + s\,C_{gs\_Hi}\,v_{gs\_Hi}(s) \tag{3.19-1}$$
$$i_{Lpd\_Hi}(s) = -\,i_{Rg\_Hi}(s) + i_{Lps\_Hi}(s) \tag{3.19-2}$$
$$i_{Lps\_Hi}(s) = i_{Rg\_Hi}(s) + i_{Lpl\_Hi}(s) \tag{3.19-3}$$
$$i_{Lpl\_Hi}(s) = i_{Lpd\_Lo}(s) - I_o(s) \tag{3.19-4}$$
$$i_{Rg\_Lo}(s) = s\,C_{gd\_Lo}\,v_{gd\_Lo}(s) + s\,C_{gs\_Lo}\,v_{gs\_Lo}(s) \tag{3.19-5}$$
$$i_{Lpd\_Lo}(s) = i_{Lps\_Lo}(s) - i_{Rg\_Lo}(s) \tag{3.19-6}$$
$$\begin{aligned} i_{Lps\_Lo}(s) = {} & s\,C_{gs\_Lo}\,v_{gs\_Lo}(s) + i_{ch\_Lo}(s) \\ & + s\,C_{ds\_Lo}\,v_{ds\_Lo}(s) + s\,C_{sb\_Lo}\,v_{sb\_Lo}(s) \end{aligned} \tag{3.19-7}$$

$$v_{gs\_Hi}(s) = -R_{g\_Hi}\, i_{Rg\_Hi}(s) - s\, L_{ps\_Hi}\, i_{Lps\_Hi}(s) \tag{3.19-8}$$

$$v_{gd\_Hi}(s) = v_{gs\_Hi}(s) - v_{ds\_Hi}(s) \tag{3.19-9}$$

$$v_{sb\_Hi}(s) = \frac{v_{ds\_Hi}(s)}{1 + s\, R_{sb\_Hi}\, C_{sb\_Hi}} \tag{3.19-10}$$

$$\begin{aligned} v_{ds\_Hi}(s) = {} & \frac{1}{s\, C_{ds\_Hi}}(i_{Lpd\_Hi}(s) + s\, C_{gd\_Hi}\, v_{gd\_Hi}(s) \\ & - s\, C_{sb\_Hi}\, v_{sb\_Hi}(s)) \end{aligned} \tag{3.19-11}$$

$$v_{gd\_Lo}(s) = v_{gs\_Lo}(s) - v_{ds\_Lo}(s) \tag{3.19-12}$$

$$\begin{aligned} v_{gs\_Lo}(s) = {} & v_{g\_Lo}(s) - R_{g\_Lo}\, i_{Rg\_Lo}(s) \\ & - s\, L_{ps\_Lo}\, i_{Lps\_Lo}(s) \end{aligned} \tag{3.19-13}$$

$$v_{sb\_Lo}(s) = \frac{v_{ds\_Lo}(s)}{1 + s\, R_{sb\_Lo}\, C_{sb\_Lo}} \tag{3.19-14}$$

$$\begin{aligned} v_{ds\_Lo}(s) = {} & -s\, L_{pd\_Hi}\, i_{Lpd\_Hi}(s) - s\, L_{ps\_Hi}\, i_{Lps\_Hi}(s) \\ & - s\, L_{pl\_Hi}\, i_{Lpl\_Hi}(s) - s\, L_{pd\_Lo}\, i_{Lpd\_Lo}(s) \\ & - s\, L_{ps\_Lo}\, i_{Lps\_Lo}(s) - v_{ds\_Hi}(s) + V_{in}(s). \end{aligned} \tag{3.19-15}$$

If the body diode D_{Hi} conducts, (3.19-11) is replaced by $v_{ds\_Hi}(s) = -V_b/s$ where V_b is the diode forward voltage. Moreover, the diode current is determined by

$$i_{D\_Hi}(s) = -i_{Lpd\_Hi}(s) - s\, C_{gd\_Hi}\, v_{gd\_Hi}(s). \tag{3.20}$$

Furthermore, the reverse recovery charge Q_{rr} is considered in the switching transient analysis. After the forward current of the body diode D_{Hi} goes to zero, the diode conducts a current in reverse direction until the area under this reverse current calculated starting from the zero crossing reaches the reverse recovery charge Q_{rr}, which can be found in the datasheet.

In order to reduce the calculation effort, a numerical solution of the circuit equations of both intervals is preferred to a closed-form solution.

As an example, the calculated turn on and turn off waveforms are shown in Figure 3.7 for MOSFETs IXFX64N60P from IXYS based on numerical calculation results with circuit parameters as given in Table 3.1. The effects of the parasitic components on the switching transient behavior are well demonstrated. For the turn on waveforms (cf. Figure 3.7(a)),

the slope of the gate-source voltage v_{gs_Lo} is lower when the drain current i_{Lpd_Lo} is increasing than in the previous interval with $i_{Lpd\_Lo} = 0$. This is caused by the voltage across the source inductance v_{Lps_Lo} which reduces the effective gate source voltage. At the same time, the drain-source voltage v_{ds_Lo} decreases proportionally to $d(i_{Lpd\_Lo})/dt$. The ringing is caused by the parasitic inductances in connection with the inter-electrode capacitances of MOSFETs. The small RC snubbers provide sufficient damping, so that overvoltage transient spikes are suppressed. The capacitive displacement currents, which charge/discharge the drain-source capacitances C_{ds_Lo} / C_{ds_Hi} and the capacitors C_{sb_Lo} / C_{sb_Hi} of the RC snubbers, play an important role in the turn off waveforms (cf. Figure 3.7(b)), and result in an almost about linear increase/decrease of the drain-source voltages v_{ds_Lo} / v_{ds_Hi}.

Table 3.1: Circuit parameters of the equivalent circuit for the switching behavior analysis of MOSFETs IXFX64N60P. *

Description	Parameter
DC source voltage	$V_{in} = 300$ V
Inductive load current	$I_o = 10$ A
Gate supply voltage	$V_G = 12$ V
Gate resistors	$R_{g\_Hi}(\text{on}) = R_{g\_Lo}(\text{on}) = 8.2\ \Omega$
	$R_{g\_Hi}(\text{off}) = R_{g\_Lo}(\text{off}) = 3.5\ \Omega$
RC snubbers	$R_{sb\_Hi} = R_{sb\_Lo} = 18.5\ \Omega$
	$C_{sb\_Hi} = C_{sb\_Lo} = 390$ pF
Parasitic inductances	$L_{pd\_Hi} = 14$ nH
	$L_{ps\_Hi} = 10$ nH
	$L_{pl\_Hi} = 2$ nH
	$L_{pd\_Lo} = 12$ nH
	$L_{ps\_Lo} = 10$ nH

* Other parameters are available in the datasheet of MOSFET IXFX64N60P.

The transient power losses of the MOSFETs S_{Hi} and S_{Lo} are

$$p_{ds\_Hi}(t) = v_{ds\_Hi}(t)\, i_{Lpd\_Hi}(t) \tag{3.21}$$

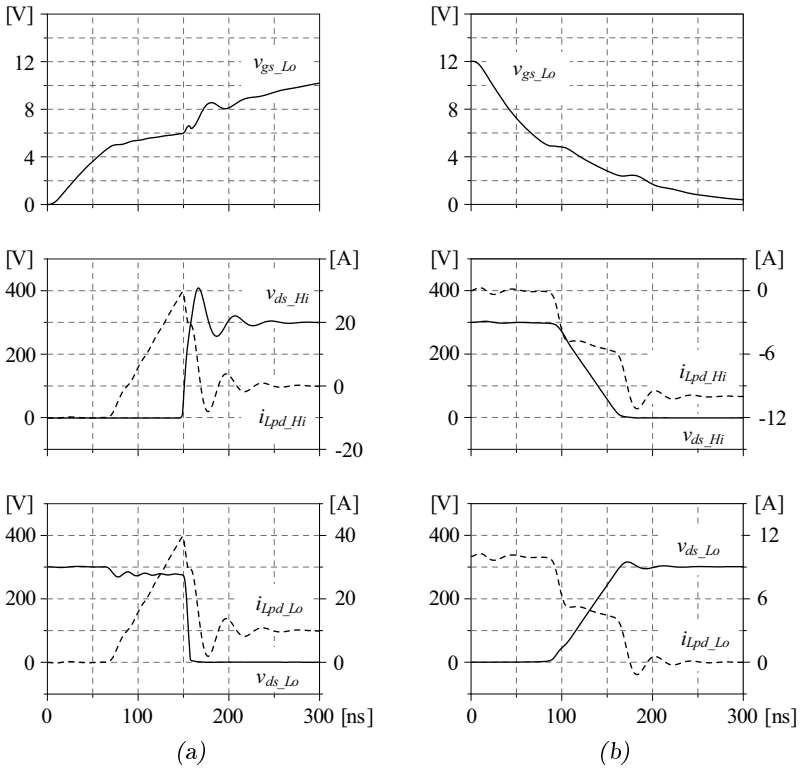


Figure 3.7: (a) Turn-on and (b) turn-off waveforms of a bridge leg employing MOSFETs IXFX64N60P based on numerical calculations.

and

$$p_{ds\_Lo}(t) = v_{ds\_Lo}(t)\, i_{Lpd\_Lo}(t). \tag{3.22}$$

The total energy dissipated in the two MOSFETs S_{Hi} and S_{Lo} within a the commutation interval can be estimated as

$$E_{sw} = t_{step} \sum_{k=0}^{n-1} [\frac{p_{ds\_Hi}(t_k) + p_{ds\_Hi}(t_{k+1})}{2} + \frac{p_{ds\_Lo}(t_k) + p_{ds\_Lo}(t_{k+1})}{2}], \tag{3.23}$$

where t_{step} is the time step for the numerical calculation of the switching behavior analysis and nt_{step} is the duration of the commutation interval.

Again, as an example, the dependency of the energy dissipation E_{sw} on the drain current I_{d_Lo} is illustrated for a bridge leg built with MOSFETs IXFX64N60P from IXYS in Figure 3.8, where the drain current I_{d_Lo} is positive when the current in the MOSFET S_{Lo} is diverted to the body diode D_{Hi}, i.e. the zero-voltage switching occurs, and is negative when the current in the body diode D_{Lo} is diverted to the MOSFET S_{Hi}, i.e. hard switching occurs. As expected, the energy dissipated for zero-voltage switching is much less than for the hard switching, where the energy lost during the ringing period, i.e. the energy for the reverse recovery of the body diode and stored in the output capacitor of the MOSFET, is the dominant part. Therefore, it is clearly desirable to operate the converter with zero-voltage switching in order to have lower losses and lower electromagnetic interference (EMI).

3.4.2 Magnetic Components Losses

The main magnetic component in the converter is the three-winding transformer, which provides electrical isolation and the matching of different voltage levels of the buses by suitable winding turns ratios. Additionally, series inductors are required if the leakage inductances of the transformer are too small for a precise control of the power transfer with a limited resolution of the phase shift angles. There are two kinds of losses in magnetic components: core losses and winding losses.

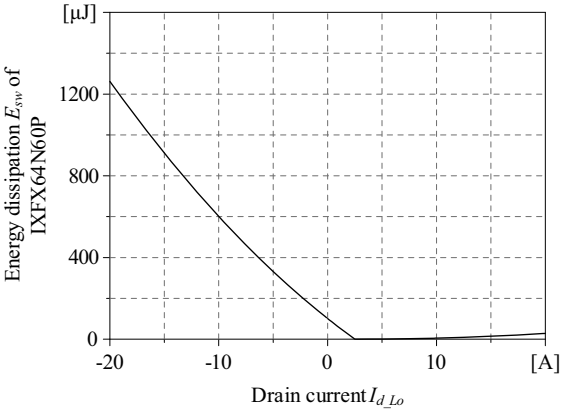


Figure 3.8: Dependency of the energy dissipation E_{sw} of of a MOSFET IXFX64N60P employed in a bridge leg on the drain current I_{d_Lo}. The drain current I_{d_Lo} is positive when the current in the MOSFET S_{Lo} is diverted to the body diode D_{Hi}, i.e. when zero-voltage-switching occurs, and is negative when the current in the body diode D_{Lo} is diverted to the MOSFET S_{Hi}, i.e. for hard-switching.

Core Losses

With the assumption of a sinusoidal excitation and uniform magnetic flux distribution inside the core, the core losses can be calculated using the empirical Steinmetz equation [81]

$$P_{core} = C_m \, f_s^{\alpha} \, B_{max}^{\beta} \, V_{core}, \tag{3.24}$$

where B_{max} is the maximum flux density, V_{core} is the core volume, C_m, α and β are three material constants provided by the manufacturer; alternatively the constants could be extracted from specific core loss data by curve fitting.

Winding Losses

The winding losses increase dramatically with frequency due to the eddy currents. The litz wire, made of many isolated strands twisted or woven together in a specific pattern, is used for the windings of the HV and the

42 V sides in order to reduce the AC resistances of the windings.

The analytical expression for the AC resistance of a litz wire winding for the assumption of a one-dimensional magnetic field and a sinusoidal current excitation is derived in [82] as

$$R_{ac\_litz} = R_{dc\_litz} \frac{\gamma_d}{2}\left[\gamma_{skin} - 2\pi n_s^2\left(\eta_e^2 + \eta_i^2\frac{n_t d_s^2}{2\pi n_s d_w^2}\right)\left(\frac{4(n_l^2-1)}{3}+1\right)\gamma_{prox}\right] \tag{3.25}$$

with

$$\begin{aligned}
R_{dc_litz} &= \frac{4\,\rho_{Cu}}{\pi\, n_s\, d_s^2} n_t\, l_t \\
\gamma_{skin} &= \frac{\mathrm{ber}(\gamma_d)\mathrm{bei}'(\gamma_d) - \mathrm{bei}(\gamma_d)\mathrm{ber}'(\gamma_d)}{\mathrm{ber}'^2(\gamma_d) + \mathrm{bei}'^2(\gamma_d)} \\
\gamma_{prox} &= \frac{\mathrm{ber}_2(\gamma_d)\mathrm{ber}'(\gamma_d) + \mathrm{bei}_2(\gamma_d)\mathrm{bei}'(\gamma_d)}{\mathrm{ber}^2(\gamma_d) + \mathrm{bei}^2(\gamma_d)} \\
\gamma_d &= \frac{d_s}{\sqrt{2}\,\delta_{fs}} \\
\eta_e &= \frac{d_s}{t_w}\sqrt{\frac{\pi}{4}} \\
\eta_i &= \frac{d_s}{t_s}\sqrt{\frac{\pi}{4}},
\end{aligned}$$

where

- n_l, n_t and l_t are the parameters of the winding, i.e. n_l and n_t are the numbers of layers and turns of the winding, and l_t is the average length of one turn of the winding;
- n_s, d_s, d_w, t_s and t_w are the parameters associated with the litz wire, i.e. n_s is the number of strands in the litz wire, d_s is the diameter of a single strand of the litz wire, d_w is the overall diameter of the litz wire excluding the insulating layer, t_s is the distance between the centers of two adjacent strands in the same litz wire and t_w is the distance between the centers of two adjacent litz wires in the same winding;

- $\delta_{fs} = \sqrt{\rho_{Cu}/(\pi f_s \, \mu_0 \, \mu_{Cu})}$ is the skin depth of copper at the switching frequency f_s;
- ρ_{Cu}, μ_0 and μ_{Cu} are the material constants, i.e. ρ_{Cu} is the copper resistivity at a given operating temperature, μ_0 the permeability of the free space and $\mu_{Cu} = 1$ is the relative permeability of copper;
- additionally, $\mathrm{ber_v}$ and $\mathrm{bei_v}$ stand for the Bessel-real and Bessel-imaginary parts.

Due to the high current, the winding of the 14 V bus side is made of a solid foil. The winding arrangement with the planar core and the associated m.m.f. diagram of an operating point, e.g. the optimum operating point A (cf. Figure 3.10), are shown in Figure 3.9. With the same assumption of a one-dimensional magnetic field and a sinusoidal current excitation, the AC resistance of the solid foil winding can be calculated according to [83] as

$$R_{ac\_solid} = R_{dc\_solid}\gamma_h[(2m^2-2m+1)G_1(\gamma_h)-4m(m-1)G_2(\gamma_h)] \quad (3.26)$$

with

$$\begin{aligned}
R_{dc_solid} &= \frac{\rho_{Cu}}{h_f \, w_f} n_t \, l_t \\
G_1(\gamma_h) &= \frac{\sinh(2\gamma_h) + \sin(2\gamma_h)}{\cosh(2\gamma_h) - \cos(2\gamma_h)} \\
G_2(\gamma_h) &= \frac{\sinh(\gamma_h)\cos(\gamma_h) + \cosh(\gamma_h)\sin(\gamma_h)}{\cosh(2\gamma_h) - \cos(2\gamma_h)} \\
\gamma_h &= \frac{h_f}{\delta_{fs}} \\
m &= \frac{\mathfrak{F}(1)}{\mathfrak{F}(1) - \mathfrak{F}(2)} \\
\mathfrak{F}(1) &= n_{t_1} \, I_{L1_rms} \\
\mathfrak{F}(2) &= n_{t_2} \, I_{L2_rms},
\end{aligned}$$

where h_f and w_f are the height and width of the single layer solid foil, $\mathfrak{F}(1)$ and $\mathfrak{F}(2)$ are the magnetomotive forces on the HV and 42 V sides as illustrated in Figure 3.9, n_{t_1} and n_{t_2} are the numbers of turns of the winding on the HV side (port 1) and the 42 V side (port 2).

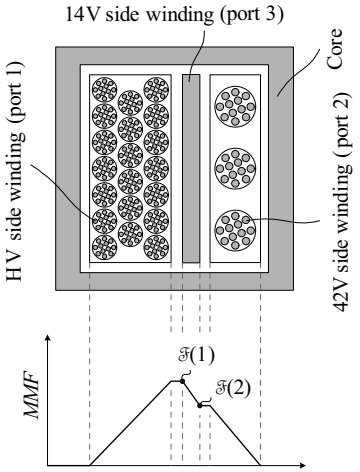


Figure 3.9: Transformer winding arrangement and associated m.m.f. diagram for operation in optimum operating point A (cf. Figure 3.10).

Therefore, the total losses of one winding P_{wind} can be calculated as

$$P_{wind} \approx= 2I_{d\_rms}^2 R_{ac}, \tag{3.27}$$

where I_{d_rms} denotes the RMS value of the current flowing through the MOSFET which is $1/\sqrt{2}$ of that of the associated transformer winding since each MOSFET in the full-bridge conducts for half a switching cycle, R_{ac} is the ac resistance of the winding for switching frequency, no matter if it is made of litz wire or solid foil.

3.5 Optimum Operating Point

The overall converter losses, which are composed of conduction and switching losses of the MOSFETs, and the core and the winding losses of the magnetic components, can be evaluated numerically for every operating point in the admissible operating area *Area A* (cf. Figure 3.5). Any point in the operating area *Area A* is determined by the fundamental power (cf. (3.1)), and not by the total power. However, as the difference between these two power values is relatively small, it is acceptable to define

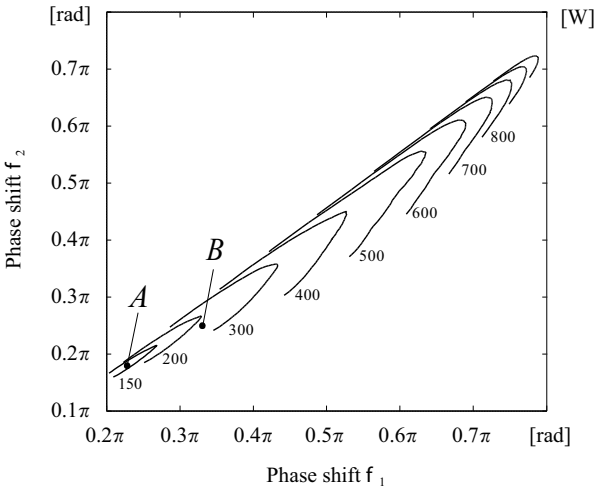
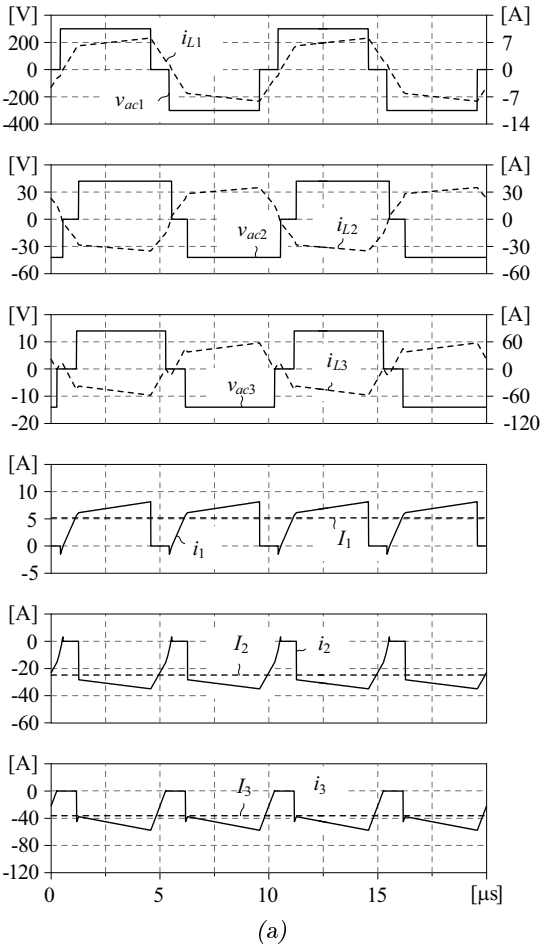


Figure 3.10: Overall converter losses in the whole admissible operating area *Area A* in dependency on ϕ_1 and ϕ_2; operating point A results in minimum overall converter losses. Operating parameters and circuit parameters as for Figure 3.5.

the operating point by the fundamental power.

In order to speed up the calculation process and still to guarantee sufficient accuracy, a discrete grid is chosen, which divides the allowable range of each variable into 50 values and each value is then used in the numerical calculation. It should be noted that the allowable range of the dependent variable, i.e. of the phase shift angle ϕ_2, varies depending on the value of the independent variable, i.e. the phase shift angle ϕ_1, in this case (cf. Figure 3.5).

The contour plot of the overall converter losses for all grid points is illustrated in Figure 3.10, for a particular power transfer and circuit parameters as in Figure 3.5. Figure 3.10 shows that for operating point A results in minimum overall converter losses. This is clearly verified by another operating point B, which is characterized by significantly higher current magnitudes and higher voltage *and* current phase displacements and significantly higher losses, as illustrated by a simulation of the steady-state waveforms (cf. Figure 3.11).



(a)

Figure 3.11: Simulation of steady-state waveforms for operating point A (a) and B (b) in Figure 3.10. The current magnitudes and the voltage and current phase displacements of the operating point B are higher than those of operating point A, resulting in significantly higher losses.

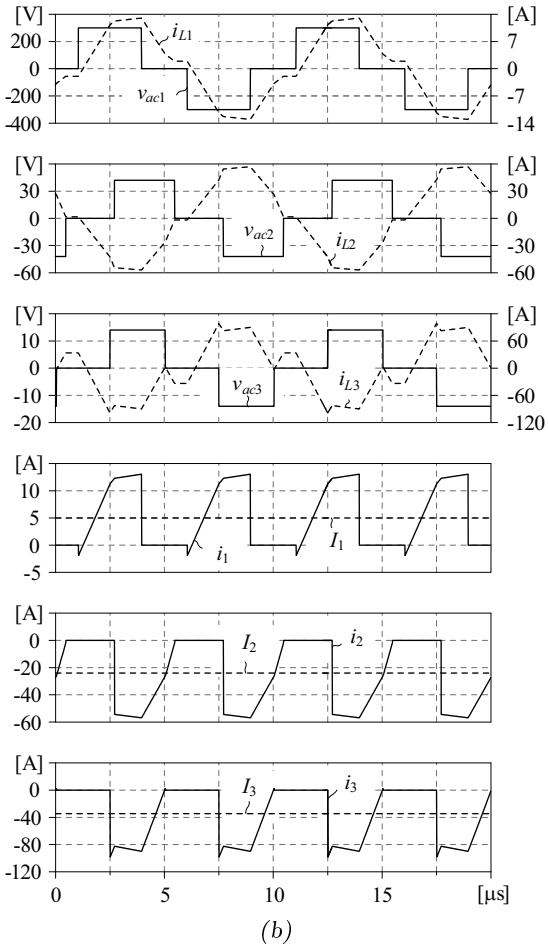


Figure 3.11: Simulation of steady-state waveforms for operating point A (a) and B (b) in Figure 3.10. The current magnitudes and the voltage and current phase displacements of the operating point B are higher than those of operating point A, resulting in significantly higher losses (continued).

Figure 3.12 depicts the estimated power loss distribution of the three-port converter for the optimum operating point A. It can be observed that:

- the switching losses of the MOSFETs are a dominant part of the total losses, i.e. 45%, although all MOSFETs in the converter operate with zero-voltage switching (cf. Figure 3.11(a)). The MOSFETs of the full-bridge on the 42 V side (port 2) contribute the largest share due to the high currents at the switching instants and the large parasitic inductances;
- considering the MOSFET conduction losses, the MOSFETs of the full-bridge on the HV side (port 1) show higher losses than the other MOSFETs due to the larger on-resistance as a result of the required higher voltage capability;
- the core losses of the transformer are relatively low since the amplitude of the flux density in the core is much smaller than the saturation value of the material;
- regarding the transformer winding losses, the winding on the HV side (port 1) causes higher losses than the winding on the 42 V side (port 2) due to the longer length of the winding on the HV side (port 1). The high losses of the copper foil winding on the 14 V side (port 3) are caused by the large ac resistance since this winding is placed in the middle of the other two windings (cf. Figure 3.9);
- the inductor losses are relatively low due to small inductance values required.

3.6 Experimental Results

The theoretical considerations detailed above have been verified with an experimental set-up, with a circuit schematic of the power stage as depicted in Figure 3.13 and circuit parameters as given in Table 2.2.

In the implemented three-port system, there are three different LC filters connecting the ports of the converter to the voltage sources or the RC load, i.e. connecting port 1 to the voltage source $V_{1M} = 300$ V,

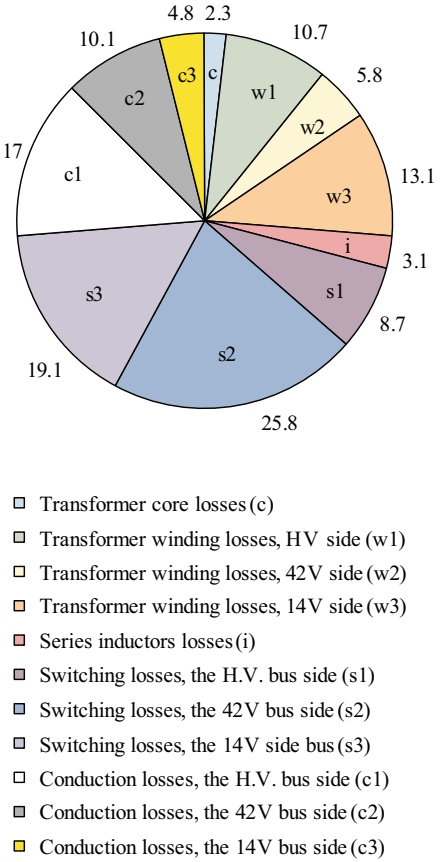


Figure 3.12: Estimated power losses distribution (in Watts) of the three-port converter for the optimum operating point A (cf. Figure 3.10).

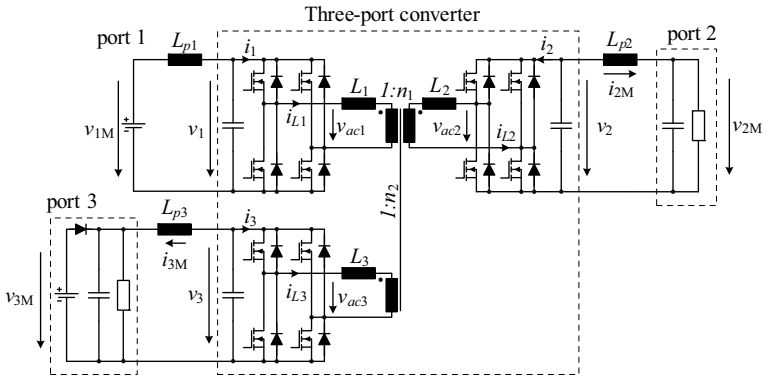


Figure 3.13: Implemented three-port system, where three LC filters connect the ports to the sources or loads.

port 2 to the RC load, and port 3 to the RC load arranged in parallel to the voltage source $V_{3M} = 14$ V. Accordingly, port 3 can sink or source power or remain at the zero power. Film/ceramic capacitors are placed near to the outputs of the full-bridge units in order to absorb the high frequency ac ripple currents generated by the full-bridge cells and keep the port voltage variations lower than 1%. L_{p1}, L_{p2} and L_{p3}, which are the parasitic inductances (or possibly small auxiliary inductors), are used to smooth the flowing currents since these currents are measured and some of them act as controlled variables in the control system, which will be explained in Chapter 5.

The switching devices are implemented with power MOSFETs:

- two IRF2804S MOSFETs from IR are connected in parallel to form a high current switching device for the bridge on the 14 V side;
- IXFX64N60P MOSFETs from IXYS and IRF2907 MOSFETs from IR are employed in the bridge on the HV and 42 V sides, respectively, where each switch is formed by a simple device.

The planar transformer comprises an ELP 64/10/50 ferrite core from EPCOS, a single turn copper foil winding on the 14 V side, a 3-turn litz wire winding for the 42 V side and a 20-turn litz wire winding for the HV side.

Figure 3.14 illustrates the measured steady-state operation results, showing

- the voltages between the phase leg midpoints in the full-bridge units, i.e. v_{ac1}, v_{ac2} and v_{ac3};
- the input current of each winding, i.e. i_{L1}, i_{L2}, i_{L3}.

The voltage waveforms are measured directly at the phase leg midpoints of the full-bridge unit, so the voltages of the lead inductances of MOSFET and PCB layout inductances are excluded, resulting in the difference between the oscilloscope recorded waveforms and the ideal ones, especially for the waveforms v_{ac3} (cf. Figure 3.14 (c) and (f), Figure 3.15 (c)) when the corresponding current i_{L3} changes rapidly.

The particular operating point for Figure 3.14 is point A and point B for Figure 3.10. In optimal operating point A, the converter shows minimum overall losses, resulting in an efficiency of 91.7%. By altering the operating point to point B, where significantly higher current amplitudes and/or significantly higher losses occur(cf. Figure 3.14), the efficiency is only 72.6%.

Moreover, it is verified in Figure 3.15(c) that a zero net power flow can be achieved for port 3 while power is transferred between the two other ports.

Furthermore, Figure 3.16 shows the good accordance between the calculated and the measured efficiencies for the optimum operating point and it is observed that the efficiency is above 90% over a wide range of output power (0 W to 500 W for port 3 and -1 kW for port 2). Therefore, the converter successfully operates with minimum losses control.

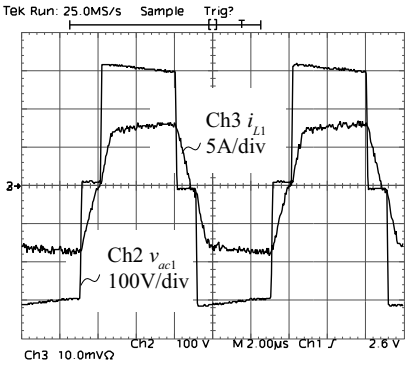
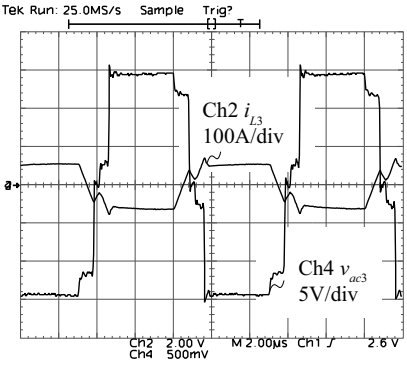
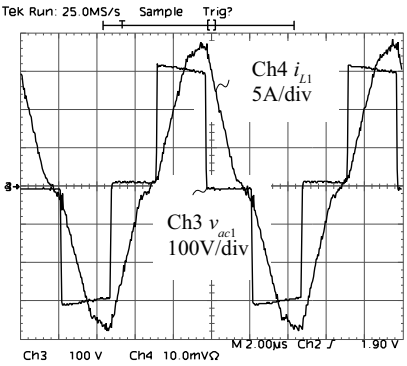


Figure 3.14: Measured waveforms, showing the voltages between the phase leg midpoints of the full-bridge units and the input current of each winding. (a), (b), (c) are related to operating point A and (d), (e), (f) to operating point B **(cf. Figure 3.10)** with P_2 = -1 kW and P_3 = -500 W. One has to note, that operating point A in general is characterized by the lowest system losses.

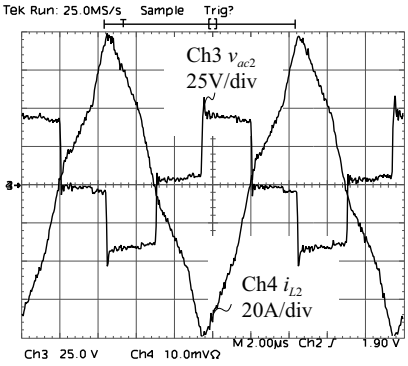


(c)



(d)

Figure 3.14: Measured waveforms, showing the voltages between the phase leg midpoints of the full-bridge units and the input current of each winding. (a), (b), (c) are related to operating point A and (d), (e), (f) to operating point B **(cf. Figure 3.10)** with P_2 = -1 kW and P_3 = -500 W. One has to note, that operating point A in general is characterized by the lowest system losses (continued).



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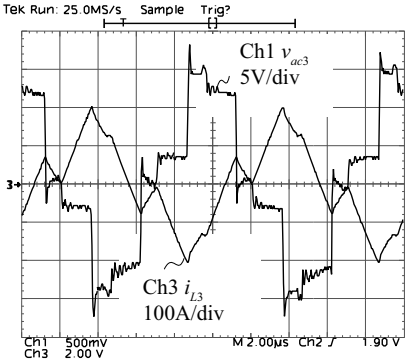


(f)

Figure 3.14: Measured waveforms, showing the voltages between the phase leg midpoints of the full-bridge units and the input current of each winding. (a), (b), (c) are related to operating point A and (d), (e), (f) to operating point B **(cf. Figure 3.10)** with P_2 = -1 kW and P_3 = -500 W. One has to note, that operating point A in general is characterized by the lowest system losses (continued).

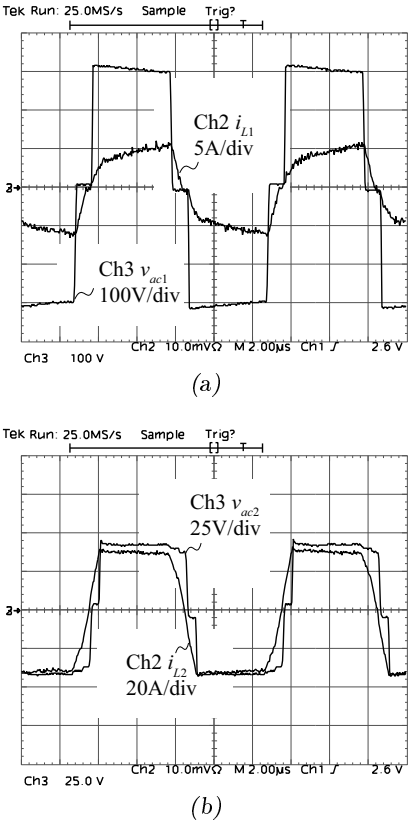
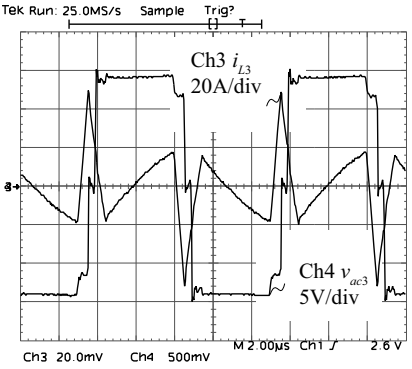


Figure 3.15: Measured waveforms, showing the voltages between the phase leg midpoints of the full-bridge units and the related transformer winding currents, for the optimum operating point with P_2 = -1 kW and P_3 = 0 W.



(c)

Figure 3.15: Measured waveforms, showing the voltages between the phase leg midpoints of the full-bridge units and the related transformer winding currents, for the optimum operating point with P_2 = -1 kW and P_3 = 0 W (continued).

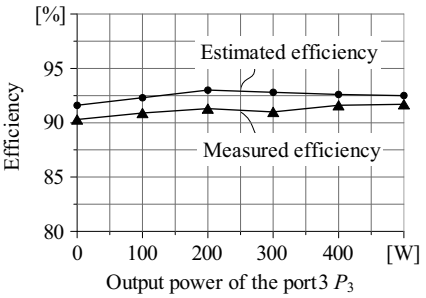


Figure 3.16: Comparison of the estimated and the measured total system efficiency for different output power levels of port 3 with the constant output power of port 2, i.e. P_2 = -1kW).

3.7 Summary

In this chapter, the duty cycle control for optimizing the system behavior is introduced, besides the phase shift control mainly managing the power flow between the ports. The circulation of the active power inside the three-port converter, which would not contribute to active input or output power of the ports, is prevented. The overall system losses, which are composed of conduction and switching losses of the MOSFETs, and core losses and winding losses of the magnetic components, are estimated. Based on this consideration, the optimum operating point characterized by the minimum overall system losses is obtained.

The above theoretical considerations are verified by an experimental set-up. The efficiency of the converter is improved from 72.6% for a non-optimum operating point to 91.7% in the optimum operating point. Moreover, it is found that the calculated and the measured efficiencies of the optimum operating point are in good accordance.

Chapter 4

Small-signal Analysis of Two-port Converter

4.1 Introduction

For a power electronics converter, one of the most important objectives is to achieve high dynamics, e.g. the good load regulation, that is to maintain the output voltage at a constant level despite changes of the load. The frequency responses of the controlled variables, e.g. the output voltage, to changes of controlling variables and/or perturbations of the source inputs are the necessary information for designing the feedback controller, which is usually employed to ensure system stability and enhance dynamic performance.

In the literature, most of the research performed for the three-port converter listed in chapter 1 has focused on the circuit topologies and the steady-state analysis. Little work has been done in the area of small-signal modelling of the converter. A simple approximative way to analyze the control properties of the DAB converter, from which the proposed three-port converter is derived, was proposed in [84] and was adopted later also in [85,86]. There, the control-to-output-current small-signal transfer function is derived from the steady-state output current since the converter acts, in the stationary operation, as a current source. However, this excludes dynamics of the leakage inductance and the resonant transition

intervals (where the resonant capacitors, - i.e. the output capacitors of MOSFETs and external snubber capacitors, if required - resonate with the leakage inductance, realizing the zero-voltage switching) are simply ignored, leading to the degradation of the accuracy of the model.

This chapter presents a general approach to achieve a full-order model for the DAB converter and this method is applicable to the three-pot converter. The modelling procedure, briefly discussed in Section 4.2, is basically based on the general discrete-time modelling method stated in [87,88], which has been previously applied to resonant converters, and takes the small-signal behavior of the converter into account only at one time instant in each sampling cycle; no further information is considered in between these instants. Special attention has been paid to the leakage inductance current, which is essentially an alternating current so that its small signal changes differ significantly when the sampling position is changed. Therefore, the small signal analysis for developing the proposed model is based on the discrete-time half-cycle-average (HCA) value. A similar averaging concept is found in [89,90], where the small-signal characteristics of a resonant converter are analyzed and a discrete-time simulation method is discussed, respectively.

4.2 Transfer Function Determination

A switching converter is a nonlinear, time-variant circuit. The feedback controller, which can be implemented either analog or digital to ensure the stability and enhance the dynamics performance, is mainly designed in the continuous-time domain because the design methods for continuous-time systems are well-developed and familiar to the circuit designer. Therefore, it is important to know the frequency response of the output signal due to perturbations in the controlling signal and/or the source inputs, i.e. to know the transfer function

$$G_{vs}(s) = \frac{\Delta v_2(s)}{\Delta \phi_1(s)}. \tag{4.1}$$

$G_{vs}(s)$ illustrates the relationship between the Laplace transform of a perturbation in the continuous-time controlling signal $\Delta\phi_1(t)$ to the Laplace transform of the resulting perturbation in the continuous-time output voltage $\Delta v_2(t)$ for the phase-shift bidirectional converter if the output

voltage is the controlled variable. The corresponding small signal system is shown in Figure 4.1.

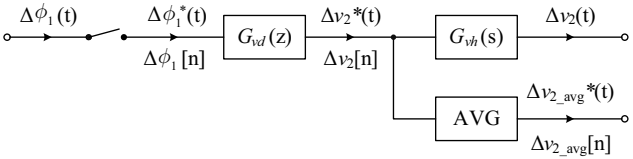


Figure 4.1: Small signal system for the phase-shift bidirectional DC-DC converter.

It is difficult to build a full-order small-signal model for the phase-shift controlled converter using the conventional state-space averaging technique since the ac current of the leakage inductance, whose average value over one switching cycle is always zero, can not be a state variable in the model derived by using the state-space averaging method.

An exact continuous-time analytical model in [91, 92], that matches the measured result from a frequency response analyzer exactly at all frequencies, has been developed based on the small-signal frequency response theory. However, this approach would be mathematically too complicated if applied to the phase-shift bidirectional converter.

Viewing that a pulse-width modulator is basically a small-signal sampler and the phase-shift angle perturbations act as a string of impulses $\Delta\phi_1[k]$, the discrete-time modelling method is a natural way to describe the periodic operation and control of the converter. Using the general discrete-time modelling method stated in [87, 88], a pulse transfer function $G_{vd}(z)$

$$G_{vd}(z) = \frac{\Delta v_2(z)}{\Delta\phi_1(z)}, \tag{4.2}$$

which relates the samples of the perturbation in the control signal $\Delta\phi_1[k]$ to the samples of the resulting perturbation of the output voltage $\Delta v_2[k]$ in the z-domain, can be determined.

Clearly, the discrete-time modelling method takes only the small-signal behavior of the converter at one time instant in each sampling cycle into account, and nothing in between the sampling instants. Considering the ripple of the voltage and current waveforms, different positions of this time instant within the switching cycle lead to differences

in the prediction of the frequency response, as has been verified in [93]. Furthermore, it actually is the small signal perturbation of the local average value that is of great interest, and not of value at a particular time instant. Therefore, the small signal change of the discrete-time half-cycle-average (HCA) value of the output voltage $\Delta v_{2\_avg}[k]$, which is explained in detail in Section 4.4.4, is used to develop a new pulse transfer function

$$G_{vd\_avg}(z) = \frac{\Delta v_{2\_avg}(z)}{\Delta \phi_1(z)} \tag{4.3}$$

for the phase-shift bidirectional DC-DC converter.

The pulse transfer function $G_{vd\_avg}(z)$ can be transformed from the z-domain to the s-domain by substituting $e^{sT_{samp}}$ for z, resulting in $G^*_{vd\_avg}(s)$, which approximates to $G_{vs}(s)$

$$G_{vs}(s) \approx G^*_{vd\_avg}(s) = \frac{\Delta v^*_{2\_avg}(s)}{\Delta \phi^*_1(s)} = G_{vd\_avg}(z)\big|_{z=e^{sT_{samp}}}, \tag{4.4}$$

where T_{samp} denotes the half switching cycle since the state variables are sampled every half switching cycle due to the symmetric operation of the phase-shift bidirectional converter, and $\Delta v^*_{2\_avg}(s)$ and $\Delta \phi^*_1(s)$ are the Laplace transforms of the sampled small signal changes of the average output voltage and the phase shift angle, respectively.

In the following, the DAB DC-DC converter is selected as an example to illustrate the above modelling procedure step by step.

4.3 Converter Description

A DAB DC-DC converter, with the low-voltage (LV) and high-voltage (HV) full-bridge units connected to a battery and/or a RC load, is illustrated in Figure 4.2. The midpoints of the two full-bridge units are connected with an intermediary circuit, composed of an ideal transformer T_1 with $1 : n_1$ turns ratio, a series inductor L_s and a series resistor R_s. L_s is the leakage inductance of the transformer (possibly also the inductance of an additional series inductor if it is necessary). R_s, which is neglected in the steady-state analysis in Chapter 2, is included here in order to have a result which is more close to reality and represents the sum of the on-resistances of the switches, the transformer winding resistances and all

contact resistances.

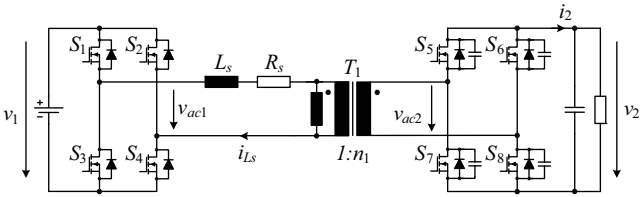


Figure 4.2: DAB DC-DC converter with a battery and a RC load.

The 50% duty-ratio gate signals are applied to all switches. For the sake of simplicity, the duty cycle variation of the full-bridge output voltages presented in Chapter 3 in order to have lower losses is not considered here. Therefore, there is only one controlling variable, i.e. the phase shift angle ϕ_1.

To achieve soft-switching, a small resonant transition interval between two gate signals is necessary to allow the output capacitances (possibly additional snubber capacitors) of the off-state MOSFETs to be discharged by the leakage inductance current and the devices to be turned on under zero-voltage condition after their body diodes conduct. This resonant transition interval in the HV unit is included in the following modelling since it has large influence on the low-frequency gain of the magnitude response, which is discussed in Section 4.6. Therefore, each MOSFET in the HV unit is modelled here as ideal switch in parallel with its body diode and its output capacitance C_{oss}. Although the MOSFETs in the LV unit also have a parasitic output capacitance, the energy in this output capacitance is much less than that for the MOSFETs of the HV unit. Therefore, the resonant transition time for the LV unit is negligible and the MOSFETs in the LV unit are considered to have instantaneous turn-on and turn-off.

Figure 4.3(a) shows the idealized primary-referred waveforms of the terminal voltages of the intermediate circuit, v_{ac1r} and v_{ac2r}, the leakage inductance current i_{Lsr}, the output current i_{2r} and the output voltage v_{2r} for the steady-state operation within one switching cycle $T_s = 2T_{samp}$. Owing to the symmetric operation of the DAB converter over a complete switching cycle, only the positive half switching cycle of v_{ac1r} is briefly explained here, in which the converter goes through three switching states

where the primary-referred equivalent circuits of the switching states are shown in Figures 4.3(b), (c) and (d). $C_{ossr} = n_1^2 C_{ossr}$, $C_{fr} = n_1^2 C_f$ and $R_{lr} = R_l/n_1^2$ are the primary-referred output capacitance of the MOSFET in the HV unit, the output filter capacitance and the load resistance, respectively.

Switching state:

1. $T_a = [t_0, t_1]$: At t_0, S_2 and S_3 are turned off and S_1 and S_4 are turned on. The terminal voltage v_{ac1r} of the intermediate circuit increases from $-V_{1r}$ to V_{1r} immediately. Due to the conduction of S_6 and S_7, the output voltage v_{2r} is applied to the other side of the intermediate circuit with the inverse polarity. The parasitic output capacitors of the off-state MOSFETs S_5 and S_8 are in parallel with the RC load and their voltage is clamped to the output voltage v_{2r}.

2. $T_b = [t_1, t_2]$: S_6 and S_7 are turned off at t_1. The output capacitors of S_5-S_8 and L_{sr} begin to resonant, making the voltages across the output capacitors of S_5 and S_8 fall from v_{2r} and the voltages across the output capacitors of S_6 and S_7 rise from zero. The interval ends when the voltages of the output capacitors of S_5 and S_8 decrease to zero and/or the body diodes are forward biased. The output current i_{2r} in this interval is zero and the RC load is separated from the rest of the power stage.

3. $T_c = [t_2, t_0 + T_{samp}]$: S_5 and S_8 are gated on at the zero voltage. The output voltage v_{2r} is equal to the terminal voltage v_{ac2r} of the intermediate circuit. The output capacitors of S_6 and S_7 are in parallel with the RC load and their voltages are equal to the output voltage v_{2r}.

4.4 Large-signal Discrete-time Description

In this section the large-signal discrete-time description for the DAB DC-DC converter is developed. Considering only the linear time-invariant elements of the converter, we first write the continuous-time state-space mathematical model that describes the converter for every switching state in the half switching cycle. Suitable approximations are made in order to find closed-form expressions for the state variables. This then leads to

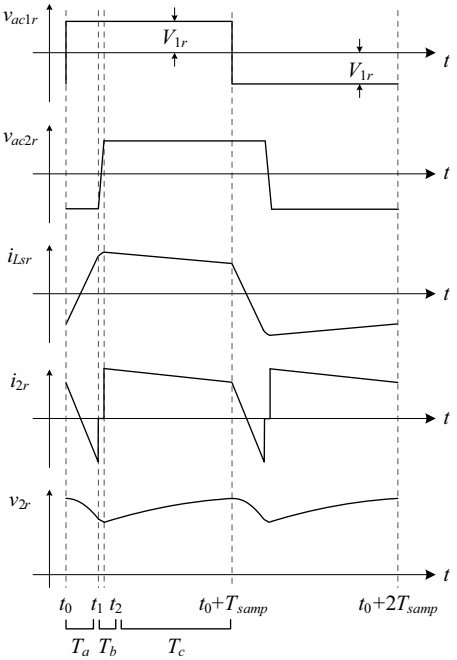


Figure 4.3: (a) Idealized primary-referred time behaviors of the terminal voltages v_{ac1r} and v_{ac2r} of the intermediate circuit, leakage inductance current i_{Lsr}, output current i_{2r} and output voltage v_{2r} for steady-state operation; the waveforms are shown for one switching cycle $T_s = 2T_{samp}$. (b)-(d) Primary-referred equivalent circuits for three switching states.

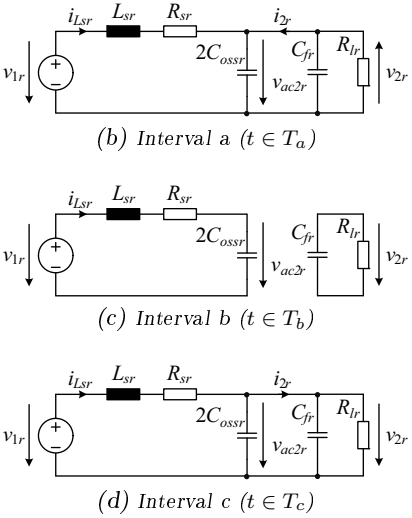


Figure 4.3: (a) Idealized primary-referred time behaviors of the terminal voltages v_{ac1r} and v_{ac2r} of the intermediate circuit, leakage inductance current i_{Lsr}, output current i_{2r} and output voltage v_{2r} for steady-state operation; the waveforms are shown for one switching cycle $T_s = 2T_{samp}$. (b)-(d) Primary-referred equivalent circuits for three switching states (continued).

a discrete-time model that describes the evolution of the state variables from the beginning of a half switching cycle to the end of the same half cycle. The half-cycle-average is also introduced in order to reduce the differences of the predicted frequency response caused by the different sampling positions in the discrete-time modelling. The developed large-signal discrete-time model is also verified by the simulation results.

4.4.1 State-space Mathematical Model

The state variables of the converter are chosen to be the leakage inductance current $i_{Lsr}(t)$, the output voltage $v_{2r}(t)$ and the terminal voltage $v_{ac2r}(t)$ of the intermediate circuit. $v_{ac2r}(t)$, which in interval a is $-v_{2r}(t)$ and is $v_{2r}(t)$ in interval c, represents the output capacitance voltages of the MOSFETs in the HV unit in interval b. The state vector $\mathbf{x}(t) = [i_{Lsr}(t)\ v_{2r}(t)\ v_{ac2r}(t)]^T$ is denoted by $\mathbf{x_a}(t)$ for interval a, by $\mathbf{x_b}(t)$ for interval b, and by $\mathbf{x_c}(t)$ for interval c to distinguish the solutions in the three switching states. Considering the primary-referred equivalent circuits in Figures 4.3(b)-(d), the converter can be described by the following state-space equations

$$\begin{aligned} \dot{\mathbf{x}}_\mathbf{a}(t) &= \mathbf{A_1}\mathbf{x_a}(t) + \mathbf{b_1}V_1 \quad t \in T_a \\ \dot{\mathbf{x}}_\mathbf{b}(t) &= \mathbf{A_2}\mathbf{x_b}(t) + \mathbf{b_2}V_1 \quad t \in T_b \\ \dot{\mathbf{x}}_\mathbf{c}(t) &= \mathbf{A_3}\mathbf{x_c}(t) + \mathbf{b_3}V_1 \quad t \in T_c, \end{aligned} \tag{4.5}$$

where

$$\mathbf{A_1} = \begin{bmatrix} -1/\tau_s & 1/L_{sr} & 0 \\ -1/C_{tr} & -1/\tau_t & 0 \\ 1/C_{tr} & 1/\tau_t & 0 \end{bmatrix}$$

$$\mathbf{A_2} = \begin{bmatrix} -1/\tau_s & 0 & -1/L_{sr} \\ 0 & -1/\tau_f & 0 \\ 1/C_{ossr} & 0 & 0 \end{bmatrix}$$

$$\mathbf{A_3} = \begin{bmatrix} -1/\tau_s & -1/L_{sr} & 0 \\ 1/C_{tr} & -1/\tau_t & 0 \\ 1/C_{tr} & -1/\tau_t & 0 \end{bmatrix}$$

$$\mathbf{b_1} = \mathbf{b_2} = \mathbf{b_3} = \begin{bmatrix} 1/L_{sr} & 0 & 0 \end{bmatrix}^T$$

$$C_{tr} = (C_{fr} + 2C_{ossr})$$

$$\tau_t = R_{lr} C_{tr}$$

$$\tau_f = R_{lr} C_{fr}$$

$$\tau_s = L_{sr}/R_{sr}.$$

The exact solutions of these state-space equations (4.5) are

$$\mathbf{x_a}(t) = \begin{bmatrix} i_{Lsr\_a}(e^{M_1 t}, e^{M_2 t}) \\ v_{2r\_a}(e^{M_1 t}, e^{M_2 t}) \\ -v_{2r\_a}(e^{M_1 t}, e^{M_2 t}) \end{bmatrix} = \begin{bmatrix} i_{Lsr\_a}(t) \\ v_{2r\_a}(t) \\ -v_{2r\_a}(t) \end{bmatrix} \quad t \in T_a$$

$$\mathbf{x_b}(t) = \begin{bmatrix} i_{Lsr\_b}(e^{M_3 t}, e^{M_4 t}) \\ v_{2r\_b}(e^{M_5 t}) \\ v_{ac2r\_b}(e^{M_3 t}, e^{M_4 t}) \end{bmatrix} = \begin{bmatrix} i_{Lsr\_b}(t) \\ v_{2r\_b}(t) \\ v_{ac2r\_b}(t) \end{bmatrix} \quad t \in T_b \qquad (4.6)$$

$$\mathbf{x_c}(t) = \begin{bmatrix} i_{Lsr\_c}(e^{M_1 t}, e^{M_2 t}) \\ v_{2r\_c}(e^{M_1 t}, e^{M_2 t}) \\ v_{2r\_c}(e^{M_1 t}, e^{M_2 t}) \end{bmatrix} = \begin{bmatrix} i_{Lsr\_c}(t) \\ v_{2r\_c}(t) \\ v_{2r\_c}(t) \end{bmatrix} \quad t \in T_c$$

with

$$\begin{aligned}
M_1 &= -(\tau_t + \tau_s + \sqrt{(\tau_t - \tau_s)^2 - 4\tau_t\tau_s^2/\tau_l})/(2\tau_t\tau_s) \\
M_2 &= -(\tau_t + \tau_s - \sqrt{(\tau_t - \tau_s)^2 - 4\tau_t\tau_s^2/\tau_l})/(2\tau_t\tau_s) \\
M_3 &= -(1 + \sqrt{1 - 4\omega_o\tau_s^2})/(2\tau_s) \\
M_4 &= -(1 - \sqrt{1 - 4\omega_o\tau_s^2})/(2\tau_s) \\
M_5 &= -1/\tau_f \\
\tau_l &= L_{sr}/R_{lr} \\
\omega_o &= 1/(L_{sr}C_{ossr}).
\end{aligned}$$

The state vector $\mathbf{x}(t)$ is continuous over the time instants t_1 and t_2 since the inductor currents and the capacitor voltages can not change instantaneously, and so

$$\begin{aligned}
\mathbf{x_a}(t_1) &= \mathbf{x_b}(t_1) \\
\mathbf{x_b}(t_2) &= \mathbf{x_c}(t_2).
\end{aligned} \tag{4.7}$$

Moreover, due to the odd symmetry of the leakage inductance current $i_{Lsr}(t)$ and the even symmetry of the output voltage $v_{2r}(t)$ as shown in Figure 4.3(a), we have

$$\begin{aligned}
i_{Lsr_a}(t_0) &= -i_{Lsr_c}(t_0 + T_{samp}) \\
v_{2r_a}(t_0) &= v_{2r_c}(t_0 + T_{samp}).
\end{aligned} \tag{4.8}$$

By inserting (4.7) and (4.8) into (4.6), the initial condition $\mathbf{x}(t_0)$ can be determined, however it is usually complicated and may only be calculated numerically. Therefore, an approximation of the exponential function of time, which is involved in the state vector expression (4.6), is necessary if a closed-form solution is sought.

4.4.2 Approximation

The exponential function of time e^{at} can be expressed in terms of an infinite convergent series as

$$e^{at} = \sum_{n=0}^{\infty} \frac{(at)^n}{n!} = 1 + \frac{a}{1!}t + \frac{a^2}{2!}t^2 + \cdots + \frac{a^n}{n!}t^n + \cdots, \tag{4.9}$$

where a is the coefficient and t is the independent variable.

The state vector $\mathbf{x}(t)$ can be approximated by replacing the exponential term with the n-order series where the resulting n-order polynomial function is denoted by $\mathbf{x}_{(n)}(t)$. The more higher-order terms are included in the exponential expansion are included, the closer the approximation is to the actual function, however this also increases the complexity of the state vector expression and also the model of the converter. So there is a trade off between complexity and accuracy. Recognizing this, the highest order term included in the exponential expansion is determined according to a limited allowed deviation from the actual function, i.e. the deviation should be smaller than 5% of the variation of the polynomial function value over the whole interval.

As an example, we consider the state vector $\mathbf{x_a}(t)$ for interval a. The leakage inductance current $i_{Lsr\_a}(t)$ can be simplified to $i_{Lsr\_a(n)}(t)$ by neglecting terms with ordinal number higher than n in the exponential expansion as given below

$$i_{Lsr\_a}(t) \approx i_{Lsr\_a}(t)\Big|_{\substack{e^{M_1 t}=1+\frac{M_1}{1!}t+\frac{M_1^2}{2!}t^2\cdots+\frac{M_1^n}{n!}t^n \\ e^{M_2 t}=1+\frac{M_2}{1!}t+\frac{M_2^2}{2!}t^2\cdots+\frac{M_2^n}{n!}t^n}} = i_{Lsr\_a(n)}(t). \quad (4.10)$$

By comparing the first-order approximation $i_{Lsr\_a(1)}(t)$ and actual function $i_{Lsr\_a}(t)$ (cf. Figure 4.4(a)), we can find that the first-order approximation $i_{Lsr\_a(1)}(t)$ is accurate enough to represent $i_{Lsr\_a}(t)$. Although the output voltage $v_{2r\_a}(t)$ contains the same exponential terms, $e^{M_1 t}$ and $e^{M_2 t}$, Figure 4.4(b) shows that first-order approximation $v_{2r\_a(1)}(t)$ deviates largely from the actual function. Therefore, the second-order term in the series of $e^{M_1 t}$ and $e^{M_2 t}$ when the replacement is implemented.

In a summary, the state vector (4.6) can be approximated by the

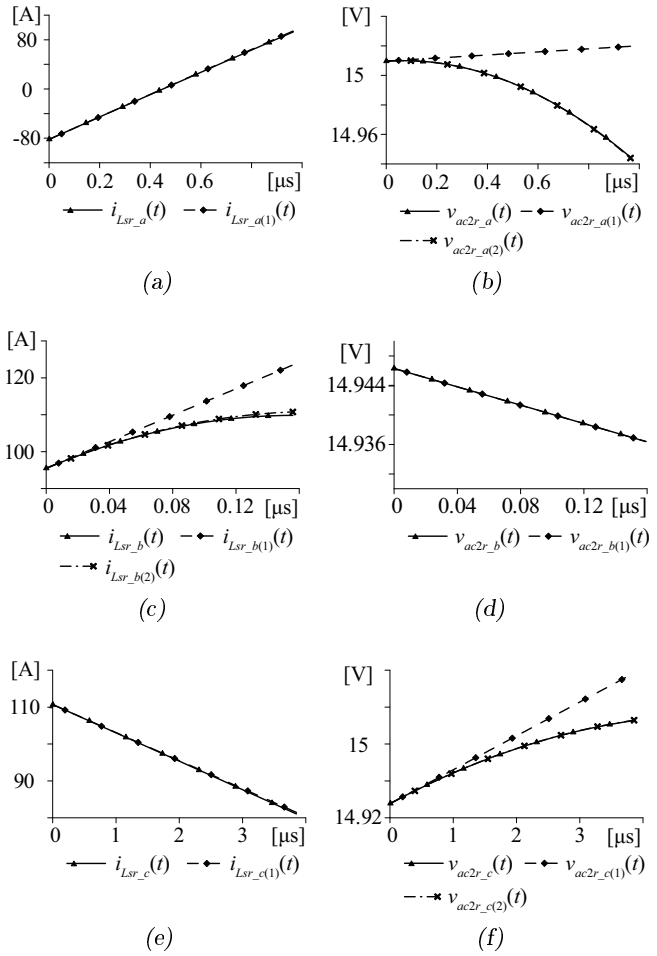


Figure 4.4: (a)-(g) Comparison of the actual state variable instantaneous waveforms with their first- and/or second-order approximations. The circuit and operating parameters are given in Table 4.1 as for Model (d).

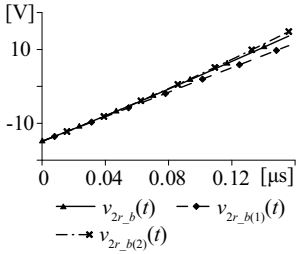


Figure 4.4: (a)-(g) Comparison of the actual state variable instantaneous waveforms with their first- and/or second-order approximations. The circuit and operating parameters are given in Table 4.1 as for Model (d) (continued).

polynomial functions with small deviation from the actual functions as

$$\begin{aligned}
\mathbf{x_a}(t) &= \begin{bmatrix} i_{Lsr_a}(t) \\ v_{2r_a}(t) \\ -v_{2r_a}(t) \end{bmatrix} \approx \begin{bmatrix} i_{Lsr_a(1)}(t) \\ v_{2r_a(2)}(t) \\ -v_{2r_a(2)}(t) \end{bmatrix} \quad t \in T_a \\
\mathbf{x_b}(t) &= \begin{bmatrix} i_{Lsr_b}(t) \\ v_{2r_b}(t) \\ v_{ac2r_b}(t) \end{bmatrix} \approx \begin{bmatrix} i_{1b(2)}(t) \\ v_{2r_b(1)}(t) \\ v_{ac2r_b(2)}(t) \end{bmatrix} \quad t \in T_b \qquad (4.11) \\
\mathbf{x_c}(t) &= \begin{bmatrix} i_{Lsr_c}(t) \\ v_{2r_c}(t) \\ v_{2r_c}(t) \end{bmatrix} \approx \begin{bmatrix} i_{1c(1)}(t) \\ v_{2r_c(2)}(t) \\ v_{2r_c(2)}(t) \end{bmatrix} \quad t \in T_c.
\end{aligned}$$

4.4.3 Discretization

As stated in [87, 88], the discrete-time modelling method only describes the small-signal behavior of the converter at a sample time instant in each sampling cycle, and does not consider any information in between these instants. Moreover, different positions of the sampling instant result in differences of the predicted frequency response. The above differences can be minimized with the concept of half-cycle-averaging described in next Section 4.4.4. Therefore, the converter waveforms can be sampled at any position in the sampling cycle. Here, only half a switching cycle has to be considered due to the symmetric operation of the DAB converter.

One switching cycle includes two sampling cycles, the positive half switching cycle of v_{ac1r}, which is indicated as an odd k sampling cycle, and the negative half switching cycle of v_{ac1r}, which is indicated as an even k sampling cycle. Let $\mathbf{x}[k]$ represent the state vector at the beginning of the k^{th} sampling period

$$\mathbf{x}[k] = \left[i_{Lsr}[k]\ v_{2r}[k]\ v_{ac2r}[k]\right]^T, \tag{4.12}$$

where t is replaced by kT_{samp}, and k is an integer.

When k is odd, the terminal voltage $v_{ac2r}(t)$ of the intermediary circuit is equal to the inverse of the output voltage $v_{2r}(t)$, i.e. $v_{ac2r}[k] = -v_{2r}[k]$ since a pair of diagonal switches conducts in interval a (cf. Figure 4.3(b)). Similarly, $v_{ac2r}[k] = v_{2r}[k]$ when k is even. The terminal voltage $v_{ac2r}[k]$ can be removed from the state vector $\mathbf{x}[k]$, which now is

$$\mathbf{x}[k] = \left[i_{Lsr}[k]\ v_{2r}[k]\right]^T. \tag{4.13}$$

The input voltage V_1 is considered as constant since we are interested only in the control-to-output response. At the time instant t_2, i.e. at the end of interval b, the response of the terminal voltage $v_{ac2r}(t)$ and the output voltage $v_{2r}(t)$ can be expressed as functions of the state variables $\mathbf{x}[k]$, the control input $\phi_1[k]$ at the beginning of the period and the time duration $T_b[k]$ of interval b in the period

$$\begin{aligned} v_{ac2r}(t_2) &= f_{vac2r\_b}(\mathbf{x}[k], \phi_1[k], T_b[k]) \\ v_{2r}(t_2) &= f_{v2r\_b}(\mathbf{x}[k], \phi_1[k], T_b[k]). \end{aligned} \tag{4.14}$$

The time instant t_2 is also the starting point of interval c, in which $v_{ac2r}(t) = v_{2r}(t)$ due to the conduction of another pair of diagonal switches. Therefore,

$$v_{ac2r}(t_2) = v_{2r}(t_2). \tag{4.15}$$

Substituting (4.14) into (4.15), the time duration $T_b[k]$ of interval b can be determined and is expressed as a function of the state variables $\mathbf{x}[k]$ and the control input $\phi_1[k]$

$$T_b[k] = f_{tb}(\mathbf{x}[k], \phi_1[k]). \tag{4.16}$$

Combining (4.16) and the approximated state vector expression (4.11),

the state vector at the end of the k^{th} half switching period $\mathbf{x}[k+1]$ when k is odd can be expressed as a function of the initial conditions $\mathbf{x}[k]$ and $\phi_1[k]$

$$\mathbf{x}[k+1] = \begin{bmatrix} f_i'(\mathbf{x}[k], \phi_1[k]) \\ f_v'(\mathbf{x}[k], \phi_1[k]) \end{bmatrix}. \tag{4.17}$$

The leakage inductance current $i_{Lsr}[k+1]$ at the end of the k^{th} half switching cycle has an inverse sign compared to $i_{Lsr}[k]$ at the beginning of the same half switching cycle due to its odd symmetry. Substituting $i_{Lsr}[k] = -i_{Lsr}[k]$ into (4.17) when k is odd or $i_{Lsr}[k+1] = -i_{Lsr}[k+1]$ into a similar group of the difference equations describing the second half switching cycle when k is even, a general discrete state vector equation, which can be updated every half switching cycle, is obtained

$$\mathbf{x}[k+1] = \begin{bmatrix} f_i(\mathbf{x}[k], \phi_1[k]) \\ f_v(\mathbf{x}[k], \phi_1[k]) \end{bmatrix} = \begin{bmatrix} f_i[k] \\ f_v[k] \end{bmatrix}. \tag{4.18}$$

4.4.4 Averaging over a Half Switching Cycle

In the DAB DC-DC converter, the leakage inductance current is purely an AC current and has relatively large ripple. This leads to differences of the predicted frequency response obtained by discrete-time modelling method for different sampling time instants. Considering this, we introduce a new sample $v_{2r\_avg}[k+1]$ to minimize this difference, which represents the averaged value of the output voltage defined as

$$\begin{aligned} v_{2r\_avg}[k+1] &= \frac{1}{T_{samp}} \int_{kT_{samp}}^{(k+1)T_{samp}} v_{2r}(t)dt \\ &= f_{v\_avg}(\mathbf{x}[k], \phi_1[k]) = f_{v\_avg}[k]. \end{aligned} \tag{4.19}$$

This new sample $v_{2r\_avg}[k+1]$, which is expressed as a function $f_{v\_avg}[k]$ in terms of the initial value of the state vector $\mathbf{x}[k]$ and the control signal $\phi_1[k]$, is used instead of $v_{2r}[k+1]$ to develop the large-signal discrete-time model.

4.4.5 Large-signal Discrete-time Model Verification

To verify the accuracy of the developed model, which can be easily implemented in a mathematical software, e.g. in MAPLE, a detailed switching model of the DAB DC-DC converter is built in SIMPLORER, a PSpice-like simulation software. The dynamic response of the converter to a perturbation of the control input, which is a sinusoidal signal with 1/10 switching frequency and 5% steady-state value as amplitude, is carried out for the above two models, respectively. The perturbation in the control input $\Delta\phi_1$, the calculation and simulation results of the leakage inductance current i_{Lsr} and the output voltage v_{2r} are shown in Figure 4.5, where solid lines and broken line represent the instantaneous simulation results and the averaged value of the output voltage from the detailed switching model; squares and rhombuses mark the conventional discrete samples and the discrete average samples based on the developed model. The similarity between the discrete average samples $v_{2r\_avg}[k]$ and the averaged value of the simulated output voltage $v_{2r\_avg}(t)$ in shape, frequency and magnitude confirms the validity of the developed large-signal model.

4.5 Perturbation around a Steady State

A switching converter with an appropriate control operates in a cyclic steady state. It is important to know the dynamic response to a small perturbation in the control signal of the converter around this steady state in order to design a feedback controller to ensure stability and enhance performance of the entire system.

The starting point is the large-signal discrete-time model in (4.13), (4.18) and (4.19) for the DAB converter developed in the last section. When a small perturbation occurs in the control signal, the state vector and the output variable deviate from their steady state values, i.e.

$$\begin{aligned}
\phi_1[k] &= \phi_1[k] + \Delta\phi_1[k] \\
\mathbf{x}[k] &= \mathbf{X}[k] + \Delta\mathbf{x}[k] \\
v_{2r_avg}[k] &= V_{2r_avg}[k] + \Delta v_{2r_avg}[k] \\
\mathbf{x}[k+1] &= \mathbf{X}[k+1] + \Delta\mathbf{x}[k+1] \\
v_{2r_avg}[k+1] &= V_{2r_avg}[k+1] + \Delta v_{2r_avg}[k+1].
\end{aligned} \tag{4.20}$$

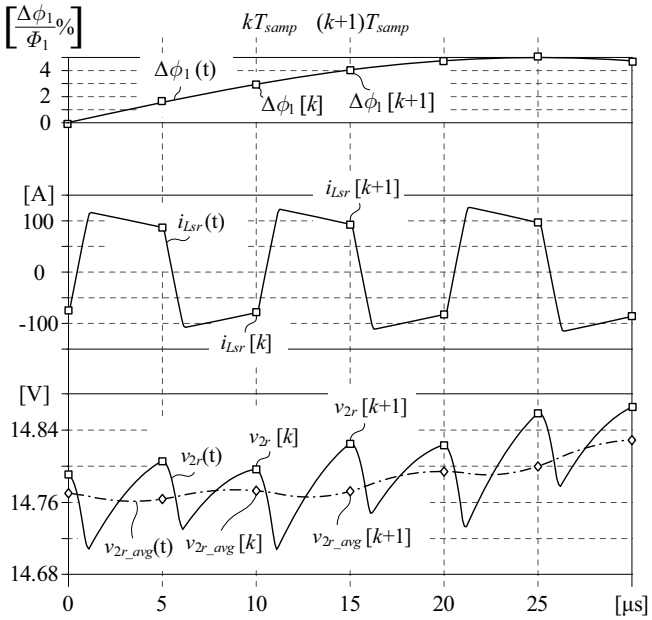


Figure 4.5: Comparison of the calculated DAB DC-DC converter dynamic response using the developed model and the simulated waveforms of the detailed switching model to a perturbation of the control input. Solid and broken line represent the instantaneous simulation results and the averaged value of the output voltage of the detailed switching model, respectively. Squares and rhombuses mark the conventional discrete samples and the discrete average samples of the developed model, respectively. The assumed circuit and operating parameters are given in Table 4.1.

where capital letters refer to the steady states and the terms involving Δ represent small signal variations.

Substituting (4.20) into (4.18) and (4.19), applying a Taylor series expansion around the steady state and neglecting the second and higher order terms, we obtain

$$\begin{aligned} \Delta\mathbf{x}[k+1] &= \mathbf{A}\Delta\mathbf{x}[k] + \mathbf{B}\Delta\phi_1[k] \\ \Delta v_{2r\_avg}[k+1] &= \mathbf{C}\Delta\mathbf{x}[k] + \mathbf{E}\Delta\phi_1[k] \end{aligned} \tag{4.21}$$

with

$$\mathbf{A} = \begin{bmatrix} \dfrac{\partial f_i[k]}{i_{Lsr}[k]} & \dfrac{\partial f_i[k]}{v_{2r}[k]} \\ \dfrac{\partial f_v[k]}{i_{Lsr}[k]} & \dfrac{\partial f_v[k]}{v_{2r}[k]} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} \dfrac{\partial f_i[k]}{\phi_1[k]} \\ \dfrac{\partial f_v[k]}{\phi_1[k]} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} \dfrac{\partial f_{v\_avg}[k]}{i_{Lsr}[k]} & \dfrac{\partial f_{v\_avg}[k]}{v_{2r}[k]} \end{bmatrix}$$

$$\mathbf{E} = \begin{bmatrix} \dfrac{\partial f_{v\_avg}[k]}{\phi_1[k]} \end{bmatrix}.$$

Using the z-transformation on (4.21), the control-to-output-voltage small-signal transfer function can be written as

$$\begin{aligned} G^*_{vd\_avg}(s) &= \frac{\Delta v^*_{2\_avg}(s)}{\Delta\phi^*_1(s)} \\ &= \left.\frac{\Delta v_{2\_avg}(z)}{\Delta\phi_1(z)}\right|_{z=e^{sT_{samp}}} = \left.\frac{n_1\Delta v_{2r\_avg}(z)}{\Delta\phi_1(z)}\right|_{z=e^{sT_{samp}}} \\ &= n_1(\mathbf{C}(z\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}+\mathbf{E})\Big|_{z=e^{sT_{samp}}}, \end{aligned} \tag{4.22}$$

where $\mathbf{I}$ is the identity matrix.

4.6 Simulation and Experimental Results

The experimental setup for measuring the control loop frequency response shown in Figure 4.6 has been built and experimentally tested to verify the proposed dynamic model. The prototype is designed for a power transfer of 1 kW, a switching frequency of 100 kHz, a LV port voltage of 14 V and a nominal HV port voltage of 280 V. The circuit parameters for the power stage of the prototype are given in Table 4.1. The switching devices are implemented with power MOSFETs and two IRF2804S MOSFETs are connected in parallel to form a high current switching device for the LV side. The planar transformer comprises an ELP 64/10/50 ferrite core from EPCOS, a single turn copper foil winding on the LV side and a 20-turn litz wire winding for the HV side. Additionally, a series auxiliary inductor is employed since the leakage inductance of the transformer is so small that very precise digital control phase shift angle would be needed to properly control the power transfer.

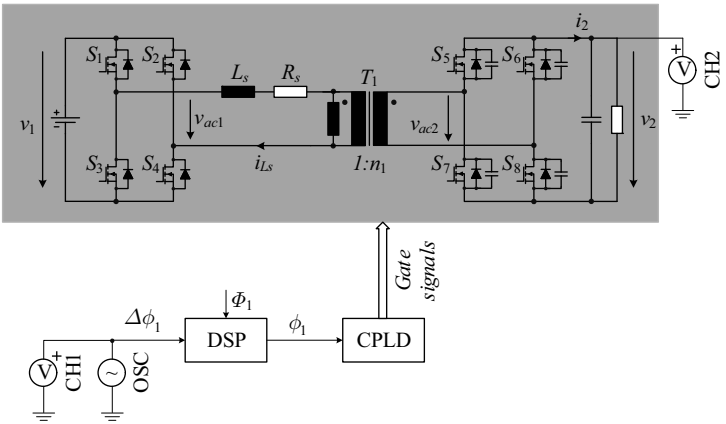


Figure 4.6: Experimental setup for measuring the loop frequency response.

The film/ceramic capacitors, employed as output filter capacitors in the RC load, are placed near to the outputs of the full-bridge units in order to absorb the high frequency AC ripple currents generated by the full-bridge units effectively. No current sensor is inserted between the devices and the filter capacitors. Therefore, the control-to-output-current frequency response is obtained by the detailed switching model simulation

Table 4.1: Circuit and operating parameters for the analytical models, the simulation and the experimental setup.

Parameter	Model (a), (b)	Model (c), (d) and simulation	Experimental converter
V_1	14 V	14 V	14 V
S_1-S_4			IRF2804S*2
L_s	0.16 μH	0.16 μH	0.16 μH[a]
R_s	2.5 mΩ	2.5 mΩ	
n_1	20	20	20
S_5-S_8			IXFX64N60P
C_{oss}		876 pF[b]	390 pF[c]
R_l	82 Ω	82 Ω	82 Ω
C_f	2.82 μF	2.82 μF	2.82 μF
ϕ_1[d]	830 ns[e]	720 ns	720 ns
T_{samp}[f]	5 μs	5 μs	5 μs

[a] Leakage inductance of the transformer T_1 and additional inductor (36 μH) connected in series with the secondary winding of the transformer T_1.

[b] Output capacitance of the MOSFET in the HV unit and snubber capacitor.

[c] Snubber capacitor.

[d] Phase shift angle expressed in seconds which can be transformed into radians; e.g. 830 ns $* \pi / T_{samp} = 0.166\pi$.

[e] Half of the resonant transition time is added.

[f] Sampling time, which is the half switching cycle time.

in SIMPLORER, as shown in Figure 4.7.

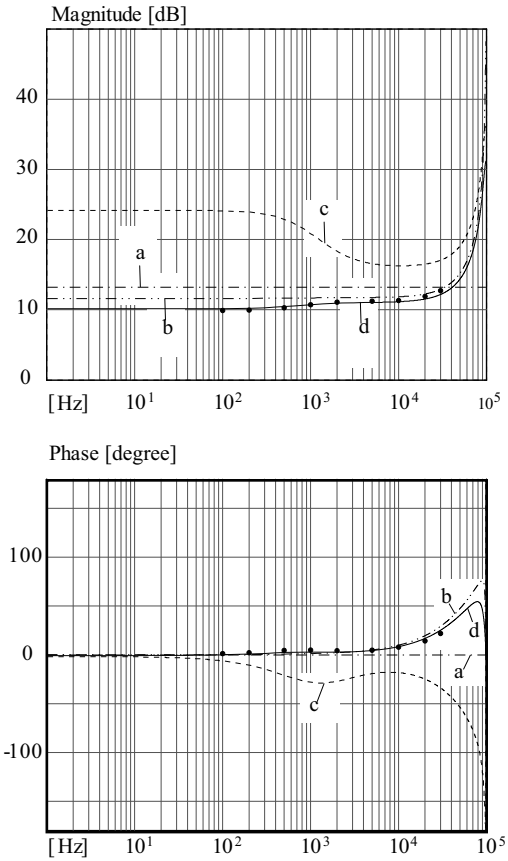


Figure 4.7: Control-to-output-current frequency responses of the DAB DC-DC converter as predicted by Models (a), (b), (c) and (d). Dots represent the detailed switching model simulation results obtained using SIMPLORER.

Furthermore, the control-to-output-voltage response is measured in the frequency domain and illustrated in Figure 4.8. A perturbation $\Delta\phi_1$ of the phase displacement (cf. Figure 4.6) is generated by the Venable Model 350 frequency response analyzer and sampled by the A/D converter of the Analog Devices ADSP-21992 160 MHz DSP. The phase shift

angle value ϕ_1, including the sampled perturbation $\Delta\phi_1$ and the steady-state value ϕ_1, is sent from the DSP to the Lattice ispMACH4512V CPLD to generate the 100 kHz gate signals. There is one switching cycle delay from the perturbation generated by frequency response analyzer to the perturbation of the gate signals. This delay effect, which creates the additional phase shift in the phase response at high frequencies, has been removed from the experimental results.

For comparison, the corresponding frequency responses predicted by four different models with the circuit and operating parameters given in Table 4.1 are also shown in Figure 4.7 and Figure 4.8:

- Model (a), the model derived from the steady-state current, which is presented in [84];
- Model (b), the model derived based on the proposed discrete-time half-cycle-average modelling method, but with the resonant transition intervals neglected;
- Model (c), the model derived based on the conventional discrete-time modelling method without averaging over a half switching cycle, with the resonant transition intervals included;
- Model (d), the developed model with the transfer function given by (4.22). The model is based on the proposed discrete-time half-cycle-average modelling method and considers the resonant transition intervals.

For all of the models, a 2.5 mΩ resistance R_s in the series with the leakage inductance represents the conduction losses of the converter, which slightly reduces the gain of the magnitude response.

For Model (a) and (b), the resonant transition intervals indicated as interval b in Figure 4.3 are neglected, i.e. the converter only goes through intervals a and c within a half switching cycle. The time durations of the interval a and c in Model (a) and Model (b) are both increased by half of the resonant transition time compared to Model (c) and (d). The time duration ϕ_{1_ab} of the phase shift stage indicated as interval a in Model (a) and Model (b) is the sum of half of the resonant transition time t_t and ϕ_{1_cd} for Model (c) and Model (d); i.e. for an example operating

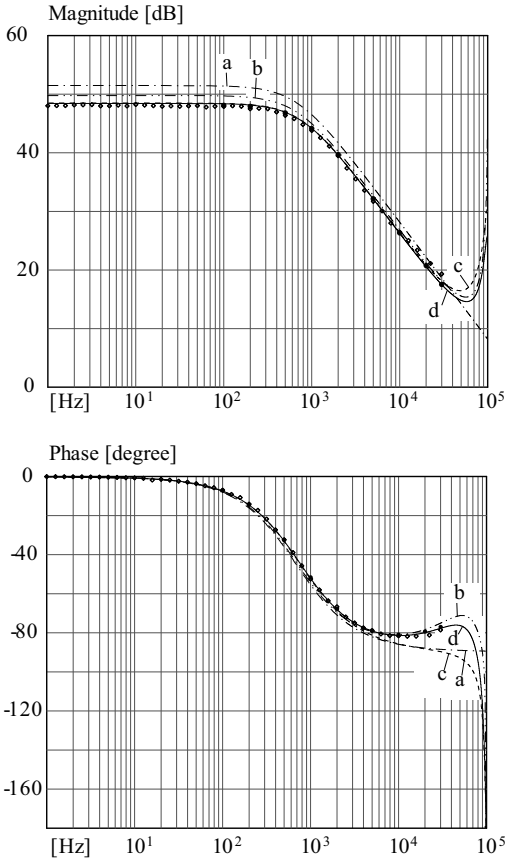


Figure 4.8: Control-to-output-voltage frequency responses of the DAB DC-DC converter as predicted by Models (a), (b), (c) and (d). Dots and rhombuses represent the detailed switching model simulation results obtained using SIMPLORER and the measured results obtained using a Venable Model 350 frequency response analyzer, respectively.

point with circuit parameters given in Table 4.1, this results in

$$\begin{aligned}\phi_{1\_ab} &= \phi_{1\_cd} + t_t/2 \\ &= 720\text{ns} + 220\text{ns}/2 \\ &= 720\text{ns} + 110\text{ns} \\ &= 830\text{ns}.\end{aligned} \tag{4.23}$$

This results in a dc gain predicted by Model (b) higher than that of Model (d) although the same methodology is used for deriving Model (b) and Model (d).

The leakage inductance current is purely an AC current and has a large current swing, therefore the control-to-output frequency response of all discrete models depends significantly on the sampling position. In this paper the sampling position is chosen to be at the time instant t_0, which is at the beginning of interval a. However, in Model (c) a peak detector is applied to the output current in order to better measure the frequency response. Even with the use of the peak detector there is still a large deviation in the predicted response compared to the simulation and experimental results, which can be seen especially in the low-frequency gain of the control-to-output-current magnitude response (cf. Figure 4.7). Once the proposed half-cycle-average concept is adopted, i.e. for Model (d), this deviation is dramatically reduced.

As can be seen, the proposed model gives the most accurate response compared to the experimental results, i.e. the response of the new model shown by a solid line is almost identical to the experimentally measured response represented by the rhombuses in a frequency range up to nearly one third of the switching frequency. The improvement gained by the new model over the other models is obvious, especially considering the low-frequency gain and the phase characteristics at high frequencies.

4.7 Summary

This chapter has proposed a general modelling approach for the DAB converter, which is also applicable to the three-port converter. In this method, the basic operation of the DAB converter with the inclusion of the resonant transition intervals is explained, the state-space mathematical

model is developed based on approximations, the discrete-time response of the half-cycle-average value of an output variable is derived and compared with results of a detailed circuit simulation to verify the accuracy of the modelling, and the discrete-time large-signal model is linearized to reveal the small-signal characteristics of the converter.

A 1 kW prototype is built and the output voltage frequency response is measured. It is found that the developed model provides the accurate frequency response, up to one third of the switching frequency, when compared to measurement results.

Chapter 5

Control Strategy for the Three-port Converter

5.1 Introduction

It is difficult to build a full-order small-signal model for the phase-shift controlled converter using the conventional state-space averaging technique since the ac current of the leakage inductance, whose average value over one switching cycle is always zero, can not be a state variable in the model derived using the state-space averaging method. The full-order small-signal model of the DAB converter is presented in the Chapter 4 using the discrete-time modelling method and the half-cycle-average concept. According to the Figure 4.7 and 4.8, where the control-to-output-current and control-to-output-voltage frequency responses of the DAB converter predicted by four different models are plotted, the proposed model provides the most accurate frequency response, up to one third of the switching frequency.

Generally in the digital control system, the ratio between the sampling rate and the system bandwidth may be required to be 10 to 20 considering the smoothness issue and the reduction of the delay between the control inputs and outputs [94]. That is, the small-signal model should predict the frequency response precisely up to 5 kHz in the case where the sampling rate of the digital control is 50 kHz. Although the full-order

small-signal model stated in the Chapter 4 is accurate enough in the interesting frequency range of the digital control technique, it is mathematically complicated. This chapter aims to present a simple approximative way to derive a control-oriented system model.

Furthermore, as mentioned in Section 3.3.3, two degrees of the freedom, i.e. the phase shift angles ϕ_1 and ϕ_2, are available as control variables. For the multiple voltage electrical system in the HEVs and FCVs, where energy storage elements, such as batteries or super-capacitors, are connected to the buses to stabilize the bus voltages, it is desirable to control the charging/discharging currents. Therefore two port currents of the converter, e.g., i_2 and i_3 (cf. Figure 2.1), could be the control objectives. The system could be considered as a two input (ϕ_1 and ϕ_2) and two output (i_2 and i_3) system. The design and the implementation of the control strategy for this multi-variable system are also discussed in this chapter.

5.2 Implementation of the Control Strategy

Figure 3.13 (redrawn here as Figure 5.1) shows the implemented three-port system, where port 1 is connected with a voltage source $V_1 = 300$ V, port 2 is connected with a RC load, and port 3 is connected with a RC load in parallel to a voltage source $V_3 = 14$ V; therefore port 3 can sink or source power or remain at zero power. L_{p1}, L_{p2} and L_{p3} are the parasitic stray inductances (or possibly small discrete external inductors) acting as parts of the CLC filters, and are used to limit the ripple currents flowing through the electrolytic capacitors into the RC loads. Film/ceramic capacitors are placed near to the outputs of the full-bridge cells in order to absorb the high frequency ac ripple currents effectively. Therefore, i_{2M} and i_{3M} are measured instead of i_2 and i_3, respectively. The output voltage v_{2M} of port 2 is also regulated. Therefore, the whole control system includes two inner current loops and one outer voltage loop.

The control strategy is implemented in an Analog Devices ADSP-21992 160 MHz DSP and a Lattice ispMACH4512V CPLD. The values of the five degrees of freedom, i.e. the phase displacements ϕ_1 *and* ϕ_2 and the duty cycles δ_1, δ_2 *and* δ_3 of the optimum operating point, are calculated numerically in advance and are stored in the DSP as look-up tables with the current reference signals as index parameters. The elements of the decoupling matrix (cf. Section 5.4) are also calculated in advance and

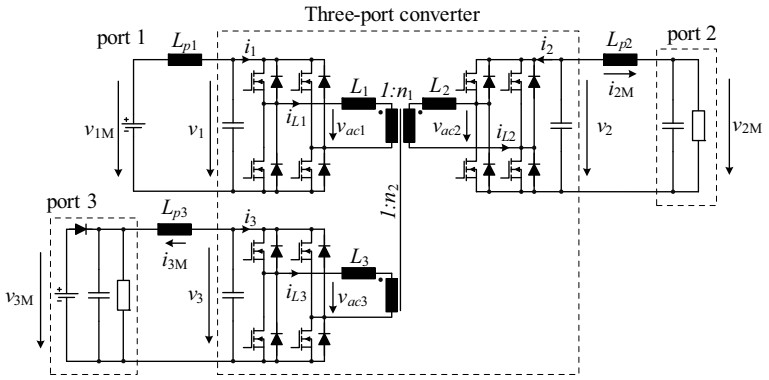


Figure 5.1: Implemented three-port system. Port 1 is connected with a voltage source; port 2 is connected with a RC Load and port 3 is connected with a RC load in parallel to a voltage source.

stored in the DSP as look-up tables.

The DSP operates with a sampling frequency of 50 kHz for all the current and voltage control loops. The voltage v_{2M} is first sampled by the DSP internal 14-bit ADC and then the voltage controller generates the reference i_{2M_ref} for the inner current loop. The current reference values are used as inputs to the multiple look-up tables to calculate the phase displacements and duty cycles. To generate higher precision output values from the look-up tables, the DSP uses linear interpolation rather than the direct discrete values. Thus the system is then able to operate closer to its optimal point. The outputs of the two phase shift angle look-up tables are adjusted by the controllers and manipulated by the decoupling network to eliminate the interaction between two current loops. Then together with the outputs of three duty cycle look-up tables, the five values are written into the CPLD where the correct 100 kHz PWM patterns are generated.

5.3 Small-signal Model

Assuming that a system operation close to the optimum point A is ensured by the look-up tables, where the five degrees of freedom can be obtained with the reference signals I_{2_ref} and I_{3_ref} as the index parameters, the

controller only has to slightly adjust the control variables, i.e. ϕ_1 and ϕ_2, in a given operating region. Accordingly, a simple approximative way to derive the control-oriented system model is to linearize the static control-to-output characteristic of the converter around the operating point, i.e. to let the leakage inductances tend to zero.

A similar application of this technique is found in [84], where a two-port dc-dc converter was analyzed. The resulting small-signal model is included in Section 4.6 as Model (a). Comparing the frequency responses of Model (a) and the proposed Model (d) in Chapter 4, it is found that:

- The phase responses of Models (a) and (d) in Figure 4.7 and 4.8 are almost identical at low frequencies since the pole due to the leakage inductance appears only at high frequencies, close to the converter switching frequency. Therefore, the influence of the leakage inductance can be neglected if the model is used to predict low-frequency dynamics.
- The difference of the DC gains of the magnitude responses of Models (a) and (d) is caused by the duration of the resonant transition, as explained in Section 4.6 (cf. (4.23)). By adding half of the resonant transition time of Model (d) to the phase-shift time, Model (a) can also provide a magnitude response with accurate DC gain.

Therefore, the small-signal model, which can predict the accurate frequency response in the interesting frequency range of the digital control, can be derived in a simple approximative way. The procedure of deriving such a model port 2 is illustrated in the following.

The current i_2 can be expressed according to (3.10) and (3.11) as

$$\begin{aligned} &= \frac{P_{21} + P_{23}}{V_{2r}\, n_1} \\ &= \frac{-P_{12} + P_{23}}{V_{2r}\, n_1} \\ &= -\frac{4}{\pi^3 f_s L_{12r}\, n_1} V_{1r} \cos(\delta_1) \cos(\delta_2) \sin(\phi_1) \\ &\quad + \frac{4}{\pi^3 f_s L_{23r}\, n_1} V_{3r} \cos(\delta_2) \cos(\delta_3) \sin(\phi_2 - \phi_1). \end{aligned} \tag{5.1}$$

The Taylor series of the above port current i_2 around the operating

point A is

$$\begin{aligned} i_2 &= I_{2A} + \Delta i_2 \\ &= K_{1A}\sin(\phi_{1A}) + K_{2A}\sin(\phi_{2A} - \phi_{1A}) \\ &\quad + K_{1A}\cos(\phi_{1A})\Delta\phi_1 - K_{2A}\cos(\phi_{2A} - \phi_{1A})\Delta\phi_1 \\ &\quad + K_{2A}\cos(\phi_{2A} - \phi_{1A})\Delta\phi_2 \\ &= I_{2A} + G_{11}\Delta\phi_1 + G_{12}\Delta\phi_2, \end{aligned} \tag{5.2}$$

where

$$\begin{aligned} G_{11} &= K_{1A}\cos(\phi_{1A}) - K_{2A}\cos(\phi_{2A} - \phi_{1A}) \\ G_{12} &= K_{2A}\cos(\phi_{2A} - \phi_{1A}) \\ I_{2A} &= K_{1A}\sin(\phi_{1A}) + K_{2A}\sin(\phi_{2A} - \phi_{1A}) \end{aligned}$$

with

$$\begin{aligned} K_{1A} &= -\frac{4}{\pi^3 f_s L_{12r}\, n_1} V_{1r}\cos(\delta_{1A})\cos(\delta_{2A}) \\ K_{2A} &= \frac{4}{\pi^3 f_s L_{23r}\, n_1} V_{3r}\cos(\delta_{2A})\cos(\delta_{3A}). \end{aligned}$$

In analogy, the Taylor series of the port current i_3 at the operating point A can be obtained as

$$\begin{aligned} i_3 &= I_{3A} + \Delta i_3 \\ &= I_{3A} + G_{21}\Delta\phi_1 + G_{22}\Delta\phi_2, \end{aligned} \tag{5.3}$$

where

$$\begin{aligned} G_{21} &= K_{4A}\cos(\phi_{2A} - \phi_{1A}) \\ G_{22} &= K_{3A}\cos(\phi_{2A}) - K_{4A}\cos(\phi_{2A} - \phi_{1A}) \\ I_{3A} &= K_{3A}\sin(\phi_{2A}) - K_{4A}\sin(\phi_{2A} - \phi_{1A}) \end{aligned}$$

with

$$\begin{aligned} K_{3A} &= -\frac{4}{\pi^3 f_s L_{13r}\, n_2} V_{1r}\cos(\delta_{1A})\cos(\delta_{3A}) \\ K_{4A} &= \frac{4}{\pi^3 f_s L_{23r}\, n_2} V_{2r}\cos(\delta_{2A})\cos(\delta_{3A}). \end{aligned}$$

In summary, we have for the small signal transfer function matrix of the three-port converter around the operating point A

$$\Delta\mathbf{I} = \begin{bmatrix}\Delta i_2 \\ \Delta i_3\end{bmatrix} = \begin{bmatrix}G_{11} & G_{12} \\ G_{21} & G_{22}\end{bmatrix} \begin{bmatrix}\Delta\phi_1 \\ \Delta\phi_2\end{bmatrix} = \mathbf{G}\,\Delta\mathbf{\Phi}. \tag{5.4}$$

5.4 Design of the Decoupling Network

It can be observed from (5.4) that there is an interaction between the two current loops, which can be eliminated via a special compensation network, i.e. a decoupling network $\mathbf{H}$. The role of the decoupling network is to decompose a multi-variable control system into independent single-loop sub-systems. Thus the system can be controlled using independent loop controllers, e.g, $G_{PI\_2I}(s)$ and $G_{PI\_3I}(s)$, as depicted in the block diagram shown as Figure 5.2, where the non-interacting decoupling control structure proposed in [95] is adopted.

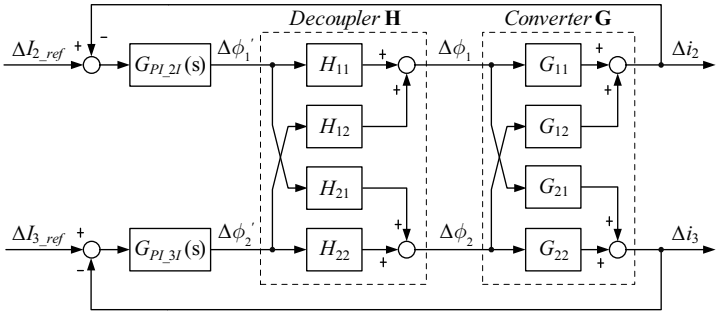


Figure 5.2: Block diagram of the control system with the decoupling network. $\mathbf{G}$ is the small signal transfer function matrix of the three-port converter and $\mathbf{H}$ denotes the transfer function matrix of the decoupling network.

In order to achieve independent control loops, i.e. $\mathbf{X} = \mathbf{GH} = \mathrm{diag}[x_1, x_2]$, the decoupling matrix has to be designed as

$$\begin{aligned}\mathbf{H} &= \begin{bmatrix}H_{11} & H_{12} \\ H_{21} & H_{22}\end{bmatrix} = \mathbf{G}^{-1} = \begin{bmatrix}G_{11} & G_{12} \\ G_{21} & G_{22}\end{bmatrix}^{-1} \\ &= \frac{1}{G_{11}G_{22} - G_{12}G_{21}} \begin{bmatrix}G_{22} & -G_{12} \\ -G_{21} & G_{11}\end{bmatrix}.\end{aligned} \tag{5.5}$$

Thus, $\mathbf{X} = \mathbf{GH} = \mathbf{GG^{-1}} = \text{diag}[1, 1]$. For every optimum operating point A, the small signal transfer function matrix $\mathbf{G}$ of the converter only contains the constants, i.e. no pole or zero is involved since the leakage inductance dynamics are already neglected; same is true for the decoupling network $\mathbf{H}$, which is the inverse matrix of $\mathbf{G}$. Therefore, based on the optimum operating point look up table mentioned above, the elements of the decoupling matrix can be calculated in advance and be stored as look up tables as well.

5.5 Control Loops

In the control system, there are three control loops, two inner current loops and one outer voltage loop, as illustrated in the block diagram Figure 5.3. The response of the voltage loop is slower than the current loops in order to minimize their interaction. This is a typical approach for designing cascaded controllers. Here, we assume that the controllers are well designed and there is no interaction between the loops, i.e. the current loops and the voltage loop are totally decoupled. Accordingly, the output of the voltage loop is considered as constant when analyzing the current loops and for reading values from the look-up tables.

The transfer function of the control loop i_{2M} illustrated in Figure 5.3 with the consideration of the decoupling network is

$$G_{2I}(s) = G_{2I\_M}(s)\, G_{2I\_A}(s)\, G_{AD}(s)\, G_{2I\_D}(s), \tag{5.6}$$

where $G_{2I\_M}(s)$ denotes the $I_2(s)$ to $I_{2M}(s)$ transfer function, $G_{2I\_A}(s)$ and $G_{2I\_D}(s)$ represent the anti-aliasing low-pass filter and the digital low-pass filter, $G_{AD}(s)$ is the transfer function of the sample and hold circuit in the A/D converter. The current loop i_{3M} and voltage loop v_{2M} have similar blocks, except G_{2V_M}(s), which describes the RC load connected to port 2.

Bode plots of the theoretical open loop gain of these loops are illustrated with dashed lines in Figure 5.4, where it can be observed that the magnitude of the gain of the loop controlling i_{2M} is constant at low frequency and starts to drop off beyond the lowest pole frequency of the digital filter. So a PI controller would be sufficient to regulate this loop. The zero of the PI controller is placed around the lowest pole frequency

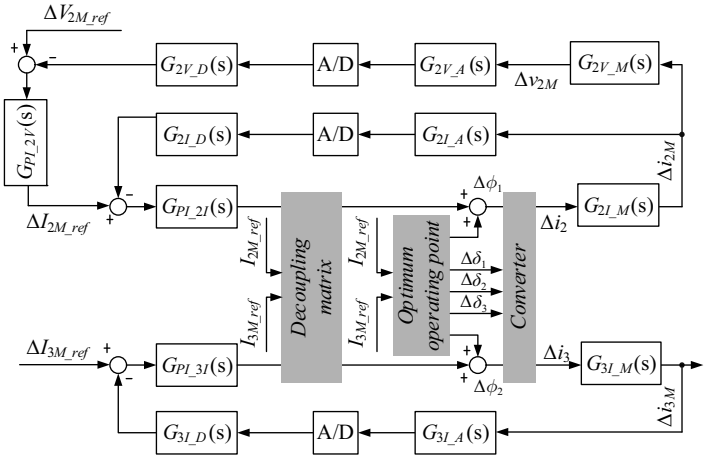


Figure 5.3: Block diagram of the control loops of the implemented three-port converter.

in order to achieve a drop off of the magnitude of -20 dB/dec at the gain crossover frequency; the proportional gain in the PI controller is selected such that enough margin is left between the gain crossover frequency and the frequency where the drop off in the magnitude is -40 dB/dec. In a similar way, the PI controller for the loop controlling i_{3M} can be designed. Due to the pole resulting from the resistor and the capacitor of the RC load, the magnitude of the gain of the loop controlling v_{2M} drops off earlier than that of the loop controlling i_{2M}. The zero of the PI controller for the voltage loop is placed around the pole caused by the RC load. The resulting open-loop gain Bode plots of the three loops including PI controllers are also shown in Figure 5.4, where it can be found that the gain crossover frequencies of the two current loops are around 700 Hz and that the crossover frequency of the voltage loop is around 100 Hz. Although the bandwidth of the two current loops are close, their interaction is avoided by the decoupling network which will be verified experimentally in Section 5.6. The bandwidth of the loop controlling i_{2M} is much higher than that of the loop controlling v_{2M}, so the interaction between these two loops can be minimized. Therefore, the three loops are acting independently.

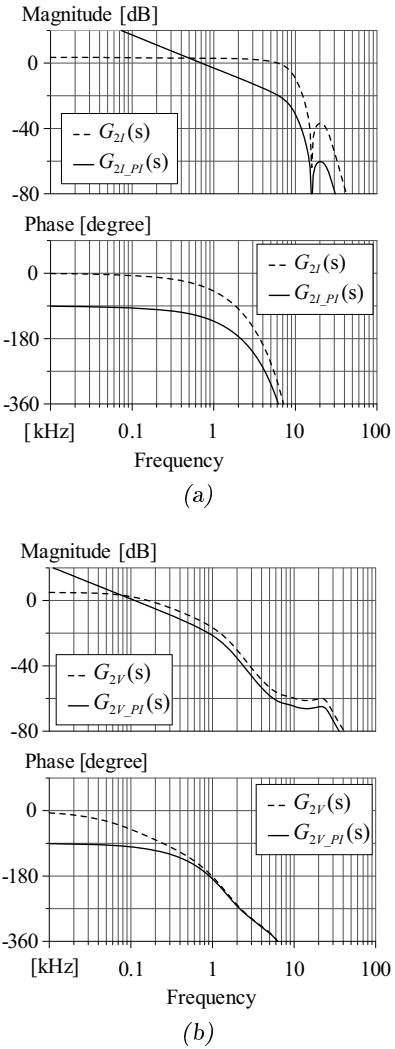
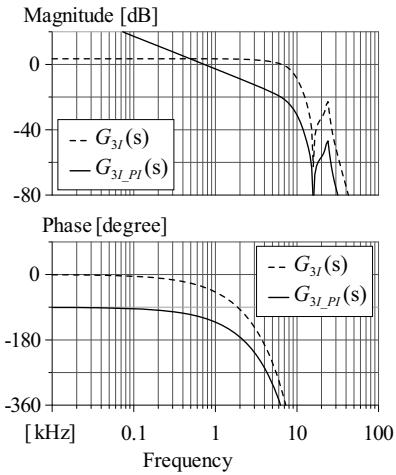


Figure 5.4: Bode plots of the open loop gains of the three-port converter and bode plots of the loop gains with PI controllers: (a) current loop controlling i_{2M}; (b) voltage loop controlling v_{2M}; (c) current loop controlling i_{3M}.



(c)

Figure 5.4: Bode plots of the open loop gains of the three-port converter and bode plots of the loop gains with PI controllers: (a) current control loop i_{2M}; (b) voltage control loop v_{2M}; (c) current control loop i_{3M} (continued).

5.6 Experimental Results

The measured dynamic system behavior, i.e. the response of two port currents i_{2M} and i_{3M} and of the voltage v_{2M} of port 2 in response to current reference I_{3M_ref} variations along with the constant voltage reference signal V_{2M_ref} = 42 V(P_{2_ref} = -1kW), is shown in Figure 5.5. At the beginning the current reference signal I_{3M_ref} is 0 A. It steps to 35.7 A (P_{3_ref} = -500 W) and later steps back to 0 A. From the measured result, the voltage v_{2M} and the current i_{2M} are well regulated, i.e. always kept around the reference values. The control also shows excellent dynamics and no cross-coupling of the control loops is remaining, i.e. the variation of the current reference signal i_{3M} does not influence on the performance of another current loop i_{2M}. This verifies the decoupling of the control loops.

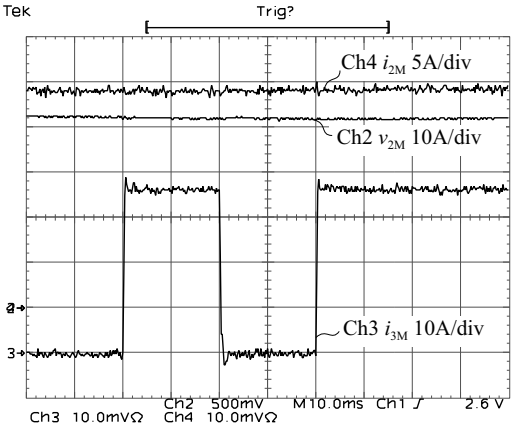


Figure 5.5: Measured dynamic system behavior with a pulsating current reference signal I_{3M_ref} = 0 A, = 35.7 A (P_{3_ref} = -500 W), = 0 A and = 35.7 A and a constant voltage reference signal V_{2M_ref} = 42 V (P_{2_ref} = -1 kW).

5.7 Summary

The control strategy of the three-port converter prototype is of high importance. A system operation with minimum overall power losses is

ensured by pre-calculated look-up tables stored in the DSP. A simple control-oriented system model is presented, which is derived by linearization of the static control-to-output characteristic of the converter since the controller only has to slightly adjust the control variables. The resulting model can predict the accurate frequency response in the frequency range relevant for the digital control. Moreover, the design of the decoupling network, which can decompose the multi-variable control system into independent single-loop subsystems and/or eliminate loop interactions, has been performed since the three-port converter system is a two-input and two-output system. Finally, experimental results verify the decoupled and fast dynamic response of the three-port converter.

Chapter 6

Conclusion

In this thesis, a multi-port converter, which employs less components and shows lower complexity than conventional two-port converters with an intermediate power bus, is studied. Special attention is given to potential applications in multiple voltage electrical systems of hybrid electric vehicles and fuel cell vehicles. Bidirectional power flow capability for the ports interconnecting storage elements and the galvanic isolation between the sources and storage elements are the features of the proposed multi-port converter. The conclusions on the work are grouped for each chapter.

In Chapter 2, an isolated three-port bidirectional converter topology, which consists of three full-bridge units and a high frequency three-winding transformer, is proposed. This topology enables the power transfer between any two ports. In addition, the leakage inductances of the transformer and the output capacitances of the MOSFETs are utilized to achieve the zero-voltage switching for the MOSFETs. The steady-state analysis of the proposed topology is performed based on a Δ-type primary-referred equivalent circuit. There, by properly adjusting the phase shift angle values of the applied voltages, an independent control of the power flow between the ports can be achieved.

In Chapter 3, a duty cycle control for optimizing the system behavior is introduced, in addition to the phase shift control. The circulation of active power inside the three-port converter, which would not contribute to the active input or output power of the ports, is prevented. The overall system losses, which are composed of conduction and switching losses

of the MOSFETs, and of core losses and winding losses of the magnetic components, are estimated. The optimum operating point characterized by the minimum overall system losses is obtained. The theoretical considerations are verified by an experimental set-up. The efficiency of the converter is improved from 72.6% for a non-optimum operating point to 91.7% in the optimum operating point. Moreover, it is found that the calculated and the measured efficiencies of the optimum operating point are in good accordance.

In Chapter 4 a general modelling approach for the DAB converter is proposed, which is also applicable to the three-port converter. For this method, the basic operation of the DAB converter with the inclusion of the resonant transition intervals is explained; the state-space model and the approximations made to simplify the analysis are discussed; the discrete-time response of the half-cycle-average value of an output variable is derived and compared with the detailed circuit simulation to verify the accuracy of the modelling, and the discrete-time large-signal model is linearized to reveal the small-signal characteristics of the converter. A 1 kW prototype is built and the output voltage frequency response is measured. From a comparison to the experimental system, it is found that the developed model provides the accurate frequency response, up to one third of the switching frequency.

The control strategy of the three-port prototype is treated in Chapter 5. A system operation with minimum overall power losses is ensured by pre-calculated look-up tables stored in the DSP. A simple control-oriented system model is presented, which is derived by linearization of the static control-to-output characteristic of the converter since the controller only has to slightly adjust the control variables defined by the look-up table outputs. The resulting model can predict the accurate frequency response in the frequency range relevant for the digital control. Moreover, the design of the decoupling network, which splits the multi-variable control system into independent single-loop subsystems and eliminates control loop interactions, is performed since the three-port converter system is a two-input and two-output system. Finally, experimental results verify the decoupled and fast dynamic response of the three-port converter.

As an overall conclusion one could state that the three-port converter has a large potential for various future applications.

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