ETH zürich

Tutorial

Advanced Modeling and Multi-Objective Optimization / Evaluation of SiC Converter Systems

Ralph M. Burkart & Johann W. Kolar

ETH Zurich, Switzerland

Power Electronic Systems Laboratory

www.pes.ee.ethz.ch

Outline

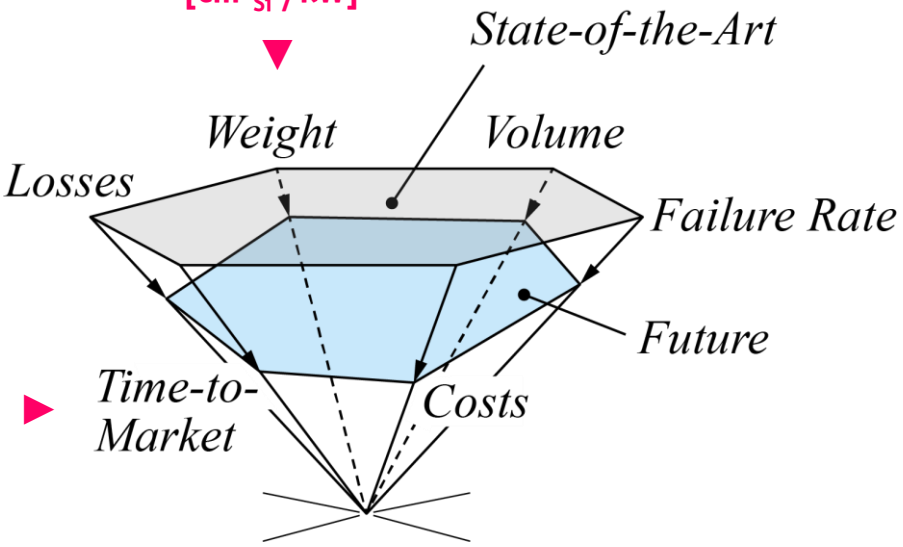
- Introduction
- Basic Multi-Objective Optimization Approach
- *Component Models incl. Costs*
- *Converter Optimization / Evaluation – Example I*
- *Converter Optimization / Evaluation – Example II*
- Conclusions

Introduction

Performance Trends
Performance Space
Pareto Front
Design Space

Power Electronics Converters Performance Trends

Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

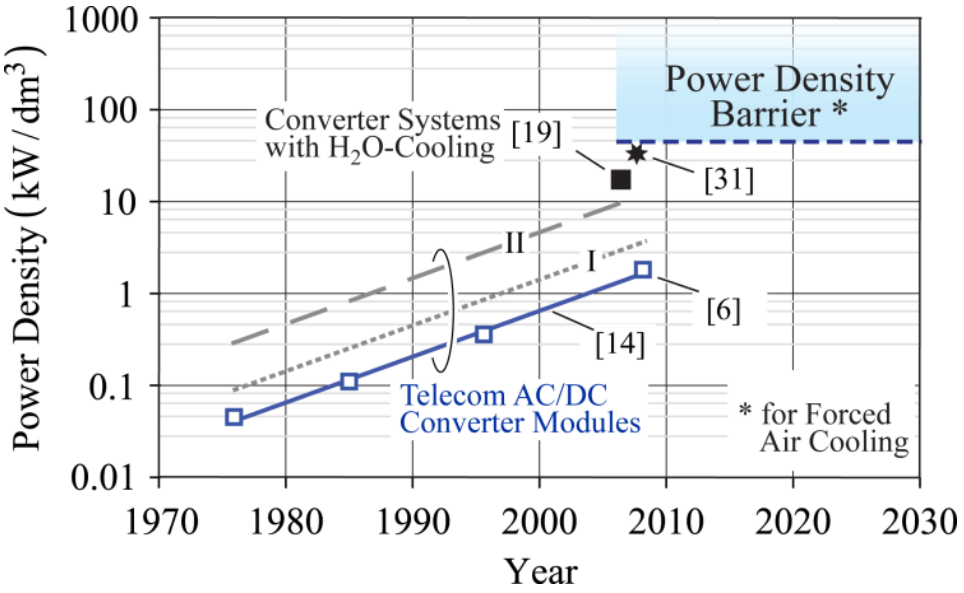


Performance Indices

- Power Density [kW/dm^3]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]

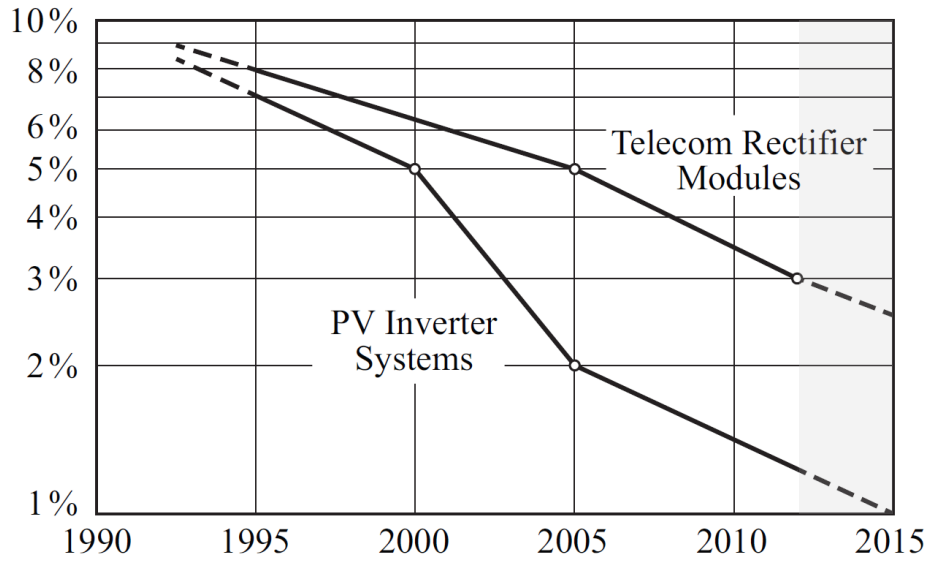
▶ Performance Improvements (1)

- **Power Density**
  - **Telecom Power Supply Modules:**
    Typ. Factor 2 over 10 Years



▶ Performance Improvements (2)

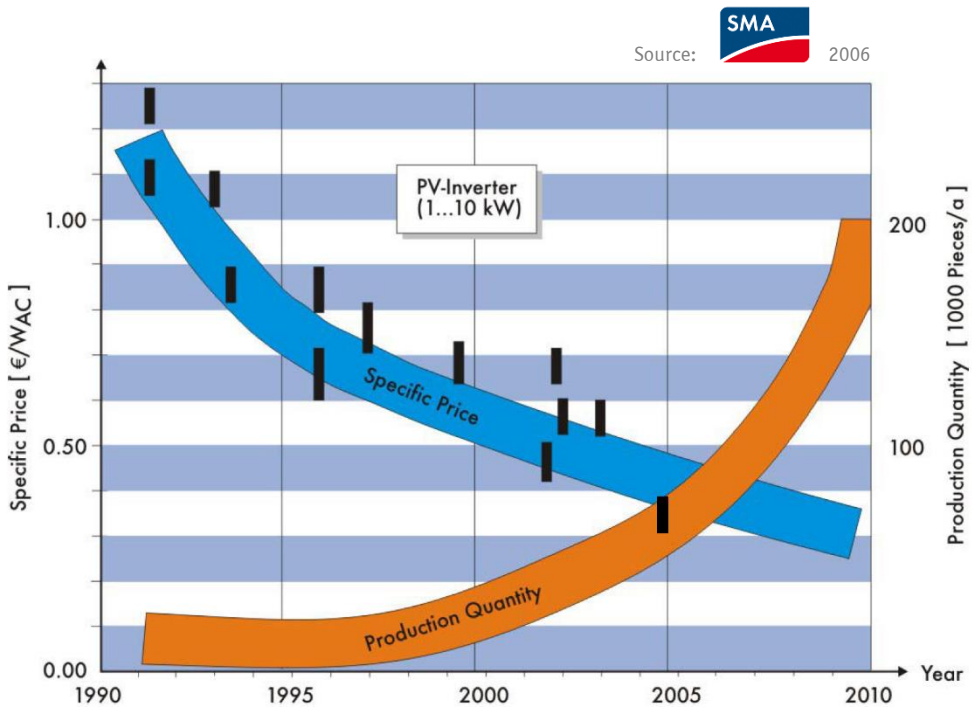
Inefficiency (Losses)... $1-\eta$



- **Efficiency**
  - **PV Inverters: Typ. Loss Red. of Typ. Factor 2 over 5 Years**

Performance Improvements (3)

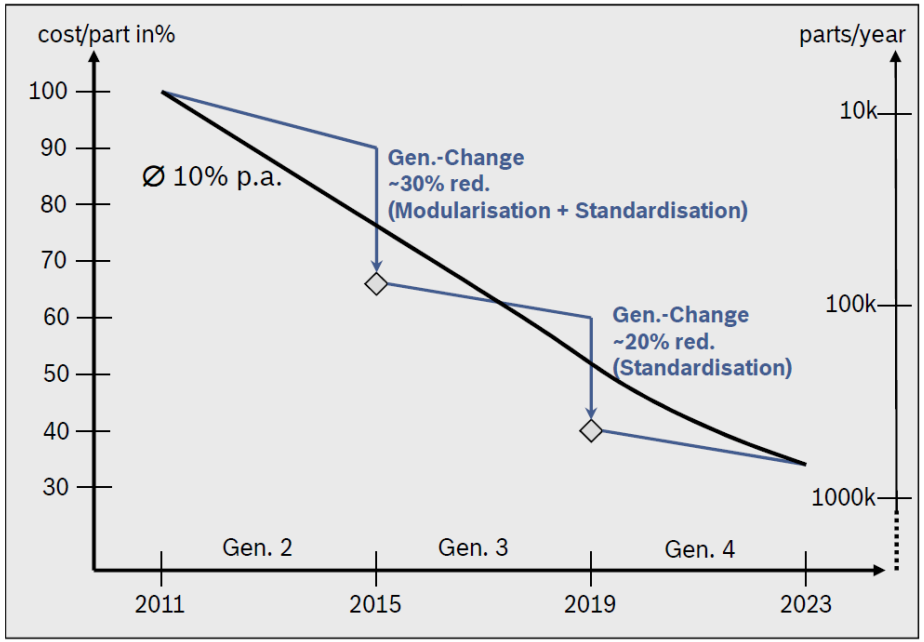
Source: SMA 2006



- **Costs**
  - **Importance of Economy of Scale**

Performance Improvements (4)

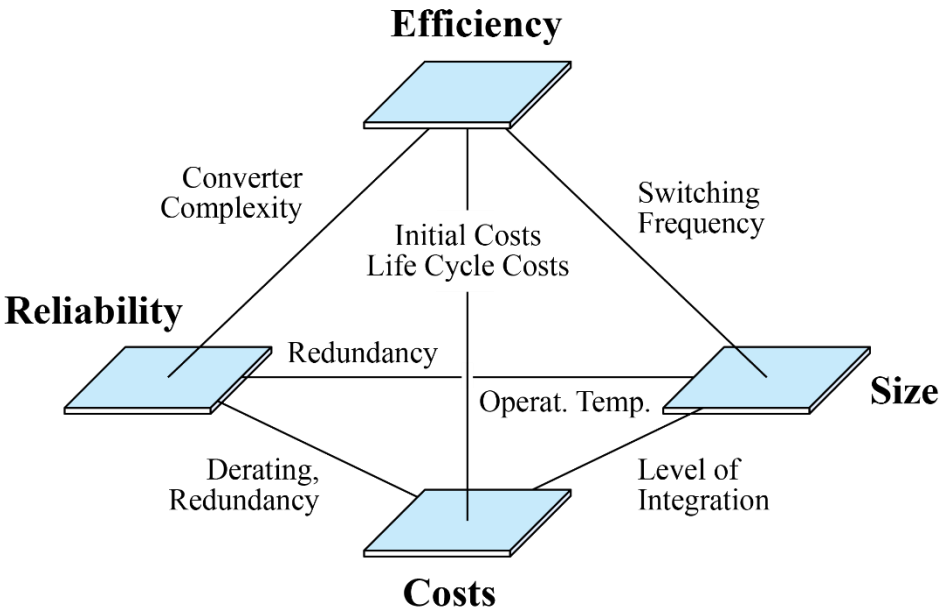
Source: PCIM 2013



- **Costs**
  - Automotive: Typ. 10% / a
  - Economy of Scale !

▶ Design Challenge

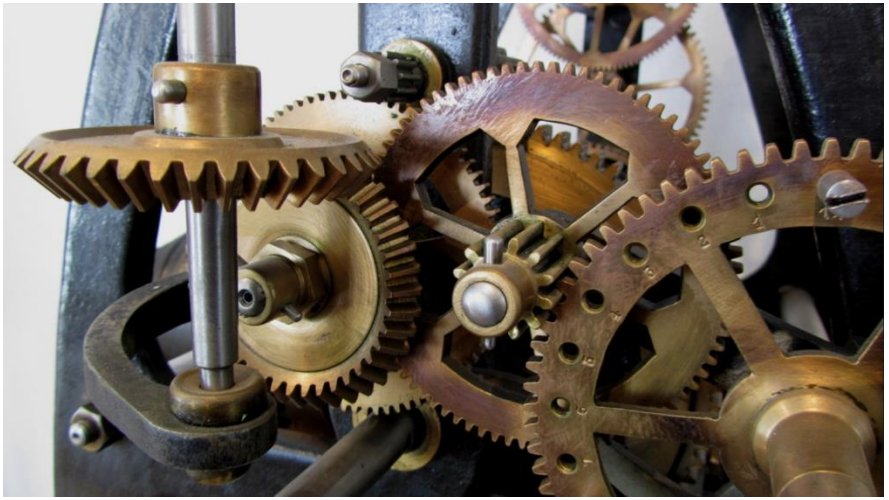
- Mutual Coupling of Performance Indices → Trade-Off Analysis (!)



— For Optimized Systems Several Performance Indices Cannot be Improved Simultaneously

▶ Design Challenge

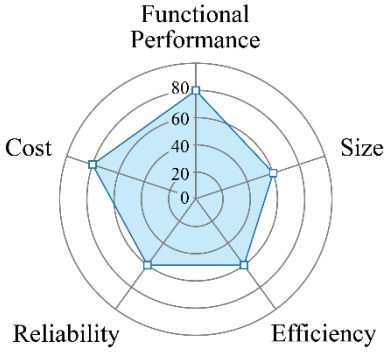
- Mutual Coupling of Performance Indices → Trade-Off Analysis (!)



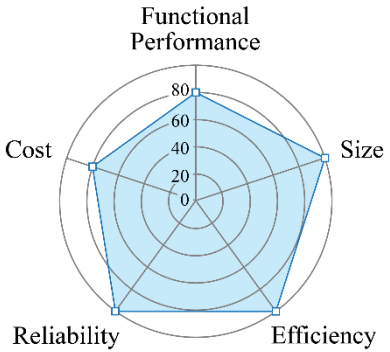
— For Optimized Systems Several Performance Indices Cannot be Improved Simultaneously

Graphical Representation of Performance

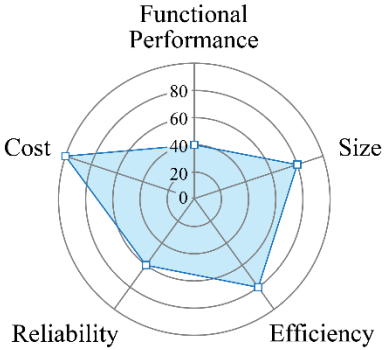
- **Design for Specific Performance Profiles / Trade-Offs Dependent on Application**



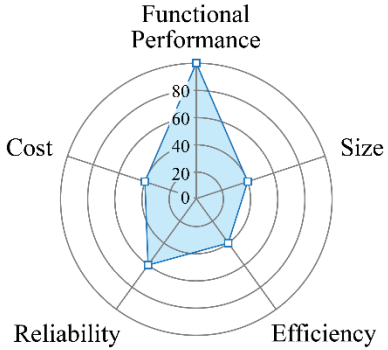
Industry Applications



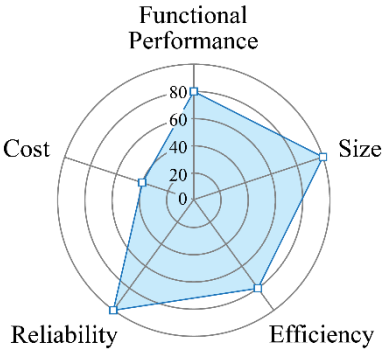
Information & Communication Industry



Domestic Applications



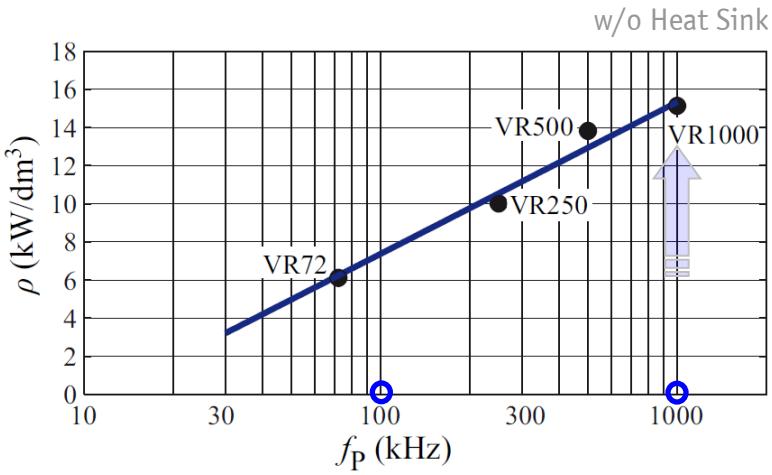
Laboratory Applications



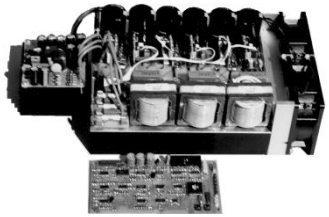
Aerospace Applications

Mutual Coupling of Performances (1)

- Experimental Exploration of the Power Density Improvement of a Three-Phase PFC Rectifier System with Increasing Switching Frequency



f_P = 50 kHz
ρ = 3 kW/dm³



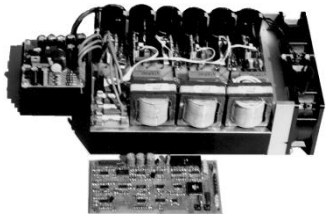
f_P = 72 kHz
ρ = 4.6 kW/dm³

f_P = 250 kHz
ρ = 10 kW/dm³

f_P = 1 MHz
ρ = 14.1 kW/dm³

Mutual Coupling of Performances (2)

- Experimental Exploration of the Power Density Improvement of a Three-Phase PFC Rectifier System with Increasing Switching Frequency



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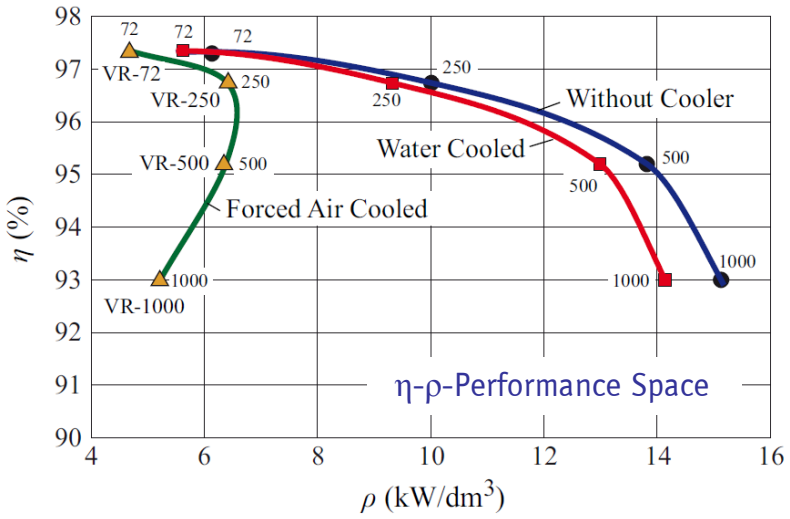
f_P = 1 MHz
ρ = 14.1 kW/dm³

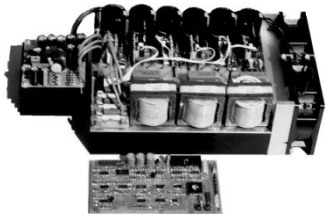
Consideration of a Single Performance Index is NOT Sufficient (!)

Mutual Coupling of Performances (3)

- Consideration of a Single Performance Index is NOT Sufficient (!)
- Trade-Off of Performances Must be Considered → η-ρ-Performance Limit



f_P = 50 kHz
ρ = 3 kW/dm³



f_P = 72 kHz
ρ = 4.6 kW/dm³

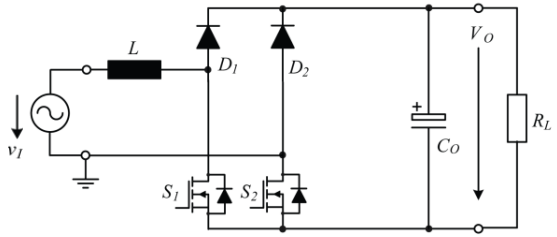
f_P = 250 kHz
ρ = 10 kW/dm³

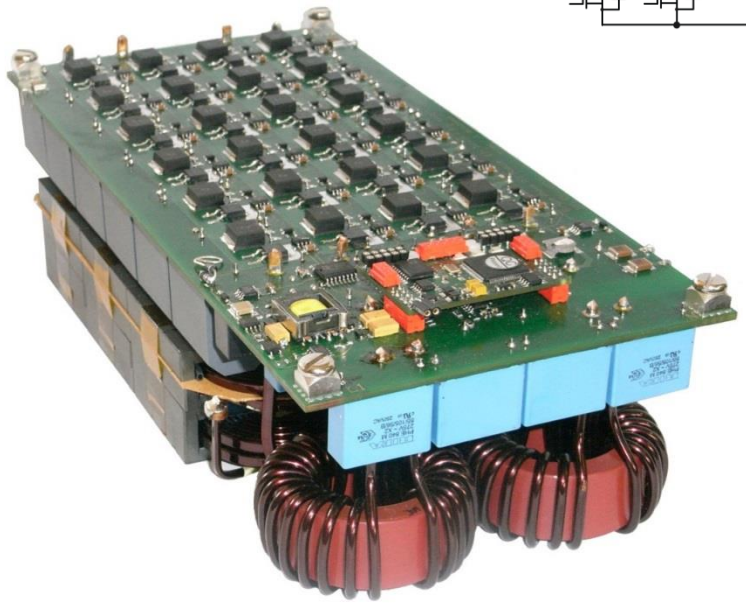
f_P = 1 MHz
ρ = 14.1 kW/dm³

▶ Example of η-ρ-Trade-Off (1)

■ 1-Φ Boost-Type PFC Rectifier

▶ Si CoolMOS, 99mΩ/600V
▶ SiC Diodes, 10A/600V





P_O=3.2kW
U_N=230V±10%
U_O=365V

f_P=33kHz ±3kHz

Two Interleaved
1.6kW Systems

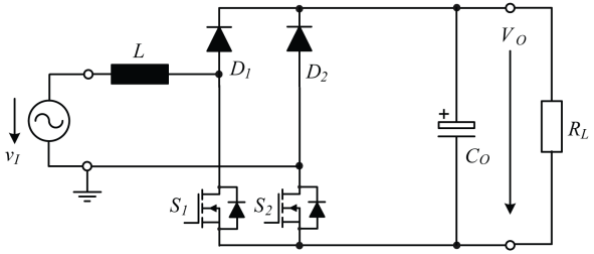
▼

★ 99.2% @ 1.1kW/dm³

▶ Example of η-ρ-Trade-Off (2)

■ 1-Φ Boost-Type PFC Rectifier

▶ Si CoolMOS
▶ SiC Diodes



P_O=3.2kW
U_N=230V±10%
U_O=400V

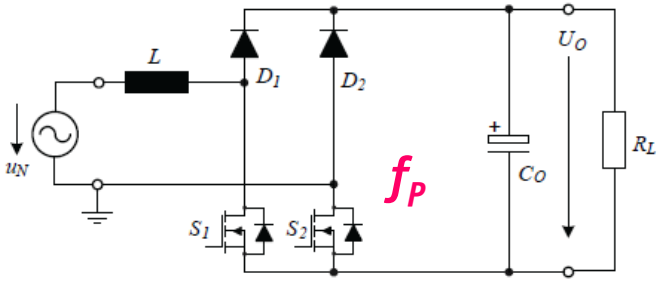
f_P=450kHz ±50kHz

Two Interleaved
1.6kW Systems

▼

★ 5.5kW/dm³ @ 95.8%

Derivation of the η-ρ-Performance Characteristic



* Semiconductors / Heatsink
* Output Capacitor
* Inductor

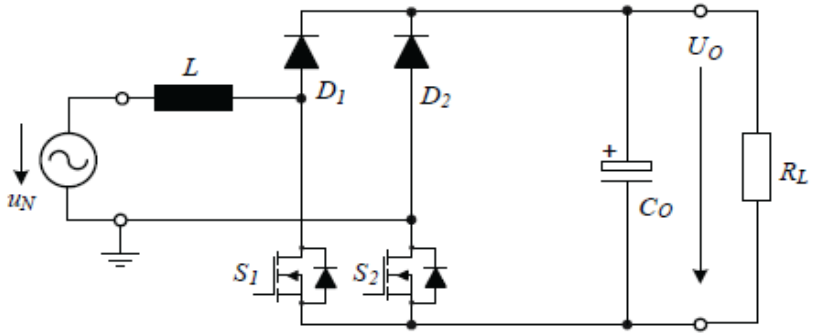
▶ Analysis of η-ρ-Performance Characteristic (1)

■ Specifications / Assumptions

- Rated Output Power P_2
- Const. Input Current Ripple Δi_L
- Const. Output Capacitance C_0 (Energy Storage)
- Const. T_j of Power Semiconductors ≈ T_s
- Def. Ambient Temperature T_a

■ Dependency of Component Losses / Volumes on Switching Frequency f_P

- Input Inductor
- Output Capacitor
- Semiconductors /Heatsink



▶ Analysis of η-ρ-Performance Characteristic (2)

■ Input Inductor

$$\Delta i \propto \frac{U_O}{L} T_P \rightarrow \quad \frac{\Delta i}{I} \propto \frac{U_O}{LI} \frac{1}{f_P} \rightarrow \quad LI \propto \frac{U_O}{\alpha_{\Delta i}} \frac{1}{f_P} \rightarrow \quad LI^2 \propto \frac{U_O I}{\alpha_{\Delta i}} \frac{1}{f_P}$$

($\alpha_{\Delta i}$: $\propto P_O$)

— Inductor Power Density

$$V_L \propto \frac{1}{2} LI^2 \propto \frac{P_O}{f_P} \rightarrow \rho_L = \frac{P_O}{V_L} \propto f_P$$

— Relative Inductor Losses

$$P_L = P_W + P_C \approx P_0 + k_L f_P^{\alpha_L} \rightarrow \varepsilon_L = \frac{P_L}{P_O} \propto (1 + \kappa_L f_P^{\alpha_L})$$

■ Output Capacitor

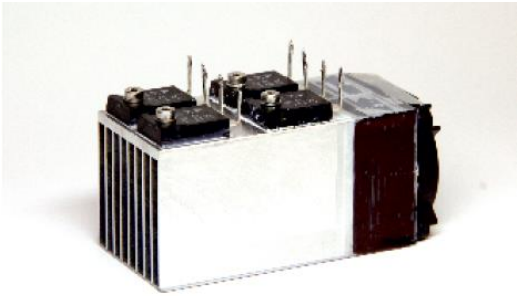
$$V_C \propto \frac{1}{2} CU_O^2 = \text{const.} \rightarrow \rho_C = \frac{P_O}{V_C} = \text{const.} \qquad P_C \approx 0 \rightarrow \varepsilon_L \approx 0$$

▶ Analysis of η-ρ-Performance Characteristic (3)

■ Semiconductors & Heatsink

Cooling System Performance Index

$$[CSPI] = \left[\frac{\frac{\mathrm{W}}{\mathrm{K}}}{\mathrm{dm}^3} \right]$$



— Relative Semiconductor Losses

$$P_S = P_C + P_P \approx P_C + k_P f_P \quad \rightarrow \quad \varepsilon_S = \frac{P_S}{P_O} \propto (1 + \kappa_P f_P)$$

— Heatsink Volume / "Power Density"

$$CSPI = \frac{G_{th}}{V_S} = \frac{P_S}{\Delta T_{s-a}} \frac{1}{V_S} \quad \rightarrow \quad \rho_S = \frac{P_O}{V_S} = \Delta T_{s-a} CSPI \frac{P_O}{P_S} = \Delta T_{s-a} CSPI \ \varepsilon_S^{-1}$$

▶ Analysis of η-ρ-Performance Characteristic (4)

■ System Efficiency & Power Density in Dependency of f_P

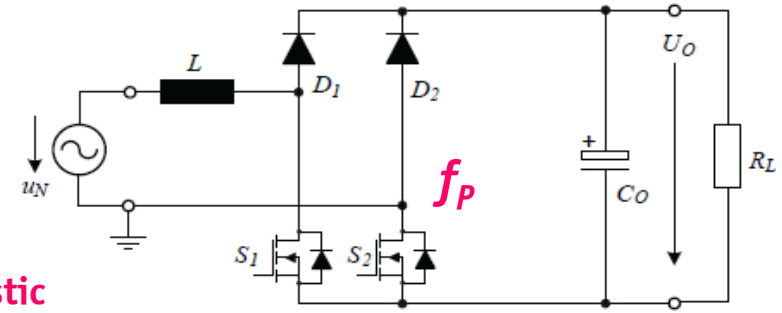
— Efficiency

$$\eta = \frac{P_O}{P_i} = \frac{P_i - (P_L + P_S)}{P_i} = 1 - \frac{(P_L + P_S)}{P_i} \approx 1 - \frac{(P_L + P_S)}{P_O} = 1 - (\varepsilon_L + \varepsilon_S)$$

— Power Density

$$\rho = \frac{P_O}{V} = \frac{P_O}{V_L + V_S + V_C} = \frac{1}{\frac{V_L}{P_O} + \frac{V_S}{P_O} + \frac{V_C}{P_O}} \rightarrow$$

$$\rho = (\rho_L^{-1} + \rho_C^{-1} + \rho_S^{-1})^{-1}$$

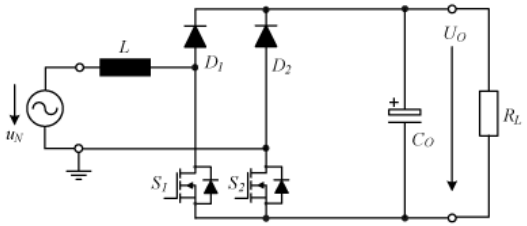


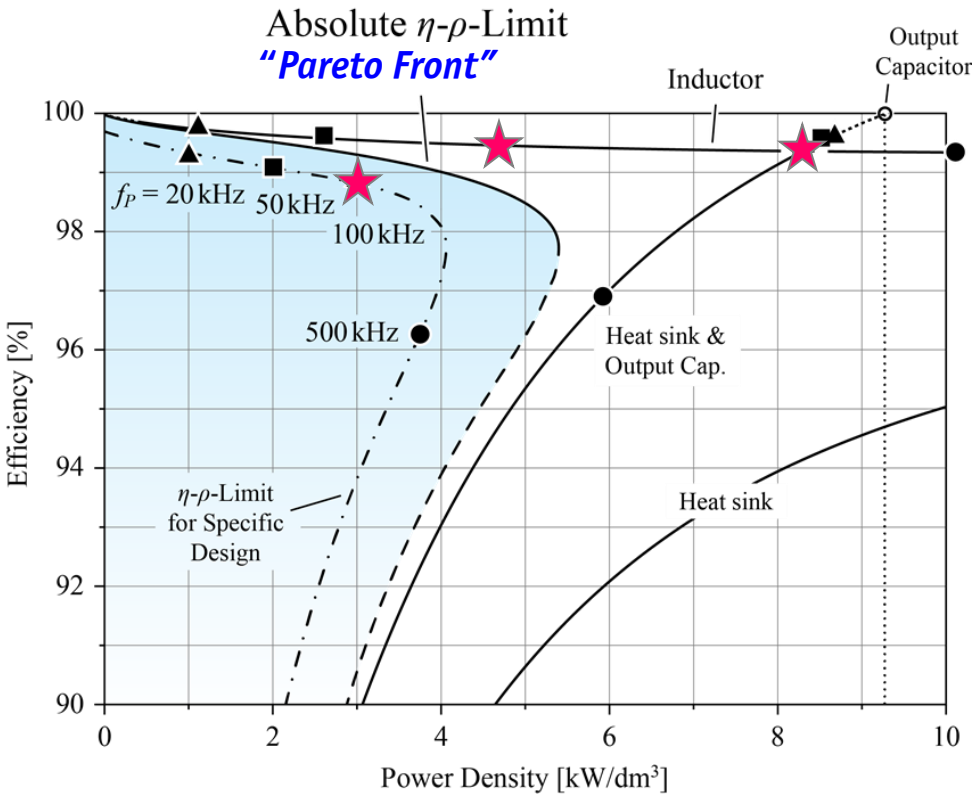
— f_P as Parameter of $\eta = \eta\{\rho\}$ - Characteristic

▶ Analysis of η-ρ-Performance Characteristic (5)

- Specific Design → Only f_P as Variable Design Parameter
- Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute η-ρ-Performance Limit

★ f_P =100kHz

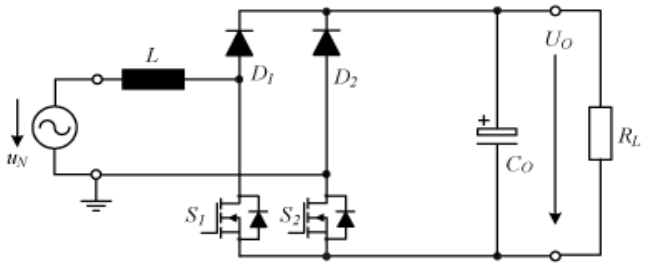




Determination of the η-ρ-Pareto Front

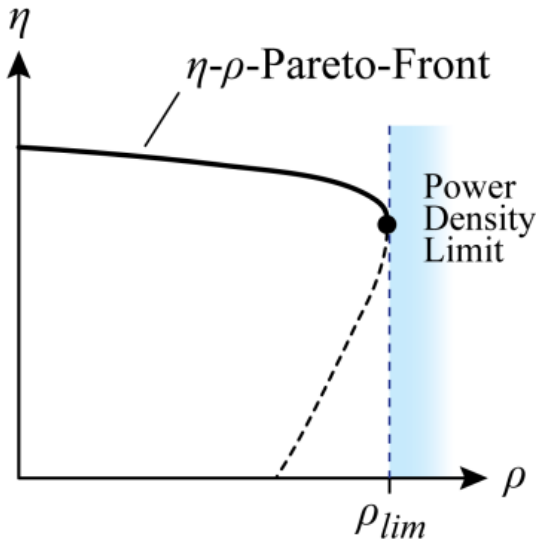
- Comp.-Level Degrees of Freedom of the Design

— Core Geometry / Material
— Single / Multiple Airgaps
— Solid / Litz Wire, Foils
— Winding Topology
— Natural / Forced Conv. Cooling
— Hard-/Soft-Switching
— Si / SiC
— etc.
— etc.
— etc.



- System-Level Degrees of Freedom

— Circuit Topology
— Modulation Scheme
— etc.
— etc.
— etc.



- Only η-ρ-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)

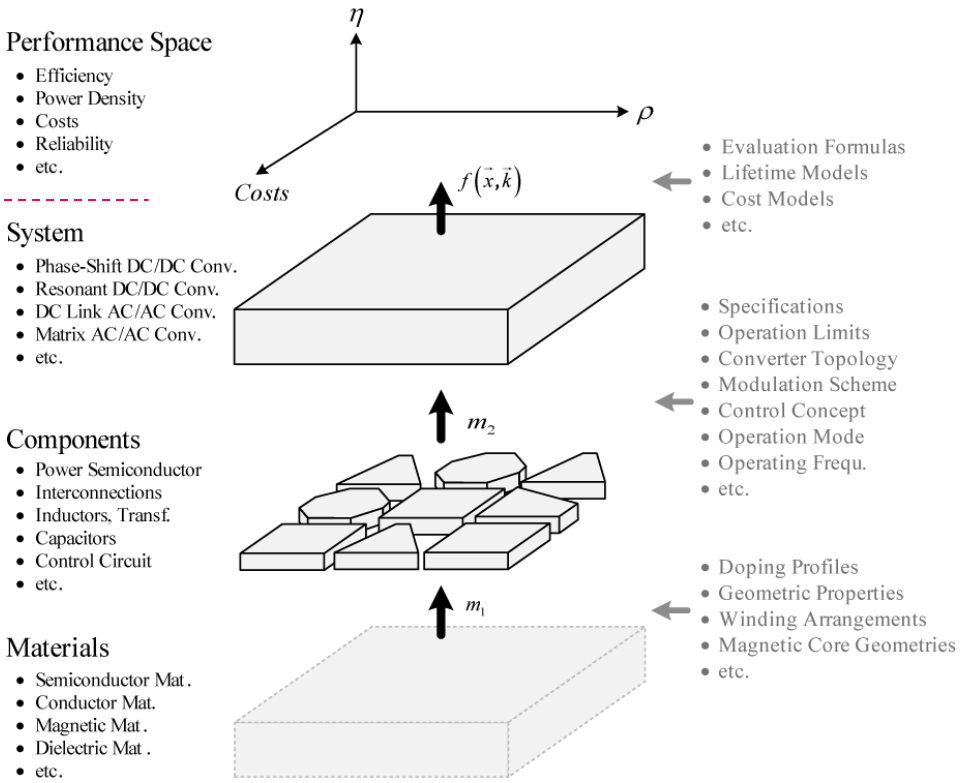
Basic Multi-Objective Optimization Approach

Abstraction of Converter Design
Component / System Modeling
Design / Performance Space
Pareto Front

Abstraction of Power Converter Design

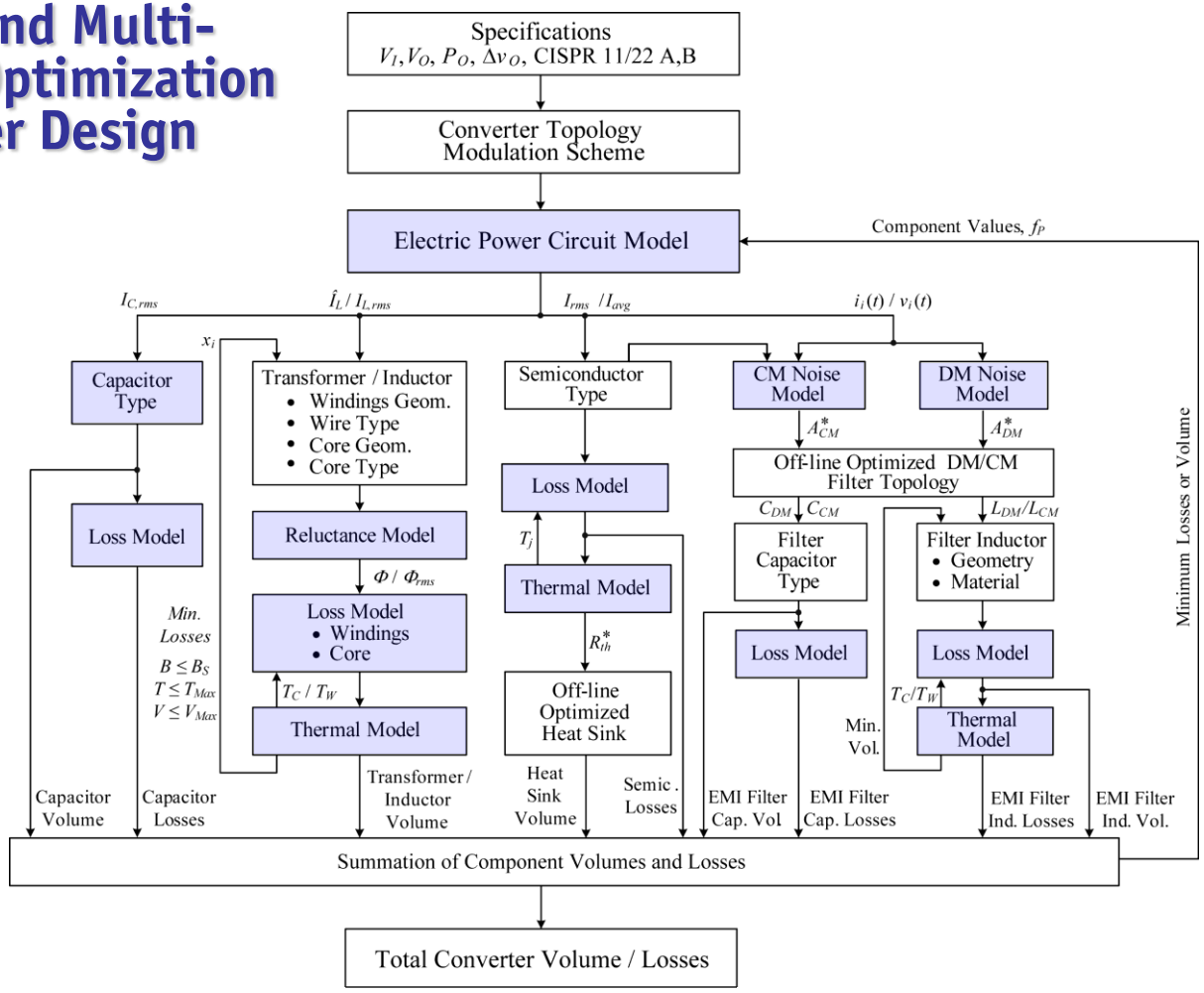
Performance Space

Design Space



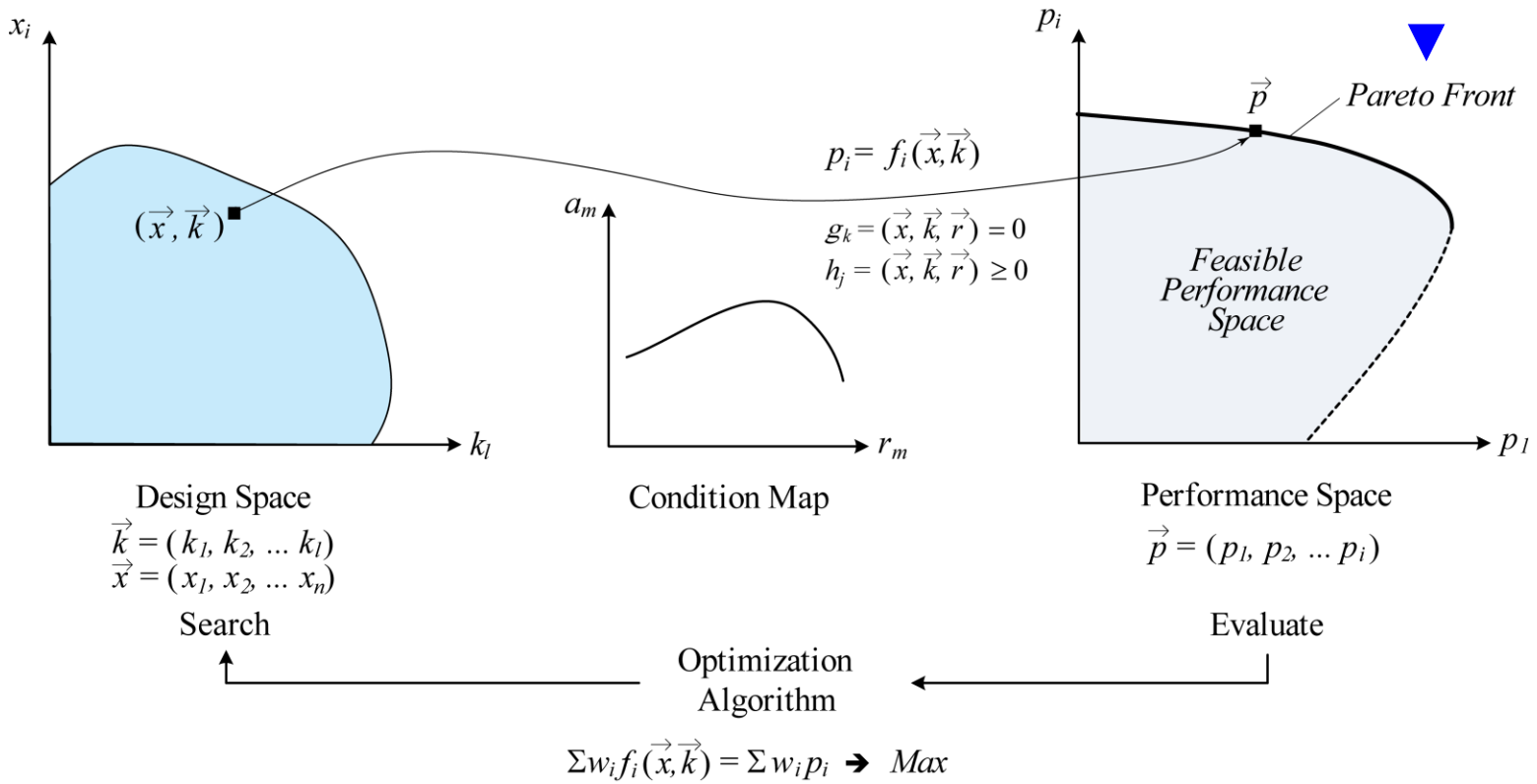
- Mapping of *Design Space* into System *Performance Space*

Modeling and Multi-Objective Optimization of Converter Design



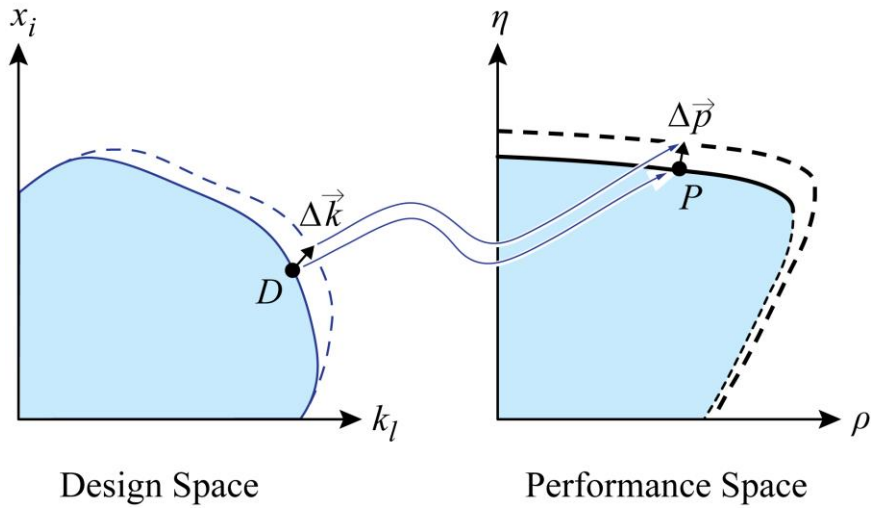
Multi-Objective Converter Design Optimization

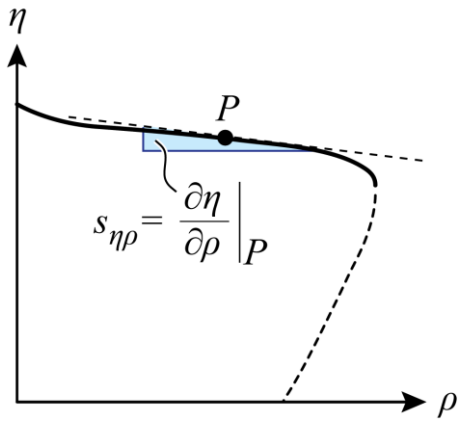
- *Pareto Front* - **Limit of Feasible Performance Space**



Technology Sensitivity Analysis Based on η-ρ-Pareto Front

- Sensitivity to Technology Advancements
- Trade-off Analysis





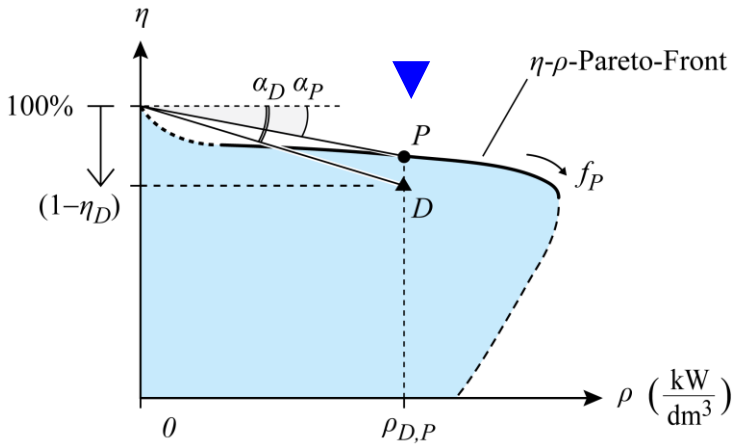
Converter Performance Evaluation Based on η-ρ-Pareto Front

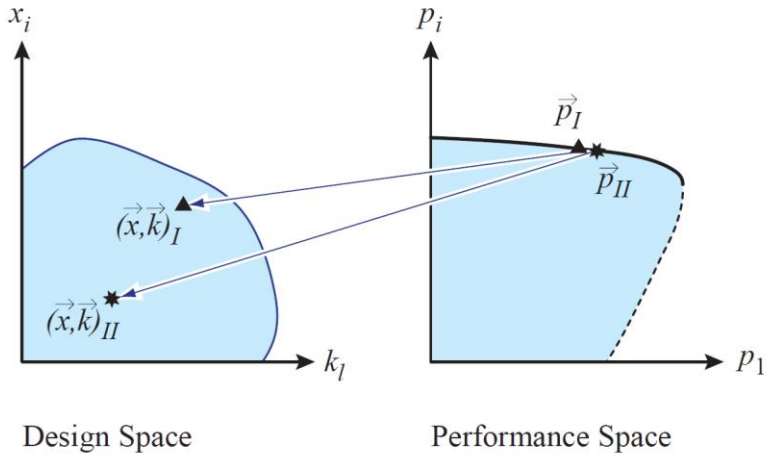
Performance Indicator

$$\tan\alpha_D = \frac{1-\eta_D}{\rho_D}$$

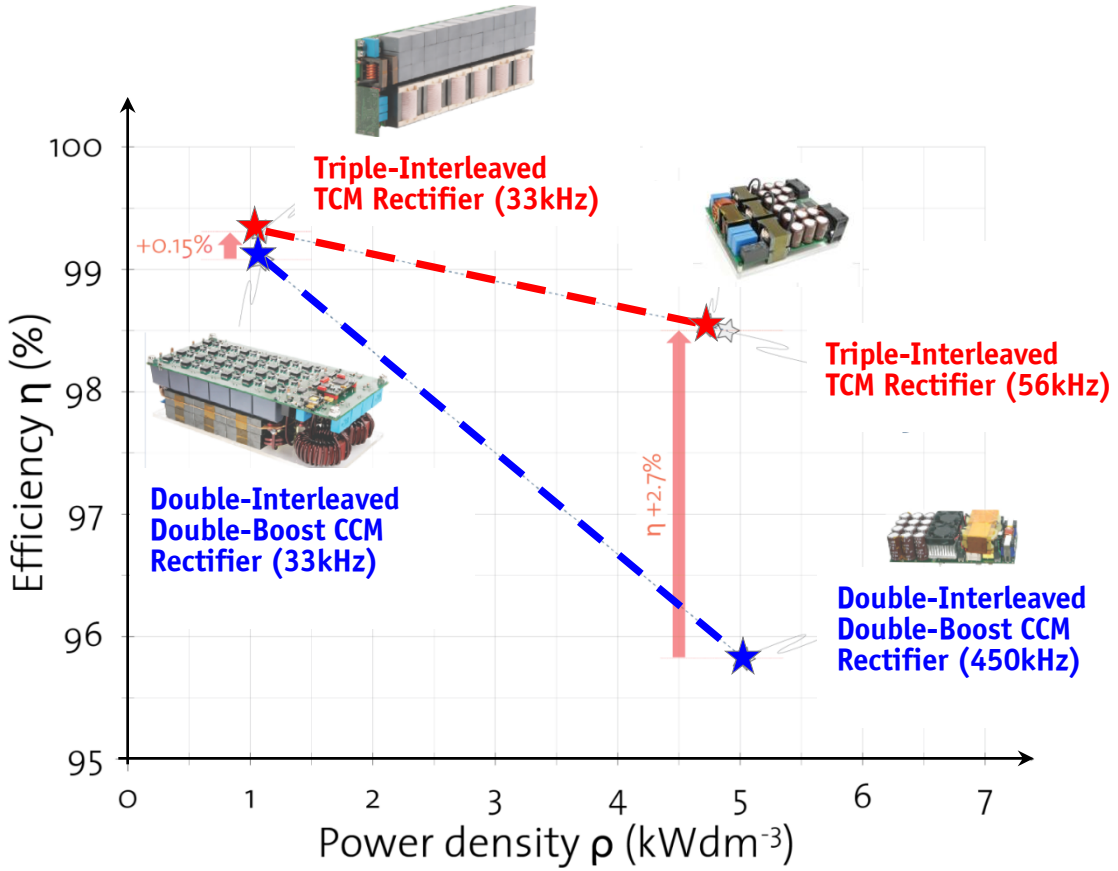
Design Space Diversity

Design Variables & Constraints Related to Two Adjacent Points of the Pareto Front





Converter Performance Evaluation Based on η-ρ-Pareto Front



3D-Performance Space Including Costs

▶ Industry Perspective

- Priorities

1. Costs
2. Costs
3. Costs
4. Robustness
5. Power Density
6. Efficiency ..... + Modularity / Scalability / Ease of Integration into Systems / etc.

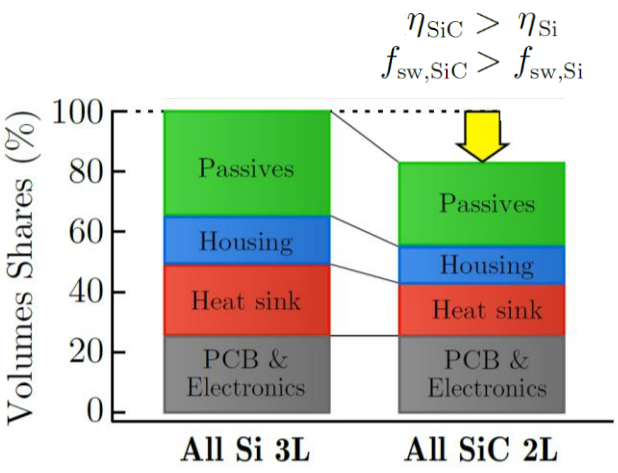
— Basic Discrepancy (!)

* Most Important Industry Figure "Unknown" to Univ.
* Costs Not Considered in Applic.-Oriented Research

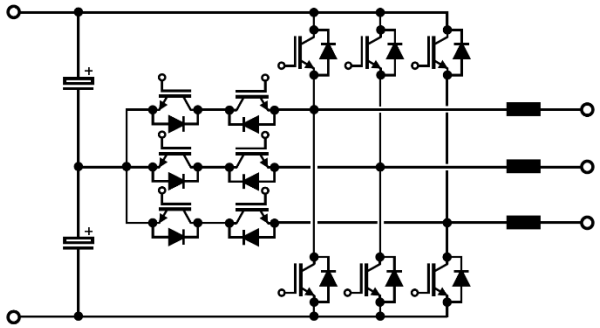
Requirement for Quantitative Cost Models

- **Advantages / Competitiveness of SiC Can Only be Revealed Considering Full System Costs**

  - Considering Only Volumes is Insufficient
  - Initial / Manufacturing Costs
  - Life Cycle Costs
  - Complexity / Reliability
  - Functionality

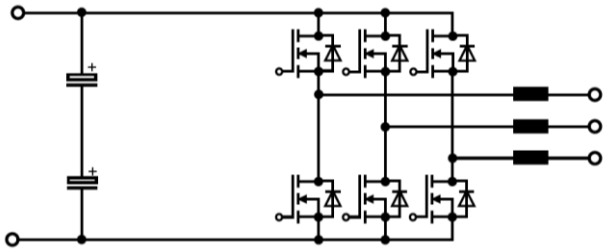


State-of-the-Art
→ Si IGBTs



All Si 3L

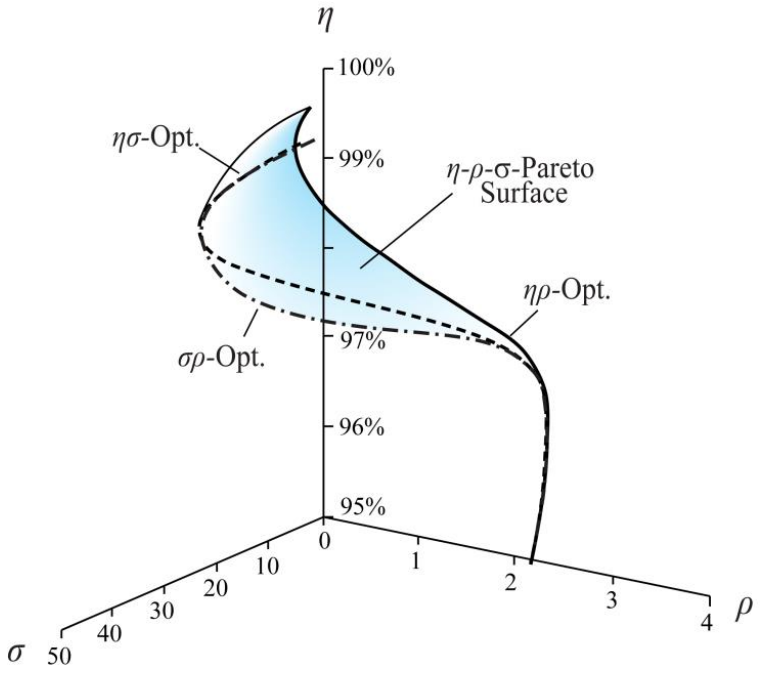
Advanced
→ SiC MOSFETs

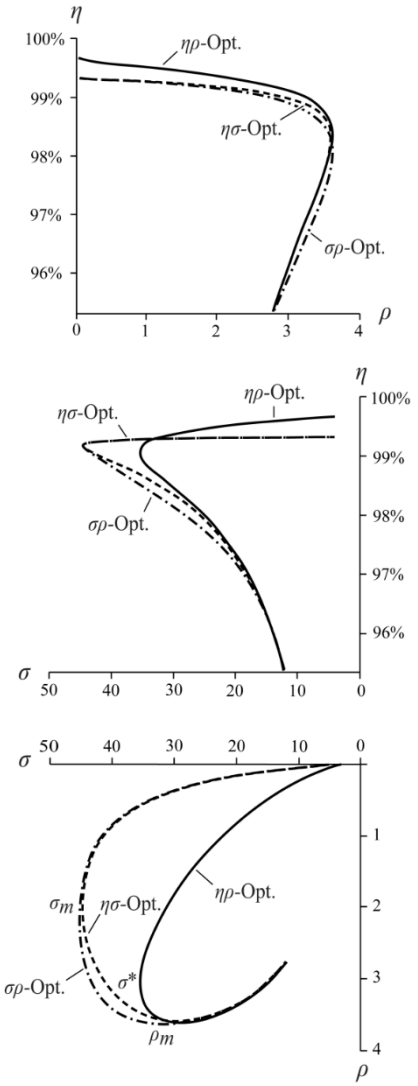


All SiC 2L

Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

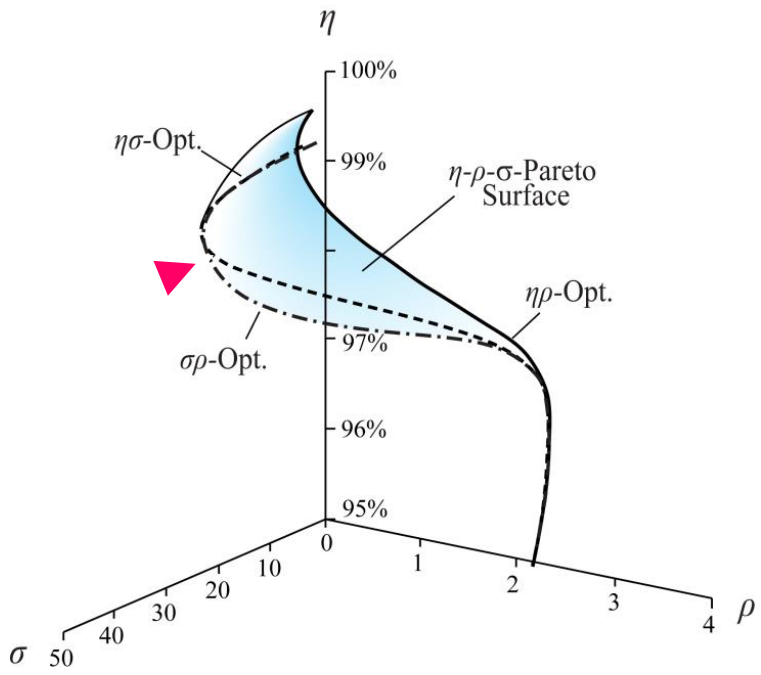
- σ: kW/$

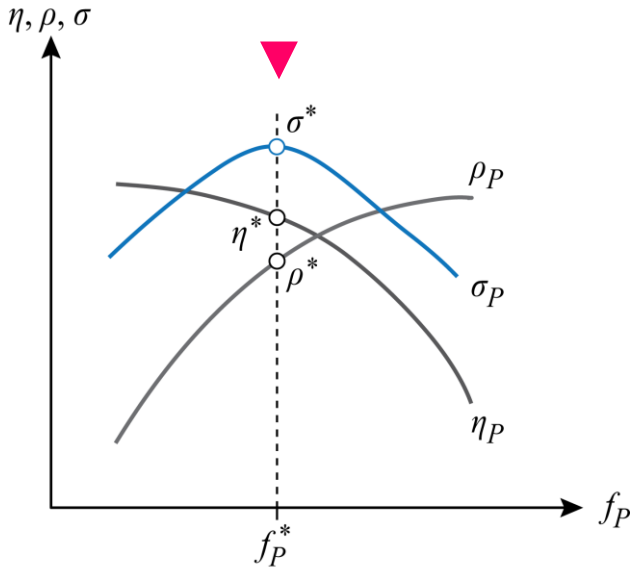




Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- Maximum σ [kW/$], Related Efficiency and Power Density
- Definition of *"Technology Node"* → $(\eta^*,\rho^*,\sigma^*,f_P^*)$





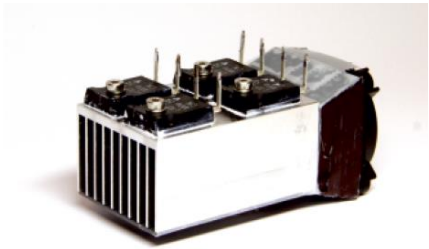
Modeling of Components

Efficiency
Power Density
Costs 

Power Semiconductors and Cooling Systems

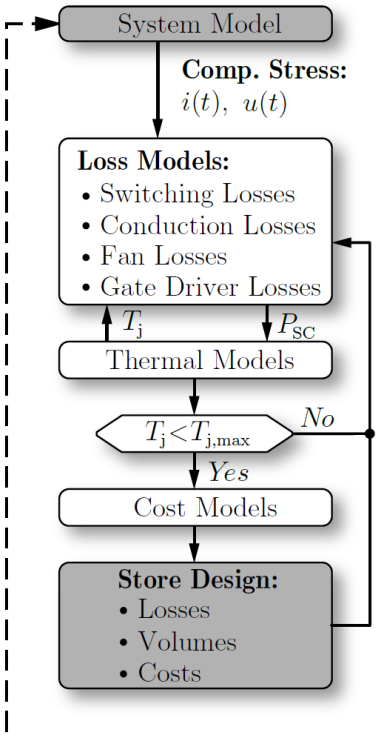
* *Cond./Switching Loss Models*
* *Thermal Models*
* *Cost Models* →

Modeling Tasks and Design Variables



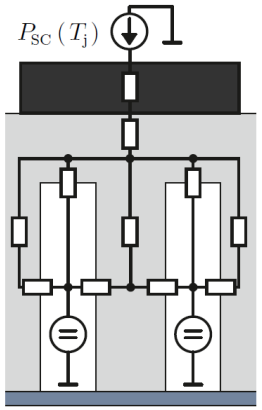
Design Routine

System Design Variables:
- f_{sw}
- Component Values L, C
- Modulation Scheme

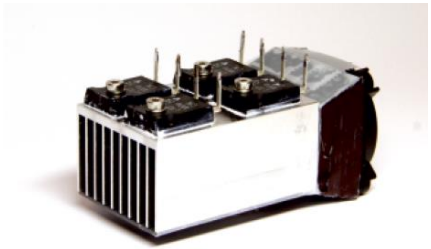


Component Design Variables:
- Semiconductor Type
- # parallel / A_{chip}
- Cooling System /$R_{th,hsa}$
  - Sink Dimensions
  - Sink Material
  - Fan Type
  - # Fans

Thermal Model



Conduction Losses

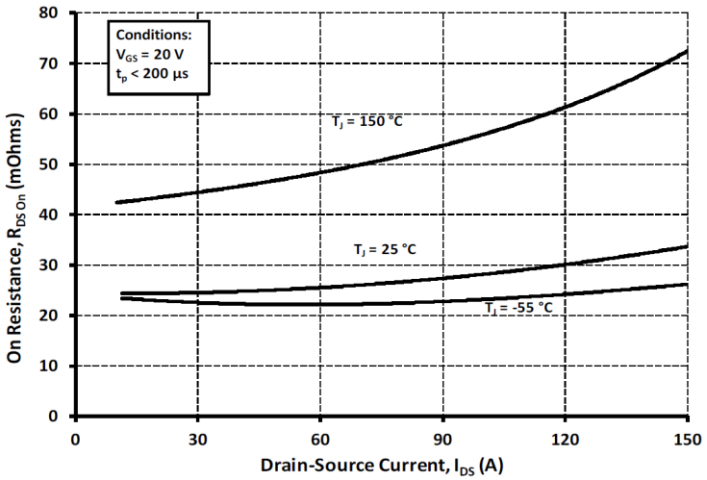


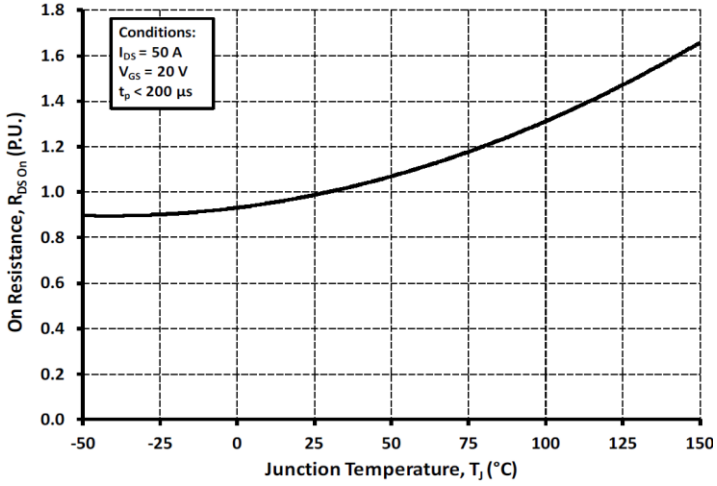
MOSFET Conduction Losses

$$P_{\text{cond}}(i(t), T_{\text{j}}) = R_{\text{ds,on}}(i(t), T_{\text{j}}) \cdot i(t)^2$$

Take from Data Sheet

Source: CREE





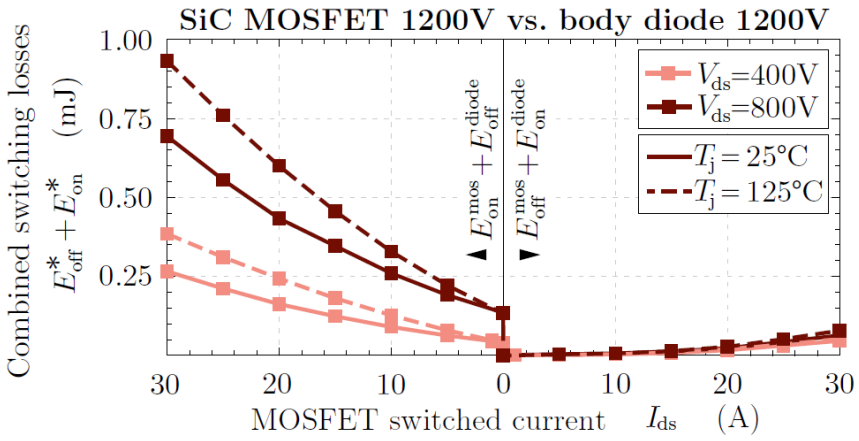
Switching Losses

MOSFET Switching Losses

$$P_{\mathrm{sw}} = \frac{1}{T}\sum_i \left[E_{\mathrm{on}}\left(I_{\mathrm{on},i}, V_{\mathrm{on},i}, T_{\mathrm{j}}\right) + E_{\mathrm{off}}\left(I_{\mathrm{off},i}, V_{\mathrm{off},i}, T_{\mathrm{j}}\right) \right]$$

Layout-Dependent / Measurements Required

Measurement Results

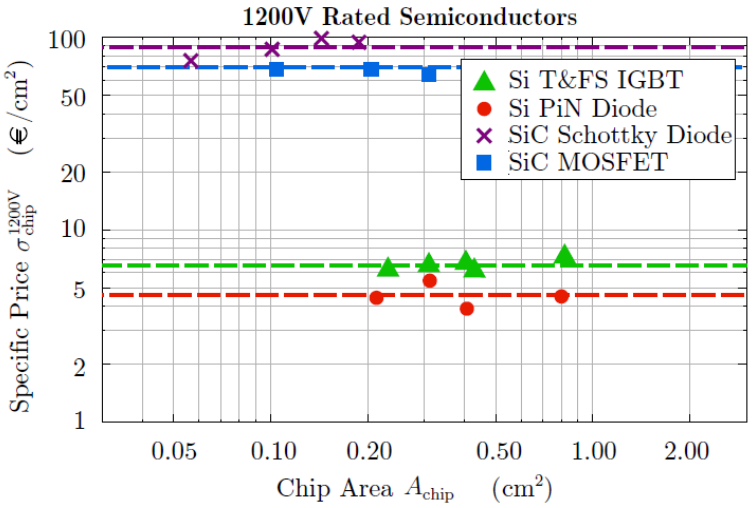


Semiconductor Costs

- **Source of Cost Data**
  - Distributors
  - Better: Manufacturer Data @ MOQ = const.
- **Cost Model**

$$\Sigma_{SC} = \Sigma_{pack} + \sigma_{chip} \cdot A_{chip}$$

  - Parameters Based on Fitted Data
  - Inter-/Extrapolation of Semiconductor Costs

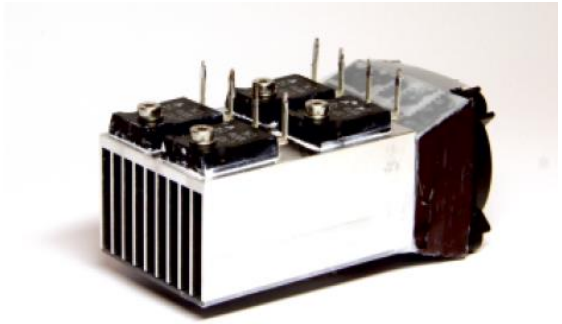


Fitted Manufacturer Data for MOQ = 50k

Chip technology:	Si T&FS IGBT	Si PiN diode	Si CoolMos CS7	SiC Schottky diode	SiC MOSFET
$\sigma_{chip,\infty}^{600V}$ (€/cm²)	5.52	2.46	30.27	46.24	61.14
$\sigma_{chip,\infty}^{1200V}$ (€/cm²)	6.57	4.46		86.47	72.01
Package type:	**TO-247-3**	**SOT-227**	**Module (23.2 cm²)**	**Module (29.9 cm²)**	**Module (37.6 cm²)**
$\Sigma_{pack,\infty}$ (€/unit)	0.55	8.10	7.62	10.01	15.06

MOQ ... Minimum Order Quantity

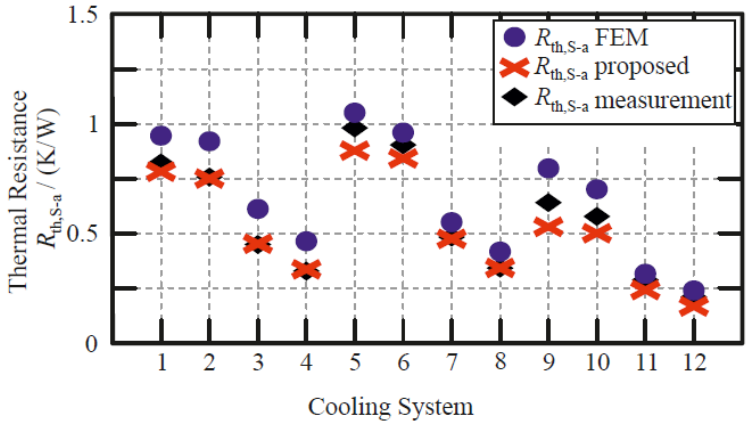
Cooling System Modeling



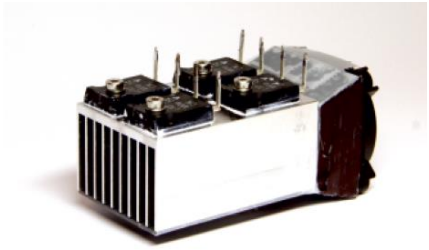
- Geometry, Fans
  - Heat Sink Dimensions
  - Heat Sink Material
  - Fan Type
  - # of Fans

- Fluid Dynamics Models
- Thermodynamics Models

- Experimental Verification



Cooling System Costs



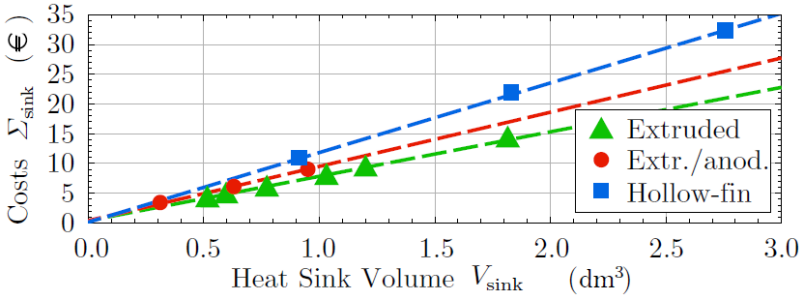
Fan Costs

- Distributors
- Better: Manufacturer Data @ MOQ = const.

Cost Model for Heat Sinks

$$\Sigma_{\text{sink}} = \Sigma_{\text{sink}}^{\text{fc}} + \sigma_{\text{sink}} \cdot V_{\text{sink}}$$

- Based on Fitted Manufacturer Data



- Fitted Manufacturer Data for MOQ = 10k

Heatsink type:	Extruded	Extruded/ anodized	Hollow-fin
$\sigma_{\text{sink},\infty}$ (€/dm³)	7.69	9.30	11.94
$\Sigma^{\text{fc}}_{\text{sink},\infty}$ (€/unit)	0.23	0.25	0.17

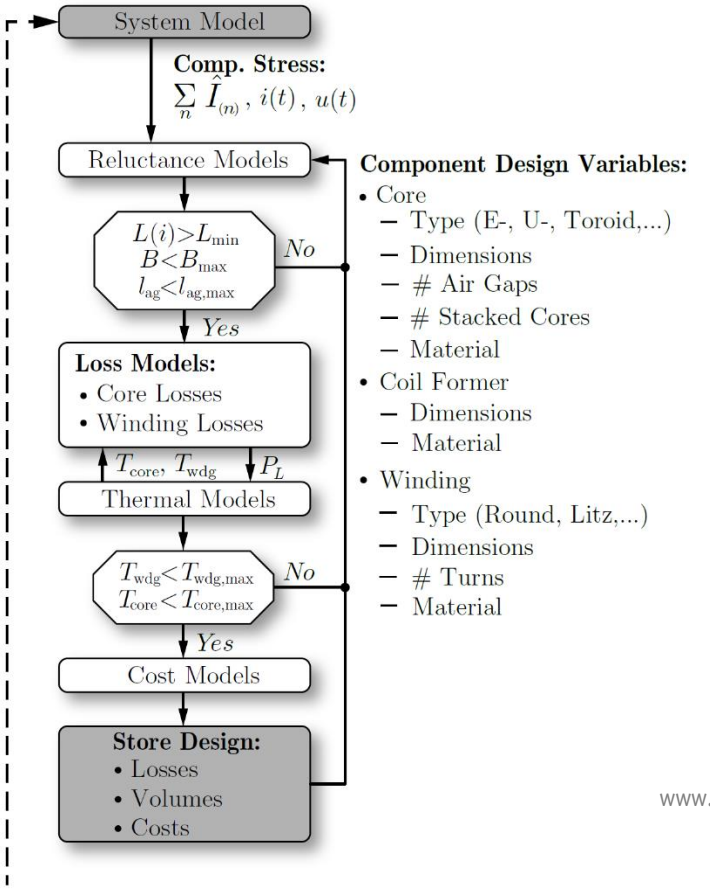
Magnetic Components

* Core/Winding Loss Models
* Reluctance Models
* Thermal Models
* Cost Models

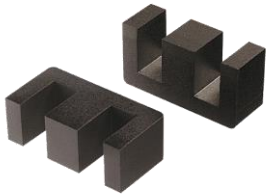
Modeling Tasks and Design Variables

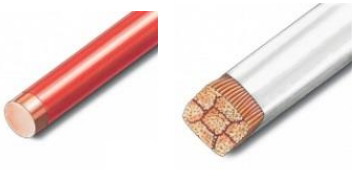
Design Routine

System Design Variables:
- f_{sw}
- Component Values L, C
- Modulation Scheme



Component Design Variables:
- Core
  - Type (E-, U-, Toroid,...)
  - Dimensions
  - # Air Gaps
  - # Stacked Cores
  - Material
- Coil Former
  - Dimensions
  - Material
- Winding
  - Type (Round, Litz,...)
  - Dimensions
  - # Turns
  - Material





www.pack-feindraehte.de
www.jiricek.de

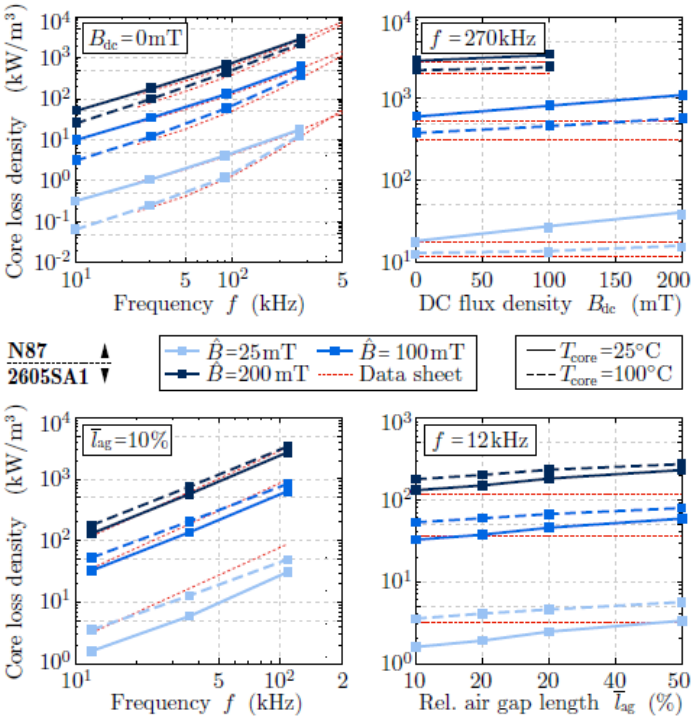
Core Losses

- Improved² Steinmetz Equation

$$P_{\text{core}} = V_{\text{core}} \cdot \frac{1}{T} \cdot \sum_i k_i \, \Delta T_i^{1-\alpha_i} \, |\Delta B_i|^{\beta_i}$$

- Improvement (1): Arbitrary Waveforms
- Improvement (2): Operating Point-Dependent Parameters

- Requires Extensive Measurements
- Sweeps: f, B_{ac}, B_{dc}, T_{core}, l_{ag}

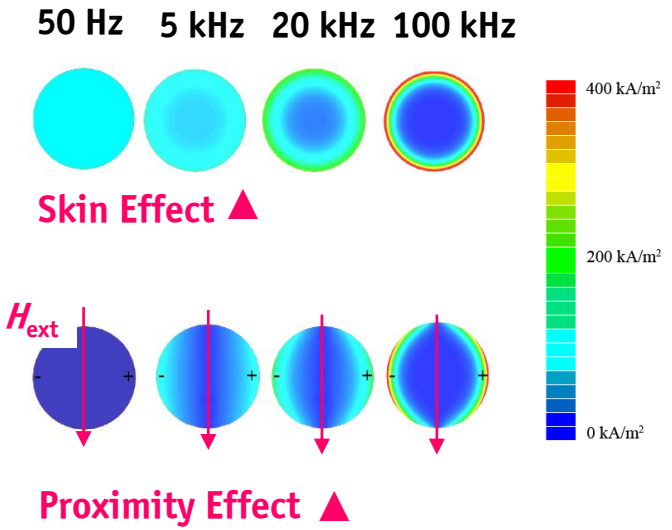


Winding Losses

Winding Losses

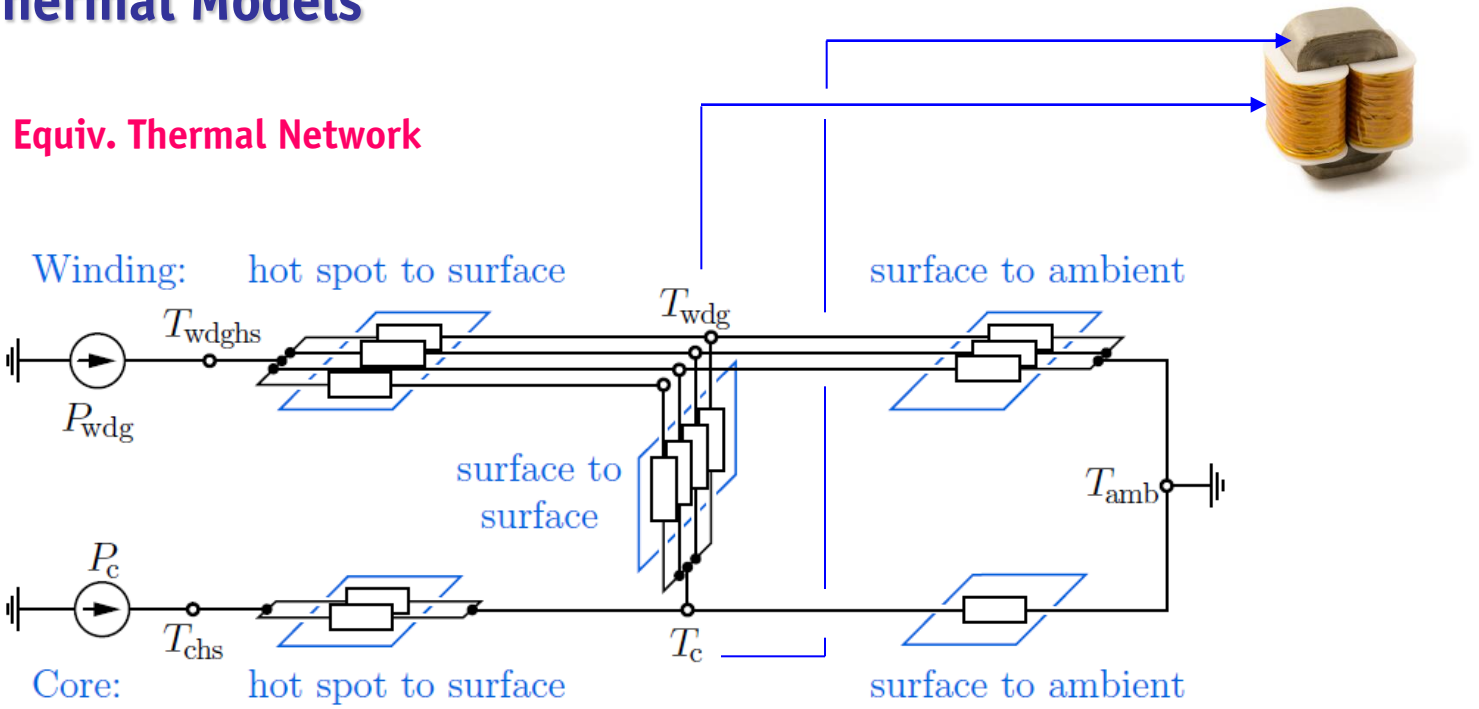
$$P_{\mathrm{wdg}} = R_{\mathrm{dc}}(T_{\mathrm{wdg}}) \cdot \sum_n \left\{ F_{\mathrm{skin}}(f_n, T_{\mathrm{wdg}}) + G_{\mathrm{prox}}(f_n, T_{\mathrm{wdg}}) \cdot \overline{H}^2_{\mathrm{ext},(n)} \right\} \cdot \hat{I}^2_{(n)}$$

- Skin and Proximity Effects Contribute to Winding Losses
- Frequency-, Temperature- and Geometry-Dependency
- Analytical Formulas for F_{skin}, G_{prox} and H_{ext} Available



Thermal Models

3D Equiv. Thermal Network



Significance

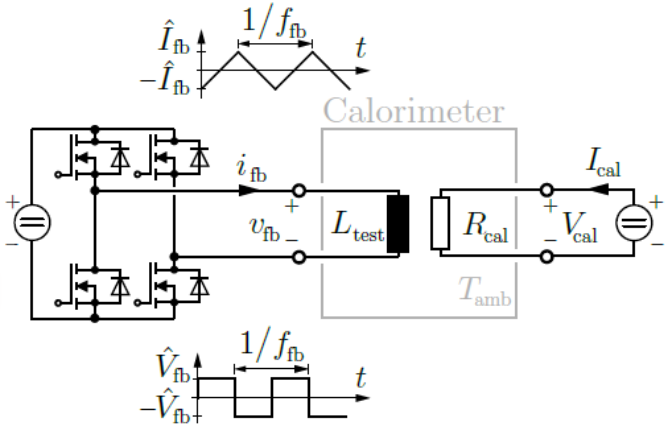
- Avoid Overheating
- Improve Loss Calculation

Heat Transfer Mechanisms

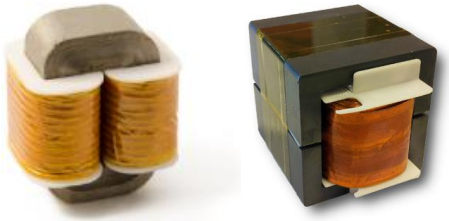
- Conduction
- Radiation
- Natural Convection

Verification of Multi-Physics Models

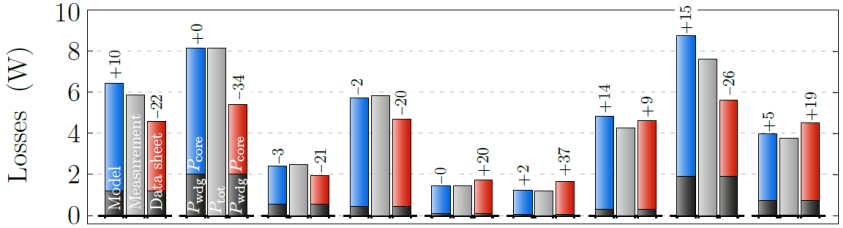
Setup



Test Inductors

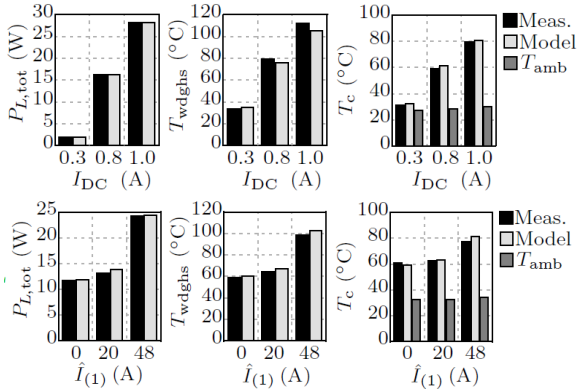


Loss Model Verification



$\hat{B}$ (mT)	150	270	80	93	45	35	140	120	60
f (kHz)	10	5	12	20	25	3	12	15	35
l_{ag} (%)	20	20	30	20	20	20	10	30	20
T_{core}(°C)	55	87	82	50	37	32	48	110	64

Thermal Model Verification



Magnetics Costs

Model

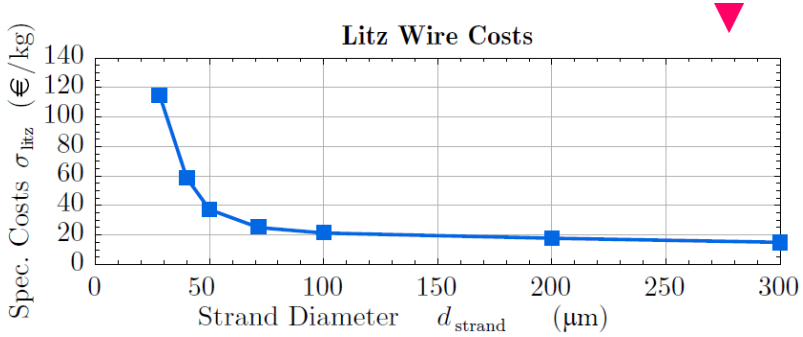
$$\Sigma_L = \frac{1}{GM}\left(\Sigma_{\text{core}} + \Sigma_{\text{wdg}} + \Sigma_{\text{lab}}\right)$$

$$\Sigma_{\text{core}} = N_{\text{stack}} \cdot \Sigma_{\text{core}}^{\text{fc}} + \sigma_{\text{core}} W_{\text{core}}$$

$$\Sigma_{\text{wdg}} = \Sigma_{\text{wdg}}^{\text{fc}} + \sigma_{\text{wdg}} W_{\text{wdg}}$$

$$\Sigma_{\text{lab}} = \Sigma_{\text{lab}}^{\text{fc}} + \sigma_{\text{lab}} W_{\text{wdg}}$$

Example: Manufact. Data for Litz Wire for MOQ = 1 Metric Ton



Source of Data

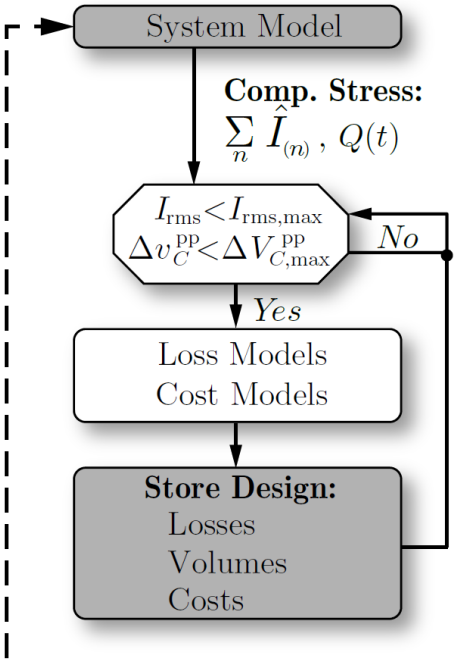
- Core Manufacturers
- Conductor Manufacturers
- Suppliers of Magn. Components

Capacitors

* Loss Models
* Cost Models

Modeling Tasks & Design Variables

System Design Variables:
- f_{sw}
- Component Values L, C
- Modulation Scheme



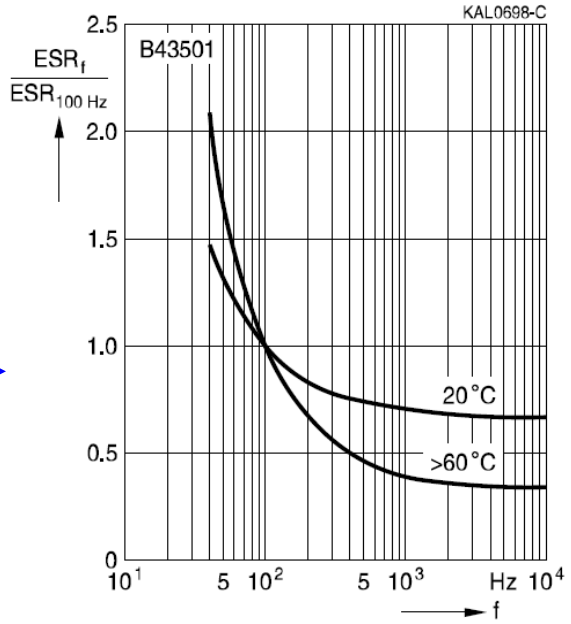
Component Design Variables:
- Capacitor Type (Film, Electrolytic,...)
- Rated Capacitance
- Rated Voltage
- # Parallel
- # Serial

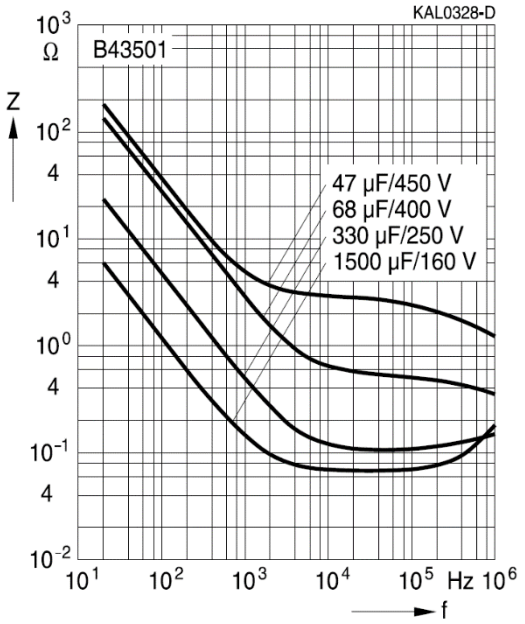
Capacitor Losses

Electrolytic Capacitor Losses

$$P_C = \sum_n ESR(f_{(n)}, T_{\text{amb}}) \cdot \frac{1}{2}\hat{I}^2_{(n)}$$

— Take from Data Sheet





Capacitor Costs

Cost Models

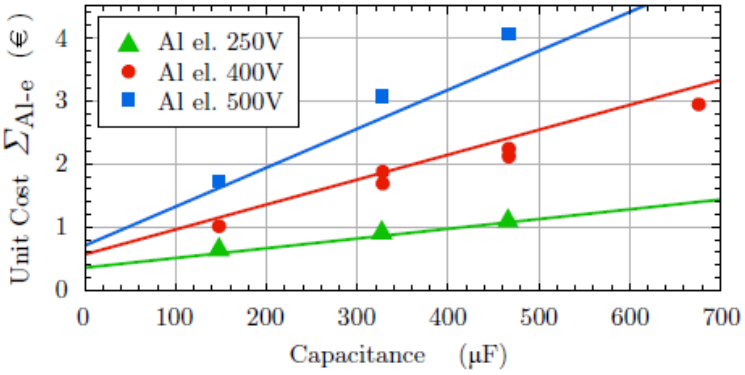
$$\Sigma_{\text{Al-e}} = b_{\text{Al-e}} V_{\text{r}} + c_{\text{Al-e}} C_{\text{r}} V_{\text{r}}^2$$
$$\Sigma_{\text{film}} = a_{\text{film}} + b_{\text{film}} V_{\text{r}} + c_{\text{film}} C_{\text{r}}$$

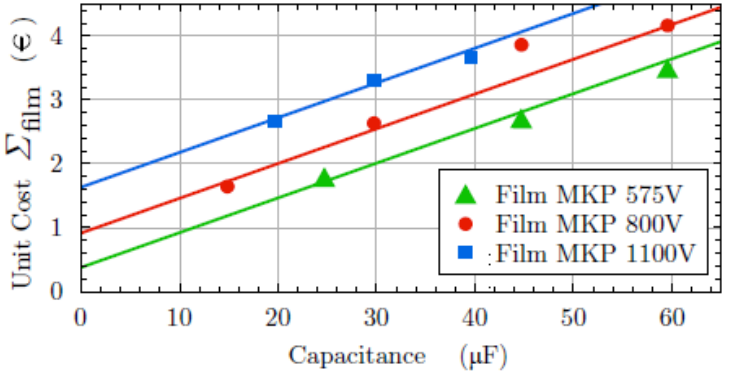
— Parameters Based on Fitted Data

Source of Cost Data

— Distributors
— Better: Manufact. Data @ MOQ = const.

Fitted Manufact. Data for MOQ = 50k



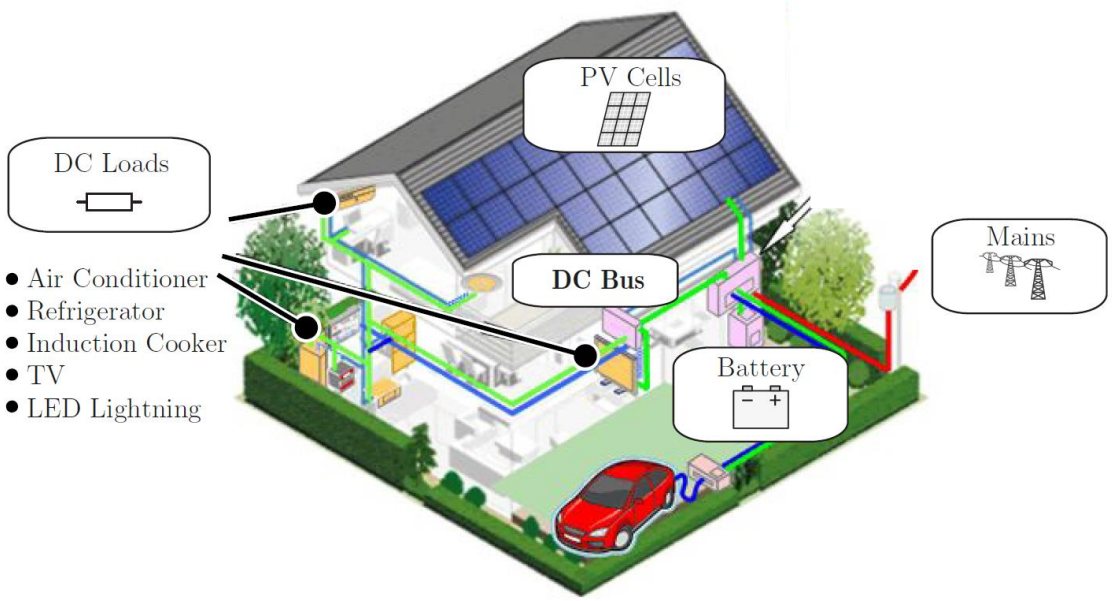


Converter Optimization Example I

Isolated DC/DC Converter
Topologies/Modulation Schemes
Materials/Components
Optimization
η-ρ-σ-Pareto Surface
Hardware Prototype →

Application

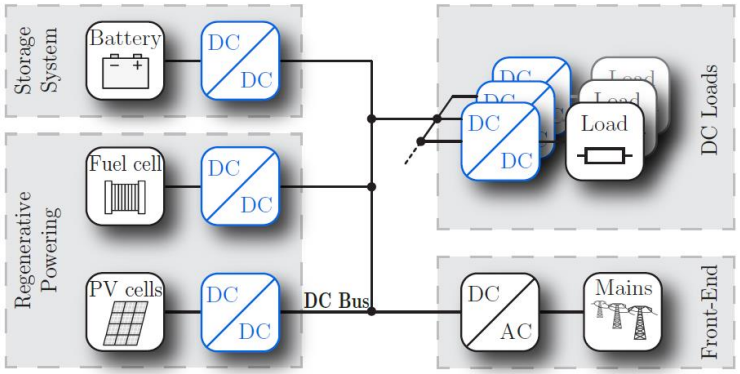
Next Generation Residential Energy Management System



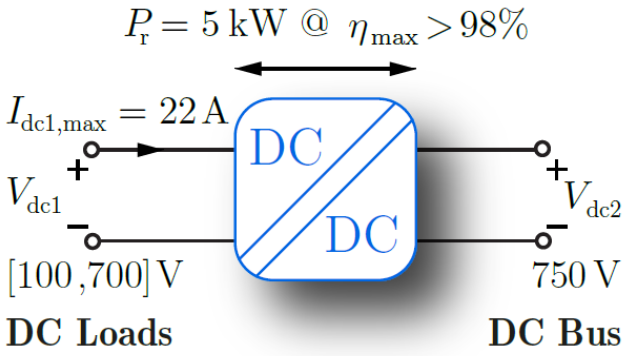
- Renewable Energy Sources, Local Storage Systems
- DC Distribution Bus
- Intelligent Load Management Algorithm
- Possible Element of Future Smart Grid System
- DC Microgrids Already Employed in Data Centers, Ships, Airplanes

Bidirectional Wide Input Voltage Range Isolated DC/DC Converter

Structure of DC Microgrid



Universal DC/DC Converter



Universal DC/DC Converter

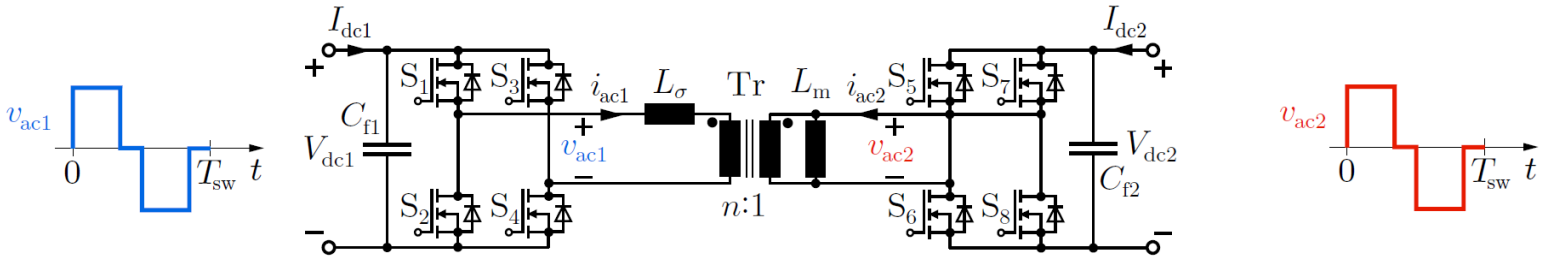
- Bidirectional Power Flow
- Galvanic Isolation
- Wide Voltage Range
- High Partial Load Efficiency

Advantages

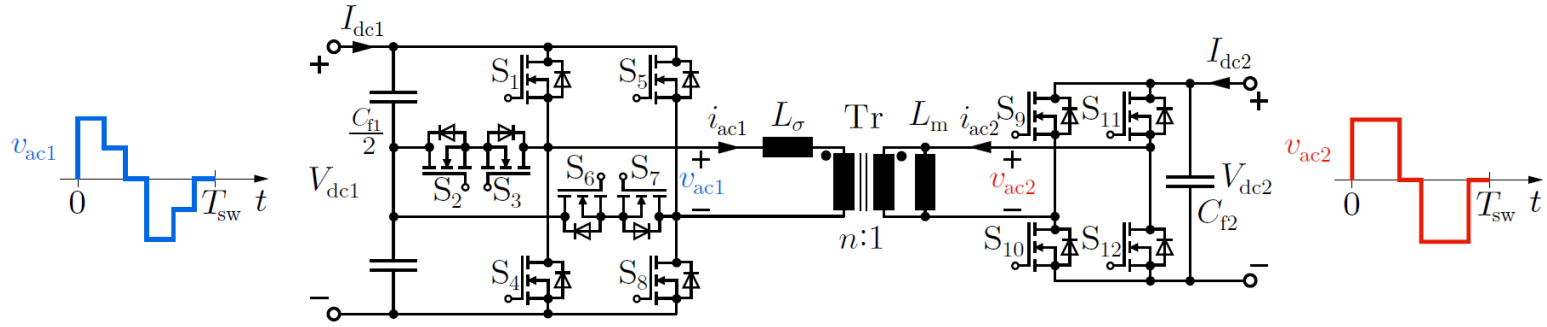
- Reduced System Complexity
- Lower Overall Development Costs
- Economies of Scale

Converter Topologies

Conv. 3-Level Dual Active Bridge (3L-DAB)

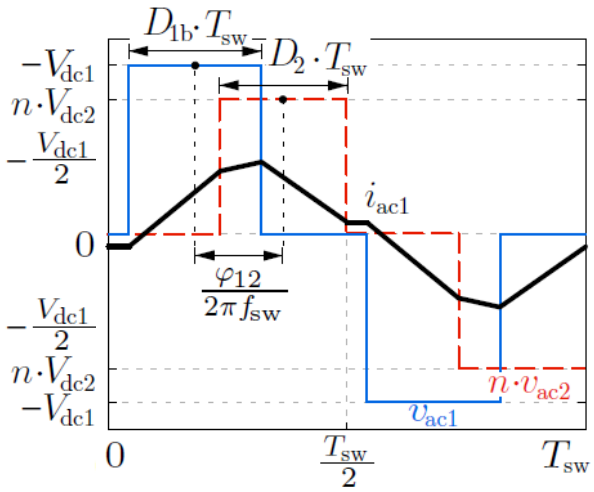


Advanced 5-Level Dual Active Bridge (5L-DAB)



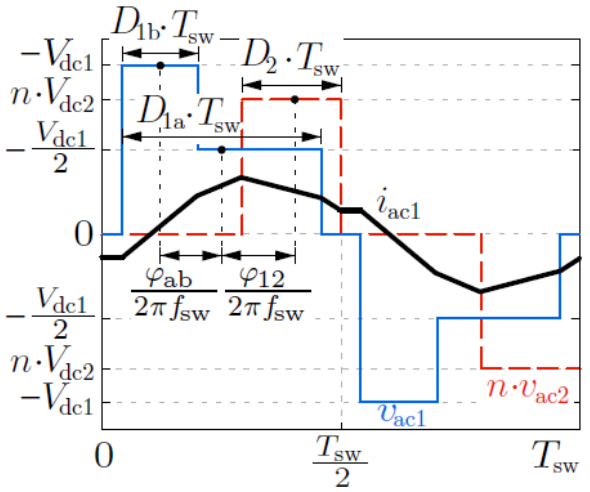
Modulation Schemes

3-Level Dual Active Bridge



$$\vec{\Xi}_{3\mathrm{LDAB}} = (D_{1b}, D_{1b}, D_2, \ 0 \ , \varphi_{12})^\top$$

5-Level Dual Active Bridge



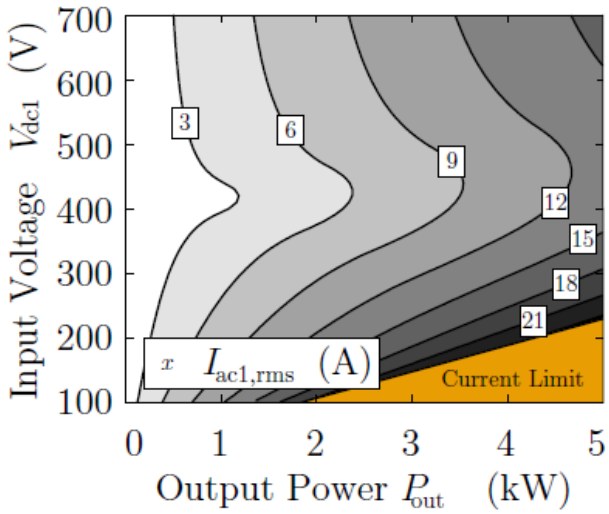
$$\vec{\Xi}_{5\mathrm{LDAB}} = (D_{1a}, D_{1b}, D_2, \varphi_{ab}, \varphi_{12})^\top$$

$$\vec{\Xi}^* = \arg\min_{\vec{\Xi}} \ I_{\mathrm{ac1,rms}}(n^*, L_\sigma^*, \vec{\Lambda}^*, \vec{\Xi})$$
$$\text{with} \quad \vec{\Lambda}^* = (V_{\mathrm{dc1}}^*, V_{\mathrm{dc2}}^*, P_{\mathrm{out}}^*)^\top$$

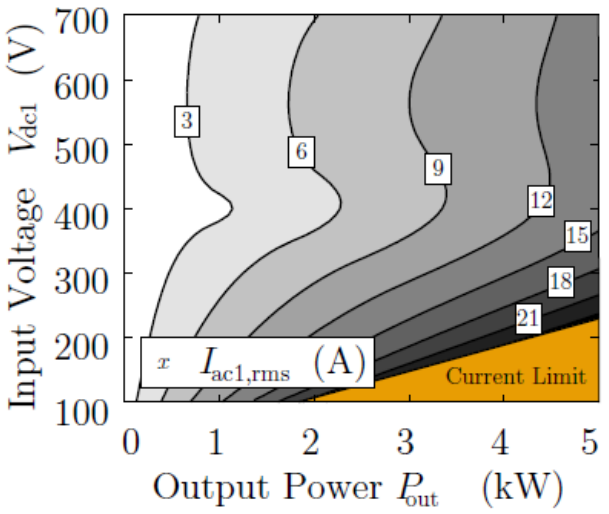
— Choose Control Parameters $\vec{\Xi}$ so as to Minimize Transformer RMS Current $I_{\mathrm{ac1,rms}}$

Modulation Schemes

- 3-Level Dual Active Bridge

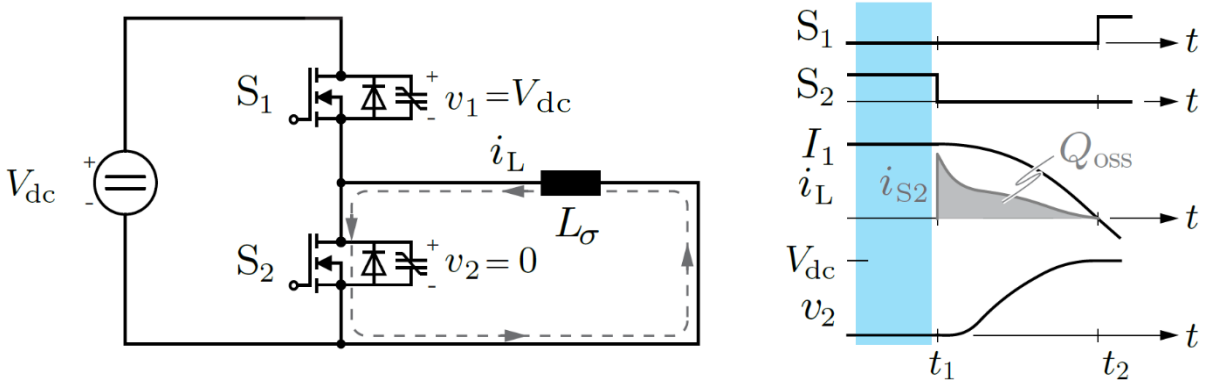


- 5-Level Dual Active Bridge



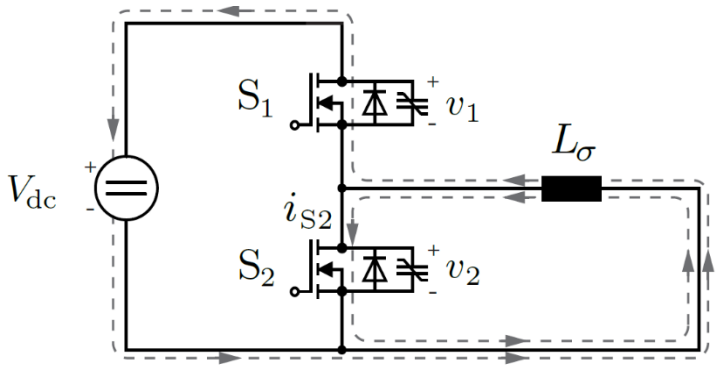
— Significantly Lower RMS Currents of 5L-DAB Due to Higher DOF of Modulation

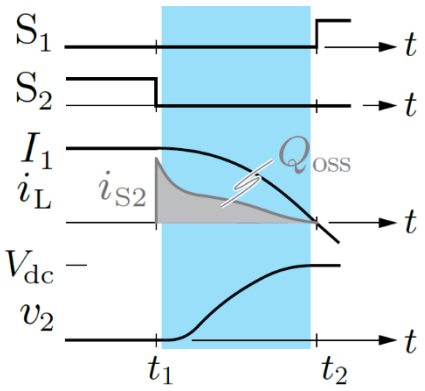
Modulation Schemes - Zero Voltage Switching (1)



- $W_{t1} = E_{oss}(V_{dc}) + \frac{1}{2} L_\sigma I_1^2$

Modulation Schemes - Zero Voltage Switching (2)



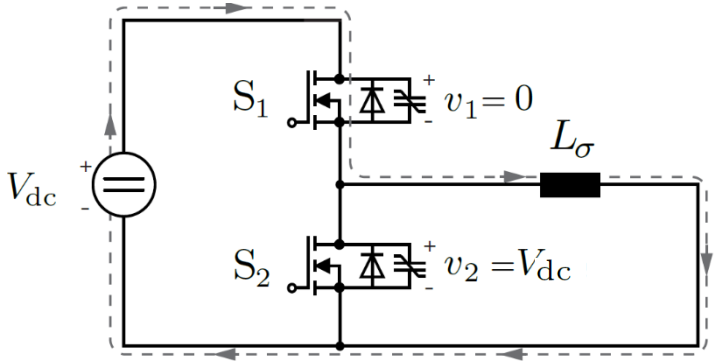


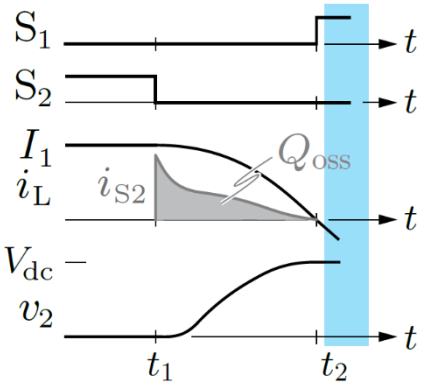
- $W_{t1} = E_{\mathrm{oss}}(V_{\mathrm{dc}}) + \frac{1}{2} L_\sigma I_1^2$

$i_L(t_2) = 0$

- $W_{t2} = E_{\mathrm{oss}}(V_{\mathrm{dc}}) + Q_{\mathrm{oss}}(V_{\mathrm{dc}}) \cdot V_{\mathrm{dc}}$

Modulation Schemes - Zero Voltage Switching (3)





$i_L(t_2) = 0$

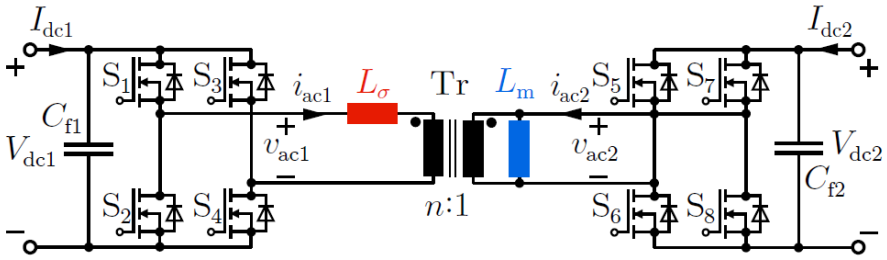
- $W_{t1} = E_{\mathrm{oss}}(V_{\mathrm{dc}}) + \frac{1}{2} L_\sigma I_1^2$
- $W_{t2} = E_{\mathrm{oss}}(V_{\mathrm{dc}}) + Q_{\mathrm{oss}}(V_{\mathrm{dc}}) \cdot V_{\mathrm{dc}}$
- $\frac{1}{2} L_\sigma I_1^2 \geq Q_{\mathrm{oss}}(V_{\mathrm{dc}}) \cdot V_{\mathrm{dc}}$

Modulation Schemes - Zero Voltage Switching (4)

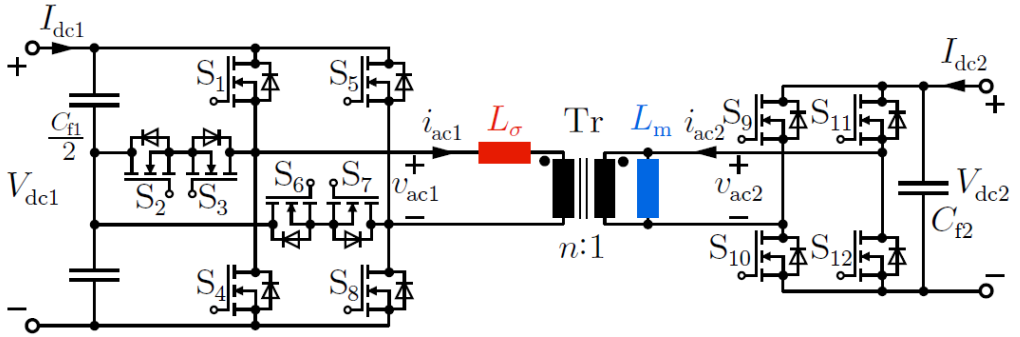
Achieving ZVS

- L_σ Usually Provides Not Enough Charge
- Add L_m for Additional (Reactive) Current
- At Low Power and/or Too Short Dead Time Intervals Still not Sufficient → Partial ZVS / Add. Switching Losses

3-Level Dual Active Bridge



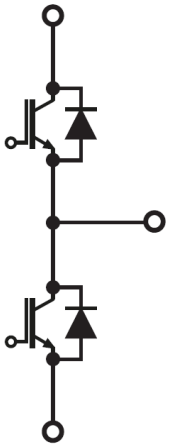
5-Level Dual Active Bridge



Components and Materials

Power Semiconductors

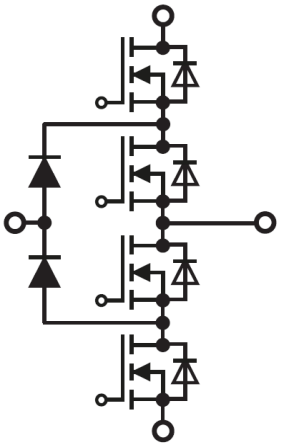
Si IGBT



- Inexpensive
- 1200 V

- Cond. Losses Not Scalable
- No ZVS Possible
- Tail Currents
- ZCS Difficult to Achieve

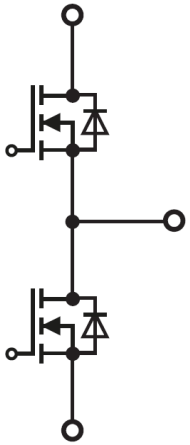
Si SJ MOSFET



- Conduction Losses Scalable
- ZVS But Non-Zero Sw. Losses (!)

- Large Specific C_{oss}
- Only 650 V
- NPC Half-Bridge Necessary
- Increased Part Count

SiC VD-MOSFET



- Cond. Losses Scalable
- Very Low ZVS Losses
- 1200 V
- Low Specific C_{oss}

- Costs

Overview of Components and Materials

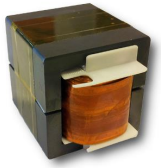
3-Level Dual Active Bridge

- CREE SiC MOSFET 80 mΩ 1200 V
- 2 x on Variable Voltage Side
- 1 x on Fixed Voltage Side

5-Level Dual Active Bridge

- CREE SiC MOSFET 80 mΩ 1200 V
- Scaled 600 V SiC Switch
- Variable Chip Sizes
- Same Total Semicond. Cost as 3L-DAB

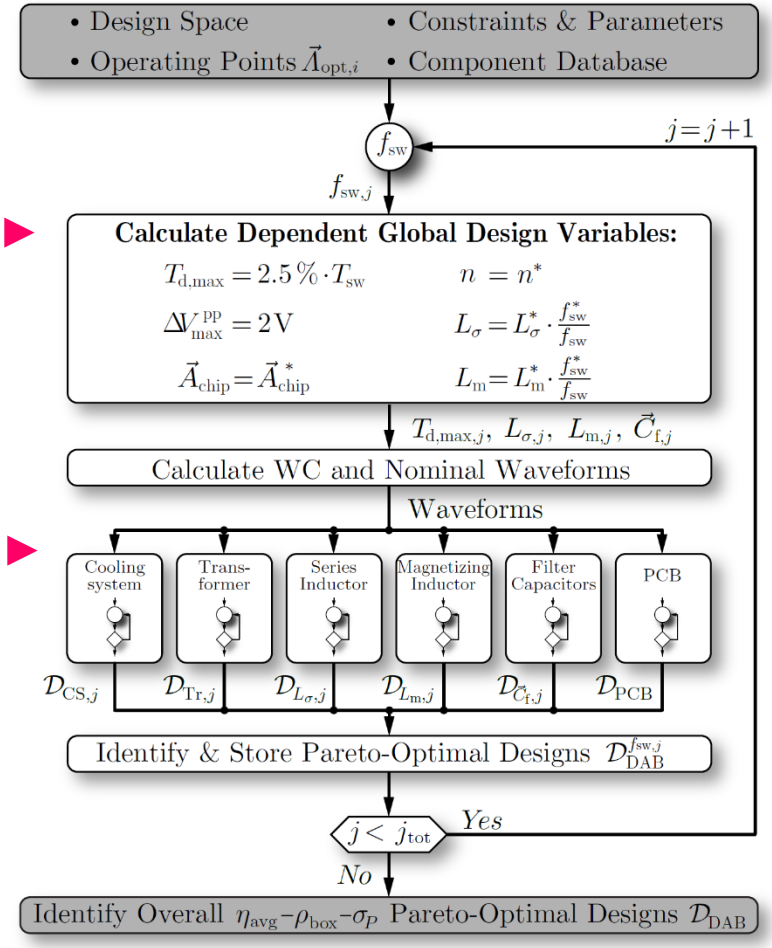
- Optimized Aluminum Heat Sinks
- Range of Low Power DC Fans



- EPCOS N87 Ferrite E & ELP Cores
- Litz Wire with Range of Strand Diameters

- EPCOS MKP DC Film Capacitors
- 575 V and 1100 V Rated

Global Optimization Routine (1)



Global System Optimization

Dependent Global Design Variables

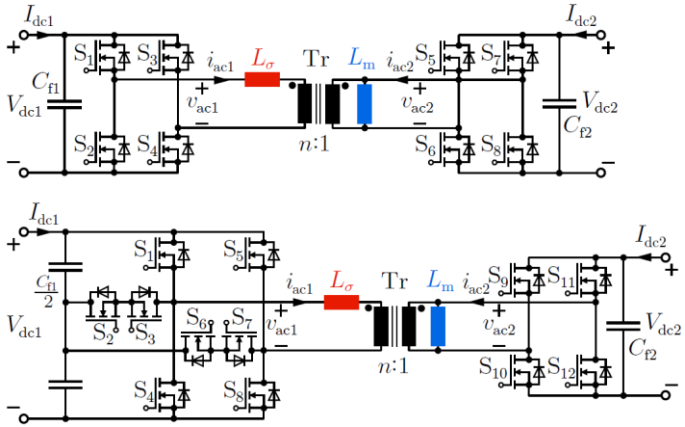
Local Component Optimization

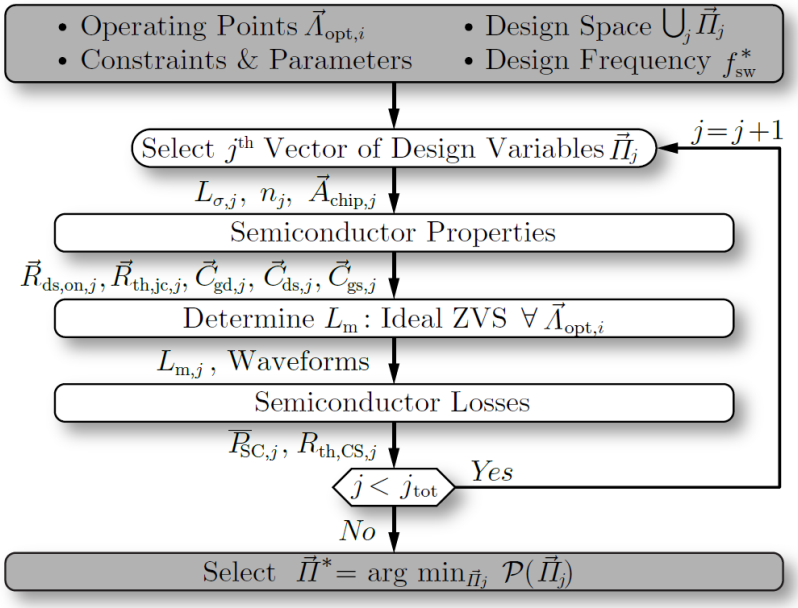
▶ Global Optimization Routine (2)

■ Offline Design Variable Optimization

— L_σ , L_m and n Determine Waveforms
— Optimize with Chip Area Distribution

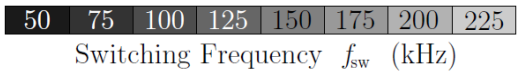
▶ Minimum Semiconductor Losses
▶ ZVS for All Operating Points
▶ Design Frequency: 50 kHz

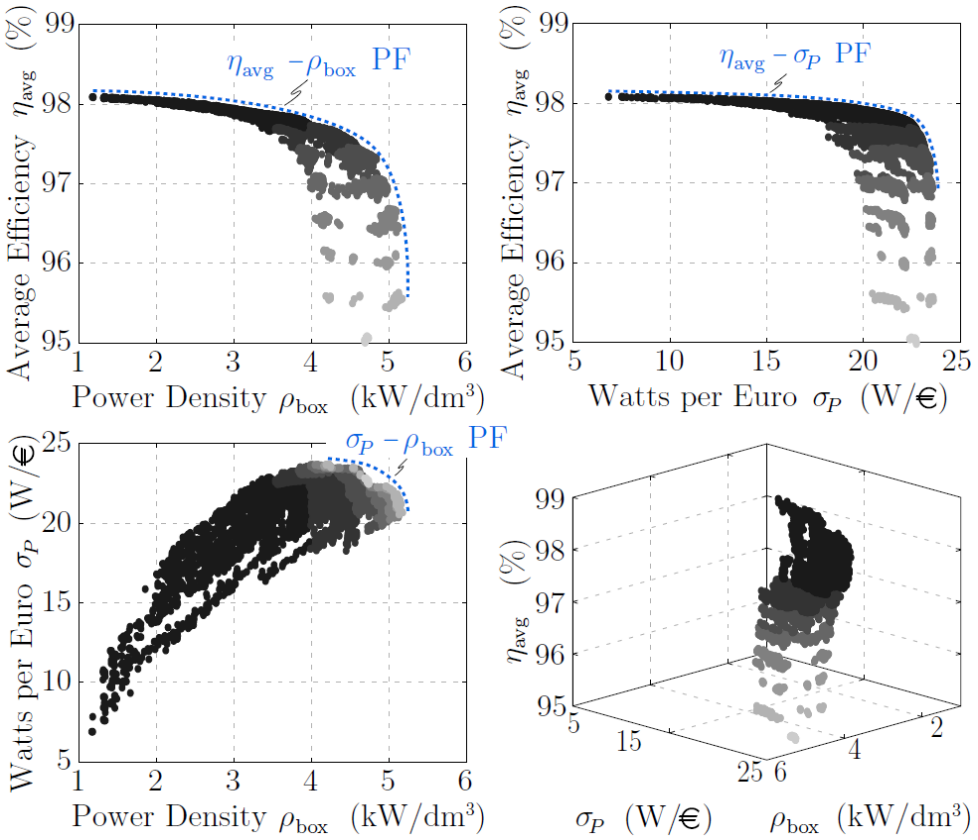




Optimization Results - Pareto Surfaces (1)

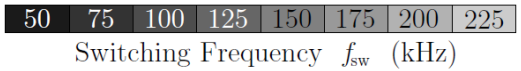
- 3-Level Dual Active Bridge

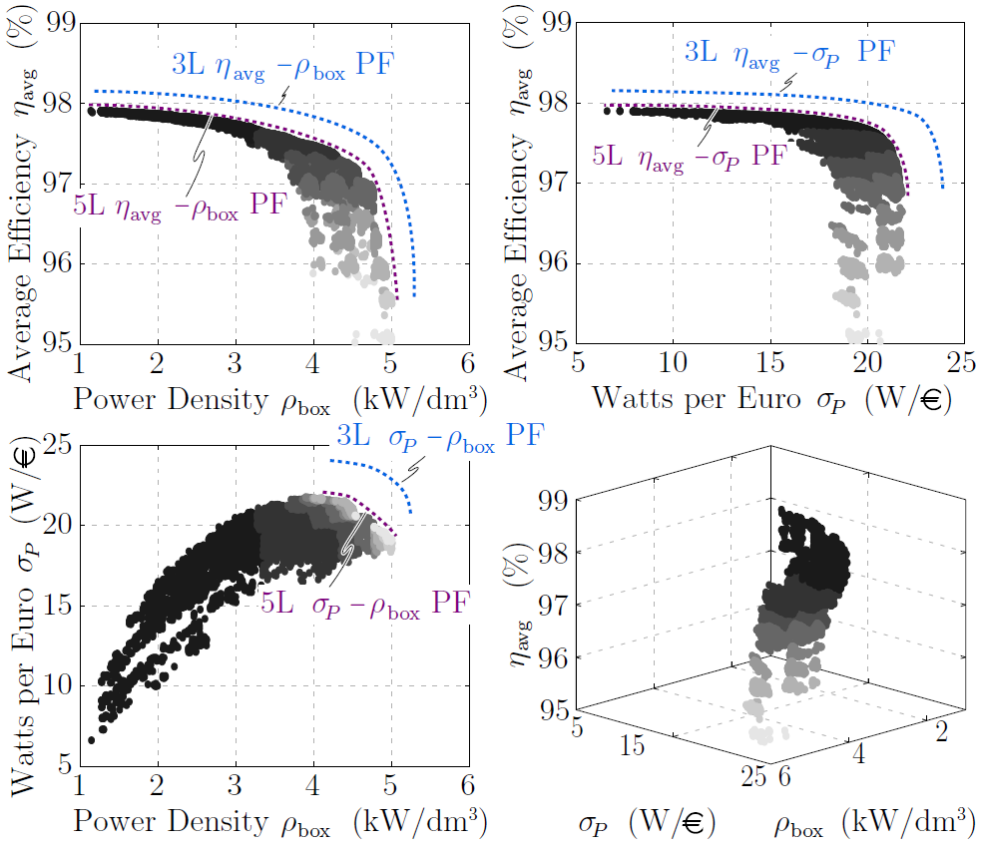




Optimization Results - Pareto Surfaces (2)

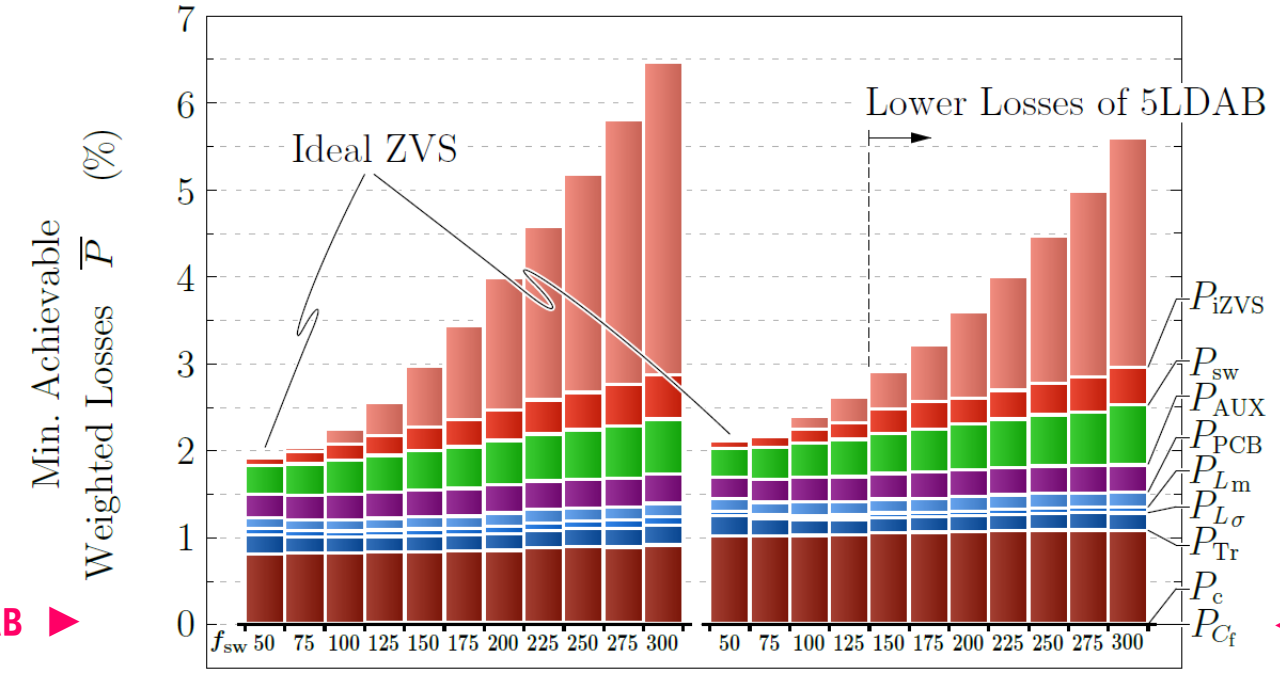
- 5-Level Dual Active Bridge





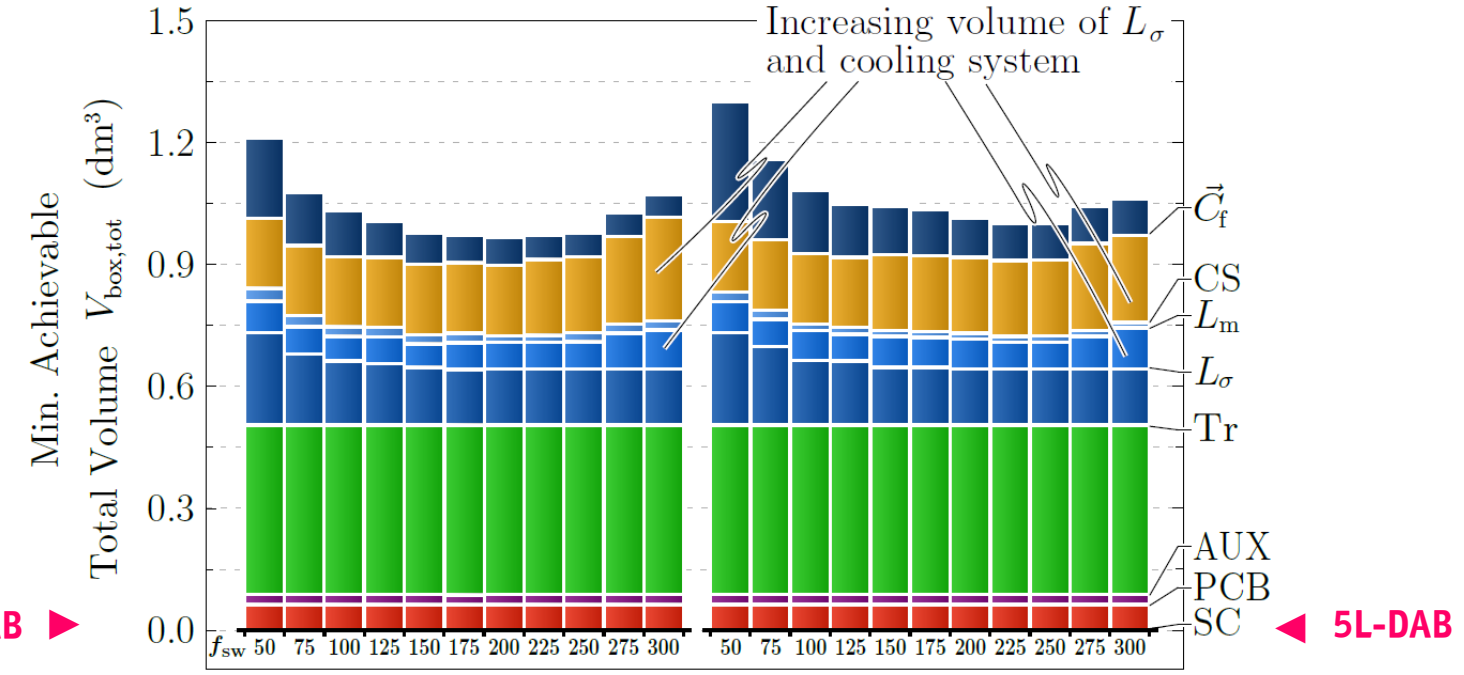
Optimization Results - Component Breakdown (1)

- Lower RMS Currents Overcompensated by Low Chip Utilization
- Higher 5L-DAB Conduction Losses P_c
- Lower 5L-DAB Switching Losses P_{sw} and Incomplete ZVS P_{iZVS} Losses Due to More Uniform Current Waveforms



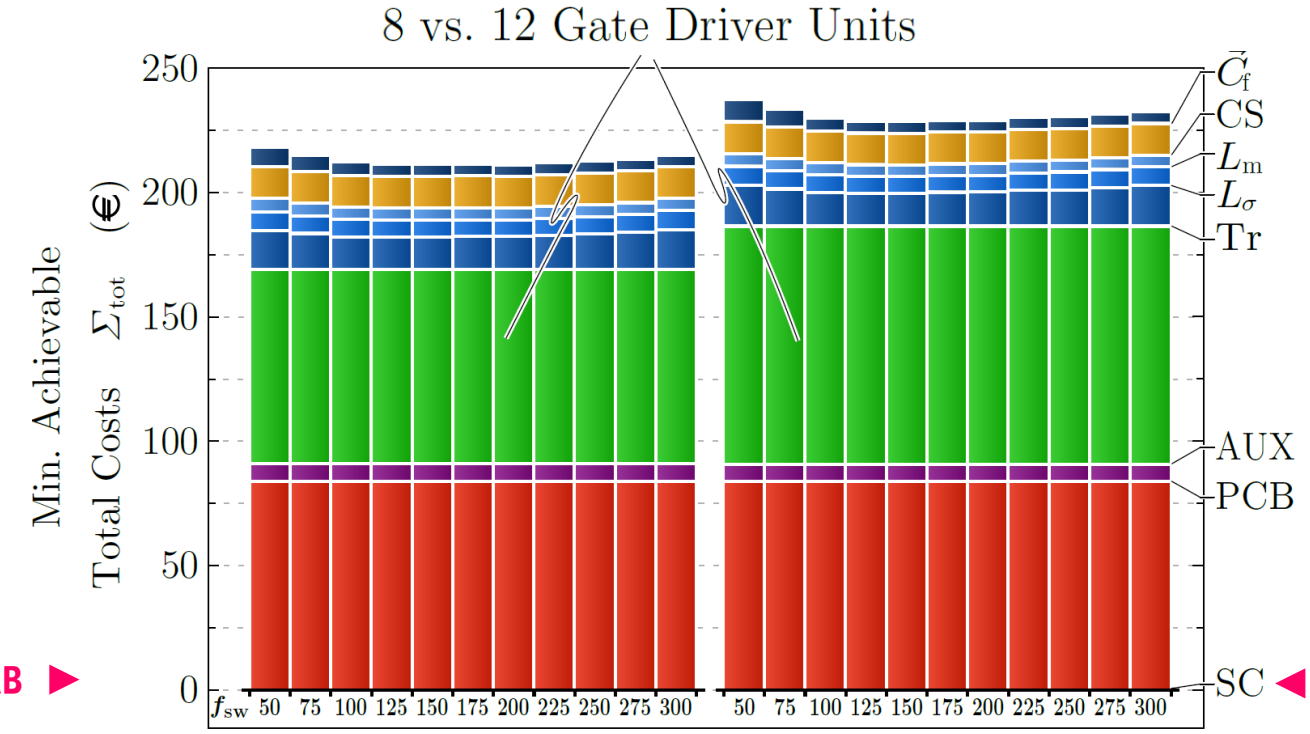
▶ Optimization Results - Component Breakdown (2)

- Higher 5L-DAB Volume Mainly Due to Higher Capacitance for Midpoint Balancing
- Increase of Magnetics Volume at High f_{sw} Due to High Core Losses
- Auxiliary Based on Prototype – Industrial Auxiliary Approx. Half the Volume



Optimization Results - Component Breakdown (3)

- Higher f_{sw} Allows for Lower Volume of Passives
- However, Magnetics Require More Expensive Litz Wire, Capacitors are Inexpensive
- Main Costs are Semiconductors and Auxiliary
- Auxiliary (incl. Gate Drivers) Based on Prototype – Industrial Auxiliary Approx. Half the Costs

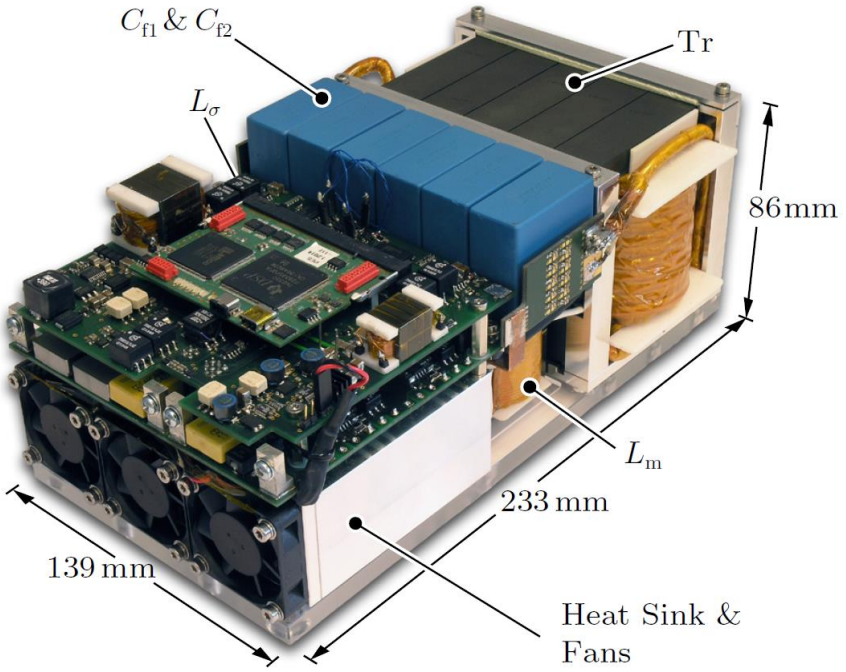


3L-DAB ▶ ◀ 5L-DAB

Experimental Verification (1)

- Hardware Prototype of Three-Level Dual Active Bridge (3L-DAB)

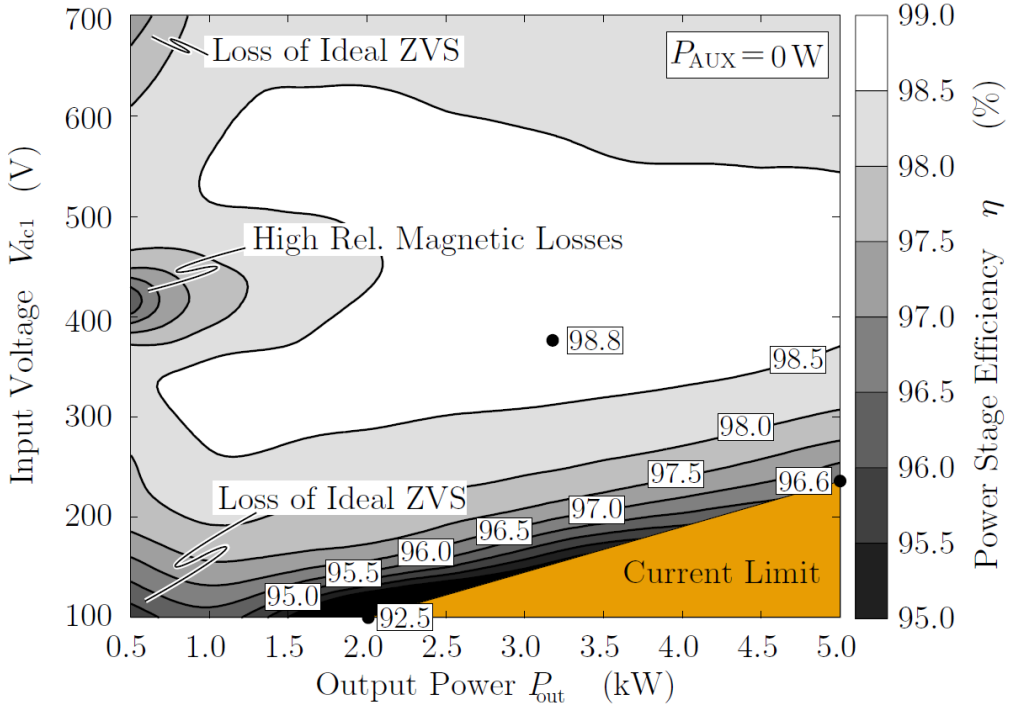
P = 5 kW
V_i = [100, 700] V
V_o = 750 V
f_{sw} = 50 kHz
V_{box} = 2.8 dm³ (171 in³)



- Power Density 1.8 kW/dm³
- Peak Efficiency 98.5%
- Average Efficiency 97.6%

Experimental Verification (2)

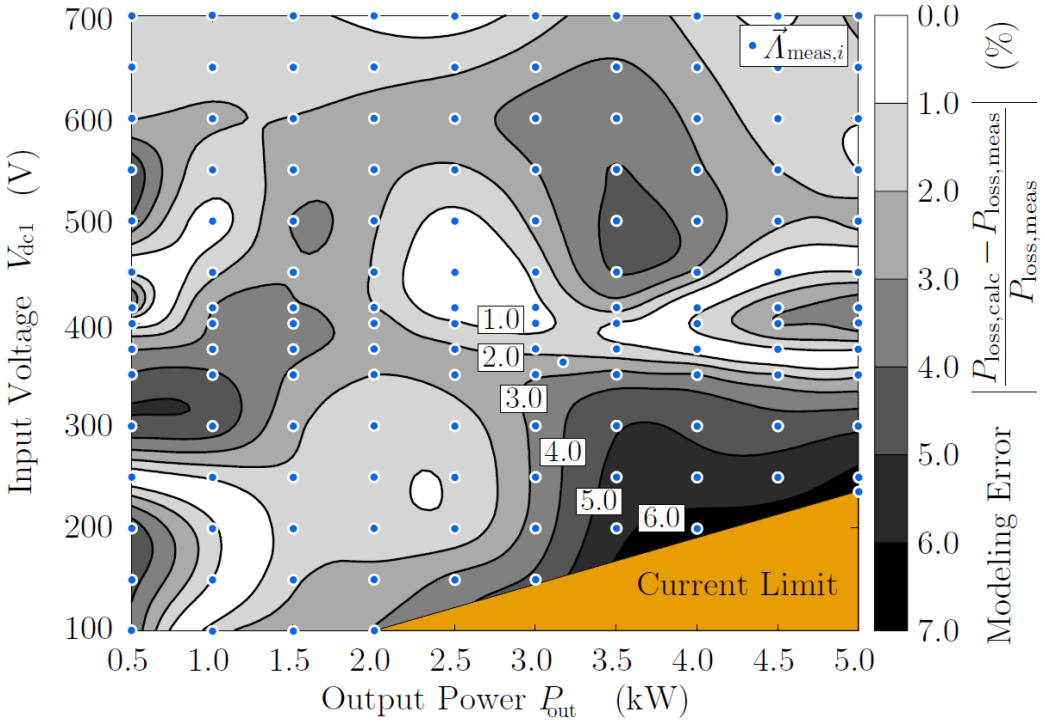
- **Very High Efficiency Despite High Functionality**



- Peak Efficiencies of 98.8% (Without Auxiliary) and 98.5% (incl. 10W Aux. Power)
- High Efficiency Over Extremely Wide Parameter Range
- ZVS in Most Operating Points

Experimental Verification (3)

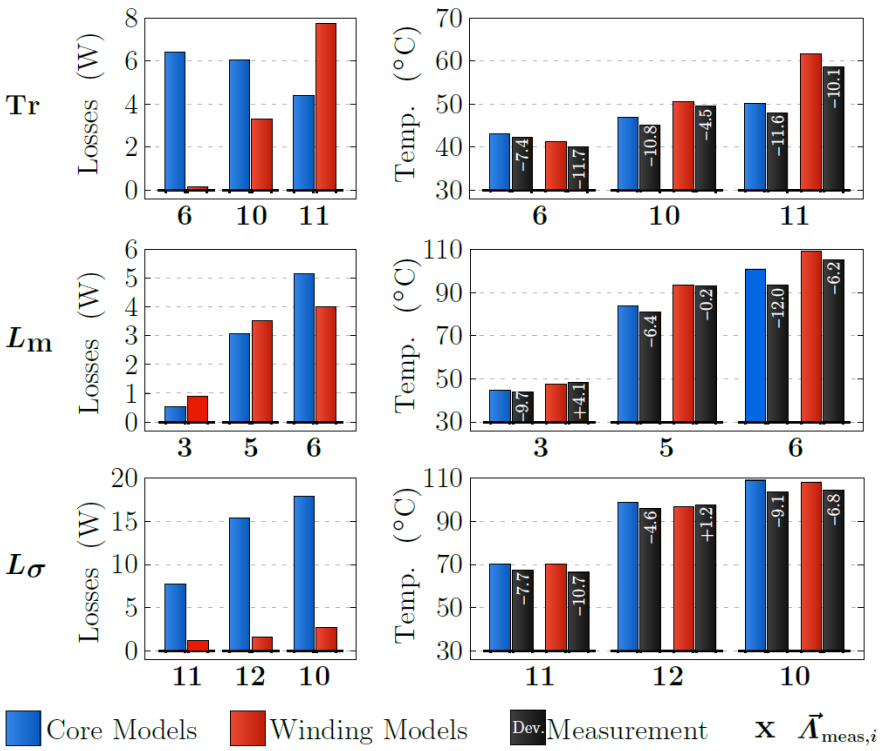
- **Very High Model Accuracy**



- **Average Error 2.5%**
- **Maximum Error 7.8%**
- **Widely Varying Mix of Loss Contributions**

Experimental Verification (4)

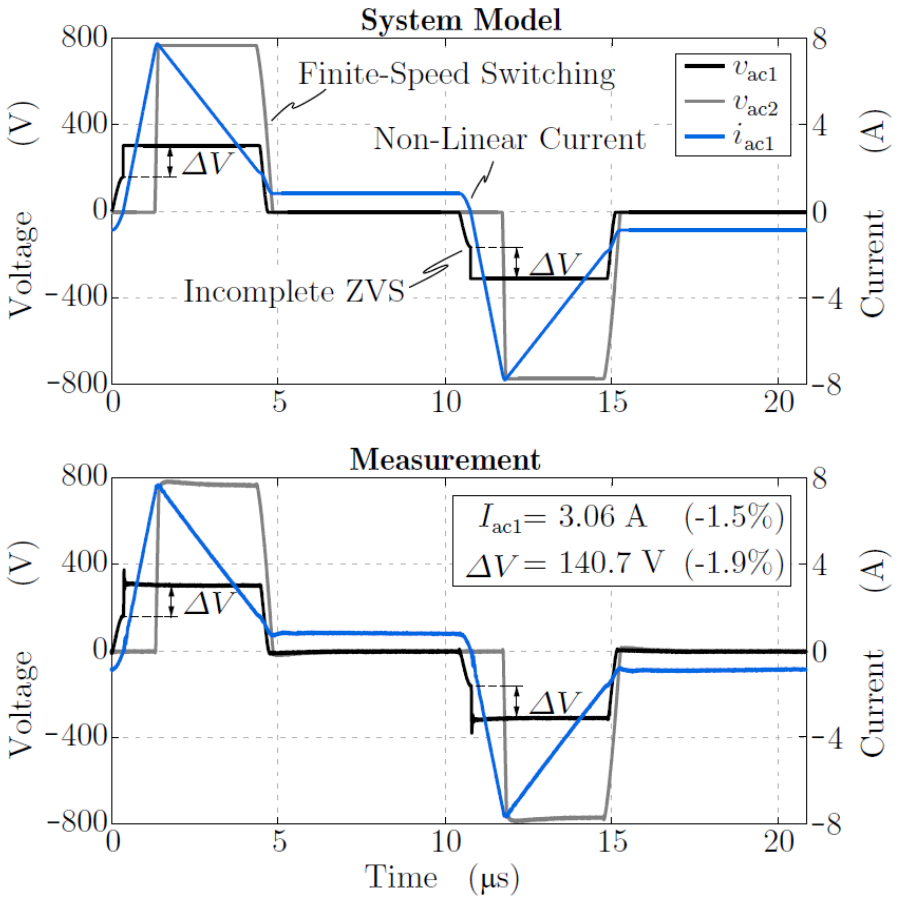
- **High Accuracy of Thermal Modeling**



— **Supports Calculated Loss Modeling**
— **Temperatures Generally Underestimated → Wiring, Thermal Coupling**

Experimental Verification (5)

- **Accuracy Prediction of Voltage and Current Waveforms**



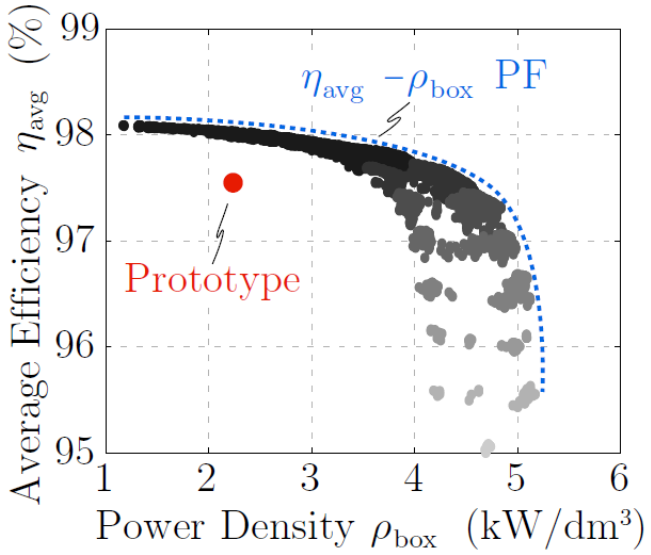
- Non-Linear Switching-Transitions
- Incomplete ZVS Transitions

Experimental Verification (6)

Comparison to Pareto Surface

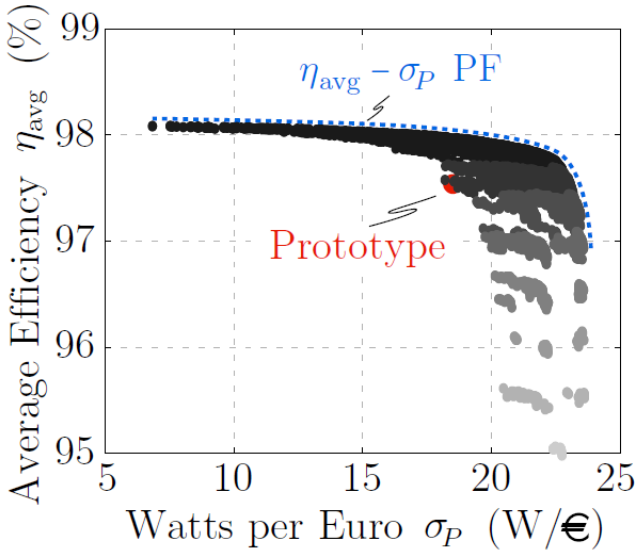
— Prototype Development

* No Optimization Routine
* Target Power Density of 2.0 kW/dm³



— Improvements with Advanced Multi-Objective Optimization

* 0.3% Higher Eff. @ Same Volume/Costs
* 40% Lower Volume and 20% Lower Costs @ Same Efficiency



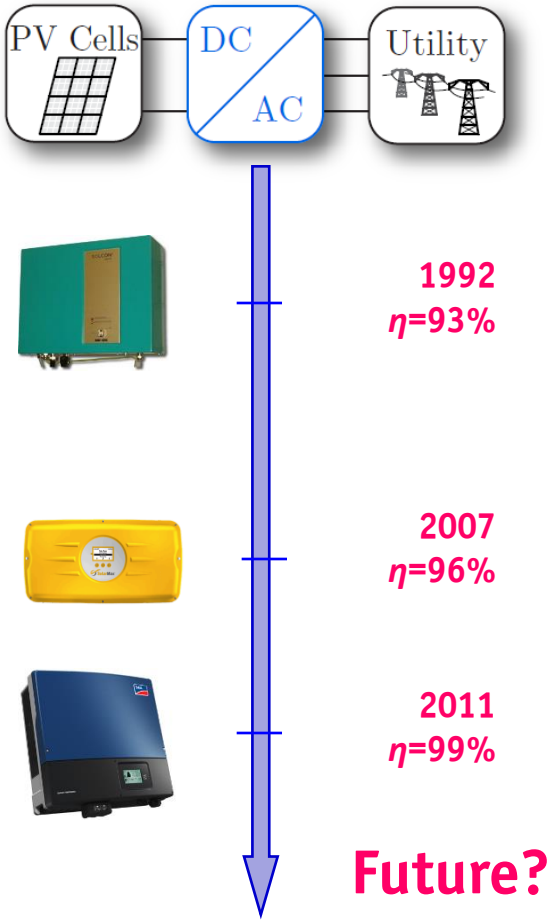
Conclusions Example I

- 3L-DAB Clearly Superior over 5L-DAB
  - More Efficient (Chip Area Utilization)
  - Higher Power Density (Capacitors)
  - Lower Costs (Gate Drivers)
  - Much Simpler → Reliability
  - High Functionality (Voltage Range, Galv. Isolation, Bidir.) @ High Efficiency
  - Could not be Achieved w/o SiC
- ZVS
  - Difficult to Achieve at Low Load and/or High Switching Frequencies
  - Parasitic Capacitances (Semicond. Package (!) to Heat Sink, Magnetics, PCB Layout) Become Highly Important Due to Required Add. Charge
- Usefulness of Multi-Objective Optimization Routine
  - High Accuracy of Models
  - Improvements for Prototype Revealed

Converter Optimization Example II

DC/AC PV Application
Topologies/Modulation Schemes
Materials/Components
Optimization
Pareto Surfaces
LCC Post-Processing 

▶ Motivation (1)



- Advancements in PV Converter Design and Development
  - 1990s – 2000s
    - Main Focus on Efficiency
    - Improvements from 90% to >98%
  - 2010s
    - Econom. Downturn and Slower Market Growth
    - Main Focus on Costs (!)
- Ongoing Discussion on Whether and How SiC Can Improve PV-Inv. Performance (!)

▶ Motivation (2)

■ Opportunities of SiC in PV Applications

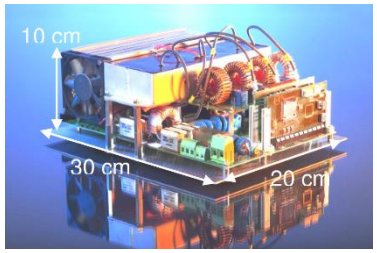
(1) Same Sw. Frequ. and Higher Eff. @ Same Volume → Costs?
(2) Higher Sw. Frequ. and Lower Volume @ Same Eff. → Costs?
(3) Other Topologies/Modul. Schemes (e.g. Higher Voltages, ZVS Operation, 2-Level, etc...)

▶ Systematic Multi-Objective Optimization Imperative!

■ State of Research

— Only Very Few Contributions with Multi-Objective Optimization
— Mostly Case Studies of Single Prototype and Single Frequency, Main Inductance etc.

Source: Fraunhofer ISE



5kW 2-Level w/o DC/DC
η=96.8% @ 48kHz
η=93.0% @ 144kHz
ρ = 0.83 kW/dm^3

▶ Optimal?

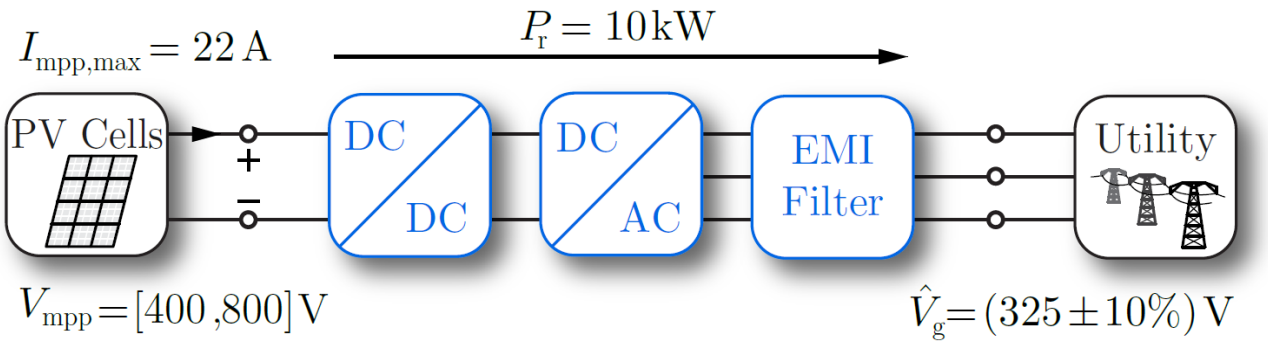
Source: SMA

20.5kW 3-Level w/o DC/DC
η=98.6% @ 16kHz
ρ = 0.17 kW/dm^3 @ 52kg

▶ Optimal?

Application and Goals

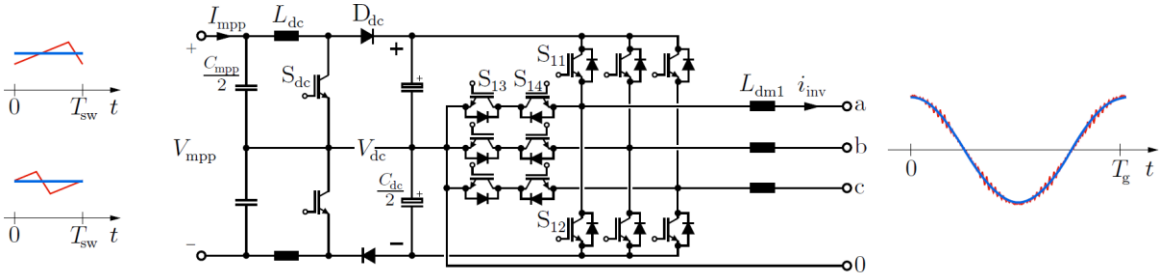
- Single-Input/Single-MPP-Tracker Multi-String PV Converter
- DC/DC Boost Converter for Wide MPP Voltage Range
- Output EMI Filter
- Typical Residential Application



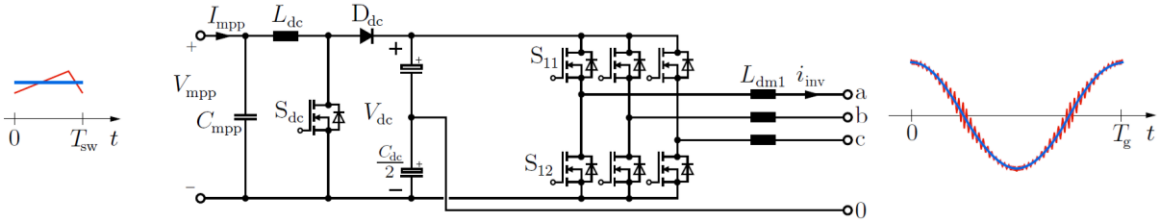
- Systematic Multi-Objective η-ρ-σ-Comparison of Si vs. SiC
- Exploit Excellent Hard- *AND* Soft-Switching Capabilities of SiC
- Find Useful Switching Frequency and Current Ripple Ranges
- Find Appropriate Core Material

▶ Topologies - Converter Stages

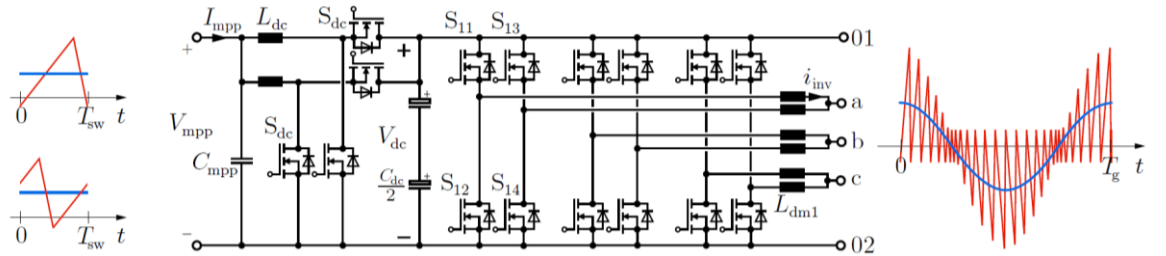
- **All Si IGBT 3-Level PWM Inverter (3L-PWM)**



- **All SiC MOSFET 2-Level PWM Inverter (2L-PWM)**

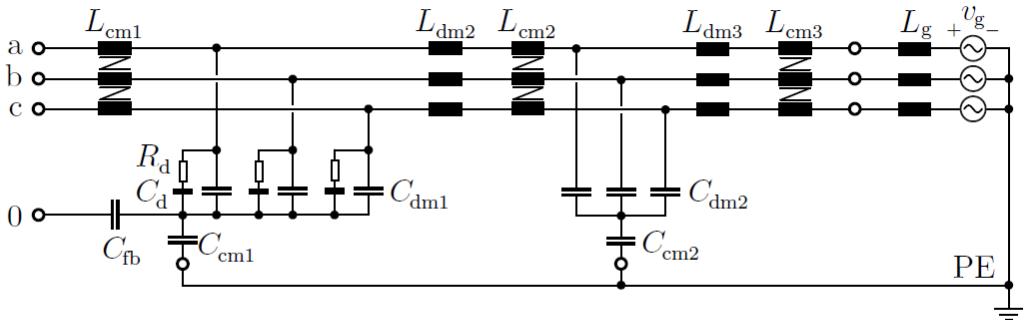


- **All SiC MOSFET 2-Level Double-Interleaved TCM-Inverter (2L-TCM)**

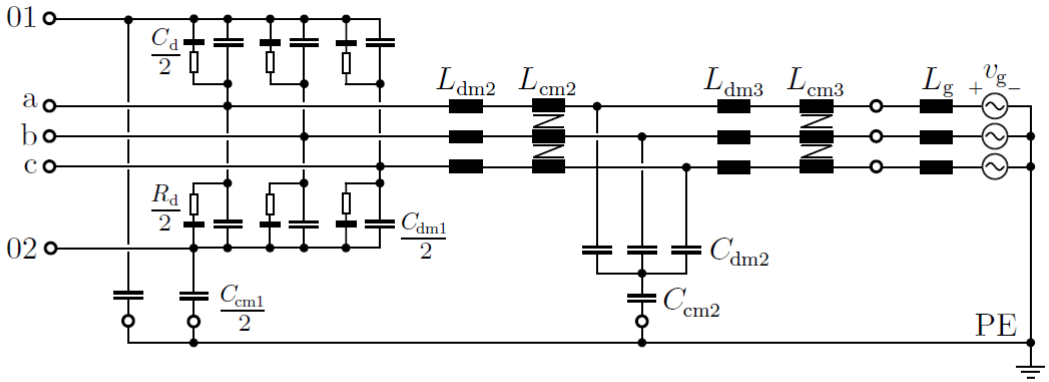


▶ Topologies - Filter Stages

- 2-Stage DM & CM Filter for 2L-PWM and 3LP-WM



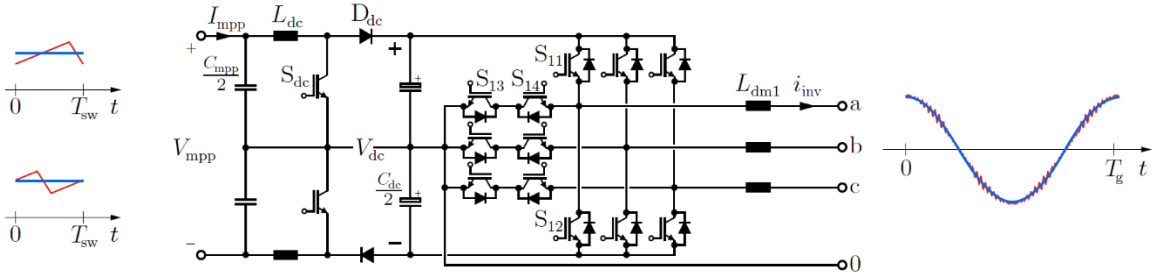
- 2-Stage DM & CM Filter for 2L-TCM
- TCM Inductor Acting as DM & CM Inductance



Modulation Schemes - PWM Converters

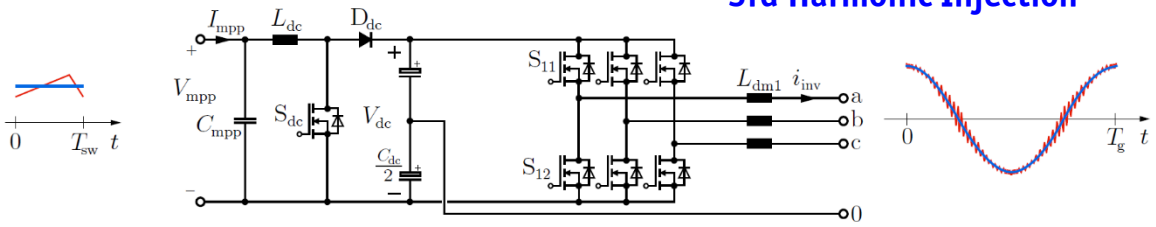
Three-Level PWM Inverter (3L-PMW)

- Symmetric Boost Converter
- Interleaved Operation
- Part. Compensation of LF DC-Link Midpoint Variation
- 3-Level T-Type Converter
- 3-Level PWM Modulation
- 3rd Harmonic Injection



Two-Level PWM Inverter (2L-PMW)

- Standard DC/DC Booster
- Standard Modulation
- 2-Level Converter
- 2-Level PWM Modulation
- 3rd Harmonic Injection

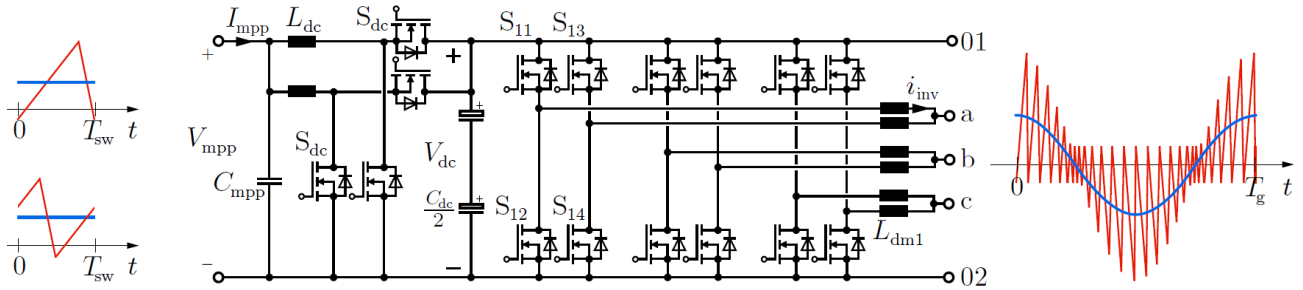


Modulation Schemes - TCM Converter

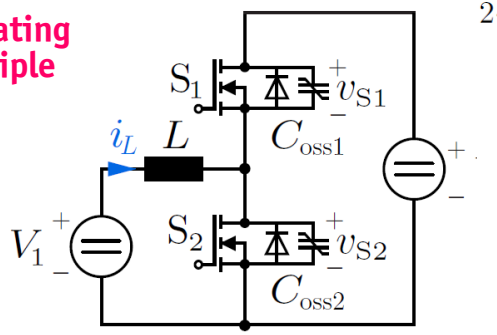
Two-Level TCM Inverter (2L-TCM)

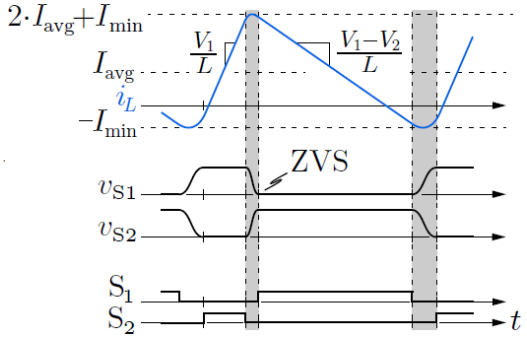
- 2-Level/Double Interleaved Booster
- Interleaved TCM Operation
- Turn-Off of Branch in Partial Load

- 2-Level/Double Interleaved
- Interleaved TCM Operation
- Turn-Off of Branch in Partial Load



TCM Operating Principle

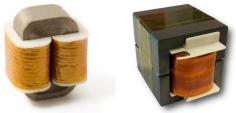
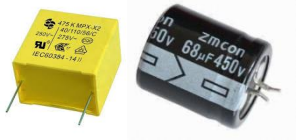




- ZVS for All Sw. Transitions
- Variable f_{sw}

- I_{min} to Limit f_{sw}
- Losses Due to I_{min} @ Low Loads

Components and Materials

	3L-PWM ▼	2L-PWM ▼	2L-TCM ▼
Power Semiconductors	 — 6 x Infineon Si IGBT H3 25 A 1200 V / PiN Diode — 6 x Infineon Si IGBT T&F 30 A 600 V / PiN Diode — 2 x Infineon Si IGBT T&F 30 A 600 V — Infineon Si PiN Diode 45 A 600 V	— 7 x CREE SiC MOSFET 80 mΩ 1200 V — 1 x CREE SiC Schottky Diode 20 A 1200 V	— 16 x CREE SiC MOSFET 80 mΩ 1200 V
Cooling System	 — Optimized Al Heat Sinks — Range of Sanyo Low Power Long Life DC Fans		
Main Induct.	 — METGLAS 2605SA1 Amorphous Iron C Cores — Solid Round Wire	*Or*	— EPCOS N87 Ferrite E Cores — Litz Wire With Range of Strand Diameters
DC Caps	 — EPCOS MKP DC Film Capacitors 575V and 1100 V for MPP Cap. — EPCOS Long Life Al Electrolytic Capacitors 500 V for DC-Link Cap.		
Filter	 — EPCOS X2 (DM/CM) and Y2 (CM) EMI Capacitors — Magnetics KoolMu Gapless Powder Cores / Solid Round Wire (DM) — VAC Vitroperm 250F/500F Nanocrystalline Toroid Cores / Solid Round Wire (CM)		

▶ Global Optimization Routine

■ Independent Design Variables

— **3L-PWM**

$$\vec{\Pi}_{\text{sys}}^{\text{3LPWM}} : f_{\text{sw}} \in [6, 36]\,\text{kHz}, \quad \Delta I_{L,\text{max}}^{\text{pp}} \in [5, 60]\,\%$$

— **2L-PWM**

$$\vec{\Pi}_{\text{sys}}^{\text{2LPWM}} : f_{\text{sw}} \in [12, 72]\,\text{kHz}, \; \Delta I_{L,\text{max}}^{\text{pp}} \in [5, 60]\,\%$$

— **2L-TCM**

$$\vec{\Pi}_{\text{sys}}^{\text{2LTCM}} : f_{\text{sw,min}} \in [12, 84]\,\text{kHz}, \quad k_{f_{\text{sw}}} \in [4, 12]$$

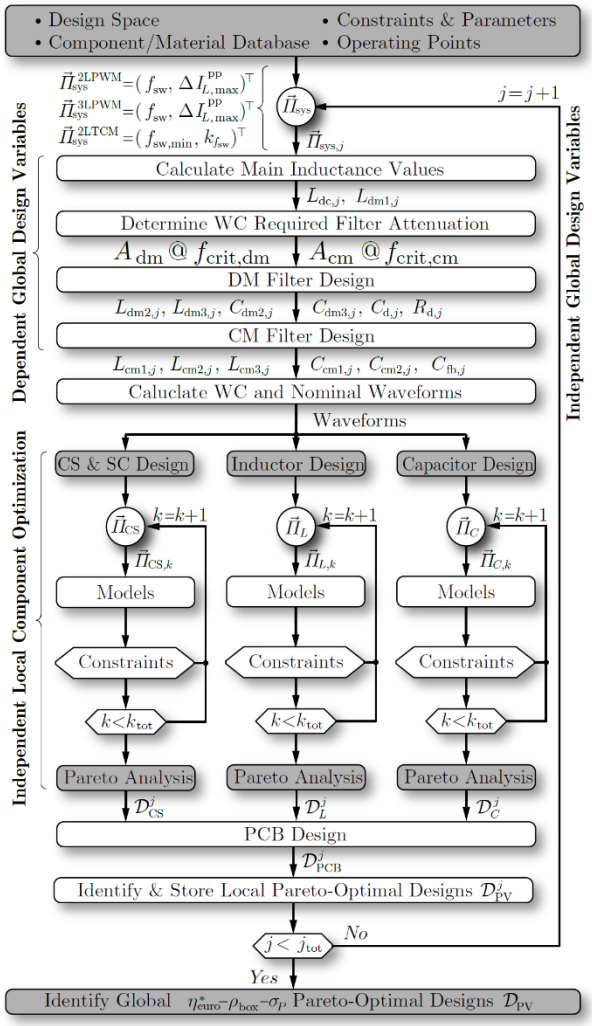
■ Dependent Design Variables

— **Main Inductances Function of f_{sw} and $\Delta I_{L,max}^{pp}$**
— **Filter Components Based on CISPR Class B**

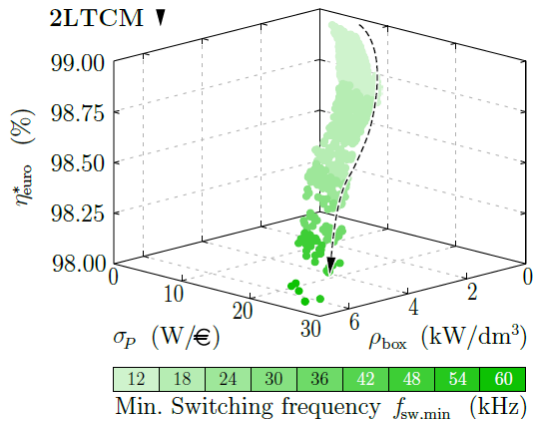
■ European Efficiency

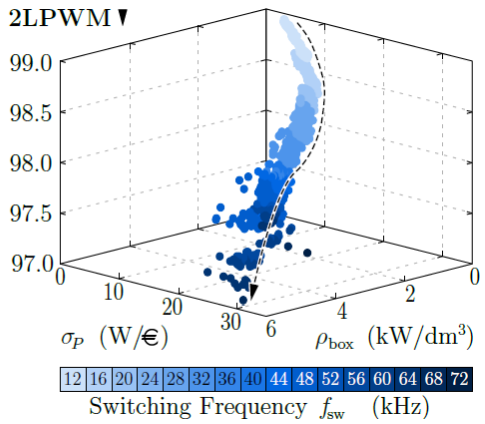
$$\eta_{\text{euro}} = 0.05 \cdot \eta_{0.03 \cdot P_r} + 0.1 \cdot \eta_{0.1 \cdot P_r} + 0.2 \cdot \eta_{0.2 \cdot P_r} + 0.3 \cdot \eta_{0.3 \cdot P_r} + 0.5 \cdot \eta_{0.5 \cdot P_r} + 1 \cdot \eta_{1.0 \cdot P_r}$$

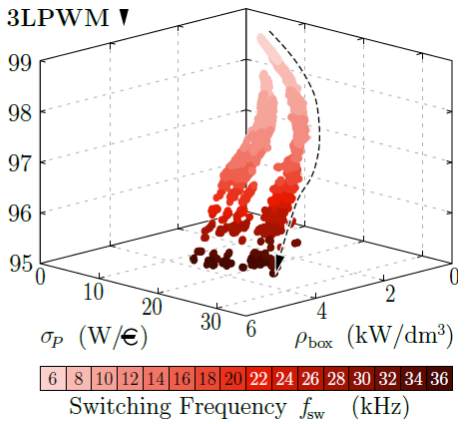
— **Add. Weighted for {525, 575, 625} V MPP Voltage**



▶ Optimization Results - Pareto Surfaces (1)







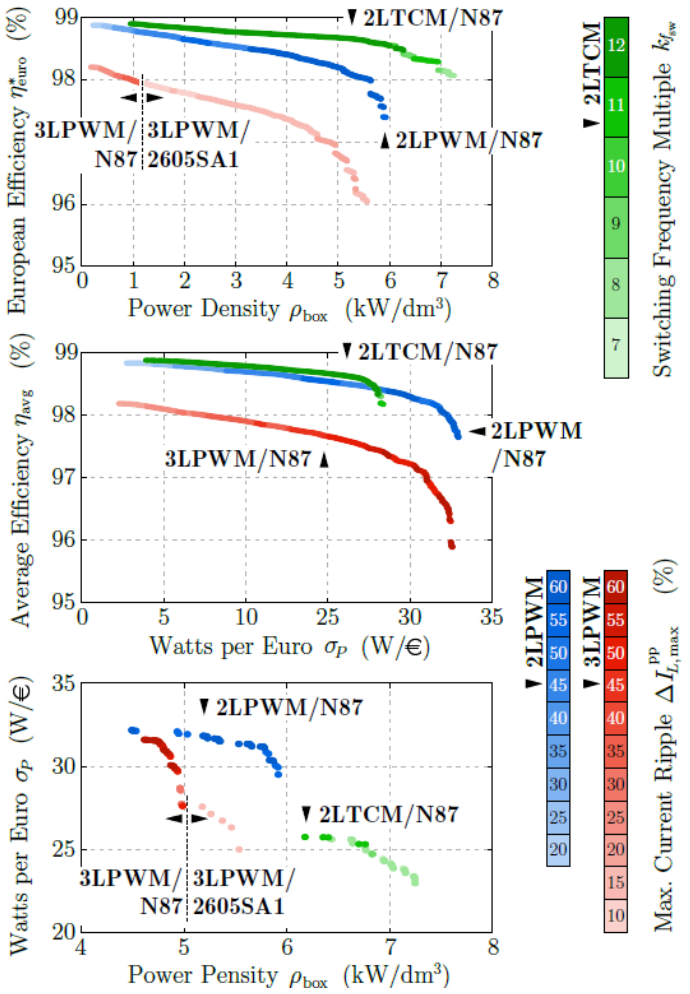
- No Pareto-Optimal Designs for $f_{sw,min}$> 60 kHz
- No METGLAS Amorphous Iron Designs

- Pareto-Optimal Designs for Entire Considered f_{sw} Range
- No METGLAS Amorphous Iron Designs

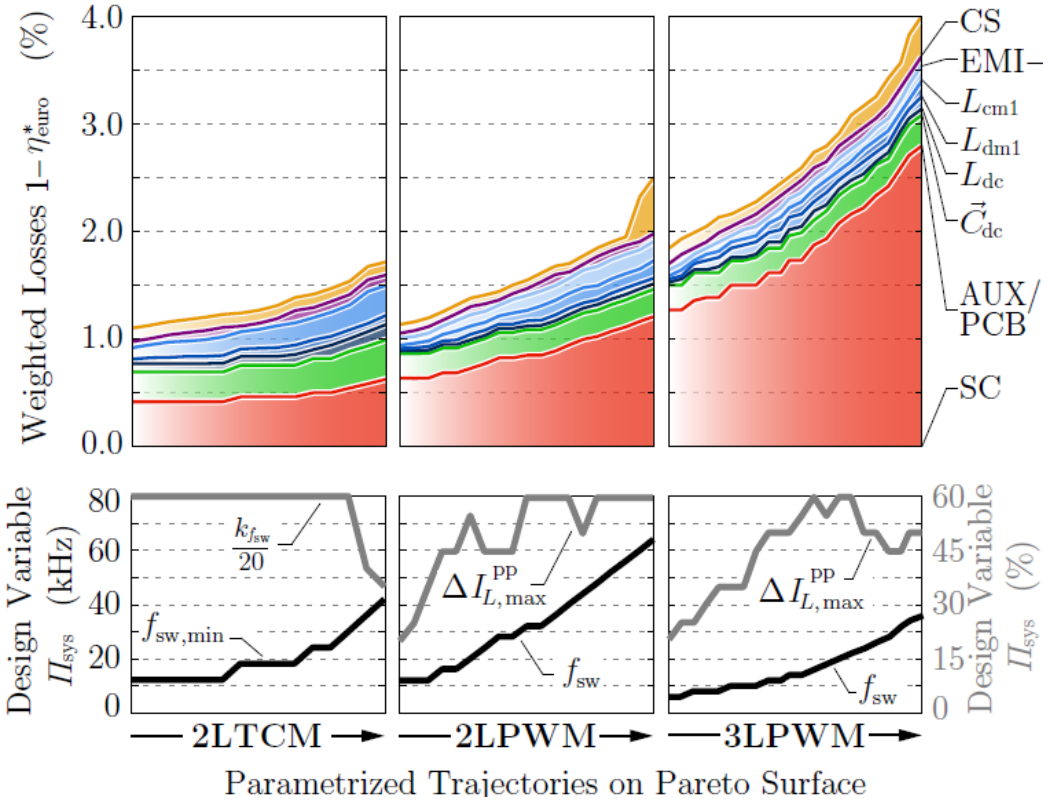
- Pareto-Optimal Designs for Entire Considered f_{sw} Range
- METGLAS Amorphous Iron and Ferrite Designs

Optimization Results - Pareto Surfaces (2)

- **3L-PWM Core Material**
  - Compact Designs with Amorphous Core Material @ Low Ripples
  - Cheap Designs with Ferrite @ High Ripples Despite Larger Volume
- **2L-TCM Core Material**
  - Only Ferrite for 2L-TCM Due Large HF Excitations
  - Expected Result
- **2L-PWM Core Material**
  - Ferrite @ High Ripples Cheaper *AND* Smaller - Unexpected Result (!)
  - Amorphous Core Material too High Losses Already @ Low Ripples, High Flux Density Not Exploited

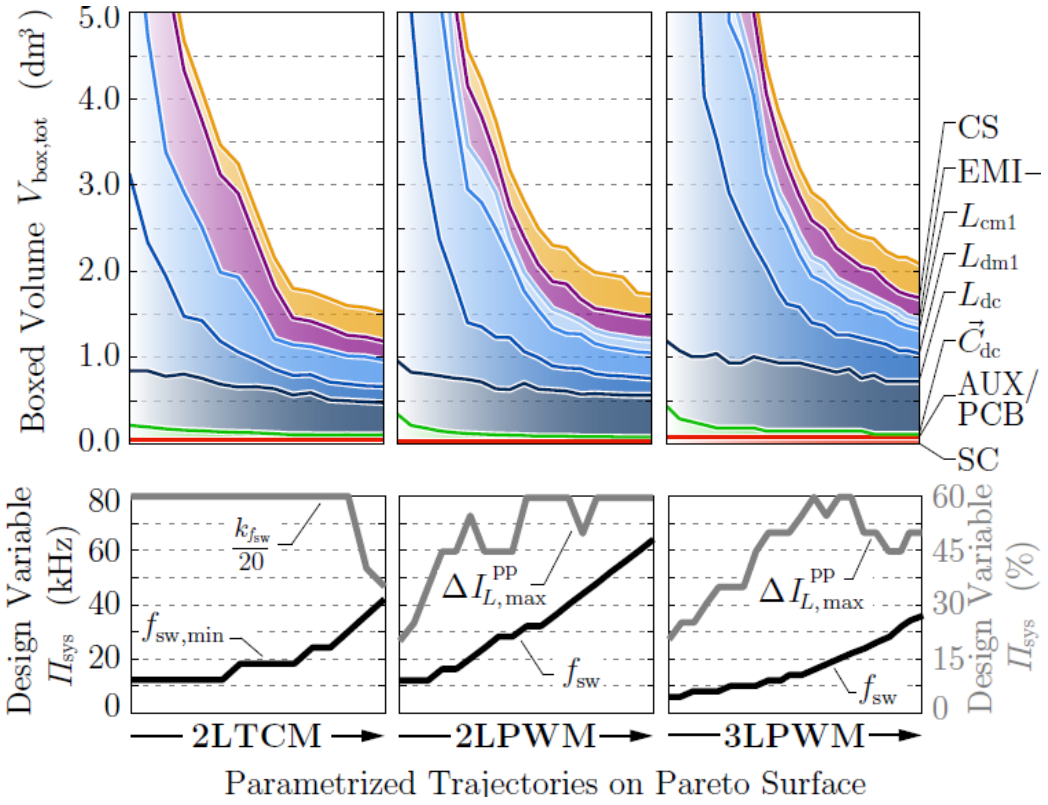


▶ Optimization Results – Component Breakdowns (1)



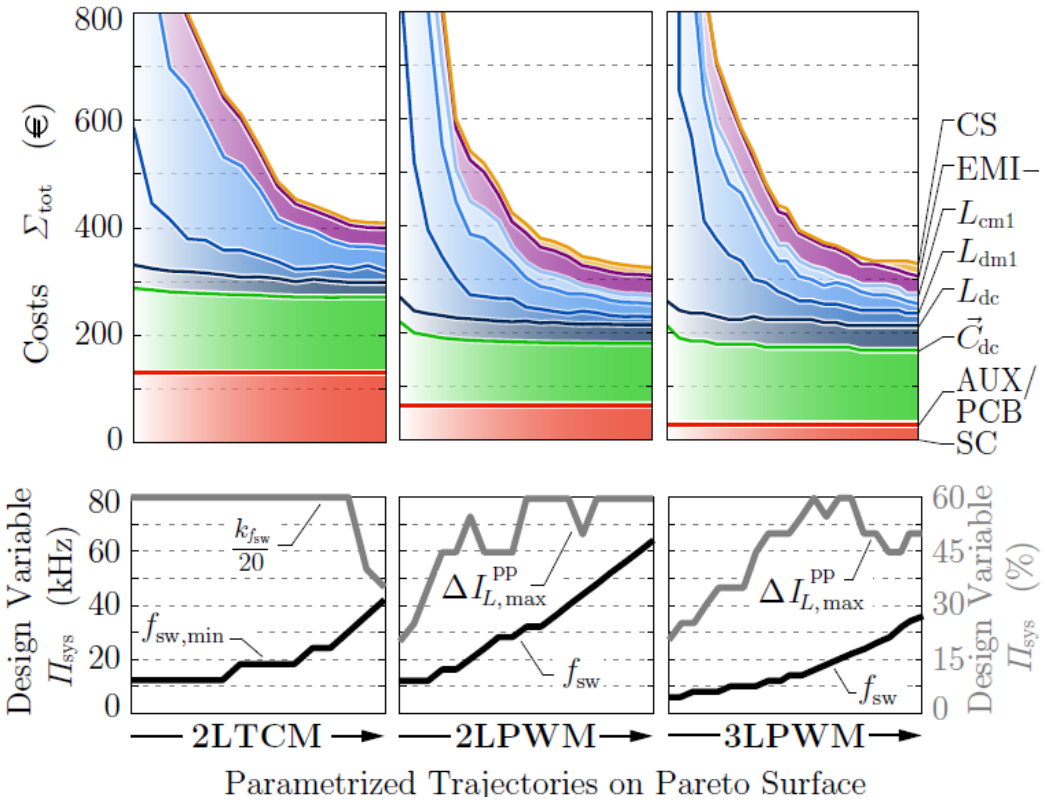
- Semiconductor Losses Clearly Dominating (35 to 70%)

▶ Optimization Results – Component Breakdowns (2)



- DC Caps of 3L-PWM Largest Because of Midpoint Variation / Balancing

Optimization Results – Component Breakdowns (3)



- Higher Gate Driver Costs (incl. in Aux.) of 3L-PWM Compensates Lower Si Semicond. Costs

▶ Optimization Results - Semiconductor Losses

- **Sensitivities of Semiconductor Losses**

— **2L-TCM**

* Wide Sw. Frequency Range / Lower I_{min} Results in Lower Conduction Losses

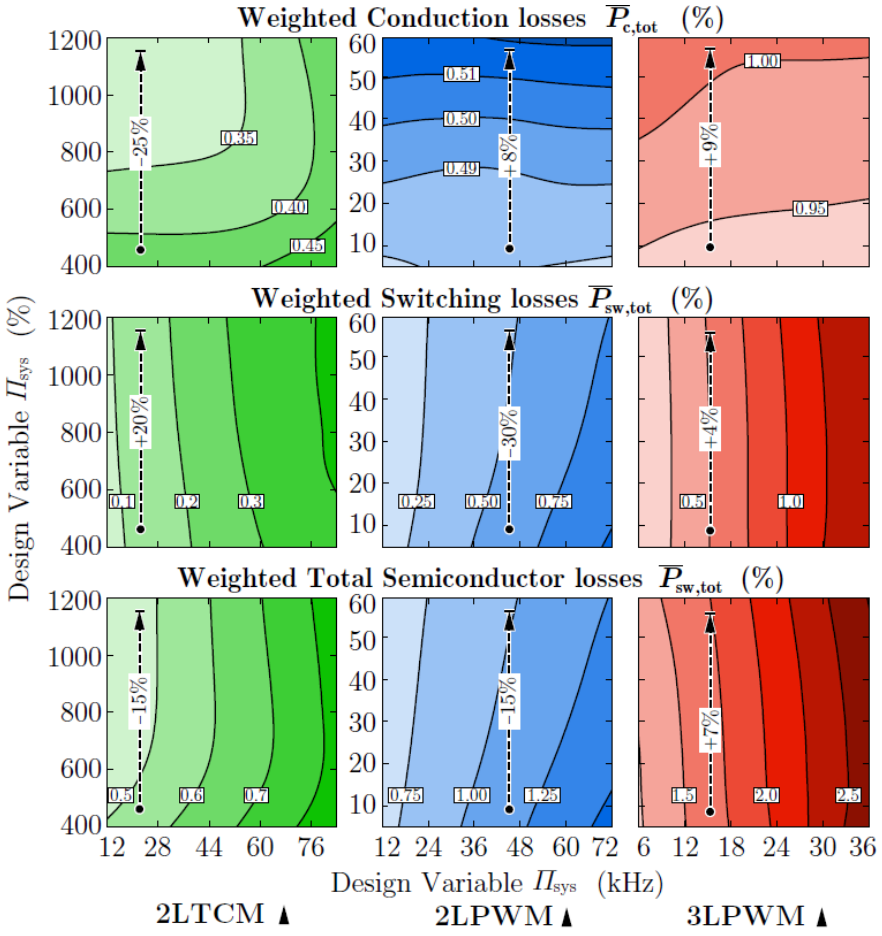
— **2L-PWM**

* High Ripple Operation Lower Switching Losses Due ZVS

— **3L-PWM**

* No ZVS for IGBTs

* High Ripples are Causing Higher Cond. Losses



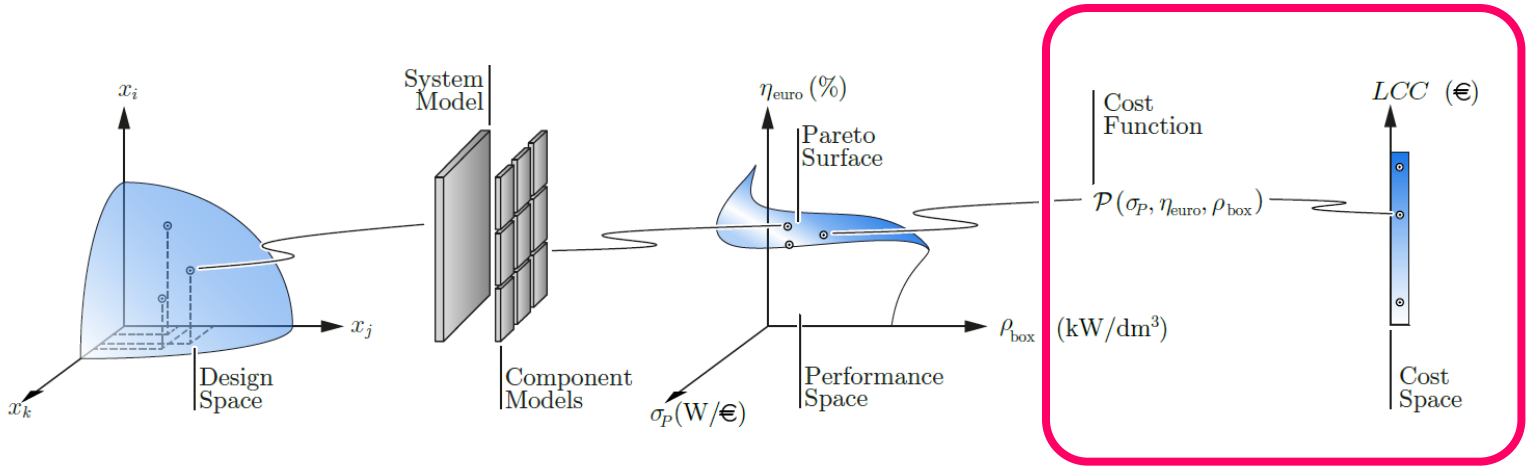
Extension to Multi-Objective Optimization Approach

Performance Space Analysis

- 3 Performance Measures: η, ρ, σ
- Reveals Absolute Performance Limits / Trade-Offs Between Performances

LCC Analysis

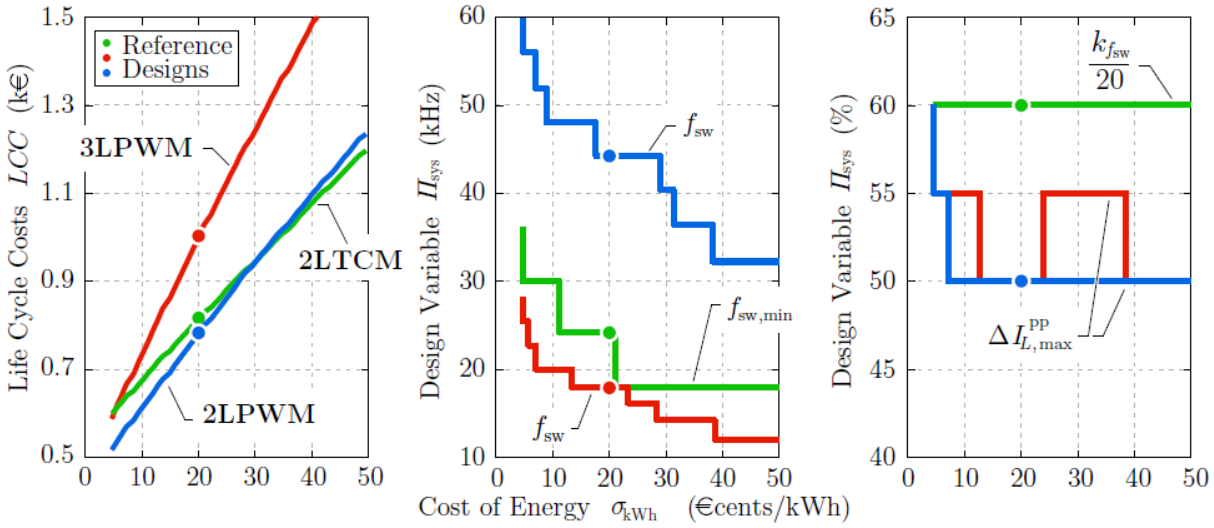
- Post-Processing of Pareto-Optimal Designs
- Determination of Min.-LCC Design
- Arbitrary Cost Function Possible



- Which is the Best Solution Weighting η, ρ, σ, e.g. in Form of Life-Cycle Costs (LCC)?
- How Much Better is the Best Design?
- Optimal Switching Frequency?

Post-Processing

LCC – Analysis (1)



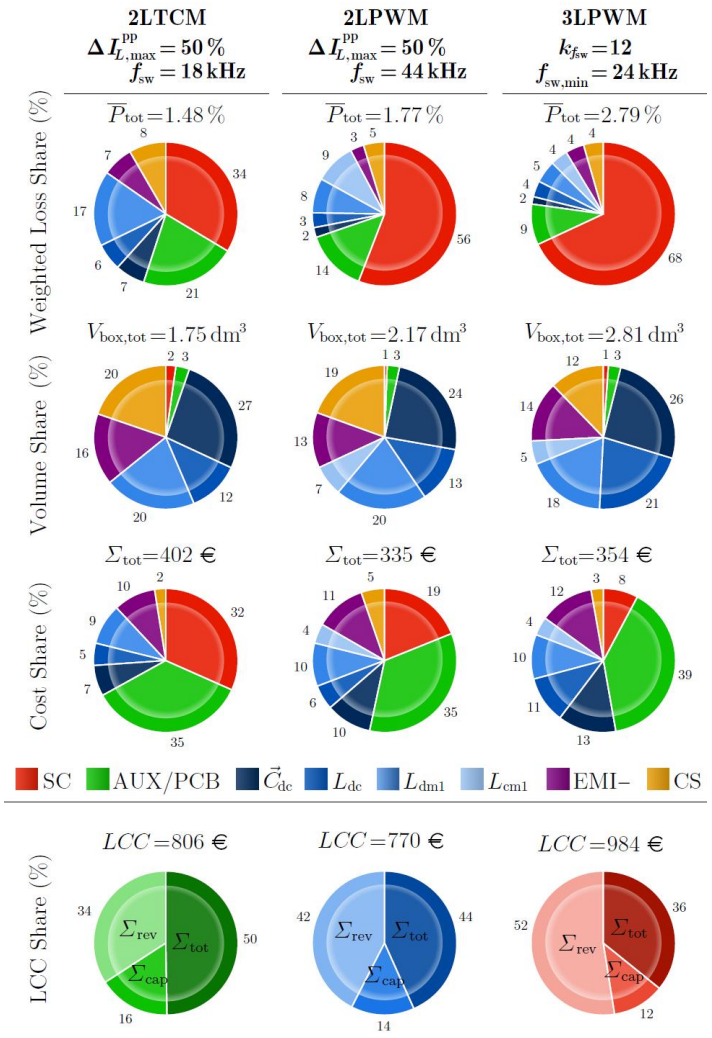
- Simple Life-Cycle Costs (LCC) Function for Mapping into 1D Cost Space
- Initial Costs, Capital Costs and Lost Revenue (=Losses) Based on Net-Present-Value (NPV) Analysis

$$LCC = \Sigma_{tot} + \sum_{n=1}^{N} \left\{ q \cdot \Sigma_{tot} + \Sigma_{losses}(\eta_{euro}) \right\} \cdot \frac{1}{(1+q)^n}$$

- Assumptions $q = 5\,\%/\text{year}$ $N = 10$ years

Post-Processing

- LCC – Analysis (2)



- **Best System**
  2L-PWM @ 44kHz & 50% Ripple

- 22% Lower *LCC* than 3L-PWM
- 5% Lower *LCC* than 2L-TCM
- Simplest Design
- Probably Highest Reliability
- Volume Advantage Not Considered Yet (Housing!)

▶ Conclusions - Example II

■ SiC Systems Superior to State-of-The-Art Si System

- Generally Higher Efficiency and Power Density of SiC
- Initial Costs only Marginally Lower (SiC 2L-PWM) or Higher (SiC 2L-TCM)
- TCM Operated System More Complex but With Highest Potential for Further Improvements

■ LCC Analysis to Determine Optimal Design

- SiC 2L-PWM @ 44 kHz vs. Si 3L-PWM @ 18 kHz → 22% Lower LCC of SiC
- Initial Costs 5% Lower
- Smaller Housing and Higher Reliability Not Considered Yet

■ Usefulness of Multi-Objective Optimization Routine

- SiC can Improve η, ρ, and σ Simultaneously
- Optimal Switching Frequencies Lower than in Previous Publications
- Results/Findings Not Possible with η-, ρ- or η-ρ-Optimizations or Single Prototypes

- ***Conclusions*** →

Overall Summary

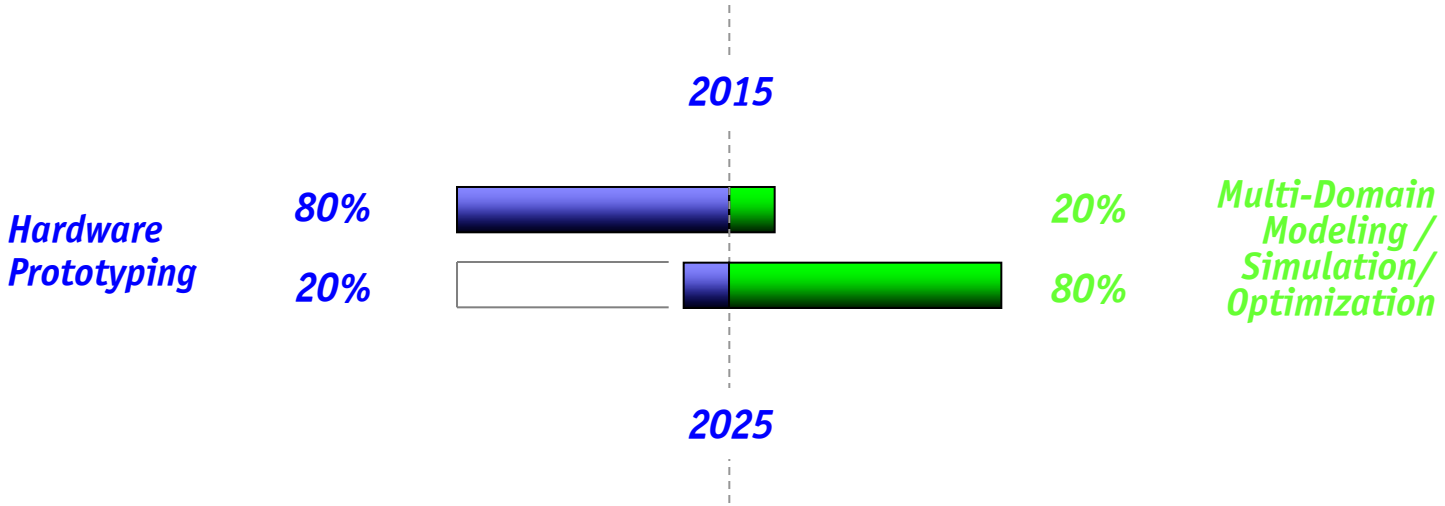
- Only Full System Level η-ρ-σ-Optimization Reveals Full Adv. of SiC (!)
  - Adv. Cannot be Identified for 1:1 Replacement or only 1D-Optimization
- Rel. Low Optimum SiC Sw. Frequencies Calculated Compared to Literature
  - 44kHz for 2L-SiC Inverter vs. 18kHz for 3L-Si-IGBT Inverter
  - Frequently Incomplete Models Employed in Publications
- Advantages of SiC Concerning Efficiency, Power Density & Costs
  - Lower System Complexity (2L vs. 3L) / Higher Reliability
  - Saving in Passives Overcompensates Higher SiC Costs
- SiC Allows Massive η-ρ-Gain vs. 1200V Si for High-Frequ. DC/DC Converters
  - Design for Minim. Parasitic Cap. to Ensure ZVS @ Low Effort
  - Research on HF Magnetics / TCM ZVS Schemes / Packaging Mandatory

SiC →

- Higher Efficiency / Power Density @ Same Costs
- Lower Complexity / Higher Reliability
- Higher Functionality

▶ Future Design Process

- **Main Challenges: Modeling (EMI, etc.) & Transfer to Industry**



- Reduces Time-to-Market
- More Application Specific Solutions (PCB, Power Module, and even Chips)
- Only Way to Understand Mutual Dependencies of Performances / Sensitivities (!)
- Simulate What Cannot Any More be Measured (High Integration Level)

Future Research

▶ Future Challenges

- Consider Converters like "Integrated Circuits"
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

— "Converter" → "Systems" (Microgrid) or "Hybrid Systems" (Autom. / Aircraft)
— "Time" → "Integral over Time"
— "Power" → "Energy"

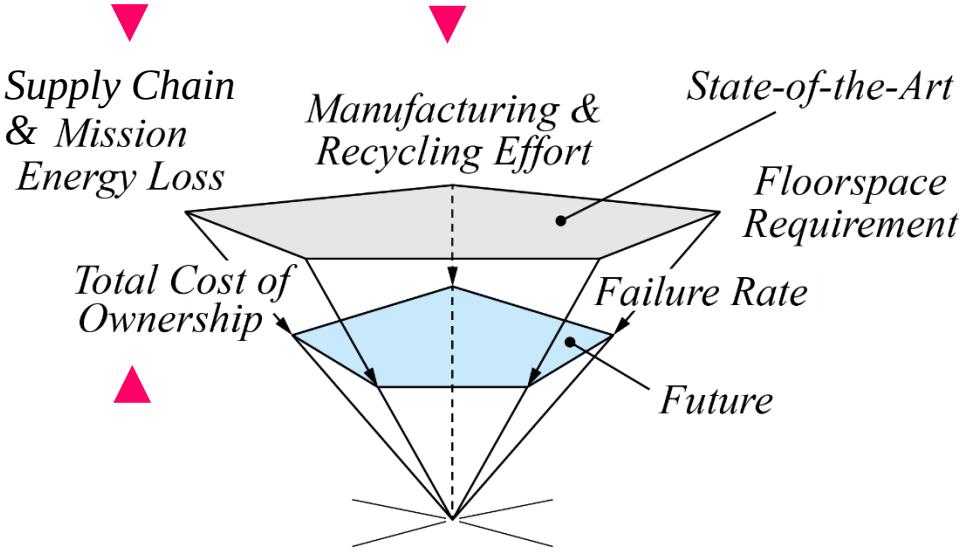
$$p(t) \quad \rightarrow \quad \int_0^t p(t)\,\mathrm{d}t$$

— Power Conversion → Energy Management / Distribution
— Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
— Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
— Cap. Filtering → Energy Storage & Demand Side Management
— Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
— etc.

▶ New Power Electronics Systems Performance Figures/Trends

■ **Complete Set of New Performance Indices**

- Power Density [kW/m^2]
- Environm. Impact [kWs/kW]
- TCO [$/kW]
- Mission Efficiency [%]
- Failure Rate [h^{-1}]



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[7] **P. A. M. Bezerra, F. Krismer, R. M. Burkart, J. W. Kolar,** *"Bidirectional Isolated Non-Resonant DAB DC-DC Converter for Ultra-Wide Input Voltage Range Applications,"* Proceedings of the IEEE International Power Electronics and Application Conference and Exposition (PEAC 2014), Shanghai, China, November 5-8, 2014.

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[9] **R. M. Burkart, J. W. Kolar,** *"η-ρ-σ Pareto-Optimization of All- SiC Multi-Level Dual Active Bridge Topologies with Ultra-Wide Input Voltage Range,"* IEEE Transactions on Power Electronics, submitted for review.

[10] **R. M. Burkart, C. Dittli, J. W. Kolar,** *"Comparative Life-Cycle-Cost Analysis of Si and SiC PV Converter Systems Based on Advanced η-ρ-σ Multi-Objective Optimization Techniques,"* IEEE Transactions on Power Electronics, submitted for review.

About the Speakers

Johann W. Kolar is a Fellow of the IEEE and is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 50 Ph.D. students. He has published over 650 scientific papers in international journals and conference proceedings and 3 book chapters, and has filed more than 120 patents. He received 21 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, and the ETH Zurich Golden Owl Award for excellence in teaching. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, Solid-State Transformers, Power Supplies on Chip, and ultra-high speed and bearingless motors.

Ralph M. Burkart received his M.Sc. degree in electrical engineering from the Federal Institute of Technology (ETH), Zurich, Switzerland, in 2011. During his studies, he majored in power electronics, electrical machines and control engineering. In the framework of his Master Thesis he designed and implemented a high-dynamic inverter system for active magnetic bearings in an ultra-high speed electrical drive system. Since 2011, he has been a Ph.D. student at the Power Electronic Systems Laboratory at ETH Zurich. His main research area is multi-domain modeling of power electronics components and multi-objective optimization of photovoltaic DC/DC and DC/AC converter systems employing SiC power semiconductors.

Thank You!

Questions