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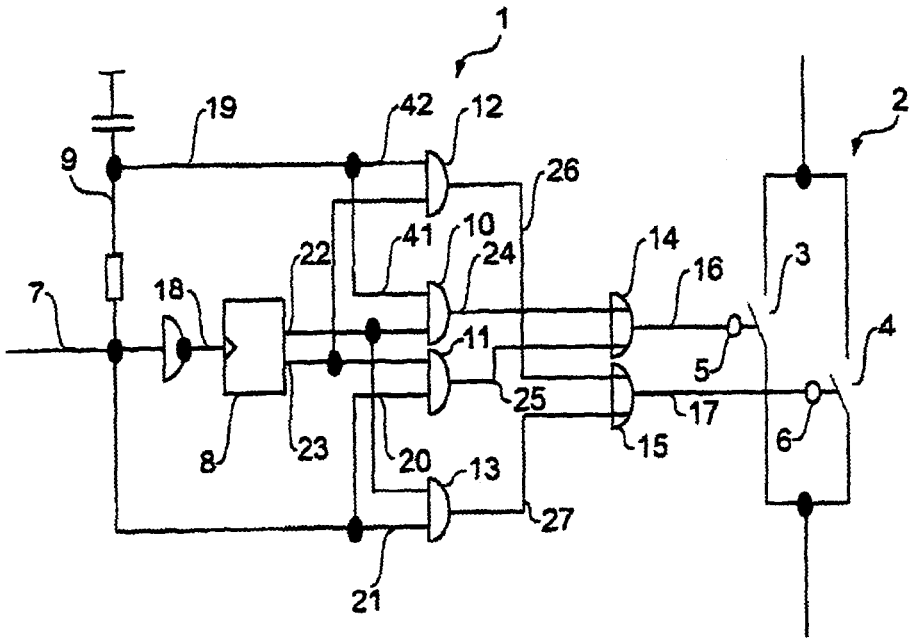
(54) Title: A METHOD AND APPARATUS FOR PARALLEL OPERATION OF ELECTRONIC POWER SWITCHES



(57) Abstract: The present invention relates to systems, methods and apparatus for the parallel operation of electronic power switches (3, 4) with negative temperature coefficient of the forward voltage or wide tolerance of the switching threshold voltages.

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A METHOD AND APPARATUS FOR PARALLEL OPERATION OF ELECTRONIC POWER SWITCHES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to systems, methods and apparatus for the parallel operation of electronic power switches with negative temperature coefficient of the forward voltage or wide tolerance of the switching threshold voltages.

Description of the Prior Art

Valves of power electronic systems of high power are realized frequently by direct parallel connection of single switches. A substantial limitation in this type of connection, however, is that stationary, as well as, dynamic symmetrical current division cannot be guaranteed.

In particular, when single switches show a negative temperature coefficient of the forward voltage, then, because of the spread of characteristic values of the components, a small difference in current division inevitably follows, which causes a relatively higher junction temperature for one switch. The consequence of this temperature rise is that the forward voltage decreases and the current loading increases for that switch. This positive feedback results in the switch taking over the total current for the connection and thus overloading.

Furthermore, for voltage-controlled power-semiconductors, different switching threshold voltages produce an asymmetrical division of the switching losses between the single switches. Traditionally, this asymmetry is overcome by increasingly complex current controllers and measurement of the single switch currents.

Thus, there is a need for a simple (*i.e.*, not complex) method, system and apparatus to provide control for the direct parallel single switches making up a valve, which creates a symmetrical division of the conduction and switching losses between the single switches.

SUMMARY OF THE INVENTION

The present invention relates to non-complex methods, systems and apparatus for controlling direct parallel single switches making up a valve, which create a symmetrical division of the conduction and switching losses between the single switches.

The basic idea of the invention is to create a stationary or dynamic symmetrical current division. This is accomplished by not impressing current simultaneously to the parallel single switches making up a valve, *i.e.* to turn them on in an alternating fashion rather than at the same time.

If a control signal for one valve, *e.g.* consisting of two single switches, exists, only every other turn-on signal is accepted from one single switch, during the conduction time, the other single switch is blocked. In fact, one switch is stressed with double current in comparison with ideal parallel operation, however, it is only driven with the half relative on time duration, which causes no difference in the conduction losses at current-independent constant forward voltage (as given, *e.g.*, for Isolated Gate Bipolar Transistors, "IGBTs") in comparison with ideal symmetrical simultaneous parallel operation. There is also no difference concerning the switching losses, based on the assumption that the switching energy loss is directly proportional to the switched current, which is achieved in practice with sufficiently good accuracy: every single switch is only switched with half pulse frequency and the permissible peak current load of a single switch is substantially higher than the current value occurring during symmetrical simultaneous parallel operation. An analogous expansion of the method to a higher number of parallel switches is possible in a simple way.

One embodiment of a method according to the invention to guarantee a symmetrical load of valves with forward voltage drop proportional to the current and positive temperature coefficient of the forward voltage (*e.g.*, power Metal Oxide

Semiconductor Field-Effect Transistors, "power-MOSFETs") comprises displacing the instants of switching time of the single switches relative to each other, but at least by the switching delay time and by the signal traveling time if a driver stage is provided. With that, the single switches take over the turn-on and the turn-off command alternately and they are stressed by turn-on switching power loss and turn-off switching power loss alternately. A simultaneous conduction of both switches does not cause any problems because of the positive temperature coefficient and the given self-stability of the current division.

If a control signal for the valve is given, *e.g.*, the first switch takes over the turn-on command directly and the second switch is turned on with a small time lag, and therefore without switching losses. The turn-off command is applied directly to the first switch, too, and to the second switch with a small time lag, so there are no turn-off switching losses for the first switch, the breaking and the turn-off switching losses are taken over by the second switch, respectively. At the following control signal the sequence of the control commands of both switches is reversed, *i.e.* the second switch is turned on directly according to the given turn-on command while the first switch is turned on with a small time lag, so the turn-on switching losses are carried by the second switch and the turn-off switching losses are carried by the first switch. Therefore, a symmetrical division of the turn-on and turn-off switching power losses on both switches is obtained. A symmetrical division of the conduction losses on both switches is guaranteed, because the time lag of the switching commands is usually substantially smaller than the on time duration of the switches and therefore basically both switches are in conducting state simultaneously. Because of the complete utilization of the silicon chip area available for current conduction the forward power losses are minimized. An analogous expansion of the method to a higher number of parallel switches is possible in a simple way, keeping the advantages with regard to the state of the art.

A further embodiment of the present invention comprises an apparatus for two parallel single switches, wherein the control signal of the valve is applied to a frequency divider (fed back master-slave flip-flop and toggle flip-flop, respectively), to the first input of a first AND-gate, assigned to the first switch, and to the first input of a second AND-gate, assigned to the second switch. For the following

considerations the "high"-level of the control signal shall be assigned to the turn-on state, and the "low"-level shall be assigned to the turn-off state. There are two outputs of the toggle flip-flop available always showing inverse logic levels. That output changing with a negative edge of the control signal from "low" to "high" remaining at this level for a whole pulse period of the control signal and changing with the following negative edge of the control signal to the "low"-level (halving of the frequency) is connected with the second input of the first AND-gate. The inverted output of the toggle flip-flop is connected with the second input of the second AND-gate. The output of the first AND-gate is used for controlling the first switch, the output of the second AND-gate is used for controlling the second switch, interposing a driver stage if necessary. Due to the AND-comparison with a signal with half pulse frequency for the first switch every second control pulse is gated out (the assigned output of the toggle flip-flop shows a "low"-level). Those gated out control pulses are executed by the second switch, its AND-gate is controlled by the inverted output of the toggle flip-flop, which is in conduction state while the first AND-gate is blocking. There results, that only every second control pulse is transmitted, the control pulses lying between the control pulses of the first switch are applied to the second switch. Both switches are alternating in on-state and in off-state, shifted by a half pulse period. For both switches there result equal conduction losses and equal switching losses, but problems according to simultaneous conducting and switching of direct parallel valves are avoided.

For a further embodiment of the present invention, one toggle flip-flop and one AND-gate for each switch is provided and the control information is transmitted alternating to a switch by appropriate gating of the control signal with the outputs of the toggle flip-flop, respectively. Furthermore, the control information is connected with a time-delay element with a delay time resulting from the switching lag time of the driver stage and from the lag time of the switches, the resulting slightly time-delayed control pulses are transmitted alternating to the first and second switch. AND-gates gate out every second time delayed control pulse again, the second inputs of the gates are connected with the outputs of the toggle flip-flop. The resulting control information for the first and second switch is each generated by an OR-gate.

The inputs of the first OR-gate, assigned to the first switch, are connected to the output of the first AND-gate and to the output of the additional provided AND-gate. The inputs of this AND-gate are connected to the time delayed control information and to the output of the toggle flip-flop, which controls the gate in such a manner that time delayed control pulses are placed between the control information of the first switch occurring with half pulse frequency. The generation of the control information of the second switch results analogous, by which every control pulse causes an immediately turn-on of the first switch and a slightly time-delayed turn-on of the second switch, the first switch is turned off immediately by a control pulse, whereas the second switch's turn off is time-delayed.

For this control pulse, the first switch carries the turn-on losses, the second switch carries the turn-off losses, and both switches take part at the current conduction simultaneously, with the exception of the time delay. Both switches change their part at the following control pulse, by which a symmetrical division of conduction losses and switching losses for both switches is guaranteed, and always the whole silicon chip area is available for conducting the valve current. When the time-delay element is left out and the AND-gate inputs, connect to the output of the time-delay element, are connected to ground ("low"), the apparatus may be programmable for applications wherein the switches have a positive temperature coefficient of the forward voltage or for applications with the need for slightly time-delayed switching. In both cases minimal conduction losses at resistive conducting-state characteristic of the switches shall be achieved.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description, serve to explain the principles of the invention.

Figure 1 shows the current configuration of a particular embodiment of the present invention.

Figure 2 shows the signal behavior over time for a particular embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to implementations of the present invention as illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used through the drawings and the following description to refer to the same or like parts.

As illustrated in Figure 1, the invention concerns methods and apparatuses for parallel operation of electronic power switches (3) and (4) with negative temperature coefficient of the forward voltage and/or wide tolerance of the switching threshold voltages. With the apparatus (1) according to the invention a control signal (7) applied by a preceding control unit is divided up into control signals (16) and (17) for the electronic switches (3) and (4). The clock input (18) of a toggle flip-flop (8) is connected with the inverted control information, and a signal (22) and an inverted signal (23), respectively, with half control frequency is generated. AND-operations (11), (13) and (10), (12) of one of the flip-flop-outputs with the control pulse (7) and the slight time-delayed control pulse (19), tapped off from the output of the time-delay element (9), respectively, gate out the even or the odd control pulses (the pulses shall be continuously and increasingly numbered with increasing time). The resulting auxiliary signals with half clock frequency are assembled by OR-gates (14) and (15), in such a manner that, *e.g.*, switch (4) is turned on at the beginning of an even control signal, and switch (3) turns on slightly time-delayed and loss-free, respectively, by the assigned pulse of the control pulse (19). On the other hand no turn-off losses are caused while turning off switch (4) at the end of the even control pulse, switch (3) takes over the valve current and turns it off slightly time-delayed. For the following and every odd control pulse, respectively, the facts are inverted: switch (3) is stressed by turn-on losses, and switch (4) is stressed by turn-off losses. Therefore, both switches are stressed symmetrically with turn-on and turn-off energy losses, and with sufficiently good approximation the silicon chip area of both switches (3) and (4) is available for current conduction during a full conduction interval of the valve (2), by which minimal conduction losses result.

In the following, the invention is explained with Figs. 1 and 2 in more detail. Fig. 1 shows the circuit configuration of the apparatus (1) for the control according to the invention of a valve (2) comprising direct parallel connection of two electronic switches (3) and (4) with control inputs (5) and (6). The control signal (7) generated by a preceding control unit is divided by the apparatus (1), which consists of a toggle flip-flop (8), a time-delay element (9) (in a simple way, the time-delay can be realized-by a RC-low pass in connection with the switching thresholds of subsequent gates), two AND-gates (10, 11) and (12, 13), assigned to the switches (3) and (4), an OR-gate (14), assigned to the switch (3), and an OR-gate (15), assigned to the switch (4). The divided up signal (16) and (17), occurring at the outputs of the OR-gates (14) and (15), is connected with the control inputs (5) and (6) of the electronic switches (3) and (4). The inverted control information (7) is connected with the clock input (18) of the flip-flop (8), *e.g.*, realized as known by NAND-gates, and connected by the time-delay element (9) with output (19) and directly with the inputs (20) and (21) of the AND-gates (11) and (13). The time-delayed control information (19) is connected with the inputs of the AND-gates (10) and (12). Furthermore, the output (22) (designated as "Q" in usual technical nomenclature) of flip-flop (8) is connected with the second inputs of the AND-gates (10) and (13) and the inverse output (23) ("$\overline{Q}$") of flip-flop (8) is connected with the second inputs of the AND-gates (11) and (12). The outputs (24) and (25) of the AND-gates (10) and (11) are connected with the inputs of the OR-gate (14), and the outputs (26) and (27) of the AND-gates (12) and (13) are connected with the inputs of the OR-gate (15).

The function of the apparatus according to the invention is explained by the signal time behaviors shown in Fig. 2. The signal behavior is designated by the related inputs and outputs of the components in Fig. 1. The control signal is generated by pulses (28, 29, 30, 31 etc.); the time-delayed control information (19) is also generated by pulses (32, 33, 34, 35, etc.).

Due to a negative edge (36) of the inverted control signal applied at the clock input (18) of flip-flop (8) the logic state of the flip-flop-output (22) changes from "low" to "high", and at the following negative edge (37) of signal (18) the state changes from "high" to "low", by which the generated signals at output (22) and at output (23) (inverse to output (22)) of flip-flop (8) occur with half frequency

compared with the control signal (7). Due to the AND-operation (10) of the time-delayed control information (19) and of the flip-flop-output (22) there results an auxiliary signal (24), where only every second pulse (32, 34, etc.) of the time-delayed control information (19) occurs, the odd pulses (33, 35 etc.) are gated out. Due to the AND-operation (11) of the flip-flop-output (23) and the not-time-delayed control information (7), the undelayed odd control pulses (29, 31 etc.) are transmitted to the output (25) and the even control pulses (28, 30 etc.) are gated out. With the OR-operation (14) of the outputs (24) and (25) of the AND-gates (10) and (11) there results a control signal (16) for the electronic switch (3), composed of even time-delayed control pulses (32, 34 etc.) and of odd undelayed control pulses (29, 31 etc.) lying in between the time-delayed pulses. The control signal (17) of the electronic switch (4) is generated in an analogous way by AND-gates (12) and (13) and the subsequent OR-operation (17) of the outputs (26) and (27) of the AND-gates (12) and (13), using the even undelayed control pulses (28, 30 etc.) and the odd time-delayed control pulses (29, 31 etc.) lying in between. Therefore, switch (4) is turned on with edge (36) (at the beginning of an even control pulse, in general), by which the turn-on of switch (3) at instant of time (38) is loss-free at sufficient time-delay. On the other hand, the turn-off of switch (4) at instant of time (39) is loss-free, the valve current is taken over by switch (3) and turned off at instant of time (40) with a slight time-delay. For the next control pulse (29) (and every odd pulse, in general) the facts are inverted: switch (3) shows turn-on losses and switch (4) turn-off losses. Both switches are stressed symmetrically with turn-on and turn-off energy losses, with sufficiently good approximation during every conducting interval of the valve (2) the silicon chip area of both switches (3) and (4) is available for current conduction, by which the minimal conduction losses are resulting.

If inputs (41) and (42) of the AND-gates (10) and (12) are not connected with output (19) of the time-delay element (9) but with ground, the time-delayed control signals (32, 34 etc.) contained in control signal (16) of switch (3) and the time-delayed control signals (33, 35 etc.) contained in control signal (17) of switch (4) are suppressed. Therefore, both switches are conducting alternately.

The present invention is not limited in scope by the specific embodiments described which are intended as single illustrations of individual aspects of the

invention. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. Method for symmetrical division of the conduction losses and of the switching losses of a valve (2) on the consisting direct parallel electronic switches (3) and (4): The control of the switches (3) and (4) occurs in such a manner that the current is not applied to the single switches at the same time, the switches are turned on alternately and not simultaneously. The given sequence of pulses for a valve has to be divided up to both single switches in such a manner that only every second turn-on command is taken over from a single switch, during the conduction state of one single switch the other switch has to be blocked, by which both switches are switched with half pulse frequency and driven with half relative on time duration.

2. Method for symmetrical division of the conduction losses and of the switching losses of a valve (2) on the consisting direct parallel electronic switches (3) and (4). The instants of switching time of the single switches (3) and (4) are slightly displaced relative to each other, but at least by the switching lag time and by the time delay of a possible driver stage, in a way, that the single switches (3) and (4) take over the turn-on and the turn-off of the valve (2) alternately and are stresses by turn-on and turn-off energy losses alternately, respectively. Basically they are involved in the conduction of the total current simultaneously. *E.g.*, the first switch is turned on by a first (and odd in general, respectively) control pulse given for the valve, the second switch is turned on with a slight time delay. The first switch is stressed by the total turn-on losses, the second switch is turned on without any switching losses. The control pulse for turning off is applied directly to the first switch and time-delayed to the second switch, by which there are no turn-off losses are caused for the first switch and the second switch takes over the turn-off and is stressed by the total turn-off losses, respectively. For the following (and even in general, respectively) control pulse the order of control is inverted for both switches: the second switch is turned on directly by the control signal given for the valve, while the first switch is turned on with a slight time delay, by which the second switch is stressed by the turn-on losses and the first switch is stressed by the turn-off losses. With that, a symmetrical division on both switches of the turn-on and turn-off energy losses and because of

approximately simultaneous conduction of the switches of the conducting losses is achieved.

3. Apparatus for practical implementation of the method according to claim No. 1 for two parallel single switches (3) and (4): The control signal (7) of valve (2) is connected with the input of a frequency divider, with the input of an AND-gate, assigned to the first switch (3), and with the input of an AND-gate, assigned to the second switch (4). The "high"-level of the control signal (7) is assigned to the on-state, whereas the "low"-level is assigned to the off-state. At the output of the toggle flip-flop there are always two inverse levels available, the output changing with a negative edge of the control signal from "low" to "high", staying at this level for a pulse period of the control signal, and changing to the "low"-level with the following negative edge of the control-signal is connected to the second input of the first AND-gate, while the inverted output of the toggle flip-flop is connected to the second input of the second AND-gate. The output of the first AND-gate controls the first switch, and the output of the second AND-gate controls the second switch, subsequently connected to a driver stage if necessary. For the first switch every second control pulse is gated out by the AND-operation with a signal with half pulse frequency, the gated out signals for switch (3) are executed by switch (4), the AND gate assigned to switch (4) is controlled by the inverted output of the toggle flip-flop, so if the AND-gate assigned to switch (3) is blocking, the AND gate assigned to switch (4) is in on-state. Thereby only every second control pulse is transmitted to switch (3), the control pulses lying in between the control pulses of switch (3) are applied to switch (4), by which both switches are in on-state and off-state alternately and are stressed by equal conducting and switching losses.

4. Apparatus (1) for practical implementation of the method according to claim No. 2: The control signal (7) generated by a preceded control unit is divided up into control signals (16) and (17) for the electronic power switches (3) and (4). The inverted control information (7) is connected with the clock input (18) of a fed back master-slave and toggle flip-flop (8), respectively, realized by NAND-gates as known, and besides that connected with a time-delay element (9) with the output (19) and

connected direct with the inputs (20) and (21) of the AND-gates (11) and (13). The time-delayed control information (19) is connected with one of the inputs of each AND-gate (10) and (12). The output (22) of flip-flop (8) is connected with the second inputs of the AND-gates (10) and (13), while the inverted output (23) of flip-flop (8) is connected with the second inputs of the AND-gates (11) and (12). The outputs (24) and (25) of the AND-gates (10) and (11) are connected with the inputs of the OR-gate (14), the outputs (26) and (27) of the AND-gates (12) and (13) are connected with the inputs of the OR-gate (15). With this, with the control signal (7) consisting of pulses (28, 29, 30, 31, etc.) and pulses (32, 33, 34, 35, etc.) assigned to the time-delayed control information (19) a control signal (16) for the electronic switch (3) is generated, consisting of even time-delayed control pulses (32, 34, etc.) and odd undelayed control pulses (29, 31, etc.) lying in between. For switch (4) a control signal (17) is generated, consisting of even undelayed control pulses (28, 30, etc.) and of odd time-delayed control pulses (33, 35, etc.) lying in between. Due to this both switches are stressed symmetrically by equal turn-on and turn-off switching energy losses, and with sufficiently good approximation the silicon chip area of both switches (3) and (4) is available for current conduction during a full conduction interval of the valve (2), by which minimal conduction losses result. If the inputs (41) and (42) of the AND-gates (10) and (12) are disconnected from output (19) of the time-delay element (9) and connected with ground and logical "low", respectively, the function of the apparatus (1) corresponds to the function according to claim No. 3. Thereby, with an external switching circuit of low complexity the function of apparatus (1) at integrated implementation is programmable for applications according to claim No. 1 or No. 2.

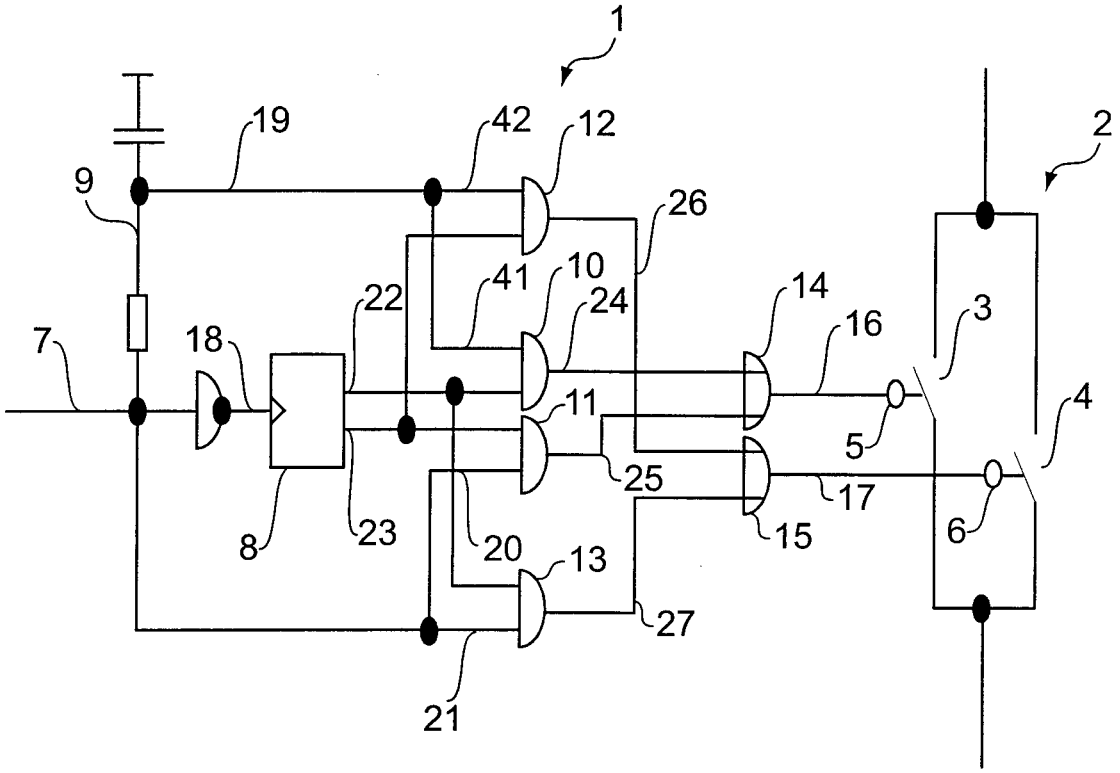

FIG. 1

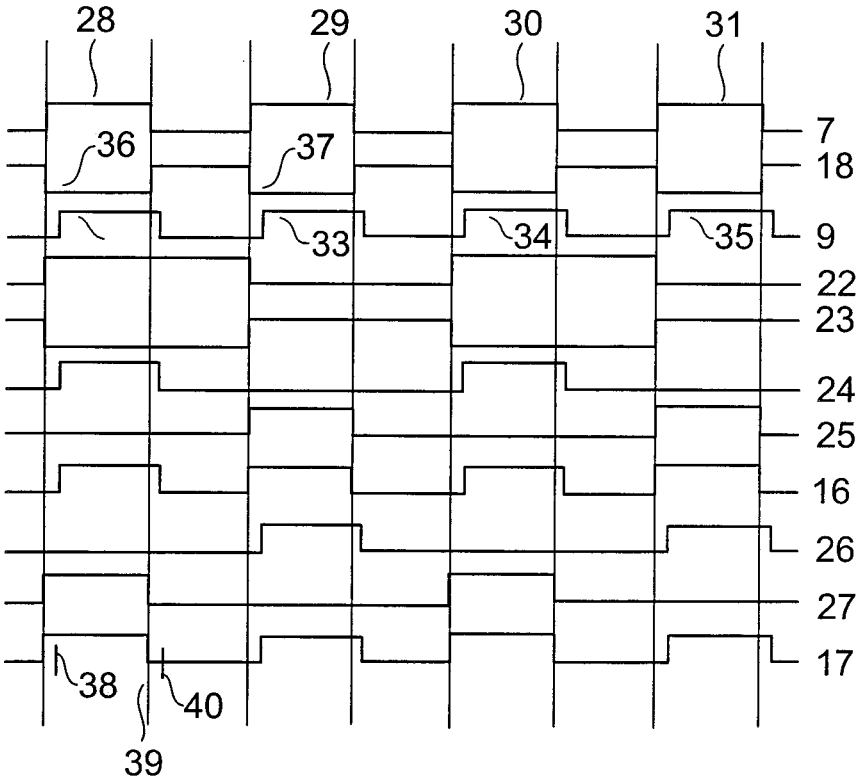

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB00/00656

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H03K 17/62
US CL : 327/365, 403

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,534,815 A (BADYAL) 09 July 1996 (09.07.1996), Fig. 2A.	1-4

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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