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ULTRA–HIGH PERFORMANCE TELECOM DC–DC CONVERTER

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*For my parents
Sieglinde and Jürgen*

Telecommunication and data provision are cornerstones of our modern society. The evolution of the multimedia network around the world started more than one century ago and, as a consequence, the power supplies for the telecom facilities and the parallel-emerging data centres passed through the entire evolution of power electronic systems. Telecom facilities and data centres have started to merge with the digitalisation of the telecom networks. Ever since the following internet boom in the nineties of the last century, the demand on a high-performance data storage, transmission, and computation is rapidly increased. Concurrently, the demanded performance of the modules in the power supply chain and the Information and Communication Technology (ICT) equipment has severely increased. The development of highly compact converter systems counteract the increased demand on space for the ICT-equipment and additionally enables a more-efficient cooling in the data centres. The continuous expansion of digital networks and data centres, as well as the increasing energy prices and the advanced environmental awareness result in shifting drivers for the power-supply development towards an efficient energy transmission and distribution, whereas the power density of the system should remain on a high level.

In this thesis, the limits for the power density and efficiency for DC-DC converters as part of the power supply chain in data centres or telecommunication facilities is investigated. Based on comprehensive analytical thermal, electrical, and magnetic models, the system performance is calculated with the selected free design parameters. Furthermore, these analytical models provide the basis for an automated determination of the optimal design parameters with respect to the maximum power density and/or the maximum efficiency.

Based on the examples of a series-parallel-resonant converter and a phase-shift pulse-width-modulated DC-DC converter with current doubler rectifier, the analytical determination of the maximum power density based on an optimisation algorithm is explained in detail in chapter 2. With the resulting optimised design parameters, the corresponding prototype systems are realised with which the applied analytical models are validated. Moreover, an almost loss-less snubber circuit for the hard-switched rectifier elements of general phase-shift converters is presented, which detracts the ringing energy from the core of the magnetic components and provides this energy for further utilisation.

In addition, a phase-shift pulse-width-modulated DC-DC converter

with centre-tapped transformer and second-order output filter is optimised with respect to energy efficiency. The optimisation objective is a load-dependent efficiency profile with a maximum efficiency of 99 %. The analytical models, the realised prototype, and the model-validation measurements are detailed in chapter 3. Moreover, the sensitivities of the component parameters on the resulting system performance are investigated. Finally, the influence of the model accuracy on the optimal design parameters is evaluated in chapter 4, and an outlook on further steps in research is given.

Telekommunikation und die Bereitstellung von Daten jeglicher Art sind Grundsteine unserer modernen Gesellschaft. Die Evolution der multimedialen Vernetzung der Erde begann vor mehr als einem Jahrhundert und somit durchliefen die Spannungsversorgungen für die Telekommunikationseinrichtungen und die zunächst parallel aufkommenden Rechenzentren die vollständige Evolution leistungselektronischer Systeme. Mit der Digitalisierung der Telekommunikationsnetze begannen die Telekommunikationseinrichtungen und Rechenzentren zu verschmelzen. Seit dem darauffolgenden Internet-Boom in den neunziger Jahren des letzten Jahrhunderts stieg der Bedarf an einer hoch-leistungsfähigen Datenübertragung, Datenspeicherung und Datenverarbeitung rasant an. Gleichzeitig stieg die Performanceanforderung an die Module der Spannungsversorgungskette und des Datenverarbeitungsequipments massiv an. Die Entwicklung hoch-kompakter und hoch-effizienter Umrüster wirkt dem gestiegenen Platzbedarf des Datenverarbeitungsequipments entgegen und ermöglicht darüber hinaus eine effizientere Kühlung der Rechenzentren. Der anhaltende Ausbau der digitalen Netze und Rechenzentren sowie die steigenden Energiepreise und das erhöhte Umweltbewusstsein verlagern die Zielsetzung bei der Entwicklung moderner Spannungsversorgungen hin zu einer effizienten Energieübertragung und -verteilung, während die Leistungsdichte auf einem hohen Niveau gehalten werden soll.

In der vorliegenden Arbeit sind die Grenzen der Leistungsdichte und Energieeffizienz für Gleichspannungswandler als Teil der Energieübertragungskette in einem Rechenzentrum oder in einer Telekommunikationseinrichtung untersucht. Basierend auf umfangreichen analytischen thermischen, elektrischen und magnetischen Modellen wird die Systemperformance mit der Vorgabe der freien Designparameter berechnet. Diese Modelle bilden des Weiteren die Grundlage für eine automatisierte Berechnung der optimalen Designparameter in Hinblick auf die maximale Leistungsdichte und maximale Effizienz.

Am Beispiel eines Serien-Parallel-Resonanzwandlers und eines pulsweitenmodulierten Gleichspannungswandlers mit Stromverdoppler-Gleichrichterschaltung ist die analytische Berechnung der maximalen Leistungsdichte in Kapitel 2 mithilfe eines Optimierungsalgorithmus im Detail erklärt. Auf Basis der berechneten optimalen Designparameter werden entsprechende Prototypen realisiert und die angewendeten analytischen Modelle experimentell validiert. Darüber hin-

aus wird eine quasi-verlustfreie Entlastungsschaltung für die hart-geschalteten Gleichrichterelemente von pulsweitenmodulierten Gleichspannungswandlern präsentiert, welche die Schwingungsenergie aus dem Kern der magnetischen Komponente entzieht und zur weiteren Verwendung zur Verfügung stellt.

Des Weiteren ist ein pulsweitenmodulierter Gleichspannungswandler mit Zwei-Wicklungstransformator und einem Ausgangsfilter zweiter Ordnung in Hinsicht auf Energieeffizienz optimiert. Das Optimierungsziel ist eine maximale Effizienz von 99 % unter weiterer Berücksichtigung der Teillast-Effizienz. Die analytischen Modelle, der realisierte Prototyp sowie die Validierungsmessungen sind im Detail in Kapitel 3 präsentiert. Darüber hinaus werden die Sensitivitäten der resultierenden Performance bezüglich der Komponentenparameter untersucht. Der Einfluss der Modellgenauigkeit auf die optimalen Designparameter wird in Kapitel 4 evaluiert und ein Ausblick auf weitere Forschungen gegeben.

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1

The Challenge of a High-Performance Design An Introduction

The evolution of power electronic systems has now been going on for a century and the exact start, in accordance with the definition of power electronics¹ might be in 1911, when E. F. W. Alexanderson of the General Electric Company (GE) filed a patent application for modulating the current from a high frequency alternator [1, 2]. Alexanderson described a 72 kW magnetic amplifier circuit for radio telephony [3], in today's literature commonly named saturable reactors and transducers, which enabled the transatlantic communication between the United States of America and Europe soon afterwards.

In the 1920's there was a rapid development of vacuum tubes, followed shortly afterwards by gas and vapour filled tubes (thyratrons and ignitrons) [1]. In 1930 the New York Subway installed 3 MW grid-controlled mercury-arc rectifiers for DC-motor traction and mercury-arc cycloconverters for universal motor traction were introduced on German railways one year later [4]. Gas and vapour filled tubes were widely used until the mid-1960s.

The principle operation of semiconductor switching devices was described and patented by J. E. Lilienfeld for a Field Effect Transistors (FET) in 1925 in Canada and one year later in the U.S.A. [5]. In 1948, J. Bardeen, W. Brattain and W. Shockley of the Bell Laboratories in-

¹"Power electronics is the technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form." [1]

vented the point-contact transistor, shortly followed by the junction transistor in 1951 [1, 4]. The revolution of silicon power electronic devices started with the introduction of GE's Silicon Controlled Rectifier (SCR), known since the 1960's as a thyristor, which initialised the step from the gas and vapour filled tubes S-curve [6] to the power semiconductors S-curve. A major step in the development process occurred in the 1970's with the introduction of a giant transistor for DC-motor drives around 1975, a power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in 1978, the high power Gate Turn-Off thyristor (GTO) in 1980 and finally the Insulated Gate Bipolar Transistor (IGBT) in 1983 [1, 4]. The era of modern power electronics had begun.

Since the 1970's power semiconductor devices have greatly improved. Besides higher voltage and current ratings, new device materials have been introduced, e.g. silicon carbide (SiC) and gallium nitride (GaN), allowing e.g. higher junction temperatures and smaller on-resistances or faster switching, respectively. The weight of power electronics modules was reduced by factor of more than eight from 1975 to 1998; the footprint size has been reduced by 40 % and the number of solder layers has been reduced from five to one thereby increasing reliability drastically [7]. In the same time the on-resistance of power MOSFETs (e.g. 50 V, Infineon) has been halved [7]. Major advances in power electronics have been mostly based on the improvement steps of power semiconductor devices.

The advances in semiconductor devices will retain its major influence in power electronics in future, however, in consequence of the interdisciplinarity of power electronic systems, environmental, economic and social changes will largely determine the performance drivers of power electronic systems in future. In the next section, an introduction of the most important performance indices and trends of power electronic systems will be given, followed by an abstract perspective on the modulation of the mapping function connecting the available design space with the obtainable performance space in section 1.2. In the ever growing number of telecommunication facilities and data centres the performance of power electronic systems has a major influence on their economic and ecological characteristics. The construction and design challenges as well as the improvement prospects of the facilities subsystems are introduced and discussed in section 1.3. In the power supply chain for the actual load in data centres and telecom facilities – the Information and Communication Technology (ICT) equipment – the

performance of the power supply unit has a major impact on the total facility performance. Independent on the facility DC-DC converters are necessarily applied in this supply chain. Suitable topologies for telecommunication DC-DC converters are discussed in section 1.4 at the end of this chapter.

1.1 Performance Indices of Power Electronic Systems

With the beginning of modern power electronics after the power semiconductor revolution new dimensions have been enabled and added to the research fields. Power electronics research has shifted from enabling the technology itself to orientating on the system performance, which is quantified by performance indices. The manufacturers of power supplies are usually the suppliers of Original Equipment Manufacturers (OEM) which are influenced themselves by their customers – the actual end-users – and their demands are passed back to the power supplies manufacturers. For that reason, the research and development departments (R&D) are barely technology driven - rather technology-responsive [8]. The resulting most important R&D drivers and performance indices, respectively, are the system cost, losses, volume, weight and failure rate as illustrated in **Fig. 1.1**. The *ideal* power supply for the consumer can be found in the centre of the performance diagram, there the equipment is of zero costs, operates without losses, is infinitesimal small/light and is operating without maintenance effort forever. Even though this utopian wish can't be fulfilled, innovations and improvements in power electronics are clearly enabling big steps towards the centre of the performance diagram in **Fig. 1.1**.

The performance indices are commonly normalized in order to allow the characterization of a system independent of nominal values, i.e. integral properties of the converter are evaluated with relative quantities [9], e.g. the volume referred to the output power. The most commonly used normalized performance indices resulting from the performance drivers in **Fig. 1.1** - power density, efficiency, output power per unit weight, relative costs and mean time between failures - are introduced in the following.

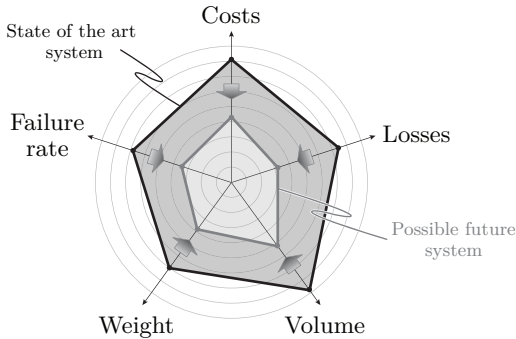


Figure 1.1: Graphical representation of the performance indices for state of the art and future systems.

Power Density The commonly used relative representation of the system volume or compactness is the power density ρ , the ratio of rated output power P_{out} to the system volume V_{sys} ,

$$\rho = \frac{P_{\text{out}}}{V_{\text{sys}}} \left(\frac{\text{kW}}{\text{dm}^3}, \frac{\text{kVA}}{\text{dm}^3} \right); \quad (1.1)$$

$1 \text{ kW/dm}^3 = 1 \text{ kW}/\ell = 1 \text{ W/cm}^3 \cong 16.4 \text{ W/in}^3$ and $100 \text{ W/in}^3 \cong 6.1 \text{ kW/dm}^3$. Alternatively, a power density could be declared with respect to partial volumes, for instance magnetic devices, heat sinks or an auxiliary supply, and the nominal output power could be the replaced by the maximum output power, if different, and the partial-volume respective power.

The power density has been one of the most important drivers for power electronics for the last decades and in the course of miniaturisation still has a high significance. As an example the pursuit on high-power-density telecom Power Supply Units (PSU) can be observed in consequence of the continuously increasing demand on data centres and telecommunication facilities. In fact, until some years ago the Capital Expenditure (CapEx) for data centres have been measured on the occupied cross-section area [10] and power density has been figured out as most important performance index for power electronics roadmaps [11].

The system size and consequently the power density are mainly determined by the heat sinks and the passive circuit components, such as

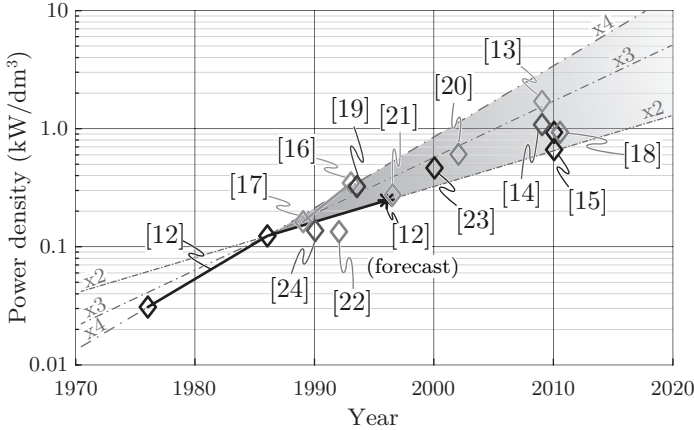


Figure 1.2: Power density ρ of realised telecom Power Supply Units (PSU). (Rectified output voltage $V_{\text{out}} = 46..56$ Vdc; output power $\approx 1..10$ kW)

capacitors and inductors. The innovations and improvements of power semiconductors, allowing higher switching frequency and lower conduction and switching losses, have mainly enabled a considerable system volume reduction. An increase of the switching frequency by a factor of 10 can result in an increase of the power density by factor of 1.5 to 2 [12, 25]. Some power density milestones are presented in **Fig. 1.2** for telecom PSUs which are utilised to rectify the single- or three-phase supply voltage of the mains into a DC-output voltage V_{out} typically between 46 and 56 V.² Considering the mid-eighties power density of $\rho \approx 0.12 \text{ kW/dm}^3$ as origin [12], three straight lines are plotted in the diagram for the following investigations, identifying the doubling, tripling and quadrupling of the power density within a decade (marked with x2, x3 and x4, respectively, in **Fig. 1.2**). As presented in [12], the power density has been quadrupled from 1976 to 1986 and the forecast, which showed a further doubling until 1996 (marked with a “*”) has been later proved by [21]. An even higher increase as the predicted doubling of the system power-density in that decade has been shown by [17] (approx. tripling) and even the continuation of the quadrupling-trend in the previous decade has been featured by the rectifier systems presented

²More detailed specifications can be found in section 1.3.

in [16, 19].

Right after the millennium-turn, the power densities of realised PSUs have been approximately on the tripling-trend line considering the origin in the eighties (e.g. [20, 23]). At the end of the first decade of the 21st century, the power density of applied telecom PSUs can be found between the doubling and the tripling trend line (e.g. [13–15, 18]). A continuation of the quadrupling-trend appears to be difficult, on one hand because a power-density-increase is besides the improvements and innovations of the power semiconductor industry also depending on the advancements of the passive components, which could be observed only to a minor degree in the last decades [8]. On the other hand, the focus of the development and research of power electronic systems is not merely on a single performance index as the power density, but rather on multiple performance indices at the same time, allowing for instance smaller costs while accepting a smaller power density conversely. The identification of the theoretical power-density barrier, i.e. the limit of power density when only focusing on this single performance index, is one of the major parts of this thesis presented for telecom DC-DC converter systems in chapter 2.

Efficiency The market for switching power supplies has grown with the raising market for desktop computers and the global network; and still, the annual investment growth forecast e.g. for telecom and data-com power supplies over a power range of some watts to several kilowatts is higher than 15 % [26]. At the same time, the demand on electric energy has grown as well and power electronics is becoming the key technology for a more sustainable generation, distribution and use of electric energy. Besides the ecological aspects, power electronics development and research is strongly driven by economic considerations. This progression is shown clearly for instance for telecom and data centre PSUs: until some years ago, it took 20 to 30 years until the costs for powering and cooling have been equal to the purchasing cost of the PSU [10]. However, because of the falling prices for power electronic equipment and the contrary increasing energy prices, the operating costs exceed the hardware costs nowadays in less than two years [10]. This leads to a move towards the development of more efficient power supplies. Consequently, besides power density, the system efficiency η is one of the most important physical performance indices to characterise a power

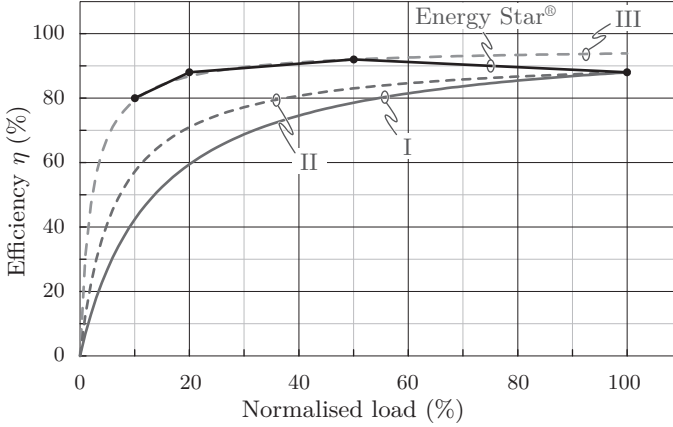


Figure 1.3: System efficiency in dependency of the relative rated output power $P_{\text{out}}/P_{\text{out,N}}$ as proposed in the Energy Star® requirements for computer servers [27]. I: efficiency graph of a system with constant losses over the entire load range; II+III system with constant and load-dependent losses.

electronic system,

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \left(1 + \frac{P_{\text{loss}}}{P_{\text{out}}}\right)^{-1} \approx 1 - \frac{P_{\text{loss}}}{P_{\text{out}}}, \quad (1.2)$$

with the system input power P_{in} , the output power P_{out} , and the total system losses P_{loss} .

The system efficiency is usually specified for the rated output power ($P_{\text{out}} = P_{\text{out,N}}$). However, in several fields of application converter systems are frequently not only operated at full load and in consequence the corresponding efficiency specifications and regulations are specified together with part-load efficiencies, e.g. $\eta_{10\%}$, $\eta_{20\%}$, $\eta_{50\%}$ and $\eta_{100\%}$ as proposed in the Energy Star® requirements for computer servers [27]. In **Fig. 1.3** the suggested required part-load efficiency values for computer server power supplies (single output, AC-DC & DC-DC) are illustrated for a rated output power higher than 1 kW regarding Energy Star® [27].

A power supply system with constant losses over the entire load range and with a full-load efficiency similar to Energy Star®, i.e. $\eta_{100\%} = 88\%$, cannot accomplish the required part-load-efficiency as

illustrated in **Fig. 1.3** (marked with I). Neither the system II can fulfil the requirements whose total losses are the sum of constant and load-dependent losses linearly decreasing with the output power³, although the part-load efficiency could be improved and is more realistic regarding to a physical system. In order to meet the part-load efficiency requirements, the constant system losses can only have a minor share of the total losses, as e.g. shown for the efficiency graph of system III⁴ in **Fig. 1.3**. That implicates that low-power consumers, e.g. the digital control and the auxiliary supply, have to be thoroughly considered during the design process of high-efficiency power supplies. Moreover, these and further subsystems consuming an almost fixed amount of power even though the converter systems is not transmitting energy to the output if no load is applied. As a result of these fixed losses – also called shunt, no-load, tare or parallel losses – an efficiency curve starts at zero at no-load as illustrated in **Fig. 1.3**.

Alternatively to the specification of discrete efficiency points, the mean efficiency over the output power range could be applied as, for instance, for photovoltaic inverters [28] or, with the knowledge of the mission/load profile, the more precisely specifying Mean Mission Efficiency [9, 29]. In order to enable a direct calculation of the required cooling effort and heat emissions, respectively, the relative losses are calculated to characterise the power electronic system [9],

$$\frac{P_{\text{loss}}}{P_{\text{out}}} = \frac{1 - \eta}{\eta}. \quad (1.3)$$

For big systems like data centres, which consist of several subsystems ensuring the system energy balance, the Power Usage Effectiveness (PUE) as suggested e.g. in [30] could appropriately be applied to describe the system efficiency,

$$\text{PUE} = \frac{P_{\text{fac}}}{P_{\text{ICT}}}, \quad (1.4)$$

with the total power delivered to the facility P_{fac} and the power supplied to the intrinsic load P_{ICT} which is in this case the ICT-equipment.

³The constant losses of system II equal the load-dependent losses at 100 % output power and the total losses are $\eta_{100\%}=88\%$, similar to Energy Star®.

⁴System III shows constant and load-dependent losses which are equal at 50 % load and the sum of both is equal to $\eta_{50\%}=92\%$, similar to Energy Star® at this point.

As indicated before, the efficiency is more and more in the focus for power electronics development and research which leads to higher efficiency converter systems on the market. As the power density, the efficiency is strongly coupled to other performance indices and higher system efficiency can besides components and topology advances only be achieved with e.g. more volume and weight as well as higher cost. Because of the major importance, chapter 3 is dedicated to the identification of the interdependency and limits of the system efficiency of telecom DC-DC converter systems, the second major aspect of this thesis.

Output Power per Unit Weight The system weight W_{sys} is barely investigated in literature at the moment, however, in the course of evolution towards Electric Vehicles (EV), More Electric Aircraft (MEA) and for several other fields of applications - especially in the area of mobility - the weight of the required power electronic system is important, because of the direct coupling between system weight and energy consumption. As the result of this coupling and the increasing awareness concerning energy consumption a weight-regarding normalised performance index, i.e. the output power per unit weight, γ [9],

$$\gamma = \frac{P_{\text{out}}}{W_{\text{sys}}} \left(\frac{\text{kW}}{\text{kg}}, \frac{\text{kVA}}{\text{kg}} \right), \quad (1.5)$$

has to be considered in future system designs.

Relative Costs The market for power electronic systems is mainly driven by the requirements of the end user. The literature agrees on identifying the system costs as the most powerful driver for the market, e.g. [8, 26, 31–33]. More than 77 % of OEMs in the field of power supplies named costs as the most important non-product power supply vendor selection criteria [8]. As a result, the manufacturing costs have been reduced for instance by 30 % per electronic function and year in the power semiconductor industry [32]. The power that can be installed for a given system price C_{sys} ,

$$\sigma = \frac{P_{\text{out}}}{C_{\text{sys}}} \text{ e.g. } \left(\frac{\text{kW}}{\text{€}} \right), \quad (1.6)$$

can be used as normalized performance index to specify the system [9].

Mean Time Between Failures (MTBF) Nearly 41 % of OEMs identify reliability as an important product selection criteria for power supplies [26]. The reliability requirements are usually specified in the form of a Mean Time Between Failure (MTBF) [34], the inverse of the random failure rate λ ,

$$\text{MTBF} = \frac{\int_0^T R_T(t)dt}{1 - R_T(t)} = \frac{1}{\lambda}, \quad (1.7)$$

with the reliability function $R_T(t)$ and the point in time T . The reliability model for the applied system components, e.g. for power modules [35, 36], are commonly complex and challenging to establish. Moreover, a power electronic system often contains several hundred models aggravating the computation of the integral. An approximation as e.g. proposed in [34] could be applied in this case.

Power density, efficiency, output power per unit weight, relative costs, and mean time between failures - all five performance indices which influence the design of power electronic systems are approaching the costumer's demands and specifications. The resulting system performance is consequently a trade-off between different target whereas in special applications certainly the highest possible value of a specific performance index might be claimed. Moreover, for roadmaps and future research and development orientations of OEMs, the examination and knowledge of the limit of a single performance index is the corner stone. In this thesis the two, for telecom power supplies most important non-product performance indices – power density and efficiency – are investigated in order to identify the highest possible performances for this type of power electronics system. The principle approach to obtain these limits is explained in the following section.

1.2 Design for Highest Performances

The performance of a power electronic system depends on the system design, i.e. the determination of possible design parameter which results in the required system performance. The key for investigating the performance is consequently the exploration of the subordinate levels of a power electronic system and the therein contained elements. In order to obtain the highest performance, the system elements have to be

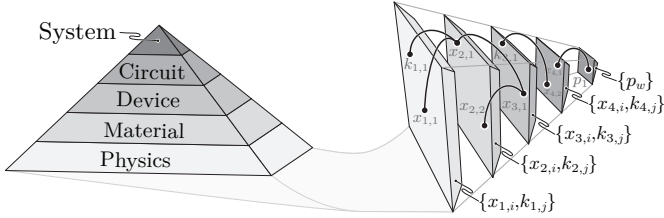


Figure 1.4: Levels of a power electronic system.

defined in the way that the optimum performance related to a specified optimisation criterion is accomplished.

From a hierarchical perspective a power electronic system can be divided into five technology levels [32]: fundamental physics - material - device - circuit - system. Each level provides the basis for the next level above and the respective lower level forms the design space of the respective next higher level(s). The free design parameters \vec{x} and constants \vec{k} , which configure the design space, enable a specific performance \vec{p} in the next level above as illustrated in **Fig. 1.4**.

For instance, with Ohm's law, e.g. $x_{1,1}$, and the resistivity of the material copper, e.g. $k_{1,1}$, of the fundamental physics level, the electrical DC-resistance, e.g. $x_{2,1}$, is defined as function of the cross-section area, e.g. $k_{2,1}$, and length, e.g. $k_{2,2}$. The material can be used as bus bars, e.g. $x_{3,1}$ in the device level, for interconnecting two circuit elements, e.g. $x_{4,1}$ and $x_{4,1}$, and thus has an influence on the system performance, e.g. p_2 , which could be assigned to the converter efficiency η .

The elements of the single level have theoretical and practical limits which are partly almost fix; for instance the laws of physics are changing very rarely. On the other side, limits might change very rapidly – for instance because of new technological inventions and economical rethinking, respectively. Either way, the limits of each level-element have to be considered in the performance analysis for authentic results.

If the performance exploration is concentrated on the entire power electronic system rather than single devices or materials, the four lower levels (fundamental, material, device, circuit) can be summarized to the design space - the basis for enabling the power electronic system⁵. The resulting summarized free design parameters $\vec{x} = (x_1, x_2, \dots, x_n)$ have to be determined during the system design process and a specific system

⁵The following variable names refer to the designators proposed in [9, 37, 38].

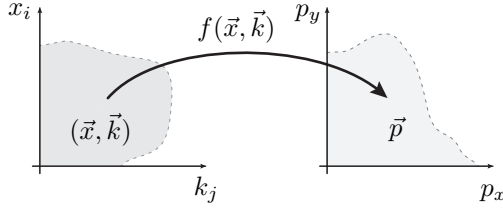


Figure 1.5: Mathematical perspective of mapping the design space to the performance space of a power electronic system.

performance $\vec{p} = (p_1, p_2 \dots p_m)$ results.

During the conventional design process, the design parameters \vec{x} are determined based on the performance requirements $\vec{r} = (r_1, r_2 \dots r_s)$ and design constants $\vec{k} = (k_1, k_2 \dots k_l)$. The design parameters \vec{x} , performance requirements \vec{r} , and constants \vec{k} are related together with the design constraints $g_i(\vec{x}, \vec{k}, \vec{r}) = 0$. Because of the complexity of the power electronic system, the number of design variables \vec{x} exceeds the number of design constraints g_i resulting in an extremely large number of sets of possible solutions for the design variables \vec{x} satisfying the requirements \vec{r} and constraints g_i . However, an optimum performance regarding one or more performance indexes $p_{w, \text{opt}}$ ($w = 1, 2 \dots m$) is generally not obtained with that design approach.

For a performance-specific exploration of the power electronics system design a mathematical description $f(\vec{x}, \vec{k})$ is necessary to map the design space consisting of the free and constant design parameters (\vec{x} and \vec{k}) to the performance space \vec{p} , as illustrated in **Fig. 1.5** [9, 38]. The feasible design space is constituted by the physical and theoretical limits of the containing elements and the constraint functions g_i and h_j ,

$$g_i(\vec{x}, \vec{k}, \vec{r}) = 0, \quad i = 1, 2, \dots p, \quad (1.8)$$

$$h_j(\vec{x}, \vec{k}, \vec{r}) \geq 0, \quad j = 1, 2, \dots q, \quad (1.9)$$

which describe e.g. performance requirements and specifications, inner system states and limits. The resulting performance space is consequently limited as well and the optimum design related to a performance index p_w ($w = 1, 2 \dots m$) is obtained if the mapping function

$f(\vec{x}, \vec{k})$, defined as optimum design criterion, is maximal,

$$f(\vec{x}, \vec{k}) \rightarrow \max. \quad (1.10)$$

If for instance the power density ρ of a power electronic system at the nominal output power P_{out} is defined as performance index p_1 , and the highest possible value for $p_1 = p_{1,\text{max}}$ is the aim of the system design considering the side conditions (g_i and h_j), the mapping function $f(\vec{x}, \vec{k})$ describes the sum of the n volume-contributing elements V_i ($i = 1 \dots n$) of the examined system,

$$f(\vec{x}, \vec{k}) = \frac{\sum_{i=1}^n V_i}{P_{\text{out}}}. \quad (1.11)$$

The optimal design parameters \vec{x}_{opt} can be obtained by applying an automatic optimisation procedure varying the free design parameters x_u until the highest feasible performance for p_1 ,

$$p_1 = p_{1,\text{max}} = f(\vec{x}_{\text{opt}}, \vec{k}),$$

results. This system design approach has been successfully applied for ultra-compact and high efficiency telecom DC-DC power supplies as described in chapter 2 and chapter 3, respectively.

1.3 Telecom Facilities and Data Centre Supply Chain

Telecommunication facilities and data centres are an important cornerstone of our modern society. These “silent companions” enable almost every security and economically relevant interactions, e.g. control and guidance of the air/land/water transport, financial transactions or ecological calamities warnings. Malfunctions of the involved facilities may result in chaos, breakdown of the public life or even represent hazards to live and health. In addition to the security relevant services, data centres provide an almost infinite appearing reservoir of data bases utilised for scientific research and computation, as well as social networks, news and all the entertainment provided by the World Wide Web. The architectures for powering the different types of the facilities and the associated challenges are the focus of this section.

The evolution of the today's global communication and data transfer network and the involved data centres started with the development and the continuous extension of the telephony network and the thereby necessary telecommunication (telecom) facilities, i.e. access, service and switching nodes. In parallel started latish the installation of data storage and processing centres, mainly constituted in big research facilities and companies. These arrangements are different regarding maintenance, structure and powering. Telecom facilities are historically DC-powered and availability has been the highest priority, whereas data communication centres are AC-powered and rather service orientated.

In the course of the worldwide digitalisation of the telephony networks and the internet boom in the early nineties, five separate networks for telephony, mobile telephony, data communication, router/internet communication and broadband communications started to merge [39]. The broadband technology, starting with the Integrated Services Digital Network (ISDN), later e.g. Asynchronous Digital Subscriber Line (ADSL) and Very High Bit rate Digital Subscriber Line (VDSL), is providing the possibility of fast data processing, exchange and recall to a large share of the population. The demand on information and entertainment is rapidly increasing and as a result, already in the late nineties, 60 % of the total access network and IT energy consumption has been used for the costumers personal computers, 30 % for the application servers, 5 % for the switching nodes and another 5 % for the access nodes [39]. Since then, numerous data centres – also called “server farms” or “internet hotels” – have been founded; and still, the annual growth rate of shipped server equipment has been 17 % in 2004 [40] and the global market for data communication annually exceeds USD 100 Billion [41].

1.3.1 Telecom Facility Power Supply Chain

After the invention of the telephone by Philipp Reis in 1861 and the improvements made by Alexander G. Bell and David E. Hughes in 1876, one of the first public telephone networks has been set in operation in 1881 in Berlin, Germany, supplied by a local battery system [42]. The principle of the DC-powered telecom facilities was left unchanged, even though the rectifier connected to the local power grid, charging the battery and supplying the DC-bus, went through the whole history of power electronics - from the mercury-arc rectifiers in the nineteen-twenties,

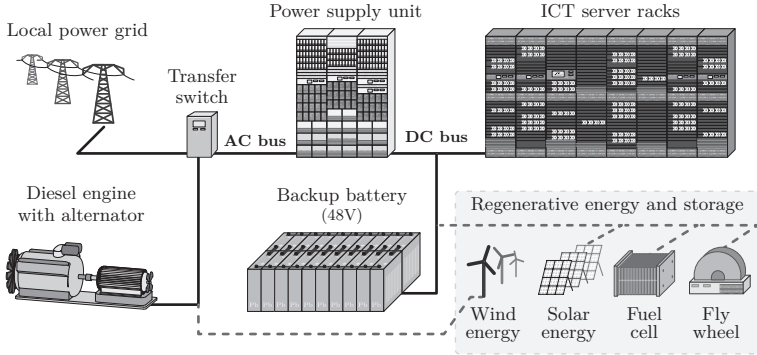


Figure 1.6: Structure of telecom facilities with a 48 V DC-bus.

selenium rectifiers, magnetically controlled rectifiers, to the point of introduction of silicon semiconductors, such as thyristors, GTOs and MOSFETs.

The typical structure of a telecom facility is illustrated in **Fig. 1.6**. The facilities are commonly connected to the local single- or three-phase grid during normal operation. In series with a transfer switch, the mains voltage is rectified in the Power Supply Unit (PSU) and converted down to the voltage level of the DC-bus. The universal standard DC-bus voltage⁶ is 48 V, defined by the European Telecommunications Standards Institute (ETSI) and the American National Standards Institute (ANSI) [39], limited by the maximum allowed voltage for electronic devices without additional protection, as defined in the international standard for protection and safety of low-voltage installations [44], with consideration of a battery voltage tolerance. This low bus voltage allows the work on the operating system with a minimum risk of personal injury without special safety precautions. The safety voltage has been increased to 60 V [44] and therefore ICT-equipment with a nominal input voltage of 52 V to 54 V is available on the market, counteracting the higher power demand of the ICT-equipment and the accruing ohmic losses in the bus cables.

In the case of a local power grid breakdown, backup batteries supply the facilities immediately with the required energy. The batteries are directly connected via circuit breakers or fuses with the DC-bus and

⁶The bus voltage is rather -48 V relating to Earth potential, e.g. [43], mainly because of the corrosion reduction of the copper wires installed in the ground.

thus mainly determining the bus voltage. By the end of the sixties, 23 plus three additional flooded lead acid battery cells (“23/26 el”) have been deployed with a resulting bus voltage range of 45 to 53 V [45]. The additional three battery cells supplied with a separate rectifier could be switched to the bus in order to compensate variable loads. From the mid-seventies until the mid-eighties 24 battery cells (“24 el”) have been installed with an voltage range of 41 to 55 V [45]. Since the mid-eighties switched mode rectifiers are deployed (52.8 V [45]), today commonly with low maintenance Value-Regulated Lead-Acid batteries (VRLA). The required input voltage range of the telecom equipment connected to the bus is determined by the battery voltage range and the conversion efficiency might decrease at lower battery voltage, e.g. in case of a prolonged breakdown. The battery hold-up time is approximately three hours for an autonomous operation [46], depending on the requirements, and therefore the volume occupied by the batteries might result in high space requirement in the facilities.

The availability of telecom facilities has a very high priority and the three hours back-up time of the batteries is commonly not sufficient as prolonged breakdowns of several hours or days, for instance caused by human mistakes, or accidents, or severe weather, are important to master besides the rather seldom occurring short and medium interrupts, mostly caused by failures of the PSU. For this reason, generally diesel engines coupled with alternators are installed which provide energy for 150 to 300 hours autonomous operation [46]. In case of a prolonged mains breakdown the generator is switched to the rectifier stage via the transfer switch recharging the battery and supplying the facilities. The diesel generators can be replaced by fuel cells, e.g. proposed in [45, 47], and the battery can be replaced or be supported by High Speed Flywheels (HSF), e.g. in [39, 47, 48].

In some inaccessible regions a local power grid is not available and other power sources must be used. Already in the mid-seventies, solar photovoltaic cells have been applied for powering telecom facilities in isolated areas of Australia [49]. The back-up batteries there are exposed to high stress because of the daily sun-cycle and the superimposed annual cycle and must offer a huge back-up time up to 10 or 15 days [49]. Moreover, the battery charge should not be lower than 50 % during poor weather in order to enlarge the battery lifetime. The lead-acid batteries are as a result the most-expensive part of the powering system, followed by the solar panels, as presented for instance in [49] for a 11 kW-system

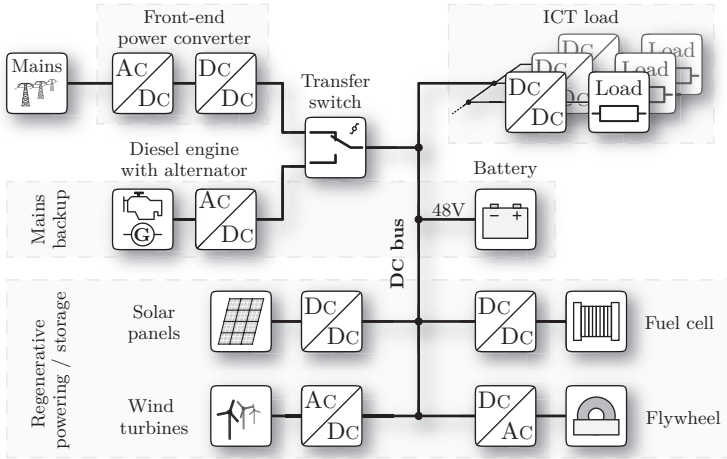


Figure 1.7: Schematic of a DC-powered telecom facility.

installed in 1978. The life-time requirements are nevertheless around 15 years.

Besides the autonomous powering of the telecom facilities, renewable energy sources could be deployed in addition to the local power grid, e.g. [46, 47, 50, 51]. Wind turbines and solar photovoltaic cells as illustrated in **Fig. 1.6** are feasible as supportive energy sources.

A summary of the telecom facility power supply is schematically shown in **Fig. 1.7**. The Power Supply Unit (PSU) which rectifies the mains voltage and provides the 48 V DC-bus voltage is divided into two conversion stages: the front-end AC-DC rectifier, today commonly with Power Factor Correction (PFC), and the DC-DC converter connected in series to step the intermediate circuit voltage galvanically isolated down (400 V to 48 V). Historically, the PSU has been composed of a transformer for the galvanically isolated voltage step-down followed by a rectifier.

The complexity of the complete powering system and the number of power conversions in case of the DC-bussed facilities are much less than e.g. for an AC-bussed data centre as shown below in this section. Telecom facilities offer therefore an inherently higher reliability.

The different demanded on-board voltage levels of the telecom equipment are generated with Voltage Regulation Modules (VRMs),

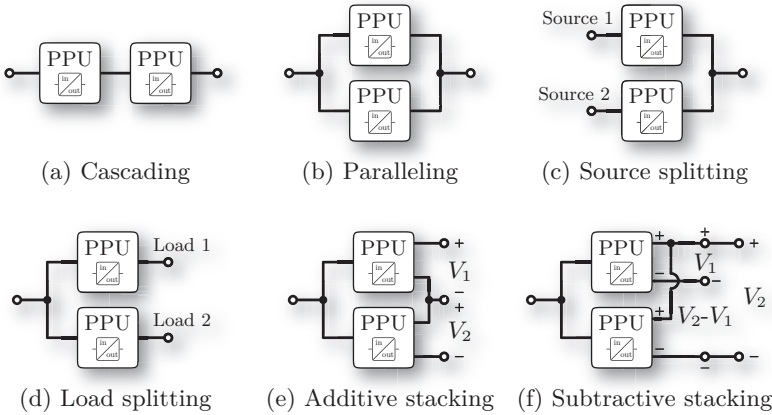


Figure 1.8: Basic structures for power distribution [52, 53]: (a) Cascading, (b) Paralleling, (c) Source splitting (d) Load splitting (e) Additive stacking, (f) Subtractive stacking. (PPU = Power Processing Unit).

i.e. DC-DC converters which step the DC-bus voltage (48 V) down to 12 V, 5 V, 3.3 V, etc.

Distributed Power Systems (DPS) The initial power supply unit in telecom facilities has been *centralised*, i.e. the only conversion stage has been the galvanically isolated rectifier which provided the required voltage of the telecom equipment. The advantage of centralised powering is that the thermal management is concentrated in a single box; however, the power system with a single conversion stage is not flexible and usually fails to provide the required regulation performance at the point of load [52] due to the bus impedance. Moreover, the availability of a centralised power supply is inherently small.

In consequence of the today's required performance in data centres and telecom facilities, the trend is away from *centralised* system to Distributed Power Systems (DPS) which are able to provide the required dynamic and accuracy, e.g. for the low voltage and high-frequency clocked processors. The complexity of the powering system thereby increases and multiple power conversion stages are in different locations, as for instance shown in **Fig. 1.7** for modern telecom facilities. The basic structures of distributed power systems are shown in **Fig. 1.8**

[52, 53]:

- (a) Cascading
- (b) Paralleling
- (c) Source splitting
- (d) Load splitting
- (e) Additive stacking
- (f) Subtractive stacking.

Because the discussion of the below presented more complex data centres is partly based on distributed power systems the basic DPS structures are shortly described in the following.

Cascading of power supplies is applied for efficiently providing high conversion ratios and adequate dynamic load regulation. In **Fig. 1.7**, for instance, the PSU is divided into rectifier commonly with PFC for rectifying the mains voltage to an intermediate DC-voltage (approx. 400 V for the single-phase European 230 V AC-grid), followed by a DC-DC converter which steps down the intermediate circuit voltage to the demanded DC-bus voltage (e.g. 48 V). The current carried in the DC-bus should be small in order to avoid expensive and heavy copper wiring. For that reason the bus voltage is usually higher than the load voltage and thus a further cascading is deployed for the VRMs located close to the load which step down the DC-bus voltage to the demanded load voltage with fast control loops for regulating highly dynamic load variations. In addition to the fast responses, variation of the bus voltage can be compensated, e.g. in case of an autonomous battery supply and the associated bus-voltage decrease.

Paralleling power converters is the basic method behind modularisation and widely used in data centres and telecom facilities. The need of modular architectures originates from the costumers demand for flexible, reliable, standardised, higher power supplies. Off-the-shelf available standardised modules, e.g. paralleled in the PSUs to obtain the specified power range, lower the engineering costs and time, resulting in an increased competitiveness. Modularisation also enables redundancy for higher reliability of the power supply: $m + r$ modules are installed, with the m demanded modules and the additional r redundant modules, which allow r units, e.g. usually $r=1$ [52] or for high-available systems even $r=m$), to fail for an uninterrupted system operation and

maintenance, and furthermore reduce the thermal and electric stresses of the components. Besides the application to obtain a higher availability, redundant PSU-modules are for instance further used for faster charging the back-up batteries after a line break-down. An additional advantage of paralleling modules in single power supplies is the possibility of interleaved switching operation which enables the reduction of magnetic components and a higher effective switching frequency, resulting in higher control bandwidth and faster dynamic response, the prevention of abnormal or even damaging system conditions [52], and moreover, the reduction of harmonics and Electromagnetic Interference (EMI) due to the current ripple reduction, resulting in smaller filter components.

Source splitting is used to increase the reliability and power range of a power supply, similarly to paralleling. By applying separated converters for supplying a common load the uninterrupted supply of the telecom equipment is ensured (amongst others), as for instance shown in **Fig. 1.7**, where the DC-bus can be powered either by the local network via the PSU or the backup battery. A further typical application is the separation of the mains-phases, where each phase is connected to an own PSU, resulting in a higher availability of power in case a module fails.

Load splitting is commonly referred to a distributed power system and is applied, e.g. in large scale facilities and in case various voltage levels are required. Splitting of the load DC-DC converters in **Fig. 1.7**, for instance, and the close connection to the load enables an adequate voltage regulation, the minimisation of noise interference effects between the loads [52] and the isolation of the noise generation from the rest of the system. In addition to the system level, further on-board VRMs for multiple voltage levels are deployed in the equipment modules itself.

Stacking of power supplies is commonly applied for realising non-standard or very precise voltages with standard modules. Higher or mirrored voltages can be implemented with additive stacking as illustrated in **Fig. 1.8(e)**, whereas the low voltages for processors are partly realised with subtractive stacking as shown in **Fig. 1.8(f)**.

These basic structures are applied in complex systems like data centres in order to fulfil the high-performance requirements of the computer equipment.

1.3.2 Data Centre Power Supply Chain

Data centres, installed for computation and data storage in the first place, look back to a steeply growing system performance during the last century. The computation speed and capacity of the storing devices are continuously increasing and the performance (size, computation speed, storage capacity, price, etc.) of available computer equipment is wide-ranged – from small home servers to megawatt server farms. Different to telecom facilities, where the uninterrupted availability has the highest priority, data processing and storage centres are more batch-orientated, i.e. the equipment must be able to be fast upgraded, extended and swapped, respectively. Because of the demanded flexibility and the wide-range application area, the merger of classical telecom facilities with data processing and storage centres are commonly AC-bussed with the local standard grid voltage.

A possible structure of a medium-scale data centre is schematically illustrated in **Fig. 1.9**. The main branch, supplying the data processing and communication equipment (ICT-load), is connected via circuit breakers to the local power grid. The first unit in the power supply chain is the Uninterruptible Power Supply (UPS) guaranteeing the continuously powering for the equipment in case of a line breakdown. The energy backup is provided by batteries similar to telecom facilities, however, the battery voltage is commonly higher than 48 V and may reach 400 V and more [41]. For an uninterrupted 3 hours supply, e.g. 54 cells are required for a 10-kVA system and 206 cells for a 300-kVA system [41]. In case of a prolonged line breakdown of several hours or days, commonly an alternator operated by a diesel engine is installed in the facility in order to limit the size and costs for the UPS system.

The UPS is followed by the Power Distribution Unit (PDU), which commonly provides besides circuit breakers, a galvanic isolation, load balancing and reactive power compensation. Besides rack-based centralised UPS systems, in some data centres, more costly decentralised UPS are applied for single important racks in order to reduce the complexity of the PDU because of the inherent power factor correction of the UPS systems.

The power distribution units are followed by the Power Supply Units (PSUs), which are adapted to the required voltage level of the Information and Communication Technology (ICT)-equipment. The communication equipment, for instance, is traditionally 48 V-DC-powered [54] and the PSU thus rectifies the AC-bus voltage, e.g. 230 V in Europe,

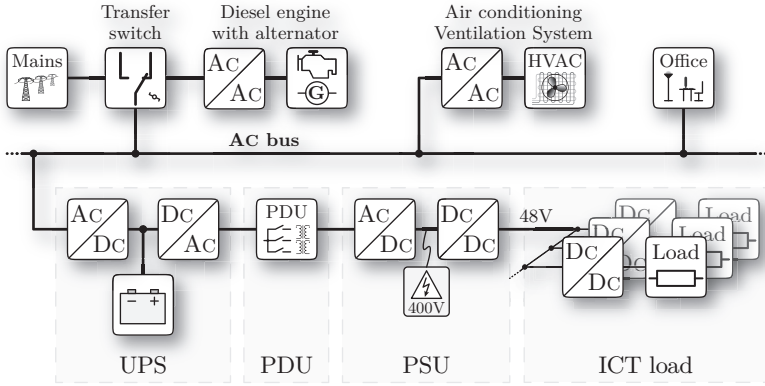


Figure 1.9: Schematic of an AC-powered data centre (UPS = Uninterruptible Power Supply, PDU = Power Distribution Unit, PSU = Power Supply Unit). For the UPS system the double-conversion type, most-applied above 5 kVA, is shown.

and galvanically isolates and steps down the voltage in a second conversion stage. Especially in large-scale data centres, there are several racks completely equipped with PSUs, whereas for small business servers the PSU can be found directly in the rack units.

Additional on-board DC-DC converters (point of load converters) are installed in the rack units, ranging from 10 W to more than 200 W, for powering the low-voltage processors. The required voltage has decreased from the 5.0 V TTL logic in the mid-sixties, to 3.3 V for 5th generation processors in the mid-nineties, and down to 1.0 V in 2001 [54]. The current demand meanwhile has increased by a factor of 10 from 13 A for the 2.0-2.5 V 6th generation processors in 1996-98 to 100 A in 2001 [54]. Because of the highly dynamic loads requiring current slew rates of 100 A/ μ s and more, the load converters must be well-decoupled from the system, by providing fast regulators and high band-width control loops.

In a strict sense, almost all the energy provided by the local network is converted into heat in a data centre. The facility must be consequently cooled down to a reasonably low temperature allowing the devices to operate in the respective Safe Operating Area (SOA) and therefore, a system for Heating, Ventilation, and Air-Conditioning

(HVAC)⁷ is necessary, which itself is a high-power consumer in the data centre. Besides the ICT-equipment, the HVAC system, as well as building establishment, like office spaces and lighting, are supplied by the alternator in case of a line breakdown.

Compared to the telecom facilities as depicted in **Fig. 1.7** the number of conversion stages between the local grid and the ICT-equipment is higher in the AC-bussed data centre cf. **Fig. 1.9**: three stages in the telecom facility and minimum of five stages in the AC-bussed data centre. The presented UPS system in **Fig. 1.9**, for instance, includes minimum of two conversion stages: the rectification of the AC-bus voltage to the battery intermediate circuit voltage and the inversion of the DC-voltage to the AC-bus. Both, rectifier and inverter carry there the entire load current during normal operation and consequently, this UPS system has a high share on the occurring losses. The different structures of UPS systems and their application areas are shortly discussed in the following section.

1.3.3 Uninterruptible Power Supply (UPS) Systems

Mostly depended on the power level and required response time there are four main types of UPS systems as shown in **Fig. 1.10** [55, 56]:

- (a) Standby UPS
- (b) Line interactive UPS
- (c) Double conversion UPS
- (d) Delta conversion UPS.

In the following paragraphs the main UPS architectures are briefly introduced.

Standby UPS, cf. **Fig. 1.10 (a)**, are commonly used for low power systems like for desktop computers. The inverter operates only in case of a line breakdown and the UPS provides therefore a high system efficiency. Additional filter structures enable an adequate noise reduction. A special form of the standby UPS is the **standby-ferro UPS**, where the transfer switch in **Fig. 1.10 (a)** is replaced by a transformer. This kind of UPS has been once dominant in the 3 to 15 kVA range [56], however, is not commonly used anymore because of the low efficiency

⁷Common definitions are additionally Computer Room Air-Conditioning unit (CRAC) and/or Computer Room Air Handler (CRAH).

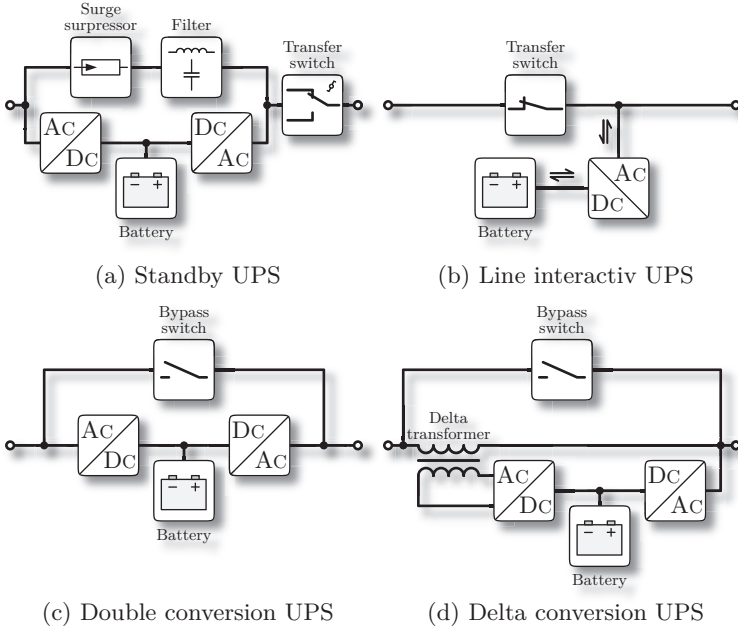


Figure 1.10: Schematics of the four main architectures of UPS systems.

and a fundamental instability when operating with modern computer loads⁸.

Line interactive UPS, cf. **Fig. 1.10 (b)**, is the most common design for web and department servers in the power range of 0.5 to 5 kVA and have a small share (approximately 19 %) in the 20.1 to 50 kVA power range [55]. A bidirectional inverter is used for charging the battery and providing the uninterrupted power delivery to the ICT-equipment. This type of UPS provides a high efficiency (97 to 98 %) over the entire load range [55] as the inverter only operates while charging the battery or during a line breakdown like the standard standby UPS.

Double conversion UPS, cf. **Fig. 1.10 (c)**, is the most common type in the power range above 10 kVA. Because the battery charger and

⁸The reason of the instability is the capacitive behaviour of the PFC-loads and the inductive behaviour of the PDU transformer which form a ringing circuit resulting in high currents [56]

the inverter both carry the entire power flow to the load, the resulting reliability and conversion efficiency of this UPS system is lower compared to e.g. standard standby UPS. However, the efficiency range of available double-conversion UPS systems is quite large because many manufacturers incorporate higher efficiency systems in their product range: 85 % to 94 % at 50 % load and up to 95 % at full load [56].

Delta-conversion UPS, cf. **Fig. 1.10 (d)**, is a relatively new system introduced by American Power Conversion Corp. (APC)⁹ in order to reduce the drawbacks of the double-conversion on-line design. The UPS systems are available in the power range of 5 kVA to 1.6 MVA with dual purposes: control of the input power characteristics, i.e. sinusoidal current and voltage waveforms, as well as harmonics reduction, and control of the input current, i.e. regulation of the battery charge [56]. The most important advantage of the delta conversion UPS are the significant reduction of the power losses: 96 % to 97 % at 50 % load and 97 % at full load.

For a 1-MVA data centre the efficiency gain of the delta-conversion UPS already results in 20 kW lower losses compared to the highest-efficiency double-conversion UPS and thereby inherently an even higher facility efficiency because of the cooling effort reduction. That emphasises the high influence of the UPS system on the data centre efficiency and operation costs. A summary of the loss distribution in a typical data centre is given in the following in order to identify the important potentials for improvements.

1.3.4 Typical Loss Distribution of Data Centres

The losses in the data centre, emerging because of non-ideal power conversion and the related cooling effort, are getting more and more a big concern of the operators as the energy bill for powering, cooling and lighting is up to one half of the total data centre costs (sum of energy bill, hardware and software costs) [40, 48, 57–59]. The typical loss distribution of a data centre with a PUE = 2.75 (according to equation (1.4)) is illustrated in **Fig. 1.11** referring to data presented in [47]¹⁰.

Almost a third of the supplied energy is used for the cooling system, cf. **Fig. 1.11** [47]; for the system with a higher PUE = 2.13 as presented

⁹Now part of Schneider Electric SA.

¹⁰Approximately similar distributions can be found in [30, 48, 57].

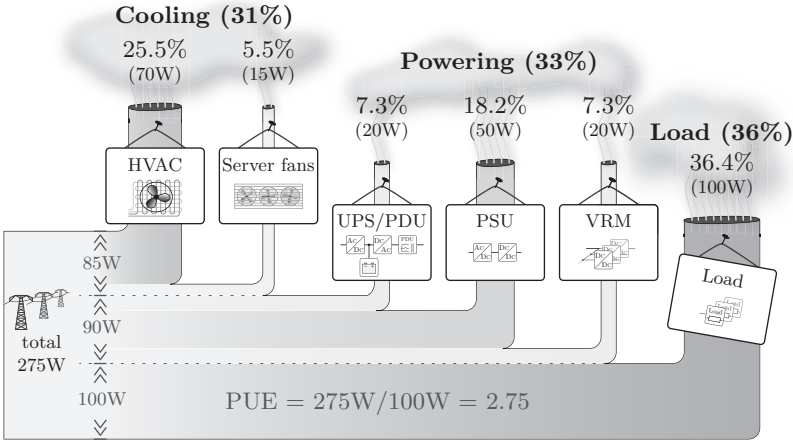


Figure 1.11: Typical distribution of losses in today's data centres. (Data extracted from [47] for a data centre with a Power Usage Effectiveness, cf. (1.4), of $PUE = 2.75$.)

in [30]¹¹ the loss-share of the cooling system is even higher: 23% for the chiller, 3% for the humidifier outside the facility and 15% for the CRAC/CRAH systems inside, which results in 41% of the total energy supplied to the data centre.

Further 7.3% of the supplied energy are used for the power conversion in the uninterruptible power supply and power distribution unit (approximately two third thereof in the UPS and one third in the PDU [57]). The power supply unit and load converters additionally consume one third of the total energy for the voltage conversion. Only approximately one third of the assimilated energy in **Fig. 1.11** is consequently available for the actual load: the ICT-equipment. A similar result is presented in the investigation of [48]: a 1U 300 W server rack unit requires a total power of $P_{\text{tot}} = 973 \text{ W}$ to be operated.

Powering and cooling of servers accounted for 1.2% of the entire United States (U.S.) electricity consumption in 2005 [58]; the complete information and communication technology consumed 8% of the electricity – both in the European Union (2009 [51]) and in the U.S. (already in 1998 [47]). In consequence of the current data centre losses and the

¹¹The basis of this investigation has been a typical high-availability data centre operating at 30% of the design capacity.

continuously increasing demand on ICT, there is an urgent need for action, making the power conversion with all the belonging contributors more efficient and thereby contributing in environment protection and additionally saving a high amount of money for the energy bill. In the following section, the challenges and possibilities for more efficient data centres are highlighted.

1.3.5 “Go Green” - Challenges and Possibilities

Investigations in more efficient facilities have been especially expedited since the introduction and expansion of ISDN in the mid-eighties. Since then, the aspiration of the power supply manufactures has been the exaltation of the power density (e.g. [50]) in order to increase the cooling efficiency and counteract the rising space required for the digital equipment. The continuous demand on ICT, rising energy prices and increased ecological awareness, force the manufactures to provide further solutions for more efficient data centres. The challenges and possibilities for more “green” facilities are discussed in the following paragraphs.

Power Density Besides the improvements regarding competitiveness, marketing and room utilisation, developing and providing high-power-density equipment generally offers the technical advantage that compact systems can be cooled down more efficiently: the occupied area in the facility is smaller and thereby the cooling volume is decreased. Additionally, compact systems are providing shorter airflow paths, less air mixing, and higher heat rejection temperatures [57]. Today’s applied rack units provide a power supply ranging from 2 to 6 kW [47, 48]; new High Density (HD) racks are available with 12 to 20 kW [48, 57], and the industry prediction is that the density will grow up to 40 kW per rack or cabinet in the next few years [48] resulting in an improved chiller efficiency and increased air conditioning capacity [57]. The efficiency exaltation by increasing the power density is coupled to physical limitations of the applied components. The efficiency border can be exceeded by increasing the efficiency of the installed IT and non-IT components and the advancements in power distribution as discussed below.

Cooling System (HVAC/CRAC/CRAH) The cooling system has major impact on the loss distribution as shown in **Fig. 1.11**. Besides the above mentioned reduction of the cooling volume, the energy required for facility air conditioning can be further decreased by reducing the heat generated in the computer room, i.e. by increasing the efficiency of the power conversion, and by developing and installing highly efficient HVAC systems. Furthermore, the cooling systems are usually over-dimensioned because of the complicate prediction of losses and to facilitate the possibility for extending the server room. New row-based cooling systems may be a good solution as investigated in [57]: for a data-centre-typical operation at 30 % of the rated load capability, the cooling effectiveness for the room cooling is approximately 66 %, whereas the cooling effectiveness for the row-based cooling could be increased to 90 % [57]. Another reason for installing oversized HVAC systems is the necessity to cool down occurring hot-spots in the computer room to the specified maximum allowed temperature. An intelligent load distribution and load-depended variable speed drives for the fans are an arising solution for that challenge.

In many regions of the earth the promising opportunity exists of cooling the facility partly or even completely with outside air, as presented e.g. in [58]: if the outside air temperature is about 4 to 6 °C the chillers are shut down entirely and the resulting energy savings are 300 kW an hour (!); in [57] the estimated efficiency gain is 5 to 10 %.

The potential loss-reduction by an improved cooling system is up to 30% as shown in [30].

The fundamental power distribution method has a substantial influence on the data centre efficiency. As presented above, different approaches are pursued powering telecom facilities and data centres resulting in different structures, complexities and performances. The opportunities and challenges applying different bus structures (DC, AC, and High-Frequency (HF) AC), the respective waveforms and voltage levels are discussed in the following.

DC-Powered Data Centres Besides in telecom facilities, DC-power systems are deployed for instance in mainframe computers, space vehicles, the international space station, aircraft, ships, and radar stations [60]. In literature, e.g. [40, 47, 48, 57], very promising developments can be found suggesting data centres with a DC-bus as the better option for more efficiently powering the classical data centres

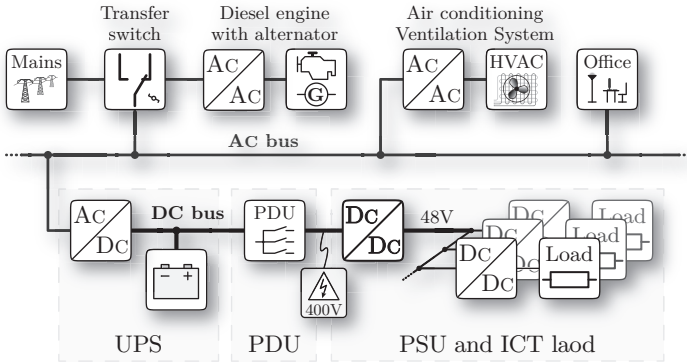


Figure 1.12: Schematic of a DC-powered data centre.

than with an AC-bus. The main advantages of DC-distributed facilities are based on the lower complexity of the supply chain as shown in **Fig. 1.12** which directly results in a decreased energy demand for the power conversion stages. Furthermore, the power density increases by 30 % [40] and due to the resulting reduction of the cooling volume, the PUE is indirectly further improved.

The presented power savings in [40, 47, 48, 57], when shifting from AC- to DC-powered data centres, are between 13 and 35 %, depending on the applied equipment and the utilisation of load capability. In addition to the cost-reduction for purchasing, installing, and maintaining the hardware, the energy bill can be drastically decreased¹².

Approximately 10 % of the service interrupts are caused by power supplies [41]. In consequence of a lower devices count the reliability of a system increases; therefore the MTBF of a typical AC-data centre is approximately 100'000 hours whereas DC-powered data centres achieve a seventy times higher MTBF of 7'000'000 hours [40].

In [47] a DC-powered data centre is introduced where the DC-bus voltage has been increased from the telecom-typical 48 V to approximately 400 V in order to counteract the continuously growing demand on power of the ICT equipment, cf. **Fig. 1.12**. Because of the decreased current in the bus bars, the conduction losses can be reduced and the

¹²Taking a 1-MW data centre operated at 50 % load capability and a key account price of CHF 0.15 per kW/h exclusive VAT as basis, the annual energy bill savings are around a quarter million CHFs!

opportunity emerges to apply lighter and less expensive cables. For this configuration, the mains voltage is rectified and regulated to 400 V and distributed at this voltage level to the racks, where a DC-DC converter steps down the high bus voltage to the demanded rack unit inputs, e.g. 48 V for telecom equipment. The conversion stages are comparable to the telecom facility in **Fig. 1.7**, only the front-end AC-DC rectifier with PFC and the 400 V to 48 V DC-DC converter are split there and the intermediate circuit voltage is now the bus voltage. The battery voltage is thereby 400 V, if connected directly to the bus¹³, which might reduce the battery lifetime and increase the failure rate λ by a factor of 10 due to charge-unbalances in the series connected batteries [41]. Moreover, the extra-low voltage range (SELV and PELV)¹⁴ of 120 V (DC) according to [44, 61] is exceeded and therefore special isolation and safety measures are required. For instance, the maintenance on an operating system is not readily possible and special bus bars, connectors and circuit breakers have to be installed.

The preferred DC-bus voltage is commonly still kept below 60 V in order to avoid basic protection measures according to [44, 61] and the existing 48 V telecom standard is considered as the most practical and economical option, e.g. in [41, 48, 54], also because of the mature standardised available 48 V-ICT-equipment. Lower bus voltages, for instance the direct supply of the load with 3.3 V, are not practicable because of the high power demand, the conduction losses in bus bars, and the required bulky cables. Furthermore, the digital voltage levels are changing over the years, as mentioned above, and the regulation of, e.g. ± 100 mV, for the highly dynamic ICT-loads is almost not achievable with a single-stage converter due to the bus impedance, even though the costs for a single-stage conversion are smaller [62].

Aside the fact that the voltage level has a high influence on the system performance, the global standardisation of a DC-voltage level appears to be simpler compared to AC-voltages because the existing 14 different national AC grid voltages [41] are commonly employed in the respective national data centres. The application of global standardised DC-equipment offers inherently the opportunity of lower hardware purchasing costs and higher performance, due to a possible optimisation for a single input and output voltage rather than wide voltage-range

¹³Another approach is the connection via an additional bidirectional DC-DC converter as battery charger and for supplying the power in case of a mains-breakdown.

¹⁴SELV = Safety Extra-Low Voltage, PELV = Protected Extra-Low Voltage

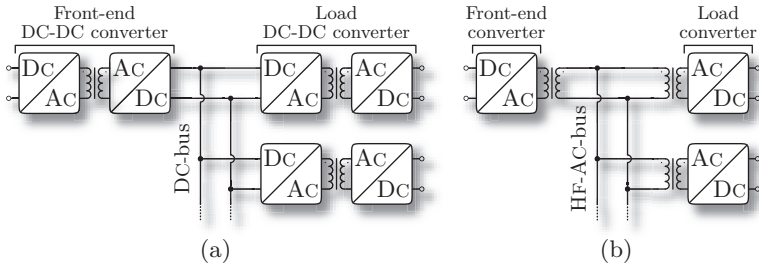


Figure 1.13: Power distribution: (a) DC bus, (b) HF AC bus [53].

equipment.

Nevertheless, the change from AC- to DC-powered data centres is a drastic change since the life-time of the power supply chain equipment is generally longer than for the ICT-equipment and the corresponding investment is high. To give an example, the available 80 %-efficient DC-power supplies are commonly 10 % cheaper than 90 %-efficient DC-power supplies [47]. It will take some time to adopt the market for the DC-modules and to convince the operators to install highly efficient DC-equipment, even though the ecologic and economic advantages cannot be dismissed and the basic concept of DC-powered facilities is not new.

High-Frequency AC-Bus A further reduction of conversion steps could be achieved with a high-frequency (HF) AC-distributed power system, where the bus frequency is determined by the PSU, which is typically in the kHz-range and thus much higher than the grid frequency (50/60 Hz). The basic idea is to omit the rectifier of the front-end PSU and the inverter of the load converter which are parts of a DC-distributed system as illustrated in **Fig. 1.13** [53]. Theoretically, the change from the data centre with DC-bus, cf. **Fig. 1.12**, to the HF-AC-DPS as illustrated in **Fig. 1.13** can further increase the efficiency and reduce the costs because of the simplified system configuration.

Nevertheless, the HF-AC-distribution has not been widely accepted due to potential challenges such as bus distortion, high frequency losses and Electromagnetic Interference (EMI) noise [60]. In addition to the bus voltage, the bus frequency and waveform have to be considered which both have a major impact on the system performance. For the frequency, there is a trade-off between system volume, costs and losses, considering the special bus-wiring and skin effect losses in the cable.

The frequency is thereby practically limited to 200 kHz [60].

Possible voltage shapes are square wave, sine wave and trapezoidal waveforms. The square wave can be simply achieved by a common front-end PWM inverter; however, the redundant extension of power supplies is difficult, due to the required synchronisation, and the high harmonics in the bus result in high EMI noise and losses.

Fewer harmonics and thereby less EMI related effects are obtained by applying sine waves for the HF-AC-bus. Also the transformers operate more efficiently compared with the application of square waves, however, the sine wave generation is more complex and commonly connected with high circulating energy, which decreases the system efficiency. Furthermore, the installation of redundant systems cannot be solved with this approach.

In [60], a HF-AC-bus with trapezoidal waveform is suggested enabling redundancy of $(n+1)$ front-end converters in parallel. The structure additionally features a compromised EMI and harmonic level and more efficient power conversion. However, the structure is more complicated and the bus waveform shape as well as the voltage and EMI levels would change with the number of front-end converters in parallel [60].

Although the HF-AC-bus has been considered already in the early nineties, e.g. in [53], the structure is not established and remains in a conceptual stage as there are multiple practical challenges, such as the high EMI level, the realisation of the system redundancy, or the connection with the back-up system. In addition, system interactions and the stability of series- and parallel-connected front-end inverters, bus and load rectifiers have to be investigated due to the highly dynamic load.

The power distribution of the high frequency AC-bus is even more complicated than for a grid-frequency operated AC-bus, because the frequency, magnitude and phase synchronisation have to be faster by three orders of magnitude. The occurrence of harmonic distortion is an important issue for any AC-bus in principle, because for a proper filter design the load must be well known, which complicates and limits the upgrade or extension of ICT-equipment. Commonly, the systems are over-dimensioned, which results in higher costs, or even more expensive active harmonic filters are applied, which are less reliable [41].

Uninterruptible Power Supply (UPS) In case of a local network breakdown, the energy for operation must be immediately delivered by the back-up batteries of the UPS. Because of the high energy demand typically double conversion UPS are applied in data centres as presented in section 1.3.3, cf. **Fig. 1.10(c)**. This type of UPS is permanently in the supply chain and the entire energy flow is processed through this UPS system. As a result, the UPS system is a major contributor to the data centre losses, cf. **Fig. 1.11**.

One possibility to increase the UPS efficiency is to reduce the conversion steps as e.g. in a DC-powered data centre as discussed above. If the required UPS type cannot be changed the rectifier and inverter have to operate more efficiently. Most data centres operate in the load-capability range of 10 % to 30 %, there the UPS features an efficiency of only 60 % to 80 % [30]. In high-efficiency UPS systems the energy demand at light load is reduced by 65 % [57] which further reduces the amount of energy needed for the cooling system. Global efficiency requirements and standards, as e.g. stated for power supplies as discussed in the next paragraph, are additional instruments to guide the market towards more efficient UPS. For instance in [55], an efficiency of 90 % at 20 % load and of 95 % at 50 % and full load is proposed for UPS above 200 kW, which would result in 2.8 TWh and USD 280'000'000 annual savings in the USA, if all the installed UPS systems would fulfil these standard¹⁵.

Power Supply Unit (PSU) The PSU of data centres and telecom facilities is a further major contributor to the losses as shown in **Fig. 1.11**. The power conversion steps – AC-DC with PFC to the intermediate circuit voltage of for example 400 V and the DC-DC conversion to for example 48 V for telecom equipment – are essential, both in telecom facilities and data centres, only the place or composition in the power supply chain differs, cf. **Fig. 1.7**, **Fig. 1.9** and **Fig. 1.12**, and thus the conversion stages cannot be excluded. As a consequence, a contribution to increase the facility efficiency by improving the PSU can only be obtained by increasing the power density (and thereby decreasing the cooling effort) or increasing the PSU efficiency itself.

¹⁵The study has been based on the operation with 38 % load capability and the UPS system (> 200 kW) featured an efficiency of 93 % instead of 85.2 % with this load. Further information and numbers for different power levels can be found in [55] as well.

Table 1.1: Energy Star[®] efficiency requirements for computer server single-output power supplies (AC-DC rectifier for AC-powered and DC-DC converter for DC-powered data centres) [27].

Rated output power	10 % load	20 % load	50 % load	100 % load
≤ 500 W	70 %	82 %	89 %	85 %
> 500 W to 1 kW	75 %	85 %	89 %	85 %
> 1 kW	80 %	88 %	92 %	88 %

Energy Star[®]¹⁶, a joint program of the U.S. Environmental Protection Agency (EPA) and the U.S. Department of Energy (DOE), released requirements for computer server power supply units in May 2009 [27], which imply a compulsory efficiency for single output AC-DC server supplies (for AC-powered data centres) and DC-DC supplies (for DC-powered data centres), as shown in **Tab. 1.1** and in **Fig. 1.3** on page 7¹⁷. The required efficiencies are proposed for multiple load points in order to achieve higher efficiencies at part load as well, where the power supplies are typically operated.

Accordingly to the loss distribution in **Fig. 1.11**, the gap from the conventionally-applied to the highly efficient power supply units is high which motivates to investigate higher efficiencies for these modules in the power supply chain. Moreover, the improvement in power conversion increases again both, the data centre efficiency directly and indirectly because of the reduced cooling effort. Besides, heat-related hardware failures can additionally be reduced.

Load Converters A further design-challenge arises from the following load converters (voltage regulator modules (VRM)): since the eighties this conversion stage, e.g. 48 V to 5 V, has been optimised for maximum power density and fast response time [64], which became necessary with the increased usage of the Very-Large-Scale Integration (VLSI) technology and the related high power demand and fast current transients. Because of the negative input impedance of the power sup-

¹⁶Energy Star[®] labels are deployed for electronic equipment since 1992 in the USA, since 2002 in the EU and since 2009 in Switzerland [63].

¹⁷In **Fig. 1.3**, the graph for power supplies with a power rating higher than 1 kW is depicted.

plies, which induces right-half-plane poles in the converter's loop gain, the stability of the converters as part of a DPS has to be a priority concern and stability analysis e.g. Nyquist Criterion [64], Middlebrook's Criterion (voltage-mode control) [65], or multiple criteria (current-mode control) [66] have to be investigated. The power density will stay a driving force for load converter development in order to counteract the increasing power demand of the VLSI processors. In addition to stability, response time, and power density, the efficiency is more and more a sales argument and organisations such as Energy Star® included the computer equipment in their efficiency requirement program, which is justified by the high amount of losses during the power conversion as shown in **Fig. 1.11**.

An optimisation of the load converters, e.g. with respect to power density or efficiency, provide generally better results if the voltage levels are tightly specified. If the front-end PSU voltage regulation is very accurate, the VRMs can be optimised with a higher performance gain and consequently, a trade-off between load converter and PSU has to be found. However, in case of a DC-powered facility, where the bus voltage is determined by the battery, the required input voltage range of the VRMs is 42 V to 56 V [50].

Data Centre Planning and Operation The efficiency of the data centre can be significantly increased by improving the particular components of the supply chain, as discussed above. A further high potential for increasing the system efficiency is to consider the data centre as a whole during the planning phase and the later operation.

The exact IT-load is usually not known and the possibility to extend the system with further ICT-equipment has often to be persevered, which results indirectly in an oversizing of the applied components of the power supply chain and the cooling system. In data centres with demanded high availability, the components of the supply chain are oversized on purpose, called *derating*, in order to avoid the operation close the maximum design capacity. A derating of 10 % to 20 % is recommended for highly available data centres [30]. Another reason for oversizing is the inaccurate estimation of the losses in the power supply chain due to imprecise loss and load models or incomplete documentation in the data sheets, e.g. the specification of the efficiency for a single load point. The oversizing of the power supply chain components results automatically in an oversizing of the cooling system and thereby

in additional heat generation resulting in a further cooling demand and lower system efficiency. The reduction of the oversizing is a big opportunity for savings in a data centre. Applying modular adaptable architectures allows the load-dependent adaption of the facility (rated power and required cooling system) and a loss-reduction of 50 % [30].


The underutilisation of the components in the power supply chain is a further large inefficiency contributor in the data centre. At the typical 30 % load capacity utilisation level, over 70 % of the electricity costs are caused by the non-ideal power conversion and cooling [30]. An intelligent PDU, monitoring and distribution of the computation tasks to the ICT-equipment in medium to large scale data centres, would enable the power supply chain to operate in close vicinity to the maximum efficiency. The shut-down of unused computation equipment further increases the facility efficiency due to the lower-load losses.

Data centres and telecom facilities are one of the most important engines in our modern society. The continuous technical progression of ICT-equipment, such as the 64-bit processors which enable more computation-intensive applications, the enlargement of the existing facilities, and the installation of new data centre, however, involve the irresistible demand on energy for this branch. The operators and manufactures are therefore responsible for an economical and efficient utilisation of energy and material resources. Many companies have started investing in services and products helping to reduce the ICT-energy demand¹⁸. The gain to drastically increase the efficiency is huge, as presented in this section. In particular, the advancements of the power conversion stages in the power supply chain offer the opportunity of a relevant contribution.

One essential power supply stage for ICT-equipment is the DC-DC converter in the power supply unit, which is installed in several data centres and telecom facilities. The performance investigation of the telecom DC-DC converter is subject of this thesis and therefore possible topologies for this power conversion stage are presented in the following section.

¹⁸IBM for instance planed to invest one billion USD a year for that purpose [58].

Table 1.2: Specifications of the evaluated DC-DC converter.

		
Input voltage	V_{in}	400 V
Output voltage	V_{out}	48...56 V
Output power	P_{out}	5 kW
Output ripple voltage	$v_{out,pp}$	300 mV _{pp}
Max. ambient temperature	T_a	45 °C

1.4 Telecom DC-DC Converter Topologies

The necessary DC-DC converter stage as part of the power supply unit, installed in the above presented and several further data centre types, cf. schematics in **Fig. 1.7**, **Fig. 1.9** and **Fig. 1.12**, converts the DC-bus voltage or intermediate-circuit voltage of $V_{out} = 400$ V down to $V_{out} = 48$ V to 56 V (depending on the connected ICT equipment) with an allowed output voltage ripple $v_{out,pp}$ of 300 mV_{pp} (peak-to-peak). In order to meet the higher power demand in server racks, the output power level P_{out} is fixed to 5 kW for the DC-DC converter in the following investigations. The ambient temperature T_a during the normal power supply operation is supposed not to exceed 45 °C . Moreover, galvanic isolation is commonly required for the power supplies source–load decoupling. The multitude of possible converter topologies suitable for the specifications summarised in **Tab. 1.2**, is discussed in this section.

An unidirectional power flow in the DC-DC converter from the input (DC-bus or intermediate circuit) to the output (ICT load) satisfies the specifications of the required converter topology. The application of a bidirectional converter, however, is in principle possible. A comprehensive analysis of different bidirectional DC-DC converters applicable for wide-voltage-range on the high- and low-voltage side, and 2 kW power conversion is elaborately presented in [67]. There, it is shown that an advanced control of the converter can additionally improve the system efficiency. Because of the increased control complexity and partly higher number of components, bidirectional converter types are not explicitly investigated in the following, even though some topologies are suitable

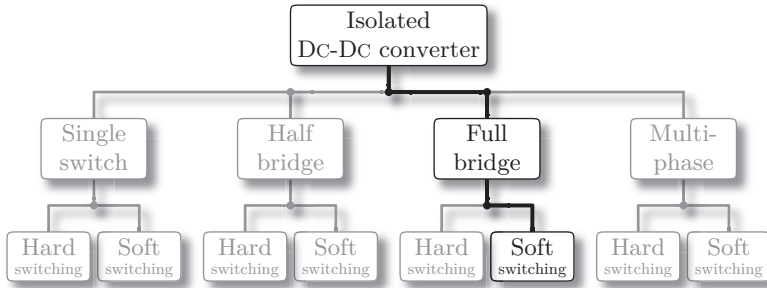


Figure 1.14: Overview of galvanically isolated DC-DC converters.

for bidirectional power conversion.

The investigations are concentrated on single-stage topologies, i.e. a single inverter followed by a single rectifier, in order to minimise the complexity and components count. Multi-stage converter systems, however, can be advantageous if a wide input voltage range is required which is here not the case.

The galvanic isolation can be obtained with several converter topologies, i.e. single-switch, half-bridge, full-bridge, as well as multi-phase structures, as illustrated in **Fig. 1.14**. The different structures can generally be divided into hard-switched and soft-switched topologies, whereas the hard-switched converter is hardly applicable for high-performance systems, as the losses due to the non-ideal switching result in lower efficiency and higher cooling volume. For that reason the grey branches in the tree diagram in **Fig. 1.14** are not further considered in this evaluation.

The aspiration towards highest performance with respect to power density and efficiency further excludes the application of **single-switch topologies** for the specified power level. Isolated single-switch DC-DC converters, such as flyback and forward converter, provide a low complexity and are popular in low-power applications below 100 W. Furthermore, the basically hard-switched topologies require additional circuit components and measures to obtain soft-switching, as for instance presented in [68–72], whereby the applicable power level can be increased to approximately 500 W, however, the converter complexity increases and auxiliary circuits are commonly avoided especially for higher power in favour of reliability. In addition, because of the uni-

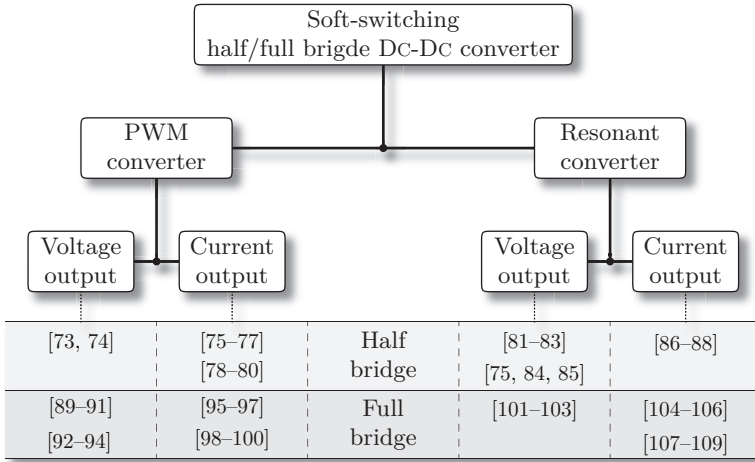


Figure 1.15: Overview soft-switched half- and full-bridge DC-DC converters.

directional utilization of the transformer (forward converter) and two-winding inductor (flyback converter) the magnetic components become bulky and not practicable for the specified power level. Moreover, the blocking voltage of the inverter switches is typically two times the input voltage V_{in} and the performance of available power semiconductors is reduced for the required voltage level (minimum 1 kV blocking-capability), whereas for instance in a full-bridge inverter, high-performance 600-V-MOSFETs can be applied. In the following topology introduction, single-switch DC-DC converters are therefore not further considered.

The remaining converter topologies according to **Fig. 1.14**, suitable for the galvanically isolated power conversion, are summarised in **Fig. 1.15**. The soft-switching power supplies based on a half or full bridge can be divided into resonant and Pulse-Width-Modulated (PWM) converters. Both inverter topologies, resonant and PWM, can be connected to different rectifier stages with voltage or current output. Because of the bidirectional magnetisation of the transformer, similar full-wave rectifier topologies can be applied for both, half-bridge and full-bridge topologies. The basic full-wave rectifier stages as presented in **Fig. 1.16**¹⁹ are briefly introduced in the following.

¹⁹Note, that in the schematics of **Fig. 1.16** diodes have been applied in the rec-

Full-Wave Rectifier Stages The most famous full-wave rectifier is the **bridge rectifier** as shown in **Fig. 1.16 (a)**, also known as Graetz circuit, named after its inventor Leo Graetz. Depending on the polarity of the applied transformer voltage, two diagonal diodes of the H-bridge are conducting if the transformer voltage exceeds the voltage of the output filter capacitor C_{out} . The diode's blocking voltage is thereby beneficially clamped to the output capacitor voltage, neglecting the voltage drop over the parasitic inductances. The transformer consists only of a single secondary winding enabling a simple assembly, however, with the drawback that two of the four diodes are simultaneously in the conduction path leading to high conduction losses in the semiconductors. Moreover, since there is no smoothing inductor on the rectifier stage, the inverter stage must provide an adequate inductance in order to limit the current slope. The current ripple on the primary and secondary side is usually high for this topology resulting in a higher flux in the transformer and the necessity of a higher filter capacitance and thereby a compromise between losses and component volume must be found.

Only two diodes are necessary for the rectifier stage with a **centre-tapped** transformer in **Fig. 1.16 (b)**. This rectifier stage is commonly used for high-current applications in order to reduce the conduction losses in the semiconductors. The drawback is the more complex transformer with two secondary windings. Furthermore, the inherent leakage inductance between the two windings in series with the current commutation path increase the voltage ringing due to the non-ideal current commutation in the hard-switched rectifier. A further disadvantage is the required voltage rating which is higher compared to the Graetz circuit, as the applied reverse voltage is the sum of the output voltage V_{out} and the transformed primary side voltage. The current and voltage waveforms in the inverter stage are in principle similar to those of the bridge rectifier, and the current slope has to be adjusted by inverter as well.

For high output voltage applications the **voltage doubler** rectifier in **Fig. 1.16 (c)** is potentially advantageous (e.g. [110–113]). This topology requires two diodes, similar to the rectifier with centre-tapped transformer, however, only a single secondary transformer winding is required and thus the advantages of the full-bridge and centre-tapped

tifiers allowing the required unidirectional power flow; however, the diodes can be replaced by actively switched semiconductors such as MOSFET as well.

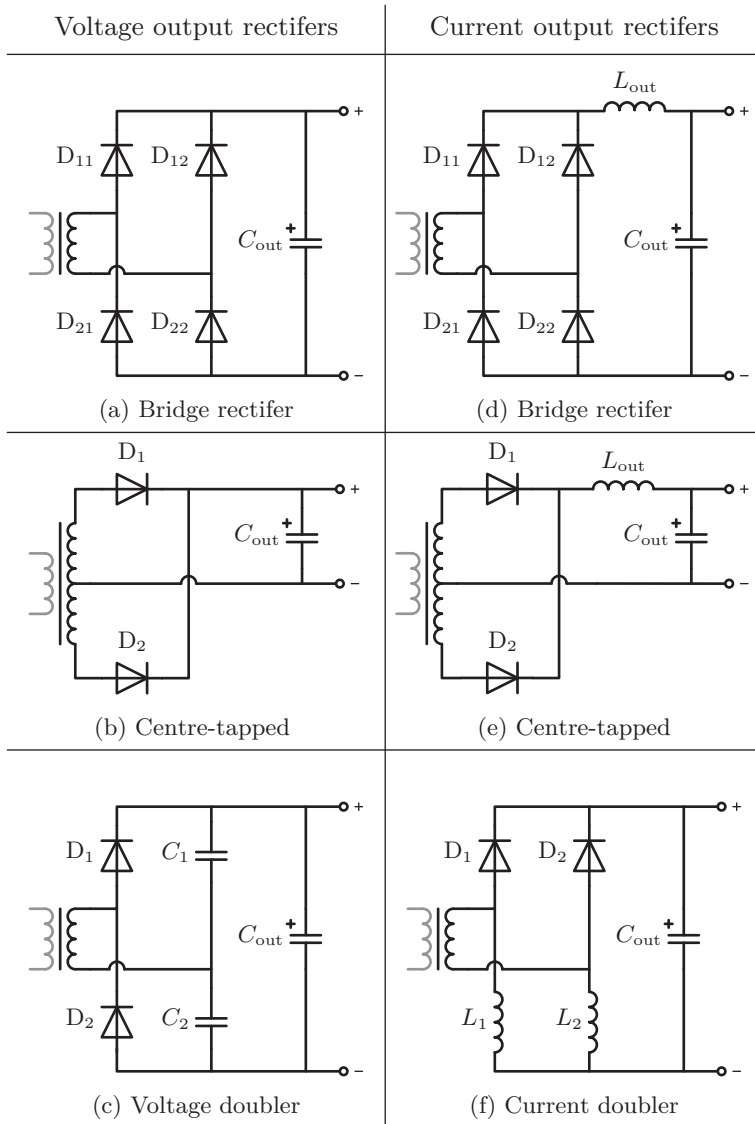


Figure 1.16: Basic full-wave rectifier topologies. Note, that the diodes can be replaced by controllable semiconductor devices, allowing synchronous rectification and/or bidirectional power conversion.

rectifiers are combined. For every half-wave one of the two voltage doubler capacitors ($C_{\text{DC},1}$ or $C_{\text{DC},2}$) is recharged and the filter capacitor C_{out} can be small or even omitted. For applications with continuous high current flow, the voltage doubler topology is less applicable as the capacitors become very bulky for the demanded output voltage ripple $v_{\text{out,pp}}$.

On the right-hand side of **Fig. 1.16** the basic rectifier stages with impressed output current are depicted. The **bridge rectifier** in **Fig. 1.16 (a)** is extended by the output inductor L_{out} , cf. **Fig. 1.16 (d)**, which additionally influences the current waveform in the inverter stage. The added inductor increases the complexity and the losses of the rectifier stage. Furthermore, the blocking voltage of the diodes is increased because of the additional voltage drop over the inductor. However, the output inductor enables the omission of current-slope limiting measures in the inverter stage and additionally offers an increased filter order for the output.

The rectifier with **centre-tapped** transformer and **LC-output** filter as shown in **Fig. 1.16 (d)** reveals a similar behaviour regarding current smoothing and influence on the inverter as the bridge rectifier with current output. The drawback is again the increase of the required voltage rating of the diodes and the thereby decreased performance of applicable semiconductors. This rectifier topology is preferably used in applications with high output current as the rectifier stage with centre-tapped transformer without output inductor, cf. **Fig. 1.16 (b)**, as the basic advantages and disadvantages regarding winding complexity and diodes losses described above are still valid.

Applicable for higher currents is as well the **current doubler** rectifier stage in **Fig. 1.16 (f)**. The smoothing inductor L_{out} is divided into two separated inductors, each carrying approximately half of the output current simultaneously. The drawback of two separated inductors L_1 and L_2 and the associated higher complexity for connection and increased assembly volume is compensated with the advantages that only one secondary winding is necessary, compared to the rectifier stage with centre-tapped transformer, and less displacement effects occur because of the halved output current. If the output current ripple, ideally smoothed out by the output filter capacitor, is similar to the centre-tapped and bridge rectifier with LC-output, the current ripple in the current doubler inductors is higher because of the interleaving, resulting in slightly higher core and HF-winding losses. Nevertheless,

the current doubler is a common rectifier stage for the specified data centre and telecom DC-DC power supply.

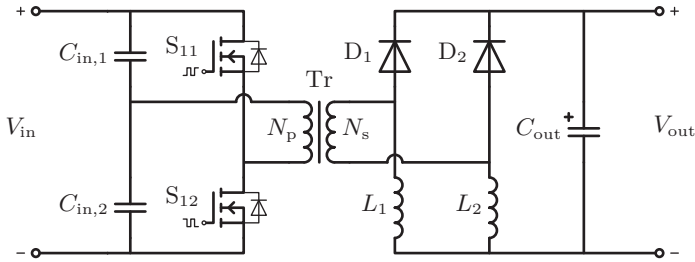
The presented full-wave rectifier topologies can be combined with resonant and PWM half-bridge and full-bridge inverters as illustrated in **Fig. 1.15**. Some of the resulting suitable topologies are presented in the following.

Half-Bridge DC-DC Converter In the tree diagram in **Fig. 1.15**, a few corresponding references are given for each half-bridge inverter and DC-link combination. One of the basic half-bridge structures is the **PWM-controlled** inverter with current doubler rectifier stage as presented in **Fig. 1.17 (a)**. For a symmetric control²⁰ of the two inverter switches the converter is inherently hard switched. In order to obtain soft-switching, either an additional circuitry has to be added, e.g. the auxiliary circuit in [114, 115], or active switches and a respective (bidirectional) control have to be employed, e.g. [77–79], or the control of the primary side switches is asymmetrical, i.e. there are only two main states where always one of the half-bridge switches is turned on, e.g. [75, 76]. The asymmetric half bridge shown in **Fig. 1.17 (a)** is commonly used for an output power up to 1 kW and suitable for supplying ICT-equipment, i.e. for the converter with 400 V input and 48 V output voltage as for instance presented in [75, 80]. For higher power demand the converter stages have to be paralleled in the server racks as described in section 1.3.1.

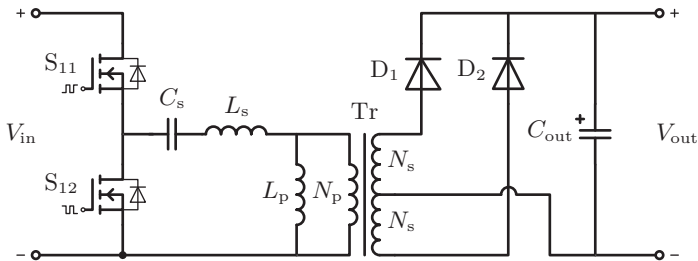
The voltage applied to the transformer in an asymmetric half bridge is half of the input voltage V_{in} , cf. **Fig. 1.17 (a)**, and thereby the current has to be doubled compared to topologies, where the full input voltage is applied, if the same power should be transmitted. Moreover, because of the asymmetric on-times of switches, the utilisation of the switches and passive components differs depending on the switching state, i.e. if the positive or negative voltage is applied to the transformer. The components such as the switches, the DC-link capacitors, and the transformer must consequently be designed for higher VA-ratings, which limits the power level for a high efficiency and high performance application of the half-bridge converter.

The advantage of the low complexity and simple control can be capitalised, however, in the power range below 1 kW, especially as on-

²⁰The on-time of the upper and lower switch is equal. After each on-state, both switches are turned off.



(a) Asymmetric half bridge with current doubler rectifier



(b) LLC resonant half bridge with center-tapped transformer

Figure 1.17: Typical half-bridge topologies: (a) asymmetric half-bridge PWM converter with current doubler output, (b) LLC-resonant half-bridge converter with centre-tapped transformer.

board load converter for the ICT-equipment with a wide input voltage range of approximately 36 V to 75 V and output voltages of for instance 12 V (e.g. [76] with 200 W output power or [77] with 750 W output power), 5 V (e.g. [78] with 100 W output power), and 3.3 V ([79] with 66 W).

Pulse-width-modulated half-bridge converters with voltage output are advantageously used for higher voltage applications, e.g. for bi-directional power conversion with a HV-side-connected fuel cell and LV-side-connected battery in fuel-cell vehicles [73, 74]. The power limitations for high-performance systems are similar to the above-described current output PWM converter.

Another main branch of the tree diagram in **Fig. 1.15** is consti-

tuted by **resonant** topologies. The following brief introduction of basic resonant half-bridge topologies is related to Steigerwald's comparison-publication [87]. By adding an inductor L_s in series to the transformer in **Fig. 1.17 (a)**, a **series-resonant converter** is realised²¹. The series inductance determines and limits the primary current rather than the output filter inductor. Consequently, a voltage output rectifier such as the centre-tapped topology in **Fig. 1.16 (b)** is sufficient, reducing the voltage stress of the diodes because of the output capacitor clamping. On the contrary, the current stress for the filter capacitor is high and especially for a demanded low output voltage ripple the capacitance must be high. The main disadvantage of the series-resonant converter, however, is the inability to control the output voltage at very low or no load²² [87]. Series-resonant converters have typically a high part-load efficiency as the current in the components decreases with decreasing load. The main advantage of the series-resonant converter, and resonant converters in principle, is the approximately sinusoidal current waveforms due to the resonant circuit, decreasing the high-frequency effects in the transformer windings. Series-resonant converters have been suggested, amongst others, for load converter operation in [88] for ISDN-equipment (36 V to 75 V input and 5 V output voltage).

If in addition to the series inductor L_s a resonant capacitor C_p is added in parallel to the transformer in **Fig. 1.17 (a)** a **parallel-resonant converter** is realised²³. Similar to the series-resonant converter the parallel-resonant converter is more suitable for constant loads and small input voltage range, even though the parallel-resonant converter is able to be controlled for small and no load (for operation above the resonance frequency). However, the current in the resonant tank is more or less independent of the load, i.e. as the load decreases, the frequency increases to regulate the output voltage, but the resonant tank current is approximately unchanged; thus the part-load efficiency substantially suffers. An advantage is that the parallel-resonant converter is inherently short-circuit-proofed, as in case of a shortened parallel capacitor the square wave is applied to the series inductor and the current is

²¹The resonant tank is represented by the added series inductance and the input capacitors $C_{in,1}$ and $C_{in,2}$

²²The reason of the uncontrollable voltage is that the quality factor $Q = X_L/R_L$ (whereas X_L is the series impedance and R_L is the load resistance) is increasing for decreasing loads and the converter gain (V_{out}/V_{in}) is almost constant for $Q < 1$.

²³ Note, that C_p is the only resonant capacitor and the DC-link capacitors $C_{in,1}$ and $C_{in,2}$ serve only to split the input voltage as in the asymmetrical half bridge.

limited by this impedance.

The combination of both, series and parallel-resonant tank components, results in the **series-parallel-resonant converter (LCC)**, i.e. the resonant tank consists of a series capacitor (in case of the asymmetric half bridge in **Fig. 1.17 (a)** $C_{in,1}$ and $C_{in,2}$ can be used), a series inductor and the capacitor in parallel to the transformer. The benefits of the series- and parallel-resonant converters are thereby combined and the main disadvantages, i.e. the lack of no-load regulation and load-independent circulating currents, are solved with series-parallel-resonant converters, which can be operated with a large input voltage range. By transferring the parallel capacitance to the secondary side, the leakage inductance of the transformer can be used as series inductance for all three resonant topologies described so far.

The LCC-resonant converter arrangement of the inductor and the two capacitors is one of twenty-six possible configurations resulting in a resonant tank²⁴ out of the forty-eight theoretical combinations of arranging three resonant components, i.e. inductors and/or capacitors [116]. One further arrangement is obtained by swapping the parallel capacitor with an inductor. This type of converter has been discussed already in the eighties, e.g. [117], and has been later revisited for instance with the aim of an efficient telecom power supply with 50 V output voltage by [81] and is now mainly known as **LLC resonant converter** which is frequently analysed and discussed in literature, e.g. in [118–120]. The LLC-resonant converter as illustrated in **Fig. 1.17 (b)** is often suggested as front-end DC-DC converter in telecom power supply units with 300 V to 400 V input and 48 V output voltage, cf. [75, 82–85, 121]. The LLC is also suggested as ICT-load converter, e.g. for 48 V input and 1.5 V output voltage in [122] or the direct multiple voltage conversion 180 V to 370 V input down to 5 V and 1.8 V (20 W and 10 W) output voltage in [123]. Mainly because of the integration of the magnetic components, e.g. in [84, 120], the converter system can obtain a high power density.

Similar to the PWM-controlled half-bridge converter topologies the suggested resonant half-bridge converters for telecom PSUs are commonly applied for output power levels below 1 kW, as the efficient utilisation of the components is limited by the required VA-ratings for higher power conversion. The demanded server-cabinet power (e.g.

²⁴Only a few of the twenty-six resonant arrangements result in a load-independent transfer function and are suitable for power converters [116].

4.5 kW [124]) can consequently only be obtained by paralleling multiple power supply units if half-bridge topologies should be applied. The power density of the power stage in the cabinet can be further increased by applying high-performance PSUs with higher power ratings, which is possible with full-bridge converter topologies presented in the following.

Basic Full-Bridge DC-DC Converter While accepting an increased circuit complexity half-bridge topologies can be extended by one additional bridge leg enabling further degrees of freedom in respect to converter control and high performance power transfer. The principle classification of converter topologies in **Fig. 1.15** is also valid for full-bridge topologies, besides the above presented half-bridge converters. Both, resonant and PWM converters are suitable for the investigated performance and specifications of telecom power supplies.

PWM Full-Bridge Converters Full-bridge PWM converters can be operated either hard or soft-switched mainly depending on the control cycle of the switches, similar to PWM half-bridge converters. The extension by the second half-bridge leg enables the application of the positive and negative input voltage V_{in} as well as zero-voltage to the transformer. In hard-switched controlled PWM converters the zero-voltage is generated by turning all four switches off. In soft-switching converters the four switches are each turned on for half of the switching cycle T_p and the powering and free-wheeling states are generated by shifting the phase between the bridge legs. Within the free-wheeling states zero voltage is applied to the transformer; these states are generated if the two high-side or the two low-side switches are turned on. The on-time for the switches applied in the hard-switched inverter is, contrary to the soft-switching inverter switches, limited by the duty cycle D $T_p/2$ ($D \in (0, 1)$). The required current-rating for the switches and VA-rating for the transformer are consequently smaller. However, the achievable performance employing a soft-switching modulation is usually higher because the cooling volume can be reduced due to the decreased losses in the switches and the transformer volume is smaller because of the potentially higher switching frequency. Therefore, hard-switching converters are not further considered in the following.

Pulse-width-modulated full-bridge converters with **voltage output**, cf. left column in **Fig. 1.16**, are popular especially for high-power

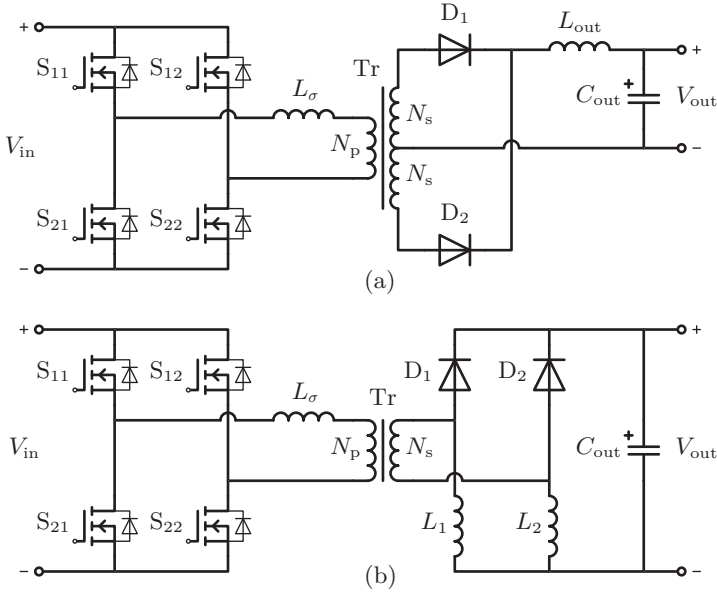


Figure 1.18: Typical phase-shift PWM full-bridge DC-DC converter with current output: (a) with centre-tapped transformer and LC-output filter, (b) with current doubler rectifier.

high-voltage applications such as the bi-directional power conversion between a fuel cell and the battery in FEVs (e.g. [67, 92, 94]). The application of voltage output PWM converters in telecom PSUs is possible, however, the inherently high current ripple in the transformer is unfavourable for a high-performance design because of the high VA-ratings and thus rather appropriate for low output power applications such as load converters, e.g. [89, 90, 125].

Pulse-width-modulated full-bridge DC-DC converters with **current output** designed for the telecom PSU specifications, cf. **Tab. 1.2**, are frequently proposed in scientific publications. The current output bridge rectifier as e.g. presented in [126–128] with the telecom-specific parameters for 1 kW to 2 kW converter, offers a simple transformer-winding arrangement, however, with the drawback that two rectifier diodes are concurrently in the current path resulting in higher conduction losses. For a higher output power demand, a centre-tapped

transformer with two rectifier diodes as shown in **Fig. 1.18 (a)** can advantageously be applied, e.g. in [96, 100, 129–131]. The drawbacks are the increased complexity of the transformer and the leakage inductance arising between the two secondary windings which is a further undesirable parasitic element in the current commutation path. The alternative to the centre-tapped rectifier is the current doubler shown in **Fig. 1.18 (b)** with a single secondary winding and split output inductors carrying concurrently approximately the half output current as presented e.g. [95] for a 5 kW telecom supply. The soft-switching in both converter topologies is achieved by adding an additional inductance in series to the transformer, which can be achieved by separating the primary and secondary winding(s) and thus increasing the leakage inductance²⁵.

The loss of the soft-switching ability at light load is often addressed as drawback of the PWM converter. The range can be adjusted by the energy stored in the series inductance, i.e. a compromise between the low-load losses and the inductance value have to be defined, as described in section 3.1, which has a major influence, e.g. on the amount of circulating energy and the current waveform and therewith associated the component size and conduction losses. Moreover, when losing the soft-switching such as Zero-Voltage-Switching (ZVS) the voltage ringing is even higher as for the hard-switched PWM converter because of the increased energy storage. By extending the standard PWM converter with additional circuit elements the ZVS-range can be extended down to light-load operation.

One possibility is connecting a saturable inductor in series with the transformer as presented e.g. in [132–134]. The inductance value can thereby be adjusted for low load current, i.e. a relatively high inductance is chosen. As soon as the primary current reaches the current saturation level of the inductor, the inductance rapidly decreases and the primary current rises with a high slope to the primary-side-related output current, while the energy in the inductance stays almost constant. The effective duty cycle, i.e. the time transferring energy from the input to the output, is thus increased and the circulating energy in the full bridge decreased, resulting in lower conduction losses. The disadvantages of this approach are the additional winding and core losses in the saturable inductor. If the resonant inductor is shifted from the primary

²⁵This approach is additionally advantageous in respect to the isolation of primary and secondary winding and a good common-mode EMI performance.

side to the secondary side²⁶, as for instance proposed in [98, 133], the flux changes only from zero to the positive saturation level, whereas the flux changes from the negative to the positive saturation level in case the inductor is connected to the transformer primary winding. The core-losses can thereby be decreased while accepting an additional saturable inductor.

A further possibility increasing the ZVS-range is the application of an auxiliary commutation circuit (Auxiliary Resonant Commutated Pole ARCP) as proposed e.g. in [135], which provides the required energy to remain soft-switching during light-load condition by switching an additional resonant inductor to the current commutation circuit. The complexity of the converter topology and control is thereby considerably increased, which might be accepted for high power converters, e.g. 100 kW in [136]. The demanded soft-switching can also be provided by an additional transformer [129] or an actively switched capacitive network [90].

A further drawback of the basic PWM converter topology is that the rectifier diodes (or synchronous-rectifier switches) are hard-switched requiring additional measures in order to limit the voltage ringing after the current commutation between the diodes. Different solutions have been proposed for reducing the voltage ringing amplitude such as voltage clamping circuits [126, 137] or active clamping circuits [138]. In section 2.3, an almost lossless magnetic snubber is introduced which efficiently damps the voltage ringing by removing the ringing energy from the transformer.

A detailed converter operation analysis of the current output PWM converters shown **Fig. 1.18** can be found in section 2.2 and section 3.1.

Resonant Full-Bridge Converters Besides the restriction of resonant action during current commutation as in fixed-frequency PWM converters, the resonant tank components can be extended for a complete resonant operation, cf. **Fig. 1.15**. As presented above for the half-bridge converter, the resonant tank can comprise two, three or more passive components. The most common resonant converter topologies are presented in **Fig. 1.19**. The combination of the series-

²⁶The saturable inductor is now split and an inductor is placed directly before each rectifier diode of the centre-tapped rectifier or, if a full-bridge rectifier is used, between the cathodes of the high-side and the anodes of the low-side diodes, cf. e.g. [133].

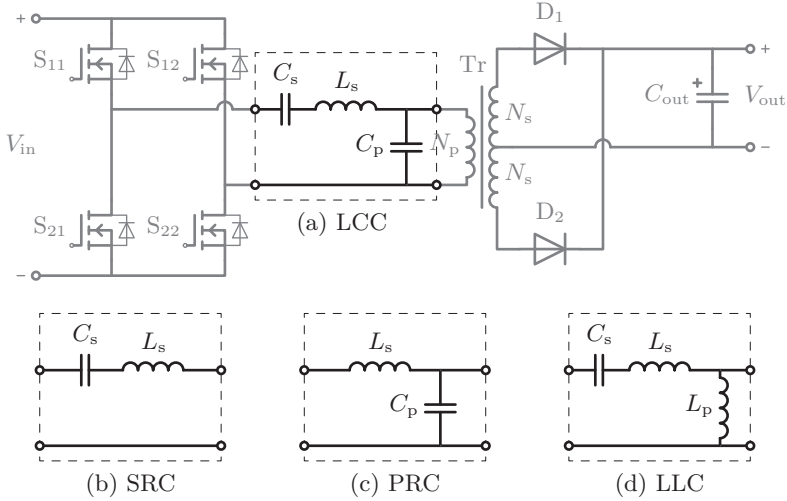


Figure 1.19: Resonant full-bridge DC-DC converter with centre tapped rectifier and voltage output: (a) series-parallel-resonant (LCC), (b) series-resonant (SRC), (c) parallel-resonant (PRC) (d) LLC converter.

resonant converter in **Fig. 1.19 (b)** and the parallel-resonant converter in **Fig. 1.19 (c)** results in the series-parallel-resonant DC-DC converter (LCC) in **Fig. 1.19 (a)**. A further topology applying three resonant components is the LLC resonant DC-DC converter in **Fig. 1.19 (d)**, similar to the half-bridge topology. The performance of the different resonant topologies is analogous to half-bridge converter.

Series-resonant full-bridge converters (SRC), e.g. proposed with a typical telecom specification and of 2.9 kW in [101], have a high part-load efficiency as the device currents decrease proportional to the load and the series capacitor blocks the DC-component avoiding a transformer saturation [104]. Similar to the half-bridge converter, the output voltage cannot be controlled at low or no-load conditions and the output filter capacitance must carry a high ripple current [104]. Compared to a phase-shift PWM converter, series-resonant converters have higher primary current peak- and RMS-values resulting in higher conduction losses (up to 70 % higher losses depending on the output voltage [101]).

Parallel-Resonant full-bridge converter (PRC) are applied in telecom applications as for example proposed in [105] for a 2.7-kW supply. The converter topology enables the operation down to no-load while accepting higher losses in the light-load range as the current in the resonant tank is almost independent from the load. The converter is inherently short-circuit-proofed like the half-bridge counterpart. In the comprehensive comparison of phase-shift PWM and parallel-resonant converters in [105] it is shown that the efficiency above 70 % of the rated output power is similar and therefore, the required cooling system volume is almost equal. Below the mid-load range, the PWM converter provides an even higher efficiency due to the higher amount of circulating energy in the resonant tank. However, if the PWM converter loses the soft-switching ability at light load, the efficiency decreases with a higher slope than for the parallel-resonant converter. The VA-ratings of the resonant converter are approximately 19 % higher resulting in a lower power density and higher costs. However, the parallel-resonant converter EMI performance is better than for the phase-shift PWM converter due to the reduced harmonic amplitudes and present frequencies as presented in [105]; the PWM converter show substantially worse EMI behaviour when losing the soft-switching ability. Therefore, bulkier EMI filters have to be applied for the phase-shift PWM converter.

The **series-parallel-resonant** full-bridge DC-DC converter (LCC) as shown in **Fig. 1.19 (a)** combines the desirable features of the series-resonant and parallel-resonant converters while overcoming the main disadvantages of both above-presented converters, i.e. increased low-load efficiency and no-load regulation ability. Similar to the half-bridge LCC converter, the parallel capacitor C_p can be shifted to the secondary side in order to apply the transformer leakage inductance as series inductor L_s and thereby increasing the power density of the converter. In [106] a performance comparison of phase-shift PWM converter and series-parallel-resonant converter for telecom application is presented for a 3-kW systems. The resulting performance presented is similar for both topologies [106]. For higher frequencies, the LCC approach might result in a higher converter efficiency, however, it is figured out that depending on the operation condition the PWM or the LCC-resonant converter is more appropriate. Typically the magnetics in resonant converters are bulkier than in PWM converters as the resonant inductor(s) must process the entire power transfer plus the additional circulating

VA²⁷. The resonant capacitors have to be suitable for high-current and high-voltage operation while the Equivalent Series Resistance (ESR) should be small in order to reduce the losses in the resonant tank. A disadvantage of the resonant converter is the slightly increased complexity of the variable frequency control. The sinusoidal currents and the ability of soft-switching for both, primary side and secondary switches are advantageous especially with respect to the EMI performance. A further advantage is that the output inductance can be small or omitted; moreover, an increased leakage inductance of the transformer, e.g. because of a high-voltage isolation between the windings, is not penalising the converter performance [139].

The **LLC-resonant** converter is often discussed as half-bridge topology, however, the three-components resonant tank can be applied in full-bridge converters as well, cf. **Fig. 1.19 (d)** [102]. While accepting the increased complexity for the gate drives and control of a second half-bridge branch, the full-bridge LLC-resonant converter can potentially offer an increased performance for high-power systems. In the half-bridge converter, only the first half cycle is used to charge resonant tank, which is discharged in the second half cycle, whereas in the LLC full-bridge both half cycles are utilised for transferring energy from the DC-source to the resonant tank. The RMS-current in a full-bridge switch is almost halved and because of the squared influence, the total conduction losses of the full-bridge switches can be halved and the reliability is increased because of the reduced current stress. Due to the decreased resonant tank RMS-current, conduction losses in the primary windings are decreased and because of the almost doubled voltage applied to the transformer primary side, the turns ratio can be increased, i.e. the turns number of the secondary winding can be reduced resulting in less winding losses, even though the kVA-rating of the transformer is almost similar to the half-bridge topology. Furthermore, the current and voltage stresses of the series-resonant tank components is reduced resulting in smaller conduction and core losses in the series inductor L_s ; furthermore, a series capacitor C_s with decreased voltage capability, potentially smaller loss-factor $\tan \delta$, and smaller component volume can be applied.

LLC- and LCC-resonant converters are both suitable topologies for a high-performance design and a general prediction which topology res-

²⁷The VA rating of resonant inductors is typically three times the power delivered [139].

ults in a better performance cannot be stated without an optimised design based evaluation²⁸. Similarly, for the comparison of the phase-shift pulse-width-modulated converter and the resonant converter a statement about a general performance advantage is barely possible, as according to the specific application and performance requirements one topology might be preferable. Moreover, as shown in the following chapters of this thesis, the performances are tightly coupled.

1.5 Contribution and Outline of this Thesis

The demand for high-performance power supplies for telecom applications is one of the major interests of the OEM's research and development in order to contribute to environmental protection and to be able to compete in the highly competitive market. The performance of the converter systems is subjected to physical laws and limitations, which consequently result in performance limitations.

The objective of this work is to identify the limitations of the most important physical performance indices of telecom DC-DC power supplies, the power density and efficiency, and furthermore, to shown the mapping of the design space into the performance space and the interdependency of the design parameters involved.

In the following section, chapter 2, automatic optimisation procedures are introduced to identify the maximum feasible power density of telecom DC-DC power supplies for a series-parallel-resonant converter (LLC) and a phase-shift PWM converter with current doubler rectifier. The optimisation results are validated with measurements on ultra-compact prototypes constructed based on the determined optimal design parameters.

The second important technical performance index for telecom PSUs is the efficiency of the power conversion. The evaluation of the efficiency limit of a phase-shift PWM telecom power supply and the underlying dependency on the design parameters are subject of chapter 3. A high-efficiency demonstrator was constructed to validate the calculated

²⁸The design of a low-power LLC- and a LCC-resonant full-bridge converter prototype in [103] results in a higher efficiency for the LLC resonant converter and a higher power density of the LCC-resonant converter because of the smaller magnetic components. Furthermore, the integration of a series and parallel inductance in the transformer of the LLC converter is very sensible in respect to manufacturing tolerances.

efficiency optimum with measurement results.

The comprehensive analytical models applied in the optimisation procedures have been validated with simulations and measurements. The sensitivity of the accuracy of these models on the optimal design is content of chapter 4.

Conference Papers

- ▶ U. Badstuebner, A. Stupar, J.W. Kolar, “Sensitivity of Telecom DC-DC Converter Optimization to the Level of Detail of the System Model”, *Proceedings of the Applied Power Electronics Conference and Exposition (APEC)*, Fort Worth, TX, March 6-10, 2011.
- ▶ U. Badstuebner, J. Biela, J.W. Kolar, “An Optimized, 99 % Efficient, 5 kW, Phase-Shift PWM DC-DC Converter for Data Centers and Telecom Applications”, *Proceedings of the IEEE/IEEE International Power Electronics Conference (ECCE Asia)*, Sapporo, Japan, June 21-24, 2010.
- ▶ D. Christen, U. Badstuebner, J. Biela, J. W. Kolar, “Calorimetric Power Loss Measurement for Highly Efficient Converters”, *Proceedings of the IEEE/IEEE International Power Electronics Conference (ECCE Asia)*, Sapporo, Japan, June 21-24, 2010.
- ▶ J. W. Kolar, J. Biela, S. Waffler, T. Friedli, U. Badstuebner, “Performance Trends and Limitations of Power Electronic Systems”, *Invited Plenary Paper at the 6th International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, March, 16-18, 2010.
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Honour: Best Presentation Award
- ▶ U. Badstuebner, J. Biela, B. Fässler, D. Hösli, J. W. Kolar, “An Optimized 5 kW, 147 Win⁻³ Telecom Phase-Shift DC-DC Converter with Magnetically Integrated Current Doubler”, *Proceed-*

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- ▶ J.W. Kolar, J. Biela, U. Badstuebner, “Impact of Power Density Maximization on Efficiency of DC-DC Converter Systems”, *Proceedings of the 7th International Conference on Power Electronics - Plenary Paper (ICPE)*, Daegu, South Korea, Oct. 22 - 26, 2007.
- ▶ J. Biela, U. Badstuebner, J. W. Kolar, “Design of a 5 kW, 1 U, 10 kW/ltr. Resonant DC-DC Converter for Telecom Applications”, *Proceedings of the International Telecommunications Energy Conference (INTELEC)*, Rome, Italy, pp. 677-685, Sept. 30 - Oct. 4, 2007.

Journal Papers

- ▶ U. Badstuebner, J. Biela, D. Christen, J.W. Kolar, “Optimization of a 5-kW Telecom Phase-Shift DC-DC Converter With Magnetically Integrated Current Doubler”, *IEEE Transactions on Industrial Electronics*, Vol. 58, No. 10, pp. 4736-4745, Oct. 2011
- ▶ J. Biela, U. Badstuebner, J.W. Kolar, “Design of a 5 kW, 1 U, 10 kW/ltr. Resonant DC-DC Converter for Telecom Applications”, *IEEE Transactions on Power Electronics*, Vol. 24, No. 7, pp. 1701-1710, July 2009.
- ▶ J. Biela, U. Badstuebner, J.W. Kolar, “Impact of Power Density Maximization on Efficiency of DC-DC Converter Systems”, *IEEE Transactions on Power Electronics*, Vol. 24, No. 1, pp. 288 - 300, Jan. 2009.

Patents

- ▶ U. Badstübner, J.W. Kolar, J. Miniböck, “Verfahren zur Begrenzung von Überspannungen an den Ausgangs-Dioden eines potentialgetrennten DC/DC-Konverters.” CH 704 460 (A2)

- J. Biela, U. Badstübner, “Verlustlose Überspannungsbegrenzung von Gleichrichterioden.” CH 700 418 (A2)

2

Power-Density-Optimised Systems

The maximisation of the power density has been the major physical performance driver for telecom power supplies in the 1990s as a result of the digitalisation and the global expansion of communication networks. Very compact converters became necessary in order to counteract the increasing demand for space for the ICT equipment and the power supply units. Compact power supplies reduce the need for declining raw material resources on the one hand and improve the cooling effectiveness on the other. These enhancements inherently enable a (partial) drastic reduction of the operating and purchasing costs. Above all, a compact design is a meaningful sales argument and increases the competitiveness of the power supply manufacturers in a highly competitive market.

Power density will remain one of the most important physical performance drivers due to the above-mentioned advances. Knowledge about the achievable power density is therefore of special interest for the manufacturers in order to analyse their own current market position and to generate road maps for future developments. This chapter is dedicated to an approach to identify and develop converter systems with, in principle, the highest feasible power density. This design approach is presented and validated for two different telecom DC-DC converter topologies: the series-parallel-resonant converter with centre-tapped secondary winding transformer and voltage output in section 2.1 and the phase-shift PWM DC-DC converter with current doubler rectifier in section 2.2. The optimisation process is based on comprehensive analytical models of the converter operation, the component losses and the resulting volumes. In addition to the respective highest converter-power-density, the procedure enables a profound discussion about the

interdependency of (free) design parameters and their influence on the resulting performance. The design approach and the analytical models used are validated by simulations and measurements on prototypes which have been constructed with the component values resulting from the proposed design process¹.

The disadvantage of the hard-switched rectifier diodes in PWM DC-DC converters requires an over-dimensioning of the voltage blocking capability, which commonly results in higher diodes losses and volumes (larger devices or heat sinks), or in the necessity of an additional voltage-limiting circuit. In section 2.3, a low-complexity magnetic snubber circuit is introduced, efficiently reducing and limiting the voltage ringing across the rectifier after the non-ideal current commutation.

2.1 Series-Parallel-Resonant Converter

The series-parallel-resonant (LCC) converter is a suitable topology for the specified 400 V to 48.56 V 5-kW telecom DC-DC converter which combines the advantages of the series- and the parallel-resonant converter as discussed in section 1.4. As a result of the specified power and the high output current a full bridge input stage in combination with a centre-tapped secondary winding transformer and two rectifier diodes has been chosen for an efficient power transfer, potentially resulting in a high power density.

In **Fig. 2.1** the LCC-resonant converter is shown with the parallel-resonant tank capacitance C_p transferred to the secondary side of the transformer in order to utilise the transformer leakage inductance (additionally) for the series-resonant tank inductance L_s or to enable the integration of the series inductance into the transformer. The basic current and voltage waveforms of the full bridge are similar to the LCC-resonant converter with primary-side parallel capacitor. However, the filter characteristics for the transformer change and the transformer winding current is equal to the almost sinusoidal resonant tank current rather than the trapezoidal current waveform behind the parallel capacitor C_p . The HF-losses of the transformer can thereby be reduced as the current contains fewer harmonics; however, the RMS-currents are higher in the transformer. Moreover, because the capacitor is transferred to the secondary side, the capacitance is changed (squared with

¹The results have been published in [140] and [141].

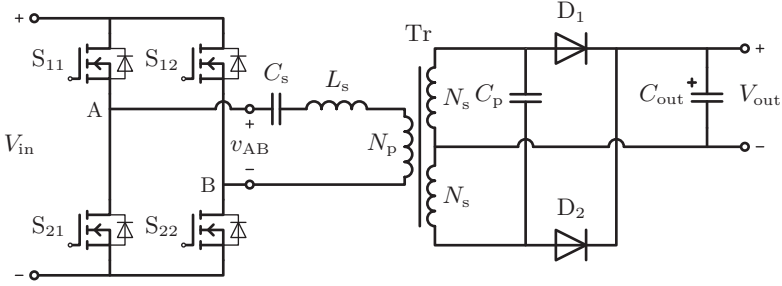


Figure 2.1: Schematic of the series-parallel-resonant (LCC) converter with centre-tapped secondary winding transformer and voltage output. (Note, the parallel capacitor C_p has been transferred to the transformer secondary side.)

the transformer transfer ratio $n = N_p/2N_s$ and as the voltage is stepped down according to the telecom converter specification, the current rating of the capacitor is increased whereas the voltage rating is decreased.

After (and before) the system of transformer and parallel capacitor C_p , the current and voltage waveforms applied to the rectifier, output filter stage, and resonant tank are similar independent of the arrangement of the two components. There are basically two suitable topologies for the output filter stage of the DC-DC converter, cf. section 1.4: the voltage output (capacitive C-filter) and the current output (inductive-capacitive LC-filter). A performance comparison with respect to the achievable power density of the filter stage is discussed in the following.

LC-filter versus C-filter

Depending on the implemented output filter, the characteristic current and voltage waveforms differ for a first-order C-filter and a second-order LC-filter as illustrated in **Fig. 2.2**², which in consequence have a significant influence on the optimum converter design and the component values.

If the LC-filter cf. **Fig. 2.2 (a)** is applied the output stage features characteristics of a current source and, with sufficiently large output inductance L_{out} , the current through the rectifier (D_1 and D_2) is almost

²Note, that in **Fig. 2.2** a special control strategy has been applied in order to operate one full-bridge leg with ZCS-condition and the other leg with ZVS-condition as further discussed below in this subsection.

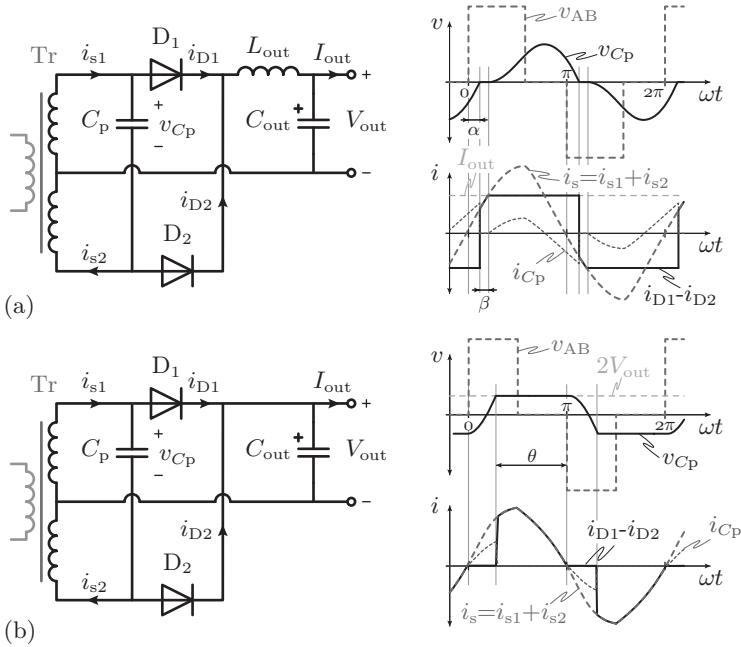


Figure 2.2: Suitable output filter stages for the telecom DC-DC converter with centre-tapped secondary winding transformer; schematic and basic waveforms for (a) LC-filter and (b) C-filter. (v_{AB} is the voltage applied to the resonant tank as illustrated in **Fig. 2.1**.)

rectangular, determined by the almost constant current through the output inductor. The current stress for the output capacitor C_{out} is therefore small and the specified output voltage ripple $v_{out,pp}$ can be realised with a small capacitance value.

For an analysis of the LC-filter two different modes have to be distinguished [142, 143]: the continuous voltage mode (CCV) and the discontinuous voltage mode (DCV) of the parallel capacitor C_p . The discontinuous voltage mode commonly occurs during heavy load condition which is shown in **Fig. 2.2 (a)**. For a specific angle β , cf. the current-diagram in **Fig. 2.2 (a)**, both rectifier diodes are conducting, starting with the zero-crossing of the parallel-capacitor voltage v_{Cp} and ending when the (transferred) resonant tank input current $i_s = i_{s1} + i_{s2}$ reaches the inductor current level which is almost equal to the output

current I_{out} . During that interval β , the capacitor voltage is clamped to zero, resulting in a distortion of v_{C_p} , which has to be considered in the analytical modelling [142, 143]. After that interval, one rectifier diode draws the almost constant inductor current and the remaining part of the almost sinusoidal resonant tank current ($i_s - I_{\text{out}}$) is utilised to charge or discharge the parallel capacitor C_p . Consequently, both centre-tapped windings are carrying the capacitor current i_{C_p} during the complete switching period causing additional losses in the transformer.

The characteristic output filter stage waveforms of a first-order capacitive filter are shown in **Fig. 2.2 (b)**. The capacitor voltage v_{C_p} is clamped to twice the output voltage V_{out} (in case the centre-tapped transformer is applied) for the current-conduction angle θ , cf. **Fig. 2.2 (b)**. During the charge and discharge-process of the parallel capacitor (angle $\pi - \theta$, where $|v_{C_p}| \leq 2V_{\text{out}}$) the rectifier diodes D_1 and D_2 are reversed biased and no current is transferred to the output. As soon as twice the output voltage is reached across C_p , one diode conducts the resonant current and only one of the centre-tapped windings is in the current path to the load and output capacitor. During the charging angle of the parallel capacitor ($\pi - \theta$) the filter capacitor C_{out} delivers the demanded output power and therefore the required output capacitance is significantly higher than in the LC-filter in order to meet the output voltage ripple specification. Moreover, the filter capacitor RMS-current is higher and has inherently to be carried by the diodes, windings, and the resonant tank, too, resulting in higher conduction losses.

The preselection of the filter topology for the high-power-density design is discussed in [144, 145]. The filter component values are determined based on the required voltage ripple ($\Delta v_{\text{out}} \leq 300 \text{ mVpp}$) and a maximum current ripple of $\pm 7.5\%$ for the LC-filter [144, 145]:

	C_{out}	R_{ESR}	L_{out}	$I_{C_{\text{out}},\text{RMS}}$
LC-filter	30 μF	-	5 μH	4.6 A
C-filter	470 μF	50 $\mu\Omega$	-	52 A

As identified above, the RMS-current values in the output capacitor and the capacitance itself are significantly higher for the C-filter compared to the LC-filter. With the capacitance per volume³ for electrolytic

³The characteristic component values relating capacitance per volume and

Table 2.1: Comparison of LC- and C-filter volume based on electrolytic and ceramic capacitors as presented in [144, 145].

	Electrolytic		Ceramic	
	Cylindrical	Cuboid	SMD-device	Mounted
$(\mu\text{F}/\text{cm}^3)$	170	134	111	90
$(I_{\text{AC}}/\text{cm}^3)$	0.25 A	0.19 A	41.6 A	35.1 A
LC-filter volume $(C_{\text{out}} + L_{\text{out}})$	Only capacitance considered: $0.22 \text{ cm}^3 + 40.9 \text{ cm}^3$		$0.32 \text{ cm}^3 + 40.9 \text{ cm}^3$	
	Ripple current I_{AC} included: $24.2 \text{ cm}^3 + 40.9 \text{ cm}^3$			
C-filter volume (C_{out})	Only capacitance considered: 3.7 cm^3		5.4 cm^3	
	Ripple current I_{AC} included: 273 cm^3			

and ceramic capacitors as presented in **Tab. 2.1** (taken from [144, 145]) the filter volume can be approximated. Electrolytic capacitors feature a higher capacitance per volume which is reduced if the more practically orientated cuboid-shaped outline is considered rather than the cylindrical shape. If only the theoretical capacitance value for C_{out} is considered, the LC-filter volume would result in approximately 41 cm^3 mainly determined by the high inductor volume ($> 40 \text{ cm}^3$). However, because of the high Equivalent Series Resistance (ESR) and the related low current-carrying capability of electrolytic capacitors, the resulting capacitor volume is almost 60 % higher and results in more than 65 cm^3 total filter volume. In case of a pure C-filter, the impact of the high ESR of electrolytic capacitors results in a tremendous volume increase: the actual filter volume would significantly increase from 3.7 cm^3 to the unacceptable volume of 273 cm^3 , which would result in an output capacitance $C_{\text{out}}=36 \text{ mF}$.

When applying ceramic capacitors, the resulting filter volume can be reduced due to the higher current-carrying capability, even though the capacitance per volume is smaller⁴. For the LC-filter the applica-

current-carrying capability in **Tab. 2.1** are based on compact state-of-the-art products [144, 145].

⁴The capacitances per volume in **Tab. 2.1** are specified for the net volume of a

tion of ceramic capacitors results in $V_C \approx 41 \text{ cm}^3$ which is only marginally higher than the volume calculated with the theoretical capacitance, as the filter volume is mainly determined by the output inductor. Considerable improvements can be obtained for the capacitive output filter when applying ceramic capacitors as the resulting filter volume decreases to 5.4 cm^3 (including the PCB-volume for mounting). The maximum thermally possible ripple current of 233 A allows the operation with reduced temperature stress.

Based on the results in **Tab. 2.1** the capacitive filter has been identified as the more suitable topology with regard to the high-power-density design and the LCC-resonant converter with centre-tapped secondary winding transformer and C-filter is therefore further investigated and optimised in this section.

Steady-State Waveforms of the LCC Converter with C-Filter

Resonant converters can be either controlled by switching frequency or duty-cycle variations. Half-bridge resonant converters are commonly frequency-controlled and the duty cycle is constant, i.e. the high- and the low-side switch are each turned on for one half of the switching period, which has been analysed e.g. in [146, 147]. Due to the second bridge leg, a full-bridge resonant converter features a further degree of freedom and can therefore be controlled by duty-cycle variations whereas the switching frequency is automatically adjusted [110, 148]. This control method can be beneficially⁵ applied to switch one leg with zero-current (ZCS) and the other with zero-voltage (ZVS)⁶ which is considered in the evaluation of the here investigated topology. If MOSFETs are applied in both bridge legs it is furthermore possible to switch the ZCS-leg slightly before the zero-crossing of the resonant current i_p in order recharge the parasitic capacitances of the MOSFETs and obtain ZVS in the ZCS-bridge-leg as well. In the following paragraph, the characteristic waveforms are briefly discussed as basis for the analytical modelling below in this section.

Generally, there are four main switching states: two powering states, in which the diagonal H-bridge switches are turned on and the positive or negative input voltage is thereby applied to the resonant tank, and

SMD-device including the additionally required PCB- and mounting volume.

⁵In high-power applications, IGBTs could for instance be implemented in the ZCS-leg and MOSFETs in the ZVS-leg [110, 149].

⁶ZVS is obtained for operation above the resonance frequency [150].

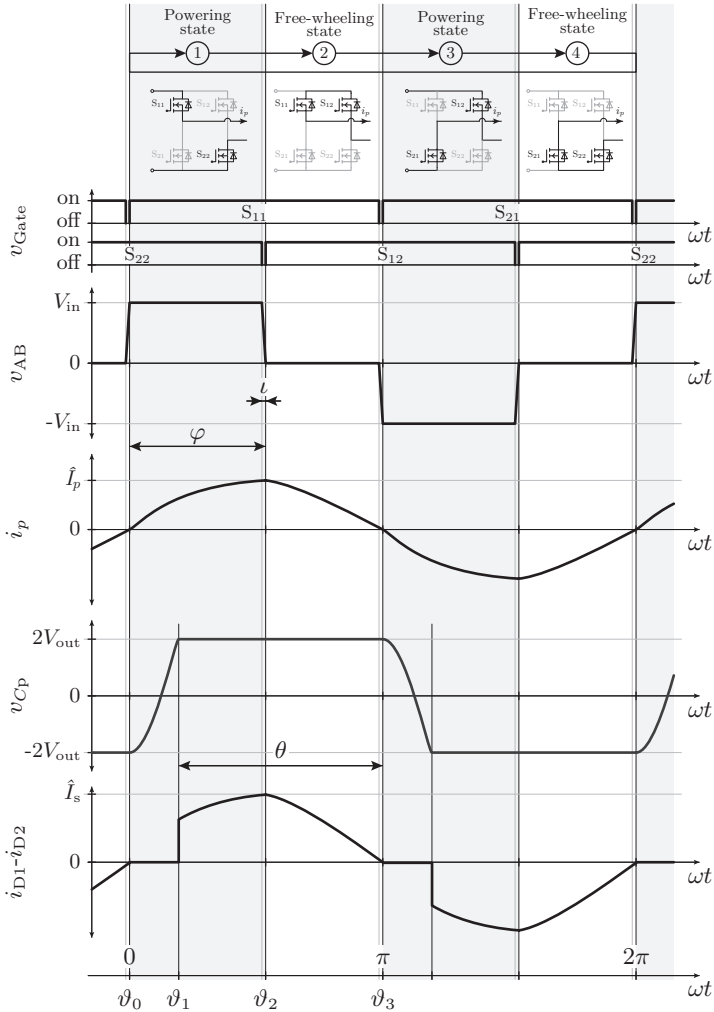


Figure 2.3: Characteristic current and voltage waveforms of the LCC-resonant converter with C-filter.

two free-wheeling states, in which the high-side or low-side switches are turned on short-circuiting the resonant tank. The variables defined and the description of the characteristic waveforms in the following refer to

Fig. 2.3 and Fig. 2.4.

$\vartheta_0 \leq \omega t \leq \vartheta_1$ (**Fig. 2.4 (a)**) At the beginning of the first powering state ①, the resonant current i_p crosses zero and the high-side switch S_{11} of the ZCS-bridge-leg is turned on. Since the low-side switch S_{22} is conducting (turned on in the preceding free-wheeling state), the positive converter input voltage is applied to the resonant tank ($v_{AB} = V_{in}$). The current in the rectifier diode D_2 decreases to zero at the end of the preceding state (ZCS switching scheme) and D_2 is at ϑ_0 reverse-biased. As the voltage over D_1 is still negative (at ϑ_0 : $v_{D1} = v_{Cp} = -2V_{out}$), both rectifier diodes are reverse-biased and the transferred resonant current is entirely utilised for charging the parallel capacitor C_p from $-2V_{out}$ to $2V_{out}$. Note, that during this interval both secondary windings are carrying the transferred resonant current and the effective transfer ratio n is now halved, i.e. $n' = N_p/2 N_s$.

$\vartheta_1 \leq \omega t \leq \vartheta_2$ (**Fig. 2.4 (b)+(c)**) At the time $\omega t = \vartheta_1$, the parallel-capacitor voltage v_{Cp} reaches twice the output voltage and the rectifier diode D_1 starts conducting and therefore v_{Cp} is clamped to $2V_{out}$. In this interval the converter is still operating in the powering phase ①, however the actual power transfer from the input to the output starts with $\omega t = \vartheta_1$. The power transfer in state ① ends when the low-side switch S_{22} is turned off. The active power transfer angle is therefore defined as $\varphi - (\pi - \theta)$. The turn-on of the high-side switch S_{12} is delayed by $\omega t = \iota$ (interlock-delay) in order to guarantee the resonant discharge of the parasitic MOSFET output capacitance of the high-side switch and simultaneously recharging of the parasitic low-side switch capacitance, i.e. the high-side switch is turned on at zero-voltage (ZVS).

$\vartheta_2 \leq \omega t \leq \vartheta_3$ (**Fig. 2.4 (d)**) With the ZVS turn-on of the high-side switch S_{12} at $\omega t = \vartheta_2$ the resonant current is free-wheeling in the primary side and reaches zero at $\omega t = \vartheta_3$. Slightly before the current zero-crossing the high-side switch S_{11} of the ZCS-leg is turned off allowing the low-side switch S_{21} to turn on with zero current and possibly zero voltage at $\omega t = \vartheta_3$, where the free-wheeling state ② ends.

After the ZCS-turn-on of S_{21} the second powering phase ③ starts and the negative input voltage is applied to the resonant tank. The states of the first half of the switching period $\omega t \in \langle 0, \pi \rangle = \langle \vartheta_0, \vartheta_3 \rangle$ are

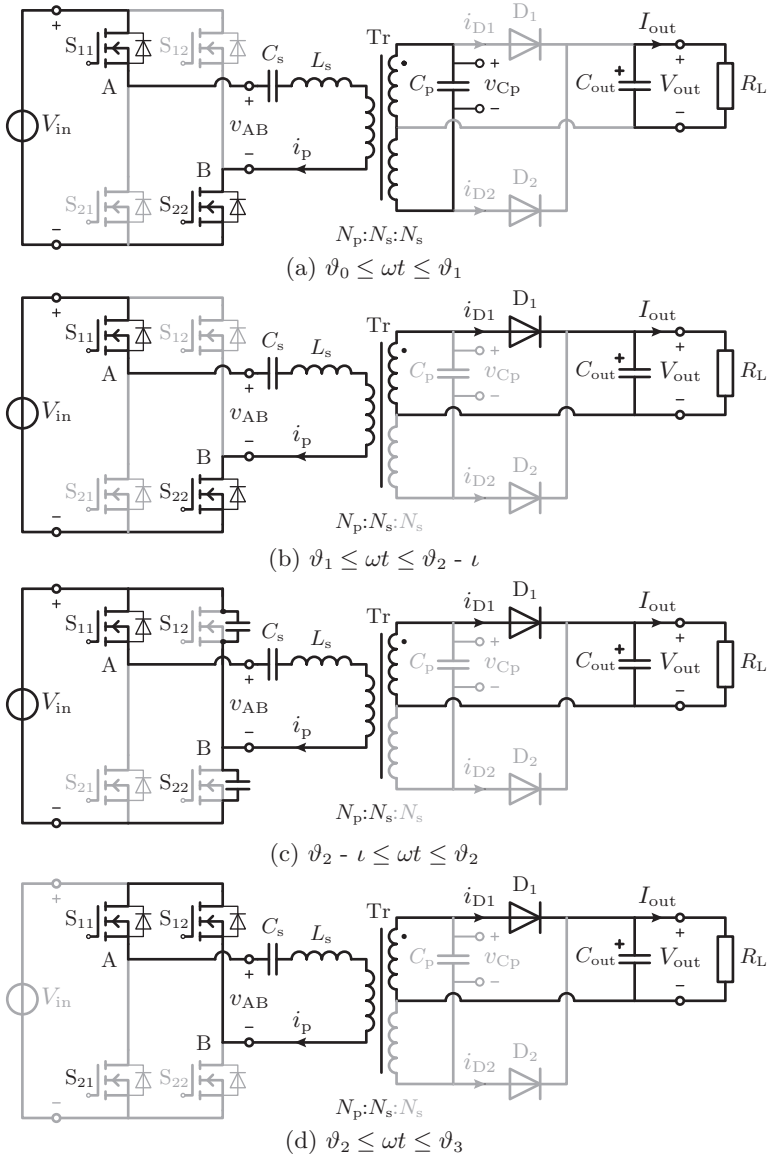


Figure 2.4: Switching states with highlighted current paths for the first half cycle of the LCC-resonant converter with C-filter.

now recurring with inverted voltage and current values, cf. **Fig. 2.3**: powering state ③ and free-wheeling state ④.

Fundamental-Frequency-Analysis-Based Design

The design of a resonant converter system is generally more complex compared to pulse-width-modulated systems. Especially the determination of the resonant tank component values L_s , C_s and C_p of the series-parallel-resonant converter is challenging because of the inherently higher amount of free parameters during the design process, as well as the interdependency and strong influence on the converter operation and performance [151, 152]. A basic analysis of resonant converter systems, which enables an analytical-based converter design, is presented in the frequently referenced comparison of half-bridge resonant topologies by Steigerwald [87]. The analysis there is based on the first harmonic representation of the voltage and current waveforms. With the assumption of a sinusoidal resonant tank current a fundamental frequency analysis delivers adequate results as the higher harmonics of the resonant tank voltage v_{AB} are not contributing to the power transmission from the input to the output of the resonant tank in this case. The LC-output filter connected to the resonant tank is represented by an equivalent AC-resistance in [87]. This approach, however, is less adequate for a capacitive output filter as the power is only transferred during the conduction angle θ and the equivalent load at the tank output cannot be considered as purely resistive [110]. Extended analyses based on the fundamental frequency considering the capacitive output filter are presented e.g. in [146, 147, 153]. Ivensky proposed a first-harmonic analysis in [147, 153] which is based on an equivalent RC-model allowing a straight-forward calculation of the operating point. This model has been adapted and extended for the series-parallel-resonant converter with secondary-side connected parallel-resonant tank capacitor C_p and the centre-tapped secondary winding transformer as shown in **Fig. 2.1**, furthermore considering the applied duty cycle and frequency control. The resulting analytical description is summarised in the following as basis for a discussion about the influence of the value selection of the resonant tank components on the converter design. The deviation of this model following the proposed approach in [147] and further explanations are presented in the appendix (section A).

The fundamental frequency analysis is based on the following assumptions:

- sinusoidal transformer primary (resonant tank) and secondary side currents (i_p and $i_s = i_{s1} + i_{s2}$)
- constant input and output voltages V_{in} and V_{out}
- ideal components, i.e. efficiency $\eta = 1$.

Furthermore, the transformer primary side resonant tank components (L_s , C_s), voltage and current waveforms are transferred to the rectifier side for this analysis.

The starting point of the analysis is the parallel-capacitor voltage v_{C_p} , cf. **Fig. 2.5**, which is clamped to $2V_{out}$ during the conduction angle θ and charged by half⁷ of the secondary side resonant current $i_s = i_{s1} + i_{s2}$ during $0 \leq \omega t \leq \pi - \theta$ (and $\pi \leq \omega t \leq 2\pi - \theta$, respectively), resulting in

$$v_{C_p}(\omega t) = \frac{2V_{out}}{1 + \cos(\theta)} [(1 - \cos(\theta)) - 2\cos(\omega t)] \quad (2.1)$$

for that interval. In the course of the capacitor voltage determination the peak value of the resonant current can be determined, cf. section A:

$$\hat{I}_s = \frac{8V_{out}\omega C_p}{1 + \cos(\theta)}. \quad (2.2)$$

The expression for the conduction angle θ can be found with the equation for the average output current, cf. section A (A.6) and (A.7), which results in:

$$\theta = 2 \tan^{-1} \left(\sqrt{\frac{8}{\pi} \frac{1}{\omega R_L C_p}} \right). \quad (2.3)$$

Based on the analytical description of the capacitor voltage, the first harmonic components (Fourier coefficients $a_{v(1)}$, $b_{v(1)}$ and the phase angle $\xi_{v(1)}$, cf. **Fig. 2.5**, between the zero-crossing of the resonant current at ϑ_0 and the fundamental capacitor voltage $v_{C_p(1)}$) can be determined. The ratio between the peak voltage $\hat{V}_{C_p(1)}$ and the converter output voltage V_{out} is defined as,

$$\frac{\hat{V}_{C_p(1)}}{V_{out}} = 2k_v = \frac{4}{\pi} \frac{\sqrt{[\pi - \theta + \sin(\theta) \cos(\theta)]^2 + \sin^4(\theta)}}{1 + \cos(\theta)} \quad (2.4)$$

⁷Note, the effective turns ratio during the charging phase $0 \leq \omega t \leq \pi - \theta$ and $\pi \leq \omega t \leq 2\pi - \theta$ is $N_p/2 N_s$.

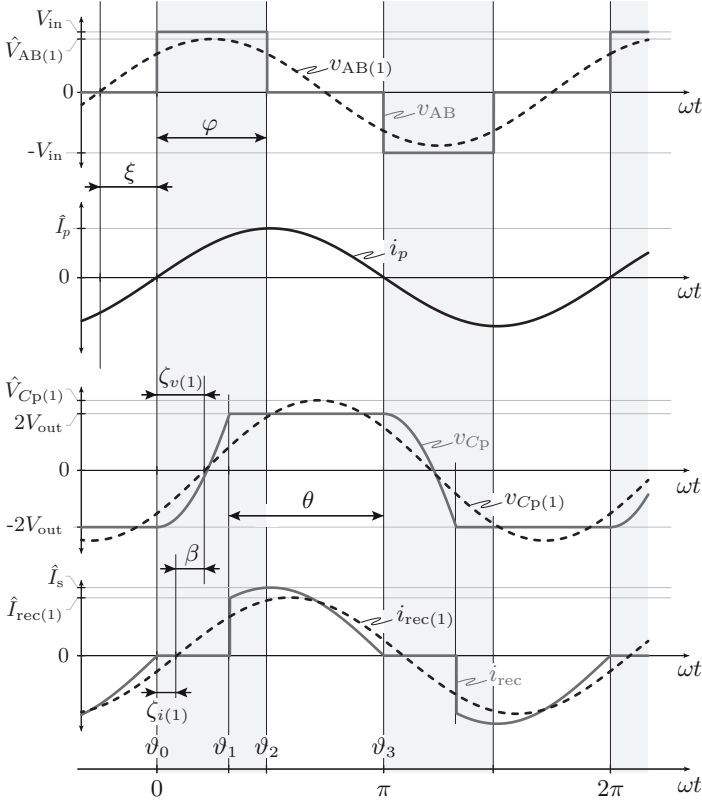


Figure 2.5: Basic voltage and current waveforms of the fundamental frequency analysis of the series-parallel-resonant converter with centre-tapped secondary winding transformer, secondary-side parallel capacitor C_p and C-output filter.

with the voltage factor k_v which could be approximated according to [147] by,

$$k_v \approx 1 + 0.27 \sin\left(\frac{\theta}{2}\right). \quad (2.5)$$

In the next step the first harmonic of the rectifier input current i_{rec} is determined. This current is zero during the charging process of C_p and equal to the transferred resonant current during the conduction phase θ , cf. **Fig. 2.5**. Considering the phase angle $\zeta_{i(1)}$ between the

zero-crossing of the resonant current i_p and the fundamental rectifier input current $i_{\text{rec}(1)}$,

$$\zeta_{i(1)} = \tan^{-1} \left(-\frac{\sin^2(\theta)}{\theta - \frac{1}{2} \sin(2\theta)} \right), \quad (2.6)$$

the angle between the fundamental rectifier input current $i_{\text{rec}(1)}$ and the fundamental parallel-capacitor voltage $v_{Cp(1)}$ can be defined,

$$\beta = \zeta_{v(1)} - \zeta_{i(1)}. \quad (2.7)$$

The equivalent RC-circuit connected to the output of the resonant tank, cf. **Fig. A.3** on page 261, can be determined with (2.7) as

$$\begin{aligned} R_e &= 2 k_v^2 R_L, \\ C_e &= \frac{\tan |\beta|}{2 k_v^2 \omega R_L}, \end{aligned} \quad (2.8)$$

with the equivalent resistance R_e and equivalent capacitance C_e .

At the input of the resonant tank the positive or negative converter input voltage V_{in} is applied during the powering phases and the resonant tank is short-circuited during the free-wheeling phases. The fundamental frequency analysis results in the voltage amplitude

$$\hat{V}'_{AB(1)} = \frac{4 V_{\text{in}}}{n \pi} \cos(\xi), \quad (2.9)$$

where ξ is the phase angle related to the zero-crossing of the resonant tank current (given by (A.37) on page 264). As illustrated in **Fig. 2.5** this phase angle is equal to half of the free-wheeling phase angle because of the applied control scheme; therefore, the powering phase and free-wheeling phase angles (φ and $\pi - \varphi$ cf. **Fig. 2.3**) can be analytically described with the resonant tank components and the equivalent RC-circuit. The ratio between the fundamental voltage amplitude of the input and output of the resonant circuit can be derived from the resonant tank circuit, cf. **Fig. A.3 (a)** on page 261, as

$$\frac{\hat{V}_{Cp(1)}}{\hat{V}'_{AB(1)}} = \frac{V_{\text{out}}}{V_{\text{in}}} \frac{n \pi k_v}{4} \frac{2}{\cos \xi} = k_v^* \frac{2}{\cos \xi}, \quad (2.10)$$

where the voltage factor k_v^* is given by [147],

$$k_v^* = \dots = \frac{1}{\sqrt{\left\{1 - \frac{C_p}{C'_s} \left[\left(\frac{\omega}{\omega_s} \right)^2 - 1 \right] \left(1 + \frac{\tan|\beta|}{\omega C_p R_e} \right) \right\}^2 + \left\{ \frac{C_p}{C'_s} \left[\left(\frac{\omega}{\omega_s} \right)^2 - 1 \right] \frac{1}{\omega C_p R_e} \right\}^2}} \quad (2.11)$$

with the resonances frequency of the series-resonant circuit ω_s

$$\omega_s = \frac{1}{\sqrt{L_s C_s}}. \quad (2.12)$$

For the following discussions the normalised output voltage V_{out}^* and the quality factor Q_s are introduced⁸:

$$V_{out}^* = \frac{n V_{out}}{V_{in}} = \frac{4}{\pi} \frac{k_v^*}{k_v} = \frac{\cos^2(\xi)}{\sin^2(\frac{\theta}{2})} \quad (2.13)$$

and

$$Q_s = \frac{\omega_s L_s}{R_L}. \quad (2.14)$$

According to (2.14) the quality factor Q_s is decreasing with the resistive load (reciprocally with the load resistance R_L) and is further dependent on series-resonant components L_s and C_s .

Discussion: Parameter Influence The equations presented above show the strong influence of the resonant tank components L_s , C_s , and C_p on the converter operation, e.g. concerning switching frequency, load-dependent frequency band and current amplitudes, and are thereby determining the resulting converter performance. The theoretical possibility of component value selections is almost unlimited and further complicated by the three interdependent degrees of freedom. Practical limitations for the converter design can be obtained from the fundamental frequency analysis as discussed in the following paragraph.

The switching frequency is mainly determined by the series-resonant circuit, i.e. with the aspired converter control the full-load switching

⁸The derivations of (2.13) and (2.14) are presented in the appendix A on page 255ff. and the resulting curves for a specific set of parameters are illustrated in **Fig. A.4** on page 266.

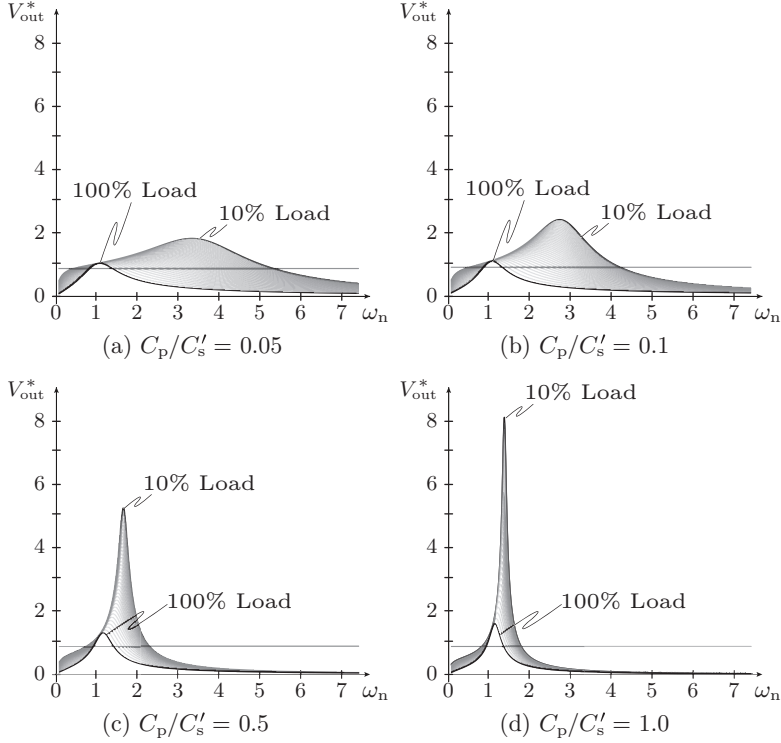


Figure 2.6: Normalised output voltage V_{out}^* versus normalised frequency $\omega_n = \omega/\omega_s$ for different resonant tank capacitor ratio C_p/C'_s .

frequency is slightly higher than the series-resonant frequency in (2.12) and is increasing with decreasing load. The parallel-resonant capacitor C_p is influencing the rectifier conduction angle θ which defines the power transfer duration and should be therefore high, i.e. a value close to π is desired. Conferring (2.3), the conduction angle θ is converging to zero for high parallel capacitances C_p and converging towards π for very small values of C_p , which would be desirable in terms of switching-period utilisation. The parallel-resonant capacitor C_p and in this way the resonant capacitor ratio C_p/C'_s are further mainly determining the operating-point frequency band from full load to no-load as illustrated

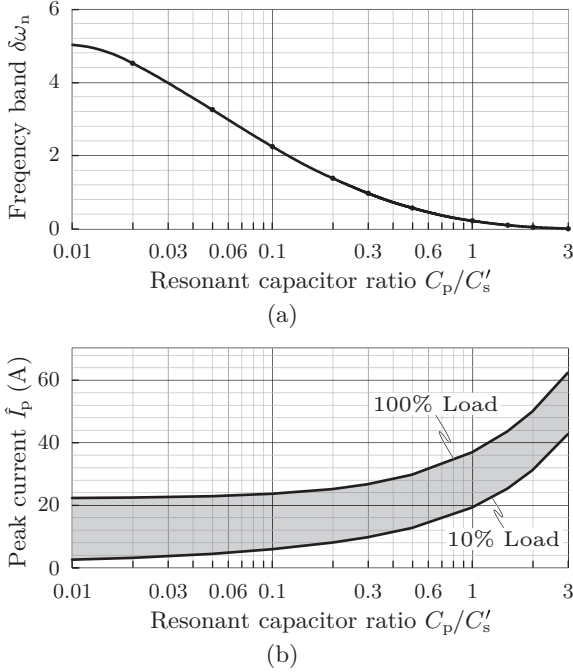


Figure 2.7: Influence of the resonant tank capacitor ratio C_p/C'_s on: (a) frequency band $\delta\omega_n = \omega_{n,(100\% \text{ Load})} - \omega_{n,(10\% \text{ Load})}$ and (b) the primary side resonant current peak \hat{I}_p .

in **Fig. 2.6** for the normalised output voltage V_{out}^* ⁹. As presented in **Fig. 2.6**, higher transfer ratios C_p/C_s result in higher peak values of V_{out}^* and a tighter load-depending array of curves. As the intersection of the fixed normalised output voltage $nV_{\text{out}}/V_{\text{in}}$ and the load-depending curve approximately determine the respective operating point, a high resonant capacitance value is preferable in order obtain a small load-dependent frequency variation, contrary to the desired small value of C_p to allow a high rectifier conduction angle θ . Small values of the series-resonant capacitor C_s additionally result in the acquired tight

⁹The normalised output voltage V_{out}^* is determined, cf. (2.13), by the voltage factors k_v and k_v^* ((2.4) or (2.5), respectively, and (2.11)). However, the influence of C_p/C_s on the frequency band is not directly apparent from these equations and is therefore graphically analysed with **Fig. 2.6**.

switching frequency band, however, cf. (2.12), the absolute switching frequency is high in this case, potentially resulting in higher frequency-dependent losses. In addition to the broad switching frequency band, a too small resonant capacitor ratio results in the challenge of ensuring the controllability at light load as the converter performance is inherently converging to that of a series-resonant converter.

The influence of the parallel-capacitor ratio on the switching frequency band $\delta\omega_n$, which is defined as the frequency range between the operation frequencies at full load and 10 % load, is additionally illustrated in **Fig. 2.7(a)**. The range is tight in case of a parallel-resonant converter operation, i.e. the parallel capacitance prevails notably the series capacitance. The disadvantage of a parallel-resonant converter-like operation are the higher RMS-currents in the circuit devices as discussed in section 1.4 and illustrated in **Fig. 2.7(b)** for the amplitude of the resonant tank current \hat{I}_p for full load and 10 % of the nominal output power. The high amount of reactive power for parallel-resonant converter operation therefore results in higher losses at full load and, moreover, in a significantly lower part-load efficiency¹⁰.

In addition to the resonant capacitor ratio, the quality factor Q_s of the series-resonant circuit determines the current stress and losses in the components. As shown in **Fig. 2.8**, a parameter design which leads to a high full-load quality factor results in lower peak-currents of the resonant tank and higher quality-factor variation from full load to 10 % load; low Q -factor designs result in both, higher full-load and higher part-load RMS-currents. The drawbacks of the high Q , however, are the high amount of energy in the magnetic devices and the inherently higher volume of those components.

The brief overview of the parameter influence on the converter operation explained above indicates the challenging and commonly iteratively solved design process. The practical design considerations initially include the determination of a feasible switching frequency in order to limit the complexity of the control and, with expert knowledge, to get a first insight into the volume, size and losses to be expected. In close relationship with the determination of the switching frequency is the definition of the quality factor which is practically limited by the size of the resonant inductor ($Q < 5$ [146]). The definition of the parallel capacitor and the resonant tank capacitor ratio C_p/C_s is basically a

¹⁰Directives as the Energy Star® requirements for computer servers [27] are most-likely not fulfilled with this performance.

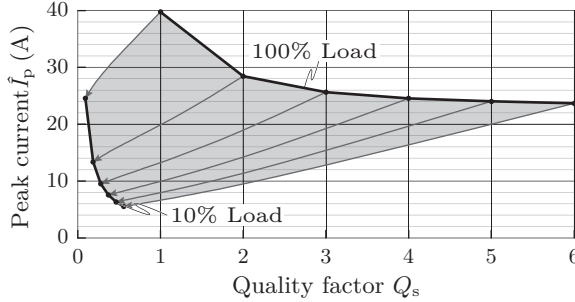


Figure 2.8: Primary side resonant tank current peaks \hat{I}_p in dependency of the initial quality factor Q_s .

trade-off between the switching frequency band (small C_p/C_s) and a small ratio of resonant tank current amplitude and average input current \hat{I}_p/I_{in} (high C_p/C_s). Further practical limitations are given by the components, e.g. maximum current ratings of the semiconductors and voltage rating of the resonant tank capacitors. This design process requires a comprehensive knowledge base in that area. Moreover, the determination of an optimised design according to a performance index (or even multiple performance indices) is difficult and time-consuming for such a complex power electronic system. An appropriate selection of design parameters is provided by an automatic design procedure enabling the optimum design, i.e. the determination of the maximum achievable power density in this chapter, which is introduced in the following subsection.

2.1.1 Design Process of Power-Density-Optimised LCC-Resonant Converter

The fundamental frequency analysis explained above shows the impact of the resonant tank component values selection on the converter operation and indicates the major influence on the resulting power density of the converter system. The actual design procedure determining the component values, such as for the resonant tank and transformer (geometry and windings), which eventually result in the optimal design, i.e. the converter with highest achievable power density, has been suggested in [144, 145]. The proposed flow chart of an optimisation procedure as

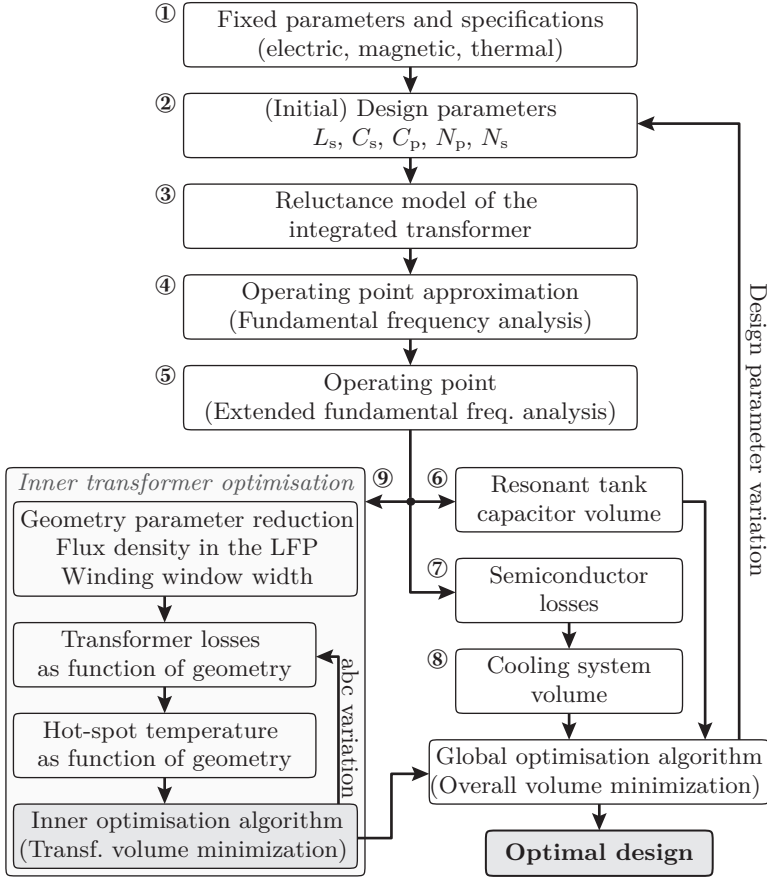


Figure 2.9: Automatic design procedure for optimising the series-parallel-resonant converter (LCC) in respect to power density [145].

illustrated in **Fig. 2.9** automatically determines the optimal component values for the power-density-optimal design which is briefly summarised in the following paragraphs. The underlying models used in the optimisation procedure are presented in next section 2.1.2.

The first step of the optimisation procedure (step ①) is the definition of preset electric, magnetic, and thermal parameters and the converter specifications (input and output voltage, output power, ambient tem-

perature), thermal limitations of applied materials and components, as well as material characteristics, e.g. Steinmetz parameters and thermal resistances.

In the next step ②, initial values of the design parameters (resonant tank component values L_s , C_s , C_p , and transformer primary and secondary side turns numbers N_p and N_s) can be specified. The initial set of design parameters ideally has no influence on the resulting optimised component values, however, potentially reduces the computation time for the optimised design.

With regard to a compact design an integrated magnetic component is considered in the optimisation process, combining series inductance L_s and transformer Tr in a single core¹¹. The component values of the underlying reluctance model of the integrated transformer are determined based on the set of (initial) design parameters in step ③.

In order to reduce the computation time in the next step of the procedure – the determination of the operating point with the associated component voltage and current waveforms, and the flux distribution – an approximated operating point is calculated based on Steigerwald's AC-analysis by determining an equivalent AC-resistance [87]. The switching frequency is thereby determined analytically as presented in [149].

The solution space of the extended fundamental analysis is restricted with the approximated operating point in step ⑤, where the operating point is derived numerically by a set of analytical equations considering higher harmonics of the resonant tank current. The corner stone for the following loss calculation is placed with the determination of the operating point in step ⑤, i.e. the calculation of all relevant component voltage, current and flux waveforms. As the accuracy of the analytical description of the converter operating point is propagated in the loss and volume calculation, the increased computation time because of the – at least – the third harmonic comprehension is justified for the sake of obtaining accurate optimisation results.

The volume and losses of the resonant tank capacitors C_s and C_p can be directly determined in step ⑥ with the current load and switching frequency calculated in step ⑤ and the specified material specifications in step ①.

The switching, conduction, and gate drive losses can be further dir-

¹¹The resulting magnetic component composed of the series inductance and the transformer is named integrated transformer in the following.

ectly determined in step ⑦ with the frequency and respective RMS and turn-off current values from step ⑤ and the underlying analytical models of the semiconductor devices (full-bridge MOSFETs and rectifier diodes). The calculated losses together with the parameters specified first (step ①), e.g. ambient temperature, thermal resistances, maximum junction temperature, and heat sink materials, are applied in step ⑧ to calculate the volume of the semiconductor heat sinks including the high-performance fan for the forced air cooling system based on the Cooling System Performance Index (CSPI) introduced by Drofenik in [154],

$$\text{CSPI} = \frac{1}{R_{\text{th},\text{S-a}} V_{\text{CS}}} \left(\frac{\text{W}}{\text{K dm}^3} \right), \quad (2.15)$$

with the thermal resistance of the heat sink $R_{\text{th},\text{S-a}}$ from the base plate surface to ambient and the cooling system volume V_{CS} .

The geometry parameters of the integrated transformer are determined in an inner optimisation loop in step ⑨ in order to reduce the number of design parameters as defined in step ② and thereby the computation time of the global optimisation loop. Inside, the winding window width is there primarily determined by calculating the optimal foil thickness applying Hurley's analytical formula proposed in [155], depending on the calculated switching frequency and turns number in the present loop-pass. A second geometry parameter can be eliminated by setting the flux density of the Leakage Flux Path (LFP) to the same value as the middle leg, which is clarified in section 2.1.2. The remaining three geometry design parameters are determined by the inner optimisation algorithm, where firstly the winding and core losses in the transformer are determined in dependency of these parameters and secondly, with an underlying thermal model of the integrated transformer, the hot-spot temperature is calculated. The inner optimisation algorithm varies the three remaining geometry parameters while keeping the maximum temperatures of the windings and the core as well as the maximum flux density below the specified limits (in step ①) until the minimum transformer volume is found. Practical limitations of the geometry parameters resulting from the manufacturing process are further considered as constraints in the inner optimisation loop.

The sum of the heat sink volume, capacitor volume, and optimised integrated transformer volume for the present set of design parameters (as defined in step ②) are forwarded to the global optimisation algorithm which changes the free design parameters of the outer loop

(step ②) until the global volume minimum for the specified constraints is found.

This design procedure has been applied for the power-density optimisation of the series-parallel-resonant telecom DC-DC converter. The optimisation results are presented in the section 2.1.3 and previously, in the next subsection, the analytical models applied in the procedure are summarised.

2.1.2 Analytical Converter Models

The underlying analytical models for the design procedure described are summarised in this subsection according to the sequence of evaluation in the optimisation procedure. Firstly, the analytical converter model determining the operating point with the respective relevant voltage and current waveforms is described. The models determining the losses and volumes of the resonant tank capacitors, the semiconductors and the resulting cooling system are explained in the next step. Finally the thermal models for the integrated transformer are introduced. The model descriptions are published in [144, 145].

Analytical Converter Operating Point Model

The determination of the operating point, i.e. the calculation of the switching frequency, duty cycle, and phase angles, and the thereby resulting possibility of computing all relevant device's voltage and current waveforms is the cornerstone of the following calculation of the losses and volumes. The model accuracy for that first step is therefore important in order to obtain reliable overall optimisation results. The analysis of the operating point is partly based on the extended fundamental analysis shown in [143] and [142], adapted for the use of a capacitive output filter instead of the there-applied LC-output filter and for the control method as described in the introduction of section 2.1, i.e. for one leg switched with ZVS-condition and the other with ZCS-condition. The basic idea of the analysis is to determine the input impedance Z_{in} of the resonant circuit in order to determine, for example, the switching frequency and duty cycle. Included in the following derivations of the operating point equations is an underlying reluctance model of the integrated transformer. Furthermore, the analysis is based on the following assumptions:

- The resonant currents of the primary and secondary side of the transformer (i_p and $i_s = i_{s1} + i_{s2}$) are sinusoidal with a 3rd harmonic component.
- All applied components (passive and active) are ideal.
- The output voltage is constant, i.e. the output filter capacitor C_{out} is sufficiently large.
- The converter operates with the described control scheme for all operating points.

The third harmonic of the resonant current is considered in addition to the fundamental frequency in order to increase the model accuracy.

The start of the derivation is, similar to the introduced fundamental frequency analysis on page 60ff., the determination of the parallel-capacitor voltage v_{Cp} , cf. (2.1) and **Fig. 2.5** on page 71¹²,

$$v_{Cp}(\omega t) = \begin{cases} \frac{2 V_{out}}{1 + \cos(\theta)} [(1 - \cos(\theta)) - 2 \cos(\omega t)] & \text{for } 0 \leq \omega t < \pi - \theta \\ 2 V_{out} & \text{for } \pi - \theta \leq \omega t < \pi \end{cases} \quad (2.16)$$

assuming that a sinusoidal resonant current during the charging phase of the parallel capacitor $0 \leq \omega t < \pi - \theta$. The resonant current through the secondary windings is represented by the first and third harmonics¹³,

$$i_s = \hat{I}_{s(1)} \sin(\omega t) + \hat{I}_{s(3)} \sin(3\omega t), \quad (2.17)$$

with the amplitudes of the respective harmonic $\hat{I}_{s(\nu)}$. The resonant current i_s is charging the parallel capacitor C_p from $-2 V_{out}$ to $2 V_{out}$ during the interval $\omega t \in \langle 0, \pi - \theta \rangle$ with an effective turns ratio $N_p/2N_s$, which is generally assumed for the following derivations. During the interval $\omega t \in \langle \pi - \theta, \pi \rangle$ the resonant current is supplying the load via the rectifier with an effect transfer ratio N_p/N_s and therefore the average

¹²The derivation of this equation is given in the appendix A.

¹³Because of the symmetry of the resonant current the even harmonics are cancelled.

rectifier current I_{rec} is given by,

$$\begin{aligned} I_{\text{rec}} = \frac{V_{\text{out}}}{R_L} &= \frac{1}{\pi} \int_{\pi-\theta}^{\pi} \left[2 \hat{I}_{s(1)} \sin(\omega t) + 2 \hat{I}_{s(3)} \sin(3\omega t) \right] d\omega t \\ &= \frac{2}{\pi} \hat{I}_{s(1)} (1 - \cos(\theta)) + \frac{2}{3\pi} \hat{I}_{s(3)} (1 - \cos(3\theta)). \end{aligned} \quad (2.18)$$

(Note, that the factor 2 for the peak values of the respective harmonics is required during that interval due to the specified transfer ratio $N_p/2N_s$.) Equation (2.18) can be solved analytically for the current conduction angle θ ¹⁴.

In the next step the equivalent resonant circuit output impedance $Z_{\text{CpR}(\nu)}$, cf. **Fig. 2.10**, for the respective harmonic ($\nu = 1, 3$) is calculated by determining the parallel-capacitor voltage harmonics with

$$v_{\text{Cp}(\nu)} = \frac{1}{\pi} \int_0^{\pi} v_{\text{Cp}}(\omega t) e^{-j\nu\omega t} d\omega t, \quad (2.19)$$

and the corresponding AC-correlation,

$$Z_{\text{CpR}(\nu)} = \frac{v_{\text{Cp}(\nu)}}{i_{\text{s}(\nu)}}. \quad (2.20)$$

In the next step, the input impedance Z_{in} of the resonant circuit is determined based on the model which includes the series-resonance circuit and the transformer. In order to establish an interface between the magnetic structure and the electric circuit a reluctance model of the integrated transformer assembly is applied as presented in **Fig. 2.10**. The general derivation of the reluctance model from the fundamental laws of electromagnetism, proposed by Faraday, Ampère and Gauss, is summarised in the appendix (section B) based on [156]. Following the assumption that the magnetic field is constant in a given segment and in parallel to the path of integration, the line and surface integrals do not have to be explicitly solved and the equations are simplified so that they can be applied to an equivalent reluctance circuit which can be investigated in analogy to an electric circuit by the familiar laws of Ohm and Kirchhoff. This assumption is widely fulfilled for highly-permeable materials such as ferrite and amorphous alloys, neglecting

¹⁴The expression for θ is much longer compared to the fundamental-frequency analysis (2.3) and therefore omitted.

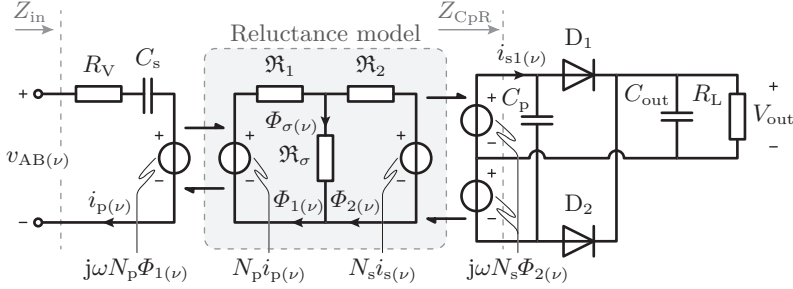


Figure 2.10: Equivalent circuit including a reluctance model for the series-parallel-resonant converter with integrated transformer and capacitive output filter. (R_V is the internal resistance of the voltage source $v_{AB(\nu)}$).

flux-crowding effects. By applying the reluctance model, even high-complex structures, resulting for instance from the integration of magnetic components on a single core or by adding further flux paths, e.g. leakage paths, can conveniently be analysed with a reasonable accuracy level, as shown, for example in [142].

The envisaged design of the integrated transformer can be modelled with sufficient accuracy by the reluctance circuit presented **Fig. 2.10** [142]. The leakage flux $\Phi_\sigma = \Phi_1 - \Phi_2$ determines the series inductance which can be adjusted by varying the air gap and the corresponding reluctance of the leakage flux path \mathfrak{R}_σ . Applying Kirchhoff's voltage law, the magnetomotive forces of the primary and one secondary winding is given by

$$\begin{aligned} N_p i_p(\nu) &= \mathfrak{R}_1 \Phi_1(\nu) + \mathfrak{R}_\sigma (\Phi_1(\nu) - \Phi_2(\nu)) \\ N_s i_s(\nu) &= -\mathfrak{R}_2 \Phi_2(\nu) + \mathfrak{R}_\sigma (\Phi_1(\nu) - \Phi_2(\nu)). \end{aligned} \quad (2.21)$$

Solving these equations and applying Faraday's law, cf. (B.11), the inductances can be determined [142] as

$$\begin{aligned} L_1 &= \frac{N_p^2 (\mathfrak{R}_2 + \mathfrak{R}_\sigma)}{\mathfrak{R}_1 \mathfrak{R}_2 + \mathfrak{R}_1 \mathfrak{R}_\sigma + \mathfrak{R}_2 \mathfrak{R}_\sigma}, \\ L_2 &= \frac{N_s^2 (\mathfrak{R}_1 + \mathfrak{R}_\sigma)}{\mathfrak{R}_1 \mathfrak{R}_2 + \mathfrak{R}_1 \mathfrak{R}_\sigma + \mathfrak{R}_2 \mathfrak{R}_\sigma}, \\ L_{\sigma(p)} &= \frac{N_p^2}{\mathfrak{R}_1 + \mathfrak{R}_\sigma} \quad L_{\sigma(s)} = \frac{N_s^2}{\mathfrak{R}_2 + \mathfrak{R}_\sigma}, \end{aligned} \quad (2.22)$$

where L_1 and L_2 are the corresponding inductances of the primary and secondary windings and $L_{\sigma(p)}$ is the leakage (series) inductance referred to the primary side; $L_{\sigma(s)}$ accordingly to the secondary side.

Considering the set of linear magnetomotive force equations (2.21) the primary winding flux $\Phi_{1(\nu)}$ and therewith the primary voltage can be calculated. Furthermore, from the resonant tank loop an expression for the harmonic sinusoidal tank input voltage can be found,

$$v_{AB(\nu)} = \frac{i_{p(\nu)}}{j\nu\omega C_s} + i_{p(\nu)}R_V + j\nu\omega N_p\Phi_{1(\nu)}, \quad (2.23)$$

where R_V is the internal resistance of the voltage source $v_{AB(\nu)}$. The requested resonant tank input impedance including the load is obtained by inserting the derived equation (2.23) in

$$Z_{in(\nu)} = \frac{v_{AB(\nu)}}{i_{p(\nu)}}. \quad (2.24)$$

Based on the resonant tank input impedance $Z_{in(\nu)}$ the system equations are given by the phase-shift to the resonant input current

$$0 = \frac{\nu\pi}{2}(1 - D) - \tan^{-1} \left(\frac{\Im(Z_{in(\nu)})}{\Re(Z_{in(\nu)})} \right) \quad (2.25)$$

with the duty cycle D and the amplitude $\hat{I}_{p(\nu)}$ of the primary harmonic currents

$$\hat{I}_{p(\nu)} = \frac{4 V_{in}}{\nu\pi |Z_{in(\nu)}|} \cos \left(\frac{\nu\pi}{2}(1 - D) \right). \quad (2.26)$$

The system equations (2.25) and (2.26) are solved numerically for the frequency and duty cycle of the operating point and therefore all required device voltages, currents, and flux distributions are determined for the following loss calculations.

Semiconductor Losses and Volumes

In respect of the power density computation, the cooling system volume is determined with the equation of the empirical CSPI value given in (2.15), i.e. the thermal resistance $R_{th,S-a}$ between heat sink mounting plate and ambient has to be calculated for a given operating point considering the specified constraints for maximum junction temperature $T_{j,max}$ as well as material constants. Depending on the heat sink assembly, e.g. geometry, material, optimisation degree of the fins, and the

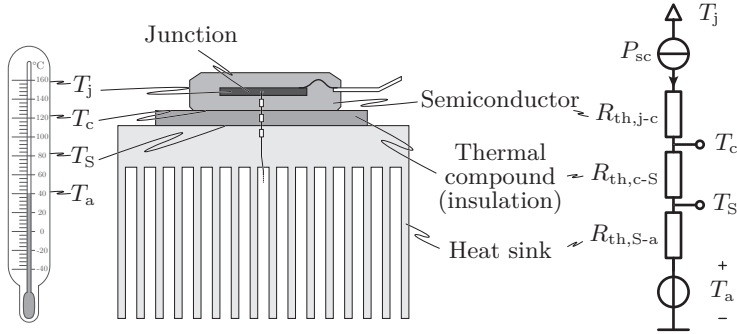


Figure 2.11: Derivation of a simple equivalent thermal model for a semiconductor mounted on a heat sink.

applied fan, the CSPI can be specified according to [154, 157, 158]¹⁵. The determination of the thermal resistance $R_{th,S-a}$ is based on a simplified thermal model as shown in **Fig. 2.11**. It is assumed that the heat flux \dot{Q} , which is generated in the junction of the semiconductor because of the non-ideal conduction and switching behaviour, is entirely transferred via the thermal resistance $R_{th,j-c}$ from the junction to the case. Border effects on the semiconductor base plate and heat emission to the ambient via the device's case are neglected or included in the empirically determined $R_{th,j-c}$, respectively, which is given in the data sheet.

The thermal resistance of the thermal grease and the used insulation foil, where applicable, is summarised in $R_{th,c-S}$ and can be obtained from the data sheet of the applied materials. The maximum allowed junction temperatures $T_{j,max}$ of the power devices are defined by the designer, referring to the values given in the data sheet and possibly considering a safety margin in order to increase the reliability.

The temperature on top of the heat sink mounting plate T_s (and therefore the necessary thermal resistance of the heat sink $R_{th,S-a}$) for the specified ambient temperature T_a is determined with the equivalent thermal circuit in **Fig. 2.11** based on the semiconductor losses P_{sc} , whose analytical models are derived in the following.

The MOSFET RMS-currents in the ZCS- and ZVS-leg of the half

¹⁵If the heat sink is for instance manufactured from copper with optimised fin's assembly and used in combination with a high-performance fan, the CSPI can be set as $23 \text{ W}/(\text{K dm}^3)$, cf. [154, 157, 158].

bridge can be determined with the fundamental and third harmonic of the resonant tank current (referred to the primary side of the transformer) calculated above,

$$I_{Tzcs} = \frac{1}{2} \sqrt{\hat{I}_{p(1)}^2 + \hat{I}_{p(3)}^2}, \quad (2.27)$$

and

$$I_{Tzvs} = \sqrt{\frac{1}{2\pi} \int_0^\phi \left(\hat{I}_{p(1)} \sin(\omega t) + \hat{I}_{p(3)} \sin(3\omega t) \right)^2 d\omega t}. \quad (2.28)$$

The anti-parallel diodes of the ZCS-MOSFETs are considered not to conduct in normal operation. In order to determine the conduction losses in the diodes of the ZVS-MOSFETs the average currents must be determined,

$$I_{Dzvs} = \sqrt{\frac{1}{2\pi} \int_\phi^\pi \left(\hat{I}_{p(1)} \sin(\omega t) + \hat{I}_{p(3)} \sin(3\omega t) \right) d\omega t}. \quad (2.29)$$

The average current in the rectifier diodes is given by

$$I_{Drec} = \frac{3 \hat{I}_{s(1)} (1 - \cos(\theta)) + \hat{I}_{s(3)} (1 - \cos(3\theta))}{3\pi}. \quad (2.30)$$

The switching losses in the H-bridge MOSFETs are low for the considered control method. The ZCS-MOSFETs are switched slightly before the zero-crossing of the resonant current in order to charge and discharge the parasitic capacitances of the high- and low-side MOSFETs during the interlock delay time t_{ild} (or interlock delay angle ι in **Fig. 2.3**, respectively) so that ZVS-conditions are obtained in this bridge leg¹⁶ as well. The phase-shift between the current crossing and turn-off and the interlock delay time are consequently chosen such that the current is sufficient for a complete discharge of the output capacitor during t_{ild} before turning-on the MOSFET. In that case, the switching losses are negligible for the ZCS-leg [149].

¹⁶In high-power applications IGBT's could advantageously be applied in the ZCS. In this case, a direct switching at the zero-crossing of the resonant current is commonly considered.

In the ZVS-leg, the turn-off current is disparately larger than for the ZCS-leg which could result in switching losses. The turn-off-current-dependent losses have been determined by measurements [149] for the MOSFET APT50M75 from Microsemi (former Advanced Power Technologies (APT)) considered in the inverter stage. Based on these investigations, an empirical equation for the switching losses in the ZVS-leg MOSFETs is given by

$$P_{\text{sw,zvs}} = 2 \cdot (1.9 I_{\text{p,off}}^2 - 38 I_{\text{p,off}} + 140) \cdot 10^{-7} \cdot f_{\text{sw}} \quad (2.31)$$

for turn-off currents higher than $I_{\text{p,off}} \geq 15 \text{ A}$ (f_{sw} is switching frequency in Hz). Otherwise the switching losses are negligible ($I_{\text{p,off}} < 15 \text{ A}$).

The conduction losses P_{cond} in the power semiconductors can be determined with the derived equations for the currents as

$$P_{\text{cond}} = R_{\text{DS,on}} (2 I_{\text{Tzcs}}^2 + 2 I_{\text{Tzvs}}^2) + 2 V_{\text{F,D}} I_{\text{Dzvs}} + 2 V_{\text{F,rec}} I_{\text{Drec}} \quad (2.32)$$

Additional losses occur in the gate drive circuits of the MOSFETs mainly depending on the characteristics of the applied MOSFETs (gate charge Q_{G} ¹⁷ and gate-source capacitance C_{GS}), the electrical control characteristics (gate-source voltage applied at the gate referring to the source for turn-on $V_{\text{GS,on}}$ and turn-off $V_{\text{GS,off}}$ of the MOSFET), and the switching frequency f_{sw} . The MOSFET's characteristic charges and capacitances can usually be extracted directly from data sheets¹⁸. The turn-on and turn-off energy not supplied back to the source can be approximated by [149]

$$E_{\text{drive}} = V_{\text{GS,on}} (Q_{\text{G}} + V_{\text{GS,off}} C_{\text{GS}}) + V_{\text{GS,off}} (Q_{\text{G}} + V_{\text{GS,off}} C_{\text{GS}}) \quad (2.33)$$

and the respective losses are determined with

$$P_{\text{drive}} = E_{\text{drive}} \cdot f_{\text{sw}}. \quad (2.34)$$

¹⁷ The gate charge characteristic $Q_{\text{G}}(V_{\text{GS}})$ (dependent on the gate-source voltage V_{GS}) given in the date sheet was applied for the loss-calculation. $Q_{\text{G}}(V_{\text{GS}})$ is typically defined for a specific drain-source voltage V_{DS} , which is the case for hard-switching. The gate charge value is slightly lower for soft-switching; that implies lower losses in the gate drives.

¹⁸ Further specified electrical parameters, such as the specified threshold voltage, the desired slew rate, and maximum current and voltage ratings, have to be considered in advance for the later prototype design.

(If the gate driver is connected to the heat sink, the gate driver losses are added to the power semiconductor losses to determine the cooling system volume.)

The maximal allowed temperature on the mounting plate of the heat sink T_S can be determined with the calculated losses in the semiconductors, cf. **Fig. 2.11**,

$$T_S = T_{j,\max} - P_{sc} (R_{th,j-c} + R_{th,c-S}) \quad (2.35)$$

where P_{sc} is the power losses of the respective semiconductor device, i.e. P_{Tzcs} , $P_{Tzvs} + P_{Dzvs}$, P_{Drec} , and P_{drive} if applicable, and $(R_{th,j-c} + R_{th,c-S})$ is the related thermal resistance between junction and base plate. If the semiconductors are mounted on the same heat sink, the minimum value of T_S determined with (2.35) for the MOSFETs and diodes eventually defines the maximum allowed heat sink temperature in this case, in order to guarantee the specified maximum junction temperature limit $T_{j,\max}$,

$$T_S \leq \min \left\{ \begin{array}{l} T_{j,\max,Tzcs} - (R_{th,j-c,Tzcs} + R_{th,c-S,Tzcs}) P_{Tzcs}, \\ T_{j,\max,Tzvs} - (R_{th,j-c,Tzvs} + R_{th,c-S,Tzvs}) P_{Tzvs}, \\ T_{j,\max,Drec} - (R_{th,j-c,Drec} + R_{th,c-S,Drec}) P_{Drec} \end{array} \right\}, \quad (2.36)$$

where P_{Tzvs} and P_{Tzcs} are the losses in a ZVS-leg and ZCS-leg MOSFET of the inverter, and P_{Drec} is the power loss in a rectifier diode. According to **Fig. 2.11** the maximum heat sink resistance $R_{th,S-a}$ (mounting plate to ambient) can be calculated with

$$R_{th,S-a} \leq \frac{T_S - T_a}{P_{semi}}. \quad (2.37)$$

The semiconductor heat sink volume can now be directly determined with (2.15) and the defined CSPI.

Resonant Tank Capacitors Losses and Volumes

The resonant tank capacitors C_s and C_p are charged from their negative to their positive voltage amplitude and back to the initial voltage during a switching cycle and are therefore exposed to a high voltage and current stress. Capacitors with a low loss factor $\tan \delta$ are consequently required for the resonant converter in order to reduce the losses and the resulting volume. Moreover, the voltage-dependency of the capacitance should

be very small in order to avoid voltage and current distortions during the charging process. These requirements reduce the available types to ceramic and polypropylene foil capacitors with the dielectric material C0G (also known as NP0)¹⁹. The capacitance per volume, however, is significantly smaller for foil capacitors and therefore multilayer ceramic capacitors have been selected for the high-power-density supply.

A commercially available component has to be chosen in the first place to include the required specifications in the optimisation process for determining the capacitor volumes and losses. The 3.9 nF/800 V C0G multilayer ceramic capacitor in a 1210 SMD housing from Novacap [160] has been chosen as a reference component because this component sets the benchmark regarding capacitance-per-volume rating at AC-voltages with a high HF amplitude at the time of realisation. Based on that capacitor, the volume per capacitor has been determined with the geometry specification of the data sheet as

$$\frac{V_C}{C} = \frac{(3.18 + 0.75)(2.54 + 0.25)(1.65 + 0.75)}{3.9 \cdot 10^{-9}} \left(\frac{\text{mm}^3}{\text{F}} \right), \quad (2.38)$$

with the assumption, that the capacitors are mounted on both sides of a 1.5-mm standard PCB with a 0.75-mm gap in the direction of the terminal and, perpendicular to that direction, a gap of 0.25 mm. The volume of the PCB is included in the calculation by adding half of the PCB-thickness to each capacitor height. By multiplying the given capacitance-per-volume ratio with the actual series- or parallel-resonant capacitance value, the volume V_C can be directly be determined with (2.38).

The dielectric losses in the capacitor are calculated considering the loss factor $\tan \delta$ as specified in the data sheet with

$$P_C = \omega C \tan \delta V_{C,\text{rms}}^2, \quad (2.39)$$

where ω is the angular frequency $\omega = 2\pi f_{\text{sw}}$ and $V_{C,\text{rms}}$ is the capacitor RMS-voltage. The maximum allowed dielectric losses can be determined by multiplying the required capacitance with the component-specific losses-per-capacitance

$$\frac{P_{C,\text{max}}}{C} = \frac{0.35}{3.9 \cdot 10^{-9}} \left(1 - \frac{T_a - 40^\circ\text{C}}{125^\circ\text{C} - 40^\circ\text{C}} \right) \left(\frac{\text{W}}{\text{F}} \right), \quad (2.40)$$

¹⁹The denotations C0G and NP0 refer to the same dielectric material, a mixture of metal oxides and titanates [159]. The denotation C0G is a standardised EIA-code defined by the Electronics Industries Association (EIA).

which is based on the loss-limit of 0.35 W per 1210-housing (maximum operation temperature of 125 °C). To verify the specified safe operation area, the calculated actual and maximum allowed dielectric losses are compared. If the actual losses P_C are higher than the maximum allowed dielectric losses $P_{C,\max}$, no feasible design can be found and therefore the present set of design parameters is discarded and the global optimisation algorithm continues with a new parameter set.

Transformer Losses and Volume

The optimal transformer volume is determined in each global optimisation loop cycle for a given set of global design parameters (L_s , C_s , C_p , N_p , N_s); the transformer geometry is calculated in an inner optimisation loop by varying the geometry parameters until the minimum volume is found. As a boundary condition, the maximum temperature in the transformer has to be kept below a specified limit, similarly to the above presented calculation of the semiconductor heat sink volume. The transformer volume calculation is, however, different in that the absolute thermal resistances of the devices are not a priori specified and the losses cannot directly be determined with a computed operating point because both are depending on the geometry. Therefore, the losses and thermal models applied in the inner optimisation process are required as function of geometry which in turn has to be predefined. The necessary models are derived in the following paragraphs.

Transformer Geometry The geometry model is explained based on the realised transformer assembly as shown in **Fig. 2.12(a)**. The transformer core and windings are actively cooled by transferring the losses via a Heat Transfer Component (HTC) to an additional transformer heat sink. This advanced cooling concept for magnetic devices is presented in [161]. The derived underlying thermal model applied in the design procedure is described below in this section.

Foil windings have been applied for a good thermal linkage to the HTC and a compact design. The heat generation is thereby potentially higher in the secondary windings (compared to the primary winding) because of the higher current RMS-values and current harmonics in the transformer secondary side. The secondary windings are therefore wound first around the centre-leg HTC because of the higher thermal conductivity and more efficient cooling. The primary winding is wound

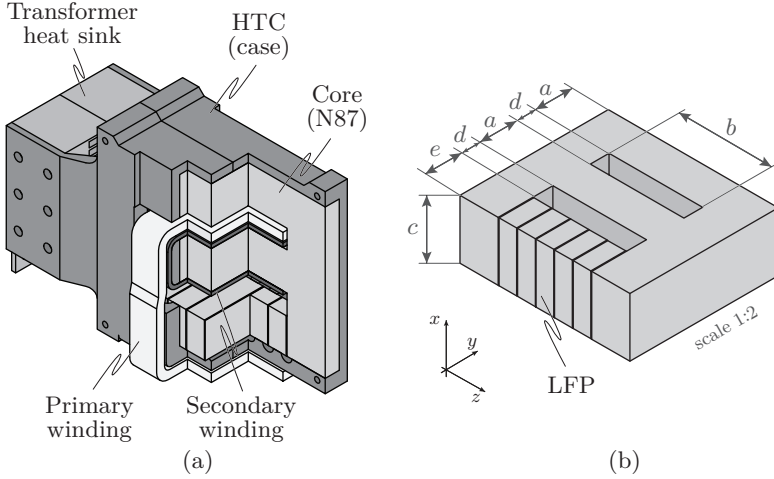


Figure 2.12: Integrated transformer geometry model. (a) Realised transformer design, (b) core geometry design parameters.

around the Leakage Flux Path (LFP) and the secondary winding on the centre leg as shown in **Fig. 2.12(a)**²⁰.

The transformer core is embedded in the heat transfer component which concurrently functions as case and retainer of the remaining converter system. The five geometry design parameters of the core (a , b , c , d , and e) are illustrated in **Fig. 2.12(b)**. The air gap l_σ in the leakage flux path (LFP leg) is distributed in six parts in order to reduce the flux emission and possible eddy current effects in the HTC and the windings. With respect to a simpler manufacturing, the leg-thickness of the outer and inner leg are equally given by the value a , determined with the outer-leg flux $\hat{\Phi}_1$ ²¹. The heights of the two winding windows are similarly chosen as d for the same reason. The core and transformer (bounding box) volume can be directly determined as function of these geometry parameters.

A further reduction of the computation time can be obtained by

²⁰Note, that the reluctance model presented in **Fig. 2.10** is still valid for this winding assembly as presented in appendix section B.

²¹This approach is possible as the flux amplitudes in the outer leg $\hat{\Phi}_1$ is higher than in the centre leg $\hat{\Phi}_2$, therefore the flux density of the centre leg will not exceed the outer-leg flux density which is supervised for possible saturation during the optimisation process.

eliminating some of the design parameters. Thus first of all the height of the leakage path e is described as function of the outer leg thickness a by assuming the same maximum flux density in both legs, i.e. with $\Phi = B \cdot A$ follows

$$e = \frac{\Phi_{\sigma}}{\Phi_1} a . \quad (2.41)$$

A further reduction of the free design parameters results from the determination of the optimal foil thicknesses of the primary and secondary windings, as explained in the next paragraph, which determines the winding window width d . The remaining three of the originally five design parameters (a , b and c) are systematically changed by the algorithm of the inner optimisation procedure in order to determine the minimum transformer volume.

Optimal Foil Thickness The analytical equations for determining the losses due to the skin and proximity effect are derived in the appendix section C and shortly summarised in the following. As illustrated in **Fig. 2.13** (taken from the appendix), the losses due to the skin effect are decreasing with the thickness of the foil whereas the proximity effect losses are increasing. As a result, an optimal layer thickness can be found where the total winding losses (the sum of the skin and proximity effect losses) are minimal, independent of the foil width b . The minimum can be found numerically as shown in appendix section C, decreasing with the increasing number of winding layers N . An analytical solution, however, cannot be determined directly from the loss equations due to the skin and proximity effect (2.49) and (2.56).

Hurley et al. demonstrated in [155] an approximation of the frequency-dependent terms in the loss equations, cf. (2.51) and (2.54), with polynomials and furthermore identified that already third-order polynomials yield in an error less than 1.2 % for the skin-effect term and less than 8.4 % for the proximity effect term if the ratio Δ between foil thickness d and skin depth δ_0 ($\Delta = d/\delta_0$) is less than 1.2. This is commonly the case as Δ is in the range of 0.3 to 1 for the optimised foil thickness and the approximation is therefore sufficiently accurate.

The derivation of the optimal thickness as presented in the appendix section C and proposed in [155] is valid for an arbitrary current waveform $i(t)$ carried by the windings which can be represented by its

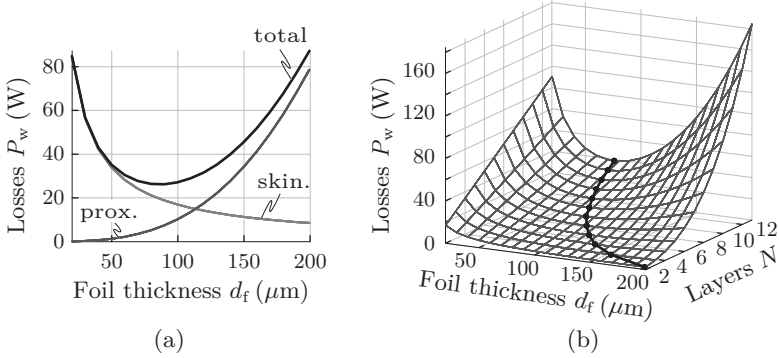


Figure 2.13: High-frequency losses in foil conductors. (a) Skin and proximity losses as function of the foil thickness d (b) Total HF-winding losses in dependency of the foil thickness and numbers of layers. *Underlying parameters:* Copper foil, $\sigma = 5.9 \cdot 10^7 \Omega^{-1} \text{m}^{-1}$, $b=50 \text{ mm}$, $\hat{I}=100 \text{ A}$, $f=100 \text{ kHz}$.

Fourier-series

$$i(t) = I_{\text{DC}} + \sum_{\nu=1}^{\infty} \hat{I}_{\nu} \cos(\nu \omega t + \phi_{\nu}) \quad (2.42)$$

where I_{DC} is the DC-component of $i(t)$ and \hat{I}_{ν} is the magnitude of the ν^{th} current harmonic. Due to the orthogonality of the sine-functions with different frequencies, the RMS-value is given by

$$I^2 = I_{\text{DC}}^2 + \sum_{\nu=1}^{\infty} I_{\nu}^2 \quad (2.43)$$

where $I_{\nu} = \hat{I}_{\nu}/\sqrt{2}$ is the RMS-value of the corresponding ν^{th} harmonic. The derivative of the RMS-value with respect to the time is furthermore determined with [155, 162]

$$I'^2 = \omega^2 \sum_{\nu=1}^{\infty} \frac{1}{2} \nu^2 \hat{I}_{\nu}^2 = \omega^2 \sum_{\nu=1}^{\infty} \nu^2 I_{\nu}^2. \quad (2.44)$$

The optimal foil thickness based on the approximation for an arbitrary current waveform can now be calculated with

$$d_{\text{opt}} = \frac{1}{\sqrt[4]{\Psi}} \sqrt{\frac{\omega I}{I'}} \delta_0. \quad (2.45)$$

where δ_0 is the skin depth for the fundamental frequency

$$\delta_0 = \frac{1}{\sqrt{\pi f \sigma \mu_0}}, \quad (2.46)$$

σ is the conductivity of the foil and Ψ is defined following Hurely [155] as

$$\Psi = \frac{5N^2 - 1}{15}, \quad (2.47)$$

where N is the number of turns for the respective winding.

For a sinusoidal current $i(t)$, where the RMS-current I and its derivative I' are given by

$$I = \frac{\hat{I}}{\sqrt{2}} \quad \text{and} \quad I' = \omega \frac{\hat{I}}{\sqrt{2}}$$

the optimal foil thickness is determined by substituting these equations into (2.45) resulting in

$$d_{\text{opt},\sin} = \frac{1}{\sqrt[4]{\Psi}} \delta_0.$$

As the current waveforms in the primary and secondary windings of the centre-tapped transformer have been determined analytically during the operating point calculation and the required RMS-value and its derivative can be derived from this analytical description, the optimal foil thickness can directly be determined with (2.45). The fundamental and third harmonic of the current have been considered in the calculation for the primary winding. The current in the centre-tapped secondary winding, however, significantly differs from the sinusoidal shape and therefore current harmonics up to the 12th have been considered for calculating the optimal foil thickness. The resulting optimal thickness for the primary and secondary windings, considering the insulation layers between the turns and four millimetres of space for mounting, are summed up in order to obtain the winding window height d , cf. **Fig. 2.12(b)**. Note, that both winding windows show the same height for sake of simpler manufacturing.

The remaining geometry parameters a , b , and c are determined in the inner optimisation process supervising the maximum allowed flux density and temperature applying the thermal model. The losses in the windings and in the core must be evaluated first for evaluating the thermal performance. The geometry-dependent winding losses including high-frequency losses are presented in the following.

Winding Losses

Winding losses emerge in a current-carrying conductor due to the electric resistance and – according to Joule’s law – heat is generated in the conductor. The winding resistance resulting for a conductor which carries DC-current and which is not exposed to an external magnetic field can be determined with

$$R_{\text{DC}} = \frac{l}{\sigma A} \quad (2.48)$$

where l is the conductor length, σ is electrical conductivity, and A is the cross-section area of the conductor.

If the conductor is carrying an alternating current, resulting in an alternating magnetic field self-induced in the conductor, or if the conductor is exposed to an external alternating magnetic field or the combination of both, which is commonly the case in transformer and inductor windings, eddy currents are induced in the conductor, which in turn increase the effective winding resistance R_{AC} .

The occurrence of losses due to eddy currents is basically described by the skin and the proximity effect:

- **Skin effect:** The alternating current in the conductor generates an alternating magnetic field outside and inside the conductor. The latter induces in turn local electric fields in this conductor. Accordingly, due to the alternating electric field, eddy currents are occurring within the conductor and, as a consequence, the current density is reduced in the middle and increased near the surface of the conductor.
- **Proximity effect:** In a conductor, exposed to an external magnetic field or to a superposition of several external magnetic fields, as for example caused by the other winding turns or air gaps, local electric fields are induced in the conductor. As a consequence, eddy currents are generated resulting in a current-density displacement within the conductor.

Both, skin and proximity effect and the corresponding inhomogeneous distribution of the current density inside the conductor can be derived from Maxwell’s equations. A closed analytical solution for Maxwell’s equations for the three-dimensional assemblies of transformer and inductors can, however, not be found. The accurate determination

applying numerical methods such as Finite Elements Methods (FEM) is furthermore not practicable during the optimisation process as the computation time for even low-complexity two-dimensional structures is much higher than the aspired ones. Under certain assumptions, a one-dimensional approach can be applied which allows the analytical determination of the current distribution and the resulting winding losses. The one-dimensional approach has been presented in Dowell's frequently cited tutorial paper [163]. Based on the one-dimensional approach, the losses due to the skin and proximity effect are derived step by step from Maxwell's equations in the appendix, section C, on page 273ff., using mainly the explanations in [149, 155, 164–166] (sorted by the date of publication).

The current density distribution has to be determined to calculate the **skin effect** losses. Thus, the diffusion equation of the magnetic field is derived from the Ampère-Maxwell's law and Gauss' law for magnetic fields neglecting the displacement currents and assuming a non-magnetic conductor with a relative permeability of $\mu_r \approx 1$, cf. (C.15). It is further assumed, that the foil conductor, which carries a current in the direction of x , is infinitely long and that the foil thickness d is much smaller than the foil width b_f ($d \ll b_f$) as illustrated in **Fig. 2.14(a)** on top. The H-field exhibits only a component in the direction of z with these assumptions, which results in a common one-dimensional second-order differential equation, cf. (C.17). The differential equation can be solved for the magnetic field intensity in the foil conductor as function of the y -position, cf. (C.21), with the magnetic field intensity on the surfaces (determined by applying Ampère's law, cf. (B.3)) as boundary conditions. The derivative of the magnetic field intensity H_z with respect to y results in the y -dependency of the current density J_x in direction of x , cf. (C.22). The ohmic winding losses per unit length due to the skin effect P'_s are determined by integrating the quadratic absolute value of the current density J_x along the conductor²²; this result in

$$P'_s = R'_{\text{DC}} F_F \hat{I}^2 \quad \text{in} \left(\frac{\text{W}}{\text{m}} \right), \quad (2.49)$$

where R'_{DC} is the frequency-independent electrical resistance per unit length,

$$R'_{\text{DC}} = \frac{1}{\sigma b_f d} \quad \text{in} \left(\frac{\Omega}{\text{m}} \right), \quad (2.50)$$

²²The horizontal symmetry axis is located in the middle of the conductor.

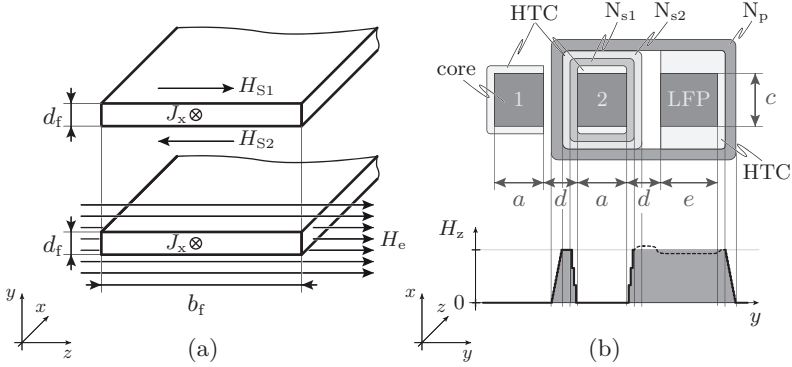


Figure 2.14: Foil conductor geometry parameters utilised to derive skin and proximity effect losses (a). Cut through the winding arrangement of the integrated transformer (b).

and the term F_F , which describes the increase of the DC-resistance with the frequency due to the skin effect,

$$F_F = \frac{\Delta}{4} \frac{\sinh(\Delta) + \sin(\Delta)}{\cosh(\Delta) - \cos(\Delta)}. \quad (2.51)$$

The DC-resistance per unit length is dependent on the foil-width b_f which is, contrary to the assumption, for practical reasons such as winding assembling and insulation slightly smaller as the winding window width b . The occurring error, however, can be corrected by adjusting the electrical conductivity σ with the porosity factor η_1 , cf. (C.39), as explained in the appendix on page 282f. The foil thickness d is replaced by the optimal foil thickness d_{opt} for the respective winding as presented in the previous subsection.

The variable Δ in the frequency-dependent term F_F represents the ratio between the foil thickness d and the skin depth δ_0 as defined in (2.46), i.e.

$$\Delta = \frac{d}{\delta_0} = d \sqrt{\pi f \sigma \mu_0}. \quad (2.52)$$

As shown in **Fig. 2.13(a)** the losses due to the skin effect are decreasing with increasing foil thickness d .

The losses due to the **proximity effect** are caused by the induced eddy currents in a conductor due to an external alternating electrical

field \hat{H}_e as illustrated in **Fig. 2.14**. The external electrical field exhibits only a component in the direction of z (H_{ez}) and it is further assumed that the magnetic field is homogeneous outside the conductor. The determination of the proximity losses is similar to the skin effect. The magnetic field intensity H_z inside the conductor can be determined according to (C.28) (page 279) and with its derivation with respect to the position y in the conductor, the current density J_x can be calculated in dependency of y , cf. (C.29). The integration of the squared current density along the conductor in the direction of y , cf. (C.30), results in an expression for the ohmic losses P'_p per unit length in a single layer due to the proximity effect,

$$P'_p = R'_{DC} G_F \hat{H}_{ez}^2 \quad \text{in} \quad \left(\frac{W}{m} \right), \quad (2.53)$$

where R'_{DC} is the DC-resistance per unit length as defined in (2.50) and G_F is a frequency dependent term,

$$G_F = b_f^2 \Delta \frac{\sinh(\Delta) - \sin(\Delta)}{\cosh(\Delta) + \cos(\Delta)}. \quad (2.54)$$

The losses due to the skin effect can directly be determined by multiplying (2.49) with the average winding length as the self-induced eddy currents are independent from the winding arrangement. Referring to (2.53), the field distribution resulting from the winding arrangement has to be considered in the calculations of the proximity effect losses. The winding arrangement is illustrated in **Fig. 2.14(b)** by a cut through the profile of the transformer core. As the expected conduction losses are higher due to the higher currents, the secondary winding is proposed to be wound around the centre leg and therefore the winding length is reduced and better coupled to the HTC (Heat Transfer Component) of the cooling system. The primary winding is wound around both, centre leg and leakage flux path. The determination of the resulting magnetic field distribution is again based on the one-dimensional approach as presented in [163] neglecting fringing and crossover effects which could only be determined numerically. The H-field therefore only exhibits a component in the direction of z in parallel to the winding. It is further assumed that the foil entirely utilises the winding width²³ and the

²³The occurring error can be corrected by the porosity factor, similarly to the skin effect, cf. page 282.

relative permeability μ_r of the core is much higher than that of the insulation material between the winding layers. The magnetic field can be determined by applying Ampère's law for each layer of the winding, cf. (C.34). In **Fig. 2.14(b)** the magnitude of the magnetic field intensity H_z is sketched below the corresponding transformer profile. The H-field is established layer by layer in the most left primary winding and reduced in the secondary winding to zero before the centre leg core segment. On the right-hand side of the centre leg cf. **Fig. 2.14(b)**, the H-field is established in the secondary winding to its maximum value. The exact field distribution in the winding window and in the leakage path cannot be determined readily with the analytical one-dimensional approach, however, the computation is not necessary for this approximation. It is further assumed, that field emission around the air gaps is small (distributed air gaps) and the influence on the winding is therefore neglected. (In the most-right winding, cf. **Fig. 2.14(b)**, the field distribution is mirrored to the distribution of the right-hand side centre-leg winding).

As mentioned above, the magnetic field intensity is assumed to be equal on both sides of the foil winding. Therefore, the average field between the two surfaces of the conductor which are in parallel to the magnetic field is determined for the corresponding layer m ,

$$H_{zm,\text{avg}} = \frac{2m-1}{2} \frac{\hat{I}}{b_f} \quad m \in \langle 1, N \rangle. \quad (2.55)$$

The total losses per unit length in a winding due to the proximity effect P'_p are represented by the sum of the losses in the single winding layers (cf. (2.53)),

$$\begin{aligned} P'_p &= R'_{\text{DC}} G_F \sum_{m=1}^N H_{zm,\text{avg}}^2 \\ &= R'_{\text{DC}} G_F \sum_{m=1}^N \frac{(2m-1)^2}{4b_f^2} \hat{I}^2 \\ &= R'_{\text{DC}} G_F N \frac{4N^2-1}{12b_f^2} \hat{I}^2. \end{aligned} \quad (2.56)$$

Up to this point, a sinusoidal current has been considered for the determination of the winding losses. As the current waveform, especially in secondary winding, considerably differs from a sinusoidal shape, the winding current is represented by its Fourier-series and, due to the

orthogonality of the skin and proximity losses, cf. section C.4, the resulting winding losses per unit length P'_w (skin and proximity effect) can be obtained from the sum of the losses up to the ν^{th} current harmonic,

$$P'_w = R'_{\text{DC}} \sum_{\nu=1}^{\infty} \left[\left(F_{F\nu} + G_{F\nu} \frac{4N^2 - 1}{12 b_f^2} \right) N \hat{I}_\nu^2 \right] \quad \text{in } \left(\frac{\text{W}}{\text{m}} \right), \quad (2.57)$$

with the frequency-dependent weighting factors for the DC-resistance

$$\begin{aligned} F_{F\nu} &= \frac{\sinh(\Delta_\nu) + \sin(\Delta_\nu)}{\cosh(\Delta_\nu) - \cos(\Delta_\nu)} \frac{\Delta_\nu}{4}, \\ G_{F\nu} &= \frac{\sinh(\Delta_\nu) - \sin(\Delta_\nu)}{\cosh(\Delta_\nu) + \cos(\Delta_\nu)} \Delta_\nu b_f^2, \end{aligned} \quad (2.58)$$

and the ratio between the (optimised) foil thickness d and the skin depth δ_ν for the corresponding ν^{th} harmonic frequency

$$\Delta_\nu = \frac{d}{\delta_\nu} = d \sqrt{\pi \nu f \sigma \mu_0} = \sqrt{\nu} \Delta. \quad (2.59)$$

The winding losses per unit length P'_w must now be multiplied by the average winding length l_{avg} of the corresponding winding in order to calculate the total losses. The winding length l_{avg} can be simply determined by the geometry of the winding arrangement, cf. **Fig. 2.14**, as function on the free core parameters a and e . The further considered thicknesses of the HTC and isolation foil between the windings are pre-defined parameters. The winding losses P_w are determined with

$$P_w = R_{\text{DC}} \sum_{\nu=1}^{\infty} \left[\left(F_{F\nu} + G_{F\nu} \frac{4N^2 - 1}{12 b_f^2} \right) \hat{I}_\nu^2 \right] \quad \text{in } (\text{W}), \quad (2.60)$$

with the absolute DC-winding-resistance R_{DC} ,

$$R_{\text{DC}} = \frac{N l_{\text{avg}}}{\sigma b_f d}, \quad (2.61)$$

by inserting the respective turns number of the primary or secondary winding ($N = N_p$ or N_s), the optimal foil thicknesses ($d = d_{\text{opt,p}}$ or $d_{\text{opt,s}}$), and the average winding length ($l_{\text{avg}} = l_{\text{avg,p}}$ or $l_{\text{avg,s}}$).

The influence of the switching-cycle-dependent energising of the centre-tapped windings is small but explained for the sake of completeness in the following. During the conduction phases, cf. **Fig. 2.4(b)–(d)** on page 68, only one of the two secondary windings is conducting

the transformed resonant current. This implies for the proposed transformer winding arrangement, cf. **Fig. 2.12(a)** or **Fig. 2.14**, that in one half switching cycle, the core-facing (inner) secondary winding is carrying the transformed resonant current and in the second half of the switching period the primary-winding facing (outer) secondary winding is conducting current. If the inner winding is conducting, the generated alternating magnetic field induces eddy currents in the outer winding as well. The resulting losses due to the proximity effect in the non-conducting winding are rather small; however, these losses are considered in the calculation during the optimisation process.

Core Losses

In addition to the losses in the transformer and inductor windings, the losses in the magnetic materials have a considerably influence on the total loss distribution of the converter system. There are basically three loss mechanisms involving the core losses:

- ▶ (static) hysteresis losses
- ▶ eddy current losses
- ▶ residual or relaxation losses.

Hysteresis losses are caused by the partly lossy magnetisation mechanism in magnetic materials which results in the typical hysteresis-shaped magnetisation curve (the magnetic induction B as function of the applied external magnetic field H). In [167], Goodenough explained the reversible processes and the corresponding energy stored in the lattice in analogy of the potential energy stored in a mechanical spring which is compressed by an external force. The irreversible processes result in heat dissipation in the lattice [167]. The physical process which results in the dissipated energy occurs for each traversal of the hysteresis loop. Consequently, the hysteresis losses increase proportional to the frequency.

Eddy current losses in the core occur, similar to the winding losses, due to the electric currents induced by the alternating magnetic field and the thereby resulting eddy currents. The losses are mainly depending on the conductivity and the assembly of the magnetic core and furthermore quadratically dependent on the frequency of the applied magnetic field. Therefore, eddy current losses appear most notably in

the iron-based cores. In order to apply iron-based cores anyhow in higher frequency applications, the cores are commonly manufactured laminated bundle of iron foils, insulated against each other, which reduces the area for the inducing magnetic field. Furthermore, the electric resistance of the material can be reduced by special metal-based alloys. Due to the small conductivity σ , eddy current losses are significantly reduced in ferrite which are consequently applicable up to microwave frequencies.

Residual or relaxation losses are caused by relaxation processes in the magnetic materials: if the thermal equilibrium of the core is abruptly changed by some external forces, the re-establishment of the new thermal equilibrium of this magnetic system and the corresponding energy change are governed by the relaxation process [167]. Goodenough stated in [167] that the precise interaction mechanism responsible for the magnetic relaxation process is not completely understood, however, an adequate derivation is given there.

Details about the theory of the loss mechanism, the calculation and measurements can be found in the corresponding literature e.g. in [167–169].

The possibly most practicable approach for calculating the core losses per unit volume is given by the empirical equation,

$$P_V = k f^\alpha \hat{B}^\beta, \quad (2.62)$$

which is commonly known as the Steinmetz equation, named after C. P. Steinmetz who described more than hundred years ago the losses due to the AC-magnetisation [170–172] (republished in [173]). The variables k , α and β are correspondingly the Steinmetz parameters. These material-specific parameters can be extracted from the manufacturer's data sheet which usually provides the loss-curves per volume or per weight as a function of frequency f , flux density \hat{B} , and temperature²⁴.

The Steinmetz equation provides adequate results if the flux-waveform is approximately sinusoidal²⁵. Based on this assumption, the

²⁴The Steinmetz parameters can be extracted by curve-fitting of the given loss curve(s) in the data sheet with the polynomial (2.62) as basis for the curve-fit.

²⁵For non-sinusoidal fluxes, the Steinmetz equation can be extend as presented for the PWM converter in section 2.2.2 and section 3.3.

losses P_c in the core can be determined with

$$\begin{aligned}
 P_c &= k f^\alpha \left[\left(\frac{\phi_1}{A_{1,2}} \right)^\beta V_1 + \left(\frac{\phi_2}{A_{1,2}} \right)^\beta V_2 + \left(\frac{\phi_\sigma}{A_\sigma} \right)^\beta V_\sigma \right] \\
 &= k f^\alpha \left[\left(\frac{\phi_1}{A_{1,2}} \right)^\beta (V_1 + V_\sigma) + \left(\frac{\phi_2}{A_{1,2}} \right)^\beta V_2 \right], \tag{2.63}
 \end{aligned}$$

where V_1 , V_2 and V_σ are the volumes of the outer leg, the centre leg, and the leakage flux path, $A_{1,2}$ is cross sectional area of the outer and centre leg and A_σ is the cross sectional area of the leakage flux path. As the variable e is determined such that the flux densities in the leakage flux path and outer leg are equal, the corresponding terms in (2.63) can be combined. The volume of the core segments can directly be parametrised with the core geometry depicted in **Fig. 2.12(b)**.

The losses in the transformer – winding losses, cf. (2.60), and core losses, cf. (2.63) – are given as function of the three remaining transformer design parameters. In the next step, a thermal model has to be derived as function of the geometry and the losses in order to assure the compliance of the specified maximum allowed hot-spot temperatures.

Thermal Transformer Model

The thermal model describes the dissipation of the transformer losses in dependency of the geometry parameters and the thermal specifications of the applied materials. There are basically three loss mechanisms which characterise the heat transfer from the heat (loss) source to the ambient:

- heat conduction
- heat convection
- heat radiation.

The heat transfer mechanisms are described by the laws of Fourier (or Biot), Newton, and Stefan-Boltzmann which are summarised in the appendix, section D.1, considering a homogeneous heat flux distribution.

All three heat transmission mechanisms – conduction, convection, radiation – can be observed in the magnetic component and the applied cooling system. In compact systems, the surface area which is available for heat radiation and free convection is reduced. On the contrary, the

losses in the magnetic components are potentially increasing with decreasing volume, what is shown in chapter 3. The ratio of losses per surface area is consequently increasing with increasing power density which finally limits the volume reduction as the generated heat cannot be dissipated via the surface any more. In order to assure the specified temperature limits of the windings (and the corresponding ohmic losses), the insulation, and the core, the magnetic components are commonly cooled with forced convection, e.g. the forced air-cooled applying fans. The convection coefficient α , cf. (D.3) in section D.1, can thereby be increased from $5\text{--}15\text{ Wm}^{-2}\text{K}^{-1}$ (free convection) to $30\text{--}60\text{ Wm}^{-2}\text{K}^{-1}$ for forced convection [161] which defines the new volume limitation for the applied cooling method.

The cooling surface can generally be increased by applying a heat sink, a common approach for cooling semiconductor devices, which results in a higher convection coefficient.

The application of a thermal coupling between the magnetic device and the heat sink via a Heat Transfer Components (HTC) is presented in [161, 174]. The heat transfer coefficient can thereby be increased significantly up to $300\text{--}600\text{ Wm}^{-2}\text{K}^{-1}$ which consequently enables a further power-density-increase of the magnetic devices. Materials with a high thermal conductivity are required for the HTC. In [161] three suitable materials have been investigated: copper ($\lambda \approx 380\text{ Wm}^{-1}\text{K}^{-1}$), an aluminium matrix with industrial diamonds ($\lambda \approx 650\text{ Wm}^{-1}\text{K}^{-1}$), and a heat pipe ($\lambda > 10'000\text{ Wm}^{-1}\text{K}^{-1}$). Because of the lower costs and the better machinability copper has been finally selected which enables a sufficient thermal characteristics as shown in [161].

Analytical equations of the temperature distribution are applied as function of the geometry for the inner optimisation process of the transformer. The evaluation of the three-dimensional heat propagation is complex and the solution of the non-linear differential equations can usually only be determined with numerical techniques (Computational Fluid Dynamics (CFD), using for example FEM) which is not appropriate in the optimisation process due to the computational effort. Therefore, only one-dimensional analytical equations are applied which are based on a transmission line model, as for example explained in [175] and briefly summarised in the appendix, section D.2. Because of the analogy of thermal and electrical circuits (as already used in section 2.1.2) the transmission line model can be used for describing the temperature distribution (corresponds to the voltage) and heat flux rate

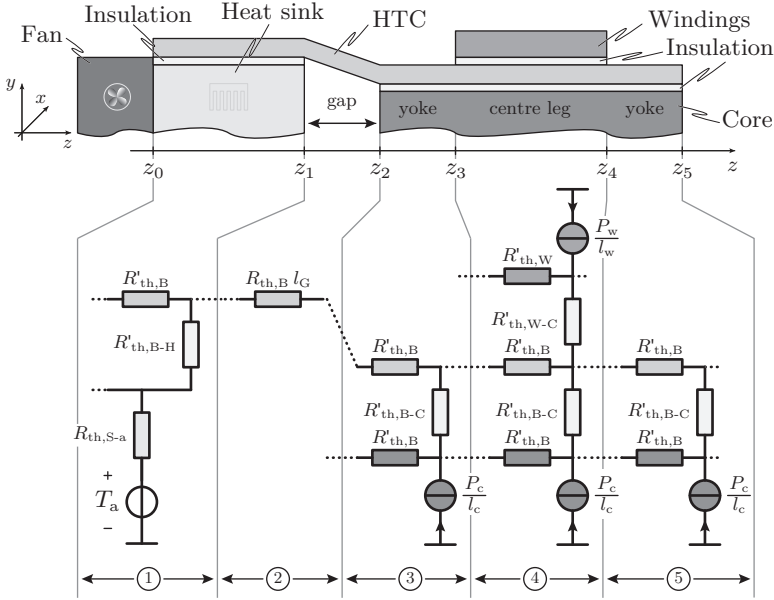


Figure 2.15: Advanced cooling of the integrated transformer: thermal connection of the heat sources (winding and core losses) via heat transfer components (HTC) with a heat sink and underlying transmission line equivalent model.

or power (corresponds to the electric current) in the heat transfer components, and the windings and the core. There, the reactive elements of the equivalent transmission line are neglected as the loss-injection is considered to be constant.

It is further assumed that no heat is dissipated via heat convection or radiation. The resulting worst-case transmission line models for the corresponding transformer sections are presented in **Fig. 2.15**. The approach for determining the temperature distribution is exemplarily shown for the most left section of the cooling system. According to the high thermal conductivity of the heat sink it is assumed that there is no heat flux in the direction of z , i.e. the losses are directly dissipated from the surface of the heat sink into the fins. The resulting transmission line model consists of thermal resistances $R'_{th,B}$ per unit length of the HTC in the direction of z and the thermal resistance of the insulation

foil $R'_{\text{th,B-H}}$ in the direction of y . The elementary cell is equivalent to a two-wire transmission line without reactive components, cf. section D.2. The corresponding differential equation describing the heat flux rate $P_{\text{HTC}}(z)$ in the HTC is

$$\frac{\partial^2}{\partial z^2} P_{\text{HTC}}(z) = P_{\text{HTC}}(z) \frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}} \quad (2.64)$$

with the initial conditions

$$\begin{aligned} P_{\text{HTC}}(z_0) &= 0 \\ P_{\text{HTC}}(z_1) &= -(P_c + P_w) \end{aligned} \quad (2.65)$$

based on the assumption that winding and core losses (P_w and P_c) are entirely carried by the HTC. The solution of the differential equation considering the initial conditions is given by

$$P_{\text{HTC}}(z) = -(P_c + P_w) \frac{\sinh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z\right)}{\sinh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z_1\right)}. \quad (2.66)$$

The temperature distribution $T_{\text{HTC}}(z)$ in the HTC can be found by integrating the flow rate of the heat energy

$$T_{\text{HTC}}(z) = - \int_{z_0}^{z_1} P_{\text{HTC}}(\tilde{z}) R'_{\text{th,B}} d\tilde{z} + T_{\text{HS}}, \quad (2.67)$$

which results in

$$\begin{aligned} T_{\text{HTC}}(z) &= (P_c + P_w) \sqrt{R'_{\text{th,B}} R'_{\text{th,B-H}}} \cdot \dots \\ &\dots \cdot \frac{1 - \cosh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z\right)}{\sinh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z_1\right)} + T_{\text{HS}}, \end{aligned} \quad (2.68)$$

where T_{HS} is the surface temperature of the heat sink which is assumed to be isothermal due to the high thermal conductivity of the heat sink material.

In the section ② of **Fig. 2.15** (section between the heat sink and core), the temperature rises linearly because of the assumed constant losses in the HTC, cf. (D.23). The temperature distribution in the heat transfer component above the core is determined with the transmission line approach. The transformer is thereby divided into three sections ③–⑤. In the left core section ③ only the core losses are responsible for the injection of heat energy into the HTC. In the middle section ④, core and winding losses are injected and in the right section ⑤ again only core losses are injected. As the boundary and initial conditions are interdependent for the three sections the differential equations have to be solved simultaneously. The derivation of the differential equation system and the corresponding initial conditions are presented in the appendix, section D.3. Due to the complexity of the solutions the equations are not shown here.

Once the temperature distribution in the heat transfer component is known, the maximum temperature in the winding can be determined. The highest winding temperature is thereby located on the most-outer winding layer as the heat dissipation via radiation or convection is neglected in this worst-case calculation. The temperature drop from the first layer, whose distribution is given by the solution of the transmission line equation, to the outer winding layer can be calculated with

$$\Delta T_w = \sum_{n_p=1}^{N_p} \frac{n_p P_{w,p}}{N_p} R_{th,INS} + \sum_{n_s=1}^{N_s} \left(\frac{n_s P_{w,s}}{N_s} + P_{w,p} \right) R_{th,INS}, \quad (2.69)$$

where $P_{w,p}$ and $P_{w,s}$ are the losses in the primary and secondary winding with the corresponding turns numbers N_p and N_s . $R_{th,INS}$ is the thermal resistance of the winding insulation. Note, that (2.69) is based on the assumption that the temperature is equally distributed in the copper and insulation layer.

It is assumed that the heat flow starts in the middle of the outer legs for modelling the temperature drop of the core, i.e. the place where the two E-cores are commonly linked to obtain the considered transformer core, and continues in both directions over the outer yokes to the middle leg, there the main HTC is located as illustrated in **Fig. D.3(a)**. The temperature drop $T_{c,i}$ is consequently maximal in the middle of the core leg i and can be calculated with

$$\Delta T_{c,i} = \frac{R_{th,C,i}}{2} P_{c,i}, \quad (2.70)$$

where $P_{c,i}$ is the generated core loss in the leg i and $R_{th,C,i}$ is the corresponding thermal resistance in that leg. As the thermal conductivity of ferrite is relatively low ($\lambda \approx 3.5\text{--}4.3\text{ Wm}^{-1}\text{K}^{-1}$ [168]) the temperature drop could be high, especially for cores with a small cross-sectional area, which results in high mechanic stress. A thin heat transfer component connected to the middle-leg HTC decreases the temperature drop. Considering a constant heat injection into the HTC, the temperature distribution can be calculated according to (2.68) which results from the transmission line equation for the section ① where the heat sink is connected with the HTC²⁶.

Note that if the heat transfer components are applied on both sides, the presented model can be simply adjusted by imaginarily cutting the cooling system into two parts along the middle of the transformer and considering only half of the injected core and winding losses.

An effective cooling system can only be obtained by applying a heat transfer component with a high thermal conductivity. These materials, however, commonly exhibit also a high electric conductivity, which makes the heat transfer component prone to eddy current effects if exposed to a magnetic field. The possibly emerging losses are not considered in the model as the magnetic field on the outer surface of the core is rather small due to the high permeability of the core. In fact, in [161] it is shown using 3-D FEM simulations, that the eddy-current losses occurring in the HTC are significantly smaller compared to the actual transformer losses²⁷. The field emission in close vicinity of air gaps can result in much higher losses in HTC due to eddy currents. In the realised prototype, the air gap is distributed in order to reduce the field emission and the HTC is locally cut away above the air gap in order to prevent a loss induction in the HTC.

The resulting maximum temperature can now be calculated for a set of geometry parameters based on the derived transmission line and loss models. The inner optimisation algorithm varies the geometry parameters systematically while keeping the flux density and hot-spot-temperatures in the specified ranges until the minimum transformer volume is found. The resulting transformer volume together with the volumes of the residual converter components enter the global optim-

²⁶More details can be found in the appendix, section D.3. Alternatively, the more accurate equations of section ③ can be derived, cf. (D.28).

²⁷The simulated losses in the HTC have been in the range of 50–150 mW for a 5-kW system with 30–40 W winding losses [161].

isation algorithm. The design parameters (L_s , C_s , C_p , N_p , and N_s) are varied until the highest power density is found. The optimisation results are discussed in the next subsection.

2.1.3 Optimisation Results

Based on the optimisation procedure presented in section 2.1.1 with the underlying models from the preceding subsection the optimal design of the series-parallel-resonant converter has been calculated based on Biela's models [144]. The results are summarised in this section.

The main material and components specifications used in the optimisation process are presented in **Tab. 2.2**. The height of the converter system is restricted to one rack unit (1 U, i.e. ≈ 44 mm), which has a strong influence on the converter design, especially on the transformer design.

The optimisation procedure furthermore considers only full-load operation because the determination of the power density has been the single optimisation objective. The results of every pass through the optimisation cycle (one set of design parameters) are stored in an external file in order to get a deeper understanding about the influence of the single components on the optimal design.

An optimum converter volume can be found for each operation frequency, which results from the set of design parameters at full load. This is illustrated in **Fig. 2.16**, where the net component volumes are plotted²⁸. There is a minimum of the system volume and maximum of the power density, respectively, at a full load switching frequency of $f_{sw} \approx 134$ kHz.

The highest share on the volume distribution has the integrated transformer whose minimum volume can be found close to $f_{sw} \approx 134$ kHz as well. If the switching frequency is increased due to the variation of the resonant tank component values, the converter volume increases mainly driven by the necessarily wider winding window width b , cf. **Fig. 2.12(b)**, because of the HF-losses in the windings, which are causing the optimal foil thickness to decrease and in turn the foil width b_f to increase in order to keep the current density and consequently the

²⁸Note, that the resulting prototype-power-density is smaller because the necessary volumes for e.g. wiring and spacing are strongly depended on the later component and module arrangement and can therefore not entirely be modelled in the calculation phase of the converter system.

Table 2.2: Constraints and specifications applied in the optimisation procedure.

Transformer	
Core	Ferrite N87 (EPCOS) $T_{c,max} \leq 115\text{ }^{\circ}\text{C}$
Winding	Copper foil, $\lambda_{Cu} = 380\text{ Wm}^{-1}\text{K}^{-1}$ $\sigma_{Cu} = 56 \cdot 10^6\text{ }\Omega^{-1}\text{m}^{-1}$ $T_{w,max} \leq 125\text{ }^{\circ}\text{C}$
Insulation	Pond-Ply [®] (Bergquist) $\lambda = 0.8\text{ Wm}^{-1}\text{K}^{-1}$, thickness $127\text{ }\mu\text{m}$
Inverter stage	
MOSFETs	APT50M75 (Microsemi, former APT) $R_{DS,on} = 150\text{ m}\Omega$ ($125\text{ }^{\circ}\text{C}$) $R_{th,j-S} = 0.32\text{ KW}^{-1}$ (incl. thermal grease) $T_{j,max} \leq 140\text{ }^{\circ}\text{C}$ (max. junction temperature)
Driver	IXDN414SI (IXYS)
Rectifier stage	
Diodes	APT100S20 (Microsemi), Schottky rectifier $V_F = 0.9\text{ V}$ (100 A , $125\text{ }^{\circ}\text{C}$) $R_{th,j-S} = 0.36\text{ KW}^{-1}$ (incl. thermal grease) $T_{j,max} \leq 140\text{ }^{\circ}\text{C}$ (max. junction temperature)
Resonant Tank	
C_s, C_p	3.9 nF , 800 V , C0G (NOVACAP)
Miscellaneous	
Electrical	$V_{in} = 400\text{ V}$, $V_{out} = 54\text{ V}$ (nominal), $P_{out} = 5\text{ kW}$
CSPI	$25\text{ WK}^{-1}\text{dm}^{-3}$ (copper-based heat sink)
Ambient	$T_a = 40\text{ }^{\circ}\text{C}$
Control	MachXO 2280C (Lattice)
Height	max. 1 U (1.75 in , $\approx 44\text{ mm}$)

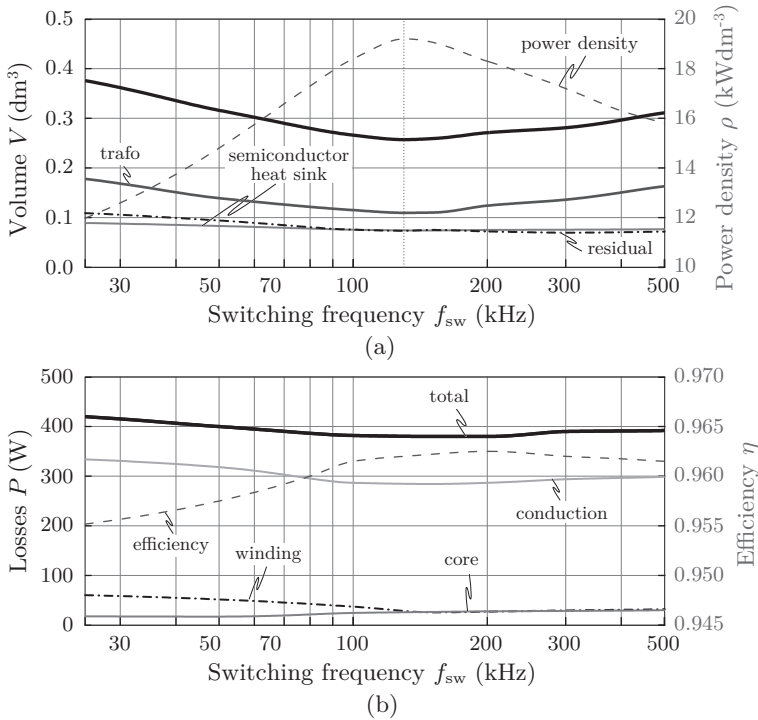


Figure 2.16: Volumes and losses of the power-density-optimised LCC-resonant converter. (Switching losses and losses in the resonant tank are comparably small and therefore not plotted).

winding losses approximately on the same level. If the switching frequency is smaller than the optimal value the cross-sectional area of the core must be increased in order to keep the flux density B constant. In case of an increased cross-sectional area of the core²⁹ the volume can consequently only be kept at the same level if the winding window width b is decreased which results in higher winding losses.

The volumes of the semiconductor heat sinks are approximately constant for the different frequencies, mainly due to the widely frequency-independent semiconductor losses (only the small gate driver and

²⁹Note, that the possible increase of the flux density is limited by B_{\max} which defines the minimum core cross-sectional area for the corresponding switching frequency.

Table 2.3: Optimisation results of the LCC-resonant converter.

Transformer		Resonant tank
Geometry	Characteristics	
$a = 14.0 \text{ mm}$	$N_p = 14$	$L_s = 26.5 \text{ } \mu\text{H}$
$b = 31.1 \text{ mm}$	$N_s = 2:2$	$C_s = 98.5 \text{ nF}$
$c = 12.2 \text{ mm}$	$T_{w,\max} = 124 \text{ }^\circ\text{C}$	$C_p = 26.0 \text{ nF}$
$d = 7.0 \text{ mm}$	$T_{c,\max} = 115 \text{ }^\circ\text{C}$	$f_{sw} = 134 \text{ kHz}$
$e = 10.6 \text{ mm}$	$B_{\max} = 300 \text{ mT}$	(full load)

switching losses are frequency dependent, cf. section 2.1.2). The tendency of an increasing semiconductor heat sink volume with lower frequency is caused by the resonant tank: as shown in section 2.1 and the appendix, section A, the resonant tank components are increasing with decreasing switching frequency. As a consequence, the reactive power and/or the resonant current increases, which is carried by the full-bridge semiconductors. This results in higher losses and therefore in a higher heat sink volume. This increase can be seen as well for the residual volume, cf. **Fig. 2.16**, where the resonant tank capacitors are included.

The design parameters which result in the converter system with minimum volume are presented in **Tab. 2.3**. The converter operates with a switching frequency of 135 kHz at full load. At this frequency, the rectifier diodes have the highest share on the losses with $P_{\text{rec}} = 83.3 \text{ W}$ ³⁰. A heat sink volume of $V_{\text{rec}} = 0.037 \text{ dm}^3$ is necessary to guarantee the specified temperature limit at $T_a = 40 \text{ }^\circ\text{C}$ ambient temperature with the resulting heat sink surface temperature of $T_{S,\text{semi}} = 130.8 \text{ }^\circ\text{C}$ and the assumed CSPI of 25. The MOSFETs on the inverter side have the second largest share on the losses with $P_{\text{inv}} = 69 \text{ W}$ ($P_{\text{sw}}=5 \text{ W}$ switching losses and $P_{\text{cond}} = 64 \text{ W}$ conduction losses), which results in a cooling volume³¹ of $V_{\text{inv}} = 0.03 \text{ dm}^3$.

The heat sink surface temperatures are determined such that the

³⁰Note, that the diode losses are assumed to be independent of the switching frequency.

³¹The heat sink surface temperatures are determined such that the maximum allowed junction temperatures are still guaranteed if the rectifier and the full bridge would be mounted on the same heat sink. The heat sink surface temperatures are consequently similar.

maximum allowed junction temperatures are still guaranteed if the rectifier and the full bridge would be mounted on the same heat sink.

The integrated transformer contributes with $P_{\text{Tr}} = 69 \text{ W}$ to the loss distribution ($P_{\text{w}} = 21.9 \text{ W}$ winding and $P_{\text{c}} = 23.5 \text{ W}$ core losses). With the described thermal model the overall transformer volume (including heat sink) occupy more than one third of the final system volume (approximately $V_{\text{Tr}} = 0.110 \text{ dm}^3$). The heat sink of the semiconductors (including the semiconductors) and the residual volumes, i.e. control PCB, fan, resonant and output capacitors, contribute both with approximately $V_{\text{res}} = 0.074 \text{ dm}^3$ to the volume distribution. The overall net component volume is $V_{\text{tot}} = 0.257 \text{ dm}^3$ which results in a theoretical power density of $\rho = 19.4 \text{ kWdm}^{-3}$. This value is, however, strongly dependent on the converter design. In the next subsection, the prototype design is presented, which finally results in a power density of $\rho = 10.4 \text{ kWdm}^{-3}$ (171 Win^{-3}).

2.1.4 Realised Ultra-Compact LCC Prototype

A prototype of a high-power-density series-parallel-resonant converter has been designed for the validation of the applied analytical models. The resonant tank components are slightly different³² compared to the above-presented design parameters ($C_{\text{s}} = 160 \text{ nF}$, $C_{\text{p}} = 120 \text{ nF}$, $L_{\text{s}} = 30 \text{ }\mu\text{H}$) so that the operating frequency is 120 kHz instead of the above-presented 135 kHz . The prototype is explained in the first part of this section. The measurement results performed with the prototype are discussed and compared with the values resulting from the analytical models at the end of the section.

Cooling System

Based on the calculated losses in the semiconductors and the transformer, the required cooling volume for the heat sinks are determined with the underlying empirical cooling system performance index (CSPI) defined by Drofenik³³ [154], cf. the thermal model as described in section 2.1.2 and in the appendix, section D. The design of the heat sink,

³²The design parameters for the prototype result from an earlier optimisation run, where a lower number of optimisation loop iterations have been performed. The overall converter losses are at the same level, only the power density could be improved theoretically by 0.2 kWdm^{-3} .

³³In [157], Drofenik also presents an analytical approach to determine the CSPI.

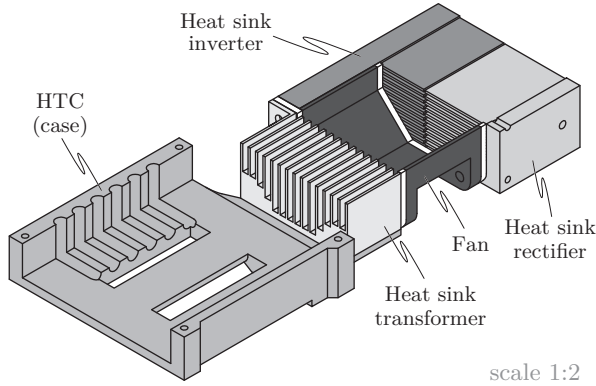


Figure 2.17: Cut through the cooling system of the LCC-resonant converter (on a scale of 1:2).

i.e. the geometry parameters such as outer lengths, number of fins, fin thickness, and space between the fins, has to be defined in the next step.

The heat sink in combination with the applied forced air cooling method is a complex system, where all three described heat transfer mechanisms (convection, conduction and radiation, cf. the appendix, section D), are interacting. Drofenik plausibly summarised in [154] the correlations between the design parameters and their influence on the heat sink performance. It is further shown that there is generally an optimum geometric design for a fan – heat sink combination which results in the minimum thermal resistance $R_{th,S-a}$ and a significantly improved cooling. The differential and accurate empirical equations describing the complex heat flow mechanism from the heat-source facing surface of the heat sink to the ambient are implemented together with a data base of fan characteristics in a small Java program³⁴, which determines the optimum geometric design based on the following pre-defined specifications.

As mentioned in the last section, a maximum height of 1 U is one of the optimisation constraints. Because of that limitation a high performance fan (SanAce 40 from Sanyo-Denki) with outer dimensions of $40 \times 40 \times 28 \text{ mm}^3$ has been selected, which therefore defines the cross-sectional area of the front of the heat sink and furthermore the static

³⁴The program is called CoolAir and has been programmed by Drofenik [154].

pressure – air flow characteristic. The length of the semiconductor heat sink is further determined by the dimensions of the semiconductors and the required spacing. The required mounting area for the full bridge multiplied by approximately half of the fan cross-sectional area would result in a higher volume compared to the volume determined in the optimisation process. The cooling fins are therefore not applied over the entire mounting area as shown in **Fig. 2.17**. The transformer heat sink dimensions are fixed by the determined heat sink volume and the fan cross-sectional area. The producibility of the heat sink arrangement is considered in the determination of the fin geometry, which commonly results in the selection of a sub-optimum with a resulting thermal resistance which is still close to the calculated one. This process becomes partly iterative if the desired thermal resistance cannot be guaranteed with the sub-optimums. The final fin-arrangement for the inverter and diodes heat sink is: 22 fins with a thickness of 0.8 mm and a space of 1.07 mm. Optimal dimensions for the transformer are 15 fins with a thickness of 0.8 mm and 2 mm spacing.

A cut through the middle of the constructed LCC-resonant converter cooling system is presented in **Fig. 2.17**. The thickness of the base plate of the full-bridge semiconductor devices has been first approximated so that the specified temperature limitations are guaranteed. The entire cooling system has been furthermore modelled and validated with the CFD (Computational Fluid Dynamics) software ICEPAK from ANSYS®. The fan is placed in between the transformer and the semiconductor heat sinks. The three heat sinks are electrically and also to some extent thermally separated. The transformer heat sink is connected with the heat transfer component (HTC) which additionally provides a case for the ferrite core. The above mentioned grooves in the transformer case at the positions of the distributed air gaps which should avoid the induction of eddy current losses in the HTC are also visible in **Fig. 2.17**.

The high performance fan takes the air from the space between the core and transformer heat sink and presses this already heated air through the two semiconductor heat sinks which is illustrated in top view of the converter system in **Fig. 2.18**. There, the rectifier side with the diodes and the capacitor PCB (output and parallel-resonant capacitor) are on the top of the figure. The output terminal carrying approximately 100 A at full load is also placed on this PCB. The diodes and capacitor/terminal PCB are connected via laser-cut copper bars

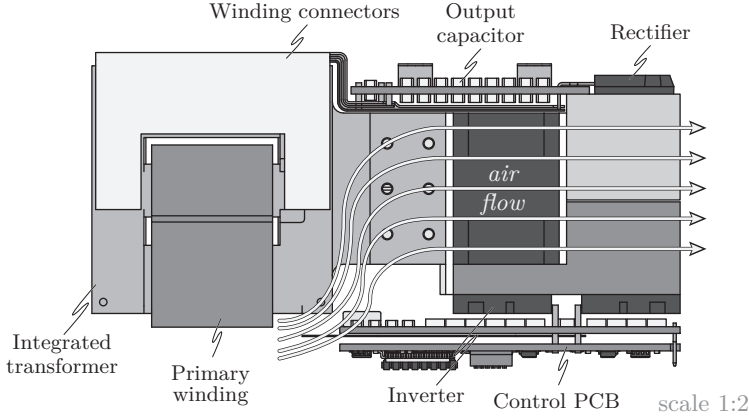


Figure 2.18: Top view of the LCC converter (on a scale of 1:2).

with the secondary windings of the transformer. The terminals of the foil windings are split and connected to the left and to the right with the cooper bars for a better current distribution.

The terminals of the primary winding are placed on the lower side of the transformer in **Fig. 2.18**. One winding end is directly connected via a copper bar with the MOSFETs of the one bridge leg and the second winding end is connected via a cable to the PCB with the series-resonant capacitors. With a small current transformer on top of the capacitor PCB (around the cable), the primary side current is detected for the system control which ensures the zero current switching conditions for the corresponding switching leg. On the lower capacitor PCB are the series-resonant capacitor and some intermediate circuit capacitors releasing a low-inductance supply for fast switching transients of the full-bridge MOSFETs. On the right side of the capacitor PCB are the input terminals.

The control PCB is the outermost PCB in **Fig. 2.18** which is equipped with the gate driver circuits, auxiliary power supplies for different voltage levels, resonant current and output voltage measurements and the CPLD (Complex Programmable Logic Device) for the digital control (MachXO 2280C from Lattice Semiconductor Corp.). The switching state machine³⁵ can easily be implemented with the CPLD,

³⁵Because of the zero-current detection and the corresponding implementation

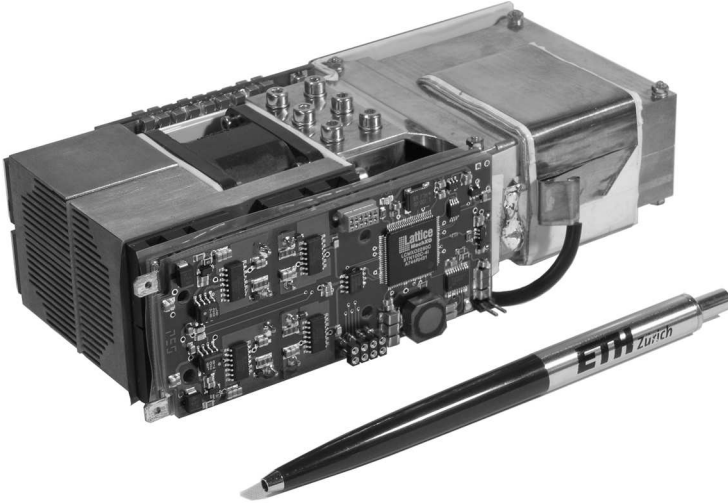


Figure 2.19: Front view photo of the realised prototype of the LLC resonant converter. Power density: $\rho = 10.4 \text{ kWdm}^{-3}$ (171 Win^{-3}).

however, the calculation of the control parameter values is rather complicated. Nevertheless, a larger CPLD or FPGA (Field Programmable Gate Array) including a small kernel for mathematical calculations or alternatively an additional DSP (Digital Signal Processor) have not been applied because of the higher space requirement.

Similarly, for sake of saving space, the high-side full-bridge MOSFETs are supplied by a low-complex bootstrap circuit topology which allows the exclusion of two galvanically isolated power supplies for the high-side gate driver. A photo of the realised prototype is shown in **Fig. 2.19** with view from the control PCB and in **Fig. 2.20** with view to the rectifier stage with the output capacitor PCB and the terminals. The very compact design with a resulting power density of 10.4 kWdm^{-3} is not least enabled by the custom-made ferrite core manufactured by EPCOS³⁶.

The measurement results performed on the presented high-power-

of several security states the switching state machine of a resonant converter is somewhat more complex than for a PWM converter.

³⁶Now a member of the TDK-EPC Corporation.

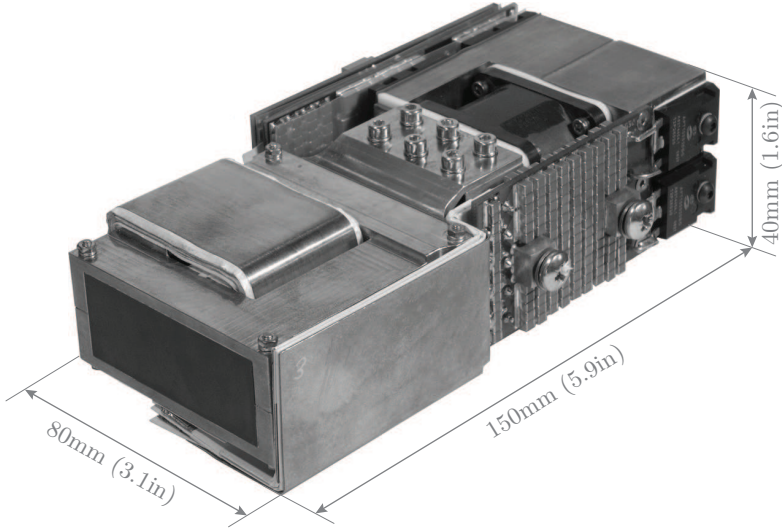


Figure 2.20: Back view photo of the realised high-power-density prototype of the LCC-resonant converter. Power density: $\rho = 10.4 \text{ kWdm}^{-3}$ (171 Win^{-3}).

density LCC-resonant converter are discussed in the next subsection.

Measurement Results

The operating point values determined with the analytical converter model have to be investigated in the first step, as the later loss and volume models are mainly depend on the accuracy of the calculated current and voltage waveforms. In **Fig. 2.21** the oscillogram of the resonant tank input voltage v_{AB} and current i_{AB} is presented for full-load operation. The converter operates with zero voltage switching so that the voltage curve is free from overshoots. Enough energy is stored in the series inductance to guarantee ZVS-conditions for the ZVS-bridge-leg. In the second bridge leg (ZCS-leg), which is supposed to switch at the zero-crossing of the resonant current, zero voltage switching can only be achieved by triggering the switching a certain time before the zero-crossing of the current as shown in **Fig. 2.21**.

The resonant current is almost sinusoidal which justifies the application of the extended fundamental frequency approach. The small

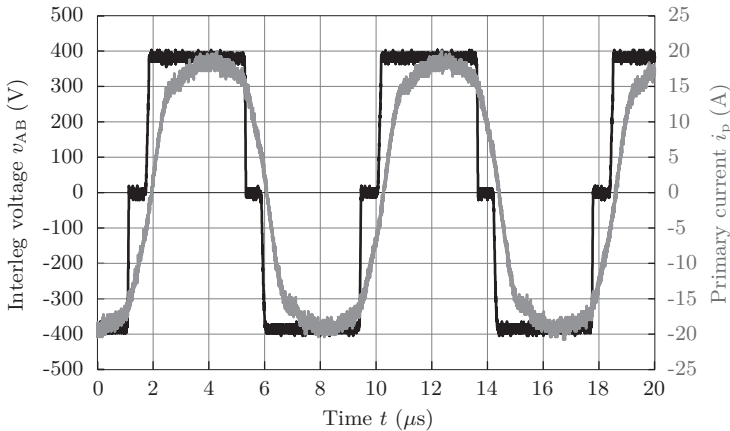


Figure 2.21: Measurement results performed on the ultra-compact LCC-resonant converter. Resonant circuit input voltage v_{AB} and current i_p . $V_{in} = 400\text{ V}$, $V_{out} = 54\text{ V}$, $P_{out} = 5\text{ kW}$.

superimposed ringing around the maximum and minimum is reflected from the secondary side which is discussed below.

The RMS-currents resulting from the calculation, simulation and measurements match very well as shown exemplary in **Tab. 2.4** for the primary side transformer current i_p (resonant tank input current). The simulation results in **Tab. 2.4** have been determined with Simplorer (ANSYS Inc.) where the reluctance model can be implemented, as well as parasitic elements of the circuit components. It can be further concluded from **Tab. 2.4** that the calculated and measured frequency which is determined by the resonant tank components are equal.

Differences in the operating point values occur for the loss-dependent values as the impact of the parasitic elements is not considered in the analytical converter model. In consequence the measured duty cycle D is approximately 16% higher than calculated. The influence on the loss models, however, is rather small as each MOSFET and diode is conducting for half of the duty cycle and the flux in the core is not considerably changing and neither is the current in the winding.

The next validation step is dedicated to the converter performance, i.e. the converter losses. From **Tab. 2.4** it can be seen, that the measured full-load efficiency is approximately 1.6% lower than calculated and 0.8% lower than simulated. There are mainly two possible loss

Table 2.4: Comparison of main operating parameters resulting from the analytical calculation, electric circuit simulation, and measurements on the prototype.

		Calculated	Simulated	Measured
Input voltage	V_{in}	400.0 V	400.0 V	400.2 V
Input current	I_{in}	13.0 A	13.1 A	12.97 A
Input power	P_{in}	5.20 kW	5.24 kW	5.19 kW
Pri. current (RMS)	I_p	15.3 A	15.1 A	15.3 A
Output voltage	V_{out}	54.0 V	54.0 V	53.4 V
Output current	I_{out}	92.6 A	92.5 A	91.8 A
Output power	P_{out}	5.00 kW	5.00 kW	4.91 kW
Efficiency	η	0.962	0.954	0.946
Duty-cycle	D	0.73	0.78	0.85
Switching frequency	f_{sw}	120.0 kHz	114.0 kHz	120.1 kHz

contributors which haven't been modelled. One type of neglected losses results from the parasitic circuit elements which form resonant circuits with other reactive parasitic and reactive circuit elements. The resulting reactive power in these circuits is additionally generating ohmic losses in the system. Some parasitic elements have already been included in the circuit simulator, such as the parallel capacitances of the semiconductors and windings, and the inductance caused by the transformer terminals. The distinctive current and voltage ringing behaviour measured on the rectifier side (discussed below) can be matched quite accurately with the simulation. However, as presented in **Tab. 2.4**, the efficiency deviation from the measurements cannot entirely be explained with these parasitic elements.

The second loss contributor, which is neglected in the modulation, is caused by the electric resistance of terminals and connection. Thermal measurements with an infrared (IR) camera during the converter operation identified possible loss sources due to the increased temperatures. The thermal image of the converter at full-load operation is presented in **Fig. 2.22**. Possible reflections on the surface of the converter components, which eventually could result in a wrong temperature display, are avoided by varnishing measurement points with a special coating

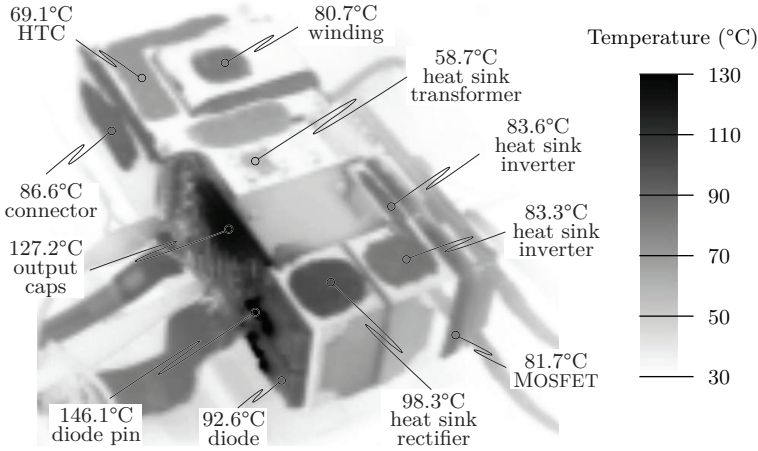


Figure 2.22: Thermal measurements on the LCC-resonant converter at full load. The ambient temperature in the laboratory has been $T_a \approx 23^\circ\text{C}$.

on the surface³⁷. Generally, it can be stated based on the measurement results in **Fig. 2.22**, that the analytical temperature model is conservative enough to keep the actually occurring temperatures below the analytically determined values with the underlying worst-case model neglecting free heat convection and radiation. Considering the laboratory ambient temperature of $\approx 23^\circ\text{C}$ instead of the specified ambient temperature of 40°C in the optimisation procedure, the temperature margin to the calculated values is between 10 and 20°C .

The thermal image in **Fig. 2.22** furthermore identifies hot spot temperatures over 140°C in the terminals of the Schottky diodes. The diodes are specified for 120 A maximum forward current, which would result in a current density of 109 to 297 A/mm^2 in the terminals according to the specified tolerance of the dimensions. In particular problematic is the anode pin whereas the cathode is thermally and electrically connected to the cooling pad on the backside of the diode case. Therefore, the diodes terminals have been further investigated. The second investigation concerns the diode itself as the diodes heat sink shows a 18 % higher temperature as the full-bridge heat sink whereas the tem-

³⁷ “Velvet coating 9560” from 3M or “NEXTEL® Velvet Coating 811-21” from Mankiewicz, respectively, both with an emissivity of approx. 1.0, have been applied.

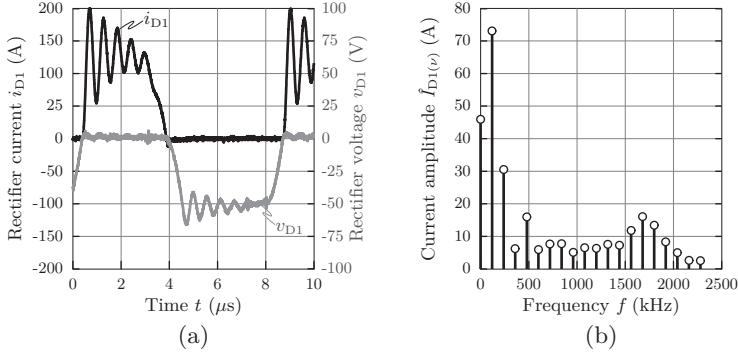


Figure 2.23: Rectifier voltage v_{D1} and current i_{D1} measurement at full load: (a) Rectifier diode current and voltage waveforms, (b) Harmonic spectrum of the diode current.

peratures should be approximately similar.

The terminal resistance between the winding output and the diode pin (close to the case) has been first measured with a four-wire measurement technique³⁸ which results in 1.89 m Ω and 1.79 m Ω for the two interconnections (winding $N_{s1} \rightarrow$ diode D_1 and winding $N_{s2} \rightarrow$ diode D_2). This measurement has been validated by applying a current of 5 A through the terminals and measuring the voltage drop and current (no noticeable temperature increase, measured resistance: 1.90 m Ω). In a second step the DC-current through the interconnection has been raised to the approximately existing diodes RMS-current of 80 A. The resistance increased to 2.93 m Ω which results in over 28 W (!) losses in both connections with the measured RMS-value of 77 A.

So far, only the DC-resistance of the interconnections have been considered. In the next step, the harmonic spectrum of the measured diode current has been determined to establish the HF-losses. As shown in **Fig. 2.23**, a high-frequency current is superimposed to the ideal current considered in the analytical converter model, cf. **Fig. 2.3** and **Fig. 2.5**. The main cause of the superimposed currents is the parasitic terminal inductance in resonance with the parallel capacitance of the resonant tank (with the current path back over the non-conducting centre-tapped winding) and the output capacitor. This results in relatively large harmonic current amplitudes in the lower mega-Hertz band,

³⁸Measurement device: high-performance Keithley 2001 series, calibrated.

e.g. 16.1 A at the 14th harmonic (additional losses of approx. 1.7 MHz) . The measured spectrum in **Fig. 2.23(b)** has been applied in a 3-D FEM simulator (ANSYS[®] MAXWELL 3D), where the interconnection including the terminal pin of the diode has been modelled. The sum of the losses of the simulated eddy-current (all harmonics with an amplitude higher than 1A have been considered) has been 16.7 W for each connection, i.e. 33.4 W total losses in the rectifier connections considering HF-effects. Compared to the DC-based measurements, approximately 5 W are occurring in the interconnections due to HF-effects.

In a second step the losses in the diodes itself have been determined. In the optimisation procedure the losses have been model based on the specified forward voltage drop (data sheet) and average current which result in losses of approx. 83 W. A similar DC-method as described above has been applied to validate these losses: a DC-current has been supplied to the output terminals so that both rectifier diodes have been conducting. The forward voltage drops have been measured (close to the case) and the losses determined. The plot of the measured DC-current with the resulting losses shows an approximately linearly relationship. The measurement results show that the calculated losses of 83 W are obtained if a DC-current of approximately 114 A is supplied by the external current source. This current value (57 A per diode) is significantly lower than the measured diode RMS-current of 77 A during the converter full-load operation. If the measured 154 A DC current is supplied by a current source, the diode losses result in approximately 113 W, i.e. approximately 30 W additional losses are occurring in the diodes. The loss value resulting from this approach was additionally validated by thermal measurements: at the supply of approximately 160 A the heat distribution approximately matches³⁹.

The sum of the two investigated loss contributors – interconnection resistances in the rectifier and additional diode losses – results in 63.4 W additional losses therefore the calculated efficiency is increased to 95.0 % which is less than 0.5 % higher than the measured efficiency. In other words, there are still 24.5 W additional losses. Parts of the losses can certainly be found in the interconnections on the primary side including the tracks on the PCB. The thermal image **Fig. 2.22** identifies the output capacitor board as additional heat source. Based on the design, the high output current is carried by the copper bars beneath the output PCB and the middle layer of the PCB only carries the ripple current.

³⁹HF-losses not included.

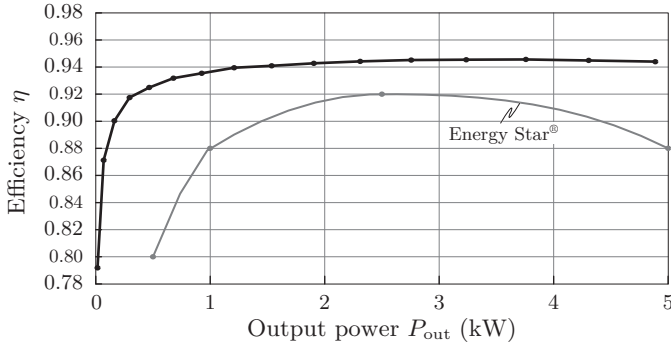


Figure 2.24: Measured load-dependent efficiency of the LLC-resonant converter.

This fact was validated during the DC-measurements presented above by supervising the thermal images: the inner layers of the PCB are only heated up by the output and diode terminals. However, the AC current in the capacitors is increased by the superimposed HF-currents due to the parasitic circuit elements. The losses in the capacitor can be determined with

$$P_C = 2\pi f C \tan(\delta) V^2, \quad (2.71)$$

whereas the dissipation factor $\tan(\delta)$ is non-linearly dependent on the temperature, the frequency, and the voltage. A superimposed voltage-ringing has been measured with a small amplitude of 0.5 mV at a frequency of 1.8 MHz. The losses would already be 37 W for assuming $\tan(\delta) = 0.05$ and considering the output capacitance of 523.6 μF . The accurate value of the dissipation factor cannot be extracted from the data sheet because of the interdependence of frequency, applied voltage and temperature.

The additional losses in the diode could be implemented as empirically determined losses in the optimisation procedure – similar to the empirically determined MOSFET switching losses. The additional losses in the interconnections are widely dependent on the converter design and are therefore almost impossible to model accurately with analytical expressions. However, the model could be improved by empirical assumptions obtained from former designs.

The measured efficiency curve shown in **Fig. 2.24** exhibits a flat

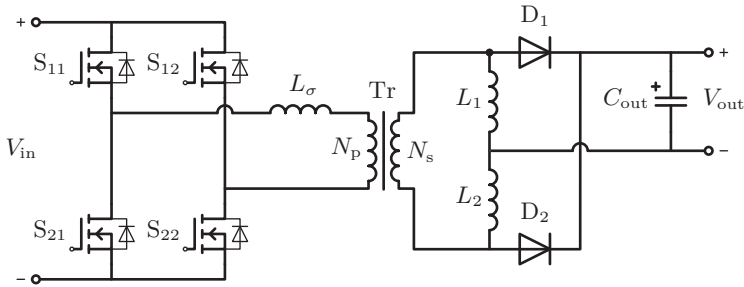


Figure 2.25: Schematic of the phase-shift PWM converter with current doubler rectifier stage (CDR).

behaviour over a wide load range. If the converter would be applied in a DC-powered data centre, the required efficiency curve proposed by Energy Star[®], cf. **Fig. 2.24** could be well exceeded with the presented prototype of the high-power-density converter system.

2.2 Phase-Shift PWM Converter with Current Doubler Rectifier (CDR)

The second investigated converter topology is the phase-shift pulse-width modulated DC-DC converter with current doubler rectifier stage as presented in **Fig. 2.25**. This topology is frequently applied for DC-DC converters with higher output currents because of the low complexity and the simple control. It is shown in this section, that the current doubler topology is suitable for a high-power-density design. The applied approach is similar to the before presented optimisation strategy for the series-parallel-resonant converter. The structure of this section is therefore according to the last section. First, the operation principle is summarised followed by a description of the optimisation procedure in section 2.2.1. Thereafter, the underlying models are explained in section 2.2.2 and the optimisation results are presented in section 2.2.3. For the presented prototype, an integrated structure of the magnetic components is chosen, i.e. the two output inductors and the transformer are integrated on a single magnetic core as presented in section 2.2.4. The realised prototype, designed and assembled to validate the optimisation results, is presented as a last point in section 2.2.5.

Steady-State Waveforms

The switching cycle of a phase-shift PWM converter can be generally divided into four states: two powering phases and two free-wheeling phases, similar to the above presented resonant topology. The resulting basic (neglecting parasitics) characteristic current and voltage waveforms are presented in **Fig. 2.26** and summarised in the following. The corresponding switching states are illustrated in **Fig. 2.27**.

$t_0 \leq t \leq t_2$ (**Fig. 2.27 (a)**) The powering phase, section ①, cf. **Fig. 2.26**, starts at t_0 , where the switch S_{11} is turned on under zero voltage conditions, as the output capacitance of this MOSFET has been discharged before during the interlock delay time t_{ild} utilising the energy stored in the leakage inductance L_σ . The positive input voltage is consequently applied to the transformer (and L_σ) which is carrying the negative current $-I_{p3}$ from the free-wheeling phase before. Mainly the leakage inductance L_σ is determining the current slope from the negative current $-I_{p3}$ to the positive current I_{p1} at t_2 . At t_1 , the current crosses the zero-line of the primary-side transformer current i_p .

During $t_0 \leq t \leq t_2$, no energy is transferred from the converter input to the output. The secondary side transformer current follows the primary side current and changes the direction. The current in both filter inductors L_1 and L_2 are continuing to decrease during this phase. The voltage over the transformer is still clamped to approximately zero as both rectifier diodes are conducting. The current in the diodes is commutating from D_2 to D_1 and D_2 is hard switched off in t_2 ⁴⁰.

$t_2 \leq t \leq t_3$ (**Fig. 2.27 (b)**) At t_2 , the power transfer from the input to the output starts as the diode D_2 is blocking and the voltage over the transformer secondary side is approximately equal to the transferred input voltage ($V_{in} N_s/N_p$). The positive primary current slope is determined by the inductor L_2 and L_σ . The inductor L_1 is connected via D_1 in parallel with the output capacitor and the current is decreasing with a slope $-V_{out}/L_1$. The sum of both inductor currents, $i_{L1} + i_{L2}$, exhibits a positive slope, charging the output capacitor as the current sum is higher than the average output current I_{out} .

⁴⁰As the circuit elements are initially considered to be ideal, no reverse current peak or voltage overshoot is shown in **Fig. 2.26**.

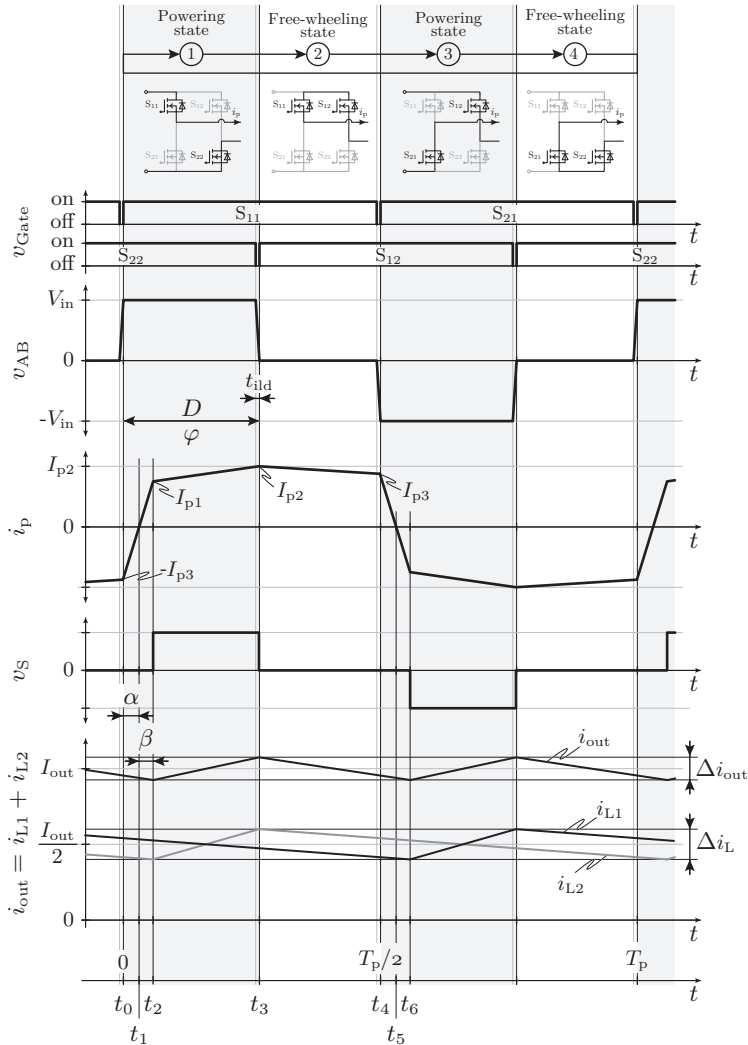


Figure 2.26: Characteristic current and voltage waveforms of the phase-shift PWM converter with current doubler output.

During the interlock-delay time t_{ild} before t_3 , the MOSFET S_{22} is turned off and the resonant charging of the output capacitance of S_{22}

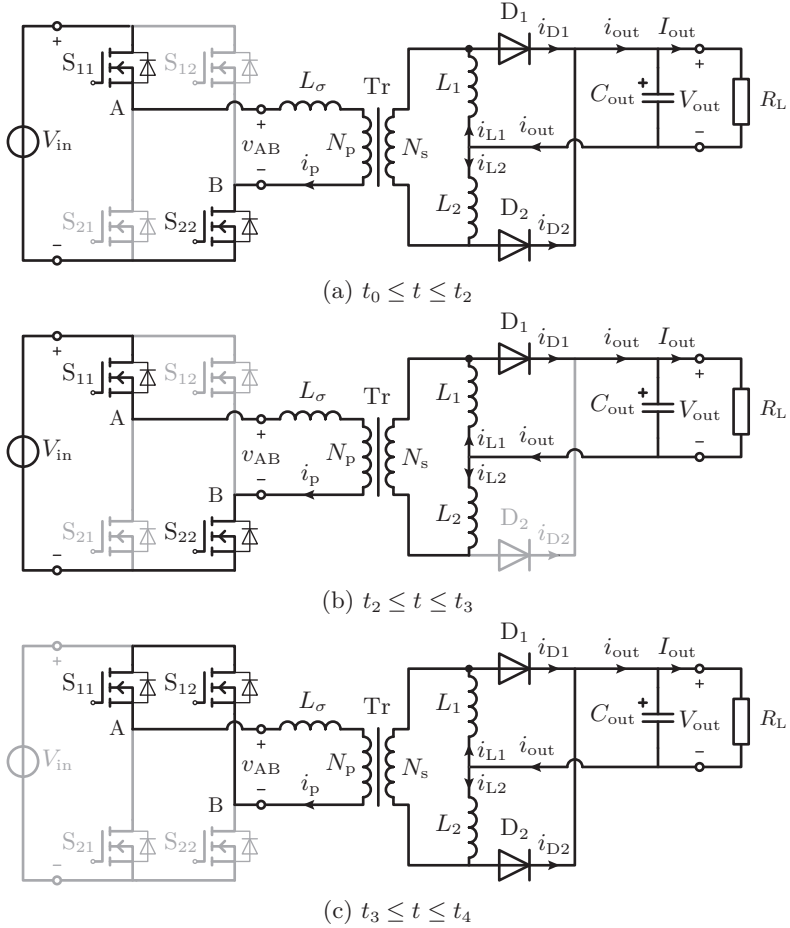


Figure 2.27: Switching states with highlighted current paths for the first switching cycles of the phase-shift PWM converter with current doubler rectifier stage.

and the resonant discharge of the output capacitance of the high-side switch S_{12} starts. When $t = t_3$, S_{12} can be turned on with ZVS-conditions.

$t_3 \leq t \leq t_4$ (**Fig. 2.27 (c)**) At t_3 , where S_{12} is turned on, the voltage of the transformer is clamped to zero and the primary side current i_p is free-wheeling in the loop formed by the high-side switches. Consequently, no energy is transferred from the input to the output of the converter system. The rectifier diode D_1 is conducting the output current, whereas D_2 stays reversed-biased because of the presence of the voltage drop across the leakage inductance, which eventually results in a hard commutation once the input voltage is re-applied to the transformer. The secondary-side referred leakage inductance L'_σ is in series with the inductance L_2 , determining the negative current slope in combination with the output voltage applied to this series connection.

The high-side MOSFET S_{11} is turned off a short time before the end of this phase ③ ($t_4 - t_{ild}$) in order to guarantee ZVS-conditions for the low-side switch S_{21} which is turned on at $t = t_4$.

At t_4 the second half of the switching cycle starts and the mirrored current and voltage waveforms can be described analogous to the first half-cycle $t_0 \leq t \leq t_4$. The corresponding equations for the above briefly described switching states are presented in section 2.2.2, where the analytical converter models are derived.

2.2.1 Design Process of Power-Density-Optimised PWM CDR Converter

The determination of the free design parameters resulting in the power-density-optimised system is analogous to the approach presented above for the series-parallel-resonant converter in section 2.1.1: an automatic design procedure is implemented with underlying analytical converter models varying the design parameters until the minimum volume is found. The sequence plan of this procedure and the therein applied subunits are briefly explained in the following based on the illustration in **Fig. 2.28**. The underlying analytical models are presented in the next subsection (section 2.1.2).

The starting point of the design process is the declaration of fixed electrical, thermal, and magnetic specifications and parameters in step ①, cf. in **Fig. 2.28**, such as the input and output voltages, thermal limitations of the applied components and materials, the ambient temperature, thermal resistances, flux density limitations of the core and the corresponding Steinmetz parameters.

In step ②, the initial set of appropriate, possibly experience-based

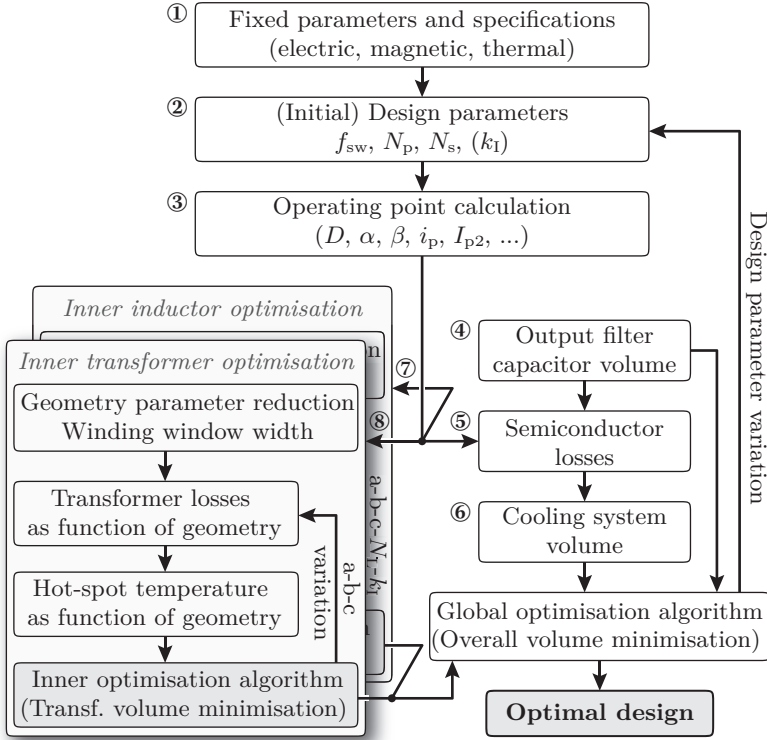


Figure 2.28: Automatic design procedure for optimising the phase-shift PWM converter concerning power density.

design parameters can be defined in order to reduce the computation time of the optimisation algorithm. The switching frequency can be directly defined for the PWM control contrary to the resonant converter. The number of design parameters of the outer loop can therefore be reduced to three: besides the switching frequency f_{sw} , the number of primary and secondary turns (N_p and N_s) has to be selected. The geometry design parameters of the transformer and inductors cores are determined in inner optimisation loops similar to the LCC-resonant-converter optimisation. As further design parameter the inductance value, or the corresponding current ripple values, respectively, could be defined in the outer loop. This parameter mainly defines the volume

of the inductors and to some extent the transformer and MOSFET heat sink volumes because the RMS-current values depend on the inductance. If this dependency is neglected, the optimal inductance value or current ripple can be determined in the inner optimisation process of the inductor and the total computation time can therefore be reduced.

In the third section, step ③, the operating point is determined, i.e. all required steady-state current and voltage waveforms and the corresponding characteristic values are calculated. Mainly the duty cycle D (or the equivalent phase-shift angle φ), the duty-cycle loss $\alpha + \beta$ ⁴¹, the MOSFETs turn-off currents I_{p2} and I_{p3} as well as devices RMS-values are determined. If the inductance value or the inductor current ripple is not defined as outer-loop design parameter, the determined equations are still dependent on one of these values and are propagated in that way to the next loop-sequences.

The next sequences – the output filter capacitor volume determination in step ④, the calculation of the semiconductor losses in ⑤, and the determination of the required heat sink volumes based on the losses and the cooling system performance index – are similar to the LCC-resonant-converter optimisation. The analytical expression for the resulting heat sink and filter capacitor volumes are given as function of the ripple current if the inductor is not defined at this point.

In step ⑥, the inductor geometry and consequently the volume of the inductors L_1 and L_2 are determined in an inner optimisation process. If the inductance value or the directly related current ripple factor k_I is not defined in the outer loop, k_I is an additional free parameter varying in the inner optimisation loop. The resulting design parameters are the characteristic core geometry values and the turn's number which are optimised for the smallest inductor volume. An advanced cooling method is applied for the inductor, similar to the transformer of the LCC-resonant converter shown above. The optimisation algorithm further guarantees the specified temperature and flux density limits. Ever since the determination of the optimal inductance values $L_{1,2}$, the characteristic operating point values and the volumes of the filter capacitor and semiconductor heat sinks can now be numerically determined.

The second inner optimisation procedure determines the volume-optimal geometry of the transformer. Similar to the transformer op-

⁴¹During the time interval $t \in \langle t_0, t_2 \rangle$ of the powering phase, no power is transferred from the input to the output of the converter as the transformer secondary side voltage is still clamped to zero by the rectifier. The effective duty cycle is therefore $D_{\text{eff}} = D - (\alpha + \beta)$.

timisation of the LCC-resonant converter and the inductor geometry optimisation, this procedure is based on an analytical description of the losses as function of the core geometry. The temperature distribution is given as function of the geometry with the further implemented thermal model of the applied forced air cooling method. The geometry design parameters are systematically varied by the inner optimisation algorithm considering to the specified temperatures and flux density limits until the minimum transformer volume is found.

The determined volumes of the transformer, inductors, filter capacitors, semiconductor heat sinks as well as further fixed volumes for the converter control are passed to the global optimisation algorithm, which varies the outer-loop design parameters systematically until the converter system with highest power density is found.

The optimisation results are presented below the summary of the underlying analytical models of this design process presented in next section.

2.2.2 Analytical Converter Models

The phase-shift PWM converter exhibits basically different waveform characteristics compared the above modelled resonant converter. The analytical description of the operating point can be approximated with a simpler model as presented in the following. Several loss-models applied for the series-parallel-resonant converter, however, can be adapted for the application in the phase-shift PWM converter optimisation procedure.

Analytical Converter Operation Model

The transformer primary side current waveform i_p is illustrated in **Fig. 2.26**. The switched currents of the full-bridge legs (I_{p2} and I_{p3}), as well as the point, where the effective power-transfer phase starts (I_{p1}) are essential for the further calculation. During the time interval $t \in \langle t_1, t_5 \rangle$ the primary current i_p is positive and can be described in four piecewise linear parts:

$t_1 \leq t \leq t_2$ The positive input voltage $v_{AB} = +V_{in}$ is applied to the transformer and the primary current i_p increases approximately linear from zero to I_{p1} , determined by the transformers leakage inductance

L_σ ,

$$i_{p,a}(t) = \frac{I_{p1}}{\beta \frac{T_p}{2}} \left(t - \alpha \frac{T_p}{2} \right), \quad (2.72)$$

where T_p is the switching period and α and β are defined, cf. **Fig. 2.26**, as

$$\alpha = t_1 - t_0 \quad \text{and} \quad \beta = t_2 - t_1.$$

During this interval, both rectifier diodes (D_1, D_2) are conducting, thus the transformer secondary side voltage v_s is clamped to zero and therefore, no power is transferred from the primary to the secondary side. At $t = t_2 = (\alpha + \beta) T_p/2$, the primary current $i_p(t_2)$ equals the transformed current doubler inductor current

$$i_p(t_2) = I_{p1} = i_{L2} N_s/N_p.$$

$t_2 \leq t \leq t_3$ Mainly delimited by the current doubler inductance L_2 and L_σ the primary current $i_p(t)$ increases from I_{p1} to I_{p2} . The linear primary current shape in the powering state ①, cf. **Fig. 2.26**, can be calculated with

$$i_{p,b}(t) = \frac{I_{p2} - I_{p1}}{(D - (\alpha + \beta)) \frac{T_p}{2}} \left(t - (\alpha + \beta) \frac{T_p}{2} \right) + I_{p1}, \quad (2.73)$$

where D is the total duty cycle.

A certain time (interlock delay time t_{ild}) before $t = t_3 = D T_p/2$, the low-side MOSFET S_{22} is turned off in order to obtain ZVS-conditions for the high-side MOSFET S_{12} . At $t = t_3$, $i_p(t)$ reaches the maximum value ($\hat{I}_p = I_{p2}$); S_{12} is turned on.

$t_3 \leq t \leq t_4$ During this interval the primary current $i_p(t)$ is free-wheeling (state ②, cf. **Fig. 2.26**) in the high-side-switch loop. The transformer voltage v_{AB} is clamped to zero (neglecting the voltage drop over the MOSFETs and the leakage inductance) and the current $i_p(t)$ decreases from I_{p2} to I_{p3} . During this interval, $i_p(t)$ is mainly determined by the transformer leakage inductance L_σ in series with the transferred current doubler inductances $L_{1,2} (N_p/N_s)^2$,

$$i_{p,c}(t) = \frac{I_{p3} - I_{p2}}{(1 - D) \frac{T_p}{2}} \left(t - D \frac{T_p}{2} \right) + I_{p2}. \quad (2.74)$$

At $t = t_4 - t_{\text{ild}}$, the high-side switch of the left bridge leg A (S_{11}) is turned off and the low-side switch S_{21} is turned on at $t = t_4 = T_p/2$ under ZVS-conditions.

$t_4 \leq t \leq t_5$ When changing from the free-wheeling state ② to the powering state ③ cf. **Fig. 2.26**, the negative input voltage is applied to the transformer ($v_{AB} = -V_{\text{in}}$) and $i_p(t)$ decreases to zero,

$$i_{p,d}(t) = -\frac{I_{p3}}{\alpha \frac{T_p}{2}} \left(t - \frac{T_p}{2} \right) + I_{p3}. \quad (2.75)$$

The current slope is determined by the transformer leakage inductance L_σ .

The next four intervals after the zero-crossing of the transformer primary side current can be described in analogy of the above presented states in $t_1 \leq t \leq t_5$ with inversed signs.

By substituting the derived piecewise linear current equations in (2.72) – (2.75) in (2.76) and solving this equation, an analytical expression for the RMS-value I_p is resulting for the loss calculations.

$$I_p^2 = \frac{2}{T_p} \left[\int_{\alpha T_p/2}^{(\alpha+\beta) T_p/2} (i_{p,a}(t))^2 dt + \int_{(\alpha+\beta) T_p/2}^D (i_{p,b}(t))^2 dt + \dots \right. \\ \left. \dots + \int_{D T_p/2}^{T_p/2} (i_{p,c}(t))^2 dt + \int_{T_p/2}^{(1+\alpha) T_p/2} (i_{p,d}(t))^2 dt \right] \quad (2.76)$$

The duty cycle D (or phase-shift φ , respectively), which defines the converter output voltage, is divided into the effective duty cycle D_{eff} ⁴² and the duty-cycle loss D_{loss} caused by the leakage inductance of the transformer (or a possibly additional series inductance which could extend the ZVS-range). The effective duty cycle depends on twice the output voltage V_{out} and the input voltage V_{in} (transferred to the secondary side of the transformer). The expression for the total duty cycle is given by

$$D = 2 \frac{V_{\text{out}}}{V_{\text{in}}} \frac{N_p}{N_s} + (\alpha + \beta). \quad (2.77)$$

⁴²The power is transferred from the input to the rectifier stage of the converter during the effective duty-cycle interval.

With the duty-cycle loss $D_{\text{loss}} = \alpha + \beta$.

The equations (2.72) – (2.77) require the knowledge of α and β in order to numerically determine the operating point. The derivation of these parameters is presented in the following.

The sum of the two current doubler inductor currents $i_{\text{out}} = i_{L1} + i_{L2}$ exhibits the DC-component I_{out} , which is defined as average output current. The minimum and maximum currents can be expressed as

$$\min, \max [i_{\text{out}}] = I_{\text{out}} \pm \frac{1}{2} \Delta i_{\text{out}} \quad (2.78)$$

with the output current ripple Δi_{out} , cf. **Fig. 2.26**. Assuming that the output filter capacitor absorbs the entire ripple current Δi_{out} , the load current is constant and it is thus determined with the average output power P_{out} and average output voltage V_{out} ,

$$I_{\text{out}} = \frac{P_{\text{out}}}{V_{\text{out}}}. \quad (2.79)$$

The admissible current ripple Δi_{out} is defined by the current ripple factor k_I , a design parameter of the optimisation process ($k_I \in \langle 0, 0.2 \rangle$), which is related to the volume of the inductors and of the output filter capacitor,

$$\Delta i_{\text{out}} = k_I I_{\text{out}}. \quad (2.80)$$

During the interval $t \in \langle t_3, t_6 \rangle$, where the transformer voltage is clamped to zero, both inductor currents i_{L1} and i_{L2} are decreasing with a identical slope, as illustrated in **Fig. 2.26**. The relationship between the output current ripple Δi_{out} and the variation of the inductor current during this interval ($\Delta i_{L,a} = \Delta i_{L1,a} = \Delta i_{L2,a}$) can be expressed as

$$\Delta i_{\text{out}} = 2 \Delta i_{L,a}. \quad (2.81)$$

The current ripple (peak-to-peak value) Δi_L in the output inductors L_1 and L_2 can be calculated with

$$\Delta i_L = \frac{V_{\text{out}}}{L_1} (2 - D + \alpha + \beta) \frac{T_p}{2}, \quad (2.82)$$

assuming the constant inductor current slope as shown in **Fig. 2.26**. The current ripple $\Delta i_{L,a}$ during the interval $t \in \langle t_3, t_6 \rangle$ can now be determined with the rule of three

$$\Delta i_{L,a} = \Delta i_L \frac{1 - D + \alpha + \beta}{2 - D + \alpha + \beta}. \quad (2.83)$$

Substituting (2.83) in (2.81) and using (2.80), the peak-to-peak value of the current in the inductor L_1 or L_2 can be determined in dependency of the current ripple factor k_1 and the average output current I_{out} ,

$$\Delta i_L = \frac{1}{2} \frac{2 - D + \alpha + \beta}{1 - D + \alpha + \beta} k_1 I_{\text{out}}. \quad (2.84)$$

The inductance value of L_1 and L_2 can similarly be determined considering the interval $t \in \langle t_3, t_6 \rangle$ and using the linearised inductor voltage formula and the output current ripple definition (2.80),

$$L_1 = L_2 = V_{\text{out}} \frac{(1 - D + \alpha + \beta) T_p}{k_1 I_{\text{out}}}. \quad (2.85)$$

The characteristic primary current value I_{p1} can be directly determined graphically from **Fig. 2.26** with the knowledge of the ripple current Δi_L , considering the primary-side referred inductor current i_{L2} at the point $t = t_2$,

$$I_{p1} = \frac{N_s}{N_p} \left(\frac{I_{\text{out}}}{2} - \frac{\Delta i_L}{2} \right), \quad (2.86)$$

as i_{L2} (referred to the inverter stage) is similar to i_p during the interval $t \in \langle t_2, t_3 \rangle$, cf. **Fig. 2.27(b)**.

The current value I_{p2} can directly be determined considering again the primary-side referred inductor current i_{L2} at the point $t = t_3$ in **Fig. 2.26**,

$$I_{p2} = \frac{N_s}{N_p} \left(\frac{I_{\text{out}}}{2} + \frac{\Delta i_L}{2} \right). \quad (2.87)$$

During the free-wheeling phase ②, the transformer voltage is clamped by the high-side switches and therefore the rectifier-stage referred leakage inductance L'_σ and the inductance L_2 are connected in series, cf. **Fig. 2.27(c)**. Accordingly, the output voltage V_{out} is applied to the series connection of the two inductors $L'_\sigma + L_2$, neglecting the forward voltage drops over the MOSFETs and D_1 ⁴³. The current i_{p3} at the point $t = t_4$ can be determined with

$$I_{p3} = I_{p2} - \frac{N_s}{N_p} \frac{V_{\text{out}}}{L_\sigma (N_s/N_p)^2 + L_2} (1 - D) \frac{T_p}{2}, \quad (2.88)$$

⁴³The rectifier diodes D_2 is still reversed-biased because of the voltage drop over the leakage inductance L_σ .

with the linearised current decrease during the interval $t \in \langle t_3, t_4 \rangle$.

There are two more equations required to enable the determination of the three characteristic primary current points, and α and β . As shown in **Fig. 2.26** is the current slope during the duty-cycle loss interval is constant and the quotient β over α can consequently be defined with

$$\frac{\beta}{\alpha} = \frac{I_{p1}}{I_{p3}}. \quad (2.89)$$

As the duty-cycle loss is mainly determined by the leakage inductance, a further expression for $\alpha + \beta$ based on the linearised voltage equation of the inductor current during the duty-cycle loss interval $t \in \langle t_0, t_1 \rangle$ can be defined as

$$\alpha + \beta = \frac{L_\sigma}{V_{in} T_p/2} (I_{p1} + I_{p3}). \quad (2.90)$$

The equation system consisting of (2.86)–(2.90) can now be solved for the five unknown values I_{p1} , I_{p2} , I_{p3} , α , and β . The solutions, which are very long equations and therefore not explicitly presented here, allow the complete description of all required current and voltage waveforms for determining the losses in the converter components.

Semiconductor Losses and Volumes

The approach for determining the semiconductor losses and volumes is similar to the one presented for the series-parallel-resonant converter in section 2.1.2 on page 85: first, the losses in semiconductor are determined based on the calculated operating point, and in the second step, the cooling system volume is approximated with the empirically determined CSPI.

Except for the small interlock delay times t_{ild} , where the resonant voltage and current transition in the full-bridge legs take place, two MOSFETs are always in the conduction path of the primary side current i_p , i.e. the current in all MOSFETs is carried by the turned-on channel and not by the anti-parallel body diode. The conduction losses in a MOSFET can therefore be determined with

$$P_{cond,T} = R_{DS,on} I_T^2, \quad (2.91)$$

where $R_{DS,on}$ is the on-resistance of the MOSFET and I_T is the RMS-current value of a MOSFET. With the assumption (and control), that

every MOSFET is turned on for half a switching cycle and conducting the primary current during the corresponding interval, the resulting RMS-current values are equal for the four full-bridge switches.

As a zero voltage switching control is implemented for the full-bridge MOSFETs the switching losses are very low – only ohmic losses might occur because of the on-resistance. Similar to the above presented resonant converter, these losses are determined with an empirical expression based on measurements with the designated MOSFET (APT50M75 from Microsemi),

$$P_{\text{sw,zvs}} = 2 \left(1.9 I_{\text{p,off}}^2 - 38 I_{\text{p,off}} + 140 \right) \cdot 10^{-7} f_{\text{sw}}, \quad (2.92)$$

in case the turn-off current $I_{\text{p,off}}$ (I_{p2} or I_{p3}) is higher than 15 A; the switching losses are negligible if the turned-off current is below 15 A.

A constant forward voltage drop V_f is assumed for the rectifier diodes, and the losses are approximated with

$$P_{\text{cond,D}} = V_f \frac{I_{\text{out}}}{2}. \quad (2.93)$$

As identified during the measurements with the resonant converter prototype, the approximation (2.93) might not be sufficiently accurate. The measurement-based knowledge from an equivalent system with the same devices applied can be included by developing empirical equations out of the measurement results. The differential on-resistance of the diode r_{on} , if provided by the OEM, can be furthermore included into the loss determination

$$P_{\text{cond,D}} = V_f \frac{I_{\text{out}}}{2} + r_{\text{on}} I_{\text{D}}^2, \quad (2.94)$$

where I_{D} is the RMS-current through the rectifier diode which can be calculated with the determined operating point waveforms. As Schottky diodes are considered, the losses due to the reverse recovery effect are neglected.

In terms of an accurate determination of the total losses, the gate driver can be included in the loss calculation using (2.33) and (2.34) on page 88. If the gate driver circuit is considered in the cooling system, the losses have to be included for the volume determination of the heat sinks.

The linear thermal model as illustrated in **Fig. 2.11** on page 86 is applied similarly to the resonant converter for the determination of the

cooling system volume. The thermal resistances can be extracted from the data sheets of the applied materials and devices. The temperature drop T_S from the heat sink surface to the ambient, which finally determines the required thermal resistance $R_{th,S-a}$ of the heat sink and consequently its volume, has to be determined such that none of the applied semiconductor devices exceeds the specified maximum junction temperature, i.e.

$$T_S \leq \min \left\{ \begin{array}{l} T_{j,max,TA} - (R_{th,j-c,TA} + R_{th,c-S,TA}) P_{TA}, \\ T_{j,max,TB} - (R_{th,j-c,TB} + R_{th,c-S,TB}) P_{TB}, \\ T_{j,max,DR} - (R_{th,j-c,DR} + R_{th,c-S,DR}) P_{DR} \end{array} \right\} \quad (2.95)$$

where $T_{j,max,TA}$ and $T_{j,max,TB}$, are the junction temperatures of the MOSFETs in the left and right bridge leg and $T_{j,max,DR}$ is the junction temperature of the rectifier diodes. The corresponding thermal resistances between junction and case as well as the thermal resistance between case and heat-sink surface (which includes the thermal grease or the applied insulation foil) are e.g. given by $R_{th,j-c,TA}$ and $R_{th,c-S,TA}$ for the left bridge leg.

The maximum heat sink thermal resistance (base plate to ambient) $R_{th,S-a}$ defined as

$$R_{th,S-a} \leq \frac{T_S - T_a}{P_{semi}}, \quad (2.96)$$

can be calculated for the specified ambient temperature T_a and the determined sum of the semiconductor losses P_{semi} . With the definition of the cooling performance index CSPI [154],

$$CSPI = \frac{1}{R_{th,S-a} \cdot V_{CS}} \left(\frac{W}{K \cdot dm^3} \right), \quad (2.97)$$

the cooling system volume V_{CS} of the semiconductor can be directly calculated.

Output Filter Capacitor

Depending on the inductance value, set by the optimisation algorithm, the output filter capacitor C_{out} might carry high frequency ripple currents with considerable amplitudes. In order to limit the losses and the temperature rise, dielectrics with a low loss factor $\tan(\delta)$ are required. X7R ceramic capacitors in a 1210 housing from Murata (2.2 μF , 100 V)

are provided for the prototype, which have a very high allowed ripple current per volume ratio.

The output voltage v_{out} across the filter capacitor C_{out} , which has been considered to have only a DC-component V_{out} so far, increases during the charging process, i.e. when the sum of the inductor currents i_{out} is larger than the DC-output current, $i_{\text{out}} > I_{\text{out}}$. According to **Fig. 2.26**, this is true for half of the effective duty cycle D_{eff} (current increase) and half of the effective free-wheeling time $(1 - D_{\text{eff}})$ (current decrease). The required capacitance value C_{out} is calculated with the currents and the maximum allowed output ripple voltage $V_{\text{Cp-p}} = 300 \text{ mV}_{\text{pp}}$,

$$C_{\text{out}} = \frac{1}{V_{\text{Cp-p}}} \left[\int_0^{1/2 D_{\text{eff}} T_{\text{p}}/2} \frac{\Delta I_{\text{out}}}{D_{\text{eff}} \frac{T_{\text{p}}}{2}} t \, dt + \dots \right. \\ \left. \dots + \int_0^{1/2 (1-D_{\text{eff}}) T_{\text{p}}/2} \frac{\Delta I_{\text{out}}}{(1 - D_{\text{eff}}) \frac{T_{\text{p}}}{2}} t \, dt \right]. \quad (2.98)$$

The device-specific volume-per-capacitance ratio has to be defined for the resulting filter capacitor volume V_{C} based on the geometric parameters provided by the data sheet and the space required for mounting, similar to the approach presented for the resonant converter, cf. (2.38) on page 90,

$$\frac{V_{\text{C}}}{C} = \frac{(3.5 + 1.0)(2.5)(2.5 + 0.75)}{0.8 \cdot 2.2 \cdot 10^{-6}} \left(\frac{\text{mm}^3}{\text{F}} \right). \quad (2.99)$$

The total filter volume is then determined by multiplying the required capacitance value resulting from (2.98) with the respective volume-per-capacitance ratio.

The dielectric losses in the filter capacitor are calculated with the loss factor $\tan(\delta)$ as specified in the data sheet with

$$P_{\text{C}} = \omega C_{\text{out}} \tan(\delta) V_{\text{Cout}}^2, \quad (2.100)$$

where ω is the angular frequency $\omega = 2\pi f_{\text{sw}}$ and V_{Cout} is the capacitor RMS-ripple voltage.

Similar to the approach applied for the resonant converter, the component-specific maximum allowed dielectric losses $P_{\text{C,max}}$ are additionally determined with the losses-per-capacitance ratio, cf. (2.40)

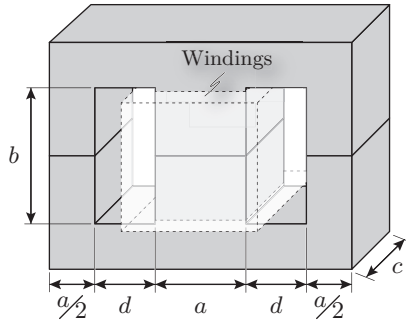


Figure 2.29: Geometry model applied for the transformer and inductors of the phase-shift PWM converter with current doubler rectifier.

on page 90, based on the loss-limit of the applied 1210-housing (max. 0.35 W per case) and the maximum operation temperature of 125 °C. In case the losses P_C are higher than the maximum permissible dielectric losses $P_{C,\max}$, no feasible design can be found and therefore the present set of design parameters is discarded and the global optimisation algorithm continues with a new parameter set.

Also the dependency of the capacitance on the temperature and output voltage can be considered in the design process for an accurate volume determination. In (2.99) the tolerance coefficient of 0.8 has been included for that reason.

Transformer and Inductor Model

Similar to the LCC-resonant converter, the shape of the transformer and inductor are optimised with respect to the minimum volume. This optimisation is based on models describing the losses (winding and core) and the temperature distribution in the magnetic device as function of the geometry. These models are summarised in the following.

The applied core geometry model is illustrated in **Fig. 2.29**. This model is valid for both, transformer and output inductor, considering an assembly with E-cores. As an alternative, C-cores could be applied, whereas the geometry model and the applied loss models are equivalent and remain unchanged. The advanced forced air-cooling as explained in the appendix, section D, and already used with the LCC-resonant converter, cf. section 2.1.2, is dedicated for the phase-shift converter

with current doubler as well⁴⁴. The windings are arranged around the middle leg – the transformer secondary winding is thereby the inner winding, and the primary winding, because of the smaller RMS current, is arranged outside.

The winding window height d , cf. **Fig. 2.29**, can be eliminated before entering the inner optimisation loop by determining the optimal foil thickness as described in the appendix, section C, and similarly applied for the LCC-resonant converter in section 2.1.2. As the windings are not carrying a sinusoidal current, the generalised equation provided by Hurley et al. in [155] is utilised,

$$d_{\text{opt}} = \frac{1}{\sqrt[4]{\Psi}} \sqrt{\frac{\omega I_w}{I'_w}} \delta_0, \quad (2.101)$$

where Ψ is defined as

$$\Psi = \frac{5 N^2 - 1}{15}$$

and δ_0 is the skin depth, I_w is RMS current in the corresponding winding, I'_w its derivative, ω is the angular frequency, and N is the number of turns⁴⁵. In addition to the sum of the transformer windings or the single inductor winding, space for the assembling is furthermore considered in the determination of the winding height d .

The determination of the winding losses for the applied elementary winding arrangement is based on the consideration (as presented in [155] and summarised in the appendix, section C.5) that the effective resistance R_{eff} of an optimised winding is given by

$$R_{\text{eff}} \Big|_{\text{opt}} = \frac{4}{3} R_{\text{DC}} \Big|_{\text{opt}}, \quad (2.102)$$

whereas the optimised DC-winding-resistance R_{DC} can be determined with

$$R_{\text{DC}} \Big|_{\text{opt}} = \frac{N l_w}{\sigma_{\text{Cu}} b d_{\text{opt}}}. \quad (2.103)$$

⁴⁴Note, that the heat transfer component (HTC) in the middle leg is not shown in **Fig. 2.29**.

⁴⁵The derivation of these equations can be found in the appendix, section C, and the corresponding publication [155].

The equation (2.102) is valid for arbitrary current waveforms [155]. The winding losses can consequently simply be determined with

$$P_{wx} = R_{DCx} \left|_{\text{opt}x} I_{\text{rms}x} = \frac{N_x l_{wx}}{\sigma_{\text{Cu}} b d_{\text{opt}x}} I_{\text{rms}x} \quad (2.104)$$

where x is the index of the related winding (x : primary, secondary, inductor winding).

Contrary to the resonant converter, the current and voltage waveforms applied to the transformer are non-sinusoidal; accordingly using the Steinmetz equation, cf. (2.62) on page 103, for determining the core losses might result in inaccuracies. The research group around Sullivan published in [176] an improved method to determine the core losses per unit volume for a non-sinusoidal flux density waveform,

$$P'_{c,V} = k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha}, \quad (2.105)$$

where ΔB is the peak-to-peak flux density and k_i can be approximated by

$$k_i = \frac{k}{2^{\beta+1} \pi^{\alpha-1} \left(0.2761 + \frac{1.7061}{\alpha+1.354} \right)}, \quad (2.106)$$

and α , β and k are the Steinmetz parameters for the applied ferrite material.

The flux density ripple for the transformer ΔB can be approximated with

$$\Delta B = \frac{V_{\text{in}} D T_p/2}{N_p A_c}, \quad (2.107)$$

and (2.105) can be further simplified to determine the losses in the transformer per unit length

$$P'_{c,\text{Tr}} = \frac{k_i \Delta B^{\alpha-\beta}}{T_p} 2 \left(\frac{V_{\text{in}}}{N_p A_c} \right)^\alpha D T_p/2, \quad (2.108)$$

where A_c is the cross-sectional area of the transformer core.

The flux variation for an inductor can be approximated with

$$\Delta B_L = \frac{L_1 \Delta i_L}{N_L A_{c,L}}, \quad (2.109)$$

and with Sullivan's approximation [176] the core losses per unit length for one inductor are given by

$$P'_{c,L} = \frac{k_i \Delta B^{\alpha-\beta}}{T_p} \left[\left(\frac{V_{out}}{N_L A_{c,L}} \right)^\alpha D^{T_p/2} + \dots \right. \\ \left. \dots + \left(\frac{V_{in}^{N_s/N_p} - V_{out}}{N_L A_{c,L}} \right)^\alpha (2-D)^{T_p/2} \right], \quad (2.110)$$

where $A_{c,L}$ is the cross-sectional area of the inductor core.

The advanced cooling method for magnetic devices as shown for the LCC-resonant converter and generally derived in appendix, section D, is considered for the transformer of the phase shift converter and for the current doubler inductors. The modelling of the cooling system is based on the transmission line equations which are solved for the corresponding equivalent electric circuit to determine the temperature distribution and hence the hot-spot temperatures in the windings and the core. The geometry and the corresponding equivalent electric circuit are illustrated in **Fig. 2.15** on page 106. The derivation of the equations describing the piecewise temperature distribution is explained in the appendix, section D.

The losses and temperature distribution are given as function of the remaining geometry parameters a , b , and c , cf. **Fig. 2.29**. These parameters are varied systematically by the inner optimisation algorithm with respect to the minimum volume considering the specified maximum temperatures in the winding and the core as well as the maximum flux density. The resulting minimised volume is passed to the global optimisation algorithm where the design parameters of the outer loop are varied until the minimum converter volume is found. The optimisation results are shown in the next subsection.

2.2.3 Optimisation Results

The main parameters and specifications considered as fixed values in the optimisation procedure are presented in **Tab. 2.5**. The majority of these parameters are similar to the applied LCC-resonant-converter specifications. The cooling system performance index (CSPI) is slightly reduced in order to apply aluminium instead of copper for the cooling system which is practically more relevant because of the better machinability and especially because of the lower costs.

Table 2.5: Constraints and specifications applied in the optimisation procedure for the phase-shift PWM converter with current doubler.

Transformer / Inductor	
Core	Ferrite N87 (EPCOS) $T_{c,max} \leq 115\text{ }^{\circ}\text{C}$ $B_{max} = 300\text{ mT}$
Winding	Copper foil, $\lambda_{Cu} = 380\text{ Wm}^{-1}\text{K}^{-1}$ $\sigma_{Cu} = 56 \cdot 10^6\text{ }\Omega^{-1}\text{m}^{-1}$ $T_{w,max} \leq 125\text{ }^{\circ}\text{C}$
Insulation	Pond-Ply® (Bergquist) $\lambda = 0.8\text{ Wm}^{-1}\text{K}^{-1}$, thickness $127\text{ }\mu\text{m}$
Inverter stage	
MOSFETS	APT50M75 (Microsemi, former APT) $R_{DS,on} = 150\text{ m}\Omega$ ($125\text{ }^{\circ}\text{C}$) $R_{th,j-S} = 0.32\text{ KW}^{-1}$ (incl. thermal grease) $T_{j,max} \leq 140\text{ }^{\circ}\text{C}$ (max. junction temperature)
Driver	IXDN414SI (IXYS)
Rectifier stage	
Diodes	APT100S20 (Microsemi), Schottky rectifier $V_F = 0.9\text{ V}$ (100 A , $125\text{ }^{\circ}\text{C}$) $R_{th,j-S} = 0.36\text{ KW}^{-1}$ (incl. thermal grease) $T_{j,max} \leq 140\text{ }^{\circ}\text{C}$ (max. junction temperature)
Output capacitor	
C_{out}	$2.2\text{ }\mu\text{F}$, 100 V , X7R, 1210-housing (Murata)
Miscellaneous	
Electrical	$V_{in} = 400\text{ V}$, $V_{out} = 54\text{ V}$, $P_{out} = 5\text{ kW}$
CSPI	$23\text{ WK}^{-1}\text{dm}^{-3}$ (aluminium-based heat sink)
Ambient	$T_a = 40\text{ }^{\circ}\text{C}$
Control	CPLD MachXO 2280C (Lattice)
Height	max. 1 U ($1.75\text{ in} \approx 44\text{ mm}$)

The volumes and losses resulting from the optimisation process are illustrated in **Fig. 2.30** in dependency of the switching frequency. The minimum calculated volume $V \approx 0.33 \text{ dm}^3$ (20.1 in^3) is reached at a switching frequency of $f_{\text{sw}} \approx 200 \text{ kHz}$. At this point, only the net components volumes are considered as the final converter volume depends strongly on the mechanical design. The resulting power density considering the net component volumes is $\rho \approx 15.2 \text{ kWdm}^{-3}$ (249 Win^{-3}) which is approximately 20 % more compared to the series-parallel-resonant converter with integrated magnetics. The calculated efficiency at the volume-optimised switching frequency is $\eta \approx 95.2 \%$ which can be increased to the maximum of 95.5 % at approximately 100 kHz switching frequency, still optimising for volume, if the power density is approximately 5 % decreased.

As shown in **Fig. 2.30**, the total converter volume at lower frequencies is mainly determined by the magnetic components as the magnetic flux density B is increasing, however limited by the core material ($B_{\text{max}} = 300 \text{ mT}$ for the applied ferrite material). Furthermore, the required current-doubler inductance is increasing with decreasing frequencies in order to guarantee an adequate (and limited) current ripple in the output filter and to limit the current peaks in the inverter stage. For low frequency-operation, which is commonly the case for highly efficient converter systems, a magnetic material allowing a higher flux density would be more appropriate especially for the inductors.

The winding and core losses in the magnetic components are both depending on the switching frequency which results in a loss-increase and therefore an increase of the required cooling volume for higher frequencies⁴⁶. The conduction losses of the rectifier diodes are assumed to be independent from the switching frequency. The conduction losses in the MOSFETs are in contrary increasing as the RMS-current is higher due to the decreased effective duty cycle (the leakage inductance is assumed to be constant in the modulation). The switching losses in the MOSFETs, however, are vastly increasing with increasing frequencies resulting in a higher required cooling volume. MOSFETs with a smaller output capacitance (but higher on-resistance) are therefore more appropriate at higher switching frequencies. The gate driver losses are furthermore (linearly) increasing with the switching frequency.

⁴⁶The loss and volume increase is not particularly shown in **Fig. 2.30** as the frequency is limited to 500 kHz in order to present more details around the optimised switching frequency.

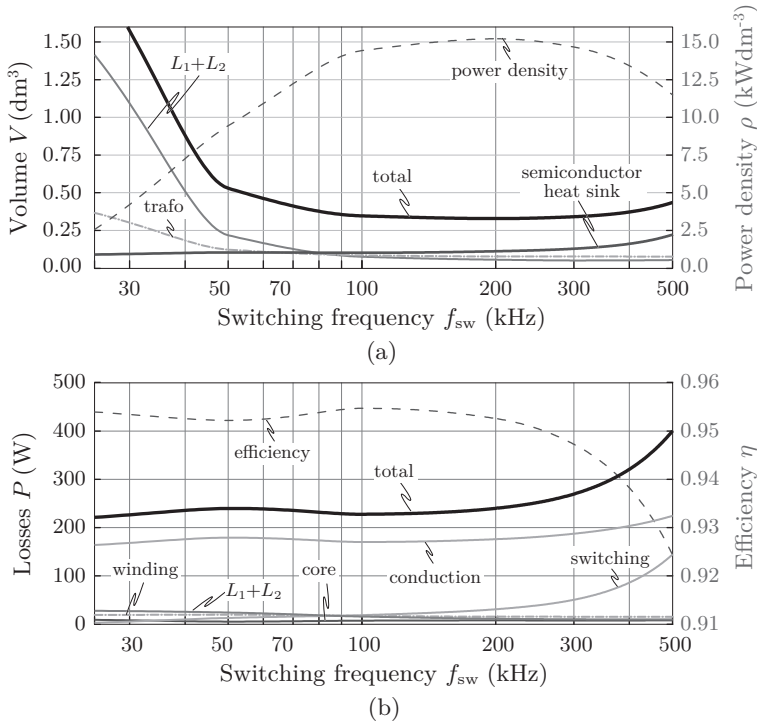


Figure 2.30: Volumes (a) and losses (b) as function of the switching frequency of the power-density-optimised phase-shift converter with current doubler output. (Note, the residual frequency-independent volumes and losses are omitted because of the small amount.)

The conduction losses of the MOSFETs are slightly increased at 50 kHz due to the integer value of the turns number. The volume-optimised turns ratio N_p/N_s results in slightly higher RMS-currents, which is shown by the efficiency drop at 50 kHz in **Fig. 2.30(b)**.

The constant volumes considered, for example for the auxiliary supply and control, are omitted in **Fig. 2.30** for the sake of clarity. Additionally not depicted is the output capacitor volume, which is dependent on the switching frequency. However, the volume share is rather small compared to, for example the net capacitive filter for the above presented LCC-resonant converter.

The characteristic values resulting for power-density-optimised con-

Table 2.6: Power-density-optimisation results for the phase-shift PWM converter with current doubler rectifier.

Operating point		
Switching frequency	200 kHz	
Duty cycle	0.81	
Power density	15.2 kWdm ⁻³ (249 Win ⁻³)	
Efficiency	0.95	
Transformer		
Volumes: Core+HTC+wind.	0.029 dm ³ (1.79 in ³)	
Heat sink	0.048 dm ³ (2.93 in ³)	
Losses: Winding	15.1 W	
Core	7.4 W	
Flux density	300 mT	
Leakage inductance	2 μ H	
Output inductor		
Volumes L_1 and L_2	0.056 dm ³ (3.42 in ³)	
Losses L_1 and L_2	20.1 W	
Flux density	300 mT	
Output inductance	6.8 μ H	
Semiconductors		
Volume: Heat sink	0.112 dm ³ (6.83 in ³)	
Losses: MOSFET conduction ..	92.4 W	
MOSFET switching	27.9 W	
Rectifier conduction ...	83.3 W	

verter system are summarised in **Tab. 2.6**. The optimum system is operated with a switching frequency of 200 kHz (duty cycle $D=0.81$) where the system features an efficiency of approximately 95 % (calculated) at full load. The ZVS-condition is guaranteed with a transformer leakage inductance of 2 μ H. The transformer operates with the maximum flux density of 300 mT resulting in approximately 22.5 W total losses.

The optimised current doubler inductance is 6.8 μ H and the resulting

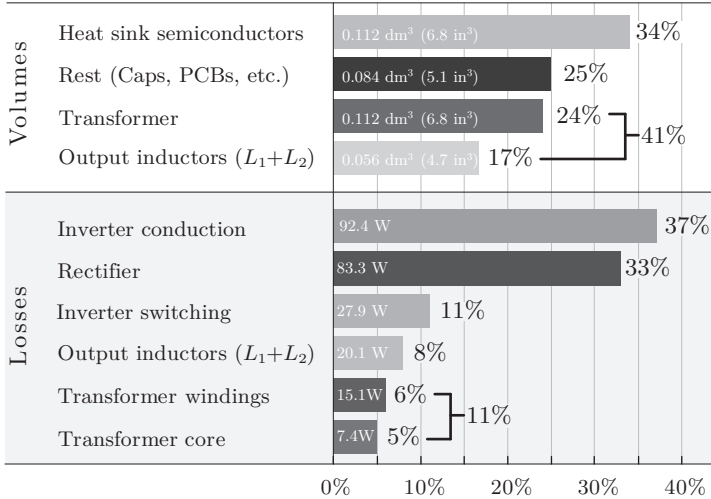


Figure 2.31: Loss and volume distribution of the power-density-optimised phase-shift converter with current doubler rectifier.

inductor flux density is similar to the transformer at the maximum specified value of 300 mT. Approximately 10 W losses are calculated for each inductor. The magnetic components together have the highest share on the volume distribution (41 %) followed by the semiconductor heat sinks (approximately one third of the total volume) as illustrated in **Fig. 2.31**. The residual components, such as the output capacitor and PCBs, result in a considerable volume share of 25 %.

The second-highest share on the losses is contributed by the rectifier diodes (one third of the total losses). A solution with higher efficiency would be the application of a synchronous rectifier employing paralleled MOSFETs which would, however, increase the required mounting space as well as the space for the gate driver circuits (including the galvanically isolated power supply and signal transfer). The total losses in the transformer are 22.5 W and the losses in the two current doubler inductors are 20.1 W. These losses could only be decreased by increasing the devices volumes. The residual losses, for example in the output capacitors and auxiliary supply, are not listed because of the comparably small loss share.

A reduction of the volume can be obtained by the integration of the

magnetic components (transformer and current doubler inductors) on a single core. Possible concepts are discussed in the following subsection.

2.2.4 Magnetic Integration of the CDR

The integration of the transformer and current doubler inductors on a single core has been discussed, e.g. in [177–182] (sorted by the year of publication). Due to the integration, the calculated theoretical volume reduction for the prototype constructed is more than six percent, if only the net device volumes are considered. However, the space required for spacing, mounting and interconnections is even for high-power-density systems up to a third of the total volume, and therefore the actual power-density-gain of the magnetic integration is more than ten percent. The characteristic converter operation excluding the integrated magnetic component remains basically unchanged.

The main three integration concepts for the current doubler as presented in **Fig. 2.32** are summarised in the following⁴⁷. In the concept shown in **Fig. 2.32(a)**, the former single secondary winding is split into two windings arranged on the outer leg of the E-core. The primary winding remains on the centre leg. Two air-gaps are introduced on the outer legs of the E-core which determines the inductance values of the equivalent current doubler filter inductors. The resulting flux distribution in the three legs is illustrated on the right-hand side of **Fig. 2.32(b)**. The centre-leg flux $\Phi_c = \Phi_2 - \Phi_1$ resulting from the applied voltage v_{AB} shows a high peak-to-peak value which results in considerable core losses. A further disadvantage of this integration concept is that standard E-cores which commonly obtain the air gaps in the centre leg cannot be applied. Furthermore, this concept results in a high stray field because of the leakage flux between the primary and secondary windings which potentially results in increased electro-magnetic interferences.

The leakage flux can be reduced by applying the concept presented in **Fig. 2.32(b)**, where the primary winding is doubled and each half is arranged together with the secondary windings on the outer legs. The flux distribution and consequently the relatively high flux ripple in the centre leg remains equal compared concept (a)⁴⁸. The filter inductance

⁴⁷More detailed information as well as analytical models can be found in the listed literature.

⁴⁸The equivalent reluctance models of the integrated magnetic devices are similar or convertible into each other, respectively, as shown in **Fig. 2.33(a)** and

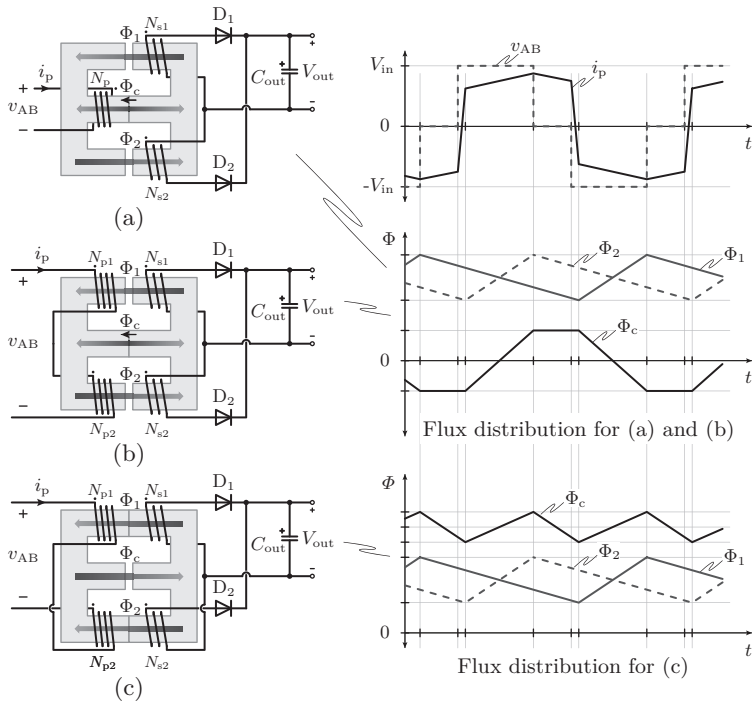


Figure 2.32: Concepts for integrating the magnetic components of a phase-shift PWM converter with current doubler on a single core.

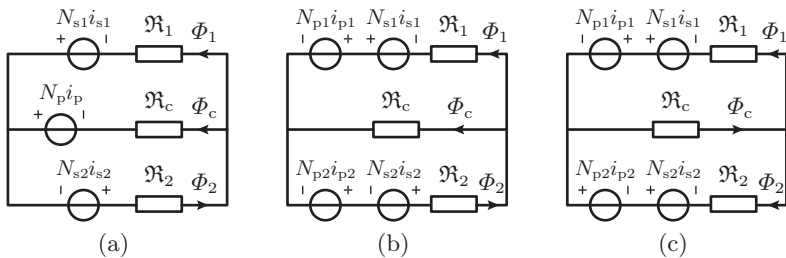


Figure 2.33: Corresponding reluctance models for the magnetic integration of transformer and current doubler inductors.

value is still adjusted with the air gaps in the outer legs so that standard E-cores are not suitable.

In [178], the concept according to **Fig. 2.32(c)** is introduced which is obtained by changing the direction of the flux injection Φ_2 . As illustrated in **Fig. 2.32(c)** and **Fig. 2.33(c)** this change is realised by swapping the terminal connection of the primary and secondary winding arranged on leg 2. The main advantage of this concept is the reduction of the flux ripple in the centre leg as shown in **Fig. 2.32(c)** resulting in a reduction of the core losses⁴⁹. This concept furthermore allows the application of standard E-cores forming the air gap in the centre leg which adjusts the original current doubler inductances L_1 and L_2 ,

$$L_{1,2} = \frac{N_{s1,2}^2}{\mathfrak{R}_{1,2} + 2 \mathfrak{R}_c}, \quad (2.111)$$

which can be derived by analysing the characteristic operation waveforms, as e.g. in [179, 183, 184]. The reluctances can be determined with the permeability of the applied ferrite material and the geometry parameters of the core, cf. **Fig. 2.29**,

$$\begin{aligned} \mathfrak{R}_c &= \frac{b + a/2}{\mu_0 \mu_r a c} - \frac{l_\sigma}{\mu_0 a c} \\ \mathfrak{R}_1 &= \frac{b + 2d + 2a}{\mu_0 \mu_r \frac{a}{2} c}, \end{aligned} \quad (2.112)$$

where l_σ is the required air gap length to adjust the inductance which can be determined by substituting (2.112) in (2.111) and solving for l_σ .

Because its advantages, concept (c) is considered for the prototype design as illustrated in **Fig. 2.34**. The principle current and voltage waveforms excluding the integrated magnetic device remain unchanged as mentioned above. During the powering state, i.e. state ①, cf. **Fig. 2.26**, where the positive input voltage V_{in} is applied to the primary side of the transformer, the voltage v_{s1} across the secondary winding N_{s1} is positive and diode D_1 is forward biased, whereas v_{s2} , cf. **Fig. 2.34**, is negative and D_2 is consequently reverse-biased. D_1 is further conducting in the free-wheeling state ②. Once the current has changed the direction after the negative input voltage is applied to the primary side in the powering state ③, the secondary side current commutates hard to

Fig. 2.33(b).

⁴⁹The flux ripple could theoretically be cancelled with a duty cycle of 50 %.

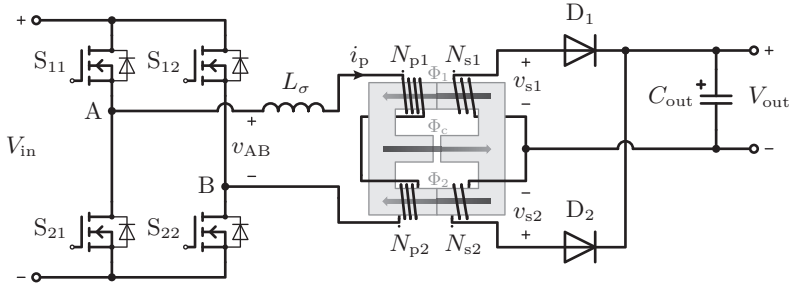


Figure 2.34: Schematic of the phase-shift PWM converter with integrated current doubler inductors.

D_2 . This current commutation results in voltage overshoots because of the energy stored in the leakage inductance between the two secondary windings. As the resulting voltage peak has to be damped in order to apply the suggested Schottky diode rectifier, an almost loss-less snubber circuit is applied as introduced in section 2.3.

The discrete current doubler filter inductors of the original converter design carry approximately half of the output current at each time over a switching period. If the secondary windings N_{s1} and N_{s2} are related to the integrated inductances, it can be concluded that virtually only one inductor is carrying the entire output current. The original name “current doubler” is in that perspective not entirely correct any more. However, as the characteristic current and voltage waveforms outside the magnetic device remain unchanged, the designation “integrated” current doubler is further used.

The geometry parameters of the integrated magnetic device have to be determined. Similar to the discrete devices, an optimal core geometry exists for the integrated assembly which results in the minimum volume. The integrated structure has therefore been analytically described and the geometry parameters are optimised with respect to a maximum power density, comparable to the inner optimisation process as presented above. The pre-optimised specifications which define the operating point such as switching frequency, inductance values, and turns ratio have further been employed in order to validate the original analytical operation models. The operating point including the model of the integrated structure in the global optimisation process might differ from the original design. In [183, 184] the optimised geometry

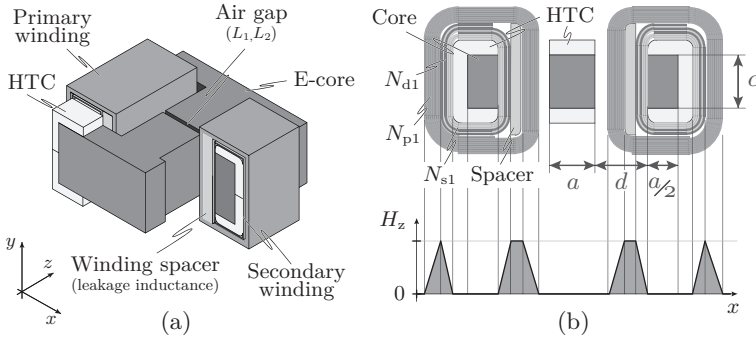


Figure 2.35: Winding arrangement of the integrated current doubler. (a) E-cores with windings (a cuboid is cut out to show more details); (b) Cut through the core and windings in the x - y plane.

parameters have been determined. The resulting optimal parameters are close to an assembly with standard E-core E653227 from EPCOS (optimised volume: 0.18 dm^3 ; assembly with standard core: 0.219 dm^3).

More details of the transformer assembly are presented in **Fig. 2.35**. The windings are arranged on the outer legs as described before and illustrated in **Fig. 2.34**. A heat transfer component (HTC⁵⁰) is applied which functions additionally as case for the E-cores similarly as for the high-power-density LCC-resonant prototype. More details about the cooling system are presented in the next subsection together with the realised prototype. As a specific amount of leakage inductance is required for the ZVS-operation ($2 \mu\text{H}$ have been determined) the existing leakage flux is slightly increased by providing a space between the primary and secondary winding, cf. **Fig. 2.35(a)** and **(b)**. The field emission outside the windings is small compared for example to the integration concept in **Fig. 2.32(a)** and the spacer thickness resulting in the required leakage inductance can be calculated with the energy E_m stored in the space,

$$E_m = \frac{1}{2} \int \mu_0 H_z^2 b_f l_w dx = \frac{1}{2} L_\sigma I_p^2, \quad (2.113)$$

where b_f is the foil width and l_w is the winding length. The effective leakage inductance is the sum of the leakage inductance of the two outer

⁵⁰The HTC in **Fig. 2.35** is not entirely shown in order to present the E-cores below. The complete HTC which additionally functions as case is shown in **Fig. 2.36**.

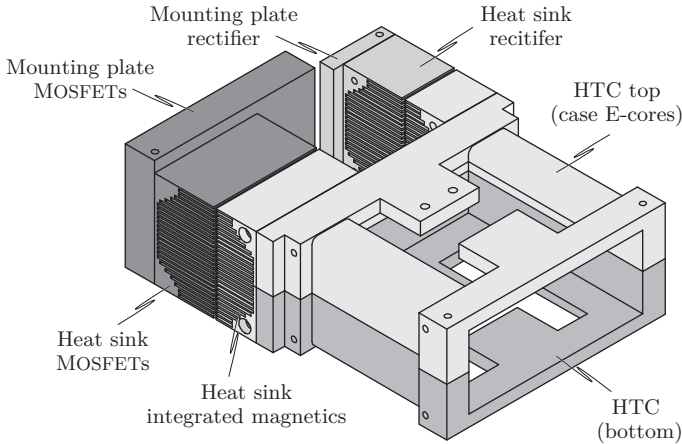


Figure 2.36: Applied cooling system for the phase-shift converter with integrated magnetics.

legs, as shown by the almost constant magnetic field in the region of the winding spacer in **Fig. 2.35(b)**.

As a closer look at **Fig. 2.35(b)** shows, an additional winding N_{d1} (and furthermore N_{d2} on the second outer leg) is interleaved with the secondary winding. This winding is part of a snubber network as presented in section 2.3.

The high-power-density prototype with the described integrated magnetic device and the applied standard E-cores is presented in the next subsection.

2.2.5 Realised Ultra-Compact CDR Prototype

The basis for assembling the prototype is the cooling system as shown in **Fig. 2.36** consisting of four parts: the heat sinks for the semiconductors (MOSFETs and rectifier diodes) and the (top and bottom) case for the set of E-cores of the integrated magnetic device, which intrinsically functions as heat transfer component and heat sink. Across the air gap in the centre leg the HTC is cut preventing eddy current injection due to the field emission of the gap. A high-performance fan is placed in the middle of the cooling system, cf. **Fig. 2.37**.

Table 2.7: Components and construction details for the prototype of the phase-shift PWM converter with integrated magnetics.

Semiconductor			
MOSFETs	Microsemi APT81H50L TO-264	Rectifier diodes	Microsemi APT100S20B TO-247
Gate driver	IXYS IXDN414SI 14 A-type	Control	Lattice CPLD LCMXO2280
Integrated magnetics			
Core	EPCOS E653227	Turns ratio	$N_p:N_s$ 11:4
Primary Winding		Secondary Winding	
Foil Thickness	50 μm	Foil Thickness	100 μm
Snubber and Filter Network			
Turns No.	$N_d = 2$	Foil thickness	50 μm
Snubber diode	ST Microelect. STPS60170CT TO-220	Output Caps ($C_{out}=50 \mu\text{F}$)	Murata (X7R) 2.2 $\mu\text{F}/100 \text{ V}$ 1210-housing

The determination of the optimal heat sink geometry is similar as for the LCC-resonant converter based on the approach as summarised by Drofenik in [154, 157, 158]. In the master thesis [183] the cooling system shown in **Fig. 2.36** has been modelled and optimised with respect to minimum volume, considering the specified maximum allowed temperature of the core, insulation, and MOSFETs as constraints and neglecting the heat transfer to the ambient via the surface of the HTC, i.e. no heat radiation and no free convection was considered. The applied calculation has been validated by the 3D CFD simulation software ICEPACK. The resulting deviation compared to the calculated values is between -8 % and -13 %, which is sufficiently accurate and leaves a small safety margin in case of higher losses as calculated.

The main specifications of the prototype design are summarised in **Tab. 2.7**. The snubber network and the listed specifications are ex-

plained in the next section. In **Fig. 2.37** a CAD drawing of the realised prototype is shown. A cuboid is cut out the system on the right-hand side in order to present some more details from inside of the case. The windings are connected with flat laser-cut copper bars to the rectifier stage and the full bridge⁵¹ and, moreover, the copper bars are directly connected with the terminals of the semiconductor devices, where possible. As thermally conductive insulation material for the windings, Bond-Ply[®] from Bergquist has been applied (similar as for the resonant converter prototype). The MOSFETs are electrically isolated from the heat-sink with High-Flow[®] (Bergquist), whereas the diodes are directly mounted on the heat sink with a thermal grease (HTCP Plus from Electrolube), as the heat sink is electrically isolated from the surrounding components. The heat flow is from the rectifier side to the MOSFET's heat sink.

On the front-side of the converter the control-PCB with a 3.3 V power supply, digital control, output-voltage measurement, and the ADC for the control, as well as the gate-driver circuits and programming interfaces is arranged. The control signal and PWM-signal generation for the full-bridge switches is implemented in VHDL on the CPLD LCMXO2280 from Lattice. A more convenient combination of CPLD and floating point digital signal processor (DSP) is not applied for sake of compactness. The power supply of the high-side-switch gate-driver circuits are realised with a bootstrap circuit in order to avoid the required volume for a galvanically isolated power supply.

The measured primary side current and voltage waveforms under full-load conditions are presented in **Fig. 2.38**. Due to the zero voltage switching of the full-bridge MOSFETs no voltage ringing can be observed on v_{AB} . The primary current waveform i_p in **Fig. 2.38** differs from the basic waveform (as shown for example in **Fig. 2.26** on page 128) at the points where the positive or negative input voltage is applied to the transformer. The observed current peaks occur due to the active damping network, which takes part at the power conversion in this phase. As soon as the damping network is inactive after a certain time, the current slope is similar to the basic current doubler waveforms without oscillations⁵².

In **Fig. 2.39** the measured efficiency is presented in dependency of

⁵¹The full-bridge connectors are not shown in **Fig. 2.37** as they are located on the rear side of the converter.

⁵²The snubber network is presented in the next section.

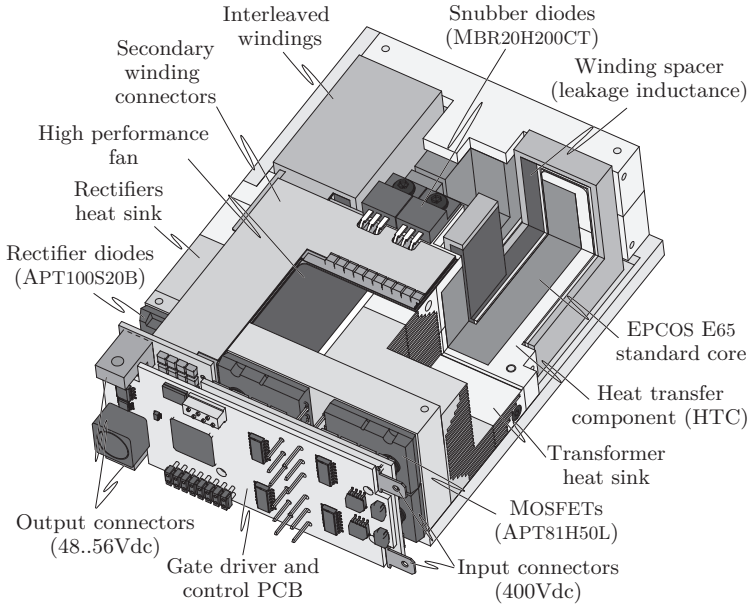


Figure 2.37: CAD drawing of the phase-shift PWM converter with integrated current doubler assembly. A cuboid has been cut out in order to present more details.

the output power and for different output voltage levels. As shown in **Fig. 2.31**, the efficiency is mainly influenced by the conduction losses of the power semiconductors, which explains the higher efficiency levels for higher output voltages because of the smaller RMS-current values. The efficiency curves are flat in a wide load range, i.e. for 20 %..100 % of rated load. The deviation of the measured (94.4 %) and calculated efficiency (95.2 %) is 0.8 % which corresponds to approximately 44 W higher losses than calculated. Thermal measurements identified similarly to the LCC-resonant-converter prototype the diodes connections as an additional heat loss source (more than 30 W losses have been identified in section 2.1.4 as additional loss source). A thermal measurement with an infrared camera excludes the semiconductors and the magnetic device as main contributors to the additional losses as the calculated and measured heat sink temperatures are in good agreement (MOSFET 94 °C measured, 100 °C calculated; rectifier 113 °C measured, 112 °C

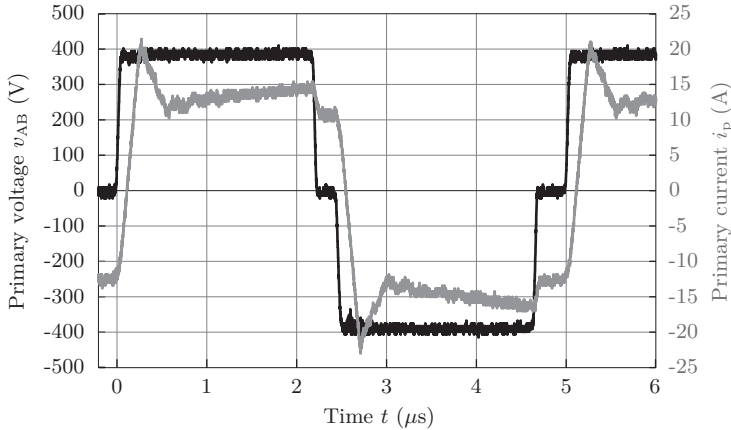


Figure 2.38: Measured primary side current and voltage waveforms of the phase-shift PWM converter with integrated current doubler rectifier at full load ($V_{in} = 400\text{ V}$, $V_{out} = 54\text{ V}$, $P_{out} = 5\text{ kW}$).

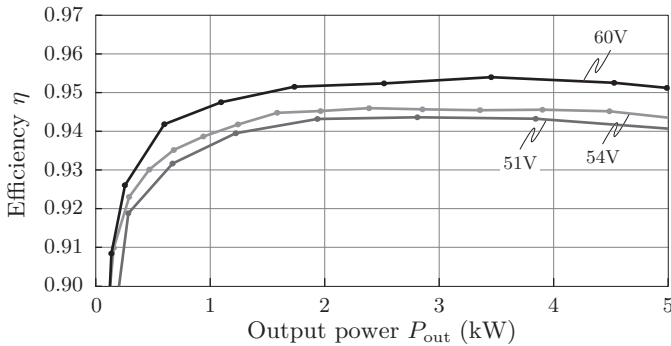


Figure 2.39: Measured efficiency with phase-shift PWM converter with integrated current doubler in dependency of the output power.

calculated).

A photo of the prototype converter is presented in **Fig. 2.40**⁵³. The resulting power density of this prototype is 9 kWdm^{-3} (147 Win^{-3}), i.e. approximately 15 % more volume as the LLC-resonant prototype. Both

⁵³The aluminium cover on top of the case is not assembled in order to present some more details (winding and snubber circuit.)

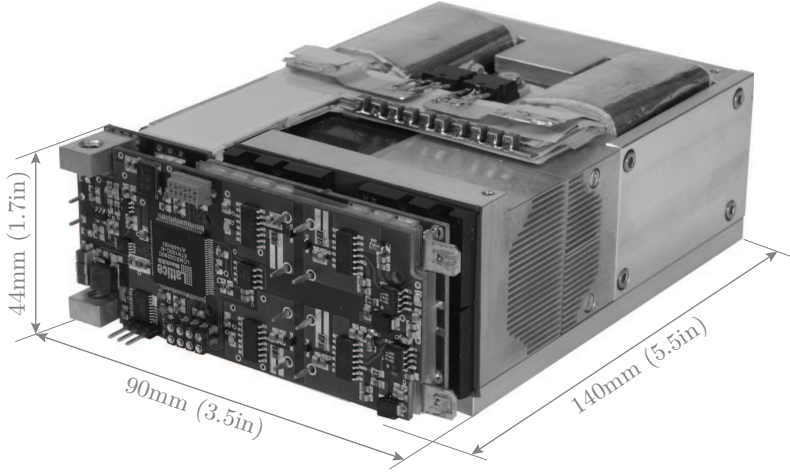


Figure 2.40: Photo of the realised 5-kW phase-shift converter prototype with integrated current doubler. (The top cover is removed to show the windings and the snubber circuit.) Power density: $\rho = 9.0 \text{ kWdm}^{-3}$ (148 Win^{-3}).

optimised systems which are based on different converter topologies obtain quite similar power densities, especially if the phase-shift converter prototype would have been assembled with a custom-made core as well.

In the next section, the applied snubber circuit is presented which guarantees the rectifier operation in the specified Safe Operating Area (SOA).

2.3 Loss-Less Snubber Circuits

The conventional current doubler and generally most of the PWM converter topologies operate with a hard-commutated secondary side rectifier. During the turn-off process of a rectifier diode (as discrete device or as anti-parallel body diode of a MOSFET) the recovery charge in the diode results in a overcharging of the parasitic device output capacitance related to the reverse-recovery current peak⁵⁴. This overcharging, because of the energy stored in the (parasitic) leakage inductance of

⁵⁴The modelling of the recovery process is discussed in section 3.3.

the rectifier circuit results in a voltage overshoot across the rectifier. The parasitic circuit elements (winding capacitance, leakage inductance, parasitic output capacitance of the diodes) and the output capacitor form a resonant tank in which a voltage ringing is initiated by the overcharged diodes output capacitance. The ringing energy is dissipated in the rectifier circuit which results in additional losses. Moreover, the overvoltage resulting from the ringing can destroy the semiconductor device because of the limited blocking voltage capability.

One possibility to guarantee a reliable operation of the converter is the application of diodes (or MOSFETs in case of a synchronous rectifier) with a higher blocking voltage capability which would however result in higher losses due to the increased channel resistance and forward voltage drop, if the chip area remains constant, or in a higher chip area, e.g. by applying devices in parallel. Both possibilities result in a higher volume (due to the increased heat sink or mounting area) which is undesirable. A higher blocking voltage capability furthermore excludes commonly the application of Schottky rectifiers as these devices are rarely available for higher current and voltage specifications compared to the used devices. An application of common silicon devices, however, results in even higher voltage peaks because of the significantly higher recovery effects.

If the circuit topology should remain unchanged, i.e. no auxiliary circuits which force the current commutation during the free-wheeling phase where the voltage is clamped, e.g. [77] should be employed, and the proposed rectifier diodes should still be used, the application of a snubber circuit is a second possibility. Snubber circuits can generally be classified into lossy and (almost) lossless snubber topologies. In the first listed class, the ringing energy is dissipated in the snubber circuit elements, e.g. the classical RC and RCD snubber circuits or the voltage-clamping with a Zener diode. Lossy snubbers are not further considered here because the ringing energy is relatively high for the given electrical specifications which would result in a large snubber volume necessary to dissipate the generated heat.

The second class contains the (almost) lossless snubber circuits which are preferred for systems with high output power (above 500 W). The basic idea is to clamp the rectifier voltage and transfer the ringing energy to the output (or input) or to provide the energy to other system sub-circuits, such as an auxiliary power supply. These snubber circuits can employ actively switched semiconductors, as presented for

instance in [185, 186], or one or more diodes, i.e. passively switched devices. In the literature, a high number of possible topologies exists for both strategies. For the sake of a low control complexity only non-actively switched circuits are further considered. Two representatives are exemplarily investigated in the following.

The integrated magnetics and the rectifier stage including the parasitic circuit elements (L_w , C_w , and C_d) contributing to the resonant tank and the measured voltage ringing⁵⁵ across the rectifier diode D_1 are presented in **Fig. 2.41(a)**⁵⁶. The measured voltage exhibits a distinctive ringing and the voltage amplitude is more than twice of the ideal blocking voltage ($2V_{out}$). If the converter would be operated with the nominal output voltage, the ringing voltage amplitude would exceed the specified blocking voltage of the applied diodes ($V_R = 200\text{ V}$) and possibly destroy the devices or at least generate higher losses due to the avalanche energy.

The snubber circuit shown in **Fig. 2.41(b)** and published in [187] consists of two diodes (D_{s1} and D_{s2}) and one capacitance C_{s1} . In case of the current commutation from D_1 to D_2 the blocking voltage is built up and the capacitor C_{s1} is charged via the snubber diode D_{s1} during the time when ringing voltage amplitude is higher than the ideal blocking voltage. During the negative ringing cycle (diodes voltage $v_{D1} < 2V_{out}$) the capacitor C_{s1} is (partly) discharged via the second diode D_{s2} and the energy is transferred to the output of the converter. These charging and discharging processes via D_{s1} and D_{s2} are repeated for the following ringing periods and the ringing energy is successively removed. Besides ohmic losses in the diodes and connections and the dielectric losses in the snubber capacitor, not further losses are generated in this snubber circuit. The measured voltage v_{D1} across the rectifier diode applying this snubber circuit is presented on the right-hand side of **Fig. 2.41(b)**. It can be observed that the voltage amplitude is generally damped compared to the un-damped ringing voltage (grey curve in **Fig. 2.41(b)**), however, the first voltage peak exhibits still a high magnitude (approximately 20 % reduced) which could still push the rectifier diode into the avalanche.

⁵⁵Note, that in order to operate in the specified SOA of the rectifier diodes, the converter input and output voltage have been reduced during the measurements.

⁵⁶In the schematics of **Fig. 2.41** only the parasitic and snubber circuit elements of the rectifier diode D_1 are presented due to the lack of space. A snubber circuit has to be employed for the practical system also for the second rectifier path with diode D_2 .

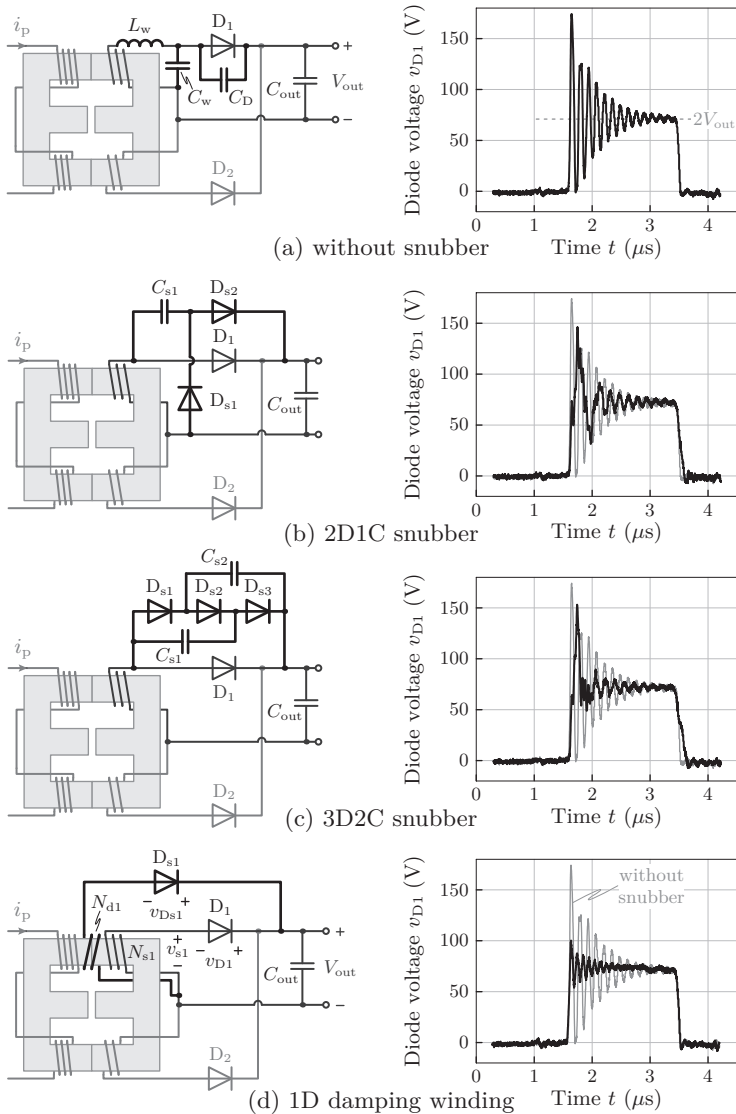


Figure 2.41: Comparison of different snubber circuits for D_1 applied in the phase-shift PWM converter prototype. Note, that the measurements have been performed with a reduced input voltage ($V_{in}=200$ V, $V_{out} = 35$ V) to guarantee the diode's blocking voltage limitations.

A further snubber topology consisting of two capacitors (C_{s1} , C_{s2}) and three diodes (D_{s1} , D_{s2} , D_{s3}) is presented in **Fig. 2.41(c)** which has been also discussed in [187]. The different charge and discharge current paths are similar to the above described circuit: if the ringing voltage exceeds the ideal blocking voltage, both snubber capacitors are charged via the diode D_{s2} . During the negative cycle ($v_{D1} < 2 V_{out}$) the capacitors are discharged via D_{s1} and D_{s2} . The application of three additional snubber circuit elements for every rectifier diode (compared to **Fig. 2.41(b)**) results in the almost-cancellation of the negative ringing cycle and the voltage is approximately clamped to the ideal blocking voltage thereafter, however, the voltage peak of the first ringing cycle is still on the same voltage level as for 2D1C snubber, which is shown in **Fig. 2.41(b)**, and the risk of a device destruction therefore still exists.

The snubber circuit in **Fig. 2.41(d)** has been added to also dampen the first ringing voltage peak⁵⁷. The snubber circuit, which is described in [188] consists only of a small snubber winding N_{d1} and a snubber diode D_{s1} . Regarding the circuit diagram in **Fig. 2.41(d)**, the snubber diode D_{s1} becomes forward-biased ($v_{Ds1} \leq 0$) when the voltage v_{d1} across the damping winding N_{s1} is higher than the output voltage V_{out} ($V_{out} = v_{Ds1} + v_{d1}$), i.e. the voltage across the damping winding is clamped to the output voltage ($V_{Nd1,max} = V_{out}$). The basic idea behind the snubber circuit is that the damping winding N_{d1} and secondary winding N_{s1} are magnetically coupled and the voltage relationship of both windings is given by

$$v_{s1} = v_{d1} \frac{N_{s1}}{N_{d1}}, \quad (2.114)$$

assuming an ideal coupling between the two windings. As a consequence, the maximum voltage across the rectifier diode is clamped to

$$\begin{aligned} V_{D1,max} &= |V_{s1,max}| + V_{out} \\ &= |V_{d1,max}| \frac{N_{s1}}{N_{d1}} + V_{out} \\ &= V_{out} \left(1 + \frac{N_{s1}}{N_{d1}} \right). \end{aligned} \quad (2.115)$$

Assuming that the snubber should not contribute to the power transfer from the input to the output of the converter, the level of the maximum

⁵⁷Necessity is the mother of invention.

rectifier blocking voltage $V_{D1,\max}$ should be slightly higher than the ideal blocking voltage, i.e. $V_{D1,\max} \geq 2V_{\text{out}}$. The turns number of the damping winding N_{d1} should in this case be smaller than the secondary winding turns number N_{s1} ($N_{d1} \leq N_{s1}$), which directly results from (2.115).

The resulting blocking voltage across the rectifier diode D_1 is presented on the right-hand side of **Fig. 2.41(d)**. The voltage ringing could be drastically reduced by a factor of four. The remaining voltage ringing is caused by the leakage inductance between the damping and secondary winding which should be consequently kept low. The good coupling of the damping and secondary winding in the prototype is obtained by interleaving the two windings as presented in **Fig. 2.35** on page 155. The required high coupling coefficient further explains why the damping winding should for instance not be wound around the centre leg, which would, however, be possible as the magnetic flux caused by the voltage ringing is present in the centre leg as well.

As indicated above, the active power transfer of the snubber circuit would be possible as well, if the number of turns of the damping network would be equal or even higher than the turns number of the secondary winding and the snubber diodes would be selected with the corresponding current-carrying capability.

The active snubber circuit generally removes magnetic energy mainly from the ferrite core and transfers the energy directly to the output of the system. The primary current i_p differs therefore from the waveform of the conventional current doubler without the presented snubber network. The current slope during the rectifier commutation is limited by the leakage inductance between the primary and secondary winding. As long as the snubber network is active, additional energy is transferred to the output which can be observed by the small superimposed triangular current as presented in **Fig. 2.38** on page 160.

Universal Application of the proposed Snubber Circuit

The introduced “lossless” snubber topology is not restricted to the presented integrated current doubler and can be rather universally applied for galvanically isolated DC-DC converters. Moreover, the snubber circuit topology can be every half or full wave rectifier circuit, favourably with voltage output, e.g. the half-wave rectifier for every winding as presented above, or the full-wave rectifier as illustrated on the left-hand side of **Fig. 1.16** on page 41. The removed ringing energy can

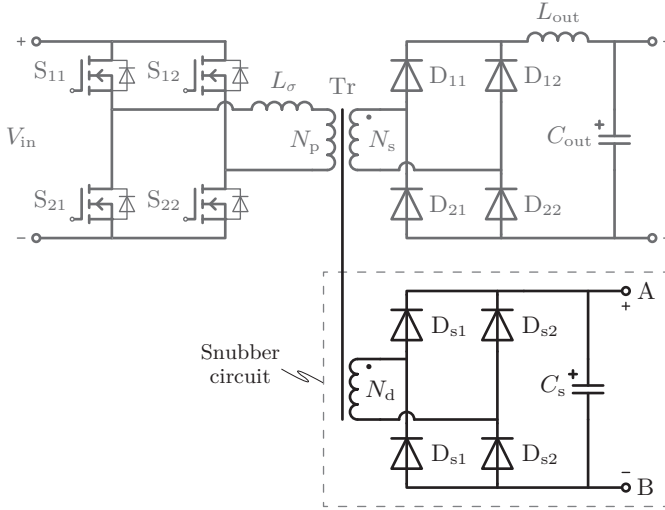


Figure 2.42: Example for the application of the “lossless” magnetic snubber circuit.

furthermore be supplied to a variety of loads, e.g. the actual converter load at the output as presented above, the input of the converter system, an auxiliary power supply, or fans.

A further example for a full-bridge DC-DC converter with bridge rectifier is presented in **Fig. 2.42** where the magnetic snubber circuit is a bridge rectifier consisting of the diodes $D_{s1}..D_{s4}$ and possibly an output capacitance C_s . Feeding back the ringing energy to input of a converter system, i.e. connecting the snubber output terminals *A* and *B* with the corresponding input terminal of V_{in} can be especially advantageous during the start-up phase of the converter system as the snubber circuit would be immediately active. On the contrary, a part of the power would be transferred via the snubber network during the start up if the snubber network is connected to the output, as the output voltage is initially zero and the snubber circuit exhibits a low-impedance current path compared to the LC-filter of the converter rectifier in **Fig. 2.42**. Feeding back the energy to the input consequently allows the implementation of diodes with a smaller current rating. The maximum voltage of the rectifier diodes $D_{11}..D_{22}$ is in this case given

by:

$$V_{D11,\max} = V_{\text{in}} \frac{N_s}{N_d}. \quad (2.116)$$

The snubber network should practically only transfer the ringing energy back to the input of the converter in this case. The maximum rectifier diode voltage $V_{D11,\max}$ therefore has to be adjusted slightly above the ideal blocking voltage ($v_{L\text{out}} + V_{\text{out}} = V_{\text{in}} N_s/N_p$) and consequently, the turns number of the damping winding N_d is defined as

$$N_d \leq N_p. \quad (2.117)$$

A general description of the proposed snubber topology can be found in the pending patents [188, 189].

3

Efficiency-Optimised Systems

The demand for high-power-density converter systems has been one of the most important performance drivers for power electronic systems for several decades. This trend could be well observed in the telecom power supply sector due to the increased demand on space for the ICT equipment and the facilitation of a more-efficient cooling. Power density will remain an important performance index in the future; however, in this young millennium a shift of the performance drivers to more efficient converter systems can already be seen. As discussed in chapter 1, this trend is driven mainly by increased environmental awareness and by the high operating costs of increasingly larger data centres.

This chapter is dedicated to the design of a highly efficient converter system. The initial aim is to show, that an efficiency of 99 % is possible for galvanically-isolated DC-DC converters even with a standard topology. The basic idea of the design approach for this high efficiency converter is similar to the approach for the high-power-density converter introduced above: the converter system is modelled with analytical equations which are applied in an optimisation procedure. The optimisation criterion is now the efficiency, or more precisely, the load-dependent efficiency related to the Energy Star® requirements for computer servers [27].

The operation characteristics of the selected converter system are introduced in section 3.1. The optimisation procedure for the high-efficiency design is presented in section 3.2 followed by a presentation of the underlying analytical models in section 3.3. The optimisation results are discussed in section 3.4 and the converter prototype is introduced in section 3.5. In conclusion, the sensitivities of the converter performance on the design parameters are discussed in section 3.6.

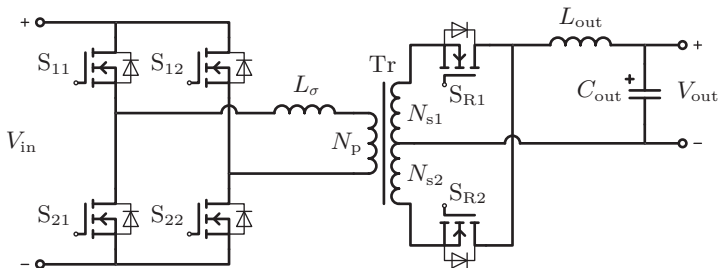


Figure 3.1: Schematic of the phase-shift PWM converter with centre-tapped secondary winding transformer (CTR) and LC-output filter.

3.1 Phase-Shift PWM Converter with Centre-Tapped Secondary Winding Transformer

The variety of the power supplies suitable for telecom applications has been discussed in section 1.4. The design space of high-efficiency power supplies is somewhat restricted to converter systems which feature the ability of soft-switching, small RMS-currents, and synchronous rectification in order to reduce the conduction losses in the output stage. The required galvanic isolation (telecom specification), high power transfer (project-defined 5 kW), and low complexity (reliability) further restrict the design space. The topologies applied in the high-power-density system basically fulfil the listed demands. It is further shown in chapter 2 that the resulting performance of two generally different topologies (LCC-resonant converter and phase-shift PWM converter) is almost similar.

The phase-shift PWM converter with a LC-output filter (CTR) as shown in **Fig. 3.1** fulfils the basic demands on the converter system and furthermore this topology confirms that the targeted efficiency is possible with a standard topology. The inverter stage is built with a full bridge. The galvanic isolation and voltage step-down is provided by a centre-tapped secondary winding transformer followed by the two-switch synchronous rectifier and the LC-output filter.

The operating principle of this topology, which is close to that of the phase-shift PWM converter with current doubler output stage (section 2.2), is summarised in this subsection based on the characteristic

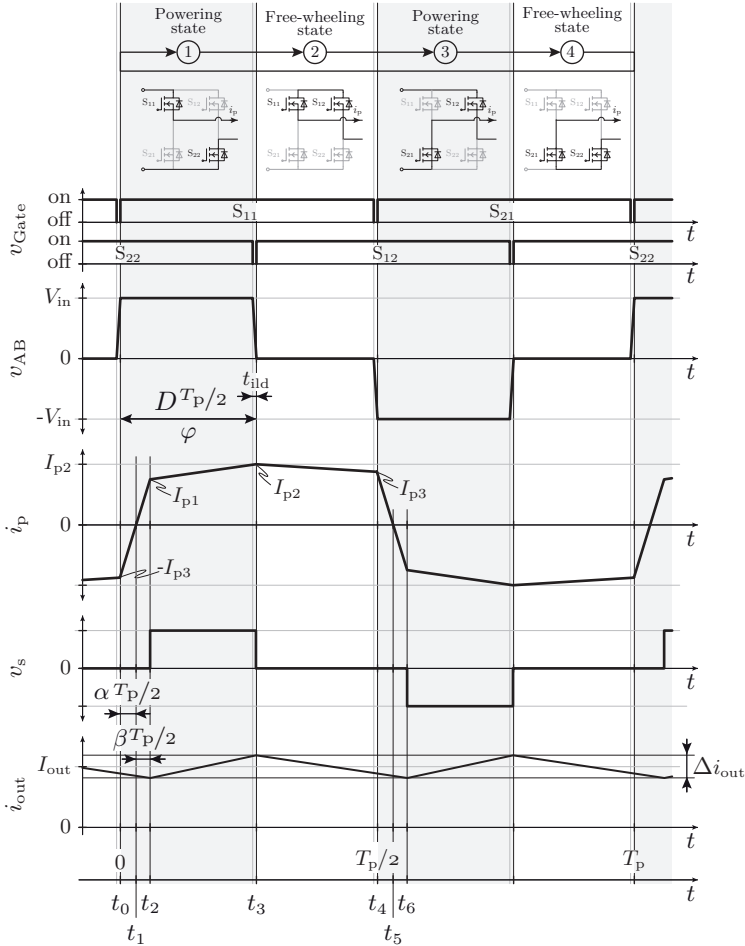


Figure 3.2: Characteristic current and voltage waveforms for the full bridge phase-shift PWM converter with centre-tapped secondary winding transformer and LC-output filter.

current and voltage waveforms in **Fig. 3.2** and the current-conduction paths for a half switching cycle $t_0 \leq t \leq t_4$ illustrated in **Fig. 3.3**.

$t_0 \leq t \leq t_2$ (**Fig. 3.3 (a)**) The powering-state ① starts when the high-side switch S_{11} is turned on with ZVS-conditions. The voltage across the mutual inductance of the transformer is still clamped by the rectifier and the converter input voltage is therefore applied to the leakage inductance of the transformer. In consequence, the primary current rises from the negative value $i_p = -I_{p3}$ remaining from the last free-wheeling state to the positive value $i_p = I_{p1}$. During this time interval, $t \in (t_0, t_2)$, where no power is transferred from the converter input to the output, the current commutates from S_{R2} to S_{R1} . At the point t_2 the body diode of S_{R2} is (hard) turned off and the entire secondary current is carried by the upper transformer winding N_{s1} .

$t_2 \leq t \leq t_3$ (**Fig. 3.3 (b)**) As soon as the rectifier switch S_{R1} carries the entire output current i_{out} , energy is transferred from the converter input to the output. The primary current rises from I_{p1} to I_{p2} mainly determined by the (primary-side-related) output inductance L_{out} . At $t_3 - t_{ild}$ (t_{ild} denominates the interlock delay time) the low-side MOSFET S_{22} is turned off and the parasitic output capacitance of the high-side switch is discharged whereas the voltage across the low-side switch increases to the converter input voltage. At point t_3 the high-side switch S_{12} can be turned on under ZVS-conditions.

$t_3 \leq t \leq t_4$ (**Fig. 3.3 (c)**) In state ② the current is free-wheeling in the high-side MOSFETs. The negative primary current slope is mainly determined by the rectifier stage, i.e. the output inductor in parallel with the output voltage. During free-wheeling state ② the second rectifier MOSFET S_{R2} can already be turned on under ZVS-conditions, however, the current will not commute noticeably to the second part of the centre-tapped winding and S_{R2} as no voltage is applied to the leakage inductance between the windings, which would force the current to change.

3.2 Design Process of an Efficiency-Optimised Phase-Shift PWM CTR Converter

The number of design parameters requires a comprehensive evaluation even though a standard topology has been selected. The main design parameters are illustrated in **Fig. 3.4**. These design parameters are in

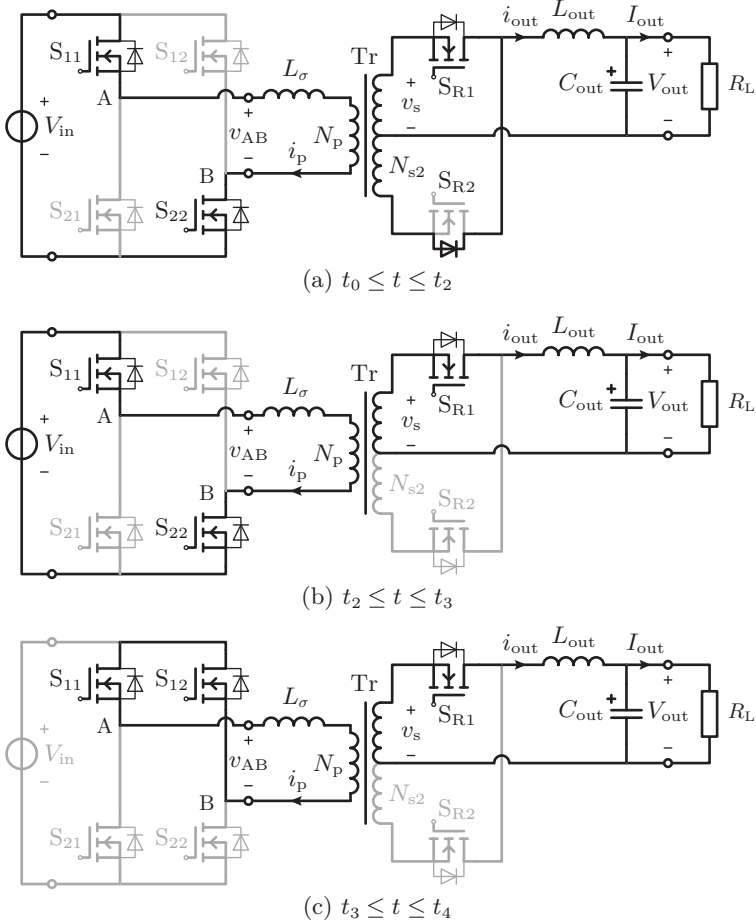


Figure 3.3: Switching states with emphasised current paths for the first switching cycle of the phase-shift PWM converter with centre-tapped transformer and LC-output filter.

principle similar to the power-density-optimised system. Besides the selection of the inverter and rectifier MOSFETs the model considers the option to connect semiconductors in parallel in order to decrease the conduction losses in the devices.

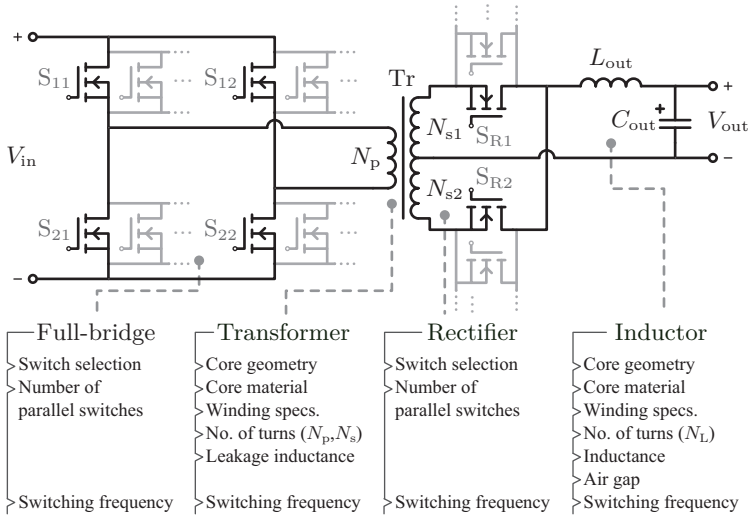


Figure 3.4: Main design parameters of the phase-shift PWM converter with centre-tapped secondary winding transformer and LC-output filter.

The design parameters for the magnetic devices remain unchanged for the new optimisation criteria, i.e. for optimising efficiency. During the design process, the core material and geometry, as well as the winding specifications (number of turns, winding geometry) and the inductance values must be determined.

The switching frequency has a major impact on the resulting design parameters of each component as it directly influences the losses in the semiconductors, cores, and windings. The parameter-interdependence, however, is much more pronounced and a sequential determination of these parameters will not necessarily result in a global optimum. Therefore, an automatic design procedure is applied as illustrated in **Fig. 3.5** – an approach similar to the high-power-density converter design process. The optimisation procedure is explained in the following paragraphs and the underlying comprehensive analytical models are presented in the next section.

The design procedure starts with the specification of fixed parameters in step ①, i.e. the selection of electrical, magnetic, and thermal material properties and converter constraints. Some materials and devices

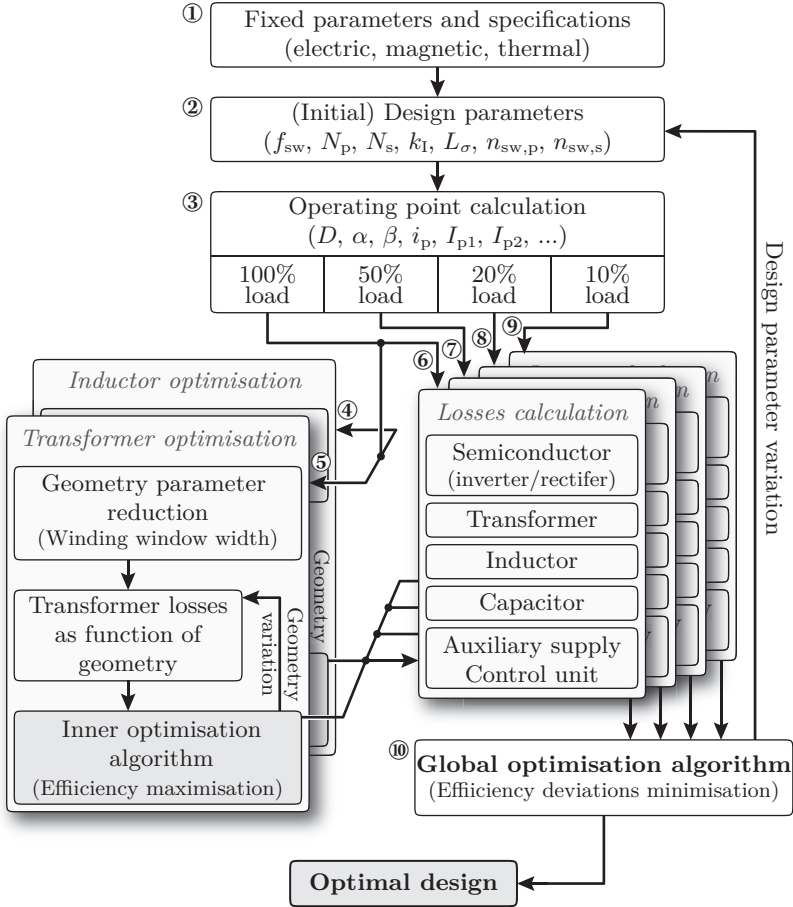


Figure 3.5: Automatic efficiency optimum design procedure for the phase-shift PWM converter considering the part-load efficiencies according to the Energy Star[®] requirements for computer servers [27].

are additionally fixed for sake of an acceptable computation time and the number of design parameters is therefore reduced. The materials for the transformer and inductor cores are for instance preselected, mainly based on knowledge obtained with the high-power-density converter designs. Moreover, the MOSFETs for the inverter and rectifier stage

are set as fixed parameters, stored in a data base of available high-performance devices resulting from preliminary runs of the optimisation procedure.

The initial design parameters can be defined in step ② based on experiences and knowledge which can reduce the computation time for the global optimisation algorithm.

Seven design parameters are considered in the global optimisation loop, cf. **Fig. 3.5**: the leakage inductance L_σ ¹ which defines the ZVS-range, the output current ripple factor k_I which defines the output inductance, the primary and secondary turns numbers N_p and N_s , as well as the number of paralleled inverter and rectifier MOSFETs $n_{sw,p}$ and $n_{sw,s}$. The remaining design parameters which determine the core geometry of the magnetic components as well as the number of turns of the inductor winding (in sum ten more parameters) could be further defined and varied in the outer global optimisation loop. These parameters, however, are determined in inner optimisation loops for the transformer and for the inductor² considering the computation time.

Moreover, only integer values are considered for the turn numbers (N_p and N_s) and the number of paralleled inverter and rectifier switches ($n_{sw,p}$ and $n_{sw,s}$). This is both practical and reduces the computation time. A further reduction of computation time can be achieved by preselecting the switching frequency points around the expected minimum, e.g. 16 kHz, 25 kHz, 37.5 kHz, 50 kHz, 100 kHz and 200 kHz. The minimum switching frequency for this example is selected right above the audible frequency and more frequency points are considered between 16 kHz and 50 kHz, as the optimum switching frequency is assumed to be in that range.

The remaining outer loop design parameter values – the permissible output current ripple factor k_I and the transformer leakage inductance L_σ – are varied in a certain range by the optimisation algorithm. The ripple factor k_I is defined as

$$k_I = \frac{\Delta i_{out}}{I_{out}} \quad (3.1)$$

¹Note, it is assumed that the leakage inductance provided by the transformer can be sufficiently adjusted in order to obtain zero-voltage switching.

²This approach might result in a very small deviation from the global efficiency optimum, as these design parameters are optimised for full load and the complete load-range is not considered contrary to the outer-loop design parameters as explained below.

where Δi_{out} is the current ripple in the output inductor and I_{out} is the DC-output current, cf. **Fig. 3.2**. The actual optimisation loop is launched with the design parameters of step ②.

The first step in the loop (step ③) is the calculation of the operating point, i.e. the determination of all relevant current and voltage waveforms. The required output filter inductance L_{out} and the capacitance C_{out} are calculated for full load condition with the given specifications. The determination of current and voltage waveforms and the respective RMS and average values, and furthermore the harmonics are the basis for the following loss calculations. The operating point is thereby determined for four different load levels according to the Energy Star® requirements for computer servers [27], i.e. for 10 %, 20 %, 50 % and 100 % of the rated output power.

In the next step, the geometry of the inductor (step ④) and the transformer (step ⑤) is determined in two inner optimisation procedures, where the geometry design parameters for the transformer E-Cores and the inductor C-Cores with foil windings are changed systematically, until the minimal full-load losses are found while the flux density B is kept below the respective limit (transformer: $B_{\text{max}} = 300 \text{ mT}$, core material ferrite N87; inductor: $B_{\text{max}} = 1.2 \text{ T}$, core material Metglas® 2605SA1). Furthermore, a volume-limitation is necessary for the magnetic components, as the efficiency-optimisation otherwise would result in unbounded volumes as presented in section 3.4. In a first step of the inner optimisation process, the design parameter defining the height of the winding window is, similarly to power-density-optimised systems, pre-determined by calculating the optimal foil-thickness for the present loop design parameter as presented in [155]. Especially for small output current ripple factors k_I , where the current ripple Δi_{out} is small compared to the DC-current I_{out} , large values of the foil thickness would result and thus, the thickness of the inductor foil winding is limited to $500 \mu\text{m}$, which is practically feasible.

The losses in the inductor and transformer are analytically modelled as function of the remaining geometry parameters. The core-loss calculation is based on Sullivan's extended Steinmetz equation for non-sinusoidal current waveforms [176] and the determination of the winding losses is based on Dowell's one-dimensional approach [163] considering HF-losses due the skin and proximity effect. The turns number N_L of the inductor winding is thereby modelled as function of the geometry parameters (including the air gap) as presented in section 3.3 where

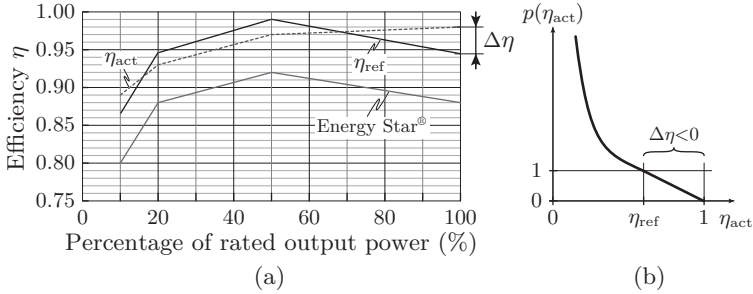


Figure 3.6: Determination of the optimisation criterion in the proposed efficiency optimisation procedure. (a) Efficiency as function of the rated output power. (b) Penalty function in dependency of the actual efficiency.

the models are described in detail. The geometry design parameters are systematically varied by the inner optimisation algorithm until the minimum device losses are found and the resulting optimised parameters are passed to the outer loop.

After the determination of the optimised magnetic component geometry and with determined operating point (steps ③..⑤) the losses in the magnetic components (including core and HF-winding losses), the losses in the inverter and rectifier MOSFETs (including conduction, switching and gate driver losses), dielectric losses in the output capacitor as well as the losses in the auxiliary power supply and control circuit are calculated in accordance with the Energy Star[®] requirements for computer servers [27] at 10 %, 20 %, 50 %, and 100 % load. The loss models applied for these steps ⑥..⑨ are presented in the next section.

After the part-load losses have been calculated in the steps ⑥..⑨, the quality index is calculated in step ⑩ at the end of an optimisation loop cycle. The optimisation goal of 99 % maximum efficiency and the information about the demanded part-load efficiencies according to the Energy Star[®] requirements are inherently considered in the optimisation criterion: an efficiency reference curve is based on the proposed Energy Star[®] efficiency points and shifted up such that the maximum efficiency features 99 % as illustrated in **Fig. 3.6(a)**. For the actual efficiency points $\eta_{act\nu}$ ($\nu \in \{10\%, 20\%, 50\%, 100\%\}$), calculated in the steps ⑥..⑨ with the present loop parameters, the deviation to the ref-

erence efficiency $\eta_{\text{ref } \nu}$ is determined:

$$\Delta\eta_{\nu} = \eta_{\text{ref } \nu} - \eta_{\text{act } \nu} \quad (3.2)$$

as illustrated in **Fig. 3.6(a)**. A penalty value is calculated with a penalty function $p(\Delta\eta_{\nu})$ for the resulting efficiency deviations $\Delta\eta_{\nu}$ as illustrated in **Fig. 3.6(b)** and analytically defined as

$$p(\Delta\eta_{\nu}) = \begin{cases} \frac{1}{1 - \eta_{\text{ref } \nu}} (1 - \eta_{\text{act } \nu}), & \text{for } \Delta\eta < 0 \\ \frac{1}{(1 - \eta_{\text{ref } \nu} + \eta_{\text{act } \nu})^{20}}, & \text{for } \Delta\eta \geq 0 \end{cases} \quad (3.3)$$

which is linearly decreasing for deviations $\Delta\eta_{\nu}$ smaller than zero, and monotonically increasing (polynomial function) for deviations $\Delta\eta_{\nu}$ larger than zero; the penalty results in 1, if the actual value and the reference value are equal ($\eta_{\text{ref } \nu} = \eta_{\text{act } \nu}$). The sum of the resulting penalty values $p(\Delta\eta_{\nu})$ determines the quality index oc which is minimised by the global optimisation algorithm,

$$oc = \sum_{\nu} p(\Delta\eta_{\nu}) w_{\nu}, \quad (3.4)$$

where w_{ν} is a possible weighting factor to emphasise the corresponding efficiency value³. The global optimisation algorithm changes in step ⑩ the design parameter values systematically, until the minimum quality index is found, i.e. the design is determined whose efficiency curve is most-similar to the reference efficiency characteristic. The outputs of the optimisation procedure are the design parameter values of the optimised converter which directly enable a prototype assembly. The optimisation results are introduced and discussed in section 3.4 after the summary of the applied analytical models in the next section.

3.3 Analytical Converter Models

The underlying analytical models applied in the optimisation procedure are derived in four subsections: first, the formulas for calculating the operating point are introduced in section 3.3.1. After that, the equations for determining the losses in the power semiconductors and

³All weights w_{ν} are set to $w_{\nu} \equiv 1$ for the later presented optimisation runs.

the associated driver circuits are derived in section 3.3.2. In the third subsection, the calculation of the magnetic components is presented (section 3.3.3) and finally the losses in the residual components, mainly in the capacitors are given in section 3.3.4.

3.3.1 Operating Point

The determination of the operating point and the associated current and voltage waveforms is coupled to the modelling of the transformer for a galvanically isolated DC-DC converter system. In section 2.1.2, a reluctance model is applied for a transformer with integrated series inductor for the LCC-resonant converter, whereas in section 2.2.2 an ideal transformer model is applied for the two-windings of the standard phase-shift converter with current doubler rectifier stage⁴. The operating point model applied for the phase-shift PWM converter with centre-tapped secondary winding transformer discussed in this chapter is based on a coupled inductor equivalent circuit which is illustrated in **Fig. 3.7**. The coupled-inductor model enables the consideration of non-ideal coupling between the windings and furthermore the influence of the mutual inductance, based on engineering experiences or as a (free) design parameter during the optimisation process⁵. The inductance L_2 (which is considered to be equal to L_3) and the transfer ratio k_{Tr} can be calculated with the definition of the inductance L_1 and the design parameter L_σ , and the coupling coefficient c_{12} as

$$\begin{aligned} c_{12} &= 1 - \frac{L_{\sigma,1}}{L_1} \\ L_2 &= L_1 \left(\frac{N_s}{N_p} \right)^2 \\ k_{Tr} &= \frac{1}{c_{12}} \sqrt{\frac{L_1}{L_2}} \end{aligned} \tag{3.5}$$

where N_p and N_s are the turns numbers of the primary and secondary windings and $L_{\sigma,1}$ is the primary-side related leakage inductance ($L_{\sigma,1}$ corresponds to L_σ).

⁴A reluctance model has been applied as well for the analytical calculations of the integrated transformer, combining transformer and current doubler inductors.

⁵The coupled-inductor model can alternatively be applied for an ideal-assumed transformer; moreover, this model can be transferred to other transformer models.

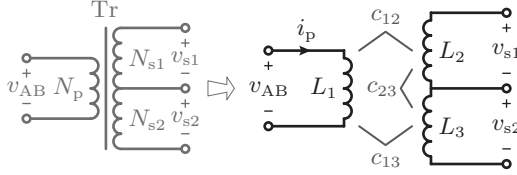


Figure 3.7: Coupled inductances model of the centre-tapped transformer.

The following derivation of the analytical operating point model is based to the presented characteristic current and voltage waveforms as illustrated in **Fig. 3.2** on page 171. The primary current waveform can be divided into three piecewise linear sections ($t \in \langle t_0, t_4 \rangle$) according to **Fig. 3.2** and **Fig. 3.3**), which describe the first half of the switching cycle and can be mirrored in order to obtain the second half cycle. The current slopes are defined by the inductances (L_1 , L_2 , L_3) and coupling coefficients (c_{12} , c_{13} , c_{23}) of the centre-tapped transformer, cf. **Fig. 3.7**, and the output inductance L_{out} .

$t_0 \leq t \leq t_2$ The input voltage V_{in} is applied to the primary side of the transformer and the current slope is limited by the leakage inductance. Assuming that the inductances L_2 and L_3 and the corresponding coupling coefficients in respect to L_1 (c_{12} and c_{13}) are equal, the formula for determining the current slope in this section can be simplified to

$$\frac{\Delta i_{p,1}}{t_2 - t_0} = V_{\text{in}} \frac{1 + c_{23}}{L_1 [1 + c_{23} - 2(c_{12})^2]} \quad (3.6)$$

where c_{23} is the coupling coefficient between the two secondary windings (cf. **Fig. 3.7**).

$t_2 \leq t \leq t_3$ During this interval of the powering state, the energy is transferred form the converter input to the output stage. With the applied input voltage V_{in} , the resulting output voltage V_{out} , and the calculated output inductance L_{out} , the current slope of this section can be determined as

$$\frac{\Delta i_{p,2}}{t_2 - t_3} = \frac{V_{\text{in}} (L_{\text{out}} + L_2) - V_{\text{out}} \sqrt{L_1} \sqrt{L_2} c_{12}}{L_1 [L_{\text{out}} + L_2 (1 - (c_{12})^2)]}. \quad (3.7)$$

The output inductance L_{out} is defined by the allowed inductor current ripple Δi_{out} (cf. (3.1)) considering full-load conditions,

$$L_{\text{out}} = \frac{\frac{V_{\text{in}}}{k_{\text{Tr}}} - V_{\text{out}}}{\Delta i_{\text{out}}} D_{\text{eff}} \frac{T_{\text{p}}}{2}, \quad (3.8)$$

where T_{p} is the switching cycle duration and D_{eff} is the effective duty cycle which can be defined (neglecting the converter losses) as

$$D_{\text{eff}} = k_{\text{Tr}} \frac{V_{\text{out}}}{V_{\text{in}}}. \quad (3.9)$$

$t_3 \leq t \leq t_4$ The converter operates in the free-wheeling phase, where the transformer is short-circuited by the high-side MOSFETs (or low-side MOSFETs, respectively). The primary side current slope is mainly determined by the rectifier stage and can be calculated with,

$$\frac{\Delta i_{\text{p},3}}{t_4 - t_3} = \frac{V_{\text{out}} \sqrt{L_2} c_{12}}{\sqrt{L_1} [L_{\text{out}} + L_2 (1 - (c_{12})^2)]}. \quad (3.10)$$

The current slopes $\Delta i_{\text{p},1}$, $\Delta i_{\text{p},2}$, and $\Delta i_{\text{p},3}$ for the corresponding time intervals are furthermore defined by the characteristic current inflexion points $I_{\text{p}1}..I_{\text{p}3}$ as illustrated in **Fig. 3.2** which can be expressed as

$$\begin{aligned} \frac{\Delta i_{\text{p},1}}{t_2 - t_0} &= \frac{I_{\text{p}1} + I_{\text{p}3}}{(\alpha + \beta) \frac{T_{\text{p}}}{2}} \\ \frac{\Delta i_{\text{p},2}}{t_3 - t_2} &= \frac{I_{\text{p}2} - I_{\text{p}1}}{(D - \alpha - \beta) \frac{T_{\text{p}}}{2}} \\ \frac{\Delta i_{\text{p},3}}{t_4 - t_3} &= \frac{I_{\text{p}2} - I_{\text{p}3}}{(1 - D) \frac{T_{\text{p}}}{2}}, \end{aligned} \quad (3.11)$$

where D is the (loss-less) duty cycle, which is defined as the sum of the effective duty cycle and the duty cycle loss due to the leakage inductance,

$$D = k_{\text{Tr}} \frac{V_{\text{out}}}{V_{\text{in}}} + \alpha + \beta. \quad (3.12)$$

By inserting (3.6), (3.7), (3.10), and (3.12) in (3.11) and solving for $I_{\text{p}1}$, $I_{\text{p}2}$ and $I_{\text{p}3}$, the resulting solutions are only depending on α and β which define the duty cycle loss (cf. **Fig. 3.2**). To eliminate α and β ,

two additional equations have to be formulated. The first expression is derived from the periodicity of the primary current,

$$0 = \frac{\Delta i_{p,1}}{t_2 - t_0} \beta \frac{T_p}{2} + \frac{\Delta i_{p,2}}{t_3 - t_2} (D - \alpha - \beta) \frac{T_p}{2} - \dots \quad (3.13)$$

$$\dots - \frac{\Delta i_{p,3}}{t_4 - t_3} (1 - D) \frac{T_p}{2} - \frac{\Delta i_{p,1}}{t_2 - t_0} \alpha \frac{T_p}{2}.$$

For the second expression, the equation of the average output power is derived,

$$P_{\text{out}} = V_{\text{out}} \frac{2}{T_p} k_{\text{Tr}} \left[\int_{\alpha T_p/2}^{(\alpha+\beta) T_p/2} \frac{\Delta i_{p,1}}{t_2 - t_0} \left(t - \alpha \frac{T_p}{2} \right) dt + \dots \right. \\ \dots + \int_{(\alpha+\beta) T_p/2}^{D T_p/2} I_{p1} + \frac{\Delta i_{p,2}}{t_3 - t_2} \left(t - (\alpha + \beta) \frac{T_p}{2} \right) dt + \dots \quad (3.14)$$

$$\dots + \int_{D T_p/2}^{T_p/2} I_{p2} - \frac{\Delta i_{p,3}}{t_4 - t_3} \left(t - D \frac{T_p}{2} \right) dt + \dots$$

$$\left. \dots + \int_{T_p/2}^{(1+\alpha) T_p/2} I_{p3} - \frac{\Delta i_{p,1}}{t_2 - t_0} \left(t - \frac{T_p}{2} \right) dt \right],$$

with

$$I_{p1} = \frac{\Delta i_{p,1}}{t_2 - t_0} \alpha \frac{T_p}{2} \quad (3.15)$$

$$I_{p2} = I_{p1} + \frac{\Delta i_{p,2}}{t_3 - t_2} (D - \alpha - \beta) \frac{T_p}{2}$$

$$I_{p3} = I_{p2} - \frac{\Delta i_{p,3}}{t_4 - t_3} (1 - D) \frac{T_p}{2}.$$

Equations (3.13) and (3.14) can be solved for α and β by inserting the characteristic current points from the solutions of (3.11). The closed analytical solutions for I_{p1} , I_{p2} , and I_{p3} , as well as for α and β are long expressions which are omitted here for the sake of brevity. The definition of the current and voltage waveforms allows the calculation of the RMS-values, the derivation of the RMS-values, and the determination of the harmonics of the transformer, inductor, capacitor, and semiconductor currents for the following loss calculations.

3.3.2 Semiconductor Losses

Losses in the power semiconductors occur mainly due to the non-zero on-resistance $R_{DS,on}$ (conduction losses), the parasitic output capacitance C_{oss} as part of a resonant circuit, which eventually results in switching losses, and furthermore the gate-charge Q_G ⁶, which causes losses in the gate-driver circuit during the switching transitions. The conduction and gate driver losses can be similarly determined as shown previously in the loss calculation of the high-power-density systems. Newly implemented in the optimisation process of the proposed high-efficiency converter is the possibility of paralleling switching devices which has a major influence of the system performance⁷. The conduction losses in the MOSFETs can consequently be calculated with

$$P_{cond} = \frac{R_{DS,on}}{n_{sw}} I_{sw}^2 \quad (3.16)$$

where $R_{DS,on}$ is the on-resistance of a single switch, I_{sw} is the RMS-current carried by the (paralleled) MOSFETs, and n_{sw} is the number of paralleled devices which represents a single switch, e.g. S_{11} or S_{R1} . The losses in the gate circuit of a single switch can furthermore be determined with

$$P_{drive} = n_{sw} (V_{GS,on} Q_G f_{sw} + P_{driver}), \quad (3.17)$$

considering the stand-by losses of the driver-IC P_{driver} as well. $V_{GS,on}$ is the positive applied gate-source voltage during the on-state of the MOSFET. The turn-off voltage $V_{GS,off}$ is considered to be zero. If a negative off-state voltage $V_{GS,off}$ is applied to the gate, equations (2.33) and (2.34) on page 88 can alternatively be applied.

The conduction and gate-driver losses can similarly be determined for the inverter and synchronous-rectifier MOSFETs with (3.16) and (3.17). The switching mechanism, however, is different in the inverter and the rectifier stage. The switching losses are therefore discussed separately in the following subsections.

⁶The applied Q_G -value refers to hard-switching, cf. footnote 17 on page 88.

⁷Discrete devices available from the manufacturer have been considered and the corresponding specifications compiled in a data base. An approach less orientated to practice is to base the calculation on a freely-variable size of the silicon-chips, from which specific values such as on-resistance and output capacitance can be determined.

Switching Losses in the Inverter Stage

The inverter stage is generally supposed to operate under ZVS-conditions by inserting a small interlock delay between the switching states of the MOSFETs in a bridge leg. During this interlock interval, the input voltage across the turned-off MOSFET is transferred to the other bridge-leg MOSFET by removing the charge in the parasitic output-capacitance of the switch that will be turned on at the end of the interval. This resonant charging mechanism is defined by the contributing resonant tank components, mainly the leakage inductance L_σ in the commutation path⁸ and the MOSFET's output capacitance C_{oss} , as well as the interlock delay time t_{ild} . If the voltage transfer in the bridge leg is incomplete, i.e. a residual voltage is remaining across the MOSFET which is turned-on, switching losses occur in the device. Potentially for part-load conditions, the energy stored in the leakage inductance could be insufficient for the complete discharge of C_{oss} during the defined interlock-delay time. A more detailed discussion about the determination of the design parameters t_{ild} , the MOSFET selection, and the number of paralleled switches, which define the total output capacitance C_{oss} , as well as the selection of the leakage inductance is presented in section 3.4. In the following paragraphs, the analytical switching-loss model is derived.

The parasitic output capacitance of a MOSFET is non-linearly dependent on the applied voltage. If the drain-source voltage is small, the capacitance is high, whereas the capacitance value is non-linearly decreasing if the drain-source voltage is increasing. The voltage transition between the two output capacitances is consequently also non-linear, which has been explained for instance in [190] for a bridge-less AC-DC rectifier with power factor correction. In order to calculate the possibly residual voltage across the MOSFET to be turned on, an energy-equivalent output capacitance $C_{oss,eq}$ is determined which contains the same amount energy for the applied converter input voltage V_{in} .

The energy E_C stored in a voltage-dependent capacitor $C_{oss}(v_{DS})$,

⁸In addition to the transformer leakage inductance, the inductance resulting from the connections and terminals also contribute to the resulting commutation-path inductance. However, the transformer leakage inductance has the greater influence and is therefore further considered.

which is charged from zero volts to the voltage V_{in} is defined by

$$E_C = \int_0^{V_{\text{in}}} v_{\text{DS}} C_{\text{oss}}(v_{\text{DS}}) dv_{\text{DS}}. \quad (3.18)$$

The energy E_{Ceq} stored in a in the energy-equivalent capacitor $C_{\text{oss,eq}}$ is dependent on the applied voltage (V_{in}) and can be determined with

$$E_{\text{Ceq}} = C_{\text{oss,eq}} \int_0^{V_{\text{in}}} v_{\text{DS}} dv_{\text{DS}} = \frac{1}{2} C_{\text{oss,eq}} V_{\text{in}}^2. \quad (3.19)$$

By equating (3.18) with (3.19) and solving for $C_{\text{oss,eq}}$ the expression for the energy-equivalent capacitance can be found

$$C_{\text{oss,eq}} = \frac{2}{V_{\text{in}}^2} \int_0^{V_{\text{in}}} v_{\text{DS}} C_{\text{oss}}(v_{\text{DS}}) dv_{\text{DS}}. \quad (3.20)$$

With (3.20) the energy-equivalent capacitance can be extracted from the voltage-dependent capacitance $C_{\text{oss}}(v_{\text{DS}})$ as shown in **Fig. 3.8(a)**, which is commonly specified in the corresponding device data sheets⁹.

During the switching transition the parasitic output capacitances of the MOSFETs in a bridge leg are connected in parallel, assuming that the converter input capacitance is much larger than the paralleled output capacitances, i.e. the constant voltage source V_{in} is short-circuited for the AC-considerations. The paralleled capacitors are furthermore connected in parallel with the series connection of the leakage inductance and the on-resistance of the conducting MOSFET of the opposite bridge leg. The differential equations describing the current and voltage transition are given by

$$\begin{aligned} \frac{d}{dt} i_{\text{p}}(t) &= \frac{v_{\text{DS}}(t) - i_{\text{p}}(t) R_{\text{DS,on}}}{L_{\sigma}} \\ \frac{d}{dt} v_{\text{DS}}(t) &= -\frac{1}{2} \frac{i_{\text{p}}(t)}{C_{\text{oss,eq}}} \end{aligned} \quad (3.21)$$

⁹Note, besides the energy-equivalent output capacitance also a time-related and charge-equivalent output capacitance can be defined. These values are partly given for specific voltages in the manufacturer's data sheets. The difference between the energy- and time-equivalent capacitance and the influence to the circuit operation is for instance discussed in [191].

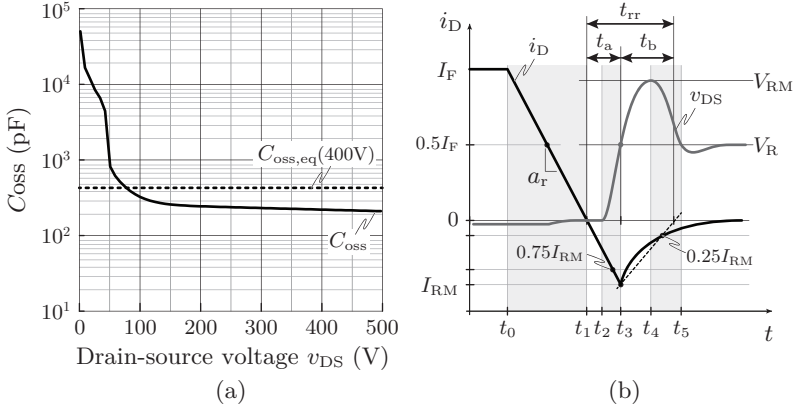


Figure 3.8: (a) Voltage-dependent and energy-equivalent output capacitance for a power MOSFET IPW60R045CP from Infineon. (b) Basic turn-off transient of a (body) diode.

with the boundary conditions

$$i_p(t_{off}) = I_{p,off} \quad \text{and} \quad v_{DS}(t_{off}) = V_{in}, \quad (3.22)$$

where $I_{p,off}$ is the current in the conducting MOSFET (and L_σ) at $t = t_{off}$ where the MOSFET is turned off. The set of differential equations (3.21) can be solved for the drain-source voltage $v_{DS}(t)$ applying the boundary conditions (3.22)¹⁰. If the first zero-crossing of $v_{DS}(t)$ would occur after the interlock-delay time, at t_{ild} , a residual voltage $V_{DS,on} = v_{DS,on}(t_{ild})$ is still present across the MOSFET which is switched on at the time t_{ild} .

The energy stored in the capacitor can be determined with the residual voltage $V_{DS,on}$ based on the data provided in the manufacturer's data sheet, where the voltage-dependent energy is commonly given or could be determined with (3.18) from the given voltage-dependent output-capacitance characteristic. In the optimisation process, the characteristic energy curve of the applied MOSFET is described by piecewise polynomial functions dependent on the residual voltage $E_{oss}(v_{DS})$ which are extracted from the data sheets and stored in a MOSFET's data base. The switching losses $P_{sw,p}$ in one inverter switch (consisting

¹⁰The solution is a long algebraic expression which is omitted for sake of brevity.

of $n_{\text{sw,p}}$ paralleled MOSFETs) can be determined with

$$P_{\text{sw,p}} = n_{\text{sw,p}} E_{\text{oss}}(V_{\text{DS,on}}) f_{\text{sw}}. \quad (3.23)$$

Remark In the switching-loss model described above, only the losses are considered, which are caused by an incomplete charging process in the bridge leg. However, potentially additional losses during the switching process occur in the device irrespective of whether zero voltage switching is achieved or not. A part of this loss could be explained by the increased resistance of the contracted channel through which the charge carriers pass in order to charge the parasitic capacitance. A modelling of these losses is even more complicated as the loss-source cannot be entirely explained. Practically, these losses could be measured for a soft-switching process and described by an empirical equation, as for instance applied in the modelling of the high-power-density systems in the preceding chapter.

Switching Losses in the Synchronous Rectifier

The MOSFETs applied in the synchronous rectifier can be turned on during the free-wheeling state, where the transformer voltage is clamped to approximately zero, i.e. the MOSFETs are turned on with ZVS-conditions. In contrast the current is in the anti-parallel body diode of the turned-off MOSFET hard-commutated, which results in reverse-recovery losses. The analytical model of this commutation is derived in the following paragraphs.

The basic turn-off behaviour of a (body) diode is shown in **Fig. 3.8(b)**. The start of the current transition in the Synchronous-Rectifier (SR) MOSFET at the point t_0 is initiated by the inverter side state-change from the free-wheeling phase to the powering phase. The SR MOSFET is commonly turned off before t_0 and the current is carried by the body diode rather than the intrinsic MOSFET channel. However, as explained below and validated with measurements in section 3.5, the turn-off during the current transition can improve the efficiency. The current slope a_{r} , cf. **Fig. 3.8(b)**, is determined by the inductance L_{com} in the commutation path, mainly the sum of the winding leakage inductances, as well as the inductance in the terminals and connections.

At point t_1 , the drain current i_{D} through the MOSFET SR_1 crosses the zero line; the commutation phase ends and the storage phase starts. The current continues to flow with negative direction removing the re-

covery charge in the body diode and charging the parasitic output capacitance. The recovery charge is mainly determined by the diffusion charge $q_D(t)$ which is built up as soon as the current commutates to the body diodes and is partly removed during the time interval $t \in \langle t_0, t_1 \rangle$. The storage phase ends at t_2 when the total excess carrier concentration at the junction reduces to zero [192].

At point t_2 the voltage across the parasitic output capacitance starts to increase to the level of the applied steady-state voltage ($V_R = 2 V_{in}/k_{Tr}$) at point t_3 , which allows the charge to recombine. At point t_3 , the MOSFET current i_{s1} reaches the reverse recovery peak I_{RM} .

After the voltage-build-up phase, the reverse current decreases with the rate of the diffusion and recombination process in the base region of the device [192], and the voltage increases to the maximum, where this inductive phase, cf. [192], ends at point t_4 .

During the recovery phase $t \in \langle t_4, t_5 \rangle$ the blocking voltage decreases from the peak value V_{RM} to the steady-state value. Due to the leakage inductance and the parasitic capacitances, a voltage and current ringing can be observed which is not shown in **Fig. 3.8(b)**, as in the following loss-model the total losses occurring during the commutation process are considered.

The characteristic turn-off waveforms in **Fig. 3.8(b)** are idealised and can be separated into two piecewise linear sections: during the interval $t \in \langle t_0, t_3 \rangle$ the current is linearly decreasing from the forward conducting current I_{FM} at the turn-off to the reverse-recovery current peak I_{RM} ; during the interval $t \in \langle t_3, t_5 \rangle$ the current is exponentially increasing from I_{RM} to zero:

$$i_{s1}(t) = \begin{cases} I_{FM} - a_r (t - t_0) & \text{for } t \in \langle t_0, t_3 \rangle \\ -I_{RM} \exp\left(-\frac{t - t_3}{\tau_{rr}}\right) & \text{for } t \in \langle t_3, t_5 \rangle \end{cases} \quad (3.24)$$

where a_r is the current slope, which is defined according to the JEDEC-standard [193] between 50 % of the switched-off current I_{FM} and 75 % of reverse-recovery peak I_{RM} . The time constant τ_{rr} can be defined by a straight line starting at I_{RM} and the point of intersection of the device current and the current level $0.25 I_{RM}$, i.e. $i_{s1}(t) = 0.25 I_{RM}$ according to [193] and **Fig. 3.8**.

In [194] a lumped-charge modelling technique is used to describe a physics-based model of a power diode, which directly links the external

electrical characteristics with the internal carrier distribution and their transport characteristics. An equation for the reverse recovery peak I_{RM} is derived, which is only dependent on the effective carrier lifetime τ_3 ,

$$I_{\text{RM}} = a_{\text{r}} (\tau_3 - \tau_{\text{rr}}) \left[1 - \exp \left(-\frac{t_{\text{a}}}{\tau_3} \right) \right]. \quad (3.25)$$

This transcendental equation can be numerically solved for τ_3 based on data sheet values or measurements¹¹. With the knowledge of τ_3 , the diffusion charge $q_{\text{D}}(t)$ can be determined (derivation below) which is necessary for the loss model as explained in the following paragraphs.

At the point t_3 , where the current reaches the reverse-recovery peak I_{RM} , the voltage in the parasitic output capacitance C_{oss} reaches the steady-state blocking voltage V_{R} and the energy stored in commutation inductance L_{com} and the (equivalent) output capacitance $C_{\text{oss,eq}}$ are given by

$$\begin{aligned} E_{\text{ind}} &= \frac{1}{2} L_{\text{com}} I_{\text{RM}}^2 \\ E_{\text{cap}} &= \frac{1}{2} C_{\text{oss,eq}} V_{\text{R}}^2. \end{aligned} \quad (3.26)$$

The energy stored in the inductor E_{ind} is in succession transferred to the parasitic output capacitor which eventually results in an overcharging and the voltage peak V_{RM} (which can be approximated based on this consideration and (3.26)). As the impedance of the converter output filter is much higher than the impedance of the commutation circuit, this energy is not transferred to the output, rather successively removed in the resistive components of the current-commutation path¹². This energy E_{ind} consequently determines the switching losses due to the recovery effect in the here applied loss model.

According to **Fig. 3.8(b)**, the involved switching charge Q_{sw} can be found in the enclosed area of abscissa and the reverse current down to I_{RM} :

$$Q_{\text{sw}} = \frac{I_{\text{RM}}}{2} t_{\text{a}} = \frac{I_{\text{RM}}^2}{2 a_{\text{r}}} \quad (3.27)$$

¹¹If only discrete values are given in the data sheets rather than the measured curve, the determination of τ_3 based on (3.25) might not be sufficiently accurate in case there is no evidence that the values are given in accordance to the JEDEC-standard [193]. Measurements of the MOSFET characteristic are preferred in either case.

¹²This further results in a distinct voltage ringing damped by the resistive components which is not shown for the basic waveform in **Fig. 3.8(b)**.

which can be solved for I_{RM}^2 and substituted in (3.26) which results in

$$E_{\text{sw}} = L_{\text{com}} a_{\text{r}} Q_{\text{sw}}. \quad (3.28)$$

This can be further simplified to

$$E_{\text{sw}} = V_{\text{R}} Q_{\text{sw}}. \quad (3.29)$$

The energy E_{sw} which eventually results in switching losses is, cf. (3.29), dependent from the blocking voltage applied to the device ($V_{\text{R}} = 2 V_{\text{in}}/k_{\text{Tr}}$) and Q_{sw} which is basically the sum of the diffusion charge $Q_{\text{D}} = q_{\text{D}}(t_1)$ and the voltage-equivalent charge in the parasitic output capacitance, $Q_{\text{oss,eq}}$, i.e.

$$Q_{\text{sw}} = Q_{\text{D}} + Q_{\text{oss,eq}} \quad (3.30)$$

where $Q_{\text{oss,eq}}$ can similarly as the energy-equivalent output capacitance $C_{\text{oss,eq}}$ be determined based on the voltage-dependent output capacitance provided in data sheets,

$$Q_{\text{oss,eq}} = \int_0^{V_{\text{R}}} C_{\text{oss}}(v_{\text{DS}}) dv_{\text{DS}}. \quad (3.31)$$

The residual component for determining the losses is consequently the modulation of the diffusion charge $q_{\text{D}}(t)$. The steady-state diffusion charge of a power diode is according to [195] defined as

$$Q_{\text{D}} = I_{\text{F}} \tau_3 \quad (3.32)$$

which would be present at the time t_0 if the MOSFET would have been turned off at the beginning of the free-wheeling phase and the current would have been carried by the body diode. As the MOSFET is assumed to be turned off at the time t_0 or even later, the diffusion charge starts to be established at the point where the current commutates to the body diode. Assuming that the current commutates at t_0 , the current in the body-diode is defined as

$$i_{\text{D}}(t) = \begin{cases} I_{\text{F}} - a_{\text{r}} t & \text{for } t \in \langle t_0, t_1 \rangle \\ 0 & \text{otherwise} \end{cases}. \quad (3.33)$$

The dynamic behaviour of the diffusions charge can be approximated with a low-pass filter [194] and therefore be determined in the

Laplace domain by multiplying the filter function with the corresponding Laplace-transformed diode current $\mathcal{L}\{i_D(t)\}$. The inverse Laplace transformation describes the diffusion charge in the time domain:

$$\begin{aligned} q_D(t) &= \mathcal{L}^{-1} \left\{ \frac{\tau_3}{1 + s \tau_3} \mathcal{L}\{i_D(t)\} \right\} \\ &= \mathcal{L}^{-1} \left\{ \frac{\tau_3}{1 + s \tau_3} \left(\frac{I_F}{s} - \frac{a_r}{s^2} \right) \right\} \end{aligned} \quad (3.34)$$

where $s = j\omega$ is the complex angular frequency. The inverse Laplace transformation results in the expression for $q_D(t)$

$$q_D(t) = \tau_3 \left(I_F - a_r (t - \tau_3) - (I_F + a_r \tau_3) \exp \left(-\frac{t}{\tau_3} \right) \right). \quad (3.35)$$

The current slope a_r is approximated with the transformer's leakage inductances in the current-commutation path and the effective carrier lifetime τ_3 has been determined by measurements. According to (3.35), the diffusion charge $q_D(t)$ is low if the turned-off current I_F is low. The losses are consequently reduced if the MOSFET is turned off shortly before the zero-crossing of the current, considering the delay-time of the gate-circuit in order to prevent to short-circuit the transformer. In the optimisation process, the turned-off current is assumed to be one third of the secondary side related current I_{p3} in order to leave a small safety margin.

The turned-off current I_F in (3.35) is substituted by

$$I_F = \frac{1}{3} \frac{1}{n_{sw,s}} I_{p,3} k_{Tr}$$

and the diffusion charge Q_D is evaluated for $t = I_F^{1/a_r}$ to determine the total losses in the SR-switch consisting of $n_{sw,s}$ paralleled MOSFETs. By substituting Q_D in (3.30) and the resulting switching charge Q_{sw} in (3.29) the losses are determined with

$$P_{sw,SR} = E_{sw} n_{sw,s} f_{sw}. \quad (3.36)$$

Remark The diffusion charge (or recovery charge Q_{rr}^*) is sometimes provided in the data sheet; however, Mösslacher and Görgens point out in [196] that Q_{rr}^* is dependent on the measurement method and the definition¹³, which might exclude the adequate utilisation of

¹³The JEDEC-standard [193] and [197] are not necessarily applied for the provided data.

the provided values. Nevertheless, the effective carrier lifetime of fast-recovery body diodes is rather small which results in a small diffusion charge. The switching charge is in this case almost exclusively influenced by the charge of the parasitic output capacitance and the diffusion charge can be neglected. This is also true for very fast or very slow current commutation processes as less diffusion charge is established in the first case and the charge carriers are partly recombining in the second case.

3.3.3 Losses in the Magnetic Components

In the inner optimisation procedures, the geometry design parameter values of the magnetic components, cf. **Fig. 3.9**, are varied systematically in order to obtain the minimum losses, considering the flux density limitation B_{\max} of the applied core material. The component volumes of the transformer and inductor (bounding box) are furthermore limited as the losses are continuously decreasing for increasing volumes as discussed in section 3.4.

The first step in the inner optimisation is the reduction of the design geometry parameter d (winding window-width cf. **Fig. 3.9**) by determining the optimal foil thickness d_{opt} based on Hurley's analytical design approach [155], summarised in section C.5,

$$d_{\text{opt}} = \frac{1}{\sqrt[4]{\Psi}} \sqrt{\frac{2 \pi f_{\text{sw}} I_{\text{rms}}}{I'_{\text{rms}}}} \delta_0, \quad (3.37)$$

where I_{rms} have to be substituted by the primary and secondary side RMS-current values and their corresponding derivatives I'_{rms} , respectively, δ_0 is the skin-depth at the fundamental (switching) frequency f_{sw} (cf. (C.16) on page 276) and Ψ is defined as [155]

$$\Psi = \frac{5 N^2 - 1}{15}. \quad (3.38)$$

As an example¹⁴, the RMS-current and the corresponding time deriv-

¹⁴The other RMS-current values and the corresponding derivatives are as well derived from the operating point, however, not presented here as the equations are comparatively long.

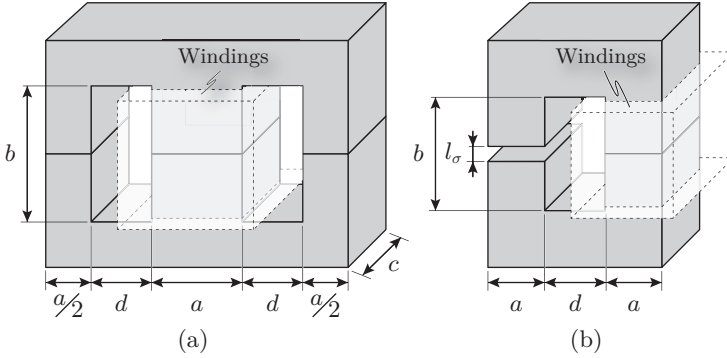


Figure 3.9: Geometry model of the centre-tapped secondary winding transformer (a) and the output filter inductor (b).

ative of the inductor winding current are determined with

$$I_{Lout} = \frac{1}{6} \sqrt{36 I_{out} + 3 k_1^2 I_{out}^2}$$

$$I'_{Lout} = \frac{\sqrt{4} k_1 I_{out}}{T_p} \sqrt{\frac{1}{|(D-1-\alpha-\beta)(D-\alpha-\beta)|}}. \quad (3.39)$$

The peak-to-peak flux density ΔB in the transformer is approximated with

$$\Delta B = \frac{V_{in} D T_p / 2}{N_p A_c}, \quad (3.40)$$

where A_c is the core cross-sectional area ($A_c = a c$, cf. **Fig. 3.9(a)**). The maximum flux density B_{max} is half of the peak-to-peak flux density. The core losses can be determined with Sullivan's extended Steinmetz formula [176]

$$P_{c,Tr} = \frac{k_{i,Tr} \Delta B^{(\alpha_{Tr}-\beta_{Tr})}}{T_p} 2 \left(\frac{V_{in}}{N_p A_c} D \frac{T_p}{2} \right) V_c, \quad (3.41)$$

where V_c is the volume of the transformer core (which can simply be derived from **Fig. 3.9(a)**); α_{Tr} , β_{Tr} and k_{Tr} are the Steinmetz-parameter and $k_{i,Tr}$ is defined in [176]

$$k_{i,Tr} = \frac{k_{Tr}}{2^{(\beta_{Tr}+1)} \pi^{(\alpha_{Tr}-1)} \left(0.2761 \frac{1.7061}{\alpha_{Tr}+1.354} \right)}. \quad (3.42)$$

The winding-loss model consider the skin and proximity effect based on the Dowell's one-dimensional approach [163], as well as the explanations basically provided by Ferreira and Hurley in [164] and [155, 198]. The derivation of the loss-equation is furthermore summarised in section C. The losses due to the skin effect in the primary transformer winding are determined with the magnitudes $\hat{I}_{p,\nu}$ of the ν^{th} current-harmonics,

$$P_{\text{skin},p} = R_{\text{DC},p} \hat{I}_{p,0}^2 + \sum_{\nu=1}^{n_{\nu,p}} R_{\text{DC},p} \frac{\Delta_p}{4} \frac{\sinh \Delta_p + \sin \Delta_p}{\cosh \Delta_p - \cos \Delta_p} \hat{I}_{p,\nu}^2, \quad (3.43)$$

where $n_{\nu,p}$ is the number of calculated current-harmonics. $R_{\text{DC},p}$ is the DC-resistance of the primary winding which is determined by the geometry parameters (b_f is the foil width and $l_{w,p}$ the length of the primary side winding) and the electrical resistivity of copper ρ_{Cu} ,

$$R_{\text{DC},p} = \frac{l_{w,p} \rho_{\text{Cu}}}{d_{\text{opt},p} b_f}. \quad (3.44)$$

The ratio Δ_p of the determined optimal foil thickness $d_{\text{opt},p}$ and the frequency-dependent skin-depth of the ν^{th} harmonic is furthermore defined as

$$\Delta_p = \frac{d_{\text{opt},p}}{\sqrt{\frac{\rho_{\text{Cu}}}{\pi \nu f_{\text{sw}} \mu_0}}}, \quad (3.45)$$

where μ_0 is the permeability of free space.

The losses due to the proximity effect in the primary winding are defined as:

$$\begin{aligned} P_{\text{prox},p} = & \sum_{\nu=1}^{n_{\nu,p}} \sum_{m=1}^{N_p} \frac{b_f \rho_{\text{Cu}}}{\sqrt{\frac{\rho_{\text{Cu}}}{\pi \nu f_{\text{sw}} \mu_0}}} \frac{\sinh \Delta_p + \sin \Delta_p}{\cosh \Delta_p - \cos \Delta_p} \cdot \dots \\ & \dots \cdot \left(\frac{1}{2b} \hat{I}_{p,\nu} (2m-1) \right)^2 \frac{l_{w,p}}{N_p}. \end{aligned} \quad (3.46)$$

The winding losses in the secondary windings are basically calculated with the same approach as for the primary windings. Due to the centre-tapped winding, however, two cases have to be considered for calculating the losses due to the proximity effect as illustrated in **Fig. 3.10**. If the current is carried by the inner secondary winding

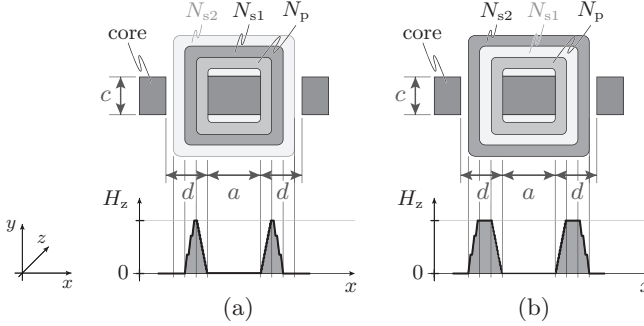


Figure 3.10: Winding arrangement of the centre-tapped transformer. (a) Corresponding H-field if the inner secondary winding is conducting, (b) Corresponding H-field if the outer secondary winding is conducting.

N_{s1} , which is arranged between the core-facing primary winding N_p and the outer winding N_{s2} , only N_{s1} is exposed to the established magnetic field and losses are consequently only generated in N_{s1} , cf. **Fig. 3.10(a)**. If the outer secondary winding N_{s2} carries the rectifier current, cf. **Fig. 3.10(b)**, additional eddy-current losses are generated in the inner secondary winding N_{s1} , which is exposed to the constant H-field of the adjacent windings. The additional loss term is given by

$$P_{\text{prox},s1(b)} = \sum_{\nu=1}^{n_{\nu,s}} \frac{b_f \rho_{Cu}}{\sqrt{\frac{\rho_{Cu}}{\pi \nu f_{sw} \mu_0}}} \frac{\sinh \Delta_s + \sin \Delta_s}{\cosh \Delta_s - \cos \Delta_s} \left(\frac{N_{s1} \hat{I}_{s2,\nu}}{b} \right)^2 \frac{l_{w,s1}}{N_s} \quad (3.47)$$

where s is the index for the secondary winding and the variable definition is in analogy to the primary winding. The resulting losses $P_{w,s}$ in the secondary windings is determined with

$$P_{w,s} = P_{\text{skin},s1} + P_{\text{skin},s2} + P_{\text{prox},s1} + P_{\text{prox},s2} + P_{\text{prox},s1(b)} \quad (3.48)$$

where $P_{\text{skin},s1}$, $P_{\text{skin},s2}$, $P_{\text{prox},s1}$ and $P_{\text{prox},s2}$ can be calculated by substituting the corresponding parameters in (3.43) and (3.46), respectively.

The losses due to the skin and proximity effect in the output inductor are modelled with the same approach as for the transformer primary winding in analogy to (3.43) and (3.46). The HF-component, however, have only a minor influence on the inductor winding losses, as

the output current exhibits only a small AC-component Δi_{out} compared to the DC-component I_{out} . The optimal foil thickness, cf. (3.37), might consequently result in high values and is therefore limited to 500 μm which is practically realisable.

The peak-to-peak flux density ΔB_{Lout} can be calculated with

$$\Delta B_{\text{Lout}} = \frac{L_{\text{out}} k_{\text{I}} I_{\text{out}}}{N_{\text{L}} A_{\text{c,L}}}, \quad (3.49)$$

where N_{L} is the turns number and $A_{\text{c,L}}$ is the cross-sectional area of the inductor core. The maximum flux density is defined as

$$B_{\text{max,L}} = \frac{L_{\text{out}} (I_{\text{out}} + \frac{1}{2} k_{\text{I}} I_{\text{out}})}{N_{\text{L}} A_{\text{c,L}}}. \quad (3.50)$$

The losses in the inductor core are determined similar to the transformer core losses based on the Sullivan's extended Steinmetz formula [176]:

$$\begin{aligned} P_{\text{c,L}} = & k_{\text{i,L}} \frac{\Delta B_{\text{Lout}}^{\beta_{\text{L}} - \alpha_{\text{L}}}}{T_{\text{p}}} 2 \left[\left(\frac{L_{\text{out}} \Delta I_{\text{out}}}{D T_{\text{p}/2} N_{\text{L}} A_{\text{c,L}}} \right)^{\alpha_{\text{L}}} D \frac{T_{\text{p}}}{2} + \dots \right. \\ & \left. \dots + \left(\frac{L_{\text{out}} \Delta I_{\text{out}}}{(1 - D) T_{\text{p}/2} N_{\text{L}} A_{\text{c,L}}} \right)^{\alpha_{\text{L}}} (1 - D) \frac{T_{\text{p}}}{2} \right] V_{\text{c,L}} \end{aligned} \quad (3.51)$$

where $V_{\text{c,L}}$ is the core volume which can be determined with the geometry model presented in **Fig. 3.9(b)** and $k_{\text{i,L}}$ is defined with (3.42).

3.3.4 Dielectric Losses in the Output Capacitors

With the applied output capacitor¹⁵ C_{out} and the given loss factor $\tan \delta$ the losses are determined with

$$P_{\text{C}} = \frac{I_{\text{C,rms}}^2 \tan \delta}{2 \pi f_{\text{sw}} C_{\text{out}}}, \quad (3.52)$$

where $I_{\text{C,rms}}$ is the RMS-value of the capacitor ripple current. It is assumed, that the output current I_{out} has only a DC-component and the entire ripple current Δi_{out} is carried by the output capacitor. The

¹⁵The required capacitance value is obtained by paralleling the selected 2.2 μF - 100 V capacitors (X7R - 1210 housing) from muRata.

capacitance can be calculated with the allowed voltage ripple V_{pp} by solving (3.53) with respect to C_{out} :

$$V_{pp} = \frac{1}{C_{out}} \left[\int_0^{D T_{p/4}} \frac{I_{out} k_I}{D T_{p/2}} t dt + \int_0^{(1-D) T_{p/4}} \frac{I_{out} k_I}{(1-D) T_{p/2}} t dt \right]. \quad (3.53)$$

The losses in the auxiliary supply and control unit are considered to be constant over the entire load range and set to 2 W.

3.4 Optimisation Results

Based on the design procedure introduced in **Fig. 3.2** and the applied analytical converter models, an efficiency-optimised DC-DC converter has been calculated and is presented in this section. The resulting system efficiency is mainly determined by the power semiconductors and the magnetic components. The influence of the semiconductor (pre-) selection and specification of the inductor and transformer volume are discussed in the first two subsections (section 3.4.1 and section 3.4.2) and the optimisation results are presented in section 3.4.3.

3.4.1 Performance-Influence of Semiconductors

As the first step in the optimisation procedure the fixed design parameters have to be defined, amongst others, the electric (and thermal) specifications of the applied semiconductors. Several power MOSFETs (in total nineteen) which are specified for the required voltage ranges in the inverter and synchronous rectifier have been investigated and the provided data was stored in a data base, mainly the voltage-dependent output capacitance $C_{oss}(v_{DS})$ and the stored-energy curves $E_{oss}(v_{DS})$, the energy-equivalent output capacitance $C_{oss,eq}$, the on-resistance $R_{DS,on}$ (or on-conductance $G_{DS,on}$, respectively), and the gate charge Q_G . The selection of the MOSFETs is an additional (free) design parameter during the optimisation process which could be varied by the optimisation algorithm, which would however increase the computation time; therefore, the MOSFETs have been pre-selected as discussed in the following.

A Figure Of Merit (FOM) is commonly defined for the identification of suitable MOSFETs, based on the on-conductance $G_{DS,on}$, which

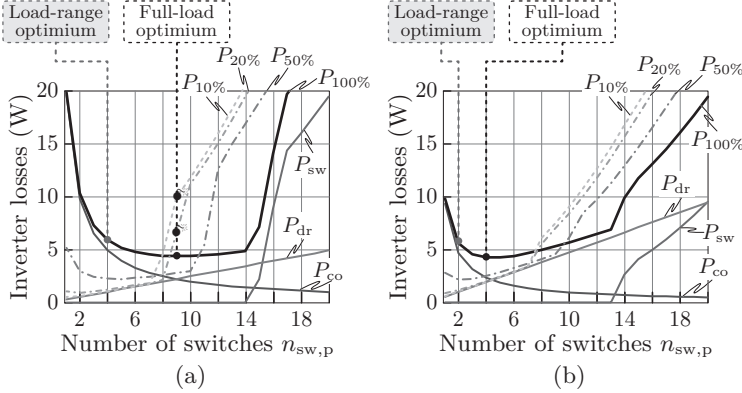


Figure 3.11: Semiconductor losses in the inverter stage in dependency of the number of paralleled switches. (a) CoolMOS™ IPW60R045CP from Infineon. (b) MDmesh™ STY112N65M5 from STMicroelectronics. *Underlying parameters:* $L_{1,\sigma} = 2\mu H$, $k_{Iout} = 0.03$, $N_p = 32$, $N_s = 5$, $f_{sw} = 25\text{ kHz}$.

should be high for small conduction losses, and the energy-equivalent output capacitance of the device $C_{oss,eq}$, which should be small in order to obtain small or even no switching losses over almost the whole power range [38],

$$FOM = \frac{G_{DS,on}}{C_{oss,eq}}, \quad (3.54)$$

and consequently high FOM-values are aspired. This definition of the FOM is usually applied for hard-switching topologies, however, might not result in the best choice for the converter system at hand, which is basically operated with soft-switching but might lose this ability at light load. The MOSFETs have therefore been pre-selected by analysing the performance according to the optimisation criterion as defined in section 3.2 based on the analytical modelling applied in design procedure.

The CoolMOS™ IPW60R045CP from Infineon is exemplary applied for the loss-calculation in **Fig. 3.11(a)**. Considering the full-load losses in **Fig. 3.11(a)**, the conduction losses P_{co} are reciprocally decreasing with the increasing number of paralleled MOSFETs $n_{sw,p}$, whereas the gate driver losses P_{dr} linearly increase with $n_{sw,p}$. The switching losses P_{sw} are approximately zero if the interlock delay time t_{ild} between the

switching states is sufficient for the complete charge-transfer between the parasitic output capacitors of the MOSFETs in a bridge leg. If the effective output-capacitance, which increases with increasing number of paralleled devices, reaches a value where the charge-transfer is incomplete, the losses are first non-linearly increasing¹⁶; if the capacitance is so high, that the capacitors could almost not be dis-/charged during the interlock delay time and the MOSFETs are completely hard turned off, the switching losses increase almost linearly with $n_{sw,p}$.

If the number of paralleled inverter MOSFETs $n_{sw,p}$ would be chosen for full load, the respective optimal value according to the example shown in **Fig. 3.11(a)** would be $n_{sw,p} = 9$, where the total full-load inverter-losses are only $P_{100\%} = 4.4 \text{ W}$ ¹⁷. However, at part load, e.g. at 10 % of the rated output power, the total inverter losses would drastically increase to $P_{10\%} = 9.9 \text{ W}$, i.e. at 10 % load the losses would be almost doubled. Depending on the device, as well as the turn's ratio, the corresponding duty cycle and current characteristics the resulting loss-difference could even be much worse.

The optimal choice for $n_{sw,p}$ according to the defined optimisation criterion is to parallel only $n_{sw,p} = 4$ switches, which results in increased full-load losses ($4.4 \text{ W} \Rightarrow 5.9 \text{ W}$) due to the higher conduction losses; however, the part load losses are drastically decreased e.g. for 10 % load: $9.9 \text{ W} \Rightarrow 1.0 \text{ W}$. Depending on the operating point resulting from the design parameter values the optimal number of parallel switches might however be different.

In **Fig. 3.11(b)** a further example of the inverter losses in dependency of the number of paralleled switches is presented for another high-performance MOSFET: the MDmesh™ STY112N65M5 from STMicroelectronics. This device features a higher chip area which results in a smaller on-resistance but a higher output capacitance and gate charge. If the same number of paralleled switches as for the above selected CoolMOS™ would be applied, the conduction losses could be decreased; however, the switching losses and the losses in the gate-driver circuit would be higher. The optimum is consequently also different compared to the example above: if only full-load losses were considered, the optimum number of switches would be $n_{sw,p} = 4$ which results in 4.2 W

¹⁶Due to the non-linear output capacitance of the MOSFETs the voltage-slew rate is rather small for low voltages (C_{oss} is high).

¹⁷Due to the small losses, the junction-temperature in the devices can be kept small and therefore the on-resistance of 25°C multiplied with the safety factor of 1.5 has been considered for the comparison of the investigated MOSFETs.

losses; if the load-range from 10 % to 100 % is considered, $n_{\text{sw,p}} = 2$ would be the optimum choice which results in 5.6 W total inverter losses at full load.

Compared to the example with the power transistor IPW60R045CP (Infineon) the optimum losses are only slightly different (0.3 W for the part-load-range optimisation and 0.2 W for the full-load optimisation). In the design-procedure the MDmeshTM STY112N65M5 power transistor (STMicroelectronics) have been considered as the resulting number of switches is smaller and thus the power density can be slightly improved.

3.4.2 Performance-Influence of Magnetic Devices

In the inner optimisation procedure of the magnetic devices, the geometry design parameter values are varied systematically by the optimisation algorithm until the minimum device-losses result for the present operating point defined in the outer loop. In addition to the material-specific flux-limitation, the device volume is also limited and used as constraint in the inner design procedures. The influence of the volume-limitation on the efficiency-optimal design is shown in **Fig. 3.12**, where the optimised transformer losses are illustrated in dependency of the volume-limitation. The limited flux density leads to a minimum core cross-section area and/or primary turns number N_p , respectively. The corresponding efficiency-optimised losses for small volumes are higher because of a higher flux in the core and higher resistance in the winding because of the reduced winding-window width b . The more volume is allowed, the larger the foil width and/or the smaller the number of primary turns, and thus the smaller are the resulting losses. However, the losses-curve becomes rather flat for larger allowed volumes: an increase of the core area would lead to a reduction of the core losses; however the losses due to the skin and proximity effect are contrary increasing due to a higher winding length and must be balanced with a larger winding-width in order to reduce the DC-resistance of the windings.

The resulting efficiency-optimised core geometries for a fixed operating point is illustrated at the top of **Fig. 3.12**. The optimised cores for high volume limitation exhibit a large winding window width b , as foil windings are considered in the optimisation¹⁸. The core-geometry

¹⁸The optimised winding thickness is analytically determined first and therefore fixed in the optimisation process for a given operating point. The only possibility

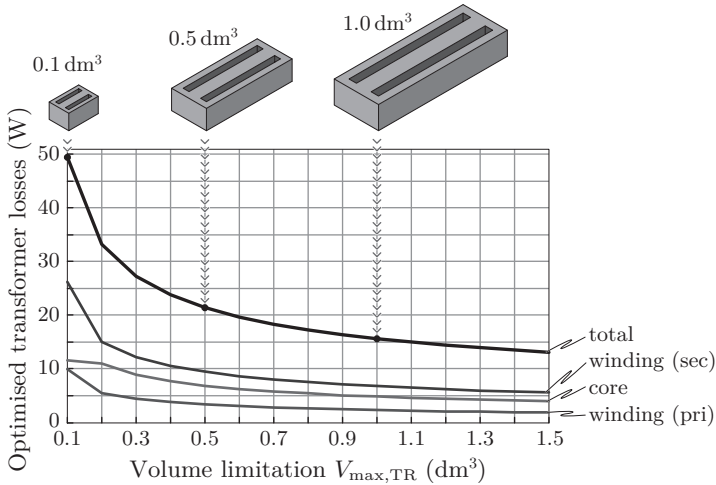


Figure 3.12: Efficiency-optimised transformer losses in dependency of the allowed transformer volume (bounding box around the final transformer, i.e. including windings, which have been omitted in the CAD-drawing). *Example values:* $L_{1,\sigma}=2\mu H$, $k_{Iout}=0.03$, $N_p=32$, $N_s=5$, $f_{sw}=25\text{ kHz}$.

might be different if for example litz-wires would be considered, i.e. the winding-window width would possibly be smaller, however, the optimised core and winding losses are expected to be similar because the core expansion is just shifted in direction and the copper filling factor is constant for the optimised winding specifications.

Regardless of whether litz or foil windings are considered in the design process, the volume has to be limited in the case of an efficiency-optimisation procedure. The transformer volume is limited to 1.0 dm^3 and the output inductor volume to 0.5 dm^3 for the investigated telecom system to achieve the efficiency-goal of 99 %. The volume-limitation can be tighter for a fixed output voltage specification rather than the considered output voltage range of $V_{out} = 46.56\text{ V}$, as further discussed in the next subsection. Furthermore, the optimised semiconductor losses cannot be improved without changing the devices and therefore, the only possibility to reduce the converter system losses is to reduce the magnetic components losses by increasing the volume.

to reduce the DC-resistance is consequently to increase the winding-width b_f .

Table 3.1: Fixed parameters applied in the optimisation procedure.

Electric Specifications			
Input	$V_{\text{in}} = 400 \text{ V}$ $D_{\text{max}} = 0.95$	Output	$V_{\text{out}} = 46 \text{ V}..56 \text{ V}$ $\Delta v_{\text{out}} = 300 \text{ mVpp}$ $P_{\text{out}} = 5 \text{ kW}$
Semiconductors			
Inverter	ST STY112N65M5	Rectifier	IR IRF4668Pbf
MOSFETs	MDmesh TM TO-247 MAX	MOSFETs	HEXFET [®] TO-247
Gate driver	IXYS IXDD414 14 A-type	Control	TI TMS320F2808 DSP
Magnetic devices			
Transformer	Ferrite N87 $B_{\text{max,Tr}} \leq 300 \text{ mT}$ $V_{\text{max,Tr}} \leq 1.0 \text{ dm}^3$	Inductor	Metglas [®] 2605SA1 $B_{\text{max,L}} \leq 1.2 \text{ T}$ $V_{\text{max,L}} \leq 0.5 \text{ dm}^3$

3.4.3 Efficiency-Optimal Converter System

In the starting point for the design procedure the fixed parameters as listed in **Tab. 3.1** have been specified. The maximum allowed volume for the transformer $V_{\text{max,TR}} = 1.0 \text{ dm}^3$ (61 in^3) has been chosen as a limit, as the losses in the magnetic components show only a small decrease above this level, as shown in **Fig. 3.12**. That is a high price to pay for the aim of 99 % efficiency and the wide output voltage range. The higher the output voltage the higher the duty cycle¹⁹ and therefore the turns-ratio choice is limited. The nominal output voltage $V_{\text{out,n}} = 50 \text{ V}$ results in a smaller duty cycle which might not be ideal with respect to the highly efficient power transfer. The maximum output inductor volume has been set to $V_{\text{max,L}} = 0.5 \text{ dm}^3$ (30.5 in^3).

The inverter and synchronous-rectifier MOSFETs have been preselected based on the optimisation results for a fixed operating point, which has been determined during pre-runs of the optimisation procedure. The best results for the inverter full-bridge switches were achieved with

¹⁹The duty cycle is limited to 95 % for the worst case (lowest efficiency and highest output voltage) to ensure a reasonable controller dynamic.

Table 3.2: Optimised design parameter values considering a volume limit of 1.0 dm^3 (61 in^3) for the transformer and 0.5 dm^3 (30.5 in^3) for the output inductor.

f_{sw} (kHz)	Turn numbers			MOSFETs		L_σ	L_{out}	C_{out}	k_I
	N_p	N_s	N_L	$n_{\text{sw,p}}$	$n_{\text{sw,s}}$	(μH)	(μH)	(μF)	(%)
16.0	32	5	8	3	7	4.8	77.8	52.1	4
25.0	32	5	8	2	5	4.8	99.6	25.0	3
37.5	32	5	7	2	4	3.0	66.5	11.1	2
50.0	32	5	8	2	3	2.0	99.8	4.2	1
100.0	25	4	6	1	2	0.3	54.7	2.1	1
200.0	19	3	7	1	2	0.3	8.7	3.1	3

the power transistor MDmeshTM STY112N65M5 from STMicroelectronics. The HEXFET[®] IRF4668PbF from International Rectifier has been selected as MOSFET applied in the synchronous rectifier.

The remaining outer-loop design parameter values resulting from the optimisation procedure are presented in **Tab. 3.2** for six frequency points. According the defined optimisation criterion, which considers the part-load losses, the optimum is achieved at a switching frequency of $f_{\text{sw}} = 16 \text{ kHz}$ and is increasing with higher frequencies as shown in **Fig. 3.13(a)**. Due to the flux density limitation, the number of turns of the magnetic components is higher for lower switching frequencies. The output inductance can be reduced at higher frequency, which results in smaller winding turns numbers, as well, while the current ripple is almost constant.

The optimised number $n_{\text{sw,p}}$ of paralleled MOSFETs in the inverter stage is continuously decreasing for higher switching frequencies due to the incomplete dis-/charging of the parasitic output capacitances especially at low-load conditions which results in switching losses. However, this results in higher conduction losses (higher on-resistance) and the total inverter losses are therefore increasing as well for higher frequencies, as illustrated in **Fig. 3.13(b)**. The bend in the total losses curve for example above 50 kHz is mainly caused by this effect, as the number of paralleled switches in the inverter stage is changed from two to one. This effect is even more drastic for the synchronous-rectifier switches as the switching losses are always present in the hard-commutating

rectifier with only a small dependency from the load. The number of paralleled inverter and synchronous-rectifier MOSFETs, $n_{\text{sw,p}}$ and $n_{\text{sw,s}}$, are furthermore decreasing at higher switching frequencies because of the frequency-dependent gate drive losses.

In addition to the losses in the synchronous rectifier, the losses in the magnetic components have a high influence in the low-frequency range because of the volume limitation as illustrated in **Fig. 3.13(b)**. Furthermore, the minimum number of turns increases due to the flux density limitations, which leads to higher winding losses. Due to the decreasing number of turns and smaller required core-cross sectional areas for higher switching frequencies, losses in the magnetic components also decrease. The winding losses, due to proximity and skin effect, as well as core losses increase again for frequencies higher than 200 kHz.

The losses for the output inductor are mainly caused by the winding losses, which decrease for higher frequencies due to the decreasing turns number. However, for higher switching frequencies, HF-winding losses and core losses increase similarly as for the transformer. The remaining losses (control unit, auxiliary supply, output capacitors) stay approx. constant over the entire frequency range.

The load-dependent efficiency graph of the optimised DC-DC converter system which operates with 16 kHz switching frequency is depicted in **Fig. 3.13(c)**. The Energy Star[®] requirements are clearly excelled in the entire load range. Moreover, the maximum efficiency of 99 % could be reached at half-load and the optimisation goal is fulfilled. The full-load efficiency is still at a very high level (98.9 %), i.e. even less than 51 W losses are generated in the converter when operating with 5 kW and 50 V output power. The efficiency curve features a flat characteristic also for light load ($\eta = 98.4 \%$ at 20 % load). Below 20 % load, the efficiency drops due to the constant loss components, switching and core losses.

The distribution of the device-losses is illustrated with examples for full load and 10 % load in **Fig. 3.13(d)**. At full load, the synchronous-rectifier MOSFETs have the biggest share of the losses, mainly caused by the conduction losses (78 % of the SR-losses). The full-load losses could consequently be reduced by increasing the number of paralleled MOSFETs, which would however result in increased switching losses at low-load operation. The synchronous rectifier has still a high influence on the losses at low-load operation (29 %), however, the switching losses are dominating (82 % of the SR-losses) and the SR-conduction losses

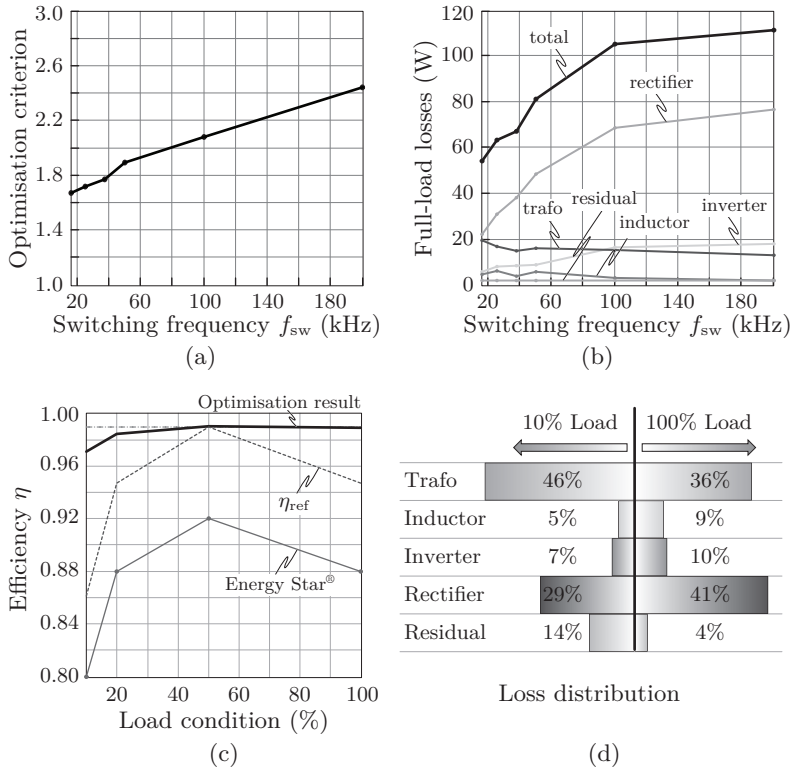


Figure 3.13: Optimisation results for the high-efficiency DC-DC converter system (output voltage range $V_{out} = 46..56$ V, graphics shown for nominal output voltage $V_{out,n} = 50$). (a) Optimisation criteria in dependency of switching frequency. (b) Full-load losses in dependency of switching frequency. (c) Efficiency of the optimal system in dependency of the load. (d) Losses distribution at full load and 10 % load.

only contribute with 1 % to the total losses.

The transformer has with 36 % the second-biggest loss-share on the total full-load losses mainly determined by the windings. If the converter operates only with 10 % load, the transformer contributes most to the converter losses (46 %), almost exclusively caused by the core

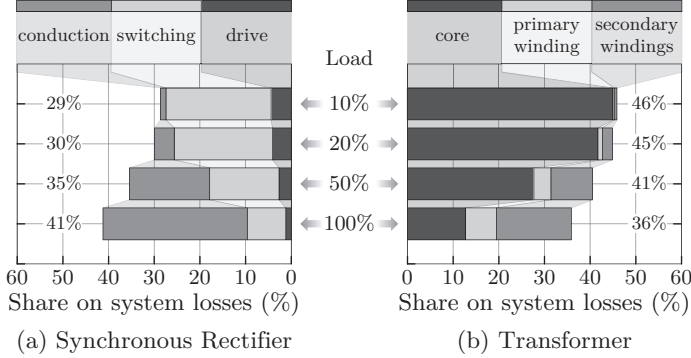


Figure 3.14: Load-dependent loss distribution of (a) the synchronous rectifier and (b) the transformer.

losses which are almost constant over the entire load-range²⁰.

The inverter MOSFETs have only a minor share on the losses (10 % at full load and 7 % at 10 % load). At full load the inverter losses are mainly determined by the conduction losses whereas at 10 % load by the switching losses, similar to the synchronous rectifier.

Fig. 3.13(d) furthermore reveals the influence of the control circuit and output capacitor (“residual” losses). While these losses at full load have only a minor share on the total converter losses (about 4 %), the almost constant residual losses²¹ contribute with 14 % at 10 % load, more than the inverter and inductor together.

The resulting optimised geometry parameters determined in the inner optimisation procedures of the magnetic components are summarised in **Tab. 3.3**.

Optimisation for a Fixed Output Voltage $V_{\text{out},n} = 50 \text{ V}$ If the output voltage range is of minor interest and only the nominal voltage is considered, the optimisation would result in an improved system performance compared to the wide-range optimisation. As an example, the allowed volumes for the magnetic components could be reduced

²⁰The core losses are only slightly decreasing with the load due to the smaller duty cycle.

²¹The control losses are assumed to be constant and the losses in the output capacitor are almost constant as the ripple current which is filtered does only slightly change with the duty cycle in the load-range.

Table 3.3: Efficiency-optimised geometry design parameters.

Transformer	Inductor
$a = 28.6 \text{ mm}$	$a = 22.4 \text{ mm}$
$b = 165.5 \text{ mm}$	$b = 125.4 \text{ mm}$
$c = 48.3 \text{ mm}$	$c = 39.0 \text{ mm}$
$d_{\text{opt,p}} = 55.8 \text{ }\mu\text{m}$	$d_{\text{opt,L}} = 500 \text{ }\mu\text{m}$
$d_{\text{opt,s}} = 167.3 \text{ }\mu\text{m}$	$l_{\sigma} = 0.85 \text{ mm}$

and the optimisation goal of 99 % at half-load could still be reached. For this investigation, the design procedure has been repeated with the same constraints as presented in **Tab. 3.1** – only the volume of the transformer has been reduced from 1.0 dm^3 to 0.6 dm^3 and the allowed volume of the output inductor has been reduced from 0.5 dm^3 to 0.4 dm^3 – thus the net volume of the magnet components has been reduced by one third. The resulting optimised winding ratio is $N_p:N_s = 36:5$, two MOSFETs would be paralleled in the inverter stage and for the synchronous rectifier six MOSFETs are in parallel. The cross-sectional area of the magnetic components is almost equal with the optimisation results shown above, but the winding window could be reduced as the RMS-current is reduced due to a better-utilised duty cycle. The efficiency curve of the optimised system does almost not change compared to the optimised system with a wide output voltage range. The loss-distribution has slightly changed, as the losses in the transformer are higher but the losses in the semiconductors are smaller (optimal utilisation of the duty cycle and smaller RMS-currents).

In the next section, a prototype of a high efficient converter is assembled in order to validate the applied analytical models in the optimisation procedure.

3.5 Realised High-Efficiency CTR Prototype

A prototype has been designed based on the design parameters resulting from the optimisation procedure for the validation of the proposed analytical converter models. The measurement results are discussed and compared with the calculation results. An improved switching strategy for the synchronous-rectifier MOSFETs is furthermore discussed which

Table 3.4: Applied components in the CTR-prototype.

Transformer		Inductor	
Core	EPCOS E70/33/32 2 sets in parallel	Core	Metglas® AMCC320 legs cut
Windings	– litz wires – $N_p = 22$ 175x0.2 mm (pri) $N_s = 3$ 600x0.2 mm (sec)	Windings	– litz wires – $N_L = 4$ 1200x0.2 mm
		Inductance	$L_{out} = 43.6 \mu\text{H}$
		Air gap	$l_\sigma = 519 \mu\text{m}$
Inverter		Rectifier	
MOSFETS	Infineon CoolMOS™ IPW60R041C6 $n_{sw,p} = 2$	MOSFETS	Int. Rectifier HEXFET® IR IRF4668PbF $n_{sw,s} = (\text{up to}) 11$
Output Capacitor			
Murata X7R, 2.2 μF /100 V, 44 in parallel			

results in a higher efficiency.

The prototype presented results from an efficiency-optimisation with a volume limit of both, transformer and output inductor, of only 0.3 dm^3 . The resulting power density is still reasonable (2.3 kWdm^{-3}) and even though an efficiency of 98.9 % instead of the aim of 99.0 % is possible, the prototype gave a great possibility to validate the operating point and the loss models and to eventually enable model adjustments.

Standard components available on the market at the time of the assembly were considered for the construction of the converter prototype. The resulting optimised core geometry for the maximum volume of 0.3 dm^3 of the transformer can be realised approximately by paralleling two EPCOS E70/33/32 core-sets. The resulting inductor-core cross-section area is close to the Metglas® AMCC 320 core, whereas the legs of this C-core have been cut due to the over-sized winding window width of the commercial core for this application.

Copper foils have been considered in the optimisation procedure for the windings and the optimal thicknesses have been determined. In

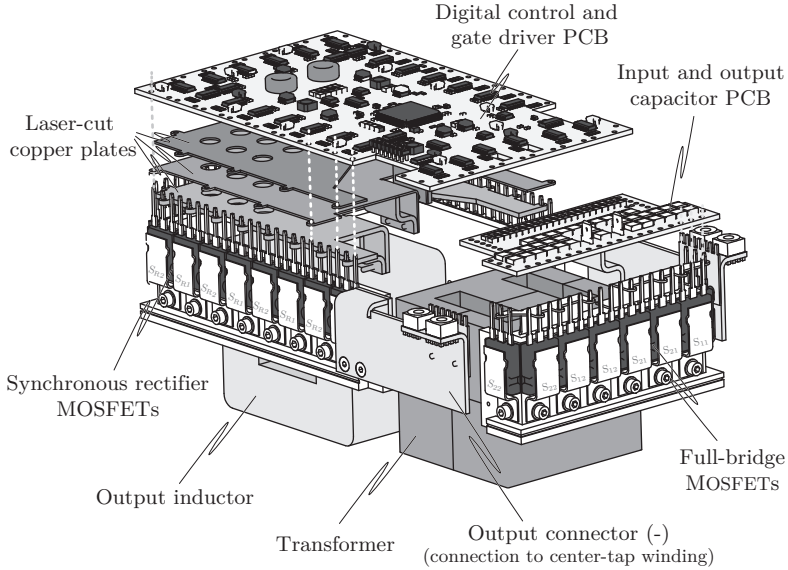


Figure 3.15: Exploded assembly drawing of the realised high-efficient converter prototype. (The case not shown; on a scale of 1:3.)

order to utilise the winding window of the standard cores mentioned above, litz wires have been applied instead of foil windings (details are presented in **Tab. 3.4**). The applied litz wire for the primary winding don't result in minimal losses as the single-wire diameter is not optimal regarding to the high-frequency losses, however, the more feasible 350x0.1-mm-litz-wire package was, without notice, not available at the time of construction.

Furthermore, the foreseen inverter MOSFETs (STMicroelectronics MDmesh™ STY112N65M5) which had been introduced during the calculations, were still not available at the time of the construction and therefore the Infineon CoolMOS™ IPW60R041C6 power transistor was used. As the Infineon CoolMOS™ device features a higher on-resistance ($R_{DS,on} = 41 \text{ m}\Omega$, compared to very low on-resistance of $R_{DS,on} = 19 \text{ m}\Omega$ of the STY112N65M5), the conduction losses are higher as further discussed below. A summary of the components used is given in **Tab. 3.4**.

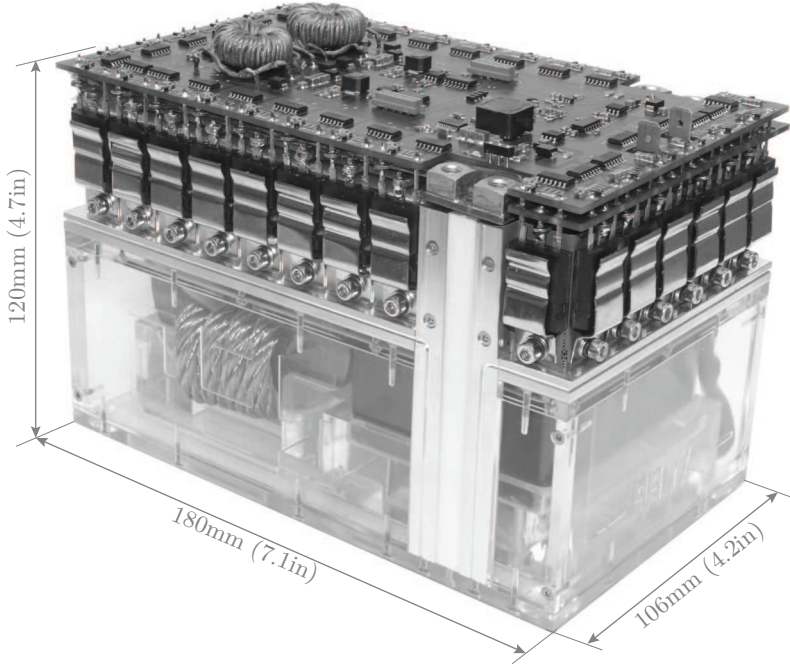


Figure 3.16: Constructed highly efficient DC-DC converter prototype (400 V to 46 V..56 V, 5 kW output power, efficiency $\eta > 98.6\%$, power density $\rho = 2.3 \text{ kWdm}^{-3}$, i.e. 36 Win^{-3}).

Due to the selection of commercially-available cores instead of the calculated ones, the volume is higher than the volume limit of 0.3 dm^3 (18.3 in^3) used in the optimisation procedure: the volume of the transformer is 0.48 dm^3 (29.2 in^3) and 0.39 dm^3 (23.1 in^3) is the output inductor volume. The larger volume theoretically results in further improvements of the calculated efficiency of the magnetic devices, but with a lower power density. Due to the used core-assembly in the prototype, the cross-sectional area is increased by factor 1.5, which results in decreased core losses by a factor of ≈ 2.8 (from 10.0 W to 3.6 W). The drawback in the assembly is the smaller winding-window height, where the calculated optimal foil windings could not be used and the resulting winding losses are higher.

The exploded assembly drawing of the high-efficiency prototype

constructed is shown in **Fig. 3.15**. The MOSFETs are clamped on two mounting frames (one for the synchronous-rectifier MOSFETs and one for the inverter MOSFETs), which are electrically isolated. The synchronous-rectifier MOSFETs are directly mounted with thermal grease on the base plate (alternately, i.e. SR_{1a} - SR_{2a} - SR_{1b} ...), as the drains have the common inductor potential. The phase-change material Hi-Flow[®] 300P from Bergquist has been applied as electric isolation for the inverter switches. The low-resistive connections between the MOSFETs and windings were featured by designing laser-cut copper plates and thus no power is carried in the Printed Circuit Boards (PCBs). A PCB with the output capacitors and input capacitors²² for the inverter MOSFETs is arranged first above the connection layers. On top of the converter system is the control-electronics PCB with the required power supplies for voltage adjustments and galvanic isolation (SR-gate-drive circuits), current and voltage-measurement circuits, gate-drive circuits and digital control.

The mounting frames for the MOSFETs are arranged around the magnetic devices (transformer and output inductor). Contrary to the power-density-optimised systems presented in chapter 2 the components contributing to the power-transfer (transformer, inductor and MOSFETs) are cooled solely by free convection. The final prototype assembly is shown in **Fig. 3.16**.

The calculated loss-distribution at full-load conditions ($V_{out} = 48\text{ V}$) is shown in **Fig. 3.17**. The highest share on the total converter losses has the transformer (more than 50 %), mainly caused by the high HF-winding losses $P_w \approx 46.5\text{ W}$ due to high proximity losses because of the applied non-ideal litz wire. With a more appropriate litz wire package, e.g. 350x0.1 mm, the losses could be reduced to 33.7 W which would already result in a maximum efficiency of 98.8 %. Additionally, as shown in the previous section, the losses could be further reduced if a higher volume would be permitted.

Almost one third of the total losses are caused by the synchronous-rectifier MOSFETs. If only eight of the possible eleven MOSFETs were applied, the half-load losses could be slightly reduced from 12.1 W to 11.4 W, however, the full-load losses would increase from 23.2 W to 26.5 W.

²²Some intermediate circuit (input) capacitors have been mounted in close vicinity of the inverter MOSFETs in order create a low-inductive supply for the fast switching transitions.

	Volumes		←	→	Losses	
Inverter	0.058 dm ³	3%			13%	12.2 W
Rectifier	0.148 dm ³	6%			28%	23.2 W
Trafo	0.428 dm ³	19%			52%	46.5 W
Inductor	0.560 dm ³	24%			6%	5.0 W
Residual	0.124 dm ³	9%			3%	3.0 W
Con./Space	0.892 dm ³	39%				

Figure 3.17: Volume and loss distribution for the assembled prototype. Output voltage $V_{\text{out}} = 48 \text{ V}$, $P_{\text{out}} = 5 \text{ kW}$.

The third highest loss-share is caused by the inverter MOSFETs. If the devices STY112N65M5 with the prosed specifications would be applied, the full-load losses could be decreased from 12.2 W to 6.7 W. Almost the same result would be reached, if more of the applied Infineon devices would have been used, e.g. five power MOSFETs IPW60R041C6 in parallel would result in 6.8 W total inverter losses at full load²³.

The output inductor has only the fourth-highest loss-share. As HF-losses have only a minor influence on the winding losses, smaller losses could here be achieved, if more copper would be applied. The inductor core-losses have almost no influence on the loss distribution (less than 1 W).

The losses in the control electronics and the auxiliary supply are almost constant over the entire load range. In the prototype, the Digital Signal Processor (DSP) TI TMS320F2808 is clocked with a reduced frequency (20 MHz instead of 100 MHz), which reduces the DSP power consumption by 62 % from approx. 550 mW to 210 mW [199]. The design of the control electronics, e.g. the galvanically isolated power supplies for the synchronous rectifiers and the gate-driver circuits are furthermore focused on efficiency as well. The measured input power for the entire control electronics – excluding the gate drive losses and the auxiliary power supply – is only 610 mW during operation.

Measurement Results

The measured transformer primary current i_p and the voltage waveform v_{AB} at full-load operation of the converter system ($V_{\text{in}} = 400 \text{ V}$,

²³The additional device costs and the required higher volume are not considered.

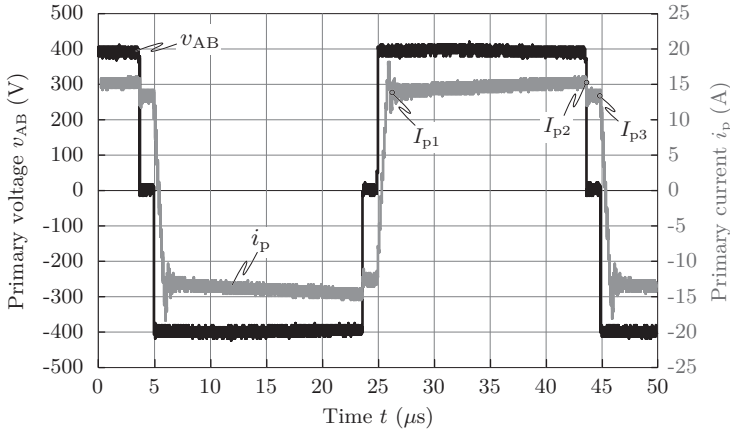


Figure 3.18: Measured transformer primary current i_p and voltage v_{AB} at full-load operation, $V_{out} = 48 \text{ V}$, $P_{out} = 5065 \text{ W}$.

$V_{out} = 48 \text{ V}$, $P_{out} = 5065 \text{ W}$) are illustrated in **Fig. 3.18**. The converter is operating with zero voltage switching conditions and therefore v_{AB} exhibits no voltage-overshoot. The small overshoot of the primary transformer current i_p is caused by the reverse-recovery current of the synchronous rectifier reflected from the transformer secondary side. The characteristic current points I_{p1} , I_{p2} and I_{p3} are emphasised in **Fig. 3.18** and further investigated for the operating-point modelling.

A summary of the characteristic values of the operating point are presented in **Tab. 3.5**. The first column shows the values resulting from the analytical models applied in the optimisation procedure. The characteristic values in the second column were determined with an electric circuit simulation software (GeckoCIRCUITS [200]), where additional parasitic elements, e.g. output capacitors of the MOSFETs, have been considered. In the third column, the characteristic values resulting from the measurements as presented in **Fig. 3.18**. The values shown in **Tab. 3.5** are in close agreement and the applied analytical converter model can be confirmed.

The measured converter efficiency as function of the output power is presented in **Fig. 3.19**. The measurement shows that the required Energy Star®-efficiency is clearly exceeded; in the entire load range the efficiency exhibits a flat characteristic even at light load. The cal-

Table 3.5: Validation of the analytical operating-point model; comparison of the characteristic operating point values resulting in the optimisation procedure, simulation and measurements.

	Calculation	Simulation	Measurement
V_{in}	400.0 V	400.0 V	399.7 V
V_{out}	48.0 V	48.0 V	48.1 V
P_{out}	5000 W	5000 W	5065 W
Duty cycle	0.909	0.908	0.933
I_{P1}	13.2 A	13.8 A	13.8 A
I_{P2}	15.3 A	15.2 A	15.2 A
I_{P3}	15.0 A	11.8 A	13.3 A
$I_{P,rms}$	14.2 A	13.9 A	14.1 A

culated efficiency for the applied components, cf. **Tab. 3.4**, and the reference efficiency (optimisation goal) are plotted as well. The calculated and measured efficiencies are almost equal over a wide load range; only at light load the measured and calculated curves are diverging and the absolute efficiency difference at 10 % load is $\approx 2\%$. With the assumption that with the consistency of the total losses, the losses of the discrete components are consistent, the loss models are validated with the measurements. The measurements have been repeated several times in order to confirm this assumption. In addition, the number of the paralleled synchronous-rectifier MOSFETs has been reduced and the measurements again exhibit a very good agreement, so that it can be assumed, that with the analytical model of the synchronous rectifier the generated losses can be approximated correctly.

The loss-distribution can furthermore be validated to some extent with a thermal image of the operating converter system²⁴ as presented in **Fig. 3.20**. The thermal image shows the converter operating at full load for more than 30 min so that the steady-state temperature is reached. Although the system components are cooled solely by free convection, the maximum temperature is below 80 °C (ambient-temperature $T_a = 27^\circ\text{C}$). Due to the low-resistance connection (both, thermally and electrical) the heat from the transformer is transferred

²⁴In order to measure the temperature of the magnetic components, the acrylic glass-box of the prototype assembly as shown in **Fig. 3.16** has been removed.

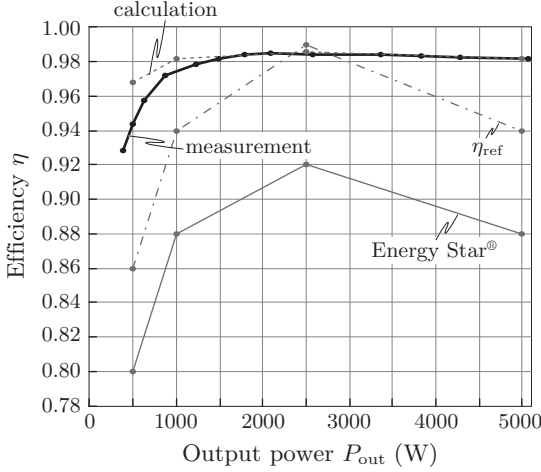


Figure 3.19: Measured efficiency of the prototype. $V_{in} = 400\text{ V}$, $V_{out} = 48\text{ V}$, $P_{out} = 383..5065\text{ W}$.

also to the rectifier and inverter MOSFETs which blurs the thermal distribution, however, the transformer which has the highest loss-share, cf. **Fig. 3.17**, clearly exhibits the highest temperature as shown **Fig. 3.19**. The inductor, which only contributes 6 % to the system losses, exhibits the lowest temperature, whereas the semiconductor temperatures are between the transformer and inductor temperatures similarly as their loss-contribution. Some more investigations of the transformer, connections and synchronous-rectifier losses are summarised in the following paragraphs.

Transformer Losses The thermal image (**Fig. 3.20**) and the loss-calculations (**Fig. 3.17**) for full-load operation, identify both the transformer as the component with the highest contribution on the losses in the prototype. In order to validate the transformer loss-model a comparative measurement is performed: DC-current sources are connected to the windings of an identically-assembled transformer and the currents are increased in steps once the steady state temperature is reached. The cooling conditions are almost identical to the operation conditions in the converter. The temperatures from the thermal images are compared with the temperatures in **Fig. 3.20** (full-load operation).

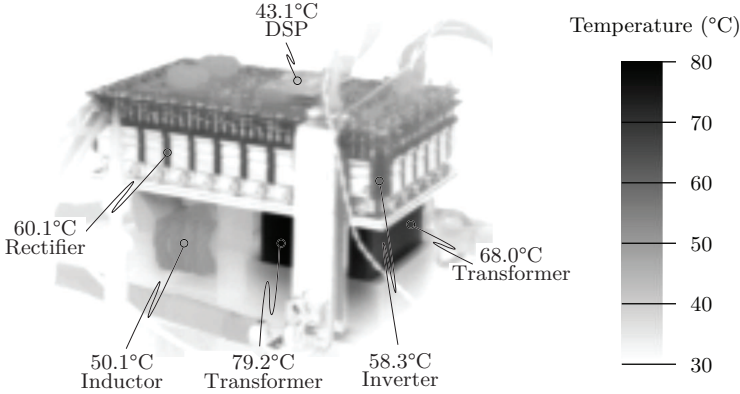


Figure 3.20: Thermal image measured with an infra-red camera. Steady-state temperatures (system has been operating more than 30 min at full load: $V_{in} = 400\text{ V}$, $V_{out} = 48\text{ V}$, $P_{out} = 5047\text{ W}$, ambient temperature $T_a = 27^\circ\text{C}$). The acrylic glass-box as shown in **Fig. 3.16** has been removed in order to measure the temperatures of the magnetic components.

An equivalent temperature has been reached once the sum of the measured primary and secondary winding DC-losses has been above 42W. Compared to the calculated losses $P_{Tr} \approx 46\text{ W}$ (including core and HF-winding losses), the difference is approx. 4 W.

During the experiment described above, the DC-winding-resistances can be measured as well, which are only slightly higher than the calculated values:

	Calc. R_{DC}	Meas. R_{DC}
Primary winding	$\approx 17.1\text{ m}\Omega$	$\approx 17.5\text{ m}\Omega$
Secondary winding	$\approx 0.94\text{ m}\Omega$	$\approx 1.1\text{ m}\Omega$

However, the slight difference between the calculated and measured resistance on the secondary winding ($0.16\text{ m}\Omega$) already causes approx. 2 W additional losses.

Further losses can be caused by parameter tolerances of the core. The measured core losses, performed with the measurement system and the underlying method described in [201] are approx. 1 W higher than calculated with the Steinmetz-parameters gained from the data sheet (which are commonly subjected to comparatively high tolerances).

It has been further identified in [169], that core losses are also generated if the magnetic flux is constant after a time interval with changing flux, which is the case during the free-wheeling phase. These losses are not considered in Sullivan's extended Steinmetz-formula [176] as applied in (3.41). These losses are generated due to relaxation effects, cf. section 2.1.2, or for example [167], and can be included in loss-calculations by applying an improved generalized Steinmetz equation (i^2 GSE) as described in [202].

Inter-Connection Losses The losses (DC and AC) in the interconnections and terminals are neglected in the analytical models, due to their strong dependence on the realisation. In order to determine the losses caused in the interconnections, the inverter MOSFETs S_{11} and S_{22} as well as the synchronous-rectifier switches S_{R1} and S_{R2} are turned on and current sources are connected to the input and output of the converter system in order to determine the DC-resistance. The input-DC-current is carried by MOSFETs S_{11} , MOSFETs S_{22} and the primary winding whereas the supplied output current is carried by MOSFETs S_{R1} , MOSFETs S_{R2} , both secondary transformer windings and the output inductor winding. The resulting interconnection DC-resistance, (measured resistance minus the calculated resistances for the semiconductors and windings) is only 0.1 m Ω , which results in approx. 1 W higher losses at full-load conditions. However, the AC-resistance of the interconnections is not considered. (A high-accurate impedance-measurement is difficult due to the small resistance values. Comprehensive 3-D FEM-simulations with exact geometric and electric models could be applied instead.)

Synchronous Rectifier The synchronous rectifier takes a comparably high influence on the total system losses over the entire load-range as illustrated in **Fig. 3.13(d)** and **Fig. 3.14** (page 206 and 207); at part load mainly due to the switching losses and at high load mainly because of the conduction losses. One possibility of reducing the switching losses in the synchronous rectifier is the determination of the optimum turn-off point in time $t_{\text{off,SR}}$ as discussed in the following paragraph.

In **Fig. 3.21**, the drain current i_D , the drain-source voltage v_{DS} and the control signal of the rectifier switch S_{R2} during the turn-off phase are illustrated. If the rectifier MOSFETs are turned off when the inverter switching state changes from the free-wheeling phase to the

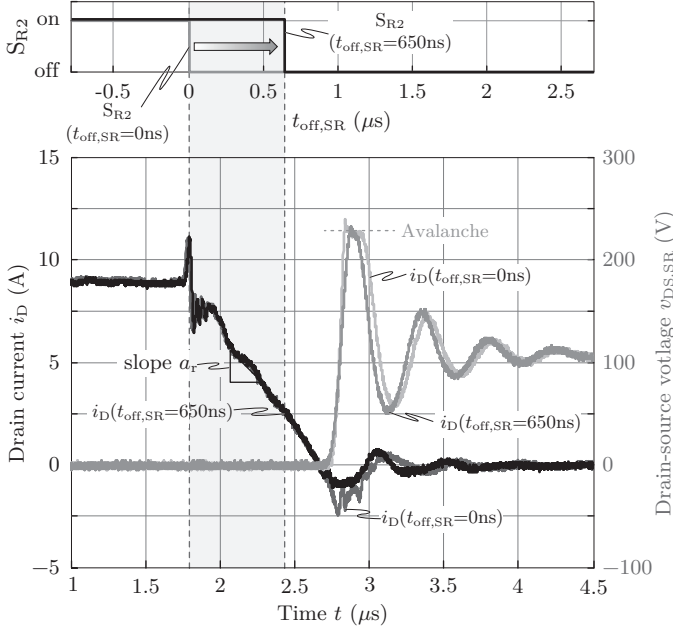


Figure 3.21: Measured drain current i_D and drain-source voltage v_{DS} waveform of a synchronous-rectifier MOSFET when turning off for $t_{\text{off,SR}} = 650 \text{ ns}$ and $t_{\text{off,SR}} = 0 \text{ ns}$ (light-grey curves). The control signal for MOSFETs S_{R2} is shown at the top.

active phase ($t_{\text{off,SR}} = 0$ in **Fig. 3.21**), the current commutates first from the MOSFET-channel to the body diode and then to the opposite synchronous-rectifier MOSFET. This hard commutation results in additional recovery losses, in forward conduction losses and possibly in further losses due to avalanche effects, as shown in **Fig. 3.21**. The high voltage ringing, due to the parasitic resonance tank formed by the secondary winding leakage inductance and the parasitic output capacitance of the synchronous-rectifier MOSFETs, can be reduced by a bifilar secondary winding implementation, resulting in a smaller stored leakage energy, however with the disadvantage of a higher winding-capacitance.

If a time delay for the turn-off-signal of the rectifier switch is implemented, i.e. $t_{\text{off,SR}} > 0$, the losses also change due to the reduced body diode conduction time. The forward conduction losses during the

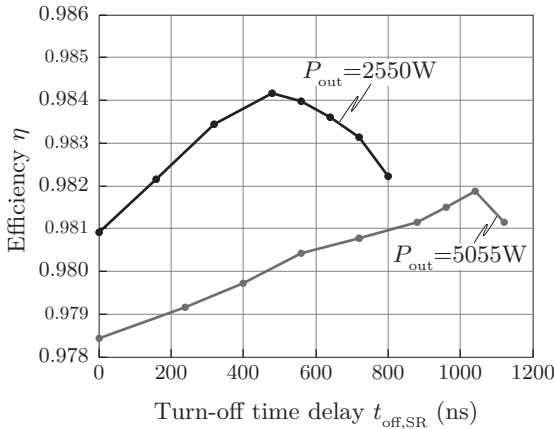


Figure 3.22: Measured efficiency for the converter system in dependency of the turn-off delay time of the synchronous rectifier after the full bridge changes from the free-wheeling to the powering state.

current-commutation are reduced, on the one hand. On the other hand, the recovery charge is reduced, which results in a decreased reverse-current peak I_{RM} and the reduced over-voltage results in smaller or no avalanche energy, respectively. The improvements can be seen in **Fig. 3.22**, where the influence of the turn-off-time $t_{\text{off,SR}}$ on the system efficiency η is shown. At full-load operation ($P_{\text{out}} \approx 5055\text{ W}$), the efficiency can be improved by approx. 0.35 %, i.e. the losses are reduced by over 18 W, which is almost 20 % of the measured total losses. The share of forward conduction losses to the total loss reduction is approx. 22 % ($\approx 4\text{ W}$). The efficiency at 50 % load ($P_{\text{out}} \approx 2050\text{ W}$) could be increased by 0.32 %, i.e. a loss-reduction of 8.6 W (again, almost 20 % of the measured total losses) could be achieved.

As can be seen in **Fig. 3.22**, there is an optimum turn-off time. If the turn-off time is higher than the optimum and thus the current has completely commutated to the opposite rectifier switch, the losses are quickly increase and could destroy the MOSFETs as a continued conduction of the (still) turned-on rectifier causes a short circuit. The optimum turn-off time, which is dependent on the output current, can be stored as a table in the DSP.

The recovery charge is small, if the MOSFET is switched off at the

optimal $t_{\text{off,SR}}$ due to the smaller current, which has to be switched off. The total (measured) charge is reduced from 392 nC at $t_{\text{off,SR}} = 0$ to approx. 208 nC at full load and the optimal point of time $t_{\text{off,SR}} = 650$ ns. A further decrease is not possible for the given slew rate because of the presence of the remaining parasitic output capacitor charge Q_{oss} . The turn-off losses due to the output capacitor and the remaining recovery charge (diffusion charge) have been included in the optimisation procedure as presented in section 3.3.2.

The analytical models have been validated by the measurement results. Nevertheless, as some components considered in the optimisation procedure were not available, the prototype constructed does not reach the targeted efficiency. In order to improve the efficiency with the prototype, the following design parameter values are changed:

- ▶ Primary winding litz wires 420x0.1 mm.
- ▶ Secondary winding litz wires 600x0.2 mm.
- ▶ Number of paralleled sync. rectifier switches $n_{\text{sw,s}} = 7$.
- ▶ Losses in the control electronic are reduced to the measured value $P_{\text{aux}} = 610$ mW.
- ▶ The MOSFETs ST STY112N65M5 are applied in the inverter.

The resulting efficiency at 50 % load with only this slightly adopted prototype design parameter values is $\eta = 98.9\%$ (26.9 W total losses).

3.6 Design Parameter Influence

The major efficiency-influencing components are the transformer, the output inductor, and the inverter and rectifier MOSFETs as discussed in section 3.4, e.g. in **Fig. 3.13** on page 206. In this section, the influence of these components is quantified by calculating the influence of changing characteristic component specifications on the system performance. This investigation is based on the efficiency-optimised system shown in section 3.4.

The quality index in dependency of the number of paralleled MOSFETs ($n_{\text{sw,p}}$ and $n_{\text{sw,s}}$) is illustrated in **Fig. 3.23(a)**. The optimum can be found if two inverter switches and 4 rectifier switches are in parallel in this example ($f_{\text{sw}} = 37.5$ kHz). In **Fig. 3.23(b)**, the half-load losses

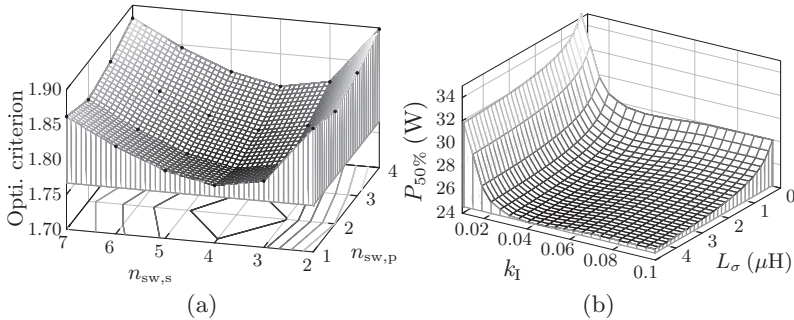


Figure 3.23: Cross section of the performance landscape for different design parameters. (a) Optimisation criteria, i.e. quality index in dependency of the number of parallel MOSFETs ($n_{sw,P}, n_{sw,S}$) ($f_{sw}=37.5$ kHz) (b) Half-load efficiency in dependency of leakage inductance L_σ and output current ripple factor k_I ($f_{sw}=16$ kHz).

in dependency of the output current ripple factor k_I and the leakage inductance L_σ is shown for a lower switching frequency ($f_{sw} = 16$ kHz). The optimum design there can be found with an output ripple factor around 4 % (± 2 A) and a leakage inductance of 4.7 μH ; at this point the half-load losses are approximately minimal as well. The landscapes in **Fig. 3.23** generally feature a flat characteristic for the optimised DC-DC converter, which can be anticipated for this kind of physical system. This enables a sensitivity analysis by slightly changing the system parameters of the of the efficiency-optimised DC-DC converter.

Inverter Influence The continuous improvements of MOSFETs especially with a blocking capability around 600 V in the last decade enables a small on-resistance, however, usually with the drawback of a higher output capacitance C_{oss} . Highly-efficient converter systems with the ability of soft-switching are commonly operated with a low switching frequency so that the ZVS-range can be efficiently increased by increasing the interlock delay time and leakage inductance if MOSFETs with a high output capacitance are applied. The on-resistance is of major interest for these systems.

If the on-resistance of the applied MOSFET could be halved, the total full-bridge losses (driving, switching and conduction losses) would be reduced by 42 % when operating at full load and by 26 % at half

load. The total converter losses would be reduced by 4 % (full load) and 2 % (half load), respectively, and the efficiency would be increased from 99.0 % to 99.1 % at half load (98.9 % to 99.0 % at full load).

The reduction of the on-resistance would allow to achieve the aim of a half-load efficiency of $\eta = 99\%$ if the number of paralleled inverter MOSFETs would be reduced from three to one. In this case, the full-load losses would be increased by 3 % (as the inverter losses increase by 30 % to 7.3 W). However, at 50 % load the efficiency could be improved as the losses there are mainly determined by the driving and switching losses around this load-point.

Synchronous-Rectifier Influence The synchronous rectifier has the biggest share on the full-load losses as presented in **Fig. 3.13**. If similar improvements, as can be seen for the 600-V-MOSFETs, would also be assumed for MOSFETs in the blocking voltage range up to 200 V, the system performance with respect to efficiency (as well as power density) could be significantly increased. In addition to the reduction of the on-resistance, the (simultaneous) reduction of the output capacitance and the recovery effects are desirable for the hard-switched rectifier MOSFETs; nevertheless, these physical parameters are inversely interdependent and the improvement of one parameter is commonly reached at the expense of another parameter if the semiconductor technology remains unchanged.

The same imaginary scenario as for the inverter MOSFETs is applied for the rectifier switches and the on-resistance of the optimised system is reduced to half of the initial value (which has been 1.5 times the typical on-resistance). The rectifier losses could be reduced by 38 % at full-load operation and 25 % at half load. The total converter losses could be reduced by almost 9 % at half load and 16 % at full load. The full-load efficiency would increase from 98.9 % to 99.1 %.

The biggest advantage might again be that the number of switches could be reduced which is particularly advantageously for the hard-switched synchronous rectifier as the switching losses can be reduced. If only two switches were applied in parallel, 99.0 % efficiency could still be achieved at half load, however, the full-load losses would be increased by 22 %. It therefore would be more practical to implement 3 switches in parallel where the total converter losses are almost the same as for the optimised system (+3 %, from 54.2 W to 56.0 W).

Another possibility would be to leave the number of paralleled MOS-

Table 3.6: Rectifier losses for different improvement scenarios.

	Driving losses		Conduction losses	
	50 %	100 %	50 %	100 %
	load	load	load	load
Optimisation result	0.65 W	0.65 W	4.28 W	17.07 W
$1/2 R_{DS,on}$	0.65 W	0.65 W	2.14 W	8.54 W
$1/2 R_{DS,on}, n_{sw,s} = 2$	0.19 W	0.19 W	7.49 W	29.88 W
$1/2 R_{DS,on}, n_{sw,s} = 3$	0.28 W	0.28 W	4.99 W	19.92 W
	Switching losses		Rectifier losses	
	50 %	100 %	50 %	100 %
	load	load	load	load
Optimisation result	4.54 W	4.54 W	8.63 W	22.27 W
$1/2 R_{DS,on}$	4.54 W	4.54 W	6.49 W	13.73 W
$1/2 R_{DS,on}, n_{sw,s} = 2$	4.23 W	4.23 W	9.64 W	34.30 W
$1/2 R_{DS,on}, n_{sw,s} = 3$	3.86 W	3.86 W	7.42 W	24.06 W

FETs with the desired reduced on-resistance constant and the resulting high efficiency would allow a volume reduction of the magnetic components, still considering the efficiency-optimisation criteria as introduced in section 3.2. The resulting losses are summarised in **Tab. 3.6**.

Transformer Influence The transformer contributes the second-largest share of the losses of the efficiency-optimised system, cf. **Fig. 3.13** on page 206. The transformer itself is optimised in an inner optimisation process, i.e. the geometry of the core is varied until the minimum losses (sum of HF-winding and core losses) are found while the flux density and volume have to remain in a certain limit. The possibilities to reduce the winding losses by changing the material constraints are more or less small on a practical point of view, as copper would have to be replaced by a material with a higher conductivity, e.g. silver. The core losses could be reduced by changing the material, i.e. changing the B-H-hysteresis loop characteristics. The core losses are determined with the extended Steinmetz formula ((3.41) on page 194), where $k_{i,Tr}$, α_{Tr} and β_{Tr} are constants found by a curve-fitting. (The factor $k_{i,Tr}$ is calculated with (3.42), depending on the Steinmetz para-

Table 3.7: Transformer losses for different improvement scenarios.

	Core Losses		Winding losses	
	50 % load	100 % load	50 % load	100 % load
Optimisation result	6.75 W	6.88 W	3.12 W	12.52 W
$1/2 k_{Tr}$	3.38 W	3.44 W	3.12 W	12.52 W
$1/2 k_{Tr}, 2.7 b_{Tr}$	1.68 W	1.71 W	8.42 W	33.7 W
	Transformer losses		Volume	
	50 % load	100 % load		
Optimisation result	9.87 W	19.40 W	1.0 dm ³	
$1/2 k_{Tr}$	6.50 W	15.96 W	1.0 dm ³	
$1/2 k_{Tr}, 2.7 b_{Tr}$	10.10 W	35.41 W	0.47 dm ³	

meters k_{Tr} , α_{Tr} and β_{Tr} .) The values of α_{Tr} and β_{Tr} are determining the frequency behaviour of the core-loss value. The proportionality factor k_{Tr} is changed for illustration purposes in the following paragraph.

If the proportionality factor k_{Tr} could be halved, the transformer losses at half load would decrease by 34 % from 9.9 W to 6.50 W and the transformer losses at full load could be reduced from 19.4 W to 16.0 W (18 % decrease), as shown in **Tab. 3.7**. The resulting efficiency could be increased to $\eta = 99.2\%$ at half load.

The possibility of reducing the volume of the magnetic component could be of greater interest. If the winding window size would be reduced by 63 % the resulting volume would be decreased by 53 % from 1 dm³ to 0.47 dm³. Even though the core- and winding losses are not optimal in terms of the defined optimisation criteria, the efficiency would be still 99 % at half load. As the core volume is decreased, the core losses are further decreased to 1.68 W at half load and 1.71 W at full load, respectively. The resulting winding losses, however, are increased (because of the smaller copper cross-sectional area). This results in higher transformer losses (16 W more compared to the original optimised design) especially at full load. The resulting losses are summarised in **Tab. 3.7**.

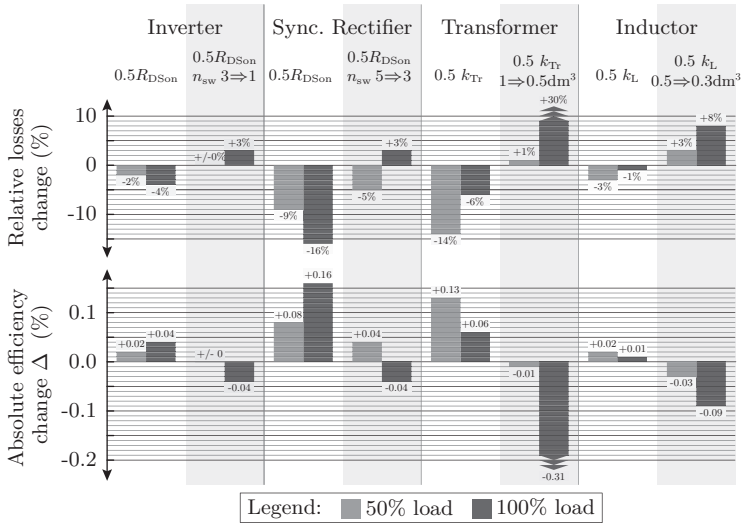


Figure 3.24: Summary of the presented influences of changing material specifications for the converter system performance.

Output-Inductor Influence The losses in the output inductor have only a minor influence on the total converter system losses. As the inductor-current ripple is only small, the passed-through B-H-loop is only small, which results in low core losses. At full load the core losses are 629 mW which is less than 1.2 % of the total system losses. The reduction of the Steinmetz-parameter k_L would therefore not result in a significant change.

If the constant factor k_L could be halved the resulting inductor losses at half load could be reduced by 36 % from 1.7 W to 1.1 W. However, the volume could again be drastically reduced from 0.5 dm^3 to less than 0.3 dm^3 , if the winding-window-size b_L would be reduced by 55 %. The resulting half-load efficiency would still be 99 %.

The resulting influences explained in the four preceding paragraphs above are summarised in **Fig. 3.24**.

4

Model Sensitivity

The analytical models applied in the design procedures for the power-density- and efficiency-optimised telecom DC-DC converter systems in chapter 2 and chapter 3 feature a good compromise between performance-modelling accuracy and computation time. Nevertheless, the analytical modelling is complex and time-consuming; moreover, the total computation time for calculating, for example, the efficiency-optimised system in chapter 3, is several days¹, even though the number of free design parameter has been reduced. A possible reduction of the model complexity would permit a reduction in both the computation time and the time-consuming modelling.

This chapter is dedicated to the investigation of the influence of the model's accuracy on the resulting optimised system performance. The evaluation is based on an efficiency-optimised reference-system as shown in section 4.1. The influence of the optimisation criterion on the performance is discussed in section 4.2. The model accuracy required is investigated in section 4.3, where the complexity of the model is reduced in steps and the corresponding influence on the optimised design determined.

The essence of this chapter has been published in [203].

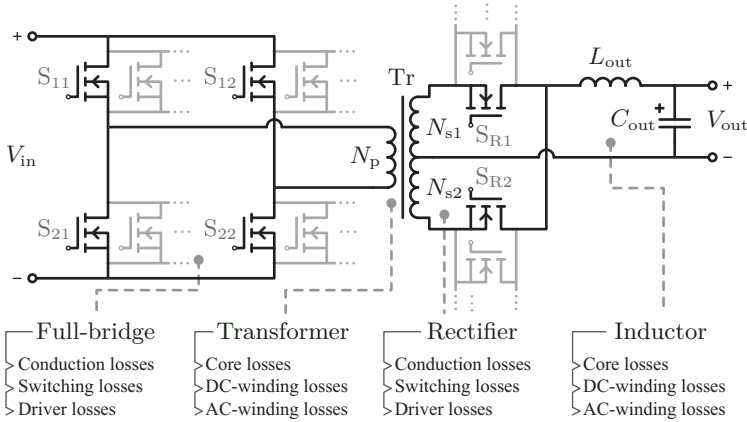


Figure 4.1: Schematic of the phase-shift PWM converter with centre-tapped secondary winding transformer and LC-output filter. The main determined losses of the reference system are illustrated.

4.1 A Compact Efficiency-Optimised System

The phase-shift PWM DC-DC converter with centre-tapped secondary winding transformer and LC-output filter as shown in **Fig. 4.1** is taken as basis for the investigations in this chapter. The analytical loss models, summarised in section 3.3, have been applied in the efficiency-design-procedure as introduced in section 3.2. The corresponding main losses in the semiconductor devices and magnetic components, determined during the calculation of the optimal design, are illustrated in **Fig. 4.1**. The fixed parameters for the converter system are mostly taken over from the efficiency-optimised system shown in section 3.4, cf. **Tab. 3.1** on page 203. The inverter MOSFETs from STMicroelectronics, however, have been replaced by Infineon CoolMOS™ of type IPW60R041C6 and, for a more compact design, the transformer volume (bounding box) has been limited to 0.5 dm^3 (31 in^3) and the inductor volume limited to 0.3 dm^3 (18 in^3). The applied core materials and the corresponding flux-density limitations remain (transformer: ferrite N87, $B_{\max, \text{Tr}} \leq 300 \text{ mT}$; inductor: Metglas® 2605SA1, $B_{\max, \text{L}} \leq 1.2 \text{ T}$).

¹The calculations have been performed on a 64-Bit machine with two Intel® Xeon® E5620 (quad-core) 2.4 GHz processors and 64 GB RAM. Seven of the eight available cores have been used in parallel for the computations.

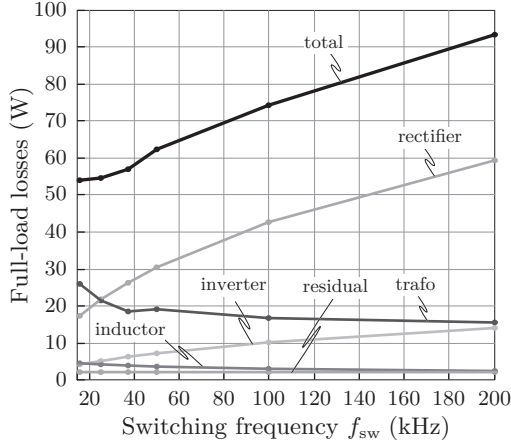


Figure 4.2: Full-load losses of the full-load optimised chapter-4-reference system in dependency of the switching frequency.

The objective of the design procedure was initially efficiency maximisation considering only the full-load operation, contrary to the optimisation criterion as shown in section 3.2² (a penalty function for the efficiency deviations for the load range from 10 % to 100 % of the rated output power). The losses in dependency of the frequency are illustrated in **Fig. 4.2**. The optimum switching frequency can, in the same way as for the load-range-optimised system in chapter 3, be found at the lowest-considered frequency (slightly above the audible frequency). However, the total-losses only slightly up to a switching frequency of 50 kHz. The transformer contributes with the highest share to the total full-load losses in the low-frequency band, caused mainly by the winding losses due to the flux-density-limitation and the minimum cross-section area of the core³ required in consequence. If the volume would be further limited, the optimal switching frequency would be shifted to higher values. The HF-winding-losses due to the skin and proximity effect influence the transformer losses for higher frequencies so that the losses increase again (not shown in **Fig. 4.2**).

²In the next section this optimisation goal is compared with the penalty function applied in section 3.2 and a further single-objective optimisation for half load.

³The resulting maximum flux density is approximately $B_{max} \approx 170$ mT at full-load operation.

The above considerations apply similarly to the output inductor, however, the HF-winding losses are almost negligible and the core losses⁴ are relatively small as the maximum peak-to-peak output current ripple is limited to 10 % of the DC-output current, remaining the winding losses due to the DC-resistance as dominant component. The share on the total system losses is below 10 % in the considered load range and the full-load inductor losses are only approx. 4.5 W, which would allow further volume reductions without the necessity of advanced cooling methods⁵.

The inverter MOSFETs are supposed to operate with zero-voltage switching and therefore, the switching losses are negligible over a wide load-range, but the driving losses are frequency-dependent causing the overall inverter full-load losses to increase marginally with increasing frequency.

The MOSFETs applied in the synchronous rectifier are hard-switched and the switching losses are significantly contributing to the total converter losses. As a result, losses in the rectifier increase sharply with increasing frequency so that, at higher frequencies, the rectifier losses become dominant. The residual losses are almost constant over the entire frequency range as they are influenced mainly by the auxiliary supply, measurement and control electronics, and the comparatively small frequency-dependent output capacitor losses. As the rectifier losses become dominant at higher frequencies, the total converter losses at full load always increase with increasing frequency, as shown in **Fig. 4.2**. Therefore, the minimum losses and/or highest efficiency are achieved at the lowest switching frequency⁶ for the specified volume limits.

The highest efficiency with the reference system shown here is obtained at full load as a consequence of the selected optimisation criterion. The load-dependent efficiency curve is illustrated in **Fig. 4.4**, together with the results for different optimisation objectives as shown in section 4.2. A peak efficiency of at least 98.9 % is achieved at full load, even though the limiting volumes of the magnetic components have been halved compared to the 99-%-efficient system shown in chapter 3. At half load, the efficiency is 98.8 % and the minimum efficiency is 95.1 % at

⁴The maximum flux-density resulting for the optimised core is small, i.e. $B_{\max} \approx 270$ mT at full-load operation – far below the specified limit.

⁵However, the resulting higher inductor losses would have to be accepted.

⁶The resulting converter design parameter values are summarised in table **Tab. 4.1** in section 4.2 and compared with the parameters resulting from the load-range and half-load-optimised system.

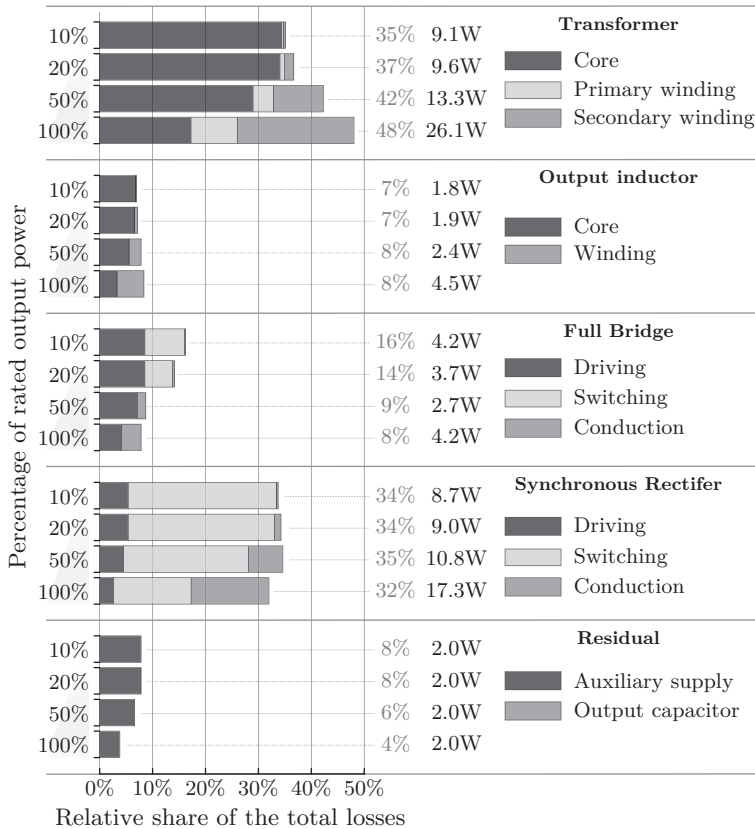


Figure 4.3: Losses distribution of the full-load-optimised reference system.

10% load. The efficiency of the full-load-optimised system far exceeds the Energy Star® requirements for computer servers over the entire load range.

A breakdown of the losses by the converter components and for different load levels of the full-load-optimised reference system is illustrated in **Fig. 4.3**. The synchronous-rectifier MOSFETs and the transformer together account for the largest loss fraction, being approx. 70-80% of the total losses across the entire load range. At full load (for which the converter has been optimised) the frequency depend-

ent losses are almost equal to the non-frequency dependent losses. Although this results in almost 99 % efficiency at full load, at lower loads the frequency-dependent losses result in a significantly lower efficiency, especially below 50 % load. In the magnetic components, core losses remain large at lower loads whereas the winding losses greatly decrease.

The distribution-shift of the losses for the magnetic devices (winding losses at high load \Rightarrow core losses at low load) and further the distribution-shift of the semiconductors (conduction losses at high load \Rightarrow switching losses at low load) as discussed in section 3.6 can be seen for this full-load-optimised system as well.

A large number of MOSFETs is paralleled to minimise the semiconductor conduction losses at full load: seven MOSFETs are employed for each full-bridge switch, and fifteen MOSFETs for each rectifier switch. As a result of the enlarged parasitic output capacitance of the MOSFETs, ZVS no longer occurs below 50 % load in the inverter switches and this results in significant switching losses, which combined with the driver losses cause the total full-bridge losses to be the same at 10 % load as at 100 % load. The share of the inverter losses doubles and the efficiency decrease from 100 % to 10 % load.

Similarly, the losses in the rectifier MOSFETs are completely unbalanced at low loads, i.e. the switching losses greatly exceed the conduction losses. The residual losses, mostly caused by the auxiliary supply, are essentially constant over the entire load range, which results in a more severe impact on the efficiency at low loads than at higher loads.

4.2 Influence of the Optimisation Goal

Depending on the environment in which the converter is operated, the design objective might differ, for example the converter might be required to operate mainly at 50 % load, and should therefore have the maximum efficiency at this load point. Alternatively, a required minimum efficiency may be specified for several load points, as for example proposed in the Energy Star[®] requirements for computer servers as applied in chapter 3. The influence of the optimisation goal on the converter design is analysed in this section. Three systems are compared: system ① is the full-load-optimised system described in section 4.1; system ② is a converter optimised for peak efficiency at half load; and system ③ is a converter optimised for part-load efficiency according to Energy Star[®] with the optimisation criterion explained in section 3.2.

Table 4.1: Comparison of resulting design parameter values. (Denomination of the geometry parameters as defined in **Fig. 3.9** on page 194).

Design parameter	Optimisation objective		
	Ⓐ full load	Ⓑ half load	Ⓒ part load
Switching frequency	16.0 kHz	16.0 kHz	16.0 kHz
Paralleled full-bridge switches	7	3	3
Paralleled sync. rectifier switches	15	8	6
Transformer turns $N_p : N_s$	32 : 5	32 : 5	32 : 5
Leakage inductance L_σ	6.0 μH	6.0 μH	6.0 μH
Leg thickness a	22 mm	22 mm	22 mm
Window width b	105 mm	105 mm	105 mm
Core thickness c	42 mm	42 mm	42 mm
Primary winding foil thickness	60 μm	59 μm	59 μm
Secondary winding foil thickness	179 μm	178 μm	178 μm
Output inductor turns N_L	8	7	7
Inductance L_{out}	31 μH	52 μH	62 μH
Leg thickness a	16 mm	19 mm	19 mm
Window width b	140 mm	95 mm	83 mm
Core thickness c	24 mm	34 mm	38 mm
Winding foil thickness	500 μm	500 μm	500 μm
Air gap length l_σ	1.03 mm	0.79 mm	0.82 mm

It should be noted that the inner optimisation loops for the transformer and inductor, cf. **Fig. 3.5** on page 175, always consider full load only in order to reduce the computation time and to meet the full-load constraints. The transformer geometry parameters in the three systems are nearly identical for this reason. The resulting design parameters for the three different designs are summarised in **Tab. 4.1**.

The resultant part-load efficiencies of the three different converter designs are compared in **Fig. 4.4**. According to the defined optimisation criteria, system Ⓐ has the highest efficiency at full load, 98.9%, compared to 98.8% for Ⓑ and 98.7% for Ⓒ. At half load, systems

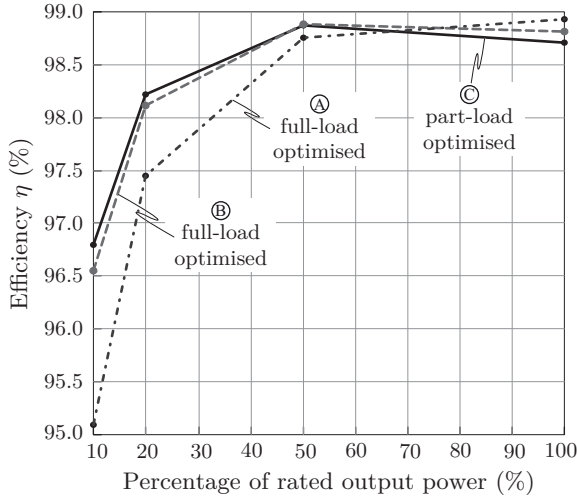


Figure 4.4: Efficiency as function of the output power for full-load-optimised ①, half-load-optimised ② and part-load-optimised ③ converter system.

② and ③ achieve 98.9 % efficiency, while system ① is slightly lower at 98.8 %. Because the part-load efficiency is included in the optimisation criterion of system ③, the efficiency at low loads is slightly higher as for system ②, while the efficiency of ① is significantly lower: 95.1 % at 10 % load compared to 96.6 % for ② and 96.8 % for ③, and 97.5 % at 20 % load compared to 98.1 % for ② and 98.2 % for system ③. The similar behaviour of the half-load-optimised system ② and load-range-optimised system ③ can be explained by the fact that the part-load reference used for ③ places the peak efficiency at 50 % load, which makes the optimisation objective for ③ and ② comparable.

The loss distribution for the three designs is illustrated in **Fig. 4.5** exemplary at 10 % load and 100 % load. The loss distributions of the part-load-optimised and the half-load-optimised systems (③ and ②) are almost similar, in correspondence with the two resulting designs shown in **Tab. 4.1**. As the transformer is nearly identical for the systems, the transformer losses are also very similar, but their share of the total losses differs primarily due to the different number of paralleled switches used in each system. Compared to system ①, systems ② and ③ both

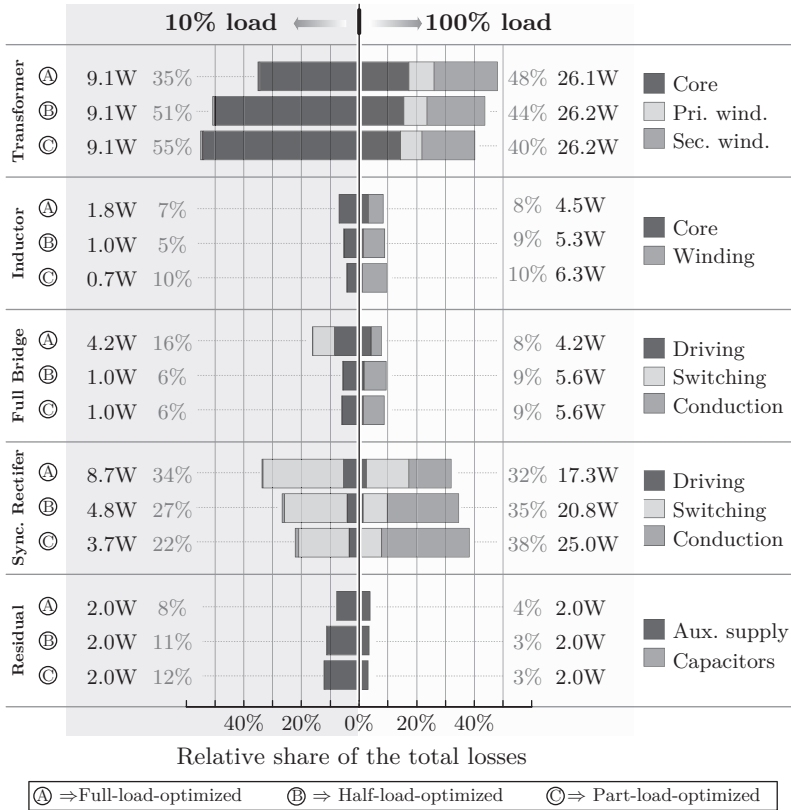


Figure 4.5: Losses distribution for full-load-optimised Ⓐ, half-load-optimised Ⓑ and part-load-optimised Ⓒ converter system.

have approximately half as many paralleled switches in the inverter stage and synchronous rectifier. The conduction and switching losses for the half-load- and part-load-optimised systems are balanced at a lower load point, where the conduction losses are lower, however, the conduction losses are higher at full load (in contrast to the full-load-optimised system). On the other hand, switching and driving losses are noticeably lower in systems Ⓑ and Ⓒ than in system Ⓐ because less MOSFETs have been paralleled.

The HF-winding losses and core losses in the inductor are influenced

by the output current-ripple; accordingly the optimised ripple factor k_I is rather small and the winding losses therefore mostly dependent on the DC-component of the output current. In the high-output-power range, the inductor losses are mainly determined by the winding losses, whereas the core losses dominate at lower loads. As a consequence the optimisation algorithm minimises the output current ripple (increasing the inductance) in the half-load and part-load-optimised systems to favour the core-loss-reduction more than the winding losses. As the winding losses dominate the losses in the upper load-range, the full-load optimisation allows a larger inductor current ripple, resulting in the smaller inductance given in **Tab. 4.1**. As a result, the inductor losses are smaller at full load for the full-load-optimised system compared to the other two systems, but larger at lower loads, cf. **Fig. 4.5**.

The three examples discussed above show that the choice of the optimisation criterion has a significant impact on the resulting design and its loss distribution. Nevertheless, a simple design goal such as the peak efficiency at full load delivers a high efficiency ($>95\%$) over the entire load range greatly fulfilling the Energy Star[®] requirement for computer servers.

4.3 Reduction of the Model Complexity

The reference system in this section is again the full-load optimised system from section 4.1 as the single-load optimisation inherently allows a simpler interpretation of the design parameters and therefore reduces the validation to the essential aspect of this section, the model sensitivity. The reference system is calculated based on comprehensive / detailed converter and component models. In order to gain insight into the robustness of the optimisation process, i.e. to understand which level of detail of modelling is required for achieving the (almost) exact optimal design parameter values, the model complexity has been reduced step by step and the optimisation process has been run with the simplified models. The resulting optimised design parameter values, such as core geometry of the magnetic components and number of paralleled semi-conductors, have permitted a re-run of the single calculation-loop with the comprehensive models as illustrated in **Fig. 4.6**. The re-calculated performance of the optimised systems using different Model Complexity Reduction Levels (MCRL) is compared with the system performance of the reference system. This is done for each MCRL in order to determine

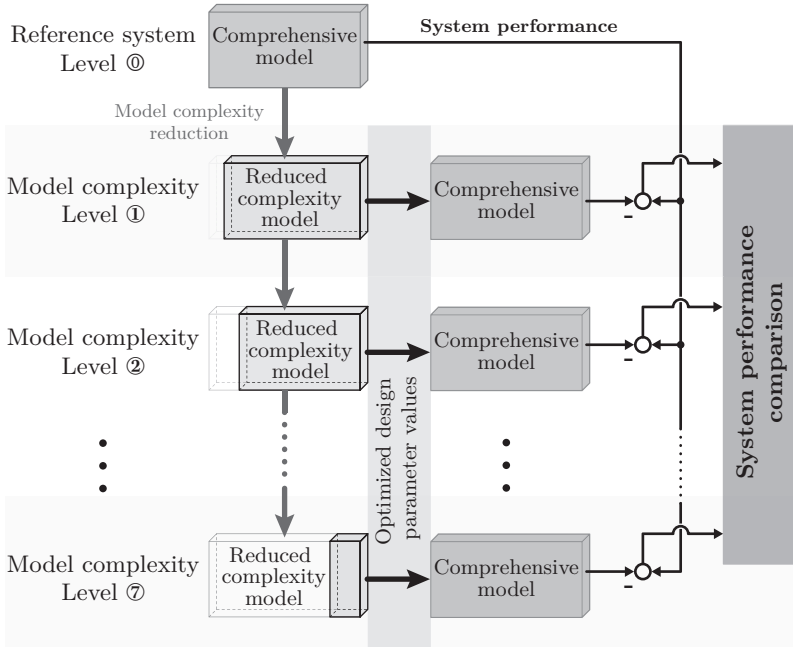


Figure 4.6: Illustration of the model reduction procedure, showing the optimisation performed with the reduced models, the accurate calculation of the losses of the resulting systems with comprehensive models, and the comparison of the resulting performance.

the difference in the performance space and identify the potential for model simplifications.

The overview of the applied MCRLs is given in **Tab. 4.2**. For every MCRL one of the loss models described in section 3.3 has been simplified or omitted. In the following paragraphs the discussion for each level is presented based on the performance comparison with respect to the reference system from section 4.1. The efficiency and loss values given in the following correspond to the full-load operation if not stated differently, for sake of clarity.

Model Complexity Reduction Level (MCRL) ① In the reference system (① in table 4.2) the currents in the primary and secondary windings are approximated up to the 30th harmonic in order to accur-

Table 4.2: Model complexity reduction Levels (MCRL)

Loss-model	Model complexity reduction Level							
	①	①	②	③	④	⑤	⑥	⑦
Transformer HF-winding	•							
1 st harmonic winding	•	•						
DC-winding	•	•	•	•	•	•	•	•
Accurate core losses	•	•	•					
Inductor HF-winding	•	•	•	•				
DC-winding	•	•	•	•	•	•	•	•
Accurate core losses	•	•	•	•	•			
Full bridge Driving	•	•	•	•	•	•	•	•
Conduction	•	•	•	•	•	•	•	•
Switching	•	•	•	•	•	•		
Sync. Rectifier Driving	•	•	•	•	•	•	•	•
Conduction	•	•	•	•	•	•	•	•
Switching	•	•	•	•	•	•	•	

ately determine the High-Frequency (HF) winding losses. In the first MCRL (①) only the fundamental frequency is considered. The relative deviation of the primary and secondary winding losses between the reference system and the optimised MCRL ① system is 18 % and 13 %, respectively. However, the design parameter values of the transformer change only marginally, e.g. the core geometry parameters change by only $\pm 2\text{-}4\%$ and thus the resulting performance of the reduced-model-complexity-optimised system ① is almost the same - the absolute total converter losses increase by less than 200 mW.

MCRL ② Calculating only the first harmonic does not result in a significant decrease of computational effort compared to calculating several harmonics, since a Fourier analysis must be performed in either case. Moreover, considering only the first harmonic results in a relatively high error of the calculated system performance for this topology, which operates with an almost rectangular primary current waveform, although the resulting optimised design parameters are almost similar, as shown

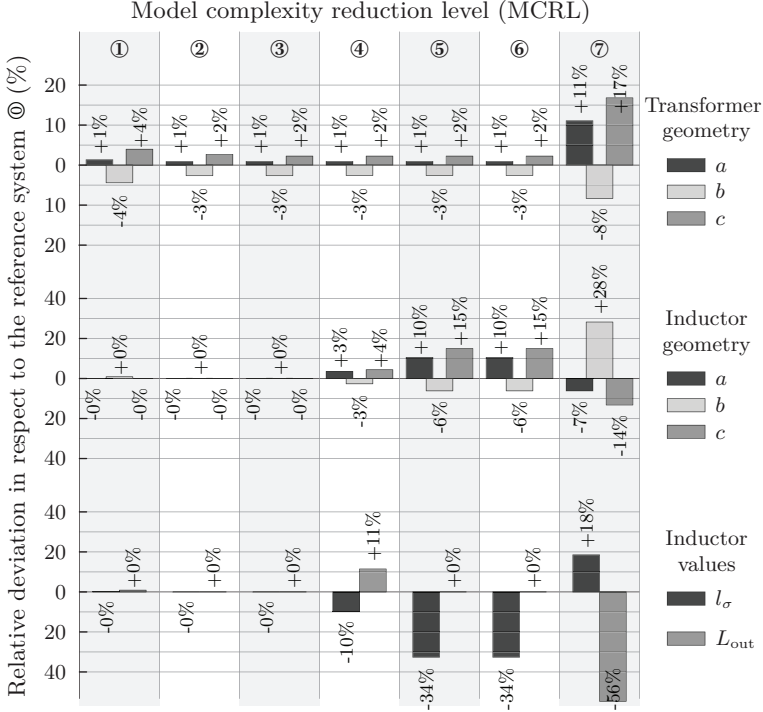


Figure 4.7: Relative deviation of the design parameter values resulting from the reduced-model-complexity-optimisation in respect to the design parameter values of the reference system.

above. In the second complexity reduction step MCRL ②, only the RMS-value of the current and the DC-resistance are considered.

The calculated total converter losses are just 4 % lower (for MCRL-①-modelling 7 %) and therefore the influence on the design parameter values is also low ($\pm 1\text{-}3\%$), cf. **Fig. 4.7**. Furthermore, compared to the reference system, the reduced-model-complexity-optimised system again results in a negligible performance decline - less than 100 mW of additional losses.

MCRL ③ The transformer core losses are calculated with Sullivan’s extended Steinmetz formula for non-sinusoidal waveforms (3.41) (page 194) as proposed in [176]. In MCRL ③, only the simple Steinmetz

formula is considered for calculating the core-losses per volume

$$P_{c,v} = k f_{sw}^{\alpha} \hat{B}^{\beta} \quad (4.1)$$

where k , α and β are the Steinmetz parameters obtained from the data sheets, f_{sw} is the switching frequency and \hat{B} is the amplitude of the flux density.

Compared to MCRL ② the change of the calculated core losses is negligible (approx. -0.5 %) and accordingly the resulting design parameter values and converter system performance remain unchanged too.

MCRL ④ Similar to the transformer-MCRL ②, only DC-losses are considered in the MCRL ④ inductor windings. Even though the HF-component of the output inductor current is small compared to the DC-component and the share of the winding losses in the total losses is only 5 %, cf. **Fig. 4.3**, the resulting design parameter values of the converter change. As shown in **Fig. 4.7** the inductor geometry parameter values change by $\pm 3\text{-}4\%$ and the calculated optimal output inductance L_{out} is 11 % higher. The interdependency of the design parameters can be pointed out at this MCRL as well, as the number of paralleled MOSFETs used is reduced from seven to six for the inverter stage and from 15 to 14 for the rectifier stage due to the decreased RMS-values of the currents in the devices.

The decline in the actual system efficiency for the MCRL ④ is negligible compared to the reference system because of the small share on the system losses.

MCRL ⑤ The core losses in the inductor are small (less than 3 W at full load) as the flux ripple is kept small by the optimisation algorithm discussed in section 4.2. In MCRL ⑤, the core losses are calculated with the simple Steinmetz formula (4.1) for sinusoidal current waveforms, further neglecting the DC-offset of the flux. The relative error of the calculated core losses is high (approx. 54 %,) but the absolute error is less than 1 W. The resulting optimised design parameter values, however, are changed again: the optimum inductance is almost the same as for the reference system and the cross-sectional area determined by the core geometry parameters a and c is increased as shown in **Fig. 4.7**.

Again, because of the comparatively small share of the total system losses, the resulting system performance is only minimally worse, even though the core losses are increased by $\approx 5\%$.

MCRL ⑥ The switching losses of the inverter MOSFETs in the converter are commonly negligible at full load as there is enough energy stored in the leakage inductance to fulfil the zero-voltage-switching condition. Thus, for a full-load optimisation, the resulting system performance does not change if the calculation of the full-bridge switching losses is omitted, as validated for MCRL ⑥. The only limitation for the number of paralleled MOSFETs $n_{sw,p}$ are the (frequency-dependent) losses in the gate-driver, which are contrary to the conduction losses linearly increasing with $n_{sw,p}$. Thus, the driving losses cannot be neglected because the number of paralleled switches would be unlimited as the effective on-resistance and therefore the total conduction losses would decrease with every switch added in parallel.

Note that the resulting system performance for the part-load optimisation would be much more affected by this model-complexity reduction as the number of switches would be increased resulting in high switching losses at part load as explained in section 4.2.

MCRL ⑦ Unlike the inverter switches, the synchronous rectifier MOSFETs are switched hard at any load condition. Neglecting the switching losses of the rectifier switches, as is done in MCRL ⑦, not only has a large influence on the accuracy of the loss calculation but also on the system performance.

The frequency-dependence of the rectifier switching losses is the main force in the optimisation, resulting in the low switching frequency ($f_{sw}=16\text{ kHz}$) of the optimised system. By omitting the SR-switching losses, the resulting optimal switching frequency is higher ($f_{sw}=37.5\text{ kHz}$) as the core losses in the magnetic components are lower at higher frequencies as shown in **Fig. 4.2**. Due to the interdependency of the design parameter values, the geometry parameters are changed by $\pm 8.17\%$ for the transformer and $\pm 7.28\%$ for the output inductor; the inductance is reduced by more than 55 %.

The number of paralleled inverter switches is reduced from seven to four because of the increased driving losses due to the higher switching frequency. This results in increased conduction losses. In contrast the number of paralleled synchronous-rectifier MOSFETs is now only limited by the driving losses and thus results in an increase from 15 to the unrealistic value of 23. The absolute deviation of the calculated total losses due to the reduced complexity model is more than 18 W (a decrease of approx. 34 % in calculated losses).

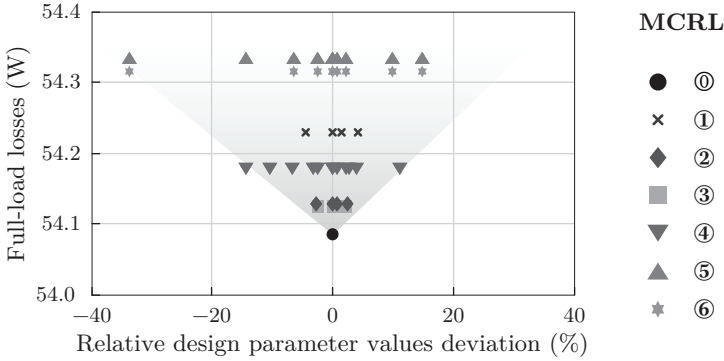


Figure 4.8: Influence of the deviation of the design parameter values resulting from the model complexity reduction on the full-load losses. (Note that MCRL ⑦ is omitted for the sake of clarity as the deviation and the resulting loss is much higher.)

Compared to the reference system, the calculated system performance of the reduced-model-complexity-optimised system, recalculated with the complete models, is significantly lower. The resulting total losses are increased from 54 W to 68 W (25 % higher) and the efficiency is decreased from 98.9 % to 98.6 %. Even more pronounced is the decrease of the efficiency at 10 % load, from 95.1 % to 91.9 %, i.e. the converter losses increase by more than 70 %.

A further model complexity reduction for the synchronous rectifier, i.e. neglecting driving and/or conduction losses, would prevent a sensible optimisation process.

The full-load losses, determined with the complete analytical models, based on the design parameters resulting from the reduced-model-complexity-optimisations, as function of the deviations of the design parameter from the reference design, is illustrated in **Fig. 4.8**⁷. Every point in the figure presents a design parameter value such as the number of paralleled MOSFETs, core geometry parameters or the switching frequency. In principle, the higher the variation of the design parameter values the higher the distance from the reference-system optimum (MCRL ⑦ in **Fig. 4.8**). The absolute deviation of the full-load losses

⁷The losses resulting from the MCRL ⑦ are not shown in **Fig. 4.8** because of the high deviations as discussed above. However, the principal trend of full-load losses in dependency of the deviation shown in **Fig. 4.8** holds also for MCRL ⑦.

for the MCRL ① - ⑥ is small as presented above. A drastic change occurs when rectifier switching losses are neglected in MCRL ⑦.

It can be concluded, from the perspective of a design engineer, that despite the simplification of the analytical models still reasonable design parameter values are resulting, even though the determined system performance is incorrect. Nevertheless, a certain degree of engineering intuition and knowledge is necessary to identify the loss contributors with a minor influence, which can be therefore neglected. Moreover, the design process with simplified models is commonly further favoured by additional performance constraints such as cost, weight and power density, which limits for instance the maximum number of MOSFETs.

5

Conclusion - Optimal Design Spaces

Telecommunication power supplies have passed through the entire evolution of power electronic systems. After the merger of telecom facilities and data centres, and the communication-boom starting with the introduction of ISDN in the late 1980s, the main physical performance driver for power supplies development was initially the power density. Out of the necessity of requiring more and more space for the ICT-equipment, it has been made a virtue, because the highly-compact systems allow higher-efficiency cooling and therefore a reduction of the operation costs. The IT-industry has become an important global energy-consumer due to the expansion and broad provision of digital services in the 1990s and the rapid increase of computation and transmission speed ever since. The move of the performance driver towards efficient power supply equipment since the millennium is an ecological and economical reaction to the continuously increasing power demand.

The limits of the achievable power density and efficiency of DC-DC converters for telecom applications are evaluated in chapter 2 and chapter 3 applying design procedures based on comprehensive analytical converter models. The optimisation results are summarised and compared in section 5.1. The extension of the single-objective optimisation towards multi-objective design procedures is given as an outlook in section 5.2. In the conclusion of the thesis, possible future improvements for data-centres are summarised in section 5.3.

5.1 Power-Density- and Efficiency-Optimised Performance Spaces

The maximisation of system-power-density is discussed in chapter 2, using a series-parallel-resonant DC-DC converter and a phase-shift PWM DC-DC converter with current doubler rectifier as examples. The calculation of the maximum power density is based on comprehensive analytical electric, magnetic, and thermal models for the converters applied in automatic design procedures in order to determine the optimal design parameters. The magnetic components have been integrated using a single core for both converter designs, i.e. the series-resonant inductor has been integrated with the centre-tapped secondary winding transformer of the series-parallel-resonant converter (LCC) and the current-doubler inductors and the transformer of the phase-shift PWM converter (CDR) are integrated based on a single core. The optimised converter system features an almost similar performance even though the operating principles are different (resonant vs. phase-shift PWM). The LCC-resonant-converter prototype features a power density of 10.4 kWdm^{-3} with a copper-based cooling system. In [204] the cooling system has been further investigated and it could be shown that the converter volume of an aluminium-based cooling system would be increased by only 2.6 %, i.e. the power density of the converter system decreases from 10.4 kWdm^{-3} to 10.15 kWdm^{-3} (the volume of the aluminium cooling system itself is approx. 5.3 % higher). The potential for a further increase of the power density is given, at least to a small degree, as the net-component volume is much smaller¹. A more drastic increase of the power density is possible, if the cooling concept is changed from the applied advanced forced-air cooling method to water cooling. Based on the optimal design values of the LCC-resonant-converter prototype, the power density could be increased by 63 % from 10.4 kWdm^{-3} to approx. 17 kWdm^{-3} .

Compared to the copper-based LCC-resonant converter, the prototype of the phase-shift PWM converter with current doubler rectifier exhibits an approximately 15 % higher volume. This handicap is reduced if the prototype heat sinks would be manufactured from copper and a custom-made core with the geometry-parameters resulting from

¹The continuous improvements of a half-bridge LLC-resonant converter prototype, last but not least enabled by the improved integration of magnetic components, results for instance in 10.8 kWdm^{-3} , starting from 1.7 kWdm^{-3} as shown in [84].

the design procedure would be applied similar to the LCC-resonant converter. The measured efficiency of both converter systems is around 95 %.

Because of the changing driving forces for the development of telecom power supplies, efficiency became the most-important physical performance index. Identification of the technical limit for this performance index has been one of the major parts of this thesis. The evaluation approach has been adopted from the power-density-optimised system. Based on comprehensive analytical models of the employed components the system performance can be evaluated within an automatic design procedure. The optimisation criteria is defined according to the Energy Star® requirements for computer servers over the load-range between 10 % and 100 %, and the aspired efficiency has been 99 % at half load. This high aim of 99 % has been reached for the investigated standard topology, a phase-shift PWM converter with centre-tapped secondary winding transformer and LC-output filter. The high efficiency is borne by the volume increase of the magnetic components, as the total power loss of the state-of-the-art semiconductor devices that have been considered in the course of the design exhibits a minimum defined by the trade-off between conduction, switching and gate-drive losses. The resulting power density of 1.9 kWdm^{-3} can still keep up with the power density of modern power supplies; however, the resulting system volume is approximately five times higher than for the power-density-optimised system volumes. The system volume can be decreased by limiting the output voltage range; e.g. if just the nominal output voltage of 50 V is considered instead of the voltage range 46 V to 56 V the power density can already be increased by 26 % from 1.9 kWdm^{-3} to approximately 2.4 kWdm^{-3} . A prototype has been designed based on standard components to validate the applied loss models. The prototype with a power density of 2.2 kWdm^{-3} features an efficiency of 98.5 %, which can be increased up to 98.9 % by applying latest technology inverter MOSFETs and a different winding arrangement.

The parameter-sensitivity analysis in chapter 3.6 shows that improvements of the semiconductors applied in the synchronous rectifier and of the core material of the transformer in particular would allow a further increase of the efficiency and/or would allow to reduce the volume of the magnetic components and the number of semiconductors.

The relative loss and volume distributions of the optimised te-

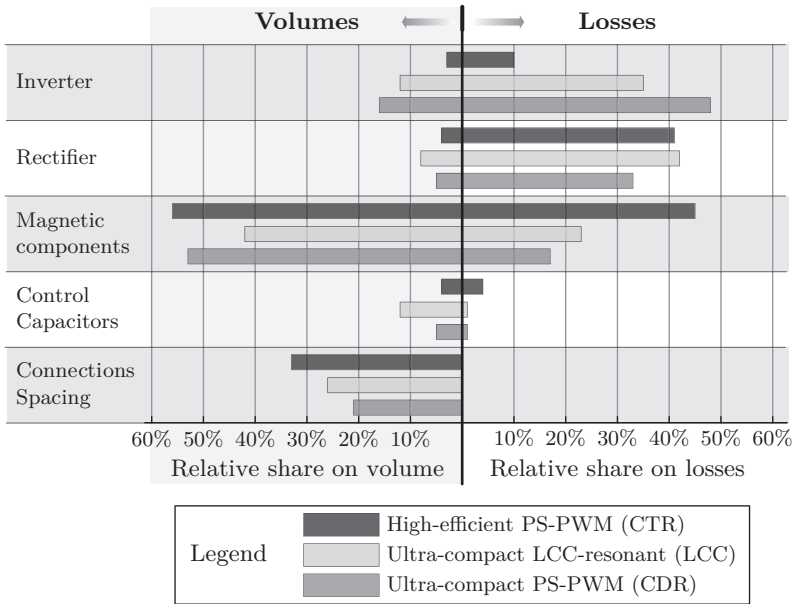


Figure 5.1: Comparison of the relative loss and volume distribution of the high-power-density LCC-resonant (LCC) and phase-shift PWM DC-DC converter with integrated current doubler (CDR) and the high-efficiency phase-shift PWM converter with LC-output filter (CTR).

lecom DC-DC power supplies are summarised in **Fig. 5.1**. Due to the advances achieved for the MOSFETs applied in the inverter stage and the possibility of decreasing the conduction losses by paralleling of switches the relative share of the inverter on the total losses and the volume could be decreased for the high-efficiency converter. The relative loss and volume distributions of the rectifier stage are almost equal for the ultra-compact and the high-efficiency system. The volume share of the magnetic components (integrated series inductor for the series-parallel-resonant converter (LCC), integrated Current Doubler inductors (CDR), discrete output inductor and transformer for the high-efficiency converter) is also almost equal, but the loss-share of the magnetic components for the high-efficiency system is almost doubled, whereas the loss-share of the inverter is proportionally de-

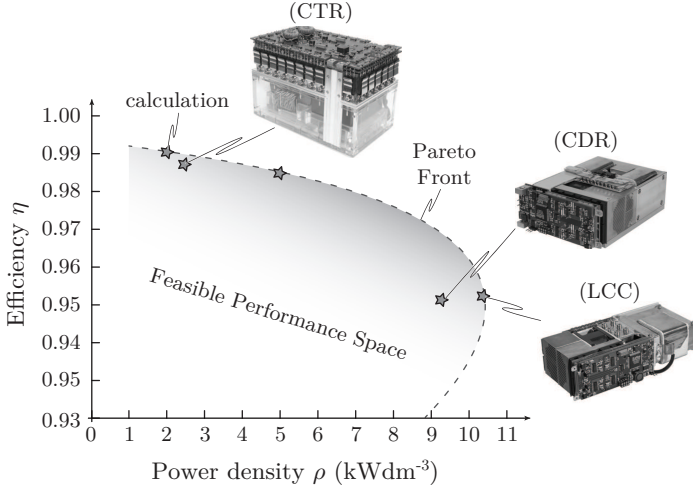


Figure 5.2: Performance space for optimised telecom DC-DC converter systems.

creased. The volume-share of the control and capacitors is higher for the LCC-resonant converter as a capacitive output filter is applied and (to some extent) also due to the resonant tank capacitors. The relative losses in the control of the highly efficient converter have greater influence on the converter performance. The resulting relative share of the volume required for the spacing of components and connections is slightly higher for the highly efficient converter, mainly due to the bulky wiring required to decrease the resistance. Nevertheless, the required connection space is comparable for both, i.e. the high-efficiency and the high-power-density system, and results in a relatively high share of one-fourth to one-third of the total volume.

In conclusion, the investigations of high-power-density and highly efficient systems revealed that with a reasonable effort it is possible to construct a 99-%-efficient DC-DC converter with a power density of approximately 2 kWdm^{-3} or an ultra-compact converter system with a power density of 10 kWdm^{-3} and an efficiency of approximately 95 %. These performance points have been plotted in the power-density – efficiency plane in **Fig. 5.2**². The connection line between the optimised

²A further prototype system is plotted with a power density of 5 kWdm^{-3} and

converter systems resulting from designs with varying weights for power density and efficiency is called a Pareto Front and discussed in the next section.

Considering the complete Power Supply Unit (PSU), made up of an AC-DC rectifier with power factor correction and the DC-DC converter system, it is possible to construct a system with a power density from 2.5 to 3 kWdm⁻³ and 97 % overall system efficiency with a reasonable realisation-effort. Converter designs beyond this performance are hardly possible with state-of-the-art components and standard topologies. Moreover, in the near future cost optimisation will take in an even higher influence as performance driver on the development of modern power supplies while maintaining the power density and efficiency at a high level.

5.2 Multi-Objective Pareto-Optimal Designs

The power-density limit for two DC-DC converter systems is introduced in chapter 2 whilst it is shown in chapter 3 that an efficiency of 99 % can be reached with a still reasonable effort. The volume for the magnetic components has been limited in the optimisation process as the magnetic component losses modelled are decreasing with increasing volume³. As a consequence, the optimised efficiency resulting is reduced if the volume limit for the magnetic components is aggravated, as shown for example for the highly efficient reference system in chapter 4. There is an efficiency-optimum for each volume limit and these optimal points, plotted in the power-density ρ – efficiency η plane define the boundary of the feasible performance space – the Pareto Front, as shown in **Fig. 5.2**.

The Pareto Front is generally obtained by varying the weights of the two considered performance indices⁴, in **Fig. 5.2** the weights for the power density and efficiency. The Pareto Front is commonly formed by the optimised η – ρ points of different converter topologies, such as shown by Kolar in [38] for AC-DC PFC systems, i.e. the Pareto Front is section

98.5 % efficiency which is not presented in the thesis.

³As a consequence, an infinite volume would result for the transformer and inductor from an efficiency optimisation if the volume would not be limited.

⁴In the optimisation shown with respect only to power density the weight for the power density $w_\rho = 1$ whereas the weight for the efficiency $w_\eta = 0$, and for the efficiency-optimisation the weights are inverted, $w_\rho = 0$ and $w_\eta = 1$.

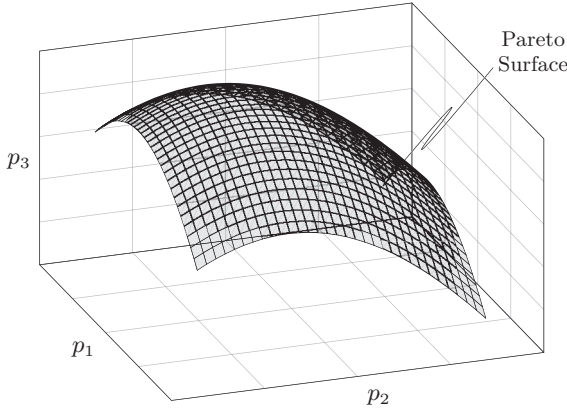


Figure 5.3: Principle diagram of the Pareto Surface, resulting from the optimisation considering three performance indices.

by section defined by the topology with the best local performance.

The identified performance limits, i.e. the Pareto Front and/or the identification of the feasible performance space is a powerful tool for OEMs to evaluate their position in the market and to define roadmaps for future developments as discussed in [9]. Moreover, combined with the sensitivity analysis, as for example presented in section 3.6, the crucial opportunities for performance improvements and therefore important research areas can be identified.

The optimisation process with respect to two performance indices described above, such as the power density and efficiency in **Fig. 5.2**, results in a two-dimensional Pareto Front. However, more than two performance indices are commonly relevant for practical applications; especially the system costs are a major performance driver. When considering a third performance index the performance-plane is extended to a three-dimensional feasible performance space and the Pareto Front is represented by a Pareto Surface, which determines the optimal converter designs with respect to the three performance indices p_1 , p_2 , and p_3 as illustrated in **Fig. 5.3**. In principle, the multi-objective optimisation can be extended by further performance indices such as weight per volume or reliability (MTBF). The applied design approach remains unchanged, in principle, only the corresponding analytical models have to be added and the aspired optimisation criteria have to be defined.

5.3 Improvements for Future Data Centres

The power supply unit is one major part of the data centre and contributes the highest share of the losses in the power supply chain, consisting of the uninterruptible power supply, the power distribution unit and the ICT-specific voltage regulation modules. The improvements in efficiency and power density of the power supply unit affect the entire data-centre efficiency in an even higher degree as the cooling effort can be reduced as discussed in section 1.3. The performance-optimisation-approach shown can be used for the other modules of the power supply chain and the data centre power consumption can therefore be further decreased.

The practical-reasonable efficiency limitations of the AC-DC rectifier and DC-DC converter are both approximately 99 % as is shown in [38] for the rectifier stage and in this thesis for the DC-DC converter. The combination of both high-efficiency power conversion stages in the power supply units would result in a total efficiency of approximately 98 %. This significant efficiency improvement is not least enabled by higher costs for the magnetic components and the applied semiconductors. Even though the increased hardware costs might be acceptable to the operator and the highly efficient power supply unit could be applied in data centres, the conceptual layout of the data centre power distribution must be considered as well. As an example, if a 98-%-efficient 5-kW power supply unit is applied and connected to the 3-phase mains⁵ with a 10 m long cable, utilised with less than half of the intended current of the European standard⁶, the losses in the cable are almost 20 W, i.e. one-fifth of the losses of the high-efficiency power supply unit⁷! In general, the power distribution has a major influence on the data centre performance. The move from classical AC-powered data centres to DC-powered data-centres can drastically increase the overall efficiency as discussed in section 1.3. Moreover, an “intelligent” load-distribution such that the distributed power supply chain operates in the efficiency maximum are challenges to future improvements.

⁵In the calculation the European 230 V-network with the corresponding small currents is assumed.

⁶Currents up to 15 A, require a 1.5-mm² wire cross-section [205], applied in a cable channel on a wall with 30 °C ambient temperature.

⁷If the standardised current density of 10 A mm⁻² according to [205] would be applied, the losses would be approx. 80 W in the forward and return path.

Above all improvements provided by the power electronics industry, the ecological sensibility and the purposeful employment of the available multimedia services are the responsibility of every end-user and this eventually determines the conservation of our limited natural resources.



Fundamental Frequency Analysis of the LCC-Resonant Converter

The fundamental frequency analysis of series-parallel-resonant LCC converters with centre-tapped secondary winding transformer and capacitive output filter is summarised in this section, which has been excluded in section 2.1 for brevity. An often-referenced and well-illustrated analysis of half-bridge resonant converters based on the first harmonic of the resonant current is introduced by Steigerwald in [87]. In this analysis, an equivalent resistance R_{AC} is calculated which is connected in parallel with the resonant tank resulting in an adequate correlation with the measurement results for a LC-output filter. If a capacitive output filter is applied a similar calculation will result in higher deviations because of the discontinuous rectifier current. In [147, 153], Ivensky suggested a fundamental-frequency analysis for parallel-resonant and series-parallel-resonant converters with C-output filter based on an equivalent RC-circuit. This analysis has been extended in [110, 148] for the special control method with zero-current switching in one bridge leg and zero-voltage switching in the other leg as illustrated in **Fig. A.2** (and further explained in section 2.1). The analysis introduced below follows the suggested calculations in [147, 148] which have been adapted and extended for the analysis with a centre-tapped secondary winding transformer and secondary-side-connected parallel capacitor C_p as illustrated in **Fig. A.1**.

The fundamental analysis below is based on the assumptions:

- Sinusoidal primary and secondary as side currents (i_{Ls} and $i_s = i_{s1} + i_{s2}$)

to half of the sum of the sinusoidal secondary side currents, $i_s = i_{s1} + i_{s2}$, which is equal to the transferred transformer primary side current $i_s = i'_p = n \cdot i_p$, with the transfer ratio $n = N_p/N_s$, i.e.

$$i_{Cp} = \frac{1}{2}i_s = \frac{n}{2}i_p = n_1i_p. \quad (\text{A.1})$$

The capacitor voltage is given with the assumed sinusoidal current for that interval as

$$\begin{aligned} v_{Cp}(\omega t) &= \frac{1}{\omega C_p} \cdot \int_0^{\omega t} \frac{\hat{I}_s}{2} \cdot \sin(\vartheta) d\vartheta \\ &= \frac{\hat{I}_s}{2\omega C_p} \cdot (1 - \cos(\omega t)) + v_{Cp}(\vartheta_0). \end{aligned} \quad (\text{A.2})$$

An expression for the peak-value \hat{I}_s of the capacitor current can be found with the starting condition $v_{Cp}(\omega t = \vartheta_0 = 0) = -2V_{\text{out}}$ and the capacitor voltage at the end of the interval $v_{Cp}(\omega t = \vartheta_1 = \pi - \theta) = 2V_{\text{out}}$,

$$\hat{I}_s = \frac{8V_{\text{out}}\omega C_p}{1 + \cos(\theta)} = \frac{8V_{\text{out}}\omega C_p}{2\cos^2\left(\frac{\theta}{2}\right)}, \quad (\text{A.3})$$

and the capacitor voltage for the interval $0 \leq \omega t \leq \pi - \theta$ results in

$$v_{Cp}(\omega t) = \frac{2V_{\text{out}}}{1 + \cos(\theta)} [(1 - \cos(\theta)) - 2\cos(\omega t)]. \quad (\text{A.4})$$

During the interval $\pi - \theta \leq \omega t \leq \pi$ the capacitor voltage is clamped to twice of the output voltage,

$$v_{Cp}(\omega t) = 2V_{\text{out}}.$$

The **conduction angel** θ can be obtained by analysing the output current. Only during the interval $\pi - \theta \leq \omega t \leq \pi$ power is transferred to the output of the converter and the average output current is given by

$$\begin{aligned} I_{\text{out}} &= I_{D,\text{av}} \\ &= \frac{2}{2\pi} \int_{\pi-\theta}^{\pi} \hat{I}_s \sin(\vartheta) d\vartheta \\ &= \frac{2\hat{I}_s}{\pi} \sin^2\left(\frac{\theta}{2}\right), \end{aligned} \quad (\text{A.5})$$

where $I_{D,av}$ is the average of the rectifier output current $i_D = i_{D1} + i_{D2}$. The output current is given by,

$$I_{out} = \frac{8}{\pi} V_{out} \omega C_p \tan^2 \left(\frac{\theta}{2} \right) \quad (A.6)$$

with the peak value of the transformer current \hat{I}_s from (A.3). The current through the resistive load R_L is additionally defined as

$$I_{out} = \frac{V_{out}}{R_L} \quad (A.7)$$

for a constant output voltage V_{out} . The conduction angle θ can be determined with (A.6) and (A.7) as

$$\theta = 2 \tan^{-1} \left(\sqrt{\frac{8}{\pi} \frac{1}{\omega R_L C_p}} \right). \quad (A.8)$$

The Fourier coefficients ($a_{v(1)}$, $b_{v(1)}$) for the fundamental $v_{Cp(1)}$ of the parallel-capacitor voltage are

$$\begin{aligned} a_{v(1)} = \frac{2}{\pi} & \left[\int_0^{\pi-\theta} \frac{2 V_{out}}{1 + \cos(\theta)} (1 - \cos(\theta) - 2 \cos(\omega t)) \cos(\omega t) d\omega t + \right. \\ & \left. \dots + \int_{\pi-\theta}^{\pi} 2 V_{out} \cos(\omega t) d\omega t \right] \end{aligned} \quad (A.9)$$

resulting in

$$a_{v(1)} = -\frac{4 V_{out}}{\pi} \frac{\pi - \theta + \sin(\theta) \cos(\theta)}{1 + \cos(\theta)} \quad (A.10)$$

and

$$\begin{aligned} b_{v(1)} = \frac{2}{\pi} & \left[\int_0^{\pi-\theta} \frac{2 V_{out}}{1 + \cos(\theta)} (1 - \cos(\theta) - 2 \cos(\omega t)) \sin(\omega t) d\omega t + \right. \\ & \left. \dots + \int_{\pi-\theta}^{\pi} 2 V_{out} \sin(\omega t) d\omega t \right] \end{aligned} \quad (A.11)$$

resulting in

$$b_{v(1)} = \frac{4V_{\text{out}}}{\pi}(1 - \cos(\theta)). \quad (\text{A.12})$$

The peak value $\hat{V}_{Cp(1)}$ of the fundamental of v_{Cp} can be calculated based on (A.10) and (A.12) as

$$\begin{aligned} \hat{V}_{Cp(1)} &= \sqrt{a_{v(1)}^2 + b_{v(1)}^2} \\ &= \frac{4V_{\text{out}}}{\pi(1 + \cos(\theta))} \sqrt{[\pi - \theta + \sin(\theta) \cos(\theta)]^2 + \sin^4(\theta)} \\ &= 2V_{\text{out}} k_v, \end{aligned} \quad (\text{A.13})$$

where k_v is a voltage factor

$$\begin{aligned} k_v &= \frac{\hat{V}_{Cp(1)}}{2V_{\text{out}}} \\ &= \frac{2}{\pi} \frac{\sqrt{[\pi - \theta + \sin(\theta) \cos(\theta)]^2 + \sin^4(\theta)}}{1 + \cos(\theta)}, \end{aligned} \quad (\text{A.14})$$

which could be approximated according to [147] with,

$$k_v \approx 1 + 0.27 \sin\left(\frac{\theta}{2}\right). \quad (\text{A.15})$$

The phase angle of the fundamental of the capacitor voltage v_{Cp} referring to ϑ_0 , cf. **Fig. A.2**, is

$$\begin{aligned} \zeta_{v(1)} &= \tan^{-1} \left(\frac{a_{v(1)}}{b_{v(1)}} \right) \\ &= \tan^{-1} \left(-\frac{\pi - \theta + \sin(\theta) \cos(\theta)}{\sin^2(\theta)} \right). \end{aligned} \quad (\text{A.16})$$

The phase angle $\zeta_{v(1)}$ results in negative values as $a_{v(1)} < 0$.

Rectifier Input Current (i_{rec}) In the next step, the phase angle $\zeta_{i(1)}$ of the rectifier input current $i_{\text{rec}} = i_{D1} - i_{D2}$ should be calculated in order to obtain an equivalent circuit for output filter and load,

$$i_{\text{rec}} = \begin{cases} 0 & \text{for } 0 \leq \omega t \leq \pi - \theta \text{ and } \pi \leq \omega t \leq 2\pi - \theta \\ \hat{I}_s \sin(\omega t) & \text{for } \pi - \theta \leq \omega t \leq \pi \text{ and } 2\pi - \theta \leq \omega t \leq 2\pi. \end{cases} \quad (\text{A.17})$$

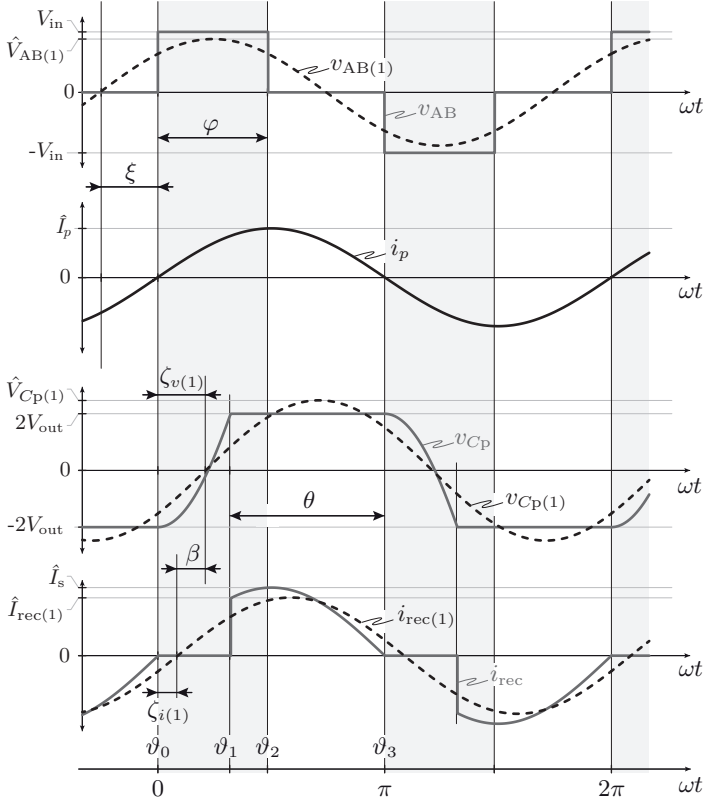


Figure A.2: Basic voltage and current waveforms of the fundamental frequency analysis of the series-parallel-resonant converter with centre-tapped secondary winding transformer, secondary-side parallel capacitor C_p and C-output filter.

The Fourier analysis of the rectifier input current results in the corresponding Fourier coefficients

$$\begin{aligned}
 a_{i(1)} &= \frac{2}{\pi} \int_{\pi-\theta}^{\pi} \hat{I}_s \sin(\omega t) \cos(\omega t) d\omega t \\
 &= -\frac{\hat{I}_s}{\pi} \sin^2(\theta)
 \end{aligned} \tag{A.18}$$

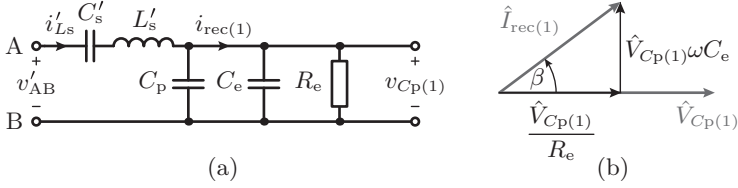


Figure A.3: Equivalent RC-circuit consisting of R_e and C_e replacing the rectifier, output filter and resistive load (a) and vector diagram of the respective fundamental input current and voltage (b).

and

$$\begin{aligned} b_{i(1)} &= \frac{2}{\pi} \int_{\pi-\theta}^{\pi} \hat{I}_s \sin^2(\omega t) d\omega t \\ &= \frac{\hat{I}_s}{\pi} \left(\theta - \frac{1}{2} \sin(2\theta) \right). \end{aligned} \quad (\text{A.19})$$

The phase angle relating to ϑ_0 is determined with (A.18) and (A.19),

$$\begin{aligned} \zeta_{i(1)} &= \tan^{-1} \left(\frac{a_{i(1)}}{b_{i(1)}} \right) \\ &= \tan^{-1} \left(-\frac{\sin^2(\theta)}{\theta - \frac{1}{2} \sin(2\theta)} \right) \\ &= \tan^{-1} \left(-\frac{1 - \cos(2\theta)}{2\theta - \sin(2\theta)} \right). \end{aligned} \quad (\text{A.20})$$

Equivalent Output Circuit The difference between the phase angles of the fundamental rectifier input current i_{rec} and the fundamental of voltage v_{CP} across the parallel capacitor, defined as

$$\beta = \zeta_{v(1)} - \zeta_{i(1)}, \quad (\text{A.21})$$

is negative, i.e. $i_{rec(1)}$ is leading $v_{CP(1)}$ and therefore the rectifier, output filter and resistive load can be modelled as an equivalent first-order RC-circuit as illustrated in **Fig. A.3 (a)**. With the expression for the output power

$$P_{out} = \frac{V_{out}^2}{R_L} = \frac{\frac{1}{2} \hat{V}_{CP(1)}^2}{R_e} \quad (\text{A.22})$$

and by applying (A.14) the equivalent resistance R_e can be calculated,

$$R_e = 2 k_v^2 R_L. \quad (\text{A.23})$$

According to the vector diagram in **Fig. A.3 (b)** the equivalent capacitance C_e can be described with the expression of the phase-angle difference β ,

$$\tan |\beta| = \omega C_e R_e. \quad (\text{A.24})$$

By substituting R_e with (A.23) in (A.24), C_e can be obtained as

$$C_e = \frac{\tan |\beta|}{2 k_v^2 \omega R_L}. \quad (\text{A.25})$$

A further expression for the peak value of the equivalent-circuit input current \hat{I}_{rec} is according to **Fig. A.3 (b)**

$$\hat{I}_{\text{rec}(1)} = \frac{\hat{V}_{C_P(1)}}{R_e \cos |\beta|} \quad (\text{A.26})$$

or by applying (A.7), (A.14) and (A.23)

$$\hat{I}_{\text{rec}(1)} = \frac{I_{\text{out}}}{k_v \cos |\beta|}. \quad (\text{A.27})$$

Resonant Tank Input Voltage (v_{AB}) In the next step the first harmonic of the resonant tank input voltage v_{AB} is determined. Based on the control scheme of the resonant converter as described in section 2.1, the positive input voltage V_{in} is applied during the powering phase (angle φ cf. **Fig. A.2**) to the resonant tank starting at $\omega t = \vartheta_0$ where the resonant current i_{Ls} crosses zero and becomes positive. During the free-wheeling phases ($\varphi \leq \omega t \leq \pi$ and $\pi + \varphi \leq \omega t \leq 2\pi$) the resonant tank is short-circuited by the low-side or high-side switches. The free-wheeling-phase angle $\pi - \varphi$ is thereby equal to twice the phase angle ξ of the first harmonic $v_{AB(1)}$ relating to ϑ_0 , cf. **Fig. A.2**. The Fourier coefficients of the first harmonic $v_{AB(1)}$ of the resonant tank voltage are therefore represented by

$$\begin{aligned} a_{vAB(1)} &= \frac{2}{\pi} \int_0^{\pi-2\xi} V_{\text{in}} \cos(\omega t) d\omega t \\ &= \frac{2}{\pi} \sin(2\xi) \end{aligned} \quad (\text{A.28})$$

and

$$\begin{aligned} b_{\text{vAB}(1)} &= \frac{2}{\pi} \int_0^{\pi-2\xi} V_{\text{in}} \sin(\omega t) d\omega t \\ &= \frac{2}{\pi} (1 + \cos(2\xi)). \end{aligned} \quad (\text{A.29})$$

The peak value $\hat{V}_{\text{AB}(1)}$ of the resonant tank voltage can be determined by applying (A.28) and (A.28) as

$$\begin{aligned} \hat{V}_{\text{AB}(1)} &= \sqrt{a_{\text{vAB}(1)}^2 + b_{\text{vAB}(1)}^2} \\ &= \frac{4V_{\text{in}}}{\pi} \cos(\xi), \end{aligned} \quad (\text{A.30})$$

and referring to the secondary side ,cf. **Fig. A.3**,

$$\hat{V}'_{\text{AB}(1)} = \frac{4V_{\text{in}}}{n\pi} \cos(\xi). \quad (\text{A.31})$$

An expression for the AC voltage transfer ratio from the input to the output of the resonant tank can be found with (A.13) and (A.31),

$$\begin{aligned} \frac{\hat{V}_{\text{CP}(1)}}{\hat{V}'_{\text{AB}(1)}} &= \frac{V_{\text{out}}}{V_{\text{in}}} \frac{n\pi k_{\text{v}}}{4} \frac{2}{\cos \xi} \\ &= k_{\text{v}}^* \frac{2}{\cos \xi}, \end{aligned} \quad (\text{A.32})$$

where k_{v}^* can be obtained from the equivalent circuit in **Fig. A.3 (a)** as introduced in [147, 153] as

$$\begin{aligned} k_{\text{v}}^* &= \dots \\ &= \frac{1}{\sqrt{\left(1 + \frac{C_{\text{p}} + C_{\text{e}}}{C'_{\text{s}}} - \omega^2 L'_{\text{s}} (C_{\text{p}} + C_{\text{e}})\right)^2 + \left(\omega L'_{\text{s}} - \frac{1}{\omega C'_{\text{r}}}\right)^2 \frac{1}{R_{\text{e}}^2}}} \\ &= \frac{1}{\sqrt{\left\{1 - \frac{C_{\text{p}}}{C'_{\text{s}}} \left[\left(\frac{\omega}{\omega_{\text{s}}}\right)^2 - 1\right] \left(1 + \frac{C_{\text{e}}}{C_{\text{p}}}\right)\right\}^2 + \left\{\frac{C_{\text{p}}}{C'_{\text{s}}} \left[\left(\frac{\omega}{\omega_{\text{s}}}\right)^2 - 1\right] \frac{1}{\omega C_{\text{p}} R_{\text{e}}}\right\}^2}} \\ &= \frac{1}{\sqrt{\left\{1 - \frac{C_{\text{p}}}{C'_{\text{s}}} \left[\left(\frac{\omega}{\omega_{\text{s}}}\right)^2 - 1\right] \left(1 + \frac{\tan|\beta|}{\omega C_{\text{p}} R_{\text{e}}}\right)\right\}^2 + \left\{\frac{C_{\text{p}}}{C'_{\text{s}}} \left[\left(\frac{\omega}{\omega_{\text{s}}}\right)^2 - 1\right] \frac{1}{\omega C_{\text{p}} R_{\text{e}}}\right\}^2}} \end{aligned} \quad (\text{A.33})$$

with the series-resonance frequency

$$\omega_s = \frac{1}{\sqrt{L_s C_s}}. \quad (\text{A.34})$$

The DC transfer ratio of the converter can be defined as

$$V_{\text{out}}^* = \frac{n V_{\text{out}}}{V_{\text{in}}} = \frac{V_{\text{out}}}{\hat{V}_{C_p(1)}} \frac{\hat{V}_{C_p(1)}}{\hat{V}_{AB(1)}} \frac{\hat{V}'_{AB(1)}}{V_{\text{in}}} n \quad (\text{A.35})$$

and by inserting (A.14), (A.32), and (A.31) the normalised output voltage becomes

$$V_{\text{out}}^* = \frac{4 k_v^*}{\pi k_v}. \quad (\text{A.36})$$

In addition to the voltage transfer ratio the input phase angle ξ of the resonant circuit, i.e. the phase angel between the fundamentals of v_{AB} and i_{L_s} can be derived from the equivalent circuit in **Fig. A.3 (a)** [147, 153]

$$\begin{aligned} \tan(\xi) &= \frac{1}{\omega C_p R_e} \frac{C_p}{C'_s} \left\{ \left(\frac{\omega}{\omega_s} \right)^2 [1 + \omega^2 (C_p + C_e)^2 R_e^2] - 1 \right\} - \dots \\ &\quad \dots - [\omega (C_p + C_e) R_e] \left(1 + \frac{C_p + C_e}{C'_s} \right) \\ &= \frac{1}{\omega C_p R_e} \left\{ \frac{C_p}{C'_s} [1 + (\omega C_p R_e + \tan |\beta|)^2] - 1 \right\} - \dots \\ &\quad \dots - (\omega C_p R_e + \tan |\beta|) \left[1 + \frac{C_p}{C'_s} \left(1 + \frac{\tan |\beta|}{\omega C_p R_e} \right) \right]. \end{aligned} \quad (\text{A.37})$$

Input Current I_{in} The duration of the powering phases are determined with the definition of the phase angle ξ , resulting in the current-transfer angle of the converter input to the resonant tank; the average input current is defined as

$$I_{\text{in}} = \frac{2}{2\pi} \int_0^{\pi-2\xi} \hat{I}_{L_s} \sin(\omega t) d\omega t = \frac{2\hat{I}_{L_s}}{\pi} \cos^2(\xi) = \frac{2\hat{I}_s}{n\pi} \cos^2(\xi) \quad (\text{A.38})$$

and by applying (A.5)

$$I_{\text{in}} = \frac{I_{\text{out}}}{n} \frac{\cos^2(\xi)}{\sin^2(\frac{\theta}{2})}. \quad (\text{A.39})$$

A further definition of the **normalised output voltage** is given by

$$V_{\text{out}}^* = \frac{nV_{\text{out}}}{V_{\text{in}}} = \frac{\cos^2(\xi)}{\sin^2(\frac{\theta}{2})} \quad (\text{A.40})$$

with the assumption of an ideal power conversion, i.e. $V_{\text{in}} I_{\text{in}} = V_{\text{out}} I_{\text{out}}$.

Q-Factor Based on **Fig. A.3** an expression of the complex voltage ratio is

$$\frac{\hat{v}_{C_{\text{p}}(1)}}{\hat{v}'_{\text{AB}(1)}} = \frac{-jX_{C_{\text{pe}}}\|R_{\text{e}}}{-jX_{C'_{\text{s}}} + jX_{L'_{\text{s}}} - jX_{C_{\text{pe}}}\|R_{\text{e}}}, \quad (\text{A.41})$$

where $X_{C_{\text{pe}}}$ is the summarised impedance of the parallel-connected capacitors C_{p} and C_{e} . The normalisation of (A.41) results in

$$\frac{\hat{v}_{C_{\text{p}}(1)}}{\hat{v}'_{\text{AB}(1)}} = \frac{1}{\sqrt{\left(1 + \frac{C_{\text{pe}}}{C'_{\text{s}}} + \omega^2 L'_{\text{s}} C_{\text{pe}}\right) + j \frac{1}{R_{\text{e}}} \sqrt{\frac{L'_{\text{s}}}{C'_{\text{s}}}} \left(\frac{\omega}{\omega_{\text{s}}} - \frac{\omega_{\text{s}}}{\omega}\right)}}. \quad (\text{A.42})$$

The quality factor (Q-factor) can be directly obtained from the normalised equation (A.42) as

$$Q = \frac{1}{R_{\text{e}}} \sqrt{\frac{L_{\text{s}}}{C_{\text{s}}}} = \frac{\omega_{\text{s}} L_{\text{s}}}{R_{\text{e}}} = \frac{1}{2k_{\text{v}}^2} \frac{\omega_{\text{s}} L_{\text{s}}}{R_{\text{L}}}. \quad (\text{A.43})$$

Q_{s} is defined based on (A.43) for further investigations by omitting the voltage factor k_{v} as

$$Q_{\text{s}} = \frac{\omega_{\text{s}} L_{\text{s}}}{R_{\text{L}}}. \quad (\text{A.44})$$

The quality factor Q_{s} is depended on series-resonant components L_{s} and C_{s} and the resistive load R_{L} . With the applied definition, the Q-factor is decreasing with the load resistance. As an example, in the diagrams of **Fig. A.4** the Q_{s} -values 3, 1.5, 0.6, and 0.3 are related to the loads defined in the Energy Star[®] requirements for computer servers, i.e. 100 %, 50 %, 20 %, and 10 % of full load, respectively. The intersection of the constant normalised output voltage (determined by the constant input and output voltage as well as the turns ratio) with the parameter-depended normalised output voltage (right-hand-side of (A.40)) defines the operation point of the system. According to **Fig. A.4(a)**, the switching frequency is increasing reciprocally

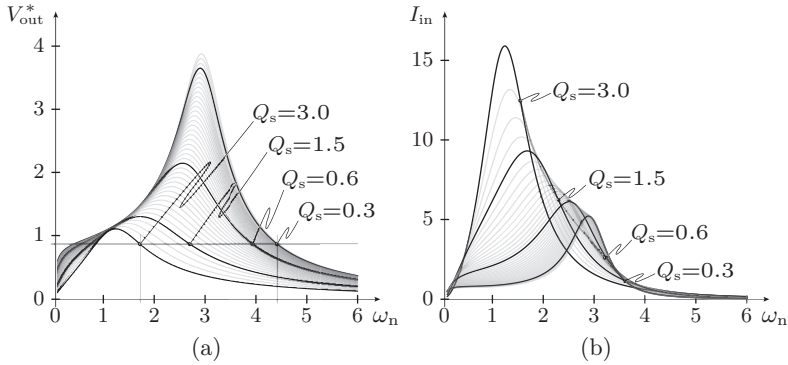


Figure A.4: Normalised output voltage V_{out}^* and average input current I_{in} in dependency of the normalised frequency $\omega_n = \omega/\omega_s$.

with the load resistance and/or Q_s . The average input current is decreasing with the load resistance and the corresponding load-dependent operating points are located on a parabola shaped curve as shown in **Fig. A.4(b)**.

The switching frequency is therefore determined by inserting the expressions for the phase-angle ξ and conduction angle θ and numerically solving (A.40) or (A.39), respectively, for the angular switching frequency ω .

The discussion about the influence and interdependency of the resonant tank component values on the converter operation is shown in section 2.1.

B

Magnetic Components Modelling Equivalent Reluctance Circuit

The analytical models of the magnetic components (transformer and inductors) have to be considered during the optimisation processes and therefore an interface between the geometry and the magnetic and the electric behaviour has to be developed. Especially for integrated structures, the geometric assembly exhibits higher complexity compared to a two-winding transformer, but still can be described applying equivalent reluctance models. Furthermore, deviations from the ideal magnetic component behaviour such as leakage inductances can be modelled with a relatively low effort. As the reluctance models have been applied several times for different magnetic components in this thesis, a short summary and derivation of the magnetic component modelling is given in this section following Witulski's concise tutorial paper about transformer and coupled inductor modelling [156].

B.1 Basic Electromagnetic Laws

The laws of Faraday, Ampère and Gauss are the primarily applied relations when analysing magnetic structures and are therefore briefly reviewed. The integral form of Faraday's law is given by

$$\oint_l \vec{E} \, d\vec{l} = -\frac{\partial}{\partial t} \int_S \vec{B} \, d\vec{s} \quad (\text{B.1})$$

where \vec{E} is the (directed) electric field and \vec{B} is the magnetic flux density. The left-hand side of (B.1) is known as the electromotive force

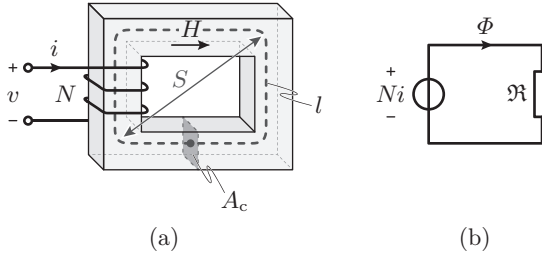


Figure B.1: Application of Ampère’s law to a simple magnetic structure with single winding and a ferrite core (a); and the related equivalent reluctance circuit (b) [156].

(emf) or, in a specific case, the induced voltage v . The integral of the magnetic flux density over a surface S on the right side of (B.1) is the expression of the magnetic flux Φ (not to be mistaken with the Gauss’ law of magnetic field (below) integrated over a closed surface), i.e. the complete right-hand side of (B.1) determines the rate of change of the magnetic flux Φ . Faraday’s law can therefore more conveniently be expressed by

$$v = N \frac{d\Phi}{dt}, \quad (\text{B.2})$$

where N is the number of turns formed by a conductor exposed to the magnetic field.

Ampère’s law can be seen as the magnetic counterpart to Faraday’s law of induction and the integral form is given by

$$\oint_l \vec{H} \, d\vec{l} = \int_S \vec{J} \, d\vec{s} = i \quad (\text{B.3})$$

where \vec{H} is the magnetic field intensity, \vec{J} is current density and i is the current passing through the surface S . Paraphrasing (B.3), Ampère’s law states that the integral of the magnetic field around a closed path is equal to the total current passing through the surface S enclosed by the path l as illustrated in **Fig. B.3(a)**.

The last fundamental law applied for the derivation of the equivalent reluctance model is Gauss’s law for magnetic fields, given in integral form as

$$\oint_{S_A} \vec{B} \, d\vec{s} = 0 \quad (\text{B.4})$$

stating that the total magnetic flux passing through any closed three-dimensional surface S_A is zero; or in other words, the inward flowing (negative) magnetic flux must be exactly balanced with the outward flowing (positive) magnetic flux [166].

The magnetic flux density \vec{B} and the magnetic field \vec{H} are linked with the relationship

$$\vec{B} = \mu_0 \mu_r \vec{H} \quad (\text{B.5})$$

where μ_0 is the permeability of free space ($\mu_0 = 4\pi \cdot 10^{-7} \text{ Vs A}^{-1} \text{ m}^{-1}$) and μ_r is the material dependent relative permeability. In free space, the relative permeability is unity and the relationship (B.5) is linear. In ferromagnetic materials, B and H are linked by the material-specific B - H -curve with saturation regions (positive and negative maximum flux density B_{\max}) and the typical hysteresis. In the approximately linear part the permeability of highly permeable materials like ferrites ($\mu_r \approx 10^2 \dots 10^4$ [168]) results in a high flux density for a given magnetic field H , cf. (B.5).

B.2 Equivalent Reluctance Circuit Model

The purpose of establishing an equivalent reluctance circuit model is the possibility of a straightforward integration into the comprehensive analytical equation database for determining the performance of a complex converter system. For that reason the electromagnetic laws must be simplified so that the magnetic flux can be determined without evaluating the line and surface integrals. The basic assumptions for the model are, therefore, that the magnetic field is constant in an investigated segment and is furthermore aligned in the direction of the path of integration. These assumptions are sufficiently fulfilled for segments of a uniform ferromagnetic material or small distances in free space [156]. With these assumptions, Ampère's law (B.3) as illustrated in **Fig. B.1(a)** is reduced in the simplest case to

$$H l = N i. \quad (\text{B.6})$$

With the definition of the magnetic flux $\Phi = B A_c$ (where A_c is the cross-sectional area penetrated by the magnetic field as illustrated in **Fig. B.1(a)**) and by applying (B.5) an expression for the magnetomot-

ive force \mathfrak{F} (mmf) can be found

$$\left. \begin{aligned} \vec{B} &= \mu_0 \mu_r \vec{H} \\ \Phi &= B A_c \end{aligned} \right\} \quad \mathfrak{F} = \Phi \frac{l}{\mu A_c} = \Phi \mathfrak{R} = N i, \quad (\text{B.7})$$

where $\mu = \mu_0 \mu_r$ is the material permeability and the reluctance \mathfrak{R} refers to the magnetic path l as shown in **Fig. B.1(a)**. As the magnetomotive force $\mathfrak{F} = N i$ is linearly related to the magnetic flux Φ via the reluctance \mathfrak{R} , an equivalent magnetic circuit can be defined in analogy to an electric circuit described by Ohm's law as illustrated in **Fig. B.1(b)**, where the voltage correlates to the magnetomotive force \mathfrak{F} , the current to the magnetic flux Φ and the resistance to the reluctance \mathfrak{R} .

Furthermore, Kirchhoff's voltage and current laws for electric circuits are applicable for the equivalent magnetic circuit as well. On the one hand, the reluctance \mathfrak{R} can be subdivided into m smaller reluctances \mathfrak{R}_i ($i = 1..m$) corresponding to segments of \mathfrak{R} with path lengths $l_1, l_2, .. l_m$ and therefore Ampère's law can be stated as

$$\sum_{i=1}^n \mathfrak{F}_i = \sum_{i=1}^m \Phi \mathfrak{R}_i \quad (\text{B.8})$$

for a mesh of the magnetic circuit equivalent to Kirchhoff's voltage law. On the other hand, Gauss's law for magnetic circuits (B.4) states that the sum of the magnetic fluxes entering and exiting a magnetic node must be zero, in analogy to Kirchhoff's current law, which can be expressed as

$$\sum_{i=1}^k \Phi_i = 0. \quad (\text{B.9})$$

The magnetic circuit can be analysed with the above introduced equations and the well-known electric circuits' laws. The magnetic flux for the simple example in **Fig. B.1(b)** is given by

$$\Phi = \frac{N i}{\mathfrak{R}}. \quad (\text{B.10})$$

By applying Faraday's law the linkage to the electric circuit can be established through

$$v = N \frac{d\Phi}{dt} = \frac{N^2}{\mathfrak{R}} \frac{di}{dt} = L \frac{di}{dt}. \quad (\text{B.11})$$

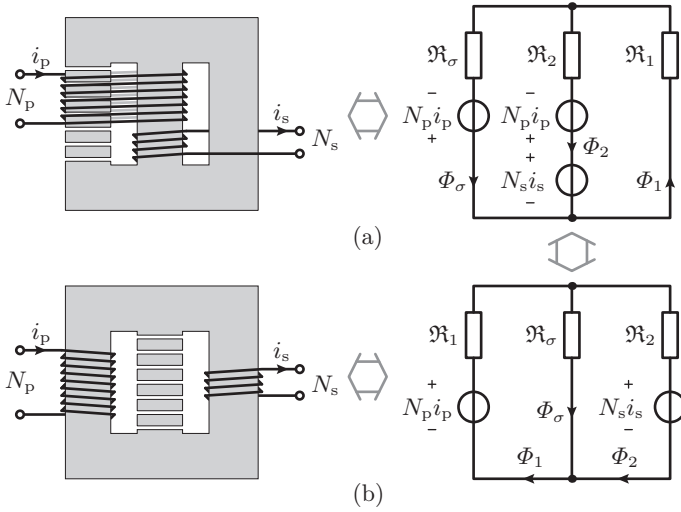


Figure B.2: Reluctance model derivation of the integrated transformer for the series-parallel-resonant converter (a) and possible equivalent transformer assembly (b)

Additionally important in the optimisation process is the link to the geometry of the magnetic structure which is given for the simple example by

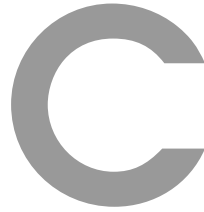
$$L = N^2 \frac{\mu A_c}{l}. \quad (\text{B.12})$$

The equivalent magnetic circuit can be extended by further windings (magnetomotive forces) and magnetic flux paths, i.e. additional core segments with \mathfrak{R}_1 , \mathfrak{R}_2 etc. and leakage flux paths with $\mathfrak{R}_{\sigma 1}$, $\mathfrak{R}_{\sigma 2}$, etc. right up to highly complex magnetic structures can be defined. These structures can still be investigated with classical electric circuit analysis methods. Further examples are given, for instance, in the here quoted tutorial paper of Witulski [156] or for the integrated transformer of a series-parallel-resonant converter in [142]. The analytical description of the integrated magnetic structures for the series-parallel-resonant converter in section 2.1 or the PWM converter with integrated current doubler in section 2.2 are based on the here derived reluctance model as well. For the series-parallel-resonant converter, the winding arrangement as presented in **Fig. B.2(a)** is applied. The correspond-

ing reluctance model is shown on the right side. The mesh equations for the reluctance model can be re-arranged as

$$\begin{aligned} N_p i_p &= \mathfrak{R}_1 \Phi_1 + \mathfrak{R}_\sigma (\Phi_1 - \Phi_2) \\ N_s i_s &= -\mathfrak{R}_2 \Phi_2 + \mathfrak{R}_\sigma (\Phi_1 - \Phi_2). \end{aligned} \tag{B.13}$$

The mesh equations of the reluctance model for the corresponding winding and transformer arrangement in **Fig. B.2(b)** result in the same equations (B.13), i.e. the two reluctance models are equivalent.



Winding Losses in Magnetic Devices

The magnetic components of a converter system have a major influence on the resulting converter performance, regardless of which performance index is investigated. For the determination of the system operating point, the losses in the magnetic and electronic devices are commonly neglected as the influence on the characteristic waveforms is rather small. The physical performance indices, such as power density, efficiency, and output power per unit weight, are mainly determined by the losses in the windings and in the core of a transformer or inductor. The design parameters in the proposed optimisation processes are consequently primarily influenced by the losses. A summary about the calculation of winding losses in the applied foil windings considering the dependence on the operating point and geometry parameters is presented in this section.

The winding losses are occurring due to the electrical resistance of a current-carrying conductor. For DC-currents the resistance can be simply calculated for a given geometry and material as

$$R_{\text{DC}} = \frac{l}{\sigma A}, \quad (\text{C.1})$$

where l is the conductor length, σ is the electrical conductivity of the applied material (the reciprocal of the electrical resistivity ρ) and A is the cross-sectional area of the conductor. If the conductor is carrying an alternating current or if the conductor is exposed to an alternating magnetic field – both is commonly the case in the windings of the magnetic devices of power electronic systems – the effective resistance of the conductor is increased due to eddy currents and the current density is unevenly distributed over the cross-section of the conductor. There

basically two effects are describing the occurrence of eddy currents:

- **Skin effect:** The alternating current in the conductor generates an alternating magnetic field in the conductor itself, which in turn induces an electrical field in this conductor. Because of the alternating electrical field, eddy currents flow within the conductor and, as a consequence, the current density is reduced in the middle and increased in regions close to the surface of the conductor.

- **Proximity effect:** Besides the magnetic field generated within the current-carrying inductor, a magnetic field is additionally generated outside the conductor. A further magnetic field, frequently existing in magnetic components, is generated around an air gap. In a second conductor, which is exposed to one or the superposition of several external magnetic fields, an electric field is induced which generates eddy currents and partly changes the current density in the conductor.

The calculation of the skin and proximity effect is related to Maxwell's equations, which cannot be analytically solved readily for the three-dimensional structure of an inductor or transformer. Furthermore, the accurate determination with the aid of Finite Elements Methods (FEM) is not practicable as the computation time even for low-complexity two-dimensional structures is much beyond the aspired time values during the optimisation processes. The following derivation of the losses is therefore based on Dowell's one-dimensional approach for analytically determining eddy current effects in transformer windings [163]. Additionally, the publications of Ferreira [164] and Hurley [155, 198] are consulted, as well as the derivations and explanations in [149, 165, 166, 206].

Following the analytical description of heat propagation, the diffusion of electromagnetic fields can be described by second-order differential equations. With the assumptions, that the considered materials are homogeneous and linear and the investigated parameters, i.e. currents, voltages and field, are sinusoidal¹, Maxwell's equations can be written

¹The time-derivative of a sinusoidal function f can be represented by multiplying the function f with $j\omega$.

as

$$\operatorname{div} \vec{E} = \frac{q_{\text{enc}}}{\epsilon} \quad \text{Gauss' law for electric fields} \quad (\text{C.2})$$

$$\operatorname{rot} \vec{E} = -j\omega \vec{B} \quad \text{Faraday's law} \quad (\text{C.3})$$

$$\operatorname{div} \vec{B} = 0 \quad \text{Gauss' law for magnetic fields} \quad (\text{C.4})$$

$$\operatorname{rot} \vec{B} = j\omega \epsilon \mu \vec{B} + \mu \vec{J} \quad \text{Ampère-Maxwell's law} \quad (\text{C.5})$$

where q_{enc} is the enclosed charge, $\epsilon = \epsilon_0 \epsilon_r$ is absolute permittivity (the product of the free-space permittivity ϵ_0 and relative permittivity ϵ_r). In order to decouple the electric and magnetic fields in Faraday's law (C.3) and Ampère-Maxwell's law (C.5) the field equations are transformed into differential equations. The current density described by Ohm's law

$$\vec{J} = \sigma \vec{E} \quad (\text{C.6})$$

is substituted in (C.5) resulting in

$$\operatorname{rot} \vec{B} = (\sigma + j\omega\epsilon) \mu \vec{E}. \quad (\text{C.7})$$

Applying Faraday's law (C.3) in (C.7)

$$\operatorname{rot}(\operatorname{rot} \vec{E}) = \operatorname{grad}(\operatorname{div} \vec{E}) - \nabla^2 \vec{E} = -(\sigma + j\omega\epsilon) j\omega\mu \vec{E} \quad (\text{C.8})$$

and with Gauss's law of electric fields (C.2), (C.8) results in

$$\nabla^2 \vec{E} = \operatorname{grad} \frac{q_{\text{enc}}}{\epsilon} + (\sigma + j\omega\epsilon) j\omega\mu \vec{E}. \quad (\text{C.9})$$

Similarly to the derivation of the electric field differential equation (C.9) from Ampère-Maxwell's law, the second-order differential equation for the magnetic field can be derived from Faraday's law (C.3) by inserting equation (C.7) solved for \vec{E} which results in:

$$\operatorname{rot}(\operatorname{rot} \vec{B}) = \operatorname{grad}(\operatorname{div} \vec{B}) - \nabla^2 \vec{B} = -(\sigma + j\omega\epsilon) j\omega\mu \vec{B}. \quad (\text{C.10})$$

Due to Gauss' law for magnetism, which implies that magnetic monopoles do not exist (contrary to electric fields), (C.10) can be further simplified:

$$\nabla^2 \vec{B} = (\sigma + j\omega\epsilon) j\omega\mu \vec{B}. \quad (\text{C.11})$$

The term $\operatorname{grad}(q_{\text{enc}}/\epsilon)$ in (C.9) describes the induced charge distribution perpendicular to the current-flow direction which is caused

by quasi-static electrical field, e.g. due to applied voltages between the winding layers of a transformer with a specific winding capacitance [149]. Neglecting the induced charge distribution, (C.9) and (C.11) are similar for magnetic and electric field.

The term $-\omega^2\epsilon\mu$ in both equations (C.9) and (C.11) describes the displacement current. In electric conductors, the displacement current can be neglected (whereas, for instance, the determination of the capacitive currents between windings is depended on this term [149]). The equations (C.9) and (C.11) can be simplified with the neglected displacement current to

$$\nabla^2 \vec{E} = j\omega\sigma\mu\vec{E} \quad (\text{C.12})$$

$$\nabla^2 \vec{B} = j\omega\sigma\mu\vec{B} \quad (\text{C.13})$$

and by applying Ohm's law (C.22) to

$$\nabla^2 \vec{J} = j\omega\sigma\mu\vec{J} \quad (\text{C.14})$$

where \vec{J} describes the current flow in the conductor including the eddy currents.

C.1 Skin Effect in Foil Conductors

With the derived differential equation (C.13), the current distribution in a foil conductor which carries a current in the direction x , cf. **Fig. C.1**, is determined, i.e. the skin effect is analysed. The flux density in (C.13) can be substituted by $\mu_0 \vec{H}$ for non-magnetic conductive materials with a relative permeability $\mu_r \approx 1$,

$$\nabla^2 \vec{H} = \alpha^2 \vec{H} \quad (\text{C.15})$$

with

$$\alpha = \frac{1+j}{\delta_0}$$

and the skin depth δ_0

$$\delta_0 = \frac{1}{\sqrt{\pi f \sigma \mu_0}}. \quad (\text{C.16})$$

The magnetic field intensity within the conductor can be considered as independent of the x and z position with the assumptions, that

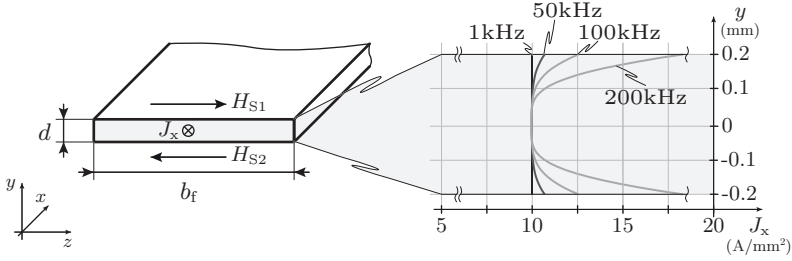


Figure C.1: Cut through an infinitely long foil conductor carrying a current in the direction of x with the related current density as function of the position in direction of y . *Underlying parameters:* Copper foil, $\sigma = 5.9 \cdot 10^7 \Omega^{-1} \text{m}^{-1}$, $b = 50 \text{ mm}$, $d = 400 \mu\text{m}$, $\hat{I} = 100 \text{ A}$.

current flows in the positive-defined direction of x of an infinitely long conductor and that the foil thickness d is much smaller than its width b_f ($d \ll b_f$, cf. **Fig. C.1**). Furthermore, it is assumed that the magnetic field only exhibits a component in the direction of z . Due to the one-dimensional approach, the differential equation (C.15) is simplified to

$$\frac{d^2}{dy^2} H_z = \alpha^2 H_z \quad (\text{C.17})$$

with the general solution

$$H_z = K_1 e^{\alpha y} + K_2 e^{-\alpha y}. \quad (\text{C.18})$$

The magnetic field intensity on the surface of the conductor can be determined with Ampère's law (B.3) and the given assumptions as

$$H_{S1} = -H_{S2} = \frac{\hat{I}}{2b}. \quad (\text{C.19})$$

Applying (C.19) as boundary condition in (C.18) the coefficients K_1 and K_2 can be calculated,

$$K_1 = -K_2 = \frac{\hat{I}}{4b \sinh\left(\frac{\alpha d}{2}\right)}, \quad (\text{C.20})$$

and therefore the inner magnetic field intensity in direction of z in dependency of y can be determined,

$$H_z = \frac{\hat{I} \sinh(\alpha y)}{2b \sinh\left(\frac{\alpha d}{2}\right)}. \quad (\text{C.21})$$

The current density J_x in the foil conductor is calculated by differentiating the magnetic field intensity H_z with respect to y ,

$$J_x = \frac{d}{dy} H_z = \frac{\alpha \hat{I} \cosh(\alpha y)}{2b \sinh\left(\frac{\alpha d}{2}\right)}. \quad (\text{C.22})$$

The ohmic losses per unit length due to the skin effect P'_s can now be determined with the current density (horizontal symmetry axis in the middle of the conductor)

$$\begin{aligned} P'_s &= \frac{b}{2\sigma} \int_{-d/2}^{d/2} |J_x|^2 dy \\ &= \frac{\hat{I}^2}{4b\sigma\delta_0} \frac{\sinh(\Delta) + \sin(\Delta)}{\cosh(\Delta) - \cos(\Delta)} \quad \text{in} \left(\frac{\text{W}}{\text{m}} \right) \end{aligned} \quad (\text{C.23})$$

where Δ is defined as the ration of foil thickness d and the skin depth δ_0

$$\Delta = \frac{d}{\delta_0}. \quad (\text{C.24})$$

The skin effect losses per unit length are given by

$$P'_s = R_{\text{dc}} F_F \hat{I}^2 \quad \text{in} \left(\frac{\text{W}}{\text{m}} \right) \quad (\text{C.25})$$

with the definition of the frequency-independent electrical resistance per unit length R'_{DC} ,

$$R'_{\text{DC}} = \frac{1}{\sigma b d} \quad \text{in} \left(\frac{\Omega}{\text{m}} \right), \quad (\text{C.26})$$

and the term F_F , which describes the increase of the resistance with the frequency due to the skin effect

$$F_F = \frac{\Delta}{4} \frac{\sinh(\Delta) + \sin(\Delta)}{\cosh(\Delta) - \cos(\Delta)}. \quad (\text{C.27})$$

C.2 Proximity Effect in Foil Conductors

If an electric conductor is exposed to an external field as illustrated in **Fig. C.2**, eddy currents are induced in the conductor. It is assumed

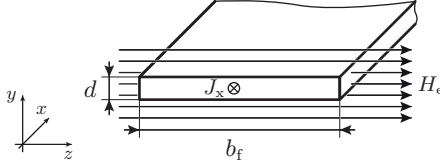


Figure C.2: Cut through a foil conductor exposed to an external magnetic field with the magnitude \hat{H}_e .

that the magnetic field \vec{H}_e exhibits only a component in the direction of z and the field intensity is homogeneous outside the conductor with the magnitude \hat{H}_{ez} . Inserting this boundary condition into the general solution of the one-dimensional differential equation (C.18), the magnetic field intensity H_z inside the conductor is given by

$$H_z = \frac{\cosh(\alpha y)}{\cosh\left(\frac{\alpha d}{2}\right)} \hat{H}_{ez} \quad (\text{C.28})$$

which is differentiated with respect to the position y in order to get the current density,

$$J_x = \frac{d}{dy} H_z = \frac{\alpha \sinh(\alpha y)}{\cosh\left(\frac{\alpha d}{2}\right)} \hat{H}_{ez}. \quad (\text{C.29})$$

The resistive losses per unit length due to the proximity effect can now be determined similar to the losses due to the skin effect P'_p

$$\begin{aligned} P'_p &= \frac{b}{2\sigma} \int_{-d/2}^{d/2} |J_x|^2 dy \\ &= \frac{b}{\sigma \delta_0} \frac{\sinh(\Delta) - \sin(\Delta)}{\cosh(\Delta) + \cos(\Delta)} \hat{H}_e^2 \quad \text{in} \left(\frac{\text{W}}{\text{m}} \right) \end{aligned} \quad (\text{C.30})$$

and with the definition of the frequency-dependent term G_F

$$G_F = b^2 \Delta \frac{\sinh(\Delta) - \sin(\Delta)}{\cosh(\Delta) + \cos(\Delta)} \quad (\text{C.31})$$

the losses due the proximity effect can expressed as

$$P'_p = R'_{DC} G_F \hat{H}_{ez}^2 \quad \text{in} \left(\frac{\text{W}}{\text{m}} \right). \quad (\text{C.32})$$

The sum of the losses due to the proximity effect and the skin effect are the total frequency-dependent losses per unit length P'_w in a single conductor,

$$P'_w = R'_{DC} \left(F_F \hat{I}^2 + G_F \hat{H}_{ez}^2 \right) \quad \text{in} \quad \left(\frac{W}{m} \right). \quad (\text{C.33})$$

C.3 HF-Losses in Winding Arrangements

The losses due to the skin and proximity effect of a single conductor can be determined with (C.25) and (C.32) or (C.33), respectively. The windings of transformers and inductors commonly consist of multiple conductor layers. The skin and proximity losses in a winding arrangement are established in the following paragraphs based on the above introduced derivations for a single conductor.

The losses due to the skin effect in a current-carrying conductor are self-induced, i.e. skin effect losses are independent of the winding arrangement. The winding losses due to the skin effect can therefore directly be determined by multiplying the losses per unit length (C.25) with the respective length of the winding.

The losses due to the proximity effect in a conductor are induced because of an external magnetic field generated from the adjacent windings², i.e. the magnetic field to which the winding is exposed, has to be determined. Similarly as presented above, a one-dimensional approach following [163] is applied for the loss derivation, neglecting 2-D or 3-D fringing and crossover effects which could be only determined for special geometries (semi-)analytically [206] and are commonly calculated by applying numerical methods, e.g. FEM or the Partial Element Equivalent Circuit (PEEC) concept [208].

A section of the transformer core, for example the left side of an E-core centre leg with two windings (N_1 and N_2), is illustrated in **Fig. C.3** with the corresponding \vec{H} -field which exhibits only a field component H_z in direction of z in parallel to the foil conductor (1-D approach of [163]). It is further assumed that the foil winding entirely fills the winding window in the direction of z and the relative permeability μ_r of the core is much higher than in the winding window (air or insulation

²The following derivations only refer to the windings themselves as sources for the external magnetic field. Other sources, as for instance air gaps, are not further considered. The influence of air gaps is explained for example in [149, 206, 207]

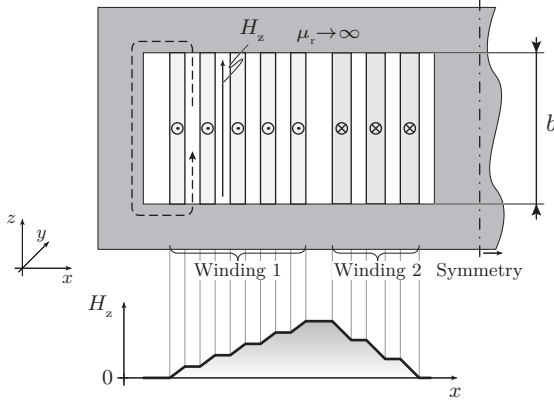


Figure C.3: Cut through of a transformer section with two windings and the corresponding approximated magnetic field.

materials with $\mu_r \approx 1$), ideally $\mu_r \rightarrow \infty$. With Ampère's law, the magnetic field for the most left winding in **Fig. C.3** can be determined

$$\oint_C \vec{H} d\vec{l} = b \int_{x_1}^{x_2} J_y dx \quad (\text{C.34})$$

and therefore the magnitude of the magnetic field \hat{H}_{z1} between winding 1 and 2 can for instance be calculated with

$$\hat{H}_{z1} = \frac{\hat{I}}{b}. \quad (\text{C.35})$$

For the determination of the proximity losses it is assumed that the value of the magnetic field is equal on both sides of the conductor. This approximation is sufficiently accurate if the maximum value of the magnetic field in the winding arrangement is much higher compared to the actual field gradient between both surfaces of a foil in parallel to the magnet field. The average field intensity $H_{zm, \text{avg}}$ between the two surfaces is considered in the optimisation process as the constant magnetic field intensity for the respective conductor of the winding turn m

$$H_{zm, \text{avg}} = \frac{2m-1}{2} \frac{\hat{I}}{b} \quad m \in \langle 1, N \rangle \quad (\text{C.36})$$

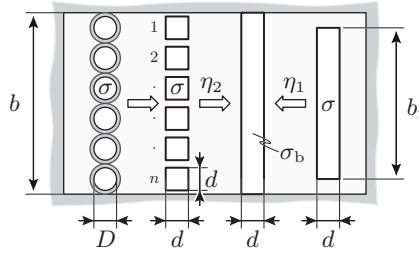


Figure C.4: Porosity factor for foils and round conductors [155, 163, 164].

where N is the turns number of the winding. The total losses in the winding with N turns can therefore be determined with the amplitude \hat{I} of the carried current and the average winding length l_{avg}

$$\begin{aligned} P_w &= R'_{\text{DC}} \left(F_F \hat{I}^2 N + G_F \sum_{m=1}^N H_{zm,\text{avg}}^2 \right) l_{\text{avg}} \\ &= R'_{\text{DC}} \left(F_F + G_F \frac{4N^2 - 1}{12b^2} \right) \hat{I}^2 N l_{\text{avg}} \quad \text{in (W)} \quad (\text{C.37}) \\ &= R_{\text{DC}} \left(F_F + G_F \frac{4N^2 - 1}{12b^2} \right) \hat{I}^2 \end{aligned}$$

where R'_{DC} is the DC-resistance per unit length as defined in (C.26) and R_{DC} is the absolute DC-winding resistance

$$R_{\text{DC}} = \frac{N l_{\text{avg}}}{\sigma b d} \quad \text{in } (\Omega). \quad (\text{C.38})$$

The presented approach for determining the winding losses can be applied for different winding arrangements, for example for interleaved or centre-tapped windings, where the calculation of the magnetic field intensity has to be adopted.

Porosity Factor for Foil Windings and Conductors If the foil winding width is smaller than the assumed winding window width $b_f < b$, cf. **Fig. C.4**, the derived formulas for the high-frequency winding losses can still be applied by transferring the winding conductivity σ to the effective conductivity σ_b [155, 164]

$$\sigma_b = \eta_i \sigma \quad i \in \langle 1, 2 \rangle \quad (\text{C.39})$$

with the porosity factors

$$\eta_1 = \frac{b_f}{b} \quad \text{and} \quad \eta_2 = \frac{n d}{b}. \quad (\text{C.40})$$

As illustrated in **Fig. C.4** round wires and split windings can be modelled with the presented approach as well with the porosity factor η_2 and projected diameter D ,

$$d = \sqrt{\frac{\pi}{4}} D. \quad (\text{C.41})$$

This approach exhibits a sufficient accuracy if the porosity factor is close to one. The accuracy can be increased by applying an improved analytical method as suggested in [164].

C.4 Orthogonality of Skin and Proximity Effect Losses

In the preceding sections, the skin and proximity losses have been investigated separately. This approach is legitimated because of the assumed uniform magnetic field, which originates from other field sources, for example adjacent windings. The uniformity results in the orthogonality of proximity and skin effect losses. The orthogonality has been proved e.g. by Ferreira in [164] and is furthermore exploited in the loss-calculation for the PWM-converter which exhibits non-sinusoidal currents with high harmonic amplitudes. As the losses due to harmonics commonly have an important influence on the losses of magnetic devices, the total losses are determined by summing the corresponding losses for each current harmonic. Because of the direct connection with the description of the skin and proximity losses, the orthogonality derivation is briefly summarised in the following based on [149, 164] for the sake of completeness.

The Fourier-series of a non-sinusoidal current with the complex Fourier-coefficients \mathbf{I}_ν where ν denominates the ν^{th} harmonic is given by

$$I(t) = \mathbf{I}_0 + \mathbf{I}_1 \cos(\omega t) + \dots + \mathbf{I}_\nu \cos(\nu \omega t) + \dots \quad (\text{C.42})$$

and the corresponding current density is \mathbf{J}_ν in the conductor, which carries a current in direction of x , is only dependent on the coordinates

y and z ,

$$J(y, z, t) = \mathbf{J}_0(y, z) + \mathbf{J}_1(y, z) \cos(\omega t) + \dots + \mathbf{J}_\nu(y, z) \cos(\nu \omega t) + \dots \quad (\text{C.43})$$

The frequency-dependent power dissipation per unit length P'_w in the conductor can now be calculated with

$$P'_w = \frac{1}{\sigma T} \int_A \int_0^T |J(y, z, t)|^2 dt dA \quad (\text{C.44})$$

where T is the period and A is the cross-sectional area of the conductor. Due to the orthogonality of the cosine functions, only the integrals with cosine functions of same frequency result in a non-zero value, i.e.

$$\int_0^{2\pi} \cos(\alpha \omega t) \cdot \cos(\beta \omega t) d\omega t \quad \begin{cases} = 0 & \text{for } \alpha \neq \beta \\ \neq 0 & \text{for } \alpha = \beta \end{cases}$$

and therefore (C.44) can be written as

$$P_u = \frac{1}{2\sigma} \sum_{i=0}^{\infty} \int_A \mathbf{J}_i \cdot \mathbf{J}_i^* dA. \quad (\text{C.45})$$

The equation (C.45) becomes

$$P'_w = \frac{1}{2\sigma} \sum_{\nu=0}^{\infty} \int_A (\mathbf{J}_{s\nu} + \mathbf{J}_{p\nu})(\mathbf{J}_{s\nu}^* + \mathbf{J}_{p\nu}^*) dA \quad (\text{C.46})$$

by designating the resulting current densities due to the skin and proximity effect (\mathbf{J}_s and \mathbf{J}_p). If an axis of symmetry can be found for the conductors and the magnetic field is uniform and in parallel to this symmetry axis, the induced current distribution \mathbf{J}_p shows a reciprocal symmetry [164] and therefore, the integral parts for the area consisting of the product of J_p and J_s are zero, i.e.

$$\int_A J_s J_p dA = 0 \quad (\text{C.47})$$

and therefore (C.46) can be simplified to

$$\begin{aligned} P'_w &= \frac{1}{2\sigma} \sum_{\nu=0}^{\infty} \int_A (\mathbf{J}_{s\nu} \mathbf{J}_{s\nu}^* + \mathbf{J}_{p\nu} \mathbf{J}_{p\nu}^*) dA \\ &= \sum_{\nu=0}^{\infty} P'_{s\nu} + P'_{p\nu} \end{aligned} \quad \square \quad (\text{C.48})$$

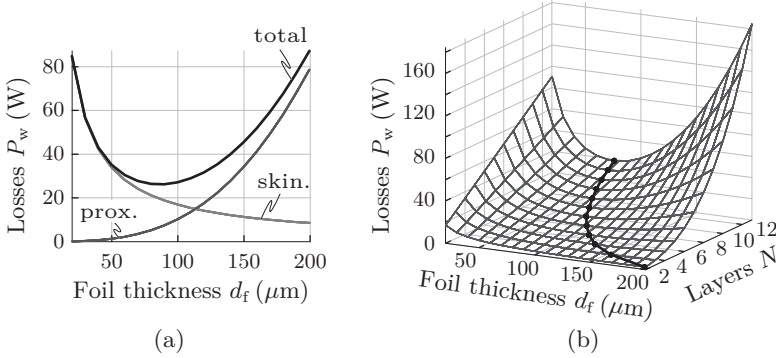


Figure C.5: High-frequency losses in foil conductors. (a) Skin and proximity losses in dependency of the foil thickness d (b) Total HF-winding losses in dependency of the foil thickness and numbers of layers *Underlying parameters: Copper foil, $\sigma = 5.9 \cdot 10^7 \Omega^{-1} \text{m}^{-1}$, $b=50 \text{ mm}$, $\hat{I}=100 \text{ A}$, $f=100 \text{ kHz}$.*

where $P'_{s\nu}$ and $P'_{p\nu}$ are the losses per unit length due to skin and proximity effect for the ν^{th} harmonic.

C.5 Optimal Foil Thickness

In the previous subsections, the equations for determining the losses due to the skin and proximity effect ((C.25) and (C.32)) have been derived. The losses in dependency of the foil thickness are illustrated in **Fig. C.5(a)** for a specific set of parameters. The losses due to the skin effect are decreasing with the foil thickness d but the proximity effect in contrary increases; accordingly, an optimal foil thickness d_{opt} can numerically be determined, however, an analytical solution cannot directly be derived from (C.25) and (C.32).

Hurley et al. [155] approximated the frequency-dependent factors F_F and G_F , cf. (C.27) and (C.31), in order to find an analytical solution

for the foil thickness resulting in minimum losses:

$$\frac{\sinh(\Delta) + \sin(\Delta)}{\cosh(\Delta) - \cos(\Delta)} \approx \frac{2}{\Delta} + \frac{1}{90}\Delta^3 - \frac{1}{37800}\Delta^7 + O(\Delta^{11}) \quad (\text{C.49})$$

$$\frac{\sinh(\Delta) - \sin(\Delta)}{\cosh(\Delta) + \cos(\Delta)} \approx \frac{1}{6}\Delta^3 - \frac{17}{2520}\Delta^7 + O(\Delta^{11}). \quad (\text{C.50})$$

If only the polynomial up to the third order is considered, the relative error incurred in (C.49) is less than 1.2 %, and less than 8.4 % for (C.50) if $\Delta < 1.2$ [155]. As the ratio Δ is commonly in the range of 0.3 to 1, the approximation is sufficiently accurate. The derivation of an analytical expression for the optimal foil thickness based on the above proposed approximation is present in the following based on Hurley's articulate journal paper from 2000 [155].

Inserting the approximations (C.49) and (C.50) in (C.37), the winding losses P_w for sinusoidal currents with the switching frequency f are given by

$$P_w \approx R_{\text{DC}} \left[\left(\frac{1}{2} + \frac{\Delta^4}{360} \right) + \left(\frac{\Delta^4}{72} (4N^2 - 1) \right) \right] \hat{I}^2 \quad (\text{C.51})$$

where Δ is the foil-thickness-to-skin-depth ratio above defined in (C.24) and R_{DC} is the absolute DC-winding-resistance cf. (C.38)

$$\Delta = \frac{d}{\delta_0} = d \sqrt{\pi f \sigma \mu_0}$$

$$R_{\text{DC}} = \frac{N l_{\text{avg}}}{\sigma b h} \quad \text{in } (\Omega).$$

Simplifying (C.51) results in

$$P \approx R_{\text{DC}} \left[1 + \frac{\Psi}{3} \Delta^4 \right] \left(\frac{\hat{I}}{\sqrt{2}} \right)^2 \quad (\text{C.52})$$

where Ψ is defined following Hurley [155] as

$$\Psi = \frac{5N^2 - 1}{15} \quad (\text{C.53})$$

and the term $\hat{I}/\sqrt{2} = I$ represents the RMS-value of the sinusoidal winding current I . Dividing (C.52) by the RMS-winding current I and

the absolute DC-winding resistance R_{DC} , an expression for the ratio between the absolute AC- and DC-resistance results

$$\frac{R_{\text{AC}}}{R_{\text{DC}}} \approx 1 + \frac{\Psi}{3} \Delta^4 \quad (\text{C.54})$$

because the winding losses can be defined also as $P_{\text{w}} = R_{\text{AC}} I^2$.

For the generalisation of the above presented equations, an arbitrary period current waveform is represented by its Fourier-series, i.e.

$$i(t) = I_{\text{DC}} + \sum_{\nu=1}^{\infty} \hat{I}_{\nu} \cos(\nu \omega t + \phi_{\nu}), \quad (\text{C.55})$$

where \hat{I}_{ν} is the magnitude of the ν^{th} current harmonic and $I_{\nu} = \hat{I}_{\nu}/\sqrt{2}$ represents the corresponding RMS-value. The total winding losses can further be defined as

$$P_{\text{w}} = R_{\text{DC}} I_{\text{DC}}^2 + R_{\text{DC}} \sum_{\nu=1}^{\infty} k_{\text{p}\nu} I_{\nu}^2 \quad (\text{C.56})$$

where $k_{\text{p}\nu}$ is the AC-resistance factor at the ν^{th} harmonic which can be derived from (C.37) with the factors F_{F} and G_{F} , cf. (C.27) and (C.31),

$$\begin{aligned} k_{\text{p}\nu} = \frac{\sqrt{\nu} \Delta}{2} & \left(\frac{\sinh(\sqrt{\nu} \Delta) + \sin(\sqrt{\nu} \Delta)}{\cosh(\sqrt{\nu} \Delta) - \cos(\sqrt{\nu} \Delta)} + \dots \right. \\ & \left. \dots + \frac{4N^2 - 1}{3} \frac{\sinh(\sqrt{\nu} \Delta) - \sin(\sqrt{\nu} \Delta)}{\cosh(\sqrt{\nu} \Delta) + \cos(\sqrt{\nu} \Delta)} \right) \end{aligned} \quad (\text{C.57})$$

or, following Hurely et al. in [155], as

$$\begin{aligned} k_{\text{p}\nu} = \sqrt{\nu} \Delta & \left(\frac{\sinh(2\sqrt{\nu} \Delta) + \sin(2\sqrt{\nu} \Delta)}{\cosh(2\sqrt{\nu} \Delta) - \cos(2\sqrt{\nu} \Delta)} + \dots \right. \\ & \left. \dots + \frac{2(N^2 - 1)}{3} \frac{\sinh(\sqrt{\nu} \Delta) - \sin(\sqrt{\nu} \Delta)}{\cosh(\sqrt{\nu} \Delta) + \cos(\sqrt{\nu} \Delta)} \right). \end{aligned} \quad (\text{C.58})$$

Both equations (C.57) and (C.58) are similar, which can be determined by substituting the following transformation (C.59) (taken from Ferreira [164]) in (C.58).

$$\begin{aligned} \frac{\sinh(2\alpha) + \sin(2\alpha)}{\cosh(2\alpha) - \cos(2\alpha)} &= \\ \frac{1}{2} \left[\frac{\sinh(\alpha) + \sin(\alpha)}{\cosh(\alpha) - \cos(\alpha)} + \frac{\sinh(\alpha) - \sin(\alpha)}{\cosh(\alpha) + \cos(\alpha)} \right]. \end{aligned} \quad (\text{C.59})$$

Substituting the definition of an effective AC-resistance resulting from

$$P_w = R_{\text{eff}} I^2 \quad (\text{C.60})$$

where I is the RMS-value of the winding current $i(t)$, the ratio between the effective and the DC-resistance is given by

$$\frac{R_{\text{eff}}}{R_{\text{DC}}} = \frac{I_{\text{DC}}^2 + \sum_{\nu=1}^{\infty} k_{p\nu} I_{\nu}^2}{I^2}. \quad (\text{C.61})$$

Using the found equation for the approximated AC-to-DC-resistance ratio (C.54) and defining the skin depth $\delta_{\nu} = \delta_0 / \sqrt{\nu}$ of the ν^{th} harmonic, the approximated AC-resistance factor is given by

$$k_{p\nu} \approx 1 + \frac{\Psi}{3} \nu^2 \Delta^4. \quad (\text{C.62})$$

The resistance ratio can be approximated by substituting (C.62) in (C.61) as

$$\frac{R_{\text{eff}}}{R_{\text{DC}}} \approx \frac{I_{\text{DC}}^2 + \sum_{\nu=1}^{\infty} I_{\nu}^2 + \frac{\Psi}{3} \Delta^4 \sum_{\nu=1}^{\infty} \nu^2 I_{\nu}^2}{I^2}, \quad (\text{C.63})$$

where the RMS-value of the winding current I can further be expressed by

$$I^2 = I_{\text{DC}}^2 + \sum_{\nu=1}^{\infty} I_{\nu}^2. \quad (\text{C.64})$$

The differentiation of the current $i(t)$ with respect to time, cf. (C.55), is resulting as

$$\frac{d}{dt} i(t) = i'(t) = -\omega \sum_{\nu=1}^{\infty} \nu \hat{I}_{\nu} \sin(\nu \omega t + \phi_{\nu}) \quad (\text{C.65})$$

and the RMS-value of the time derivative can be determined [155, 162] with

$$I'^2 = \omega^2 \sum_{\nu=1}^{\infty} \frac{1}{2} \nu^2 \hat{I}_{\nu}^2 = \omega^2 \sum_{\nu=1}^{\infty} \nu^2 I_{\nu}^2 \quad (\text{C.66})$$

and substituted in (C.63) using (C.64), resulting in

$$\frac{R_{\text{eff}}}{R_{\text{DC}}} \approx 1 + \frac{\Psi}{3} \Delta^4 \left[\frac{I'}{\omega I} \right]^2. \quad (\text{C.67})$$

The effective resistance can be approximated by this expression for an arbitrary waveform and may be calculated without determining the Fourier coefficients for known functions listed in [155].

The final step is the determination of the optimum foil thickness d_{opt} which results in the minimum AC-resistance. According to [155], the DC-resistance R_δ of a foil conductor with the thickness δ_0 is defined as

$$\frac{R_\delta}{R_{\text{DC}}} = \frac{d}{\delta_0} = \Delta \quad (\text{C.68})$$

which implies that

$$\frac{R_{\text{eff}}}{R_{\text{DC}}} = \Delta \frac{R_{\text{eff}}}{R_\delta}. \quad (\text{C.69})$$

Substituting (C.69) in the approximation (C.67) results in

$$\frac{R_{\text{eff}}}{R_\delta} = \frac{1}{\Delta} + \frac{\Psi}{3} \Delta^3 \left[\frac{I'}{\omega I} \right]^2. \quad (\text{C.70})$$

The optimum foil thickness

$$d_{\text{opt}} = \Delta_{\text{opt}} \delta_0 \quad (\text{C.71})$$

can be found by setting the derivative of (C.70) equal to zero,

$$\frac{d}{d\Delta} \frac{R_{\text{eff}}}{R_\delta} = -\frac{1}{\Delta^2} + \Psi \Delta^2 \left[\frac{I'}{\omega I} \right]^2, \quad (\text{C.72})$$

and solving (C.72) for Δ which finally results in

$$\Delta_{\text{opt}} = \frac{1}{\sqrt[4]{\Psi}} \sqrt{\frac{\omega I}{I'}}; \quad (\text{C.73})$$

the optimum foil thickness now can be determined with

$$d_{\text{opt}} = \frac{1}{\sqrt[4]{\Psi}} \sqrt{\frac{\omega I}{I'}} \delta_0. \quad (\text{C.74})$$

Note that the substitution of (C.73) in (C.67) results in the optimum ratio of effective AC- and DC-resistance for any arbitrary winding current waveform,

$$\left. \frac{R_{\text{eff}}}{R_{\text{DC}}} \right|_{\text{opt}} = \frac{4}{3}, \quad (\text{C.75})$$

which has been established for sinusoidal currents e.g. in [168].

Hurley et al. listed the analytical equations of RMS-current values I and their time derivatives I' for several common current waveforms in [155]. For sinusoidal currents, for instance, the RMS-value and its time derivative are given by

$$I = \frac{\hat{I}}{\sqrt{2}} \quad \text{and} \quad I' = \omega \frac{\hat{I}}{\sqrt{2}}$$

and therefore the optimal foil thickness is given by

$$d_{\text{opt},\sin} = \frac{1}{\sqrt[4]{\Psi}} \delta_0. \quad (\text{C.76})$$

In the optimisation process, for example in section 3.1, the time derivative RMS-current values are additionally determined for the transformer and inductor winding for each operating point. By applying (C.74), the optimal foil thickness is calculated in the inner optimisation process to determine the transformer and inductor geometry. This approach enables the reduction of free design parameters in the optimisation and thereby the computation time is reduced.



Indirect Forced Air Cooling (Thermal Model Derivation)

The specified temperature limit for the applied materials (winding, insulation, and core) must be observed during the inner optimisation process of the transformer of the high-power-density converter. A thermal model of the transformer which describes the temperature distribution in dependency of the geometry parameters is necessary for that reason. The derivation of this model is introduced in this section, starting with a brief summary of the basic physical heat transmission mechanisms. The thermal model applied is based on transmission line equations (also known as the telegrapher's equation), which essentially describes the voltage and current propagation along electrical conductors of a transmission line. The derivation of the underlying equivalent circuit is described in section D.2. As a last point, the differential equations for the transformer design for indirect forced air cooling are derived in section D.3.

D.1 Physical Heat Transmission Mechanisms

There are basically three physical mechanisms which characterise the heat transfer from a place with a higher temperature to a place where the temperature is lower, for example from a heat (loss) source to the ambient:

- ▶ heat conduction
- ▶ heat convection

► heat radiation.

The calculation of the three-dimensional heat propagation is very complex and the solution of the partial non-linear differential equations is usually only possible with numerical techniques (Computational Fluid Dynamics (CFD), using e.g. FEM). The numerical determination of the heat propagation is due to the complexity and computational effort not practicable in the optimisation process. Therefore, only one-dimensional analytical equations are applied (similar as for the calculation of the winding losses) which are partly based on empirical relationships.

The heat flow rate \dot{Q} (the partial derivative of the total amount of energy transferred as heat Q with respect to time t) due to heat conduction is described by Fourier's law¹ which can be simplified for the considered one-dimensional approach to

$$\dot{Q} = \phi_q A = -\lambda A \frac{\partial T}{\partial x} \quad (\text{W}) \quad (\text{D.1})$$

which is further simplified with the assumption of a homogeneous heat flux distribution

$$\dot{Q} = -\lambda A \frac{T_1 - T_2}{\Delta x} \quad (\text{W})$$

with

$\lambda \dots$ thermal conductivity	(W/m K)
$\phi_q \dots$ heat flux	(W/m ²)
$A \dots$ cross-sectional area	(m ²)
$T_1, T_2 \dots$ temperatures at start/end position ($T_1 > T_2$) in	(K)
$\Delta x \dots$ length of heat flux path	(m).

The equation to determine the thermal resistance with the assumption of a homogeneous flux distribution in the material is given by

$$R_{\text{th},\lambda} = \frac{l}{\lambda A} \quad \left(\frac{\text{K}}{\text{W}} \right) \quad (\text{D.2})$$

where l is the length of the heat-conduction path.

¹This equation originates from Biot according to the publications in 1804 and 1816, however, it's commonly named after Fourier who used it 1822 as a fundamental equation in his analytical theory of heat [209].

Free or forced heat convection can be seen as special cases of the heat conduction based on the movement of molecules within fluids, i.e. gases and liquids. The heat flow rate through heat convection is described by Newton's law (one-dimensional, homogeneous)

$$\dot{Q} = \alpha A (T_S - T_F) \quad (\text{W}) \quad (\text{D.3})$$

with

$$\begin{aligned} \alpha &\dots \text{convection coefficient} && (\text{W}/\text{m}^2 \text{K}) \\ T_S &\dots \text{surface temperature} && (\text{K}) \\ T_F &\dots \text{fluid temperature} && (\text{K}) \end{aligned}$$

and the corresponding thermal resistance is defined as

$$R_{\text{th},\alpha} = \frac{\Delta T}{\dot{Q}} = \frac{1}{\alpha A} \quad \left(\frac{\text{K}}{\text{W}} \right), \quad (\text{D.4})$$

which characterises the heat transmission from a surface to a fluid, e.g. the air flow generated by a fan (forced cooling). The convection coefficient α is depending on the nature of transmission described by fluid-mechanics characteristic values (such as Reynold number Re , Prandtl number Pr , Grashof number Gr , Rayleigh number Ra) and commonly based on empirical considerations. (A summary of some typical cases related to magnetic components and the corresponding determination of α is e.g. given in [149, 169, 206]).

The heat radiation describes the heat transmission from a surface via electromagnetic waves and the radiated heat flux rate is given by Stefan-Boltzmann's law

$$\dot{Q} = \epsilon \sigma A (T_S^4 - T_A^4) \quad (\text{W}) \quad (\text{D.5})$$

where the Stefan-Boltzmann constant σ is defined as

$$\sigma = \frac{2\pi^5 k^4}{15 h^3 c^2} \quad \left(\frac{\text{W}}{\text{K}^4 \text{m}^2} \right) \quad (\text{D.6})$$

with

ϵ ... emissivity of the radiating material	(1)
σ ... Stefan-Boltzmann constant, $\sigma \approx 5.67 \cdot 10^{-8}$	(W/m ² K)
k ... Boltzmann constant, $k \approx 1.38 \cdot 10^{-23}$	(J/K)
c ... speed of light, $c \approx 3.00 \cdot 10^8$	(m/s)
h ... Planck constant, $h \approx 6.63 \cdot 10^{-34}$	(J s)
T_S ... surface temperature	(K)
T_A ... ambient temperature	(K).

The corresponding thermal resistance describing the heat radiation is given by

$$R_{\text{th},\sigma} = \frac{\Delta T}{\dot{Q}} = \frac{1}{\alpha_r A} \quad \left(\frac{\text{K}}{\text{W}} \right) \quad (\text{D.7})$$

where α_r is a heat transfer coefficient defined as

$$\alpha_r = \frac{\epsilon \sigma (T_S^4 - T_A^4)}{T_S - T_A} \quad \left(\frac{\text{W}}{\text{K m}^2} \right). \quad (\text{D.8})$$

The heat transfer coefficient is commonly determined empirically based on measurements for special setups and surfaces.

D.2 Transmission Line Equations

Electrical engineers try to describe physical relations of non-electrical fields of expertise with equivalent electric circuits where the well-known physical laws of the electrical engineering can be applied. One example is the electrical-equivalent description of thermal systems. According to this model, an electrical resistance corresponds with a thermal resistance, a voltage drop corresponds with a temperature drop over a thermal resistance and the electrical current corresponds with the heat flux rate or the power losses, respectively. Furthermore, there is an equivalent thermal capacitance. Accordingly, for the determination of the heat propagation, the electrical counterpart describing the voltage and current of an electrical transmission line with respect to distance and time can be applied, which can be calculated with a pair of linear differential equations – the so-called transmission line or telegrapher's

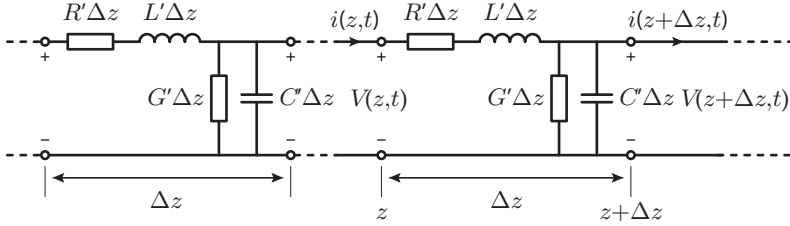


Figure D.1: The per-unit-length model used for deriving the transmission-line equation as presented in [175] .

equations. The derivation of the transmission line equation for a basic cell is described based on [175] in the following.

The derivation of the transmission line equations in [175] is based on a per-unit-length model of infinitesimal short line sections, as presented in **Fig. D.1**, where the elements, i.e. the line resistance R , the line inductance L , the capacitance between the two conductors C and the conductance G of the dielectric material separating the two conductors are described by the corresponding per-unit length values R' , L' , C' and G' . An expression for the difference between input and output voltage for a single section can be obtained directly from **Fig. D.1** as

$$V(z + \Delta z, t) - V(z, t) = -R' \Delta z I(z, t) - L' \Delta z \frac{\partial I(z, t)}{\partial t}. \quad (\text{D.9})$$

The equation for the input and output current for a single section is given cf. **Fig. D.1** by

$$I(z + \Delta z, t) - I(z, t) = -G' \Delta z V(z + \Delta z, t) - C' \Delta z \frac{\partial V(z + \Delta z, t)}{\partial t}. \quad (\text{D.10})$$

The first transmission-line equation can be derived from (D.9) by dividing by Δz and evaluating the limiting case $\Delta z \rightarrow 0$

$$\begin{aligned} \lim_{\Delta z \rightarrow 0} \frac{V(z + \Delta z, t) - V(z, t)}{\Delta z} &= \frac{\partial V(z, t)}{\partial z} \\ &= -R' I(z, t) - L' \frac{\partial I(z, t)}{\partial t}. \end{aligned} \quad (\text{D.11})$$

For deriving the second transmission-line equation from (D.10) first (D.10) is divided by Δz and $V(z + \Delta z, t)$ is substituted by (D.9) res-

ulting in

$$\begin{aligned} \frac{I(z + \Delta z, t) - I(z, t)}{\Delta z} &= -G' V(z, t) - C' \frac{\partial V(z, t)}{\partial t} + \dots \\ \dots + \Delta z \left[G' R' I(z, t) + (G' L' + R' C') \frac{\partial I(z, t)}{\partial t} + L' C' \frac{\partial^2 I(z, t)}{\partial t^2} \right]. \end{aligned} \quad (\text{D.12})$$

Considering the limiting case $\Delta z \rightarrow 0$ (D.12) results in the second transmission-line equation

$$\frac{\partial I(z, t)}{\partial z} = -G' V(z, t) - C' \frac{\partial V(z, t)}{\partial t}. \quad (\text{D.13})$$

The derivation of the transmission-line equations up to this point is already sufficient for the further thermal modelling because the per-unit-length model in **Fig. D.1** is simplified by excluding the inductance and further neglecting the (thermal) capacitance due to steady-state considerations. As a result of the neglect of the storage elements, the transmission-line equations become independent of the time t , i.e. only the static voltage drop and current distribution of a lossy conductor is considered. The time- and therefore frequency-independence are satisfactory for the thermal modelling as the time constants of the heat propagation under the steady-state conditions are comparatively large. The transmission-line equations (D.11) and (D.13) can consequently be simplified to

$$\frac{\partial V(z)}{\partial z} = -R' I(z) \quad (\text{D.14})$$

and

$$\frac{\partial I(z)}{\partial z} = -G' V(z). \quad (\text{D.15})$$

By substituting $V(z)$ in (D.14) with (D.15) the linear differential equation of the current distribution can be found

$$\frac{\partial^2 I(z)}{\partial z^2} = R' G' I(z). \quad (\text{D.16})$$

which can be projected to the distribution of the losses or heat flux rate in the corresponding thermal equivalent circuit.

Equation (D.16) can be applied directly to determine the temperature distribution of heat transfer components as shown in the next subsection. The simplified differential equation (D.16), however, has to be extended for the more complex subsections of the thermal model as shown below.

D.3 Derivation of the Temperature Distribution

All three heat-transmission mechanisms summarised in section D.1 – conduction, convection, radiation – contribute to the heat transfer in magnetic components. For high-density power electronic systems the surface areas available for free convection and heat radiation are reduced whereas the losses are potentially increased, cf. chapter 3. In order to keep the specified material temperature limits for magnetic devices with reduced surface area, forced air or liquid cooling methods are applied, which support the heat transfer mechanism.

In [161], Biela introduced an advanced cooling method where the available surface area is further increased by connecting the magnetic device with a heat sink via Heat Transfer Components (HTC). The convection coefficient α could thereby be increased by more than factor 100. This indirect forced air cooling method has been applied for the high-power-density systems presented in chapter 2 and the underlying thermal model is derived in the following.

In **Fig. D.2** a section of the cut through the transformer cooling system is illustrated. A high-performance fan generates the air flow through the heat sink, which is connected via a gap-filling thermally conductive material with the heat transfer component (HTC), cf. section ① in **Fig. D.2** on page 298. A gap is indicated in section ②, cf. **Fig. D.2**, between the magnetic device and the heat sink. In the series-parallel-resonant converter this gap has been used as intake air-channel. However, the gap is not necessarily present in the assembly, cf. for instance the final design of the high-power-density PWM converter with integrated current doubler in section 2.2. The thermal connection of the transformer is divided in three sections according to **Fig. D.2**: in section ③, only the losses in the core are injected into the HTC; in section ④, the winding and the core inject heat, and in section ⑤, heat is again injected only by the core into the HTC.

The applied thermal model is introduced below for the corresponding sections of the cooling system in **Fig. D.2**. It is assumed, that only the heat conduction mechanism is involved in the heat transfer, i.e. the heat dissipation due to free convection and radiation at the surface of the converter is neglected. This approach results in a worst-case approximation for the temperature distribution of the transformer. The eventual error is rather small because of the efficient cooling method as

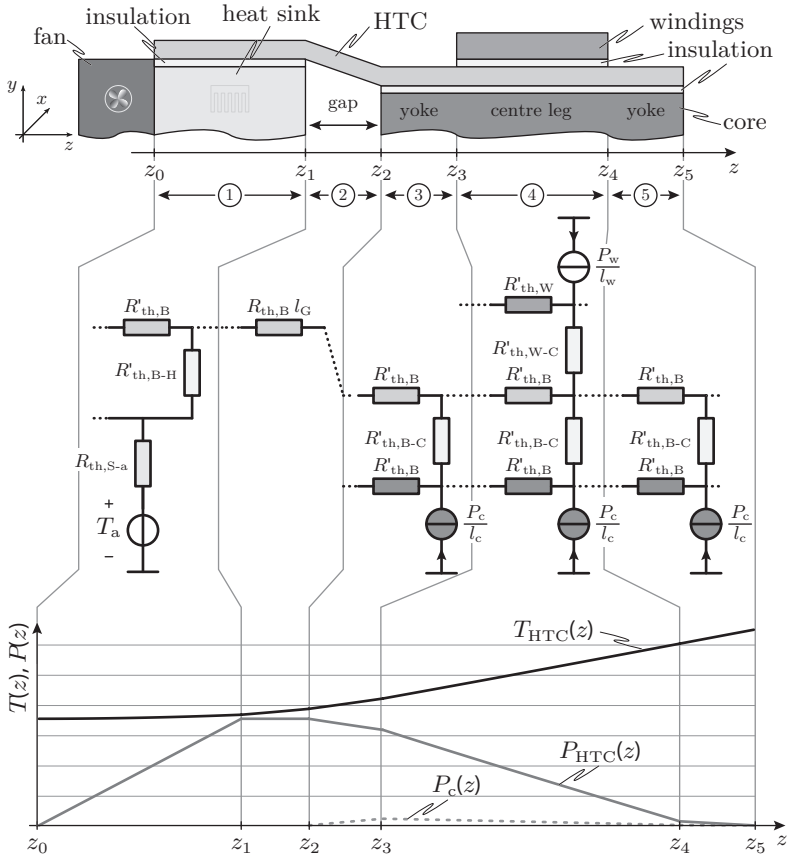


Figure D.2: Cut through the transformer and the applied indirect forced air cooling system and the corresponding equivalent thermal model based on transmission-line equations.

shown in [161].

Section ① describes the heat transfer from the HTC to the surface of the heat sink via the thermally conductive gap filler, which could be for example thermal grease or an additional insulation material. The heat sink and the corresponding thermal resistance $R_{th,H-A}$ is determined with the CSPI [154] similar to the evaluation of the semiconductor cooling system (cf. section 2.1.2). The applied per-unit-length model

described above and the corresponding transmission-line equations in section ① are consequently restricted to the HTC with the thermal resistance per unit length $R'_{\text{th,B}}$ in direction of z and the thermal transition layer with the resistance $R_{\text{th,B-H}}$ in direction of y . The heat-flux rate or loss distribution as function of the position in direction of z can be determined in analogy to the derivation of the electrical transmission line equations as presented above in section D.2. As the current in the electrical circuit is equivalent to the power losses in the equivalent thermal circuit, (D.16) can directly be applied to describe the power loss distribution $P_{\text{HTC}}(z)$ in the HTC for $z_0 \leq z \leq z_1$,

$$\frac{\partial^2}{\partial z^2} P_{\text{HTC}}(z) = P_{\text{HTC}}(z) \frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}, \quad (\text{D.17})$$

with the initial conditions

$$\begin{aligned} P_{\text{HTC}}(z_0) &= 0 \\ P_{\text{HTC}}(z_1) &= -(P_c + P_w), \end{aligned} \quad (\text{D.18})$$

assuming that the entire losses (winding losses P_w and core losses P_c) are transferred via the HTC to the heat sink. The solution of (D.17) with the initial conditions (D.18) is

$$P_{\text{HTC}}(z) = -(P_c + P_w) \frac{\sinh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z\right)}{\sinh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z_1\right)}. \quad (\text{D.19})$$

The temperature distribution $T_{\text{HTC}}(z)$ in the HTC as function of the position z can be found by integrating the loss-distribution function $P_{\text{HTC}}(z)$ along the path z ,

$$T_{\text{HTC}}(z) = - \int_{z_0}^{z_1} P_{\text{HTC}}(\tilde{z}) R'_{\text{th,B}} d\tilde{z} + T_{\text{HS}}, \quad (\text{D.20})$$

which results in

$$\begin{aligned} T_{\text{HTC}}(z) &= (P_c + P_w) \sqrt{R'_{\text{th,B}} R'_{\text{th,B-H}}} \cdot \dots \\ &\dots \cdot \frac{1 - \cosh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z\right)}{\sinh\left(\sqrt{\frac{R'_{\text{th,B}}}{R'_{\text{th,B-H}}}} z_1\right)} + T_{\text{HS}} \end{aligned} \quad (\text{D.21})$$

where T_{HS} is the surface temperature of the heat sink which is assumed to be isothermal due to the high thermal conductivity of the heat sink material.

Section ②: The loss-distribution $P_{\text{HTC}}(z)$ in the possibly applied gap between the heat sink and the transformer is constant with the assumption that no heat is dissipated via radiation or free convection, i.e. for $z_1 < z \leq z_2$ follows

$$P_{\text{HTC}}(z) = -(P_c + P_w). \quad (\text{D.22})$$

The resulting temperature distribution in the HTC in this section is linear

$$T_{\text{HTC}}(z) = -(P_c + P_w)(z - z_1) R'_{\text{th,B}} + T_{\text{HTC}}(z_1). \quad (\text{D.23})$$

In **section ③**, the core losses are injected into the HTC above the yoke. The transmission line model has to be extended by the corresponding losses per unit length $P'_c = P_c/l_c$, where P_c are the total losses and l_c is the length of the core in direction of z , the thermal resistance per unit length $R'_{\text{th,C}}$ as illustrated in **Fig. D.2**. The limit-determination for the mesh and two node equations for $z_2 < z \leq z_3$ result in

$$\frac{\partial}{\partial z} T(z) = -R'_{\text{th,C}} P_c(z) - R'_{\text{th,B}} P_{\text{HTC}}(z) \quad (\text{D.24})$$

$$\frac{\partial}{\partial z} P_{\text{HTC}}(z) = -\frac{T(z)}{R'_{\text{th,B-C}}} \quad (\text{D.25})$$

$$\frac{\partial}{\partial z} P_c(z) = -\frac{T(z)}{R'_{\text{th,B-C}}} - \frac{P_c}{l_c}, \quad (\text{D.26})$$

where $T(z)$ is the temperature drop between HTC and core surface. The transmission line equations are derived from (D.24), (D.25), and (D.26) as

$$\frac{\partial^2}{\partial z^2} P_{\text{HTC}}(z) = \frac{R'_{\text{th,C}}}{R'_{\text{th,B-C}}} P_c(z) + \frac{R'_{\text{th,B}}}{R'_{\text{th,B-C}}} P_{\text{HTC}}(z) \quad (\text{D.27})$$

$$\frac{\partial}{\partial z} P_c(z) = \frac{\partial}{\partial z} P_{\text{HTC}}(z) - \frac{P_c}{l_c}. \quad (\text{D.28})$$

The initial condition at the left end of the transformer core ($z = z_2$) are given by

$$\begin{aligned} P_{\text{HTC}}(z_2) &= -(P_c + P_w) \\ P_c(z_2) &= 0. \end{aligned} \quad (\text{D.29})$$

The initial conditions for $z = z_3$ are depending on the loss equations of the next section and vice versa. The differential equations for the respective core section ③, ④ and ⑤ have to be solved simultaneously for that reason. The temperature distribution in this section can be calculated with

$$T_{\text{HTC}}(z) = - \int_{z_2}^{z_3} P_{\text{HTC}}(\tilde{z}) R'_{\text{th,B}} d\tilde{z} + T_{\text{HTC}}(z_2). \quad (\text{D.30})$$

In **section ④** the losses are induced from the core P_c and the windings P_w into the heat transfer component. The limit-determination of the corresponding two mesh and three node equations results in (for $z_3 < z \leq z_4$)

$$\text{upper mesh} \quad \frac{\partial}{\partial z} T_u(z) = -R'_{\text{th,W}} P_w(z) - R'_{\text{th,B}} P_{\text{HTC}}(z) \quad (\text{D.31})$$

$$\text{lower mesh} \quad \frac{\partial}{\partial z} T_l(z) = -R'_{\text{th,C}} P_c(z) - R'_{\text{th,B}} P_{\text{HTC}}(z) \quad (\text{D.32})$$

and

$$\text{upper node} \quad \frac{\partial}{\partial z} P_w(z) = -\frac{T_u(z)}{R'_{\text{th,B-W}}} - \frac{P_w}{l_w} \quad (\text{D.33})$$

$$\text{middle node} \quad \frac{\partial}{\partial z} P_{\text{HTC}}(z) = -\frac{T_u(z)}{R'_{\text{th,B-W}}} - \frac{T_l(z)}{R'_{\text{th,B-C}}} \quad (\text{D.34})$$

$$\text{lower node} \quad \frac{\partial}{\partial z} P_c(z) = -\frac{T_l(z)}{R'_{\text{th,B-C}}} - \frac{P_c}{l_c}, \quad (\text{D.35})$$

where the upper mesh voltage $T_u(z)$ describes the temperature drop between the windings and the HTC and $T_l(z)$ is the temperature drop between the core surface and the HTC. The length of the middle core segments is similar to the winding width ($l_c - 2l_y = l_w$ where $l_y = z_3 - z_2$ is the length of the yoke). From these equations, a set of transmission line equations can be stated

$$\frac{\partial^2}{\partial z^2} P_c(z) = \frac{R'_{\text{th,C}}}{R'_{\text{th,B-C}}} P_c(z) + \frac{R'_{\text{th,B}}}{R'_{\text{th,B-C}}} P_{\text{HTC}}(z) \quad (\text{D.36})$$

$$\frac{\partial^2}{\partial z^2} P_w(z) = \frac{R'_{\text{th,W}}}{R'_{\text{th,B-W}}} P_w(z) + \frac{R'_{\text{th,B}}}{R'_{\text{th,B-W}}} P_{\text{HTC}}(z) \quad (\text{D.37})$$

$$\frac{\partial}{\partial z} P_{\text{HTC}}(z) = \frac{\partial}{\partial z} P_w(z) + \frac{\partial}{\partial z} P_c(z) + \frac{P_w}{l_w} + \frac{P_c}{l_c}. \quad (\text{D.38})$$

The initial conditions at the boundaries of the sections are given by

$$\begin{aligned}
 P_w(z_3) &= 0 & P_w(z_4) &= 0 \\
 P_{\text{HTC}}(z_{3-}) &= P_{\text{HTC}}(z_{3+}) & P_{\text{HTC}}(z_{4-}) &= P_{\text{HTC}}(z_{4+}) \\
 P_c(z_{3-}) &= P_c(z_{3+}) & P_c(z_{4-}) &= P_c(z_{4+}).
 \end{aligned} \tag{D.39}$$

Once the differential equations are solved together with the corresponding transmission line equations of ③ and ⑤, the temperature distribution can be calculated

$$T_{\text{HTC}}(z) = - \int_{z_3}^{z_4} P_{\text{HTC}}(\tilde{z}) R'_{\text{th,B}} d\tilde{z} + T_{\text{HTC}}(z_3). \tag{D.40}$$

In **section ⑤** the transmission line equations are similar to section ③, cf. (D.27) and (D.28). The additional conditions for $z_4 < z \leq z_5$ are

$$\begin{aligned}
 P_{\text{HTC}}(z_5) &= 0 \\
 P_c(z_5) &= 0 \\
 \frac{\partial^2}{\partial z^2} P_{\text{HTC}} \big|_{z=z_5} &= 0.
 \end{aligned} \tag{D.41}$$

The corresponding temperature distribution in the heat transfer component is given by

$$T_{\text{HTC}}(z) = - \int_{z_4}^{z_5} P_{\text{HTC}}(\tilde{z}) R'_{\text{th,B}} d\tilde{z} + T_{\text{HTC}}(z_4). \tag{D.42}$$

The system of differential equations for section ③ - ⑤ can now be solved and the eleven independent constants can be determined with the given initial conditions².

The temperature distributions are determined by integrating the heat distribution over the length of the corresponding sections, cf. (D.20), (D.23), (D.30), (D.40) and (D.42), which results in the temperature distribution shown in **Fig. D.2**. With the assumption, that no heat is dissipated due to convection or radiation, the temperatures in the core and windings are higher than in the HTC according to the thermal connection. In the next step the maximum temperatures in the windings and the core are therefore determined.

²The solution of the differential equations results in involved equations with hyperbolic functions which are not presented for sake of readability.

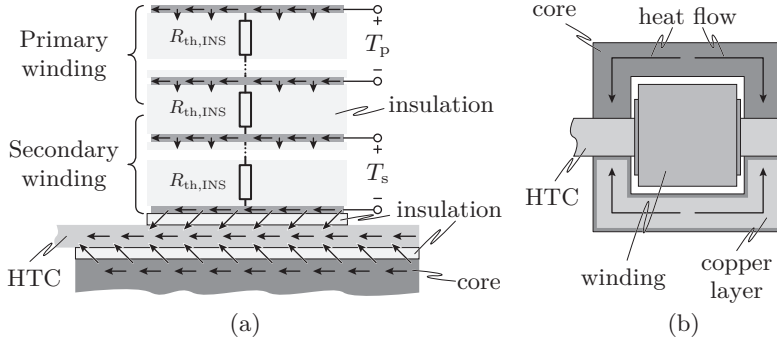


Figure D.3: Illustration for thermal model. (a) Winding arrangement with thermal resistances of the insulation (considering constant layer temperature); (b) Considered heat flow in the core.

D.3.1 Temperature Distribution in the Windings

Foil windings which are wound around the centre leg are considered in the thermal model of the transformer as illustrated in **Fig. D.2** and **Fig. D.3(b)**. The secondary windings are directly linked to the heat transfer component as shown in **Fig. D.3(a)**, each separated by a thermally-conductive insulation foil with a thermal resistance $R_{th,INS}$. The primary winding, where less losses are considered because of the much smaller RMS-current values, are wound around the secondary winding, also individually separated by the insulation foil with $R_{th,INS}$. Due to the high thermal conductivity of copper compared to the insulation foil, the temperature is assumed to be constant in a winding layer and consequently, only the temperature drop across the winding layers is considered. The temperature drop ΔT_w across the primary and secondary winding can hence be simply determined with

$$\Delta T_w = \sum_{n_p=1}^{N_p} \frac{n_p P_{w,p}}{N_p} R_{th,INS} + \sum_{n_s=1}^{N_s} \left(\frac{n_s P_{w,s}}{N_s} + P_{w,p} \right) R_{th,INS} \quad (D.43)$$

where $P_{w,p}$ and $P_{w,s}$ are the losses in the primary and secondary winding with the corresponding turns number N_p and N_s . The thermal resistance can be calculated with (D.2).

The maximum temperature is found in the outer winding layer with the assumed worst-case model. In practice the temperature drop is

lower because the heat is additionally dissipated via heat convection and radiation.

D.3.2 Temperature Distribution in the Core

It is assumed, that the heat flow starts in the middle of the outer legs for the modelling of the temperature distribution in the core, i.e. the place where the two E-cores are commonly linked to obtain the considered transformer core, and continues in both directions over the outer yokes to the middle leg. There the main HTC is located as illustrated in **Fig. D.3(b)**. The temperature drop $T_{c,i}$ is consequently maximal in the middle of the core leg i and can be calculated with

$$\Delta T_{c,i} = \frac{R_{th,C,i}}{2} P_{c,i}, \quad (D.44)$$

where $P_{c,i}$ is the generated core loss in the leg i and $R_{th,C,i}$ is the corresponding thermal resistance of that leg.

The temperature drop across the core can obtain values of several ten degrees because of the low thermal conductivity, which further results in mechanical stress. Even a thin copper layer could already reduce the temperature drop by a factor of five according to [174]. In the presented high-power-density converter systems the temperature drops have be reduced by applying a heat-conductive material around the core, which further functions as case and linkage to the converter system.

The temperature drop can be again determined with the transmission-line model, similar to the above-presented equations of section ③ or ⑤. If the low thermal conductivity in the core is neglected, i.e. a constant head-injection is assumed (worst-case), the differential equations can be simplified to those of section ①. The temperature drop in the HTC with the considered heat flow from the half of the outer leg $l_{leg}/2$ is in this case given by

$$\Delta T_{HTC} = \frac{P_{c,i}}{2} \sqrt{R'_{th,HTC2} R'_{th,Cu}} \frac{1 - \cosh\left(\frac{R'_{th,B-C}}{R'_{th,HTC2}} \frac{l_{leg}}{2}\right)}{\sinh\left(\frac{R'_{th,B-C}}{R'_{th,B}} \frac{l_{leg}}{2}\right)}, \quad (D.45)$$

where $R_{th,HTC2}$ is thermal resistance of the applied heat transfer layer over the outer core legs.

D.3.3 Induced Eddy Currents in the Heat Transfer Component

The power-density increase is enabled with the introduced cooling method while the maximum allowed material temperatures are assured. For an efficient cooling, the heat-transfer-component material must provide a high thermal conductivity, which in turn is commonly connected with a high electrical conductivity as well. As the HTC is arranged in a close vicinity of the core and winding, eddy currents are potentially induced in the HTC because of the alternating magnetic field, which results in eddy-current losses.

The magnetic field in close vicinity of ferrite cores applied in power electronic systems is commonly small (usually some 100 A/m for transformers in the kW-range [161]) due to the significantly higher permeability of the core compared to air or an electrically-conductive material ($\mu_r \approx 1$) which concentrates the flux in the core instead of the air or the HTC.

In [161], the loss-induction in the HTC due to eddy currents has been investigated applying 3-D FEM simulations³. It is shown there, that the induced eddy-current losses are in the range of 50-150 mW depending on the geometric arrangement of the components. For the considered 5 kW system, the transformer losses are in the range of 30 to 40 W and the improvement due to the HTC application more than outweighs the resulting eddy-current effects.

In the vicinity of air gaps, however, the field distribution should be determined because of the placement of the heat transfer component across the emanating magnetic field could result in undesirable eddy-current effects. In the introduced highly compact series-parallel-resonant converter, the air-gap has been distributed in order to reduce the field emission and the HTC across the air gap has been specifically shaped, i.e. cut out cf. section 2.1.4. In the current doubler design, the HTC has been completely omitted across the air gap of the integrated transformer, cf. section 2.2.5.

As a last point in the model description it should be noted, that the thermal model can be simply modified if the heat transfer components are applied on both sides of the transformer core. In this case, the

³The 1-D approach as presented to determine the winding losses in section C is not suitable for an accurate determination of the magnetic field distribution and therefore not appropriate for calculating eddy current losses in the HTC.

transformer is imaginary cut in the middle of the direction y and it is assumed, that only half of the core and the winding losses ($1/2 P_c$ and $1/2 P_w$) are present in each of the two pieces. The derived equations for the temperature distribution can than directly be used.

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Curriculum Vitae

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Work Experiences

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