

3- Φ AC/DC Solid-State Transformer Concepts for Next-Generation AI Datacenters

Johann W. Kolar^{*|**} et al.

^{*} Technical University Vienna, Mechatronics & Power Electronics Institute

^{**} ETH Zurich, Advanced Mechatronic Systems Group

www.tuwien.at/en/etit/mpei/pes

Aug. 14, 2026
ZPEC 2026



3- Φ AC/DC Solid-State Transformer Concepts for Next-Generation AI Datacenters

Johann W. Kolar^{*|**} & Jonas Huber^{***}

^{*} Technical University Vienna, Mechatronics & Power Electronics Institute

^{**} ETH Zurich, Advanced Mechatronic Systems Group

^{***} ETH Zurich, Power Electronics & Drive Systems Laboratory

Aug. 14, 2026

ZPEC 2026





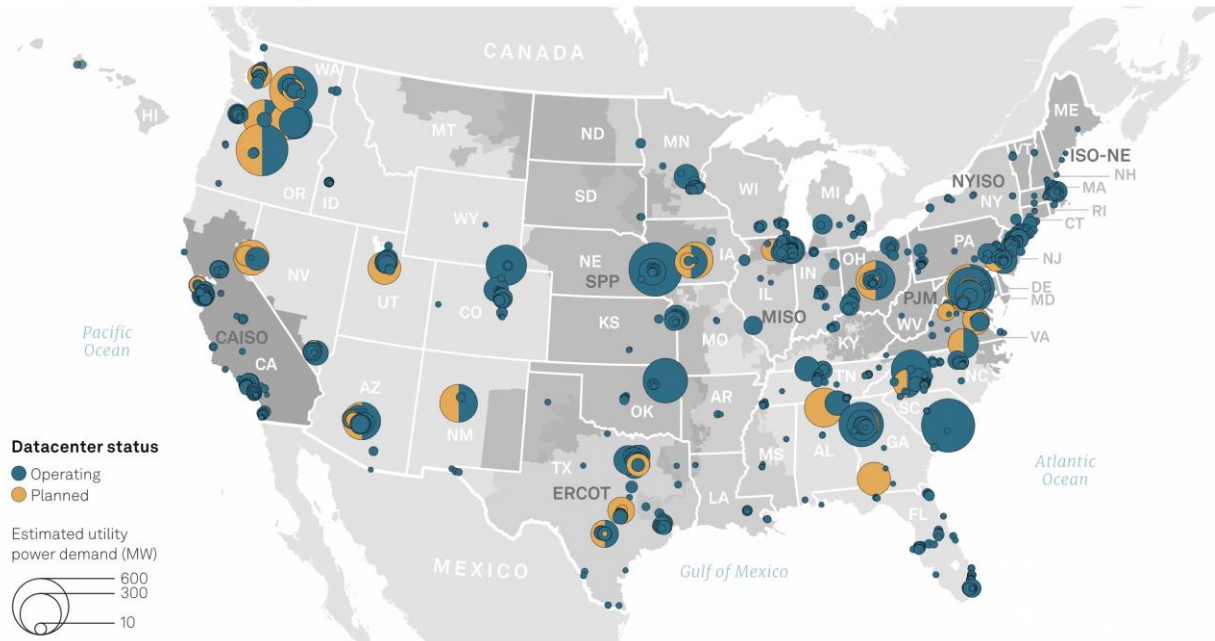
Outline

- ▶ *Introduction*
- ▶ *Two-Stage AC/DC SST Concepts*
- ▶ *Quasi-Single-Stage Topologies*
- ▶ *Single-Stage/Matrix-Type SSTs*
- ▶ *Outlook*

Future Gigawatt-Scale Datacenters

- «Explosion» of AI — Hyperscale Datacenters Providing Massive Scalable Cloud Services
- Gigawatt Power Levels — $\approx 7\ldots 12\%$ of US Electricity in 2028 / 35...65 GW ($\approx 4\%$ in 2023)

AI is expected to drive more power demand from datacenters

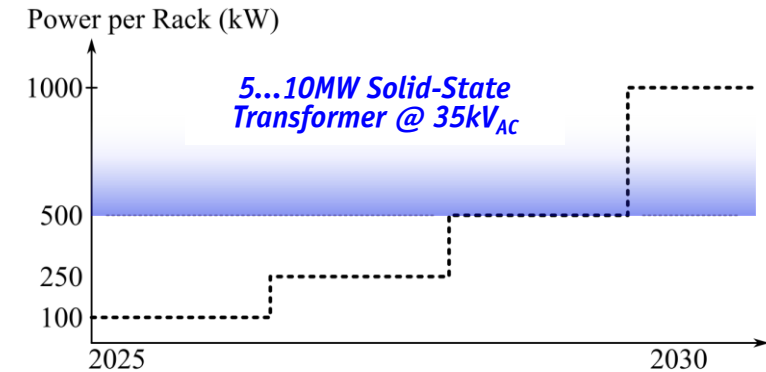
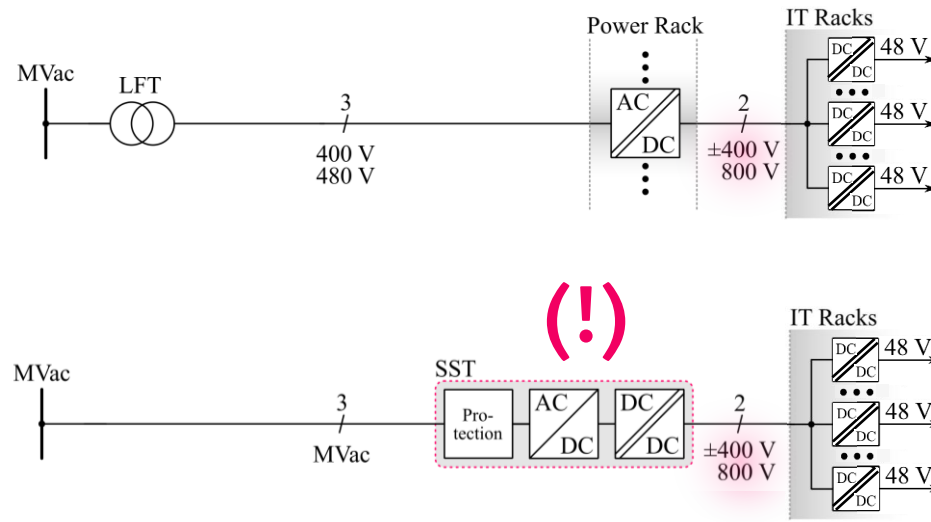


Sources: S&P Global Market Intelligence; 451 Research; S&P Global Commodity Insights

- Plans for 2.5 ... 6 ... 11 Gigawatt Campuses Co-Located w/ Nuclear Power Plants (!)
- Collaboration w/ Utilities — Datacenters as Responsive Loads for Balancing Solar & Wind Power

Future 3- Φ Medium-Voltage AC/800V DC Power Supply

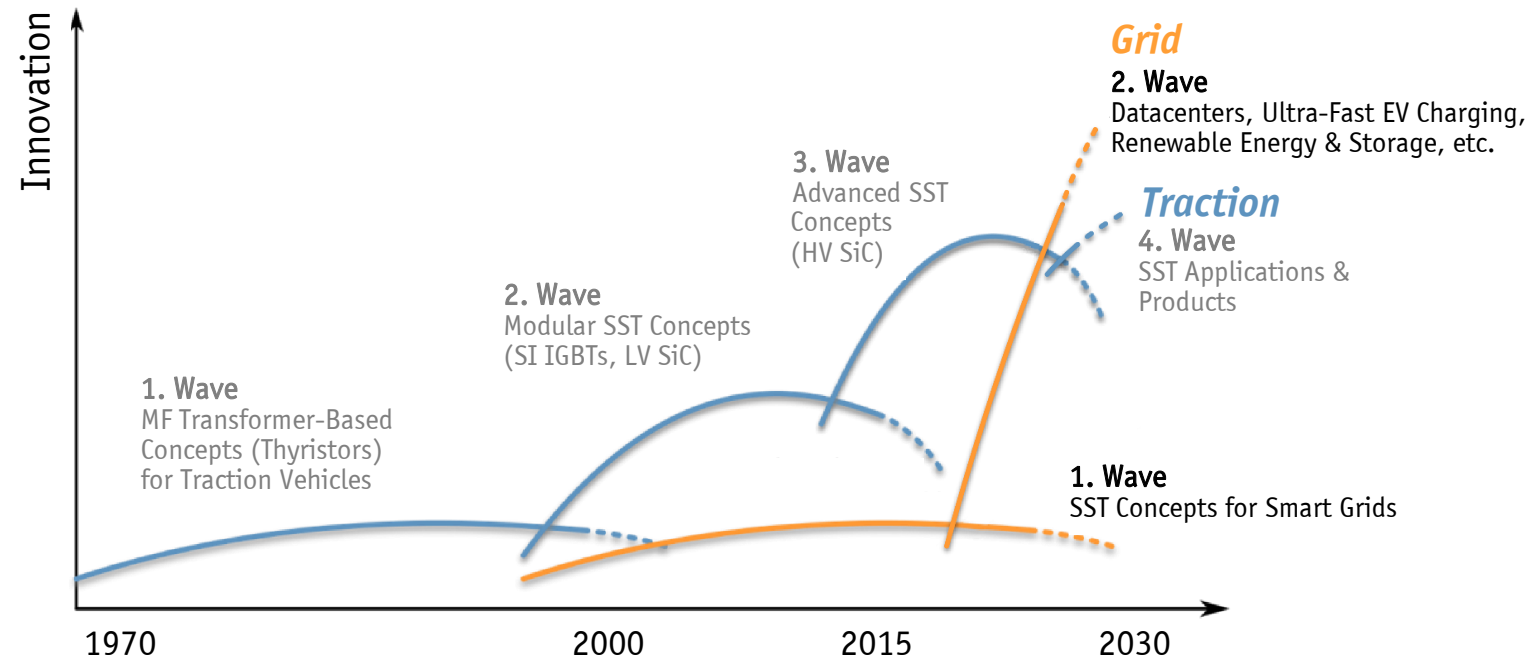
- **Near Term** — 3- Φ 400V_{AC} or 480V_{AC} or 600V_{AC} Supply & AC/DC Power Racks / Side Cars incl. Battery Buffer Units
- **Mid Term** — Medium-Voltage AC Distribution & AC/DC Solid-State Transformers (SSTs) Replacing Power Racks



- **IT Rack Power Levels Expected to Reach 1MW by 2030** / ± 400 V_{DC} or 800V_{DC} or ± 750 V_{DC} Replacing 54V_{DC} In-Rack Bus
- **Medium-Voltage AC Supplied SSTs Feature Lower Busbar Cross Sections & Lower Distribution Losses**

Remark SST Development Cycles

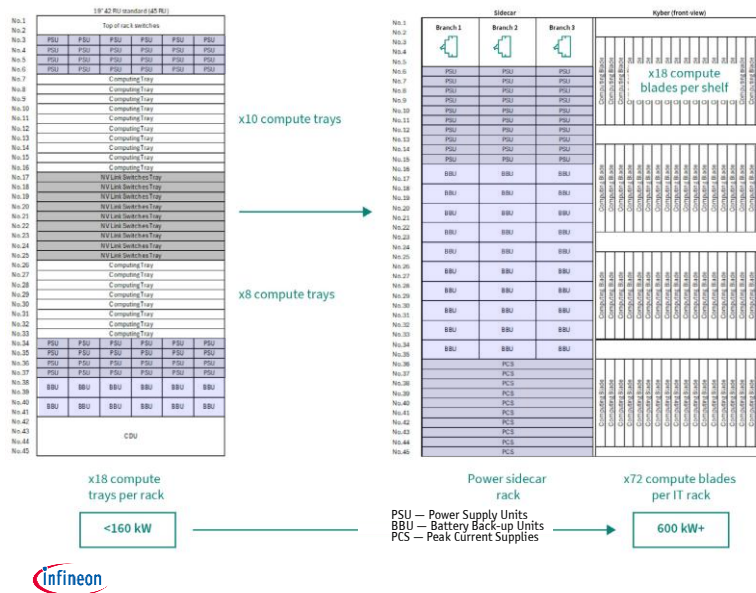
- **Traction** — Higher Efficiency / Low Volume & Mass
- **Smart Grid** — Grid Controllability / Renewables & Storage Integration / Ancillary Services
- **EV Charging** — High Power Density / Integrated Buffer Storage / Renewables Integration
- **Datacenters** — Direct MVAC-LVDC Interface / Elimination of Conversion Stages / High Efficiency



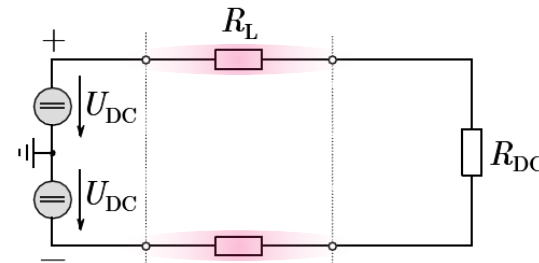
- **Development Cycles Spanning Decades** — Governed by Product Life Cycles
- **Replacement / Expansion of Legacy Systems** — Complex Multi-Objective Decisions

54V_{DC} → 800V_{DC} Rack-Level Power Distribution

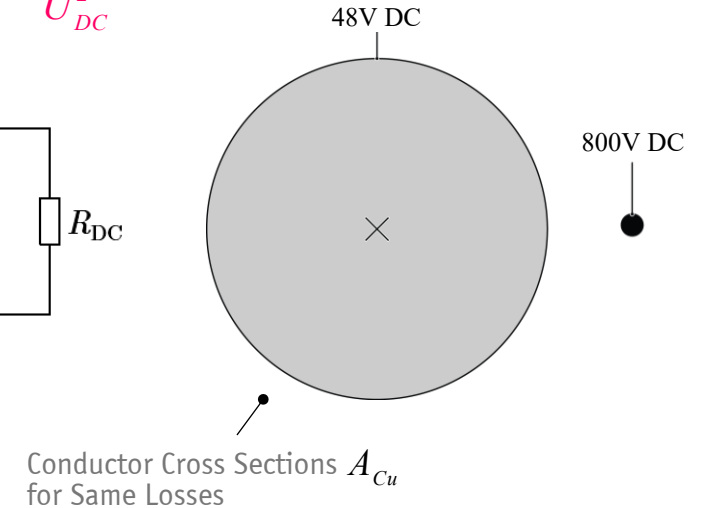
- **Quadratic(!) Dependency of Losses on Voltage Level**
- **Higher Voltage Allows Massive Reduction of Conductor Cross Section / No Bulky Busbars / Low Raw Material Effort**



$$P_{V,DC} = 2 \cdot \left(\frac{P}{2U_{DC}} \right)^2 \cdot R_L \sim \frac{1}{U_{DC}^2}$$



$$R_L = \frac{l}{\kappa A_{Cu}}$$



Conductor Cross Sections A_{Cu} for Same Losses

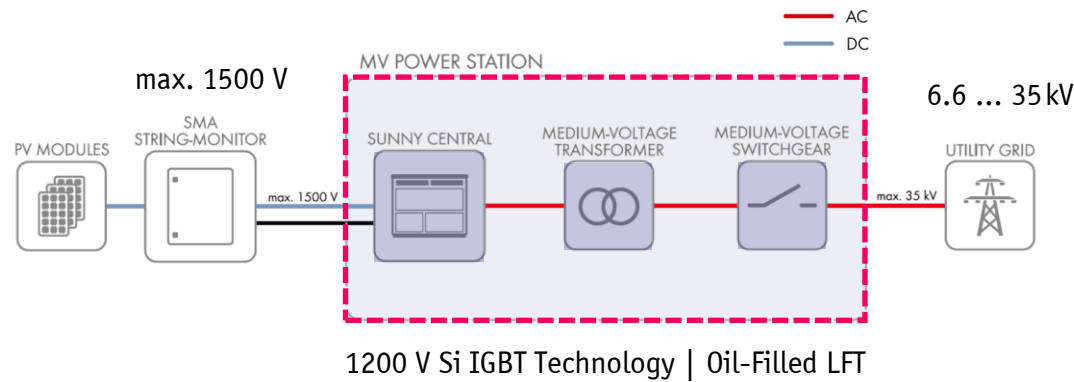
- **Next-Generation AI Workloads — 54V_{DC} In-Rack Distribution Replaced by 800V_{DC} & Separation of Power & Compute**
- **Traditional 54V_{DC} System Would Require Over 200 kg of Copper to Power a 1MW Rack**

State-of-the-Art

LFT-Based Utility-Scale PV Inverter
SST-Based High-Power EV Charging

LFT-Based 3- Φ MV AC/800V DC Power Supply

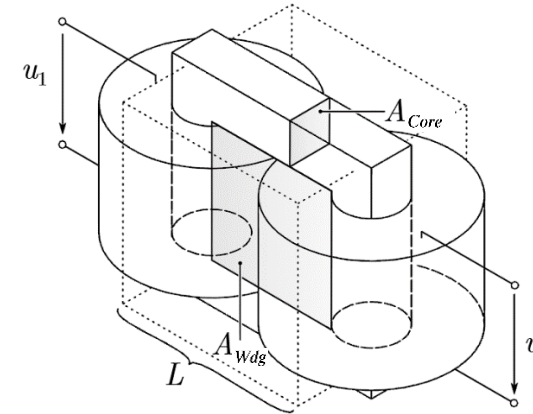
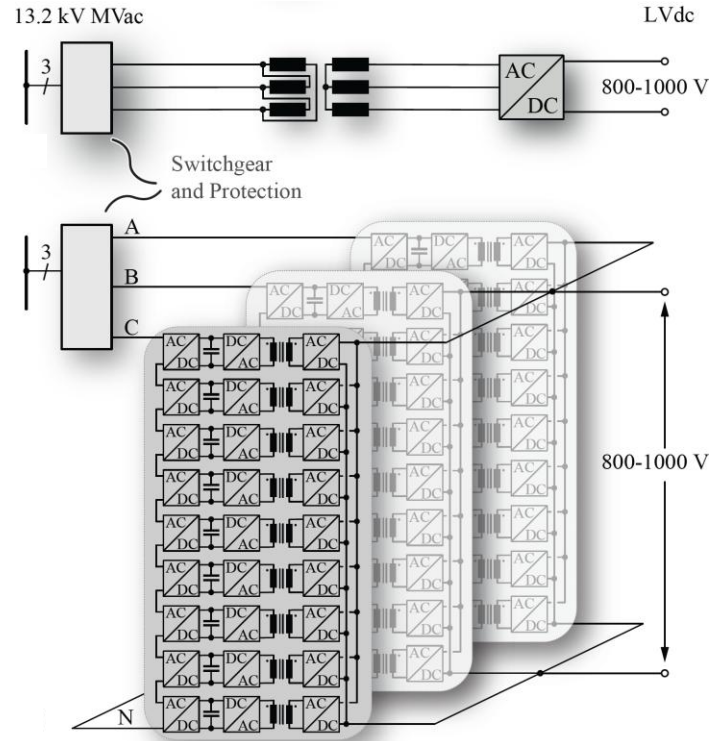
- *SOTA Turnkey Power Station for Utility-Scale PV Power Plants in 20 ft Container (6.1 m x 2.6 m x 2.4 m)*
- *3 MVA Low-Voltage Si IGBT Inverter | 50Hz Transformer (LFT) | MV Switchgear | etc. — 0.08 MW/m³*



- *98.5% CEC Inverter Efficiency / 99% Transformer Efficiency (EcoDesign, Oil-Filled)*
- *97.5% Overall Efficiency / Improvements for Si IGBTs → SiC MOSFETs & Dry Type LFT → 98+%*

LFT-Based vs. SST-Based 3-Φ MV AC/800V DC Supply

- **Conventional Realization w/ 50Hz Transformer (LFT) & Low-Voltage AC/DC Converter**
- **Fully-Modular Solid-State-Transformers (SST) w/ HF-Isolation Stages in ISOP Arrangement**



$$A_{Core} A_{Wdg} = \frac{\sqrt{2}}{\pi} \frac{P_t}{k_w J_{rms} \hat{B}_{max} f} \sim L^4$$

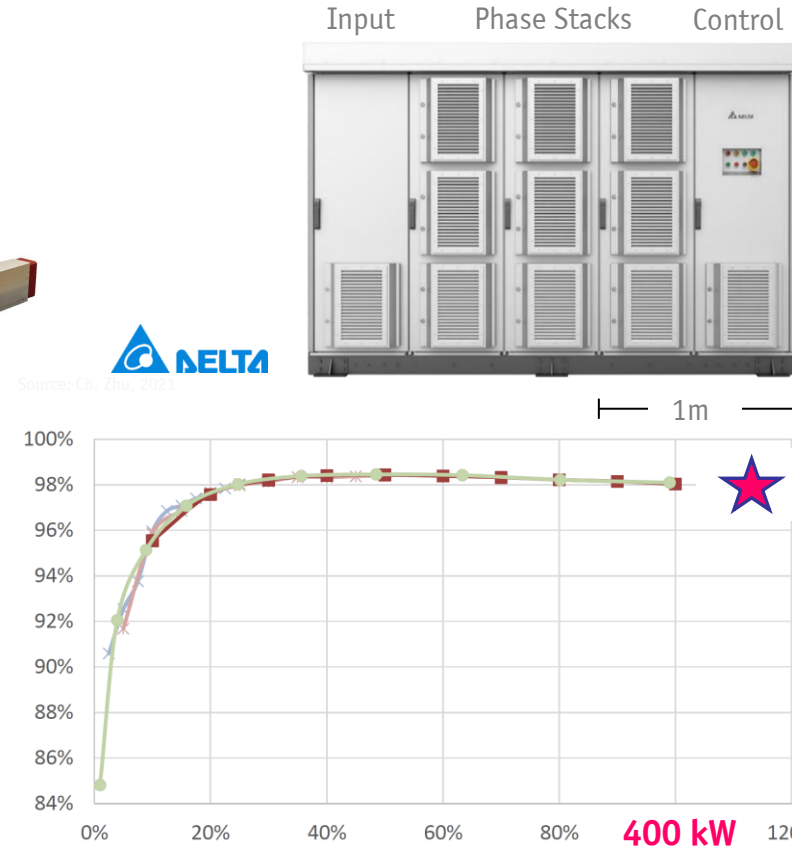
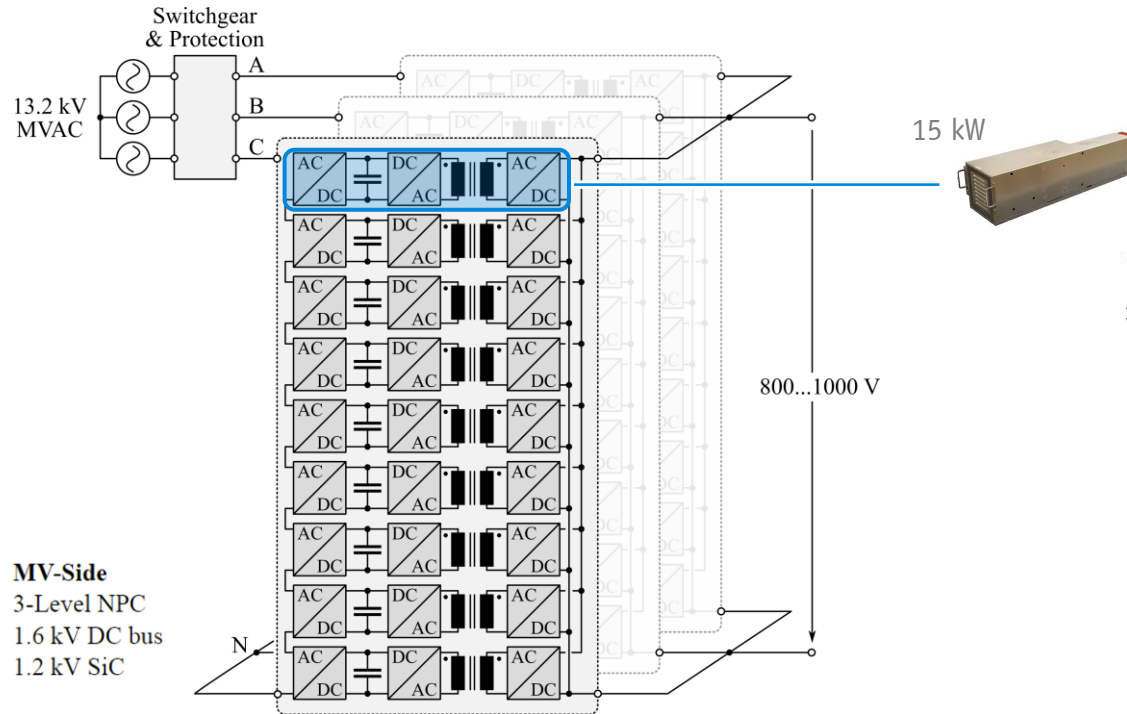
↑ ↑

$$\frac{P_t}{L^3} \sim L \cdot f$$

- **LFTs** — Excessive 100+ Weeks Delivery Time of 50/60Hz Transformers
- **MFTs** — Lower Raw Material Effort / Lower Raw Material Costs / Lower CO₂ Footprint

400kW 3- Φ 13.2kV_{AC}/800V_{DC} SST — Gen #1 1/2

- Industrial SST Prototype (US DOE Project 2018 - 2021)
- $3 \times 9 = 27$ AC/DC — DC/DC Cells $\rightarrow$ 438 Switches
- Forced-Air Cooling

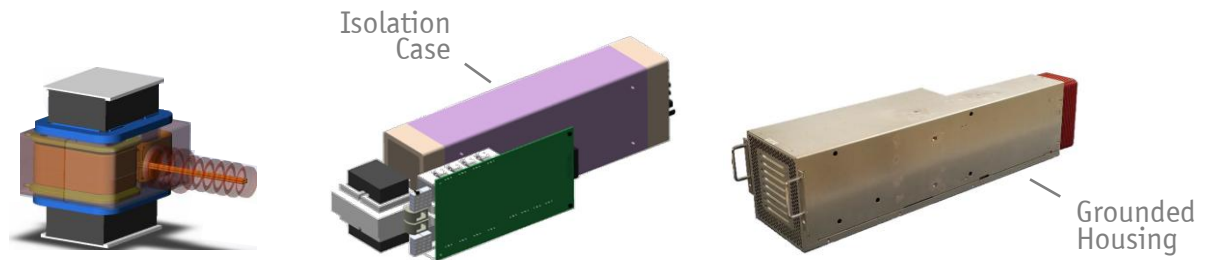
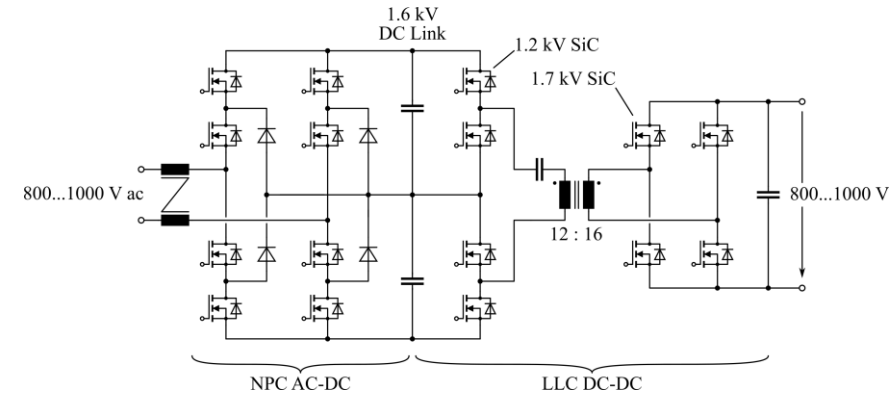
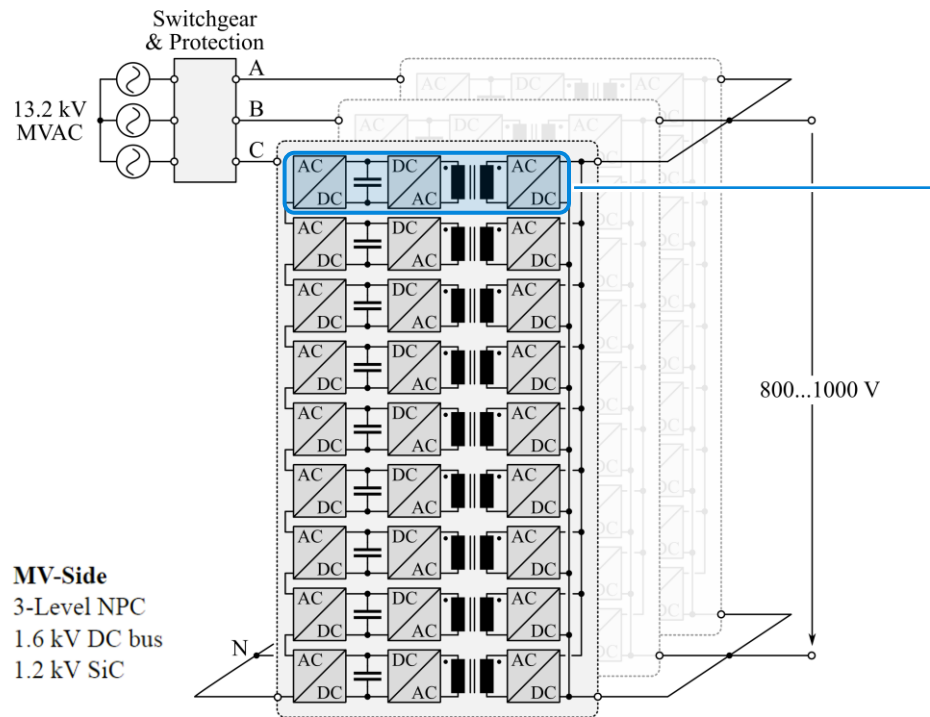


- 3000 kg Weight | 3100 x 1300 x 2100 mm Outer Dimensions
- Power Density $\rightarrow$ 0.05 kW/dm³ (System) | $\approx$ 0.5 kW/dm³ (Cells) | $\approx$ 8.5 kW/dm³ (MFT)

400kW 3- Φ 13.2kV_{AC}/800V_{DC} SST — Gen #1 2/2

- Industrial SST Prototype (US DOE Project 2018 - 2021)
- 3 x 9 = 27 AC/DC — DC/DC Cells → 438 Switches
- Forced-Air Cooling


Source: Ch. Zhu, 2021

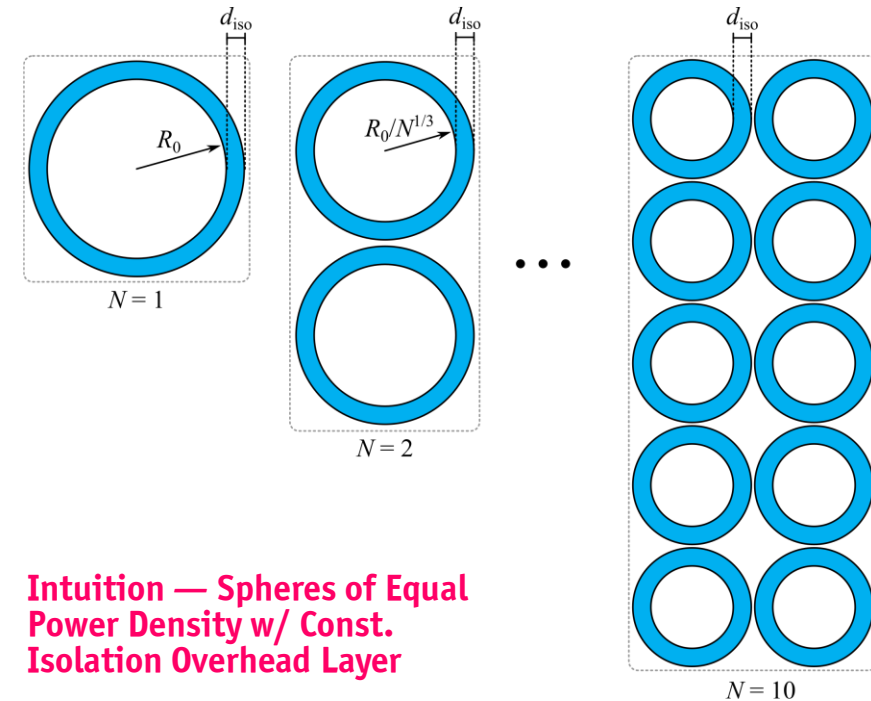
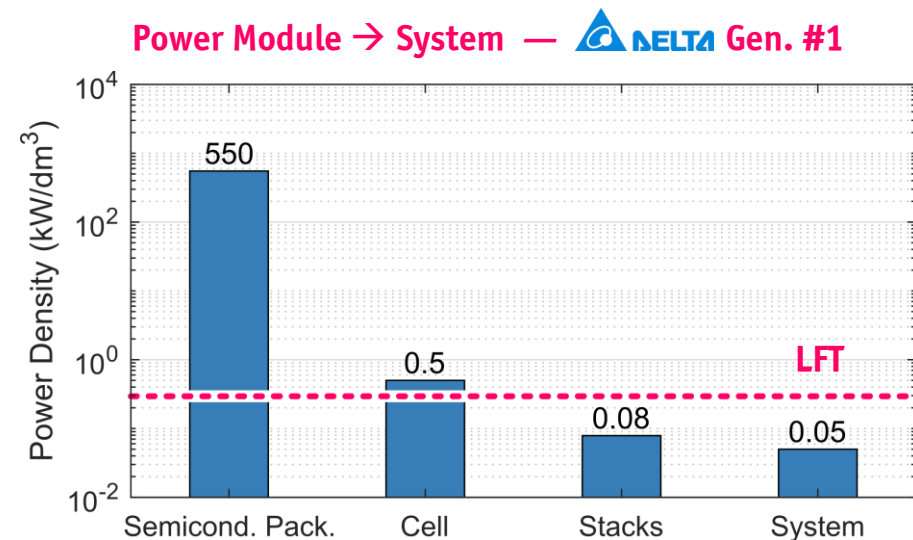


- 15 kW Cells ($\approx 0.5 \text{ kW/dm}^3$) / All-SiC Realization | 100+ kHz MFT ($\approx 8.5 \text{ kW/dm}^3$ w/o Bushing !)

Penalty of Full Modularization

- **Massive Reduction of Power Density from Cell to Full System** → «Modularization Penalty»
- **Accumulation of Isolation Distances AND Transformer Scaling (!)**

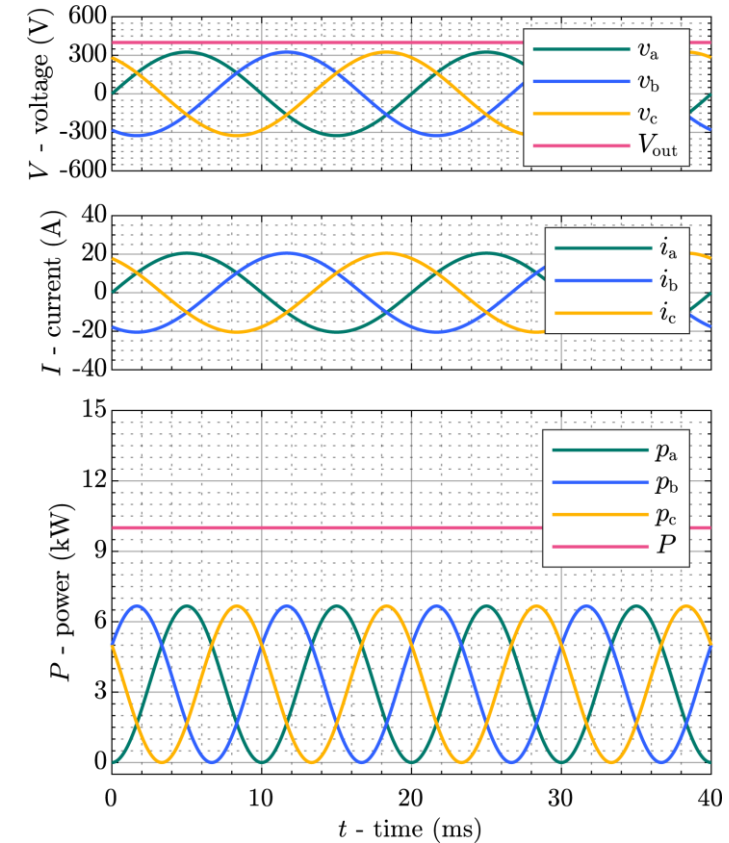
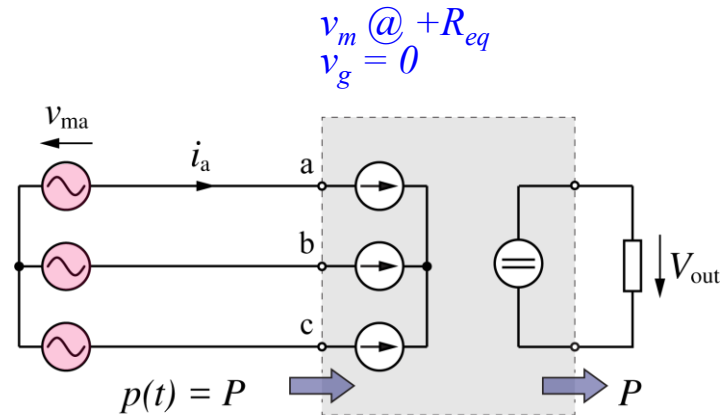
$$\frac{P_t}{L^3} \sim L \cdot f$$



- **Future 10+kV SiC Devices** → **Lower Number of Cells for Given Medium-Voltage Level**

Penalty of 3x 1- Φ AC/DC Conversion Power Pulsation

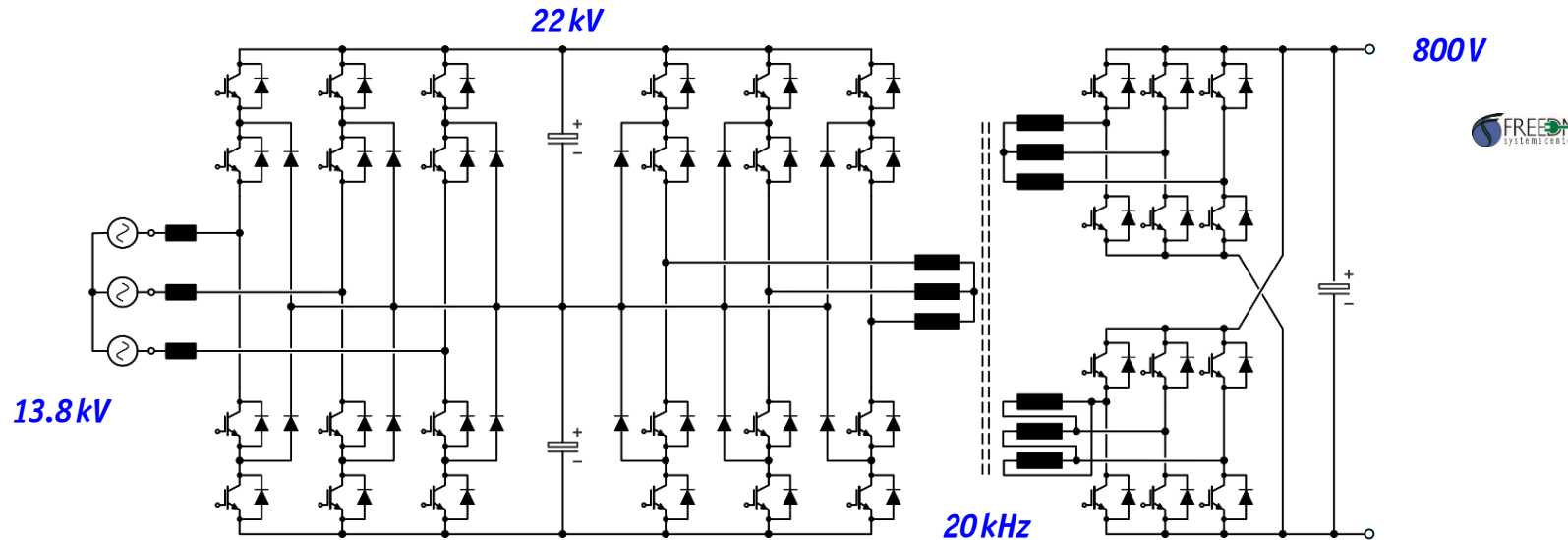
- *Symmetric 3- Φ Sinusoidal AC Mains*
- *Symmetric 3- Φ Sinusoidal Input Currents*
- *Ohmic Mains Behavior*



- *2x Mains-Frequency Input Power Pulsation in Individual Phase Units — DC-Link Buffer Capacitors*
- *Constant Overall 3- Φ Instantaneous Power*

! Remark Two-Stage Monolithic 3- Φ AC/DC SST

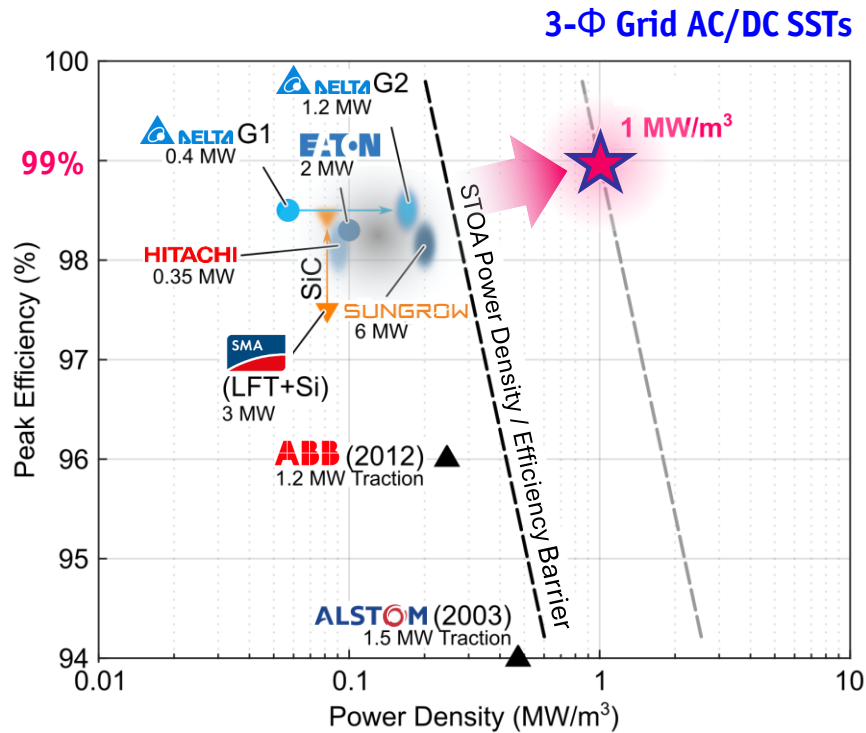
- *Non-Modular Approach / Standard Converter Topology / Low Complexity / Single-MFT*
- *15kV SiC IGBTs / 1200V SiC MOSFETs — Operation @ 13.8kV AC Mains $\rightarrow$ 800V DC*



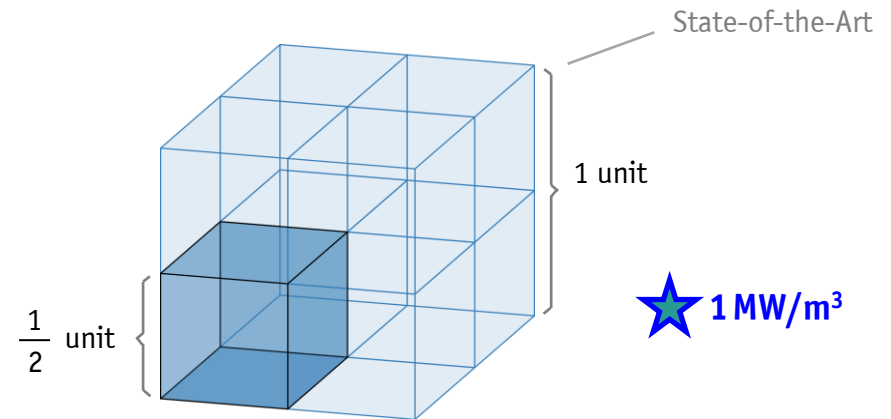
- *No Redundancy (!) — Would Require Series Connection of Power Semiconductors (!)*
- *Not Scalable to Higher Grid Voltages*

Two-Stage AC/DC SST Power Density/Efficiency Barrier

- *State-of-the-Art SST Performance Comparable to LFT-Based Solution (!)*
- *Power Densities of Typ. $\approx 0.15 \text{ MW/m}^3$ | Efficiencies of 98...98.5%*



→ *Next Generation Single-Stage SST*



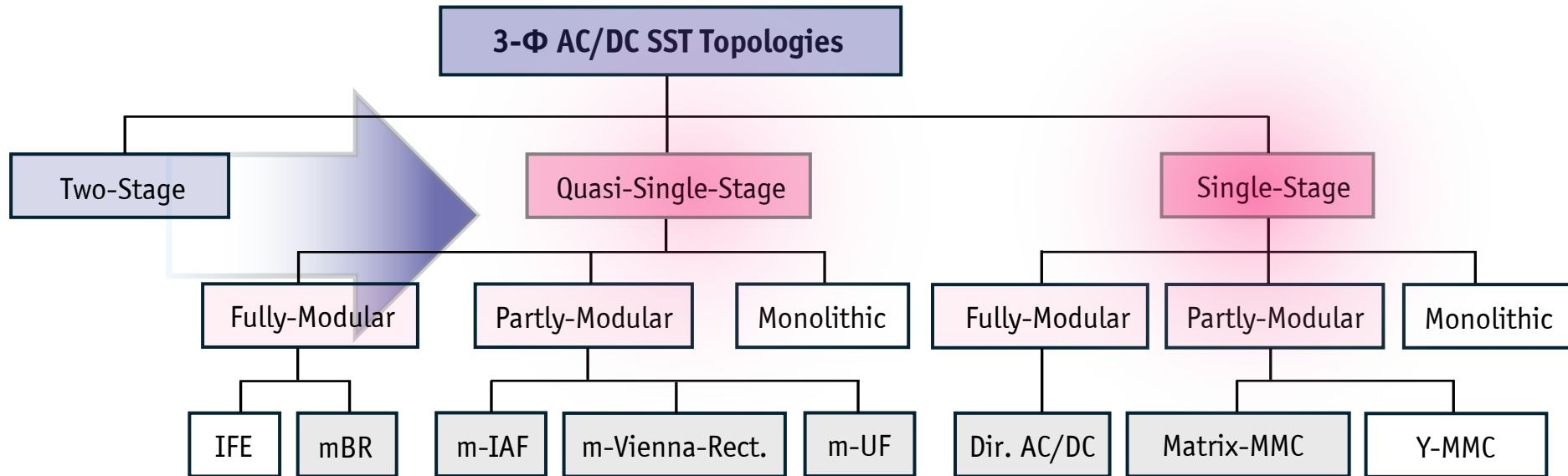
- *Next-Generation SSTs — Power Density x5...10 @ -30% Losses*
- *Full-Scale Demonstrators Complying with All Relevant Regulations Mandatory for Realistic Assessment*

Classification of SST Topologies

Two-Stage / Quasi-Single-Stage / Single-Stage
Fully-Modular / Partly-Modular / Monolithic

Next-Generation Ultra-Compact 3- Φ AC/DC SST Concepts

- *Two-Stage AC/DC-DC/DC* → *Quasi-Single-Stage OR Single-Stage AC/DC Conversion*
- *Fully-Modular Topology* → *Partly-Modular OR Monolithic Structure / Transformer Scaling Advantage*
- *Si IGBTs* → *SiC MOSFETs*

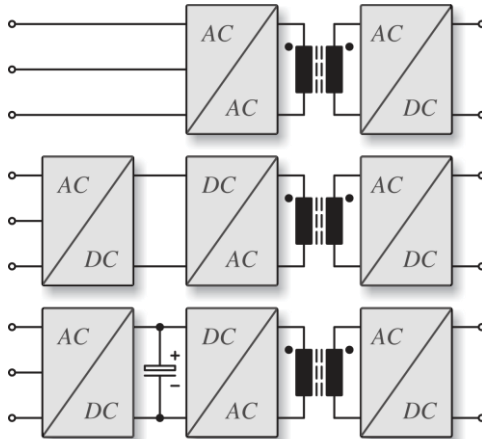


- *99% AC/DC Power Conversion Efficiency / 30% Loss Reduction Comp. to SOTA*
- *1MW/m³ Power Density / Factor 5...10 Increase in Compactness Comp. to SOTA*

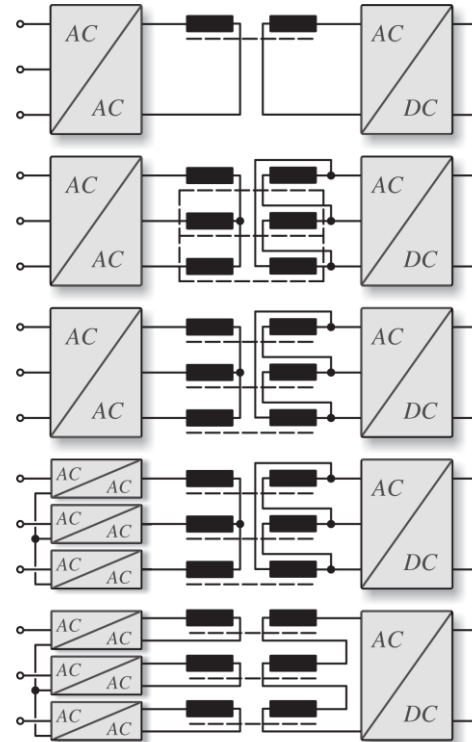
Modularity Categories
 - 3- Φ Phase-Modularity
 - Phase-String Modularity

3- Φ AC/DC Power Conversion Partitioning 1/2

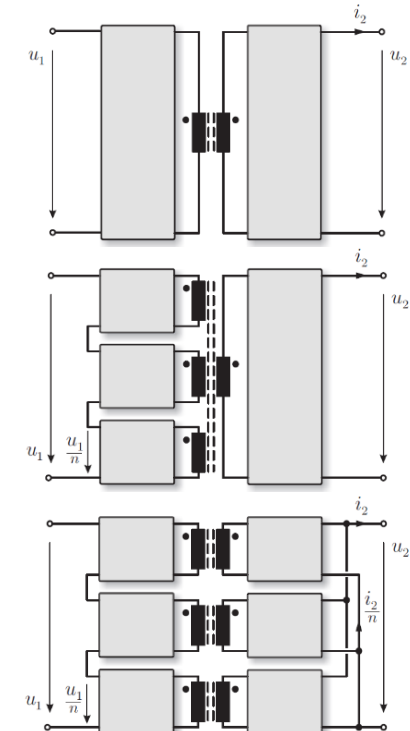
■ Degree of AC/DC Power Conversion Partitioning



■ Degree of Phase Modularity



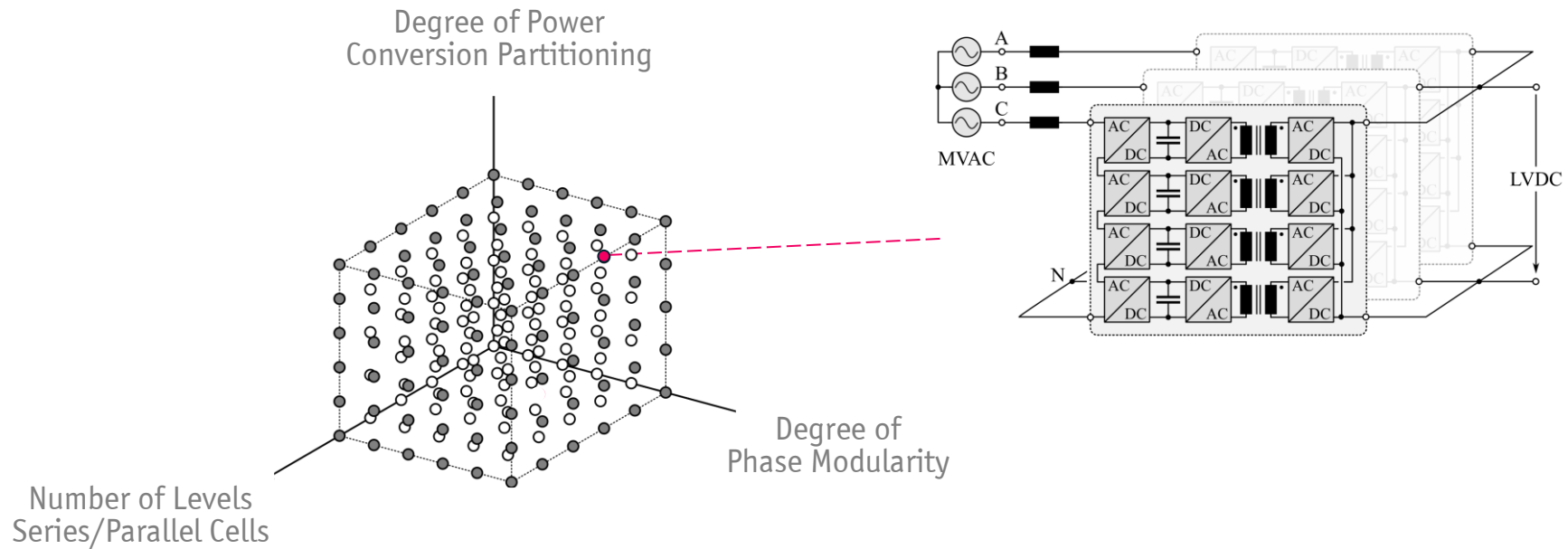
■ Number of Levels Series/Parallel Cells



■ 3-Dimensional Topology Selection Space (!)

3- Φ AC/DC Power Conversion Partitioning 2/2

- *Partitioning of AC/DC Power Conversion*
 - *Splitting of 3- Φ Systems into Individual Phases*
 - *Splitting of Operating Voltage / Current*
- *DC-Link & Matrix-Type Topologies*
 - *Phase Modularity (Electric &/or Magnetic)*
 - *Multi-Level/Cell ISOP Approaches*



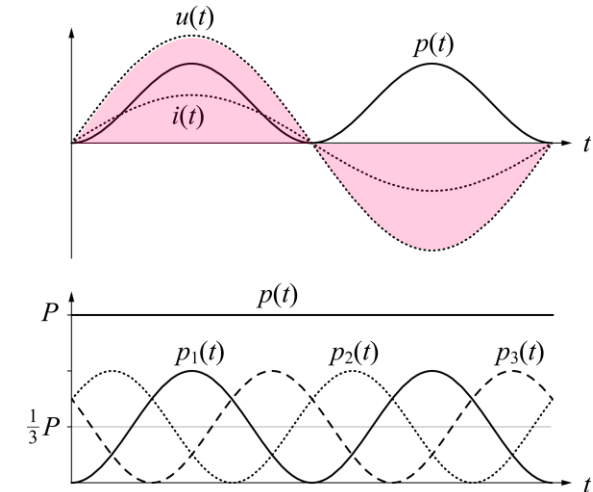
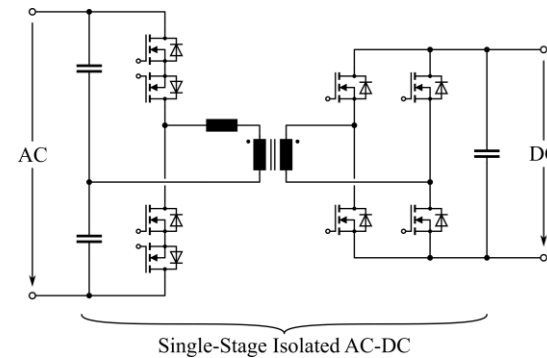
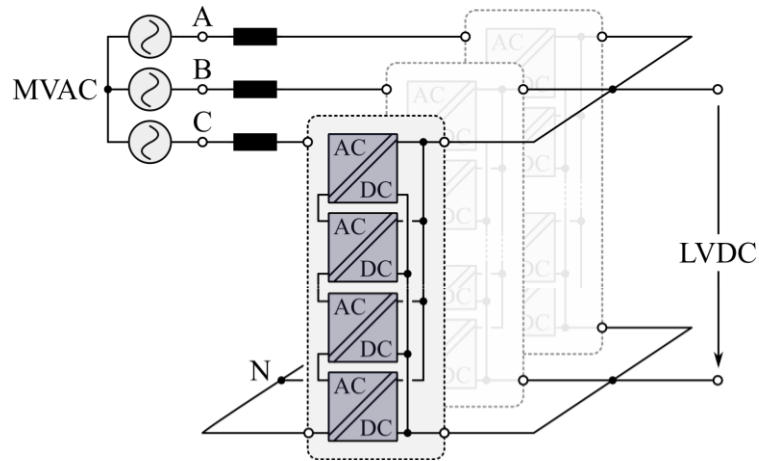
- *Extremely (!) Large Number of Possible Topologies*

Single-Stage SST Topologies
Matrix-Type SST Concepts

Single-Stage Fully-Modular 3- Φ AC/DC SST Topology

- *AC-Switch-Based Dual-Active-Bridge-Type or Resonant AC/DC Converter Sub-Modules*
- *Half-Bridge Primary Minimizes Number of MV-Side Switches / Full-Bridge Secondary Provides Higher Controllability*

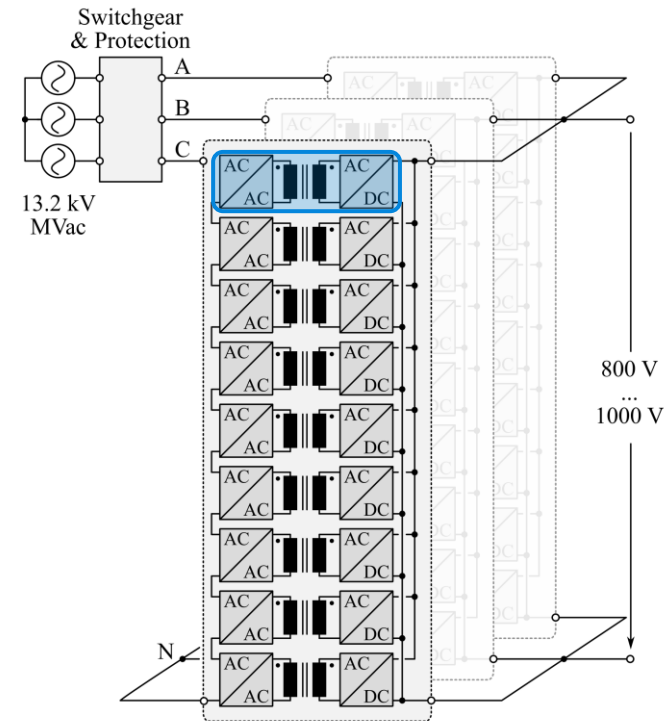
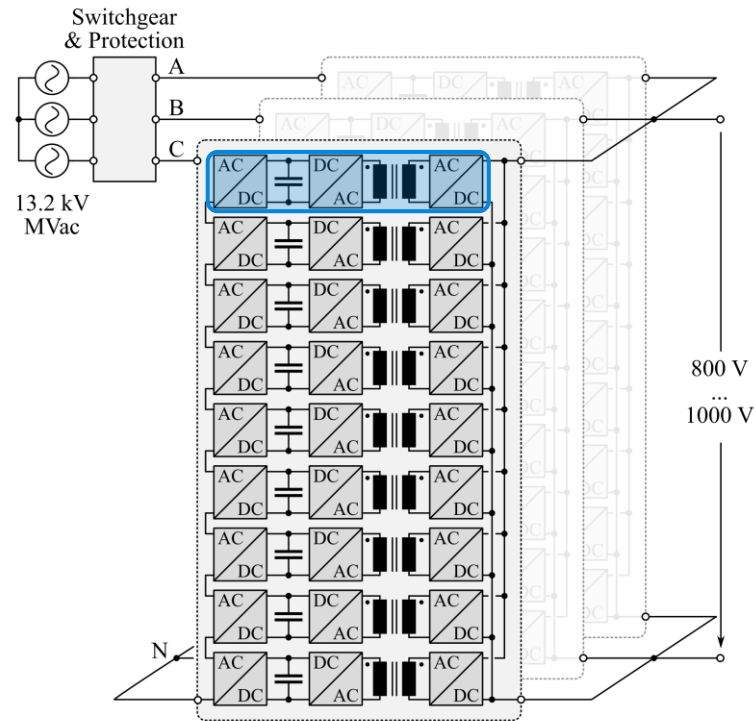
ETH Zurich
Jauch/Biela
2012



- *2x Grid Frequency Power Fluctuation / Peak Phase Power of 2/3 (!) Total 3- Φ Power / Rel. High Comp. Stresses*
- *120° «Interleaving» of Phases Results in Constant Overall Power Flow — No DC-Side Storage Required (!)*

! Remark Single-Stage vs. Two-Stage 3- Φ AC/DC SST

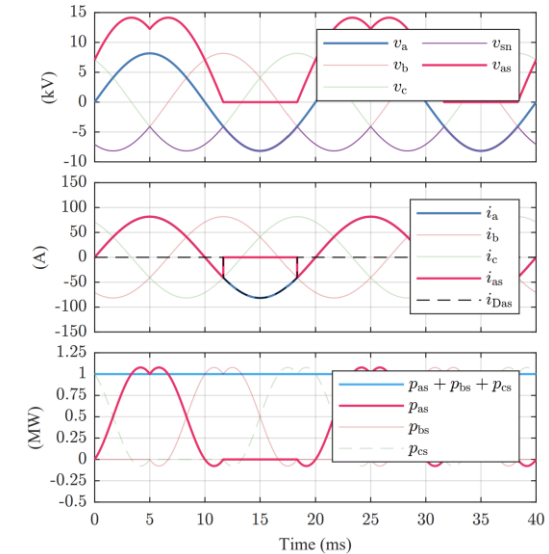
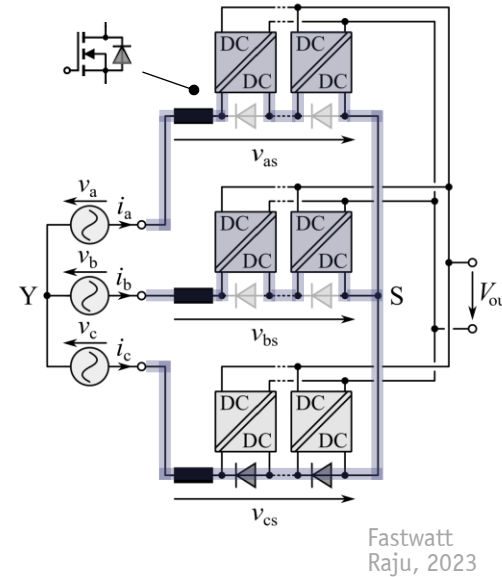
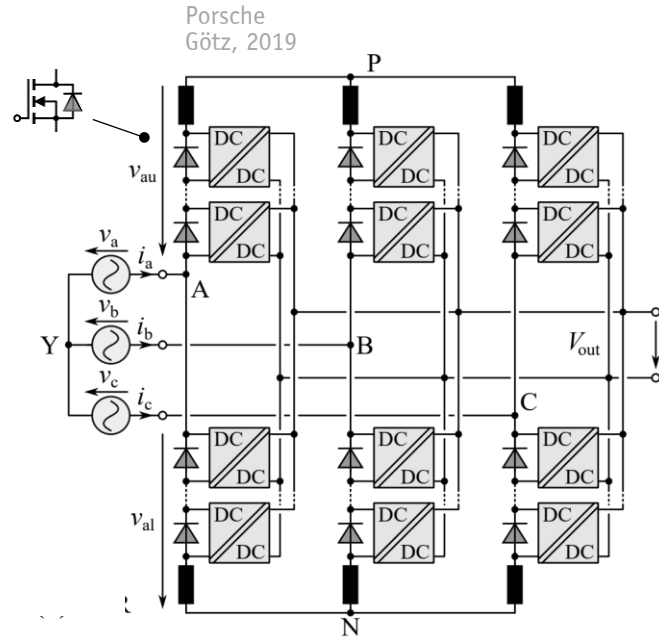
- *Functional Separation vs. Functional Integration of AC Power Factor Correction and DC/DC Conversion*
- *DC-Link Energy Buffer vs. Direct Processing of 2x Mains-Frequency Pulsating Power*



- *Implementation of Single-Stage AC/DC Power Conversion Limited by Availability of AC-Switches*

Single-Stage Modularized 3- Φ Bridge Rectifier SST

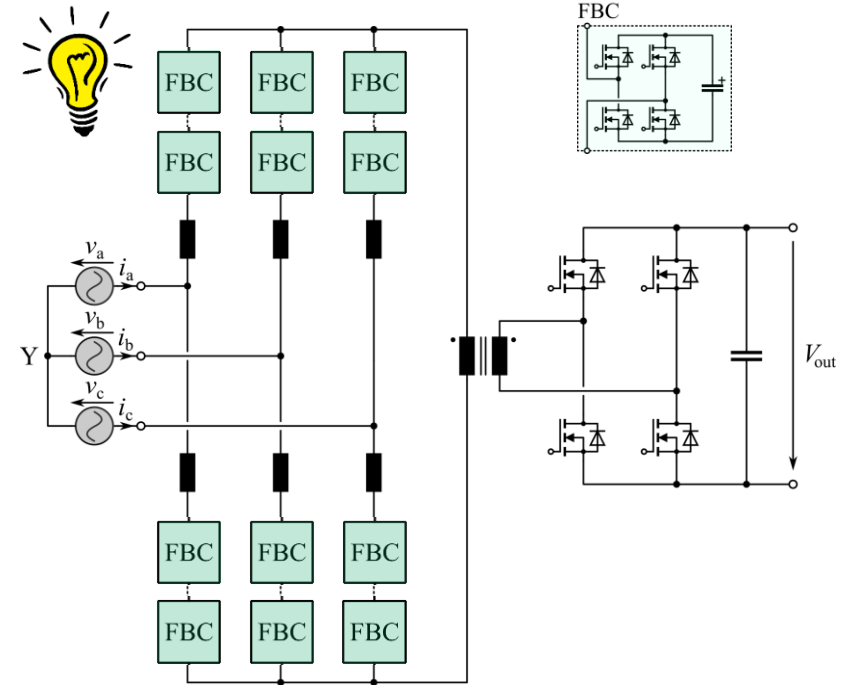
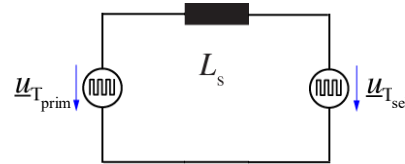
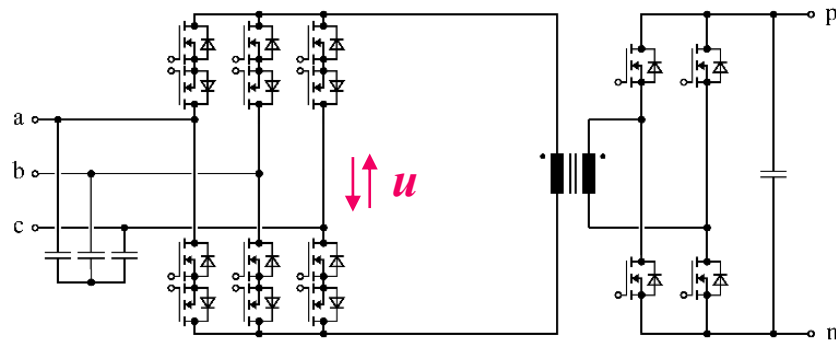
- **Voltages Across Blocking Diodes Used as Unipolar Supply of DC/DC Stages**
- **DC/DC Stage Operating Intervals Defined by the Mains Line-to-Line Voltages / Relatively Low Utilization**



- **Antiparallel Switches for Extension to Bidirectional Power Transfer**
- **Defined Voltage Sharing of Series Connected Diodes BUT Voltage Rating Defined by Line-to-Line Voltage**

Single-Stage MMLC-Based Matrix-Type 3- Φ AC/DC SST

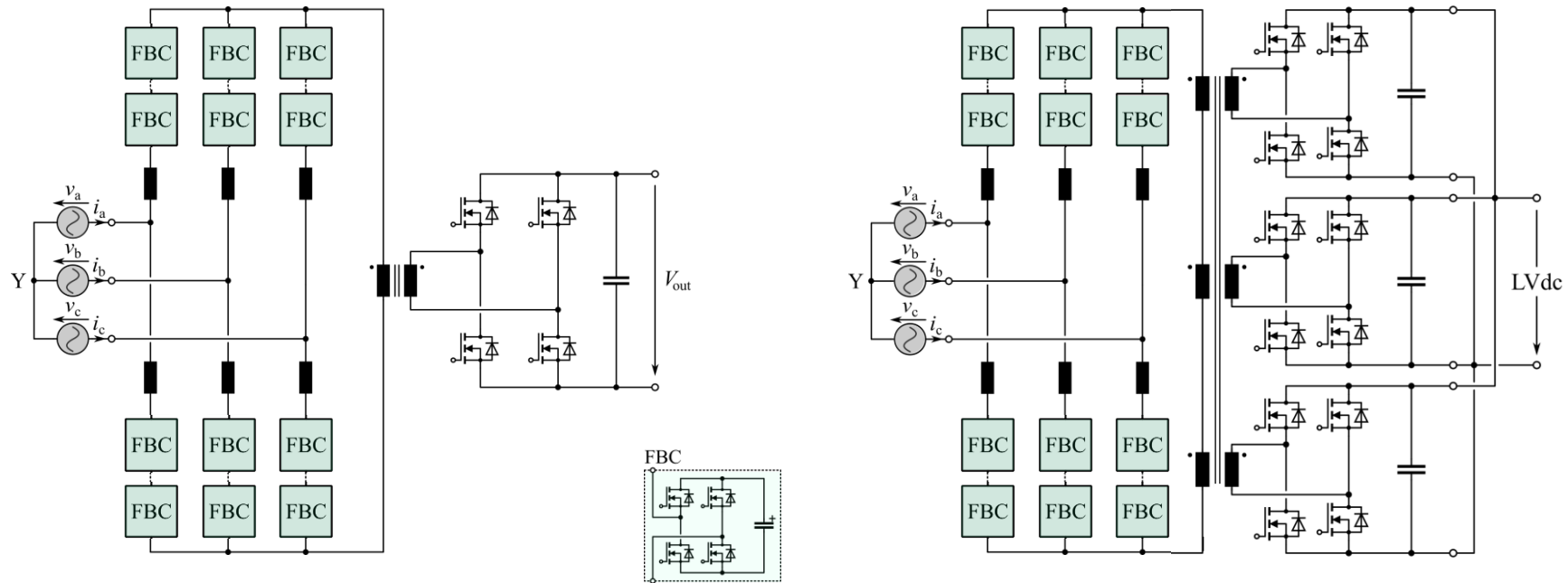
- AC-Switches Replaced w/ Full-Bridge Cells Utilizing Unipolar Power Semiconductors / Voltage Scalability
- Modularity / Redundancy Limited to Power Semiconductors / Critical Components



- Dual-Active-Bridge-Type Operation / No «Transformer Modularization Penalty» (!)
- Output-Side Current Splitting to Parallel Branches — Matrix Transformer Concepts

Single-Stage MMLC-Based Matrix-Type 3- Φ AC/DC SST

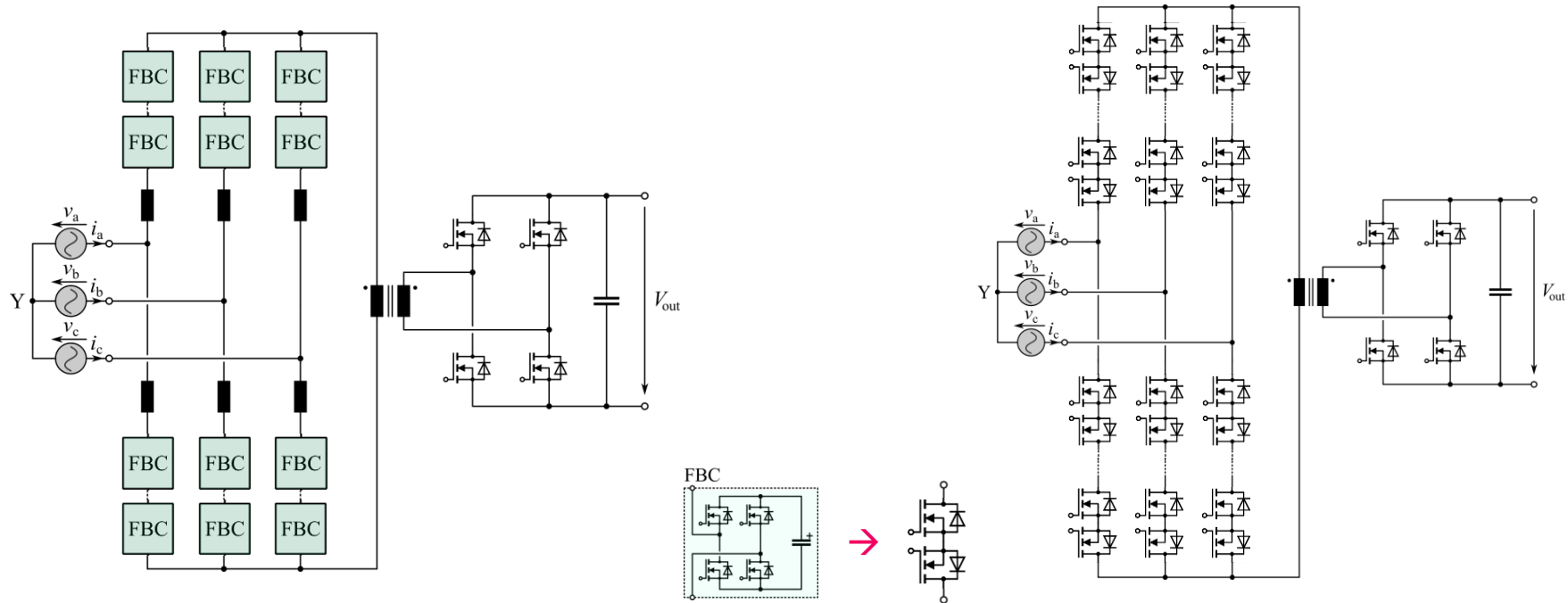
- *Matrix-Type SST — Single-Transformer / Modularity & Redundancy Limited to Lifetime-Critical Components*
- *Application of Multi-Winding Single-Core Transformer Concepts / Splitting of High Output Currents*



- *Modular-Multilevel-Converter-(MMLC)-Type Full-Bridge-Cells as Temporary Substitute of AC-Switches*
- *Realization Effort / Protection / Handling of SST-Internal Failures & Redundancy / etc. Still to be Clarified*

Single-Stage MMLC-Based Matrix-Type 3- Φ AC/DC SST

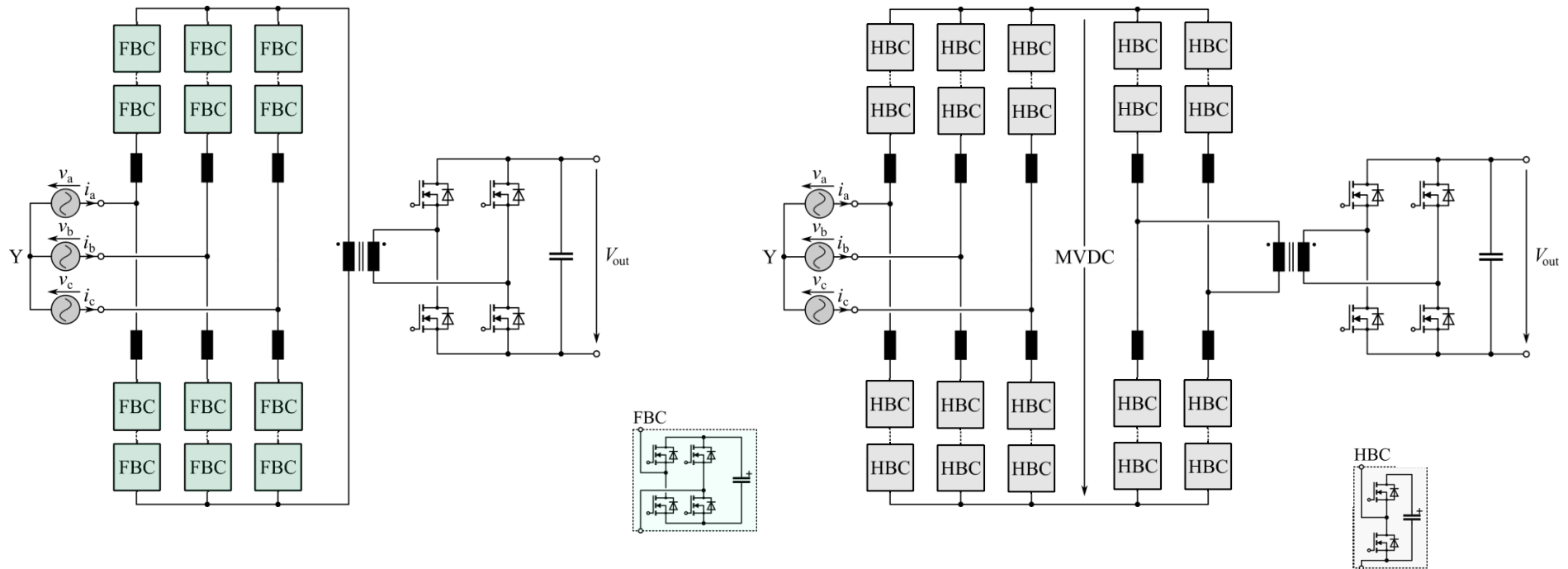
- *Matrix-Type SST — Single-Transformer / Modularity & Redundancy Limited to Lifetime-Critical Components*
- *Application of High Blocking Voltage (Monolithic) Bidirectional SiC MOSFET-Type or IGBT-Type Switches*



- *Modular-Multilevel-Converter-(MMLC)-Type Full-Bridge-Cells as Temporary Substitute of AC-Switches*
- *Realization Effort / Protection / Handling of SST-Internal Failures & Redundancy / etc. Still to be Clarified*

Direct & Indirect Matrix-Type 3- Φ AC/DC SST 1/2

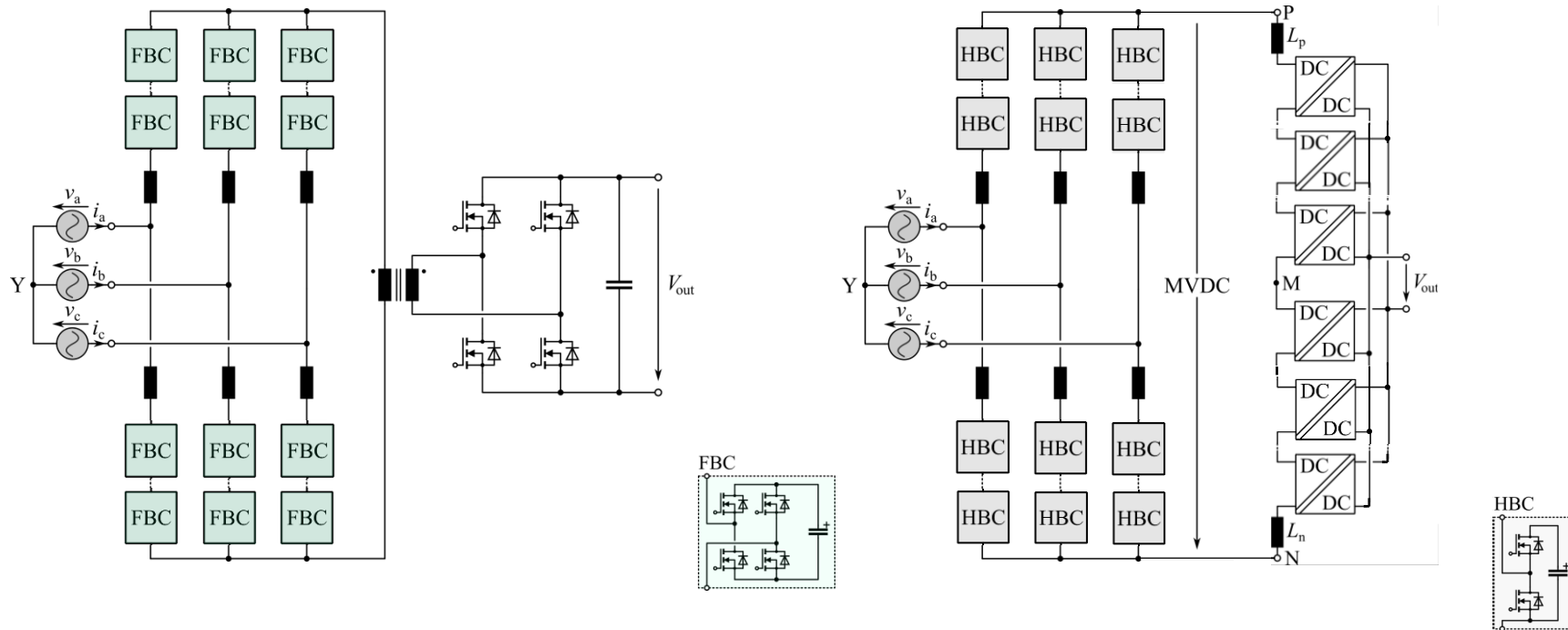
- *Indirect Approach Features Higher Control Flexibility & Higher Transformer Utilization*
- *Overhead / Underground Coupling of High-Power Front-End to Multiple $\pm 10 \dots 20 \text{ kV}_{\text{DC}} / \pm 800 \text{ V}_{\text{DC}}$ DCX-Stages*



- *Comparative Evaluation of Power Semiconductor Stresses / Protection / Reliability etc. Still to Be Clarified*

Direct & Indirect Matrix-Type 3- Φ AC/DC SST 2/2

- *Indirect Approach Features Higher Control Flexibility & Higher Transformer Utilization*
- *Overhead / Underground Coupling of High-Power Front-End to Multiple $\pm 10 \dots 20 \text{ kV}_{\text{DC}} / \pm 800 \text{ V}_{\text{DC}}$ DCX-Stages*



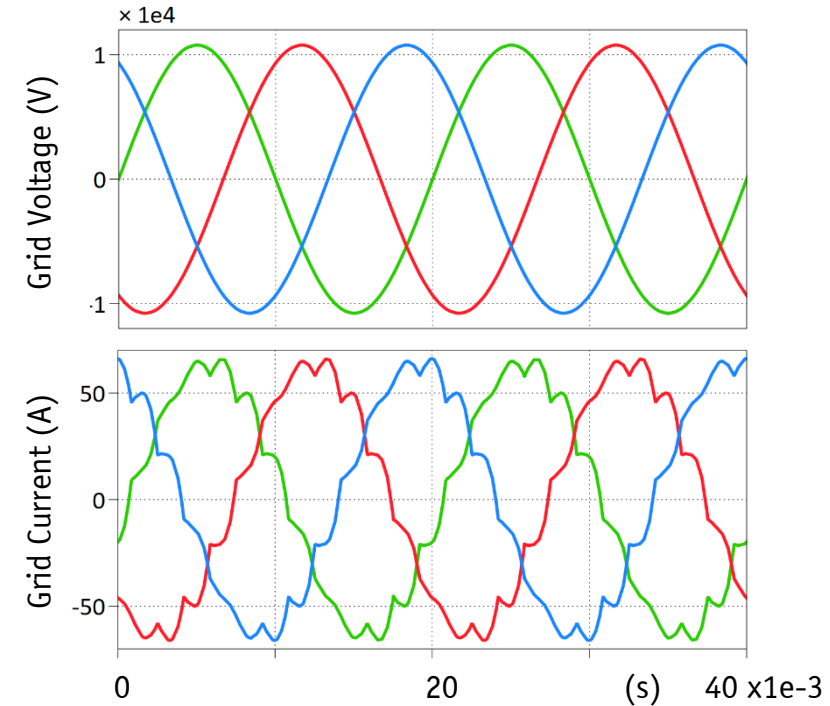
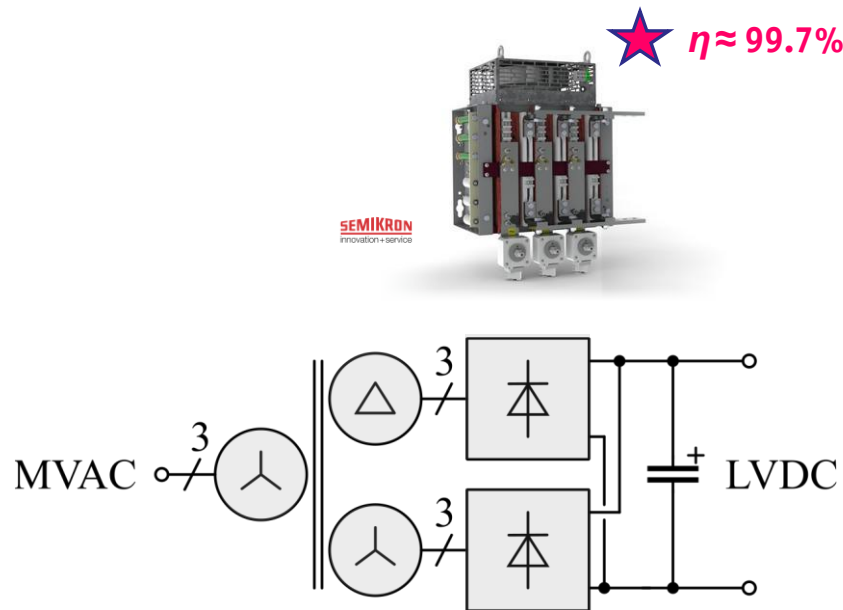
- *Comparative Evaluation of Power Semiconductor Stresses / Protection / Reliability etc. Still to Be Clarified*

*Hybrid Quasi-Single-Stage
Partly-Modular SST Concepts*



12-Pulse / Multi-Pulse 3- Φ Diode Rectifier

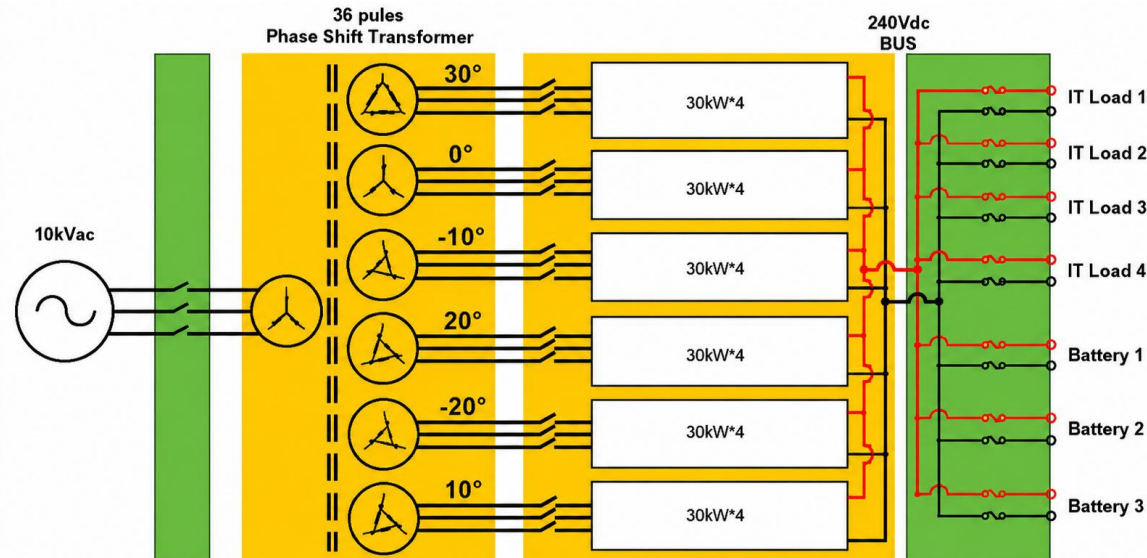
- **No Explicit PFC Stage (!)** → *Passive Realization of PFC with Phase-Shifting Transformer / No Inductors*
- **Low Complexity | High Robustness | Long Lifetime**
- **18-Pulse, 24-Pulse For High Power Levels**
- **4 kW/dm³ Rectifier Stage / Air Cooling**



- **Unidirectional**
- **No Active Output Voltage Control (Tap-Changer)**
- **Remaining Current Distortion / Reactive Power Consumption**

Remark “Panama” Datacenter Power Supply

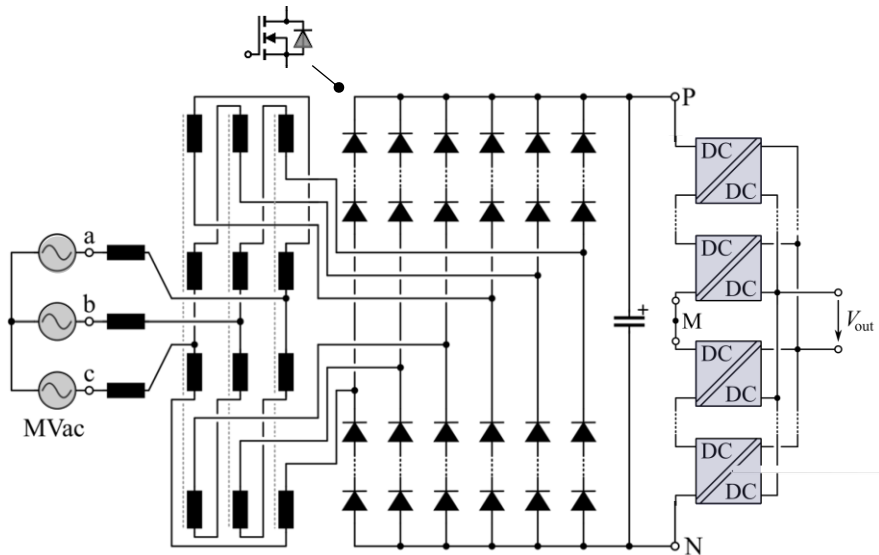
- 10kV_{AC} Medium-Voltage Input Stage Directly Supplying a 240V_{DC} Bus (Alibaba, or 336V_{DC})
- 36-Pulse Diode (!) Rectifier Topology / Low S.C. Current per Load Output / Scalable Beyond 2.5 MW
- 98.5% Efficiency & Ultra-High Reliability / 50% Smaller Installation Footprint / 20% Lower Investment \$\$\$



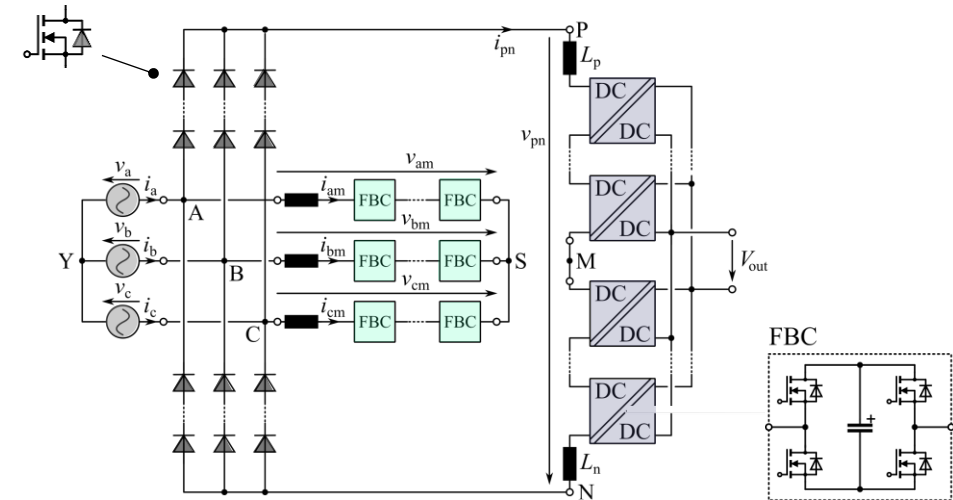
- Input Stage Topology Analogous to SIEMENS ROBICON MV Variable-Frequency Drives (2.4–13.8kVAC, 50/60Hz)
- SuperX AI Technology Ltd — “Panama”-800VDC End-to-End Solution (Employs Phase-Shift Transformers)

Hybrid Quasi-Single-Stage 3- Φ AC/DC SSTs

- **12-Pulse Line Interphase Transformer Rectifier OR 6-Pulse Diode Rectifier & AC-Connected MMLC-Type Active Filter**
- **Alternative Central Diode Rectifier & Local $\pm 10...20\text{kV}_{DC} / \pm 800\text{V}_{DC}$ DC/DC-SSTs**



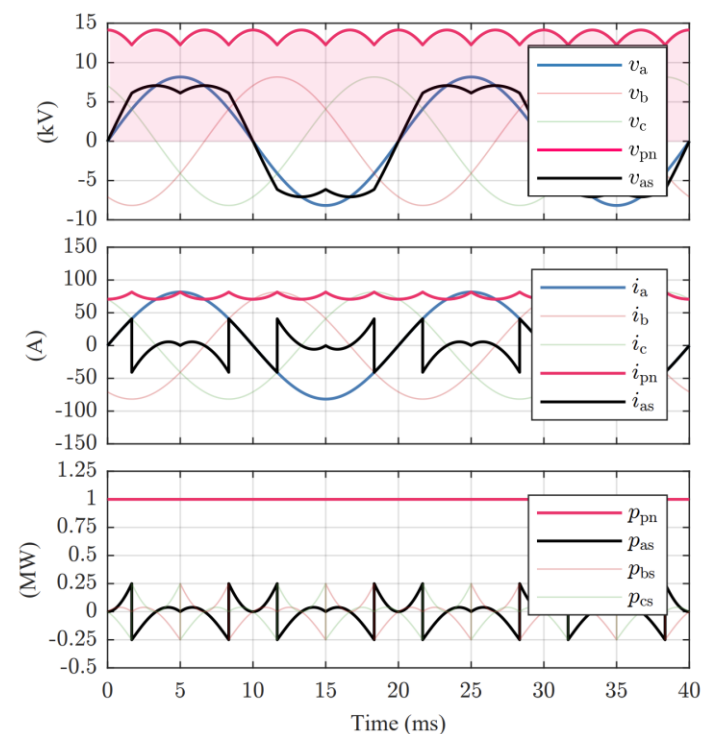
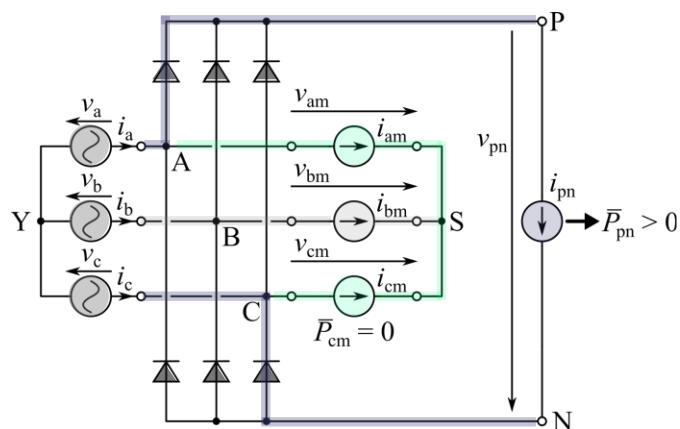
Source: EP 3905480A1, 2020
DE 3826524C2, 1988



- **Uncontrolled DC Voltage Level w/ 12-Pulse or 6-Pulse Ripple**
- **Overall Realization Effort / Protection / Handling of SST-Internal Failures & Redundancy / etc. Still to be Clarified**

3- Φ Diode-Bridge & Active-Filter Front-End

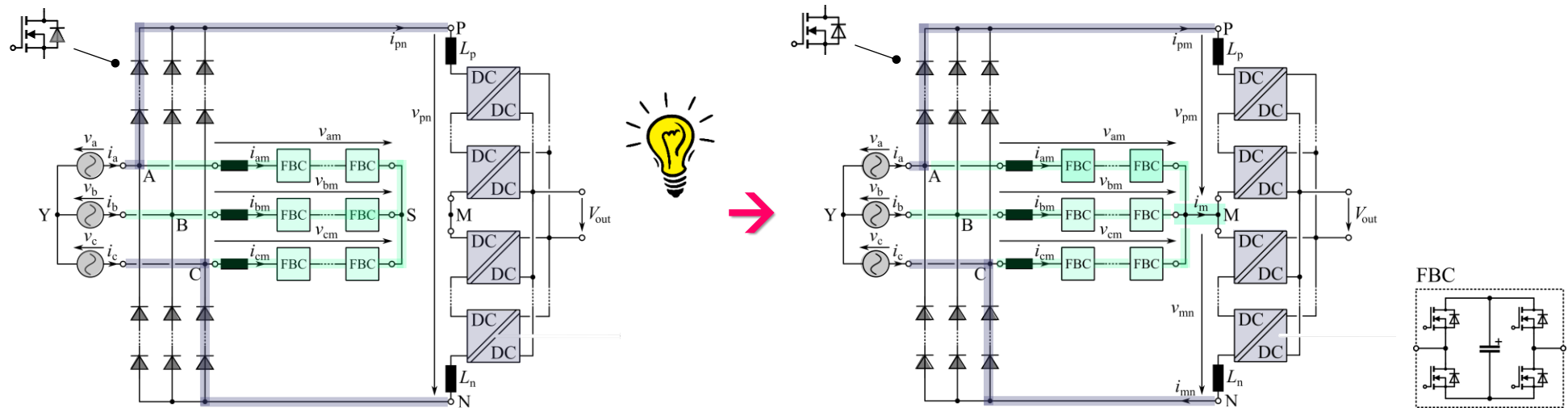
- Operation @ 10kV_{Line-to-line} AC-Mains & 1MW
- Characteristic Waveforms



- *Possible Limitation of AF Operation to Phases w/ Max. & Min. Voltage / 2-out-of-3 Filter Branches (!)*
- *Saving of AF Sw. Losses But Higher AF String Voltages*

Modularized 3- Φ VIENNA-Rectifier-Type SST

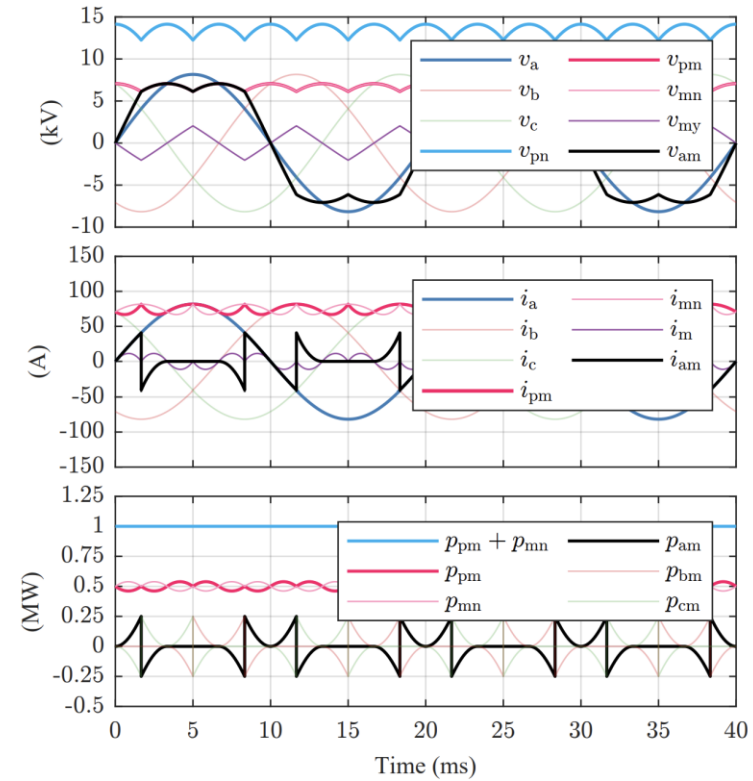
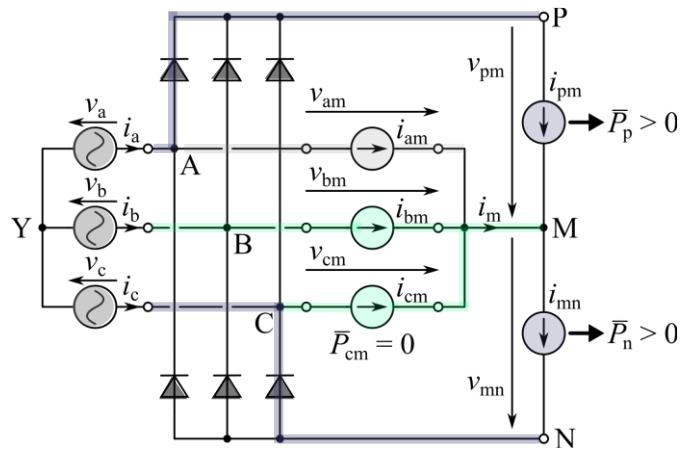
- *Active Filter Star-Point Connected to DC Output Voltage Midpoint*
- *Modularized VIENNA Rectifier Topology (mVR)*



- *Active Balancing of Upper & Lower DC/DC SST String Voltages*
- *Full-Bridge-Cell-(FBC)-String Voltages Defined by Half Mains Line-to-Line Voltage Amplitude*

3- Φ VIENNA-Rectifier-Type AC/DC SST

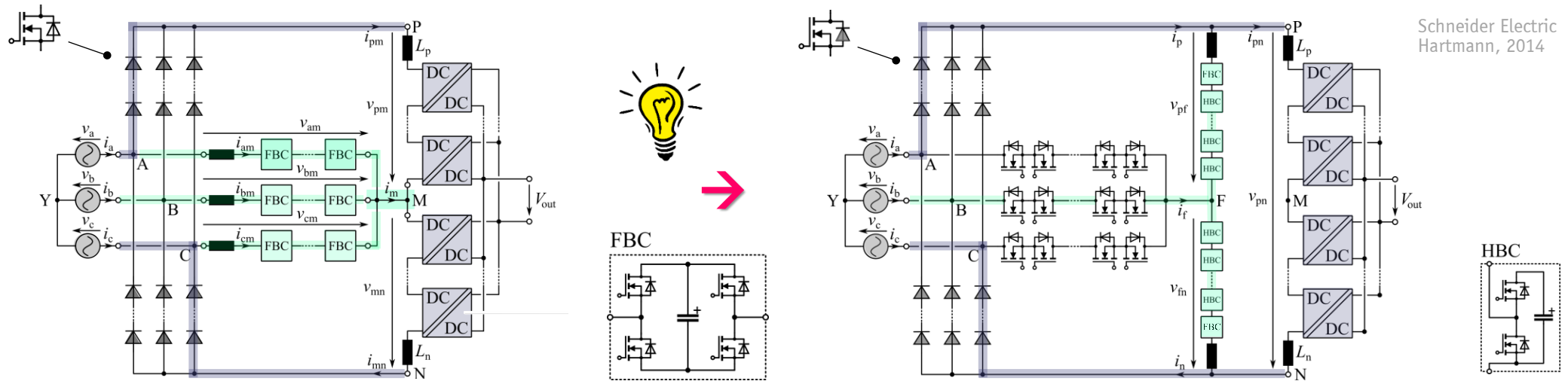
- Operation @ 10kV_{Line-to-line} AC-Mains & 1MW
- Characteristic Waveforms



- 3/3 Act. Filter Operation / All 3 Filter Branches Active / Avg. $i_m = 0$ / $i_{pm} = i_{mn}$
- Low Sw. Loss 2/3 Operation Utilizes Midpoint Connection to Allow i_m / Decouple i_{pm} and i_{mn}

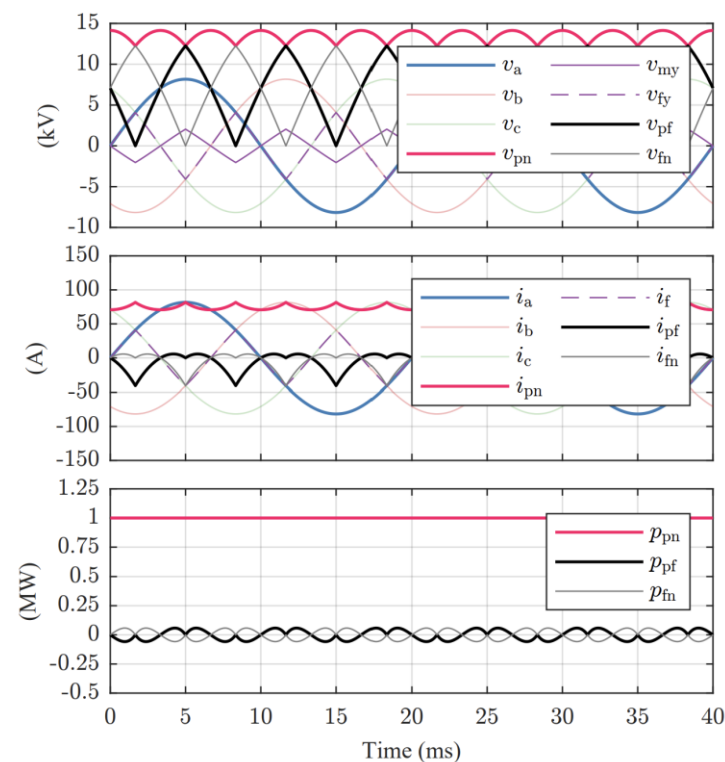
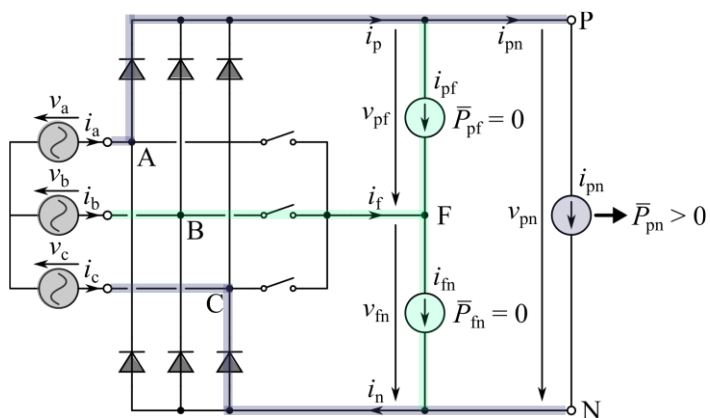
3- Φ Diode-Bridge & Integrated Active Filter SST

- **AC-Connected Active Filter (AF) w/ Full-Bridge Cells Shifted to Diode-Bridge DC Output / Half-Bridge Cells AF (!)**
- **Phase Selector Switches / Injection of Current into Phase of Not Conducting Diode Branch**



- **Lower Complexity Compared to AC-Side Active Filter / mVR**
- **Mains Frequency Commutation of Current Injector Switches / Blocking Voltage Balancing Requirement**

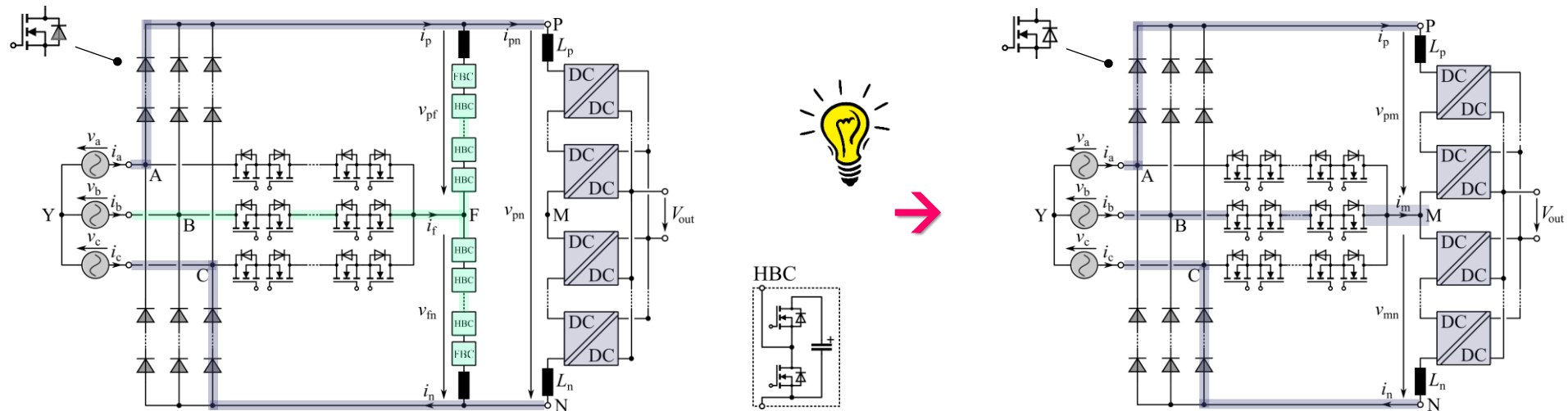
- Operation @ 10kV_{Line-to-line} AC-Mains & 1MW
- Characteristic Waveforms



- **Max. Voltage of $\sqrt{3}/2$ Grid Line-to-Line Voltage Amplitude Across Upper and Lower Filter String**
- **Low Voltage Values v_{pf} & v_{fn} @ High Values of Currents i_{pf} & i_{fn} — Low Power Rating of Filter String**

Unfolder-Front-End 3- Φ AC/DC SST

- *Combination of Integrated Active Filter & DC/DC Converter Functionality*
- *Difference of Upper & Lower DC/DC Conv. String Currents Injected into Phase with Blocking Diode Branch*

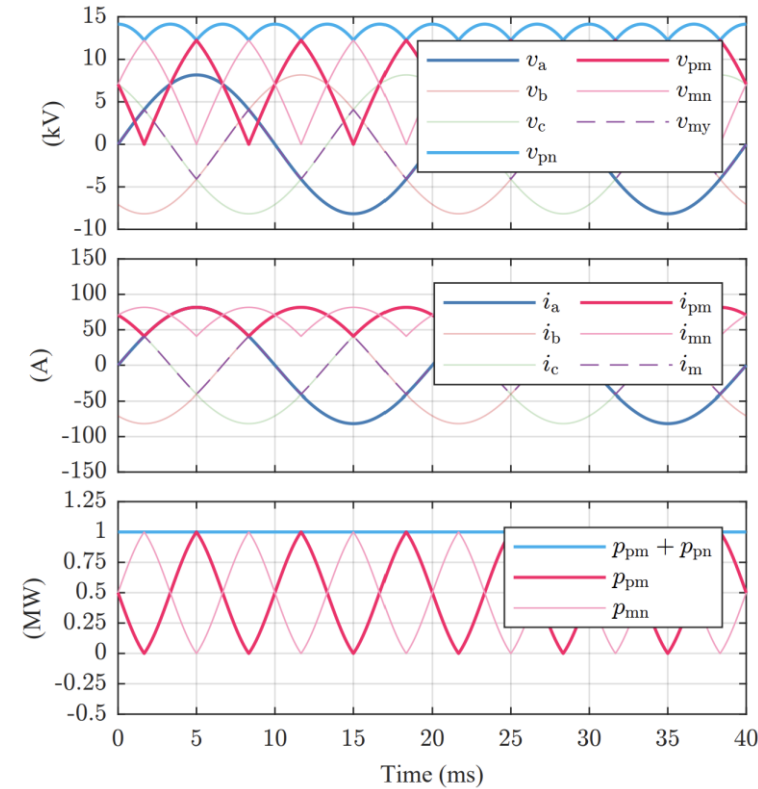
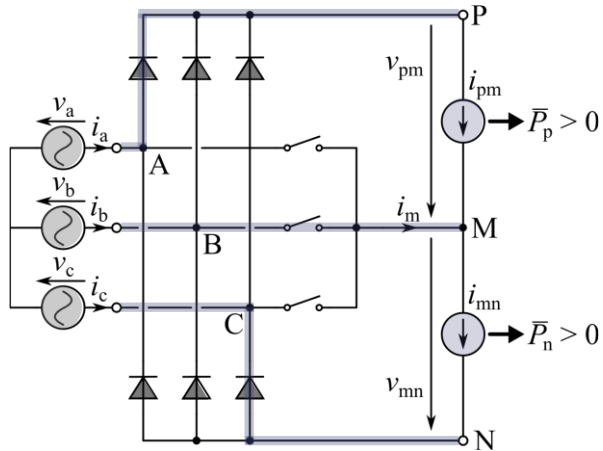


Utah State Univ.
Chen et al., 2017

- *Lower Complexity Compared to Integrated Active Filter Diode-Bridge Rectifier*
- *Large Voltage & Power Fluctuations of the DC/DC Converters Strings / Rel. Low DC/DC Stage Utilization*

Unfolder-Front-End 3- Φ AC/DC SST

- Operation @ 10kV_{Line-to-line} AC-Mains & 1MW
- Characteristic Waveforms

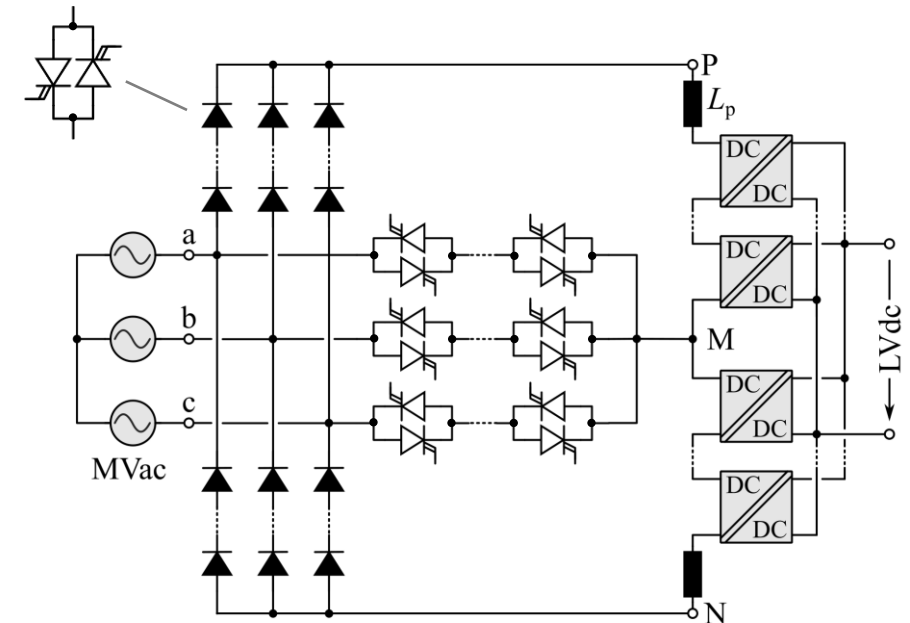
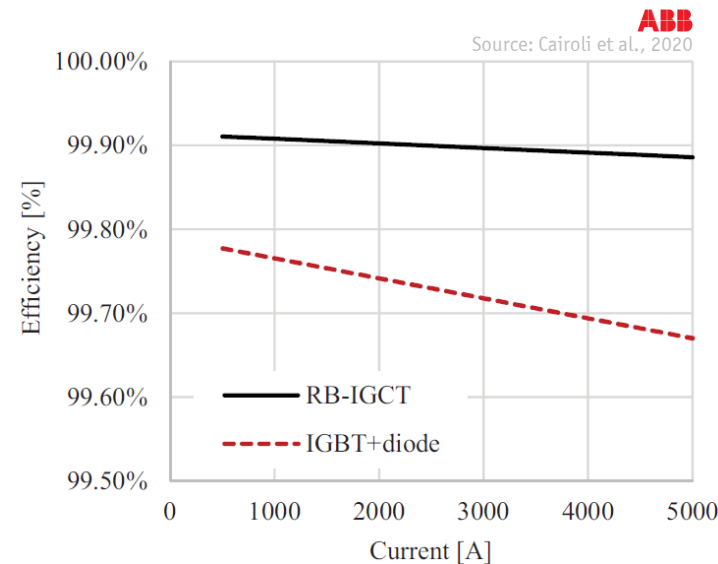
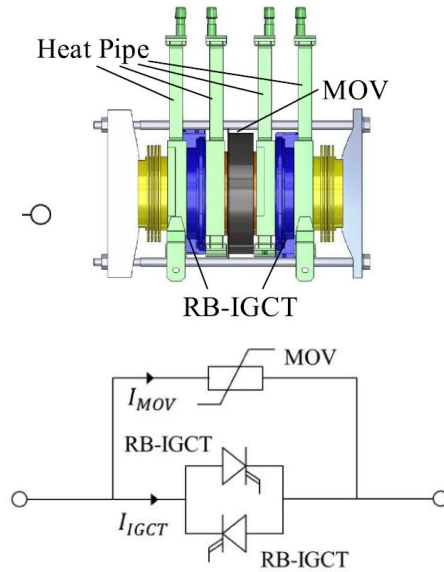


- Voltages v_{pm} & v_{fm} of DC//DC Conv. Strings Varying Btw 0... $\sqrt{3}/2$ Line-to-Line Voltage Amplitude
- Power Processed by DC//DC Conv. Strings Fluctuates Btw 0... $P_{nominal}$

*Reverse-Blocking IGCTs
Si-MOSFET & Cascaded SiC JFETs*

Reverse-Blocking-IGCT Injection Switches

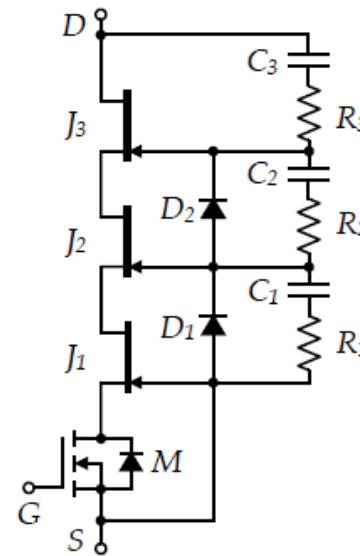
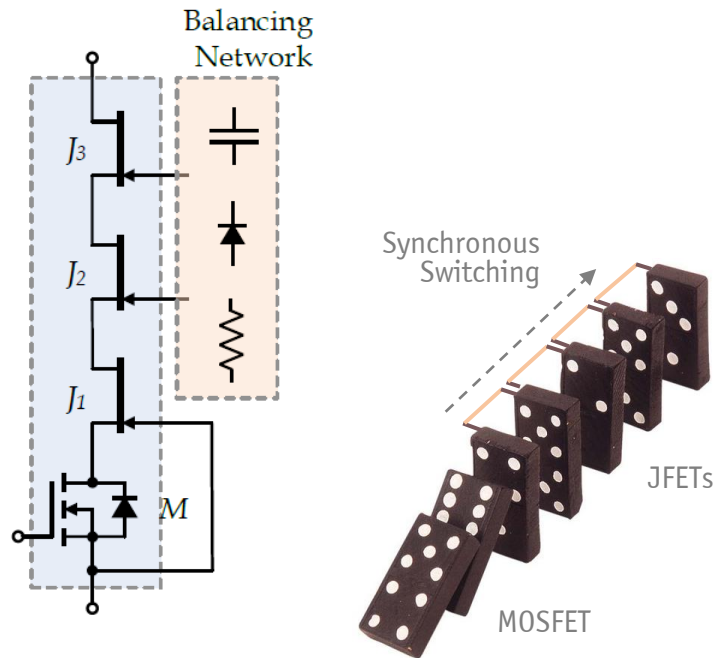
- **IGCT** — Thyristor w/ Integrated Low-Inductance Gate Drive Enabling Fast Turn-Off and High-Power Switching
- **RB IGCTs** — Full Forward & Full Reverse Blocking Capability / Typ. Used in Curr. Source Converters & DC SSCBs



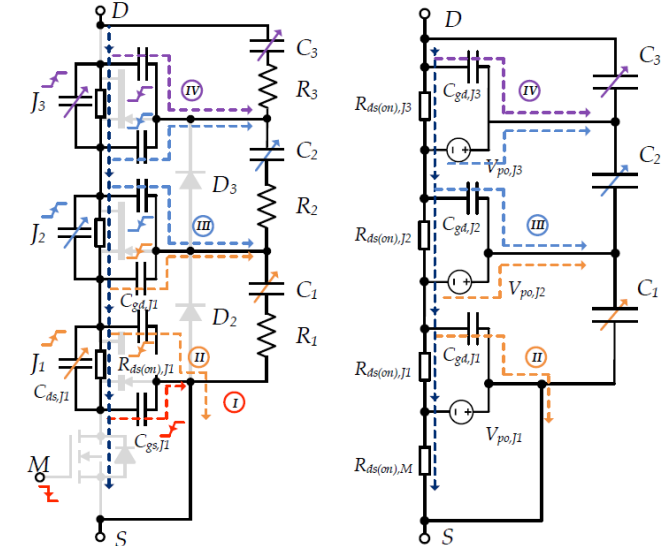
- **Specific Device Designs for Very Low On-State Losses** – 0.9V@1kA for 2.5kV Blocking Voltage / High Turn-Off Currents
- **Field Failure Rate (FIT) of GCT & Gate Unit Below 100 FIT** — Future SiC ETO Devices up to 22kV

SiC Super-Cascode Injection Switches

- **Cascode Configuration** — LV Si-MOSFET & Normally-ON SiC JFET / Linear ON-Resistance Scaling (!) / Low \$\$\$
- **Supercascode** — Series JFETs Enable High Blocking Voltage / Passive Dynamic & Static Voltage Balancing



Source: L. Gill et al., 2021, Sandia National Labs

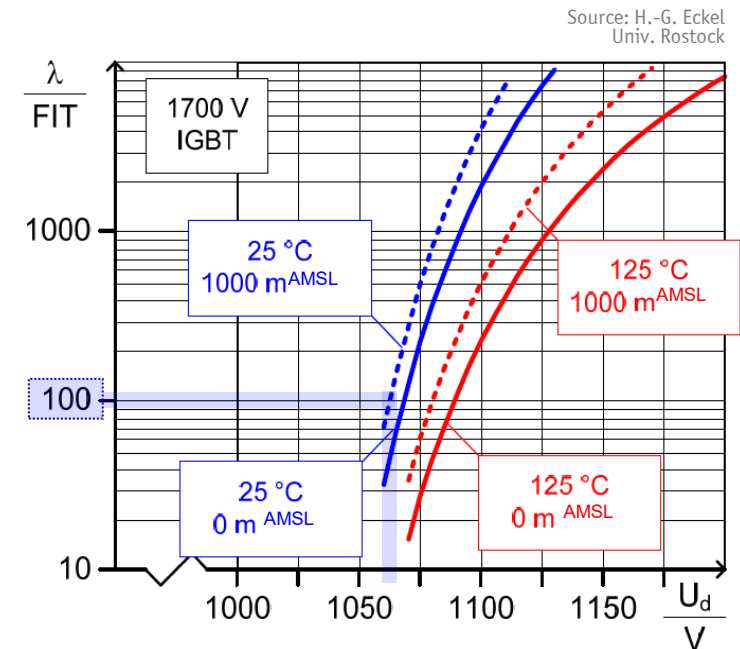
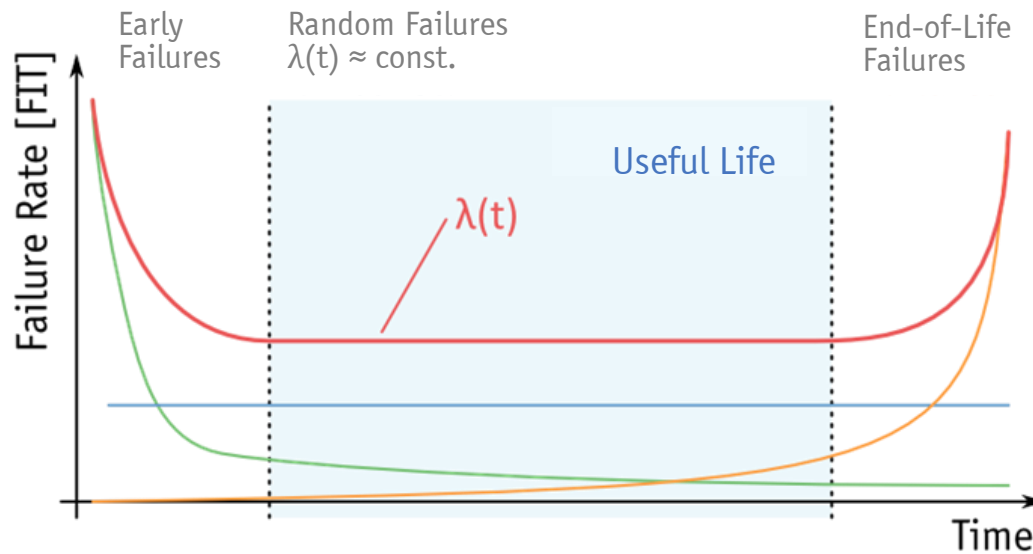


- **Different Balancing Network Topologies** — RC Snubbers & Avalanche Diodes / Challenging Design Due to Parasitics
- **Integration in Power Module Enables Controlled Parasitics** / Consistent Switching Characteristics

*Reliability for k -out-of- n
Redundancy*

Redundancy in Multi-Cell Converter Systems 1/3

- **Failure Rate $\lambda(t)$ is a Function of Time – „Bathtub Curve“**
- **Useful Life Dominated by Random Failures (e.g. Cosmic Rays) $\rightarrow \lambda(t) = \text{const.}$**
- **$[\lambda] = 1 \text{ FIT}$ (1 Failure in 10^9 h)**
- **Typ. Value for IGBTs: 100 FIT**



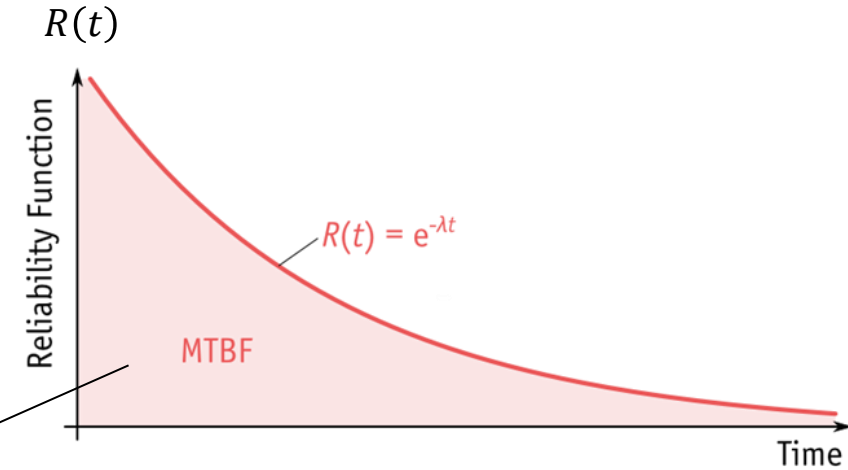
- **Sources for Empirical Component Failure Rate Data — MIL-HDBK-217F, IEC Standard 62380, etc.**

Redundancy in Multi-Cell Converter Systems 2/3

- **Reliability Function** — Probability of System being Operational after Time t

$$R(t) = e^{-\int_0^t \lambda(x) dx} = e^{-\lambda t}$$

$\lambda(t) = \text{const.}$

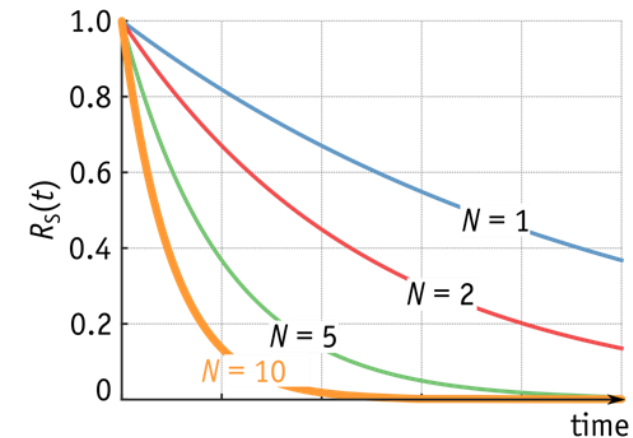
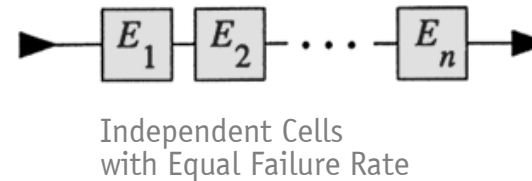


- **Mean Time Between Failures**

$$\text{MTBF} = \int_0^{\infty} R(t) dt = \int_0^{\infty} e^{-\lambda t} dt = \frac{1}{\lambda}$$

- **Series Structure**

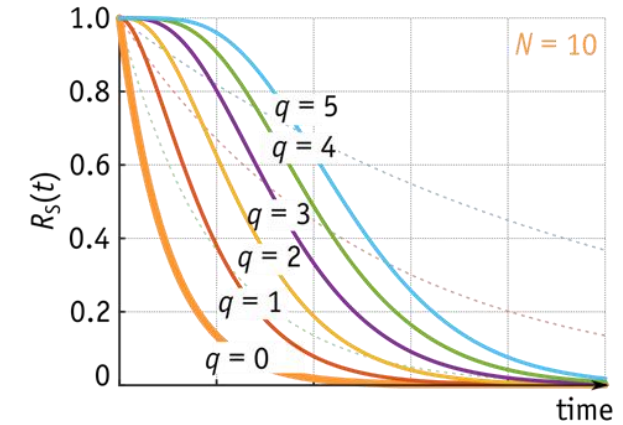
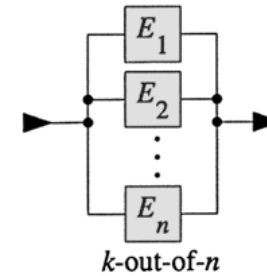
$$\lambda_S = \sum_{i=1}^n \lambda_i$$



Redundancy in Multi-Cell Converter Systems 3/3

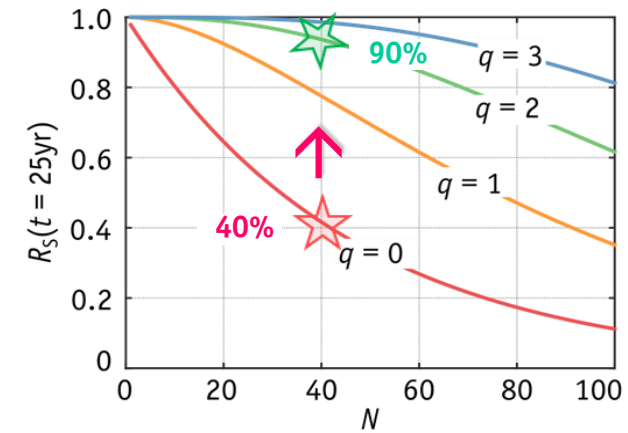
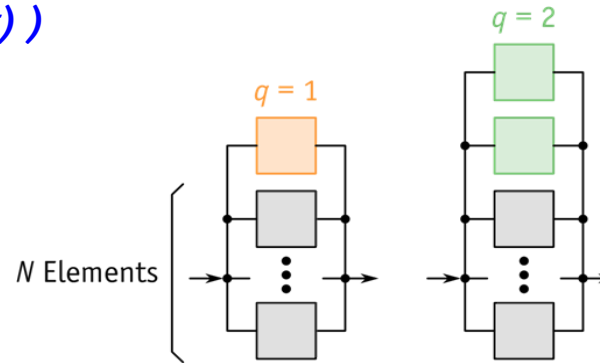
- ***k-out-of-n Redundancy***
Redundancy of Cells in Phase Stack

System is Operational as Long as at Least k -out-of- n Subsystems are Working



- ***Effect of q Redundant Cells on $R_S(t)$ and/or MTBF (Area below $R_S(t)$)***

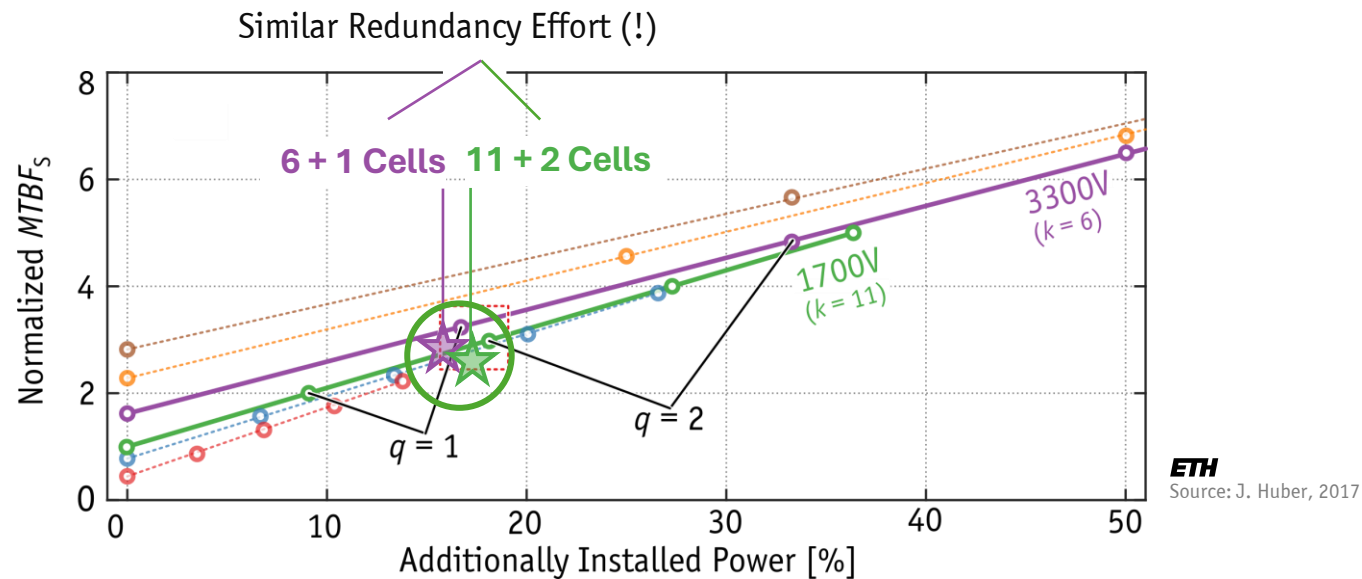
Independent Cells
with Equal Failure Rate



- ***Redundancy Significantly Improves System-Level Reliability (!)***

Cost of Redundancy

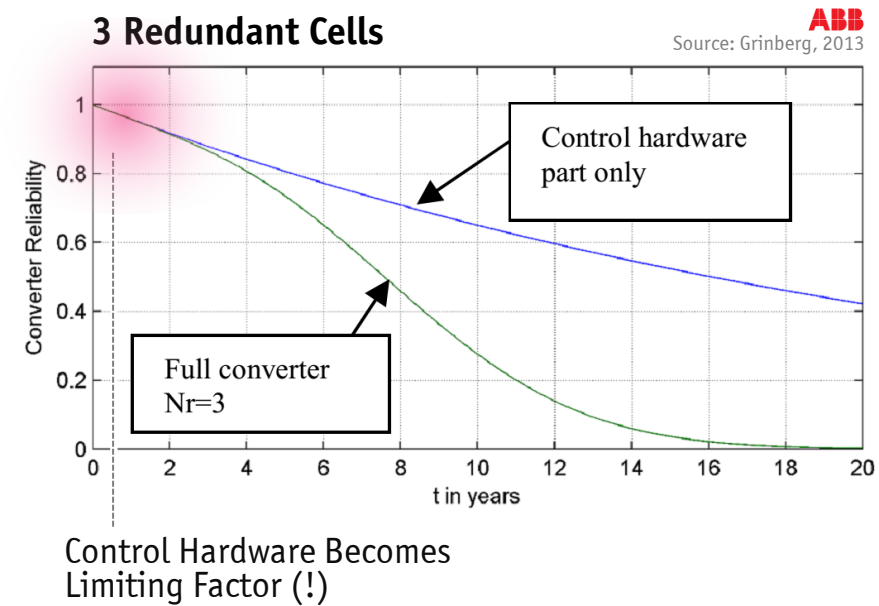
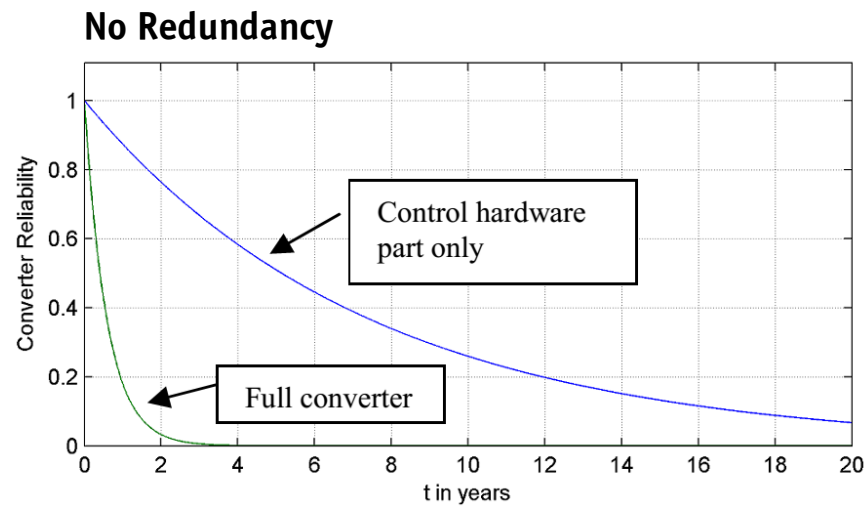
- **Redundant Cells** — *Additionally Installed But Unused Power Processing Capability (Standby)*
- **Example: Phase Stacks with Same Total DC Voltage & Different Number of Cells**



- **Similar Added Power Capability** → **Similar Normalized MTBFs**
- **Simplified Consideration / Beware Overheads and Reliability Bottlenecks – Control System etc. (!)**

Reliability “Bottlenecks”

- *Very Effective Reliability Improvement by Means of Cell-Level Redundancy — Too Good to Be True?*

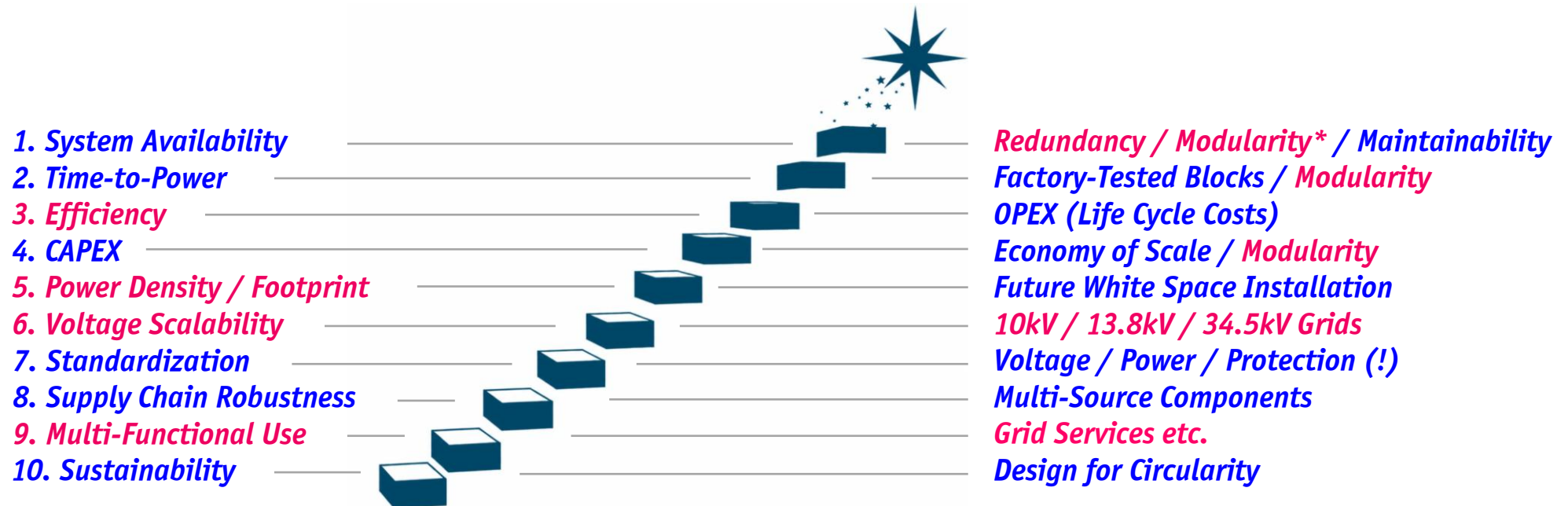


- *Redundancy Effectiveness Limited by Other (Non-Redundant) Parts of the Converter System (!)*
- *Control / Auxiliary Supplies / Communication Systems / Bypass Devices / etc.*



Short-Term Datacenter SST Priorities

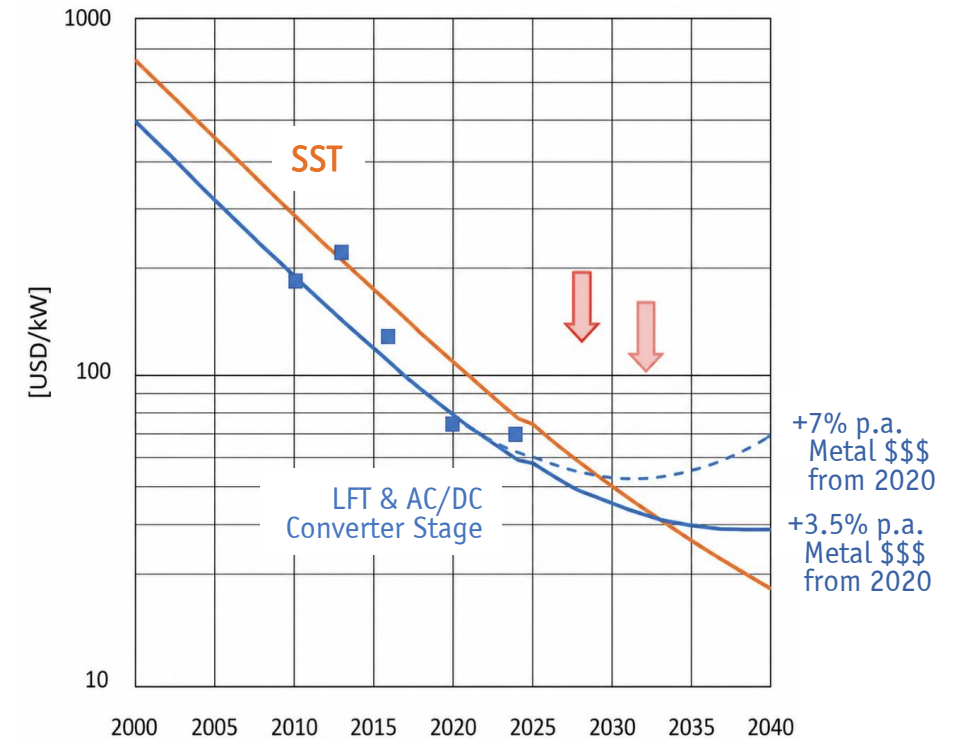
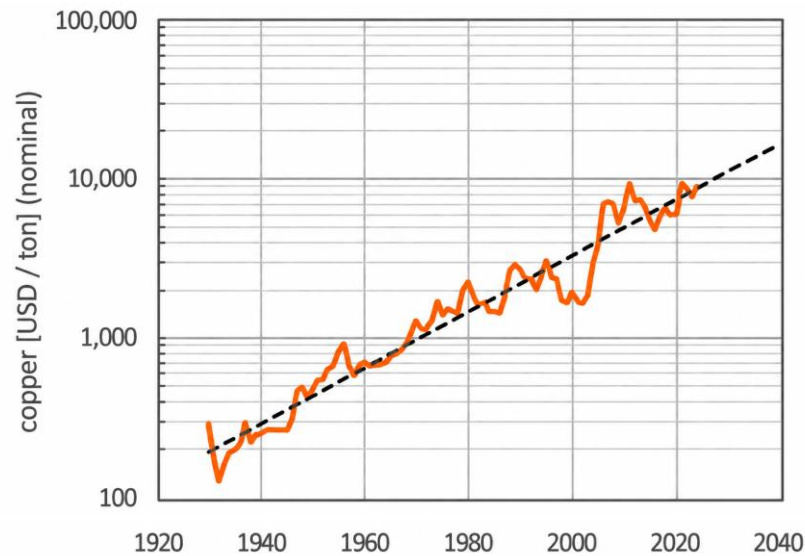
- *Major Innovation Step #1 — 54V_{DC} → 800V_{DC} / Higher Efficiency @ High Power*
- *Major Innovation Step #2 — Elimination of AC/DC-Stage of UPS / Higher Efficiency*
- *SST vs. LFT-Based-Solution — Functionally Largely Equivalent / Availability? / 99% SST Efficiency?*



- ** Large # of Modules / High Redundancy → Same Availability as for Low # of Modules @ Same Cost*
- *Complex Multi-Objective Decision Processes / Main Criteria Currently NOT Considered in Academic Research (!)*

Potential Cost Benefits of SSTs over LFT-Based Solutions

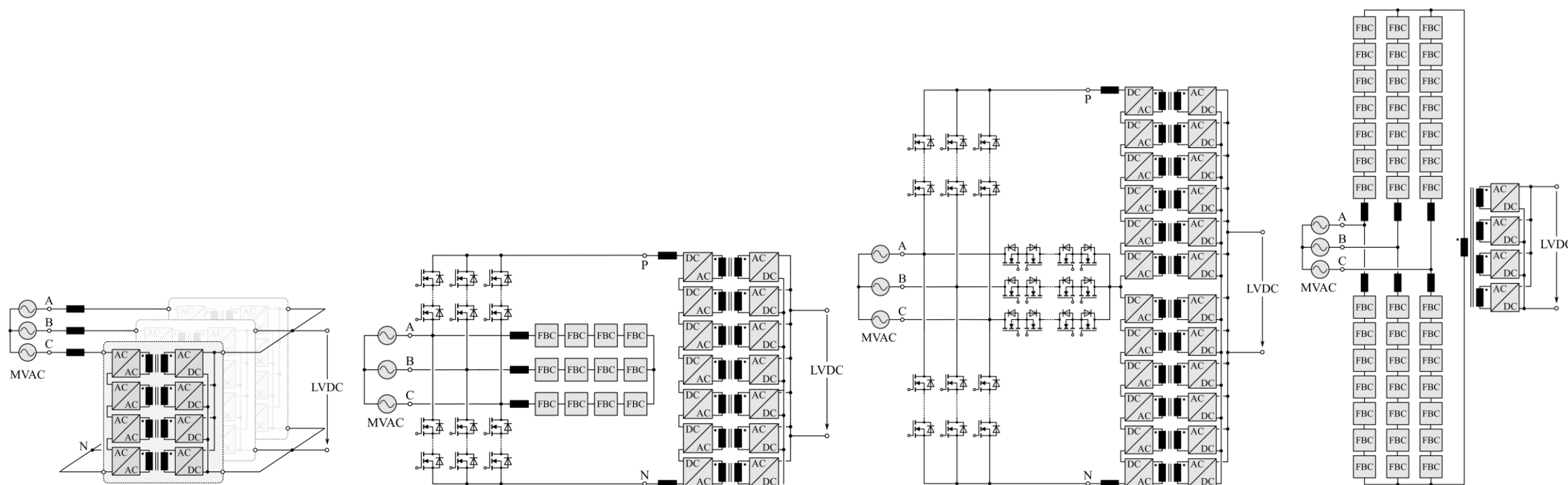
- *Calculation of Price Trends (Nominal USD) Based on International Energy Agency (IEA) Data*
- *LV AC/DC Converter — Based on Grid-Scale PV | -11% p.a. | ≈60 USD/kW*
- *LFT — +3.5% p.a. \$\$\$ of Metals Since 1920 | 10 USD/kAV*
- *SST Power Electronics \$\$\$ — 1.5x LV AC/DC Converter*
- *MFT \$\$\$ — Constant @ 15 USD/kVA*



- *LFT & Multi-Pulse Rectifier — Availability & Cost-Optimized Near-Term Solution*
- *MVAC-800 VDC SST — Integration / Density / Functionality-Optimized Longer-Term Solution*

Next-Generation 3- Φ AC/DC SST Research Scope 2/3

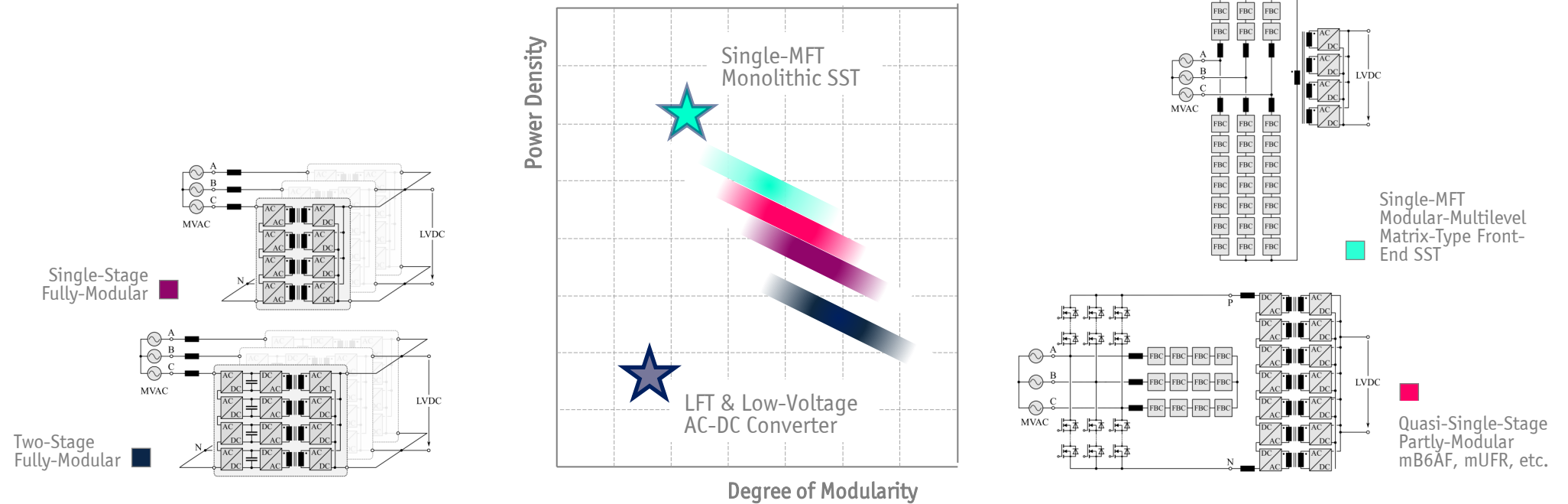
- **Fully-Modular Single-Stage** — High Modularity | Requires AC-Switches | Design for $3x P_{pk}=2/3P_{out}@100Hz$ & $3x P_{avg}=1/3P_{out}$
- **Partly-Modular Quasi-Single-Stage** — Unfolder-Type Front-End | Design for $2x P_{pk}=P_{out}@150Hz$ & $2x P_{avg}=1/2P_{out}$
- **Single-Stage Matrix-Type** — Redundancy Limited to Sw. Stages | High Transformer Utilization | Limited Modularity



- **Comparative Evaluation incl. mB6AF** — Diode-Bridge Rectifier Front-End & Active Filter Common to Several SST Units
- **Overall Realization Effort / Protection / Handling of SST-Internal Failures & Redundancy / etc. Must be Clarified**

Power Density / Modularity Trade-Off

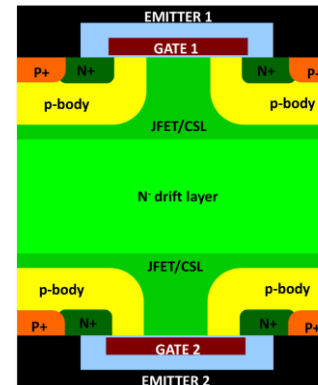
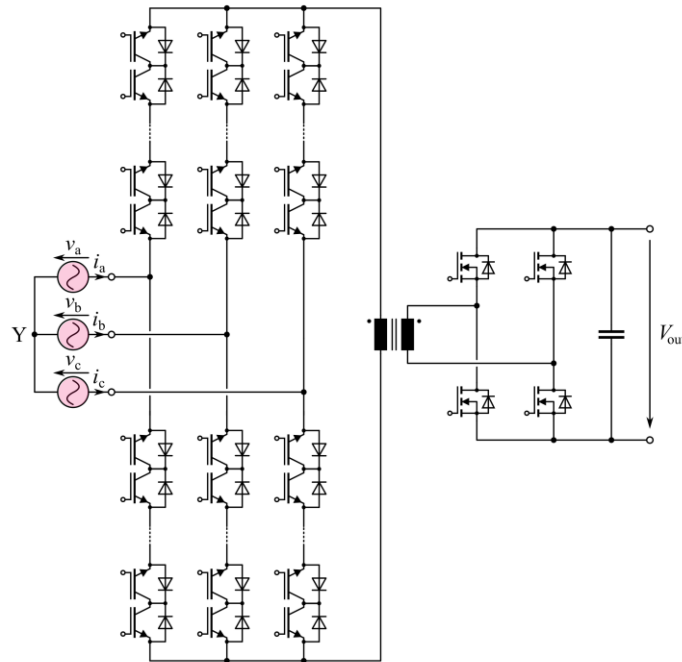
- **Transformer Scaling Law** — Favors Single-Transformer Over Multiple Transformers
- **Processing of Pulsating Power @ 100Hz or 150Hz** vs. Constant Power Flow
- **Modularization Penalty** — Accumulation of Isolation Distances



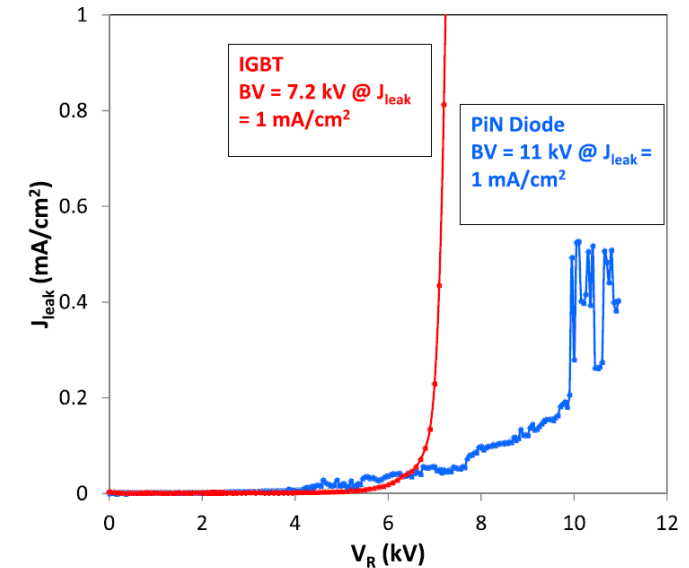
- **"Zero-Order" Engineering Estimate Shown Above** — Requires Rigorous Validation Through Future Research (!)

Next-Generation 3- Φ AC/DC SST Research Scope 3/3

- **Monolithic Bi-Directional SiC IGBT w/ Double-Sided Lithography Process on Free-Standing n^- Wafers**
- **MOS-Cells on Both Sides of Lightly Doped Drift Region / Cond. & Sw. Loss Infl. of Back-Side Gate Volt. Bias**
- **Challenging Packaging & Cooling**



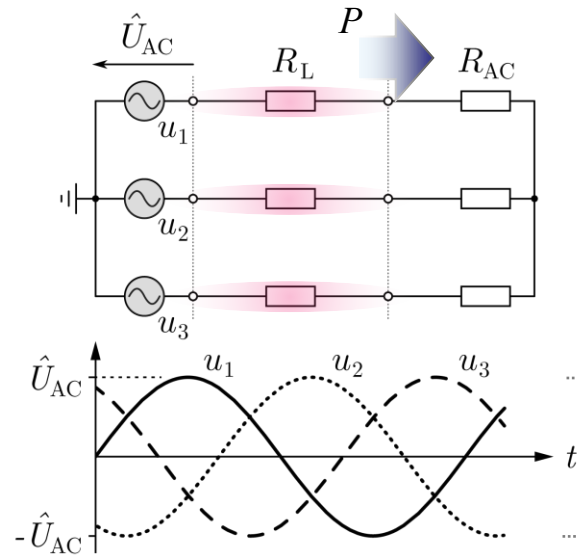
Blocking Voltage
↑↓



- **15kV BD-IGBT | Measured Blocking Capability of 7.2 kV – Epi Layer Defects etc.**
- **Shared Drift Region → “True” Monolithic Bidirectional Switch (TM-BDS)**

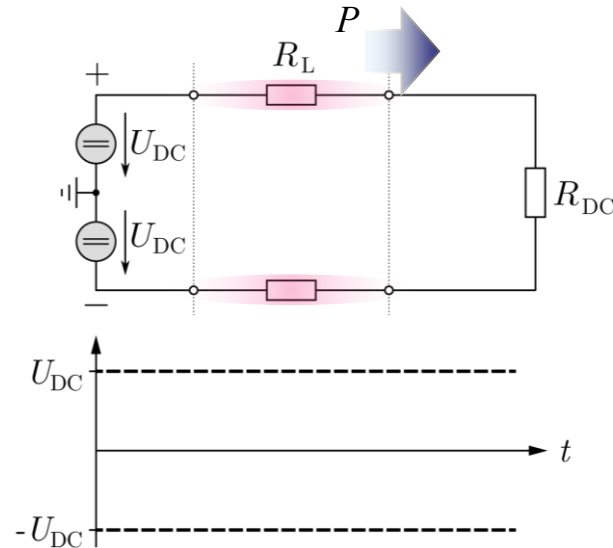
Remark DC vs. 3-Φ AC Power Distribution

- **DC Voltage** → **Max. Utilization of Isolation Voltage** → **Lower Losses & Less Conductor Material (!)**



$$P_{V,AC} = 3 \cdot \left(\frac{\frac{1}{3}P}{U_{AC}} \right)^2 \cdot R_L$$

$$\frac{P_{V,DC}}{P_{V,AC}} = \frac{3}{2} \cdot \left(\frac{U_{AC}}{U_{DC}} \right)^2 \mid_{U_{DC} = \hat{U}_{AC} = \sqrt{2} U_{AC}} = 0.75$$



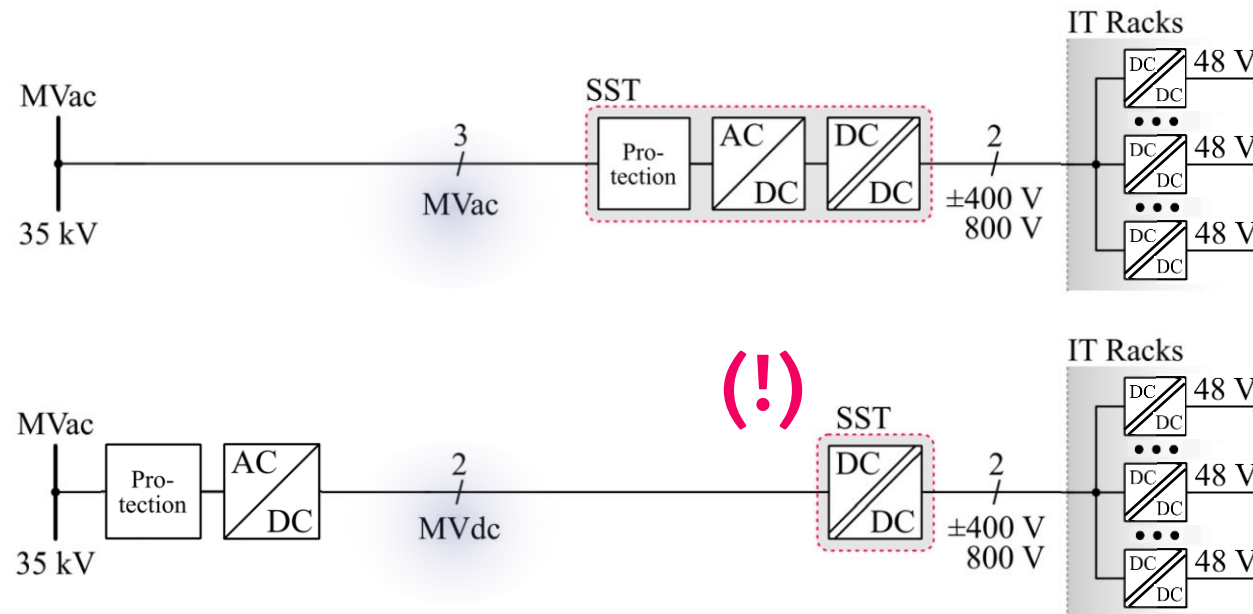
$$P_{V,DC} = 2 \cdot \left(\frac{P}{2U_{DC}} \right)^2 \cdot R_L$$

U_{AC} ... RMS Phase Voltage

- **Central MVAC Rectification & Local High-Power Density/Efficiency MVDC/LVDC SSTs**

Future MVDC vs. 3- Φ MVAC Power Distribution

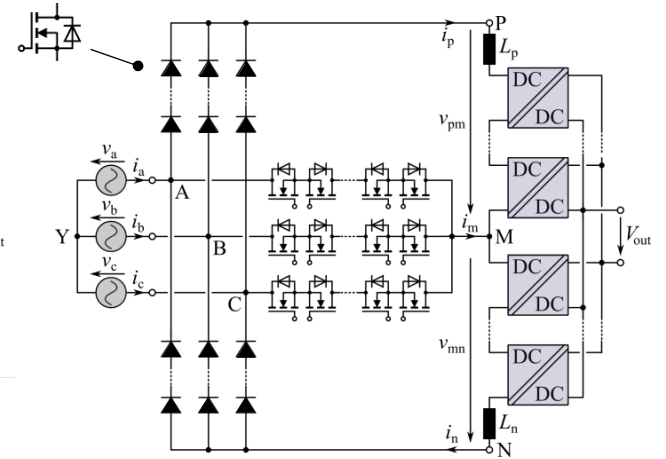
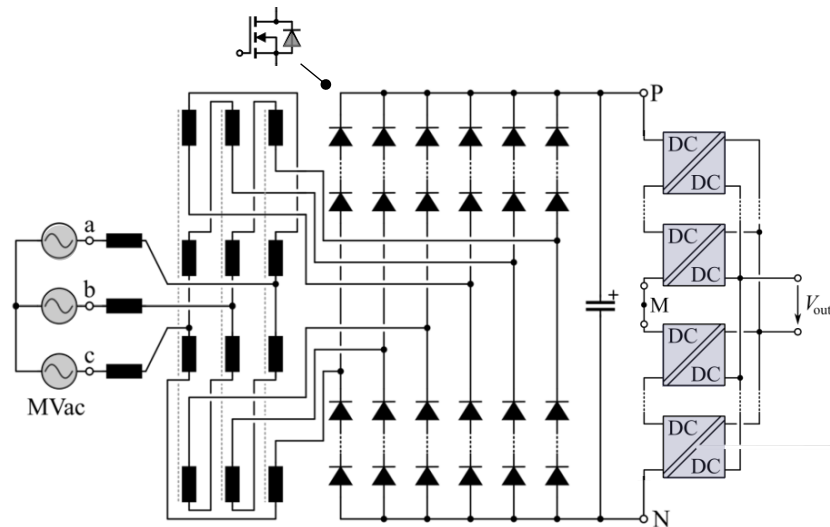
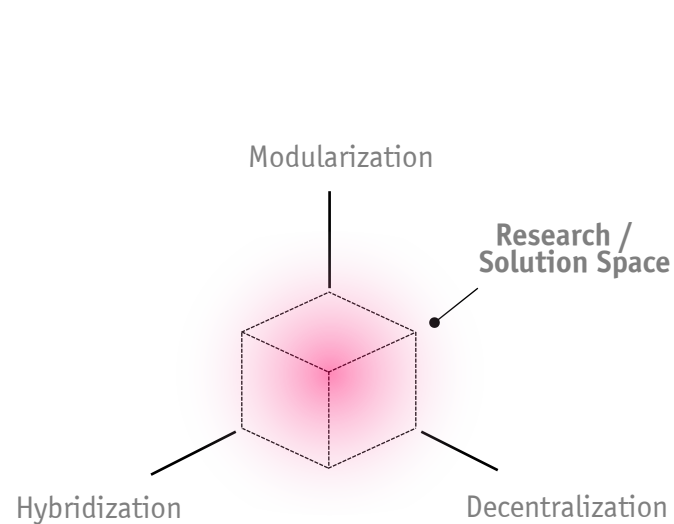
- **DC Voltage** $\rightarrow$ **Max. Utilization of Isolation Voltage** $\rightarrow$ **Lower Losses & Less Conductor Material (!)**
- **Central MVAC Rectification & Local High-Power Density High-Efficiency Low-Complexity MVDC/LVDC SSTs**



- **Analysis of SST Current-Limiting Capabilities / DC Solid-State Circuit Breaker Concepts**
- **MVDC Grid Stability Analysis incl. Local Power/Energy Buffer Concepts**

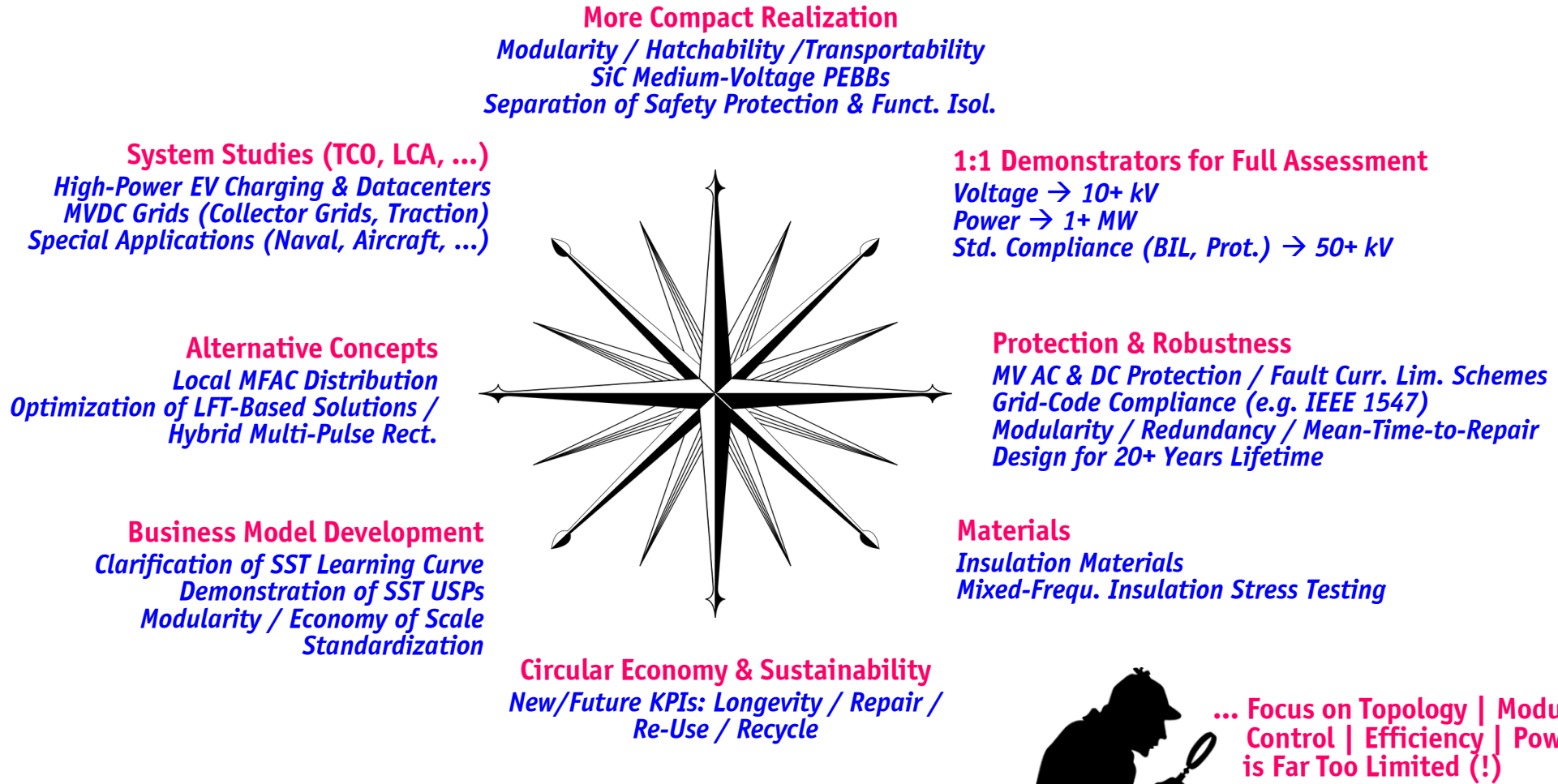
Next-Generation 3- Φ AC/DC SST Research Scope 1/3

- **Category #1 – Novel SST Concepts (Degree of Modularization & Hybridization)**
- **Category #2 – Distribution Architecture (Degree of Decentralization & Voltage Level & Protection) / $\pm 10\text{kVDC}$, 500Hz AC?**



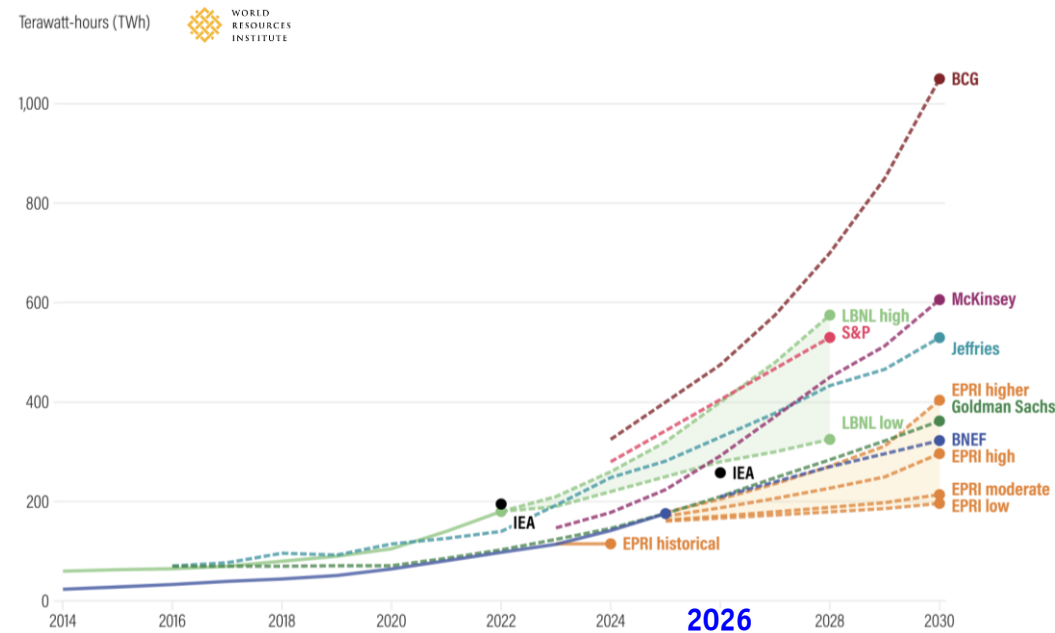
- **Keep All Converter Strings Active All Time**
- **Aim for High Utilization / Avoid Processing of $2 \times f_{\text{Mains}}$ Power and/or Fluctuating Voltage**

Research Vectors



! Remark Overbuilding & Overspending (?)

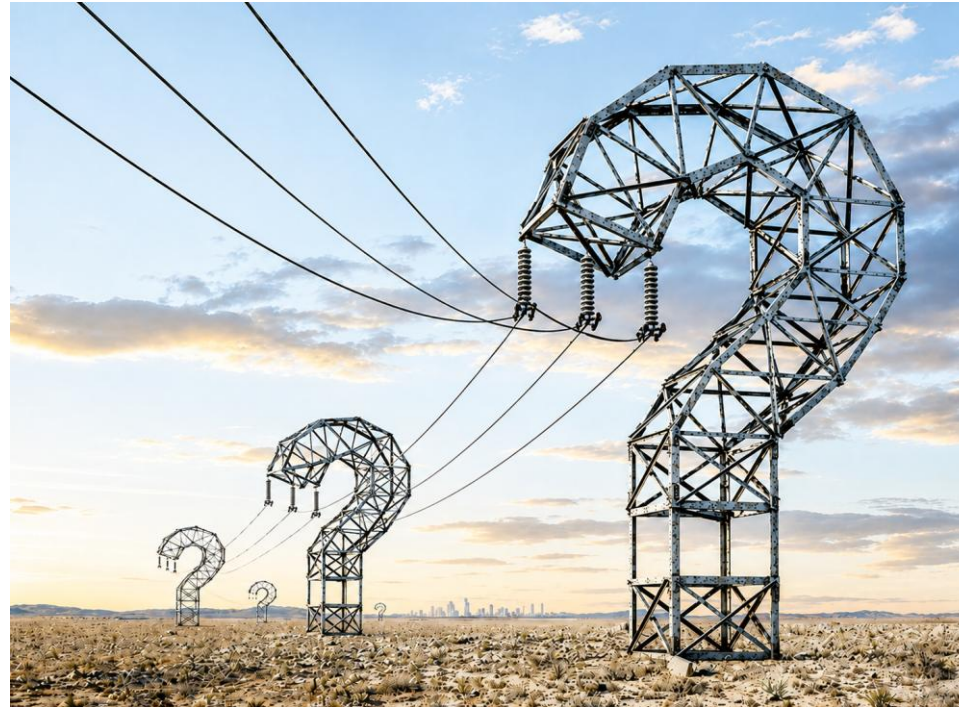
- *Extreme Variations in Projections of US Datacenter Consumption in 2030 (!)*
- *200 TWh...1000 TWh → 5 ... 25% of US Electricity Consumption*



- *Technology Leaps — Hardware/Software/Cooling/Optical Computing Promise Massive Efficiency Gains*
- *“Rather Risk Misspending x 100 Billion USD Than Be Late to Superintelligence” (M. Zuckerberg)*

Thank you!

Source: P. Aylward



Further Reading — <https://ams.ee.ethz.ch/publications.html>