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SYSTEM-LEVEL OPTIMIZATION OF THREE-PHASE THREE-LEVEL T-TYPE UPS SYSTEM

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For my wife Regina.

Contents

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Hirofui Uemura
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Abstract

Demand for highly efficient and very compact power converters has kept increasing in industrial applications such as general power supply systems, Power Conditioning Systems (PCSs) and Uninterruptible Power Supplies (UPSs) systems over the last decades. In order to optimize the performance of the converter systems and achieve both high efficiency and high power density, and multi-objective optimization must be performed during the development. A typical development process of a power converter system in an industrial company consists of several iterations of prototype hardware production, evaluation and design improvement procedures. However, the production of several prototypes results in higher development time and cost. Therefore, multi-objective optimization is an interesting alternative but has to cover several domains and must involve a large number of power components; accordingly, it is a rather complicated procedure and it is therefore difficult to perform the system-level optimization automatically.

The main goal of this thesis is to give a comprehensive automatic system-level optimization procedure of a 20 kVA three-phase three-level UPS system and an experimental evaluation of the losses, volumes and thermal models of the components. The approach includes detailed electro-thermal and magneto-thermal coupled losses / volume calculation models for power semiconductors, forced cooling extruded heat sinks, differential-mode (DM) inductors, and common-mode (CM) inductors. A simple losses / volume calculation model for capacitors, auxiliary circuits, and resistive components of the system are also included. The switching losses of different combinations of power semiconductors are experimentally measured and the most suitable semiconductor combinations for input side rectifier and output side inverter has been decided. In addition a local optimization model for DM induc-

tors including an extended compact thermal model to determine the hot-spot temperature inside a winding is proposed and experimentally evaluated. Typically, the EMI filter design is complicated and time consuming. This thesis also provides a detailed automatic two-stage EMI input filter design procedure including an EMI noise estimation technique. Combining this filter design procedure and the filter component losses / volume / thermal calculation models, the proposed optimization procedure is able to give a practically reasonable filter design under consideration of thermal constraints.

Four different magnetic materials and wide range of design parameters such as switching frequency and relative current ripple in the inductors are considered in the system-level optimization. An amorphous material is found to be a suitable selection for high efficiency and power density at reasonable cost. Optimum design parameters for hardware realization are selected based on the analysis of the trade-off between the system performances. As a result, a switching frequency of 16 kHz and a relative current ripple of 20 % are selected for 96.4 % efficiency at 2.3 kVA/dm^3 power density. In order to determine a practical number for power density, a virtual prototyping with 3D-CAD is performed. A practically realized UPS hardware achieves 0.9 kVA/dm^3 power density which shows good agreement with the virtual prototyping result. Finally, a measurement of the total system losses and an EMI test are performed on the realized hardware. Measurement result shows an efficiency of 96.5 % and confirm a less than 5 % error between measured losses and the proposed loss calculation model. Also it is confirmed that the realized EMI input filter satisfies the EMI requirement.

Kurzfassung

Der Bedarf an hocheffizienten und sehr kompakten leistungselektronischen Konvertern, wie zum Beispiel allgemein Stromversorgungen, Leistungsaufbereitungssystemen (Power Conditioning Systems, PCSs) und unterbrechungsfreien Stromversorgungen (Uninterruptible Power Supplies, UPSs), ist weiter zunehmend. Um die Leistungsfähigkeit von solchen Stromrichtersystemen zu optimieren und sowohl einen hohen Wirkungsgrad als auch eine hohe Leistungsdichte zu erzielen, muss während der Entwicklung ein Mehrkriterienoptimierungsverfahren verwendet werden. Der heute typischerweise in der Industrie angewendete Entwicklungsprozess für Stromrichtersysteme besteht aus mehreren Iterationen über Prototypenherstellung, Evaluation und anschliessende Verbesserung der Auslegung. Die Herstellung von mehreren Prototypen benötigt jedoch viel Zeit und resultiert daher in Zeitverzögerungen und hohen Kosten. Andererseits handelt es sich bei der Mehrkriterienoptimierung um einen komplexen, viele Bereiche umfassenden Vorgang, der eine grosse Zahl von Leistungskomponenten einschliesst, und daher eine automatische Optimierung auf Systemebene anspruchsvoll werden lässt.

Das hauptsächliche Ziel dieser Arbeit ist die Entwicklung eines kompletten, automatischen Optimierungsverfahrens auf Systemebene für ein dreiphasiges 20 kVA Dreilevel-UPS-System, sowie die experimentelle Evaluation der Komponentenmodellierung hinsichtlich Verlusten, Volumina und thermischen Berechnungen. Dieser Ansatz für eine Optimierung auf Systemebene umfasst ein detailliertes, gekoppeltes elektrothermisches und magnetothermisches Berechnungsmodell für Verluste und Volumina von Leistungshalbleitern, Zwangskühlsystemen basierend auf anwendungsspezifischen Kühlkörpern, sowie Gegentakt- (differential-mode, DM) und Gleichtaktdrosseln (common-mode, CM Induktivitäten). Ein einfaches Berechnungsmodell für Verluste und

Volumina von Kondensatoren, Hilfsstromkreisen und resistiven Komponenten im Stromrichter wird ebenfalls verwendet. Die Schaltverluste von verschiedenen Kombinationen von Leistungshalbleitern werden experimentell bestimmt und die geeignetsten Halbleiterkombinationen für den aktiven Eingangsgleichrichter und den Ausgangswechselrichter ausgewählt. Des Weiteren wird ein lokales Optimierungsmodell für Gegentaktdrosseln vorgeschlagen und experimentell evaluiert, welches ein erweitertes kompaktes thermisches Modell zur Ermittlung der maximalen Temperatur in der Wicklung beinhaltet. Typischerweise ist die Auslegung von EMV-Filtern eine komplizierte und zeitaufwändige Aufgabe. Die vorliegende Arbeit enthält deshalb auch ein detailliertes automatisches Auslegungsverfahren für zweistufige EMV-Filter, das eine Methode zur Abschätzung der leitungsgebundenen elektromagnetischen Störaussendung umfasst. Durch die Kombination dieses Filterauslegungsverfahrens mit den Berechnungsmodellen für Verluste und Volumina der Filterkomponenten sowie den entsprechenden thermischen Modellen kann das vorgeschlagene Optimierungsverfahren praxisnahe Filterauslegungen bestimmen, die auch thermische Einschränkungen berücksichtigen.

Die Optimierung auf Systemebene berücksichtigt vier verschiedene Magnetkernmaterialien sowie weite Parameterbereiche für beispielsweise die Schaltfrequenz oder den zulässigen relativen Stromrippel in den Filterinduktivitäten. Ein *amorphes* Kernmaterial wird als geeignete Wahl für die Erreichung eines hohen Wirkungsgrades und einer hohen Leistungsdichte bei vernünftigen Kosten identifiziert. Basierend auf der Analyse des Kompromisses zwischen den Kennwerten der entsprechenden Systeme werden optimale Auslegungsparameter für die Realisierung eines Prototypen ausgewählt. Für eine Schaltfrequenz von 16 kHz und einen relativen Stromrippel von 20 % ergeben sich so ein Wirkungsgrad von 96.4 % und eine Leistungsdichte von 2.3 kVA/dm^3. Um die praktisch realisierbare Leistungsdichte zu ermitteln, wird virtuelles Prototyping mittels 3D-CAD verwendet. Der tatsächlich realisierte Aufbau eines UPS-Systems erreicht schliesslich eine Leistungsdichte von 0.9 kVA/dm^3, was gut mit den Resultaten des virtuellen Prototypings übereinstimmt. Schlussendlich werden die gesamten Systemverluste des aufgebauten Prototypen sowie auch dessen EMV-Verhalten messtechnisch bestimmt. Die Resultate zeigen einen Wirkungsgrad von 96.5 %, was einer Abweichung von weniger als 5 % zwischen gemessenen und mit den vorgeschlagenen Verlustmodellen bestimmten Verlusten ent-

spricht. Ebenfalls kann gezeigt werden, dass das realisierte EMV-Filter die entsprechenden EMV-Anforderungen erfüllt.

Notation

Symbols

Φ_{d}	Phase displacement between the fundamental components of current and voltage	[rad]
$d\Theta$	Reference phase difference between the fundamental input voltage and the modulation signal	[rad]
$\epsilon_{\mathrm{c-hs}}$	Relative permittivity of the thermal contact material	
ϵ_{p}	Emissivity of the base plate surface	
ϵ_c	Emissivity of the magnetic core surface	
ϵ_0	Permittivity of free space	[F/m]
η	Efficiency or relative losses	[%]
$\gamma_{\mathrm{i,dc}}$	Factor of peak-to-peak HF current ripple to the average (DC) current	
$\gamma_{\mathrm{i,in}}$	Factor of peak-to-peak HF input current ripple to the LF peak current	
$\gamma_{\mathrm{i,out}}$	Factor of peak-to-peak HF output current ripple to the LF peak current	
$\gamma_{\mathrm{v,in}}$	Maximum peak-to-peak input phase voltage ripple	[V]
$\gamma_{\mathrm{v,out}}$	Maximum peak-to-peak output phase voltage ripple	[V]
λ_{air}	Thermal conductivity of air	$[\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})]$

$\lambda_{\mathrm{c,xy}}$	Thermal conductivity of the magnetic core in x and y directions	$[\mathrm{W/(m \cdot K)}]$
$\lambda_{\mathrm{c,z}}$	Thermal conductivity of the magnetic core in z direction	$[\mathrm{W/(m \cdot K)}]$
λ_{hs}	Thermal conductivity of the heat sink material	$[\mathrm{W/(m \cdot K)}]$
$\bar{\mu}$	Complex magnetic permeability	[H/m]
μ'	Real part of the complex magnetic permeability	[H/m]
μ_{r}	Relative magnetic permeability	
μ_0	Permeability of free space	[H/m]
ω	Angular frequency of the voltage fundamental	[rad/s]
$\omega_{\mathrm{in,LF}}$	Angular frequency of the input fundamental	[rad/s]
$\omega_{\mathrm{out,LF}}$	Angular frequency of the output fundamental	[rad/s]
ρ	Power density	$[\mathrm{kW/dm^3}]$
ρ_{air}	Density of air	$[\mathrm{kg/m^3}]$
ρ_{Cu}	Resistivity of the PCB trace material	$[\Omega \cdot \mathrm{m}]$
σ	Stefan-Boltzmann constant $= 5.67 \times 10^{-8}$	$[\mathrm{W/(m^2 \cdot K^4)}]$
$\sigma_{\mathrm{th,c-hs}}$	Thermal impedance of the insulation sheet	$[\mathrm{K \cdot m^2/W}]$
θ	Angle of the winding per phase of the CM inductor	[rad]
$\Delta\varphi_{\mathrm{L,cm}}$	Maximum peak-to-peak voltage-second product of the CM inductor	[Vs]
$\Delta\varphi_{\mathrm{L,dc}}$	Maximum peak-to-peak voltage-second product of the DC filter inductor	[Vs]
$\Delta\varphi_{\mathrm{L,in}}$	Maximum peak-to-peak voltage-second product of the DM inductor (input)	[Vs]
$\Delta\varphi_{\mathrm{L,out}}$	Maximum peak-to-peak voltage-second product of the DM inductor (output)	[Vs]
φ	Phase of the voltage fundamental	[rad]

$\varphi_{\mathrm{L,cm}}$	Temporal voltage-seconds of the CM inductor	[Vs]
$\varphi_{\mathrm{L,in}}$	Temporal voltage-seconds of the DM inductor	[Vs]
$\varphi_{\mathrm{L,out}}$	Temporal voltage-seconds of the DM inductor	[Vs]
ϑ_{amb}	Ambient temperature	[°C]
$\vartheta_{\mathrm{c,max}}$	Maximum operating temperature of the magnetic core	[°C]
$\vartheta_{\mathrm{chs,max}}$	Maximum inductor core hot-spot temperature	[°C]
$\vartheta_{\mathrm{j,max}}$	Maximum junction temperature	[°C]
$\vartheta_{\mathrm{whs,max}}$	Maximum inductor winding hot-spot temperature	[°C]
$A_{\mathrm{c,xy}}$	Total surface area of the magnetic core in x and y directions	[m^2]
$A_{\mathrm{c,z}}$	Total surface area of the magnetic core in z direction	[m^2]
A_{cp}	Contact area between the magnetic core surface and the base plate surface	[m^2]
A_{e}	Effective cross-section area of magnetic core	[m^2]
A_{L}	AL value of the magnetic core	[$\mathrm{H/turn}^2$]
A_{pa}	Total open surface area of the base plate	[m^2]
$A_{\mathrm{th,c-hs}}$	Cross-section area of thermal interface	[m^2]
$A_{\mathrm{th,c-hs}}$	Cross-section area of thermal contact material	[m^2]
$Att_{\mathrm{cm,req}}$	Required CM attenuation of the EMI input filter	[dB]
$Att_{\mathrm{dm,req}}$	Required DM attenuation of the EMI input filter	[dB]
Att_{cm}	CM attenuation of the EMI input filter	[dB]
Att_{dm}	DM attenuation of the EMI input filter	[dB]
$B_{\mathrm{cm,HF}}$	Magnetic flux density due to high frequency CM current	[$\mathrm{Wb/m}^2$]

$B_{\mathrm{dm,HF}}$	Magnetic flux density due to high frequency DM current	[Wb/m^2]
$B_{\mathrm{dm,LF}}$	Magnetic flux density due to low-frequency DM current	[Wb/m^2]
B_{tot}	Total magnetic flux density of the CM inductor	[Wb/m^2]
B_{pk}	Peak magnetic flux density	[Wb/m^2]
B_{sat}	Saturation magnetic flux density	[Wb/m^2]
C	Capacitance value	[F]
$C_{1,\mathrm{cm}}$	Capacitance value of the CM capacitor of the first filter stage	[F]
$C_{1,\mathrm{dc,min}}$	Minimum capacitance value of the DC-link capacitors	[F]
$C_{1,\mathrm{dc}}, C_{2,\mathrm{dc}}$	Capacitance value of the DC-link capacitors	[F]
$C_{1,\mathrm{in,max}}$	Maximum capacitance of the first stage of the EMI input filter	[F]
$C_{1,\mathrm{in,min,f}}$	Minimum capacitance of the DM capacitor to maintain the resonance frequency (input)	[F]
$C_{1,\mathrm{in,min,V}}$	Minimum capacitance of the DM capacitor to maintain the voltage ripple (input)	[F]
$C_{1,\mathrm{in,min}}$	Minimum capacitance of the first stage of the EMI input filter	[F]
$C_{1,\mathrm{in,r/s/t}}$	Capacitance of the capacitor of the first stage of the EMI input filter	[F]
$C_{1,\mathrm{max}}$	Maximum capacitance of the capacitor of the first stage of the CM filter	[F]
$C_{1,\mathrm{out,max}}$	Maximum capacitance of the first output filter stage	[F]
$C_{1,\mathrm{out,min,f}}$	Minimum capacitance of the DM capacitor to maintain the resonance frequency (output)	[F]
$C_{1,\mathrm{out,min,V}}$	Minimum capacitance of the DM capacitor to maintain the voltage ripple (output)	[F]

$C_{1,\mathrm{out,min}}$	Minimum capacitance of the first output filter stage	[F]
$C_{1,\mathrm{out,u/v/w/n}}$	Capacitance of the capacitor of the first stage of the output filter	[F]
$C_{2,\mathrm{cm}}$	Capacitance value of the CM capacitor of the second filter stage	[H]
$C_{2,\mathrm{in,r/s/t}}$	Capacitance of the capacitor of the second stage of the EMI input filter	[F]
$C_{2,\mathrm{max}}$	Maximum capacitance of the CM capacitor of the second filter stage	[F]
$C_{2,\mathrm{out,u/v/w/n}}$	Capacitance of the capacitor of the second output filter stage	[F]
C_{d}	Capacitance of the damping capacitor	[F]
C_{g}	Total parasitic capacitance between the DC-link bus and GND	[F]
$C_{\mathrm{in,d}}$	Capacitance value of the damping capacitor (input)	[F]
C_{p}	Total parasitic capacitance between the semiconductor package and GND	[F]
$\mathrm{D}_\sharp$	Symbol for diodes	
D_{sw}	Normalized period the device acts as a switch	
$\Delta E_{\mathrm{on,T}}$	Additional turn-on energy loss due to reverse recovery	[J]
$E_{\mathrm{dm,max}}$	Maximum magnitude of the DM voltage in the frequency-domain	[dBµV]
$E_{\mathrm{off,const}}$	Constant part of turn-off energy	[J]
$E_{\mathrm{off,I}}$	Proportional part of turn-off energy	[J/A]
$E_{\mathrm{on,const}}$	Constant part of turn-on energy	[J]
$E_{\mathrm{on,I}}$	Proportional part of turn-on energy	[J/A]
$E_{\mathrm{on,T,0}}$	Turn-on energy loss without reverse recovery	[J]
$G_{\mathrm{in,LISN,cm,a}}(s)$	Transfer function of the first CM current path	
$G_{\mathrm{in,LISN,cm,b}}(s)$	Transfer function of the second CM current path	

$G_{\mathrm{in,LISN,dm}}(s)$	Transfer function of the DM current path	
$\mathrm{GS}_\sharp$	Gate signal of a power semiconductor	
$\Delta I_{\mathrm{L,cm,HF}}$	Maximum high-frequency peak-to-peak CM current ripple	[A]
$\Delta I_{\mathrm{L,HF}}$	Maximum peak-to-peak inductor current ripple	[A]
$\hat{I}_{\mathrm{ac}}$	Peak value of phase current fundamental	[A]
$\hat{I}_{\mathrm{pk,LF}}$	Peak value of the current fundamental	[A]
$I_{\mathrm{avg,dc}}$	Averaged current in DC–DC converter	[A]
I_{avg}	Average current	[A]
I_{bt}	Nominal battery current	[A]
$I_{\mathrm{C,LF}}$	Low-frequency reactive current through the filter capacitor	[A]
I_{C}	Max. DC collector current of IGBTs	[A]
I_{F}	Max. DC forward current of diodes	[A]
$I_{\mathrm{in,pk}}$	Nominal input peak current	[A]
$I_{\mathrm{L,dc}}$	Averaged DC inductor current	[A]
$I_{\mathrm{leak,gnd,max}}$	Maximum leakage current to GND	[A]
$I_{\mathrm{leak,gnd}}$	Leakage current to GND	[A]
$I_{\mathrm{out,pk}}$	Nominal output peak current	[A]
$I_{\mathrm{pk,cm,3h,max}}$	Maximum low-frequency peak CM current of the EMI input filter	[A]
$I_{\mathrm{pk,cm,3h}}$	Low-frequency peak CM current of the EMI input filter	[A]
$I_{\mathrm{Rd,pk,LF}}$	Peak current through the damping resistor	[A]
$I_{\mathrm{rms,dc}}$	RMS current in DC–DC converter	[A]
I_{rms}	RMS current	[A]
$I_{\mathrm{sw,avg}}$	Averaged switching current over a single fundamental period	[A]
I_{rrm}	Maximum reverse recovery current of the semiconductor devices	[A]
L_{hs}	Length of the heat sink	[m]

L	Inductance value	[H]
L_σ	Leakage inductance	[H]
$L_{1,\mathrm{cm}}$	Inductance value of the first stage CM inductor	[H]
$L_{1,\mathrm{dc}}, L_{2,\mathrm{dc}}$	Inductance value of the DC inductor	
$L_{1,\mathrm{in,r/s/t}}$	Inductance of the inductor of the first EMI input filter stage	[H]
$L_{1,\mathrm{out,u/v/w/n}}$	Inductance of the inductor of the first output filter stage	[H]
$L_{2,\mathrm{cm}}$	Inductance value of the CM inductor of the second filter stage	[H]
$L_{2,\mathrm{in,r/s/t}}$	Inductance of the inductor of the second stage of the EMI input filter	[H]
$L_{2,\mathrm{out,u/v/w/n}}$	Inductance of the inductor of the second output filter stage	[H]
$L_{3,\mathrm{cm}}$	Inductance value of the CM inductor of the third filter stage	[H]
L_{cm}	Inductance of the CM inductor	[H]
L_{fan}	Length of the cooling fan	[m]
$L_{\mathrm{hs,min}}$	Minimum length of the heat sink unit	
$L_{\mathrm{semi,tot}}$	Required mounting length per single heat sink unit	[m]
M	Modulation index	
M_{dc}	Modulation index of the DC part	
M_{in}	Modulation index of the input rectifier part	
M_{out}	Modulation index of the output inverter part	
N	Number of turns	[turn]
N_{case}	Total number of the semiconductor cases at the input side	
N_{max}	Maximum number of iterative loop for electro-thermal model	
N_{p}	Number of paralleled modules	
N_{semi}	Number of power semiconductor parameter sets	

P_{ac}	Active power of input / output side	[W]
$P_{\mathrm{aux,tot}}$	Total power consumption of the auxiliary circuit	[W]
$P_{\mathrm{c,cm}}$	Magnetic core losses of the CM inductor	[W]
P_{c}	Total magnetic core losses	[W]
$P_{\mathrm{cs,tot}}$	Total power consumption of the cooling system	[W]
$P_{\mathrm{L,cm}}$	Total losses of the CM inductor	[W]
$P_{\mathrm{L,dm}}$	Total losses of the DM inductor	[W]
$P_{\mathrm{R,damp}}$	Total resistive losses of the C-R parallel damping circuit	[W]
$P_{\mathrm{R,pcb}}$	Total resistive losses of the PCB traces	[W]
$P_{\mathrm{semi,cond,dc}}$	Conduction losses of the semiconductor devices in the DC–DC converter	[W]
$P_{\mathrm{semi,cond}}$	Conduction losses of the semiconductor devices	[W]
$P_{\mathrm{semi,max}}$	Maximum total semiconductor losses per heat sink	[W]
$P_{\mathrm{semi,sw,dc}}$	Total switching losses of the semiconductor devices in the DC–DC converter	[W]
$P_{\mathrm{semi,sw,off,dc}}$	Turn-off switching losses of the semiconductor devices in the DC–DC converter	[W]
$P_{\mathrm{semi,sw,off}}$	Turn-off switching losses of the semiconductor devices	[W]
$P_{\mathrm{semi,sw,on,dc}}$	Turn-on switching losses of the semiconductor devices in the DC–DC converter	[W]
$P_{\mathrm{semi,sw,on}}$	Turn-on switching losses of the semiconductor devices	[W]
$P_{\mathrm{semi,sw}}$	Total switching losses of the semiconductor devices	[W]
$P_{\mathrm{semi,tot,\sharp}}$	Total semiconductor losses per device	[W]
$P_{\mathrm{semi,tot,case,\sharp}}$	Total semiconductor loss per case	[W]

$P_{\text{semi,tot,unit}}$	Total semiconductor losses per heat sink unit	[W]
$P_{\text{semi,tot}}$	Total semiconductor losses	[W]
$P_{\text{w,cm}}$	Winding losses of the CM inductor	[W]
P_{w}	Total winding losses	[W]
$\Delta Q_{\text{C,HF}}$	High frequency charge of the DM capacitor	[C]
Q_{c}	Capacitive charge of diode	[C]
Q_{rf}	Second part of reverse recovery charge of the semiconductor devices	[C]
Q_{rs}	First part of reverse recovery charge of the semiconductor devices	[C]
R_{d}	Resistance of the damping resistor	[Ω]
R_{g}	Gate resistance	[Ω]
$R_{\text{in,d}}$	Resistance value of the EMI input filter's damping resistor	[Ω]
R_{LISN}	Resistance of the LISN	[Ω]
R_{on}	On-state resistance of the semiconductor devices	[Ω]
R_{pcb}	Resistance of the PCB traces	[Ω]
$R_{\text{th,a}}$	Thermal resistance between heat sink base plate and ambient	[K/W]
$R_{\text{th,A}}$	Thermal resistance between heat sink fin and ambient	[K/W]
$R_{\text{th,c}}$	Thermal resistance between the magnetic core hot-spot and the magnetic core surface	[K/W]
$R_{\text{th,ca}}$	Thermal resistance between the magnetic core surface and ambient	[K/W]
$R_{\text{th,c-hs}}$	Thermal resistance between semiconductor case and heat sink surface	[K/W]
$R_{\text{th,cp}}$	Thermal resistance between the magnetic core surface and the base plate	[K/W]
$R_{\text{th,d}}$	Thermal resistance of heat sink base plate	[K/W]
$R_{\text{th,FIN}}$	Thermal resistance of heat sink fin	[K/W]

$R_{\mathrm{th,hs,max}}$	Maximum averaged thermal resistance of the heat sink unit	[K/W]
$R_{\mathrm{th,hs}}$	Thermal resistance of the heat sink to ambient	[K/W]
$R_{\mathrm{th,j-c,\sharp}}$	Thermal resistance between junction and case	[K/W]
$R_{\mathrm{th,pa}}$	Thermal resistance between the base plate surface and ambient	[K/W]
$R_{\mathrm{th,wa}}$	Thermal resistance between the winding surface and ambient	[K/W]
$R_{\mathrm{th,wc}}$	Thermal resistance between the winding surface and the magnetic core surface	[K/W]
$R_{\mathrm{th,whs}}$	Thermal resistance between the winding hot-spot and the winding surface	[K/W]
S_{ac}	Apparent power of input / output side	[VA]
S_{out}	Nominal apparent output power	[VA]
$\mathrm{T}_{\sharp}$	Symbol for IGBTs	
T_{amb}	Ambient temperature	[K]
$T_{\mathrm{c,max}}$	Maximum temperature of the magnetic core	[K]
T_{c}	Temperature of the magnetic core	[K]
T_{channel}	Temperature of air inside the air-channel of the heat sink	[K]
$T_{\mathrm{cm,max}}$	Maximum allowed CM inductor temperature	[K]
T_{cm}	Temperature of the CM inductor	[K]
T_{cs}	Surface temperature of the magnetic core	[K]
$T_{\mathrm{hs,max}}$	Maximum heat sink temperature	[K]
T_{hs}	Surface temperature of the heat sink	[K]
$T_{\mathrm{j,max}}$	Maximum junction temperature	[K]
T_{j}	Junction temperature of semiconductor devices	[K]
T_{j0}	Reference junction temperature of semiconductor devices	[K]

T_{ps}	Surface temperature of the metal base plate	[K]
$T_{\mathrm{whs,max}}$	Maximum temperature of the winding hot-spot	[K]
T_{whs}	Temperature of the winding hot-spot	[K]
T_{ws}	Surface temperature of the winding	[K]
$\Delta V_{\mathrm{C,HF}}$	High frequency peak-to-peak voltage ripple of the DM capacitor	[V]
$\dot{V}_{\mathrm{air}}$	Volumetric flow-rate of air inside the air-channel of the heat sink	[m^3/s]
$\hat{V}_{\mathrm{ac}}$	Peak voltage of input / output side	[V]
V_{bt}	Battery voltage	[V]
V_{cap}	Total volume of the capacitor	[dm^3]
$V_{\mathrm{cs,tot}}$	Total volume of the cooling system	[dm^3]
V_{dc}	DC-link voltage	[V]
V_{DC}	Rated voltage of capacitor	[V]
V_{dc0}	Reference voltage for switching loss model	[V]
$V_{\mathrm{dm,max}}$	Maximum magnitude of the DM voltage in the frequency-domain	[V]
V_{f}	Forward voltage drop of the semiconductor device at zero current	[V]
$V_{\mathrm{ge,off}}$	Negative gate voltage	[V]
$V_{\mathrm{ge,on}}$	Positive gate voltage	[V]
$V_{\mathrm{in,pk}}$	Peak value of the input voltage fundamental	[V]
$V_{\mathrm{L,cm}}$	Total boxed volume of the CM inductor	[dm^3]
$V_{\mathrm{L,dm}}$	Total boxed volume of the DM inductor	[dm^3]
$V_{\mathrm{L,in,pk}}$	Reference voltage peak value of the inductor in the EMI input filter	[V]
$V_{\mathrm{L,min}}$	Minimum boxed volume of an inductor	[dm^3]
$V_{\mathrm{L,out,pk}}$	Reference voltage peak value of the inductor in the output filter	[V]
$V_{\mathrm{out,pk}}$	Peak value of the output voltage fundamental	[V]

$V_{(\mathrm{BR})\mathrm{CES}}$	Maximum collector-emitter voltage of IGBTs	[V]
V_{RRM}	Repetitive peak reverse voltage of diodes	[V]
a	Optimization factor of the damping component	
b	Width of the heat sink and the cooling fan	[m]
$b_{\mathrm{clearance}}$	Clearance length between semiconductor packages	[m]
b_{TO247}	Width of the semiconductor package	[m]
c	Length of the fins	[m]
c_{air}	Thermal capacitance of air	[J/K]
d	Thickness of the heat sink base plate	[m]
d_{23}	Duty ratio of IGBTs in DC–DC converter	
d_{w}	Diameter of wire	[m]
f_{d}	Design frequency of the EMI input filter	[Hz]
$f_{\mathrm{dc,sw}}$	Operating switching frequency of the DC part	[Hz]
f_{HF}	Switching frequency	[Hz]
$f_{\mathrm{in,3h}}$	Frequency of the third harmonic of the mains frequency	[Hz]
$f_{\mathrm{in,LF}}$	Fundamental input frequency	[Hz]
$f_{\mathrm{in,sw}}$	Switching frequency of the input rectifier	[Hz]
f_{LF}	Mains frequency	[Hz]
$f_{\mathrm{out,LF}}$	Fundamental output frequency	[Hz]
$f_{\mathrm{out,sw}}$	Switching frequency of the output inverter	[Hz]
f_{res}	Resonance frequency of second filter stage	[Hz]
f_{sw}	Switching frequency	[Hz]
h	Average heat transfer coefficient	$[\mathrm{W}/(\mathrm{m}^2 \cdot \mathrm{K})]$

$i_\sharp$	Instant conduction currents of power semiconductor	[A]
$i'_{\mathrm{c,T}}$	Derivative value of collector current	[A/s]
$i_{\mathrm{L,ac}}$	Temporal current of input / output inductor	[A]
$i_{\mathrm{sw,off},\sharp}$	Temporal turn-off switching current	[A]
$i_{\mathrm{sw,on},\sharp}$	Temporal turn-on switching current	[A]
k	Filling factor of magnetic components winding	
k_{Pc}	Correction factor of magnetic core losses	
l_{c}	Effective thermal distance of the magnetic core	[m]
l_{e}	Effective mean path length of the magnetic core	[m]
l_{eff}	Effective mean path length of the leakage magnetic field	[m]
l_{eg}	Effective air gap length between the magnetic core surface and the base plate surface	[m]
l_{pcb}	Total length of PCB traces	[m]
m	Rank of the high-frequency harmonic	
$m_{\mathrm{c},1}, m_{\mathrm{c},2}$	Triangular PWM carrier signals	
$m_{\mathrm{in,r/s/t}}$	Temporal modulation signal in the input rectifier	
$m_{\mathrm{out,u/v/w}}$	Temporal modulation signal in the output inverter	
n	Number of fins	
n_{stack}	Number of stacked cores	
$t_{\mathrm{c-hs}}$	Thickness of the thermal contact material	[m]
t_{pcb}	Thickness of the PCB traces	[m]
t_{s}	Turn-on delay time due to reverse recovery	[s]
v_{ac}	Temporal voltage of input / output side	[V]
$v_{\mathrm{in,r/s/t}}$	Temporal input phase voltage	[V]

$v_{\mathrm{in,sw,cm}}$	Temporal high-frequency CM voltage in the EMI input filter	[V]
$v_{\mathrm{in,sw,r/s/t}}$	Temporal switched voltage in the input rectifier	[V]
$v_{\mathrm{in,sw,dm,r/s/t}}$	Temporal switched DM voltage in the input rectifier	[V]
$v_{\mathrm{L,in,cm}}$	Temporal voltage across the CM inductor	[V]
v_{m}	Temporal average voltage of input / output side	[V]
$v_{\mathrm{out,sw,cm}}$	Temporal high-frequency CM voltage in the output filter	[V]
$v_{\mathrm{out,sw,u/v/w/n}}$	Temporal switched voltage in the output inverter	[V]
$v_{\mathrm{out,u/v/w/n}}$	Temporal output phase voltage	[V]
$v_{\mathrm{L,in,r/s/t}}$	Temporal voltage across the DM inductor in the EMI input filter	[V]
$v_{\mathrm{L,out,u/v/w}}$	Temporal voltage across the DM inductor in the output filter	[V]
w_{pcb}	Averaged width of the PCB traces	[m]

Abbreviations

3D	Three-Dimensional
3LTTC	Three-Level T-Type Converter
CAD	Computer Aided Design
CISPR	Comité International Spécial des Perturbations Radioélectriques (International Special Committee on Radio Interference)
CM	Common-Mode
CSPI	Cooling System Performance Index
DM	Differential-Mode
DSP	Digital Signal Processor
EMI	Electro Magnetic Interference
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FWD	Free Wheeling Diode
HF	High-Frequency
IGBT	Insulated Gate Bipolar Transistor
iGSE	Improved Generalized Steinmetz Equation
LF	Low-Frequency
LISN	Line Impedance Stabilization Network
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PCS	Power Conditioning System
PWM	Pulse Width Modulation
QP	Quasi-Peak
RB	Reverse-Blocking
SBD	Schottky Barrier Diode
SE	Steinmetz Equation
Si	Silicon
SiC	Silicon Carbide
UPS	Uninterruptible Power Supply
WBG	Wide Band Gap

Chapter 1

Introduction

"Remember that TIME is Money" is a well known phrase used by Benjamin Franklin in his book *Advice to a Young Tradesman, Written by an Old One* [1]. It has been the phrase for financial traders, but not for power electronics engineers who design and develop power converter systems for various applications. However, in an industrial company, the time usage of employees is the most valuable resource in the research and development process of the power converter system. The typical power converter development process in an industrial company consists of the production of several hardware prototypes, with an evaluation and design improvement procedure. For example, a first prototype is built for finding a problem to be improved for the second or final prototype. Overheating power semiconductors, inductors, or capacitors could be one such problem to be found and localized, also failing an EMI emission test is one of the major concerns when the converter is connected to the mains. In the worst case, not only a second but also a third prototype has to be built and evaluated once again when the second prototype didn't satisfy the required specification. The amount of hardware prototyping directly affects the consumption of hardware materials and "human power." As a result, the costs of the development process, in terms of *Time* and *Money*, are increased proportionally to the number of hardware prototypes built. In addition, the demand for higher performance of the converter system has kept increasing. Performance indices of a power electronics converter are proposed in [2] and summarized as follows:

- Power density [kW/dm^3],
- Power per unit weight [kW/kg],
- Relative costs [kW/$],
- Relative losses [%],
- Failure rate [1/h].

Power per unit weight, relative losses, and failure rate might be known as the power-to-weight ratio, efficiency, and reliability / life time, respectively. In order to satisfy the high demand for increasing the performance of power converter systems, a performance-oriented optimization of the systems is becoming increasingly important for application in the industrial production procedure.

The optimization of power converter systems is a multi-domain procedure [3], which considers thermal effects and limitations besides the electric and / or magnetic characteristics of the active and passive power components. Early implementations of power converter optimizations were limited to the optimization with respect to a single performance index, e.g. power density ρ or efficiency η [4, 5, 6]. Single-objective converter optimizations, however, often yield unsatisfying remaining converter characteristics, e.g., a converter optimized for high power density may generate high losses, due to increasing losses of the high power density magnetic components. Thus, the multi-objective optimization of a PFC rectifier based on the η–ρ Pareto front is proposed in [7]. This Pareto front identifies the highest efficiency for a given power density (and vice versa) and can be used as the basis for initial decisions concerning the converter design parameters. Details on the calculation of the η–ρ Pareto front and the extension to a third variable (e.g. cost) are presented in [8].

Examples of η–ρ Pareto optimizations of power converters include the realizations of an ultra-high efficiency DC–DC converter ($\eta = 99\%$ at $\rho = 2.3\,\mathrm{kW/dm^3}$) [9] and an ultra-high efficiency PFC rectifier ($\eta = 99.2\%$ at $\rho = 1.1\,\mathrm{kW/dm^3}$) [10]. Recent publications related to η–ρ Pareto optimizations further confirm that this approach can be advantageously used for designing power converters, e.g. for the design of a 50 kW bidirectional resonant converter in [11], and the selection of a suitable five-level inverter topology in [12].

1.1 Considered application and specification

Uninterruptible Power Supply (UPS) systems ensure uninterruptible operation of highly available equipment, for example IT equipment of a data center, independent from a mains failure. For critical loads which need low input voltage distortion, a back-to-back configuration, as shown in **Figure 1.1**, is often employed, since this configuration effectively suppresses mains voltage distortions; such UPS systems are called online or double-conversion systems [13].

The UPS system investigated in this thesis is an online UPS according to **Figure 1.1** with a rated power of 20 kVA. The rms input and output line-to-neutral voltages of the considered system are 230 V, the input and output frequencies are 50 Hz, and the DC-bus voltage is kept constant at $V_{\mathrm{dc}} = 720\,\mathrm{V}$. The rectifier and inverter stages of this UPS are designed for high efficiency, since, during normal mode of operation, both stages may be continuously operated up to nominal power.

1.2 Suitable topology for UPS system

Typical three-phase rectifier and inverter topologies include conventional two-level topologies and three-level neutral point clamped (NPC) topologies [14]. Three-phase two-level converters feature a low number of diodes (rectifier) or IGBTs (inverter) with a maximum blocking voltages of 1200 V in the considered system and generate low conduction losses [15]. Two-level converters, however, require a comparably large EMI filter due to the generation of high harmonic content [16]. Three-level NPC inverters and rectifiers cause less harmonic content and, thus, allow a reduced EMI filtering effort. These converters, however, require more diodes and / or switches (maximum break-down voltages are 600 V in the given system) and generate higher conduction losses than two-level converters, since each phase current is fed through two semiconductor devices, e.g. two IGBTs, with the sum of the voltage drops across two 600 V IGBTs being greater than the voltage drop across a single 1200 V IGBT [15]. T-type NPC converters, in comparison, allow three-level operation with reduced conduction losses, since only a single diode or IGBT (again rated for 1200 V) conducts the phase current to the positive or negative bus bar of the DC-link [15]. Therefore, the T-

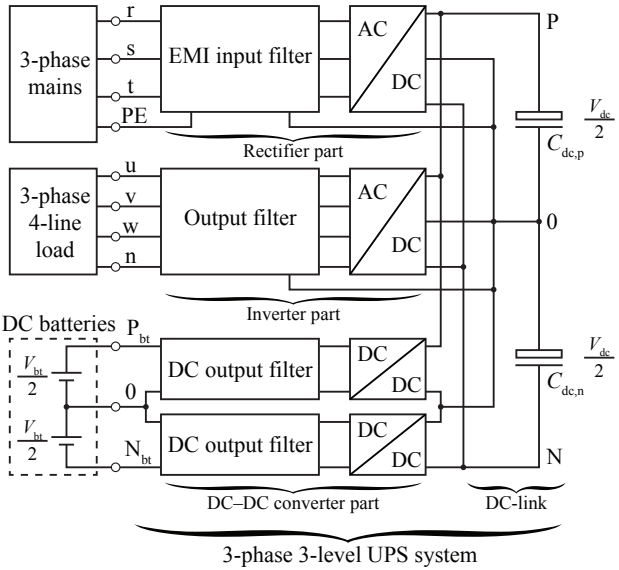


Figure 1.1: Proposed configuration of the three-phase UPS system showing EMI input filter, mains side rectifier, load side inverter, output filter, DC output filters and DC–DC converters including backup batteries.

type NPC inverter and rectifier topologies are very attractive regarding the investigated UPS system in order to achieve low conduction losses and reduced EMI filtering effort.

The T-type NPC converters require one bi-directional switch per phase, cf. **Figure 1.2**. Bi-directional switches are typically realized with a common-emitter series connection of two IGBT / Free Wheeling Diode (FWD) modules [15,17]. As a consequence, two series connected semiconductor components, a diode and an IGBT, conduct the current through the bi-directional switch. In this context, reverse blocking IGBTs (RB-IGBTs) can be advantageously used to reduce the conduction losses of T-type rectifiers and inverters [18,19,20].

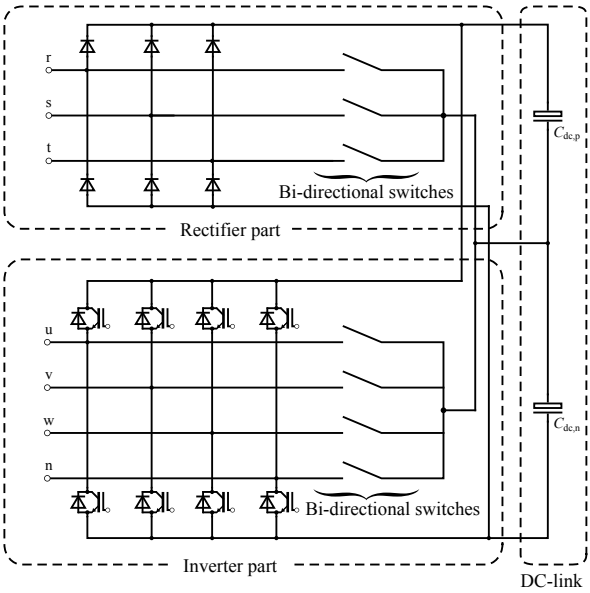


Figure 1.2: Schematic drawing of the power circuits of the mains side rectifier and the load side inverter; both, rectifier and inverter, employ three-level T-type converter (3LTTC) topologies.

1.3 Objectives and new contributions of this work

This thesis details a comprehensive comparison of the semiconductor losses of the rectifier and inverter stage of a three-phase three-level UPS system for different realizations of the bi-directional switches, which includes realizations with RB-IGBTs and different types of conventional IGBT / FWD modules. The thesis further investigates the improvements achieved with 1200 V SiC Schottky Barrier Diodes (SBDs) (instead of 1200 V Si rectifier diodes and FWDs) and 600 V SiC SBDs (instead of 600 V Si FWDs used in the bi-directional switches). A thermal model of the semiconductor packages and the cooling system are taken into account for analysis of the electro-thermal coupled loss components of the power semiconductors. A detailed thermal model for determining the hot-spot temperature of the differential mode inductor

under the condition of natural convection cooling is proposed and experimentally verified. The thesis also details the implementation of an automatic EMI input filter design procedure based on the Design Space approach.

As a result, a fully automated system-level optimization procedure for three-phase three-level T-type UPS systems is proposed. The influence of the different magnetic materials on the system-level performance is investigated and the most suitable magnetic material is selected for hardware realization. The complete system is optimized for both high efficiency and high power density with the selected magnetic material. In a next step, the optimized UPS system is built and the total system loss models are experimentally verified and compared with the measurement results. In addition, the EMI emission level is tested in order to verify the EMI input filter design model.

The new contributions of this thesis are:

- Analysis and modeling of the electro-thermal coupled loss components of the three-phase three-level T-type UPS system.
- Investigation of the most suitable semiconductor configuration for realizing the three-level T-type topology which gives minimum total semiconductor losses.
- Investigation and experimental verification of the thermal modeling for the magnetic components under natural convection cooling condition in order to determine the hot-spot temperature inside the winding or the magnetic core.
- Implementation of an automatic design procedure of the EMI input filter, the output filter and the DC output filter.
- Implementation of an automatic system-level optimization and design procedure.
- Investigation of the influence of different magnetic materials on the system-level performance.
- Hardware realization of the optimized UPS system, experimental verification and comparison of total system loss models, and EMI input filter design model.

1.4 Outline of this thesis

In the following chapters, the automated system-level optimization procedure of the three-phase three-level T-type UPS system as specified in the previous section is presented.

In **Chapter 2**, the losses, the volumes, and the thermal modeling of the active components are presented. A comparison of the semiconductor losses of the rectifier and inverter of a three-phase three-level T-type UPS system for different realizations of the bi-directional switches is given, which includes realizations with RB-IGBTs and different types of conventional IGBT / FWD modules. The chapter further investigates the improvements achieved with 1200 V SiC Schottky Barrier Diodes (SBDs) (instead of 1200 V Si rectifier diodes and FWDs) and 600 V SiC SBDs (instead of 600 V Si FWDs used in the bi-directional switches). The optimization procedure for an application specific heat sink geometry is also discussed and an experimental verification of the thermal model of the heat sink is given. In addition, the power demands of the auxiliary components, such as the gate drivers, digital controllers and current / voltage sensors, are briefly discussed.

In **Chapter 3**, the losses, the volumes, and the thermal modeling of the passive components are presented. The differential mode (DM) inductors, the common mode (CM) inductors, the capacitors, and the damping resistors are considered. Especially, the thermal modeling of the DM inductors under natural convection cooling is presented in detail. The chapter furthermore investigates the component-level optimization for the DM and the CM inductors in order to minimize both the losses and volumes. Furthermore, the losses in the damping resistors are modeled and considered as part of the passive components losses. Since the losses in the capacitors are negligible, only volume models are considered for the capacitors.

In **Chapter 4**, the implementation of an automatic filter design procedure for the two-stage EMI input filter, the two-stage output filter and the DC output filter are presented. The advantages of employing multi-stage LC filters are discussed and the Design Space approach for the considered filter structures is summarized. The EMI noise emission level estimation is performed based on simplified equivalent circuits for both the DM and CM noise current paths. The EMI filter attenuation is also calculated for the DM and CM paths separately.

In **Chapter 5**, a system-level optimization procedure is imple-

mented and a multi-objective optimization is performed in order to determine the Pareto front of the considered UPS system in the Performance Space. The electric input / output specifications and possible design variables for the investigated UPS system are also given. The chapter furthermore investigates the influence of different magnetic materials on the system-level performance, such as the efficiency and the power density, and selects the most suitable magnetic material for the hardware realization. Further investigation is performed for determining the optimal design parameters for high efficiency and high power density. As a result, a 16 kHz switching frequency and a 20 % relative current ripple with an amorphous magnetic material is selected for achieving 96.2 % efficiency at 2.3 kVA/dm^3 power density.

Since the power density is simply calculated from the boxed volume of the components, 3-Dimensional Computer Aided Design (3D CAD) is required for a virtual prototyping in order to determine the power density of a practical hardware realization. The virtual prototyping is presented in **Chapter 6** and a power density of 0.9 kVA/dm^3 is determined. This power density is achieved with a practical hardware realization. Furthermore, the experimental verification and comparison of the total efficiencies and losses of the UPS system are presented. The measurement results show 96.5 % efficiency at nominal output power which gives less than 5 % relative error of the total loss calculation.

As a conclusion, the results of this thesis are summarized and an outlook on future work is given in **Chapter 7**.

1.5 List of publications

Publications directly related to the Ph.D. project:

[I] H. Uemura, F. Krismer, Y. Okuma and J. W. Kolar, "η-ρ Pareto Optimization of 3-Phase 3-Level T-Type AC–DC–AC Converter Comprising Si and SiC Hybrid Power Stage," in *Proceedings of the International Power Electronics Conference (IPEC–ECCE Asia)*, Hiroshima, Japan, May 18-21, 2014.

[II] R. Burkart, H. Uemura and J. W. Kolar, "Optimal Inductor Design for 3-Phase Voltage-Source PWM Converters Considering Different Magnetic Materials and a Wide Switching Frequency Range," in *Proceedings of the International Power Electronics*

Conference (IPEC–ECCE Asia), Hiroshima, Japan, May 18-21, 2014.

[III] H. Uemura, F. Krismer and J. W. Kolar, "Comparative Evaluation of T-Type Topologies Comprising Standard and Reverse-Blocking IGBTs," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Denver, Colorado, USA, September 15-19, 2013.

[IV] J. Muehlethaler, H. Uemura and J. W. Kolar, "Optimal Design of EMI Filters for Single-Phase Boost PFC Circuits," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Montreal, Canada, October 25-28, 2012.

Chapter 2

Modeling losses and volumes of active components

This chapter describes the modeling of the losses and volume of active components, such as power semiconductors, the cooling system comprised of the heat sink and cooling fans, gate drivers, and digital controllers. As power semiconductors typically account for a high proportion of the losses but make a low contribution to the volume, only a loss model is considered for the power semiconductors. On the other hand, the heat sink accounts for a high proportion of the volumes and it is coupled with the semiconductor losses. The calculation of the semiconductor losses based on an electro-thermally coupled model and a model for the optimization of the heat sink will be discussed in this chapter. The power demands of the auxiliary circuits, such as gate drivers and digital controllers, were typically neglected in previous works [21, 11, 8, 2, 22, 5, 6, 10, 9] due to the comparably higher semiconductor losses. However, by applying Wide Band Gap (WBG) semiconductor device technologies to reduce semiconductor losses and optimizing other power component losses, the losses of the auxiliary circuits are no longer negligible.

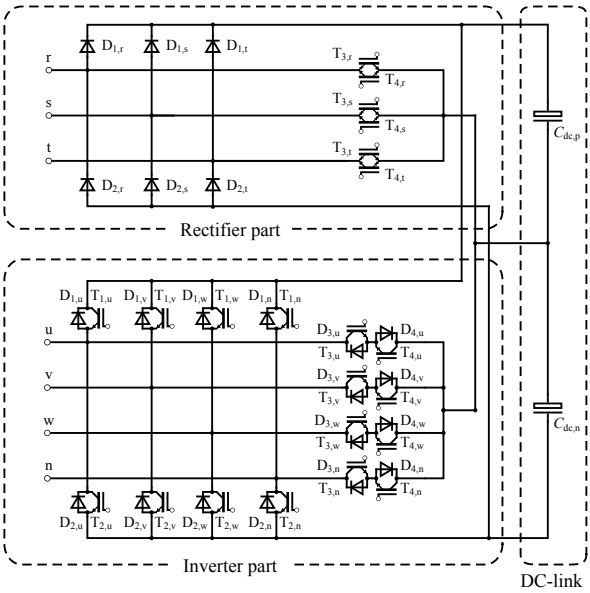


Figure 2.1: Schematic drawing of the power circuits of the mains side rectifier and the load side inverter. Both, the rectifier and inverter employ 3LTTC topologies.

2.1 Power semiconductors

This section details the modeling and comparison of semiconductor losses in the rectifier and inverter of the three-phase three-level UPS system depicted in **Figure 2.1** for different realizations of the bi-directional switches, which includes realizations with RB-IGBTs and different types of conventional IGBT / Diode modules. It investigates further improvements from the use of 1200 V SiC Schottky Barrier Diodes (SBDs) (instead of 1200 V Si diodes) and 600 V SiC SBDs (instead of the 600 V Si diodes used in the bi-directional switches).

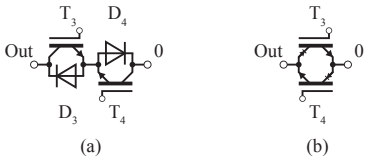


Figure 2.2: Possible realizations of a bi-directional switch: (a) realization with conventional IGBTs and diodes, (b) realization with RB-IGBTs.

2.1.1 Bi-directional power switch

Switch realization

Figure 2.2 shows two possible realizations of the bi-directional switches: with conventional IGBTs and diodes, or with RB-IGBTs. Further realizations of bi-directional switches, e.g. the realizations given in [14,17], are expected to have higher or similar conduction losses than the realization in **Figure 2.2(a)**, and are, therefore, not considered in this comparison.

Internal structure of the monolithically integrated RB-IGBT

The internal structures of a conventional IGBT and RB-IGBT and their respective depletion layers under reverse voltage conditions are shown in **Figure 2.3**. When a reverse voltage is applied to a conventional IGBT, the depletion layer extends from the backside anode (collector) towards the surface cathode (emitter). The depletion layer also extends to the diced side walls and causes high local electric fields, which are proportional to the reverse voltage. The semiconductor dicing process, however, unavoidably generates numerous crystal defects and mechanical imperfections in the diced side walls. The high local electric fields generate free carriers at these crystal defects, causing what is known as a leakage current fountain, which may irreversibly damage the IGBT [20].

The concept of an RB-IGBT and the realization of its internal structure were first introduced in 2001 [18, 19]. Deep diffusion of a p^+-side wall protection at the diced side wall surface [cf. **Figure 2.3(b)**] prevents the depletion layer from extending to the diced surface area of the IGBT under reverse voltage conditions. As a result, a huge reduction in the reverse leakage current under reverse voltage conditions is achieved.

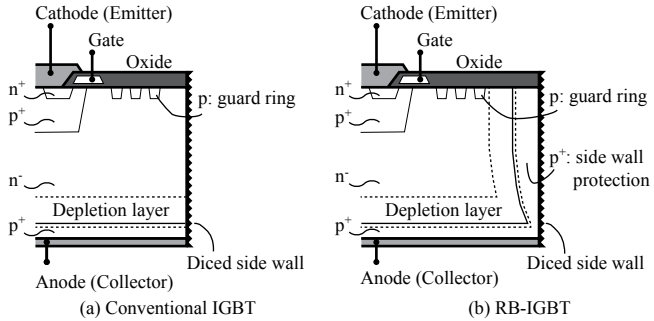


Figure 2.3: (a) Internal structure of the conventional IGBT; (b) internal structure of the RB-IGBT for reverse voltage conditions. The reverse voltage forms the depletion layers shown in (a) and (b).

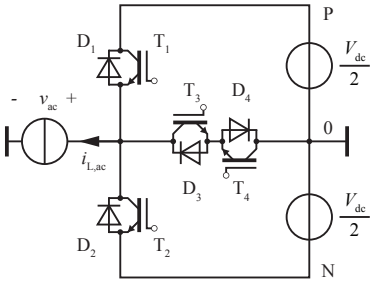


Figure 2.4: Single phase-leg of the 3LTTC converter.

Since the RB-IGBT and the conventional IGBT are only different with respect to their edge structures, the same or similar conduction and switching losses can be expected for both types of IGBTs if operated in the forward direction. The RB-IGBT, however, shows the same reverse recovery behavior as a PiN diode if operated with reverse voltage, which causes the switching losses to increase and needs to be considered in the loss model detailed in the next section.

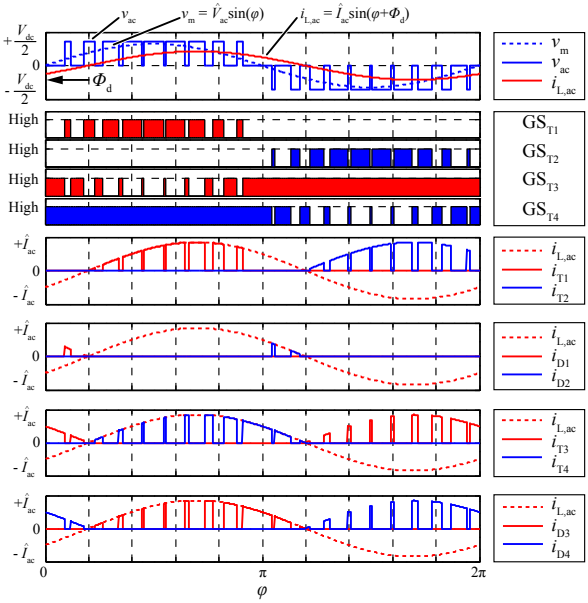


Figure 2.5: General waveforms of input / output voltage / current and corresponding gate signals $GS_\sharp$ and conduction currents $i_\sharp$ of each devices for dedicated phase shift Φ_d, voltage fundamental amplitude $\hat{V}_{ac}$, and current fundamental amplitude $\hat{I}_{ac}$.

2.1.2 Analytical loss calculation model of T-type converters

Voltage and current waveforms at AC input / output side

A single phase-leg of the 3LTTC converter is shown in **Figure 2.4**. It is implemented using four IGBTs (T_1, T_2, T_3 and T_4) and four diodes (D_1, D_2, D_3 and D_4). Here, bi-directional switches are realized with conventional IGBTs (T_3 and T_4) and diodes (D_3 and D_4). **Figure 2.5** illustrates general input / output voltage and current waveforms of a single phase-leg of the 3LTTC converter at the AC input / output side (e.g. mains input side or load output side). The gate signals and conduction currents for each device are also shown in Figure 2.5. The multi-carrier Pulse Width Modulation (PWM) scheme detailed in [23,24] that is considered in this thesis is used in this model. In Figure 2.5, v_{ac}, re-

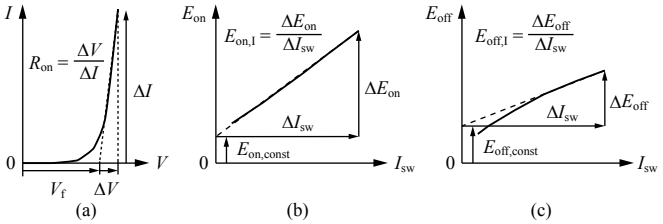


Figure 2.6: (a) General on-state characteristics of IGBTs and diodes used to determine the parameters V_{f} and R_{on} of the conduction loss model. (b), (c) A general illustration of how the parameters $E_{\mathrm{on,const}}$, $E_{\mathrm{on,I}}$, $E_{\mathrm{off,const}}$, and $E_{\mathrm{off,I}}$ of the switching loss model are extracted from the (b) turn-on and (c) turn off loss characteristics.

spectively, $i_{\mathrm{L,ac}}$, are the instantaneous input / output voltage and the instantaneous current of a single phase-leg on the AC side; v_{m} is the temporal average value of v_{ac}, which is the same as the fundamental input voltage at the mains side or the output voltage at the load side. $\mathrm{GS_{T1}}$ is the gate signal of $\mathrm{T_1}$ and i_{T1} is the instantaneous current of $\mathrm{T_1}$. The same notation is used for the other devices, $\mathrm{T_2}$, $\mathrm{T_3}$, $\mathrm{T_4}$, $\mathrm{D_1}$, $\mathrm{D_2}$, $\mathrm{D_3}$ and $\mathrm{D_4}$. Note that the high frequency current ripples are neglected, in order to simplify the loss models. $\varphi = \omega t$ denotes the phase of the fundamental voltage, Φ_{d} is the phase displacement between the fundamental components of the current and voltage, $\hat{V}_{\mathrm{ac}}$ is the amplitude of the phase voltage fundamental, and $\hat{I}_{\mathrm{ac}}$ is the amplitude of the phase current fundamental. Thus, $\Phi_{\mathrm{d}} = 0\,^\circ$ denotes the inverter mode of operation with unity power factor and $\Phi_{\mathrm{d}} = 180\,^\circ$ denotes the rectifier mode of operation with unity power factor. The voltage and current amplitudes, $\hat{V}_{\mathrm{ac}}$ and $\hat{I}_{\mathrm{ac}}$, are defined from the modulation index M and the input / output apparent power S_{ac} according to

$$\hat{V}_{\mathrm{ac}} = M\frac{V_{\mathrm{dc}}}{2}, \tag{2.1}$$

$$\hat{I}_{\mathrm{ac}} = \frac{2}{3}\cdot\frac{S_{\mathrm{ac}}}{\hat{V}_{\mathrm{ac}}}. \tag{2.2}$$

Conduction loss model

Figure 2.6(a) shows the general on-state characteristics of the IGBTs and diodes. Linearization of the characteristic, obtained at a given

junction temperature T_j, yields the loss model parameters $V_\mathrm{f}(T_\mathrm{j})$ and $R_\mathrm{on}(T_\mathrm{j})$. The corresponding losses are calculated with the rms and the average currents through the device according to

$$\begin{aligned} P_\mathrm{semi,cond} &= R_\mathrm{on}(T_\mathrm{j})\, I^2_\mathrm{rms}(M, \hat{I}_\mathrm{ac}, \Phi_\mathrm{d}) + \\ &\quad V_\mathrm{f}(T_\mathrm{j})\, I_\mathrm{avg}(M, \hat{I}_\mathrm{ac}, \Phi_\mathrm{d}). \end{aligned} \tag{2.3}$$

$R_\mathrm{on}(T_\mathrm{j})$ and $V_\mathrm{f}(T_\mathrm{j})$ denote the temperature dependent on-state resistance and forward voltage drop values of the semiconductor. The temperature dependency is considered according to [25]:

$$R_\mathrm{on}(T_\mathrm{j}) = R_\mathrm{on}(T_\mathrm{j0}) \left(\frac{T_\mathrm{j}}{T_\mathrm{j0}}\right)^{k_{\mathrm{R_{on}}}}, \tag{2.4}$$

$$V_\mathrm{f}(T_\mathrm{j}) = V_\mathrm{f}(T_\mathrm{j0}) \left(\frac{T_\mathrm{j}}{T_\mathrm{j0}}\right)^{k_{\mathrm{V_f}}}. \tag{2.5}$$

Here, T_j0 is the reference junction temperature in Kelvin, $R_\mathrm{on}(T_\mathrm{j0})$ and $V_\mathrm{f}(T_\mathrm{j0})$ are the on-state resistance and forward voltage drop at the reference junction temperature. The temperature coefficients $k_{\mathrm{R_{on}}}$ and $k_{\mathrm{V_f}}$ of all considered devices, determined with data sheet values and least mean square approximation, are listed in **Table 2.4**.

The analytical expressions for the average and rms currents through all devices are derived according to [23]. This is done by neglecting the high frequency current ripple and only considering the fundamental component of the input / output current. The currents through the IGBTs with a suggested break-down voltage of 1200 V, i.e., the two IGBTs $\mathrm{T_1}$ and $\mathrm{T_2}$ in **Figure 2.4**, are

$$I_\mathrm{rms,T12} = \hat{I}_\mathrm{ac} \left[\cos\left(\frac{\Phi_\mathrm{d}}{2}\right)\right]^2 \sqrt{\frac{2M}{3\pi}}, \tag{2.6}$$

$$\begin{aligned} I_\mathrm{avg,T12} &= \frac{\hat{I}_\mathrm{ac} M\,(\pi - \Phi_\mathrm{d})\cos(\Phi_\mathrm{d})}{4\pi} + \\ &\quad \frac{\sin(\Phi_\mathrm{d})}{4\pi}; \end{aligned} \tag{2.7}$$

the currents through $\mathrm{D_1}$ and $\mathrm{D_2}$ are

$$I_\mathrm{rms,D12} = \hat{I}_\mathrm{ac} \left[\sin\left(\frac{\Phi_\mathrm{d}}{2}\right)\right]^2 \sqrt{\frac{2M}{3\pi}}, \tag{2.8}$$

$$I_\mathrm{avg,D12} = \frac{\hat{I}_\mathrm{ac} M\,[\sin(\Phi_\mathrm{d}) - \Phi_\mathrm{d}\cos(\Phi_\mathrm{d})]}{4\pi}; \tag{2.9}$$

and the currents in each IGBT and diode of the bi-directional switch, i.e., T_3, T_4, D_3 and D_4, are

$$\begin{aligned} I_{\mathrm{rms,T34}} &= I_{\mathrm{rms,D34}} \\ &= \hat{I}_{\mathrm{ac}}\sqrt{\frac{3\pi - 2M\left[3+\cos\left(2\Phi_{\mathrm{d}}\right)\right]}{12\pi}}, \qquad (2.10) \\ I_{\mathrm{avg,T34}} &= I_{\mathrm{avg,D34}} \\ &= \frac{2\hat{I}_{\mathrm{ac}} + \hat{I}_{\mathrm{ac}} M\left(\Phi_{\mathrm{d}} - \frac{\pi}{2}\right)\cos\left(\Phi_{\mathrm{d}}\right)}{2\pi} + \\ &\quad \frac{(-1)\hat{I}_{\mathrm{ac}} M \sin\left(\Phi_{\mathrm{d}}\right)}{2\pi}. \qquad (2.11) \end{aligned}$$

These equations are valid for both the inverter and rectifier modes of operation ($0\,^\circ \leq \Phi_{\mathrm{d}} \leq 180\,^\circ$).

Switching loss model

The switching states of a single leg of the 3LTTC, except for transient states during dead time intervals, are listed in **Table 2.1**. The current commutation paths related to the switching states and the input / output current conditions are shown in **Figure 2.7**. **Figure 2.8** illustrates the general input / output voltage / current waveforms, and the corresponding switching current for each device. **Table 2.2** summarizes the expressions for the switching loss energies that result for different state transitions.

Figure 2.9 serves as a basis for explaining the switching operations that are found in the given 3LTTC converter. It depicts the considered waveform of $v_{\mathrm{ac}}(t)$ and two switching operations for the inverter mode of operation in **Figure 2.9(a)**, at $t = t_{\mathrm{a}}$ ($\mathrm{S}_{1001} \rightarrow \mathrm{S}_{0011}$) and $t = t_{\mathrm{b}}$ ($\mathrm{S}_{0011} \rightarrow \mathrm{S}_{1001}$), assuming a positive and approximately constant input / output current $i_{\mathrm{L,ac}}$. The states involved in both depicted switching operations are, thus, S_{1001} and S_{0011} and, according to **Table 2.1**, the gate signals of the switches T_1 and T_3 need to be changed. The switch T_3, however, is operated with reverse voltage and, for $v_{\mathrm{ac}}(t) = 0$ and $i_{\mathrm{ac}}(t) > 0$, T_4 and D_3 conduct the input / output current, cf. **Figure 2.7(b)**.

Figure 2.9(b) and **Figure 2.9(c)** depict the collector-to-emitter voltage (blue) and collector current (red) waveforms measured at $t = t_{\mathrm{a}}$ for T_1, and the forward voltage (blue) and current (red) waveforms for

Table 2.1: Switching states.

	Switching states		
	S_{1001}	S_{0011}	S_{0110}
T_1:	**on**	off	off
T_2:	off	off	**on**
T_3:	off	**on**	**on**
T_4:	**on**	**on**	off
v_{ac}:	$+V_{dc}/2$	0	$-V_{dc}/2$

Table 2.2: Switching loss energies.

Input / output current condition	Switching transitions	
	$S_{0011} \rightarrow S_{1001}$	$S_{1001} \rightarrow S_{0011}$
$i_{ac} > 0$	$E_{on,T12} + E_{off,D34}$	$E_{off,T12} + E_{on,D34}$
$i_{ac} < 0$	$E_{off,T34} + E_{on,D12}$	$E_{on,T34} + E_{off,D12}$

Input / output current condition	Switching transitions	
	$S_{0110} \rightarrow S_{0011}$	$S_{0011} \rightarrow S_{0110}$
$i_{ac} > 0$	$E_{on,T34} + E_{off,D12}$	$E_{off,T34} + E_{on,D12}$
$i_{ac} < 0$	$E_{off,T12} + E_{on,D34}$	$E_{on,T12} + E_{off,D34}$

D_3, which are used to determine the switching losses. T_1 effectively turns off at $t = t_{a1}$ [Figure 2.9(b)]; the clearly visible tail current makes a large contribution to the total turn-off losses $E_{off,T12}$,

$$E_{off,T12} = \int_{ta1}^{ta2} i_{c,T12}(t) \cdot v_{ce,T12}(t)\ \mathrm{d}t. \tag{2.12}$$

The turn-on losses of D_3, **Figure 2.9(c)**, are negligible.

Figure 2.9(d) and (e) show the collector-to-emitter voltages (blue) and collector currents (red) of T_1, and the forward voltages (blue) and currents (red) of D_3 at $t = t_b$. The switch T_1 turns on at $t = t_{b1}$, which causes the forward current of D_3 to fall. The forward current of D_3 is zero at $t = t_{b2}$, and, subsequently, becomes negative due to reverse recovery effects. At $t = t_{b3}$ the forward current reaches the maximum reverse recovery current I_{rrm}. **Figure 2.9(e)**, thus, shows the reverse

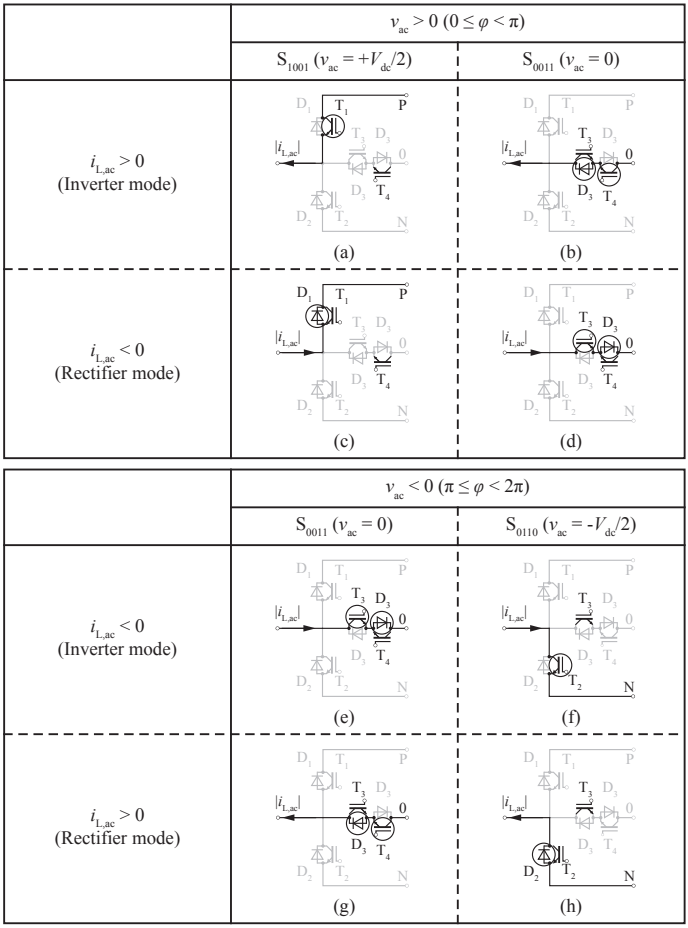


Figure 2.7: Bridge leg conduction states for Inverter and Rectifier operations. The circled devices conduct current.

recovery behavior of D_3, i.e., the internal diode on the collector side of RB-IGBT FGW85N60RB. The reverse recovery charge obtained from this figure, $Q_{rs} + Q_{rf} \approx 6.5\,\mu C$, causes reverse recovery losses of D_3 during $t_{b2} < t < t_{b5}$. Moreover, the reverse recovery behavior of D_3 causes a high temporary collector current in T_1, which increases the turn-on losses of T_1, as can be seen in Figure 2.9(d). The turn-on losses

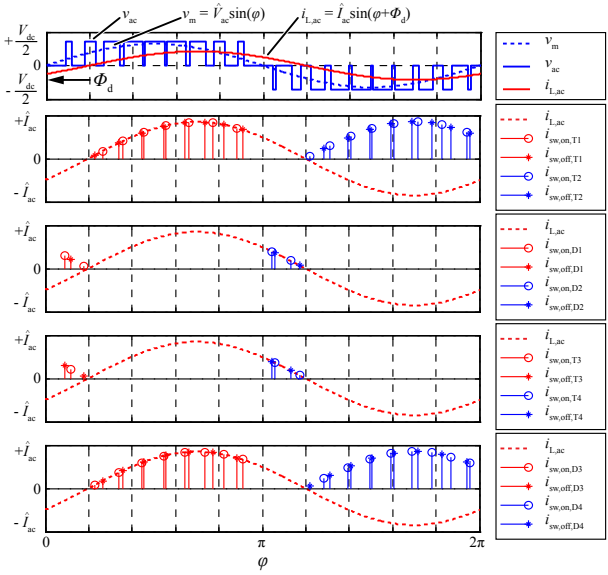


Figure 2.8: General waveforms of input / output voltage / current and the corresponding switching currents (turn-on: $i_{\mathrm{sw,on,\sharp}}$, turn-off: $i_{\mathrm{sw,off,\sharp}}$) of each device for dedicated phase shift Φ_d, voltage fundamental amplitude $\hat{V}_\mathrm{ac}$, and current fundamental amplitude $\hat{I}_\mathrm{ac}$.

$E_{\mathrm{on,T12}}$ and the reverse recovery losses $E_{\mathrm{off,D34}}$ are evaluated using

$$E_{\mathrm{on,T12}} = \int_{t\mathrm{b1}}^{t\mathrm{b4}} i_{\mathrm{c,T12}}(t) \cdot v_{\mathrm{ce,T12}}(t)\ \mathrm{d}t, \tag{2.13}$$

$$E_{\mathrm{off,D34}} = \int_{t\mathrm{b2}}^{t\mathrm{b5}} i_{\mathrm{f,D34}}(t) \cdot v_{\mathrm{f,D34}}(t)\ \mathrm{d}t. \tag{2.14}$$

The turn-off and turn-on losses for each IGBT and diode are calcu-

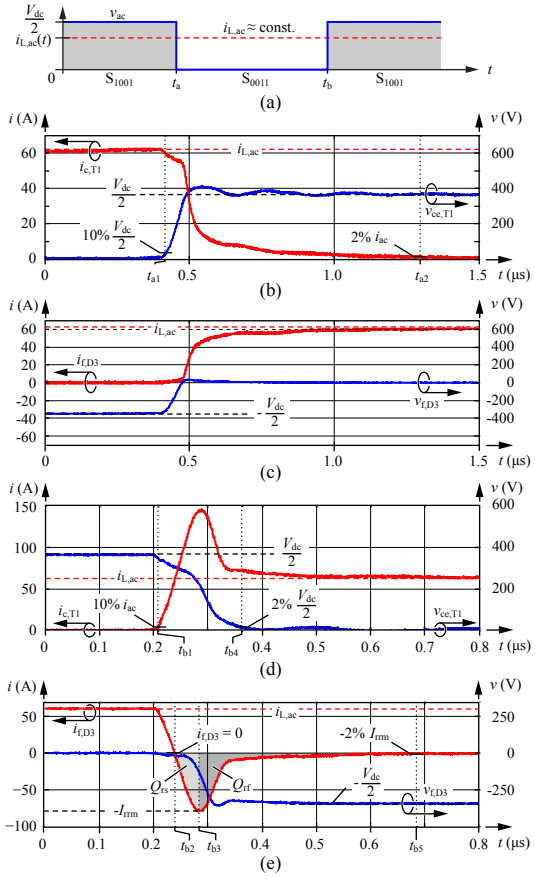


Figure 2.9: Transient collector-to-emitter voltages and collector currents during switching, obtained for $v_{\mathrm{ac}}(t) \geq 0$ and $i_{\mathrm{L,ac}}(t) > 0$ (inverter mode of operation): (a) simplified illustration of the considered input / output voltage and current waveforms showing the considered switching instants t_{a} and t_{b}; (b) and (c) waveforms measured for (b) T_1 and (c) D_3 during turn-off of T_1 at $t = t_{\mathrm{a}}$; (d) and (e) waveforms measured for (d) T_1 and (e) D_3 during turn-on of T_1 at $t = t_{\mathrm{b}}$; blue curves: collector-to-emitter voltages and forward voltages of diodes, red curves: collector currents and forward currents of diodes. Selected operating point: $V_{\mathrm{dc}} = 720\,\mathrm{V}$, $i_{\mathrm{L,ac}} = 60\,\mathrm{A} \approx$ constant. Employed semiconductor switches: T_1 and T_2: FGW40N120HD, D_3 and D_4: FGW85N60RB.

lated according to [15]:

$$\begin{aligned} P_{\text{semi,sw,off}} &= f_{\text{sw}} \Big[E_{\text{off,I}} \left(V_{\text{dc}}, T_{\text{j}} \right) I_{\text{sw,avg}} \left(\hat{I}_{\text{ac}}, \Phi_{\text{d}} \right) + \\ &\quad E_{\text{off,const}} \left(V_{\text{dc}}, T_{\text{j}} \right) D_{\text{d,sw}} \left(\Phi_{\text{d}} \right) \Big], \qquad (2.15) \\ P_{\text{semi,sw,on}} &= f_{\text{sw}} \Big[E_{\text{on,I}} \left(V_{\text{dc}}, T_{\text{j}} \right) I_{\text{sw,avg}} \left(\hat{I}_{\text{ac}}, \Phi_{\text{d}} \right) + \\ &\quad E_{\text{on,const}} \left(V_{\text{dc}}, T_{\text{j}} \right) D_{\text{d,sw}} \left(\Phi_{\text{d}} \right) \Big], \qquad (2.16) \\ P_{\text{semi,sw}} &= P_{\text{semi,sw,off}} + P_{\text{semi,sw,on}}. \qquad (2.17) \end{aligned}$$

The turn-on losses of the diodes are neglected in this thesis. $I_{\text{sw,avg}}$ denotes the averaged switching current over a single fundamental period, D_{sw} is the normalized period the device acts as a switch, and f_{sw} is the switching frequency. Analytical expressions for the average switching current are given in [26] and summarized below:

$$\begin{aligned} I_{\text{sw,avg,T12}} &= \hat{I}_{\text{ac}} \left[\frac{1 + \cos\left(\Phi_{\text{d}} \right)}{2\pi} \right], \qquad (2.18) \\ D_{\text{sw,T12}} &= \frac{\pi - \Phi_{\text{d}}}{2\pi}, \qquad (2.19) \\ I_{\text{sw,avg,T34}} &= \hat{I}_{\text{ac}} \left\{ \frac{\left[\sin\left(\frac{\Phi_{\text{d}}}{2} \right) \right]^2}{\pi} \right\}, \qquad (2.20) \\ D_{\text{sw,T34}} &= \frac{\Phi_{\text{d}}}{2\pi}, \qquad (2.21) \\ I_{\text{sw,avg,D12}} &= I_{\text{sw,avg,T34}}, \qquad (2.22) \\ D_{\text{sw,D12}} &= D_{\text{sw,T34}}, \qquad (2.23) \\ I_{\text{sw,avg,D34}} &= I_{\text{sw,avg,T12}}, \qquad (2.24) \\ D_{\text{sw,D34}} &= D_{\text{sw,T12}}. \qquad (2.25) \end{aligned}$$

$I_{\text{sw,avg,T34}}$ is the averaged switching current of T_3 and T_4 when the bi-directional switches are operated as IGBTs (e.g. switching in rectifier mode of operation) and $I_{\text{sw,avg,D34}}$ is the averaged switching current of D_3 and D_4 when the bi-directional switches are operated as diodes (e.g. switching in inverter mode of operation). The same notation is used for $D_{\text{sw,T34}}$ and $D_{\text{sw,D34}}$. These equations are valid for both the inverter and rectifier modes of operation ($0\,^\circ \leq \Phi_{\text{d}} \leq 180\,^\circ$). The six coefficients needed to calculate the switching losses, $E_{\text{off,I}}$, $E_{\text{off,const}}$, are determined for both IGBTs and diodes, and $E_{\text{on,I}}$, $E_{\text{on,const}}$, are determined for the IGBTs as shown in **Figure 2.6(b) and (c)** from

measurement results. The impact of the DC-bus voltage, V_{dc}, and the junction temperature, T_{j}, is considered according to [25]:

$$E_{\mathrm{off,I}}\left(V_{\mathrm{dc}}, T_{\mathrm{j}}\right) = E_{\mathrm{off,I}}\left(V_{\mathrm{dc0}}, T_{\mathrm{j0}}\right)\left(\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc0}}}\right)\left(\frac{T_{\mathrm{j}}}{T_{\mathrm{j0}}}\right)^{k_{\mathrm{E_{off}}}}, \quad (2.26)$$

$$E_{\mathrm{off,const}}\left(V_{\mathrm{dc}}, T_{\mathrm{j}}\right) = E_{\mathrm{off,const}}\left(V_{\mathrm{dc0}}, T_{\mathrm{j0}}\right)\left(\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc0}}}\right)\left(\frac{T_{\mathrm{j}}}{T_{\mathrm{j0}}}\right)^{k_{\mathrm{E_{off}}}}, \quad (2.27)$$

$$E_{\mathrm{on,I}}\left(V_{\mathrm{dc}}, T_{\mathrm{j}}\right) = E_{\mathrm{on,I}}\left(V_{\mathrm{dc0}}, T_{\mathrm{j0}}\right)\left(\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc0}}}\right)\left(\frac{T_{\mathrm{j}}}{T_{\mathrm{j0}}}\right)^{k_{\mathrm{E_{on}}}}, \quad (2.28)$$

$$E_{\mathrm{on,const}}\left(V_{\mathrm{dc}}, T_{\mathrm{j}}\right) = E_{\mathrm{on,const}}\left(V_{\mathrm{dc0}}, T_{\mathrm{j0}}\right)\left(\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc0}}}\right)\left(\frac{T_{\mathrm{j}}}{T_{\mathrm{j0}}}\right)^{k_{\mathrm{E_{on}}}}, \quad (2.29)$$

Here, $V_{\mathrm{dc0}} = 720\,\mathrm{V}$ is the voltage and $T_{\mathrm{j0}} = (273.15 + 150)\,\mathrm{K}$ or $(273.15 + 175)\,\mathrm{K}$ is the junction temperature at which the measurements were conducted.

Estimating the increase of the turn-on energy loss due to the reverse recovery charge of diodes

Most of the results presented in **Section 2.1.3** are solely based on experimental analysis. Only the losses of the two converter configurations which use conventional IGBTs with anti-parallel SiC SBDs C3D20060D for the bi-directional switch (configurations B3 and C3 in **Section 2.1.3**) are estimated.

According to **Section 2.1.2** the amount of reverse recovery charge, $Q_{\mathrm{rr}} = Q_{\mathrm{rs}} + Q_{\mathrm{rf}}$, for diodes (or the internal diode of the RB-IGBT on the collector side) $\mathrm{D_3}$ and $\mathrm{D_4}$ have a strong impact on the resulting turn-on losses of IGBTs $\mathrm{T_1}$ and $\mathrm{T_2}$. Thus, the turn-on switching losses available in the data sheets are not readily applicable to the presented comparison, since the T-type inverter employs different types of power semiconductor switches, i.e., $\mathrm{T_1}$ and $\mathrm{T_2}$ are conventional IGBT / diode modules with $V_{\mathrm{(BR)CES}} = 1200\,\mathrm{V}$ and $\mathrm{T_3}$ and $\mathrm{T_4}$ are RB-IGBTs or IGBT / diode modules with $V_{\mathrm{(BR)CES}} = 600\,\mathrm{V}$.

The expected turn-on losses can be estimated based on [27] using the transient voltage and current waveforms during turn-on depicted in **Figure 2.9(d) and (e)**. According to [27] the turn-on losses of the IGBT, $E_{\mathrm{on,T}}$, can be separated into two parts. The first part denotes the turn-on losses without reverse recovery,

$$E_{\mathrm{on,T,0}} = E_{\mathrm{on,T}} - \Delta E_{\mathrm{on,T}}, \quad (2.30)$$

and the second part denotes the additional losses due to reverse recovery,

$$\Delta E_{\mathrm{on,T}} \approx \left(t_{\mathrm{s}} i_{\mathrm{L,ac}} + Q_{\mathrm{rs}}\right) \frac{V_{\mathrm{dc}}}{2}; \tag{2.31}$$

t_{s} is the delay time due to reverse recovery,

$$t_{\mathrm{s}} = t_{\mathrm{b3}} - t_{\mathrm{b2}}. \tag{2.32}$$

$E_{\mathrm{on,T,0}}$ is calculated based on measurement results. The turn-on losses with SiC SBDs instead of Si diodes (configurations B3 and C3 in **Section 2.1.3**) are estimated with **(2.30)** as

$$\tilde{E}_{\mathrm{on,T}} = E_{\mathrm{on,T,0}} + \Delta\tilde{E}_{\mathrm{on,T}}, \tag{2.33}$$

where the second term denotes the estimated additional losses due to the total capacitive charge Q_{c} from SiC SBDs,

$$\Delta\tilde{E}_{\mathrm{on,T}} = \left(\tilde{t}_{\mathrm{s}} i_{\mathrm{L,ac}} + Q_{\mathrm{c}}\right) \frac{V_{\mathrm{dc}}}{2}; \tag{2.34}$$

$\tilde{t}_{\mathrm{s}}$ is the estimated delay time due to Q_{c},

$$\tilde{t}_{\mathrm{s}} = \sqrt{\frac{2Q_{\mathrm{c}}}{i'_{\mathrm{c,T}}(t_{\mathrm{b2}})}}, \tag{2.35}$$

$i'_{\mathrm{c,T}}(t_{\mathrm{b2}})$ is the value of the derivative of the collector current at $t = t_{\mathrm{b2}}$, and measurement results are used for this value. $Q_{\mathrm{c}} = 16\,\mathrm{nC}$ at a reverse voltage of $V_{\mathrm{r}} = 360\,\mathrm{V}$ is obtained from the data sheet of C3D20060D.

Thermal model

The temperature of each semiconductor's junction is calculated based on the simplified thermal resistance network model. **Figure 2.10(a)** illustrates a cross section of the power semiconductor packages mounted on a single heat sink unit. In this thesis, a TO-247 discrete package is employed for all semiconductor devices. The semiconductor chips of the IGBT and the diode are integrated into a single TO-247 package for the standard IGBT / diode power semiconductor module (e.g. T_1 and D_1). An insulation sheet is inserted between the package and the heat sink as interface material. **Figure 2.10(b)** shows an equivalent thermal resistance network model of **Figure 2.10(a)**. $P_{\mathrm{semi,tot,\sharp}}$ is the total

semiconductor loss per chip (i.e., $P_{\mathrm{semi,tot,T1}} = P_{\mathrm{semi,cond,T1}} + P_{\mathrm{semi,sw,T1}}$ for $\mathrm{T_1}$). $R_{\mathrm{th,j-c,\sharp}}$ is the thermal resistance between the junction of the semiconductor and the surface of the case, $R_{\mathrm{th,c-hs}}$ is the thermal resistance of the insulation sheet per case, and $R_{\mathrm{th,hs}}$ is the averaged thermal resistance of the heat sink unit. Here, a homogeneous surface temperature T_{hs} of the heat sink is assumed. The temperature rise $\Delta T_{\mathrm{j-c,\sharp}}$ between the junction and the surface of the case is

$$\Delta T_{\mathrm{j-c,\sharp}} = R_{\mathrm{th,j-c,\sharp}} P_{\mathrm{semi,tot,\sharp}}, \tag{2.36}$$

and the temperature rise $\Delta T_{\mathrm{c-hs,\sharp}}$ between the surface of the heat sink and the case is

$$\Delta T_{\mathrm{c-hs,\sharp}} = R_{\mathrm{th,c-hs}} P_{\mathrm{semi,tot,case,\sharp}}, \tag{2.37}$$

where $P_{\mathrm{semi,tot,case,\sharp}}$ is the total semiconductor loss per case, e.g. $P_{\mathrm{semi,tot,case,T1D1}} = P_{\mathrm{semi,tot,T1}} + P_{\mathrm{semi,tot,D1}}$ for the $\mathrm{T_1}$ / $\mathrm{D_1}$ module, and $P_{\mathrm{semi,tot,case,T2}} = P_{\mathrm{semi,tot,T2}}$ for $\mathrm{T_2}$. The temperature rise ΔT_{hs} between the ambient temperature and the surface of the heat sink is

$$\Delta T_{\mathrm{hs}} = R_{\mathrm{th,hs}} P_{\mathrm{semi,tot,unit}}, \tag{2.38}$$

$$P_{\mathrm{semi,tot,unit}} = P_{\mathrm{semi,tot,T1}} + P_{\mathrm{semi,tot,D1}} + \cdots + P_{\mathrm{semi,tot,T4}}, \tag{2.39}$$

where $P_{\mathrm{semi,tot,unit}}$ is the total semiconductor loss per heat sink unit. By summing up all the temperature rises over the thermal network, the junction temperature $T_{\mathrm{j,\sharp}}$ is calculated as

$$T_{\mathrm{j,\sharp}} = \Delta T_{\mathrm{j-c,\sharp}} + \Delta T_{\mathrm{c-hs,\sharp}} + \Delta T_{\mathrm{hs}} + T_{\mathrm{amb}}. \tag{2.40}$$

The junction temperature and loss calculation of each single device must be iterated in order to complete an electro-thermal calculation, however, an iteration including the calculation of the heat sink thermal resistance would increase the computational cost.

Therefore, by assuming the maximum heat sink temperature $T_{\mathrm{hs,max}} > T_{\mathrm{amb}}$, the thermal network model of power semiconductor devices is simplified as shown in **Figure 2.10(c) and (d)**. With this simplified equivalent thermal network model, the calculation of the junction temperature which is shown in **(2.40)** is simplified according to:

$$T_{\mathrm{\beth,\sharp}} = \Delta T_{\mathrm{j-c,\sharp}} + \Delta T_{\mathrm{c-hs,\sharp}} + T_{\mathrm{hs,max}}. \tag{2.41}$$

Here, $T_{hs,max} = (100 + 273.15)\,\mathrm{K}$ is assumed for the optimization.

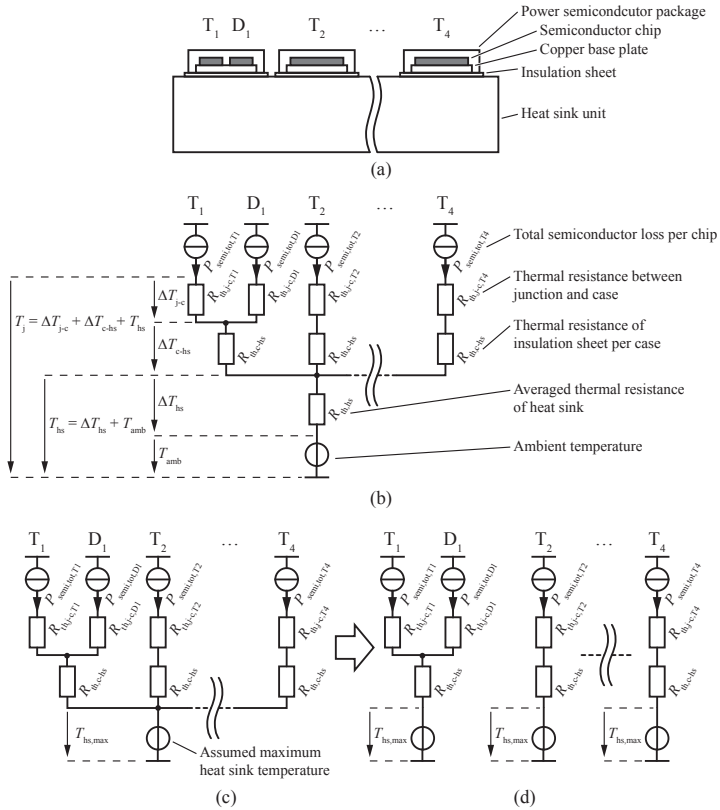


Figure 2.10: Thermal resistance network model of power semiconductor devices: (a) cross section of power semiconductor packages per single heat sink unit, (b) equivalent thermal resistance network model of power semiconductors including the averaged thermal resistance $R_{\mathrm{th,hs}}$ of the heat sink, (c) simplified thermal resistance network model with assumed maximum heat sink temperature $T_{\mathrm{hs,max}}$, and (d) equivalent thermal resistance network model for the individual power semiconductor package based on simplified thermal network model.

The thermal resistance $R_{\mathrm{th,c-hs}}$ of the insulation sheet can be calculated from the thermal impedance of the insulation sheet $\sigma_{\mathrm{th,c-hs}}\,\mathrm{K \cdot mm^2/W}$ and the cross-sectional area of the thermal inter-

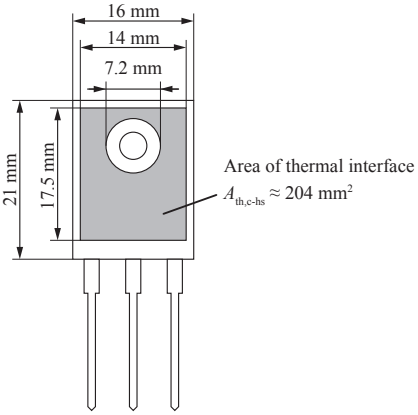


Figure 2.11: Dimensions of TO-247 package and considered area of the thermal interface.

face $A_{\mathrm{th,c-hs}}$. **Figure 2.11** depicts the dimensions of the TO-247 discrete package. From this figure, the area of the thermal interface of the TO-247 package is

$$A_{\mathrm{th,c-hs}} \approx 204\,\mathrm{mm}^2. \tag{2.42}$$

For optimization, Hi-Flow 300P [28] was employed as insulation sheet material; it has a thermal impedance of

$$\sigma_{\mathrm{th,c-hs}} \approx 123\,\mathrm{K}\cdot\mathrm{mm}^2/\mathrm{W} \tag{2.43}$$

at a mounting pressure of 10 psi and material thickness of 0.05 mm. As a result,

$$R_{\mathrm{th,c-hs}} = \frac{\sigma_{\mathrm{th,c-hs}}}{A_{\mathrm{th,c-hs}}} \approx 0.6\,\mathrm{K/W} \tag{2.44}$$

is used for the optimization in the following sections.

Loss calculation procedure

Figure 2.12 shows a flow chart of the proposed losses and junction temperature calculation procedure for the power semiconductors of the AC part. The implemented procedure requires the following to be specified:

- The switching frequency of the AC part, f_{sw};

- the modulation index M;
- the amplitude $\hat{I}_{\mathrm{ac}}$ of the input / output current fundamental;
- the phase displacement Φ_{d} between the fundamental components of current and voltage;
- the DC-link voltage V_{dc};
- the assumed surface temperature $T_{\mathrm{hs,max}}$ of the heat sink;
- the maximum number N_{max} of iterative loops for the electro-thermal model;
- the number N_{semi} of power semiconductor parameter sets;
- the power semiconductor parameter sets.

The power semiconductor parameter sets include parameters for conduction / switching loss calculation, and the thermal resistance values of the package / insulation sheet as described before. The maximum junction temperatures $T_{\mathrm{j,max}}$ of the individual semiconductor devices are considered part of the thermal model parameters. For the first step, the conduction and switching currents are calculated for all devices. In the second step, the ith parameter set of power semiconductors is selected and the parameters for the conduction / switching loss calculation are initialized with the initial junction temperature of $T_{\mathrm{j}}(t = 0) = T_{\mathrm{hs,max}}$. Next, the conduction / switching losses and junction temperatures of individual devices are calculated. If the junction temperature at the current loop t ($T_{\mathrm{j}}(t)$) exceeds the maximum junction temperature $T_{\mathrm{j,max},i}$, the iterative loop of the electro-thermal model terminates and the current design set of the semiconductor is discarded. If the calculated junction temperature is below the maximum value, then the difference between the junction temperatures $\Delta T_{\mathrm{j}}(t)$ is calculated from the previous and current iteration loop values $T_{\mathrm{j}}(t-1)$ and $T_{\mathrm{j}}(t)$. If $\Delta T_{\mathrm{j}}(t)$ is not smaller than 1 K, the iteration index of t is incremented and the parameters for the conduction / switching loss calculation are updated with the calculated junction temperature. The loss calculation procedure is then repeated. This procedure is iterated until it satisfies $\Delta T_{\mathrm{j}}(t) \leq 1\,\mathrm{K}$ in order to calculate the semiconductor losses for the thermal model in a quasi steady-state. The result that satisfies the ΔT_{j} criteria is treated as a valid result and is stored

in the design pool for subsequent procedures. If the number of iterations exceeds $N_{\max}$, the iterative electro-thermal model is treated as having failed to converge (the accuracy of the calculation result is not guaranteed). In this case, the current semiconductor design set is discarded. After this iterative procedure has been calculated for all power semiconductor parameter sets, an automatic evaluation and selection of the semiconductor sets is performed to select the optimal power semiconductor configuration that gives the minimum total semiconductor losses for high converter efficiency. The total semiconductor losses for the selected power semiconductor configuration $P_{\text{semi,tot}}$ and the required mounting length $L_{\text{semi,tot}}$ per single heat sink unit are then used in the optimization procedure for the cooling system, as discussed in **Section 2.2**.

2.1.3 Comparison of T-type converters with and without RB-IGBTs

IGBT / diode modules suitable for comparison

Different types of IGBTs are considered for the bi-directional switch, including devices optimized with respect to low conduction losses or low switching losses, in order to allow for a meaningful comparison of the losses obtained with conventional IGBTs and RB-IGBTs. **Table 2.3** lists the considered devices: Two parallel connected components IGBT1 are considered in order to achieve reduced conduction losses and, thus, the total maximum forward currents of D_1 and D_2 are 60 A. In order to reduce costs, the rated currents of the selected SiC SBDs (SBD1 and SBD2) are approximately two-thirds of the rated currents of the Si diodes. With this, the diode currents are still well below the rated diode currents. However, considerably increased conduction losses result.

- IGBT1: 1200 V IGBT + diode for T_1, T_2, D_1 and D_2.
- IGBT2: 600 V RB-IGBT for T_3, T_4, D_3 and D_4.
- IGBT3 / IGBT4: two 600 V IGBT + diodes for T_3, T_4, D_3 and D_4.
- SBD1: 1200 V SiC SBD for D_1 and D_2.
- SBD2: 600 V SiC SBD for D_3 and D_4.

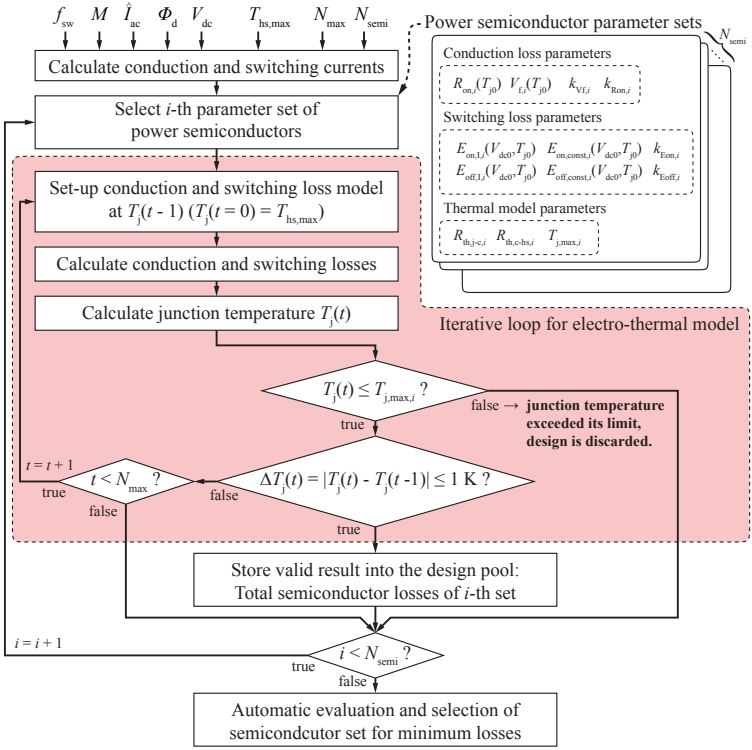


Figure 2.12: Flow chart of the power semiconductor losses and junction temperature calculation procedure.

Parameterization of the conduction loss models

The conduction loss model is parameterized with the data sheet values based on a least mean square approximation. The obtained coefficients are listed in Table 2.4. There, IGBT(T) denotes the IGBT and IGBT(D) the diode of a single package containing both, an IGBT and a diode. **Figure 2.13** depicts the forward characteristics of the considered devices.

Table 2.3: Considered semiconductor devices for loss comparison; $V_{(\mathrm{BR})\mathrm{CES}}$: maximum collector–emitter voltage of IGBTs; V_{RRM}: repetitive peak reverse voltage of diodes; I_{C}: maximum DC collector current of IGBTs; I_{F}: maximum DC forward current of diodes; N_{p}: the number of paralleled modules.

Name	Device type	$V_{(\mathrm{BR})\mathrm{CES}}$, V_{RRM}	I_{C}, I_{F}
IGBT1	Si IGBT and diode	1200 V	40 / 30 A
SBD1	SiC SBD	1200 V	18 A
IGBT2	Si RB-IGBT	600 V	85 A
IGBT3	Si IGBT and diode	600 V	75 / 30 A
IGBT4	Si IGBT and diode	600 V	75 / 30 A
SBD2	SiC SBD	600 V	20 A

Name	$R_{\mathrm{th,j-c,T}}$ / $R_{\mathrm{th,j-c,D}}$	N_{p}	Model number	Manufacturer
IGBT1	0.439 / 0.781 K/W	2	FGW40N120HD	Fuji Electric
SBD1	0.63 K/W	2	FDCW18S120	Fuji Electric
IGBT2	0.208 K/W	1	FGW85N60RB	Fuji Electric
IGBT3	0.21 / 0.9 K/W	1	IXXH75N60C3D1	IXYS
IGBT4	0.21 / 0.9 K/W	1	IXXH75N60B3D1	IXYS
SBD2	0.55 K/W	1	C3D20060D	CREE

Table 2.4: Extracted conduction loss model parameters.

Name	T_{j0} / $T_{\mathrm{j,max}}$	$V_{\mathrm{f}}(T_{j0})$	$R_{\mathrm{on}}(T_{j0})$	k_{Vf}	k_{Ron}
IGBT1(T)	175 °C	1.04 V	16 mΩ	0.0565	1.22
IGBT1(D)	175 °C	1.04 V	16 mΩ	-1.1163	0.288
SBD1	150 °C	0.75 V	37 mΩ	-0.6346	1.824
IGBT2	150 °C	1.06 V	18 mΩ	-0.3373	0.55
IGBT3(T)	150 °C	1.02 V	21 mΩ	0.0838	1.108
IGBT4(T)	150 °C	0.76 V	16 mΩ	-0.3044	1.155
IGBT3(D)	150 °C	1.01 V	18 mΩ	-1.5906	-0.819
IGBT4(D)	Same as IGBT3(D)				
SBD2	175 °C	0.72 V	65 mΩ	-0.6061	1.989

Parameterization of the switching loss models and measured switching losses

During switching, a device with a breakdown voltage of 1200 V and a second device with $V_{(\mathrm{BR})\mathrm{CES}} = 600\,\mathrm{V}$ are operated together, cf. **Section 2.1.2**, and, according to **Table 2.2**, the resulting switching losses depend on the combination of switches. With the considered IGBTs

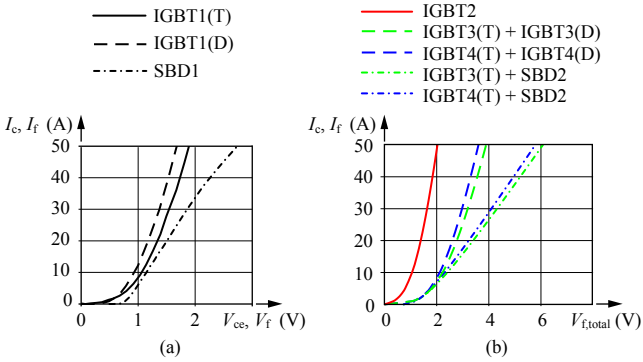


Figure 2.13: On-state forward voltage drop versus collector or forward current at $T_j = 150\,°C$, (a) for switches with $V_{(BR)CES} = 1200\,V$ and (b) for bi-directional switches, cf. **Figure 2.2**, with $V_{(BR)CES} = 600\,V$.

and SiC SBDs, the eight different combinations of devices listed in **Table 2.5** are feasible. The switching losses resulting from the first six combinations, A1, B1, C1, A2, B2 and C2, were measured with the switching loss measurement setup depicted in **Figure 2.14** under the conditions listed below:

- Employed DC-link voltage: $V_{dc} = 720\,V$;
- Junction temperatures: $T_j = 30\,°C$, $T_j = 150\,°C$;
- Gate resistance: $R_g = 5.1\,\Omega$;
- On- and off-state gate voltages: $V_{ge,on} = 16\,V$, $V_{ge,off} = -6\,V$.

The switching losses obtained for the remaining combinations, B3 and C3, were estimated using **(2.33)**.

The resulting switching losses are shown in **Figure 2.15** for all considered device combinations. The extracted parameters of the switching loss model are listed in **Table 2.6**.

In the rectifier mode of operation, the turn-on losses of T_3 and T_4, $E_{on,T34}$, and the reverse recovery losses of the diodes D_1 and D_2, $E_{off,D12}$, largely depend on the reverse recovery behavior of D_1 and D_2. Therefore, as shown in **Figure 2.15(b) and (c)**, $E_{on,T34}$ and $E_{off,D12}$ are similar for the device combinations A1, B1, and C1 and can be

Table 2.5: Combination of switching devices for comparison.

Label	1200 V IGBT for T_1 and T_2	1200 V diode for D_1 and D_2
A1	Si IGBT (IGBT1(T))	Si diode (IGBT1(D))
B1	Si IGBT (IGBT1(T))	Si diode (IGBT1(D))
C1	Si IGBT (IGBT1(T))	Si diode (IGBT1(D))
A2	Si IGBT (IGBT1(T))	SiC SBD (SBD1)
B2	Si IGBT (IGBT1(T))	SiC SBD (SBD1)
C2	Si IGBT (IGBT1(T))	SiC SBD (SBD1)
B3	Si IGBT (IGBT1(T))	SiC SBD (SBD1)
C3	Si IGBT (IGBT1(T))	SiC SBD (SBD1)

Label	600 V IGBT for T_3 and T_4	600 V diode for D_3 and D_4
A1	Si RB-IGBT (IGBT2)	Si RB-IGBT (IGBT2)
B1	Si IGBT (IGBT3(T))	Si diode (IGBT3(D))
C1	Si IGBT (IGBT4(T))	Si diode (IGBT4(D))
A2	Si RB-IGBT (IGBT2)	Si RB-IGBT (IGBT2)
B2	Si IGBT (IGBT3(T))	Si diode (IGBT3(D))
C2	Si IGBT (IGBT4(T))	Si diode (IGBT4(D))
B3	Si IGBT (IGBT3(T))	SiC SBD (SBD2)
C3	Si IGBT (IGBT4(T))	SiC SBD (SBD2)

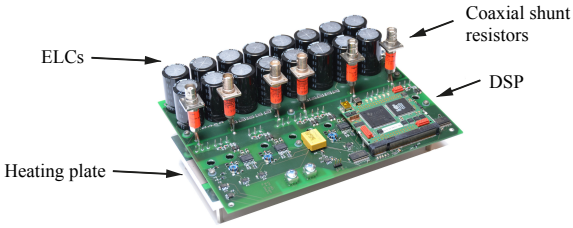


Figure 2.14: The switching loss measurement setup.

considerably reduced with SiC SBDs (combinations A2, B2, C2, A3, and B3), i.e., the type of IGBT used for T_3 and T_4 has only a small influence on the achieved turn-on losses. The IGBT selected for T_3 and T_4 mainly determines the obtained turn-off losses, cf. **Figure 2.15(a)**: it is seen that the IBGT optimized for speed yields minimum switching losses (e.g. B1); maximum switching losses result with the IGBT optimized for low conduction losses (e.g. C1), and the losses obtained with the considered RB-IGBT are in between (e.g. A1).

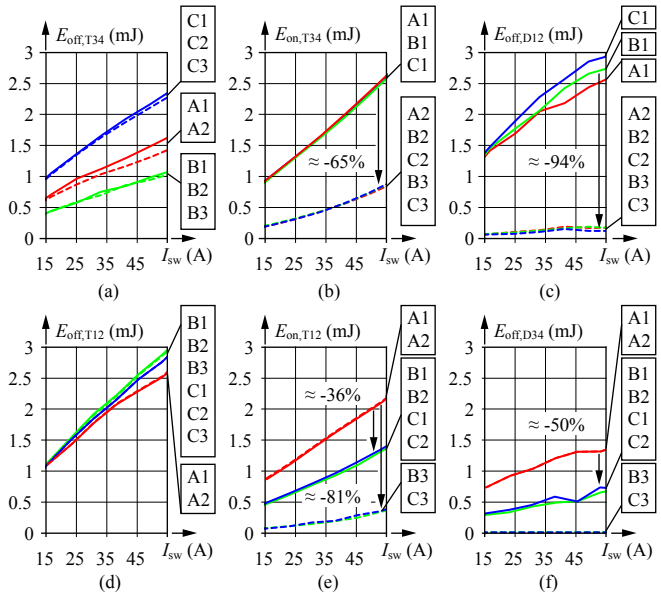


Figure 2.15: Switching losses, measured (A1, A2, A3, B1, B2, C1, C2) and estimated (B3, C3) for the different considered device combinations, different switch currents I_{sw}, $V_{dc} = 720\,V$, and $T_j = 150\,°C$: (a), (b) and (c) denote the switching losses for rectifier mode of operation and (d), (e) and (f) switching losses for the inverter mode of operation.

In inverter mode of operation, the turn-on losses of T_1 and T_2, $E_{on,T12}$, and the reverse recovery losses of D_3 and D_4, $E_{off,D34}$, mainly depend on the devices employed for D_3 and D_4. Thus, due to the relatively high reverse recovery charges of the internal diode of the RB-IGBTs on the collector side, the values for $E_{on,T12}$ and $E_{off,D34}$ are considerably higher for the configurations A1 and A2 than for the configurations using conventional IGBT / diode modules (B1, B2, B3, C2, and C3), since the use of faster and smaller chips allows a reduction of the reverse recovery charge of the employed diodes. The turn-off losses of T_1 and T_2, $E_{off,T12}$ are in large part caused by the tail currents of T_1 and T_2 and are nearly independent of the type of diode selected for D_3 and D_4.

Table 2.6: Parameter values for the switching loss models for the different device combinations being determined for $V_{\mathrm{dc0}} = 720\,\mathrm{V}$ and $T_{\mathrm{j0}} = 150\,^{\circ}\mathrm{C}$.

	1200 V IGBT (T_1 and T_2)					
	$E_{\mathrm{off,I}}$	$E_{\mathrm{off,const}}$	$k_{\mathrm{E_{off}}}$	$E_{\mathrm{on,I}}$	$E_{\mathrm{on,const}}$	$k_{\mathrm{E_{on}}}$
A1	38 µJ/A	563 µJ	0.598	32 µJ/A	364 µJ	1.767
B1	46 µJ/A	371 µJ	0.919	21 µJ/A	11 µJ	2.396
C1	45 µJ/A	383 µJ	0.929	22 µJ/A	121 µJ	1.946
A2	Same as A1			Same as A1		
B2	Same as B1			Same as B1		
C2	Same as C1			Same as C1		
B3	45 µJ/A	364 µJ	0.919	6 µJ/A	−17 µJ	2.067
C3	44 µJ/A	376 µJ	0.929	7 µJ/A	−26 µJ	0.742

	600 V IGBT (T_3 and T_4)					
	$E_{\mathrm{off,I}}$	$E_{\mathrm{off,const}}$	$k_{\mathrm{E_{off}}}$	$E_{\mathrm{on,I}}$	$E_{\mathrm{on,const}}$	$k_{\mathrm{E_{on}}}$
A1	20 µJ/A	239 µJ	2.123	38 µJ/A	234 µJ	1.259
B1	14 µJ/A	139 µJ	1.192	35 µJ/A	221 µJ	1.416
C1	30 µJ/A	417 µJ	1.006	36 µJ/A	235 µJ	1.331
A2	16 µJ/A	257 µJ	2.448	17 µJ/A	−83 µJ	-0.026
B2	14 µJ/A	149 µJ	1.191	16 µJ/A	−92 µJ	-0.423
C2	29 µJ/A	424 µJ	1.013	17 µJ/A	−94 µJ	0.146
B3	Same as B2			Same as B2		
C3	Same as C2			Same as C2		

	1200 V Diode (D_1 and D_2)			600 V Diode (D_3 and D_4)		
	$E_{\mathrm{off,I}}$	$E_{\mathrm{off,const}}$	$k_{\mathrm{E_{off}}}$	$E_{\mathrm{off,I}}$	$E_{\mathrm{off,const}}$	$k_{\mathrm{E_{off}}}$
A1	19 µJ/A	557 µJ	3.573	13 µJ/A	418 µJ	1.779
B1	23 µJ/A	559 µJ	3.139	8 µJ/A	80 µJ	2.424
C1	24 µJ/A	581 µJ	3.434	9 µJ/A	141 µJ	1.85
A2	3 µJ/A	83 µJ	0.024	Same as A1		
B2	3 µJ/A	72 µJ	-0.184	Same as B1		
C2	2 µJ/A	78 µJ	-0.477	Same as C1		
B3	Same as B2			0 µJ/A	0 µJ	0
C3	Same as C2			0 µJ/A	0 µJ	0

Loss comparisons and discussion

The total semiconductor losses of three-phase 3LTTC with and without an RB-IGBT are analyzed. In **Figure 2.16(a) and (b)**, the total semiconductor losses of the 3LTTC are presented for operation in the switching frequency range of 5 kHz to 35 kHz for rectifier and inverter

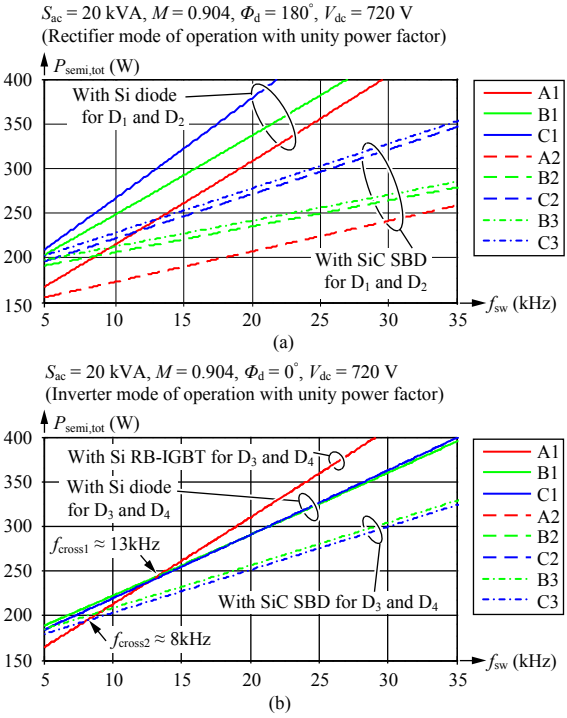


Figure 2.16: Total loss comparison of three-phase 3LTTCs for the eight different device combinations listed in **Table 2.5** operating with unity power factor, $\hat{V}_{ac} = 325\,\text{V}$ and $\hat{I}_{ac} = 41\,\text{A}$: (a) result for rectifier mode of operation ($\Phi_d = 180\,^\circ$) and (b) for inverter mode of operation ($\Phi_d = 0\,^\circ$). f_{cross1} is the crossover frequency for the total losses regarding A1 and B1 (or A1 and C1), f_{cross2} is the crossover frequency of A1 and B3 (or A1 and C3).

modes of operation, respectively.

In rectifier mode of operation, **Figure 2.16(a)**, the configuration with RB-IGBTs, A1, shows lower total losses than B1 and C1, mainly because the internal diodes of the RB-IGBTs, D_3 and D_4, generate no reverse recovery effects in the rectifier mode of operation and, thus, the reduced conduction losses of the bi-directional switch formed with RB-IGBTs directly facilitates lower total losses. A detailed inspection reveals that configuration B1 generates lower total switching losses than

A1, with configuration B1 yielding the lowest total losses at very high switching frequencies $f_{sw} > 69\,kHz$. However, the exceedingly high total losses of more than 800 W render these solutions less suitable. A further total loss reduction is achieved with the SiC SBDs being used for D_1 and D_2. Due to the zero reverse recovery charge of D_1 and D_2, large switching loss reductions of $E_{on,T34}$ and $E_{off,D12}$ are achieved as shown in **Figure 2.15(b) and (c)**. Again, the configuration with RB-IGBTs, A2, also features lower total losses than configurations B2 and C2 (up to $f_{sw} = 71\,kHz$) because of the reduced conduction losses achieved with RB-IGBTs. No improvements are achieved with configurations B3 and C3 (SiC SBDs D_3 and D_4 in parallel to conventional IGBTs T_3 and T_4) in rectifier mode of operation, since the diodes D_3 and D_4 generate no reverse recovery effects.

In inverter mode of operation, configuration A1 allows for lower total losses than configurations B1 and C1 for switching frequencies up to 13 kHz as shown in **Figure 2.16(b)**. In inverter mode of operation, D_3 and D_4 are subject to reverse recovery effects, which cause the increased total losses of configuration A1, i.e., configuration A1 shows higher values of $E_{on,T12}$ and $E_{off,D34}$ than configurations B1 and C1, cf. Figure 2.15(e) and (f). In inverter mode of operation, with unity power factor, the diodes D_1 and D_2 do not contribute to the switching losses and, therefore, the losses calculated for the configurations A2, B2, and C2, i.e., D_1 and D_2, realized with SiC SBDs, are similar to the losses calculated for the configurations A1, B1, and C1, respectively. Further total loss reductions are calculated for configurations B3 and C3 (SiC SBDs used for the diodes of D_3 and D_4) for switching frequencies greater than 8 kHz due to the zero reverse recovery charge from these SiC SBDs.

Figure 2.17 depicts the loss distributions (conduction and switching losses of all IGBTs and diodes) for the assumed total semiconductor losses of 500 W, which would give the power semiconductor part an efficiency of 97.5 %. These losses are equally distributed between the rectifier and inverter, i.e., 250 W each. Figure 2.17 also shows the switching frequency achieved for the assumed total semiconductor losses and for the different configurations. In rectifier mode of operation, **Figure 2.17(a)**, configuration A1 shows lower total conduction losses and a higher operating switching frequency of 13.9 kHz than configurations B1 (10.3 kHz) and C1 (8.7 kHz). Higher switching frequencies are achieved if D_1 and D_2 are replaced by SiC SBDs, i.e., with configurations A2

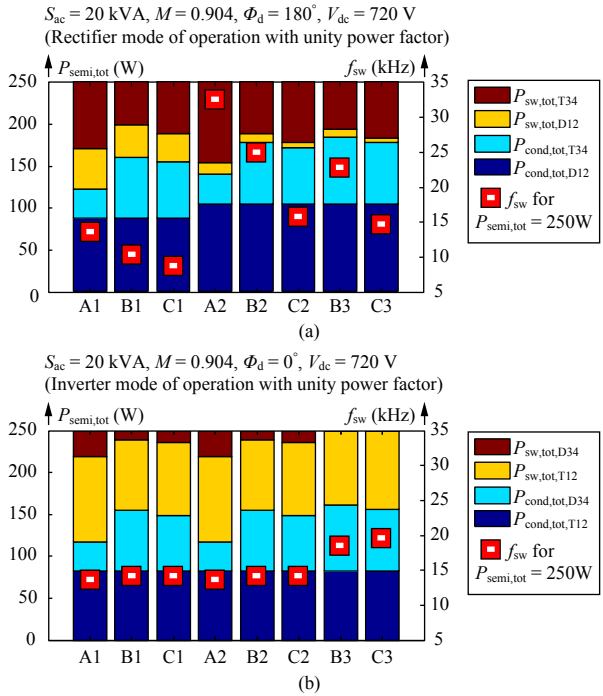


Figure 2.17: Total conduction and switching loss distributions of three-phase 3LTTC for the eight different configurations listed in **Table 2.5** and for operation with fixed total loss $P_{\mathrm{semi,tot}} = 250\,\mathrm{W}$, unity power factor, $\hat{V}_{\mathrm{ac}} = 325\,\mathrm{V}$ and $\hat{I}_{\mathrm{ac}} = 41\,\mathrm{A}$: (a) results for rectifier mode of operation ($\Phi_{\mathrm{d}} = 180\,^{\circ}$) and (b) inverter mode of operation ($\Phi_{\mathrm{d}} = 0\,^{\circ}$). The red marks show the operating switching frequencies determined for fixed total loss. $P_{\mathrm{cond,tot,T12}}$, $P_{\mathrm{cond,tot,D12}}$, $P_{\mathrm{cond,tot,T34}}$ and $P_{\mathrm{cond,tot,D34}}$ denote the total conduction losses of $\mathrm{T_1}\,/\,\mathrm{T_2}$, $\mathrm{D_1}\,/\,\mathrm{D_2}$, $\mathrm{T_3}\,/\,\mathrm{T_4}$ and $\mathrm{D_3}\,/\,\mathrm{D_4}$, respectively. $P_{\mathrm{sw,tot,T12}}$, $P_{\mathrm{sw,tot,D12}}$, $P_{\mathrm{sw,tot,T34}}$ and $P_{\mathrm{sw,tot,D34}}$ are the total switching losses of $\mathrm{T_1}\,/\,\mathrm{T_2}$, $\mathrm{D_1}\,/\,\mathrm{D_2}$, $\mathrm{T_3}\,/\,\mathrm{T_4}$ and $\mathrm{D_3}\,/\,\mathrm{D_4}$, respectively.

(32.5 kHz), B2 (25.2 kHz), and C2 (15.8 kHz). There, the total conduction losses are slightly higher than for configurations A1, B1, and C1 due to the increased conduction losses of the SiC SBDs. However, the total switching losses are reduced due to the zero reverse recovery charge of $\mathrm{D_1}$ and $\mathrm{D_2}$. Configurations B3 and C3 show higher conduction

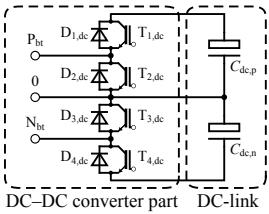


Figure 2.18: Schematic drawing of the power circuit of the bidirectional buck-boost type DC–DC converter.

losses due to the SiC SBDs that are used to realize the bi-directional switch, with no further reduction in the switching losses being achieved. Therefore, the operating switching frequencies are lower than for configurations B2 and C2. Thus, for rectifier mode of operation and assumed semiconductor losses of 250 W, configurations A2, i.e., the use of SiC SBDs for D_1 and D_2 and RB-IGBTs, features the highest achievable switching frequency.

In inverter mode of operation, **Figure 2.17(b)**, configuration A1 shows lower total conduction losses than configurations B1 and C1. However, due to the considerably higher switching losses, the lowest operating switching frequency results for configuration A1. The losses calculated for configurations A2, B2, and C2 are identical to the losses calculated for configurations A1, B1, and C1 because in inverter mode of operation with unity power factor neither conduction losses nor switching losses change if SiC SBDs are used instead of Si diodes for D_1 and D_2. However, configurations B3 and C3 allow higher switching frequencies due to the reduced total switching losses. For inverter mode of operation, configuration C3 allows the highest achievable switching frequency of 19.7 kHz.

2.1.4 Analytical loss calculation model of DC–DC converter

The three-level bi-directional DC–DC converter depicted in **Figure 2.18** is employed for the considered UPS system. This topology employs 600 V IGBTs and diodes. Based on the discussion in the previous section, 600 V Si IGBTs and 600 V SiC SBDs were selected as most suitable configuration of the power semiconductors. When the mains

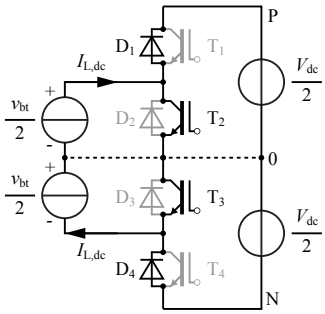


Figure 2.19: Single leg of the DC–DC boost converter.

is on-line, the DC–DC converter is operated in buck converter mode in order to charge the batteries. In that case, $T_{1,dc}$, $T_{4,dc}$, $D_{2,dc}$ and $D_{3,dc}$ are used as switching devices and energy flows from the DC-link capacitors to the batteries for charging. When the mains fails, $T_{2,dc}$, $T_{3,dc}$, $D_{1,dc}$ and $D_{4,dc}$ are used as switching devices and the DC–DC converter is operated as a boost converter. The direction of the energy flow in boost converter mode is from the battery to the DC-link capacitors for discharging the batteries in order to maintain the uninterruptible power supply function. Typically, the output power for charging the batteries is considerably smaller than the output power for discharging, and hence the loss calculation is performed for the boost converter mode.

Since detailed conduction and switching loss calculation models were discussed in the previous subsection, only the calculation model for the conduction and switching currents of the DC–DC converter are discussed in the following section.

Voltage and current waveforms of the DC–DC converter

A single leg of the DC–DC boost converter is shown in **Figure 2.19**. It is implemented using two Si IGBTs (T_2 and T_3) and two SiC SBDs (D_1 and D_4). Here, V_{bt} is the battery voltage and V_{dc} is the DC-link voltage. **Figure 2.20** illustrates the general switching voltage / current and corresponding gate signals of each device. The duty ratio for T_2 and T_3 is calculated as

$$d_{23} = 1 - \frac{V_{bt}}{V_{dc}}. \tag{2.45}$$

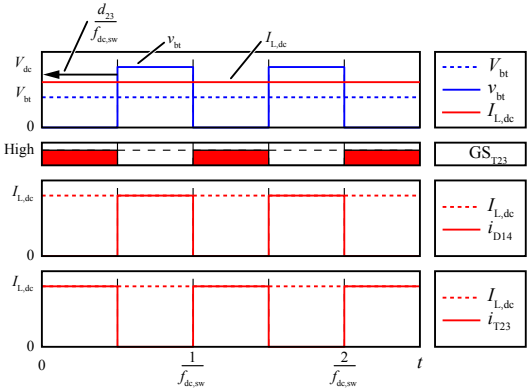


Figure 2.20: General switching waveforms of DC–DC converter and corresponding gate signals $GS_\sharp$, conduction currents $i_\sharp$ of each device for dedicated battery voltage V_{bt} and averaged inductor current $I_{L,dc}$.

The average DC current $I_{L,dc}$ through the inductor is defined from the output active power P_{ac} as

$$I_{L,dc} = \frac{P_{ac}}{V_{bt}}. \tag{2.46}$$

Conduction and switching loss model

The analytical expressions for the average and rms currents through all devices in the DC–DC converter are calculated as

$$I^2_{rms,T23,dc} = d_{23} \cdot I^2_{L,dc}, \tag{2.47}$$
$$I_{avg,T23,dc} = d_{23} \cdot I_{L,dc}, \tag{2.48}$$
$$I^2_{rms,D14,dc} = (1 - d_{23}) \cdot I^2_{L,dc}, \tag{2.49}$$
$$I_{avg,D14,dc} = (1 - d_{23}) \cdot I_{L,dc}. \tag{2.50}$$

These equations are derived by neglecting the high frequency current ripple in the boost inductors $L_{1,dc}$ and $L_{2,dc}$. Combining the temperature dependent on-state resistance $R_{on}(T_j)$ and forward voltage drop $V_f(T_j)$ of the semiconductors, the corresponding conduction losses can be calculated as

$$P_{semi,cond,dc} = R_{on}(T_j) \cdot I_{rms,dc}(d_{23}, I_{L,dc}) + V_f(T_j) \cdot I_{avg,dc}(d_{23}, I_{L,dc}). \tag{2.51}$$

The analytical expressions for the average switching currents for the DC–DC converter are summarized below:

$$I_{\mathrm{sw,avg,T23,dc}} = I_{\mathrm{L,dc}}, \tag{2.52}$$
$$D_{\mathrm{sw,T23,dc}} = 1, \tag{2.53}$$
$$I_{\mathrm{sw,avg,D14,dc}} = I_{\mathrm{sw,avg,T23,dc}}, \tag{2.54}$$
$$D_{\mathrm{sw,D14,dc}} = D_{\mathrm{sw,T23,dc}}. \tag{2.55}$$

As a result, the corresponding turn-off and turn-on losses for each IGBT and diode are calculated as

$$P_{\mathrm{semi,sw,off,dc}} = f_{\mathrm{sw,dc}} \left[E_{\mathrm{off,I}}(V_{\mathrm{dc}}, T_{\mathrm{j}}) \cdot I_{\mathrm{L,dc}} + E_{\mathrm{off,const}}(V_{\mathrm{dc}}, T_{\mathrm{j}}) \right], \tag{2.56}$$
$$P_{\mathrm{semi,sw,on,dc}} = f_{\mathrm{sw,dc}} \left[E_{\mathrm{on,I}}(V_{\mathrm{dc}}, T_{\mathrm{j}}) \cdot I_{\mathrm{L,dc}} + E_{\mathrm{on,const}}(V_{\mathrm{dc}}, T_{\mathrm{j}}) \right], \tag{2.57}$$
$$P_{\mathrm{semi,sw,dc}} = P_{\mathrm{semi,sw,off,dc}} + P_{\mathrm{semi,sw,on,dc}}. \tag{2.58}$$

2.2 Cooling system

This thesis considers a forced convection cooling system for the semiconductors. Such systems typically consist of a cooling fan and an extruded heat sink made of aluminum or copper. The power consumption of the cooling fan is treated as a cooling system power loss and has a minor contribution to the total power loss of active components. The total volumes of the cooling fan and heat sink are treated as volumes of the cooling system. In particular, the volume of the heat sink has a major impact on the total volume of the active components. Therefore, the heat sink geometry must be optimized in order to achieve high power density.

A basic optimization strategy and an analytical thermal resistance model based on a parameterized geometry for the heat sink are proposed and detailed in [29]. The original optimization strategy is modified to simplify the manufacturing of the heat sink, and employed as an optimization model of the cooling system. The modified optimization strategy and the thermal resistance model of the heat sink are summarized in this section.

2.2.1 Optimization strategy and procedure for the heat sink

The configuration and dimensions of the heat sink are depicted in **Figure 2.21(a)**. A double-sided mounting arrangement is employed in order to achieve a higher *Cooling System Performance Index* (CSPI) than the single-sided arrangement discussed in [29]. The CSPI is defined as

$$\mathrm{CSPI} = \frac{1}{R_{\mathrm{th,hs}} \cdot V_{\mathrm{cs,tot}}} \left[\frac{\mathrm{W}}{\mathrm{K} \cdot \mathrm{dm}^3}\right]. \tag{2.59}$$

Here, as in **Figure 2.21(a)**, b is the width of the heat sink and cooling fan, L_{hs} is the length of the heat sink, d is the thickness of the heat sink base plate, c is the length of the fins, n is the number of fins, and L_{fan} is the length of the cooling fan. $T_{\mathrm{hs,max}}$ is the pre-defined allowed maximum surface temperature of the heat sink, which is used for the optimization of the heat sink design. $P_{\mathrm{semi,max}}$ is the maximum total semiconductor loss per heat sink, which was discussed in the previous section. From these two values, the allowed maximum averaged thermal resistance $R_{\mathrm{th,hs,max}}$ of the heat sink unit can be calculated as

$$R_{\mathrm{th,hs,max}} = \frac{T_{\mathrm{hs,max}} - T_{\mathrm{amb}}}{P_{\mathrm{semi,max}}}\,[\mathrm{K/W}]. \tag{2.60}$$

Figure 2.21(b) shows the semiconductor package mounting configuration of the entire UPS system. In the proposed configuration, the maximum number of mounted TO-247 packages is 10 per heat sink unit at the inverter part. Therefore, the minimum length of the heat sink unit is defined as

$$L_{\mathrm{hs,min}} = L_{\mathrm{semi,tot}} = 10\,(b_{\mathrm{TO247}} + b_{\mathrm{clearance}})\,. \tag{2.61}$$

Here, $b_{\mathrm{TO247}} = 16\,\mathrm{mm}$ is the width of a single TO-247 package (cf. **Figure 2.11**), and $b_{\mathrm{clearance}} = 6\,\mathrm{mm}$ is the clearance between packages. As a result, $L_{\mathrm{hs,min}} = 220\,\mathrm{mm}$ is considered in the heat sink design optimization procedure.

The heat sink design must satisfy the following two design criteria:

- $R_{\mathrm{th,hs}} \leq R_{\mathrm{th,hs,max}}$,
- $L_{\mathrm{hs}} \leq L_{\mathrm{min}}$.

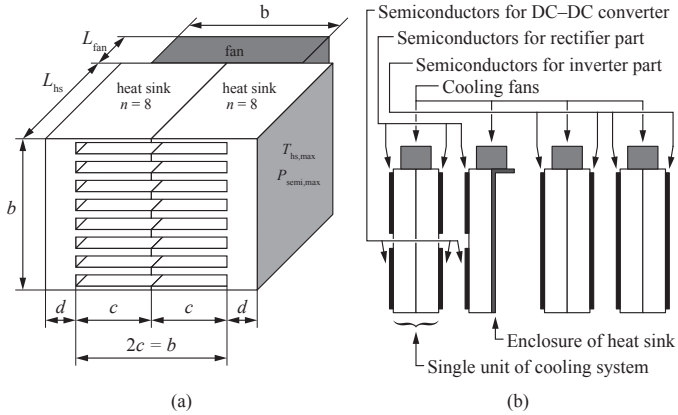


Figure 2.21: (a) Dimensions of the double-sided heat sink and cooling fans, (b) configuration of entire cooling system and distribution of semiconductors.

The heat sink optimization procedure is shown in **Figure 2.22**. $R_{\mathrm{th,hs,max}}$ and $L_{\mathrm{hs,min}}$ are given as input parameters. The thickness of the heat sink base plate is fixed, and $d = 5\,\mathrm{mm}$ is used for optimization. λ_{hs} is the thermal conductivity of the heat sink material. Typically, aluminum or copper is used for the heat sink. Due to its lower cost, aluminum ($\lambda_{\mathrm{hs}} = 236\,\mathrm{W/(m \cdot K)}$) is considered for the optimization. The cooling fan parameter sets are also included in the input parameters. These include the fan's characteristic (flow-rate vs. pressure curve), geometric dimensions, and power consumption. The cooling fans listed in **Table 2.7** are employed for optimization. The fan size defines the heat sink front geometry ($b = 2c$). The heat sink length L_{hs} is initialized with the minimum required length $L_{\mathrm{hs,min}}$. For the next step, the sweeping parameters n and t are set up in order to find the optimum combination of n and t. Here, n is the number of air channels and t is the thickness of the heat sink fins. After the iteration loop with index k, a local optimal design is selected to be evaluated with the required maximum thermal resistance. If the thermal resistance of the selected local optimal design $R_{\mathrm{th,hs}}(i,t)$ is not smaller than $R_{\mathrm{th,hs,max}}$, the length of the heat sink is increased by 10 % and the process is repeated until it satisfies $R_{\mathrm{th,hs}}(i,t) \leq R_{\mathrm{th,hs,max}}$. If the length

Table 2.7: List of cooling fans considered for optimization.

Model number	b	L_{fan}	$P_{cs,fan}$
SanAce 9GA0424P3J001	40 mm	28 mm	6.5 W
SanAce 9GA0624P1J03	60 mm	38 mm	18.0 W
SanAce 9GA0824P1S61	80 mm	38 mm	11.3 W

of heat sink L_{hs} reaches twice the minimum required length $L_{\text{hs,min}}$, the currently selected fan is discarded and the procedure is repeated with a different fan. After a valid design is found, the total boxed volume $V_{\text{cs,tot}}$ and total power consumption $P_{\text{cs,tot}}$ are calculated as

$$V_{\text{cs,tot}} = 4 \cdot b \cdot (b + 2d) \cdot (L_{\text{hs}} + L_{\text{fan}}), \tag{2.62}$$

$$P_{\text{cs,tot}} = 4 \cdot P_{\text{cs,fan}}. \tag{2.63}$$

These values are considered as the performance indices for optimization. This performance information and detailed design are stored in the main-design pool for automatic evaluation and selection of a minimal volume cooling system at the end of the heat sink optimization procedure.

2.2.2 Thermal model of the heat sink

The equivalent thermal resistance network of a single air-channel is illustrated in **Figure 2.23**. Equations for calculating all thermal resistances $R_{\text{th,d}}$, $R_{\text{th,a}}$, $R_{\text{th,FIN}}$ and $R_{\text{th,A}}$ are discussed in [29]. If the average heat transfer coefficient h is known, the thermal resistances and averaged thermal resistance $R_{\text{th,hs}}$ of the heat sink are

$$R_{\text{th,d}} = \frac{n \cdot d}{b \cdot L_{\text{hs}} \cdot \lambda_h s}, \tag{2.64}$$

$$R_{\text{th,a}} = \frac{1}{h \cdot L_{\text{hs}} \cdot s}, \tag{2.65}$$

$$R_{\text{th,A}} = \frac{1}{h \cdot L_{\text{hs}} \cdot c}, \tag{2.66}$$

$$R_{\text{th,FIN}} = \frac{c}{t \cdot L_{\text{hs}} \cdot \lambda_h s}, \tag{2.67}$$

$$R_{\text{th,hs}} = \frac{R_{\text{th,d}} + \left(R_{\text{th,FIN}} + R_{\text{th,A}}\right)/2}{n} + \frac{0.5}{\rho_{\text{air}} \cdot c_{\text{air}} \cdot \dot{V}_{\text{air}}}. \tag{2.68}$$

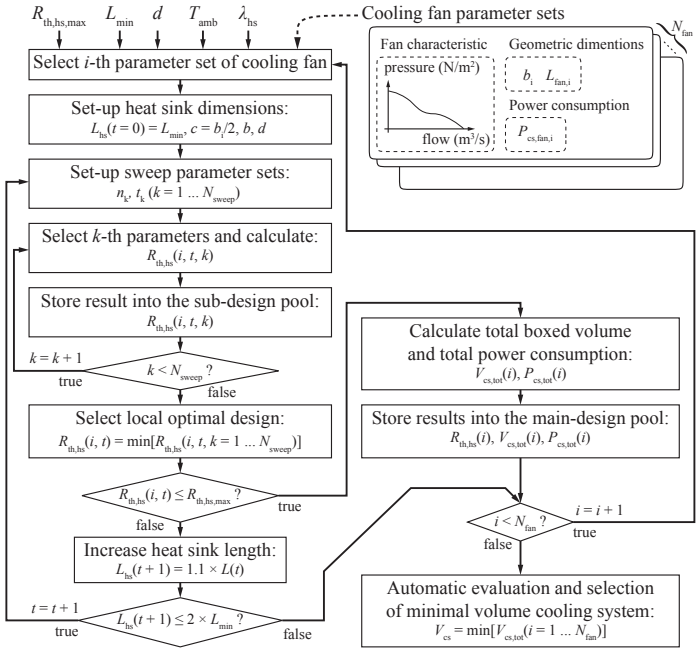


Figure 2.22: The flow chart of heat sink optimization procedure.

Here, ρ_{air} is the air density, c_{air} is the thermal capacitance of air, and $\dot{V}_{\text{air}}$ is the volumetric flow-rate of the air inside the air-channel. For the optimization, the temperature T_{channel} of the air inside the air-channel is assumed to be the same as the ambient temperature T_{amb}.

2.2.3 Experimental evaluation of thermal resistance of cooling system

Figure 2.24) shows an optimized heat sink unit employing fans of type SanAce 9GA0424P3J001. The calculated thermal resistance and CSPI of a single heat sink are shown in **Table 2.8**. In order to evaluate the heat sink design model, an experimental evaluation was performed. **Figure 2.25(a)** shows the experimental set-up for the heating resistances and the position of the temperature measurement points on the surface of the heat sink. Five 100 Ω heating resistors in TO-247 packages are mounted on each heat sink surface and connected to a controlled

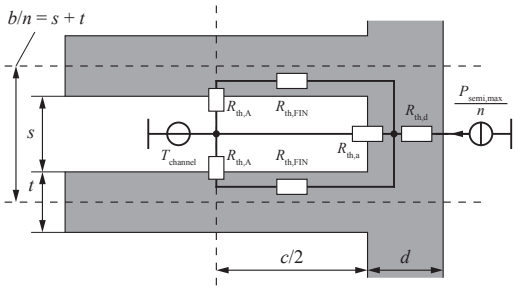


Figure 2.23: Equivalent thermal network model of a single heat sink air-channel.

Table 2.8: Optimized heat sink specification.

$R_{\mathrm{th,hs}}$	CSPI
$0.27\,\mathrm{K/W@}\vartheta = 25\,^{\circ}\mathrm{C}$	$13.5\,\mathrm{W/(K \cdot dm^3)}$

current source as shown in **Figure 2.25(b)**. The input currents for the resistors are controlled in order to give the total power of $P_{\mathrm{tot}} = 501.3\,\mathrm{W}$ to the heat sink unit. It can be seen from the thermal image of the heat sink unit under load in **Figure 2.26** that the temperature rise on the surface of the heat sink is not isotropically distributed. For comparison with the calculated result, the maximum temperature on the heat sink surface $T_{\mathrm{hs,max}}$ is measured and used to calculate the maximum thermal resistance $R_{\mathrm{th,hs,max}}$ of the heat sink unit as

$$R_{\mathrm{th,hs,max}} = \frac{T_{\mathrm{hs,max}} - T_{\mathrm{amb}}}{P_{\mathrm{tot}}}. \tag{2.69}$$

The measurement result is summarized in **Table 2.9**. It is confirmed that the heat sink design model is accurate enough to be used as a practical heat sink design procedure.

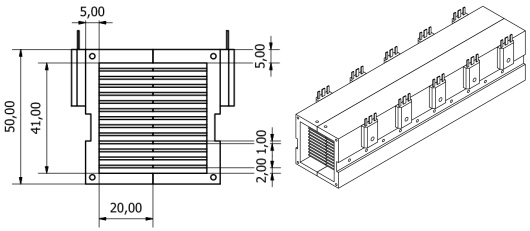


Figure 2.24: Optimized heat sink unit employing fans of type SanAce 9GA0424P3J001 with $b = 40\,\text{mm}$, $d = 5\,\text{mm}$, $L_{\text{hs}} = 220\,\text{mm}$, $n = 14$ and $t = 1\,\text{mm}$, (a) dimension of cross section and (b) entire heat sink unit.

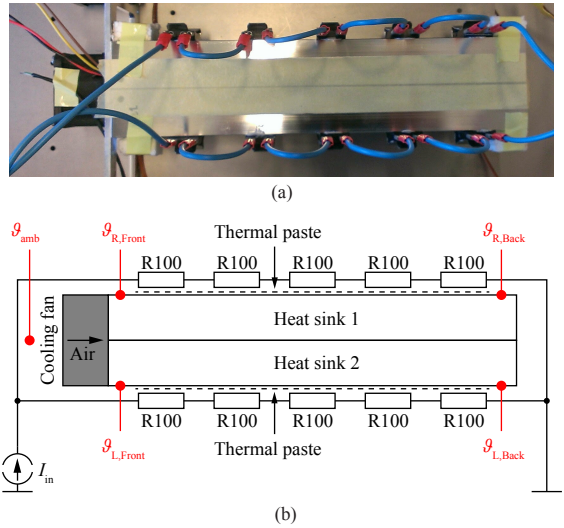
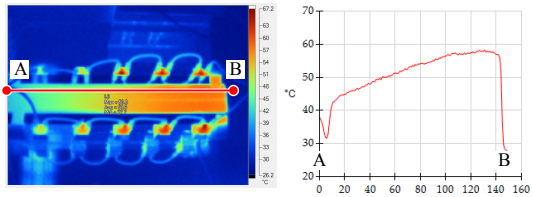


Figure 2.25: Experimental set-up of optimized heat sink unit, (a) position of heating resistors and temperature measurement points, (b) circuit schematic of heating resistors.



(a) (b)

Figure 2.26: Thermal image of the heat sink unit under a load of 500 W (a) and surface temperature profile between points A and B (b).

Table 2.9: Measurement result of heat sink unit.

ϑ_{amb}	$\vartheta_{\mathrm{hs,max}}$	P_{tot}	$R_{\mathrm{th,hs,max}}$
25 °C	97.7 °C	501.3 W	0.29 K/W

2.3 Power consumption in auxiliary circuits

The power demands of auxiliary circuits, such as gate drivers, Digital Signal Processors (DSPs), Field-Programmable Gate Arrays (FPGAs), and current sensors, are also part of the total losses of the converter system. Typically, auxiliary circuits' power demands are neglected due to their relatively low contributions compared to other power components (e.g. power semiconductors or boost inductors). However, after optimizing those power components in order to minimize losses, the contribution of the auxiliary circuits to the total losses is relatively increased, and is no longer negligible.

In this thesis, the designs of the auxiliary circuits used in the UPS system are fixed in advance. This is possible since the topology of the main power circuits and control schemes are fixed already. The total power consumption of the designed auxiliary circuits $P_{\mathrm{aux,tot}}$ is directly measured and included into the optimization results.

2.4 Conclusion

A detailed loss calculation model for the power semiconductors and a heat sink optimization model were discussed in this chapter. As both the conduction and switching losses of power semiconductors are temperature-dependent, an electro-thermal coupled model is required to calculate the losses accurately. Since power semiconductors typically make a large contribution to the total losses, suitable combinations of IGBTs and diodes for minimizing the total losses were investigated. As a result, it has been determined that combining Si RB-IGBTs with SiC SBDs is most suitable for input-side rectifiers in a wide range of switching frequencies, and combining Si IGBTs with SiC SBDs is suitable for output-side inverters that operate at higher switching frequencies, i.e., higher than 8 kHz.

The total boxed volume of the cooling system is the main contribution to the total volume of the active components. In order to increase the power density of the converter system, it is important to minimize the volume of the cooling system by keeping the thermal resistance low. In other words, increasing the CSPI of the heat sink will help achieve high power density. From this point of view, the heat sinks are configured in a double-sided heat sink unit. The optimized heat sink design has been realized and the high CSPI of 13.5 $\mathrm{W/(K \cdot dm^3)}$ was confirmed by experimental measurement.

The total losses of the semiconductors, cooling system, and auxiliary circuits ($P_{\mathrm{semi,tot}} + P_{\mathrm{cs,tot}} + P_{\mathrm{aux,tot}}$) are considered as the total losses of the active components. The total volume of the cooling system $V_{\mathrm{cs,tot}}$ is considered as the total volume of the active components for the system-level optimization.

Chapter 3

Modeling losses and volumes of passive components

This chapter describes the modeling of the losses and volumes of the passive components, such as the differential-mode (DM) and common-mode (CM) inductors and capacitors. An accurate DM inductor model with a reluctance model and winding loss model that considers high frequency (HF) winding loss effects, such as the skin effect and the proximity effect, are described in detail and modeled in [30] by the mirroring approach. Thus, the main contribution of this thesis for the inductor model is the thermal model of the DM inductor and its experimental evaluation. Therefore, in this chapter, the thermal model of the DM inductor will be described in detail. These coupled electro-magnetic and electro-thermal models are essential for accurately estimating the losses and volumes with the inductor model. For the CM inductor, a detailed design model that considers the effects of the leakage inductance, winding / core losses, and a simple thermal model is described in [31] and employed. Since the contribution of the capacitor's loss to the total losses is negligible, only the volume model is considered for the capacitors. At the end, the losses in the damping resistors and the PCB tracks are briefly discussed and a simple loss calculation model for the damping resistor and PCB tracks is described.

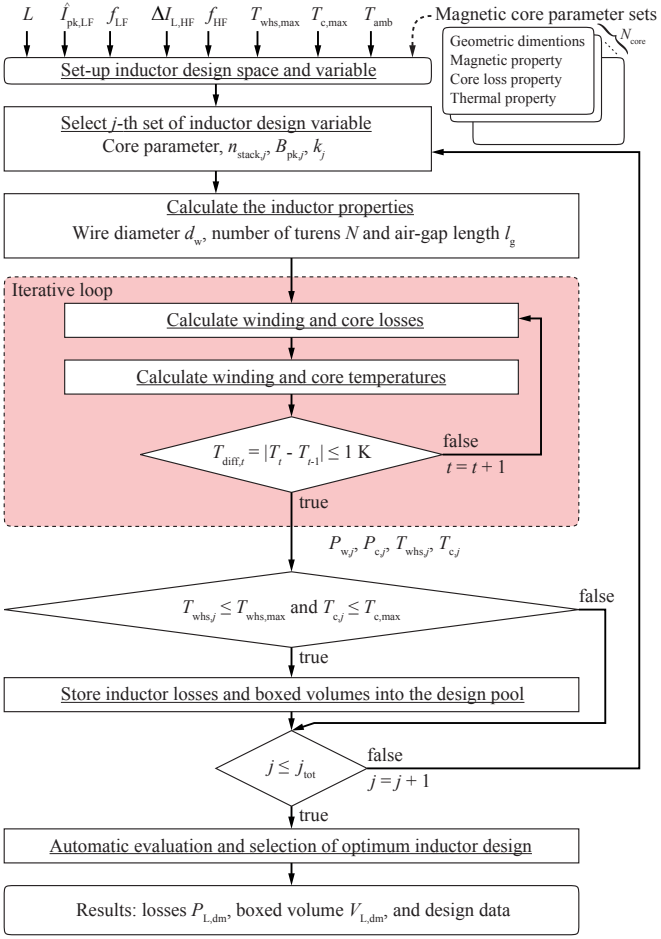


Figure 3.1: Flow chart of the DM inductor design procedure.

3.1 Differential-mode inductor

3.1.1 Procedure overview and loss model

The calculation of the inductor losses is implemented according to the flow chart depicted in **Figure 3.1**. The proposed procedure requires the specifications listed below:

- The inductance value L;
- the amplitude $\hat{I}_{\mathrm{pk,LF}}$ of the current fundamental and the mains frequency f_{LF};
- the maximum peak-to-peak inductor current ripple $\Delta I_{\mathrm{L,HF}}$ and the switching frequency f_{HF};
- the maximum allowed winding hot-spot and core temperatures, $T_{\mathrm{whs,max}}$ and $T_{\mathrm{c,max}}$, and the ambient air temperature T_{amb}.[1]

The implemented automatic inductor design procedure is based on a high number of different inductor designs and the automatic evaluation of the resulting local ρ–η Pareto front similar to the converter optimization procedure. The first step is to create the inductor Design Space. The considered inductor design variables are:

- Core material and geometry (selected from a predefined list of available magnetic cores);
- number of stacked cores n_{stack} ($n = 1$, 2, or 3);
- peak flux density B_{pk} (50% B_{sat} to 100% B_{sat} with a step size of 10%);
- filling factor k (50% to 100% with a step size of 10%).

The procedure starts with selecting the first set of design parameters from the inductor Design Space and calculates those inductor properties that can be directly calculated, such as the wire diameter, the number of turns, and the air gap length. In the next step, the procedure calculates the winding and core losses. The winding losses are separated into low (mains) frequency and high (switching) frequency losses. The low frequency losses are calculated with the DC resistance and the calculation of the high frequency losses is based on the mirroring method detailed in [30]. The inductor design considers two types of conductors, i.e. solid copper wire and high frequency litz wire. The core losses are calculated based on the improved Generalized Steinmetz Equations (iGSE) [32]. The winding and core losses, however, depend on the winding and core temperatures, which are determined using the thermal model discussed

[1] T_{amb} is the absolute ambient air temperature, i.e., $T_{\mathrm{amb}} = \vartheta_{\mathrm{amb}} + 273.15\,\mathrm{K}$. The same representation is applied for the other temperatures.

in the next Subsection. The winding and core losses and temperatures are calculated in an iterative loop according to **Figure 3.1**. This loop is repeated until all differences between previous and current calculated temperatures fall below 1 K. The losses and volumes resulting for both types of wires are evaluated with respect to the maximum allowable winding hot-spot and core temperatures (T_{whs} and T_{c}, respectively). The design results for all successful inductor designs (hot-spot temperature less than specified maximums) are stored in the pool of inductor design results. Thereafter, the design procedure selects the next set of design parameters and conducts the next inductor design. After processing the complete inductor Design Space, the results available in the pool of inductor design results are analyzed in order to determine the optimal inductor according to the following procedure:

1. The inductor in the pool with minimum boxed volume, $V_{\mathrm{L,min}} = \min(V_{\mathrm{L},j})$, is identified;

2. the inductor designs with $V_{\mathrm{L},j} > 1.2 \times V_{\mathrm{L,min}}$ are removed from the pool;

3. the inductor design with minimum losses in the remaining pool of inductor design results constitutes the considered optimal choice.

The losses of the inductors contribute relatively little to the total losses, therefore, a major optimization criterion is maximum power density. Very compact inductor designs, however, yield comparably high losses. A considerable loss reduction is achieved if a somewhat higher boxed volume is allowable, which is taken into account by the procedure given above. The total losses $P_{\mathrm{L,dm}}$ and the total boxed volume $V_{\mathrm{L,dm}}$ of the selected DM inductor resulting at the end of the procedure are used for the system-level optimization.

For DM inductors, the inductor design procedure considers E-core shapes and four different magnetic materials (*nanocrystalline*, *amorphous*, *ferrite*, and *iron powder*, cf. **Table 3.1**) with different magnetic properties, in particular different saturation flux densities (B_{sat}) and operating core temperatures ($\vartheta_{\mathrm{c,max}}$). **Table 3.2** shows the Steinmetz parameters of the magnetic materials. N.B.: Inductors using tape wound cores made of *amorphous* or *nanocrystalline* magnetic materials are subject to increased core losses in the presence of orthogonal components of the magnetic flux density, i.e., if the direction of the magnetic flux density vector is not aligned to the magnetic direction

Table 3.1: Magnetic materials for optimization.

Name	μ_r	B_sat	$\vartheta_\mathrm{c,max}$
EPCOS N87 (*Ferrite*)	2200	0.25 T	120 °C
Magnetics Kool-Mu (*Iron powder*)	26 ... 90	0.9 ... 1.0 T	100 °C
Metglas 2605SA1 (*Amorphous*)	45000	1.5 T	150 °C
Finemet FT-3M (*Nanocrystalline*)	70000	1.23 T	150 °C

Table 3.2: Steinmetz parameters of magnetic materials.

Name	Loss coefficient k [mW/m^3]	Frequency (Hz) power α	Flux density (T) power β
EPCOS N87	78.6	1.72	2.74
Magnetics Kool-Mu 26u, 40u	5002.4	1.46	2.09
Magnetics Kool-Mu 60u, 90u	26035	1.29	2.01
Metglas 2605SA1	1377.3	1.51	1.74
Finemet FT-3M	110.8	1.62	1.98

of the magnetic material, which particularly happens close to the inductor's air gap [33, 34, 21]. Currently, there is no loss model known to the author that accurately takes this effect into account. In order to still consider the expected increase in the core losses due to this effect, the core losses are multiplied by a correction factor $k_\mathrm{Pc} = 2$, which has been determined based on the results of [33].

3.1.2 Thermal model

The thermal model is implemented on the basis of [35] and estimates the hot-spot temperature inside the winding (T_whs), the temperature inside the core (T_c), the surface temperature of the winding (T_ws), and the surface temperature of the core (T_cs). It considers three different heat transfer mechanisms, i.e. *conduction*, *convection* and *radiation*. The thermal resistance network of [35] is extended by three additional thermal resistances in order to determine T_c and to consider the heat transfer from the inductor to the metal base plate on which the inductor is mounted. **Figure 3.2** depicts the resulting thermal model. The thermal resistances $R_\mathrm{th,whs}$, $R_\mathrm{th,wc}$, $R_\mathrm{th,wa}$, and $R_\mathrm{th,ca}$ are calculated according to [35].

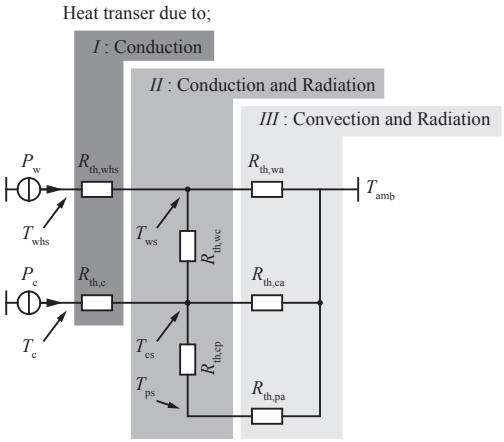


Figure 3.2: Extended thermal network of the inductor. P_w and P_c denote the total winding losses and the core losses, respectively. T_whs and T_c denote the hot-spot winding temperature and the temperature inside the core. T_ws, T_cs and T_ps are the surface temperatures of the winding, the core and the metal base plate, respectively. The base plate is considered only for the evaluation of the inductor model and it is neglected in the converter optimization in order to keep some safety margin for the inductor design.

The calculation of the temperature inside the core, T_c, assumes a constant temperature along the core legs' center lines (cf. **Figure 3.3(a)**). Thus, the additional resistance $R_\mathrm{th,c}$ represents the thermal resistance between the core legs' center lines and the core surface and is expressed as

$$\frac{1}{R_\mathrm{th,c}} = \frac{1}{R_\mathrm{th,c,xy}} + \frac{1}{R_\mathrm{th,c,z}}, \tag{3.1}$$

$$R_\mathrm{th,c,xy} = \frac{l_\mathrm{c}}{\lambda_\mathrm{c,xy} A_\mathrm{c,xy}}, \tag{3.2}$$

$$R_\mathrm{th,c,z} = \frac{d_\mathrm{c}/2}{\lambda_\mathrm{c,z} A_\mathrm{c,z}}, \tag{3.3}$$

where l_c is an effective thermal distance, $\lambda_\mathrm{c,xy}$ and $\lambda_\mathrm{c,z}$ are the direction-dependent effective thermal conductivities of the core (cf. **Figure 3.3(a)** regarding the x-, y-, and z-directions), $A_\mathrm{c,xy}$ denotes the

Table 3.3: Thermal properties of the core materials.

Material	$\lambda_{c,xy}$	$\lambda_{c,z}$
Ferrite	$4.18\,\mathrm{W/(m\cdot K)}$	$4.18\,\mathrm{W/(m\cdot K)}$
Iron powder	$8\,\mathrm{W/(m\cdot K)}$	$8\,\mathrm{W/(m\cdot K)}$
Amorphous	$7.65\,\mathrm{W/(m\cdot K)}$	$9\,\mathrm{W/(m\cdot K)}$
Nanocrystalline	$7.65\,\mathrm{W/(m\cdot K)}$	$9\,\mathrm{W/(m\cdot K)}$

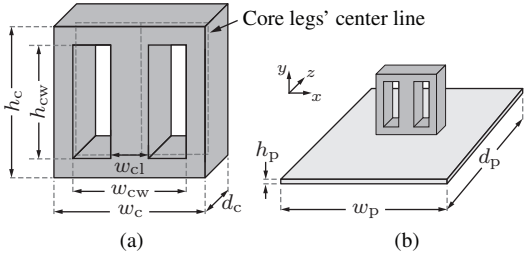


Figure 3.3: Simplified core dimensions (a) and base plate dimensions (b).

total surface area of the core in the x- and y-directions (top, bottom, and both sides; $A_{c,xy}$ also includes the surface areas inside the core windows), and $A_{c,z}$ is the surface area of the core in the z-direction (front and back). These parameters can be calculated using the core dimensions shown in **Figure 3.3(a)**:

$$l_c = \frac{w_c - w_{cw}}{4}, \tag{3.4}$$

$$A_{c,xy} = 2\left\{(h_c + w_c) + (h_{cw} + w_{cw} - w_{cl})\right\} d_c, \tag{3.5}$$

$$A_{c,z} = 2\left\{h_c w_c - h_{cw}(\, w_{cw} - w_{cl}\,)\right\}. \tag{3.6}$$

The thermal conductivities of the core materials are given in **Table 3.3**.

The second additional resistance, $R_{th,cp}$, represents the thermal resistance between the core and the base plate due to the combination of

conduction and *radiation*. It is expressed as

$$\frac{1}{R_{\mathrm{th,cp}}} = \frac{1}{R_{\mathrm{th,cond,cp}}} + \frac{1}{R_{\mathrm{th,rad,cp}}}, \tag{3.7}$$

$$R_{\mathrm{th,cond,cp}} = \frac{l_{\mathrm{eg}}}{\lambda_{\mathrm{air}} A_{\mathrm{cp}}}, \tag{3.8}$$

$$R_{\mathrm{th,rad,cp}} = \frac{1}{h_{\mathrm{rad,cp}} A_{\mathrm{cp}}} = \frac{T_{\mathrm{cs}} - T_{\mathrm{ps}}}{\epsilon_{\mathrm{cs}} \sigma \left(T_{\mathrm{cs}}^4 - T_{\mathrm{ps}}^4\right) A_{\mathrm{cp}}}. \tag{3.9}$$

An effective air gap length of $l_{\mathrm{eg}} = 0.2\,\mathrm{mm}$ between the core surface and the base plate top surface is found to yield reasonably accurate and reproducible results for all inductors measured with the test set-up detailed in a next Subsection. [2] Moreover, $\lambda_{\mathrm{air}} = 0.03\,\mathrm{W/(m \cdot K)}$ is the thermal conductivity of air at 80 °C, $A_{\mathrm{cp}} = w_{\mathrm{c}} d_{\mathrm{c}}$ is the contact area of the core and the base plate, $\epsilon_c = 0.9$ is the assumed emissivity of the core surface, and σ is the Stefan–Boltzmann constant [$= 5.67 \times 10^{-8}\,\mathrm{W/(m^2K^4)}$] [35].

The last additional resistance, $R_{\mathrm{th,pa}}$, represents the thermal resistance between the surface of the base plate and the ambient air and considers heat flux due to *convection* and *radiation*. The dimensions of the base plate are depicted in **Figure 3.3(b)** and the expressions for calculating $R_{\mathrm{th,pa}}$ are given in [35]. Further parameters are: the assumed emissivity of the base plate surface, $\epsilon_{\mathrm{p}} = 0.04$ (aluminum, polished), the total open surface area of the base plate, $A_{\mathrm{pa}} = 2\{w_{\mathrm{p}} d_{\mathrm{p}} + (w_{\mathrm{p}} + d_{\mathrm{p}})\} - A_{\mathrm{cp}}$, and the total distance passed by the air that cools the base plate, $L = d_{\mathrm{p}} + h_{\mathrm{p}}$.

3.1.3 Experimental evaluation of DM inductor model parameters

In order to evaluate the accuracy of the inductor model, i.e., the accuracies of the calculated losses and temperatures, the inductor's total losses and core and winding temperatures have been measured. The inductor test set-up and a test inductor were built as shown in **Figure 3.4**. The inductor test set-up contains an aluminum base plate

[2] Experimental results confirm the existence of a non-zero value of $R_{\mathrm{th,cp}}$, however, the exact value of the equivalent air gap length, l_{eg}, is difficult to determine and may vary depending on the inductor core and the set-up.

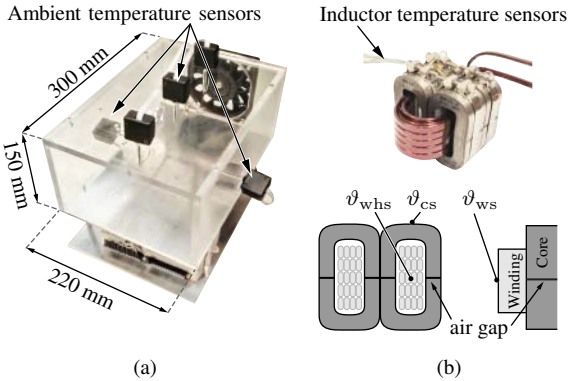


Figure 3.4: (a) Inductor test set-up with ambient air temperature sensors and air-speed sensors; (b) test inductor.

Table 3.4: Test inductor design parameters.

Core material	Metglas 2605SA1 *Amorphous*
Core size	AMCC06R3 (2 sets × 2 stacked)
Air gap width	2 × 0.5 mm
Number of turns	20 turns (5 turns × 4 layers)
R_{dc} of wire	≈ 7.8 mΩ (at 25 °C)

(dimensions: 220 mm × 300 mm × 5 mm), which supports a duct made of acrylic glass; the data logger used to process the measurement results is located below the base plate of the duct. The back side of the duct shown in **Figure 3.4** is terminated with a fan that can be used to control the air flow inside the duct. The test set-up is equipped with K-type thermocouples and air speed sensors to measure ϑ_{amb} and the air speeds at different locations inside the duct, respectively. The test inductor, shown in **Table 3.4**, employs *amorphous* core material and solid copper wire and is equipped with thermocouples, located inside the winding, at the surface of the winding, and at the surface of the core, in order to measure ϑ_{whs}, ϑ_{ws}, and ϑ_{cs} (cf. **Figure 3.4(b)**).

The inductor losses were simultaneously measured with a calorimeter and a power analyzer for a low frequency (LF) sinusoidal current with a superimposed triangular high frequency (HF) AC current. The test conditions are specified in **Table 3.5**.

Figure 3.5 compares the obtained measured and calculated induc-

Table 3.5: Test current conditions.

HF component (peak-to-peak)	$\Delta I_{\mathrm{L,HF}} = 9.5\,\mathrm{A}$
	$f_{\mathrm{HF}} = 16\,\mathrm{kHz}$
LF component	$\hat{I}_{\mathrm{pk,LF}} = 0, 20, 48\,\mathrm{A}$
	$f_{\mathrm{LF}} = 50\,\mathrm{Hz}$

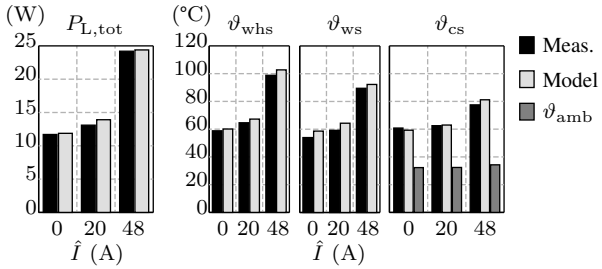


Figure 3.5: Comparison of measured and calculated inductor losses and temperatures. Measurement results are shown by black bars (Meas.) and calculation results are shown by light gray bars (Model). Ambient temperatures are shown by dark gray bars ($\vartheta_{\mathrm{amb}} \approx 33\,^{\circ}\mathrm{C}$ inside the closed box of the calorimeter).

tor losses and temperatures. A good agreement between the measured and calculated results for all considered operating points (losses and temperatures) is obtained if the core loss correction factor is reduced to $k_{\mathrm{Pc}} = 1.65$ (instead of $k_{\mathrm{Pc}} = 2$, cf. **Subsection 3.1.1**): [3] The relative error for all considered total losses and winding hot-spot temperatures is less than 10 %.

3.2 Three-phase common-mode inductor

In this thesis, a three-phase CM inductor is designed based on the design model introduced in [31]. A modeling procedure overview and few important equations from [31] for calculating the losses and temperature rise of a CM inductor are summarized in this section.

[3] The value of k_{Pc} is expected to depend on the air gap length and is, therefore, not expected to be constant. For this reason, the optimization results presented in **Chapter 5** are still based on $k_{\mathrm{Pc}} = 2$ to avoid unrealistic inductor designs.

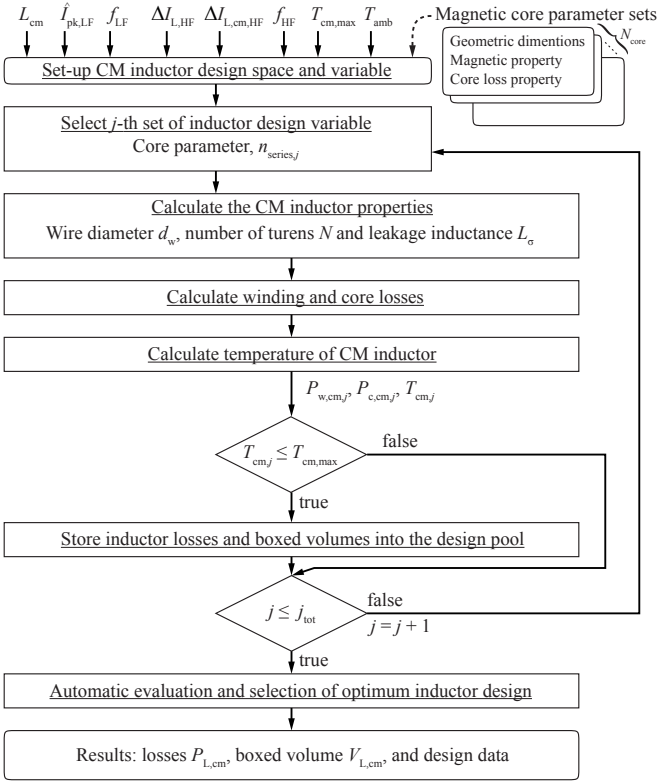


Figure 3.6: Flow chart of the CM inductor design procedure.

3.2.1 Procedure overview

A flow chart of the CM inductor modeling procedure is depicted in **Figure 3.6**. The proposed procedure requires the specifications listed below:

- The CM inductance value L_{cm};
- the fundamental DM current amplitude $\hat{I}_{\mathrm{pk,LF}}$ and mains frequency f_{LF};
- the high frequency DM peak-to-peak current ripple $\Delta I_{\mathrm{L,HF}}$, the CM peak-to-peak current ripple $\Delta I_{\mathrm{L,cm,HF}}$ and the switching frequency f_{HF};

Table 3.6: Properties of VITROPERM 500F.

Name	μ_r	B_{sat}	$\vartheta_{c,max}$
VITROPERM 500F (*Nanocrystalline*)	40000 ($f = 0\,\text{Hz}$)	1.2 T	120 °C

Table 3.7: Steinmetz parameters of VITROPERM 500F.

Name	Loss coefficient k [mW/m^3]	Frequency (Hz) power α	Flux density (T) power β
VITROPERM 500F	2.5	1.88	2.02

- the maximum allowed CM inductor temperature $T_{cm,max}$ and the ambient air temperature T_{amb}.

The first step is to create the CM inductor Design Space. In this thesis, a toroidal shape core with nanocrystalline (VITROPERM 500F [36]) material is chosen for the CM inductor design. The magnetic properties and maximum operating temperature of VITROPERM 500F are shown in **Table 3.6**. The Steinmetz parameters are shown in **Table 3.7**. The considered CM inductor design variables are:

- core size (selected from a predefined list of available magnetic toroidal cores);
- number of series connected CM inductors n_{series} ($n = 1$, 2 or 3).

The procedure starts with selecting the first set of design parameters from the CM inductor Design Space. In the first step, the inductor properties such as the wire diameter d_w, the number of turns N, and the leakage inductance L_σ are calculated. Here, a single layer configuration with round wire is considered for the CM inductor winding configuration. The number of turns can be defined as a function of the frequency f, the CM inductance L_{cm}, the real part μ' of the complex permeability $\bar{\mu}$, and the inductance per turn A_L of the core, by

$$N(f) = \text{sail}\left(\sqrt{\frac{L_{cm}}{A_L} \cdot \frac{|\bar{\mu}(f = 0\,\text{Hz})|}{\mu'(f)}}\right). \tag{3.10}$$

The equation for the leakage inductance derived in [31] gives

$$L_\sigma \cong 2.5\mu_0 N^2 \frac{A_\mathrm{e}}{l_\mathrm{eff}} \left(\frac{l_\mathrm{e}}{2} \sqrt{\frac{\pi}{A_\mathrm{e}}} \right)^{1.45}, \tag{3.11}$$

where μ_0 is the permeability of free space, A_e is the effective cross-sectional area, l_e is the mean path length of the toroidal core, and l_eff is the effective mean path length of the leakage magnetic field. The equation for l_eff is given in [31] as

$$l_\mathrm{eff} = l_\mathrm{e} \sqrt{\frac{\theta}{2\pi}} + \frac{1}{\pi} \sin \frac{\theta}{2}, \tag{3.12}$$

where θ is the angle of the winding per phase and this equation is valid for $\theta > \pi/6$. In this thesis, $\theta = 5\pi/9\,\mathrm{rad} = 100\,^\circ$ is selected.

In the next step, the flux density values due to the HF CM current $\Delta I_\mathrm{L,cm,HF}$, the HF DM current $\Delta I_\mathrm{L,HF}$, and the LF DM current $\hat{I}_\mathrm{L,LF}$ are calculated in order to check for local and global magnetic core saturation. To avoid magnetic core saturation, the following condition should always be satisfied:

$$B_\mathrm{tot} = B_\mathrm{cm,HF} + B_\mathrm{dm,HF} + B_\mathrm{dm,LF} < B_\mathrm{sat}; \tag{3.13}$$

$$B_\mathrm{cm,HF} = \frac{L_\mathrm{cm}}{N \cdot A_\mathrm{e}} \cdot \frac{\Delta I_\mathrm{L,cm,HF}}{2}, \tag{3.14}$$

$$B_\mathrm{dm,HF} = \frac{L_\sigma}{N \cdot A_\mathrm{e}} \cdot \frac{\Delta I_\mathrm{L,HF}}{2}, \tag{3.15}$$

$$B_\mathrm{dm,LF} = \frac{L_\sigma}{N \cdot A_\mathrm{e}} \cdot \hat{I}_\mathrm{L,LF}. \tag{3.16}$$

If the total flux density B_tot exceeds the flux density saturation limit B_sat, the current CM design is discarded and the design procedure is iterated with a next set of design parameters.

When the total flux density is smaller than the saturation limit, the design procedure calculates the winding losses $P_\mathrm{w,cm}$ and the core losses $P_\mathrm{c,cm}$ based on the equations derived in [31]. The total of the losses of the CM inductor is given as

$$P_\mathrm{L,cm} = P_\mathrm{w,cm} + P_\mathrm{c,cm}. \tag{3.17}$$

The equation for calculating the temperature rise of the toroidal core which is suggested in [37, 38, 39] is defined as

$$\Delta T_\mathrm{L,cm} = \left(\frac{P_\mathrm{L,cm}}{A_\mathrm{L,cm}} \right)^{0.833}, \tag{3.18}$$

Table 3.8: Test current conditions.

Type	Name	k_1 [m^3/(F · V^2)]	k_2 [m^3/(F · V)]
Al electrolytic	*EPCOS B43543 series*	3.0×10^{-7}	1.9×10^{-5}
Polypropylene film	*EPCOS B3267X series*	18.1×10^{-7}	5.4×10^{-3}

Type	Name	k_3 [m^3/V]	k_4 [m^3]
Al electrolytic	*EPCOS B43543 series*	6.5×10^{-9}	5.4×10^{-6}
Polypropylene film	*EPCOS B3267X series*	4.8×10^{-9}	1.9×10^{-6}

where $A_{\mathrm{L,cm}}$ is the wound inductor surface area. Thus, the temperature of the CM inductor is given as

$$T_{\mathrm{cm}} = \Delta T_{\mathrm{L,cm}} + T_{\mathrm{amb}}. \tag{3.19}$$

When the temperature T_{cm} exceeds the maximum limit $T_{\mathrm{cm,max}}$, the current CM inductor design is discarded. The design results for all successful CM inductor designs (hot-spot temperature less than specified maximum) are stored in the pool of CM inductor design results. After the iteration loop for the CM inductor Design Space is finished, the most suitable CM inductor design is selected automatically in the same way as was the DM inductor design. At the end, the total losses $P_{\mathrm{L,cm}}$ and the total boxed volume $V_{\mathrm{L,cm}}$ of the selected CM inductor are determined and are in a next step used for the system-level optimization.

3.3 Capacitors

The calculation of the capacitor's volume is based on the parametrized mathematical model which is discussed in [4]. The estimated total volume of the capacitor V_{cap} can be modeled using its rated voltage V_{dc}, capacitance value C, and four fitting factors k_1, k_2, k_3, k_4, as

$$V_{\mathrm{cap}}\,[\mathrm{m}^3] = k_1 \cdot C \cdot V_{\mathrm{dc}}^2 + k_2 \cdot C \cdot V_{\mathrm{dc}} + k_3 \cdot V_{\mathrm{dc}} + k_4. \tag{3.20}$$

The fitting factors for different types of capacitors are determined in [4] and summarized in **Table 3.8**. A film capacitor *EPCOS B3267X series* with a rated voltage of 450 V is selected and used for optimization and hardware realization.

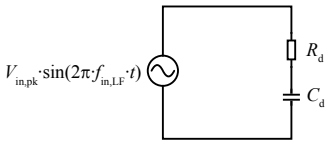


Figure 3.7: Equivalent circuit of R-C parallel damping for single phase.

3.4 Resistive components

3.4.1 Damping resistors

Two different damping resistors are employed, one in the EMI input filter, which has an R-C parallel damping structure, and the other in the output filter, which has an R-L parallel damping structure, as discussed in **Chapter 4**. Since the resistive losses of R-L parallel damping are negligible, only the resistive losses of R-C parallel damping are considered.

Figure 3.7 shows the equivalent circuit used to calculate the losses of the damping resistor. It is assumed that the main contribution to the losses comes from the low-frequency component of the input voltage source, thus, the resistive loss of the C-R parallel damping circuit is

$$P_{\text{R,damp}} = R_{\text{d}} \cdot \frac{I^2_{\text{Rd,pk,LF}}}{2}, \tag{3.21}$$

$$I_{\text{Rd,pk,LF}} = \frac{V_{\text{in,pk}}}{\sqrt{R_{\text{d}}^2 + \left(\frac{1}{2\pi \cdot f_{\text{in,LF}} \cdot C_{\text{d}}}\right)^2}}. \tag{3.22}$$

3.4.2 Resistance of PCB traces

The EMI input filter, the output filter, and the power unit are typically realized as separated Printed Circuit Boards (PCBs) and connected by wires. Usually, the PCB traces have higher resistances than the wires, due to their lower thickness. Thus, the thickness, width, and total length of the PCB traces should be large, wide, and short enough to reduce resistive losses in the traces and avoid overheating. Especially converter systems which handle high current could have a considerable amount of resistive losses in the PCBs. The total resistances of the PCB

traces could be analytically calculated if the PCB design is already fixed. The averaged resistance R_{pcb} of a PCB trace is calculated as

$$R_{\mathrm{pcb}} = \rho_{\mathrm{Cu}} \cdot \frac{l_{\mathrm{pcb}}}{t_{\mathrm{pcb}} \cdot w_{\mathrm{pcb}}}, \tag{3.23}$$

where $\rho_{\mathrm{Cu}} = 16.8\,[\mathrm{n}\Omega \cdot \mathrm{m}]$ is the resistivity of copper at $20\,^{\circ}\mathrm{C}$, l_{pcb} is the total length of the traces, t_{pcb} is the thickness of the traces, and w_{pcb} is the averaged width of the traces. Once the resistances of the traces are known, the losses $P_{\mathrm{R,pcb}}$ in the traces can be calculated as

$$P_{\mathrm{R,pcb}} = R_{\mathrm{pcb}} \cdot \frac{\hat{I}_{\mathrm{ac}}^2}{2}, \tag{3.24}$$

where $\hat{I}_{\mathrm{ac}}$ is the amplitude of the phase current fundamental. However, it is difficult to estimate the total length of the traces before the PCB design is determined. Therefore, in this thesis, R_{pcb} is directly measured on the realized PCBs and then the losses in the PCB, $P_{\mathrm{R,pcb}}$, are calculated based on the measured R_{pcb}.

3.5 Conclusion

This chapter has discussed the modeling procedure for the passive components. It also described a simple volume estimation model for the capacitors and a loss estimation model for the damping resistors. In particular, it presented a detailed thermal model of the DM inductors and evaluated this with experimental measurements. The modeling of the magnetic component is relatively complicated due to its electromagnetic, and coupled electro-thermal and magneto-thermal behavior. Such multi-domain behavior has to be considered and modeled in order to accurately calculate the losses and volumes of the magnetic components. The significant improvement of active components, i.e., power semiconductors, over the last decades concerning losses means that the contributions of the passive components' losses to the total system losses become more visible. Also, because the passive components, especially the inductors and capacitors, account for most of the volume of the converter system, accurate models for the passive component losses and volumes are vitally important for system-level optimization.

The total losses of the DM inductors, CM inductors, damping resistors, and PCB traces ($P_{\mathrm{L,dm}} + P_{\mathrm{L,cm}} + P_{\mathrm{R,damp}} + P_{\mathrm{R,pcb}}$) are considered

as the total losses of passive components, and the total of the volumes of the DM inductors, CM inductors and capacitors ($V_{\mathrm{L,dm}} + V_{\mathrm{L,cm}} + V_{\mathrm{cap}}$) is considered as the total volume of the passive components for the system-level optimization.

Chapter 4

Filter design procedure

Typically, an LC low-pass filter is connected on the input / output side of a UPS system to reduce the high-frequency harmonics of the switched voltage and to obtain a smooth voltage / current output. In addition, a power supply system which is connected to the mains at the input side must meet the Electro Magnetic Interference (EMI) standards, such as defined by CISPR [40, 41]. Recently, multi-stage LC filters have been discussed as a better option for reducing the total filter volume. In particular, the advantages of a two-stage input filter are discussed in detail in [42], where an analytical design approach (called *Design Space*) is introduced. The advantages of a two-stage filter compared with a traditional single-stage realization are:

- Higher EMI noise attenuation for same filter volume;
- Higher control dynamics.

Six specifications are defined and used as the design criteria for the design of the EMI input filter, the AC output filter, and the DC-port filter in this work. The considered design criteria of each filter are summarized in **Table 4.1**. The high-frequency (HF) current ripple at the differential-mode (DM) inductors (on the input or output side) is one of the design variables for the system-level optimization procedure and it defines the inductance value. The HF voltage ripple at the DM input / output capacitors is limited and defines the allowed minimum values of the DM capacitances. The low-frequency (LF) reactive current through the DM filter capacitors is limited in order to achieve a high

Table 4.1: Considered filter design criteria.

Criteria	EMI input filter	Output filter	DC-port filter
HF current ripple $\Delta I_{\mathrm{L,HF}}$	✓	✓	✓
HF voltage ripple $\Delta V_{\mathrm{C,HF}}$	✓	✓	✓
LF reactive current $I_{\mathrm{C,LF}}$	✓	✓	—
Resonance frequency f_{res} of second-stage	✓	✓	—
EMI noise emission level	✓	—	—

Table 4.2: Required specifications for EMI input filter.

Criteria		Required specification
$\Delta I_{\mathrm{L,HF}}$	$=$	$\gamma_{\mathrm{in}} \cdot I_{\mathrm{in,pk}}$
$\Delta V_{\mathrm{C,HF}}$	$\leq$	$0.076 \cdot V_{\mathrm{in,pk}}$
$I_{\mathrm{C,LF}}$	$\leq$	$0.1 \cdot I_{\mathrm{in,pk}}$
f_{res}	$\leq$	$0.7 \cdot f_{\mathrm{in,sw}}$
EMI noise emission level		CISPR 11 Class A

power factor (PF) on the input side or to achieve a high active output power on the output side. These criteria define the maximum allowed DM capacitance value. The HF resonance frequency of the second filter stage is also taken into account in order to avoid a high current at the resonance frequency, which might result in unexpected extra losses or an unstable control. Accordingly, the corner frequency of the second stage LC filter is constrained to be lower than the switching frequency; as a result, the minimum allowed DM capacitance value is also limited by this criterion. The EMI noise emission level is limited only on the input side. The DM capacitance value is adjusted within the range defined by the limits mentioned above. The CM inductance / capacitance values will be freely designed in order to meet the EMI requirement.

In this chapter, the Design Space approach is employed for designing the input / output filter and the detailed design procedure of the filter for meeting all the required specifications will be discussed in detail.

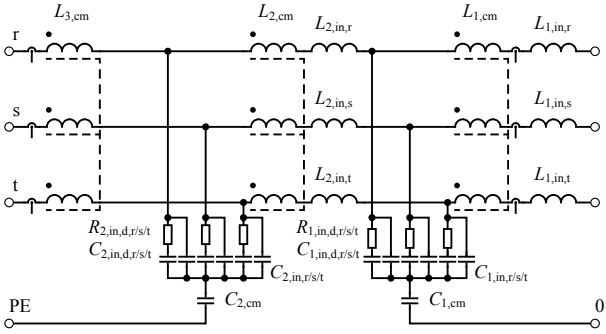


Figure 4.1: EMI input filter circuit structure.

4.1 Design of two-stage EMI input filter

Figure 4.1 depicts a full schematic of the two-stage DM and CM EMI input filter. R-C damping circuits are provided for each filter stage and a further CM choke is arranged on the mains side. The basic configuration of the EMI input filter is discussed in [43] for a three-phase three-level PWM rectifier system. The DM inductance / capacitance values of the second stage, $L_{2,\mathrm{in,r/s/t}}$ / $C_{2,\mathrm{in,r/s/t}}$, are defined from the inductance / capacitance values of the first stage, $L_{1,\mathrm{in,r/s/t}}$ / $C_{1,\mathrm{in,r/s/t}}$, with design constants n and k as shown below:

$$L_{2,\mathrm{in,r/s/t}} = n \cdot L_{1,\mathrm{in,r/s/t}}, \tag{4.1}$$

$$C_{2,\mathrm{in,r/s/t}} = k \cdot C_{1,\mathrm{in,r/s/t}}. \tag{4.2}$$

The two parameters n and k can be freely adjusted between 0 and 1 in order to find an optimal design that minimizes the volume and / or the losses. However, the optimal value of n and k for minimum filter volume is explored in detail in [42] and $n = 0.1$ and $k = 0.9$ are found to be the optimal values and will be used in this thesis.

The required specifications for the EMI input filter are summarized in **Table 4.2**. Here, γ_{in} is the required factor for the current ripple, $V_{\mathrm{in,pk}}$ is the nominal input peak voltage, $I_{\mathrm{in,pk}}$ is the nominal input peak current, V_{dc} is the DC-link voltage, $f_{\mathrm{in,LF}}$ is the fundamental input frequency, and $f_{\mathrm{in,sw}}$ is the operating switching frequency of the input rectifier. The design procedure flow chart of the EMI input filter is shown in **Figure 4.2**. In the first step, the required DM in-

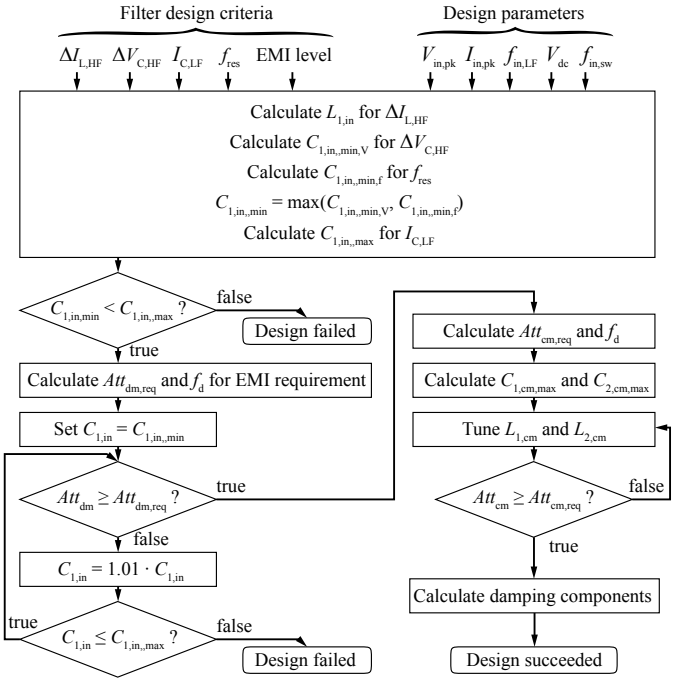


Figure 4.2: Design procedure flow chart for EMI input filter.

ductance value $L_{1,\mathrm{in}}$[1] is calculated, then the maximum / minimum capacitance values $C_{1,\mathrm{in,min}}$ / $C_{1,\mathrm{in,max}}$ are calculated. In the next step, the worst cases for the DM / CM EMI noise emission levels are separately estimated in order to calculate the required DM / CM attenuations $Att_{\mathrm{dm,req}}$ / $Att_{\mathrm{cm,req}}$ at the frequency of interest for the EMI design, which is typically called the design frequency f_{d}. The DM filter attenuation is calculated by sweeping the DM capacitance value within the range of its minimum / maximum limits until the DM attenuation satisfies the requirement. The CM filter attenuation is also calculated by sweeping the CM inductance / capacitance values within the range of their limits until the CM attenuation satisfies the requirement and the volume of the CM inductor is minimized. The local optimization procedure for minimizing the volume of a CM inductor will be discussed

[1]The subscript r/s/t will be omitted for the sake of space in this section.

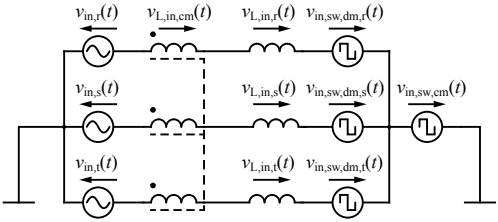


Figure 4.3: Simplified equivalent circuit of the AC side of the input rectifier system.

later. Once suitable LC values which satisfy all required specifications are found within the limits, the design of the EMI input filter is successfully finished, and then the calculated LC values are stored in the design pool. If suitable LC values are not found within the limits, the design is discarded and it will not be considered in the system-level optimization.

4.1.1 Dimensioning of LC values for current and voltage ripple requirement

Figure 4.3 shows a simplified equivalent circuit of the AC side of the input rectifier system. $v_{\mathrm{in,r}}$, $v_{\mathrm{in,s}}$ and $v_{\mathrm{in,t}}$ are input phase voltages which are defined as:

$$v_{\mathrm{in,r}}(t) = V_{\mathrm{in,pk}} \cdot \sin\left(\omega_{\mathrm{in,LF}} \cdot t\right), \tag{4.3}$$

$$v_{\mathrm{in,s}}(t) = V_{\mathrm{in,pk}} \cdot \sin\left(\omega_{\mathrm{in,LF}} \cdot t - \frac{2\pi}{3}\right), \tag{4.4}$$

$$v_{\mathrm{in,t}}(t) = V_{\mathrm{in,pk}} \cdot \sin\left(\omega_{\mathrm{in,LF}} \cdot t - \frac{4\pi}{3}\right). \tag{4.5}$$

Here, $\omega_{\mathrm{in,LF}}$ is the input fundamental angular frequency where

$$\omega_{\mathrm{in,LF}} = 2\pi \cdot f_{\mathrm{in,LF}}. \tag{4.6}$$

$v_{\mathrm{in,sw,r}}$, $v_{\mathrm{in,sw,s}}$, and $v_{\mathrm{in,sw,t}}$ (with $v_{\mathrm{in,sw,r/s/t}} = v_{\mathrm{in,sw,dm,r/s/t}} + v_{\mathrm{in,sw,cm}}$) are the switched voltages of the bridge leg inputs which can be defined

as:

$$v_{\mathrm{in,sw,r}}(t) = \begin{cases} \frac{V_{\mathrm{dc}}}{2} & (m_{\mathrm{in,r}}(t) \geq m_{\mathrm{c,1}}(t)), \\ -\frac{V_{\mathrm{dc}}}{2} & (m_{\mathrm{in,r}}(t) < m_{\mathrm{c,2}}(t)), \\ 0 & \text{otherwise}, \end{cases} \tag{4.7}$$

$$v_{\mathrm{in,sw,s}}(t) = \begin{cases} \frac{V_{\mathrm{dc}}}{2} & (m_{\mathrm{in,s}}(t) \geq m_{\mathrm{c,1}}(t)), \\ -\frac{V_{\mathrm{dc}}}{2} & (m_{\mathrm{in,s}}(t) < m_{\mathrm{c,2}}(t)), \\ 0 & \text{otherwise}, \end{cases} \tag{4.8}$$

$$v_{\mathrm{in,sw,t}}(t) = \begin{cases} \frac{V_{\mathrm{dc}}}{2} & (m_{\mathrm{in,t}}(t) \geq m_{\mathrm{c,1}}(t)), \\ -\frac{V_{\mathrm{dc}}}{2} & (m_{\mathrm{in,t}}(t) < m_{\mathrm{c,2}}(t)), \\ 0 & \text{otherwise}. \end{cases} \tag{4.9}$$

$m_{\mathrm{in,r}}$, $m_{\mathrm{in,s}}$ and $m_{\mathrm{in,t}}$ are the fundamental frequency modulation signals of each phase, where

$$m_{\mathrm{in,r}}(t) = M_{\mathrm{in}} \cdot \sin\left(\omega_{\mathrm{in,LF}} \cdot t + d\Theta\right), \tag{4.10}$$

$$m_{\mathrm{in,s}}(t) = M_{\mathrm{in}} \cdot \sin\left(\omega_{\mathrm{in,LF}} \cdot t - \frac{2\pi}{3} + d\Theta\right), \tag{4.11}$$

$$m_{\mathrm{in,t}}(t) = M_{\mathrm{in}} \cdot \sin\left(\omega_{\mathrm{in,LF}} \cdot t - \frac{4\pi}{3} + d\Theta\right). \tag{4.12}$$

Here, $M_{\mathrm{in}} = 2V_{\mathrm{in,pk}}/V_{\mathrm{dc}}$ is the modulation index on the input side. $d\Theta$ is the required phase difference between the mains voltage and the fundamental component of the pulse width modulated voltage at the input of the switching stage, which is required for the inductance current $i_{\mathrm{L,in}}$ to be in phase with the input voltage for PFC; $d\Theta$ can be calculated as

$$d\Theta = \tan^{-1}\left(\frac{V_{\mathrm{L,in,pk}}}{V_{\mathrm{in,pk}}}\right), \tag{4.13}$$

$$V_{\mathrm{L,in,pk}} = \omega_{\mathrm{in}} \cdot (n+1) L_{1,\mathrm{in}} \cdot I_{\mathrm{in,pk}}. \tag{4.14}$$

Typically, $V_{\mathrm{L,in,pk}} \ll V_{\mathrm{in,pk}}$ is valid, therefore $d\Theta \approx 0$ is considered in the design procedure. The multi-carrier Pulse Width Modulation (PWM) scheme detailed in [23, 24] is employed. $m_{\mathrm{c,1}}$ and $m_{\mathrm{c,2}}$ are

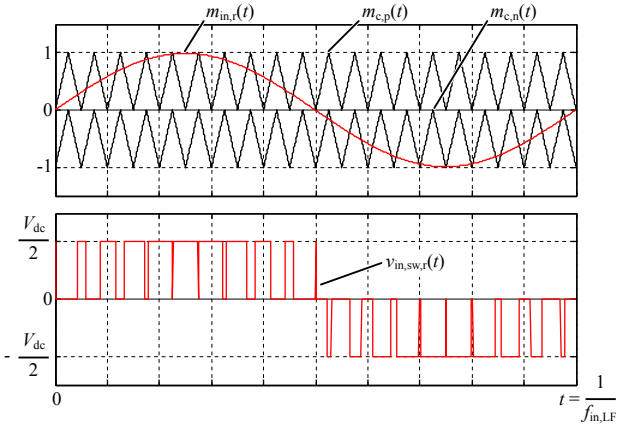


Figure 4.4: Example waveforms of modulation process and resulting switching stage phase voltage $v_{\mathrm{in,sw,r}}$ when $M_{\mathrm{in}} = 1.0$ and $f_{\mathrm{in,sw}} = 20 \cdot f_{\mathrm{in,LF}}$.

triangular PWM carrier signals with switching frequency. $m_{\mathrm{c},1}$ has a positive signal range of 0 to 1, and $m_{\mathrm{c},2}$ has a negative signal range of -1 to 0. Examples of modulation signals and switched voltage waveforms are shown in **Figure 4.4**. $v_{\mathrm{in,sw,cm}}$ is the high frequency CM voltage due to switching (in case of purely sinusoidal PWM no low-frequency component is present in $v_{\mathrm{in,sw,cm}}$),

$$v_{\mathrm{in,sw,cm}}(t) = \frac{v_{\mathrm{in,sw,r}}(t) + v_{\mathrm{in,sw,s}}(t) + v_{\mathrm{in,sw,t}}(t)}{3}. \tag{4.15}$$

Finally, the voltages across the DM inductors ($v_{\mathrm{L,in,r}}$, $v_{\mathrm{L,in,s}}$, and $v_{\mathrm{L,in,t}}$) and the voltage across the CM inductor ($v_{\mathrm{L,in,cm}}$) are calculated as

$$v_{\mathrm{L,in,cm}}(t) = -v_{\mathrm{in,sw,cm}}(t), \tag{4.16}$$
$$v_{\mathrm{L,in,r}}(t) = v_{\mathrm{in,r}}(t) - v_{\mathrm{in,sw,dm,r}}(t), \tag{4.17}$$
$$v_{\mathrm{L,in,s}}(t) = v_{\mathrm{in,s}}(t) - v_{\mathrm{in,sw,dm,s}}(t), \tag{4.18}$$
$$v_{\mathrm{L,in,t}}(t) = v_{\mathrm{in,t}}(t) - v_{\mathrm{in,sw,dm,t}}(t). \tag{4.19}$$

All voltage signals are numerically calculated in MATLAB and used for the filter design.

In order to define the required inductance value $L_{1,\mathrm{in}}$ for the defined maximum current ripple $\Delta I_{\mathrm{L,HF}}$, the maximum difference $\Delta\varphi_{\mathrm{L,in}}$ of the

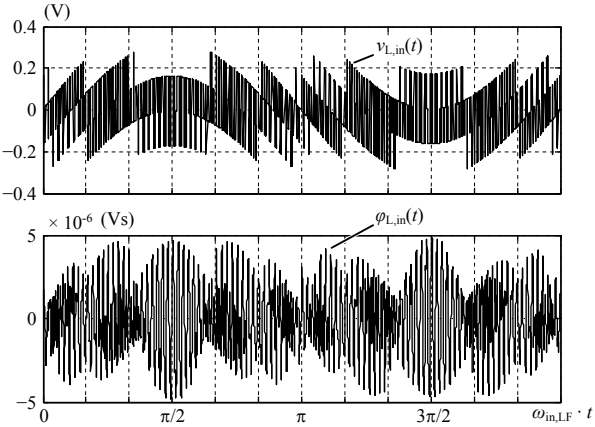


Figure 4.5: Waveform example of DM inductor voltage and voltage-time product with $M_{\mathrm{in}} = 1.0$, $f_{\mathrm{in,LF}} = 50\,\mathrm{Hz}$, $f_{\mathrm{in,sw}}/f_{\mathrm{in,LF}} = 100$, and $V_{\mathrm{dc}} = 1.0\,\mathrm{V}$.

voltage-time product over the DM inductor is calculated as

$$\Delta\varphi_{\mathrm{L,in}} = \max\left(\varphi_{\mathrm{L,in}}(t)\right) - \min\left(\varphi_{\mathrm{L,in}}(t)\right), \tag{4.20}$$

$$\varphi_{\mathrm{L,in}}(t) = \int v_{\mathrm{L,in}}(t) \cdot dt. \tag{4.21}$$

For example, the waveform of the voltage across the DM inductor and the corresponding voltage-time waveform are shown in **Figure 4.5**. The value of $\Delta\varphi_{\mathrm{L,in}}$ depends on the DC-link voltage V_{dc} and the ratio between the fundamental frequency and the switching frequency $f_{\mathrm{in,sw}}/f_{\mathrm{in,LF}}$, but also on the modulation index M_{in}. $\Delta\varphi_{\mathrm{L,in}}$ is linearly proportional with V_{dc} and the inverse of $f_{\mathrm{in,sw}}/f_{\mathrm{in,LF}}$, however, there is a non-linear relation with M_{in} as shown in **Figure 4.6**. By defining this dependency as a function of M_{in}, which is

$$\Delta\varphi_{\mathrm{L,in,1}}(M_{\mathrm{in}}), \tag{4.22}$$

the scaling function for $\Delta\varphi_{\mathrm{L,in}}(V_{\mathrm{dc}}, f_{\mathrm{in,LF}}, f_{\mathrm{in,sw}}, M_{\mathrm{in}})$ can be defined as

$$\Delta\varphi_{\mathrm{L,in}}(V_{\mathrm{dc}}, f_{\mathrm{in,LF}}, f_{\mathrm{in,sw}}, M_{\mathrm{in}}) = \frac{V_{\mathrm{dc}}}{1\,\mathrm{V}} \cdot \left(\frac{f_{\mathrm{in,LF}}}{f_{\mathrm{in,sw}}}\right) \cdot \Delta\varphi_{\mathrm{L,in,1}}(M_{\mathrm{in}}), \tag{4.23}$$

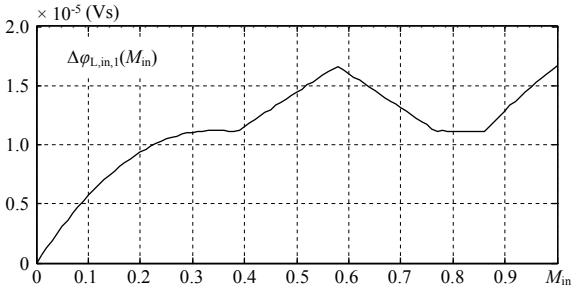


Figure 4.6: Dependency of $\Delta\varphi_{\mathrm{L,in}}$ on M_{in} with $f_{\mathrm{in,LF}} = 50\,\mathrm{Hz}$, $f_{\mathrm{in,sw}}/f_{\mathrm{in,LF}} = 20$ and $V_{\mathrm{dc}} = 1.0\,\mathrm{V}$.

where,

$$V_{\mathrm{dc}} \geq 0, \tag{4.24}$$

$$\frac{f_{\mathrm{in,LF}}}{f_{\mathrm{in,sw}}} \geq \frac{1}{20}. \tag{4.25}$$

Finally, $L_{1,\mathrm{in}}$, which gives the required current ripple $\Delta I_{\mathrm{L,HF}}$ at the defined specifications (V_{dc}, $V_{\mathrm{in,pk}}$, $f_{\mathrm{in,LF}}$ and $f_{\mathrm{in,sw}}$), can now be calculated as

$$L_{1,\mathrm{in}} = \frac{\Delta\varphi_{\mathrm{L,in}}(V_{\mathrm{dc}}, f_{\mathrm{in,LF}}, f_{\mathrm{in,sw}}, M_{\mathrm{in}})}{\Delta I_{\mathrm{L,HF}}}. \tag{4.26}$$

With the same procedure, the maximum difference of the voltage-time product over the CM inductor, $\Delta\varphi_{\mathrm{L,cm}}$, is calculated as

$$\Delta\varphi_{\mathrm{L,cm}} = \max\left(\varphi_{\mathrm{L,cm}}(t)\right) - \min\left(\varphi_{\mathrm{L,cm}}(t)\right), \tag{4.27}$$

$$\varphi_{\mathrm{L,cm}}(t) = \int v_{\mathrm{L,in,cm}}(t) \cdot dt. \tag{4.28}$$

With the resulting dependency $\Delta\varphi_{\mathrm{L,cm,1}}(M_{\mathrm{in}})$ shown in **Figure 4.7** and a scaling function for $\Delta\varphi_{\mathrm{L,cm}}(V_{\mathrm{dc}}, f_{\mathrm{in,LF}}, f_{\mathrm{in,sw}}, M_{\mathrm{in}})$, that is

$$\Delta\varphi_{\mathrm{L,cm}}(V_{\mathrm{dc}}, f_{\mathrm{in,LF}}, f_{\mathrm{in,sw}}, M_{\mathrm{in}}) = \frac{V_{\mathrm{dc}}}{1\,\mathrm{V}} \cdot \left(\frac{f_{\mathrm{in,LF}}}{f_{\mathrm{in,sw}}}\right) \cdot \Delta\varphi_{\mathrm{L,cm,1}}(M_{\mathrm{in}}), \tag{4.29}$$

the high frequency CM current ripple in the first CM filter stage is

$$\Delta I_{\mathrm{L,cm,HF}} = \frac{\Delta\varphi_{\mathrm{L,cm}}(V_{\mathrm{dc}}, f_{\mathrm{in,LF}}, f_{\mathrm{in,sw}}, M_{\mathrm{in}})}{L_{1,\mathrm{cm}}}. \tag{4.30}$$

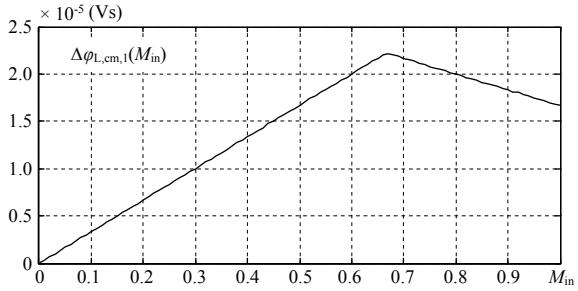


Figure 4.7: Dependency of $\Delta\varphi_{\mathrm{L,cm}}$ on M_{in} with $f_{\mathrm{in,LF}} = 50\,\mathrm{Hz}$, $f_{\mathrm{in,sw}}/f_{\mathrm{in,LF}} = 20$, and $V_{\mathrm{dc}} = 1.0\,\mathrm{V}$.

There is no design specification regarding the CM current ripple $\Delta I_{\mathrm{L,cm,HF}}$, therefore, the CM inductance value $L_{1,\mathrm{cm}}$ can be freely selected in order to satisfy, mainly, the EMI requirement.

In the next step of the EMI input filter design procedure, the minimum allowed DM capacitance value $C_{1,\mathrm{in,min,V}}$ is calculated according to the given limit $\Delta V_{\mathrm{C,HF}}$ of the high-frequency voltage ripple. If we assume a simplified time behavior of the high-frequency current ripple in the DM inductor path and / or through the DM capacitor according to **Figure 4.8**, the high-frequency charge $\Delta Q_{\mathrm{C,HF}}$ and $\Delta V_{\mathrm{C,HF}}$ are

$$\Delta Q_{\mathrm{C,HF}} = \frac{\Delta I_{\mathrm{L,HF}}}{8 \cdot f_{\mathrm{in,sw}}}, \tag{4.31}$$

$$\Delta V_{\mathrm{C,HF}} = \frac{\Delta Q_{\mathrm{C,HF}}}{(1+k) \cdot C_{1,\mathrm{in,min,V}}}; \tag{4.32}$$

therefore,

$$C_{1,\mathrm{in,min,V}} = \frac{\Delta I_{\mathrm{L,HF}}}{8 \cdot f_{\mathrm{in,sw}} \cdot (1+k) \cdot \Delta V_{\mathrm{C,HF}}}. \tag{4.33}$$

Since $\Delta I_{\mathrm{L,HF}}$, $\Delta V_{\mathrm{C,HF}}$ and k are given values from the specifications, $C_{1,\mathrm{in,min,V}}$ only depends on the switching frequency $f_{\mathrm{in,sw}}$.

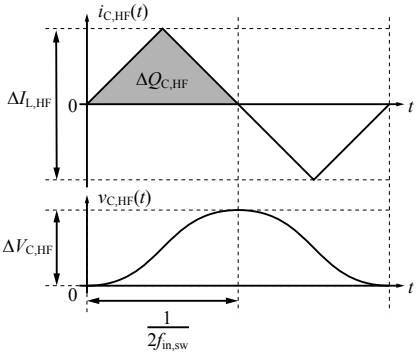


Figure 4.8: Simplified high-frequency current / voltage waveform of a DM capacitor within a single switching period.

4.1.2 Dimensioning of the C value for the reactive current and resonance frequency requirements

The maximum allowed resonance frequency of the second stage LC filter f_{res} also limits the minimum value of the DM capacitance $C_{1,\text{in,min,f}}$. The resonance frequency of the second stage LC filter is

$$f_{\text{res}} = \frac{1}{\sqrt{n \cdot L_{1,\text{in}} \cdot k \cdot C_{1,\text{in,min,f}}}} \tag{4.34}$$

and therefore

$$C_{1,\text{in,min,f}} = \frac{1}{n \cdot k \cdot L_{1,\text{in}} \cdot f_{\text{res}}^2} \tag{4.35}$$

As a result, the minimum DM capacitance value $C_{1,\text{in,min}}$ considered for the filter design is selected as

$$C_{1,\text{in,min}} = \max\left(C_{1,\text{in,min,V}}, C_{1,\text{in,min,f}}\right). \tag{4.36}$$

The limitation of the low-frequency reactive current, $I_{\text{C,LF}}$, defines the maximum value of the DM capacitance $C_{1,\text{in,max}}$; $I_{\text{C,LF}}$ is calculated as

$$I_{\text{C,LF}} = \omega_{\text{in,LF}} \cdot V_{\text{in,pk}} \cdot (1+k) \cdot C_{1,\text{in,max}}; \tag{4.37}$$

therefore,

$$C_{1,\mathrm{in,max}} = \frac{I_{\mathrm{C,LF}}}{\omega_{\mathrm{in,LF}} \cdot V_{\mathrm{in,pk}} \cdot (1+k)}. \tag{4.38}$$

As a result, the calculated minimum / maximum values of the DM capacitance $C_{1,\mathrm{in,min}}$ / $C_{1,\mathrm{in,max}}$ define boundaries of the EMI filter Design Space.

4.1.3 Dimensioning of the LC values for the EMI limitation requirements

The dimensioning of the LC values for the EMI requirement includes the following steps:

1. Estimate the DM and CM noise in the frequency domain and calculate the equivalent noise at the switching frequency.
2. Find the design frequency f_{d} and calculate required DM and CM attenuations $Att_{\mathrm{dm,req}}$ and $Att_{\mathrm{cm,req}}$, respectively.
3. Calculate the DM filter attenuation Att_{dm} at the design frequency and adjust the DM capacitance within the range of its limits until the DM attenuation satisfies $Att_{\mathrm{dm}} \geq Att_{\mathrm{dm,req}}$.
4. Calculate the maximum CM capacitance values according to the low frequency CM current limit.
5. Calculate the CM filter attenuation Att_{cm} at the design frequency and adjust the CM inductance until the CM attenuation satisfies $Att_{\mathrm{cm}} \geq Att_{\mathrm{cm,req}}$.

The first and second steps are done using the Fast Fourier Transform (FFT)[2]. In the third step, the DM filter attenuation is calculated based on the equivalent circuit of the DM filter and the transfer function approach. A simplified Line Impedance Stabilization Network[3] (LISN) circuit is included in the considered transfer function of the DM filter circuit. The fourth step is required for two different reasons: one is to limit the low-frequency CM current peak value and the other is to limit the leakage current to the ground for safety reasons. The minimum

[2]This process is done in MATLAB.
[3]Called the "Artificial Mains Network" in CISPR.

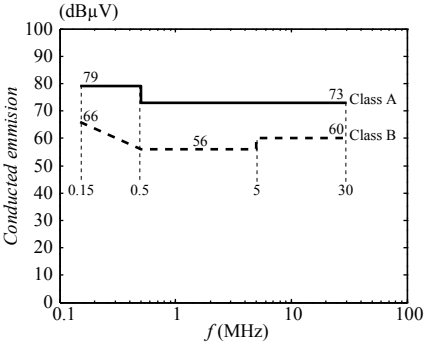


Figure 4.9: Quasi-Peak (QP) limits for conducted noise emissions on the input side of converter systems according to CISPR Publication 11.

allowed value for CM inductances that satisfy the required CM attenuation are calculated in the fifth step. An equivalent circuit including the estimated parasitic capacitances of the semiconductor devices and DC-link bus to GND is considered as discussed in [43].

EMI noise estimation and resulting EMI filter design parameters

Figure 4.9 shows quasi-peak (QP) limits for conducted emissions on the input side according to CISPR Publication 11. According to the required specification, the conducted noise emission from the converter must be lower than the Class A limit. **Figure 4.10** shows the main concept and process for the estimation of the equivalent noise emission and for defining the EMI filter design parameters, such as the design frequency and the required filter attenuation. In the first step, the DM peak voltage spectrum for the switched voltage is calculated in the frequency domain $V_{\mathrm{dm,pk}}(f)$ from the time domain waveform $v_{\mathrm{in,sw}}(t)$ using the FFT technique as follows.

$$V_{\mathrm{dm,pk}}(f) \quad = \quad \mathrm{FFT}\left(v_{\mathrm{in,sw}}(t)\right). \tag{4.39}$$

The calculated spectrum has its first peak at the fundamental modulation frequency $f_{\mathrm{in,LF}}$ and the high-frequency peaks start from the switching frequency $f_{\mathrm{in,sw}}$. Since the EMI requirement starts from

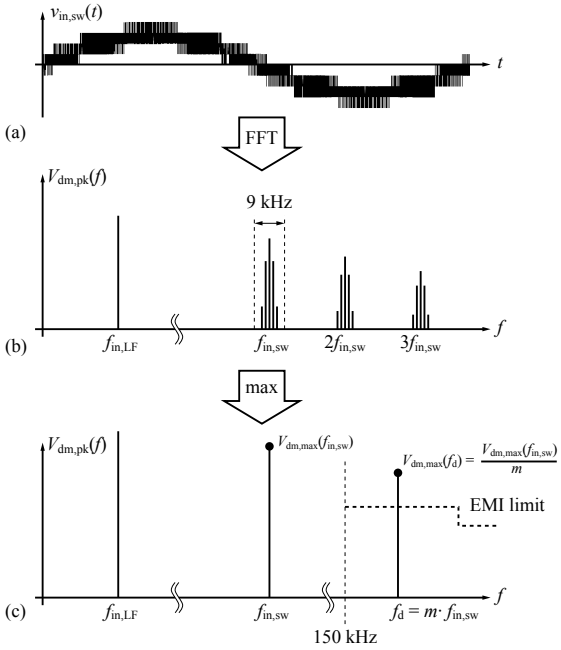


Figure 4.10: Main concept for equivalent noise estimation and process for defining the EMI filter design parameters, (a) DM switched voltage waveform $v_{\mathrm{in,sw}}(t)$ in the time domain, (b) spectrum of $v_{\mathrm{in,sw}}(t)$ in the frequency domain calculated using FFT technique, (c) estimated equivalent noise voltage magnitude at the design frequency.

150 kHz, the m-th harmonic of the switching frequency, which is the first higher harmonic after 150 kHz, is important. This rank m and design frequency f_{d} are

$$m = \mathrm{ceil}\left(\frac{150\,\mathrm{kHz}}{f_{\mathrm{in,sw}}}\right), \tag{4.40}$$

$$f_{\mathrm{d}} = m \cdot f_{\mathrm{in,sw}}. \tag{4.41}$$

Since the conducted noise voltage magnitude $V_{\mathrm{dm,max}}(f_{\mathrm{d}})$ at the design frequency f_{d} is in a first approximation m-times smaller than the magnitude of the equivalent noise voltage at the switching frequency $f_{\mathrm{in,sw}}$

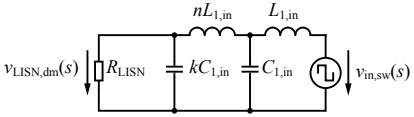


Figure 4.11: Equivalent circuit of DM filter with noise source and simplified LISN (resistor).

(assuming a rectangular voltage waveform [44]), $V_{\mathrm{dm,max}}(f_{\mathrm{d}})$ follows as

$$V_{\mathrm{dm,max}}(f_{\mathrm{d}}) = \frac{V_{\mathrm{dm,max}}(f_{\mathrm{in,sw}})}{m}, \tag{4.42}$$

$$V_{\mathrm{dm,max}}(f_{\mathrm{in,sw}}) = \max\left\{V_{\mathrm{dm,pk}}(f|_{=f_{\mathrm{in,sw}}-4.5\,\mathrm{kHz}\ldots f_{\mathrm{in,sw}}+4.5\,\mathrm{kHz}})\right\}. \tag{4.43}$$

The required attenuation for the DM filter $Att_{\mathrm{dm,req}}$ in dB is given by

$$Att_{\mathrm{dm,req}}\,[\mathrm{dB}] = E_{\mathrm{dm,max}}(f_{\mathrm{d}})\,[\mathrm{dB}\mu\mathrm{V}] - Limit(f_{\mathrm{d}})\,[\mathrm{dB}\mu\mathrm{V}] + Margin\,[\mathrm{dB}], \tag{4.44}$$

$$E_{\mathrm{dm,max}}(f_{\mathrm{d}})\,[\mathrm{dB}\mu\mathrm{V}] = 20\cdot\log\left(10^{6}\cdot V_{\mathrm{dm,max}}(f_{\mathrm{d}})\,[\mathrm{V}]\right). \tag{4.45}$$

Here, $E_{\mathrm{dm,max}}(f_{\mathrm{d}})$ is the equivalent DM noise voltage magnitude at the design frequency in dBμV and $Limit(f_{\mathrm{d}})$ is the EMI noise emission limit at f_{d} in dBμV. A $Margin$ is added to maintain the required filter attenuation in practical realizations where the filter's inductances and capacitances are subject to tolerances. In the case at hand, $Margin =$ 10 dB is chosen.

Exactly the same procedure is done for the required attenuation for the the CM filter $Att_{\mathrm{cm,req}}$ with the time domain CM voltage waveform $v_{\mathrm{in,cm}}(t)$.

Calculation of the DM filter attenuation

Figure 4.11 shows the DM filter equivalent circuit with noise signal source $v_{\mathrm{in,sw}}$ and the LISN resistor R_{LISN}. An analytical expression for the transfer function is

$$\begin{aligned} G_{\mathrm{in,LISN,dm}}(s) &= \frac{v_{\mathrm{LISN,dm}}(s)}{v_{\mathrm{in,sw}}(s)}, \\ &= \frac{R}{Denominator}, \end{aligned} \tag{4.46}$$

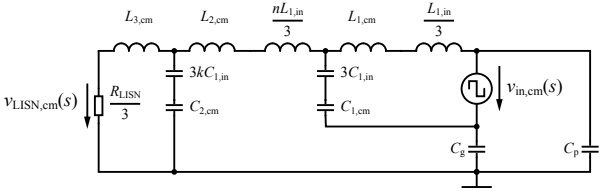


Figure 4.12: Equivalent circuit of CM filter with noise source, simplified LISN (resistor) and parasitic capacitances to GND.

where

$$\begin{aligned} Denominator &= nkRL^2C^2s^4 + nL^2Cs^3 \ldots \\ &\quad +(1+k+nk)RLCs^2 + (1+n)Ls \ldots \\ &\quad +R, \end{aligned} \tag{4.47}$$

$$R = R_{\mathrm{LISN}} = 50\,\Omega, \tag{4.48}$$

$$L = L_{1,\mathrm{in}}, \tag{4.49}$$

$$C = C_{1,\mathrm{in}}. \tag{4.50}$$

The attenuation of the DM filter at the design frequency f_d is calculated from the gain of the transfer function as follows.

$$Att_{\mathrm{dm}}(f_\mathrm{d}) = 20 \cdot \log\left\{\mathrm{Gain}\left(G_{\mathrm{in,LISN,dm}}(j \cdot 2\pi \cdot f_\mathrm{d})\right)\right\}. \tag{4.51}$$

The DM capacitance value $C_{1,\mathrm{in}}$ is swept from its minimum value $C_{1,\mathrm{in,min}}$ to its maximum value $C_{1,\mathrm{in,max}}$ until $Att_{\mathrm{dm}}(f_\mathrm{d}) \geq Att_{\mathrm{dm,req}}(f_\mathrm{d})$ is satisfied.

Calculation of maximum CM capacitances

Figure 4.12 shows an equivalent circuit of the CM filter including R_{LISN} and parasitic capacitances C_p and C_g. C_p represents the total parasitic capacitance between the semiconductor packages (the collector terminal of the IGBTs and the cathode terminal of the SBDs) and GND. This value can be analytically estimated as

$$C_\mathrm{p} = \epsilon_0 \cdot \epsilon_{\mathrm{c-hs}} \cdot \frac{A_{\mathrm{th,c-hs}}}{t_{\mathrm{c-hs}}} \cdot N_{\mathrm{case}}. \tag{4.52}$$

Here, $\epsilon_{\mathrm{c-hs}}$ is the relative permittivity of the thermal contact material between the semiconductor case and the heat sink, $t_{\mathrm{c-hs}}$ is the thickness

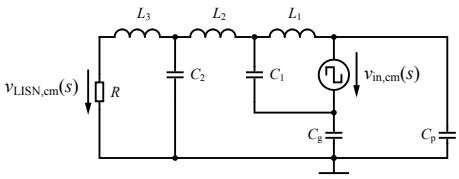


Figure 4.13: Simplified equivalent circuit of the CM filter.

of the thermal contact material, $A_{\mathrm{th,c-hs}}$ is the thermal contact area of a single semiconductor case, and N_{case} is the total number of semiconductor cases in the rectifier stage. In the case at hand, $\epsilon_{\mathrm{c-hs}} = 4.5$, $t_{\mathrm{c-hs}} = 0.05\,\mathrm{mm}$, $A_{\mathrm{th,c-hs}} = 204.3\,\mathrm{mm}^2$ and $N_{\mathrm{case}} = 18$ have been selected. As a result, $C_{\mathrm{p}} = 2.93\,\mathrm{nF}$ is assumed in the CM filter design procedure. The other parasitic capacitance C_{g} represents the total parasitic capacitance between the DC-link bus (P, M and N) and GND. However, it is difficult to estimate the value of C_{g} in the design stage. Therefore, a constant value of $C_{\mathrm{g}} = 6.0\,\mathrm{nF}$ is assumed for the design procedure.

For the sake of simplicity, the series connected DM / CM inductors and capacitors are merged into single components, as shown in **Figure 4.13** with

$$R = \frac{R_{\mathrm{LISN}}}{3} = \frac{50\,\Omega}{3}, \tag{4.53}$$

$$L_1 = L_{1,\mathrm{cm}} + \frac{L_{1,\mathrm{in}}}{3}, \tag{4.54}$$

$$L_2 = L_{2,\mathrm{cm}} + \frac{n \cdot L_{1,\mathrm{in}}}{3}, \tag{4.55}$$

$$L_3 = L_{3,\mathrm{cm}}, \tag{4.56}$$

$$C_1 = \frac{3 \cdot C_{1,in} \cdot C_{1,cm}}{3 \cdot C_{1,in} + C_{1,cm}}, \tag{4.57}$$

$$C_2 = \frac{3 \cdot k \cdot C_{1,in} \cdot C_{2,cm}}{3 \cdot k \cdot C_{1,in} + C_{2,cm}}. \tag{4.58}$$

In case of third harmonic injection modulation, the CM noise source $v_{\mathrm{in,cm}}$ contains a low frequency component at three times mains frequency, $f_{\mathrm{in,3h}} = 3 \cdot f_{\mathrm{in,LF}}$. Therefore, a high C_1 value could cause a high CM peak current through L_1 at $f_{\mathrm{in,3h}}$. Typically, the CM inductance value is chosen to be high, thus, the CM inductor could be saturated by carrying this high CM current. In order to avoid satura-

tion, the maximum low frequency CM peak current $I_{\mathrm{pk,cm,3h}}$ is limited to be lower than $I_{\mathrm{pk,cm,3h,max}}$. $I_{\mathrm{pk,cm,3h}}$ is calculated according to

$$\begin{aligned} I_{\mathrm{pk,cm,3h}} &= 2\pi \cdot f_{\mathrm{in,3h}} \cdot C_1 \cdot V_{\mathrm{cm,max}}(f_{\mathrm{in,3h}}), && (4.59)\\ V_{\mathrm{cm,max}}(f_{\mathrm{in,3h}}) &= \max\left\{V_{\mathrm{cm,pk}}(f|_{=f_{\mathrm{in,3h}}-f_{\mathrm{in,LF}}\cdots f_{\mathrm{in,3h}}+f_{\mathrm{in,LF}}})\right\} && (4.60)\\ V_{\mathrm{cm,pk}}(f) &= \mathrm{FFT}\left(v_{\mathrm{in,cm}}(t)\right). && (4.61) \end{aligned}$$

As a result, the maximum value of C_1 is

$$C_{1,\mathrm{max}} = \frac{I_{\mathrm{pk,cm,3h,max}}}{2\pi \cdot f_{\mathrm{in,3h}} \cdot V_{\mathrm{cm,max}}(f_{\mathrm{in,3h}})}. \quad (4.62)$$

In the EMI filter design procedure, $I_{\mathrm{pk,cm,3h,max}} = 0.1\,\mathrm{A}$ is chosen by hand.

For safety reasons, the maximum leakage current to GND, $I_{leak,gnd,max}$, is limited up to 3.5 mA for Class I equipment [46, 45]. Therefore, the maximum value of C_2 must be limited in order to limit the leakage current to GND. The leakage current to GND, $I_{\mathrm{leak,gnd}}$, and the maximum capacitance value for C_2 can be calculated as:

$$\begin{aligned} I_{\mathrm{leak,gnd}} &= 2\pi \cdot f_{\mathrm{in,LF}} \cdot C_2 \cdot V_{\mathrm{in,pk}}, && (4.63)\\ C_{2,\mathrm{max}} &= \frac{I_{\mathrm{leak,gnd,max}}}{2\pi \cdot f_{\mathrm{in,LF}} \cdot V_{\mathrm{in,pk}}}. && (4.64) \end{aligned}$$

Calculation of the CM filter attenuation

From the equivalent CM filter shown in **Figure 4.13**, there are two CM current paths. The first path is through C_{g} (cf. **Figure 4.14(a)**), and the second path is through C_{p} (cf. **Figure 4.14(b)**). The transfer function of the first current path $G_{\mathrm{in,LISN,cm,a}}(s)$ is

$$\begin{aligned} G_{\mathrm{in,LISN,cm,a}}(s) &= \frac{v_{\mathrm{LISN,cm,a}}(s)}{v_{\mathrm{in,cm}}(s)},\\ &= \frac{RC_{\mathrm{g}}s}{Denominator}, && (4.65) \end{aligned}$$

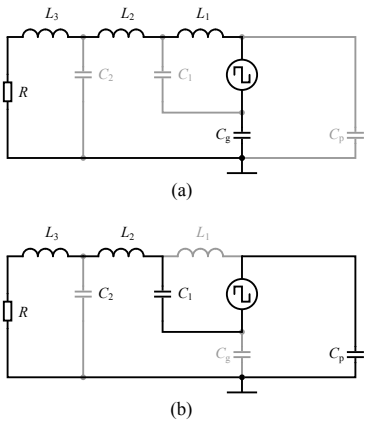


Figure 4.14: CM current paths over R_{LISN}, (a) current path through C_{g}, (b) current path through C_{p}.

where

$$\begin{aligned} \mathit{Denominator} \;=\; & C_1C_2C_{\mathrm{g}}L_1L_2L_3s^6\ldots \\ & +C_1C_2C_{\mathrm{g}}L_1L_2Rs^5\ldots \\ & +\left(C_1C_2L_1L_3+C_1C_{\mathrm{g}}L_1L_2+C_1C_{\mathrm{g}}L_1L_3\right)s^4\ldots \\ & +\left(C_2C_{\mathrm{g}}L_1L_3+C_2C_{\mathrm{g}}L_2L_3\right)s^4\ldots \\ & +\left(C_1C_2L_1R+C_1C_{\mathrm{g}}L_1R+C_2C_{\mathrm{g}}L_1R+C_2C_{\mathrm{g}}L_2R\right)s^3\ldots \\ & +\left(C_1L_1+C_2L_3+C_{\mathrm{g}}L_1+C_{\mathrm{g}}L_2+C_{\mathrm{g}}L_3\right)s^2\ldots \\ & +\left(C_2R+C_{\mathrm{g}}R\right)s+1. \end{aligned} \tag{4.66}$$

The transfer function of the second current path $G_{\mathrm{in,LISN,cm,b}}(s)$ is

$$\begin{aligned} G_{\mathrm{in,LISN,cm,b}}(s) &= \frac{v_{\mathrm{LISN,cm,b}}(s)}{-v_{\mathrm{in,cm}}(s)}, \\ &= \frac{R}{\mathit{Denominator}}, \end{aligned} \tag{4.67}$$

where

$$\mathit{Denominator} = \left(C_2L_3s^2+C_2Rs+1\right)F_1, \tag{4.68}$$

$$\begin{aligned} F_1 &= \frac{R+L_3s}{C_2L_3s^2+C_2Rs+1}+L_2s\ldots \\ &\quad +\frac{1}{C_1s}+\frac{1}{C_{\mathrm{p}}s}. \end{aligned} \tag{4.69}$$

To be on the safe side, the attenuation of both transfer functions should be higher than the required attenuation at the design frequency. There are three degrees of freedom for tuning the attenuation of the transfer functions, L_1, L_2 and L_3. In order to simplify the tuning procedure, a constant value of $L_3 = 0.5\,\mathrm{mH}$ is used. The tuning procedure is done as follows:

1. Tune L_2 from a small value to a large value until the attenuation of $G_{\mathrm{in,LISN,cm,b}}$ at the design frequency f_d satisfies the required attenuation $Att_{cm,req}$;
2. Tune L_1 until the attenuation of $G_{\mathrm{in,LISN,cm,a}}$ at the design frequency f_d satisfies the required attenuation.

The inductance values are tuned to achieve the required minimum inductance values for CM noise attenuation $L_{1,\mathrm{cm}}$ and $L_{2,\mathrm{cm}}$. These CM inductance values are stored in the filter design pool for the CM inductor optimization procedure.

4.1.4 Adding a damping component

In order to damp the resonance current, R-C parallel damping branches are added to both stages of the EMI input filter. The optimal design procedure is described fully in [47] and can be summarized as follows:

$$R_{0\mathrm{f}} = \sqrt{\frac{L_\mathrm{in}}{C_\mathrm{in}}}, \tag{4.70}$$

$$C_{\mathrm{in,d}} = a \cdot C_\mathrm{in}, \tag{4.71}$$

$$R_{\mathrm{in,d}} = R_{0\mathrm{f}} \cdot \sqrt{\frac{(2+a)(4+3a)}{2a^2(4+a)}}, \tag{4.72}$$

where $C_{\mathrm{in,d}}$ is the damping capacitance and $R_{\mathrm{in,d}}$ is damping resistance. a is an optimization factor and $a = 1$ is selected by hand.

4.2 Design of two-stage output filter

Figure 4.15 depicts a full schematic of the four-line three-phase output filter. It only consists of a two-stage DM filter with an additional R-L series damping circuit in the second stage. The DM inductance / capacitance values for

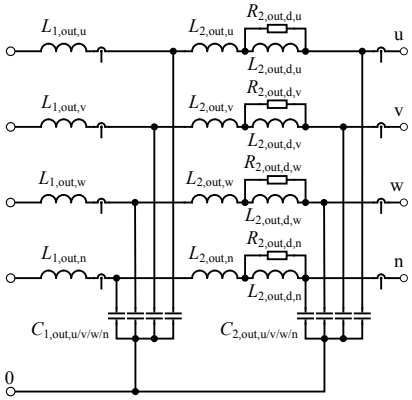


Figure 4.15: Output filter circuit structure.

the second stage $L_{2,\text{out,u/v/w/n}} \,/\, C_{2,\text{out,u/v/w/n}}$ are defined from the inductance / capacitance values for the first stage, $L_{1,\text{out,u/v/w/n}} \,/\, C_{1,\text{out,u/v/w/n}}$, with design constants $n = 0.1$ and $k = 0.9$ as discussed in the previous section:

$$L_{2,\text{out,u/v/w/n}} = n \cdot L_{1,\text{out,u/v/w/n}}, \tag{4.73}$$

$$C_{2,\text{out,u/v/w/n}} = k \cdot C_{1,\text{out,u/v/w/n}}. \tag{4.74}$$

The required specifications for the output filter are summarized in **Table 4.3**. Here, γ_{out} is the required factor for the current ripple, $V_{\text{out,pk}}$ is the nominal output voltage amplitude, $I_{\text{out,pk}}$ is the nominal output current amplitude, V_{dc} is the DC-link voltage, $f_{\text{out,LF}}$ is the fundamental output frequency, and $f_{\text{out,sw}}$ is the operating switching frequency of the output stage. The flow chart for the output filter design is shown in **Figure 4.16**.

The same procedure as for the EMI input filter design is followed, only without the EMI requirement. This means there is no CM inductor in the output filter, and therefore the calculation for the required DM inductance value $L_{1,\text{out}}$ is different from that for the EMI input filter.

Table 4.3: Required specifications of output filter.

Criteria		Required specification
$\Delta I_{\mathrm{L,HF}}$	$=$	$\gamma_{\mathrm{out}} \cdot I_{\mathrm{out,pk}}$
$\Delta V_{\mathrm{C,HF}}$	$\leq$	$0.01 \cdot V_{\mathrm{out,pk}}$
$I_{\mathrm{C,LF}}$	$\leq$	$0.2 \cdot I_{\mathrm{out,pk}}$
f_{res}	$\leq$	$0.7 \cdot f_{\mathrm{out,sw}}$
EMI noise emission level		—

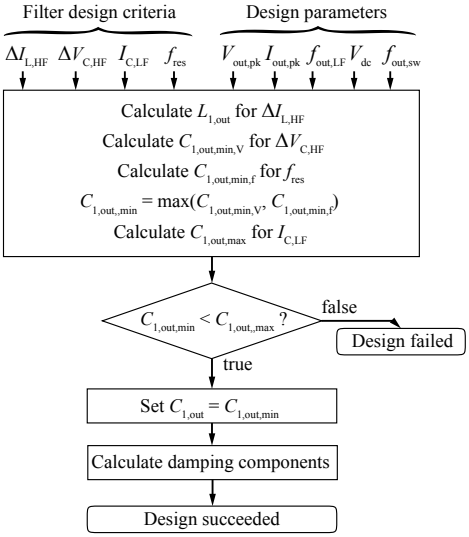


Figure 4.16: Design procedure flow chart for the output filter.

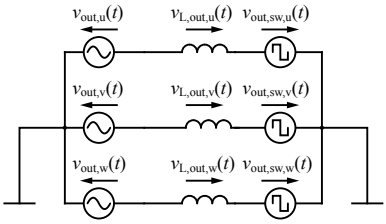


Figure 4.17: Equivalent circuit of the AC-side of the output stage.

4.2.1 Dimensioning of the LC values for the current and voltage ripple requirement

Figure 4.17 shows the equivalent circuit of the AC-side of the output stage. $v_{\mathrm{out,u}}$, $v_{\mathrm{out,v}}$, $v_{\mathrm{out,w}}$ and $v_{\mathrm{out,n}}$ are the output phase voltages, which are defined as

$$v_{\mathrm{out,u}}(t) = V_{\mathrm{out,pk}} \cdot \sin\left(\omega_{\mathrm{out,LF}} \cdot t\right), \tag{4.75}$$

$$v_{\mathrm{out,v}}(t) = V_{\mathrm{out,pk}} \cdot \sin\left(\omega_{\mathrm{out,LF}} \cdot t - \frac{2\pi}{3}\right), \tag{4.76}$$

$$v_{\mathrm{out,w}}(t) = V_{\mathrm{out,pk}} \cdot \sin\left(\omega_{\mathrm{out,LF}} \cdot t - \frac{4\pi}{3}\right), \tag{4.77}$$

$$v_{\mathrm{out,n}}(t) = 0. \tag{4.78}$$

Here, the output voltage of phase n is kept at zero. $\omega_{\mathrm{out,LF}}$ is the output angular fundamental frequency, where

$$\omega_{\mathrm{out,LF}} = 2\pi \cdot f_{\mathrm{out,LF}}. \tag{4.79}$$

$v_{\mathrm{out,sw,u}}$, $v_{\mathrm{out,sw,v}}$, $v_{\mathrm{out,sw,w}}$ and $v_{\mathrm{out,sw,n}}$ are the switched voltages of the semiconductor switching circuit, which can be defined as

$$v_{\mathrm{out,sw,u}}(t) = \begin{cases} \frac{V_{\mathrm{dc}}}{2} & \left(m_{\mathrm{out,u}}(t) \geq m_{\mathrm{c,1}}(t)\right), \\ -\frac{V_{\mathrm{dc}}}{2} & \left(m_{\mathrm{out,u}}(t) < m_{\mathrm{c,2}}(t)\right), \\ 0 & \text{otherwise,} \end{cases} \tag{4.80}$$

$$v_{\mathrm{out,sw,v}}(t) = \begin{cases} \frac{V_{\mathrm{dc}}}{2} & \left(m_{\mathrm{out,v}}(t) \geq m_{\mathrm{c,1}}(t)\right), \\ -\frac{V_{\mathrm{dc}}}{2} & \left(m_{\mathrm{out,v}}(t) < m_{\mathrm{c,2}}(t)\right), \\ 0 & \text{otherwise,} \end{cases} \tag{4.81}$$

$$v_{\mathrm{out,sw,w}}(t) = \begin{cases} \frac{V_{\mathrm{dc}}}{2} & \left(m_{\mathrm{out,w}}(t) \geq m_{\mathrm{c,1}}(t)\right), \\ -\frac{V_{\mathrm{dc}}}{2} & \left(m_{\mathrm{out,w}}(t) < m_{\mathrm{c,2}}(t)\right), \\ 0 & \text{otherwise,} \end{cases} \tag{4.82}$$

$$v_{\mathrm{out,sw,n}}(t) = 0. \tag{4.83}$$

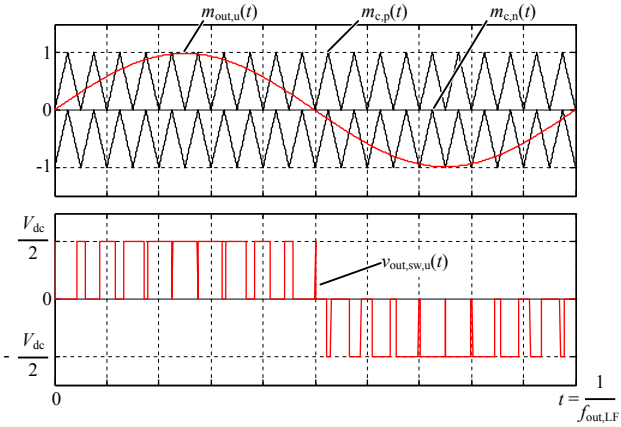


Figure 4.18: Example waveform of modulation signals and the resulting switched phase voltage for $M_{out} = 1.0$, $f_{out,sw} = 20 \cdot f_{out,LF}$ and $V_{dc} = 1.0\,V$.

$m_{out,u}$, $m_{out,v}$ and $m_{out,w}$ are the modulation signals for each phase at the fundamental frequency,

$$m_{out,u}(t) = M_{out} \cdot \sin\left(\omega_{out,LF} \cdot t\right), \tag{4.84}$$

$$m_{out,v}(t) = M_{out} \cdot \sin\left(\omega_{out,LF} \cdot t - \frac{2\pi}{3}\right), \tag{4.85}$$

$$m_{out,w}(t) = M_{out} \cdot \sin\left(\omega_{out,LF} \cdot t - \frac{4\pi}{3}\right), \tag{4.86}$$

$$m_{out,n}(t) = 0. \tag{4.87}$$

Here, $M_{out} = 2V_{out,pk}/V_{dc}$ is the modulation index. **Figure 4.18** shows the modulation signals and the resulting switched phase voltage $v_{out,sw,u}(t)$. Finally, the voltages across the inductors ($v_{L,out,u}$, $v_{L,out,v}$ and $v_{L,out,w}$) are calculated as follows.

$$v_{L,out,u}(t) = v_{out,sw,u}(t) - v_{out,u}(t), \tag{4.88}$$

$$v_{L,out,v}(t) = v_{out,sw,v}(t) - v_{out,v}(t), \tag{4.89}$$

$$v_{L,out,w}(t) = v_{out,sw,w}(t) - v_{out,w}(t). \tag{4.90}$$

The maximum difference $\Delta\varphi_{L,out}$ of voltage-time product across an inductor is also calculated for the output filter. The main difference between the EMI input filter and the output filter is that the full switched

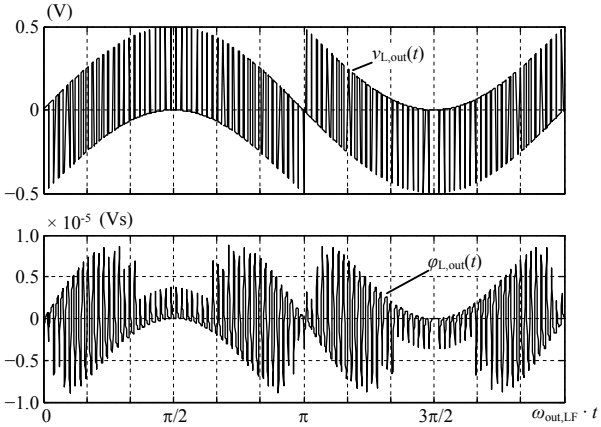


Figure 4.19: Time behavior of the inductor voltage and voltage-time product for $M_{out} = 1.0$, $f_{out,LF} = 50\,Hz$, $f_{out,sw}/f_{out,LF} = 100$ and $V_{dc} = 1.0\,V$.

HF content of a switched phase voltage $v_{out,sw,u/v/w}$ occurs across the respective phase inductor (besides the LF voltage component driving the output current). Thus, $\Delta\varphi_{L,out}$ is higher than at the input side where a CM inductor is present. $\Delta\varphi_{L,out}$ is calculated as follows.

$$\Delta\varphi_{L,out} = \max\left(\varphi_{L,out}(t)\right) - \min\left(\varphi_{L,out}(t)\right), \tag{4.91}$$

$$\varphi_{L,out}(t) = \int v_{L,out}(t) \cdot dt. \tag{4.92}$$

For example, the voltage waveform of the filter inductor and the corresponding voltage-time product are shown in **Figure 4.19**. The relationship between $\Delta\varphi_{L,out}$ and M_{out} is shown in **Figure 4.20**. By defining the dependency of $\Delta\varphi_{L,out,1}$ on M_{out} as a function $\Delta\varphi_{L,out,1}(M_{out})$, the scaling function for $\Delta\varphi_{L,out}$ is resulting as

$$\Delta\varphi_{L,out}(V_{dc}, f_{out,LF}, f_{out,sw}, M_{out}) = \frac{V_{dc}}{1\,V} \cdot \left(\frac{f_{out,LF}}{f_{out,sw}}\right) \cdot \Delta\varphi_{L,out,1}(M_{out}), \tag{4.93}$$

where

$$V_{dc} \geq 0, \tag{4.94}$$

$$\frac{f_{out,LF}}{f_{out,sw}} \geq \frac{1}{20}. \tag{4.95}$$

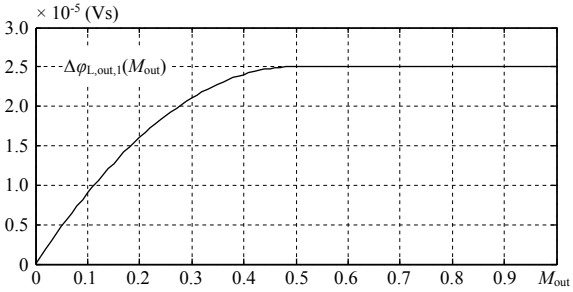


Figure 4.20: Dependency of $\Delta\varphi_{\mathrm{L,out}}$ on M_{out} for $f_{\mathrm{out,LF}} = 50\,\mathrm{Hz}$, $f_{\mathrm{out,sw}}/f_{\mathrm{out,LF}} = 100$ and $V_{\mathrm{dc}} = 1.0\,\mathrm{V}$.

Finally, the inductance $L_{1,\mathrm{out}}$ which gives the required current ripple $\Delta I_{\mathrm{L,HF}}$ at the defined specifications (V_{dc}, $V_{\mathrm{out,pk}}$, $f_{\mathrm{out,LF}}$ and $f_{\mathrm{out,sw}}$) is calculated as

$$L_{1,\mathrm{out}} = \frac{\Delta\varphi_{\mathrm{L,out}}(V_{\mathrm{dc}}, f_{\mathrm{out,LF}}, f_{\mathrm{out,sw}}, M_{\mathrm{out}})}{\Delta I_{\mathrm{L,HF}}}. \tag{4.96}$$

In the next step of the output filter design procedure, the minimum allowed DM capacitance value $C_{1,\mathrm{out,min,V}}$ is calculated based on the limit for the high frequency voltage ripple $\Delta V_{\mathrm{C,HF}}$. The high frequency charge $\Delta Q_{\mathrm{C,HF}}$ and $V_{\mathrm{C,HF}}$ are

$$\Delta Q_{\mathrm{C,HF}} = \frac{\Delta I_{\mathrm{L,HF}}}{8 \cdot f_{\mathrm{out,sw}}}, \tag{4.97}$$

$$\Delta V_{\mathrm{C,HF}} = \frac{\Delta Q_{\mathrm{C,HF}}}{(1+k) \cdot C_{1,\mathrm{out,min,V}}}; \tag{4.98}$$

therefore,

$$C_{1,\mathrm{out,min,V}} = \frac{\Delta I_{\mathrm{L,HF}}}{8 \cdot f_{\mathrm{out,sw}} \cdot (1+k) \cdot \Delta V_{\mathrm{C,HF}}}. \tag{4.99}$$

Since $\Delta I_{\mathrm{L,HF}}$, $\Delta V_{\mathrm{C,HF}}$ and k are given values from the specifications, $C_{1,\mathrm{in,min,V}}$ only depends on the switching frequency $f_{\mathrm{out,sw}}$.

4.2.2 Dimensioning of C value for the reactive current and resonance frequency requirements

The maximum allowed resonance frequency for the second stage LC filter f_{res} also limits the minimum value of the capacitance $C_{1,\text{out,min,f}}$. The resonance frequency of the second stage LC filter is

$$f_{\text{res}} = \frac{1}{\sqrt{n \cdot L_{1,\text{out}} \cdot k \cdot C_{1,\text{out,min,f}}}}, \tag{4.100}$$

and therefore

$$C_{1,\text{out,min,f}} = \frac{1}{n \cdot k \cdot L_{1,\text{out}} \cdot f_{\text{res}}^2}. \tag{4.101}$$

As a result, the minimum capacitance value is selected as

$$C_{1,\text{out,min}} = \max\left(C_{1,\text{out,min,V}}, C_{1,\text{out,min,f}}\right) \tag{4.102}$$

The limit for the low-frequency reactive current $I_{\text{C,LF}}$ defines the maximum value of the capacitance $C_{1,\text{out,max}}$. The limit for the low-frequency reactive current $I_{\text{C,LF}}$ is calculated as follows:

$$I_{\text{C,LF}} = \omega_{\text{out,LF}} \cdot V_{\text{out,pk}} \cdot (1+k) \cdot C_{1,\text{out,max}}; \tag{4.103}$$

therefore,

$$C_{1,\text{out,max}} = \frac{I_{\text{C,LF}}}{\omega_{\text{out,LF}} \cdot V_{\text{out,pk}} \cdot (1+k)}. \tag{4.104}$$

As a result, the calculated minimum / maximum value of the capacitance $C_{1,\text{out,min}} / C_{1,\text{out,max}}$ defines the boundaries of the output filter design. Since there are no constraints, $C_{1,\text{out}} = C_{1,\text{out,min}}$ will be the optimal selection. If the minimum is larger than the maximum, $C_{1,\text{out,min}} > C_{1,\text{out,max}}$, the required specifications result in a conflict and the design has to be discarded.

4.2.3 Adding a damping component

In order to damp the resonance current, R-L series damping branches are added to the second stage of the output filter. The optimal design

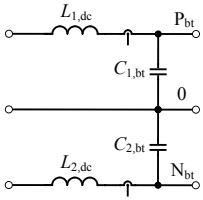


Figure 4.21: DC-port output filter circuit structure.

procedure is described fully in [47] and can be summarized as follows:

$$R_{0f} = \sqrt{\frac{L_{out}}{C_{out}}}, \tag{4.105}$$

$$L_{out,d} = a \cdot L_{out}, \tag{4.106}$$

$$R_{out,d} = R_{0f} \cdot \frac{a}{1+a}\sqrt{\frac{(2+a)(4+3a)}{2(1+a)(4+a)}}, \tag{4.107}$$

Here, $L_{out,d}$ is the damping capacitance and $R_{out,d}$ is the damping resistance. a is an optimization factor and $a = 1$ is selected by hand.

4.3 Design of the DC-port output filter

Figure 4.21 depicts the schematic of the single-stage DC-port output filter. The required filter specifications are summarized in **Table 4.4**. Here, γ_{dc} is the required factor for the current ripple, V_{bt} is the nominal battery voltage, I_{bt} is the nominal battery current, V_{dc} is the DC-link voltage, and $f_{dc,sw}$ is the operating switching frequency of the DC–DC converter stage. The filter design procedure flow chart is shown in **Figure 4.22**. There are only two design requirements.

Table 4.4: Required specifications of DC-port output filter.

Criteria		Required specification
$\Delta I_{\mathrm{L,HF}}$	=	$\gamma_{\mathrm{dc}} \cdot I_{\mathrm{bt}}$
$\Delta V_{\mathrm{C,HF}}$	≤	$0.01 \cdot V_{\mathrm{dc}}$
$I_{\mathrm{C,LF}}$		—
f_{res}		—
EMI noise emission level		—

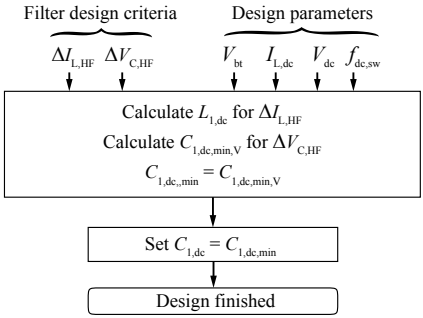


Figure 4.22: Flow chart of the DC-port output filter design procedure.

4.3.1 Dimensioning of the LC values for the current and voltage ripple requirement

The voltage-time product across the filter inductor $L_{1,\mathrm{dc}}$ is calculated as

$$\Delta\varphi_{\mathrm{L,dc}} = \frac{V_{\mathrm{bt}}}{2} \cdot \frac{M_{\mathrm{dc}}}{f_{\mathrm{dc,sw}}}, \tag{4.108}$$

$$M_{\mathrm{dc}} = 1 - \frac{V_{\mathrm{bt}}}{V_{\mathrm{dc}}}. \tag{4.109}$$

Here, M_{dc} is the modulation index, which is equal to the DC–DC converter duty ratio. Thus, the required inductance value $L_{1,\mathrm{dc}}$ is

$$L_{1,\mathrm{dc}} = \frac{\Delta\varphi_{\mathrm{L,dc}}(V_{\mathrm{dc}}, f_{\mathrm{dc,sw}}, M_{\mathrm{dc}})}{\Delta I_{\mathrm{L,HF}}}. \tag{4.110}$$

The high frequency charge $\Delta Q_{\mathrm{C,HF}}$ and the voltage ripple at DC-

link capacitor $C_{1,\mathrm{dc}}$ are

$$\Delta Q_{\mathrm{C,HF}} = \frac{M_{\mathrm{dc}}}{f_{\mathrm{dc,sw}}} \cdot \frac{P_{\mathrm{out}}}{V_{\mathrm{dc}}}, \tag{4.111}$$

$$\Delta V_{\mathrm{C,HF}} = \frac{2\Delta Q_{\mathrm{C,HF}}}{C_{1,\mathrm{dc,min}}}, \tag{4.112}$$

therefore,

$$C_{1,\mathrm{dc,min}} = \frac{2M \cdot S_{\mathrm{out}}}{f_{\mathrm{dc,sw}} \cdot V_{\mathrm{dc}} \cdot \Delta V_{\mathrm{C,HF}}}. \tag{4.113}$$

$C_{1,\mathrm{dc,min}}$ is selected as the designed value of $C_{1,\mathrm{dc}}$ and $C_{2,\mathrm{dc}}$.

4.4 Conclusion

In this section, the analytical design procedure for the EMI input filter, the output filter, and the DC-port output filter have been discussed. The design procedures for the filters are based on the Design Space approach and the required specifications for defining the boundaries for each filter were described step-by-step. Typically, designing an EMI filter is a complicated and time consuming procedure. Therefore, an analytical EMI noise estimation and the required filter design parameters, such as the design frequency and required filter attenuation, for both the DM and CM noise should be done in advance to avoid trial-and-error troubleshooting on the resulting filter hardware.

Chapter 5

System-level multi-objective optimization

Table 5.1 summarizes the requirements and specifications for the converter considered in this thesis. The maximum temperature limit specifications and the considered ambient temperature are very important: the total volume and resulting power density of the converter system is highly dependent on these parameters. In order to achieve a system with as high a power density as possible, the temperature limits are set based on the maximum admissible operating temperature of the materials (cf. **Table 3.1**). On the other hand, an ambient temperature of 55 °C is assumed, which corresponds to the operating temperature typically required in industrial applications. As discussed in **Section 2.3** and **Section 3.4.2**, the total power consumption of the auxiliary circuits $P_{\mathrm{aux,tot}}$ and the total resistance of the PCB traces R_{pcb} are directly measured on the hardware later. However, in order to take both losses into consideration in the optimization results, $P_{\mathrm{aux,tot}}$ and R_{pcb} are considered as parts of the converter specifications. Since both values are constant during the optimization procedure, there is no major effect on the optimization result.

Table 5.1: Converter specifications.

Amplitude of input phase voltage	$V_{\text{in,pk}}$	325.27 V
Input frequency	$f_{\text{in,LF}}$	50 Hz
Max. input phase voltage ripple	$\gamma_{\text{in,v}}$	7.6 %
EMI requirement		CISPR class A
Amplitude of output phase voltage	$V_{\text{out,pk}}$	325.27 V
Output frequency	$f_{\text{out,LF}}$	50 Hz
Nominal output power	S_{out}	20 kVA
Max. output voltage ripple	$\gamma_{\text{out,v}}$	1.0 %
DC-link voltage	V_{dc}	720 V
Battery voltage	V_{bt}	360 V
Ambient temperature	ϑ_{amb}	55 °C
Max. junction temperature	$\vartheta_{\text{j,max}}$	150 °C
Max. inductor winding hot-spot temperature	$\vartheta_{\text{whs,max}}$	150 °C
Max. inductor core hot-spot temperature	$\vartheta_{\text{chs,max}}$	Depends on material.
Power consumption of auxiliary circuits	$P_{\text{aux,tot}}$	23.9 W
Resistance of PCB traces	R_{pcb}	$3 \times 24\,\text{m}\Omega$

5.1 Optimization procedure

The multi-objective optimization approach presented in this thesis considers the converter and component models listed below:

- Power semiconductors: conduction and switching losses, thermal model; the volume of the semiconductors is not considered; cf. **Section 2.1**.
- Heat sink: thermal model for forced air cooling, power demand of the fan, boxed volume (heat sink plus fan); cf. **Section 2.2**.
- Inductor model: winding and core losses, thermal model, boxed volume; cf. **Section 3.1** and **3.2**.
- Capacitor model: boxed volume only (capacitor losses are neglected); cf. **Section 3.3**.
- Electrical converter model and filter design model: voltages and currents, predictions of CM and DM noise levels and filter component values to fulfill the design specifications; cf. **Chapter 4**.

Each component model facilitates the calculation of the respective loss components, the increases of the characteristic temperatures, and the

Table 5.2: Design variables for optimization.

Switching frequency of input-side	$f_{\mathrm{in,sw},n}$	8 kHz ... 40 kHz
Max. input phase current ripple	$\gamma_{\mathrm{in,i},n}$	5 % ... 40 %
Switching frequency of output-side	$f_{\mathrm{out,sw},n}$	8 kHz ... 40 kHz
Max. output current ripple	$\gamma_{\mathrm{in,i},n}$	5 % ... 40 %
Switching frequ. of DC–DC converter	$f_{\mathrm{dc,sw},n}$	8 kHz ... 40 kHz
Max. DC current ripple	$\gamma_{\mathrm{dc,i},n}$	5 % ... 40 %

component's partial volumes, as discussed in **Chapter 2** and **Chapter 3**. The losses and the increases of the component temperatures are coupled, e.g. the inductors' winding and core losses depend on the respective winding and core temperatures (according to their material properties) and vice versa (according to the properties of the inductor's thermal network, which includes the heat flux to the ambient). For this reason, not only accurate loss models, but also accurate thermal models are required. According to the list given above, a large number of publications related to component models are readily available. This is particularly true for the semiconductors [48] and the heat sink [49]. However, no detailed discussion of coupled electro-thermal models for inductors is available. Therefore, a coupled electro-thermal inductor model has been developed, implemented, and verified in this thesis (cf. **Section 3.1**).

Figure 5.1 depicts the flow chart of the optimization procedure. It automatically produces converter designs and calculates and stores the respective components' losses, temperatures, and volumes in a pool of design results. The models employed in this automatic design procedure are highly non-linear and, therefore, a large number of converter designs are studied in order to find the global optimum. Thus, in a first step, the Design Space is created for the considered power converter, which, for the AC–DC–AC part, is based on **Table 5.2**:[1]

- Switching frequencies of input and output side $f_{\mathrm{sw},n}$: from 8 kHz to 40 kHz with a step size of 1 kHz;
- rel. input and output inductor current ripples $\gamma_{\mathrm{i,in},n}$ and $\gamma_{\mathrm{i,out},n}$:

[1] This chapter is confined to the optimization of the AC–DC–AC part of the UPS, since the optimization of the DC–DC converter which is employed to interface the battery storage with the UPS DC-link, can be implemented in an analogous manner.

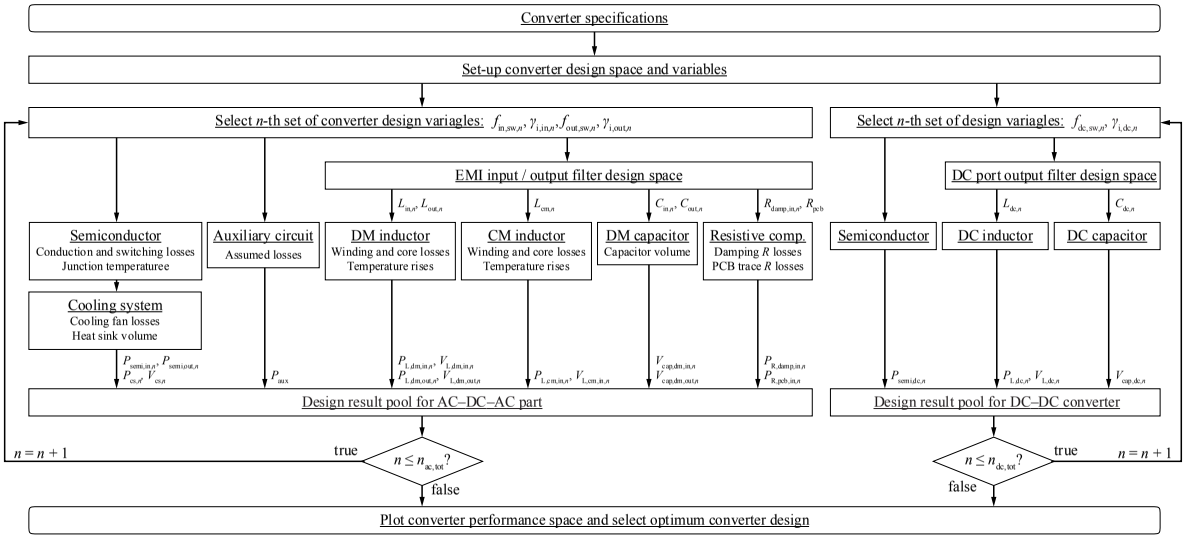


Figure 5.1: Block diagram of the optimization procedure used to determine the η–ρ Pareto front. $P_{\mathrm{semi},n}$, $P_{\mathrm{cs},n}$, $P_{\mathrm{L,dm},n}$, $P_{\mathrm{L,cm},n}$ $P_{\mathrm{R,damp},n}$ and $P_{\mathrm{R,pcb},n}$ denote the total losses of the semiconductors, the fans of the cooling system, the DM inductors, the CM inductors, the damping resistors and the PCB traces with the n-th set of design variables. P_{aux} and R_{pcb} denote the assumed total losses of the auxiliary circuit and the resistance of the PCB traces. $V_{\mathrm{cs},n}$, $V_{\mathrm{L,dm},n}$, $V_{\mathrm{L,cm},n}$, and $V_{\mathrm{cap},n}$ denote the total boxed volume of the cooling system (heat sink with fans), the DM inductors, the CM inductors, and the capacitors.

from 5% to 40% with a step size of 5%; the ratio of the maximum peak-to-peak inductor current ripple, $\Delta I_{\mathrm{L},n}$, to the amplitude of the current fundamental, $\hat{I}$, defines the relative current ripple:

$$\begin{aligned} \Delta I_{\mathrm{L}_{1,\mathrm{in}},n} &= \gamma_{\mathrm{in,i},n} \cdot \hat{I}_{\mathrm{in}}, \\ \Delta I_{\mathrm{L}_{1,\mathrm{out}},n} &= \gamma_{\mathrm{out,i},n} \cdot \hat{I}_{\mathrm{out}}; \end{aligned}$$

If required, the optimization procedure could also consider further design variables, e.g. the numbers of semiconductors operated in parallel for each switch or diode (treated here as constant; the actual numbers are given in **Table 2.3**), the base plate temperature of the heat sink (here, a base plate temperature of $\vartheta = 100\,^{\circ}\mathrm{C}$ is assumed), and the DC-link voltage (here: 720 V).

In the second step, the design procedure selects the n-th set of design variables from the Design Space and produces a single converter design. It calculates the semiconductor losses, $P_{\mathrm{semi,tot},n}$, and the respective junction temperatures for the assumed heat sink base plate temperature. With known semiconductor losses, the heat sink is optimized according to **Section 2.2**, which yields the total boxed volume of the cooling system, $V_{\mathrm{cs,tot},n}$, and the power demand of the fans, $P_{\mathrm{cs,tot},n}$. The values of the filter components are calculated according to **Chapter 4** in order to fulfill the design specifications and design variables. The total losses and the boxed volumes of the DM and CM inductors ($P_{\mathrm{L,dm,tot},n}$, $P_{\mathrm{L,cm,tot},n}$, $V_{\mathrm{L,dm,tot},n}$, $V_{\mathrm{L,cm,tot},n}$) are calculated with the inductor optimization procedure detailed in **Chapter 3**, which employs an inductor model that considers electro-thermal and magneto-thermal couplings. Furthermore, the total volume of all DM capacitors, $V_{\mathrm{C,dm},n}$, is determined for each converter design (the total volume of all the CM capacitors is found to be relatively small, i.e., negligible in the first step).

Based on all the power densities and efficiencies calculated for all converter designs, the η–ρ Pareto front can be generated in the Performance Space of the converter system, which, finally, facilitates the identification of the optimum converter design, which is discussed in following sections.

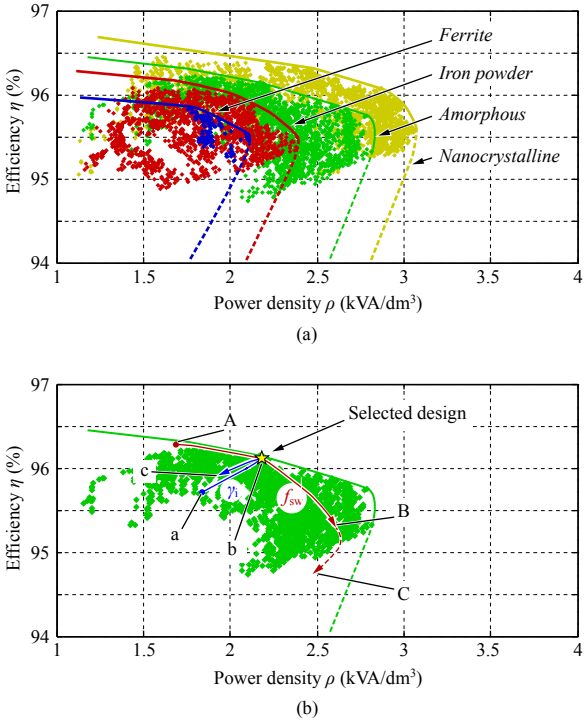


Figure 5.2: η–ρ Pareto front of the proposed UPS system with four different magnetic materials (a) and Pareto front with *amorphous material* (b).

5.2 Efficiency–power density Pareto front and discussion

Figure 5.2(a) shows the power densities and efficiencies calculated for all considered converter design points. Besides different switching frequencies and current ripples, different core materials are also considered for the DM inductors. According to these results, the highest efficiencies and highest power densities are achieved with *nanocrystalline materials*, due to the high saturation flux densities and the low core losses, even including the increased core losses with an air gap. The high saturation flux densities of *amorphous materials* also allow high power

densities. However, due to higher core losses, the achievable converter efficiencies are lower than the efficiencies achievable for *nanocrystalline materials*. Also *iron powder materials* can be used to realize the inductors. However, the permeabilities of these materials are lower than those of the other materials. In addition, the permeabilities drop with increasing flux densities, i.e., the inductances of inductors using *iron powder cores* show a non-linear dependency on the inductor current. As a consequence, the number of turns needs to be increased in order to maintain a given inductance value at an elevated current, which increases the winding losses. Due to the increased winding losses, the inductor volume has to be increased in order to respect the winding hot-spot temperature limit, which decreases the power density. Thus, for the given application, inductors using *iron powder cores* are found to be less suitable. Furthermore, *ferrite cores* are found to give comparably low power density and efficiency values, which is due to the low saturation flux density of *ferrite materials* and the relatively low switching frequencies used by reason of the employed semiconductors. Due to the high cost of *nanocrystalline materials* (23 €/kg) [22] and the comparably small difference in efficiency and power density, the *amorphous material* (16 €/kg) was selected for realizing the inductors of the converter.

Figure 5.2(b) shows how the Design Space is projected into the Performance Space:

- **Between points A and B on the red line in Figure 5.2(b)**, the *increase in switching frequency* at a constant current ripple of 20 % causes the power density to increase and the efficiency to drop. If the switching frequency exceeds a certain value, however, the power density drops (cf. **B–C in Figure 5.2(b)**); this is due to the additional converter volume needed to dissipate the heat (increased heat sink volume, additional volume of passive components due to thermal limitation).
- **Between points a and b on the blue line in Figure 5.2(b)**, the *increase in current ripple* at constant switching frequency of 16 kHz as used in the selected design causes the power density and the efficiency to increase, due to the reduction of the inductances, which helps to reduce the inductor winding losses and volumes; **between points b and c** the increasing current ripple starts to cause a deterioration in overall efficiency and power density due to the increasing inductor losses and the capacitor volumes. With higher current ripple at the same switching frequency, the inductor core losses are increased. In

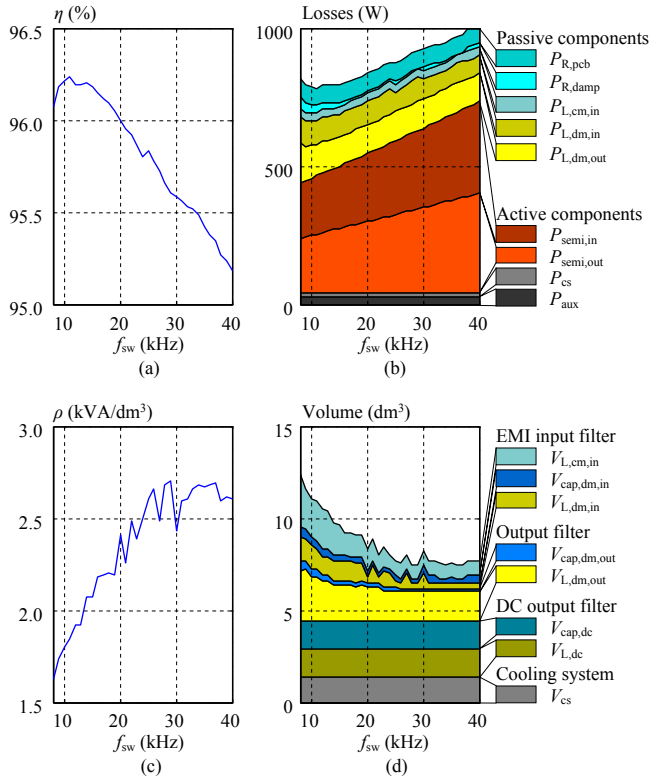


Figure 5.3: Influence of the design parameter switching frequency f_{sw} on the efficiency (a), the loss distribution (b), the power density (c), and the volume distribution (d). In this figure, the peak-to-peak current ripple is kept constant ($\gamma_i = 20\,\%$).

addition, in order to dissipate the increased heat, the inductor volumes cannot be reduced (thermal limit). Moreover, the volume of the DM capacitors increases in order to fulfill the HF voltage ripple specification with increased current ripple.

The efficiencies, loss distributions, power densities, and volume distributions calculated for different switching frequencies, constant relative input and output side current ripples of 20%, and inductors made of *amorphous cores* are shown in **Figure 5.3**. According to Figure 5.3(a), the efficiency drops with increasing switching frequency, which is mainly

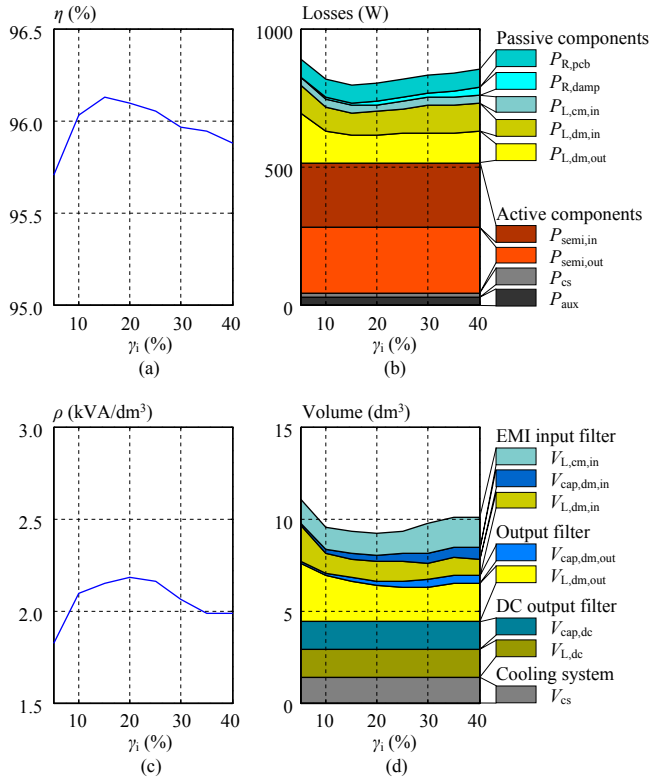


Figure 5.4: Influence of the design parameter current ripple γ_i on the efficiency (a), the loss distribution (b), the power density (c), and the volume distribution (d). In this figure, the switching frequency is kept constant ($f_{sw} = 16\,\text{kHz}$).

due to the switching losses of the power semiconductors. The power density improves with an increase in switching frequency due to the volume reduction of the passive components. However, it shows a maximum for a switching frequency of approximately 29 kHz, and no further improvement is seen with increasing switching frequency, due to the increasing HF core losses of the DM inductors and the required associated overall component surfaces needed to obey the thermal limits. A switching frequency of 16 kHz is selected in order to achieve a high efficiency and to avoid audible noise. At $f_{sw} = 16\,\text{kHz}$, the contribution

of the total semiconductor losses to the total converter losses is 59% and the contribution of the total passive components' losses is 36%. The contribution of the passive components, except the DC–DC converter inductors (DM inductors, capacitors, CM inductors and DC-link capacitors), to the total converter volume is 68%.

Figure 5.4 depicts the results calculated for different current ripples and constant switching frequency, $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$. In this case the maxima of efficiency and power density occur for similar current ripples (15% for maximum efficiency and 20% for maximum power density) on the input and output sides. According to Figure 5.4(b), the DM inductor losses decrease significantly between $5 \ldots 15\%$ current ripple, since a reduction of the inductance value significantly reduces the LF winding losses in the DM inductors. This helps to reduce the volume of the DM inductor and improves the overall power density (cf. Figure 5.4(c) and (d)). However, the DM inductor losses slightly increase for current ripples between $15\% \ldots 40\%$, due to increasing HF winding losses and core losses. Since the DM inductor losses are not decreasing, the DM inductor volume is also not decreasing in that range of current ripple. However, the DM capacitor volume increases, since the voltage ripple is kept constant and the current ripple increases. Therefore, the power density drops if the relative current ripples exceed 20%. In summary, in order to achieve a high power density, a current ripple of 20% has been selected.

5.3 Conclusion

The optimization procedure presented in this chapter employs a multi-domain approach which is based on component models that consider electric, magnetic, and thermal aspects. In particular, a coupled electro-thermal and magneto-thermal model of the inductors that features an accurate calculation of the losses, volumes, and hot-spot temperatures inside the windings contributes a detailed analysis of the relationship between Design Space and Performance Space. The presented results reveal that the system-level converter optimization based on the η–ρ Pareto front enables a high converter efficiency of 96.2% at a maximum power density of $2.3\,\mathrm{kVA/dm^3}$ for the investigated 20 kVA UPS system including the EMI input filter and the output filter. The relation between the η–ρ Performance Space and the f_{sw}–γ_{i} Design Space has been discussed and suitable design parameters for the converter system were

determined by projecting the selected performance points back into the Design Space. As a result, a switching frequency of 16 kHz, a current ripple of 20 %, and dedicated inductor realizations (DM inductors: *amorphous cores* and solid copper wires; CM inductors: *nanocrystalline cores* and solid copper wires) have been selected.

Chapter 6

Hardware prototype realization and comparison

As discussed in the previous chapter, the designs for each component, including the power semiconductors and associated heat sinks, DM / CM inductors, and DM capacitors, are optimized to achieve a high power density. **Table 6.1** summarizes the design parameters selected and the component values for the hardware realization. Summing the components' boxed volumes gives a total power density of $2.3\,\mathrm{kVA/dm^3}$. Typically, this value will likely fall by a factor of 2 to 3 when the actual hardware is built. This is because assembling components with a high density is relatively complex and most of the space will end up being occupied by air. In this chapter, Computer Aided Design (CAD) is employed to maximize the power density of the realized hardware. This is based on detailed 3D component models and virtual assembling of the converter system in the 3D CAD system ("3D virtual prototyping").

In the end, the total loss of the realized converter system is measured and compared with the calculated results in order to evaluate the proposed component models. In addition, the conducted EMI noise at the input side is also measured to confirm that the proposed EMI input filter design procedure satisfies the EMI requirement.

Table 6.1: Design parameters and component values for hardware realization.

Design parameters	
Switching frequencies	$f_{\mathrm{in,sw}} = f_{\mathrm{out,sw}} = f_{\mathrm{dc,sw}} = 16\,\mathrm{kHz}$
Current ripples	$\gamma_{\mathrm{in,i}} = \gamma_{\mathrm{out,i}} = \gamma_{\mathrm{dc,i}} = 20\,\%$
Component values for the EMI input filter	
DM inductors	$L_{1,\mathrm{in,r/s/t}} = 307\,\mu\mathrm{H}$, $L_{2,\mathrm{in,r/s/t}} = 31\,\mu\mathrm{H}$
DM capacitors	$C_{1,\mathrm{in,r/s/t}} = 10\,\mu\mathrm{F}$, $C_{2,\mathrm{in,r/s/t}} = 10\,\mu\mathrm{F}$
DM damping resistors	$R_{1,\mathrm{in,d}} = 7.6\,\Omega$, $R_{2,\mathrm{in,d}} = 2.5\,\Omega$
DM damping capacitors	$C_{1,\mathrm{in,d}} = 10\,\mu\mathrm{F}$, $C_{2,\mathrm{in,d}} = 10\,\mu\mathrm{F}$
CM inductors	$L_{1,\mathrm{cm}} = 3.8\,\mathrm{mH}$, $L_{2,\mathrm{cm}} = 4.4\,\mathrm{mH}$, $L_{3,\mathrm{cm}} = 0.5\,\mathrm{mH}$
CM capacitors	$C_{1,\mathrm{cm}} = 800\,\mathrm{nF}$, $C_{2,\mathrm{cm}} = 18\,\mathrm{nF}$
Component values for the output filter	
DM inductors	$L_{1,\mathrm{out,u/v/w/n}} = 686\,\mu\mathrm{H}$, $L_{2,\mathrm{in,u/v/w/n}} = 69\,\mu\mathrm{H}$
DM capacitors	$C_{1,\mathrm{out,u/v/w/n}} = 10\,\mu\mathrm{F}$, $C_{2,\mathrm{out,u/v/w/n}} = 10\,\mu\mathrm{F}$
DM damping resistor	$R_{2,\mathrm{out,d}} = 5.1\,\Omega$
DM damping inductor	$L_{1,\mathrm{out,d}} = 69\,\mu\mathrm{H}$
Component values for the DC output filter	
DM inductors	$L_{1,\mathrm{dc}} = L_{2,\mathrm{dc}} = 380\,\mu\mathrm{H}$
DM capacitors	$C_{1,\mathrm{bt}} = C_{2,\mathrm{bt}} = 22\,\mu\mathrm{F}$
DC-link capacitors	$C_{1,\mathrm{dc}} = C_{2,\mathrm{dc}} = 330\,\mu\mathrm{F}$

6.1 3D virtual prototyping and power density of actual realization

Figure 6.1 shows the PCBs and mechanical parts designed with 3D virtual prototyping. The figure also shows the footprint sizes of each PCB. The first step of 3D virtual prototyping only uses box models of the large components, such as inductors, capacitors and heat sink units, in order to determine their positions on the PCBs. Once the positions of the large components are fixed, the length of the sides of each PCB are determined and the PCBs are designed using the PCB CAD software, including detailed 3D models of the components. Mechanical parts such as heat sink units and the enclosure of the UPS system are designed on the mechanical CAD software.

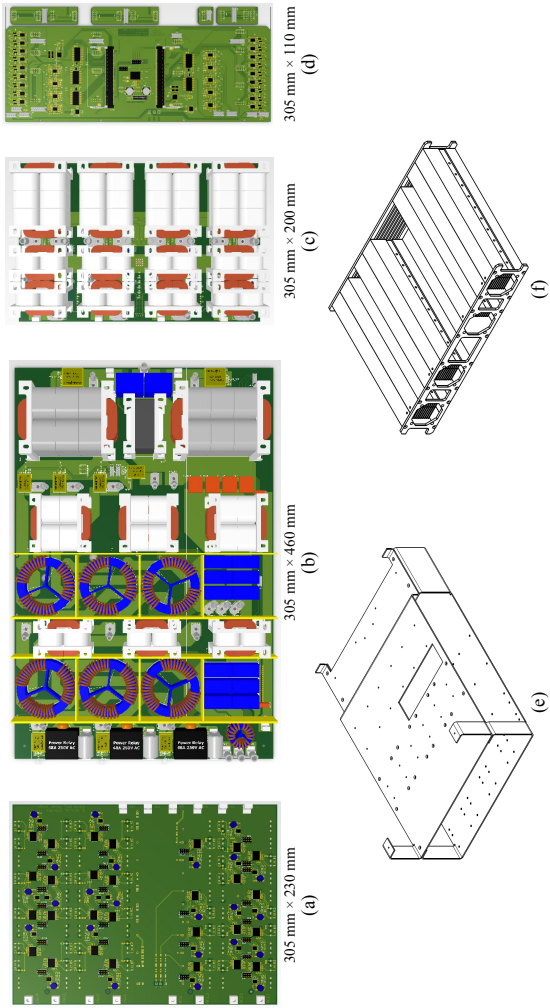


Figure 6.1: PCBs and mechanical parts designed with 3D virtual prototyping. (a) PCB of power semiconductors and gate drivers, (b) PCB of EMI input filter and DC output filter, (c) PCB of output filter, (d) PCB of control board, (e) 3D drawing of enclosure and (f) 3D drawing of heat sink. The relatively large share of empty space between components should be noted.

Figure 6.2: (a) Result of 3D virtual prototyping and (b) actual realization of the hardware. The power density resulting from virtual prototyping (0.9 kVA/dm^3) shows good agreement with actual power density.

Table 6.2: Comparison of measured and calculated losses for back-to-back operation at nominal output power.

Losses	Measured	Calculated	Difference	Error
Total	728.3 W	756.9 W	28.5 W	3.9 %
$P_{\mathrm{aux,tot}}$	23.9 W	23.9 W	—	—
$P_{\mathrm{cs,tot}}$	—	25.9 W	—	—
$P_{\mathrm{semi,tot}}$	—	397.8 W	—	—
$P_{\mathrm{L,dm,out}}$	—	106.8 W	—	—
$P_{\mathrm{L,dm,in}}$	—	77.8 W	—	—
$P_{\mathrm{L,cm,in}}$	—	44.6 W	—	—
$P_{\mathrm{R,damp}}$	—	15.3 W	—	—
$P_{\mathrm{R,pcb}}$	64.8 W	64.8 W	—	—

All the designed 3D components including PCBs are, then, virtually assembled in the 3D CAD system as shown in **Figure 6.2(a)**. The total power density of the UPS system is estimated from the 3D virtual prototyping to be approximately $0.9\,\mathrm{kVA/dm^3}$. This shows good agreement with the actual realization of the hardware which is shown in **Figure 6.2(b)**. Here, it is interesting to mention that the power density of the actual realization is about 2.6 times smaller than the power density ($2.3\,\mathrm{kVA/dm^3}$) calculated without consideration of clearance spaces. A reduction by a factor of three provides a simple and conservative estimate of the actual power density starting from the pure (boxed) component volumes.

6.2 Loss measurements

The total loss of the realized hardware was measured using a YOKOGAWA precision power analyzer WT3000 and compared with the calculated losses. In order to perform a meaningful comparison, the ambient temperature was also measured during the loss measurement and used in the loss calculation for comparison. The ambient temperature was measured at the front of the EMI input filter, i.e. at the inlet of the cooling system.

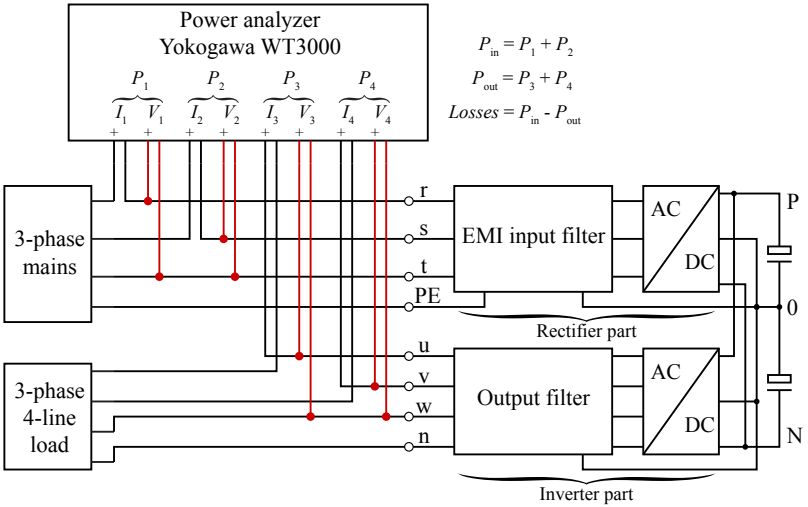


Figure 6.3: Loss measurement set-up for back-to-back operation configuration.

6.2.1 Double-conversion: Back-to-back operation

Figure 6.3 shows the loss measurement set-up for the back-to-back operation configuration. The AC three-phase input power and AC three-phase output power are measured on a power analyzer and the conversion loss and efficiency are calculated at different output power levels. The power consumptions of the cooling fans and auxiliary circuits such as DSPs, FPGAs and current / voltage sensors are measured by DC multi-meters separately and added into the total measured power losses. **Figure 6.4** shows the loss and efficiency curves for the measured and calculated results. The measured and calculated loss distribution and calculation error relative to the measured result at nominal output power are summarized in **Table 6.2**. At a nominal output power of 20 kVA, the difference between the measured and calculated losses is 28.5 W, which gives an error of only 3.9 %. The measured efficiency at nominal output power is approximately 96.5 %, which shows a good agreement with the calculated efficiency of 96.4 %. In order to perform a fair comparison with the measurement result, the losses are re-calculated with the ambient temperature of the measurement environment. In **Chapter 5**, the worst case ambient temperature of

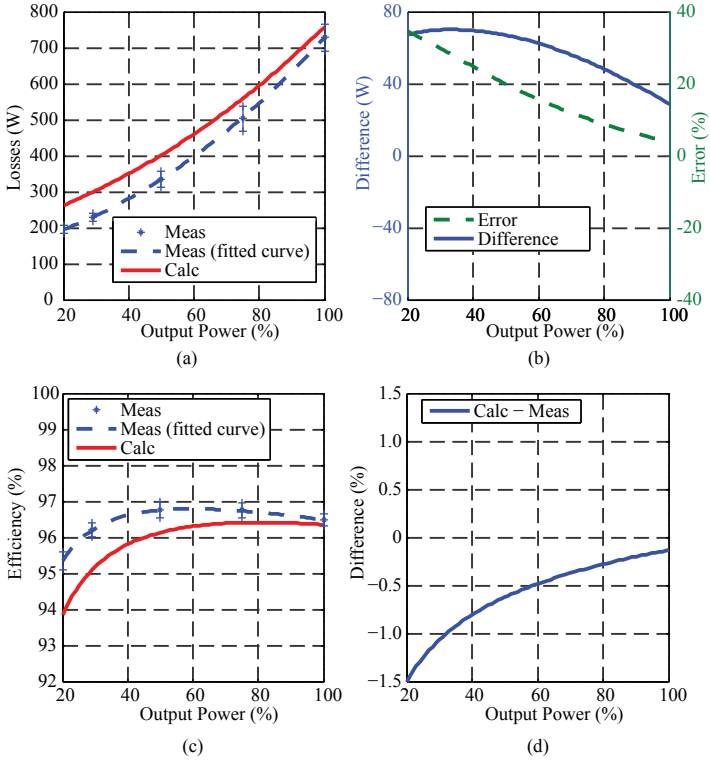


Figure 6.4: (a) Measured and calculated loss characteristics, (b) difference of measured and calculated losses, (c) measured and calculated efficiency curve, and (d) difference of measured and calculated efficiencies.

55 °C was used for design optimization. Here, the measured ambient temperature of 30 °C was used for comparison; slightly reduced losses of the semiconductors and inductors are calculated according to the lower temperatures of the components. Such comparison is enabled with the proposed coupled electro-thermal / magneto-thermal loss calculation model. As a result, the calculated efficiency (96.4 %) is higher than the optimization result (96.2 %).

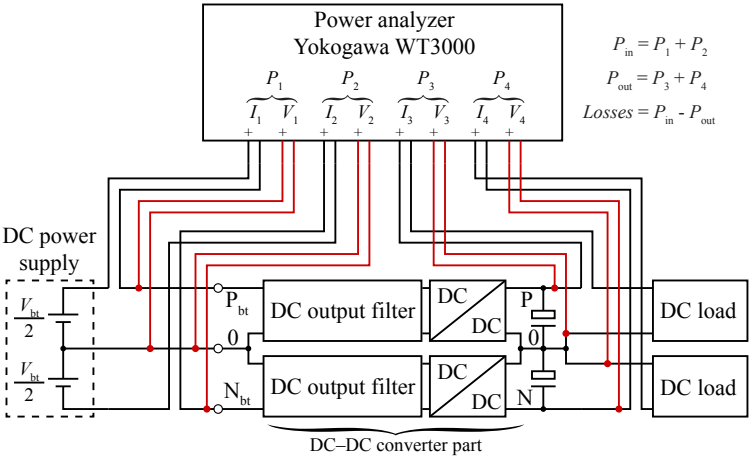


Figure 6.5: Loss measurement set-up for DC–DC converter part.

Table 6.3: Comparison of measured and calculated losses for the DC–DC converter part at nominal output power.

Losses	Measured	Calculated	Difference	Error
Total	380.6 W	378.2 W	−2.4 W	−0.6 %
$P_{\mathrm{aux,tot}}$	20.8 W	20.8 W	—	—
$P_{\mathrm{cs,tot}}$	—	25.9 W	—	—
$P_{\mathrm{semi,dc}}$	—	229.8 W	—	—
$P_{\mathrm{L,dc}}$	—	101.7 W	—	—

6.2.2 DC–DC converter

Figure 6.5 shows the loss measurement set-up for the DC–DC converter part. The input power at the battery connection port and the output power on the DC-link side are measured by a power analyzer, and the conversion loss and efficiency are calculated at different operating points and / or output power levels. **Figure 6.6** shows the measured and calculated loss and efficiency characteristics. The measured and calculated loss distributions and the calculation error relative to the measured results at nominal output power are summarized in **Table 6.3**.

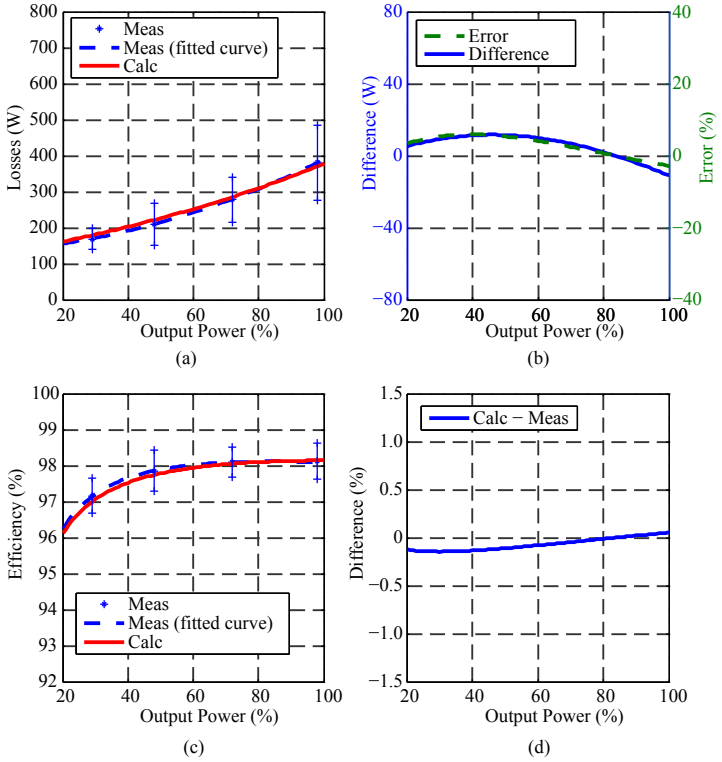


Figure 6.6: (a) Measured and calculated DC–DC converter loss characteristics, (b) difference of measured and calculated losses, (c) measured and calculated efficiency characteristics, and (d) difference of measured and calculated efficiencies. At nominal output power of 20 kW, the difference between the measured and calculated loss is −2.4 W which gives an error of only −0.6 %. The measured efficiency at nominal output power achieves approximately 98.1 % which shows very good agreement with the calculated efficiency of 98.1 %.

6.3 EMI measurement

Figure 6.7 shows the EMI measurement set-up. During the EMI measurement, the UPS system is operated in back-to-back configuration at 75 % of nominal output power due to the power limit of the employed

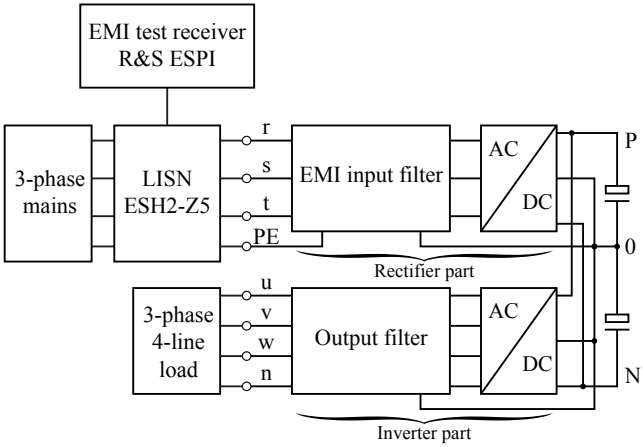


Figure 6.7: EMI measurement set-up.

LISN circuit ROHDE & SCHWARZ ESH2-Z5 [1]. The quasi-peak (QP) noise emissions for frequencies ranging from 150 kHz to 30 MHz were measured using an EMI test receiver (ROHDE & SCHWARZ ESPI Test Receiver). The result is shown in **Figure 6.8**. The measurement result shows that the designed EMI input filter fulfills the required EMI standard (CISPR 11 Class A, QP standard) at all three-phases. However, it must be mentioned that the attenuation at low frequencies (< 1 MHz) is lower than the calculated result. This is due to the parasitic components of the filter capacitor and inductors. For example, a parasitic inductance in series with the capacitor or a parasitic capacitance in parallel with the inductor is not avoidable. Accordingly, there is a strong requirement for advanced assembling techniques that can reduce these parasitic inductances and capacitances. It should also be mentioned that higher noise levels are observed around 3.3 MHz and 5.6 MHz. This is due to the switching noise of the gate driver's power supply. When only the gate driver's power supply is running before the main converter part is operated, these noise peaks are already present.

[1] It was experimentally confirmed that the difference in EMI noise emission level between 100 % and 75 % of nominal output power is negligibly small.

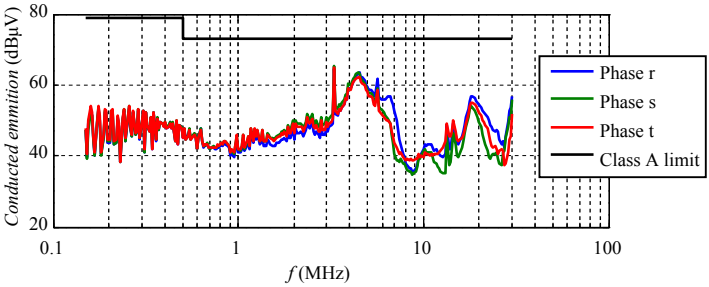


Figure 6.8: EMI measurement result.

6.4 Conclusion

In this chapter, the realized hardware and its loss and EMI measurement results are shown and compared with the calculation results. A 3D virtual prototyping approach was employed in order to maximize the power density of the actual hardware. This resulted in a power density of 0.9 kVA/dm^3; accordingly it can be concluded that a reduction by a factor of three provides a reasonable, conservative estimate of the actual power density relative to the calculated value. The loss measurement results show good agreement with the calculations; the error at nominal output power was lower than 5 %, which is accurate enough to be used for converter design in industrial applications. The EMI measurement results also show that the proposed EMI input filter design procedure is able to fulfill the required EMI standard which allows to avoid trial and error corrections after the hardware is produced. However, there is room for future improvements in estimating the effect of the parasitic components, CM noise from the output loads, and EMI noise emission from the gate drivers or the auxiliary circuit, which have not been considered in this work.

Chapter 7

Conclusions and outlook

7.1 Conclusions

In this thesis, the system-level optimization of a 20 kVA three-phase UPS system which employs a three-level T-type topology has been performed and suitable design parameters for high efficiency and high power density have been investigated.

Chapter 2 detailed a modeling method of the active components, such as the power semiconductors and related cooling systems. In **Section 2.1**, a detailed coupled electro-thermal loss calculation model of the power semiconductors has been introduced. The switching losses for the different combinations of IGBTs and diodes has been measured and a detailed comparison of the total semiconductor losses was given. It was shown that a suitable combination of the power semiconductors for the input side rectifier comprises SiC SBDs for the high- and low-side rectifying diodes and a bi-directional switch realized with anti-parallel Si RB-IGBTs for the NPC switch. SiC SBDs considerably reduce the switching losses, not only because of their nearly negligible reverse recovery losses but also due to the lower turn-on losses of the bi-directional switches. In addition, the conduction losses are reduced by using Si RB-IGBTs since only a single device is involved in the current conduction path. As a result, the combination of SiC SBDs and Si RB-IGBTs achieves minimum semiconductor losses for the input-side rectifier in a very wide switching frequency range ($8\,\text{kHz} \leq f_{\text{sw}} \leq 40\,\text{kHz}$). A suitable combination of the semiconductors for the output-side inverter is

Si IGBTs for high- and low-side switches and the bi-directional switch realized with anti-series connected SiC SBDs / Si IGBTs for the NPC switch. Since the bi-directional switches are mainly operated as diodes in inverter operation, the realization with anti-series connected SiC SBDs / Si IGBTs has advantages for the reduction of switching losses at high switching frequencies. As a result, this combination achieves minimum semiconductor losses of the output-side inverter for switching frequencies $f_{sw} \geq 8\,\text{kHz}$. A suitable combination of the power semiconductors for the DC–DC converter part is SiC SBDs and Si IGBTs due to the reduction of the switching losses contributed by the SiC SBDs. In **Section 2.2**, a detailed volume optimization procedure for the heat sink has been introduced. The volume of the heat sink is minimized by maximizing the CSPI. It has been shown that the two-sided configuration is advantageous for increasing the CSPI. Two design criteria, the minimum required averaged thermal resistance of the heat sink and the minimum required heat sink length for mounting the devices, have been discussed as constraints for the volume reduction. Since the semiconductor losses are minimized, the minimum required thermal resistance was not difficult to satisfy. On the other hand, the minimum required heat sink length became the main limitation for the volume reduction of the heat sink. This is due to employing a multi-level topology with discrete semiconductor packages. As a result, the heat sink volume stays constant over the considered switching frequency range.

Chapter 3 details a modeling method for passive components, such as the inductors and capacitors which are used in the filters. A detailed thermal modeling of the magnetic components under natural convection cooling has been introduced. Three fundamental heat transfer mechanisms, i.e. conduction, convection, and radiation, are considered in order to calculate the thermal resistance network model of the inductor. Under the natural convection cooling condition, the contribution of radiation to the total heat transfer was not negligible. The accuracy of the introduced thermal model of the inductor was experimentally verified and the error in the calculated hot-spot temperature rises was less than 15 %.

In **Chapter 4**, detailed filter design procedures for a two-stage EMI input filter, two-stage output filter, and DC output filter were given. The filter design procedures are based on the Design Space approach, including the EMI conducted noise estimation method. Damping components are also included for the EMI input filter and output filter.

As all filter components are considered in these design procedures, it is possible to perform an automatic filter design based on the introduced design procedure.

Chapter 5 details an automatic system-level design optimization procedure and a systematic investigation of system performances, in terms of efficiency and power density, for a 20 kVA UPS system. The total system efficiencies and power densities with four different magnetic materials were investigated over a wide range of switching frequencies f_{sw} and relative current ripples γ_i of the inductors, and subsequently, the most suitable design parameters were selected: $f_{sw} = 16\,\text{kHz}$ and $\gamma_i = 20\,\%$, yielding an efficiency of 96.4 % and a power density of $2.3\,\text{kVA/dm}^3$ with the amorphous material.

In **Chapter 6**, a virtual prototyping with detailed 3D-models of the components was performed in order to determine the power density of a practical realization of the UPS system. As a result, a power density of $0.9\,\text{kVA/dm}^3$ was determined and practically realized. The total losses and efficiencies of the realized hardware of this 20 kVA UPS system were experimentally measured and compared with the calculated results. The comparison showed that the measured total efficiency of 96.5 % at nominal output power shows less than 5 % error compared to the calculated value. The EMI noise emission level was also tested and the measured result showed that the realized filter satisfies the required EMI standard.

7.2 Outlook

In this thesis, a system-level optimization procedure was introduced and implemented as a way of enabling an automatic system design, including a consideration of the EMI filter design. In addition, a coupled modeling of the losses and thermal behavior for a variety of components has been covered. However, there are still some aspects that could be addressed in the course of further research in this regard:

- A detailed loss analysis and modeling of the auxiliary circuits, such as the gate drivers and power supplies, should be considered in the future. Since the losses of the main power components, such as the power semiconductors and inductors, have been intensively discussed and minimized, the contribution of the auxiliary circuits to the total losses has increased, relatively.

- An EMI noise estimation model that considers the parasitic components of the inductors, capacitors and the loads at the output side. In addition, conducted EMI noise from the gate drivers and auxiliary circuit would be one of the EMI issues to analyze in future.

- An advanced integration technique for the power semiconductors and cooling systems is required for further improvement of the power density. In this thesis, a physical limitation for the volume reduction of the cooling system was given by spatial issues instead of thermal issues. This was due to employing discrete semiconductor packages and separate heat sinks. The optimization and comparison could be done in a next step employing a power semiconductor module or PCB integrated power semiconductors. Furthermore, power modules with integrated heat sinks and different cooling techniques, such as water cooling or phase-change cooling, should be discussed and modeled in the future.

- The modeling and experimental verification of forced cooling of magnetic components could be considered. In order to increase the total power density, the magnetic components must be mounted without enough space for natural convection. Accordingly, forced convection cooling must be provided.

- In order to extend the number of dimensions in the Performance Space, the costs of the components should be analyzed and modeled in the future. In addition, the thermal resistance model which is discussed in this thesis should be extended to a thermal impedance model for considering the thermal cycle, failure rate and reliability in the Performance Space.

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