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Ultra-Efficient Three-Phase Buck-Type PFC Rectifier Systems

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Science should be free - free as in speech!

The first principle is that you must not fool yourself
and you are the easiest person to fool.

Richard Feynman

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Abstract

Today electric power is produced, transmitted and distributed almost exclusively by ac-based systems, however, a number of applications require a direct current, supplied at a tightly regulated voltage. Among these are LED lamps, electric vehicles, as well as information and communication technology equipment, such as mobile phones, computers and servers. Loads with a maximum power of $\approx 4\,\mathrm{kW}$ or more are typically supplied by a three-phase ac system, as this reduces the cabling effort and avoids the low-frequency power pulsations of single-phase ac supplies. In many applications, regulations require the rectifier to achieve near-sinusoidal mains input currents, in phase with the ac voltage, to avoid the distortion of other equipment connected to the mains by low-frequency (typ. $\leq 2.5\,\mathrm{kHz}$) current harmonics. Circuits which are capable to do so are commonly called three-phase *Power Factor Correction* (PFC) rectifiers.

Depending on the achievable dc-to-ac voltage ratio, three-phase PFC rectifiers can be classified into boost- (dc larger than ac line-to-line amplitude), buck- (dc lower than minimum of the ac line-to-line envelope), or buck-boost-type (dc larger or lower than ac) circuits. All three types may provide galvanic isolation between input and output. Generally, boost-type PFC circuits have received far more attention in scientific literature than buck-type system, even though several applications could potentially benefit from buck-type rectifiers. Among those are the fast charging of electric vehicle batteries, dc microgrids, envisioned as more efficient distribution grids in residential areas and office buildings and dc powered data centers. In these cases a dc voltage between $\approx 200\,\mathrm{V}$ and $\approx 450\,\mathrm{V}$ is required, which is within the range of buck-type PFC rectifiers supplied by a three-phase mains with a line-to-line voltage of 400 V rms or higher. Therefore, four different buck- and buck-boost-type PFC rectifiers are studied in this thesis, regarding aspects such as mains current harmonics, reactive power generation and achievable efficiency.

This thesis starts with an overview of non-isolated and isolated single-

stage three-phase PFC rectifier circuits, indicating their inventors and citing original publications. Out of 40 topologies, the non-isolated buck-type SWISS Rectifier and the integrated active filter (IAF) rectifier, as well as the isolated Phase-Modular Indirect Matrix-Type Y/Δ (IMY/D) rectifier and the matrix-type dual active bridge (DAB) rectifier are selected for further analysis.

The SWISS and the IAF circuit both use an input rectifier stage commutated at mains frequency, followed by a dc-dc conversion stage enabling output voltage control and sinusoidal mains currents. Several aspects of the SWISS Rectifier's modulation, control and circuit design are analyzed in this thesis: A modulation scheme is proposed that allows the generation of reactive power by phase shifting the input currents with respect to the mains voltages up to ±30°. Under unbalanced and/or distorted mains voltages, the SWISS Rectifier's usual control scheme results in distorted input currents which is undesirable. Ohmic mains behavior can be achieved using a proposed extension of the control circuit. Furthermore, distortions of the SWISS Rectifier's mains currents occur when two mains voltages intersect, which creates low-frequency harmonics in the rectifier's input currents. Based on a comprehensive analysis, a small modification to the SWISS Rectifier is proposed which allows a temporary pulse width modulation of the input stage in order to mitigate these distortions. Another option considered in this thesis, is to use an interleaved dc-dc converter which also allows to reduce conduction losses and/or increase the output power as the load current is split among two or more semiconductor devices. To reduce the number of inductive components required for an interleaved SWISS Rectifier, a novel close-coupled magnetic device, constructed from four U cores, is proposed and analyzed. Using this concept, an 8 kW interleaved SWISS Rectifier is designed for the highest possible efficiency as benchmark. The prototype uses commercially available 1.2 kV Silicon Carbide (SiC) MOSFETs in hard switching and has a power density of 4 kW/dm^3. Calorimetric loss measurements confirm a peak efficiency of 99.26 % at 60 % load and 99.16 % at full-load, including all auxiliary losses such as gate drivers, control and cooling.

Over the last decades data centers have become a significant consumer of electric power, with an estimated annual electricity consumption of 300 TW h. Published data indicates that systems built before the year 2005 used only about half of the consumed power for actual information technology equipment such as servers, while the other half amounted from conversion and distribution losses, air conditioning and ventilation. The resulting high operating costs started a trend towards lower conversion and cooling losses, eventually leading to new standards for 380 V dc distribution systems. Eco-

nomic considerations for telecommunication power supplies, regarding the trade-off between capital expenditure and operating costs, which results from investing in more expensive, but less lossy components, have been published already in 1978 by Goldstein at al. Their approach is extended in this thesis to select cost-optimal semiconductors, magnetic components and switching frequencies, allowing the design of life-cycle-cost optimal power converters. Considering a service life of ten years and 24/7 operation, an 8 kW IAF rectifier for 380 V dc data center applications is designed as an example. At rated load a cost-optimal efficiency of 99 % and a power density of 4 kW/dm^3 result for a rectifier using 1.2 kV SiC MOSFETs and inductors made from nanocrystalline material and rectangular wires. Measurement results confirm the calculated efficiency and compliance with CISPR 11 Class B conducted electromagnetic emission limits.

As some applications require a galvanic isolation between the ac mains and the dc output, isolated rectifier circuits are analyzed in this thesis as well. An interesting option is the phase-modular IMY/D rectifier, built from three isolated single-phase phase-modules, which are similar to a dc-dc forward converter. These phase-modules can be connected to the mains either in star- or delta-configuration, which allows a wide input voltage range. A phase-shift modulation strategy is described, which enables zero voltage switching (ZVS) for sufficiently high output currents, similar to a conventional dc-dc forward converter. Using this modulation scheme, the rectifier's control is very similar to that of a dc-dc buck converter and therefore simple to implement. Furthermore, a third harmonic current injection scheme is proposed for delta-configuration, which allows to increase the rectifier's output voltage or to reduce its conduction losses. Combined with the ZVS modulation scheme the conversion losses of a 7.5 kW hardware prototype are reduced by 10 %, resulting in a full-load efficiency of 97.2 %.

The last circuit topology analyzed in this thesis is the isolated matrix-type dual active bridge rectifier. It consists of a three-to-two line direct matrix converter on the primary-side, an isolation transformer designed with a sufficiently large leakage inductance and a full-bridge of switches on the secondary-side. Besides the input filter inductors, the isolation transformer is the only magnetic component, which is favorable as transformers and inductors typically account for a significant amount of losses, volume and cost in PFC rectifiers. Based on an equivalent circuit model a nonlinear optimization problem is formulated to calculate a modulation function that achieves sinusoidal input currents with minimal conduction losses. The obtained solution achieves ZVS for a sufficiently large output power and zero

current switching otherwise. Again, an 8 kW hardware demonstrator with a power density of 4 kW/dm^3 is built using 900 V SiC MOSFETs. Measurements confirm a full-load efficiency of 99.0 % and an input current total harmonic distortion of 3.0 %, for a loss-optimal switching frequency of 31 kHz.

The direct matrix converter used in the isolated matrix-type dual active bridge rectifier requires sophisticated multi-step commutation patterns, resulting in a relatively complex modulator. A modified circuit, called *Zurich Rectifier*, is proposed in this thesis that utilizes the same modulation scheme but replaces the direct matrix converter with a input rectifier stage followed by a T-type inverter. Calculations indicate that this circuit achieves the same or lower losses than the original design, but it requires at least two more MOSFETs and six additional diodes.

The theoretical and measurement results obtained in this thesis show that ultra-efficient three-phase buck-type PFC rectifiers are technically feasible using different non-isolated and isolated circuit topologies. A key element to build PFC rectifiers in the $\approx$ 10 kW range with efficiencies of 99 % and above, are the low conduction and switching losses of SiC MOSFET devices. While these are (currently) significantly more expensive than conventional Si MOSFETs or IGBTs, the proposed life cycle cost driven design approach shows that these efficiencies are economically feasible for applications like data centers, which typically operate 24/7 and have relatively high costs for cooling and standby generators. Further research could address life-cycle-cost-optimal converter design for applications like the fast charging of electric vehicle batteries, as significant infrastructure investments are required in the future to meet ambitious plans to increase the number of electric vehicles. With newly invented circuit topologies, improving semiconductor devices and magnetic materials, the analysis, evaluation and comparison of circuit topologies for different applications remains an ongoing task.

Kurzfassung

Die Produktion, Übertragung und Verteilung von elektrischer Energie erfolgt heute nahezu ausschliesslich mit Wechselspannungssystemen, jedoch benötigt eine Reihe von Verbrauchern präzise geregelte Gleichspannungen. Darunter fallen zum Beispiel LED Leuchtmittel, Elektrofahrzeuge, und Geräte der Informations- und Kommunikationstechnik, wie Mobiltelefone, Computer oder Server. Verbraucher mit einer maximalen Leistungsaufnahme von ca. 4 kW oder mehr, werden typisch aus dem dreiphasen Wechselspannungsnetz gespeist, da dies die Leitungsverluste reduziert und die in einer Einphasenspeisungen inhärent auftretende Leistungspulsation mit doppelter Netzfrequenz vermeidet. In vielen Anwendungen schreiben Regulierungen zudem den Bezug von nahezu sinusförmigen Strömen durch die Last vor um eine Störung anderer Verbraucher durch niederfrequente (typ. < 2.5 kHz) Harmonische des Laststromes zu vermeiden. Schaltungen die diese Anforderungen erfüllen werden üblicherweise als Gleichrichter mit Leistungsfaktorkorrektur (Power Factor Correction, PFC) bezeichnet.

Abhängig vom zulässigen Verhältnis von Gleich- und Wechselspannung können Dreiphasen-Gleichrichter in Systeme mit Hochsetzsteller- (Gleichspannung grösser als Spitzenwert der Aussenleiterwechselspannung), Tiefsetzsteller- (Gleichspannung kleiner als Minimum der positiven Einhüllenden der Aussenleiterwechselspannung) oder Hochtiefsetzstellercharakteristik (Gleichspannung grösser oder kleiner als Wechselspannung) eingeteilt werden. Weiters existieren sowohl Schaltungen ohne, als auch solche mit galvanischer Trennung zwischen Wechsel- und Gleichspannungsseite. Generall sind PFC Gleichrichterschaltungen mit Hochsetzstellercharakteristik in der wissenschaftlichen Literatur weitaus ausführlicher beschrieben als jene mit Tief- und Tiefhochsetzstellercharakteristik, obwohl einige Anwendungen von Gleichrichtern mit Tiefsetzstellercharakteristik profitieren könnten. Darunter fallen zum Beispiel: Schnelladegeräte für Elektrofahrzeuge, zukünftige lokale Gleichspannungsverteilnetze in Wohngebieten oder Bürogebäuden, sowie Rechenzentren mit Gleichspannungsverteilung. In diesen Fällen wer-

den Gleichspannungen im Bereich von ≈ 200 V bis ≈ 450 V benötigt, was bei einer Speisung aus dem Dreiphasennetz mit einer Aussenleiterspannung von 400 V einen Gleichrichter mit Tiefsetzstellercharakteristik bedingt. Daher werden in dieser Dissertation vier unterschiedliche Gleichrichterschaltungen mit Tiefsetzsteller- bzw. Hochtiefsetzstellercharkteristik hinsichtlich auftretender Störströme, möglicher Blindleistungserzeugung, und der erreichbaren Effizienz untersucht.

Die Arbeit beginnt mit einem Überblick über nicht isolierte und isolierte Dreiphasen-Gleichrichter mit Leistungsfaktorkorrektur, wobei die jeweiligen Erfinder und die frühesten verfügbaren Publikationen genannt werden. Von diesen etwa 40 Topologien werden der nichtisolierte SWISS Gleichrichter und der Gleichrichter mit Integriertem Aktivem Filter (IAF), sowie der isolierte phasenmodulare indirekte matrixartige Y/Δ Gleichrichter und der isolierte matrixartige Dual Active Bridge (DAB, zwei aktive Brücken) Gleichrichter vertieft untersucht.

Sowohl der SWISS, als auch der IAF Gleichrichter, verwenden einen nur mit Netzfrequenz kommutierten, aktiven Gleichrichter, welcher eine Gleichspannungswandlerstufe zur Erzeugung sinusförmiger Eingangsströme und zur Spannungsanpassung speist. Verschiedene Aspekte der Modulation, Steuerung, Regelung und Implementierung des SWISS Gleichrichters werden untersucht: Es wird ein Modulationsschema vorgeschlagen welches Phasenverschiebungen der Netzströme bis ±30° gegenüber den Strangspannungen erlaubt und somit die Erzeugung von kapazitiver oder induktiver Blindleistung ermöglicht. Beim Betrieb an unsymmetrischen oder nicht sinusförmigen Netzspannungen führt das bekannte Regelungsverfahren des SWISS Gleichrichters zu verzerrten Eingangsströmen, weshalb eine Modifikation der Regelstruktur vorgeschlagen wird, welche ohmsches Netzverhalten des Gleichrichters ermöglicht. Ausserdem weisen die Netzströme des SWISS Gleichrichters Verzerrungen an den Schnittpunkten der Strangspannungen auf, was zum Auftreten von tieffrequenten Harmonischen in den Netzströmen führt. Basierend auf einer eingehenden Analyse und Modellierung dieses Effekts wird eine Modifikation der Schaltungsstruktur vorgeschlagen, welche eine temporäre Pulsbreitenmodulation der Eingangsstufe erlaubt, wodurch die Stromverzerrungen vermieden werden. Ein weiterer Ansatz zu deren Vermeidung besteht in der Verwendung zweier Gleichspannungswandlerstufen welche verschränkt getaktet werden, wodurch die Spannungsrippel an den Eingangsfilterkondenstoren, und somit auch die Stromverzerrungen reduziert werden. Weiters ist dadurch eine Reduktion der Leitverluste oder eine Erhöhung des maximalen Ausgangsstromes möglich. Um den Realisie-

rungsaufwand der benötigten induktiven Komponenten zu verringern wird eine neuartige Magnetkomponente vorgeschlagen deren ferromagnetischer Kern aus vier konventionellen U-Kernen zusammengesetzt ist. Basierend auf diesem Konzept wird ein 8 kW SWISS Gleichrichter mit verschränkter Taktung und höchstmöglichem Wirkungsgrad entworfen. Der Prototyp verwendet hart schaltende, kommerziell erhältliche, 1.2 kV Siliziumcarbid (SiC) MOSFETs und erreicht eine Leistungsdichte von 4 kW/dm^3. Kalorimetrische Verlustmessungen bestätigen einen maximalen Wirkungsgrad von 99.26 % bei 60 % Last sowie 99.16 % unter Volllast, wobei alle Verluste von Hilfsbetrieben wie Schalteransteuerung, Regelung und Kühlung enthalten sind.

Mit einem geschätzen jährlichen Bedarf von 300 TW h sind Rechenzentren im Verlauf der letzten Jahrzehnte zu einem signifikanten Verbraucher von elektrischer Energie geworden. Studien zufolge wird in Rechenzentren die vor 2005 gebaut wurden nur etwa die Hälfte der bezogenen Leistung für Informationstechnologie-Geräte wie Server aufgewendeten. Die zweite Hälfte entfällt auf Umwandlungs- und Verteilungsverluste, sowie Kühlung und Ventilation. Die daraus resultierenden hohen Betriebskosten führten zu einem Trend in Richtung höherer Wirkungsgrade und tieferer Kühlungsverluste und zur Etablierung von neuen Standards für 380 V Gleichspannungsverteilung. Ökonomische Überlegungen zu Gleichrichtern in Telekommunikationsanwendungen, insbesondere die Beziehung zwischen Investitions- und Betriebskosten, welche durch die tendenziell höheren Anschaffungskosten effizienterer Bauteile resultiert, wurden bereits 1978 durch Goldstein et al. publiziert. Dieser Ansatz wird hier erweitert zu einem Verfahren zur Auswahl von kostenoptimalen Schaltern, Magnetkomponenten und Schaltfrequenzen, womit die Dimensionierung von hinsichtlich Lebenszykluskosten optimalen Konverter möglich wird. Als Anwendungsbeispiel wird ein 8 kW IAF Gleichrichter für 380 V Gleichspannungsverteilungen in Rechenzentren dimensioniert und implementiert, wobei durchgehender Betrieb über eine Lebensdauer von 10 Jahren angenommen wird. Für Nennlast resultiert ein kostenoptimaler Wirkungsgrad von 99 % bei einer Leistungsdichte von 4 kW/dm^3, wobei kommerziell verfügbare 1.2 kV SiC MOSFETs und nanokristalline Kerne mit Wicklungen aus Rechteckdrähten verwendet werden. Messergebnisse bestätigen den berechneten Wirkungsgrad sowie die Kompatibilität mit den CISPR 11 Klasse B Grenzwerten für leitungsgebundene Störströme.

Einige Anwendungen von dreiphasen Gleichrichtern erfordern zusätzlich eine galvanische Trennung zwischen dem Wechselspannungsnetz und dem Gleichspannungsausgang. Daher sind auch potentialgetrennte Gleichrichter Gegenstand dieser Arbeit. Eine interessante Topologie ist der isolierte

phasen-modulare indirekte matrixartige Y/Δ Gleichrichter, welcher aus drei isolierten einphasigen Phasenmodulen besteht, wobei jedes dieser Module ähnlich einem Vollbrückendurchflusswandler aufgebaut ist. Die Phasenmodule können netzseitig entweder in Stern (Y) oder Dreieck (Δ) geschaltet werden, woraus ein weiter Eingangsspannungsbereich resultiert. Ein Modulationsschema, basierend auf Phasenmodulation, wird in dieser Arbeit beschrieben. Es erlaubt spannungsloses Schalten bei ausreichend grossen Ausgangsströmen, ähnlich wie in einem konventionellen Durchflusswandler. Mit diesem Modulationsschema ist das regelungstechnische Verhalten des Gleichrichters sehr ähnlich einem Gleichspannungstiefsetzsteller, wodurch die Regelung des Gleichrichters mit besonders einfachen Verfahren erfolgen kann. Zusätzlich wird ein Steuerverfahren analysiert welches bei Dreieckschaltung der Phasenmodule die Erzeugung eines Kreisstromes dreifacher Netzfrequenz erlaubt und dadurch eine Erhöhung der Ausgangsspannung und/oder eine Reduktion der Leitverluste erlaubt. Zusammen mit dem Modulationsschema für spannungsloses Schalten ergibt sich an einem 7.5 kW Prototyp eine Reduktion der Verluste um 10 % unter Volllast und es wird ein Wirkungsgrad von 97.2 % erreicht.

Die vierte Schaltung welche in dieser Arbeit analysiert wird ist der isolierte matrixartige DAB Dreiphasen-Gleichrichter, welcher aus einem direkten Dreiphasen-Einphasen-Matrix-Konverter, einem Isolationstransformator mit ausreichend hoher Streuinduktivität und einer sekundärseitigen Vollbrücke aus vier Schaltern besteht. Abgesehen vom Eingangsfilter, stellt der Transformator die einzige magnetische Komponente dar, was vorteilhaft ist da Transformatoren und Induktivitäten üblicherweise für einen signifikanten Teil der Verluste, der Kosten und des Volumens von PFC Gleichrichtern verantwortlich sind. Basierend auf einer Ersatzschaltung wird ein nichtlineares Optimierungsproblem formuliert um eine Modulationsfunktion zu berechnen welche sinusförmige Eingangsströme mit minimalen Leitverlusten erlaubt. Die gefundene Lösung führt zu spannungslosem Schalten aller Halbleiter für ausreichend hohe Ausgangsleistungen, anderenfalls zu stromlosem Schalten. Wiederum wird ein 8 kW Prototyp mit einer Leistungsdichte von 4 kW/dm^3 entworfen welcher 900 V SiC MOSFETs verwendet. Messungen zeigen einen Volllastwirkungsgrad von 99.0 % und einen Oberschwingungsgehalt (THD) von 3.0 % bei einer Schaltfrequenz von 31 kHz.

Der verwendete direkte Matrix-Konverter erfordert komplexe mehrstufige Kommutierungssequenzen woraus ein relativ hoher Implementierungsaufwand des Modulators resultiert. Daher wird eine weitere abwandelte Schaltung vorgeschlagen in welcher der direkte Matrix-Konverter durch einen

netzfrequent kommutierten aktiven Gleichrichter und eine T-Typ Inverterbrücke ersetzt wird. Die resultierende Schaltung wird als *Zürich Gleichrichter* bezeichnet und verwendet die gleichen Kurvenformen für die Transformatorspannungen. Berechnungen zeigen, dass verglichen mit dem direkten Matrix-Konverter die gleichen oder geringere Gesamtverluste resultieren. Der *Zürich Gleichrichter* benötigt zwei zusätzliche MOSFETs und sechs zusätzliche Dioden, benötigt aber keine mehrstufigen Kommutierungssequenzen.

Die theoretischen und experimentellen Ergebnisse dieser Arbeit zeigen, dass hocheffiziente Dreiphasen-Gleichrichter mit Tiefsetzstellercharakteristik mittels verschiedenen nicht isolierten und isolierten Schaltungen realisierbar sind. Die tiefen Leit- und Schaltverluste moderner SiC MOSFETs stellen dabei eine Schlüsselkomponente für die Erreichung von Wirkungsgraden $\geq 99\,\%$ bei Leistungen im Bereich von $\approx 10\,\mathrm{kW}$ dar. Obwohl diese Bauelemente (gegenwärtig) wesentlich teurer sind als vergleichbare MOSFETs oder IGBTs aus Silizium, zeigt die vorgeschlagene Dimensionierung basierend auf Lebenszykluskosten, dass Konverter mit SiC Schaltern und diesen Wirkungsgraden bereits heute in Anwendungen wie Rechenzentren ökonomisch sinnvoll sind. Dies ist der Fall da Serveranlagen üblicherweise durchgehend (24/7) betrieben werden und vergleichsweise hohe Kosten für Kühlung und Notstromaggregate aufweisen, welche auch die Gleichrichterverluste abdecken müssen. Weitergehende Forschung könnte das Konzept lebenskostenoptimaler Gleichrichter auf andere Gebiete, wie zum Beispiel das Schnellladen der Batterien elektrischer Fahrzeuge erweitern, insbesondere da signifikante Investitionen nötig sein werden um bestehende, ambitionierte Pläne zur Ausweitung der Elektromobilität umzusetzen. Durch neu entwickelte Schaltungen, verbesserte Halbleiterbauelemente und magnetische Kernmaterialien bleiben die Analyse, die Evaluation und der Vergleich von Schaltungen für unterschiedliche Anwendungen weiterhin eine Aufgabe der wissenschaftlichen Forschung im Bereich der Leistungselektronik.

Abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
CAPEX	Capital Expenditure
CMC	Common-Mode Choke
CPU	Central Processing Unit
DAB	Dual Active Bridge
DC	Direct Current
DCSR	Delta-Type Current Source Rectifier
DMC	Direct Matrix Converter
ELV	Extra-Low Voltage
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ETSI	European Telecommunications Standards Institute
EV	Electric Vehicle
GaN	Gallium Nitride
GTO	Gate Turn-Off Thyristor
HF	High-Frequency
HV	High-Voltage
IAF	Integrated Active Filter
ICT	Inter-Cell Transformer
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IMDAB3R	Isolated Matrix-Type DAB Three-Phase Rectifier
IMY/D	Isolated Matrix-Type Y/Δ Rectifier
LCC	Life Cycle Cost
LED	Light Emitting Diode
LF	Low-Frequency
LUT	Lookup Table
LV	Low-Voltage
M2LC	Modular Multilevel Converter

MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MV	Medium Voltage
NLP	Nonlinear Programming
NPC	Neutral Point Clamped
OPEX	Operational Expenditure
PFC	Power Factor Correction
PHEV	Pluggable Hybrid Electric Vehicle
PUE	Power Usage Efficiency
PV	Photovoltaic
PWM	Pulse-Width Modulation
QAB	Quad Active Bridge
RB-IGBT	Reverse-Blocking IGBT
RB-IGCT	Reverse-Blocking IGCT
RES	Renewable Energy Source
RMS	Root Mean Square
SCR	Silicon Controlled Rectifier
SELV	Safety Extra Low-Voltage
Si	Silicon
SiC	Silicon Carbide
SQP	Sequential Quadratic Programming
SST	Solid State Transformer
TCO	Total Cost of Ownership
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

Arguably, the history of rectifier systems starts with the discovery of induction by Michael Faraday in 1831, which lead to the creation of the first generator using a magnet rotated beneath a coil of copper wire by Hippolyte Pixii in the following year. As the ac currents caused by the induced ac voltage were of little use, a commutator was added as mechanical rectifier effectively forming a dc generator [1, 2]. Electric power conversion without rotating machinery started around 1900 with the investigation of a mercury arc in an evacuated chamber. Initially they were investigated as light sources, but they could be employed as rectifier by using a liquid mercury electrode inside an evacuated chamber as cathode and one or more anodes, typically made from carbon or other solid conductors [3]. No moving parts are required and evaporated mercury condenses on the chamber's walls and flows back to the cathode, effectively renewing it. This allowed higher efficiency, smaller size and lower cost compared to rectifier systems based on rotating machines, but typically required a high-voltage generator and auxiliary electrode to ignite the arc [4]. In **Fig. 1.1** the picture of a three-phase half-wave rectifier can be seen. Additional control grids placed around the anodes allowed to delay the time at which the current transferred from one anode to another, thereby controlling the dc output voltage. This also enabled the construction of mercury-arc based inverter circuits which created a three-phase ac voltage

Fig. 1.1: Photograph of a three-phase half-wave mercury-arc rectifier. Manufacturer, model and technical specifications are unknown. At the bottom a wire can be seen which contacts the mercury cathode, the electrode which is used to ignite an arc at startup is located on the left below one of the three main arms. Each arm contains an anode within a wire cage that, most-likely, serves as control grid allowing to delay the anode's firing, similar to a thyristor's gate contact. (Device courtesy of Prof. J. W. Kolar).

from a dc input [5]. Mercury-arc rectifiers, enclosed in steel tanks, with power ratings of up to 3 MW were developed for railway applications during the 1920's and 1930's [6]. Also around 1900 the vacuum tube diode was invented by John Flemming, which too allowed the rectification of ac currents and was used in wireless receivers [7]. While not requiring a high-voltage ignition circuit, it uses an incandescent cathode that limits its life time. From the 1950's on metallic rectifiers based on metal-semiconductor or heterogeneous semiconductor junctions made from copper oxide, copper sulfide or selenium were used as power rectifiers, essentially starting power electronics. Typically many individual rectifier disks or plates were connected in series, forming stacks, as the blocking voltage of a single junction was limited to $\approx 20\,\mathrm{V}$ [6]. Note that also solid-state power rectifiers (diodes) and transistors, based on germanium p-n junctions, with power ratings of up to 100W, were reported already in 1952 [8].

Thyristors, also known as silicon controlled rectifiers (SCR), were invented in 1956 [9], based on the research of p-n-p-n semiconductor structures published as early as 1952 [10]. In **Fig. 1.2** the picture of a modern, medium voltage, high-power thyristor is shown. In the off-state these devices do not conduct current between the anode and cathode terminals for both voltage polarities. However, if a current pulse is provided to the gate terminal (called 'firing') while the potential of the anode is higher than that of the cathode a current flow from anode to cathode starts and the voltage between the terminals decreases to $\approx 1\,\mathrm{V}$ within a few µs. This enabled the development of a large number of new circuits and can be seen as the beginning of modern power electronics. Also, SCRs allowed to build rectifier systems that can control the dc output voltage by adjusting the thyristors' firing-angle. No mechanical contacts, such as transformer tap-changers, or saturable inductors are required to control the output voltage. Furthermore, the output voltage can be reversed to allow a power flow from the dc-side back to the ac mains, which is called inverter operation [11]. Commercial devices with a current rating of 16 A and blocking voltages up to 300 V became available from *General Electric* as early as 1959 [12]. While these early devices were typically commutated at mains frequency only, pulse width modulation schemes based on triangular carriers, or on optimized pulse patterns to reduce low order harmonics, have been studied in the 1960s [13]. Typically all controllable rectifiers built with thyristors require an inductor on the dc-side, which ensures an almost constant dc output current. An inductance value significantly higher than that of the feeding mains and/or transformer is required. The maximum dc output voltage is limited to that of a conventional diode rectifier and occurs when the thyristors are fired at the point in time were the corresponding diode would start to conduct.

1.1 Three-Phase Power Factor Correction Rectifier Circuits

Today, dc loads with more than $\approx 3.6\,\mathrm{kW}$, i.e. an equivalent single-phase ac input current of 16 A rms for a 230 V rms mains voltage, are typically supplied from the three-phase ac mains. This is due to regulatory limitations on single-phase loads in the mains and allows to reduce the amount of copper installed in the ac mains cabling as the neutral conductor can be omitted for a symmetric three-phase load. Furthermore, a continuous power can be drawn from the three-phase mains, which means that fewer energy needs to

Fig. 1.2: Photograph of a thyristor manufactured by *BBC*, rated for 4.2 kV blocking voltage and 5.5 kA rms current. The top surface serves as anode and the bottom one is connected to the cathode; the small contact on the left-hand side is the gate which is used to control the device. Inside the ceramic package a round silicon wafer with ≈ 10 cm (4 in) diameter is placed between molybdenum discs serving as electrical and thermal contact. (Device courtesy of Prof. J. W. Kolar).

be stored in the rectifier compared to single-phase systems that inherently have a power pulsation due the input voltage's sinusoidal shape.

Standards, such as *IEC 61000-3-2* (< 16 A), *IEC 61000-3-4* (> 16 A) and *IEEE 519*, pose regulations on the ac input current shape by restricting the allowed amplitude of harmonics in order to ensure the interoperability of systems connected to the public three-phase mains. Rectifier systems which are, in the ideal case, capable of creating purely sinusoidal input currents, or at least input currents with a total harmonic distortion (THD) of less than 5 %, are called *Power Factor Correction* (PFC) rectifiers. Note that conventional six-pulse diode rectifiers with low-frequency smoothing inductors either at the ac input or the dc output typically achieve power factors greater than 90 %, but their mains currents contain low-frequency harmonics (5^{th}, 7^{th}, 11^{th}, 13^{th}, ...) which lead to a THD of ≈ 30 %. So, despite its name, PFC rectifiers are not only used to achieve a power factor close to unity (typ. ≥ 99 %) but also to reduce the THD of the mains currents and to provide a controlled dc output voltage [14].

The two basic three-phase PFC rectifier circuits are shown in **Fig. 1.3**: In **(a)** the three-phase two-level boost-type PFC rectifier is shown, which consists of three ac input inductors L_{ac}, each connected between one of the mains input terminals a, b, c and a half-bridge built from two reverse-conducting switches. These three half-bridges are connected in parallel to a capacitor C_{dc} and the dc output terminals p and n. Note that the six diodes connected in antiparallel

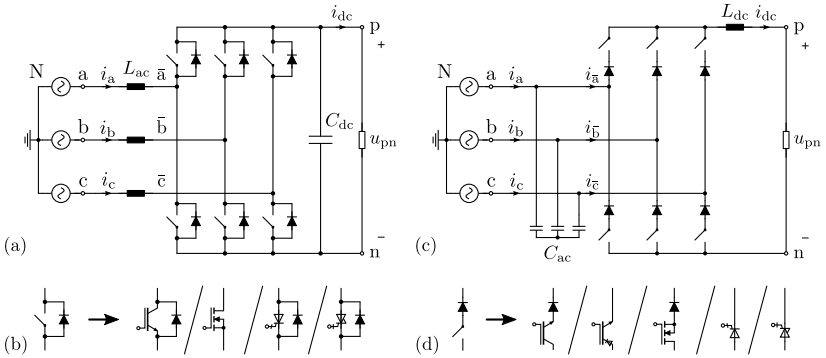

Fig. 1.3: Basic two-level three-phase PFC rectifiers: **(a)** Circuit diagram of the six-switch boost-type PFC rectifier which requires switches with bidirectional conduction, but only unidirectional voltage blocking capability. **(b)** Shows different implementation options for bidirectionally conducting switching cells: Insulated Gate Bipolar Transistor (IGBT) & Diode, MOSFET, Gate Turn-Off Thyristor (GTO) & Diode, Integrated Gate-Commutated Thyristor (IGCT) & Diode. **(c)** Circuit diagram of the six-switch buck-type PFC rectifier. Implementation options of the required switches with bidirectional blocking capability and unidirectional conduction are shown in **(d)**: IGBT & series Diode, Reverse-Blocking IGBT (RB-IGBT), MOSFET & series Diode, GTO, Reverse-Blocking IGCT.

to the switches in **(a)** essentially form a six-pulse diode rectifier. This implies that the dc output voltage u_{pn} needs to be at least as high as the peak of the ac line-to-line voltage, similar to the output voltage of a dc-dc boost converter, which can only be higher or equal to its (maximum) input voltage. Hence this classifies a boost-type rectifier. As shown in **(b)**, different semiconductor components can be used to implement the required switches. The most common options are: an antiparallel connection of an Insulated Gate Bipolar Transistor (IGBT) and a diode, a MOSFET, a Gate Turn-Off Thyristor (GTO) with an antiparallel diode and an Integrated Gate-Commutated Thyristor (IGCT) with an antiparallel diode.

The most basic three-phase buck-type rectifier is shown in **Fig. 1.3(c)**. It consists of three input filter capacitors C_{ac}, which can be connected either in Y (as shown in **Fig. 1.3**) or in delta-configuration, followed by three half-bridges of reverse-blocking switches and an inductor L_{dc} on the dc output side to ensure a constant/continuous output current i_{dc}. Accordingly, the rectifier's switches and diodes distribute the dc-side current among the phases

and/or directly impress the input currents $i_{\bar{a}}$, $i_{\bar{b}}$ and $i_{\bar{c}}$. Hence this circuit is also called *Current Source Rectifier* (CSR). Note that at least one of the three top-side switches and at least one of the three bottom-side switches needs to be turned on at all times to provide a valid conduction path for i_{dc}. Considering the voltage conversion of the system, the switches are used to select one line-to-line mains voltage, or a short circuit, and apply it to the series connection of L_{dc} and the load. Therefore the dc output voltage u_{pn} can only be lower than the minimum of a six-pulse diode rectifier's output voltage. Unlike in the boost-type rectifier, the switches need to block the mains line-to-line voltages and hence need to block voltage in both directions, however, they need to conduct current only in one direction. Such switches can be implemented with different semiconductor component arrangements. The five options shown **Fig. 1.3(d)** are: a series combination of an IGBT and a diode, a Reverse-Blocking IGBT (RB-IGBT), a MOSFET and a series diode, a Reverse-Blocking GTO and finally a Reverse-Blocking IGCT (RB-IGCT).

Even though the two circuits shown in **Fig. 1.3** are called PFC *rectifiers*, both allow a bidirectional power flow between the ac mains and the dc terminals p and n. In the boost-type PFC rectifier the switches can be used to create mains currents i_a, i_b, i_c which are 180° phase shifted compared to the corresponding ac voltages, which leads to the reversal of i_{dc}. This mode is typically referred to as inverter operation. Note that the sign of dc output voltage u_{pn} remains the same for both, rectifier and inverter operation. To achieve inverter operation in the buck-type PFC rectifier, the dc output voltage is reversed (i.e. $u_{pn} < 0$) while the sign of the dc output current i_{dc} remains the same for rectifier and inverter mode.

The rectifiers shown in **Fig. 1.3** can be seen as the most basic circuit topologies, with the lowest number of switches, diodes, inductors and capacitors, that implement a boost- or buck-type three-phase PFC rectifier. For both, boost- and buck-type PFC rectifiers a number of modifications and variants have been proposed in order to reduce losses, volume and/or costs of the circuits or to reduce the required modulation and control circuit's complexity. A brief overview of alternative boost- and buck-type circuits, without making a claim to be complete, is given in the following.

1.1.1 Multi-Level Boost-Type PFC Rectifier Circuits

In the conventional boost-type PFC rectifier (cf. **Fig. 1.3(a)**) each of the switching nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ can either be connected to the positive (p) or the negative (n) dc output terminal, hence this circuit is classified as a *two-*

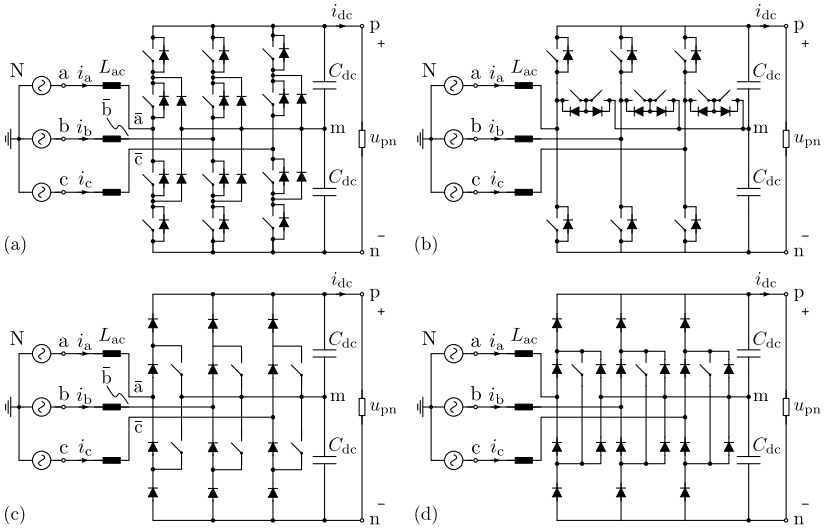

Fig. 1.4: Boost-type three-level three-phase PFC rectifier circuits: **(a)** The *Neutral Point Clamped* (NPC) rectifier, which can be modulated such that all semiconductors have to block only $u_{pn}/2$, was proposed by Baker in 1979 [15]. **(b)** Variant of the previous circuit called *T-type* rectifier, proposed by Holtz in 1977 [16]. **(c)** The *Force Commutated Three-Level Boost-Type* rectifier can be seen as a simplified version of the NPC circuit, were switches which never conduct any current in rectifier operation are omitted. It was published by Zhao et al. in 1993 [17]. **(d)** By adding six diodes only three switches are required; resulting in the original three-switch *VIENNA* Rectifier introduced by Kolar and Zach in 1994 [18].

level rectifier. The circuits shown in **Fig. 1.4** use a series connection of two capacitors C_{dc} to form a node m. Together with additional switches and/or diodes this allows the nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ to be connected to either p, m or n. Therefore the four circuits shown in **Fig. 1.4** are classified as *three-level* rectifiers.

In **Fig. 1.4(a)** the three-level *Neutral Point Clamped* (NPC) rectifier is shown. This circuit was filed as patent application by Baker in 1979 [15] and published by Akagi et al. in 1981 [19] for inverter applications. The concept of the *T-type* rectifier shown in **Fig. 1.4(b)** was proposed by Holtz in 1977 [16] and by Akagi et al. in 1981 [19] as three-point inverter. The additional output voltage level at nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ reduces the swichting frequency current ripple in the machine currents, or of the line input currents for a rectifier respectively,

thereby reducing losses. Compared to a two-level rectifier [cf. **Fig. 1.3(a)**] lower switching losses result as the three-level converters switch the same ac mains currents over only half the dc voltage. Furthermore in the *Neutral Point Clamped* (NPC) rectifier [cf. **Fig. 1.4(a)**] and in the rectifier topologies depicted in **Fig. 1.4(c)** and **Fig. 1.4(d)** all semiconductors need a blocking voltage rating of only half the dc voltage u_{pn}. This either allows operation with higher ac and dc voltages for a given semiconductor technology or to use switches and diodes with a lower blocking voltage rating. This is not the case for the *T-type* rectifier shown in **Fig. 1.4(b)** where the outer switches and diodes (connected to the p or n rail) need to be rated for the full dc voltage u_{pn}. However, the number of semiconductor elements in the conduction path is reduced, which can lead to a significant reduction of conduction losses if pn-junction based elements, such as IGBTs and pn-diodes are used. Note that the switches and diodes allowing a connection of L_{ac} to node m have to block only half of u_{pn}.

As the NPC and the T-type rectifier were originally proposed as inverter circuits it is apparent that they allow a power transfer from the dc voltage u_{pn} to the ac mains. While this is beneficial for certain applications, for example by enabling recuperation in active-front-end rectifier stages of motor drives, or even required as in solar inverters, there are also applications which do not require a bidirectional power transfer, such as power supplies for telecommunication equipment. In this case several switches can be omitted in order to reduce the cost and/or the volume of the converter. One circuit, called *Force Commutated Three-Level Boost-Type Rectifier* and proposed by Zhao et al. in 1993, is shown in **Fig. 1.4(c)** [17]. The switching nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ can be connected to node m by simultaneously turning on both switches in the bridge leg. When the switches are turned off, the corresponding mains current's sign determines the conduction state of the diodes and hence whether the switching node is connected to output node p or n. The number of switches can be reduced further using a *VIENNA Rectifier* described by Kolar et al. in 1994 and shown in **Fig. 1.4(d)** [18]. Compared to **Fig. 1.4(c)** six additional diodes are required and a higher number of devices in the conduction path result.

Under certain conditions a further reduction of the volume and/or of the losses of the rectifier's input filter inductors L_{ac} can be achieved by increasing the number of voltage levels k generated by the switching stage. One possible approach uses $k-1$ two-level half-bridges and combines their switching nodes via close-coupled inductors sometimes also called *Inter-Cell Transformers* (ICT) as shown in **Fig. 1.5(a)** for $k = 4$ voltage levels [22–25]. While this approach

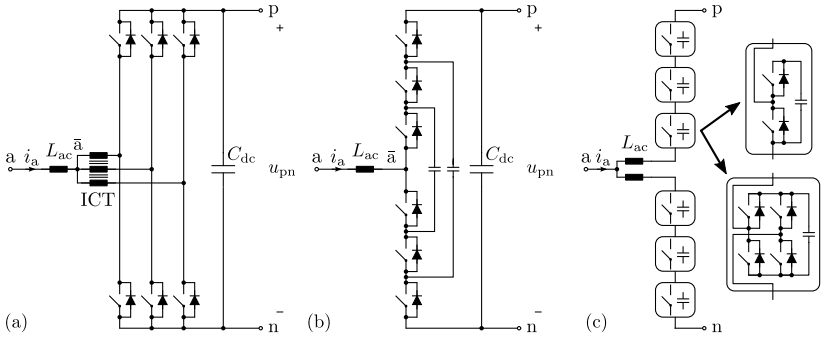

Fig. 1.5: Bridge legs for boost-type multi-level PFC rectifier circuits: **(a)** Bridge leg using three two-level half-bridges combined via an Inter-Cell Transformer (ICT) yielding four different voltage levels at node ā. **(b)** Four level *Flying Capacitor Converter* bridge leg introduced in [20] and **(c)** *Modular Multi-Level Converter* (M2LC). [21]

allows a reduction of the current ripple at the mains input and at the dc output, an additional magnetic device is required, which potentially increases costs and volume of the converter. Furthermore, all semiconductors need to block the full dc voltage u_{pn} but conduct only the $(k-1)$ part of the mains current i_a which implies that this circuit is suitable for applications with comparably low voltages but large mains currents. An equal current sharing between the different bridge legs can either be assured by proper dimensioning of the components or by feedback control of the measured bridge leg currents.

For medium voltage (MV) applications (i.e. $> 1\,\mathrm{kV}$) usually several semiconductors need to be connected in series due to the high dc voltage u_{pn} and the limited blocking voltage capability of available semiconductor devices. A possible solution is the flying capacitor structure proposed by Meynard and Foch in 1992 and shown in **Fig. 1.5(b)** for $k = 4$ voltage levels [20]. Two additional capacitors are used to ensure a symmetric sharing of the blocking voltage between the series connected switches and to create the additional voltage levels at the switching node ā. Special feedback control can be used to ensure that the flying capacitors' voltages remain close to their set point values.

A more modular approach, which is used for MV and high-voltage (HV) applications, such as solid state transformers (SST) and high-voltage dc (HVDC) transmission, is the modular multilevel converter shown in **Fig. 1.5(c)** which uses two strings of series-connected cells [26]. Each one is formed by a capacitor connected to either a half- or full-bridge of switches. Note that

only a low-voltage (compared to the total dc-link voltage) dc-link capacitor is required as it is essentially integrated into the cells. The general concept can be traced back to a patent filed in 1969 by McMurry, however, the circuit was used as inverter and each cell was connected to an isolated dc power supply [21].

Several further boost-type three-phase rectifier topologies have been suggested in the literature: For example circuits with only two switches such as the two-switch *TAIPEI* PFC rectifier [27] and the *MINNESOTA* rectifier [28], as well as circuits based on a star- or delta-configuration of switches [29] or using a mains-frequency *Scott* transformer which performs a Clarke transformation of the mains voltage [30]. These circuits are not discussed further in this thesis.

This concludes the description of boost-type rectifiers given here as an overview. In the following three-phase buck-type PFC rectifiers, some of which are derived from the basic circuit shown in **Fig. 1.3(c)**, are described.

1.1.2 Buck-Type Three-Phase PFC Rectifier Circuits

The three-phase six-switch buck-type PFC rectifier [cf. **Fig. 1.3(b)**] has two main drawbacks compared to boost-type three-phase rectifiers: First, only one out of three semiconductors (of the upper or lower half of the full-bridge) conducts current at a time, while one out two switches (of each bridge leg) conducts in the boost-type rectifier. Second, the currents $i_{\tilde{a}}$, $i_{\tilde{b}}$ and $i_{\tilde{c}}$ flowing into the half-bridges are discontinuous, which leads to a comparatively large voltage ripple at the input filter capacitors C_{ac}. As these are connected to the ac mains voltages they generate reactive power which reduces the rectifier's power factor and hence the maximum capacitance value which can be installed is limited. This implies that a trade-off between high-frequency noise currents and the rectifier's power factor exists. Several buck-type PFC rectifier circuits, which have been invented to address also these issues, are briefly discussed in the following.

Fig. 1.6(a) shows the *Delta-Type Current Source Rectifier* (DCSR) introduced by Guo et al. in 2014 [31, 32]. By adding six additional diodes to the conventional six-switch buck-type rectifier, two bottom and/or two top-side switches can conduct current simultaneously for certain switching states. This improves the utilization of the switches and/or reduces conduction losses compared to the conventional circuit. A full-load efficiency of 98 % is measured on an 8 kW prototype rectifier in [32].

In 1996 Tooth et al. proposed a *Five-Level Current Source Converter* (5L-

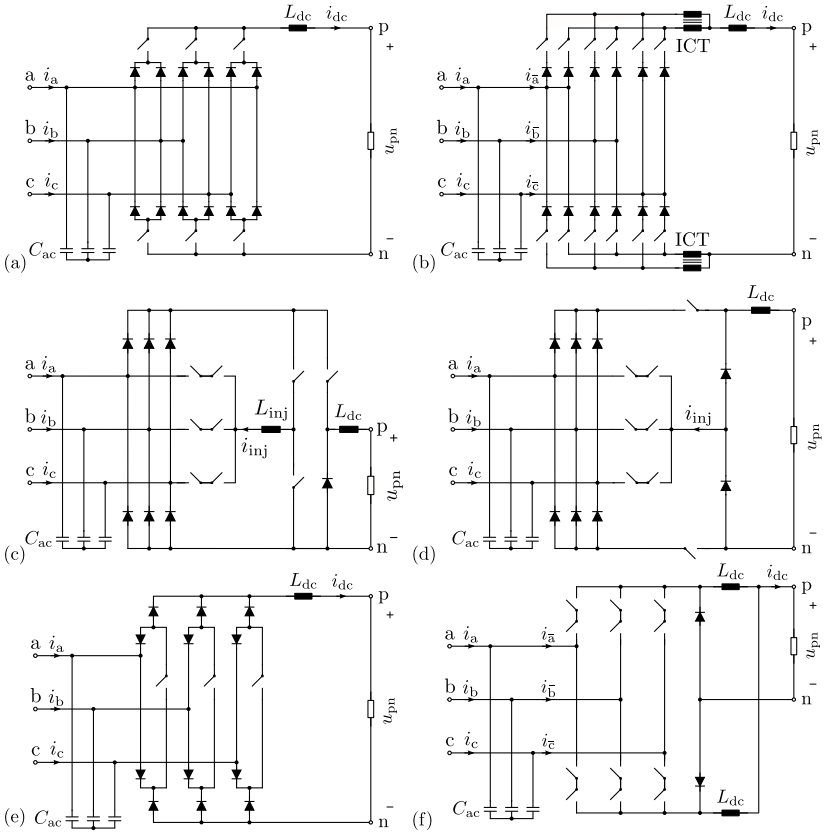

Fig. 1.6: Three-phase buck-type PFC rectifier circuits: **(a)** The *Delta-Type Current Source Rectifier* uses additional diodes to reduce the switches' conduction losses [31, 32]. **(b)** The *Five-Level Current Source Rectifier* consists of two conventional six-switch buck-type rectifiers where the dc currents are split/combined using inductors or ICTs [33, 34]. This increases the number of current levels in $i_{\bar{a}}$, $i_{\bar{b}}$, $i_{\bar{c}}$ and reduces the input capacitor voltage ripple [35]. **(c)** The *Integrated Active Filter* (IAF) rectifier consists of a six-pulse diode rectifier, a current injection network that acts as an active filter ensuring sinusoidal mains currents and an output buck converter [36]. **(d)** The *SWISS Rectifier* uses an input stage similar to the IAF rectifier and two buck-type dc-dc converter stages to achieve sinusoidal mains currents [14, 37]. **(e)** The *Three-Switch Rectifier* can be seen as the buck-type version of the VIENNA Rectifier as it requires only three switches at the expense of additional diodes and higher conduction losses [38, 39]. **(f)** Current source rectifier using a current doubler circuit for improved efficiency at large voltage step down ratios [40].

CSC), shown in **Fig. 1.6(b)**, which is composed of two conventional CSRs connected in parallel at the mains input [33]. Their dc-link currents are combined/split using four inductors or two ICTs and two inductors. Together with an appropriate control scheme, an equal sharing of the dc output current between the two conventional CSRs can be ensured [34, 35]. The resulting additional two levels in the input currents $i_{\bar{a}}$, $i_{\bar{b}}$ and $i_{\bar{c}}$ reduce the switching frequency voltage ripple's amplitude at the input filter capacitors C_{ac}. This allows to reduce the volume and/or losses of an input filter required for compliance with Electromagnetic Compatibility (EMC) regulations. For a system with an additional boost converter stage, a full-load efficiency of 95.6 % at 2.2 kW is reported in [35].

The *Integrated Active Filter* (IAF) rectifier shown in **Fig. 1.6(c)** was originally proposed for three-phase solar inverters without electrolytic capacitors by Jantsch and Verhoeve in 1997 and for drive applications by Yoo in 2009 [36, 41]. It consists of a six-pulse diode rectifier bridge supplying a conventional buck converter that provides the dc output current i_{dc}. To achieve sinusoidal mains input currents a half-bridge of switches and an inductor L_{inj} are used to create a third harmonic current i_{inj}, which is fed into the mains line where both rectifier diodes are currently off, using three bidirectionally conducting and -blocking switches. This so called *third harmonic injection circuit* can be seen as a built-in active harmonic filter, which eliminates low-frequency harmonics in the input current generated by the six-pulse diode rectifier due to $\pi/6$-wide intervals with zero current.

A related circuit is the *SWISS Rectifier* proposed by Kolar et al. in 2012 [37, 42]. Like the IAF rectifier it uses a six-pulse diode bridge combined with three bidirectional switches as input stage. The injection current i_{inj}, however, is created by two switches and two diodes acting as dc-dc buck converter stage as shown in **Fig. 1.6(d)**. Therefore no dedicated inductor is required for the injection circuit, potentially allowing reduced losses and/or lower volume than the IAF rectifier. Note that the six-pulse diode bridge and the bidirectional switches are commutated at mains frequency only, which allows to use devices optimized for low conduction losses (and higher switching loss energies) than in the conventional CSR. Furthermore the utilization of the output buck converter stages is better than in the CSR as always one out of two semiconductors conducts current.

The *Three-Switch Rectifier* introduced by Tooth in 1999 and shown in **Fig. 1.6(e)** is the three-phase buck-type PFC rectifier with the lowest number of switches that does not require a mains-frequency transformer or inductor [38]. However, this low number of switches increases the number of

semiconductors in the conduction path; in non-free-wheeling states there are six elements in the path, which leads to high conduction losses. The three-switch rectifier can be seen as the buck-type version of the original VIENNA Rectifier shown in **Fig. 1.4(d)**.

Finally **Fig. 1.6(f)** shows a current source rectifier for large voltage step-down ratios proposed by Singh et al. in 2017 [40]. It consists of six bidirectional switches feeding a current doubler rectifier stage which allows a higher efficiency if the dc output voltage is considerably lower than the ac mains line-to-line voltage.

1.1.3 Buck-Boost Three-Phase PFC Rectifiers

As certain applications require a dc output voltage which has to be higher or lower than the mains voltage depending on operating conditions, three-phase PFC rectifiers with buck-boost-characteristic have been invented. A few selected circuit topologies are briefly discussed in the following for the sake completeness. One of the first non-isolated three-phase buck-boost PFC rectifiers was proposed by Ngo in 1984 [43] and by Mechi and Funabiki in 1992 [44] and is shown in **Fig. 1.7(a)**. This circuit can be derived from a conventional buck-type CSR by changing the inductor's connection and adding a diode and output capacitor. Modulation and control of this rectifier are similar to the conventional CSR [45].

In **Fig. 1.7(b)** a SEPIC-type three-phase PFC rectifier, proposed by Kolar et al. in 1997, is shown [46]. This circuit can be derived from the three-switch VIENNA Rectifier [cf. **Fig. 1.4(d)**] and requires only three switches, but 18 diodes, six inductors and eight capacitors. Compared to other PFC rectifiers relatively high conduction losses are expected as three or four semiconductor devices exist in each conduction path.

The topology shown in **Fig. 1.7(c)** was proposed by Baumann et al. in 2000 [47] and consists of a front-end three-switch buck-type three-phase PFC rectifier followed by a dc-dc boost converter output stage. Only four switches are required, but like in the three-switch buck-type PFC rectifier [cf. **Fig. 1.6(e)**] relatively large conduction losses result as the conduction path consists of a series connection of up to seven semiconductors.

A buck-boost PFC rectifier, based on a so-called Z-source network, was introduced by Ding et al. in 2005 and is shown in **Fig. 1.7(d)**. A conventional two-level boost-type PFC rectifier is used as input stage, however, the dc-link capacitor is replaced by a Z-source network followed by an additional switch to achieve buck-boost operation. As in other Z-source circuits, all six

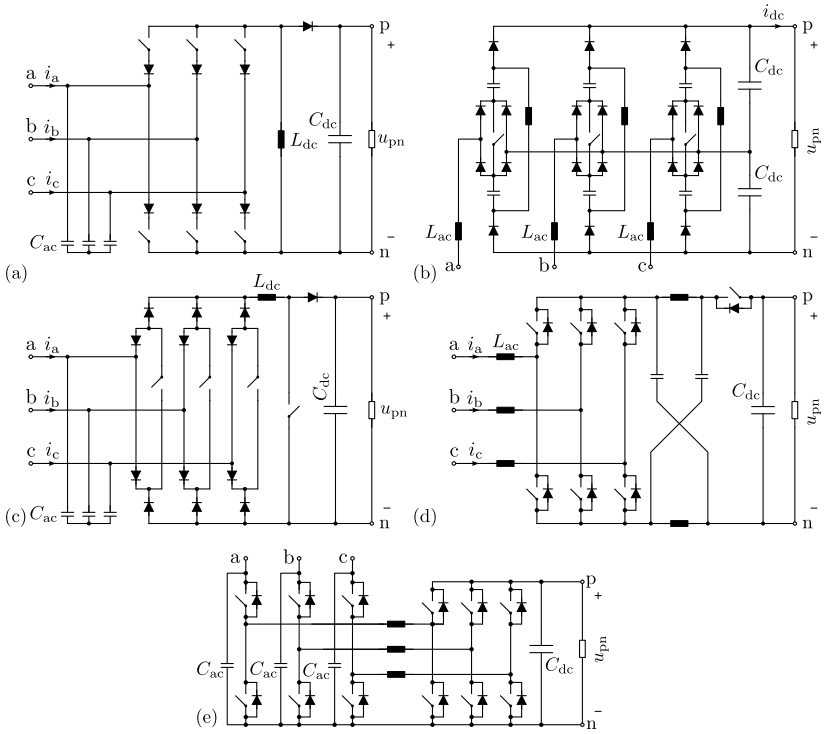

Fig. 1.7: Non-isolated buck-boost three-phase PFC rectifiers: **(a)** shows a six-switch CSR configured for buck-boost operation as introduced Ngo in 1984 [43]. In **(b)** a SEPIC-type rectifier is shown, which was derived from the VIENNA Rectifier by Kolar et al. in 1997 [46]. **(c)** In 2000 Baumann et al. proposed the combination of a three-switch buck-type PFC rectifier and dc-dc boost converter output stage [47]. **(d)** The *Z-source* rectifier uses a conventional two-level boost-type input stage connected to a so-called Z-source network of two inductors and capacitors and was introduced in 2005 by Ding et al. [48]. **(e)** Three-phase Y-Rectifier proposed as buck-boost inverter by Antivachis et al. in 2018 [49].

switches of the input stage can be turned on simultaneously (called *shoot-through* state) without short circuiting any capacitors. This gives an inherent robustness to switching errors, however, for given ac and dc voltages the blocking voltage stress of the semiconductors is typically higher compared to other PFC rectifiers.

Finally, **Fig. 1.7(e)** shows the three-phase buck-boost Y-Rectifier published by Antivachis et al. in 2018 [49]. It consists of three dc-dc buck-boost converters, each built from two half-bridges connected by an inductor. The three input-side half-bridges of these converters are connected in a star-configuration (Y-configuration) and the star-point is connected to the negative dc output terminal n, while the three output-side half-bridges are connected in parallel to the dc capacitor C_{dc} and the load. Each dc-dc converter operates independent from the others, which allows a simple control, however, compared to other circuits higher semiconductors current stresses result.

This concludes the introduction of non-isolated three-phase PFC rectifiers, isolated variants are discussed in the next section.

1.2 Three-Phase Isolated Matrix-Type PFC Rectifiers

In a number of applications galvanic isolation is required between the three-phase ac mains and the load, for example, due to safety regulations, because of different grounding schemes on ac and dc-side or because the dc load voltage is significantly higher or lower than the ac voltage. Non-isolated systems would create too high current and voltage stresses on the components in this case, rendering them impractical. Typically two-stage solutions are used in this case which consist of either a boost- or a buck-type PFC front end to ensure sinusoidal mains currents and provide a regulated dc voltage that feeds an isolated dc-dc converter. Three-phase isolated matrix-type PFC rectifiers, which allow a single-stage power transfer between the ac mains and a dc bus, have been proposed as an alternative in order to reduce the number of conversion stages and therefore the complexity, losses and/or cost. In this case the term *matrix-type* refers to the fact that the main energy storage element is an inductor or capacitor placed at the dc output of the rectifier and no intermediate storage element, which is typically found between the two subconverters of a two-stage solution, exists.

Again, a brief overview of the proposed circuits is given in the following. For the sake of clarity, the circuits are divided into buck-, boost- and buck-

boost-characteristic. Furthermore, phase-integrated systems, which use a network of switches to apply voltage to one or two transformers, can be distinguished from phase-modular systems which use three identical phase-modules derived from single-phase PFC rectifiers.

1.2.1 Phase-Integrated Matrix-Type PFC Rectifiers with Buck-Characteristic

The first phase-integrated isolated buck-type PFC rectifier was proposed by Manias et al. in 1985 and is shown in **Fig. 1.8(a)** [50]. It uses a Direct Matrix Converter (DMC) to select one line-to-line mains voltage and apply it to the primary-side of the transformer. In each switching frequency cycle two line-to-line voltages are applied with alternating polarity, creating a high-frequency ac voltage at the transformer's primary winding. Like in a dc-dc forward converter a full-bridge diode rectifier is connected to the secondary-side and an inductor L_{dc} is connected in series to the rectified voltage to ensure a constant dc output current. By replacing the direct matrix converter with an indirect matrix converter built from a six-switch buck-type circuit connected to a full-bridge inverter, as shown in **Fig. 1.8(b)**, a similar circuit results. Also this version was proposed by Manias et al. in 1985 and achieves purely sinusoidal mains input currents [50]; the same is true for the circuit depicted in **(a)**. In 1992 Vlatković et al. published the circuit shown in **Fig. 1.8(c)** which is also based on a DMC, but implements the bidirectional switches with two MOSFETs connected back-to-back in order to reduce the number elements in the conduction path [51]. Additionally the authors of [51] proposed a modulation scheme which achieves zero voltage switching (ZVS) of the matrix converter switches.

By combining a six-switch rectifier and the full-bridge inverter of the circuit in **Fig. 1.8(b)** the *VIENNA Rectifier III*, shown in **Fig. 1.8(d)** and published by Kolar et al. in 1998, can be derived [52]. The VIENNA Rectifier III requires only five active switches but has a higher number of semiconductors in the conduction paths compared to the circuits in **Fig. 1.8(b)** and **(c)**. Another concept, employing an input-side *Integrated Active Filter* stage, originally proposed by Jantsch and Verhoeve for three-phase PV inverters without electrolytic capacitors in 1997, is shown in **Fig. 1.8(e)** [36]. This rectifier circuit can be derived from the non-isolated Integrated Active Filter rectifier in **Fig. 1.6(c)** by replacing the output buck stage with a dc-dc forward converter to include galvanic isolation. In the same way, the *Swiss-Forward* rectifier shown in **Fig. 1.8(f)** is derived from the SWISS Rectifier [cf. **Fig. 1.6(d)**] by

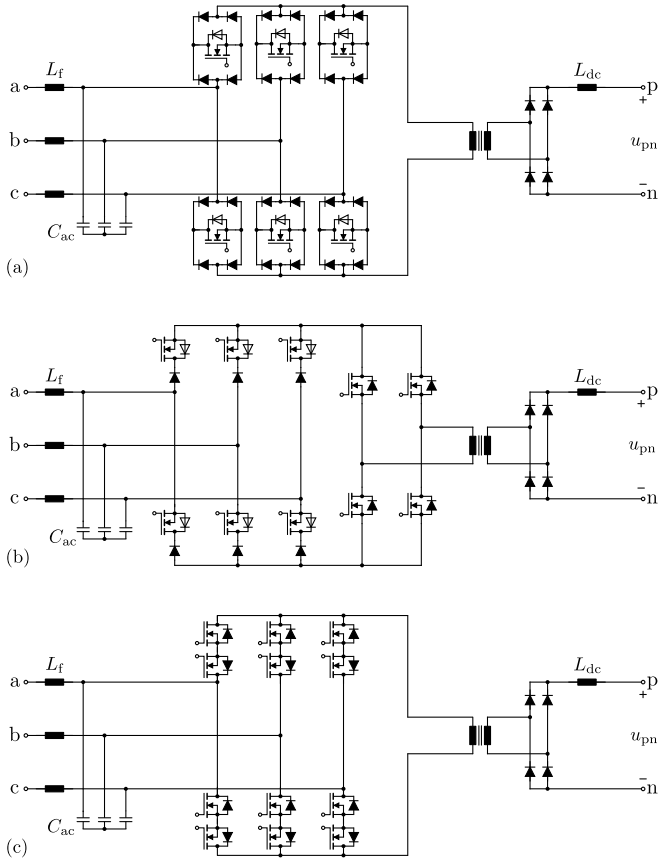

Fig. 1.8: Isolated Matrix-Type Buck PFC Rectifiers: **(a)** Direct Matrix Converter (DMC) based buck-type PFC rectifier first reported by Manias et al. in 1985 [50]. **(b)** Indirect Matrix Converter based version of the circuit in **(a)**, also published by Manias et al. [50]. **(c)** Modified version of **(a)** implementing the bidirectional switches with two MOSFETs connected back-to-back as introduced by Vlatković et al. in 1992 [51]. Figure continued on next page.

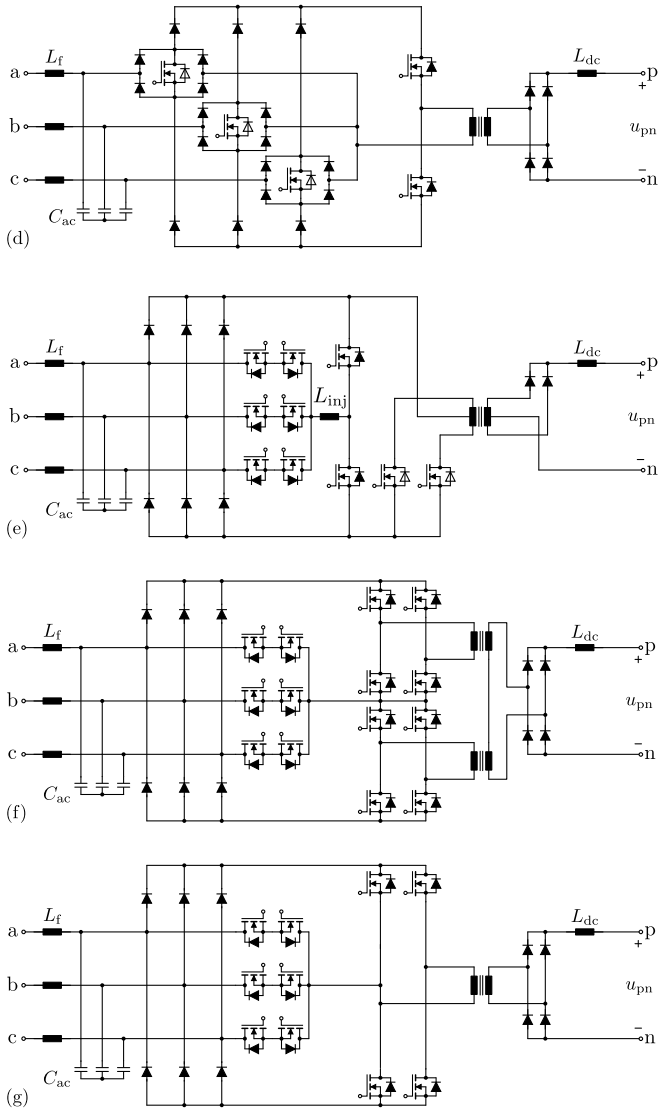

Fig. 1.8 (Cont.): (d) *VIENNA Rectifier III* introduced by Kolar et al. in 1998 [52]. **(e)** *Isolated Integrated Active Filter* rectifier conceptually introduced by Jantsch et al. in 1997 [36] with isolated push-pull dc-dc output stage. **(f)** *Swiss-Forward* rectifier published by Silva et al. in 2016 [53]. **(g)** *Isolated Single-Stage Three-Phase Full-Bridge with Current Injection Path PFC* rectifier (IS^{2}FBCIP) proposed by Zhao et al. in 2015 [54].

replacing the buck converter stages with two isolated full-bridge forward converters as described by Silva et al. in [53]. A similar rectifier called *Isolated Single-Stage Three-Phase Full-Bridge with Current Injection Path PFC* rectifier (IS²FBCIP) and shown in **Fig. 1.8(g)** was derived by Zhao et al. in 2015 as a combination of the isolated IAF (cf. **Fig. 1.8(e)**) and the Swiss-Forward rectifier [54]. However, it can also be seen as a VIENNA Rectifier III with a different implement of the phase selector switches.

1.2.2 Phase-Integrated Matrix-Type PFC Rectifiers with Boost-Characteristic

Apparently, a significantly lower number of three-phase isolated matrix-type PFC rectifiers with boost-characteristic has been described in the literature compared to systems with buck-characteristic. The reason for this is not evident but it is probably due to the typically wide output voltage range and inherent dc current limiting feature offered by buck-type rectifiers. However, systems with boost-characteristic have the advantage of continuous input currents, directly impressed by inductors, which typically allows high quality mains input currents with a low THD and high power factor.

Two isolated matrix-type PFC rectifier are shown in **Fig. 1.9**. In **(a)** the *VIENNA Rectifier II* is shown, which was introduced by Kolar et al. in 1998 [55,56]. Similar to the conventional non-isolated VIENNA Rectifier it requires only a low number of switches (five in total) at the expense of a high number of diodes and a high number of semiconductors in the conduction path. Alternatively the matrix-type rectifiers proposed by Manias [cf. **Fig. 1.8(a)** and **(b)**] can be implemented with boost-characteristic by placing boost inductors L_{ac} at the mains input and a dc capacitor C_{dc} at the output. The resulting circuit is shown in **Fig. 1.9(b)** and was published by Kawabata et al. in 1990 as isolated three-phase inverter for uninterruptible power supplies (UPS) [57].

Another solution, shown in **Fig. 1.10**, was proposed by Almeida et al. in 2017 and is based on a conventional three-level boost-type input stage using ICTs [58]. In order to achieve galvanic isolation a third winding is installed on each of the three ICTs and those are connected to three full-bridges of switches on the secondary-side. Note that no load is connected to the primary-side dc-link capacitor, instead the power drawn from the ac mains by the boost rectifier flows to the secondary-side via the ICTs. Ideally the secondary-side full-bridges generate the same voltage waveforms as the primary-side ones, however, by introducing a phase shift between primary and secondary-side the transferred power can be controlled, similar to a DAB.

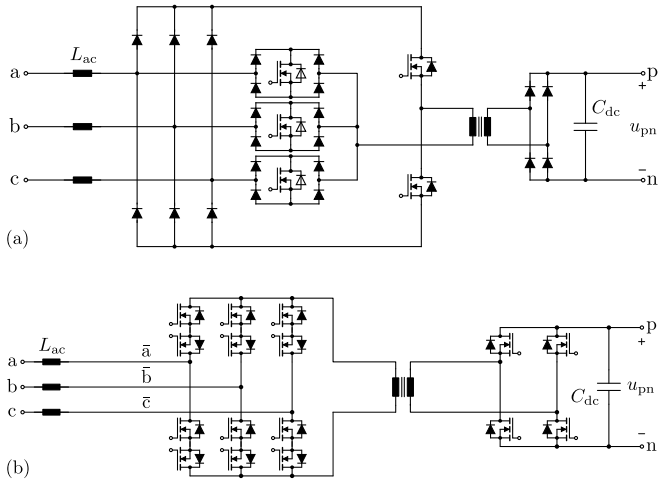

Fig. 1.9: Isolated matrix-type phase-integrated boost PFC rectifiers: **(a)** *VIENNA Rectifier II* proposed by Kolar et al. in 1998 [55, 56] and **(b)** modified version of the matrix-type PFC rectifier proposed by Manias et al. [cf. **Fig. 1.8(a)**] with boost-characteristic proposed by Kawabata et al. in 1990 [57].

In this circuit the primary-side switches simultaneously perform the PFC rectification and the generation of a switching frequency ac voltage required for the isolation transformers. As the resulting two current components are orthogonal due to the different frequencies, this allows a higher utilization of the switches and therefore potentially lower conduction losses. However, three individual isolation transformers are required and the applied voltage and resulting flux vary with twice the mains frequency, leading to higher stresses on the transformer compared to the circuits in **Fig. 1.9**.

1.2.3 Buck-Boost-Characteristic Matrix-Type PFC Rectifiers

A phase-integrated isolated matrix-type three-phase PFC rectifier with buck-boost-characteristic has been proposed by Weise et al. in 2010 as vehicle-to-grid interface for plug-in hybrid electric vehicles [59] and as grid connected inverter by Sayed et al. in 2016 [60]. The basic schematic is shown in **Fig. 1.11**. Note that filter capacitors C_{ac} are connected at the input nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ of the matrix converter and an output capacitor C_{dc} is connected to the secondary-

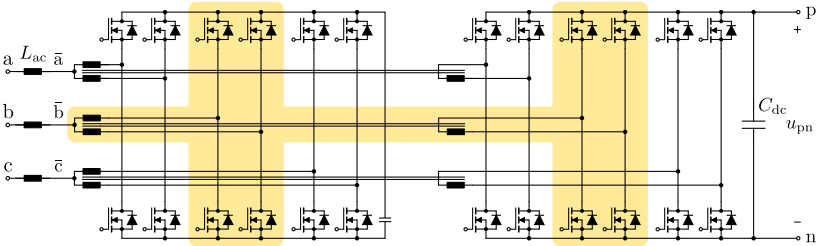

Fig. 1.10: Isolated phase-integrated matrix-type boost PFC rectifier proposed by Almeida et al. in 2017 [58]: A three-level boost-type PFC rectifier, implemented with ICTs, is used as input stage and a third winding is installed on each ICT. On the secondary-side three full-bridges apply voltages to these windings, which have ideally the same waveforms as the primary-side ICT voltages, but are phase shifted. Therefore the ICTs operate essentially like three DAB transformers and the transferred power can be controlled using the phase shift angle.

side full-bridge. This implies that the voltages across the semiconductors on both sides, i.e. the ac- and dc-side, are impressed by capacitors. Snubber circuits, which are typically required for the dc-side rectifier of isolated buck-type circuits due to the transformer's leakage inductance, are not required. In order to control the transformer current an inductor L_{ac} is placed in series with the transformer, which implies that it can potentially be implemented by the transformer's leakage inductance. This circuit can also be seen as a dual active bridge (DAB) converter, where the primary-side switches are replaced by a three-to-two direct matrix converter. The equations describing the rectifier's mains current as function of the DAB's switching times are, however, a system of coupled nonlinear equations and it is hence not trivial to deduce a modulation scheme which achieves purely sinusoidal input currents in phase with the mains voltages. While some analysis is provided by Sayed et al., only a THD of 14 % is achieved, which is typically not acceptable for a PFC rectifier.

1.2.4 Phase-Modular Matrix-Type PFC Rectifiers

All isolated rectifier circuits shown above are phase-integrated topologies that use a network of switches and diodes to select a mains voltage or current and apply it to the primary-side of the transformer. Phase-modular rectifiers, which use three separate phase-modules and potentially also three individual transformers and output rectifiers, are an alternative. In the following, several

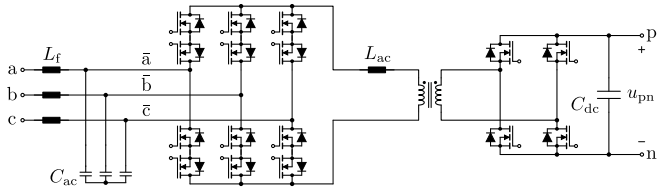

Fig. 1.11: Basic schematic of the isolated matrix-type DAB three-phase buck-boost PFC rectifier proposed by Weise et al. in 2010 as vehicle-to-grid interface [59] and as inverter by Sayed et al. in 2016 [60].

matrix-type phase-modular PFC rectifier circuits are briefly introduced in chronological order of first publication. Note that in this context *matrix-type* refers to the fact that only energy storage elements (i.e. capacitors and/or inductors) with time constants in the same order of magnitude as the switching frequency, i.e. much shorter than the mains frequency, are present in the phase-modules.

One of the earliest phase-modular three-phase rectifiers, which allows almost sinusoidal mains input currents, is shown in **Fig. 1.12** and was patented by Brewster and Barret in 1979 [61]. It uses three phase-modules connected to the ac mains in delta-configuration and in parallel at the dc output. A full-wave diode rectifier is used in each phase-module to feed an isolated, series resonant dc-dc converter which ideally presents an ohmic load to the input diode rectifier. However, purely sinusoidal input currents cannot be achieved by this circuit as the series resonant converter shows buck-type behavior and cannot create an input current if the rectified mains voltage is below the dc output voltage divided by the turns ratio. Hence distortions of the mains current around the zero crossings of each line-to-line voltage result.

Probably the first three-phase phase-modular matrix-type PFC rectifier concept reported in scientific literature was published by Kocher and Steigerwald in 1982 [62]. The circuit is shown in **Fig. 1.13(a)**: It uses three single-phase phase-modules each using a flyback converter for isolation and control of the input current. Line-to-line mains voltages are used to supply the modules which results in a delta-configuration of the modules. In their paper Kocher and Steigerwald already show that a third harmonic current can circulate between the phase-modules without disturbing the mains input currents, allowing to reduce the phase-modules modules' input current peak value. This feature is also mentioned in the preceding patent of Brewster and

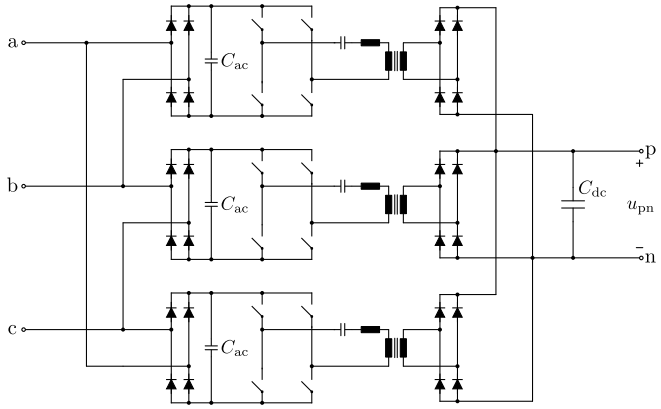

Fig. 1.12: Phase-modular three-phase rectifier concept with near sinusoidal mains currents patented by Brewster and Barret in 1979, using three single-phase ac-to-dc phase-modules, connected in delta at the mains input and in parallel at the dc output [61]. In each phase-module a full-wave diode rectifier supplies an isolated, series resonant dc-dc converter which ideally shows ohmic input behavior. Note that this circuit cannot achieve purely sinusoidal input currents as the dc-dc converter has a buck-characteristic and cannot create an input current when the rectified mains voltage is below a certain threshold.

Barret [61].

A solution based on three individual phase-modules which apply one ac line-to-line voltage to a common isolation transformer was proposed by Okuma et al. in 1994 [63]. The circuit is shown in **Fig. 1.13(b)**. Compared to a direct matrix converter type switching network as used in **Fig. 1.8(c)**, this circuit is easier to commutate, as bidirectional switches, which typically require special commutation sequences to ensure a valid current path at any time, are avoided.

The circuit shown in **Fig. 1.13(c)** was patented by Small in 1998 and consists of three phase-modules, where each one is essentially a forward converter [64]. Unlike conventional dc-dc forward converters, the phase-modules use a full-wave rectified mains voltages (either in star- or delta-connection) as input voltage and do not contain an energy storage element large enough to buffer the power pulsation at twice the mains frequency. Hence the output voltage produced by each phase-module varies with twice the mains frequency. By connecting the secondary-side windings of the three transformers

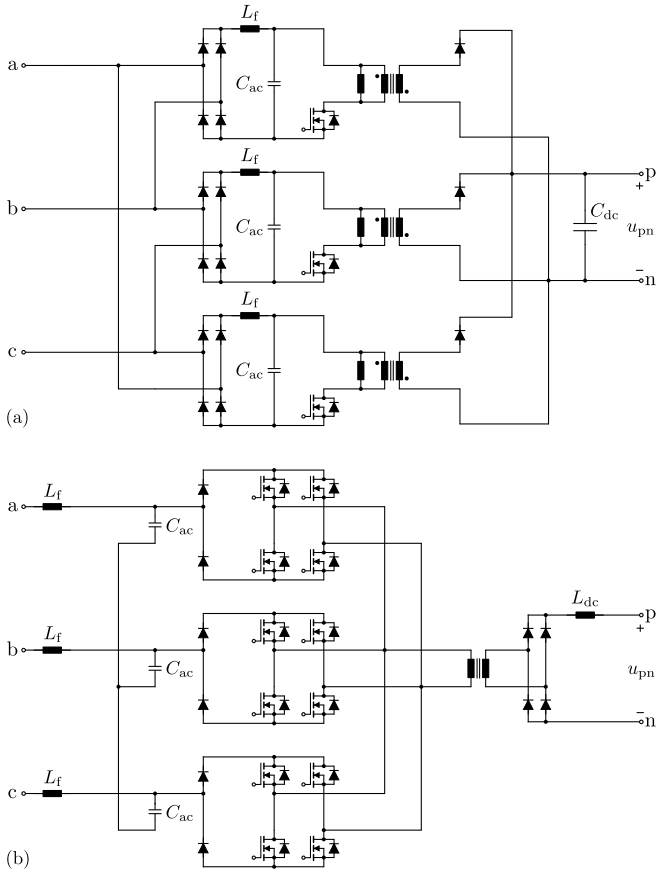

Fig. 1.13: Phase-modular isolated three-phase PFC rectifier circuits: **(a)** Three-phase PFC converter built from three identical flyback converter based phase-modules, as proposed by Kocher and Steigerwald in 1982 [62]. **(b)** PFC rectifier introduced by Okuma et al. in 1994, using three phase-modules to select one line-to-line voltage which is applied to the isolation transformer [63]. Figure continued on next page.

in series and using a common rectifier and dc output inductor L_dc a constant output current and voltage, as well as sinusoidal input currents are achieved. Note that for a star-connection of the phase-modules the star-point N of the three phase mains needs to be available which is not always the case.

Rooij et al. published a paper introducing a similar circuit, shown in

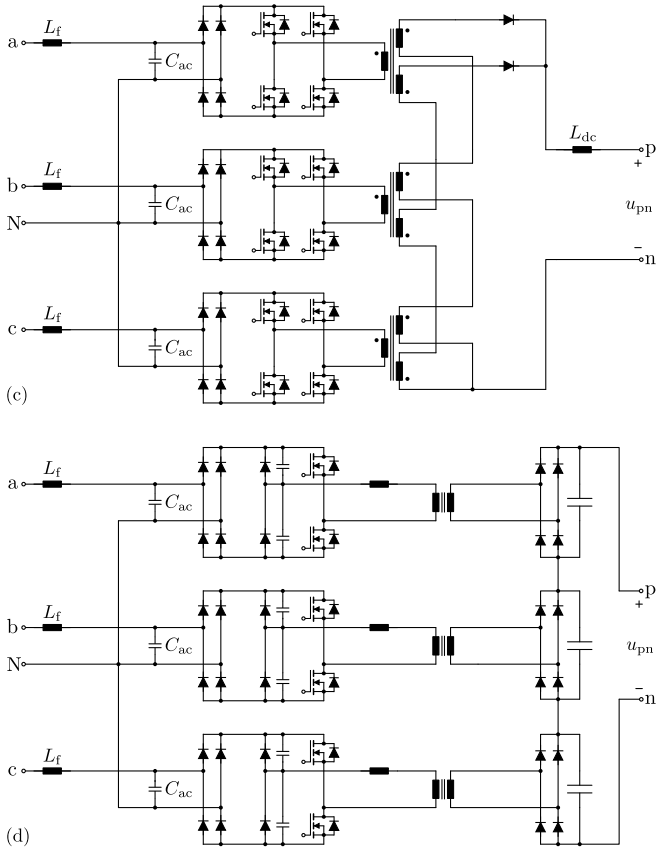

Fig. 1.13 (Cont.): (c) Rectifier patented by Small in 1998 based on forward converter like phase-modules with secondary-side windings connected in series and a common rectifier and output filter [64]. **(d)** Circuit proposed by Rooij et al. in 1998 based on partial series resonant converter modules connected in series at the output [65]. The output voltage of each module varies with twice the mains frequency, however, the three voltages sum up to a constant dc output voltage. Figure continued on next page.

Fig. 1.13(d) in 1998 [65]. Unlike the circuit of Small the individual phase-modules are partial series resonant converters and each phase-module contains a dedicated full-bridge diode rectifier and output capacitor. Again each phase-module transfers a power varying with twice the mains frequency

and therefore produces an output voltage that varies with twice the mains frequency. This poses a limitation on the capacitance of the phase-modules' output capacitors, but has the advantage of directly impressing the voltage across the output rectifier and hence no snubbers are required, unlike in circuits derived from the forward converter.

York at el. published the circuit shown in **Fig. 1.13(e)** in 1994 which uses three pulse width modulated phase-modules to create three high-frequency ac voltages which are amplitude modulated by the respective mains input phase voltages [66]. The secondary-side windings of the phase-module transformers are connected in star-configuration and the resulting symmetric three-phase high-frequency voltage system is rectified using a six-pulse diode rectifier. Low-pass filters are inserted between the phase-module switches and the primary windings of the transformers as the switching frequency is higher than the frequency at which the transformers are operated.

In 2000 Ho et al. proposed the rectifier shown in **Fig. 1.13(f)** which too consists of three forward-converter-like phase-modules, each using a full-bridge rectifier and dc output inductor on the secondary-side [67]. The phase-modules' dc outputs are connected in parallel to the dc output. As with the concept by Brewster and Barret (cf. **Fig. 1.12**) purely sinusoidal input currents are not possible with this circuit as the phase-modules have buck-characteristic and feed a dedicated output inductor. This implies that no power transfer, and hence no mains current, can be created by a phase-module if its corresponding ac input voltage is below the dc output voltage times the transformer turns ratio. Input current THD values between 10 % and 20 % were reported by Ho et al.

The circuit shown in **Fig. 1.13(g)** is based on a *Quad Active Bridge* (QAB), which can be seen as an extended version of a DAB, and was proposed by Vermulst et al. in 2014 [68, 71]. To avoid using full-bridge diode rectifiers at the input of the phase-modules (in a star-configuration) a capacitor is connected between the mains neutral N and the star-point of the phase-modules. By charging it to a value higher than the mains line-to-neutral voltage amplitude, the phase-modules' MOSFET full-bridges exhibit only positive blocking voltages. However the maximum voltage applied to the switches is more than double the value if a diode rectifier is used such as in **Fig. 1.8(e)**. Like in a conventional DAB, a full-bridge of switches is used on all four ports of the transformer system. The voltages created by the input-side full-bridges are added by connecting the secondary-side windings of the phase-module transformers in series. An inductor is connected in series with the secondary-side windings in order to control the current flow. Note that

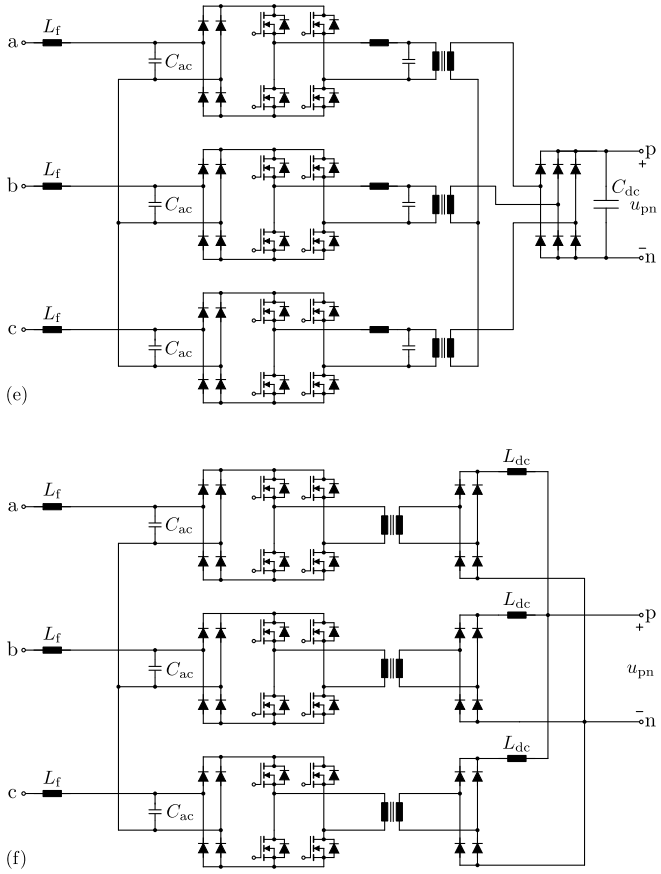

Fig. 1.13 (Cont.): (e) In 1994 York et al. proposed a circuit which uses a PWM controlled full-bridge in each phase-module to create three high-frequency voltages which are amplitude modulated by the ac mains phase voltages [66]. A six-pulse diode bridge is used to rectify the symmetric three-phase high-frequency voltages created by the star connected secondary-side transformer windings. **(f)** The three phase-modules of the rectifier proposed by Ho et al. in 2000 each employ a rectifier and an output inductor which are feeding the dc output in parallel [67]. As each phase-module is essentially a forward converter powered from a rectified mains voltage, this circuit cannot achieve purely sinusoidal mains currents. Figure continued on next page.

bidirectional power flow, i.e. operation either as rectifier or as inverter, is

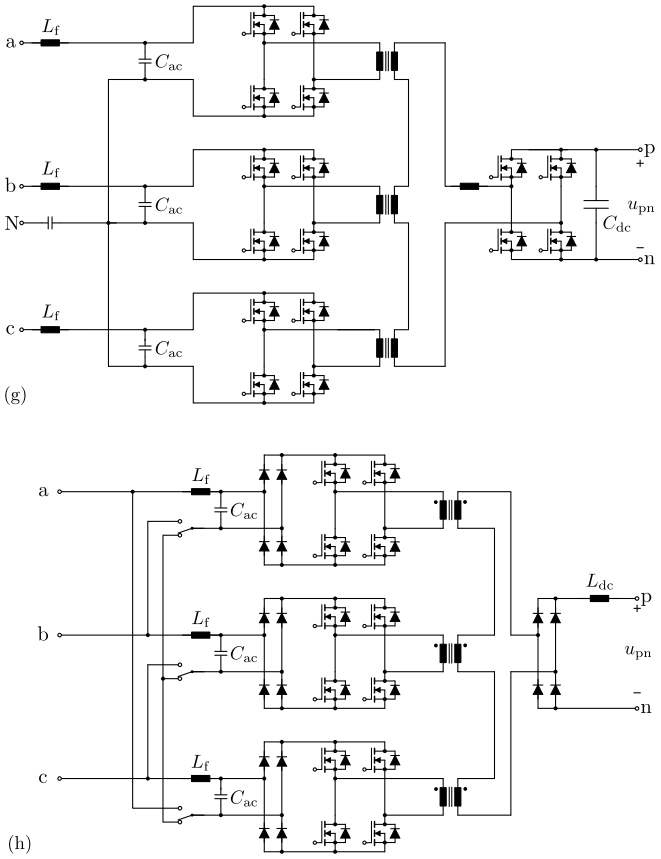

Fig. 1.13 (Cont.): (g) Quad Active Bridge (QAB) PFC rectifier proposed by Vermulst et al. in 2014 [68]. By connecting a capacitor between the mains star-point N and the star-point of the phase-modules, which are connected in star-configuration, the input rectifiers can be omitted at the expense of a higher blocking voltage rating of the switches [68]. (h) Isolated Matrix-Type Y-Δ-Rectifier (IMY/D) published by Kolar and Cortés in 2013 [69, 70], which includes three switches, e.g. mechanical contactors or relais, to connect the phase-modules' ac inputs either in star- or delta-configuration to enable a wide input voltage range.

possible with this circuit.

Finally, **Fig. 1.13(h)** shows the *Isolated Matrix-Type Y-Δ-Rectifier* (IMY/D)

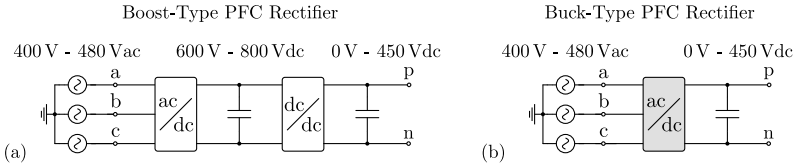

Fig. 1.14: Three-phase PFC rectifier concepts with a dc output voltage lower than the ac mains voltage. **(a)** Conventional two-stage approach were a boost-type PFC rectifier provides an intermediate dc-link with a voltage in the range of 600 V to 800 V. This voltage powers an isolated or non-isolated buck converter that provides the required output voltage in the range 0 V to 450 V. **(b)** Single-stage solution using a three-phase buck-type PFC rectifier which enables a direct power transfer from the three-phase mains to a lower dc output voltage.

published by Kolar and Cortés in 2013 [69, 70]. Similar to **Fig. 1.13(c)** three indirect matrix-type phase-modules with an isolation transformer are used and the secondary-side windings are connected in series to a common rectifier and dc output inductor. Additionally three mechanical switches at the ac input allow to connect the phase-modules either in star or delta which allows a wide ac mains voltage range. When the ac input voltage is low the phase-modules can be switched to delta-configuration which increases the input voltage of the phase-modules by a factor of $\sqrt{3}$ compared to star-configuration. Furthermore, a modulation scheme has been proposed which allows to achieve ZVS of the phase-module switches similar to a conventional phase shift full-bridge forward dc-dc converter [72].

1.3 Applications for Three-Phase Buck-Type PFC Rectifiers

Since the availability of power semiconductors capable of turning off a current, such as BJTs, GTOs, IGBTs, IGCTs and MOSFETs, boost-type PFC rectifiers have generally received more attention in research, industrial applications and scientific literature than buck-type circuits. This might be due to the fact that single-phase buck-type rectifiers cannot achieve sinusoidal input currents and are hence restricted to comparatively low power levels of typ. < 100 W. Therefore boost-type PFC rectifiers clearly dominate in single-phase applications, and it seems likely that three-phase boost-type circuits received more attention because they can be deduced from corresponding single-phase

versions. Furthermore, if a galvanic isolation is required between load and ac mains for safety reasons, or due to different grounding schemes on the ac and dc-side, a separate isolated dc-dc converter, containing a transformer, is typically inserted between rectifier and load. In this case the turns ratio and/or the isolated converter's modulation constitute degrees of freedom which allow to use a boost-type PFC rectifier regardless of the load's required dc voltage. For applications were a galvanically isolated rectifier is not required, for example because isolation is provided by an already existing mains frequency transformer, a non-isolated dc-dc buck converter is typically used, resulting in a two-stage system as shown in **Fig. 1.14(a)**.

However, there are a number of applications were non-isolated or isolated buck-type PFC rectifiers can be advantageous because they enable a single-stage power conversion, as shown in **Fig. 1.14(b)**, which can lead to a reduction of complexity (e.g. lower number of power devices, passive components and/or simpler modulation and control), higher efficiency, lower volume and/or increased reliability. As an example, three areas of applications which could benefit from using three-phase buck-type PFC rectifiers instead of two-stage solutions are described in the following.

1.3.1 Electric Vehicle Traction Battery Charging

Fast chargers for Electric Vehicles (EV) and potentially also for Pluggable Hybrid Electric Vehicles (PHEV) allow recharging the traction battery in ≈ 10 min and are seen as a key component to increase the customer acceptance of e-mobility. Such systems need to supply several tens of kW up to more than 100 kW of dc power to the vehicle [73]. Different battery voltage levels and semiconductor technologies have been analyzed in the literature, with nominal voltages of ≈ 350 V and ≈ 700 V being the most common ones [74]. As of today, commercially available passenger electric vehicles typically employ a battery with a voltage up to ≈ 450 V when fully charged and corresponding fast chargers have been developed [75, 76]. For the fast charging of these vehicles three-phase buck-type PFC rectifiers are a promising option as they provide a dc output (i.e. battery) voltage down to zero, dc output current control and achieve sinusoidal mains input currents in a single conversion stage [37, 77].

1.3.2 DC Microgrids

Concerns about the environmental side effects of electric power generation, especially the climate change induced by greenhouse gas emissions from

thermal power plants operated from fossil fuels such as coal and oil, have led to significant research and development efforts regarding *Renewable Energy Sources* (RES) and efficiency improvements over the last decades. Out of a number of proposed RES, photovoltaic (PV) cells are probably the most widespread technology today. PV cells inherently produce a dc voltage and therefore require an inverter to deliver power into the existing ac distribution grid. Note that other generators for RES, such as small wind turbines or gas fueled cogeneration systems, typically also produce a dc voltage, even when permanent magnet machines are employed. As the revolution speed of the turbine has to be adapted to operating conditions such as wind speed to achieve the best efficiency, the generator's ac voltage frequency varies and hence a conversion system allowing variable input frequency is required. These ac-ac converters usually contain an internal dc-link that could be connected to a dc microgrid, either directly or via a (isolated) dc-dc converter.

Several types of storage systems have been proposed to compensate for fluctuations in electricity production and demand. Many of those are also based on dc like batteries, supercapacitors and flywheels (with integrated ac-dc interface). Similarly a number of loads, such as efficient lighting using light emitting diodes (LEDs), televisions, computers, cell phones and similar communication devices are intrinsic dc consumers. Efforts to improve the efficiency of household appliances lead to a wider usage of variable speed drives, for example in ventilation and air conditioning systems, where reducing the speed of a fan or compressor instead of using a throttling valve typically leads to significant power savings. Today all these systems are supplied from the conventional ac mains, which implies that dozens of small ($\approx$ 10 W to 1 kW) rectifier stages, potentially with PFC functionality, are used in a typical home or office building and their number is expected to increase further. Considering this, low-voltage dc microgrids have been proposed as distribution systems in order to reduce the number of power conversion stages for improved efficiency and potentially also higher reliability [78]. These microgrids might span only a single building or a residential area with several buildings and can be combined with distributed generation from RES, such as PV cells or wind turbines and battery or flywheel storage.

Different dc voltage levels have been proposed for microgrids, for example the industry association *EMerge Alliance* has published a standard for 24 V dc microgrids in 'occupied space' such as homes or offices and a second standard for data centers which uses 380 V dc [79]. This difference is due to the general trade-off between safety and losses of the distribution system. The most common voltage levels reported in scientific literature are summarized in the

following:

- 24 V is the nominal voltage in the EMerge Alliance's standard for occupied space. This voltage is useful predominantly for low-power applications such as efficient lighting, and more than one power supply feeding several 24 V buses from a conventional ac mains might be required [80].
- 48 V is a widespread supply voltage for telecommunication equipment, especially in central offices of telephone networks. It is within the *IEC Safety Extra-Low Voltage* (SELV) range (< 60 Vdc) and typically has less legal restrictions regarding insulation and protection. Therefore, it has been proposed an alternative to 24 V systems for higher load power and/or longer wire lengths and could be beneficial for powering computers, telecommunication devices and entertainment systems [80, 81].
- 120 V is the highest voltage still within the IEC's *Extra-Low Voltage* (ELV) range and typically requires no protection against exposure of conductive parts under fault conditions [82]. It is considered by some authors as a good compromise between safety and efficiency [80].
- 230 V has been proposed as dc voltage in order to maintain the same rms value as in European ac distribution. This would potentially allow to use existing resistive heating systems without modification [82, 83].
- 325 V allows the operation of equipment designed for 230 V ac systems that contain a full-bridge diode rectifier as input stage and is considered an economically and technically attractive solution [82, 83].
- ±170 V is a system that uses a third *neutral* conductor connected to PE, in addition to the positive and negative conductors. An active balancing circuit is used to ensure that the positive and negative potential remain symmetric with respect to the neutral wire even if some loads are connected between either the positive and neutral or the negative and neutral wires. This systems allows to power loads either with 170 V or 340 V similar to 120 V/240 V rms ac split-phase systems commonly used in most of America [84].
- 380 V, sometimes also termed 400 V dc, is the nominal voltage in both the *European Telecommunications Standards Institute* (ETSI) and the EMerge Alliance standard for dc distribution in data centers [85, 86].

Lower conduction losses than in single-phase ac systems and the highest efficiency of all dc microgrid solutions are expected due to the higher voltage [83]. To address safety concerns a grounding scheme has been proposed were both rails are connected to ground via a resistor of 20 kΩ to 40 kΩ and have a nominal potential of ±190 V with respect to protective earth (PE) [78]. A number of demonstrator systems and test sites using this voltage range have been reported in literature [81, 87–90].

Almost all proposed dc microgrids require an interface converter to exchange power between the microgrid and the conventional ac mains. As distributed generation is often connected to the microgrid, a bidirectional power conversion is typically required, which allows supplying dc loads from the ac mains if local generation is not sufficient, as well as feeding excess dc power back to the ac mains. For larger office buildings and microgrids spanning several residential homes, usual power levels will be tens of kW or higher and therefore bidirectional three-phase PFC rectifiers are required. For this application, three-phase buck-type PFC rectifiers are a promising option as all proposed dc voltages are below the output voltage of six-pulse diode rectifiers and a large dc bus voltage range is expected, especially if backup batteries are connected directly to the distribution bus without an additional dc-dc converter. Supplies for 380 V systems, for example, have to operate from voltages as low as 260 V up to 410 V, which can directly be achieved by buck-type three-phase PFC rectifiers while an additional dc-dc converter would usually be required if a boost-type PFC circuit is used.

1.3.3 Data Center Power Supplies

Data centers are usually considered to be a critical infrastructure by their operators and high availability of the services provided by the servers inside the center is a necessity. Therefore an Uninterruptible Power Supply (UPS) is usually installed in the data center's power distribution system to ensure continuous operation of the servers even during outages of the public ac mains. Historically the distribution system inside the data center was based on conventional 400 V or 480 V (rms line-to-line) ac. The UPS is typically implemented as so called online or double conversion system which means that power is drawn from the feeding ac mains by a boost-type PFC rectifier to supply an intermediate dc-link which is connected to backup batteries and feeds an inverter that provides the required three-phase ac voltages for the load [91]. This configuration is shown in **Fig. 1.15(a)**, where it can be seen

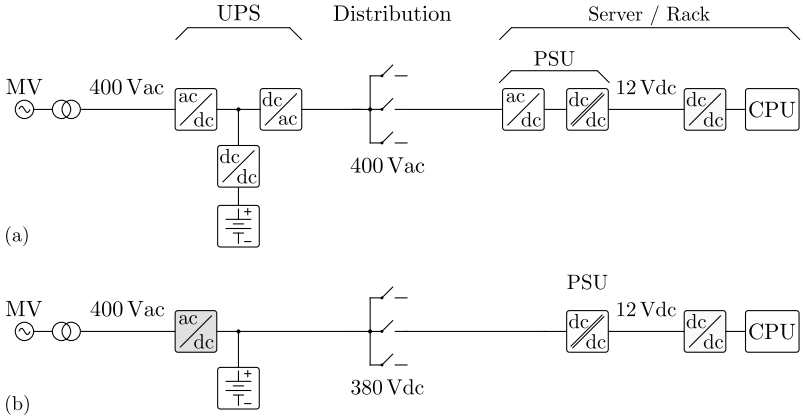

Fig. 1.15: Data center power distribution systems. **(a)** An online (also called double conversion) Uninterruptible Power Supply (UPS) supplies a 400 V three-phase ac distribution bus. Inside the rack or server a Power Supply Unit (PSU), which consists of a single-phase PFC rectifiers (distributed to the three supplying phases) and an insulated dc-dc converter, produce a dc voltage in the range of 12 V to 48 V. Finally non-isolated dc-dc converters provide the loads (e.g. a CPUs) with the required voltage of ≈ 1 V. **(b)** 380 V dc distribution system as standardized by ETSI and EMerge Alliance: By using a dc voltage for the power distribution system the UPS inverter and the PFC rectifier at the load side can be omitted [85, 86]. Compared to ac distribution efficiency improvements of ≈ 7 % have been reported [92, 93].

that together with the isolated single-phase PFC rectifiers and the point of load converters inside the server or rack, a total of 5 power conversion stages exists between the feeding ac mains and the loads, e.g. processors or hard disk drives.

In an effort to reduce the number of conversion stages to increase efficiency, reduce cost and improve reliability, dc distribution systems have been proposed and according standards have been created by the ETSI and the EMerge Alliance [85, 86]. As shown in **Fig. 1.15(b)** a distribution bus with a nominal voltage of 380 V dc connects the UPS and the load. This allows to omit the UPS inverter and the PFC input rectifiers in the servers, thereby removing two conversion stages. Note that 380 V is a nominal value and that *EN 300 132-3-1*, the ETSI standard for dc distribution in data centers, specifies a considerably larger voltage range of 260 V to 410 V for which rectifiers and power supplies have to provide nominal performance. This allows to directly connect backup batteries, for example strings of 168 lead acid cells connect

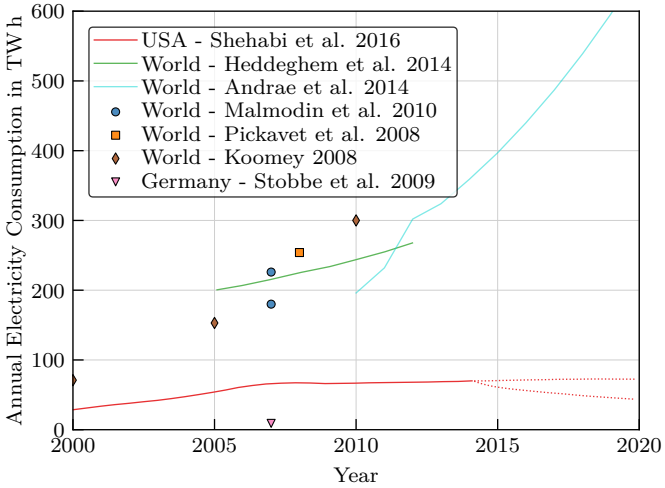

Fig. 1.16: Published estimates of data center's annual electricity consumption for the USA, Germany and world-wide. Note that most studies are based on data originally published by Koomey [94, 95]. While the trends predicted by different publications diverge, it can be assumed that today data centers consume approximately 300 TW h each year, which equals a continuous power dissipation of 34 GW.

in series, to the distribution bus without any dc-dc converters to reduce the system's complexity even further. Input power savings of ≈ 7 % have been reported for test sites using 380 V dc distribution [92, 93].

Due to the high power rating of data centers, from several hundreds of kW up to MW, three-phase PFC rectifiers are required to supply the dc distribution bus from the ac mains. Note that a boost-type PFC rectifier alone is not sufficient as input stage for a 380 V dc distribution system (highlighted in gray in **Fig. 1.15(b)**) as the dc voltage range of 260 V to 410 V is lower than the output voltage of a six-pulse diode rectifier which is ≈ 540 V. Therefore an additional dc-dc buck converter is required between the PFC's output and the dc distribution bus. Alternatively a buck-type three-phase PFC rectifier can used, potentially reducing the system's complexity, losses and cost.

In order to highlight the importance of data center power distribution systems, a brief overview of studies published on the world-wide power consumption of data centers and information and communication technology equipment is given in the following.

Data Center Electricity Consumption as Driver for Ultra-High Efficiency

Information and Communications Technology Equipment, which includes data centers, mobile and landline telephone and Internet networks, as well as end user devices like computers, cell phones and TVs, accounts for a significant share of the global electricity consumption. Especially the demand of data centers and its predicted development have received significant scientific attention after the publication of, now rebutted, claims and predictions of large demands starting in 1999 [95]. An exact measurement of the existing data centers' and telecommunication networks' demand is challenging due to many uncertainties, such as the number of installed servers, their load factors (i.e. what proportion of time servers are idle) and the efficiency of cooling and power distribution. A number of studies have been published, especially since 2008, and the estimated data center consumption of several publications, either for the world, the USA or Germany, is plotted in **Fig. 1.16**.

For the years 2005 to 2010 a world-wide annual consumption of data centers between 150 TW h and 300 TW h is estimated by most studies. Note that this is the equivalent of 17 GW to 34 GW dissipated continuously.

Malmodin et al. estimate that information and communication technology accounted for 3.2 % to 3.9 % of global electricity demand in 2007, out of which data centers used 180 TW h or 226 TW h (excluding or including networks inside the data center) [96]. For 2008 Pickavet et al. estimate an average power of 29 GW, i.e. 254 TW h for data centers and 25 GW, i.e. 219 TW h consumed by Internet and Telephone Networks [97]. Van Heddeghem et al. report similar numbers for 2005 to 2012 with an annual growth rate of 4.4 % [98]. Furthermore, the authors state that most studies are based on data originally published by Koomey in 2008 and 2011 [94, 95], but differ in the numerical results due to different classifications of what is included or excluded in the analysis and due to update estimations of the Power Usage Efficiency (PUE). PUE is defined as the data center's total input power divided by the power consumed by actual information technology equipment such as servers, switches, and routers. The work of Andrae et al. includes predictions for a longer horizon with > 600 TW h of annual data center consumption expected in 2020 [99]. However, this seems to be the result of an exponential extrapolation, which is not shared by other reports. For example, the *United States Data Center Energy Usage Report* by Shehabi et al. from the Berkeley National Laboratory, published in 2016, estimates an almost constant annual consumption of ≈ 70 TW h since 2008 and includes scenarios with stable consumption as well as ones with a reduction to 40 TW h per year [100]. For

Germany, a report by Stobbe et al. estimates 9 TW h consumption of data centers in 2007 and 6.4 TW h for telecommunication networks [101].

These numbers show that power supplies for data centers are a considerable market: Assuming a cost range of 0.05 to 0.2 EUR per kW h, a consumption of 300 TW h results in 15 to 60 billion EUR of annual electricity cost for data center operators. Note that until the year 2005 a PUE of 2 was reported as typical value, which means that 50 % of the total electricity was required by the infrastructure, such as cooling, power distribution etc. This has lead to an ongoing trend of improving the efficiency of the installations (e.g. by optimizing the cooling air flow) and that of the power supplies. Accordingly, PUE values around 1.8 are reported for 2012 with best practice data centers achieving values as low as 1.2 [98, 100]. Despite this trend to higher efficiency, Koomey writes in [94] that market structures and practices lead to a minimization of first cost instead of total cost of ownership. Similarly Brill recommends to "incorporate site costs into the economic analysis of new application decisions" and to "change IT governance to incorporate energy consumption as a significant component to total cost of ownership" in [102].

It is interesting to notice that similar considerations, regarding the cost of dissipated power in central offices of telephone networks, were published already in 1978 by Goldstein et al. [103]. The authors present a method to calculate the capital equivalent worth of saving one watt, continuously dissipated over a defined service life. This allows to make cost-optimal investment decisions regarding equipment (e.g. power supplies) with different first cost and losses. In their paper they conclude that "First, greater attention needs to be given to life-cycle cost during system and equipment design; results which are based on first cost alone are frequently misleading. For instance, the cost of energy dissipated in circuit components such as diodes and transistors may be far more significant than the first cost of the components themselves." This shows that there is an economic driver to increase the efficiency of data center power supply systems including PFC rectifiers.

1.4 Discussion

As described in the previous section, several applications, such as electric vehicle charging, dc microgrids and dc data center power supplies, require a power conversion between the three-phase ac mains and varying, lower dc voltage. In these cases, three-phase buck-type PFC rectifiers are promising circuits as they perform the power conversion in a single-stage, which reduces the control complexity and potentially allows to reduce losses. Achieving a

high conversion efficiency, ideally as high as 99 %, is especially important for data centers in order to minimize electricity cost. However, minimizing losses is also beneficial from an ecological point of view, as about two thirds of the world-wide electricity production uses fossil fuels, thereby contributing to global warming. With an increasing number of electric vehicles and the associated battery charging infrastructure, the environmental impact of three-phase PFC rectifiers can be expected to increase further.

Considering the buck-type rectifiers introduced in **Section 1.1.2**, the Integrated Active Filter rectifier [**Fig. 1.6(c)**] and the SWISS Rectifier [**Fig. 1.6(d)**] are promising circuits. Both utilize an input stage that is commutated at mains frequency only, which can be implemented with semiconductor elements optimized for very low conduction losses. Essentially, both circuits use two dc-dc converters to perform the required voltage conversion between the three-phase mains and the dc output and therefore allow rather simple modulation and control schemes. Due to the employed input stage both circuits have better utilization of the switching stages, in terms of the sum of semiconductor rms currents compared to the output current, than other buck-type rectifier circuits. Note that the IAF rectifier has only three semiconductor elements in its main conduction path, while the SWISS Rectifier has four, however the IAF rectifier requires an additional inductor and has higher overall switching losses. The SWISS Rectifier and IAF rectifier circuits are therefore selected for a closer analysis in this thesis. As the SWISS Rectifier is a relatively new concept, several questions remain, for example regarding reactive power generation at the mains interface, operation with distorted mains voltages, the impact of distortions on the input current THD, and regarding the interleaving of several switching stages to improve efficiency and/or maximum output power.

Regarding isolated matrix-type rectifiers the phase-modular IMY/D rectifier [**Fig. 1.13(h)**] is an interesting option. It features a wide input voltage range as its phase-modules can be connected either in star or delta-configuration. Using three single-phase phase-modules, which are similar to a dc-dc forward converter, allows for straightforward modulation and control schemes that ensure sinusoidal input currents, as well as to achieve ZVS under full-load. Unlike other phase-modular circuits, it does not require a connection to the three-phase mains' star-point, which is typically not available in an industrial setup. As in most phase-modular rectifiers, one isolation transformer per phase-module is required in the IMY/D rectifier, but only one common dc output inductor is used.

Finally, the matrix-type DAB buck-boost PFC rectifier (**Fig. 1.11**) is se-

lected as a promising phase-integrated, isolated PFC rectifier. It features a simple structure consisting of only six bidirectionally conducting and blocking switches on the primary-side and a conventional full-bridge of switches on the secondary-side. Those are connected via a series inductance and an isolation transformer, which can be designed to provide the required inductance value by utilizing its leakage flux. In this case an isolated PFC rectifier results that exposes only a single magnetic component to switching frequency voltages and currents, because the last stage of the ac input filter is formed by capacitors, as in all buck-type rectifiers. Due to its similarity to DAB dc-dc converters, the rectifier allows buck and boost operation, thereby giving it very wide input and output voltage ranges. However, the matrix-type DAB rectifier's modulation is quite complex, due to the absence of impressed currents with a low ripple. Furthermore, sophisticated commutation schemes are required for the primary-side switches to ensure that the transformer current, impressed by the leakage inductance, is not interrupted and that no input filter capacitors are short circuited at any time, as this would typically lead to the rectifier's destruction.

1.5 Aims and Contributions

Based on the considerations given above and due to the fact that three-phase buck-type PFC rectifiers have received considerably less attention than boost-type systems in the scientific literature, the aim of this thesis is to answer questions regarding the modulation, control and design of non-isolated and isolated three-phase buck-type PFC rectifiers. As economical and ecological considerations show a demand for very high efficient power supplies, this thesis aims to set a benchmark in terms of highest achievable efficiency for isolated and non-isolated buck-type PFC rectifiers, using commercially available materials, such as wide bandgap semiconductor devices and magnetic core materials. Therefore, the non-isolated SWISS Rectifier and the IAF rectifier, as well as the isolated IMY/D and the matrix-type DAB rectifiers are studied, in order to answer technical and scientific questions regarding achievable input current THD, reactive power generation at the mains interface, interleaving of switching stages to reduce losses and/or increase output power and highest achievable efficiency. The main contributions of this thesis are listed in the following:

- The analysis of modulation schemes for the SWISS Rectifier which enable the generation of reactive power at the ac mains interface using

analytical models, numerical simulations and verification by measurements on a hardware prototype.

- Operation of the SWISS Rectifier at unsymmetric mains voltages is analyzed and a control scheme is proposed that allows to achieve ohmic mains behavior.
- Distortions of the ac input currents exist in the SWISS Rectifier at the mains voltage sector boundaries, which impact its input current THD. The root cause of these distortions is analyzed and an analytical model of the resulting input current THD is derived.
- Based on the analysis of the SWISS Rectifier's input current distortions, different mitigation strategies are proposed and verified by simulations and measurements. Their impact on the overall rectifier performance, such as efficiency, is analyzed.
- A concept for life-cycle-cost-optimal converter design is proposed as a means to provide a fast and easy to use tool to select optimal semiconductors and magnetic components during the design phase of a power converter. The method is demonstrated by the design of an IAF rectifier for dc data centers, showing that efficiencies above 99 % are economically and technically feasible.
- Modulation and control schemes for the IMY/D rectifier are analyzed and verified by simulations and measurements. It is shown that ZVS can be achieved and a third harmonic current injection method is proposed that allows an increased output voltage range and/or lower conduction losses.
- Finally, a model of the isolated matrix-type DAB three-phase rectifier is developed and used to derive a modulation scheme which achieves PFC functionality, soft-switching and minimal conduction losses. Using these results, a 99 % efficient isolated PFC rectifier with a power density of 4 $\mathrm{kW/dm^3}$ is designed, implemented and tested.

1.6 Outline

This thesis is divided into nine chapters, organized as follows:

- **Chapter 1** provides an introduction to three-phase PFC rectifiers and lists a number of non-isolated and isolated matrix-type, boost-, buck-

and buck-boost-type three-phase PFC rectifier circuits published in scientific literature. This is done to provide an overview of known circuits and to point out their origins and inventors. Out of about 40 circuits, two non-isolated and two isolated ones are selected for detailed analysis in this thesis. Additionally three potential applications for buck-type PFC rectifiers are introduced and the economic factors creating a need for very high efficient rectifiers in data centers are outlined.

- **Chapter 2** analyzes a phase-oriented pulse width modulation (PWM) scheme for the bidirectional SWISS Rectifier that is capable of creating mains input currents that are phase shifted up to ±30° with respect to the mains voltages. This allows the generation of capacitive or inductive reactive power at the mains, which might be required in certain applications to satisfy the reactive power demand of other loads connected to the same ac mains, such as induction motors. Additionally, the operation with unsymmetrical mains voltages is analyzed and an extension of the control structure is proposed that allows to operate the rectifier with ohmic input characteristic.

- **Chapter 3** focuses on the THD of the SWISS Rectifier's ac input currents, which usually contain distortions at every 60° mains voltage sector boundary. It is shown that this is due to the switching frequency voltage ripple at the input filter capacitors and an analytic equation is derived to estimate the resulting THD given basic circuit parameters, such as output power, switching frequency and input filter inductance and capacitance values. Based on this analysis a modification of the original circuit is proposed that reduces the conduction losses in the SWISS Rectifier's input stage and allows an intermittent PWM of the input stage in order to mitigate the current distortions. Measurement results obtained with a 7.5 kW SWISS Rectifier prototype confirm that the input current THD can be reduced from 4.2 % to 1.4 % using the proposed technique.

- **Chapter 4** describes an alternative solution to reduce the switching frequency voltage ripple of the ac input capacitors and the input current distortions by interleaving the SWISS Rectifier's dc-dc output stage. In order to minimize the losses and/or volume of the resulting output filter, a new magnetic element is proposed that combines two current compensated ICTs and a common-mode filter inductor onto a single magnetic core and its magnetic and electric properties are analyzed in

detail. Furthermore, the equations for selecting semiconductors that achieve minimal losses and those for the dimensioning of the magnetic elements are derived. Based on these results, a 99.3 % efficient 8 kW SWISS Rectifier prototype using SiC MOSFETs, with a power density of 4 kW/dm^3, is designed, implemented and tested.

- **Chapter 5** demonstrates how life cycle cost (LCC), the sum of investment cost and that of the power dissipated during the service life, can be used to design cost-optimal converters. The use of cost as a single-valued objective function simplifies the converter design procedure, because Pareto trade-offs, which generally occur when designing any power electronics converter, can be avoided and/or masked. To illustrate the principle, a cost-optimal three-phase buck-type IAF PFC rectifier is designed as an input stage for a 380 V dc data center power distribution systems. Measurement results on the implemented prototype confirm a full-load efficiency of 99 % and a power density of 4 kW/dm^3 for an 8 kW rectifier, showing that ultra-high efficiencies are economically and technically feasible for powering data centers and communication technology equipment.

- **Chapter 6** analyzes advanced modulation and control strategies for the phase-modular three-phase matrix-type IMY/D rectifier. The circuit uses three individual phase-modules that can be connected in star (Y)- or delta (Δ)-configuration at the mains input, which allows a wide input voltage range without oversizing components. A modulation scheme achieving zero voltage switching (ZVS) is proposed and validated by measurements on a 7.5 kW hardware prototype. A third harmonic current injection method is proposed for the Δ-configuration that allows to increase the output voltage range and/or to reduce the conduction losses.

- **Chapter 7** focuses on the isolated matrix-type DAB three-phase PFC rectifier (IMDAB3R). An optimization problem is formulated based on a simplified circuit model to find a modulation strategy that achieves sinusoidal mains input currents and soft-switching with minimal conduction losses. Using this off-line optimized modulation scheme a 99 % efficient 8 kW rectifier prototype with a power density of 4 kW/dm^3 is designed. Measurements verify a full-load efficiency of 99.0 % with an input current THD of 3.0 %.

- **Chapter 8** proposes the novel Zurich Rectifier as an alternative to

the IMDAB3R. By replacing the direct matrix converter with an input voltage selector and a subsequent T-type inverter the complexity of the pulse width modulator is reduced, as multi-step commutation patterns are avoided. Calculations show that the Zurich Rectifier can achieve the same, or lower, losses than the IMDAB3R when using the same semiconductor devices.

- Finally, the main results and findings of this thesis are summarized in **Chapter 9**. Conclusions are drawn and an outlook for further research is provided.

1.7 List of Publications

Significant parts of the work presented in this thesis have already been published in international conference proceedings and in scientific journals. Some of the key ideas have also been filed as patent applications. All publications written in the course of this PhD thesis or in the scope of other projects are listed in the following.

Journal Papers

- L. Schrittwieser, M. Leibl, J. W. Kolar, "99% Efficient Isolated Three-Phase Matrix-Type DAB Buck-Boost PFC Rectifier," *IEEE Trans. on Power Electronics*, under review.

- L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar and T. B. Soeiro, "99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems," in *IEEE Trans. on Power Electronics*, vol. 34, no. 1, pp. 126 - 140, January 2019. DOI: 10.1109/TPEL.2018.2817074

- L. Schrittwieser, P. Cortés, L. Fässler, D. Bortis and J. W. Kolar, "Modulation and Control of a Three-Phase Phase-Modular Isolated Matrix-Type PFC Rectifier," in *IEEE Trans. on Power Electronics*, vol. 33, no. 6, pp. 4703 - 4715 , June 2018. DOI: 10.1109/TPEL.2017.2726342

- L. Schrittwieser, J. W. Kolar and T. B. Soeiro, "Novel SWISS Rectifier Modulation Scheme Preventing Input Current Distortions at Sector Boundaries," in *IEEE Trans. on Power Electronics*, vol. 32, no. 7, pp. 5771 - 5785, July 2017. DOI: 10.1109/TPEL.2016.2609935

- L. Schrittwieser, J. W. Kolar and T. B. Soeiro, "99% Efficient Three-Phase Buck-Type SiC MOSFET PFC Rectifier Minimizing Life Cycle Cost in DC Data Centers," in *CPSS Trans. on Power Electronics and Applications*, vol. 2, no. 1, pp. 47 - 58, March 2017. DOI: 10.24295/cpsstpea.2017.00006

Conference Papers

- L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar and T. B. Soeiro, "99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC),* Tampa, FL, USA, March 2017. DOI: 10.1109/APEC.2017.7931000

- L. Schrittwieser, J. W. Kolar and T. B. Soeiro, "99% Efficient Three-Phase Buck-Type SiC MOSFET PFC Rectifier Minimizing Life Cycle Cost in DC Data Centers," in *Proc. of IEEE Intern. Telecommunications Energy Conference (INTELEC),* Austin, TX, USA, October 2016. DOI: 10.1109/INTLEC.2016.7749146

- L. Schrittwieser, J. W. Kolar and T. B. Soeiro, "Novel Modulation Concept of the SWISS Rectifier Preventing Input Current Distortions at Sector Boundaries," in *Proc. of Control and Modeling for Power Electronics Conference (COMPEL),* Vancouver, BC, Canada, July 2015. DOI: 10.1109/COMPEL.2015.7236476

- L. Schrittwieser, M. F. Vancu, J. W. Kolar and T. B. Soeiro, "Control of the Input Characteristic and the Displacement Factor of Uni- and Bidirectional SWISS Rectifier for Symmetrical and Unsymmetrical Three-Phase Mains," in *Proc. of Intern. Conference on Power Electronics (ICPE-ECCE Asia),* Seoul, Korea, June 2015. DOI: 10.1109/ICPE.2015.7167764

Patents

- L. Schrittwieser, J. W. Kolar, "Potentialgetrennter AC-DC-Konverter," Swiss Patent Application, filed September 2018.

- M. Leibl, L. Schrittwieser, J. W. Kolar, D. Bortis and M. Antivachis, "Konverter zur Übertragung von elektrischer Energie zwischen einem DC und einem AC-System," Swiss Patent Application, filed September 2017.

- M. Leibl, L. Schrittwieser and J. W. Kolar, "Verfahren und Konverter zur potentialfreien elektrischen Energieübertragung," Swiss Patent Application, filed August 2017.
- L. Schrittwieser, M. Leibl, M. Haider, F. Thöny and J. W. Kolar, "Magnetische Drossel, Umrichterabschnitt und Umrichter," Swiss Patent Application, filed March 2017.
- L. Schrittwieser, J. W. Kolar, T. B. Soeiro and F. Canales, "Electrical Converter and Control Method," European Patent Application EP 3113345, filed July 2015.

Further Scientific Contributions

- J. Azurza Anderson, E. J. Hanak, L. Schrittwieser, J. W. Kolar, G. Deboy, "Towards a 99.5% Efficient All-Silicon Three-Phase Seven-Level Hybrid Active Neutral Point Clamped Inverter," in *Proc. of IEEE Intern. Power Electronics and Application Conference and Exposition (PEAC),* Shenzhen, China, November 2018.
- M. Antivachis, D. Bortis, L. Schrittwieser and J. W. Kolar, "Three-Phase Buck-Boost Y-Inverter with Wide DC Input Voltage Range," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC),* San Antonio, Texas, USA, March 2018. DOI: 10.1109/APEC.2018.8341214
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2

SWISS Rectifier Input Characteristic and Displacement Factor

This chapter introduces a phase-oriented control strategy for the uni- and bidirectional three-phase, buck-type SWISS Rectifier. It allows phase shifted sinusoidal input currents, which enables the generation of capacitive or inductive reactive power at the converter's ac mains interface. Furthermore, the operation of the SWISS Rectifier with unsymmetrical ac mains voltages is analyzed. Modifications of the control structure, allowing constant ac input power or ohmic mains behavior even with unsymmetrical ac voltages are presented. Simulations and measurements taken on a 7.5 kW bidirectional SWISS Rectifier hardware prototype demonstrate the validity of the theoretical considerations.

2.1 Introduction

The charging of Electric Vehicle batteries requires a conversion of the three-phase ac mains' voltage into an adjustable dc output voltage level [73]. This is also the case for future LV dc distribution systems and dc micro grids, which typically require a connection to the existing ac utility grid [84].

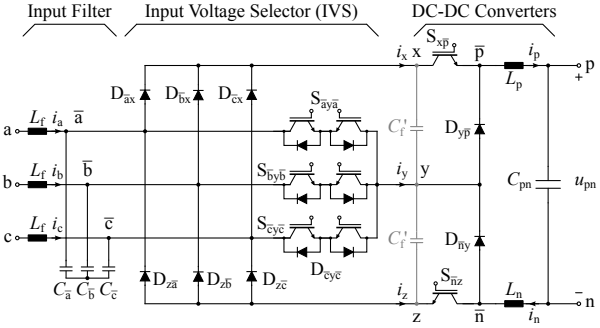

Fig. 2.1: Circuit topology of the unidirectional SWISS Rectifier, which is capable of ac-to-dc power transfer only. It consists of a low-pass input filter, a mains frequency commutated Input Voltage Selector (IVS) and two buck-type dc-dc converters as introduced in [14].

Similar dc distribution systems, with a voltage of ≈ 400 V dc, are expected to reduce the power consumption and capital cost of data centers and telco sites by reducing the number of energy conversion stages [92, 93].

Typically, if the voltage on the dc bus is lower than the full-wave rectified ac voltage, two-stage systems are used. These consist of a front-end boost-type power factor correction (PFC) rectifier stage with a 700 V − 800 V dc output, connected in series with a dc-dc converter to achieve the desired lower dc bus voltage. For these applications buck-type PFC converters, like the SWISS Rectifier, are an alternative, allowing a single-stage energy conversion between the three-phase mains and a dc bus with lower voltage.

The schematic of the unidirectional SWISS Rectifier, as introduced in [14] and [37], is shown in **Fig. 2.1**. It consists of an ac-side low-pass input filter, an Input Voltage Selector (IVS), two dc-dc buck converters and a dc output capacitor C_{pn}. Additional capacitors C_{f}' are used to minimize the commutation inductances of the buck converters. The IVS uses a three-phase full-wave diode bridge and a third harmonic injection network to connect the input phase with highest potential to node x, the one with lowest potential to node z and the remaining phase to node y. Therefore, the injection network's switches $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$ and $S_{\bar{c}y\bar{c}}$ are switching with twice the mains frequency.

A bidirectional extension of the SWISS Rectifier, introduced in [104], is shown in **Fig. 2.2**. The additional switches allow a power transfer from the dc to the ac-side. In order to enable this feedback of power into the mains the current in the dc-dc converter inductors L_{p} and L_{n} needs to be

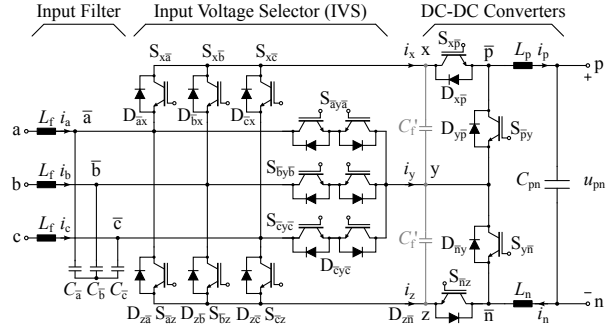

Fig. 2.2: Schematic of the bidirectional SWISS Rectifier, which is capable of ac-to-dc and dc-to-ac power transfer. It consists of a low-pass input filter, a bidirectional IVS (commutated at mains frequency) and two bidirectional dc-dc converters [104].

reversed. Therefore, switches $S_{\bar{p}y}$ and $S_{y\bar{n}}$ are connected in parallel with the buck converter diodes $D_{y\bar{p}}$ and $D_{\bar{n}y}$ of the unidirectional SWISS Rectifier. Furthermore, the diode bridge of the IVS is extended with six additional switches ($S_{x\bar{k}}$, $S_{\bar{k}z}$, $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$) in order to allow it to conduct the reversed currents $i_x < 0$ and $i_z > 0$. These additional switches are turned on when their antiparallel diode would conduct in the unidirectional SWISS Rectifier. Hence, the switches $S_{x\bar{a}}$, $S_{x\bar{b}}$, $S_{x\bar{c}}$, $S_{\bar{a}z}$, $S_{\bar{b}z}$ and $S_{\bar{c}z}$ are operated at mains frequency.

In **Section 2.2** a phase-oriented PWM control method for the uni- and bidirectional SWISS Rectifier, which allows the generation of reactive power on the ac-side input, is described together with an analysis of the topology's reactive power generation limits. Furthermore analytical formulas for the current stresses of the semiconductors and passive components are derived. Simulation results are included to validate the theoretical considerations. In **Section 2.3** the operation of the SWISS Rectifier with unsymmetrical mains voltages is analyzed. An extension to the basic control structure is proposed which achieves ohmic behavior at the ac input even with unsymmetrical mains voltages. **Section 2.4** presents measurements taken on a 7.5 kW SWISS Rectifier hardware prototype that demonstrate the proposed concept's feasibility.

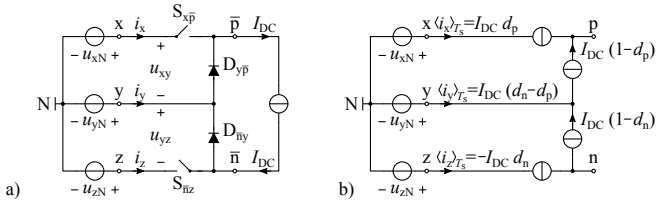

Fig. 2.3: Simplified circuit models of the unidirectional SWISS Rectifier. In a) the mains voltages, input filter and IVS are replaced with equivalent voltage sources and the output inductors (L_p and L_n) are replaced with a constant current source. By averaging over one switching frequency period T_s the schematic shown in b) results, where d_p is the duty cycle of $S_{x\bar{p}}$ and d_n is the duty cycle of $S_{\bar{n}z}$.

2.2 Operation with Phase Shifted AC Currents

As shown in [37], the SWISS Rectifier's dc-dc converters can be controlled such that the rectifier system's ac-side input currents $i_{a,b,c}$ are sinusoidal and in phase with the grid voltages. This can also be seen from the simplified schematic shown in **Fig. 2.3**. By assuming a constant dc output inductor current I_{dc}, the local average $\langle i_x \rangle_{T_s}$ of i_x over one switching frequency period T_s, can be calculated as

$$\langle i_x \rangle_{T_s} = I_{dc}\, d_p \,, \tag{2.1}$$

where d_p is the duty cycle of $S_{x\bar{p}}$. This implies that d_p can be used to control the local average of the input current i_x and hence the current in the mains' line connected to node x by the IVS. In the same way, $S_{\bar{n}z}$ and d_n can be used to control i_z. Therefore, d_p and d_n can be used to achieve sinusoidal ac input currents and to create reactive power at the system's ac input by controlling the input displacement factor. However, the generation of reactive power reduces the output voltage range as will be shown in the following.

2.2.1 Output Voltage Range

In order to achieve sinusoidal ac-side input currents the duty cycle signals d_p and d_n have to be piecewise sinusoidal as described above. Furthermore, the two dc-dc converters create a constant dc output voltage from the three output voltages of the IVS (u_{xN}, u_{yN}, u_{zN}),

$$\left\langle u_{\bar{p}N} \right\rangle_{T_s} = u_{yN}\left(1 - d_p\right) \;+\; u_{xN}\, d_p \,, \tag{2.2}$$

$$\langle u_{\bar{n}N} \rangle_{T_s} = u_{yN}\left(1 - d_n\right) \;+\; u_{zN}\, d_n \,, \tag{2.3}$$

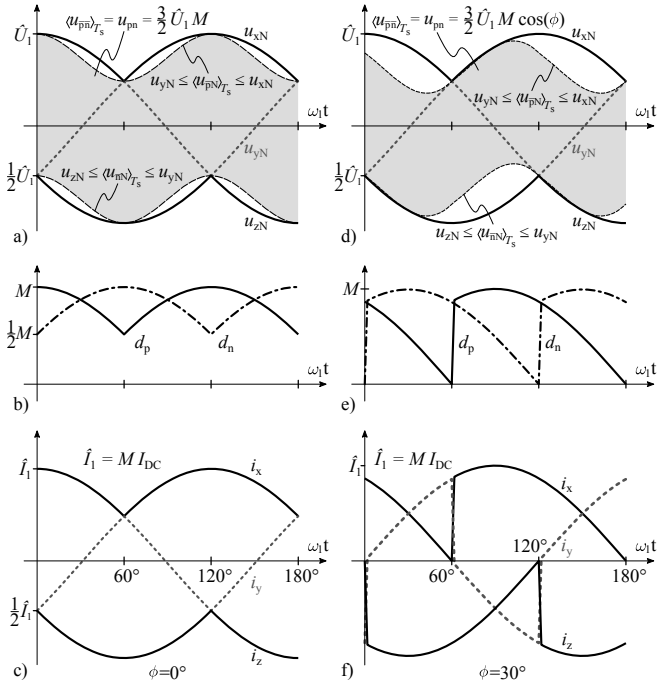

Fig. 2.4: Comparison of in phase ac input currents (a-c) and phase shifted ac input currents (d-f). a) and d) show the IVS output voltages and dc output voltage range. b) and e) show the duty cycle signals d_p and d_n which generate the ac input currents shown in c) and f).

where $\left\langle u_{\bar{\mathrm{p}}\mathrm{N}} \right\rangle_{T\mathrm{s}}$ is the local average of $u_{\bar{\mathrm{p}}\mathrm{N}}$ over one switching period T_s. Note that $\left\langle u_{\bar{\mathrm{p}}\mathrm{N}} \right\rangle_{T\mathrm{s}}$ is bounded by $u_{\mathrm{x}\mathrm{N}}$ and $u_{\mathrm{y}\mathrm{N}}$, while $\langle u_{\bar{\mathrm{n}}\mathrm{N}} \rangle_{T\mathrm{s}}$ is bounded by $u_{\mathrm{y}\mathrm{N}}$ and $u_{\mathrm{z}\mathrm{N}}$. A drawing of the resulting signals is shown in **Fig. 2.4 a-c)**.

For ohmic mains behavior the dc output voltage u_pn is therefore limited to $1.5\,\hat{U}_1$, where $\hat{U}_1$ denotes the amplitude of the mains' phase voltage [cf. **Fig. 2.4 a**]. Note that the amplitude of the two duty cycle signals (d_p, d_n) defines the system's modulation index $M \in [0;1]$ which sets the dc output voltage, $u_\mathrm{pn} = 1.5\,\hat{U}_1\,M$.

If the ac-side input currents are phase shifted by the angle ϕ (w.r.t. the mains' phase voltages) this implies that the duty cycle signals have to be shifted as well [cf. **Fig. 2.4 e)**]. Applying the phase shifted signals d_p and d_n

to the input voltages u_{xN}, u_{yN} and u_{zN} results in a reduced output voltage of

$$u_{pn} = \left\langle u_{\bar{p}\bar{n}} \right\rangle_{T_s} = \frac{3}{2} I_{dc} M \cos(\phi) \qquad M \in [0;1] \ , \tag{2.4}$$

which can also be seen in **Fig. 2.4 d)**.

2.2.2 Reactive Power Generation Limits

In **Fig. 2.4 d-f)** the ac-side input phase currents are shifted by $\phi = 30°$. Note that either d_p or d_n reaches zero at every mains' voltage sector boundary (i.e. every 60°). Any further increase of ϕ would result in negative duty cycle values and hence in a low-frequency distortion of the ac-side input currents. In order to avoid these distortions, ϕ has to be limited to

$$-\frac{\pi}{6} \leq \phi \leq \frac{\pi}{6} \ . \tag{2.5}$$

Assuming a constant dc output current I_{dc} and neglecting any losses in the semiconductors and filter components, the active and reactive power at the converter's mains interface can be derived as

$$P = \frac{3}{2} \hat{U}_1 I_{dc} M \cos(\phi) = S_{max} M \cos(\phi) \ , \tag{2.6}$$

$$Q = \frac{3}{2} \hat{U}_1 I_{dc} M \sin(\phi) = S_{max} M \sin(\phi) \ . \tag{2.7}$$

This leads to the reactive power generation limits shown in **Fig. 2.5**. Note that the same reactive power generation limits exist for the six-switch buck-type PWM converter [105].

2.2.3 Control Structure

The phase voltage oriented control structure shown in **Fig. 2.6** allows the generation of reactive power on the rectifier's ac-side using the considerations given above. As in [14], an outer loop voltage controller $R(s)$ is used in order to control the dc output voltage u_{pn} by creating a reference signal i_{dc}^* for the underlying current controller $G(s)$. The output voltage reference u_{pn}^* is added as a feedforward signal to the current controller's output to calculate the dc-dc converter output voltage reference $u_{\bar{p}\bar{n}}^*$. Dividing by the maximum dc voltage ($1.5\,\hat{U}_1 \cos(\phi)$, cf. (2.4)) yields the modulation index M.

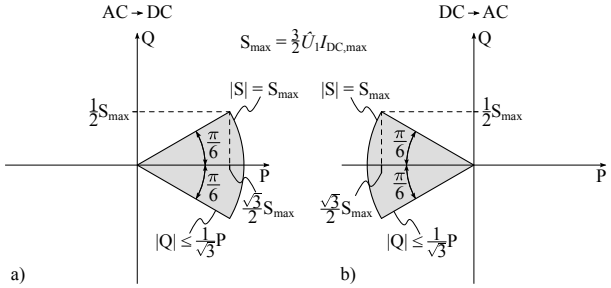

Fig. 2.5: Reactive power Q generation limits for the uni- and bidirectional SWISS Rectifier as a function of active power P and apparent power limit S_{max} for a) ac-to-dc power transfer and b) dc-to-ac power transfer.

In order to achieve sinusoidal ac input currents, M is multiplied with piecewise sinusoidal, unity amplitude shaping signals s_p and s_n. An illustration of these signals (for $\phi = 30°$) is shown in **Fig. 2.7**. The signals s_p and s_n are calculated as weighted sum from the corresponding shaping signals for ohmic behavior (s_{pd}, s_{nd}) and signals leading them by 90° (s_{pq}, s_{nq}) as shown in **Fig. 2.6**. This control structure ensures that the duty cycle signals d_p and d_n will not exceed the converter's linear operating range, provided that the conditions (2.4) and (2.5) are met.

Figure 2.8 shows simulation results for a 7.5 kW SWISS Rectifier with key parameters as listed in **Tbl. 2.1**. For the first 20 ms the rectifier operates with $\phi = -30°$ which results in inductive behavior. From $t = 20$ ms to $t = 40$ ms no phase shift is applied ($\phi = 0°$) which results in ac currents which are in phase with the phase voltages. For $t > 40$ ms the ac currents lead the voltage ($\phi = 30°$), which results in capacitive behavior.

Simulation results for the same system, but with dc-to-ac power transfer, are shown in **Fig. 2.9**. Again, the converter can be operated with a phase shift of up to $\phi = \pm 30°$ with sinusoidal input currents. This allows the generation of reactive power on the ac-side, which e.g. could be used to compensate the reactive power demand of the ac grid filter. For example, a similar approach as presented in [106] for the six-switch rectifier could be used.

2.2.4 Current Stresses

In order to select components for a SWISS Rectifier design, the current stresses of the passive components and the semiconductor devices have to be cal-

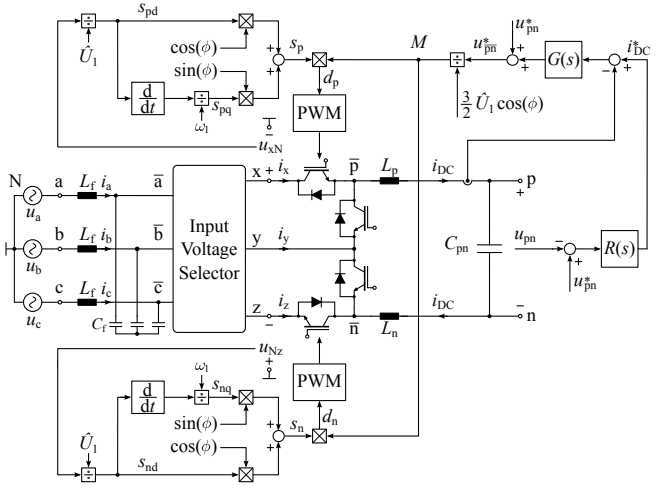

Fig. 2.6: Phase voltage oriented control structure for the bidirectional SWISS Rectifier. The sinusoidal ac-side input currents are phase shifted by ϕ with $|\phi| \leq 30°$.

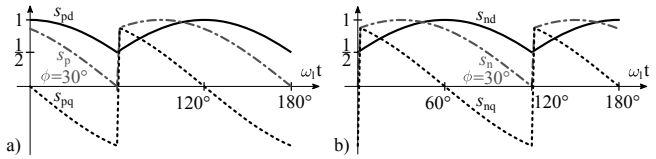

Fig. 2.7: Duty cycle shaping signals s_p and s_n used to achieve sinusoidal, phase shifted ($\phi = 30°$) inputs currents. The phase shift can be adjusted by calculating a weighted sum of active (s_{pd}, s_{nd}) and reactive (s_{pq}, s_{nq}) shaping signals as shown in **Fig. 2.6**.

culated. This section extends the analytical equations presented in [37] for phase shifted ac input currents. The following analysis assumes ac-to-dc power transfer, however, analog equations can be derived for dc-to-ac power transfer as well. Furthermore, any switching frequency ripple in the dc-side filter inductors L_p and L_n and in the ac-side filter inductors L_f is neglected.

DC-DC Converters

In ac-to-dc power transfer only the switches $S_{x\bar{p}}$ and $S_{\bar{n}z}$ and the diodes $D_{y\bar{p}}$ and $D_{\bar{n}y}$ conduct current. The switch $S_{x\bar{p}}$ conducts the dc output current I_{dc} when it is turned on while the diode $D_{y\bar{p}}$ conducts while $S_{x\bar{p}}$ is off. Neglecting

Tbl. 2.1: Specifications of Simulated SWISS Rectifier

AC Input Voltage (Line to Neutral)	$U_1 = 230\,\mathrm{V}$ rms
AC Input Frequency	$\omega_1 = 2\pi 50\,\mathrm{Hz}$
Switching Frequency	$f_s = 36\,\mathrm{kHz}$
Nominal DC Voltage	$U_{pn} = 400\,\mathrm{V}$
DC-Link Capacitor	$C_{pn} = 470\,\mu\mathrm{F}$
DC-Link Inductor	$L_p = L_n = 250\,\mu\mathrm{H}$
DC Output Power	$P = 7.5\,\mathrm{kW}$
AC Filter Inductor	$L_f = 120\,\mu\mathrm{H}$
AC Filter Capacitor	$C_{\bar{a},\bar{b},\bar{c}} = 4.4\,\mu\mathrm{F}$

the output current's switching frequency ripple this can be expressed as

$$i_{\mathrm{Sx\bar{p}}} = \begin{cases} I_{dc} & \text{if } \mathrm{S_{x\bar{p}}} \text{ is on} \\ 0 & \text{if } \mathrm{S_{x\bar{p}}} \text{ is off} \end{cases} \tag{2.8}$$

$$i_{\mathrm{Dy\bar{p}}} = I_{dc} - i_{\mathrm{Sx\bar{p}}}\,. \tag{2.9}$$

In order to calculate the rms and average current of the dc-dc converter semiconductors, the duty cycle d_p of $\mathrm{S_{x\bar{p}}}$ is required. Using **Fig. 2.6** the positive side duty cycle can be derived as

$$d_p(\omega t) = M\left[\cos(\phi)\cos(\omega t) - \sin(\phi)\sin(\omega t)\right] \tag{2.10}$$

$$\text{for } -\frac{\pi}{3} \le \omega t \le \frac{\pi}{3}\,. \tag{2.11}$$

Using (2.8) the rms current conducted by $\mathrm{S_{x\bar{p}}}$ can be calculated as

$$I_{\mathrm{Sx\bar{p}},\mathrm{rms}} = I_{dc}\sqrt{\frac{3\sqrt{3}}{2\pi}M_d} \quad \forall\ \phi \in \left[-\frac{\pi}{6};\frac{\pi}{6}\right]\,, \tag{2.12}$$

where M_d denotes the active power modulation index, defined as

$$M_d = M\cos(\phi) = \frac{P}{S_{max}}\,. \tag{2.13}$$

Similarly the average current in $\mathrm{S_{x\bar{p}}}$ can be found by integration as

$$I_{\mathrm{Sx\bar{p}},\mathrm{avg}} = I_{dc}\frac{3\sqrt{3}}{2\pi}M_d \quad \forall\ \phi \in \left[-\frac{\pi}{6};\frac{\pi}{6}\right]\,. \tag{2.14}$$

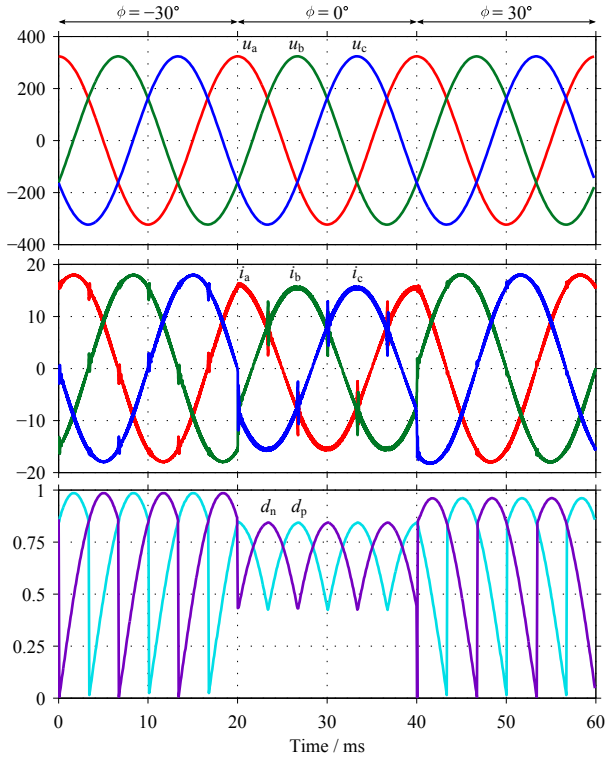

Fig. 2.8: Simulated mains voltages $u_{a,b,c}$, input currents $i_{a,b,c}$ and dc-dc converter duty cycles d_p and d_n for $\phi = -30°$ (inductive), $\phi = 0°$ (ohmic) and $\phi = 30°$ (capacitive) ac-side currents for ac-to-dc power transfer.

As the diode $D_{y\bar{p}}$ conducts the dc current I_{dc} whenever $S_{x\bar{p}}$ is turned off, its rms and average current can directly be derived using (2.12) and (2.14),

$$I_{Dy\bar{p},rms} = I_{dc}\sqrt{1 - \frac{3\sqrt{3}}{2\pi}M_d} \qquad \forall\ \phi \in \left[-\frac{\pi}{6}; \frac{\pi}{6}\right], \tag{2.15}$$

$$I_{Dy\bar{p},avg} = I_{dc}\left(1 - \frac{3\sqrt{3}}{2\pi}M_d\right) \qquad \forall\ \phi \in \left[-\frac{\pi}{6}; \frac{\pi}{6}\right]. \tag{2.16}$$

Due to the symmetry of the positive and the negative side dc-dc converters, the same current stresses result for $S_{\bar{n}z}$ and $D_{\bar{n}y}$

Note that the rms and average currents in the dc-dc converter switches

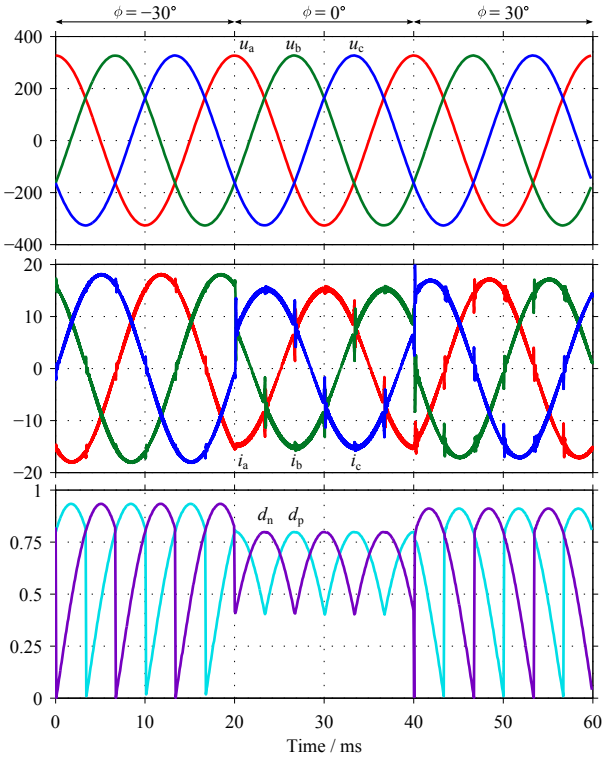

Fig. 2.9: Simulated grid voltages $u_{\mathrm{a,b,c}}$, input currents $i_{\mathrm{a,b,c}}$ and dc-dc converter duty cycles d_{p} and d_{n} for $\phi = -30°$ (capacitive), $\phi = 0°$ (ohmic) and $\phi = 30°$ (inductive) ac-side currents for dc-to-ac power transfer.

and diodes do not depend directly on ϕ, but are a function of the active power P. This implies that the current stresses, and hence the conduction losses, in the dc-dc converter semiconductors are typically independent of the reactive power Q generated on the ac-side. As the dc-dc converter switching losses depend on the input voltages u_{xy}, u_{yz} and the dc-side output current I_{dc} they do not depend on Q either. Hence only active power is processed by the dc-dc converters.

IVS Current Stresses

As can be seen from the schematic shown in **Fig. 2.1**, exactly one of the three positive side rectifier diodes ($D_{\bar{a}x}$, $D_{\bar{b}x}$, $D_{\bar{c}x}$) is conducting during each grid voltage sector. Therefore, the forward biased diode conducts the same current as the switch $S_{x\bar{p}}$. The rms and average current stress of the rectifier diodes can then be calculated using (2.12) and (2.14),

$$I_{D\bar{k}x,\mathrm{rms}} = I_{\mathrm{dc}}\sqrt{\frac{\sqrt{3}}{2\pi}M_{\mathrm{d}}} \qquad \forall\ \bar{k} \in \left\{\bar{a}, \bar{b}, \bar{c}\right\}\ , \tag{2.17}$$

$$I_{D\bar{k}x,\mathrm{avg}} = I_{\mathrm{dc}}\frac{\sqrt{3}}{2\pi}M_{\mathrm{d}} \qquad \forall\ \bar{k} \in \left\{\bar{a}, \bar{b}, \bar{c}\right\}\ . \tag{2.18}$$

Due to the circuit's symmetry the same equations result for the negative side diodes $D_{z\bar{a}}$, $D_{z\bar{b}}$, $D_{z\bar{c}}$.

In the third harmonic injection network, exactly one of the three four-quadrant switches $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$, $S_{\bar{c}y\bar{c}}$ is turned on during each grid voltage sector. Furthermore, the injection current i_{y} flows through one active switch and one diode of the turned-on four-quadrant switch. Which one of the two active switches and diodes is conducting depends on the sign of i_{y}. The same rms and average current stresses result for all four semiconductors of each four-quadrant switch due to phase symmetry. Considering only $i_{\mathrm{y}} > 0$ and the grid voltage sectors where $S_{\bar{a}y\bar{a}}$ is on ($\pi/3 < \omega t < 2\pi/3$ and $4\pi/3 < \omega t < 5\pi/3$) the current in $S_{\bar{a}y\bar{a}}$ can be expressed as

$$i_{S\bar{a}y\bar{a}} = \begin{cases} I_{\mathrm{dc}} & \text{if } d_{\mathrm{n}} > d_{\mathrm{p}} \\ 0 & \text{otherwise}\ . \end{cases} \tag{2.19}$$

The rms and average current stresses can then be found by integration:

$$I_{S\bar{k}y\bar{k},\mathrm{rms}} = I_{\mathrm{dc}}\sqrt{\frac{M_{\mathrm{d}}}{\pi}\left[\frac{1}{\cos(\phi)} - \frac{\sqrt{3}}{2}\right]} \ \forall\ \bar{k} \in \left\{\bar{a}, \bar{b}, \bar{c}\right\}, \tag{2.20}$$

$$I_{S\bar{k}y\bar{k},\mathrm{avg}} = I_{\mathrm{dc}}\frac{M_{\mathrm{d}}}{\pi}\left[\frac{1}{\cos(\phi)} - \frac{\sqrt{3}}{2}\right] \quad \forall\ \bar{k} \in \left\{\bar{a}, \bar{b}, \bar{c}\right\}\ . \tag{2.21}$$

If no reactive power is generated ($\phi = 0°$), the average current stress of the injection network switches $S_{\bar{k}y\bar{k}}$ is $\approx 15\,\%$ of the average current stress of the rectifier diodes $D_{\bar{k}x}$ and $D_{z\bar{k}}$. The same value results for the ratio of squared rms currents. This implies that the conduction losses in the injection network

switches $S_{\bar{k}y\bar{k}}$ will typically be considerably lower than the conduction losses in the rectifier diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ and the corresponding parallel switches $S_{x\bar{k}}$ and $S_{\bar{k}z}$.

Note that the rms and average current in the current injection network increase with the absolute value of the phase shift angle ϕ. The maximum rms current, occurring for $\phi = \pm 30°$, is $\approx 47\,\%$ higher compared to $\phi = 0°$ while the average current current is $\approx 115\,\%$ higher. Therefore, the conduction losses in the injection network at $\phi = \pm 30°$ are ≈ 2.15 times the losses if no reactive power ($\phi = 0°$) is generated.

Passive Components

As shown above, the generation of the reactive power on the ac-side does not influence the active power transferred to the dc-side directly. Therefore, the current and voltage stresses of the buck converter inductors (L_p, L_n) and the output capacitor (C_pn) are almost independent of the reactive power generated on the ac-side. Note that the ac-side input currents i_a, i_b, i_c depend only on the modulation index M but not on the actual phase shift angle ϕ, as can be seen from **Fig. 2.4**:

$$I_{\mathrm{a,b,c}} = I_\mathrm{dc}\,\frac{M}{\sqrt{2}} \leq I_\mathrm{dc}\,\frac{1}{\sqrt{2}}\,. \tag{2.22}$$

Finally, the rms current stress of the ac-side input filter capacitors can be calculated from the equations derived above. During each grid voltage sector either one of the rectifier diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ or the injection switch $S_{\bar{k}y\bar{k}}$ is conducting. Therefore, the corresponding rms currents can be combined using Pythagorean addition (cf. **Fig. 2.10**, $k = a$, $\bar{k} = \bar{a}$)

$$I_{\mathrm{C}\bar{\mathrm{k}},\mathrm{rms}} = \sqrt{\underbrace{I^2_{\mathrm{D}\bar{\mathrm{k}}\mathrm{x},\mathrm{rms}} + I^2_{\mathrm{Dz}\bar{\mathrm{k}},\mathrm{rms}} + 2\,I^2_{\mathrm{S}\bar{\mathrm{k}}\mathrm{y}\bar{\mathrm{k}},\mathrm{rms}}}_{I^2_{\bar{\mathrm{k}},\mathrm{rms}}} - I^2_\mathrm{k}} \tag{2.23}$$

$$= I_\mathrm{dc}\sqrt{\frac{2}{\pi}M - \frac{1}{2}M^2}\,. \tag{2.24}$$

It can be seen that the filter capacitor's rms current stress depends on the modulation index $M \in [0;1]$, but not on the phase shift angle ϕ. The highest rms current stress, which is typically required for the dimensioning of a rectifier system, can be calculated as

$$I_{\mathrm{C}\bar{\mathrm{k}},\mathrm{rms}}\,(M) \leq I_\mathrm{dc}\frac{\sqrt{2}}{\pi} \approx 0.45\,I_\mathrm{dc}\,. \tag{2.25}$$

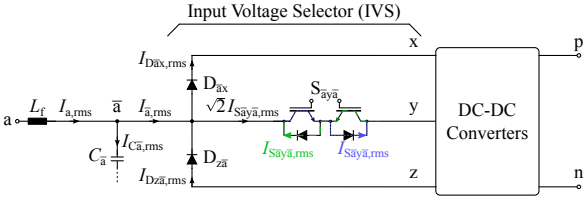

Fig. 2.10: Simplified schematic of the IVS, showing the rms currents used to calculate the filter capacitor current's rms value $I_{C\bar{a},rms}$. Phases b and c are omitted for clarity.

Numerical Results

In **Tbl. 2.2** numerical simulation results for the rms and average current stresses are compared to the corresponding values calculated using the analytical equations derived above. Two operating points, one with purely active power ($\phi = 0°$) and one with maximum reactive power ($\phi = 30°$) are shown. In both cases the deviation between the value calculated with the analytical formula and the simulation result is less than 3.4 %. Accordingly, the analytical expressions can directly be used for dimensioning the system.

2.3 Operation with Unsymmetric Mains Voltages

So far, the ac grid voltages were assumed to be purely sinusoidal, of equal amplitude and shifted by 120°. However, real ac distribution grids typically exhibit several percent of low-frequency harmonics and an asymmetry of the line voltages. In this section control strategies for constant output power and resistive mains behavior are analyzed.

2.3.1 Constant Power Transfer

It can be seen from the schematic shown in **Fig. 2.6**, that the power transferred to the rectifier's dc output is given by

$$p_{dc}(t) = u_{pn}(t)\, i_{dc}(t)\ . \tag{2.26}$$

If the output voltage controller $R(s)$ and the current controller $G(s)$ have settled, p_{dc} will be constant for stationary operation and constant load. Furthermore, the power delivered to the dc bus is almost independent of the ac

Tbl. 2.2: Comparison of Calculated and Simulated Current Stresses

	Calculation	**Simulation**	**Deviation**
ϕ	$0°$		
I_{dc}	18.75 A		
M	83.3 %		
$I_{\mathrm{Sx\bar{p},rms}}$	15.6 A	15.6 A	−0.2 %
$I_{\mathrm{Sx\bar{p},avg}}$	12.9 A	12.9 A	−0.1 %
$I_{\mathrm{Dy\bar{p},rms}}$	10.5 A	10.4 A	0.3 %
$I_{\mathrm{Dy\bar{p},avg}}$	5.83 A	5.81 A	0.3 %
$I_{\mathrm{D\bar{k}x,rms}}$	8.98 A	9.01 A	−0.3 %
$I_{\mathrm{D\bar{k}x,avg}}$	4.31 A	4.32 A	−0.3 %
$I_{\mathrm{S\bar{k}y\bar{k},rms}}$	3.53 A	3.53 A	0.3 %
$I_{\mathrm{S\bar{k}y\bar{k},avg}}$	0.67 A	0.69 A	−3.4 %
$I_{\mathrm{C\bar{k},rms}}$	8.03 A	8.20 A	−2.3 %
ϕ	$30°$		
I_{dc}	18.75 A		
M	96.2 %		
$I_{\mathrm{Sx\bar{p},rms}}$	15.6 A	15.6 A	−0.1 %
$I_{\mathrm{Sx\bar{p},avg}}$	12.9 A	12.9 A	0.0 %
$I_{\mathrm{Dy\bar{p},rms}}$	10.5 A	10.4 A	0.3 %
$I_{\mathrm{Dy\bar{p},avg}}$	5.83 A	5.81 A	0.4 %
$I_{\mathrm{D\bar{k}x,rms}}$	8.98 A	8.99 A	−0.1 %
$I_{\mathrm{D\bar{k}x,avg}}$	4.31 A	4.31 A	0 %
$I_{\mathrm{S\bar{k}y\bar{k},rms}}$	5.19 A	5.17 A	0.3 %
$I_{\mathrm{S\bar{k}y\bar{k},avg}}$	1.44 A	1.43 A	0.4 %
$I_{\mathrm{C\bar{k},rms}}$	7.26 A	7.44 A	−2.4 %

grid voltages in this case. Hence, this control scheme allows an operation of the converter with the minimal dc output filter capacitance C_{pn}.
The power drawn from the ac grid by the SWISS Rectifier is given by (2.27). If losses in the converter are neglected, the power drawn from the ac grid has to be equal to the power delivered to the dc output, as the IVS and the dc-dc converters contain only switching frequency energy storage elements,

$$p_{\mathrm{ac}}(t) = u_{\mathrm{a}}(t)\, i_{\mathrm{a}}(t) + u_{\mathrm{b}}(t)\, i_{\mathrm{b}}(t) + u_{\mathrm{c}}(t)\, i_{\mathrm{c}}(t) \tag{2.27}$$

$$p_{\mathrm{ac}}(t) = p_{\mathrm{dc}}(t) = p(t)\ . \tag{2.28}$$

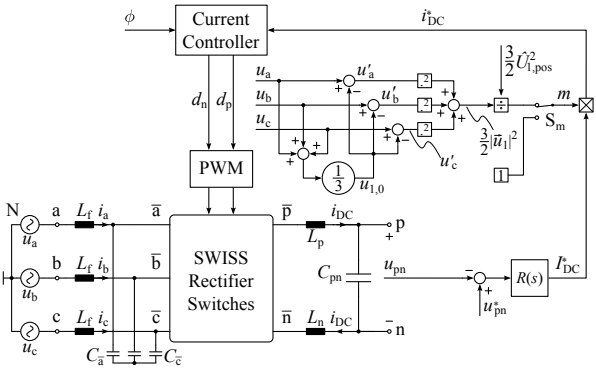

Fig. 2.11: Modified control structure allowing ohmic mains behavior for asymmetrical mains voltages $u_{a,b,c}$. The output I^*_{dc} of the dc voltage controller $R(s)$ is rescaled with a signal m that is proportional to the square of the instantaneous amplitude of the input voltage space vector, i.e. $|\vec{u}_1|^2$. The same inner loop current controller as in **Fig. 2.6** is used.

If the ac grid voltages $u_{a,b,c}$ are asymmetrical, e.g. if the amplitudes of the individual phase voltages are not equal, constant ac-side power $p_{ac} = p_{dc}$ can only be achieved with non-sinusoidal grid currents $i_{a,b,c}$.

2.3.2 Constant Input Resistance

In certain applications, the rectifier system might be required to behave like a symmetrical resistive load even with unsymmetrical grid voltages. In this case the ac-side input currents $i_{a,b,c}$ are given by (2.29). R_{in} is the resistance of one phase of a fundamental frequency rectifier equivalent circuit for star-connection. Note that, since the converter has no connection to the ac grid's neutral N, no zero-sequence current $i_0 = (i_a + i_b + i_c)/3$ can be created by the rectifier. Therefore, only the positive and negative sequence components $u'_{a,b,c}$ of the grid voltages u_1 contribute to the power flow and hence (2.30) results,

$$i_k(t) = \frac{u_k(t)}{R_{in}} \quad \forall\, k \in \{a, b, c\} \tag{2.29}$$

$$p_{ac}(t) = \frac{1}{R_{in}} \left[u'^2_a(t) + u'^2_b(t) + u'^2_c(t) \right] \quad . \tag{2.30}$$

Due do the balance of power on the ac and dc-side of the converter and (2.26), the dc-side output current $i_{\mathrm{dc}}(t)$ has to be proportional to $p_{\mathrm{ac}}(t)$. This can be achieved with the control structure shown in **Fig. 2.11**. The output signal I^*_{dc} of the dc voltage controller $R(s)$ is multiplied with a shaping signal m in order to derive the dc-link current reference for the current controller. No changes are required to the current control loop shown in **Fig. 2.6**. The signal m is calculated by subtracting the zero-sequence system of the measured input voltages $u_{\mathrm{a,b,c}}$ and summing their squares. A scaling factor of $2/3\,\hat{U}^2_{1,\mathrm{pos}}$ is used, where $\hat{U}_{1,\mathrm{pos}}$ is the amplitude of the first harmonic positive sequence system. This ensures $m = 1$ for symmetrical phase voltages with nominal amplitude $\hat{U}_1 = \hat{U}_{1,\mathrm{pos}}$.

In **Fig. 2.12** simulation results are shown for the SWISS Rectifier specified in **Tbl. 2.1**, operated at a ac grid where the amplitude of line voltage u_{a} is 23 V higher than the amplitude of line voltages u_{b} and u_{c}. Until $t = 30$ ms the converter operates with the control structure shown in **Fig. 2.6** (i.e. $m = 1$), causing low-frequency distortions of the input currents due to the constant instantaneous power flow requirement. At $t = 30$ ms the control system is changed to the structure shown in **Fig. 2.11**. Therefore, the ac-side input currents are now sinusoidal and i_{a} has a higher amplitude than i_{b} and i_{c} as expected from (2.29). Furthermore, the dc current reference signal i^*_{dc} is no longer constant due to the instantaneous power flow pulsating with twice the mains frequency.

Simulation results for the same unbalanced mains voltages as before, but with dc-to-ac power flow are shown in **Fig. 2.13**. Again constant dc power mode is selected during the first 30 ms and constant ac input resistance is used afterwards.

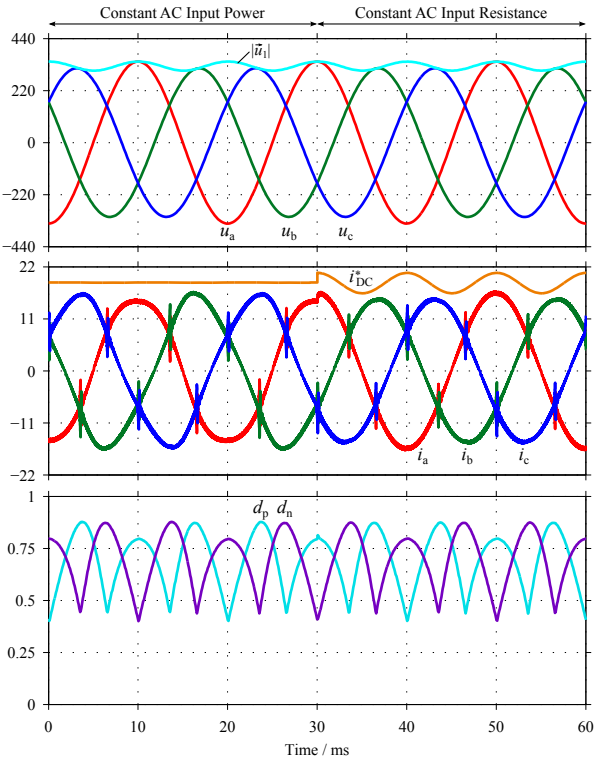

Fig. 2.12: Simulated mains line voltages $u_{a,b,c}$, input phase currents $i_{a,b,c}$, dc inductor current reference i^*_{dc} and dc-dc converter duty cycles d_p and d_n for an ac grid containing 19 V first harmonic negative sequence voltage. The rectifier transfers nominal power (7.5 kW) from the ac to the dc-side. Until $t = 30$ ms the converter is operated with constant instantaneous ac-side input power, afterwards with constant ac-side input resistance.

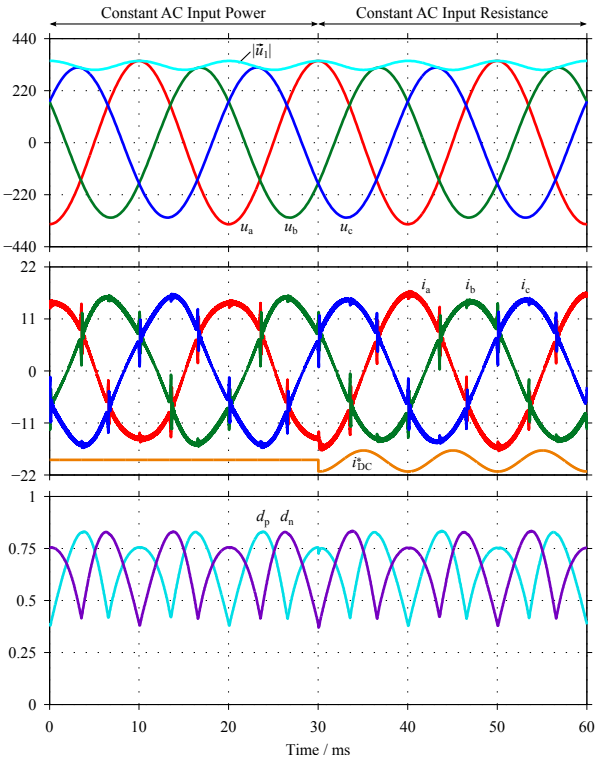

Fig. 2.13: Simulated mains line voltages $u_{a,b,c}$, input phase currents $i_{a,b,c}$, dc inductor current reference i^*_{dc} and dc-dc converter duty cycles d_p and d_n for an ac mains containing 19 V first harmonic negative sequence voltage. The rectifier transfers nominal power (7.5 kW) from the dc to the ac-side. Until $t = 30$ ms the converter is operated with constant instantaneous ac-side input power, afterwards with constant ac-side input resistance.

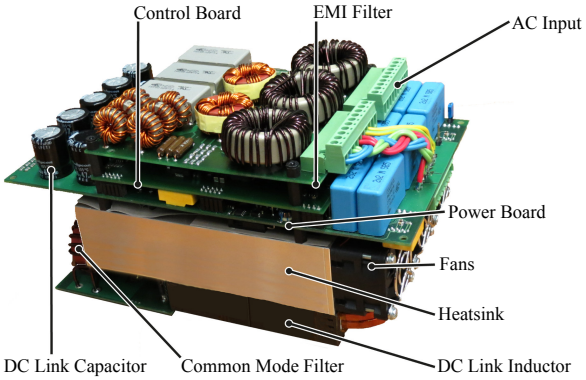

Fig. 2.14: Picture of the implemented 7.5 kW bidirectional SWISS Rectifier prototype.

2.4 Implementation Results

A SWISS Rectifier prototype has been built according to the specifications given in **Tbl. 2.1**, a picture of the prototype hardware is shown in **Fig. 2.14**. The values of all major components match those used for creating the simulation results shown in the previous sections. Measurements taken on this prototype are presented in the following.

2.4.1 Phase Shifted AC Currents

Figure 2.15 shows measurement results for ac-to-dc power transfer at 7.3 kW dc output power. Note that the voltage and current of phases a and b where measured directly, while the quantities for phase c were recreated assuming $u_a + u_b + u_c = 0$ and $i_a + i_b + i_c = 0$. During the first mains voltage period ($0 < t < 20\,\text{ms}$) the converter is operated with a phase shift of $\phi = -30°$ resulting in inductive behavior. At $t = 20\,\text{ms}$ the phase shift angle ϕ is set to zero resulting in almost purely active power drawn from the ac mains. The remaining capacitive reactive power is caused by the input filter. Finally ϕ is set to 30° at $t = 40\,\text{ms}$ resulting in capacitive behavior in the third mains voltage period shown.

The same sequence of input current phase angle steps as described above has been applied for dc-to-ac power transfer (7.5 kW) in the measurement shown in **Fig. 2.16**. For both, ac-to-dc and dc-to-ac power transfer, sinusoidal ac-side currents result for all tested values of ϕ.

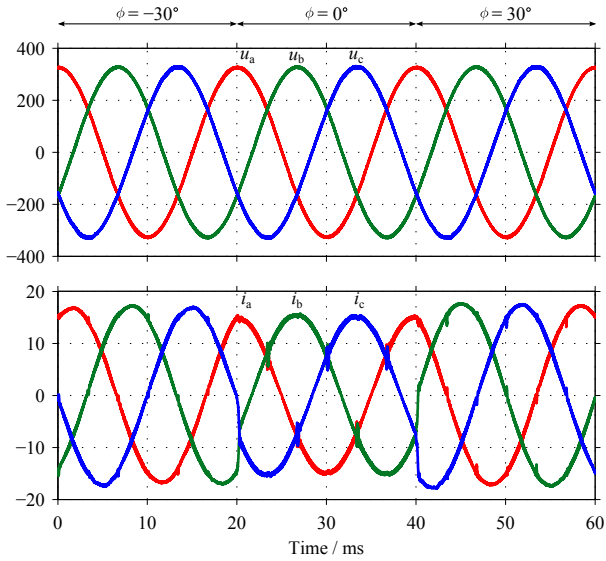

Fig. 2.15: Meaurement results for ac-to-dc power transfer, showing mains voltages $u_{a,b,c}$ and input currents $i_{a,b,c}$ for $\phi = -30°$ (inductive), $\phi = 0°$ (ohmic) and $\phi = 30°$ (capacitive) ac-side currents. Note that phase quantities a and b were measured directly, phase c quantities were recreated numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

2.4.2 Operation Under Unsymmetrical Mains Voltages

In order to test the operation of the SWISS Rectifier under unsymmetrical ac mains voltages, the control structure proposed in **Section 2.3** is implemented. A three-phase mains containing a first harmonic negative sequence voltage component with an amplitude of 19 V is used for the measurements. Note that no dc output voltage controller was used, the dc voltage u_{pn} was defined by a constant voltage source (or sink) instead.

Measurement results for ac-to-dc power transfer are shown in **Fig. 2.17**. During the first 30 ms the converter is operated with constant ac-side input power resulting in non-sinusoidal mains currents $i_{a,b,c}$. At $t = 30$ ms the control structure is changed to ohmic mains behavior, resulting in sinusoidal mains currents. Furthermore, the amplitude of i_a increases in order to achieve equal input resistance at all three lines.

The same measurement, with dc-to-ac power transfer, is shown **Fig. 2.18**. Again the SWISS Rectifier operates with constant ac power during $0 < t <$

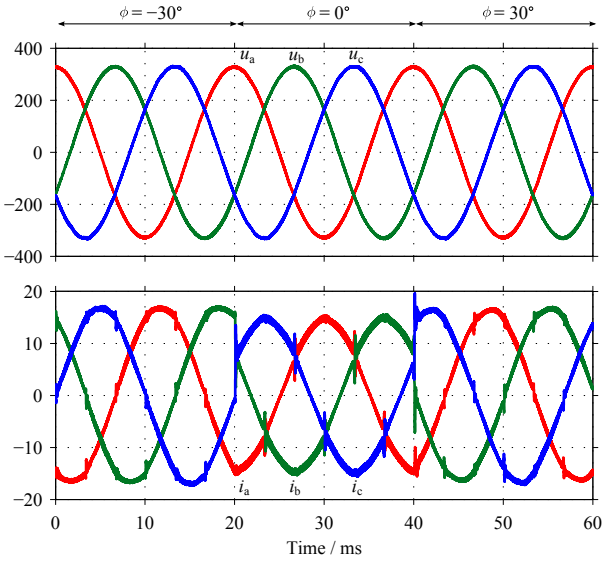

Fig. 2.16: Meaurement results for dc-to-ac power transfer, showing mains voltages $u_{a,b,c}$ and input currents $i_{a,b,c}$ for $\phi = -30°$ (inductive), $\phi = 0°$ (ohmic) and $\phi = 30°$ (capacitive) ac-side currents. Note that phase quantities a and b were measured directly, phase c quantities were recreated numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

30 ms and with constant ac resistance during 30 ms $< t <$ 60 ms.

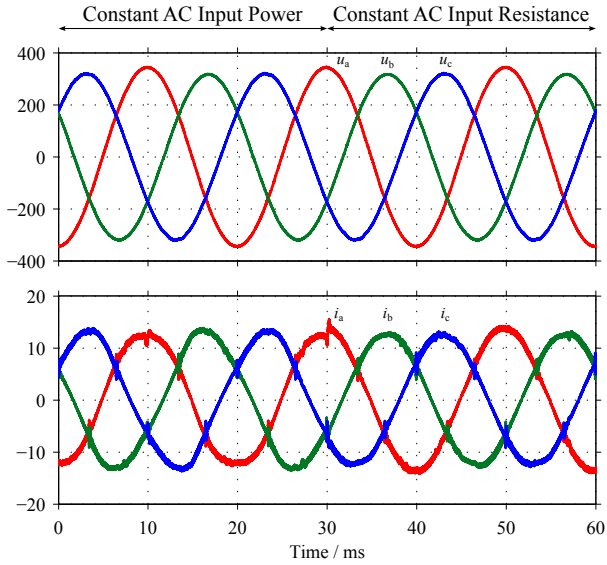

Fig. 2.17: Meaurement results for ac-to-dc power transfer, showing unsymmetrical mains voltages $u_{a,b,c}$ and input currents $i_{a,b,c}$ for constant instantaneous ac power and ohmic mains behavior. Note that phase quantities a and b were measured directly, phase c quantities were recreated numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

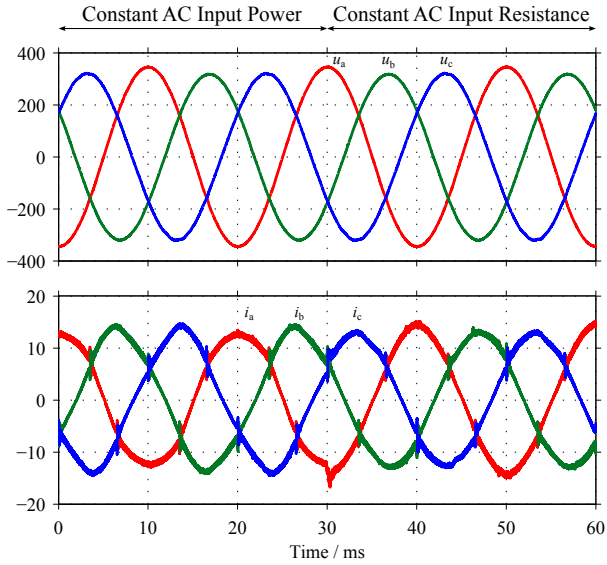

Fig. 2.18: Meaurement results for dc-to-ac power transfer, showing mains voltages $u_{a,b,c}$ and input currents $i_{a,b,c}$ for constant instantaneous ac power and ohmic mains behavior. Note that phase quantities a and b were measured directly, phase c quantities were recreated numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

2.5 Summary

In this chapter a control structure for uni- and bidirectional SWISS Rectifiers is proposed that allows the ac-side input currents to be phase shifted up to $\pm 30^\circ$ with respect to the mains' line voltages. This enables the generation of reactive power on the ac-side, which e.g. could be used to compensate the reactive power demand of the input filter or for compliance with grid codes demanding reactive power generation under certain conditions. However, the generation of reactive power reduces the output voltage range of the rectifier system.

Furthermore, analytical equations for the resulting rms and average current stresses of the converter's switches and passive components are derived for reactive power generation. The resulting formulas show that the rms current stress in the injection network's four-quadrant switches increases from $0.21\,I_{\mathrm{dc}}$ if no reactive power is generated to $0.30\,I_{\mathrm{dc}}$ at $\phi = 30^\circ$. The corresponding average current stress increases from $0.04\,I_{\mathrm{dc}}$ to $0.09\,I_{\mathrm{dc}}$. The conduction and switching losses of all other semiconductors, including the IVS' full-wave diode bridge, are not affected by the generation of reactive power.

Additionally, the operation of a SWISS Rectifier with unsymmetrical mains voltages has been analyzed. A proposed extension to the control structure allows the SWISS Rectifier to achieve ohmic mains behavior or constant power transfer even if the ac input voltages are unbalanced.

Simulations and measurements taken on a 7.5 kW laboratory prototype SWISS Rectifier demonstrate the feasibility of the proposed concepts.

3

SWISS Rectifier Modulation Scheme Preventing Input Current Distortions at Sector Boundaries

This chapter describes a new modulation concept for the uni- and bidirectional SWISS Rectifier that mitigates ac input current distortions at the mains voltage sector boundaries. An analytical model is derived and compared to simulations, which allows an estimation of the distortion's magnitude from design parameters, showing that these distortions increase the input current THD significantly. A modification of the original circuit is proposed to decouple the operation of the SWISS Rectifier's active third harmonic current injection network and its dc-dc converter switches. An algorithm is presented that allows the calculation of a temporary pulse width modulation (PWM) of the SWISS Rectifier's current injection network to mitigating the distortions. The concept is verified for both power flow directions and for operation with unsymmetrical and distorted mains voltages by measurement results taken on a bidirectional 7.5 kW SWISS Rectifier prototype. An ac input current THD of 1.3 % results for symmetric sinusoidal mains voltages and 1.4 % and 1.6 % for operation with distorted and unsymmetrical mains

voltages.

3.1 Introduction

The increasing power consumption of data centers and telecommunication equipment has led to a demand for more efficient power supply systems. As data center equipment is an intrinsic dc load, dc distribution systems are expected to provide significant gains in efficiency as rectifier stages of power supply modules can be omitted [93]. Furthermore, a direct battery buffering of the dc bus voltage allows to omit a dedicated UPS system, which increases efficiency further, improves reliability and reduces capital cost and floor space [92, 107]. Accordingly, standards for 380 V dc distribution systems have been created recently [85]. Different power delivery architectures based on dc distribution, e.g. using series-connected stacks of servers, have been described in the literature and could lead to further improvements of overall system efficiency [108].

Furthermore, several renewable energy sources (RES), such as PV modules or fuel cells generate dc power and can therefore be connected to a dc distribution systems using a dc-dc converter, which typically has a higher efficiency and lower complexity than standard dc-ac inverters. Therefore, RES can be directly connected to a data center's dc distribution system, minimizing conversion losses and forming a so-called dc microgrid. Such dc distribution systems are not limited to data centers, as loads like computers, TV sets, LED lighting and Electric Vehicles are intrinsic dc loads as well. Similar benefits as in data centers are expected from dc microgrids in office buildings, industry and residential areas. As the generation from RES does typically not match the local demand in the microgrid, an interface to the conventional ac utility grid, allowing a bidirectional energy transfer, is usually required [78, 109, 110].

As the nominal dc bus voltage of 380 V is lower than the full-wave rectified voltage of the 400 V ac mains, two-stage systems are normally used. These consist of a power factor correction stage (PFC) connected in series with a dc-dc converter. This is typically also the case for fast chargers of Electric Vehicle batteries that are powered from the three-phase mains [73, 76, 111]. In these applications buck-type PFC converters, like the six-switch buck-type rectifier [14, 105, 112–114], the three-switch buck-type PWM rectifier [39, 105, 115–117], the bidirectional nine-switch buck-type rectifier [118], the delta-type current source rectifier [32, 119] or the SWISS Rectifier (cf. **Fig. 3.1(a)** [14], are an advantageous alternative, allowing a single-stage conversion between the three-phase mains and a dc bus with lower voltage.

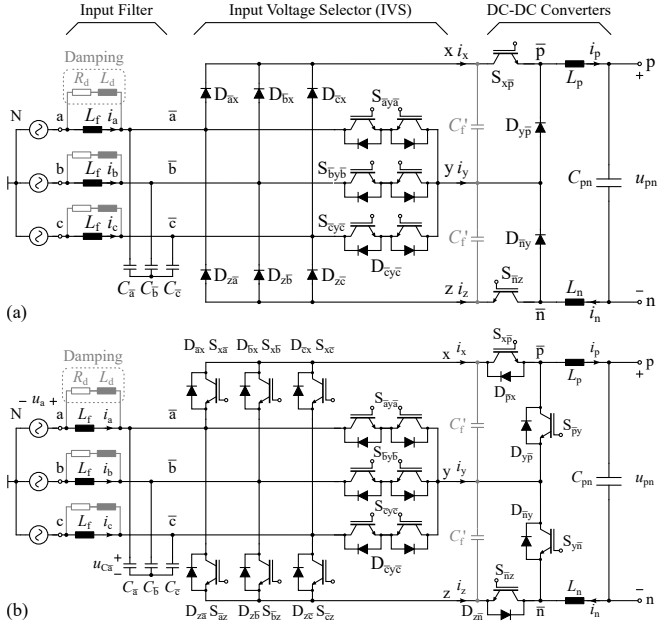

Fig. 3.1: The schematic of the unidirectional SWISS Rectifier as introduced in [14] is shown in **(a)**. An extension allowing a reversal of the dc output current (i_p, i_n), which enables bidirectional power flow, is shown in **(b)** [104].

Extensions of the SWISS Rectifier, providing bidirectional output current [104] and galvanic isolation between the ac and dc-side [53, 54], have been proposed in the literature. To cover a wide range of potential applications, both power flow directions of the bidirectional SWISS Rectifier (cf. **Fig. 3.1b**), ac-to-dc and dc-to-ac, will be analyzed separately in this chapter. The obtained results for ac-to-dc power transfer are valid also for the unidirectional SWISS Rectifier shown in **Fig. 3.1(a)**.

The schematic of the conventional SWISS Rectifier, as introduced in [14], is shown in **Fig. 3.1(a)**. It consists of an ac-side input filter, an Input Voltage Selector (IVS), two dc-dc converters ($\mathrm{S}_{\mathrm{x}\bar{\mathrm{p}}}$, $\mathrm{D}_{\mathrm{y}\bar{\mathrm{p}}}$, L_p and $\mathrm{D}_{\bar{\mathrm{n}}\mathrm{y}}$, $\mathrm{S}_{\bar{\mathrm{n}}\mathrm{z}}$, L_n) and a dc output capacitor C_pn. Additional capacitors C_f' are used to shorten the commutation paths of the two dc-dc converters. To allow a bidirectional dc output current, and hence a bidirectional power flow, additional switches can be added to the IVS and the dc-dc converters as shown in **Fig. 3.1(b)** [104]. The IVS consists of a three-phase full-wave diode bridge ($\mathrm{D}_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}\mathrm{x}}$, $\mathrm{D}_{\mathrm{z}\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}}$) with

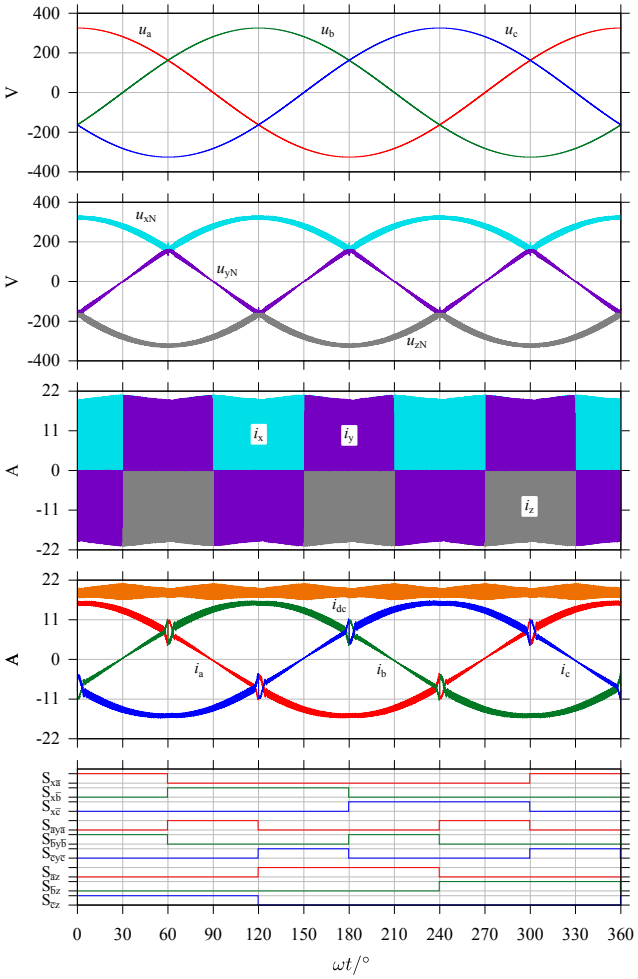

Fig. 3.2: Simulation results for the SWISS Rectifier specified in **Tbl. 3.1**, in ac-to-dc operation at nominal power. u_{xN}, u_{yN} and u_{zN} are the dc-side voltages of the IVS with reference to the ac mains' neutral N, i_x, i_y and i_z are the corresponding IVS output currents. The distortions of the ac input currents $i_{a,b,c}$ at intersections of the line voltages $u_{a,b,c}$ are visible. A low-frequency (< 10 kHz), i.e. not considering switching frequency components, input current THD of 4.2 % results.

Tbl. 3.1: Specifications of Simulated SWISS Rectifier

AC Input Voltage (Line-to-Neutral)	$U_1 = 230\,\mathrm{V_{rms}}$
AC Input Frequency	$f = 50\,\mathrm{Hz}$
Switching Frequency	$f_s = 36\,\mathrm{kHz}$
Nominal DC Voltage	$U_{pn} = 400\,\mathrm{V}$
DC-Link Capacitance	$C_{pn} = 470\,\mu\mathrm{F}$
DC-Link Inductance	$L_{p,n} = 250\,\mu\mathrm{H}$
DC Output Power	$P = 7.5\,\mathrm{kW}$
AC Filter Capacitance	$C_{\bar{a},\bar{b},\bar{c}} = 4.4\,\mu\mathrm{F}$
DC Filter Capacitance	$C_{x,y,z} = 4.4\,\mu\mathrm{F}$
AC Filter Inductance	$L_f = 120\,\mu\mathrm{H}$
AC Filter Damping	$L_d = 120\,\mu\mathrm{H}$
AC Filter Damping	$R_d = 6.8\,\Omega$

anti-parallel switches ($S_{x\bar{a},\bar{b},\bar{c}}$, $S_{\bar{a},\bar{b},\bar{c}z}$) and a third harmonic injection network ($S_{\bar{k}y\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$). Its switches are controlled such that the input phase with highest potential is connected to node x, the one with lowest potential to node z and the remaining phase to node y. Therefore, the injection network's switches $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$ and $S_{\bar{c}y\bar{c}}$ operate with twice the mains frequency, while the rectifier switches $S_{x\bar{a}}$, $S_{x\bar{b}}$, $S_{x\bar{c}}$, $S_{\bar{a}z}$, $S_{\bar{b}z}$ and $S_{\bar{c}z}$ are operated with mains frequency. This can be seen in the simulation results for a bidirectional 7.5 kW SWISS Rectifier shown in **Fig. 3.2**, where the mains voltages and the IVS output voltages u_{xN}, u_{yN} and u_{zN} are shown. Note that even though the IVS' switches are operated at mains frequency the resulting IVS currents i_x, i_y and i_z are discontinuous due to the buck-type dc-dc converters $S_{x\bar{p}}$, $S_{\bar{p}y}$ and $S_{y\bar{n}}$, $S_{\bar{n}z}$.

As described in [14], the two dc-dc converters of the SWISS Rectifier can ideally be controlled in such a way that sinusoidal ac-side input currents i_a, i_b and i_c result. While the rectifier's input currents are sinusoidal and in phase with the mains voltages, it can be seen that they are distorted at the intersections of the ac mains phase voltages u_a, u_b and u_c.

These distortions are caused by the switching frequency voltage ripple across the input filter capacitors $C_{\bar{a},\bar{b},\bar{c}}$ [120]. Note that similar input current distortions also exist in other current source rectifiers (CSR) like the six-switch buck-type CSR [113,114,121], the three-switch buck-type PWM rectifier [39,117], the delta-type CSR [119] and isolated, CSR-based circuits [122]. Detailed simulation results for the intersection interval of the line voltages u_a and u_b are shown in **Fig. 3.3**. Additionally the voltages $u_{C\bar{a}}$ and $u_{C\bar{b}}$ across the

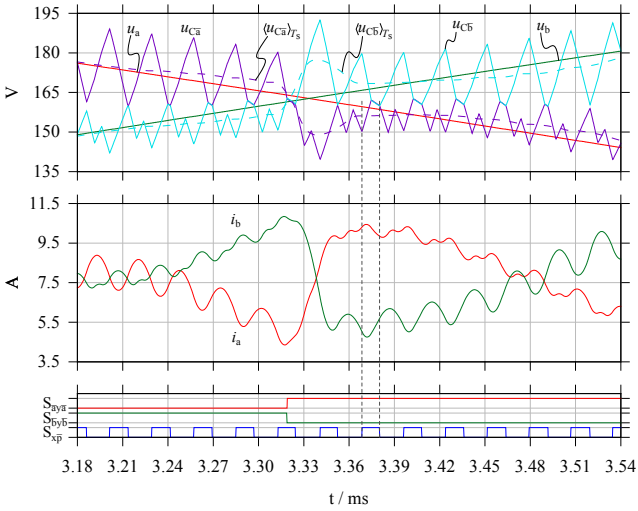

Fig. 3.3: Detailed simulation results for the first intersection at $\omega t \approx \pi/3$ showing the intersecting line voltages u_a and u_b and the corresponding filter capacitor voltages $u_{C\bar{a}}$ and $u_{C\bar{b}}$. $\langle u_{C\bar{a}}\rangle_{T_s}$ is the average of $u_{C\bar{a}}$ over one switching frequency period T_s. It can be seen that no intersection of $u_{C\bar{a}}$ and $u_{C\bar{b}}$ occurs because of $D_{\bar{a}x}$ and $D_{\bar{b}x}$ (cf. **Fig. 3.4**).

respective input filter capacitors and their local averages $\langle u_{C\bar{a}}\rangle_{T_s}$, $\langle u_{C\bar{b}}\rangle_{T_s}$ over one switching period T_s are shown. Neglecting the voltage drop due to the fundamental of the input current i_a across L_f, the local average $\langle u_{C\bar{a}}\rangle_{T_s}$ equals the corresponding mains voltage u_a before the current distortion starts. The same holds for $\langle u_{C\bar{b}}\rangle_{T_s}$ and u_b. As the voltages u_a and u_b approach each other, the instantaneous voltages $u_{C\bar{a}}$ and $u_{C\bar{b}}$ would have to intersect for this to hold true. However, this is not the case as shown in **Fig. 3.3**, because the diodes $D_{\bar{a}x}$ and $D_{\bar{b}x}$ are starting to conduct once $u_{\bar{a}\bar{b}} = u_{C\bar{a}} - u_{C\bar{b}}$ reaches zero (cf. **Fig. 3.4**). Therefore the local averages $\langle u_{C\bar{a}}\rangle_{T_s}$ and $\langle u_{C\bar{b}}\rangle_{T_s}$ no longer match the corresponding mains voltages u_a and u_b. This impresses a voltage on the input filter inductors L_f, which leads to a distortion of the input currents i_a and i_b, as shown in **Fig. 3.3**.

In the following a modified circuit topology that reduces the conduction losses in the IVS and decouples the switching operation of the dc-dc converters and the IVS is proposed, which allows to mitigate the input current distortions. For this circuit, an analysis of the current distortion's impact on

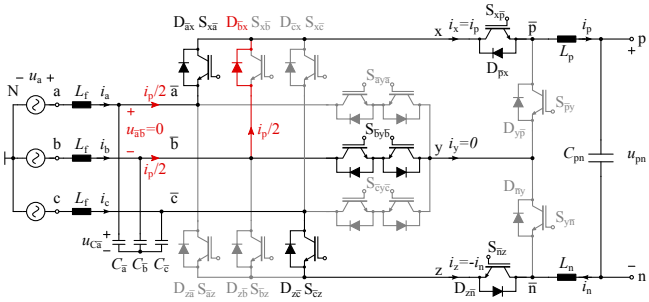

Fig. 3.4: Schematic of the SWISS Rectifier with $S_{x\bar{p}}$ turned on, showing the additional conduction path caused by the diode $D_{\bar{b}x}$ when the voltage $u_{\bar{a}\bar{b}}$, i.e. the difference of the voltages of the filter capacitors $C_{\bar{a}}$ and $C_{\bar{b}}$, reaches zero. This implies $u_{\bar{a}\bar{b}} \geq 0$ as long as $D_{\bar{a}x}/S_{x\bar{a}}$ and $S_{\bar{b}y\bar{b}}$ are turned on, which means that $u_{C\bar{a}}$ and $u_{C\bar{b}}$ cannot intersect (cf. **Fig. 3.3**).

the converter's THD is given in **Section 3.3**. Subsequently, a novel modulation concept, which mitigates the current distortions by temporary pulse width modulation of the IVS switches is introduced in **Section 3.4**. In **Section 3.5** measurement results, taken on a 7.5 kW prototype SWISS Rectifier, are presented, which verify the theoretical considerations.

3.2 DC-side Filter Capacitors

As written above, an implementation of the SWISS Rectifier typically requires additional filter capacitors C_f' in order to shorten the commutation paths of the two dc-dc converters as shown in **Fig. 3.1**. Therefore, nodes x, y and z form a kind of split dc-link that provides the input voltages u_{xy} and u_{yz} for the dc-dc converters. However, as the switches of the IVS are operated at mains frequency only, the voltages u_{xN}, u_{yN} and u_{zN}, are piecewise sinusoidal and hence form a three-phase system (cf. **Fig. 3.2**). This allows to move the input filter capacitors to the dc-side of the IVS as shown in **Fig. 3.5**.

In the following, a star-connection of the filter capacitors (C_x, C_y and C_z) is assumed. However, a line-to-line (delta) connection could be used as well. Note that a total of three capacitors of equal capacitance is required in order to load the ac mains symmetrically, even for a delta-connection, as the voltages at nodes x, y and z are piecewise sinusoidal and form a three-phase system within every 60° mains voltage sector.

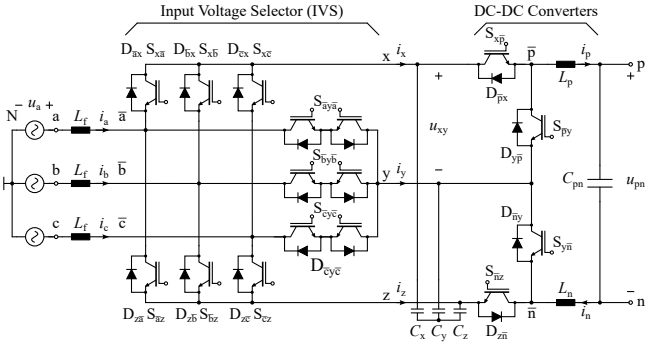

Fig. 3.5: Schematic of the bidirectional SWISS Rectifier with input filter capacitors placed at the dc-side of the IVS. A star-connection of filter capacitor is shown here, however a line-to-line (delta) connection could be used as well. The same input filter damping structure as in the original SWISS Rectifier with ac-side input filter capacitors can be used.

Placing the input filter capacitors on the dc-side of the IVS has several advantages: It shortens the commutation paths of the dc-dc converters which means that no additional capacitors C'_{f} are required. Furthermore, the currents i_{x}, i_{y} and i_{z} flowing through the IVS are continuous in the case of dc-side filter capacitors, as the IVS switches are operated at mains frequency only and hence the filter inductors L_{f} directly impress the IVS currents i_{x}, i_{y} and i_{z} during each mains voltage sector. **Fig. 3.6** shows simulation results for the same operating conditions as in **Fig. 3.2** but with dc-side EMI filter capacitors. It can be seen that i_{x}, i_{y} and i_{z} are continuous, exception in the vicinity of the mains voltage intersections. This is not the case for the original SWISS Rectifier where i_{x}, i_{y} and i_{z} are discontinuous due to the dc-dc converters, which leads to a reduction of conduction losses in the IVS switches. Assuming purely sinusoidal currents $i_{\mathrm{a,b,c}}$ in the ac input filter inductors L_{f} and a constant output inductor current $i_{\mathrm{p}} = i_{\mathrm{n}} = I_{\mathrm{dc}}$, the rms value of the rectifier diode $\mathrm{D}_{\bar{\mathrm{k}}\mathrm{x}}$, $\mathrm{D}_{\mathrm{z}\bar{\mathrm{k}}}$ current can be calculated as

$$I_{\mathrm{D}\bar{\mathrm{k}}\mathrm{x},\mathrm{rms}} = I_{\mathrm{dc}}\, M \sqrt{\frac{\sqrt{3}}{8\,\pi} + \frac{1}{6}} \tag{3.1}$$

where I_{dc} is the dc output current and $M \in [0, 1]$ is the rectifiers modulation index. For a conventional SWISS Rectifier with ac-side filter capacitors (cf.

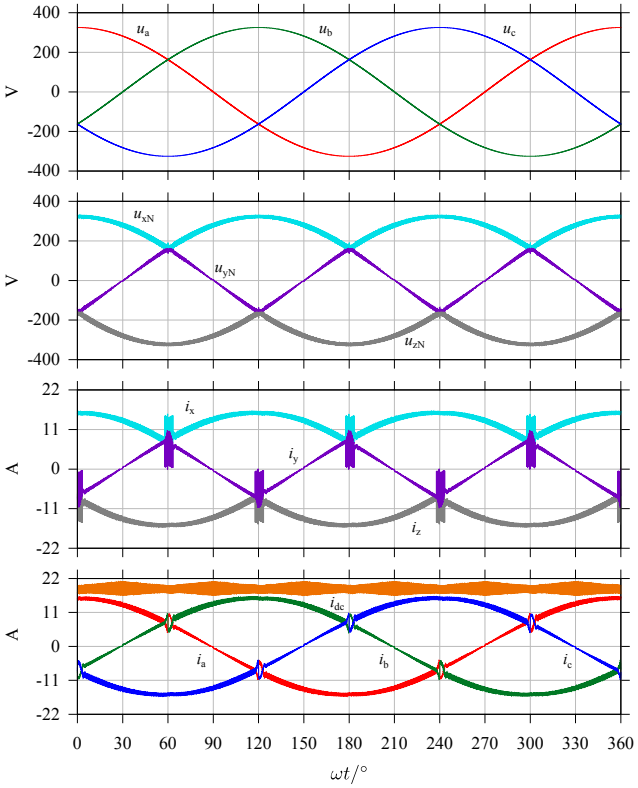

Fig. 3.6: Simulation results for a SWISS Rectifier with input filter capacitors $C_{x,y,z}$ placed on the dc-side of the IVS as shown in **Fig. 3.5** for the same operating conditions as in **Fig. 3.2**. Similar input current distortions as in **Fig. 3.2** result, however the IVS currents i_x, i_y and i_z are now continuous except in the vicinity of the mains voltage intersections.

Fig. 3.1) the corresponding value is given by:

$$I_{\bar{\mathrm{Dkx}},\mathrm{rms},\mathrm{conv}} = I_{\mathrm{dc}} \sqrt{\frac{\sqrt{3}\, M}{2\, \pi}} \tag{3.2}$$

[37]. Note that the diodes' average current does not change. Assuming a typical forward voltage drop of $U_f \approx 0.8\,\mathrm{V}$ and series resistance of $r_f \approx 33\,\mathrm{m\Omega}$ for the IVS diodes, $I_{dc} = 20\,\mathrm{A}$ and a modulation index of $M = 0.8$, the

conduction losses of the diodes are reduced by 14 %. If MOSFETs are used as synchronous rectifiers instead of diodes in the IVS the reduction would be approximately 31 % for $M = 0.8$. Similarly the rms current in the injection switches and diodes $S_{\bar{k}y\bar{k}}$ can be calculated as:

$$I_{S\bar{k}y\bar{k},\mathrm{rms}} = I_{D\bar{k}y\bar{k},\mathrm{rms}} = I_{\mathrm{dc}}\, M \sqrt{\frac{1}{12} - \frac{\sqrt{3}}{8\,\pi}} \quad , \tag{3.3}$$

and the corresponding value with ac-side EMI filter capacitors is given by:

$$I_{S\bar{k}y\bar{k},\mathrm{rms,conv}} = I_{\mathrm{dc}} \sqrt{M\,\frac{2-\sqrt{3}}{2\,\pi}} \quad . \tag{3.4}$$

Assuming the same parameters as above, the conduction losses of the injection circuit diodes and IGBTs reduce by 33 % and by 73 % if MOSFETs are used. The same values result for dc-to-ac power transfer in bidirectional SWISS Rectifiers.

Additionally, the dc-side capacitors decouple the switching operations of the IVS and the dc-dc converters. In the original bidirectional SWISS Rectifier, special commutation sequences are required in the IVS in order not to interrupt the currents i_p and i_n in the output inductors [104]. This is not the case with dc-side input filter capacitors, as C_x, C_y and C_z provide a conduction path for the IVS and the dc-dc converter currents at all valid switching states.

This implies that the SWISS Rectifier with dc-side filter capacitors can, to some extent, be considered as a system consisting of two individual converters: an IVS stage performing an ac-to-dc voltage conversion and a dc-dc converter stage that ensures sinusoidal input currents and provides dc output voltage control. Therefore, the IVS and the dc-dc converters can be designed, optimized and operated almost independently of each other. For example, several individual dc-dc converter modules could be fed from a single, high-power IVS which provides the voltages on the x, y, z busses. In this case, the IVS and the dc-dc converters could even be spatially separated, for example accommodated in different cabinets.

Note that moving the filter capacitors to the dc-side of the IVS implies that the reactive power demand of the capacitors causes a phase shift of the IVS currents i_x, i_y and i_z. In nominal operation this phase shift is typically small, for the rectifier specified in **Tbl. 3.1** a phase shift of 1.7° results. However, the phase shift angle increases with reducing load as the active power drawn

from the mains decreases. This can cause non-sinusoidal input currents in unidirectional SWISS Rectifiers at very light load ($< 5.1\,\%$ for the system specified in **Tbl. 3.1**) as i_x and i_z cannot reverse due to the diode rectifier $D_{\bar{a}x}$, $D_{\bar{b}x}$, $D_{\bar{c}x}$ and $D_{z\bar{a}}$, $D_{z\bar{b}}$, $D_{z\bar{c}}$ and hence the IVS currents cannot lead the mains voltage by more than 30° [123]. Similar current distortions exist in single-phase boost-type PFC rectifiers if a filter capacitor is placed on the dc-side of the input rectifier [124].

3.3 Input Current Distortions

As described **Section 3.1**, the conventional SWISS Rectifier exhibits ac input current distortions at the intersections of the mains' phase voltages. This is due to the switching frequency voltage ripples at the input filter capacitors which cause additional diodes in the IVS to conduct as shown in **Fig. 3.4**. Two modified modulation strategies, reducing the distortions for the conventional SWISS Rectifier with ac-side filter capacitors are described in [120]. The same current distortions result for the modified SWISS Rectifier with dc-side input filter capacitors C_x, C_y, C_z shown in **Fig. 3.5**. In this case the voltage ripples across C_x, C_y and C_z cause diodes of turned-off dc-dc converter switches to conduct as shown in **Fig. 3.7**. This results in the same mains current distortions as with ac-side filter capacitors, as can be seen from the simulation results shown in **Fig. 3.8**. An analysis of these current distortions, including the impact on the ac currents' THD, is given in the following. Based on this analysis a temporary pulse width modulation of the IVS switches is proposed in **Section 3.4** which allows a mitigation of the distortions if dc-side filter capacitors are used.

In order to derive an analytical model of the current distortions the switching frequency ripple components of the currents in L_f and $L_{p,n}$ are neglected and $i_p = i_n = I_{dc}$ is assumed. The mains voltages and currents are considered to be purely sinusoidal. Due to the phase symmetry it is sufficient to consider only the first intersection of u_a and u_b, i.e. $\omega t \approx \pi/3$. The filter capacitors are assumed to have equal capacitance, i.e. $C_x = C_y = C_z = C_f$.

As explained above, the switching frequency ripple across the input filter capacitors is the root cause of the current distortions. Therefore, an analytical expression for its peak-to-peak value $\hat{u}_{xy}$ is required. Assuming in phase carriers for $S_{x\bar{p}}$ and $S_{\bar{n}z}$, it can be seen from **Fig. 3.8** that u_{xy} assumes the peak value at the switching transitions of $S_{x\bar{p}}$. The peak-to-peak ripple can

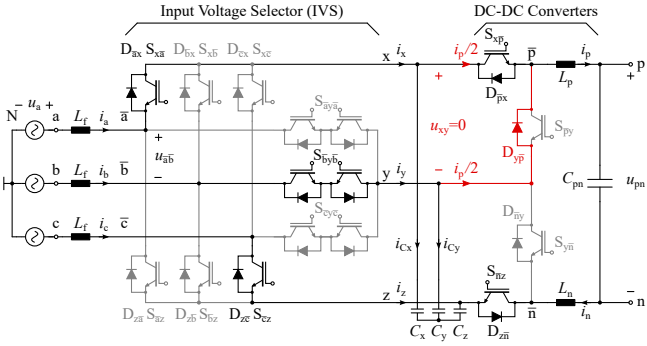

Fig. 3.7: Schematic of the SWISS Rectifier with $S_{x\bar{p}}$ turned on, showing the additional conduction path caused by the diode $D_{y\bar{p}}$ when the voltage u_{xy} across the filter capacitors C_x and C_y reaches zero. This implies that $u_{xy} \geq 0$ (cf. **Fig. 3.8**).

therefore be calculated as:

$$\begin{aligned}\hat{u}_{xy} &= \frac{1}{C_f}\int_0^{(1-d_p)/f_s} i_{Cx} - i_{Cy}\, d\tau \\ &= \frac{1}{f_s\, C_f}\left[\left(i_x - i_y\right)\left(1-d_p\right) + I_{dc}\left(d_n - d_p\right)\right] \ , \end{aligned} \tag{3.5}$$

where d_p is the duty cycle of $S_{x\bar{p}}$ and d_n is the duty cycle of $S_{\bar{n}z}$. Assuming that the SWISS Rectifier is operated such that the ac grid currents are in phase with the grid voltages and that the current distortion is short compared to the mains voltage period, the following simplifications hold:

$$d_p = M\cos(\omega\, t) \approx \frac{M}{2} \qquad \omega t \approx \frac{\pi}{3} \tag{3.6}$$

$$d_n = M\cos(\omega\, t - \frac{\pi}{3}) \approx M \ . \tag{3.7}$$

Note that M is the modulation index of the SWISS Rectifier. Neglecting any voltage drops across the switches, diodes and filter inductors, the steady state voltage transfer ratio between ac and dc-side is defined as

$$U_{pn} \approx U_{\bar{p}\bar{n}} = M\,\hat{U}_1\,\frac{3}{2} \qquad M = \frac{U_{pn}}{\frac{3}{2}\,\hat{U}_1} \in [0,1] \ , \tag{3.8}$$

where $\hat{U}_1$ is the amplitude of the ac mains line-to-neutral voltage [37]. By neglecting the mains frequency component of the filter capacitor current

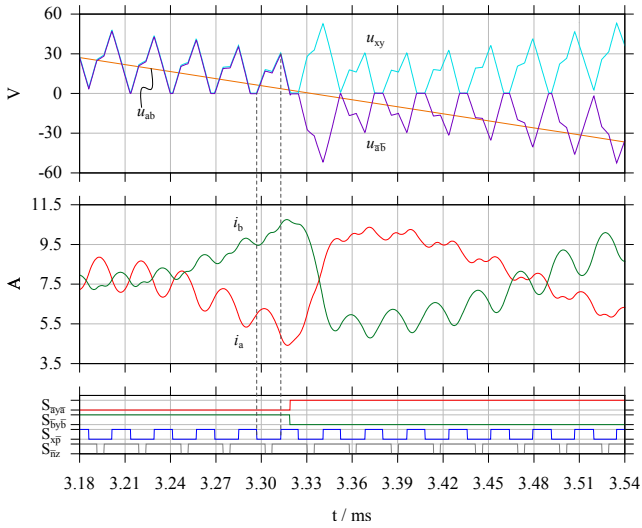

Fig. 3.8: Detailed simulation results for the first sector boundary (at $\omega t \approx \pi/3$) with input filter capacitors on the dc-side of the IVS (C_x, C_y and C_z, cf. **Fig. 3.7**). It can be seen that u_{xy} cannot become negative because of $D_{y\bar{p}}$. This implies that the average over one switching period of the voltage $u_{\bar{a}\bar{b}}$ at the input of the IVS differs significantly from the corresponding mains voltage u_{ab}. Accordingly, a distortion of the input currents i_a and i_b occurs.

$i_{Cx,y,z}$, further simplifications can be found:

$$i_x = I_{dc}\, d_p \approx I_{dc}\frac{M}{2} \tag{3.9}$$

$$i_z = -I_{dc}\, d_n \approx -I_{dc}\, M \tag{3.10}$$

$$i_y = -(i_x + i_z) \tag{3.11}$$

By combining (3.5) to (3.11) $\hat{u}_{xy}$ can approximated as

$$\hat{u}_{xy} = \frac{I_{dc}\, M}{2\, C_f\, f_s}\,. \tag{3.12}$$

When the line-to-line voltage u_{ab} becomes smaller than half the voltage ripple $\hat{u}_{xy}$ calculated in (3.5) or (3.12), the current distortion starts. Hence, the time span $t_d/2$ from the beginning of the distortion until the zero crossing of

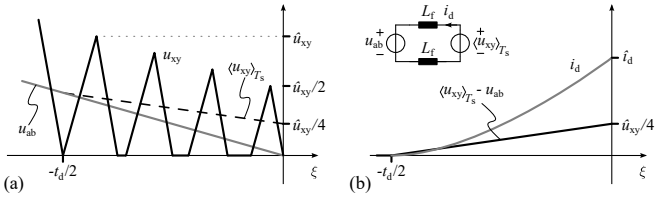

Fig. 3.9: Drawing (not to scale) of the assumptions made to derive (3.16). At the beginning of the distortion ($\xi = -t_d/2$) the local average $\langle u_{xy}\rangle_{T_s}$ of u_{xy} equals the mains voltage u_{ab}. The difference of $\langle u_{xy}\rangle_{T_s}$ and u_{ab} increases linearly until $\xi = 0$ where it reaches a peak value of $\hat{u}_{xy}/4$. This voltage, $\langle u_{xy}\rangle_{T_s} - u_{ab}$, drives the distortion current i_d in the filter inductors of the corresponding phases.

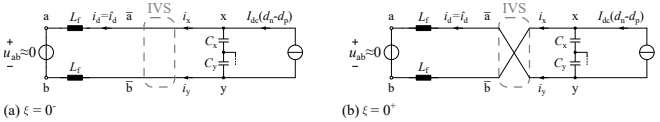

Fig. 3.10: Simplified schematics of the two phases with intersecting voltages: **(a)** before the IVS changes polarity at $\xi = 0$ and **(b)** immediately afterwards. The distortion current i_d flowing in the filter inductors L_f leads to a rapid change of u_{xy} after the IVS commutation as i_x and i_y change polarity.

the line-to-line voltage u_{ab} can be derived:

$$u_{ab}\left(\frac{\pi}{3} - \frac{\omega\, t_d}{2}\right) = \sqrt{6}\, U_1 \sin\left(\frac{\omega\, t_d}{2}\right) = \frac{\hat{u}_{xy}}{2}\,, \tag{3.13}$$

$$\frac{t_d}{2} = \frac{1}{\omega}\arcsin\left(\frac{I_{dc}\, M}{4\sqrt{6}\, U_1\, C_f\, f_s}\right) \approx \frac{1}{\omega}\frac{I_{dc}\, M}{4\sqrt{6}\, U_1\, C_f\, f_s}\,. \tag{3.14}$$

At the beginning of the current distortion $\langle u_{xy}\rangle_{T_s}$ (the average of u_{xy}

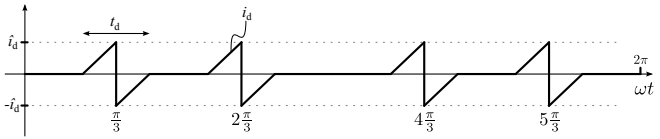

Fig. 3.11: Simplified distortion current within one mains period assumed for the rms value calculation used to derive (3.17).

over one switching period T_s) is equal to the grid voltage u_{ab}. As can be seen from **Fig. 3.8**, in the center of the distortion (at $u_{ab} = 0$), the ripple of u_{xy} is approximately half the value compared to the point in time where the current distortion starts. Therefore the local average $\langle u_{xy} \rangle_{T_s}$ of u_{xy} is approximated by a linear function as shown in **Fig. 3.9 (a)**:

$$\langle u_{xy} \rangle_{T_s}(\xi) = \frac{\hat{u}_{xy}}{4} \left[1 - \frac{\xi}{t_d/2} \right] \quad \text{for } \xi \in [-t_d/2, 0] \ . \tag{3.15}$$

During the distortion, the voltage difference between $\langle u_{xy} \rangle_{T_s}$ and u_{ab} is impressed on the input filter inductors which causes a circulating distortion current i_d.

This is shown in **Fig. 3.9(b)** and it enables an estimation of the distortion current's amplitude $\hat{i}_d$ using (3.13), (3.15) and $\sin(\omega t) \approx \omega t$:

$$\begin{aligned} \hat{i}_d &= \frac{1}{2\,L_f} \int_{-t_d/2}^{0} u_{xy} \left(\frac{\pi}{3} + \xi\,\omega \right) - u_{ab} \left(\frac{\pi}{3} + \xi\,\omega \right) d\xi \ , \\ &\approx \frac{1}{2\,L_f} \int_{-t_d/2}^{0} \frac{\hat{u}_{xy}}{4} + \frac{\hat{u}_{xy}}{4} \frac{\xi}{t_d/2}\, d\xi = \frac{\hat{u}_{xy}\, t_d}{32\, L_f} \ . \end{aligned} \tag{3.16}$$

So far, only the first half of the distortion, until u_{ab} reaches zero (at $\xi = 0$) was considered. Once u_{ab} changes its sign, the IVS commutates in order to reverse the polarity of $u_{\bar{a}\bar{b}}$. This is shown in the simplified schematics in **Fig. 3.10**. Note, that the polarity reversal of the IVS changes the sign of the IVS' dc-side currents i_x and i_y. This leads to a considerably higher peak value of u_{xy} during the first switching period after the polarity reversal. Therefore ,a higher voltage is applied to the filter inductors L_f in this cycle, which leads to a fast polarity reversal of the distortion current i_d. This can also be seen in the simulation results shown in **Fig. 3.8**. The current distortion is therefore approximately symmetric in time around the zero crossing of the line-to-line voltage u_{ab} (at $\omega t = \pi/3$).

For further analysis, the converter's mains input currents $i_{a,b,c}$ are approximated as sum of a fundamental component $i_{a,b,c(1)}$ and a distortion current i_d. Each mains line is distorted four times per grid voltage period. By modeling each distortion as one triangular wave with a period of t_d and amplitude $\hat{i}_d$ (cf. **Fig. 3.11**), the rms value I_d of i_d can be calculated as

$$I_d = \frac{\hat{i}_d}{\sqrt{3}} \sqrt{4\, t_d\, f} \ . \tag{3.17}$$

In order to determine the impact of (3.17) on the converter's THD, the following normalization is applied:

$$C_\mathrm{f} = \frac{Q_\mathrm{f}}{3\,U_1^2\,\omega} \quad Q_\mathrm{f} = P\tan(\phi_1)\,, \tag{3.18}$$

$$L_\mathrm{f} = L_\mathrm{f,p.u.}\frac{R_1}{\omega} = L_\mathrm{f,p.u.}\frac{3\,U_1^2}{\omega\,P} \quad R_1 = \frac{3\,U_1^2}{P}\,, \tag{3.19}$$

$$I_\mathrm{dc}\,M = \hat{I}_\mathrm{a,b,c(1)} = \frac{2\,P}{3\,\hat{U}_1}\,. \tag{3.20}$$

Note that ϕ_1 represents the phase shift of the input current's fundamental that results from the reactive power consumption of the input filter capacitors. The reactive power created by the filter inductors is neglected as it is typically much smaller than the Q_f.

By combining (3.17) with (3.12)-(3.16) and applying the normalizations (3.18)-(3.20) the normalized RMS value of the current distortions can be expressed as a function of general system parameters,

$$\frac{I_\mathrm{d}}{I_\mathrm{a,b,c(1)}} = \frac{\pi^2}{16\cdot 3^{5/4}}\frac{1}{L_\mathrm{f,p.u.}}\left(\frac{f}{f_\mathrm{s}}\frac{1}{\tan(\phi_1)}\right)^{5/2}\,, \tag{3.21}$$

where $I_{a,b,c(1)}$ is the RMS value of the ac-side input currents' fundamental component at nominal power. This allows an estimation of the current distortions' impact on the rectifier's input current THD. It can be seen that increasing the switching frequency or the input filter capacitors (increasing ϕ_1) reduces the magnitude of the current distortions with a power of 2.5, while it is inversely proportional to the input filter inductance.

Tbl. 3.2 shows the numerical results for the equations derived above and compares the values to results obtained from a simulation of the system specified in **Tbl. 3.1**. The calculated values are typically within 10 % of the simulation results. Furthermore, it can be seen that the low-frequency THD[1] (not considering switching frequency components) of the rectifier's input currents is 4.2 %.

3.4 Mitigating Distortions by PWM of the IVS

As described in the previous section, the ac input current distortions can have a significant contribution to the input current THD of a SWISS Rectifier. For

[1]Spectral components up to 10 kHz, i.e. up to the 200$^{\text{th}}$ harmonic of the mains frequency, are considered.

Tbl. 3.2: Comparison Between Calculation and Simulation

	Calculated	Simulated	Error
$\hat{u}_{xy}$	48.6 V	43.4 V	12 %
t_d	275 µs	279 µs	−1.4 %
$\hat{i}_d$	3.48 A	3.34 A	4.2 %
$I_d/I_{a,b,c(1)}$ (THD)	4.31 %	4.23 %	1.9 %

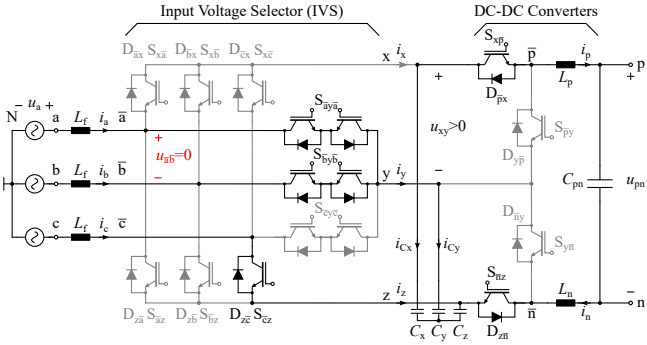

Fig. 3.12: SWISS Rectifier with dc-side input filter capacitors and ac-to-dc power transfer during the first intersection of u_a and u_b. By turning $S_{x\bar{a}}$ off and turning on $S_{\bar{a}y\bar{a}}$ the IVS' output voltage $u_{\bar{a}\bar{b}}$ is forced to zero.

the system specified in **Tbl. 3.1** current distortions with a normalized RMS value of 4.2 % result. However, the distortions can be prevented by properly modulating the switches in the IVS as will be shown in the following.

The root cause of the current distortions is the switching frequency voltage ripple across the input filter capacitors and the fact that the voltages u_{xy} and u_{yz} cannot be negative (cf. **Fig. 3.8**). However, if the input filter capacitors are placed on the dc-side of the IVS, the IVS can be used to temporarily disconnect the filter capacitors $C_{x,y,z}$ from the filter inductors L_f by simultaneously turning on two of the three injection switches, e.g. $S_{\bar{a}y\bar{a}}$ and $S_{\bar{b}y\bar{b}}$. This short-circuits the corresponding input nodes $\bar{a}$ and $\bar{b}$ and results in $u_{\bar{a}\bar{b}} = 0$, as shown in **Fig. 3.12**. Therefore, it is possible to mitigate the current distortions by toggling the second injection switch such that the average over one switching period of $u_{\bar{a}\bar{b}}$ equals the mains voltage u_{ab}.

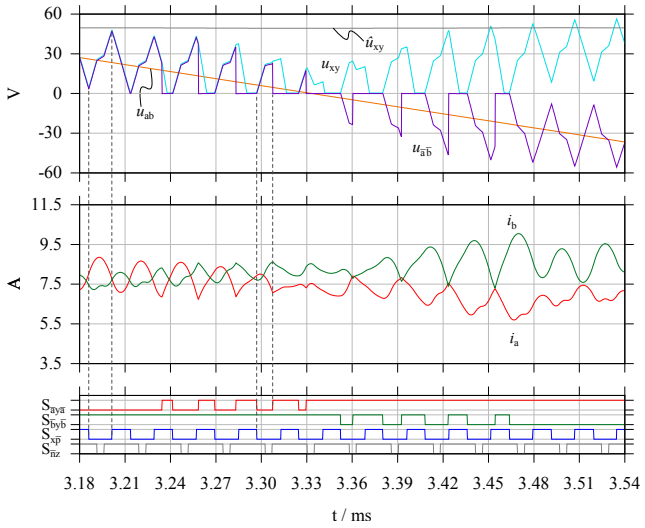

Fig. 3.13: Simulation results, showing pulse width modulated injection switches $S_{\bar{a}y\bar{a}}$ and $S_{\bar{b}y\bar{b}}$ during the first intersection of u_a and u_b which reduces the current distortions. Furthermore, the calculated peak-to-peak ripple of u_{xy} is shown as $\hat{u}_{xy}$.

3.4.1 AC-to-DC Power Transfer with In Phase Carriers

The following considerations focus on the intersection of u_a and u_b at $\omega t \approx \pi/3$ with ac-to-dc power transfer and in phase carriers of the two buck converters. It can be seen from **Fig. 3.13** that u_{xy} increases while $S_{x\bar{p}}$ is not conducting, which implies that u_{xy} is minimal when $S_{x\bar{p}}$ is turned off. Therefore, the turn-off of $S_{x\bar{p}}$ is selected as origin for an auxiliary time axis τ.

Fig. 3.14 shows a diagram of the filter capacitor voltage u_{xy} during the first half of the first intersection ($\omega t \leq \pi/3, u_a > u_b$). The additional injection switch $S_{\bar{a}y\bar{a}}$ is turned on at time τ' and is turned off together with $S_{x\bar{p}}$ in order to allow u_{xy} to charge. In order to simplify the analytical calculations u'_{xy} is

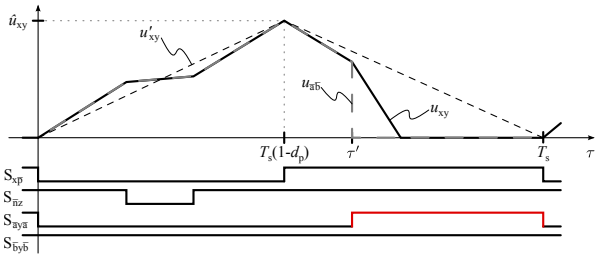

Fig. 3.14: Time behavior of the filter capacitor voltage ripple u_{xy} within one switching period T_s for ac-to-dc power transfer. The signal u'_{xy} is used as approximation for u_{xy} in order to simplify the algebraic calculations.

used as an approximation for u_{xy}:

$$u'_{xy}(\tau) = \begin{cases} \hat{u}_{xy} \, \frac{\tau}{(1-d_p)\,T_s} & \text{if } \tau \le (1-d_p)\,T_s \\ \hat{u}_{xy} \, \frac{1}{d_p} \left(1 - \frac{\tau}{T_s}\right) & \text{if } \tau > (1-d_p)\,T_s \,, \end{cases} \tag{3.22}$$

$$u_{\bar{a}\bar{b}}(\tau) = \begin{cases} u_{xy}(\tau) \approx u'_{xy}(\tau) & \text{if } \tau \le \tau' \\ 0 & \text{if } \tau > \tau' \,. \end{cases} \tag{3.23}$$

Note that either (3.5) or (3.12) can be used to estimate the peak value $\hat{u}_{xy}$. The average $\left\langle u_{\bar{a}\bar{b}}(\tau)\right\rangle_{T_s}$ over one switching frequency period T_s of the IVS output voltage $u_{\bar{a}\bar{b}}$ can be found by integration:

$$\left\langle u_{\bar{a}\bar{b}}(\tau')\right\rangle_{T_s} = \frac{1}{T_s}\int_0^{\tau'} u_{xy}(\tau)\,d\tau \approx \frac{1}{T_s}\int_0^{\tau'} u'_{xy}(\tau)\,d\tau \,. \tag{3.24}$$

In order to prevent the current distortions τ' has to be selected such that $\left\langle u_{\bar{a}\bar{b}}(\tau')\right\rangle_{T_s}$ equals the corresponding ac mains voltage u_{ab} which is used as reference value u_{ref}:

$$u_{ref} = u_a - u_b = u_{ab} \,. \tag{3.25}$$

By solving (3.24) an algebraic expression for τ' can be found:

$$u_{ref} = \left\langle u_{\bar{a}\bar{b}}(\tau')\right\rangle_{T_s} \quad \Rightarrow$$
$$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{xy}}\left(1-d_p\right)} & \text{if } u_{ref} \le \hat{u}_{xy}\,\frac{1-d_p}{2} \\ 1 - \sqrt{d_p - 2\,d_p\,\frac{u_{ref}}{\hat{u}_{xy}}} & \text{if } u_{ref} > \hat{u}_{xy}\,\frac{1-d_p}{2} \,. \end{cases} \tag{3.26}$$

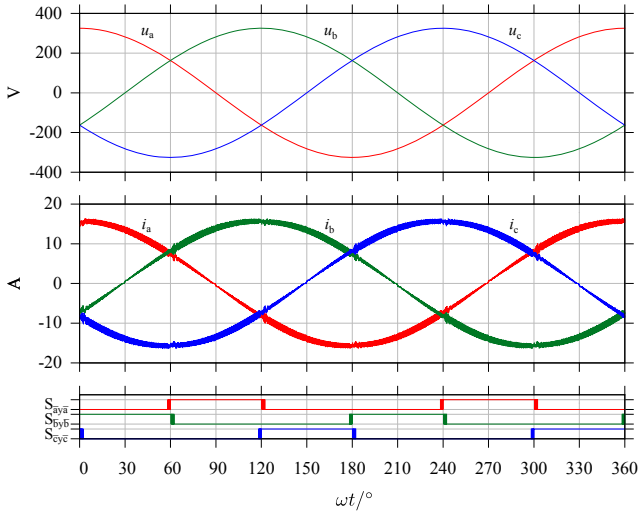

Fig. 3.15: Simulation results for the SWISS Rectifier specified in **Tbl. 3.1** using the proposed modulation technique for the IVS switches. Compared with the results in **Fig. 3.2**, the current distortions are significantly reduced, i.e. the low-frequency (< 10 kHz) THD of $i_{a,b,c}$ reduces from 4.2 % to 0.8 %.

This implies that the current distortions can be mitigated by measuring the mains voltages and evaluating equations (3.5), (3.25) and (3.26) every switching frequency cycle. The additional injection switch $S_{\bar{a}y\bar{a}}$ is then turned on at time τ' after the turn-off of $S_{x\bar{p}}$.

All considerations and calculations given above hold only for the first half of the first current distortion, i.e. for $\omega t < \pi/3$. In the second half ($\omega t > \pi/3$) the mains voltage u_{ab} becomes negative which implies that the output voltage of the IVS has to be negative as well, while the filter capacitor voltage u_{xy} remains positive. This is achieved by modulating $S_{\bar{b}y\bar{b}}$ instead of $S_{\bar{a}y\bar{a}}$, as can be seen in **Fig. 3.13**. By replacing the mains voltages u_a and u_b and the injection switches with the corresponding values, this can be generalized for the other two positive mains voltage intersections ($\omega t \approx 180°, 300°$). Furthermore, the concept can be expanded to the negative side dc-dc converter ($S_{\bar{n}z}$, d_n, u_{yz}) to mitigate the current distortions at the intersections of negative mains line voltages ($\omega t \approx 0°, 120°, 240°$). The resulting formulas are summarized in **Tbl. 3.3**. Simulation results for ac-to-dc operation of the SWISS Rectifier with

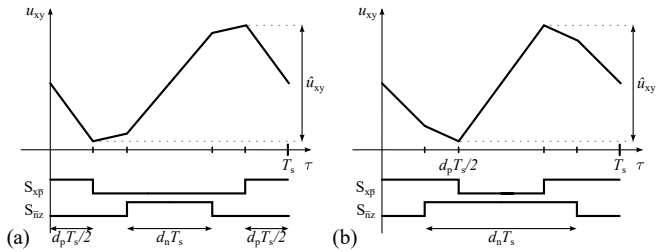

Fig. 3.16: Diagram of the filter capacitor voltage (u_{xy}) ripple for ac-to-dc power transfer with interleaved carriers. In **(a)** $d_p + d_n < 1$ holds, which implies that an interval were both switches, $S_{x\bar{p}}$ and $S_{\bar{n}z}$, are off exists. This is not the case in **(b)** where $d_p + d_n > 1$ holds and therefore $S_{\bar{n}z}$ is always on while $S_{x\bar{p}}$ is off.

the compensation enabled for all intersections are shown in **Fig. 3.15**.

3.4.2 Interleaved Carriers

For the derivation of the formulas in **Section 3.3** an operation of the SWISS Rectifier's dc-dc converters with in phase carriers is assumed. As described in [37], this leads to minimal injection current (i_y) ripple. However, the dc-dc converters could also be controlled with interleaved carriers, i.e. using two independent carriers with a phase shift of 180°. This minimizes the ripple in the dc output current $I_{dc} = i_p = i_n$, but increases the injection current's ripple (i_y). Note that an increase in injection current ripple implies an increase in the filter capacitor voltage ripple, i.e. of $\hat{u}_{xy}$ and $\hat{u}_{yz}$. Without compensation the current distortions are therefore higher compared to operation with in phase carriers.

If interleaved carriers are used the sequence of conduction states within a switching period is different than for in phase carriers. This implies that different formulas for $\hat{u}_{xy}$ and $\hat{u}_{yz}$ result. In the following the intersection of $u_a > 0$ and $u_b > 0$ at $\omega t \approx \pi/3$ is considered. It can be seen from the SWISS Rectifier's schematic (**Fig. 3.5**) that u_{xy} decreases while $S_{x\bar{p}}$ is on as power is delivered to the dc output. Consequently, u_{xy} increases while $S_{x\bar{p}}$ is off. However, two different sequences of switching states exist, depending on the modulation index of the converter, as shown in **Fig. 3.16**.

When $d_p + d_n < 1$ holds, $S_{\bar{n}z}$ switches while $S_{x\bar{p}}$ is off, resulting in the filter capacitor ripple depicted in **Fig. 3.16 (a)**. In this case $\hat{u}_{xy}$ can be approximated

as

$$\hat{u}_{\mathrm{xy,int,<1}} = \frac{T_\mathrm{s}}{C_\mathrm{f}} \left[\left(i_\mathrm{x} - i_\mathrm{y} \right) \left(1 - d_\mathrm{p} \right) + I_\mathrm{dc} d_\mathrm{n} \right] \ , \tag{3.27}$$

where T_s is the switching period of the dc-dc converters. For a high modulation index where $d_\mathrm{p} + d_\mathrm{n} > 1$ holds, $\mathrm{S_{\bar{n}z}}$ is on while $\mathrm{S_{x\bar{p}}}$ is off. The equation for $\hat{u}_\mathrm{xy}$ than simplifies to

$$\hat{u}_{\mathrm{xy,int,>1}} = \frac{T_\mathrm{s}}{C_\mathrm{f}} \left[\left(i_\mathrm{x} - i_\mathrm{y} + I_\mathrm{dc} \right) \left(1 - d_\mathrm{p} \right) \right] \ . \tag{3.28}$$

Note that equations (3.27) and (3.28) yield the same value $\hat{u}_\mathrm{xy}$ for the boundary case $d_\mathrm{p} + d_\mathrm{n} = 1$. Hence they can be combined into a continuous function:

$$\hat{u}_{\mathrm{xy,int}} = \frac{T_\mathrm{s}}{C_\mathrm{f}} \begin{cases} \left(i_\mathrm{x} - i_\mathrm{y} \right) \left(1 - d_\mathrm{p} \right) + I_\mathrm{dc} d_\mathrm{n} & \text{if } d_\mathrm{p} + d_\mathrm{n} \leq 1 \\ \left(i_\mathrm{x} - i_\mathrm{y} + I_\mathrm{dc} \right) \left(1 - d_\mathrm{p} \right) & \text{if } d_\mathrm{p} + d_\mathrm{n} > 1 \end{cases} . \tag{3.29}$$

An analog derivation can be used to obtain equations for the negative voltage intersections at $\omega t \approx 0°, 120°, 240°$ The resulting equations are summarized in **Tbl. 3.3**.

Note that the filter capacitor voltage u_xy assumes its peak value at the turn-on of $\mathrm{S_{x\bar{p}}}$, as in the case of in phase carriers (cf. **Fig. 3.13** and **Fig. 3.16**). Therefore, the modulation technique described in **Section 3.4.1** can be used to mitigate the current distortions without any further modifications.

3.4.3 DC-to-AC Power Transfer

The previous descriptions focus on ac-to-dc power transfer, however, the current distortions exist for dc-to-ac power transfer ($i_\mathrm{p} = i_\mathrm{n} < 0$) as well. A similar mitigation strategy can be used as will be shown in the following.

As depicted in **Fig. 3.17** the diode $\mathrm{D_{\bar{p}x}}$ starts to conduct for dc-to-ac power transfer once the filter capacitor voltage u_xy reaches zero. Therefore, the local average of u_xy starts to deviate from the mains voltage u_ab once the ripple is larger than $2\,u_\mathrm{ab}$ as explained above for ac-to-dc power transfer. Thus similar mains current distortions result.

In order to temporarily disconnect the mains filter inductors L_f from the filter capacitors $C_\mathrm{x,y,z}$ two rectifier switches, e.g. $\mathrm{S_{x\bar{a}}}$, $\mathrm{S_{x\bar{b}}}$ are turned on simultaneously as shown in **Fig. 3.18**. Simulation results of a SWISS Rectifier using this modulation technique are shown in **Fig. 3.19**. Note that, unlike for ac-to-dc power transfer, it is not possible to modulate the injection switches $\mathrm{S_{\bar{i}y\bar{i}}}$ ($\bar{i} = \bar{a}, \bar{b}, \bar{c}$) because u_xy has to be discharged to zero once the additional

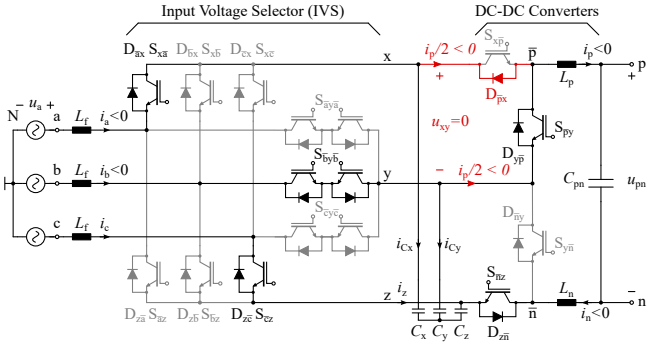

Fig. 3.17: Schematic of the SWISS Rectifier with dc-to-ac power transfer ($i_p < 0$, $i_n < 0$) during the first intersection of u_a and u_b. When the filter capacitor voltage u_{xy} reaches zero the diode $D_{\bar{p}x}$ is forward biased and starts to conduct, thus preventing u_{xy} from reversing polarity. Therefore, similar input current distortions as for ac-to-dc power transfer result (cf. **Fig. 3.7**).

switch is turned on at τ'. It can be shown that this is the case only when the rectifier switches $S_{x\bar{a},\bar{b},\bar{c}}$, $S_{\bar{a},\bar{b},\bar{c}z}$ are modulated.

The equations required to implement the mitigation algorithm for dc-to-ac power transfer are summarized in **Tbl. 3.4**. Note that the switching transition which marks the beginning of the time span τ' is different than for ac-to-dc

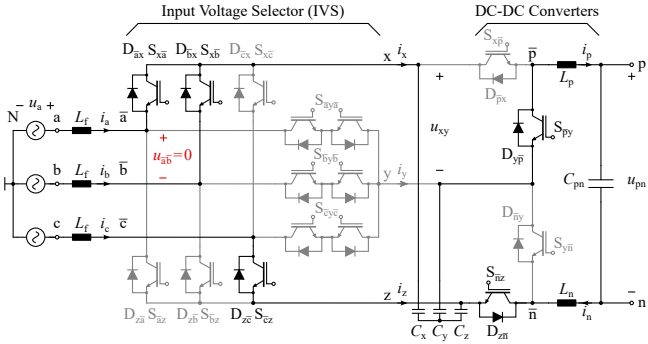

Fig. 3.18: SWISS Rectifier with dc-to-ac power transfer ($i_p < 0$, $i_n < 0$) during the first intersection of u_a and u_b. Two Rectifier switches ($S_{x\bar{a}}$, $S_{x\bar{b}}$) are turned on simultaneously ($S_{\bar{b}y\bar{b}}$ is turned off) in order to achieve $u_{\bar{a}\bar{b}} = 0$.

Tbl. 3.3: Equations Required to Implement the Distortion Mitigation Algorithm for AC-to-DC Power Transfer

Positive Voltage Intersections

Origin of τ': $S_{x\bar{p}}$ $1 \rightarrow 0$

Modulation: $S_{\bar{a}ya\bar{a}}$, $S_{\bar{b}yb\bar{b}}$, $S_{\bar{c}yc\bar{c}}$

$$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{xy}}\left(1-d_p\right)} & \text{if } u_{ref} \leq \hat{u}_{xy}\frac{1-d_p}{2} \\ 1-\sqrt{d_p\left(1-2\frac{u_{ref}}{\hat{u}_{xy}}\right)} & \text{if } u_{ref} > \hat{u}_{xy}\frac{1-d_p}{2} \end{cases}$$

In Phase Carriers:

$$\hat{u}_{xy} = \frac{T_s}{C_f}\left[\left(i_x - i_y\right)\left(1-d_p\right) + I_{dc}\left(d_n - d_p\right)\right]$$

Interleaved Carriers:

$$\hat{u}_{xy} = \frac{T_s}{C_f}\begin{cases} \left(i_x - i_y\right)\left(1-d_p\right) + I_{dc}d_n & \text{if } d_p + d_n \leq 1 \\ \left(i_x - i_y + I_{dc}\right)\left(1-d_p\right) & \text{if } d_p + d_n > 1 \end{cases}$$

Negative Voltage Intersections

Origin of τ': $S_{\bar{n}z}$ $1 \rightarrow 0$

Modulation: $S_{\bar{a}ya\bar{a}}$, $S_{\bar{b}yb\bar{b}}$, $S_{\bar{c}yc\bar{c}}$

$$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{yz}}\left(1-d_n\right)} & \text{if } u_{ref} \leq \hat{u}_{yz}\frac{1-d_n}{2} \\ 1-\sqrt{d_n\left(1-2\frac{u_{ref}}{\hat{u}_{yz}}\right)} & \text{if } u_{ref} > \hat{u}_{yz}\frac{1-d_n}{2} \end{cases}$$

In Phase Carriers:

$$\hat{u}_{yz} = \frac{T_s}{C_f}\left[\left(i_y - i_z\right)\left(1-d_n\right) + I_{dc}\left(d_p - d_n\right)\right]$$

Interleaved Carriers:

$$\hat{u}_{yz} = \frac{T_s}{C_f}\begin{cases} \left(i_y - i_z\right)\left(1-d_n\right) + I_{dc}d_p & \text{if } d_p + d_n \leq 1 \\ \left(i_y - i_z + I_{dc}\right)\left(1-d_n\right) & \text{if } d_p + d_n > 1 \end{cases}$$

power transfer. **Fig. 3.20** shows simulation results for the SWISS Rectifier specified in **Tbl. 3.1** with 7.5 kW dc-to-ac power transfer. It can be seen that the current distortions are significantly reduced.

Tbl. 3.4: Equations Required to Implement the Distortion Mitigation Algorithm for DC-to-AC Power Transfer

Positive Voltage Intersections

Origin of τ': $S_{x\bar{p}}$ $0 \rightarrow 1$

Modulation: $S_{x\bar{a}}$, $S_{x\bar{b}}$, $S_{x\bar{c}}$

$$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{xy}} d_p} & \text{if } u_{ref} \leq \hat{u}_{xy}\frac{d_p}{2} \\ 1 - \sqrt{\left(1-d_p\right)\left(1-2\frac{u_{ref}}{\hat{u}_{xy}}\right)} & \text{if } u_{ref} > \hat{u}_{xy}\frac{d_p}{2} \end{cases}$$

In Phase Carriers:

$\hat{u}_{xy} = \frac{T_s}{C_f} d_p \left(i_x - i_y - I_{dc}\right)$

Interleaved Carriers:

$$\hat{u}_{xy} = \frac{T_s}{C_f} \begin{cases} \left(i_x - i_y - I_{dc}\right) d_p - I_{dc}\left(1-d_n\right) & \text{if } d_p + d_n \leq 1 \\ \left(i_x - i_y - 2I_{dc}\right) d_p & \text{if } d_p + d_n > 1 \end{cases}$$

Negative Voltage Intersections

Origin of τ': $S_{\bar{n}z}$ $0 \rightarrow 1$

Modulation: $S_{\bar{a}z}$, $S_{\bar{b}z}$, $S_{\bar{c}z}$

$$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{yz}} d_n} & \text{if } u_{ref} \leq \hat{u}_{yz}\frac{d_n}{2} \\ 1 - \sqrt{\left(1-d_n\right)\left(1-2\frac{u_{ref}}{\hat{u}_{yz}}\right)} & \text{if } u_{ref} > \hat{u}_{yz}\frac{d_n}{2} \end{cases}$$

In Phase Carriers:

$\hat{u}_{yz} = \frac{T_s}{C_f} d_n \left(i_y - i_z - I_{dc}\right)$

Interleaved Carriers:

$$\hat{u}_{yz} = \frac{T_s}{C_f} \begin{cases} \left(i_y - i_z - 2I_{dc}\right) d_n & \text{if } d_p + d_n \leq 1 \\ \left(i_y - i_z - I_{dc}\right)\left(1-d_n\right) & \text{if } d_p + d_n > 1 \end{cases}$$

3.4.4 Robustness

In the previous analysis sinusoidal mains voltages and currents were assumed. This is typically not the case in the three-phase ac mains where some low-frequency voltage harmonics and asymmetries are usually present. However, the proposed algorithm works even with non-sinusoidal and unsymmetrical

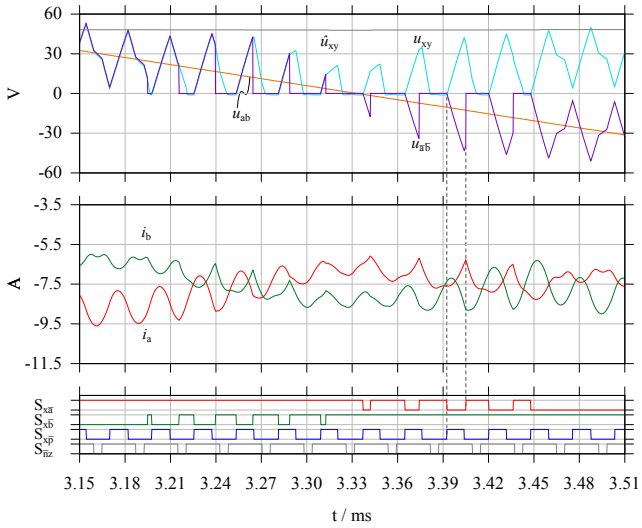

Fig. 3.19: Detailed simulation results for dc-to-ac power transfer and the first intersection of u_a and u_b showing the modulation of a second rectifier switch ($S_{x\bar{a}}$, $S_{x\bar{b}}$). The distortion in i_a and i_b is significantly reduced.

mains voltages. This is possible as the switching frequency ripple of the filter capacitor voltages u_{xy} and u_{yz} can be estimated in real time using the currents i_x, i_y and i_z and the dc-dc converter duty cycles d_p and d_n. Note that no assumption about the shape of these signals is used in the derivation of the formulas listed in **Tbl. 3.3** and **Tbl. 3.4**. The reference signal u_{ref} is derived from the measured mains voltages $u_{a,b,c}$, cf. (3.25). Again, no assumption about the actual signal shape of u_{ref} is required.

Simulation results for a three-phase mains with 5% (with reference to the fundamental) of 5th harmonic positive sequence voltage are shown in **Fig. 3.21**. It can be seen that the converter achieves ac input currents which are proportional to the according line voltages, i.e. ohmic mains behavior, and that the current distortions are significantly reduced. Note that the sector boundaries of the mains voltage are no longer at multiples of 60° due to the non-sinusoidal shape of the mains voltage. However, no change in the algorithm is required in this case, as $\hat{u}_{xy}$ and $\hat{u}_{yz}$ can continuously be estimated using the equations given in **Tbl. 3.3** and **Tbl. 3.4**. When $u_{ref} < \hat{u}_{xy}/2$ or $u_{ref} < \hat{u}_{yz}/2$ is true τ' can be calculated to modulate the corresponding IVS

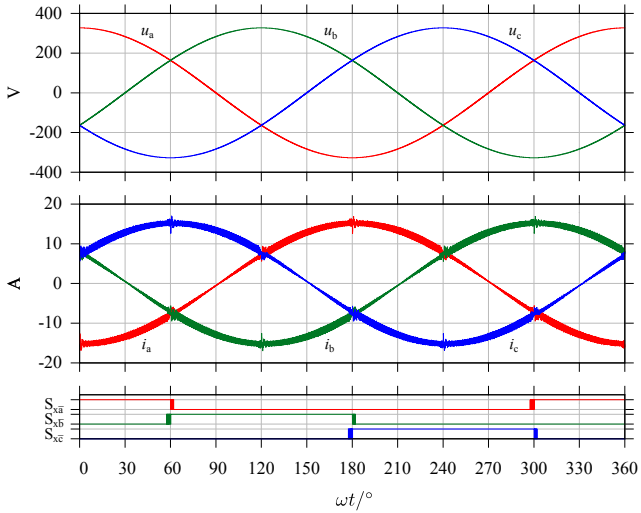

Fig. 3.20: Simulation results for the SWISS Rectifier specified in **Tbl. 3.1** with dc-to-ac power transfer and in phase carriers. The proposed algorithm is used to mitigate the current distortions.

switches which will mitigate the current distortion.

3.5 Implementation and Measurement Results

In order to demonstrate the practicability of the algorithm described above, it was implemented on a bidirectional 7.5 kW prototype SWISS Rectifier. The values of all major components used in the system are given in **Tbl. 3.1** and match the values used for the presented simulation results.

3.5.1 Implementation

A Texas Instruments TMS320F28335 DSP, which features a hardware floating point unit, and a Lattice XP2 FPGA are used to implement the converter's control and distortion mitigation algorithms. A flowchart illustrating the main calculation steps is shown in **Fig. 3.22**. Using the DSP's analog-to-digital converters the mains voltages $u_{a,b,c}$, the dc output current i_{dc} and the output voltage u_{pn} are measured at every switching frequency period. Based on the

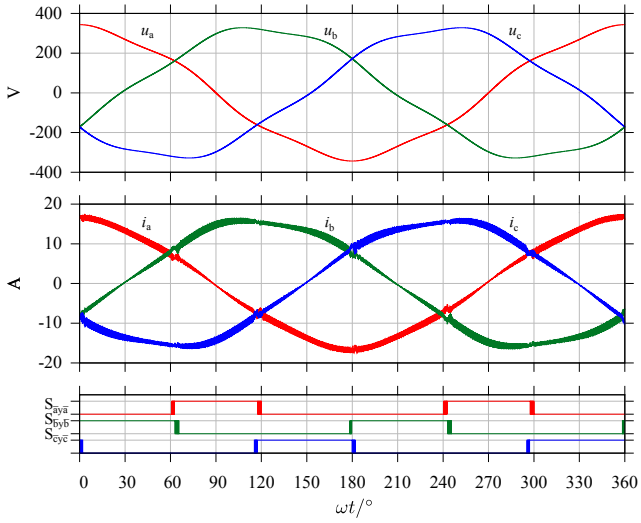

Fig. 3.21: Simulation results for the SWISS Rectifier specified in **Tbl. 3.1** with ac-to-dc power transfer, in phase carriers and 5% of 5$^{\text{th}}$ harmonic (positive sequence) present in the mains voltage. As the measured mains voltages are used in the calculation of τ' the proposed distortion mitigation algorithm works without modifications despite the non-sinusoidal mains voltages.

these measurements a cascaded controller for u_{pn} and i_{dc} is implemented in the DSP, providing ohmic mains behavior of the rectifier at unsymmetrical and distorted mains which yields the duty cycle signals d_{p} and d_{n} [123].

Using the measured dc current i_{dc} and the duty cycles d_{p} and d_{n} the input currents i_{x}, i_{y} and i_{z} and the peak-to-peak filter capacitor voltage ripple $\hat{u}_{\text{xy}}$ (or $\hat{u}_{\text{yz}}$ depending on the current mains voltage sector) are calculated at every switching frequency period. The result is compared to the reference voltage u_{ref} to detect the beginning and end of the voltage intersection period. During this period the appropriate equations according to the power flow direction, mains voltage sector and PWM carrier alignment are evaluated in order to calculate the switching time τ' of the IVS switches as explained above. The necessary equations are summarized in **Tbl. 3.3** and **Tbl. 3.4**.

In total, up to four additions or subtractions and three multiplications have to be evaluated at every controller execution to calculate $\hat{u}_{\text{xy}}$ or $\hat{u}_{\text{yz}}$. During an intersection up to three additional additions or subtractions, two multiplications, one division and one square root have to be evaluated. This

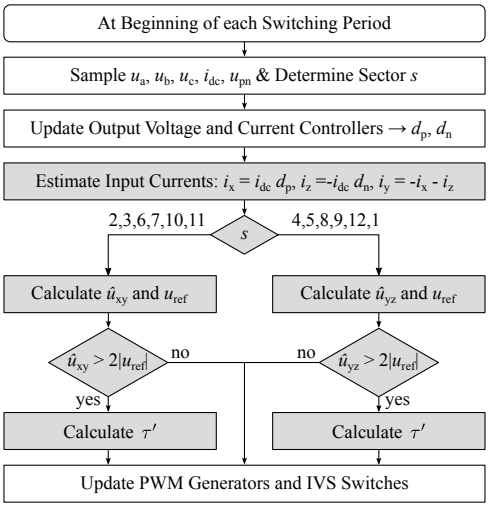

Fig. 3.22: Flowchart of the system's control algorithm, the proposed extensions are highlighted in gray. All calculations are based on the measured ac mains voltages u_a, u_b, u_c and the measured inductor current i_{dc} and output voltage u_{pn}.

is comparable to the computational effort of updating a phase-locked-loop, which is typically used to estimate mains voltage phase angles in converters connected to the three-phase mains and requires the calculation of sine or cosine functions.

3.5.2 AC-to-DC Power Transfer

Fig. 3.23 shows measurements taken on the hardware prototype operating with ac-to-dc power transfer and symmetrical sinusoidal three-phase mains voltages. The mitigation algorithm is active during the mains voltage intersections at $\omega t \approx 60°$, 120° and 180°. At $\omega t \approx 240°$ and 300° it is disabled in order to demonstrate the effect and magnitude of the current distortions in the mains currents i_a, i_b and i_c. It can be seen that the amplitude of the current distortions is reduced below the switching frequency ripple of the input current. An input current THD of 1.1 % is measured for phase a and 1.3 % for phases b and c using a *Yokogawa WT-3000* power analyzer if the mitigation algorithm is enabled for all mains voltage intersections.

Detailed results for the first intersection of u_a and u_b ($\omega t \approx 60°$) at nominal

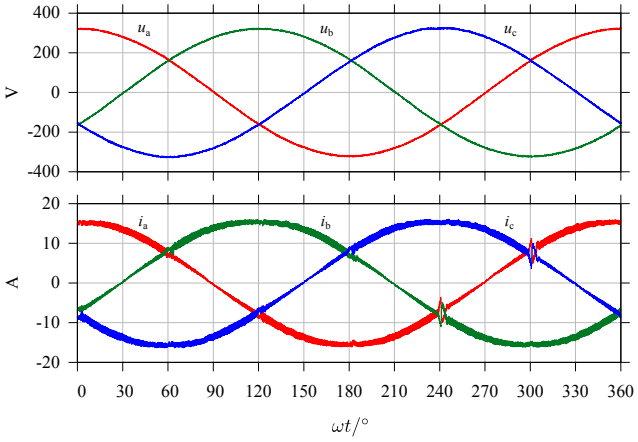

Fig. 3.23: Measurement results for the SWISS Rectifier prototype operated with $I_{dc} = 18.7$ A and $U_1 = 230$ V, the mitigation algorithm is disabled for the mains voltage intersections at $\omega t \approx 240°$ and $\omega t \approx 300°$ for illustrative purposes. Note that u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created using postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

operating conditions are shown in **Fig. 3.24**. Note that the average of the IVS voltage $u_{\bar{a}\bar{b}}$ matches the corresponding mains voltage u_{ab} even tough the filter capacitor voltage u_{xy} has a positive average at all times. Furthermore the measured input filter capacitor voltage u_{xy} and the peak-to-peak value estimated by the DSP are shown in **Fig. 3.25**. It can be seen that the estimated peak-to-peak capacitor voltage ripple $\hat{u}_{xy}$ matches the measured filter capacitor voltage u_{xy} at the beginning of the current distortion, cf. **Fig. 3.13**. Furthermore, the calculated turn-on time τ' for the additional injection switch ($S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$) is shown.

In the derivation of the mitigation algorithm the reactive power created by the filter capacitors was neglected, which might not be valid in light load conditions. Measurement results taken at nominal ac input and dc output voltage but with a reduced load current of $i_{dc} \approx 6$ A are shown in **Fig. 3.26**. A input current THD of 3 % was measured on all three phases, indicating that the mitigation algorithm still performs well under these conditions. This is due to the fact that the input filter capacitor voltage ripple also reduces with the load current. The resulting THD for the three input currents as a function

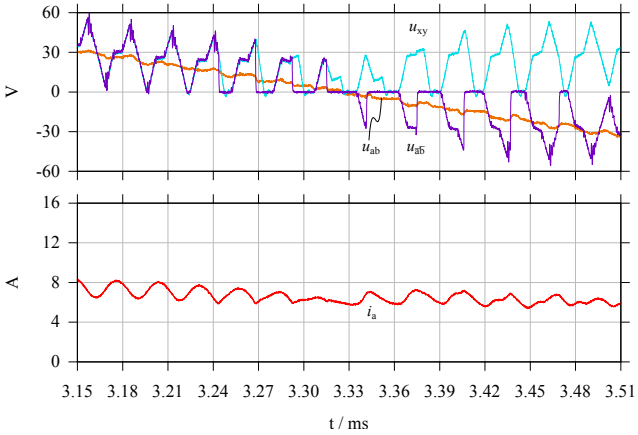

Fig. 3.24: Measurement results for the first intersection of u_a and u_b at $\omega t \approx \pi/3$ for the same operating conditions as in **Fig. 3.23**.

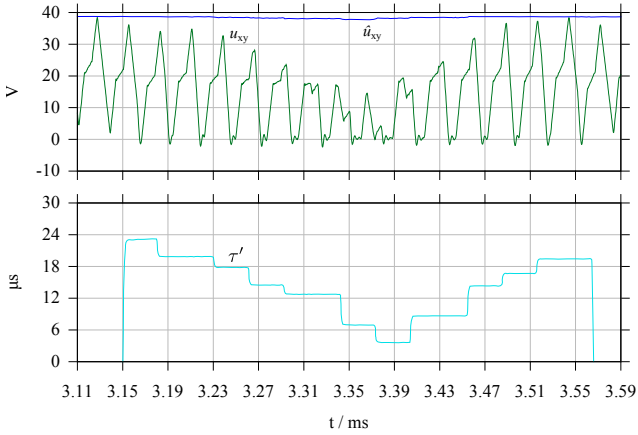

Fig. 3.25: Detailed results of the first mains voltage intersection of the mains voltages u_a and u_b ($\omega t \approx \pi/3$). Shown are the switching frequency ripple u_{xy} of the dc-side filter capacitors, the estimated peak value $\hat{u}_{xy}$ and the calculated turn-on time of the additional injection switch τ'.

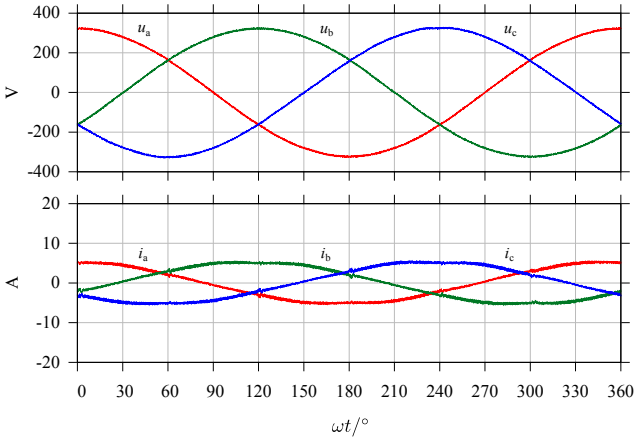

Fig. 3.26: Measurement results for low load operation ($I_{dc} \approx 6$ A). An input current THD of 3.0 % results for all three currents. Note that u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created using postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$. An input current THD of 1.3 % was measured for i_a and i_b and 1.4 % for i_c.

of load power are shown in **Fig. 3.27** together with the measured efficiency.[2]

3.5.3 Distorted and Unsymmetrical Mains Voltages

As explained in **Section 3.4.4**, the proposed algorithm is based on the measured ac input voltages, which makes it inherently robust to non-sinusoidal and unsymmetrical mains voltages. Measurement results for an unsymmetrical ac mains, containing 14 V first harmonic negative sequence voltage, resulting in a voltage u_a with a 6.8 % higher amplitude than voltages u_b and u_c, are shown in **Fig. 3.28**. The rectifier's control is configured for ohmic mains behavior as described in the previous chapter, therefore all three ac input currents are sinusoidal and i_a has a higher amplitude than i_b and i_c. An input current THD of 1.6 % was measured for phases a and b and 1.4 % for phase c.

To verify the performance of the proposed algorithm with distorted mains voltages the prototype rectifier was also connected to the lab's utility grid.

[2] Including DSP/FPGA, gate drivers and cooling losses

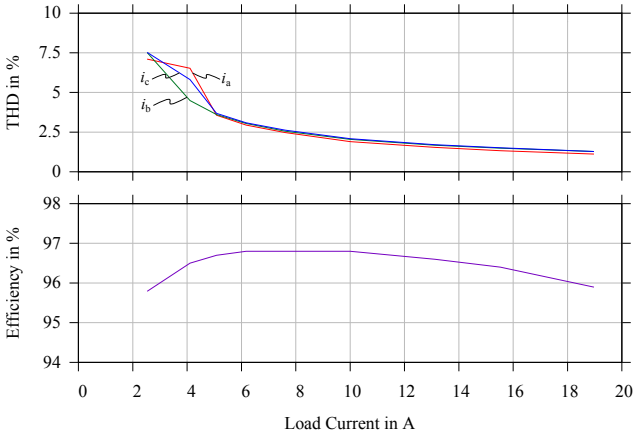

Fig. 3.27: Measured ac input current THD and converter efficiency in ac-to-dc power transfer as a function of load power with symmetrical, sinusoidal three-phase mains voltages.

The measured input voltages and currents are shown in **Fig. 3.29**. In this case the input current THD increases slightly to 1.4 %.

3.5.4 DC-to-AC Power Transfer

Measurement results for dc-to-ac power transfer at nominal power are shown in **Fig. 3.30**. Again, the mitigation algorithm is disabled during the two intersections at $\omega t \approx 240°$ and $\omega t \approx 300°$ for comparison. Furthermore, the input filter capacitor voltage u_{xy} is shown. Note that it is positive at all times, which is in accordance with **Section 3.4.3**.

Fig. 3.31 shows detailed measurements of the first intersection of u_a and u_b at $\omega t \approx 60°$ for the same operating conditions as in **Fig. 3.30**, including the input voltage $u_{\bar{a}\bar{b}}$ of the IVS. Note that the average of $u_{\bar{a}\bar{b}}$ closely follows the mains voltage u_{ab}. The mains voltage u_{ab} shows a switching frequency ripple due to the output impedance of the ac-source employed to provide the three-phase ac mains supply voltage.

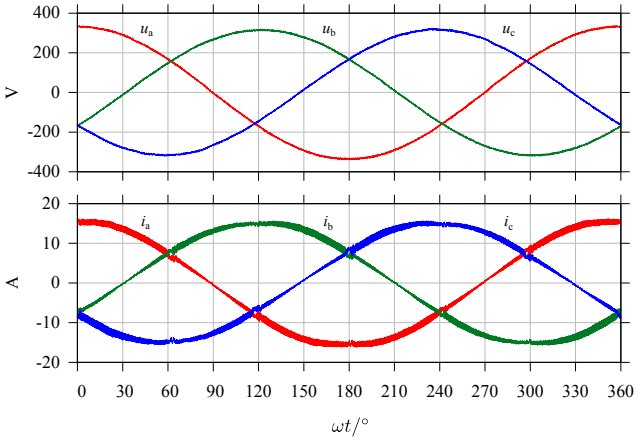

Fig. 3.28: Measurement results of the prototype converter with active mitigation algorithm operated at unsymmetrical mains voltages where u_a is 6.8 % higher in amplitude than u_b and u_c. An input current THD of 1.6 % was measured for phases a and b and 1.4 % for phase c. Note that u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created with postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

3.6 Summary

This chapter analyzes the ac input current distortions in three-phase buck-type SWISS Rectifiers, which are caused by the switching frequency voltage ripple across its input filter capacitors. An analytical model is derived that allows the estimation of the distortion current's peak value and its impact on the converter's overall THD. It is shown that the current distortion's magnitude depends on the ac-side filter inductance value, the ratio of switching frequency and ac mains frequency and the ac filter capacitance value.

In order to reduce the current distortion, a modification of the original SWISS Rectifier, which consists of an ac input filter, an IVS commutated at mains frequency and two series-connected dc-dc converters, is proposed: By moving the ac-side filter capacitors to the output side of the IVS, the dc-dc converters and the IVS can be operated independently. This allows a temporary pulse width modulation of the IVS switches at the mains voltage sector boundaries in order to mitigate the input current distortions. Furthermore, the currents in the IVS switches are continuous in the modified circuit

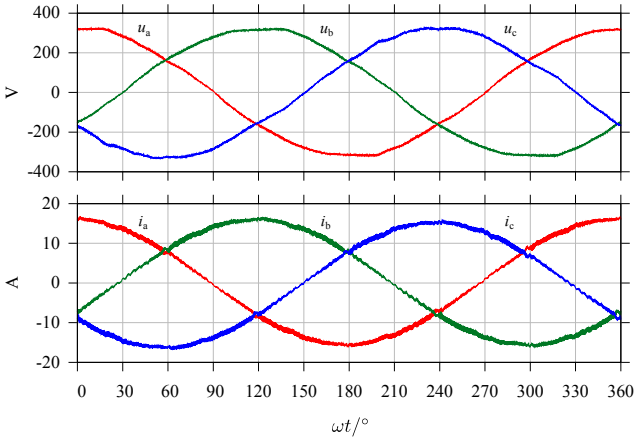

Fig. 3.29: Measurement results for the prototype converter with active mitigation algorithm operated at distorted mains voltages obtained from the lab's utility grid. u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created with postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$. An input current THD of 1.3 % was measured for i_a and i_b and 1.4 % for i_c.

topology as opposed to the original SWISS Rectifier where the IVS conducts discontinuous currents. This implies that the conduction losses in the IVS switches are reduced due to the proposed modification.

The modulation concept and the formulas required for its implementation are derived and can be applied to uni- and bidirectional SWISS Rectifiers in ac-to-dc as well as dc-to-ac power transfer. Furthermore, the proposed algorithm does not require additional sensors; the dc-link current sensor and the ac mains voltage sensors, which are typically present in a SWISS Rectifier, are sufficient. In total, seven multiplications, one division and one square root have to be evaluated once every switching cycle.

Simulations of various operating conditions and measurements taken on a 7.5 kW hardware prototype are proving the principle's feasibility.

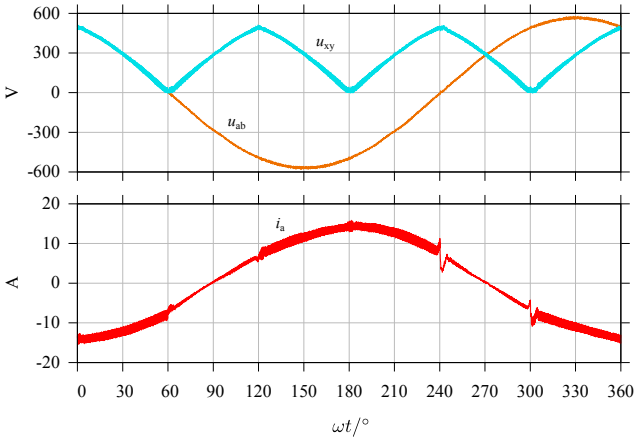

Fig. 3.30: Measurement results for the SWISS Rectifier prototype operated with nominal dc-to-ac power transfer. The distortion compensation is turned off during the intersection at $\omega t \approx 240°, 300°$ for illustrative purposes.

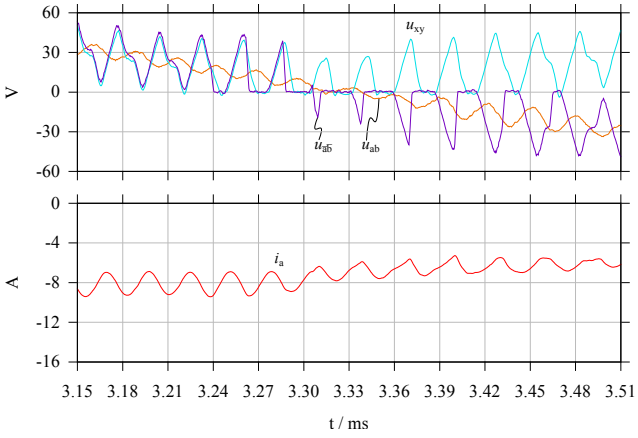

Fig. 3.31: Detailed measurement results of the first mains voltage intersection of phases a and b (at $\omega t \approx \pi/3$) for the same configuration as in **Fig. 3.30**. Shown are the voltage u_{xy} of the dc-side input filter capacitors, the line-to-line grid voltage u_{ab} and the output voltage $u_{\bar{a}\bar{b}}$ of the IVS, as well as the mains current i_a.

4

Design and Implementation of a 99.3% Efficient Interleaved SWISS Rectifier

DC power distribution systems for data centers, industrial applications and residential areas are expected to provide higher efficiency, higher reliability and lower cost compared to ac systems and have been an important research topic in recent years. In these applications an efficient power factor correction (PFC) rectifier, supplying the dc distribution bus from the conventional three-phase ac mains is typically required. This chapter analyzes the three-phase, buck-type, unity power factor SWISS Rectifier for the realization of an ultra-efficient PFC rectifier stage with 400 V rms line-to-line ac input voltage and 400 V dc output voltage. It is shown that the mains current THD of the rectifier can be improved significantly by interleaving two converter output stages. Furthermore, the dc output filter is implemented using a current compensated Integrated Common-Mode Coupled Inductor that ensures equal current sharing between the interleaved half-bridges and provides common-mode EMI filter inductance. Based on a theoretical analysis of the coupled inductor's magnetic properties, the necessary equations

and the design procedure for selecting semiconductors, magnetic core and number of turns, and the EMI filter are derived. Using 1.2 kV SiC MOSFETs, an high-efficient 8 kW, 4 kW/dm^3 (64 W/in^3) lab-scale prototype converter is designed. Measurements taken on the prototype confirm a full-power efficiency of 99.16 %, a peak efficiency of 99.26 % and the compliance to CISPR 11 Class B emission limits.

4.1 Introduction

Over the last decades the power demand of intrinsic dc loads, such as information and communication technology equipment, data centers, electric vehicle battery charging stations, LED lighting equippment, etc. increased substantially. Furthermore renewable energy sources such as PV modules, fuel cells and battery storages are also based on dc. Therefore, dc distribution systems are expected to give advantages in terms of efficiency, reliability and/or cost as the total number of conversion stages can be reduced. Consequently, dc power supplies and dc distribution systems for information and communication technology equipment, electric vehicle traction battery fast charging and dc microgrids have been a major topic in research and industry in recent years and corresponding standards have been issued [73,75–77,85,92,93,107,109,110,125,126].

In these applications, loads with typically tens of kilowatts or more, are supplied from a dc bus with ≈ 400 V that is powered from the conventional 400 V or 480 V rms (line-to-line) three-phase ac mains. Due to the high power levels sinusoidal ac input currents, in phase with the mains voltage are required. As the dc bus voltage is lower than the amplitude of the full-wave rectified three-phase line-to-line voltage, two-stage systems are normally used. These consist of a boost-type PFC rectifier front end providing ≈ 800 V dc and a subsequent step-down dc-dc converter. Buck-type PFC rectifiers, which allow a direct conversion from the three-phase ac mains to a dc bus with lower voltage, are an advantageous alternative offering potentially lower losses, volume and cost [32, 35, 127].

The schematic of the three-phase buck-type SWISS Rectifier introduced in [14] is shown in **Fig. 4.1(a)**. It consists of an ac-side EMI input filter, an Input Voltage Selector (IVS) and two buck-type dc-dc converters $S_{x\bar{p}}$, $D_{y\bar{p}}$ and $S_{\bar{n}z}$, $D_{\bar{n}y}$. Note that all diodes and switches in the IVS are commutated at mains frequency only, therefore basically no switching losses occur in the IVS. Hence, diodes with a low forward voltage drop, or MOSFET-based synchronous rectifiers can be used in the IVS. The IVS output voltages u_x, u_y, u_z are sections of sinusoidal waveforms, as the input phase with highest

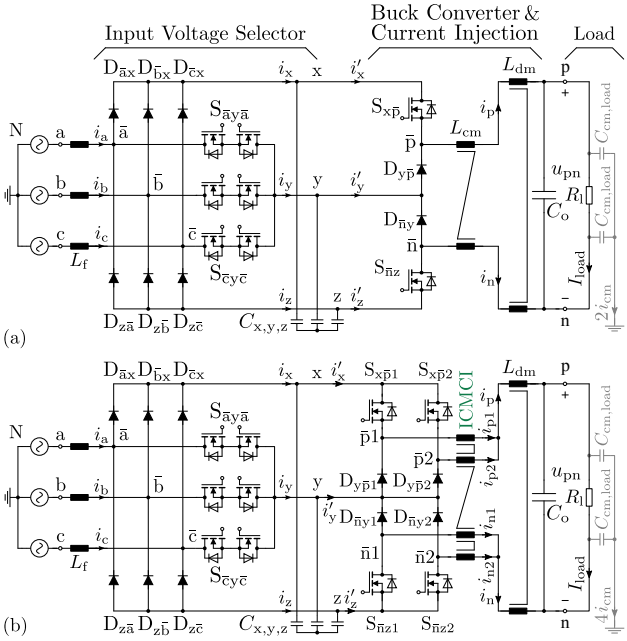

Fig. 4.1: (a) Conventional three-phase buck-type SWISS Rectifier consisting of an EMI input filter, an Input Voltage Selector commutated at mains frequency and two dc-dc buck converters as proposed in [14]. **(b)** Proposed interleaved SWISS Rectifier using a novel four winding current compensated Integrated Common-Mode Coupled Inductor (ICMCI) that is used to ensure equal current sharing $i_{p1} \approx i_{p2}$, $i_{n1} \approx i_{n2}$, and provides common-mode EMI filter inductance.

potential is always connected to node x, the one with lowest potential to z and the remaining phase to node y.

In this chapter, the conventional SWISS Rectifier (single buck converter output stage), cf. **Fig. 4.1(a)**, and the interleaved SWISS Rectifier, cf. **Fig. 4.1(b)** [129], are compared regarding their ac input and dc output properties in **Section 4.2**. The main steps and the necessary equations for the design of an ultra-efficient interleaved SWISS Rectifier are discussed in **Section 4.3**. Measurement results obtained from an 8 kW prototype are presented in **Section 4.4**. Finally, main findings are summarized in **Section 4.5**.

Tbl. 4.1: Converter Specifications

Input Voltage (Line-to-Neutral)	$U_1 = 230\,\text{V rms}$
Input Frequency	$\omega_1 = 2\pi\,50\,\text{Hz}$
Switching Frequency	$f_{sw} = 27\,\text{kHz}$
Nominal Output Voltage	$U_{pn} = 400\,\text{V}$
Nominal Output Power	$P = 8\,\text{kW}$
Input Filter Capacitance	$C_{x,y,z} = 4.4\,\mu\text{F}$
Input Filter Inductance	$L_f = 150\,\mu\text{H}$
DM Output Inductance	$L_{dm} = 350\,\mu\text{H}$
CM Output Inductance	$L_{cm} = 600\,\mu\text{H}$

4.2 SWISS Rectifier

4.2.1 Non-Interleaved SWISS Rectifier

In **Fig. 4.1(a)** the SWISS Rectifier with two coupled dc output inductors, L_{cm} for common-mode (cm) and L_{dm} differential-mode (dm) is shown. As the dc load is connected between output nodes p and n of the converter and has no connection to the star-point N of the ac mains, $i_p = -i_n$ can usually be assumed and the dm inductor alone would be sufficient for implementing the basic converter function. However, this is not the case if the load is, for example, a widespread dc distribution bus, potentially including physically large backup batteries, which can have a significant capacitance $C_{cm,load}$ to ground. This creates a conduction path from the output nodes p and n to the grounded star-point N for high-frequency cm currents i_{cm} as shown in **Fig. 4.1**. This is also the case if dedicated cm capacitors are added to the converter as part of a cm filter, which is typically required to comply with EMI regulations.

Simulation results for a conventional, i.e. non-interleaved 8 kW SWISS Rectifier specified in **Tbl. 4.1** are shown in **Fig. 4.2(a)**. It can be seen that the ac input currents i_a, i_b, i_c show a significant switching frequency ripple and distortions with an amplitude of ≈ 6 A at every 60° mains voltage sector boundary. Detailed simulation results for the vicinity of the first sector boundary at $\omega t \approx 60°$ are shown in **Fig. 4.3(a)**. These distortions are due to the switching frequency voltage ripple on the filter capacitors $C_{x,y,z}$ as described in [128]. As u_x, u_y and u_z are sections of sinusoidal waveforms due to the IVS operation, the capacitors $C_{x,y,z}$ create reactive power at the ac input, despite being connected to the dc-side of the IVS. This reactive power

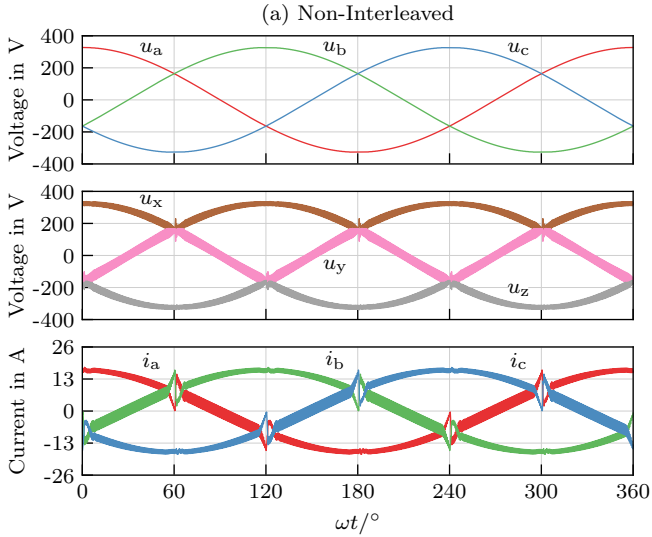

Fig. 4.2: Simulation results for a conventional and an interleaved 8 kW SWISS Rectifier (cf. **Fig. 4.1**) as specified in **Tbl. 4.1**, showing the ac line voltages $u_{a,b,c}$, the filter capacitor voltages $u_{x,y,z}$ and the resulting ac input currents $i_{a,b,c}$. **(a)** Due to the discontinuous input currents $i'_{x,y,z}$ of the non-interleaved dc-dc buck converters [cf. **Fig. 4.1(a)**] a high ripple in $u_{x,y,z}$ and in the ac input currents $i_{a,b,c}$ results. This also leads to significant distortions at each 60° mains voltage sector boundary in $i_{a,b,c}$ as described in [128]. Figure continued on next page.

demand is typically limited to a few percent of the converter's rated output power, which limits the capacitance value of $C_{x,y,z}$. As the SWISS Rectifier is a buck-type topology the input currents i'_x, i'_y and i'_z of the dc-dc converters are discontinuous. In connection with the limited capacitance of $C_{x,y,z}$, this results in a high switching frequency ripple of u_x, u_y and u_z, cf. **Fig. 4.3(a)**.

4.2.2 SWISS Rectifier with Interleaved Output Stages

To reduce the input current and voltage ripples, either the ac input filter capacitance and inductance can be increased or a higher switching frequency can be used. Both options increase volume and/or losses and cost of the converter system. In order to overcome these disadvantages two interleaved dc-dc converters can be used as output stage to reduce the input and output current ripples [111, 130, 131]. The schematic of the resulting system, denomi-

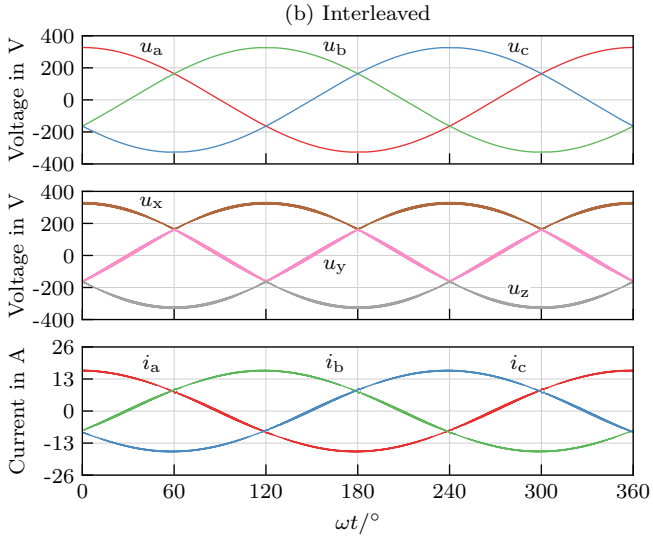

Fig. 4.2 (Cont.): (b) In the interleaved SWISS Rectifier [cf. **Fig. 4.1(b)**] the switching frequency voltage ripples of $u_{x,y,z}$ are reduced significantly due to harmonic cancellation, which reduces the ac input current ($i_{a,b,c}$) ripple and the resulting current distortions at sector boundaries.

nated as *interleaved SWISS Rectifier* in the following, is shown in **Fig. 4.1(b)** where two individual bridge legs $S_{x\bar{p}1}$ / $D_{y\bar{p}1}$ and $S_{x\bar{p}2}$ / $D_{y\bar{p}2}$ are used for the p-side, and $S_{\bar{n}z1}$ / $D_{\bar{n}y1}$, $S_{\bar{n}z2}$ / $D_{\bar{n}y2}$ are used for the n-side dc-dc converter stage.

In **Fig. 4.2(b)** simulation results for the interleaved SWISS Rectifier are shown. It can be seen that the ripple of the IVS output voltages u_x, u_y, u_z (i.e. of the filter capacitor voltages) and of the ac input currents are reduced significantly compared to **Fig. 4.2(a)**. By using the same duty cycle but 180° phase shifted carriers for the pulse width modulation of e.g. $S_{x\bar{p}1}$ and $S_{x\bar{p}2}$, the high-frequency components of the resulting input current i'_x have twice the effective frequency and half the amplitude compared to the non-interleaved case. This can be seen from the corresponding simulation results for the first mains voltage intersection at $\omega t \approx 60°$ shown in **Fig. 4.3(b)**. Due to the reduced ripple of the buck converter input currents i'_x, i'_y and i'_z, the peak-to-peak ripple on the filter capacitor voltages u_x, u_y and u_z reduces from 60 V without interleaving to 18 V with interleaving. Also the ripple and the

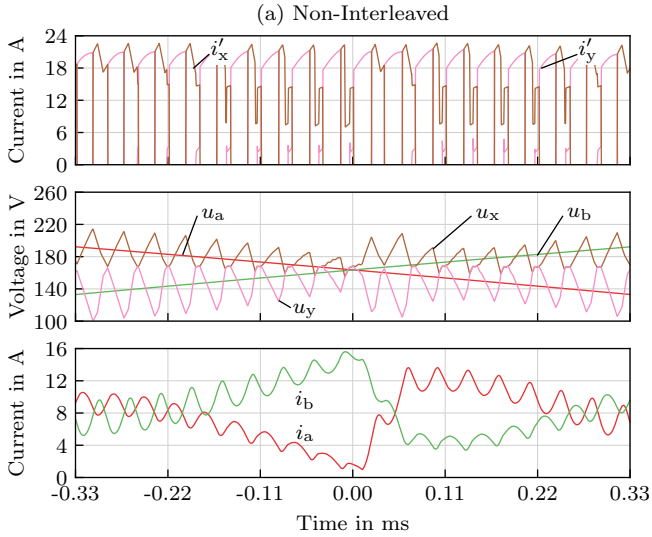

Fig. 4.3: Detailed simulation results of the first intersection of the mains line-to-neutral voltages u_a and u_b at $\omega t \approx 60°$. **(a)** The discontinuous buck converter input currents i'_x, i'_y of the conventional non-interleaved SWISS Rectifier [cf. **Fig. 4.1(a)**] lead to high switching frequency ripples of the input filter capacitor voltages u_x and u_y. As u_x and u_y cannot intersect due to $D_{y\bar{p}}$ and $S_{x\bar{p}}$, a distortion of the mains currents i_a and i_b results [128]. Figure continued on next page.

distortions of the input currents i_a, i_b and i_c occurring at every 60° mains voltage sector boundary are reduced from $\approx 6\,A$ to $< 1\,A$.

Note that the interleaved buck converters can be controlled such that the individual dc-dc converter currents are split equally, i.e. $i_{p1} = i_{p2}$ and $i_{n1} = i_{n2}$ except for the switching frequency ripple. This allows current compensated filtering of the dc-dc converter output voltages with closely coupled inductors. Ideally, these carry no dc flux component in the magnetic core and can therefore be implemented without an air-gap, leading to a larger inductance value, similar to a cm inductor. Typically this is realized with so called Intercell Transformers (ICTs) [22–25, 132], where the interleaved SWISS Rectifier requires two ICTs, one for the p- and one for the n-side bridges as shown in **Fig. 4.4(a)**. To analyze this circuit, the SWISS Rectifier's input filter, IVS, and dc-dc converters are replaced by equivalent voltage sources, which define the potentials of nodes $\bar{p}1$, $\bar{p}2$, $\bar{n}1$ and $\bar{n}2$ with respect

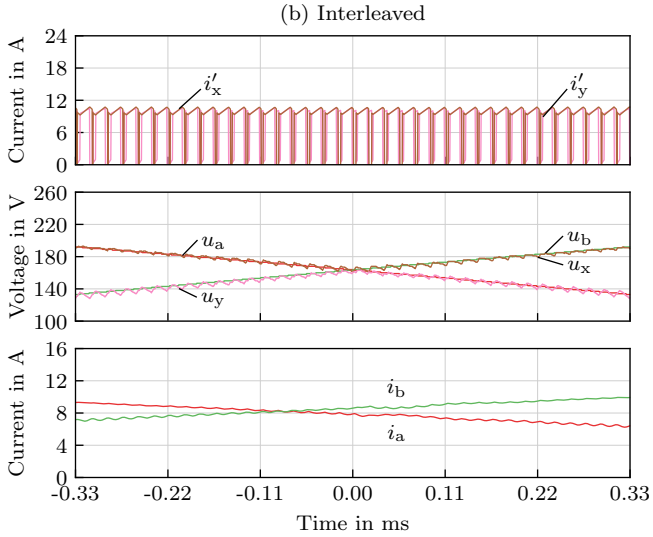

Fig. 4.3 (Cont.): (b) In case of an interleaved SWISS Rectifier [cf. **Fig. 4.1(b)**], the amplitude of i'_x, i'_y is reduced and the effective frequency is doubled, which leads to a significant reduction of the ripples in u_x and u_y. The intersection of i_a and i_b leads that of u_a and u_b by 200 µs (i.e. 3.7°) due to the reactive current created by the input filter capacitors $C_{x,y,z}$.

to the mains star-point and/or ground. These four voltage sources can be converted to a tree structure of a cm, an outer differential-mode (odm) and two inner differential-mode (idm) voltage sources as shown in **Fig. 4.4(b)**. These equivalent voltages can be calculated using a linear transformation **S**

$$\underbrace{\begin{bmatrix} u_{\mathrm{cm}} \\ u_{\mathrm{odm}} \\ u_{\mathrm{idm,p}} \\ u_{\mathrm{idm,n}} \end{bmatrix}}_{\mathbf{u}_{\mathrm{sep}}} = \underbrace{\frac{1}{4}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 2 & 2 & -2 & -2 \\ 2 & -2 & 0 & 0 \\ 0 & 0 & 2 & -2 \end{bmatrix}}_{\mathbf{S}} \cdot \underbrace{\begin{bmatrix} u_{\tilde{\mathrm{p}}1} \\ u_{\tilde{\mathrm{p}}2} \\ u_{\tilde{\mathrm{n}}1} \\ u_{\tilde{\mathrm{n}}2} \end{bmatrix}}_{\mathbf{u}}, \tag{4.1}$$

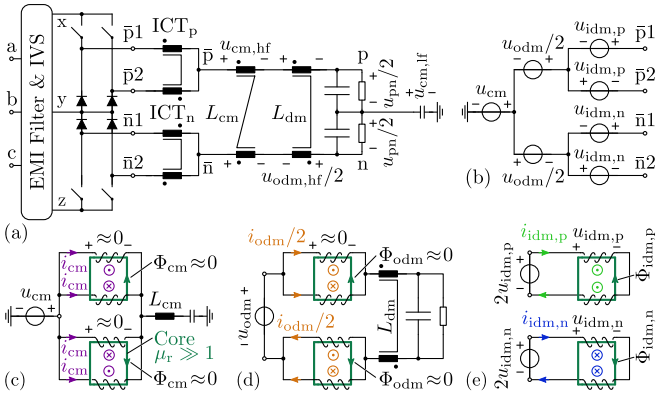

Fig. 4.4: (a) Simplified circuit diagram of the interleaved SWISS Rectifier with two Intercell Transformers (ICTs). The IVS and the dc-dc converters can be replaced by equivalent voltage sources split into common-mode (cm), outer differential-mode (odm) and p- and n-side inner dm (idm,p & idm,n) components as shown in **(b)**. For cm **(c)** and odm **(d)** the currents in the ICT windings cancel and basically no flux results in the ICTs' cores. **(e)** This is not the case for the idm voltages, which create the fluxes $\Phi_{\mathrm{idm,p}}$ and $\Phi_{\mathrm{idm,n}}$ in the ICTs' cores.

with the inverse transformation

$$\mathbf{T} = \mathbf{S}^{-1} = \frac{1}{2}\begin{bmatrix} 2 & 1 & 2 & 0 \\ 2 & 1 & -2 & 0 \\ 2 & -1 & 0 & 2 \\ 2 & -1 & 0 & -2 \end{bmatrix}. \tag{4.2}$$

It can be seen from the equivalent circuit diagrams shown in **Fig. 4.4(c)** and **(d)** that the cm and odm currents cancel in the two windings of each ICT. Therefore, neither cm nor odm flux results in the ICTs' cores, while the idm voltages are applied to the ICTs' windings and drive corresponding fluxes $\Phi_{\mathrm{idm,p}}$ and $\Phi_{\mathrm{idm,n}}$.

4.2.3 Integrated Common-Mode Coupled Inductor

In order to reduced the number of magnetic components in the interleaved SWISS Rectifier, the two ICTs and the cm inductor L_{cm} can be integrated into a single four-winding magnetic device, which is denominated as *Integrated Common-Mode Coupled Inductor* (ICMCI) in the following and is shown in

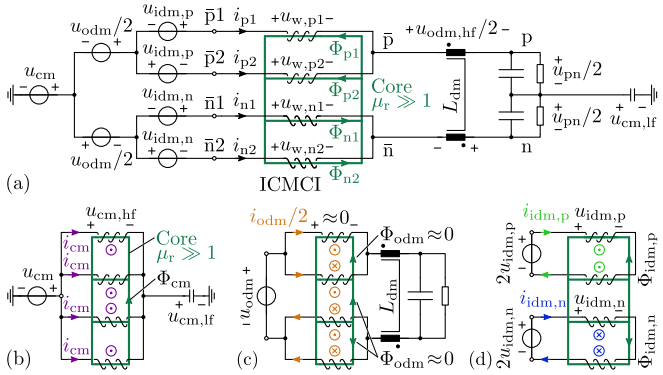

Fig. 4.5: (a) Circuit diagram of the interleaved SWISS Rectifier with an Integrated Common-Mode Coupled Inductor (ICMCI) that provides cm **(b)** and idm **(d)** inductance, hence no dedicated cm inductor L_{cm} is required. **(c)** The directions of the p- and n-side windings are selected such that the odm current i_{odm} cancels in all three windows of the core, which implies that the ICMCI does not provide odm inductance and can therefore use a core without air gaps, similar to conventional ICTs.

Fig. 4.1(b) and **Fig. 4.5(a)**. To analyze the ICMCI's magnetic properties, the mains voltages, IVS and buck converters are again replaced by a tree structure of cm/odm/idm voltage sources. Neglecting any leakage fluxes in the ICMCI,s the fluxes Φ_{p1}, Φ_{p2}, Φ_{n1}, Φ_{n2} generated by the four windings have to fulfill

$$\Phi_{\mathrm{p1}} + \Phi_{\mathrm{p2}} = \Phi_{\mathrm{n1}} + \Phi_{\mathrm{n2}} \,, \tag{4.3}$$

due to the ICMCI's core structure, cf. **Fig. 4.5(a)**. This implies that the sum of the p- and n-side winding voltages has to be equal, i.e.

$$u_{\mathrm{w,p1}} + u_{\mathrm{w,p2}} = u_{\mathrm{w,n1}} + u_{\mathrm{w,n2}} \,. \tag{4.4}$$

Using Kirchhoff's voltage law on the circuit shown in **Fig. 4.5(a)**, three additional equations can be found

$$u_{\mathrm{w,p1}} - u_{\mathrm{w,p2}} = 2\,u_{\mathrm{idm,p}} \,, \tag{4.5}$$

$$u_{\mathrm{w,n1}} - u_{\mathrm{w,n2}} = 2\,u_{\mathrm{idm,n}} \,, \tag{4.6}$$

$$u_{\mathrm{w,p1}} + u_{\mathrm{w,p2}} + u_{\mathrm{w,n1}} + u_{\mathrm{w,n2}} = 4\,\underbrace{(u_{\mathrm{cm}} - u_{\mathrm{cm,lf}})}_{u_{\mathrm{cm,hf}}} \,. \tag{4.7}$$

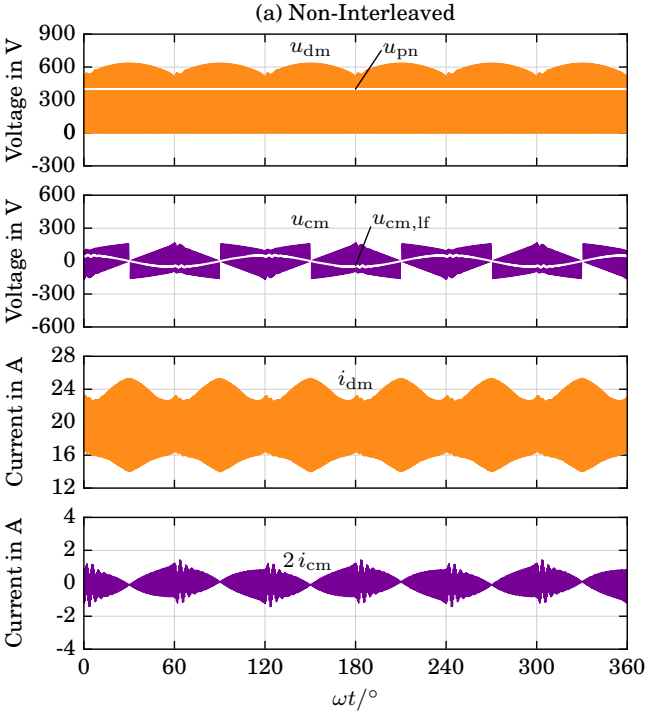

Fig. 4.6: (a) Detailed simulation results for a conventional non-interleaved SWISS Rectifier with the same operating conditions as in **Fig. 4.2**, showing dm and cm voltages u_{dm} and u_{cm} created by the dc-dc converter stages and the resulting dm current i_{dm} and the total cm current ($2\,i_{cm}$ and $4\,i_{cm}$). Figure continued on next page.

Note that $u_{cm,hf}$ is the switching frequency component of the converter's cm voltage u_{cm} as given by (4.1). Solving the system of equations defined by (4.4) – (4.7) with respect to the ICMCI's winding voltages yields

$$u_{w,p1} = \quad u_{idm,p} + u_{cm,hf}\ , \tag{4.8}$$

$$u_{w,p2} = -u_{idm,p} + u_{cm,hf}\ , \tag{4.9}$$

$$u_{w,n1} = \quad u_{idm,n} + u_{cm,hf}\ , \tag{4.10}$$

$$u_{w,n2} = -u_{idm,n} + u_{cm,hf}\ . \tag{4.11}$$

It can be seen that the ICMCI's winding voltages are defined only by the switching frequency cm voltage and the inner dm voltages, while the outer

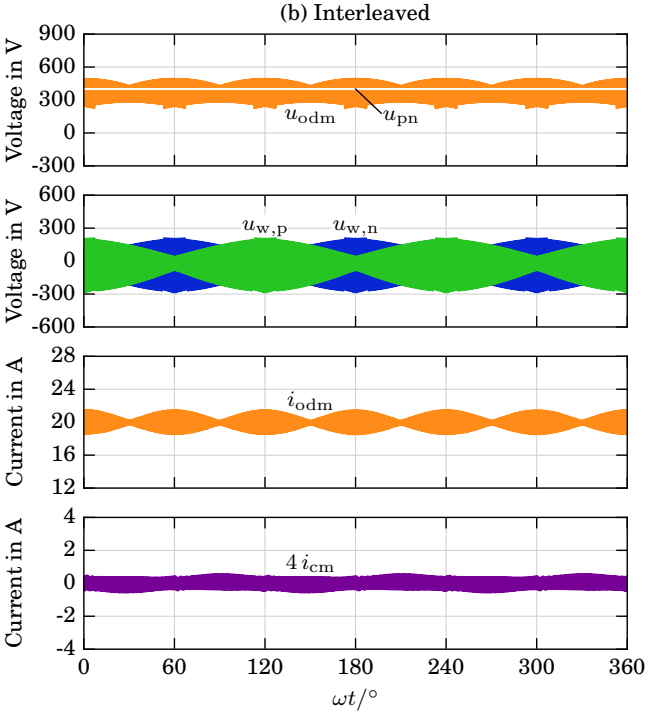

Fig. 4.6 (Cont.): (b) Simulation results of the corresponding quantities of an interleaved SWISS Rectifier employing an ICMCI. Due to the interleaving the outer differential-mode (odm) voltage u_{odm} peak-to-peak ripple reduces, which leads to a reduction of the ripple of the corresponding current i_{odm}.

dm voltage is applied only to the dm inductor L_{dm} and the dc output u_{pn} which can also be seen from the equivalent circuit diagrams in **Fig. 4.5(b-d)**

Simulation results of the ICMCI's winding voltages and the outer dm voltage for nominal operation are shown in **Fig. 4.6(b)**. Compared to a conventional non-interleaved SWISS Rectifier the (outer) dm voltage applied to L_{dm} is reduced, which leads to a significant reduction of the peak-to-peak ripple in i_{odm} compared to i_{dm} [cf **Fig. 4.6(a)**]. The same holds for the cm current i_{cm}.

In **Fig. 4.7** simulated switching frequency voltage and current waveforms for a reduced switching frequency of 9 kHz are shown for $0^\circ \leq \omega t \leq 30^\circ$. It can be seen that the ICMCI's winding voltages $u_{\mathrm{w,p1}}$, $u_{\mathrm{w,p2}}$, $u_{\mathrm{w,n1}}$ and $u_{\mathrm{w,n2}}$

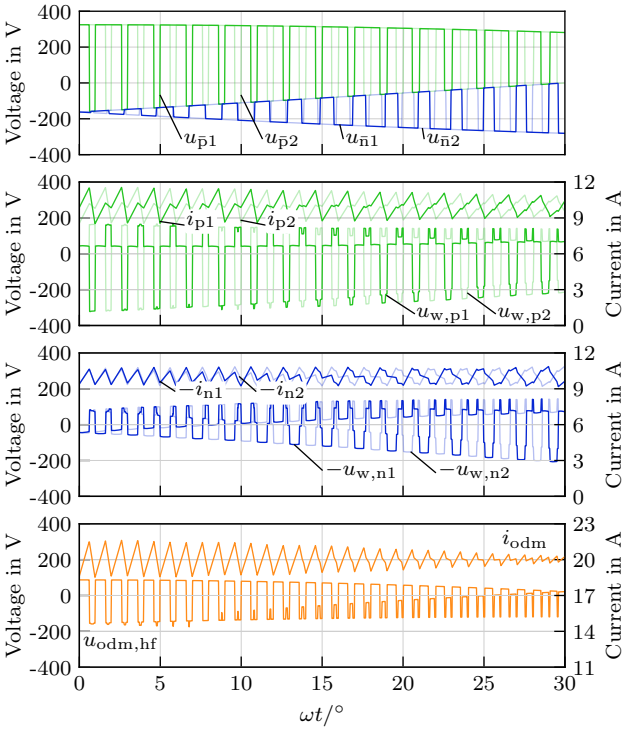

Fig. 4.7: Simulated dc-dc converter output voltages $u_{\bar{p}1}$, $u_{\bar{p}2}$ and $u_{\bar{n}1}$, $u_{\bar{n}2}$ during a 30° mains voltage sector, with a reduced switching frequency of 9 kHz. This results in the ICMCI voltages $u_{w,p1}$, $u_{w,p2}$, $u_{w,n1}$ and $u_{w,n2}$ and the outer dm voltage $u_{odm,hf}$ applied to L_{dm}.

are periodic with the switching frequency, while the voltage $u_{odm,hf}$ applied to L_{dm} shows twice that frequency due to harmonic cancellation.

4.2.4 Cube-Type ICMCI

Implementing an ICMCI with a core with four parallel branches as shown in **Fig. 4.5(a)**, typically requires either a custom core or an assembly of different core material rods and/or plates. Due to the finite permeability of the core material and leakage fluxes, different couplings between the four windings result. These disadvantages can be overcome by using a symmetric structure

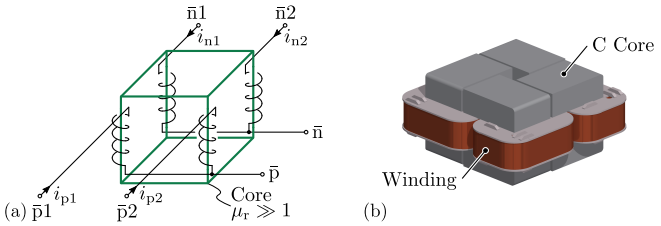

Fig. 4.8: (a) Structure of a symmetrical, cube-type ICMCI core, which is constructed from four C cores, where each core carries one winding as shown in **(b)**.

where the edges of a cube form the ICMCI's core and each of the four vertical core branches holds one winding. This structure can be assembled from four conventional C (or U) cores, each carrying one winding as shown in **Fig. 4.8**.

For a cube-type ICMCI two different possible winding configurations exist: The p-side windings can either be wound on two neighboring branches or on diagonally opposing ones. In **Fig. 4.9(a)** the neighboring case is shown were air gaps δ_1 exist in the magnetic paths connecting the p- and n-side and air gaps δ_2 exist in the perpendicular direction. Neglecting leakage fluxes and the finite permeability of the core material, the reluctance model **Fig. 4.9(b)** results. In **Fig. 4.9(c)** and **(d)** the resulting cm and idm magnetomotive forces and fluxes are shown. Alternatively, the p-side windings can be wound on diagonally opposing branches as shown in **Fig. 4.9(e)**. The corresponding reluctance model is given in **Fig. 4.9(f)**, where an air gap δ is assumed between all the individual C cores. The resulting cm and idm flux paths are shown in **Fig. 4.9(g)** and **Fig. 4.9(h)**.

In order to derive a model of the cube-type ICMCI, the reluctance models shown in **Fig. 4.9(b)** and **(f)** can be expressed as inductance matrices **L**

$$\underbrace{\begin{bmatrix} u_{\mathrm{w,p1}} \\ u_{\mathrm{w,p2}} \\ u_{\mathrm{w,n1}} \\ u_{\mathrm{w,n2}} \end{bmatrix}}_{\mathbf{u}_\mathrm{w}} = \mathbf{L}\,\frac{\partial}{\partial t}\underbrace{\begin{bmatrix} i_{\mathrm{p1}} \\ i_{\mathrm{p2}} \\ i_{\mathrm{n1}} \\ i_{\mathrm{n2}} \end{bmatrix}}_{\mathbf{i}}, \tag{4.12}$$

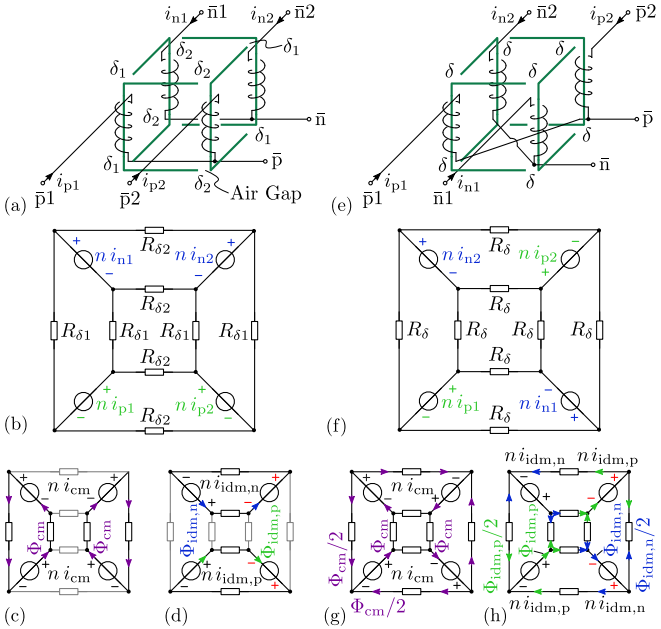

Fig. 4.9: Winding configurations for a cube-type ICMCI: In **(a)** p- and n-side windings are wound on neighboring branches. Neglecting leakage fluxes and assuming high permeability of the core, the reluctance model **(b)** results. The paths of cm and idm fluxes are shown in **(c)** and **(d)**. For the diagonally opposing winding configuration shown in **(e)** the reluctance model **(f)** results with the corresponding cm and idm fluxes **(g)** and **(h)**.

for the neighboring ($\mathbf{L}_\mathrm{n}$) and opposing ($\mathbf{L}_\mathrm{o}$) configuration as

$$\mathbf{L}_\mathrm{n} = \frac{n^2}{2}\begin{bmatrix} \frac{R_{\delta1}+R_{\delta2}}{R_{\delta1}R_{\delta2}} & \frac{-1}{R_{\delta2}} & \frac{1}{R_{\delta1}} & 0 \\ \frac{-1}{R_{\delta2}} & \frac{R_{\delta1}+R_{\delta2}}{R_{\delta1}R_{\delta2}} & 0 & \frac{1}{R_{\delta1}} \\ \frac{1}{R_{\delta1}} & 0 & \frac{R_{\delta1}+R_{\delta2}}{R_{\delta1}R_{\delta2}} & \frac{-1}{R_{\delta2}} \\ 0 & \frac{1}{R_{\delta1}} & \frac{-1}{R_{\delta2}} & \frac{R_{\delta1}+R_{\delta2}}{R_{\delta1}R_{\delta2}} \end{bmatrix}, \tag{4.13}$$

$$\mathbf{L}_\mathrm{o} = \frac{n^2}{2R_\delta}\begin{bmatrix} 2 & 0 & 1 & 1 \\ 0 & 2 & 1 & 1 \\ 1 & 1 & 2 & 0 \\ 1 & 1 & 0 & 2 \end{bmatrix}, \tag{4.14}$$

where n is the number of turns. Using the linear transformations (4.1) and (4.2), these matrices can be separated into cm, idm and odm as

$$\mathbf{u}_{\mathrm{w,sep}} = \underbrace{\mathbf{S}\,\mathbf{L}_{\mathrm{n}}\,\mathbf{T}}_{\mathbf{L}_{\mathrm{n,sep}}}\,\mathbf{i}_{\mathrm{sep}}\,, \tag{4.15}$$

$$\mathbf{L}_{\mathrm{n,sep}} = n^2 \begin{bmatrix} \frac{1}{R_{\delta 1}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{2R_{\delta 1}+R_{\delta 2}}{2R_{\delta 1}R_{\delta 2}} & \frac{1}{2R_{\delta 1}} \\ 0 & 0 & \frac{1}{2R_{\delta 1}} & \frac{2R_{\delta 1}+R_{\delta 2}}{2R_{\delta 1}R_{\delta 2}} \end{bmatrix}, \tag{4.16}$$

$$\mathbf{L}_{\mathrm{o,sep}} = \frac{n^2}{R_{\delta}} \begin{bmatrix} 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{4.17}$$

It can be seen from (4.16) and (4.17) that both winding configurations provide a cm and idm inductance but no odm inductance. This is due to the fact that leakage fluxes are neglected in the derivation. Note that in the neighboring configuration, $\mathbf{L}_{\mathrm{n,sep}}$ has two non-zero entries that are not on its principal diagonal, which implies that the two inner differential-modes are coupled. Hence, the p-side idm voltage $u_{\mathrm{idm,p}}$, applied to windings p1 and p2, will create a switching frequency ripple current in all four windings of an ICMCI in neighboring winding configuration, which will typically lead to higher conduction losses than the opposing winding configuration.

4.2.5 Modulation and Control

Similar to conventional ICTs, an equal sharing of the load current between the two p- and the two n-side windings is necessary to avoid saturating the ICMCI's core, which is typically achieved using closed loop control. The proposed control block diagram for the interleaved SWISS Rectifier with an ICMCI in opposing winding configuration is shown in **Fig. 4.10**. An outer output voltage controller G_{u} is used to control u_{pn} and determines the outer dm current reference signal i^*_{odm}. By measuring the four ICMCI currents i_{p1}, i_{p2}, i_{n1} and i_{n2}, the outer and the two inner dm currents are calculated using (4.1) and fed into the corresponding current controllers G_{odm} and G_{idm}. By adding the output voltage as a feed-forward term to the output of G_{odm} and diving by the maximum output voltage $1.5\,\hat{U}_1$, the modulation index $m \in [0,1]$ is derived [14, 123]. Multiplying m with two unity amplitude,

Tbl. 4.2: Current Stresses

Semiconductor	RMS Current	Nominal
$D_{\bar{k}x}$, $D_{z\bar{k}}$	$\hat{I}\sqrt{\frac{\sqrt{3}}{8\pi}+\frac{1}{6}}$	7.97 A
$S_{\bar{k}y\bar{k}}$	$\hat{I}\sqrt{\frac{1}{6}-\frac{\sqrt{3}}{4\pi}}$	2.79 A
$S_{x\bar{p}1,2}$, $S_{\bar{n}z1,2}$	$\hat{I}\sqrt{\frac{3\sqrt{3}}{8\pi\, m}}$	8.23 A
$D_{y\bar{p}1,2}$, $D_{\bar{n}y1,2}$	$\hat{I}\sqrt{\frac{1}{4\,m^2}-\frac{3\sqrt{3}}{8\pi\, m}}$	5.67 A
	$\hat{I} \approx \frac{2\,P}{3\,\hat{U}_1} \approx m\, I_{\mathrm{load}}$	

piece-wise sinusoidally shaped signals s_p and s_n, as described in [123] for the non-interleaved SWISS Rectifier, yields the duty cycle signals d_p and d_n. The rescaled outputs $d_{idm,p}$ and $d_{idm,n}$ of the inner dm current controllers G_{idm} are added and subtracted from d_p and d_n, in order to determine the actual duty cycles d_{p1}, d_{p2}, d_{n1} and d_{n2} of the individual bridges. Note that this allows an active control of the current sharing between the ICMCI windings. A reference value of zero is used for the inner dm currents to ensure an equal current sharing in the windings, even with unsymmetrical dc-dc converters resulting from mismatches of switching delays, unequal conduction losses, etc.

4.3 Prototype Design for Ultra-High Efficiency

For power supply systems, which are operated 24/7, as given in data centers, an ultra-high efficiency is highly desirable to minimize the cost of conversion losses and cooling and hence the operating costs of the system [133, 134]. Furthermore, a high efficiency over a wide range of output currents is required in applications where redundant supplies are used, resulting in a nominal operation at half of the rated power or less. Therefore, the design procedure for a SWISS Rectifier that achieves an efficiency of $> 99\,\%$ for $P > P_{\mathrm{rated}}/3$ for the operating conditions listed in **Tbl. 4.1** is presented in the following.

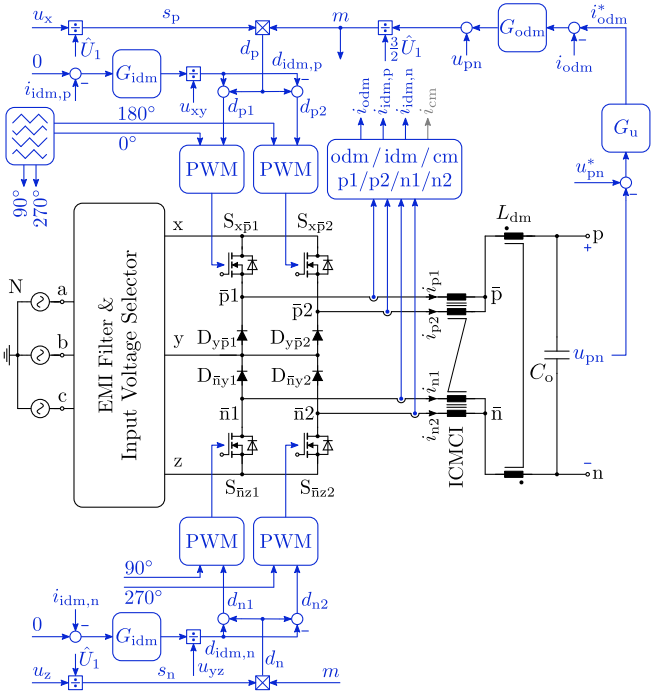

Fig. 4.10: Control block diagram for the interleaved SWISS Rectifier, using an outer feedback loop G_u to control the dc output voltage u_{pn}, which creates the reference i^*_{odm} for the outer dm current controller G_{odm}. Its output is used to derive the rectifier's modulation index $m \in [0, 1]$, which is multiplied with piece-wise sinusoidal signals s_p and s_n to derive the duty cycles d_p and d_n of the p- and n-side buck converter stages. Two additional inner dm controllers G_{idm} are used to ensure equal current sharing in the ICMCI windings by controlling the inner dm currents $i_{idm,p}$ and $i_{idm,n}$ with a setpoint value equal to zero.

4.3.1 Semiconductors

The peak reverse voltage applied to the IVS semiconductors is equal to the peak of the ac mains line-to-line voltage. This results in 680 V maximum blocking voltage for a 400 V_{rms} mains with 20 % overvoltage and therefore switches and diodes with a blocking voltage rating of 900 V or 1.2 kV are typically used. To achieve the target efficiency, the diodes $D_{\bar{k}x}$ and $D_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$ in the IVS and the diodes $D_{y\bar{p}1,2}$ and $D_{\bar{n}y1,2}$ in the dc-dc converter stages are implemented

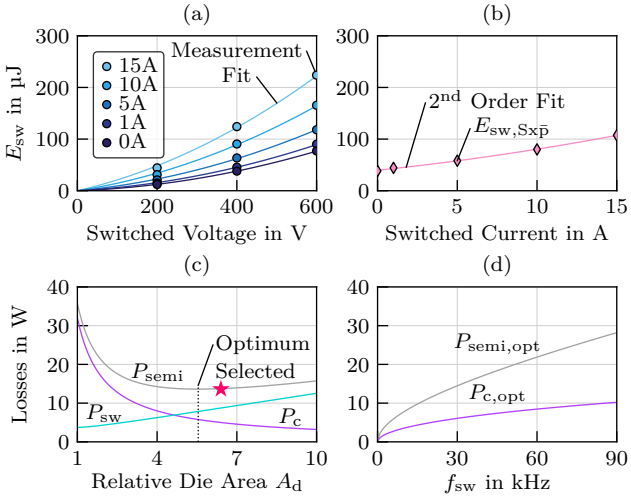

Fig. 4.11: (a) Hard switching losses E_{sw} (sum of turn-on and turn-off) of a *C2M0080120* SiC MOSFET measured in [135] for different currents and voltages, together with second order fits of E_{sw} as function of the switched voltage. **(b)** Switching losses of these SiC MOSFETs used as buck converter half-bridge $S_{x\bar{p}}/D_{y\bar{p}}$, for different switched currents. **(c)** Switching (P_{sw}) and conduction (P_c) losses of the half-bridge and their sum as a function of relative die area, with a *C2M0080120* SiC MOSFET as unit device, for $f_{sw} = 27\,\text{kHz}$ and $I_{load} = 20\,\text{A}$. **(d)** Optimal total losses and conduction losses of the half-bridge as function of the switching frequency.

with MOSFETs operated as synchronous rectifiers. Analytic expressions for the rms currents of all semiconductors, neglecting any switching frequency current ripples, are given in **Tbl. 4.2** [14, 134].

IVS

As basically no switching losses occur in the IVS, *C2M0025120* silicon carbide (SiC) MOSFETs from Wolfspeed, with a nominal $R_{DS(on)}$ of 25 mΩ, are selected for $D_{\bar{k}x}$ and $D_{z\bar{k}}$ as they have the lowest on-state resistance of commercially available MOSFETs in a TO-247 package at the time of prototype realization. Similar *C2M0080120* SiC MOSFETs, with a nominal $R_{DS(on)}$ of 80 mΩ, are used for the four-quadrant switches $S_{\bar{k}y\bar{k}}$, as the rms current is approximately three times lower than that of $D_{\bar{k}x}$ and $D_{z\bar{k}}$.

Buck Converter Stages

For the buck converter stages SiC MOSFETs are selected as well, due to their high blocking voltage rating (1.2 kV) and low conduction and switching losses compared to Si IGBTs and Si MOSFETs [135, 136]. As the SWISS Rectifier is a buck-type circuit, the dc-dc converter stages are switching a constant output current, which is essentially equal to the load current ($i \approx I_{\text{load}}$) if the switching frequency ripple is neglected, over a varying voltage. Measured hard switching losses E_{sw} of a half-bridge with two *C2M0080120* SiC MOSFETS are shown in **Fig. 4.11(a)**, as function of the switched voltage and the switched current. For each current value i a second-order function,

$$E_{\text{sw}}(i, u) \approx e_1(i)\, u + e_2(i)\, u^2 \ , \tag{4.18}$$

with parameters $e_1(i)$ and $e_2(i)$ is fitted using least squares regression. The resulting values for the parameters e_1 and e_2 are listed in **Tbl. 4.3** and the corresponding fit lines are shown in **Fig. 4.11(a)**. To calculate the switching losses of the buck converter half-bridge $\text{S}_{\text{x}\bar{\text{p}}}/\text{D}_{\text{y}\bar{\text{p}}}$, the fit lines (4.18) are averaged over the time-varying mains input voltage u_{xy} as

$$\begin{aligned} E_{\text{sw,S}\text{x}\bar{\text{p}}}(i) &= \frac{3}{\pi} \int_0^{\frac{\pi}{3}} E_{\text{sw}}(i, u_{\text{xy}}(\omega t))\ d\,\omega t \\ &\approx e_1(i)\, U_{\text{xy,avg}} + e_2(i)\, U_{\text{xy,rms}}^2 \ , \end{aligned} \tag{4.19}$$

for every measured current value i. The resulting values are shown as markers in **Fig. 4.11(b)** together with a second-order approximation,

$$E_{\text{sw,S}\text{x}\bar{\text{p}}}(i) \approx E_0 + E_1\, i + E_2\, i^2 \tag{4.20}$$

$$E_0 = 40\,\mu\text{J} \quad E_1 = 3.3\,\mu\text{J/A} \quad E_2 = 8.3\,\text{nJ/A}^2 \ , \tag{4.21}$$

of the switching losses as function of the switched current. Assuming that switching and conduction losses scale with die area A_{d} as

$$P_{\text{sw}}(A_{\text{d}}) = f_{\text{sw}}\, A_{\text{d}}\, E_{\text{sw,S}\text{x}\bar{\text{p}}}\,(J) \quad J = \frac{I_{\text{load}}}{A_{\text{d}}} \tag{4.22}$$

$$\text{and} \quad P_{\text{c}}(A_{\text{d}}) = \frac{R_{\text{DS(on)}}}{A_{\text{d}}} I_{\text{load}}^2 \ , \tag{4.23}$$

an analytical expression of the optimal die area $A_{\text{d,opt}}$, which achieves the minimal sum of switching and conduction losses for a given switching frequency,

Tbl. 4.3: Fitted Parameters for Switching Losses as Function of the Switchted Voltage

i **in A**	0	1	5	10	15
e_1 **in nJ/V**	29	44	72	120	178
e_2 **in nJ/V²**	0.16	0.18	0.21	0.26	0.32

can be derived [137]:

$$P_{\text{semi}}(A_{\text{d}}) = P_{\text{c}}(A_{\text{d}}) + P_{\text{sw}}(A_{\text{d}}) \,, \tag{4.24}$$

$$A_{\text{d,opt}} = I_{\text{load}} \sqrt{\frac{R_{\text{DS(on)}} + f_{\text{sw}} E_2}{f_{\text{sw}} E_0}} \,. \tag{4.25}$$

This is shown in **Fig. 4.11(c)** for $f_{\text{sw}} = 27\,\text{kHz}$ and for the nominal dc output current of $I_{\text{load}} = 20\,\text{A}$. The resulting minimal semiconductor losses of the half-bridge can then be calculated as

$$P_{\text{semi,opt}} = I_{\text{load}} \left[2\sqrt{f_{\text{sw}} E_0 \left(R_{\text{DS(on)}} + f_{\text{sw}} E_2 \right)} + f_{\text{sw}} E_1 \right] \tag{4.26}$$

and depend on the switching frequency as shown in **Fig. 4.11(d)**. Finally, SiC MOSFETs with an on-state resistance of 25 mΩ are selected for all buck-stage switches of the prototype rectifier which corresponds to a total of 6.4 unit devices and is close to the optimum as shown in **Fig. 4.11(c)**. The selected semiconductors and the calculated losses are summarized in **Tbl. 4.4**.

4.3.2 Dimensioning of the ICMCI

For the magnetic core of the current compensated ICMCI, *3C94* ferrite material from *Ferroxcube* is used due to its comparatively low losses. As C (or U) cores made from ferrite are not as easily available as other shapes like E cores, the smallest core which allows to achieve the desired efficiency target, a U46/40/28, was selected. The opposing winding configuration is used for the ICMCI as it features a lower current ripple than the neighboring configuration.

In order to selected the number of turns n of the ICMCI such that minimal losses and stable operation without saturation are achieved, equations for the resulting magnetic fluxes in the different parts of the core are required. Due to the symmetry of the cube-type ICMCI, it is sufficient to consider only one winding and the corresponding C core. Assuming the opposing winding configuration and omitting leakage fluxes, the flux Φ_{p1} in the vertical core

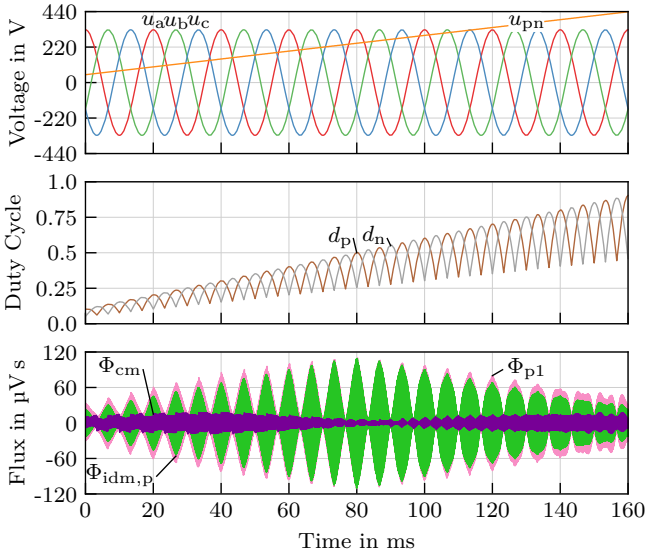

Fig. 4.12: Simulation results showing the ICMCI's cm flux Φ_{cm}, its p-side inner dm flux $\Phi_{idm,p}$ and the flux in winding p1, $\Phi_{p1} = \Phi_{cm} + \Phi_{idm,p}$, for a dc output voltage u_{pn} that increases from 49 V ($m = 0.1$) to 439 V ($m = 0.9$) within eight mains voltage periods. The maximum of Φ_{p1} occurs at 80 ms for $d_p = m = 0.5$, where $\Phi_{idm,p}$ is maximal as well and Φ_{cm} is close to zero.

branch carrying winding p1, consists only of the cm flux (Φ_{cm}) and the p-side inner dm flux ($\Phi_{idm,p}$). Both, cm and idm flux, are furthermore separated into low-frequency (lf) and high-frequency (hf), i.e. switching frequency and higher, components:

$$\Phi_{p1} = \underbrace{\Phi_{cm,lf} + \Phi_{cm,hf}}_{\Phi_{cm}} + \underbrace{\Phi_{idm,p,lf} + \Phi_{idm,p,hf}}_{\Phi_{idm,p}} . \tag{4.27}$$

Both hf flux components can be calculated from the ICMCI's winding voltages $u_{w,p1}$, $u_{w,p2}$, $u_{w,n1}$, $u_{w,n2}$ (cf. **Fig. 4.7**) by applying (4.1) and integrating over time. The lf cm flux can be calculated from the ICMCI's cm inductance L_{cm} and the lf cm current $i_{cm,lf}$ which is required to charge and discharge the cm capacitance of the load ($C_{cm,load}$) and the EMI filter capacitor (C_{fb}) as

$$\Phi_{cm,lf} = \frac{L_{cm}}{n} i_{cm,lf} \approx \frac{L_{cm}}{n} \left(C_{fb} + \frac{C_{cm,load}}{2}\right) \frac{d}{dt} u_{cm,lf} . \tag{4.28}$$

Note that the required lf cm voltage can be calculated from the IVS output voltages and the steady-state duty cycles as

$$u_{\mathrm{cm,lf}} = d_{\mathrm{p}} u_{\mathrm{x}} + (2 - d_{\mathrm{n}} - d_{\mathrm{p}})\, u_{\mathrm{y}} + d_{\mathrm{n}} u_{\mathrm{z}}\,. \tag{4.29}$$

The idm lf flux results from the lf idm current, occurring due to the current sensors' offset and gain errors, which are specified in the data sheet as $i_{\mathrm{idm,p,lf}} = 300\,\mathrm{mA}$ under worst-case conditions. This leads to:

$$\Phi_{\mathrm{idm,p,lf}} = \frac{L_{\mathrm{idm}}}{n}\, i_{\mathrm{idm,p,lf}} \leq 19\,\mu\mathrm{V\,s}\,. \tag{4.30}$$

Similar to (4.27) the flux in the horizontal branches of the core can be calculated as (cf. **Fig. 4.9**)

$$\Phi_{\mathrm{h}} = \frac{\Phi_{\mathrm{cm}}}{2} + \frac{\Phi_{\mathrm{idm,p}}}{2} + \frac{\Phi_{\mathrm{idm,n}}}{2}\,. \tag{4.31}$$

Using equations (4.27) and (4.31), the core losses occurring in the vertical and horizontal core branches can be calculated with standard approaches, such as the improved Generalized Steinmetz Equation (iGSE) [138]. The number of turns n can then be selected to achieve minimal losses in the ICMCI; $n = 20$ turns and $0.4\,\mathrm{mm} \times 15\,\mathrm{mm}$ copper foil are selected for the prototype.

Additionally, the peak flux $\hat{\Phi}_{\mathrm{p1}}$ for worst-case operating conditions is required to ensure that the peak flux density in the ICMCI's core stays below the magnetic material's saturation flux density. Note that an analytic derivation of $\hat{\Phi}_{\mathrm{p1}}$ is theoretically possible by maximizing (4.27), but out of the scope of this chapter as the waveforms are quite complex and depend on the modulation index m and the mains voltages. However, simulation results of the winding flux Φ_{p1}, as well as the cm and idm fluxes (Φ_{cm} & $\Phi_{\mathrm{idm,p}}$), are shown in **Fig. 4.12**, for the output voltage u_{pn} changing from 49 V ($m = 0.1$) to 439 V ($m = 0.9$) within eight mains voltage periods. It can be seen in **Fig. 4.12** that the winding flux Φ_{p1} assumes its maximum for $d_{\mathrm{p}} = 0.5$ at $\omega t = 0°$ (i.e. $m = 0.5$ and $u_{\mathrm{pn}} = 244\,\mathrm{V}$), which corresponds to the maximum of the hf idm flux $\hat{\Phi}_{\mathrm{idm,hf}}$ while the hf cm flux is very close to zero in this case. Therefore, the peak winding flux can be approximated as

$$\hat{\Phi}_{\mathrm{p1}} \approx \hat{\Phi}_{\mathrm{cm,lf}} + \hat{\Phi}_{\mathrm{idm,p,lf}} + \hat{\Phi}_{\mathrm{idm,hf}}\,. \tag{4.32}$$

Note that the peak lf cm current, and hence lf cm flux, occurs for $m = 0$ and can be calculated as

$$\hat{\Phi}_{\mathrm{cm,lf}} = \frac{L_{\mathrm{cm}}}{n}\, \hat{U}_1 \omega_1 C_{\mathrm{fb}} = 3.2\,\mu\mathrm{V\,s}\,. \tag{4.33}$$

Tbl. 4.4: Selected Components

Device	Chosen Part	Losses per Device
$D_{x\bar{k}}$, $D_{\bar{k}z}$	C2M0025120	1.8 W
$S_{\bar{k}y\bar{k}}$	C2M0080120	0.8 W
$S_{x\bar{p}1,2}$, $S_{\bar{n}z1,2}$	C2M0025120	4.9 W
$D_{y\bar{p}1,2}$, $D_{\bar{n}y1,2}$	C2M0025120	1.0 W
	ICMCI	$\boldsymbol{L_{dm}}$
Core	4×U46/40/28-3C94	F3CC25
Wire	0.4×15 mm (foil)	2.4×6 mm
Turns	$n = 20$, opposing conf.	2×15
Measured Inductance	$L_{idm} = 1.28$ mH $L_{cm} = 2.40$ mH $L_{odm} = 37$ µH	350 µH
Volume	420 cm^3	249 cm^3
Losses	9.6 W	2.9 W

Finally, the maximum peak hf idm flux can be derived from $u_{w,p1}$ and $u_{w,p2}$ as

$$\hat{\Phi}_{idm,hf} = \frac{3\,\hat{U}_1}{2}\frac{1}{8\,f_{sw}\,n} = 113\,\mu\text{V s}\,. \tag{4.34}$$

Together with an effective core cross section of $A_e = 392\,\text{mm}^2$ a peak flux density of

$$\hat{B}_{pk} = \frac{\hat{\Phi}_{p1}}{A_e} = 345\,\text{mT} \tag{4.35}$$

results, which is sufficiently below the core material's saturation flux density of $B_{sat} \geq 450$ mT, and allows operation with more than 20 % mains overvoltage. The main parameters and measured inductance values of the implemented ICMCI are listed in **Tbl. 4.4**. In accordance with (4.17) the ICMCI's measured cm inductance of 2.40 mH is approximately twice its idm inductance of 1.28 mH, while an odm inductance of 37 µH results due to leakage fluxes.

4.3.3 EMI Filter

A schematic of the implemented prototype rectifier, including all electromagnetic interference (EMI) filter components, is shown in **Fig. 4.13(a)** and the

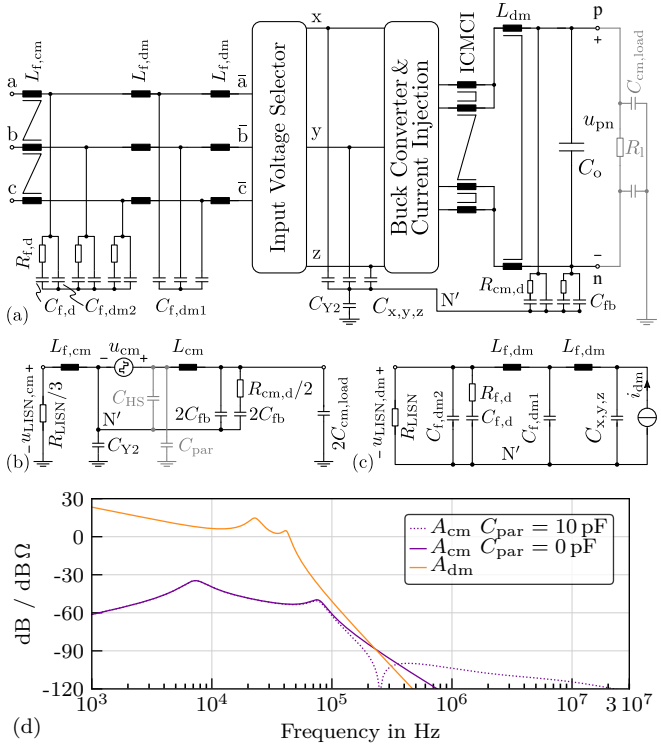

Fig. 4.13: (a) Schematic of the implemented EMI filter and **(b)** its equivalent cm circuit and **(c)** equivalent dm circuit. In **(d)** the calculated attenuation for cm and dm are plotted. The cm attenuation is shown for the ideal case and with a parasitic capacitance C_{par} = 10 pF between the buck-stage output terminals and PE.

selected components are listed in **Tbl. 4.5**. As a detailed analysis and design of the EMI filter are out of this chapter's scope, only the main differences to the design of EMI filters for conventional boost-type PFC rectifiers are discussed [139].

The cm equivalent circuit of the SWISS Rectifier with EMI filter is shown in **Fig. 4.13(b)**, where the buck converter switches are replaced by a voltage source u_{cm}. As the ICMCI provides a cm inductance L_{cm}, a first cm filter stage is implemented on the dc-side together with the feedback capacitors C_{fb} and the corresponding damping resistors $R_{cm,d}$. By connecting C_{fb} to the star-point N′ of the capacitors $C_{x,y,z}$ instead of connecting them to protective

earth (PE), the low-frequency (i.e. 150 Hz) current flowing through C_{fb} does not contribute to the rectifier's ground leakage current, which typically has to be less than 3.5 mA for safety reasons [140]. Note that the cm filter's attenuation also depends on the load's capacitance $C_{\mathrm{cm,load}}$ between the dc rails (p & n) and PE [141]. For the design and verification of the cm filter a load with a total capacitance between the dc terminals and PE of $2C_{\mathrm{cm,load}} = 8\,\mathrm{nF}$ is used. This is approximately two orders of magnitude larger than the typical $\approx 100\,\mathrm{pF}$ coupling capacitance between primary and secondary of a cascaded isolated dc-dc converter of the same power range. For applications with a considerably higher value of $C_{\mathrm{cm,load}}$, such as photovoltaic arrays which can have hundreds of nF per kW output power [142], an additional filter stage could be added between C_{o} and output terminals p and n.

Additionally, an Y2 safety-rated capacitor C_{Y2} is added between N′ and PE, to allow the cm current that flows through the load's cm capacitance $C_{\mathrm{cm,load}}$ to return to the converter, without flowing through the line impedance stabilization network (LISN). An additional cm filter inductor $L_{\mathrm{f,cm}}$ is added on the ac-side, resulting in a third-order filter with attenuation A_{cm} from u_{cm} to $u_{\mathrm{LISN,cm}}$, as plotted in **Fig. 4.13(d)**. Note that the heat sinks are connected to N′ and not to PE, in order to minimize the parasitic capacitance C_{par} between the buck-stage output terminals ($\bar{\mathrm{p}}1$, $\bar{\mathrm{p}}2$, $\bar{\mathrm{n}}1$, $\bar{\mathrm{n}}2$) and PE, as C_{par} bypasses the dc-side cm filter elements and leads to a reduced attenuation for frequencies above $\approx 400\,\mathrm{kHz}$. This can be seen from the plot in **Fig. 4.13(d)** for $C_{\mathrm{par}} = 10\,\mathrm{pF}$.

In **Fig. 4.13(c)** the dm equivalent single-phase circuit of the rectifier and the EMI filter is shown. The ac-side input of the buck-stage and the IVS are replaced by an equivalent current source i_{dm} and the filter transfer function is calculated as

$$A_{\mathrm{dm}}(\omega) = 20\,\log_{10}\left|\frac{u_{\mathrm{LISN,dm}}(\omega)}{i_{\mathrm{dm}}(\omega)}\,\frac{1}{\Omega}\right|. \tag{4.36}$$

Note that damping resistors $R_{\mathrm{f,d}}$ are added only to the second dm filter stage as the switching frequency voltage ripple at the capacitors of the first filter stage $C_{\mathrm{f,dm1}}$ would cause several watts of losses. Despite this, the resonance frequencies of the dm filter are sufficiently damped and below the effective switching frequency of 54 kHz, as can be seen from **Fig. 4.13(d)**.

4.3.4 DM Inductor

Nanocrystalline core material (*FINEMET*) is used for the dm inductor L_{dm}, due to its high saturation flux density ($\approx 1.2\,\mathrm{T}$) and lower losses compared to

Tbl. 4.5: EMI Filter Components

C_{xyz}	4.4 µF	2× Epcos TDK B32923H3225, 2.2 µF X2 rated
$C_{f,dm1}$	3 µF	2× Epcos TDK B32924C3155, 1.5 µF X2 rated
$C_{f,dm2}$	1.5 µF	Epcos TDK B32924C3155, 1.5 µF X2 rated
$C_{f,damp}$	1.5 µF	Epcos TDK B32924C3155, 1.5 µF X2 rated
C_{Y2}	22 nF	Epcos TDK B32022B3223 , 22 nF Y2 rated
$C_{cm,load}$	4 nF	Epcos TDK B32021 2.2 nF Y2 + parasitic
C_{fb}	264 nF	8× AVX 1812PC333KAT1A, 33 nF 250 V
C_o	680 µF	10× Rubycon 450BXW68MEFC, 68 µF 450 V
$R_{f,d}$	5 Ω	2 W SMD Resistor
$R_{cm,d}$	100 Ω	1 W SMD Resistor
$L_{f,dm}$	15 µH	Würth Elektronik 7443641500
$L_{f,cm}$	140 µH	VAC W380 ring core, 4 turns, 2 mm wire

amorphous alloys. Rectangular wire (2.4 mm × 6 mm) is used due to the high filling factor. The loss calculation and dimensioning of L_{dm} is similar to that of a conventional SWISS Rectifier, except that only the outer dm voltage is applied to L_{dm}. Therefore, it is omitted here for the sake of brevity.

4.3.5 Switching Frequency

Using the design equations described above, a switching frequency f_{sw} that achieves lowest converter losses can be selected. For nominal conditions and full-load an optimal frequency of 21 kHz results with total converter losses of 66.8 W. However, f_{sw} is increased to 27 kHz to lower the worst-case peak flux density (4.35) in the ICMCI and enable a 30 % margin for mains overvoltages, tolerances, transient current unbalances, etc. This increase in switching frequency leads to only 0.6 W of additional losses, which is less than one percent and is below the precision of the employed loss models.

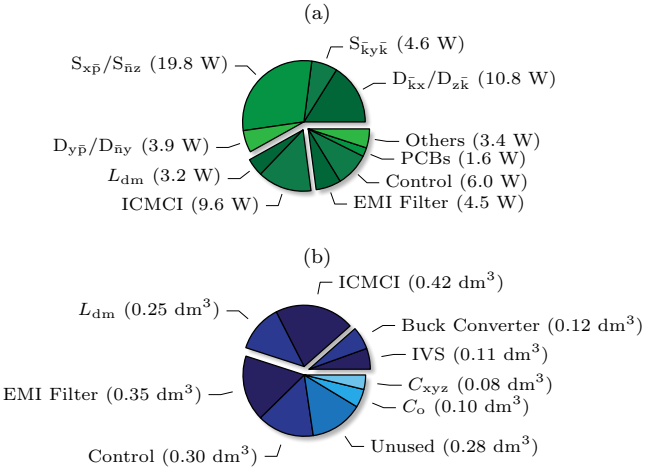

Fig. 4.14: (a) Calculated losses of the rectifier's main components for nominal operation (U_{pn} = 400 V, I_l = 20 A). The control losses include DSP/FPGA, gate drivers, fans and auxiliary supply. The corresponding volumes in dm^3 are shown in **(b)** (1 dm^3 = 61 in^3).

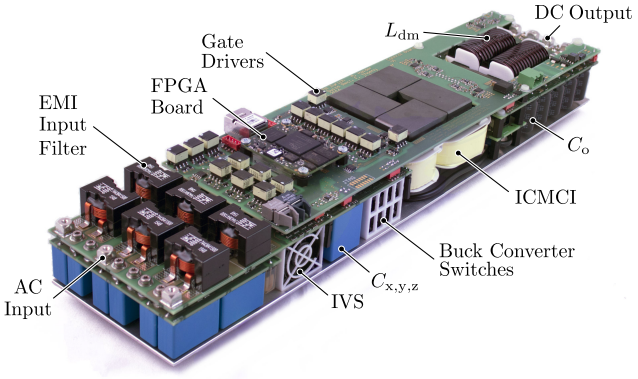

Fig. 4.15: Implemented 8 kW 400 V ac / 400 V dc interleaved SWISS Rectifier prototype (420 mm x 95 mm x 50 mm) with > 99 % efficiency (cf. **Fig. 4.20**) and a power density of 4 kW/dm^3 (66 W/in^3).

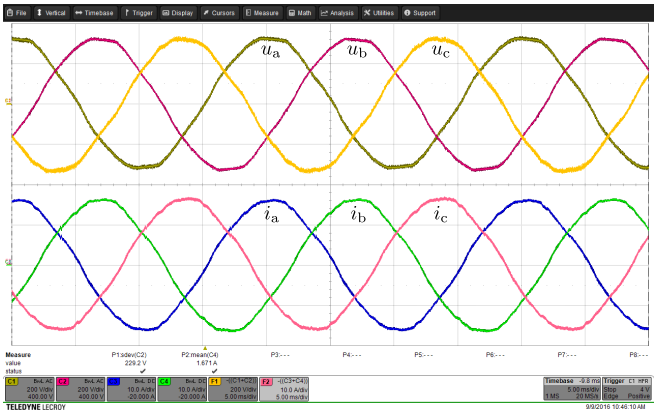

Fig. 4.16: Measured ac mains voltages $u_{a,b,c}$ (200 V / div, public mains, THD 2.3 %) and converter input currents $i_{a,b,c}$ (10 A / div) for nominal operation. Note that the quantities for phases a and b were measured directly while those of phase c are created numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

4.4 Measurement Results

The calculated losses of the selected components for nominal operation are shown in **Fig. 4.14(a)** with the corresponding volumes given in **(b)**. About 58 % of the total losses result from semiconductors, 19 % from the main magnetic components and 23 % from the EMI filter, control, gate drivers, auxiliary supply etc. A picture of the implemented hardware prototype, achieving a power density of 4.0 kW/dm^3 (66 W/in^3), is shown in **Fig. 4.15**. Measurement results taken on the prototype are presented in the following.

4.4.1 AC Input Currents

Measurement results of the rectifier's mains voltages and currents at nominal operation are shown in **Fig. 4.16**. The resulting input currents $i_{a,b,c}$ are nearly sinusoidal and free of distortions at the sector boundaries as expected from the presented simulation results. Note that the rectifier's control circuit is configured for ohmic mains behavior as described in [123]. An input current THD of 2.45 % results for a mains voltage THD of 2.29 %. In **Fig. 4.17** the measured input current THD as a function of the output current is plotted for operation with the mains voltages shown in **Fig. 4.16** and for purely sinusoidal mains voltages (voltage THD < 0.1 %) created with a three-phase

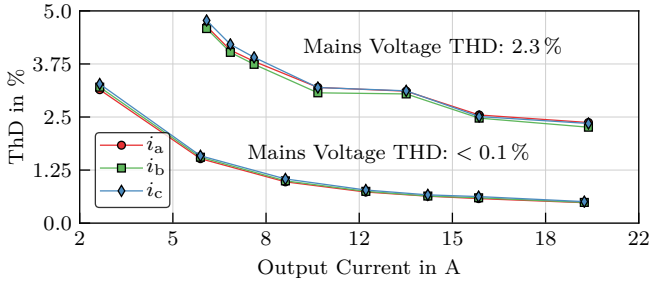

Fig. 4.17: Measured total harmonic distortion (THD) of the rectifier's mains input currents as function of dc output current for a low-distortion mains voltage (voltage THD < 0.1 %), supplied by a three-phase mains simulator, and for a typical public mains voltage with a voltage THD of 2.3 %.

mains simulator, which results in an input current THD of only 0.5 % for rated load.

4.4.2 ICMCI Current Balance

In **Fig. 4.18** measurement results for a step-change of the outer dm current reference i^*_{odm} and/or output current from 15 A to 20 A are plotted. Shown are the measured buck converter output voltage $u_{\bar{\mathrm{p}}1}$ between the ICMCI terminal $\bar{\mathrm{p}}1$ and the mains neutral N, the two positive-side ICMCI currents $i_{\mathrm{p}1}$ and $i_{\mathrm{p}2}$ and the total cm current ($4\,i_{\mathrm{cm}}$) of all four ICMCI windings. Additionally the outer dm current is approximated as $i_{\mathrm{odm}} \approx i_{\mathrm{p}1} + i_{\mathrm{p}2}$ and the positive-side inner dm current is calculated as $i_{\mathrm{idm,p}} = (i_{\mathrm{p}1} - i_{\mathrm{p}2})/2$. As expected from theoretical considerations and simulations the cm and idm current ripples are considerably smaller than the odm current ripple. Furthermore it can be seen that $i_{\mathrm{p}1}$ and $i_{\mathrm{p}2}$ remain balanced and hence $i_{\mathrm{idm,p}}$ stays close to zero, except for the switching frequency ripple, even during the transient of i_{odm}.

4.4.3 Conducted EMI

Measurement results of the rectifier's conducted EMI emission for the frequency range of 150 kHz to 30 MHz are shown in **Fig. 4.19**. Two scans with a maximum peak and an average detector are shown for 4 kHz step size, a resolution bandwidth of 9 kHz and a measurement time of 10 ms. All measured points are below the respective limits, selected peaks have been verified with the CISPR 11 quasi-peak and average detectors with 1 s measurement time.

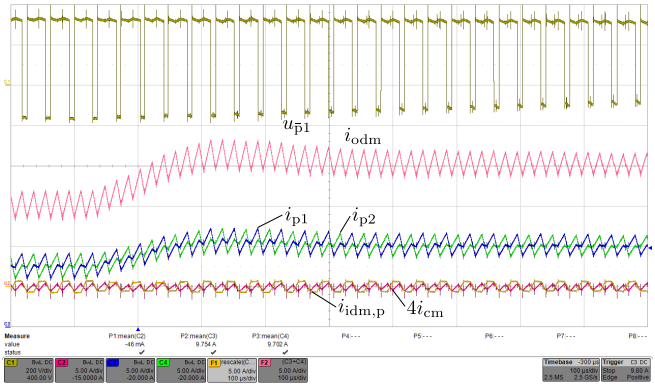

Fig. 4.18: Measurement results for a step-change of the outer dm current reference i^*_{odm} from 15 A to 20 A, showing the voltage $u_{\bar{p}1}$ (200 V / div) between the ICMCI terminal $\bar{p}1$ and the mains neutral, the two positive-side ICMCI currents i_{p1} and i_{p2} (5 A / div) and the total cm current $4i_{cm}$ (5 A / div). Additionally the outer and inner dm currents, created by data postprocessing as $i_{odm} \approx i_{p1} + i_{p2}$ and $i_{idm,p} = (i_{p1} - i_{p2})/2$ (5 A / div), are shown.

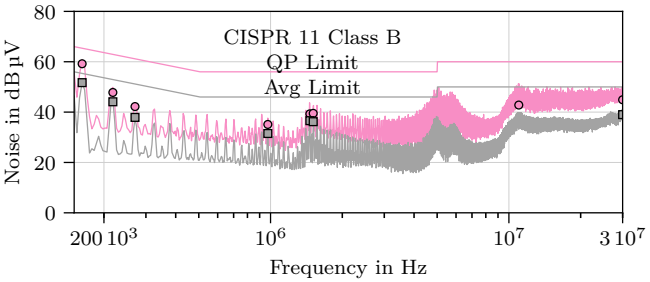

Fig. 4.19: Conducted maximum peak and average EMI noise emission of the prototype rectifier, measured with 4 kHz step size and 10 ms measurement time. Selected peaks (markers) have been measured with the CISPR 11 quasi peak and average detectors with 1 s measurement time. All measurements are below the respective limits for Class B equipment.

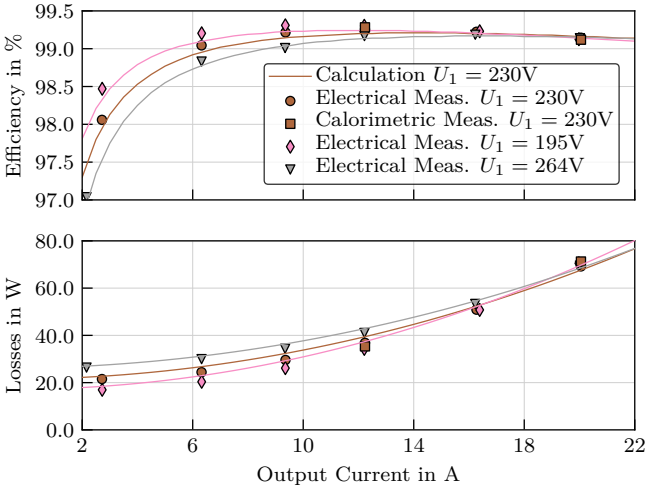

Fig. 4.20: Calculated and measured efficiency of the rectifier as function a of the dc output current, indicating that the converter achieves an efficiency above 99 % for > 30 % rated load with a peak efficiency of 99.26 %. Measurements were taken on the prototype shown in **Fig. 4.15** using a *Yokogawa WT3000* power analyzer. The peak and full-load efficiency for nominal mains voltage (U_1 = 230 V, THD < 0.1 %) have been verified with calorimetric loss measurements which closely match the electrical loss measurement.

4.4.4 Efficiency

The calculated losses and efficiency of the rectifier for U_{pn} = 400 V as function of dc load current are shown in **Fig. 4.20** for three different ac mains voltages together with measurement results taken using a *Yokogawa WT3000* power analyzer. It can be seen that the measurement results of the prototype converter match the calculated losses over a wide range of output currents. For a nominal ac mains voltage of U_1 = 230 V_{rms} a peak efficiency of η = 99.26 % (error range: 98.80 % - 99.74 %) was measured for a dc output current of 12.5 A and η = 99.16 % (error range: 98.84 % - 99.49 %) at rated load, i.e. 20 A. This, rather large, error range results because the power analyzer's user manual states that the voltage and current measurements have range- and reading-errors of 0.05 % for dc. For the selected measurement ranges this leads to an error of ±15 W at full-load, resulting in the stated error range. However, comparisons with high-precision (± ≈ 2 W) calorimetric measurements typi-

cally show an error of less than 4 W, suggesting that the the power analyzer's precision is in fact higher than the value guaranteed by the manufacturer. Due to the rather large error range of the electrical measurement, two operating points have been verified by a calorimetric loss measurement with a precision of 2 % (i.e. 1.4 W), showing only 2 W (2.9 %) higher losses than the electrical measurement [143]. Furthermore, it can be seen from **Fig. 4.20** that for a fixed low output current the losses increase with increasing ac mains voltage due to increasing core and switching losses. For high output currents this is compensated by reduced conduction losses in the input filter and IVS due to the lower mains input currents. This leads to a full-load efficiency of the rectifier that is almost independent of the ac mains voltage.

4.5 Summary

This chapter describes a three-phase buck-type unity power factor SWISS Rectifier with interleaved dc-dc converter output stages. The system allows a single-stage conversion from the three-phase mains to a lower dc voltage. Using interleaved dc-dc converter stages reduces the input current ripple and filter capacitor voltage ripple, which improves the ac input current THD and reduces the dc output current ripple. Furthermore, the required dc output inductors can be combined into a current compensated Integrated Common-Mode Coupled Inductor (ICMCI) and a differential-mode inductor. A symmetric implementation of the ICMCI, based on four conventional U cores is presented and analyzed, showing that the winding currents can be controlled by individual controllers using a proposed common- and differential-mode splitting of the currents.

Based on this approach, a high efficiency interleaved SWISS Rectifier for dc distribution and power supply systems is designed, achieving a power density of 4 kW/dm^3. Electrical and calorimetric measurements taken on a prototype verify an efficiency of 99.16 % at nominal operation with 8 kW dc output power and a peak efficiency of 99.26 %. The proposed control structure is verified, showing that an input current THD of < 5 % can be achieved over a wide range of output currents and that equal current sharing between the ICMCI windings can be achieved, even during output current transients.

In nominal operation about 58 % of the total losses result from the semiconductors and approximately 19 % result from magnetic components. This is similar to other high-efficiency rectifiers, for example, in the > 99 % efficient VIENNA Rectifier presented in [136] semiconductors cause 69 % of the losses and inductors cause 30 %. For the buck-type PFC rectifier in [127] semicon-

ductor losses of 74 % and magnetic component losses of 13 % are reported. In [144] semiconductor losses of 71 % and inductor losses of 17 % are reported for a single-phase boost-type PFC rectifier.

Further research could address potential benefits regarding efficiency and/or power density which could result from novel wide band-gap semiconductor devices such as monolithic bidirectional gallium nitride (GaN) switches which could be used in the IVS [145, 146].

5

Design and Implementation of a Life-Cycle-Cost-Optimal Integrated Active Filter Rectifier

Due to the increasing power consumption of data centers, efficient dc power distribution systems have become an important topic in research and industry over the last years and according standards have been adopted. Furthermore, the power consumed by telecommunication equipment and data centers is an economic factor for the equipment operator, which implies that all parts of the distribution system should be designed to minimize the life cycle cost, i.e. the sum of first cost and the cost of the power conversion losses. This chapter demonstrates how semiconductor technology, and die area, magnetic component volumes and switching frequency can be selected based on life cycle cost, using analytical and numerical optimizations. A three-phase buck-type PFC rectifier with integrated active filter for 380 V dc distribution systems is used as an example system, which shows that a peak efficiency of 99 % is technically and economically feasible with state-of-the-art SiC MOSFETs and nanocrystalline or ferrite cores. Measurements taken on an 8 kW, 4 kW/dm^3 hardware prototype verify a full-load efficiency of 99.0 %

and demonstrate the design's validity and feasibility.

5.1 Introduction

Information and communication technology equipment has become a significant consumer of electric power in recent years. In 2007, for example, the related annual consumption in Germany alone was 55 TW h, which equaled approximately 10 % of the countries total consumption. The annual power consumption of data centers located in Germany is approximately constant at ≈ 10 TW h since 2008 [147]. For the US, an annual data center power consumption of 60 TW h was estimated in 2006 with an energy cost of $4.5 billion [148], for 2014 an increase to 70 TW h has been reported [100]. Therefore, the cost of electric energy is a significant economic factor for data center operators and should hence be considered in investment decisions.

In conventional data centers using ac distribution systems, as shown in **Fig. 5.1(a)**, up to 50 % of the total energy consumed is used for air conditioning, distribution and conversion losses [93]. Compared to this, distribution systems based on a dc bus with a nominal voltage of 380 V offer significantly higher efficiency, improved reliability and reduced capital cost and floor space, cf. **Fig. 5.1(b)** [92]. Furthermore they allow a direct connection of lead acid batteries, consisting of 168 cells connected in series, with a typical floating cell voltage of ≈ 2.26 V, which results in a nominal bus voltage of 380 V. Accordingly, standards and components for dc distribution systems have been developed in recent years [85, 107].

Normally a boost-type power factor correction (PFC) rectifier stage is used to convert the 400 Vac mains into a dc voltage that is higher than the full-wave rectified ac input voltage, typically in the range of 700 V to 800 V. A subsequent buck converter is then required to connect the PFC rectifier output to the dc distribution bus. This configuration is also used for fast chargers of Electric Vehicle batteries, which are powered from the three-phase ac mains [77]. As an alternative, a single-stage conversion between the three-phase mains and a dc bus with lower voltage can be achieved with buck-type PFC converters, like the SWISS Rectifier, the six-switch buck rectifier or the Integrated Active Filter rectifier [14, 32, 149, 150].

The circuit topology of the Integrated Active Filter (IAF) buck-type PFC rectifier, shown in **Fig. 5.2**, was first introduced in [36] for three-phase solar inverters. A similar circuit was also proposed for drive systems with small dc-link capacitors [41]. Three major blocks can be identified in the IAF rectifier's schematic: an Input Voltage Selector (IVS) built of a line-commutated full-

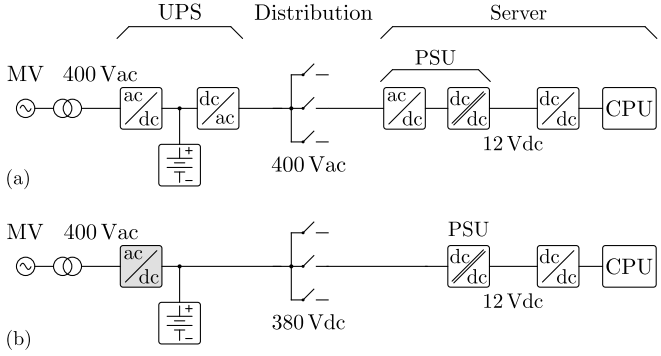

Fig. 5.1: Data center power distribution concepts: **(a)** Conventional 400 Vac distribution, using an ac output Uninterruptible Power Supply (UPS). Similar concepts can be used with 480 Vac. **(b)** Facility level dc distribution system based on a 380 Vdc bus which allows a direct connection of backup batteries [93].

wave diode rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$ and three four-quadrant switches $S_{\bar{k}y\bar{k}}$, a current injection circuit S_{xy}, S_{yz}, L_{inj} and a dc-dc buck converter S_x, D_z, L_o which provides the constant dc output voltage u_{pn}. Typically a small capacitor C'_f is required to ensure a valid conduction path during the commutation of S_{xy}, S_{yz} and S_x. Note that the IVS switches and diodes are commutated at mains frequency only, which implies that almost no switching

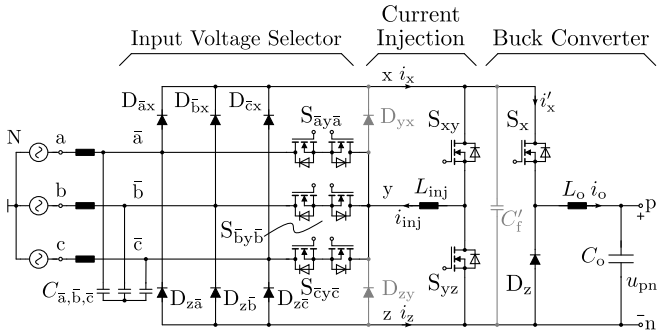

Fig. 5.2: Schematic of the Integrated Active Filter (IAF) rectifier, using an Input Voltage Selector (IVS) commutated at mains frequency, combined with a buck converter providing the output current i_o and a current injection converter which serves as active harmonic filter to achieve sinusoidal ac input currents.

Tbl. 5.1: Converter Specifications

Input Voltage (Line-to-Neutral)	$U_1 = 230\,\mathrm{V}$ rms
Input Frequency	$\omega_1 = 2\pi\,50\,\mathrm{Hz}$
Switching Frequency	$f_{sw} = 27\,\mathrm{kHz}$
Nominal Output Voltage	$U_{pn} = 400\,\mathrm{V}$
Nominal Output Power	$P_o = 8\,\mathrm{kW}$

losses occur in the IVS, therefore rectifier diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ that are optimized for a low forward voltage drop can be used.

For this chapter, the IAF buck-type PFC rectifier was selected to demonstrate a cost-driven converter design approach, as only two line-commutated diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ and one power transistor S_x are in its main conduction path [149, 151]. Based on a short review of the IAF rectifier's main properties in **Section 5.2** and using the capital equivalent worth of energy together with component cost models, a non-isolated 8 kW PFC rectifier is designed in **Section 5.3**. This allows selecting cost-optimal components such as semiconductors and inductors achieving an economically optimal converter, which minimizes life cycle cost, i.e. the sum of first cost of the converter hardware and the cost of conversion losses during the service life. Measurements taken on a hardware prototype are presented in **Section 5.4**.

5.2 Integrated Active Filter PFC Rectifier

Simulation results for an 8 kW IAF buck-type PFC rectifier (cf. **Fig. 5.2**) are shown in **Fig. 5.3**, for the system specifications given in **Tbl. 5.1**. For the IAF rectifier, the current injection circuit and the buck converter can be analyzed, optimized and operated almost independent of each other. As the dc output is provided by the buck converter (S_x, D_z, L_o), the output current i_o and voltage u_{pn} can be controlled independent of the injection circuit. This can be seen from the simulation results in **Fig. 5.3**: During $\omega t < 180°$ the current injection circuit is turned off, i.e. $i_{inj} = 0$. As the buck converter creates a constant output current i_o it consumes constant power from the ac input. Hence non-sinusoidal ac input currents $i_{a,b,c}$ result and only two ac input lines a, b, c conduct current at a time.

For $\omega t > 180°$ the injection circuit is used to create a current i_{inj} that is

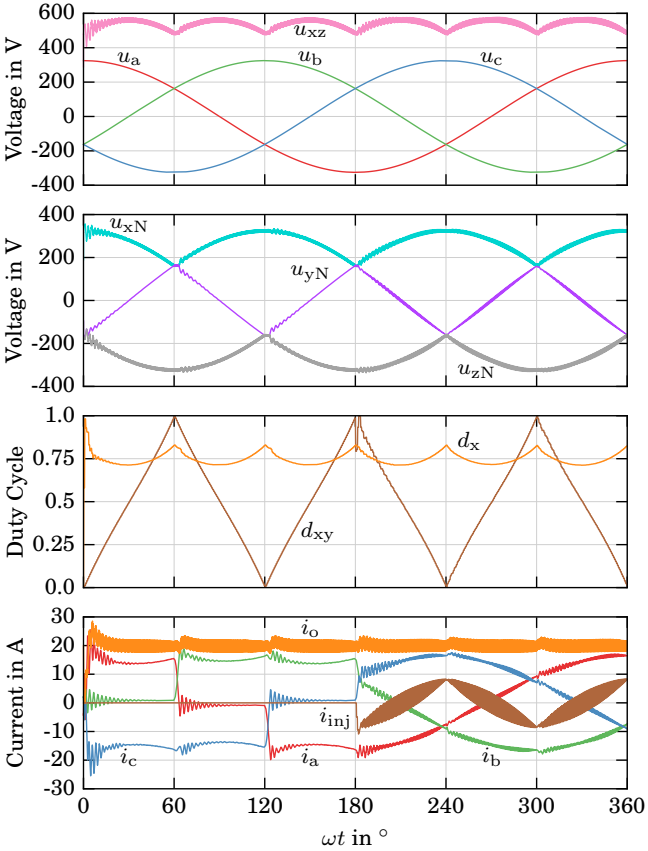

Fig. 5.3: Simulation results for an IAF buck-type PFC rectifier as shown in **Fig. 5.2**. Plotted are the ac input voltages $u_{a,b,c}$, the IVS output voltages u_{xN}, u_{yN} and u_{zN}, the buck stage duty cycle d_x, the duty cycle d_{xy} of switch S_{xy}, the output current i_o, the injection current i_{inj} and the ac input currents $i_{a,b,c}$. During $\omega t < 180°$ the injection circuit is disabled (i.e. $i_{inj} = 0$) which results in non-sinusoidal mains currents $i_{a,b,c}$.

proportional to the voltage u_{yN},

$$i_{inj}(\omega t) = -\hat{I}_1 \frac{u_{yN}(\omega t)}{\hat{U}_1} \quad \hat{I}_1 = \frac{2\,P_o}{3\,\hat{U}_1} \quad , \tag{5.1}$$

where $\hat{I}_1$ is the peak value of the rectifier's ac input line current and $\hat{U}_1$ is the ac line-to-neutral voltage amplitude. This results in sinusoidal ac input currents as shown in **Fig. 5.3**. A more detailed description of the modulation and control strategy can be found in [149], a brief description of the main components is given in the following.

5.2.1 Input Voltage Selector

As described above, the IAF rectifier uses an IVS, which connects each ac input line a, b, c to either node x, y or z. This implies that the voltages u_{xN}, u_{yN} and u_{zN} are piecewise sinusoidal and it allows to move the ac filter capacitors $C_{\bar{a},\bar{b},\bar{c}}$ from nodes $\bar{a}, \bar{b}, \bar{c}$ to nodes x, y, z as shown in **Fig. 5.4**. This shortens the commutation paths of the buck converter and the injection switches. Additionally the diode bridge currents i_x and i_z become continuous, which reduces the conduction losses in the bridge diodes $D_{\bar{k}x}$ and $D_{z\bar{k}}$ and in the four-quadrant switches $S_{\bar{k}y\bar{k}}$. The resulting rms current values can be calculated as

$$I_{D\bar{k}x,rms} = \hat{I}_1 \sqrt{\frac{\sqrt{3}}{8\pi} + \frac{1}{6}} \tag{5.2}$$

and

$$I_{S\bar{k}y\bar{k},rms} = \hat{I}_1 \sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}} \quad . \tag{5.3}$$

Assuming that MOSFETs are used as synchronous rectifiers, as shown in **Fig. 5.4**, the conduction losses are reduced by 31 % in the rectifier bridge and by 78 % in the four-quadrant switches compared to the original circuit shown in **Fig. 5.2** [128].

5.2.2 Buck Converter

It can be seen in **Fig. 5.4** that the buck converter's input is connected to u_{xz}, which is a six-pulse shaped voltage provided by the IVS' rectifier bridge,

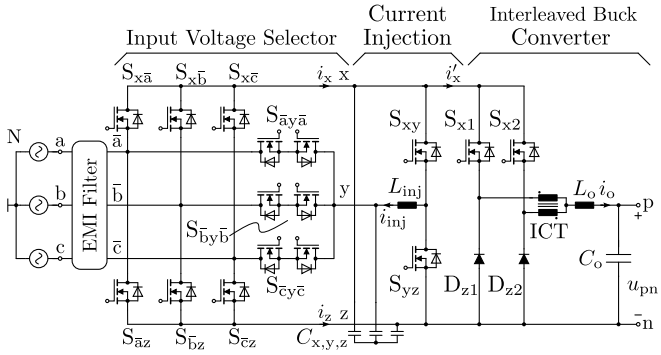

Fig. 5.4: Schematic of the IAF rectifier where the input filter capacitors have been moved from the ac-side (ā, b̄, c̄) of the IVS to its output side (x, y, z), which reduces the conduction losses [128]. The diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ are replaced with SiC MOSFETs $S_{x\bar{k}}$, $S_{\bar{k}z}$ operating as synchronous rectifiers to further increase the efficiency. An interleaved buck converter with cells S_{x1}, D_{z1} and S_{x2}, D_{z2} is used where S_{x1} and S_{x2} are controlled with 180° phase shifted PWM signals. This lowers the current ripple in i'_x which leads to a lower voltage ripple at the input filter capacitors $C_{x,y,z}$. The buck converter output inductors are implemented as an inter-cell transformer (ICT) with closely coupled windings and a single output inductor L_o.

cf. **Fig. 5.3**. Neglecting any voltage drops across the semiconductors and inductors, the dc output voltage u_{pn} can be expressed as

$$u_{pn} = \frac{3}{2}\,\hat{U}_1\, m \quad m \in [0,1] \quad , \tag{5.4}$$

where $\hat{U}_1$ is the ac line-to-neutral voltage amplitude and m is the converter's modulation index. Note that a small distortion of the output current and the mains input currents occurs at every 60° sector of the ac input voltage, i.e. at the intersection of two line voltages $u_{a,b,c}$. This is most likely due to the switching frequency ripple of the filter capacitor voltages u_{xN}, u_{yN}, u_{zN}, as similar disturbances exist in the SWISS Rectifier [128]. This voltage ripple is the result of the buck converter's discontinuous input current i'_x and could be reduced with larger $C_{x,y,z}$. However, as the capacitor voltages u_{xN}, u_{yN}, u_{zN} are piecewise sinusoidal they generate reactive power which is typically limited to 5 % to 10 % of the converter's active power rating.

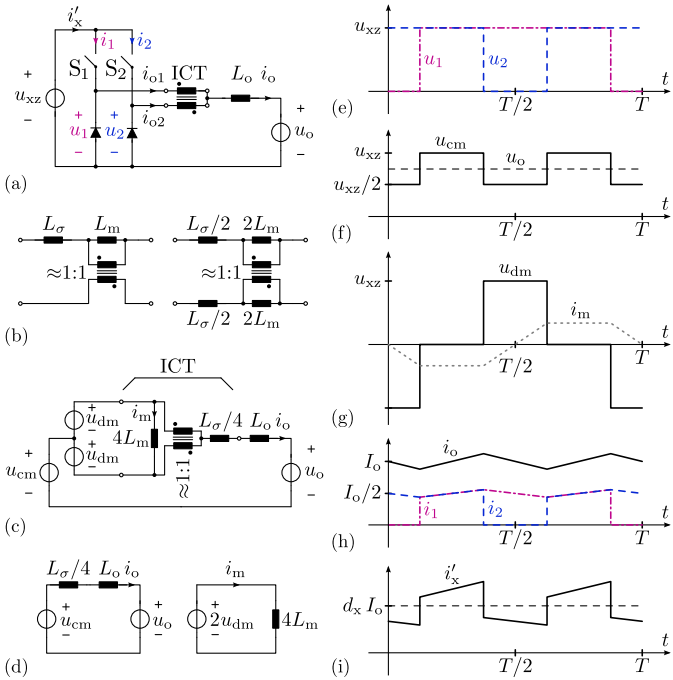

Fig. 5.5: Operating principle of an interleaved buck converter using a close-coupled inter-cell transformer (ICT). **(a)** shows the basic circuit diagram, the switches are controlled with 180° phase shifted PWM signals as shown in **(e)**. Replacing the ICT with the equivalent circuit of a non-ideal transformer as shown in **(b)** and separating voltages u_1 and u_2 into common-mode (cm) and differential-mode (dm) voltages, u_{cm} and u_{dm}, yields the circuit shown in **(c)**. It can be seen that u_{cm} is applied to L_σ and L_o and can be used to control the output current i_o, while u_{dm} defines the ICT's magnetizing current i_m as shown in **(d)**.

5.2.3 Interleaved Buck Converter

In order to reduce the buck converter's input current ripple and hence the mains input current distortions and the electromagnetic noise emission of the rectifier, an interleaved buck converter can be used, as shown in **Fig. 5.4**. By modulating the switches $\mathrm{S}_{\mathrm{x}1}$ and $\mathrm{S}_{\mathrm{x}2}$ with 180° phase shifted PWM signals, the peak-to-peak ripple in i'_x is reduced by approximately a factor of two and the ripple frequency is doubled due to cancellation of harmonics.

The dc output filter of the interleaved buck converter can be implemented

by a combination of an inter-cell transformer (ICT) with closely coupled windings and a single inductor instead of two separate inductors. Using ICTs for interleaved dc-dc converters has been extensively described in literature and has been shown to result in a reduction of the magnetic component's volume, losses and weight [22, 24, 25].

In **Fig. 5.5** the basic operating principle is shown for a duty cycle of $d_x = 0.75$ and 180° phase shifted PWM signals. The two cells S_{x1}/D_{z1} and S_{x2}/D_{z2} produce the output voltages u_1 and u_2 shown in **Fig. 5.5(e)**. These can be transformed into the corresponding common-mode (cm) and differential-mode (dm) voltages, u_{cm} and u_{dm}, cf. **Fig. 5.5(f)-(g)**

$$u_{cm} = \frac{u_1 + u_2}{2} \quad , \tag{5.5}$$

$$u_{dm} = \frac{u_1 - u_2}{2} \quad . \tag{5.6}$$

By replacing the ICT with the equivalent circuit shown in **Fig. 5.5(b)**, the circuit diagram **Fig. 5.5(c)** results, which can be decomposed into two uncoupled circuits as shown in **Fig. 5.5(d)**. It can be seen that the cm voltage u_{cm}, which is applied to the dc output inductor L_o and the ICT's leakage inductance L_σ, switches twice per switching frequency period and has a voltage step height of half the input voltage u_{xz}.

Note that unbalances in the system, such as unequal on-state resistances of the switches, duty cycle differences and mismatched PCB track resistances can lead to unbalanced ICT currents $i_{o1} \neq i_{o2}$. This results in a dc magnetization current of the ICT,

$$i_m = \frac{i_{o1} - i_{o2}}{2} \quad , \tag{5.7}$$

that could lead to a saturation of the core material. However, the dm voltage u_{dm} is applied to the ICT's magnetizing inductance L_m and can be used by an active control circuit to ensure an equal current sharing, $i_{o1} \approx i_{o2}$, in the ICT windings. Strategies for active current balancing control in ICTs have been described in the literature [152, 153].

5.3 Life Cycle Cost Based Converter Design

The design of any power electronic converter is essentially aiming for a best possible overall compromise of multiple trade-offs, which result from couplings between different components concerning their stresses and utilization.

For example, increasing the switching frequency reduces the peak-to-peak flux ripple of magnetic components, which typically leads to smaller and/or more efficient components, but also increases the switching losses of the semiconductors. This in turn requires a larger heat sink and could overcompensate the volume reduction achieved in the magnetic components. Similar trade-offs also exist on the component level, e.g. increasing the number of turns in an inductor decreases the core losses at the expense of increased winding losses. Furthermore, even for a given fixed switching frequency multiple combinations of volumes or sizes of the different components can lead to similar power densities and efficiencies. Designing an optimal converter becomes even more challenging, if more than a single circuit topology and/or several different core and winding materials are taken into account. Due to these trade-offs, a single optimal converter can typically not be found, but rather a range of Pareto-optimal designs can be calculated that achieve, for example, the highest efficiency for a given power density and vice versa.

These trade-offs can be simplified by introducing a single-valued objective function such as life cycle cost (LCC). As described in [133] and [103], the capital equivalent worth of one Watt of continuous dissipation can be used to select components in order to minimize the LCC of that component. Combined with cost models, the switching frequency, semiconductors and magnetic components are selected to achieve minimal LCC for a given service life time assuming continuous operation at rated power, as will be shown in the following for the IAF rectifier [135].

Given some basic economic parameters, such as interest and inflation rates, the capital-equivalent worth of a continuously dissipated Watt of ac power can be estimated. In 2008 the authors of [133] estimated an average value of \$14 per Watt for the US market and 15 years of service life, which implies that up to \$14 could be invested now in order to reduce the equipment's power consumption by one Watt over the next 15 years. Although the prices for electric power show a considerable geographical variation (approximately a factor of 5 in the US), the authors conclude that the cost of dissipation significantly overshadows the first cost for telecom power supplies.

5.3.1 Semiconductor Technology Comparison

An example calculation for the IVS full-wave rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ / $S_{x\bar{k}}$, $S_{\bar{k}z}$ is shown in **Fig. 5.6**, where a capital equivalent worth of $\gamma = \text{EUR } 0.12$ per kW h is assumed. Neglecting switching losses in the IVS, the device losses can be directly determined from the rms and average currents found by numerical

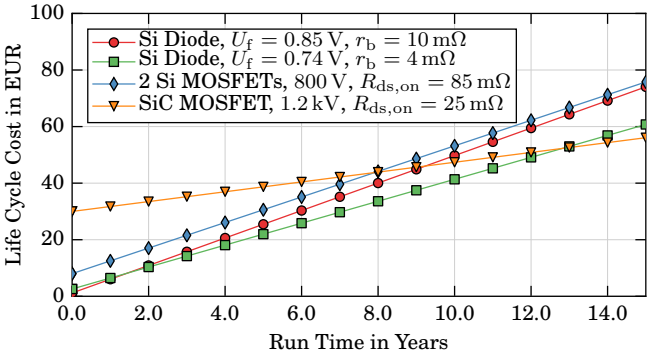

Fig. 5.6: Comparison of LCC for different implementations of the diode bridge rectifier $D_{\overline{kx}}$, $D_{z\overline{k}}$ of the IVS with $I_{rms} = 8.1\,A$, $I_{avg} = 4.6\,A$ ($P_o = 8\,kW$) and a capital equivalent worth of EUR 0.12 per kW h [133]. Switching losses are neglected as the IVS switches commutate at twice the mains frequency only. It can be seen that the significantly higher first cost of a SiC MOSFET is compensated by the reduced conduction losses of the device, achieving roughly the same LCC as Si diodes and Si MOSFETs for run times of approximately ten years, assuming continuous operation at rated power.

simulation, resulting in $I_{rms} = 8.1\,A$ and $I_{avg} = 4.6\,A$ for an 8 kW system. Assuming a service life time of 10 years or more, a SiC MOSFET with a high initial cost of approximately EUR 30 and low on-state resistance achieves the same or lower LCC than conventional Si diodes with an initial cost of EUR 2.6. The same holds for a parallel connection of two Si MOSFETs with a first cost of approximately EUR 8. Note that all devices are operated far below their thermal limits, e.g. 1.7 W of conduction losses result for the SiC MOSFTEs and $\approx 4\,W$ for the Si diodes and Si MOSFETs, but all devices are rated for more than 100 W of continuous power dissipation.

5.3.2 Semiconductors without Switching Losses

The calculation shown in **Fig. 5.6** is based on a selection of standard semiconductor devices, which might not achieve the lowest possible LCC. Using more than one device in parallel reduces the total on-state resistance $R_{DS(on)}$ of MOSFETs or the (differential) bulk resistances r_b of diodes, which lowers the conduction losses. This reduces the cost of dissipation during system operation, but increases the first cost as more devices are used, which implies that the resulting LCC is a function of the number n of devices used in parallel.

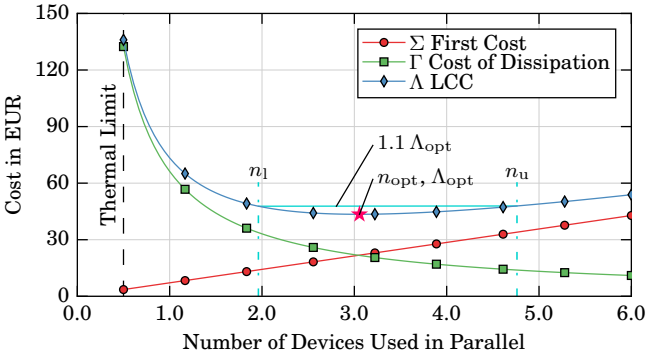

Fig. 5.7: First cost, cost of dissipated energy and LCC as a function of the number of devices connected in parallel for the rectifier bridge $S_{x\bar{k}}$, $S_{\bar{k}z}$ at nominal operation with $I_{\mathrm{rms}} = 8.1\,\mathrm{A}$ ($P_{\mathrm{o}} = 8\,\mathrm{kW}$). A SiC MOSFET with $R_{\mathrm{DS(on)}} = 96\,\mathrm{m\Omega}$ and a cost of EUR 7.14 is considered as unit device, together with a capital equivalent worth of $\gamma =$ EUR 0.12 per kW h and a run time of $t_{\mathrm{r}} = 10$ years.

For a MOSFET, continuously conducting the current I_{rms} for the run time t_{r} without switching losses, the corresponding LCC Λ can be expressed as

$$\Lambda_{\mathrm{M}}(n) = \underbrace{\gamma\, t_{\mathrm{r}}\, \frac{R_{\mathrm{DS(on)}}}{n}\, I_{\mathrm{rms}}^2}_{\text{Cost of Dissipation, } \Gamma_{\mathrm{M}}} + \underbrace{\sigma_{\mathrm{M}}\, n}_{\text{First Cost, } \Sigma_{\mathrm{M}}} , \tag{5.8}$$

where σ_{M} is the cost of a single MOSFET with an on-state resistance $R_{\mathrm{DS(on)}}$. A plot of the resulting values for $t_{\mathrm{r}} = 10$ years, $R_{\mathrm{DS(on)}} = 96\,\mathrm{m\Omega}$ and $\sigma_{\mathrm{M}} =$ EUR 7.14 is shown in **Fig. 5.7**. For a given t_{r}, the optimal number of devices n_{opt} that achieves minimal LCC, can be derived by minimizing (5.8) with respect to n as

$$n_{\mathrm{opt}} = \sqrt{\gamma\, t_{\mathrm{r}}\, \frac{R_{\mathrm{DS(on)}}}{\sigma_{\mathrm{M}}}}\, I_{\mathrm{rms}} , \tag{5.9}$$

$$\Gamma_{\mathrm{M,opt}} = \Sigma_{\mathrm{M,opt}} = \sqrt{\gamma\, t_{\mathrm{r}}\, R_{\mathrm{DS(on)}}\, \sigma_{\mathrm{M}}}\, I_{\mathrm{rms}} , \tag{5.10}$$

$$\Lambda_{\mathrm{M,opt}} = \Gamma_{\mathrm{M,opt}} + \Sigma_{\mathrm{M,opt}} = 2\sqrt{\gamma\, t_{\mathrm{r}}\, R_{\mathrm{DS(on)}}\, \sigma_{\mathrm{M}}}\, I_{\mathrm{rms}} . \tag{5.11}$$

Note that a certain minimum n_{min} exists due to the thermal limits of the device and the cooling system as indicated in **Fig. 5.7**. However, even for short run times of $t_{\mathrm{r}} \approx 1$ year the optimal n is typically larger than n_{min}.

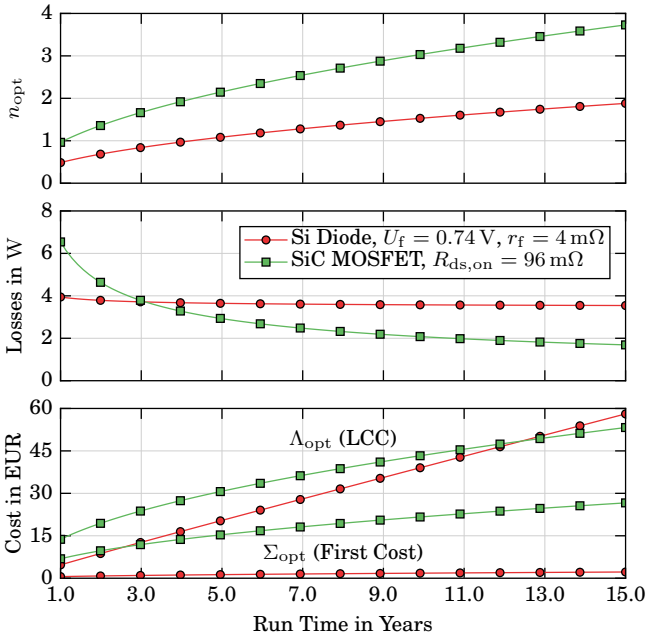

Fig. 5.8: Optimization results for Si Diodes and SiC MOSFETs showing the optimal (lowest LCC) number of parallel devices, resulting device losses, first cost and LCC as a function of the run time t_{r} in years. The same parameters as in **Fig. 5.7** are used.

This optimization can be extended from MOSEFTs to diodes modeled by a constant forward voltage drop U_{f} connected in series with a (differential) bulk resistance r_{b} as

$$\Lambda_{\mathrm{D}}(n) = \gamma\ t_{\mathrm{r}}\ \frac{r_{\mathrm{b}}}{n}\ I_{\mathrm{rms}}^2 + \gamma\ t_{\mathrm{r}}\ U_{\mathrm{f}}\ I_{\mathrm{avg}} + \sigma_{\mathrm{M}}\ n\ . \tag{5.12}$$

In this case n_{opt} does not depend on U_{f}, however the losses and hence the cost of dissipation Γ increases. An example calculation for different run times is shown in **Fig. 5.8**, where a 96 mΩ SiC MOSFET and a Si diode with $U_{\mathrm{f}} = 0.74\,\mathrm{V}$ and $r_{\mathrm{b}} = 4\,\mathrm{m\Omega}$ are considered as unit elements. For both, MOSFETs and diodes the optimal n increases proportional to $\sqrt{t_{\mathrm{r}}}$, however, for Si diodes, the resulting losses show little variation due to U_{f}. As the first cost of the considered diode is ≈ 6 times lower than the MOSFET's first cost, the Si diodes achieves lower LCC for small t_{r}, while the SiC MOSFET achieves lower LCC for $t_{\mathrm{r}} \geq 12.5$ years.

5.3.3 Device Selection

So far, n has been assumed as a real number that has to be rounded to the next integer or to the next $R_{\mathrm{DS(on)}}$ value available from the device manufacturer. This leads to a suboptimal LCC, but it can seen in **Fig. 5.7** that $\Lambda(n)$ is flat around the optimum. If a certain allowed increase α in LCC is assumed, a resulting lower and upper bound (n_l, n_u) for permissible values of n can be calculated using (5.8) as

$$n_\mathrm{l}(\alpha) = n_\mathrm{opt}\left(1+\alpha-\sqrt{(1+\alpha)^2-1}\right) , \tag{5.13}$$

$$n_\mathrm{u}(\alpha) = n_\mathrm{opt}\left(1+\alpha+\sqrt{(1+\alpha)^2-1}\right) . \tag{5.14}$$

To derive the required granularity of n, the ratio r_n of n_u and n_l can be calculated,

$$r_\mathrm{n}(\alpha) = \frac{n_\mathrm{u}(\alpha)}{n_\mathrm{l}(\alpha)} , \tag{5.15}$$

which does not depend on any device specific parameters in (5.8) and results in a value of 2.43 for $\alpha = 0.1$ (also shown in **Fig. 5.7**). This implies that the achievable LCC is at most 10 % higher than the theoretical optimum, if the ratio between two consecutive $R_{\mathrm{DS(on)}}$ values of the available devices is 2.4 or less.

5.3.4 Switching Losses

In the derivation (5.9), which gives the LCC optimal number of devices, it was assumed that switching losses can be neglected, which is typically not the case for the half-bridge $\mathrm{S_{xy}}$, $\mathrm{S_{yz}}$ used in the current injection circuit. The calculation can be extended by fitting a second-order polynomial to measured hard switching losses (turn-on and turn-off) for the switched voltage,

$$E_\mathrm{sw}(I_\mathrm{sw}) \approx E_0 + E_1 I_\mathrm{sw} + E_2 I_\mathrm{sw}^2 , \tag{5.16}$$

where I_sw is the switched current. Switching losses measured in [135] for a half-bridge of two *C2M0080120* SiC MOSFETs and 600 V dc-link voltage at various I_sw are shown in **Fig. 5.9**, together with a second-order polynomial fitted by least squares regression. If n devices are used in parallel with equal

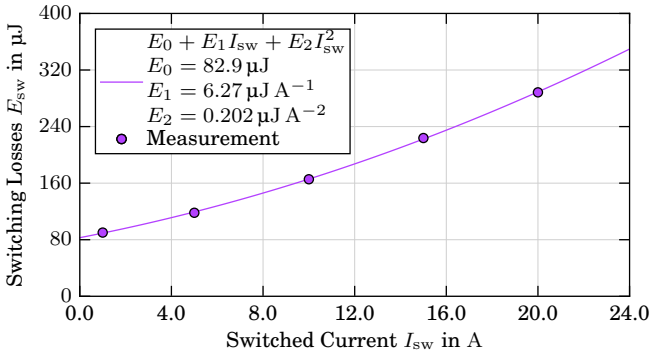

Fig. 5.9: Sum of turn-on and turn-off losses E_{sw} measured in [135] as a function of the switched current I_{sw} for a half-bridge of *C2M0080120* SiC MOSFETs with 600 V dc-link voltage at 25 °C. Additionally a second-order polynomial function fitted by least squares regression is shown and the fitted parameters are given in the legend.

current sharing and neglecting the switching frequency current ripple in the inductor, the total switching losses can be calculated as

$$E_{sw} \approx n \left[E_0 + E_1 \frac{I_{sw,avg}}{n} + E_2 \left(\frac{I_{sw,rms}}{n} \right)^2 \right] , \tag{5.17}$$

where $I_{sw,avg}$ and $I_{sw,rms}$ are the average and rms values of the switched current over one mains voltage period. It can be seen that the terms in (5.17) have the same dependency on n as those in (5.8), which implies that the optimal number of devices which achieves minimal LCC for a given f_{sw} can be approximated as

$$n_{opt} = \sqrt{\gamma\, t_r \frac{R_{DS(on)}\, I_{rms}^2 + f_{sw}\, E_2\, I_{sw,rms}^2}{\sigma_M + \gamma\, t_r\, f_{sw}\, E_0}} . \tag{5.18}$$

The resulting n_{opt}, first cost Σ_{opt} and LCC Λ_{opt} for the injection switches S_{xy}, S_{yz} are shown in **Fig. 5.10** as function of the switching frequency f_{sw}. It can be seen that n_{opt}, and therefore also Σ_{opt}, decreases with f_{sw}, while the cost of dissipation Γ increases, mainly due to the switching losses.

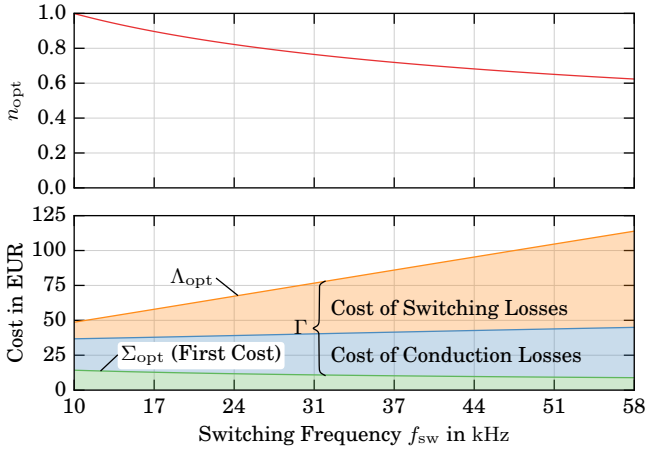

Fig. 5.10: LCC Λ and optimal number of MOSFETs in parallel n_{opt} for a half-bridge built with *C2M0080120* devices for the injection switches S_{xy} and S_{yz} with an rms current $I_{rms} = I_{sw,rms} = 4.7\,A$ and an average switched current of $I_{sw,avg} = 4.1\,A$ as a function of the switching frequency for $t_r = 10$ years.

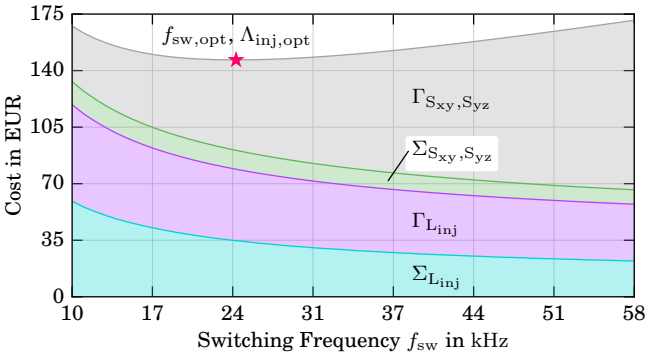

Fig. 5.11: Example showing the selection of a switching frequency f_{sw} that achieves the lowest sum of LCC for the injection switches S_{xy}, S_{yz} and the corresponding inductor L_{inj} for $t_r = 10$ years, not considering any other components of the rectifier.

5.3.5 Magnetic Components

The dimensioning of magnetic components is performed with a similar algorithm, but different to semiconductor devices analytical solutions can typically not be found. For a given f_{sw}, the current and voltage stresses created by the converter can be determined and for a selected core material, shape and size the optimal number of turns, which minimizes the sum of core and winding losses, can be determined by numerical optimization methods. Using the losses and cost models for core and winding materials the inductor's LCC is calculated, which allows the selection of an optimal core size achieving minimal LCC for the given f_{sw} and t_r.

5.3.6 Optimal Switching Frequency Selection

Once the optimal LCC of semiconductors and magnetic components have been calculated as a function of f_{sw}, these can be added in order to select a switching frequency which achieves the lowest total LCC. An example calculation for the injection circuit with the switches S_{xy}, S_{yz} and the inductor L_{inj} is shown in **Fig. 5.11**. It can be seen that the inductor's first cost $\Sigma_{L_{inj}}$ and cost of dissipation $\Gamma_{L_{inj}}$ and hence its LCC, decrease with increasing f_{sw} as opposed to the increasing LCC of the semiconductors, resulting in an optimal f_{sw}. A total run time of $t_r = 10$ years is assumed in this example.

5.3.7 Global Optimization Algorithm

In a final step, the algorithm outlined above can be extended to include the entire rectifier to determine the optimal f_{sw} and all optimal component sizes by minimizing the system's LCC,

$$\Lambda_{sys,opt}(t_r) = \min_{f_{sw}} \sum_k \Lambda_{k,opt}(f_{sw}, t_r) \,. \tag{5.19}$$

The design procedure sweeps over all relevant switching frequencies f_{sw} and considered run times t_r, where for each tupel (f_{sw}, t_r) and all components k (e.g. switches, inductors, etc.) of the system an optimal relative size $n_{k,opt}$ can be determined that achieves minimal LCC $\Lambda_{k,opt}$ for component k. This implies that all components can be designed independent of each other, which simplifies the optimization procedure. Once all components have been selected, their LCC can be summed up, yielding the system's LCC for the considered (f_{sw}, t_r). Once all designs have been calculated, the switching

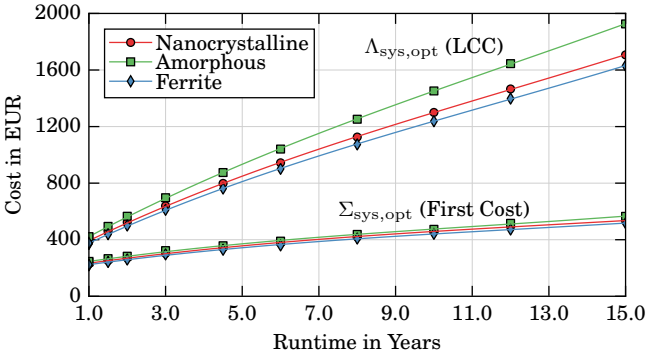

Fig. 5.12: Minimal achievable LCC and according first cost of optimal converter designs as a function of run time for different inductor core materials. It can be seen that for a run time of ten years, the first cost is $< 30\,\%$ of the total LCC. The optimization results in similar first costs for all three core materials, however the LCC of designs with ferrite and nanocrystalline inductors is slightly lower compared to solutions with amorphous cores.

frequency achieving lowest overall LCC is selected for each t_r considered in the analysis.

5.3.8 Auxiliary Components

The losses, volumes and costs of other components, such as gate drive circuits, DSP/FPGA, capacitors, PCBs, heat sinks, fans, EMI filter, etc. have to be considered as well. While their contribution to the overall converter volume, and LCC can be significant, they are almost independent of the design point in the considered application. Therefore, these auxiliary components have been considered in the design, but they were not part of the optimization.

5.3.9 Optimization Results

Fig. 5.12 shows the achievable minimal LCC $\Lambda_{\mathrm{sys,opt}}(t_\mathrm{r})$ and the resulting first cost $\Sigma_{\mathrm{sys,opt}}(t_\mathrm{r})$ as a function of run time calculated by the optimization outlined above. It can be seen that the first cost of the optimal systems is less than 30 % of the total LCC for a run time of 10 years or more. Furthermore, the LCC is comparable for all three core materials considered in the optimization. Designs using amorphous cores are expected to have slightly higher LCC

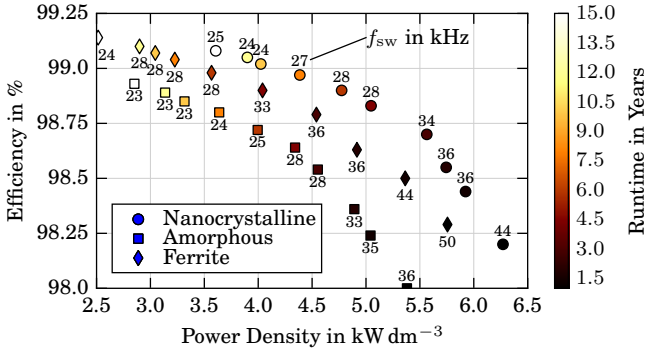

Fig. 5.13: Optimization results showing power density, efficiency and switching frequency f_{sw} of designs achieving minimal LCC for different run times and inductor core materials of ICT, L_{inj} and L_o.

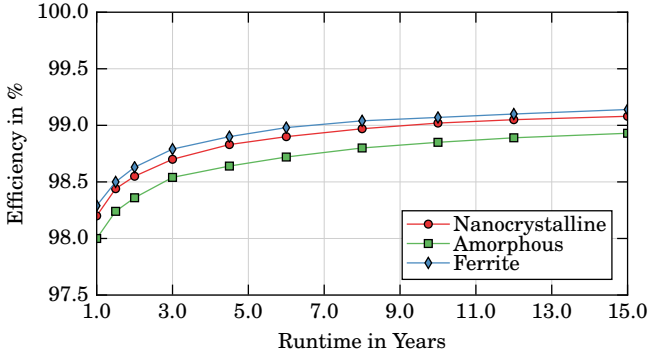

Fig. 5.14: Calculated efficiencies of LCC optimal converter designs for different run times and core materials.

than systems with nanocrystalline or ferrite cores, which is due to the higher core losses of amorphous materials.

However, the volumes and switching frequencies of the designed converters differ significantly as shown in **Fig. 5.13**; the resulting efficiency as function of t_r is shown in **Fig. 5.14**. For short run times ($\leq$ 2 years) converters with high switching frequencies and high power densities achieve minimal LCC as opposed to long run times ($\geq$ 10 years), where designs with approximately half the switching frequency, twice the volume and half the losses

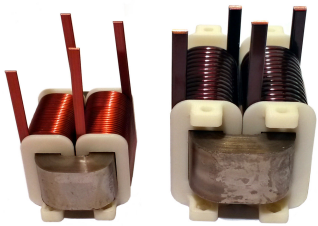

Fig. 5.15: Picture of L_{inj} and L_{o}, implemented using nanocrystalline C cores and helical windings. A boxed volume of 88 cm^3 and 249 cm^3 results for the two inductors. The specifications and parameters of the implemented inductors are given in **Tbl. 5.2**.

result. Furthermore, these results show that very high efficiencies of up to 99 % are economically feasible with available state-of-the-art SiC switches and core materials. Note that three-phase rectifiers based on Si and SiC MOSFETs with slightly lower efficiencies have been reported in the literature [127, 154], however without considering cost.

5.3.10 Selected Design

Based on the numerical optimization results the design point with $t_{\mathrm{r}} = 10$ years, $f_{\mathrm{sw}} = 27\,\mathrm{kHz}$, a power density of $4.0\,\mathrm{kW/dm^3}$ and an efficiency of 99 % was selected to implement a hardware prototype. *FINEMET* nanocrystalline cores with helical windings (cf. **Fig. 5.15**) are used, as they achieve considerably higher power density compared to designs based on ferrite. Detailed results of the optimization are shown in **Fig. 5.16**: for systems with a run time of 10 years or more, it can be seen that the semiconductors and heat sinks contribute about half of the first cost, LCC and losses, but only about 10 % to 20 % of the total volume. Furthermore, the auxiliary components, such as PCBs, gate drivers, FPGA/DSP etc. have a significant contribution to both first cost and life cycle cost, which implies that they cannot be neglected in the design process.

5.4 Hardware Prototype

Using the optimization results presented in the previous chapter, an 8 kW, prototype IAF rectifier with a switching frequency of $f_{\mathrm{sw}} = 27\,\mathrm{kHz}$, according to the specifications given in **Tbl. 5.1**, was implemented. A picture of the hardware is shown in **Fig. 5.17** and its main components are listed in **Tbl. 5.2**.

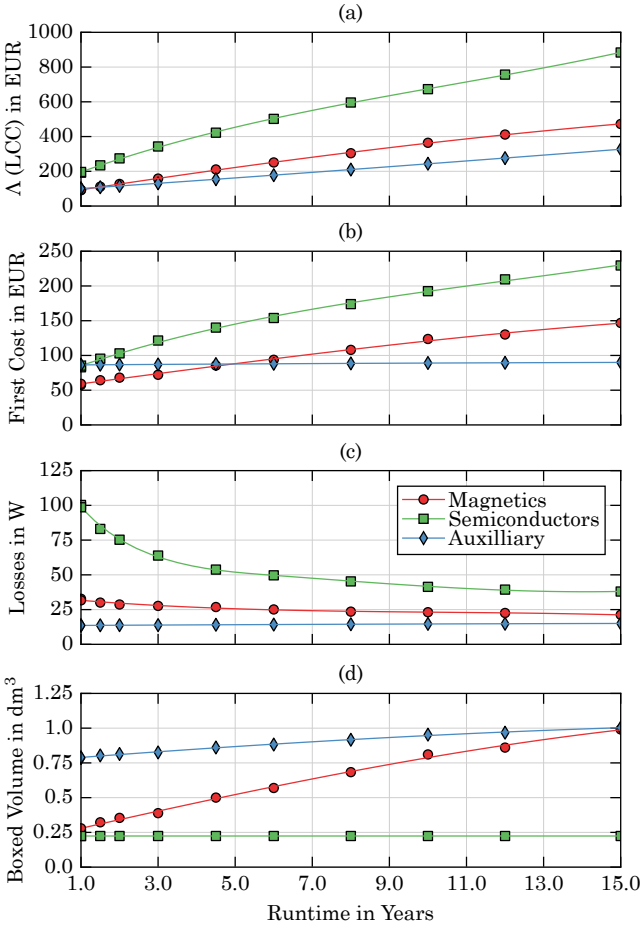

Fig. 5.16: Spline interpolated results of the numerical optimization (markers) for the semiconductors (incl. heatsinks), magnetics and remaining components (e.g. fans, gate drivers, PCBs, DSP/FPGA, capacitors, EMI filter) of the circuit shown in **Fig. 5.4**. Nanocrystalline cores with helical windings are used for all magnetic components as they offer the best performance in this case, cf. **Fig. 5.13**. Plot **(a)** shows the optimal LCC $\Lambda(t_\mathrm{r})$, **(b)** shows the corresponding optimal first cost $\Sigma(t_\mathrm{r})$, **(c)** the losses occurring in the components and **(d)** their boxed volume. It can be seen that the semiconductors contribute about half of the first cost and losses and hence the life cycle cost, but only $\approx 10\,\%$ to $20\,\%$ of the total converter volume.

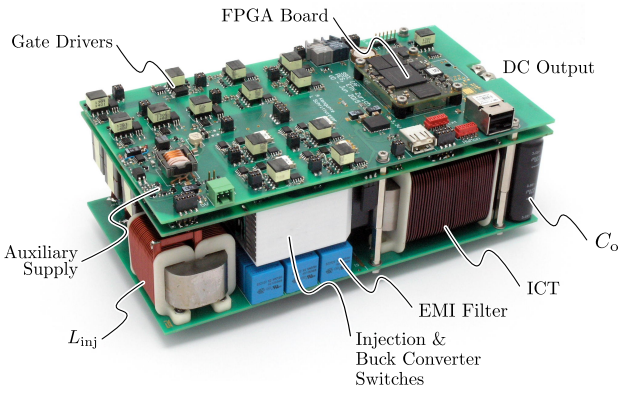

Fig. 5.17: Picture of the hardware prototype, measuring 220 mm x 118 mm x 77 mm (8.66 in x 4.65 in x 3.03 in). This results in a power density of 4.0 kW/dm^3 (65 W/in^3).

More detailed distributions of the calculated component losses for the implemented prototype at nominal operating conditions and of the corresponding component volumes are shown in **Fig. 5.18**. About 50 % of the total losses occur in the semiconductors. Core and winding losses in the main magnetic components L_o, *ICT* and L_{inj} account for ≈ 22 % of the total losses.

Tbl. 5.2: Components used in the Hardware Prototype

	L_{inj}	ICT	L_o
Core	F3CC-6.3	F3CC-25	F3CC25
Wire	1 x 4 mm	1 x 6 mm	2.4 x 6 mm
Turns	52	36:36	30
Inductance	750 µH	3 mH	300 µH
Volume	88 cm^3	245 cm^3	249 cm^3
Losses	4.8 W	6.7 W	5.5 W
$S_{x\bar{k}}$, $S_{\bar{k}z}$	C2M0025120		P_{loss} = 1.7 W
$S_{\bar{k}y\bar{k}}$	C2M0080120		P_{loss} = 0.8 W
S_{xy}, S_{yz}	C2M0080120		P_{loss} = 2.3 W
S_{x1}, S_{x2}	C2M0025120		P_{loss} = 6.3 W
D_{z1}, D_{z2}	C4D40120D		P_{loss} = 2.7 W

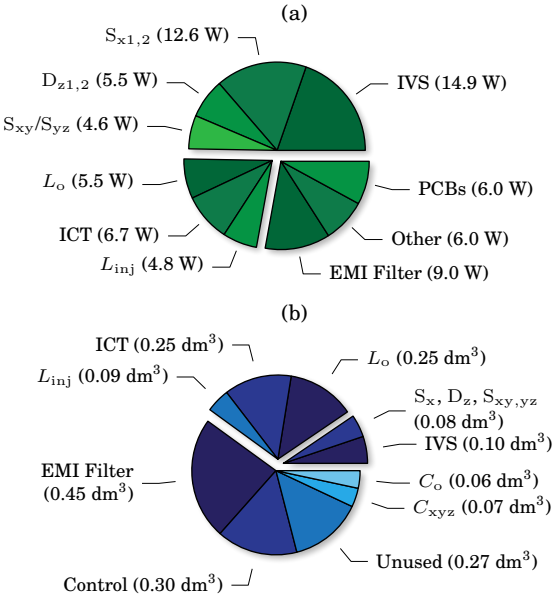

Fig. 5.18: The calculated distribution of losses for the selected design point at nominal operation is shown in **(a)**, the corresponding component volumes are shown in **(b)**. Category *other* includes fans, gate drivers, FPGA, ADCs, current sensors, auxiliary supply, etc.

The remaining 28 % occur in the EMI filter, the PCB tracks, and *other* elements such as fans, gate drivers, FPGA, current sensors etc. Measurement results of the prototype converter are presented in the following.

5.4.1 AC Input Currents

In **Fig. 5.19** measurement results of the prototype rectifier operated at full-load and nominal input voltage are shown. Sinusoidal input currents with slight distortions at the mains voltage sector boundaries result, as expected from simulation. The measured THD of the mains input currents as a function of the dc output power is shown in **Fig. 5.20**.

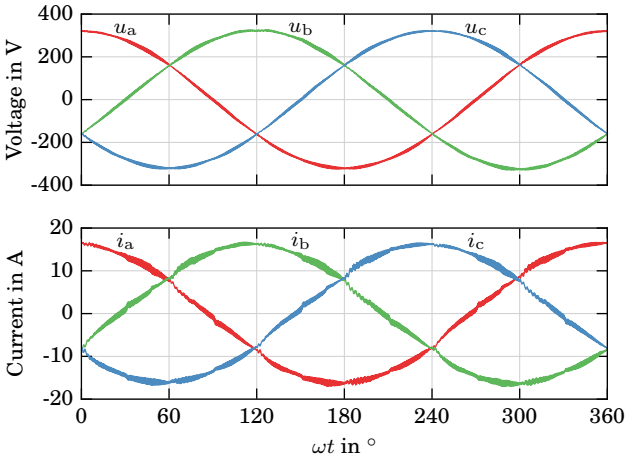

Fig. 5.19: Measurement results with the converter operating at nominal conditions and full output power, i.e. $P = 8\,\mathrm{kW}$, $U_1 = 230\,\mathrm{V_{rms}}$ and $U_{pn} = 400\,\mathrm{V}$. Note that phase quantities a and c were measured directly, quantities of line b were recreated numerically as $u_b = -u_a - u_c$ and $i_b = -i_a - i_c$.

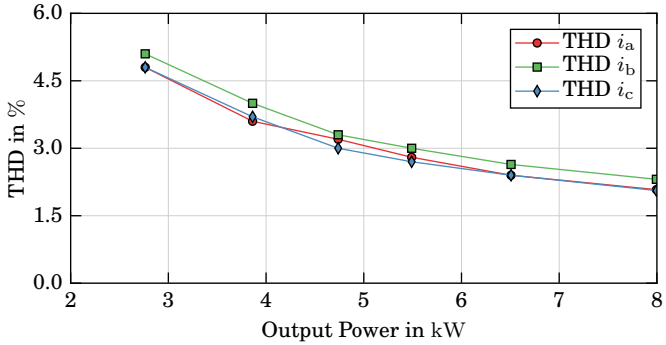

Fig. 5.20: Total harmonic distortion (THD) values of the rectifier's mains input line currents as function of output power for nominal input and output voltages, measured using a *Yokogawa WT 3000* power analyzer.

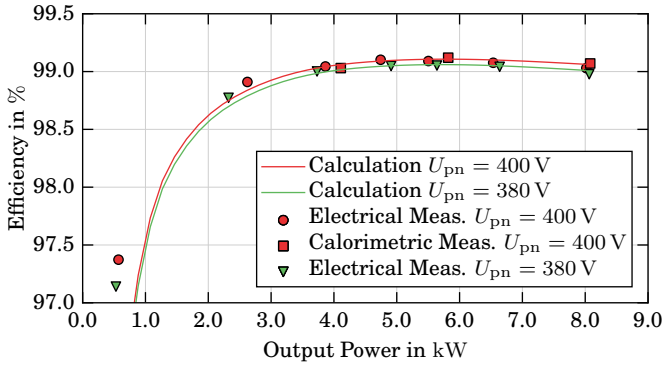

Fig. 5.21: Comparison of measured and calculated converter efficiencies for two different dc output voltages U_{pn}. The electrical efficiency measurements were performed with a *Yokogawa WT 3000* power analyzer. For $U_{\mathrm{pn}} = 400\,\mathrm{V}$ additional measurements were done using a calorimeter. All measurements were taken at nominal ac input voltage $U_1 = 230\,\mathrm{V_{rms}}$ and an ambient temperature of 30 °C.

5.4.2 Efficiency

A comparison of the rectifier's calculated and measured efficiency as a function of dc output power is shown in **Fig. 5.21**. The solid lines show the calculated efficiencies for 400 V and 380 V output voltage, while the round and triangular markers show measurements taken with a *Yokogawa WT 3000* power analyzer. Additionally, three efficiency measurements were taken based on a direct measurement of the converter's losses using a calorimeter, which closely match the values obtained by the electrical measurement.

5.4.3 ICT Current Balance

As written in **Section 5.2.3**, unsymmetries in the interleaved buck converter lead to an unbalance of the ICT currents i_{o1} and i_{o2}, which create a dc offset in the ICT's magnetizing current i_{m}. Measurement results of the buck converter output voltages u_{Dz1}, u_{Dz2}, the ICT currents and the derived magnetizing current are shown in **Fig. 5.22**. Note that no active controller was used to balance i_{o1} and i_{o2}, resulting in a peak magnetizing current of 0.73 A and an average value of 0.42 A. This corresponds to a peak core flux density of $\approx 460\,\mathrm{mT}$, which is far below the core material's saturation flux density of 1.2 T.

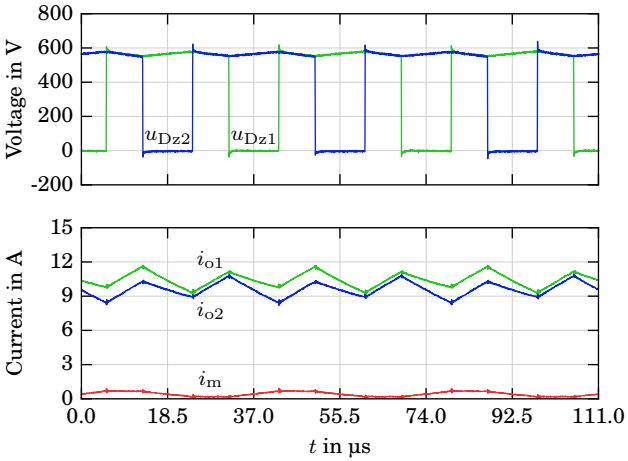

Fig. 5.22: Measurement of the interleaved buck converter output voltages u_{Dz1} and u_{Dz2}, the ICT currents i_{o1} and i_{o2} and the calculated ICT magnetizing current i_m for converter operation with nominal power at $\omega t \approx 0°$, i.e. at the peak of the six-pulse voltage u_{xz} (cf. **Fig. 5.3**) with a peak value of $i_{m,max} = 0.73\,A$.

5.4.4 Conducted EMI

A two-stage EMI filter with a reactive power consumption of $\approx 4\,\%$ of the rectifiers output power rating has been implemented. Its structure is shown in **Fig. 5.23** and the values of all components are listed in **Tbl. 5.3**. However, a detailed analysis of the filter and of its design process is out of the scope of this chapter. Measurement results of the conducted EMI noise spectrum, using the quasi-peak detector, are shown in **Fig. 5.24** together with the CISPR 11 Class B limit for the 150 kHz to 30 MHz range.

5.5 Summary

This chapter describes a life cycle cost (LCC) driven optimization process, where not only the first cost of a converter, but also the capital equivalent worth of the energy dissipated during the system's service life is considered. This allows the selection of optimal components, such as switches, inductors, transformers, etc. that achieve minimal cost for a given application, run time and switching frequency. By sweeping over a range of suitable switching frequencies, a cost-optimal converter system can then be found.

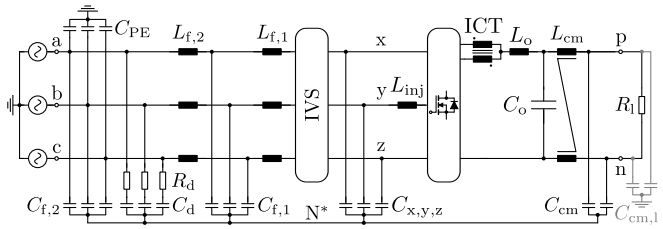

Fig. 5.23: Schematic of the implemented EMI filter with two combined cm/dm filter stages $L_{f,1}$, $C_{f,1}$ and $L_{f,2}$, $C_{f,2}$ at the ac input and an additional cm filter stage L_{cm}, C_{cm} at the dc output. The component values used in the prorotype are listed in **Tbl. 5.3**.

Tbl. 5.3: EMI Filter Components

C_{xyz}	4.4 µF	2 x 2.2 µF Epcos B32923, X2 in parallel
$L_{f,1}$	22 µH	PQ26/25, 10 turns, 1 x 4 mm wire
$C_{f,1}$	2.3 µF	5 x 470 nF Epcos B32922, X2 in parallel
$L_{f,2}$	15 µH	Würth Elektronik 7443641500
$C_{f,2}$	1.4 µF	3 x 470 nF Epcos B32922, X2 in parallel
C_d	0.9 µF	2 x 470 nF Epcos B32922, X2 in parallel
R_d	4.7 Ω	4 x 1 W 1218 SMD thick film resistors
C_{PE}	47 nF	Epcos B3202, Y2, connected to case
L_{cm}	≈ 200 µH	Vacuumschmelze W424, 5 turns, 2.5 mm wire
C_{cm}	130 nF	4 x 33 nF MLCC in parallel

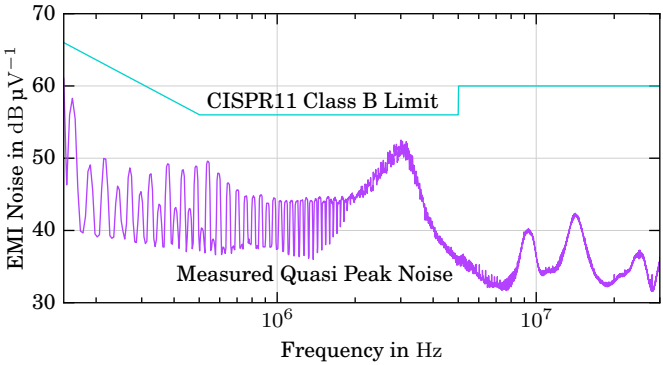

Fig. 5.24: Measured quasi-peak conducted EMI noise emission and corresponding CISPR 11 Class B limit for the 150 kHz to 30 MHz range with a bandwith of 9 kHz, measured in 4 kHz steps.

As an example, an 8 kW buck-type three-phase interleaved IAF rectifier for 380 V dc distribution systems in data center and telecommunication applications is designed. Using state-of-the-art SiC MOSFETs and nanocrystalline cores, a design with a power density of 4 kW/dm^3 and an efficiency of 99 % results. Measurement results taken on a hardware prototype verify the validity of the employed models.

However, the cost driven optimization process is not only useful for data center applications with continuous operation, but could also be used in other applications were the system operates only for a relatively short period of time. For example in an on-board charger of a plug-in hybrid vehicle, which is used only once or twice a day for a few hours, the first cost is expected to contribute a comparably higher share than in data center rectifiers. Similarly, the cost of a power electronic system's weight and volume is expected to be an important factor in aircraft, where weight has an impact on the fuel consumption and hence on the LCC. This is expected to lead to cost-optimal systems with a higher switching frequency, but lower weight and reduced efficiency. In such cases, an equivalent first cost, including weight and/or volume and the cost of conversion losses, can still be used to compare, optimize and select components, circuit topologies and converter systems achieving minimal LCC.

6

Three-Phase Phase-Modular Isolated Matrix-Type PFC Rectifier

Three-phase phase-modular isolated PFC rectifiers are an interesting alternative to phase-integrated three-phase rectifiers as matrix-type phase modules allow a single-stage isolated energy conversion between the three-phase mains and a dc bus. Therefore, this chapter presents a phase-modular isolated matrix-type rectifier, which can be connected to the mains either in star (Y) or delta (Δ) configuration, enabling a wide input voltage range. Additionally, this allows to select the voltage and current stresses of the phase module switches according to the used semiconductor technology; for example 650 V Si or GaN devices could be used in rectifiers powered from the 400 V rms or 480 V rms mains. A detailed analysis of the operating principles and switching behavior of the converter is presented, showing that zero voltage switching (ZVS) can be achieved in the phase modules. Additionally, a third harmonic current injection concept is proposed that allows an up to 15 % higher output voltage in Δ-mode. The concepts are validated with measurements taken on a 7.5 kW, 400 V dc output voltage prototype converter achieving 97.2 % efficiency and a input current THD of < 2 % at rated power.

6.1 Introduction

Today power distribution systems for sensitive equipment, which requires an uninterruptible power supply (UPS), are typically realized with backup batteries. Depending on the application, the batteries are either directly connected to a dc distribution bus or are part of a dedicated ac-ac UPS. Systems with a power level of more than $\approx 3\,\mathrm{kW}$ are typically supplied from the three-phase ac mains through a controlled rectifier, which charges the backup batteries during normal operation. In order to comply with regulations, the rectifier circuits have to achieve near sinusoidal input currents, which are in phase with the mains voltages, i.e. a power factor close to unity is required at the mains interface [42, 155]. Hence these systems are usually called power factor correction (PFC) rectifiers.

As the dc bus voltage is typically a function of the battery's state of charge, the rectifier's output current and voltage have to be controlled and an adaption of the output voltage is required. Furthermore, galvanic isolation between the ac mains and the dc bus is required in certain applications, for example for safety reasons or due to different grounding schemes on ac and dc-side. This can be achieved by cascading a standard three-phase boost-type PFC rectifier, like the VIENNA Rectifier or a six-switch boost rectifier, and a subsequent isolated dc-dc converter. As an alternative, three-phase isolated matrix-type PFC rectifiers have been proposed, which allow a single-stage energy conversion between the three-phase ac mains and a dc bus. Both direct and indirect matrix-type PFC rectifiers, as well as systems based on an integrated active filter, have been analyzed in the literature [36, 50–53, 56, 156, 157].

All topologies mentioned above can be classified as phase-integrated topologies where a network of switches and diodes is used to apply the different line-to-line mains voltages to a single high-frequency isolation transformer. As an alternative, phase-modular topologies have been proposed for both, two-stage [158–161] and matrix-type systems, where three separate phase modules are connected in star or delta at the mains input. In matrix-type systems the switches and diodes [63], and potentially also the transformer and output rectifier as well, are separated into three individual single-phase matrix-type rectifier modules. If individual phase module transformers are used, their ac output voltages can be connected in series [64, 162] or a three-phase configuration together with a three-phase diode rectifier can be used [66]. Alternatively, the secondary-side voltages of the phase module transformers can be rectified individually and then connected either in series [65] or in

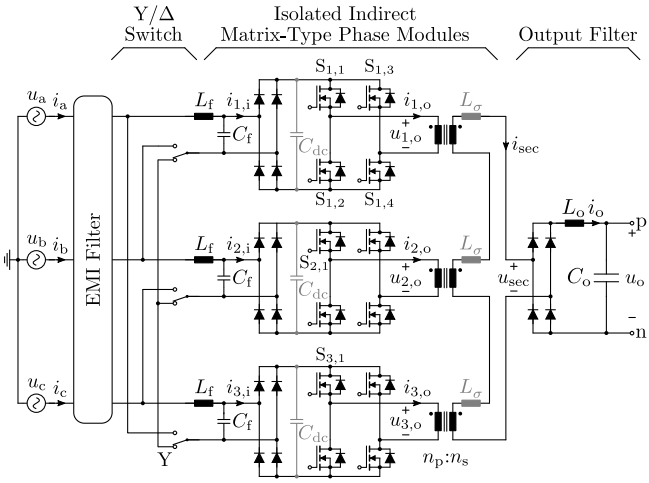

Fig. 6.1: Schematic of the three-phase phase-modular isolated Indirect Matrix-Type Y/Δ (IMY/D) rectifier as proposed in [70].

parallel [67]. If the output rectifier is replaced by switches, no dedicated dc output inductor is required and a quad active bridge converter results that allows bidirectional power flow [71].

In this chapter, the phase-modular indirect matrix-type PFC rectifier system (IMY/D rectifier), introduced in [69, 70] and shown in **Fig. 6.1**, is analyzed in detail. Each phase module consists of an input filter capacitor C_f and potentially an input filter inductor L_f, a full-wave diode rectifier, a full-bridge of switches and an isolation transformer. The secondary-side windings of the phase module transformers are connected in series, yielding the voltage u_{sec}, which is rectified by a full-wave diode bridge and low-pass filtered by the output filter L_o and C_o.

The phase modules shown in **Fig. 6.1** are derived from an indirect matrix converter, which means that the mains input voltage is first rectified by a full-bridge of diodes and then applied to the transformer by a full-bridge of MOSFETs or IGBTs. An additional capacitor $C_{dc} \ll C_f$ is required to provide a valid conduction path during the commutation of the active switches $S_{k,1..4}$. Alternatively, direct matrix-type phase modules (cf. **Fig. 6.2**), which consist of a single full-bridge of bidirectional switches could be used. These switches can, for example, be implemented by an antiseries connection of two MOSFETs, a monolithic bidirectional switch or an antiparallel connection of two reverse-

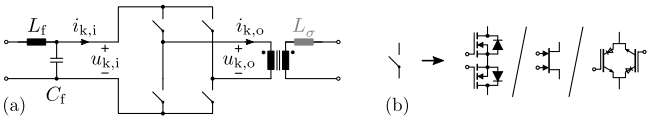

Fig. 6.2: Schematic of a direct matrix-type phase module using an full-bridge of bidirectional switches to directly apply $u_{\mathrm{k,i}}$ to the isolation transformer ($u_{\mathrm{k,o}}$) with alternating polarity. The bidirectional switches can be implemented, for example, by an antiseries connection of two MOSFETs, a monolithic bidirectional GIT [145, 163] or an antiparallel connection of two reverse-blocking IGBTs.

blocking IGBTs.

It can be seen in **Fig. 6.1** that the IMY/D rectifier is a buck-type system, as the last stage of the ac input filter are capacitors (C_f) which are impressing a voltage and as an output inductor (L_o) is connected to the switch network on the dc-side. As three individual transformers are used, the phase modules can be connected to the mains either in star (Y) or delta (Δ) configuration, which allows a wide input voltage range. Note that the individual phase-modules and the isolation transformers have to process a power pulsating with twice the mains frequency due to the single-phase nature of the individual phase modules. However, as matrix-type phase-modules are used, no low-frequency energy storage elements are required. Due to the series connection of the transformers' secondary-side windings, the powers delivered by the three phase-modules add up and the power pulsations with twice the mains frequency cancel as in other three-phase PFC rectifiers. This implies that the output filter does not require any mains frequency energy storage elements either.

The basic modulation and control principles of the IMY/D rectifier are described in **Section 6.2**. Based on these considerations a modified modulation scheme is proposed in **Section 6.3**, which allows ZVS of all phase module inverter switches. Additionally, third harmonic current injection in Δ-mode is analyzed in **Section 6.4**, showing that it allows an up to 15 % higher output voltage. Details of the implemented prototype and measurement results are discussed in **Section 6.5**.

6.2 Basic Principle of Operation

The phase-modularity of the IMY/D rectifier shown in **Fig. 6.1** can be used to derive a modulation strategy achieving sinusoidal input currents that are in

Tbl. 6.1: Electrical Specifications of Example IMY/D Rectifier

Nominal Mains Voltage (Line to Neutral)	$U_1 = 230\,\text{Vrms}$
Mains Frequency	$\omega_1 = 2\,\pi\,50\,\text{Hz}$
Nominal Output Voltage	$U_o = 400\,\text{V dc}$
Nominal Output Power	$P = 7.5\,\text{kW}$
Switching Frequency	$f_{sw} = 72\,\text{kHz}$

phase with the mains voltages

$$\begin{aligned} u_a &= \hat{U}\,\cos(\omega t) \quad , \\ u_b &= \hat{U}\,\cos(\omega t - 2\pi/3) \quad , \\ u_c &= \hat{U}\,\cos(\omega t + 2\pi/3) \quad , \end{aligned} \tag{6.1}$$

resulting in a power factor close to unity. In the following derivation, a Y-connection of the phase modules is assumed.

6.2.1 Modulation

As described above, the IMY/D rectifier consists of three individual phase modules that apply the corresponding rectified ac input voltages to the transformer primary windings. As the secondary-side windings of the transformers are connected in series, the secondary-side current i_{sec} flows through all three secondary-side windings if the output diode bridge is not free-wheeling, i.e. if at least one phase module provides an output voltage $u_{k,o}$ ($k \in \{1, 2, 3\}$) not equal to zero. Neglecting the magnetizing current of the transformers, this implies that the current $i'_o = i_o\, n_s/n_p$ transformed to the primary side flows through all phase modules' full-bridges. Note that the inverter switches $S_{k,1..4}$ in the phase modules have to be operated with 50 % duty cycle and phase shift modulation in order to provide a conduction path for i_{sec} at all times.

Therefore, when a phase-module k is applying its line voltage to its transformer (assuming Y-connection of the phase modules), the current i'_o is drawn from the phase-module's ac input. Assuming a constant dc output current I_o, the local average $\langle i_{k,i} \rangle_{T_s}$ of the phase-module's input current $i_{k,i}$ over one switching frequency period $T_{sw} = 1/f_{sw}$ can be expressed as

$$\langle i_{k,i} \rangle_{T_{sw}} = d_k\, I'_o = d_k\, \frac{n_s}{n_p}\, I_o \quad \forall\, k \in \{1, 2, 3\} \ . \tag{6.2}$$

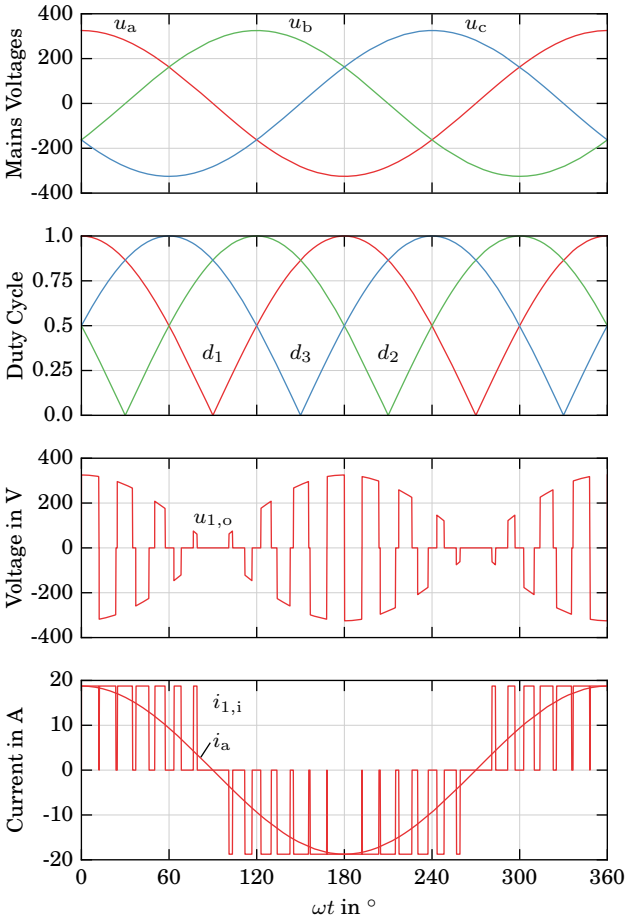

Fig. 6.3: Visualization for low switching frequency of the basic modulation scheme in Y-configuration at maximum modulation index $m = 1$: each phase module produces a square-shaped high-frequency transformer voltage $u_{k,o}$, $k \in \{1, 2, 3\}$, with a duty cycle d_k proportional to its corresponding line voltage $u_{a,b,c}$. Neglecting C_{dc}, a phase module input current $i_{k,i}$ proportional to the duty cycle d_k results. After low-pass filtering the ac input current i_a is obtained.

If sinusoidal duty cycles,

$$\begin{aligned} d_1 &= m\,|\cos(\omega t)|\,, \\ d_2 &= m\,|\cos(\omega t - 2\pi/3)|\,, \\ d_3 &= m\,|\cos(\omega t + 2\pi/3)|\,, \end{aligned} \tag{6.3}$$

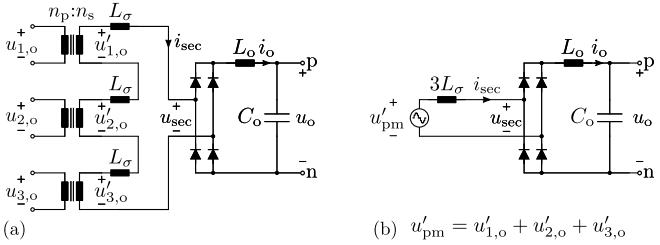

Fig. 6.4: (a) Circuit diagram of the IMY/D rectifier's output stage and **(b)** its equivalent circuit which shows the buck-type structure of the rectifier.

in phase with the ac input line voltages of the phase-modules are used, sinusoidal input currents result after low-pass filtering of the switching frequency components, as shown in **Fig. 6.3**. Note that m is the converter's modulation index and describes the current transfer ratio

$$m = \frac{\hat{I}}{I'_o} = \frac{\hat{I}}{I_o}\,\frac{n_p}{n_s} \quad m \in [0,1]\,, \tag{6.4}$$

where $\hat{I}$ is the amplitude of the ac input line currents.

Due to the series connection of the phase module transformer's secondary-side windings [cf. **Fig. 6.4(a)**], the voltage u_{sec} applied to the dc-side full-bridge diode rectifier can be approximated as

$$u_{sec} \approx \frac{n_s}{n_p}\left(u_{1,o} + u_{2,o} + u_{3,o}\right)\ , \tag{6.5}$$

assuming that the transformers' leakage inductances L_σ can be neglected. As the duty cycles and line voltages vary throughout the mains period, the output voltage pulses of the individual phase modules have different amplitude and width, however, after rectification and low-pass filtering (L_o, C_o) a dc output voltage u_o results which can be calculated as

$$u_o = \langle |u_{sec}| \rangle_{T_{sw}} \approx \frac{3}{2}\,\hat{U}\,\frac{n_s}{n_p}\,m = U_{o,max,Y}\,m\ . \tag{6.6}$$

This shows that the IMY/D rectifier is a buck-type rectifier topology, which implies that a dc output voltage u_o between zero and an upper limit $U_{o,max}$ can be generated. A measurement of the mains voltages and the resulting input currents taken at a prototype converter built according to the specifications in **Tbl. 6.1**, is shown in **Fig. 6.5**.

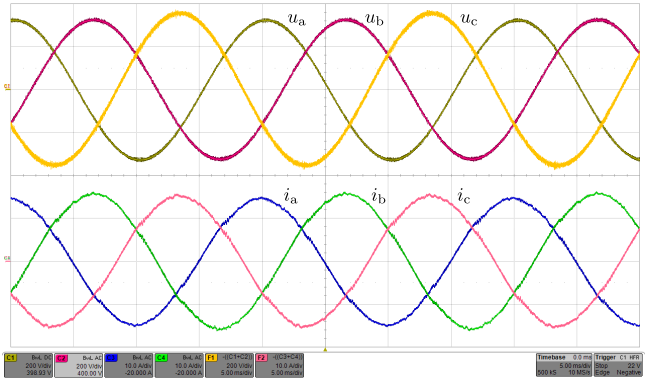

Fig. 6.5: Measurement results: Mains voltages u_a, u_b, u_c (200 V/div, 5 ms/div) and line input currents i_a, i_b, i_c (10 A/div) in Δ-mode at nominal operating conditions specified in **Tbl. 6.1**. Note that the quantities of phases a and b were measured directly while those of phase c are recreated numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$

6.2.2 Control Scheme

A control scheme based on (6.6) and the equivalent circuit shown in **Fig. 6.4** is shown in **Fig. 6.6** and has been explained in [70] and [164]; accordingly, only a brief description follows.

DC Output

The dc output is regulated by two cascaded control loops: an outer voltage controller G_u compares the dc output voltage u_o with its reference u_o^* to determine the output current reference i_o^*. This signal is compared to the measured inductor current i_o by the current controller G_i. By adding the measured output voltage u_o to its output, the desired average rectified secondary-side voltage $\langle |u_{sec}| \rangle_{T_{sw}}^*$ is derived. Dividing by $U_{o,max}$, which is a function of the mains voltage amplitude $\hat{U}$, yields the modulation index m. According to (6.3) m is multiplied with sinusoidal shaping signals derived from the measured ac mains voltages as $u_{a,b,c}/\hat{U} \in [-1;1]$. After adding a zero-sequence modulation signal m_0, the absolute value yields the duty cycle signals $d_{1,2,3}$ used by the phase shift modulators of the three phase-modules.

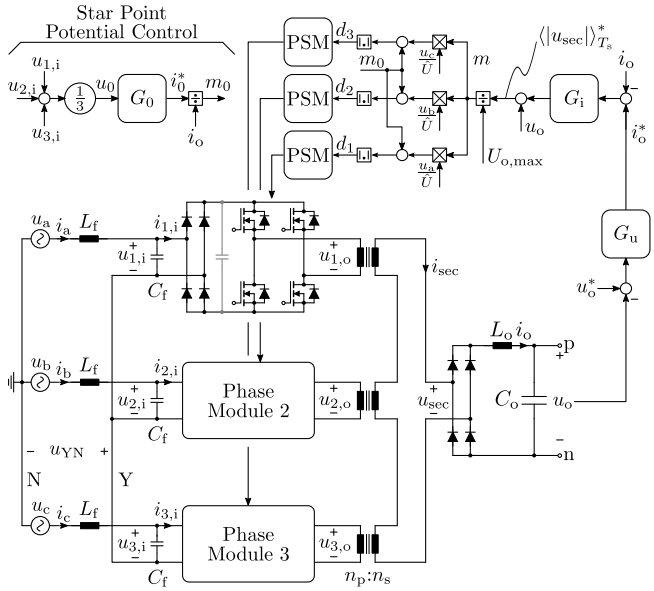

Fig. 6.6: Control block diagram of the IMY/D rectifier: An outer voltage controller G_u derives the reference i_o^* for the inner current controller G_i, which uses the modulation index m to control i_o [164]. If a Y-configuration is used, the potential of node Y (i.e. it voltage w.r.t to the ac mains neutral N, u_{YN}) is controlled by G_0 using a zero-sequence input current reference i_0^*, which yields a zero-sequence modulation index m_0. Three individual phase shift modulators (PSM) are used, each operating the two half-bridges of one phase module with 50 % duty cycle.

Star-Point Potential

In a Y-configuration, as shown in **Fig. 6.6**, the potential of the star-point Y can float with respect to the mains neutral N due to unbalances in the phase module input currents $i_{k,i}$. Assuming that the mains' zero-sequence voltage can be neglected, the voltage u_{YN} between nodes Y and N can be estimated as the zero-sequence component of the measured phase module input capacitor voltages,

$$u_{YN} \approx u_0 = \frac{1}{3}\left(u_{1,i} + u_{2,i} + u_{3,i}\right) \quad . \tag{6.7}$$

A controller G_0 is used to derive the zero-sequence current i_0^* necessary to keep u_0 close to zero. Dividing this reference by the output current i_o yields

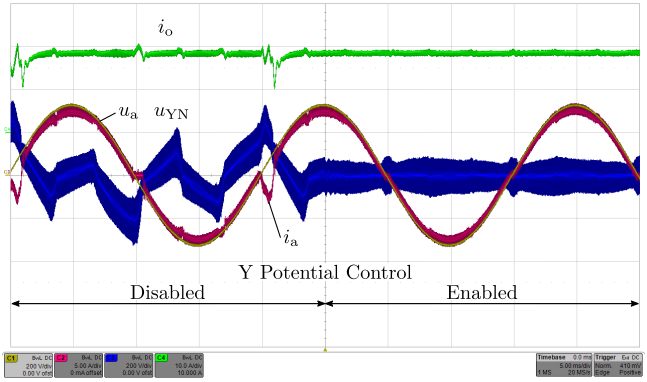

Fig. 6.7: Measurement results showing the mains voltage u_a (200 V/div), the corresponding ac input current i_a (5 A/div), the voltage u_{YN} (200 V/div) between the filter capacitor star-point Y and the mains neutral N and the output current i_o (10 A/div). During the first 25 ms the star-point potential controller is disabled which results in distortions of i_a and i_o. Once the controller is enabled, a sinusoidal input current and a constant output current are achieved.

the zero-sequence modulation signal m_0, which is added to all three phase-module modulation signals as described above. Note that G_0 can be omitted ($m_0 = 0$) if the phase modules are connected in Δ-configuration.

Measurement results taken at the prototype IMY/D rectifier in Y-configuration are shown in **Fig. 6.7**. The star-point potential controller is turned off during the first 25 ms and u_{YN} significantly deviates from zero, causing distortions in the input and output currents. Once the controller is enabled, $u_{YN} \approx 0\,\text{V}$ is achieved. Note that a significant switching frequency ripple of u_{YN} can be seen due to the discontinuous phase module input currents $i_{k,i}$ (cf. **Fig. 6.3**) and the comparatively small value of the filter capacitors C_f. As these are connected to the ac mains, their capacitance cannot be increased arbitrarily because of reactive power demand and power factor limitations, which is also the case in other buck-type rectifiers [39,119]. Additional measurement results for a step-change in the current reference signal i_o^* from 18 A to 9 A and back are shown in **Fig. 6.8**. It can be seen that the potential of the star-point Y stays close to zero even during a fast transient of i_o.

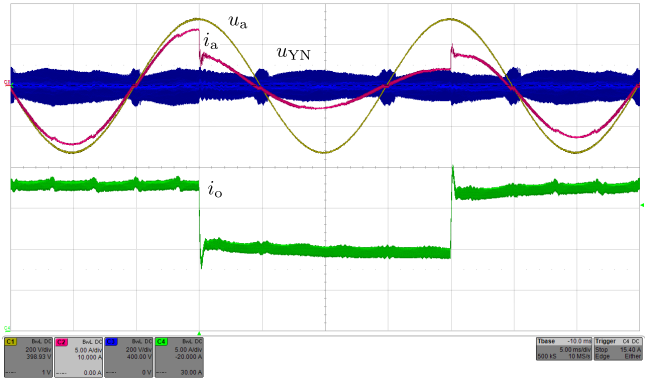

Fig. 6.8: Measurement results for step-changes of the current controller reference signal i_o^* from 18 A to 9 A and back. Shown are the output current i_o (10 A/div), the mains voltage u_a (200 V/div), the corresponding ac input current i_a (5 A/div) and the star-point voltage u_{YN} (200 V/div).

6.3 ZVS Modulation Scheme

The modulation principle described in **Section 6.2** requires that all phase modules create rectangular output voltage pulses $u_{k,o}$ with duty cycles d_k proportional to the absolute value of their corresponding ac input voltage. Note that no particular alignment of these switching frequency voltages is required for the derivation given above.

6.3.1 Symmetric Modulation

If symmetric phase shift modulation as described in [164] is used for all three phase-modules, the output voltage pulses of the phase modules are centered as shown in **Fig. 6.9**, forming a symmetric staircase voltage:

$$u'_{pm} = u'_{1,o} + u'_{2,o} + u'_{3,o} = \frac{n_s}{n_p}\left(u_{1,o} + u_{2,o} + u_{3,o}\right) \quad . \tag{6.8}$$

Note that due to the phase-shift modulation of the phase modules the dc output current i_o freewheels through the phase module switches, transformer leakage inductances L_σ and the output rectifier diodes when u'_{pm} is zero, as shown in **Fig. 6.9** and **Fig. 6.10(a)**. This is similar to a conventional phase-shift full-bridge dc-dc converter.

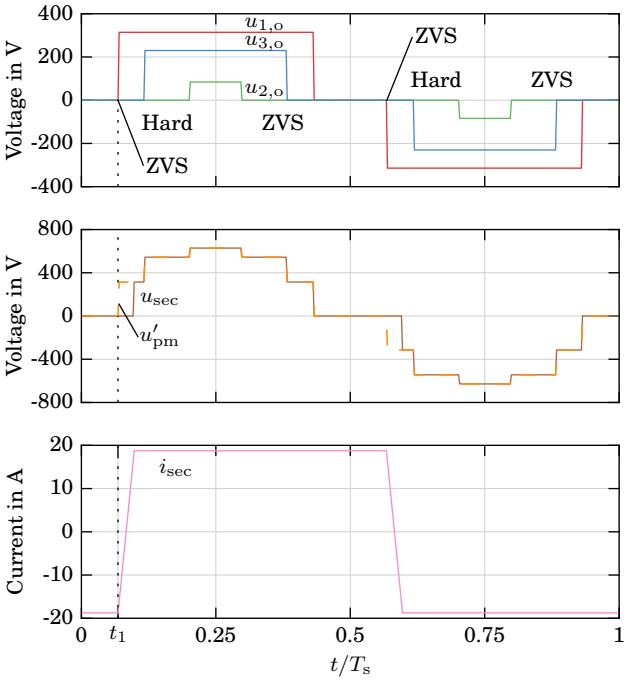

Fig. 6.9: Drawing ($n_s/n_p = 1$) of the three phase module output voltages $u_{k,o}$ and the resulting voltage u_{sec}, which is applied to the dc-side full-bridge rectifier for symmetric modulation. The switching frequency pulses in $u_{k,o}$ are center aligned. The phase module with the highest voltage ($u_{1,o}$) achieves ZVS while the remaining two phase modules typically exhibit a hard turn on.

Furthermore, as the duty cycle of each phase module is proportional to the corresponding ac line voltage, the phase module connected to the highest absolute line voltage is the first one within the switching frequency cycle to switch from a freewheeling to an active state (phase a at t_1 in **Fig. 6.9**). Provided that sufficient energy is stored in the three leakage inductances L_σ, this allows ZVS of the corresponding transistor in the phase module (module 1 in **Fig. 6.10** (b)).

However, this first transition from freewheeling to an active state impresses a voltage on L_σ that leads to a reversal of the transformer currents i_{pri} and i_{sec} and commutates the output rectifier diodes [cf. **Fig. 6.9** and **Fig. 6.10(c)**]. Therefore the switches in the remaining two phase modules

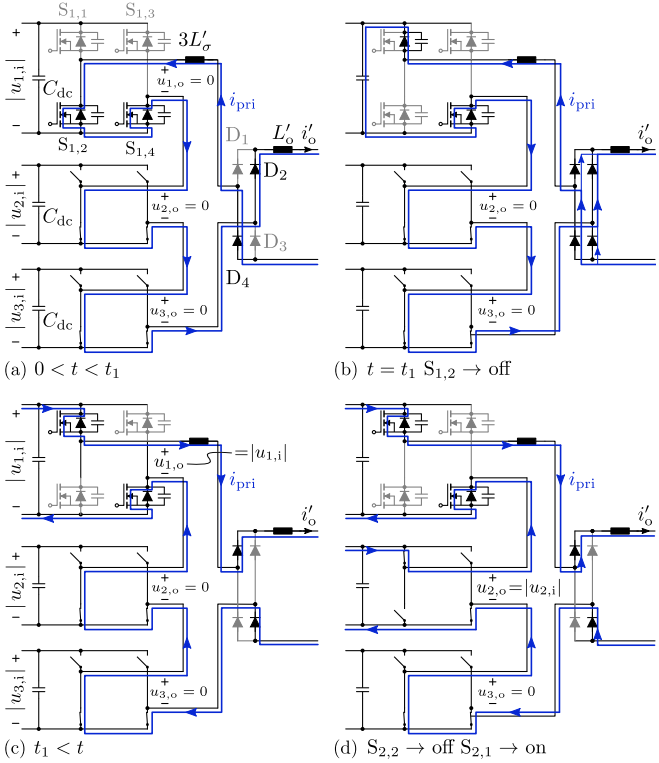

Fig. 6.10: Commutation of the phase modules (isolation transformers omitted for clarity) from freewheeling to active state in symmetric modulation: **(a)** Freewheeling at the beginning of a pulse period where $S_{k,2}$ and $S_{k,4}$ of each phase module are on. **(b)** $S_{1,2}$ is turned off at $t = t_1$, which starts a ZVS transition in phase module 1 and forces all four output rectifier diodes to conduct. **(c)** Once the transformer current has reversed D_2 and D_4 turn off. **(d)** Phase module 2 exhibits hard switching between $S_{2,2}$ and $S_{2,1}$.

exhibit hard switching as shown in **Fig. 6.10(d)**.

6.3.2 Asymmetric Modulation

In order to reduce the switching losses of the phase module switches, the voltage pulses created by the phase modules can be aligned at the switching transition from freewheeling to active state resulting in an asymmetric, falling

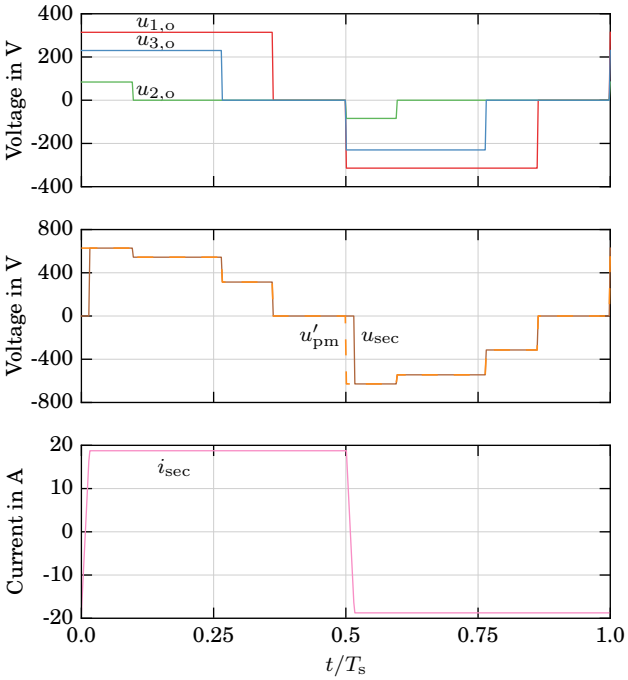

Fig. 6.11: Phase module output voltages $u_{a,b,c}$, secondary-side voltage u_{sec} and secondary-side current i_{sec} for the same operating conditions as in **Fig. 6.9** and asymmetric modulation. By aligning the rising edges of the three voltage pulses generated by the individual phase modules, ZVS can be achieved in all switching transitions, including those from freewheeling to an active state at $t \approx 0$ and $t \approx 0.5T_s$.

staircase voltage u'_{pm} as shown in **Fig. 6.11**. In this case the hard switching transitions occurring in symmetric modulation can be avoided, as the half-bridges in all three phase modules commutate simultaneously. Hence ZVS is achieved in all phase modules provided that sufficient energy is stored in the transformers' leakage inductances L_σ.

Detailed measurements for asymmetric modulation of a converter in Δ-configuration, taken at two different mains voltage phase angles ($\omega t \approx 0$ and $\omega t \approx 60°$) are plotted in **Fig. 6.12**. Shown are the phase module output voltage $u_{1,o}$ and the primary- ($i_{1,o}$) and secondary-side (i_{sec}) transformer currents. The scaling of primary- and secondary-side current is selected such that the turns ratio is taken into account; the difference between the currents is

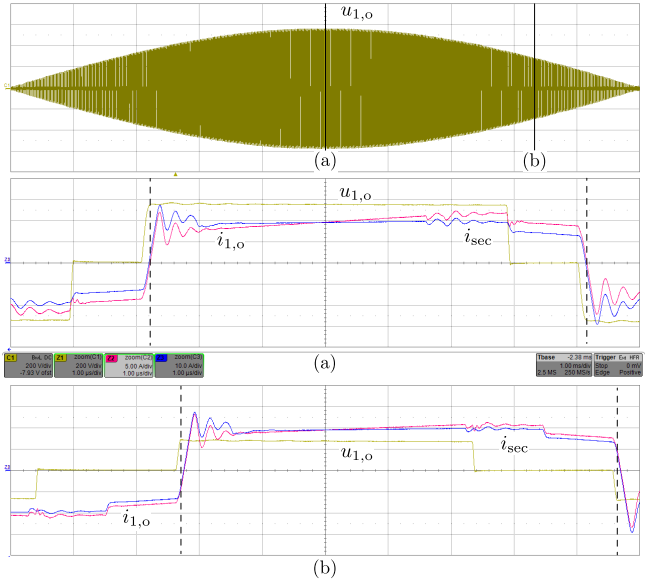

Fig. 6.12: Measurement results: The top plot shows the output voltage $u_{1,o}$ (200 V/div) of phase module 1 over one half-cycle of the mains period (1 ms/div). In **(a)** a zoom (1 µs/div) at the peak of the corresponding ac voltage ($\omega t \approx 0$) is shown with $u_{1,o}$, the output current of the phase module $i_{1,o}$ (5 A/div), and the secondary-side transformer current i_{sec} (10 A/div). **(b)** shows the corresponding plot at $\omega t \approx 60°$. It can be seen that once $u_{1,o}$ has reached its final value in a freewheeling-to-active state transition the sign of $i_{1,o}$ has not yet changed which implies that ZVS is achieved. The corresponding instants are marked with dashed lines.

due to the magnetizing current of the transformer. It can be seen that in all four freewheeling ($u_{1,o} = 0$)-to-active voltage generation ($u_{1,o} = \pm|u_{1,i}|$) transitions, marked with dashed lines, the phase module output voltage $u_{1,o}$ has reached its final value before the primary-side current $i_{1,o}$ has reversed its sign, which implies that ZVS is achieved. Once $i_{1,o}$ and i_{sec} have changed sign, an oscillation occurs between the leakage inductances L_σ and the parasitic capacitances of the output rectifier diodes. This can also be seen in **Fig. 6.13** where measurement results of i_{sec} and of the rectifier output voltage $|u_{sec}|$ are shown. In the freewheeling-to-active voltage generation transition a peak reverse voltage of 1.1 kV results for the rectifier diodes.

While a certain L_σ is required in order to achieve ZVS in the phase modules

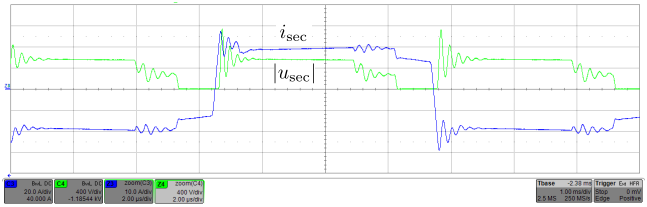

Fig. 6.13: Measurement results: Secondary-side current i_{sec} (10 A/div) and diode rectifier output voltage $|u_{\mathrm{sec}}|$ (400 V/div) during one pulse period (2 µs/div) at $\omega t \approx 0$ and nominal operation in Δ-mode. It can be seen that the switching actions of the phase modules cause oscillations of the resonant circuit formed by L_σ and parasitic capacitances of the rectifier diodes which can also be seen in the phase module output current in **Fig. 6.12**. This leads to a peak blocking voltage of ≈ 1.1 kV on the rectifier diodes for the transition from freewheeling to active voltage generation.

for a given load current, a higher L_σ will change the resonance frequency and potentially lead to higher overvoltage peaks at the output rectifier diodes. If this overvoltage exceeds the diodes' rating, snubber circuits are typically used, which lead to an increased system complexity, higher cost and/or additional losses. Note that no snubber circuits are used in the prototype as the resulting peak voltage of 1.1 kV (cf. **Fig. 6.13**) is within the diodes' rating.

ZVS Limit

The energy required in L_σ for complete ZVS can be derived from the amount of charge necessary to charge and discharge the parasitic capacitances of the three simultaneously commutating half-bridges like in phase-shift full-bridge dc-dc converters [165]. As the phase modules generally have different rectified input voltages, different charges are required for each phase module:

$$\begin{aligned} Q_1(\omega t) &= Q_{\mathrm{oss}}\left(\left|u_{1,\mathrm{i}}(\omega t)\right|\right) \ , \\ Q_2(\omega t) &= Q_{\mathrm{oss}}\left(\left|u_{2,\mathrm{i}}(\omega t)\right|\right) \ , \\ Q_3(\omega t) &= Q_{\mathrm{oss}}\left(\left|u_{3,\mathrm{i}}(\omega t)\right|\right) \ , \end{aligned} \tag{6.9}$$

where $Q_{\mathrm{oss}}(u)$ is the output capacitance charge of a single switch. This is shown in **Fig. 6.14** where $|u_{1,\mathrm{i}}| > |u_{3,\mathrm{i}}| > |u_{2,\mathrm{i}}|$ and negligible transformer magnetizing currents are assumed. Immediately after the simultaneous turn-off of switches $\mathrm{S}_{\mathrm{k},4}$ the primary-side transformer current i_{pri} splits between the parasitic capacitances of $\mathrm{S}_{\mathrm{k},3}$ and $\mathrm{S}_{\mathrm{k},4}$, cf. **Fig. 6.14(a)**. Once i_{pri} has

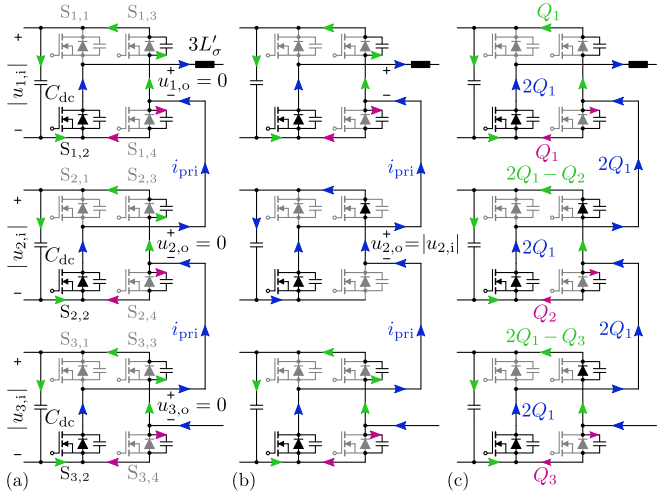

Fig. 6.14: Simultaneous free-wheeling-to-active state transition of the three phase-modules in asymmetric modulation with $|u_{1,\mathrm{i}}| > |u_{3,\mathrm{i}}| > |u_{2,\mathrm{i}}|$: **(a)** Current conduction paths immediately after the turn-off of switches $\mathrm{S}_{\mathrm{k},4}$. In each phase module the transformer current i_{pri} splits between switches $\mathrm{S}_{\mathrm{k},3}$ and $\mathrm{S}_{\mathrm{k},4}$. **(b)** The switching state change of the phase module with the lowest rectified ac input voltage (module 2) is completed (capacitance of $\mathrm{S}_{2,4}$ is charged, capacitance of $\mathrm{S}_{2,3}$ is discharged) and i_{pri} continues through $\mathrm{S}_{2,3}$'s body diode. **(c)** Charge transfer in connection with the switching state change of all phase modules from freewheeling-to-voltage generation.

transferred a charge equal to $2\,Q_2$, the body diode of $\mathrm{S}_{2,3}$ starts to conduct as phase module 2 has the lowest absolute input voltage, cf. **Fig. 6.14(b)**. The commutation finishes when $C_{1,4}$ in phase module 1 is fully charged and $C_{1,3}$ is fully discharged, which requires $2\,Q_1$ to be transferred by i_{pri}. Total charges, which are transferred through the individual components during a ZVS transition, are shown in **Fig. 6.14(c)**. Assuming $C_{\mathrm{dc}} \gg C_{\mathrm{oss}}$, the phase module input voltages $|u_{\mathrm{k,i}}|$ do not change significantly due to the additional charge and the energy E_{z} transferred from L_σ into the capacitors C_{dc} follows from **Fig. 6.14(c)** as

$$E_{\mathrm{z}} = \underbrace{|u_{1,\mathrm{i}}|\,Q_1}_{\text{Ph. Mod. 1}} + \underbrace{|u_{2,\mathrm{i}}|\,(2\,Q_1 - Q_2)}_{\text{Phase Module 2}} + \underbrace{|u_{3,\mathrm{i}}|\,(2\,Q_1 - Q_3)}_{\text{Phase Module 3}} \,. \tag{6.10}$$

In order to achieve ZVS the energy stored in the leakage inductances L_σ before the turn-off of $S_{k,4}$ has to fulfill

$$E_{L_\sigma} = \frac{1}{2}\, 3\, L_\sigma\, i_{sec}^2 \geq E_z \quad . \tag{6.11}$$

Note that in a real converter system, the value of i_{sec} at the turn-off of $S_{k,4}$ depends on several factors and parasitic effects such as:

- dc load current,
- output current i_o ripple,
- magnetizing currents of the transformers,
- parasitic capacitances (e.g. transformer windings and PCB),
- conduction losses during free-wheeling, and
- mains voltage amplitude, unbalance and distortion.

A precise calculation at which dc output current incomplete ZVS will occur would require a comprehensive analysis of these system parameters and is out of the scope here.

6.4 Δ-Configuration

The modulation scheme described in **Section 6.2.1** assumes a Y-configuration of the phase modules, resulting in a maximum ac mains current amplitude $\hat{I}_{max,Y}$ and maximum input power of $P_{max,Y}$,

$$\hat{I}_{max,Y} = I_o \frac{n_s}{n_p} \quad , \tag{6.12}$$

$$P_{max,Y} = \frac{3}{2}\, \hat{U}\, \hat{I} = \frac{3}{2}\, \hat{U} \frac{n_s}{n_p}\, I_o \quad . \tag{6.13}$$

Neglecting all losses in the converter, the maximum output voltage in Y-mode follows as

$$U_{o,max,Y} = \frac{3}{2}\, \hat{U}\, \frac{n_s}{n_p} \quad . \tag{6.14}$$

The same modulation scheme can also be applied in Δ-configuration, in which case the input and output voltages of the phase modules and therefore the

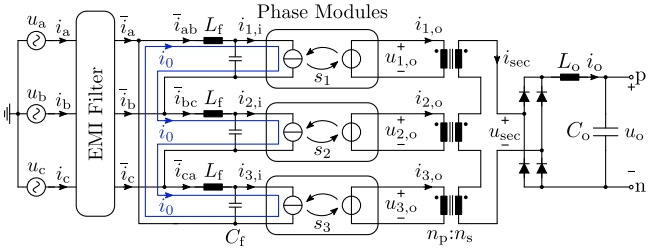

Fig. 6.15: Schematic of the rectifier in Δ-configuration, where the phase modules are replaced by controlled current and voltage sources. In Δ-configuration a zero-sequence current $\bar{i}_0$ can be used to operate the converter in overmodulation ($m \leq 2/\sqrt{3}$), which increases the maximum dc output voltage by $\approx 15\,\%$.

voltage stress of the semiconductors increase by a factor of $\sqrt{3}$ compared to Y-mode. If the same output voltage has to be created, the transformer turns ratio can be adapted accordingly, which reduces the currents in the phase modules' inverter switches by a factor of $1/\sqrt{3}$.

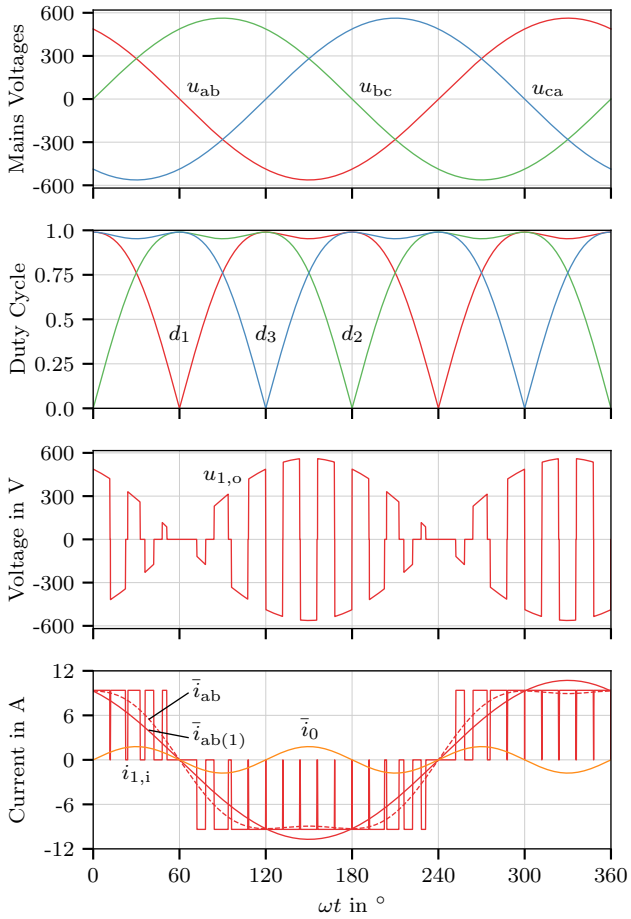

Fig. 6.16: Drawing of the modulation scheme using third harmonic current injection (3^{rd} HCI) with reduced f_{sw}, at maximum modulation index $m = 2/\sqrt{3}$: within each pulse interval each phase module produces a square-shaped high-frequency transformer voltage $u_{k,o}$, $k \in \{1, 2, 3\}$, with a duty cycle d_k. Neglecting C_{dc}, the discontinuous phase module input current $i_{k,i}$ results and after low-pass filtering by C_f and L_f input currents $\bar{i}_{ab}$, $\bar{i}_{bc}$ and $\bar{i}_{ca}$ proportional to d_k results. It can be seen that the mains frequency fundamental $\bar{i}_{ab(1)}$ of $\bar{i}_{ab}$ exceeds the peak value of $i_{1,i}$.

6.4.1 Third Harmonic Current Injection

It can be seen in **Fig. 6.15** that the ac inputs of the three phase-modules are forming a closed loop in Δ-mode, which allows a zero-sequence current

$$\bar{i}_0 = \frac{1}{3}\left(\bar{i}_{\mathrm{ab}} + \bar{i}_{\mathrm{bc}} + \bar{i}_{\mathrm{ca}}\right) \approx \frac{1}{3}\left\langle i_{1,\mathrm{i}} + i_{2,\mathrm{i}} + i_{3,\mathrm{i}}\right\rangle_{T_{\mathrm{sw}}} \tag{6.15}$$

to circulate through the phase modules without appearing in the rectifier's mains input currents $i_{\mathrm{a,b,c}}$ [62]. Note that $\bar{i}_0$ can be controlled using the zero-sequence modulation index m_0 (cf. **Fig. 6.6**), as no converter internal star-point Y exists in Δ-configuration and hence no star-point potential controller is required. As $\bar{i}_0$ circulates between the phase modules, but not through the mains voltage sources, it does not impact the active power exchange with the mains. However, the input rectifiers of the phase modules require that their input currents $i_{\mathrm{k,i}}$ have the same sign as the corresponding phase module input voltages $u_{\mathrm{k,i}}$, which implies $\bar{i}_0 = 0$ at every zero crossing of a line-to-line mains voltage. Using third harmonic current injection (3^{rd} HCI), for example as

$$m_0 = \frac{m}{6}\sin(3\,\omega t) \quad , \tag{6.16}$$

a modulation index m up to $2/\sqrt{3} \approx 1.15$ can be selected with all phase module duty cycles $d_{1,2,3} \leq 1$ [166]. A drawing of the resulting waveforms is shown in **Fig. 6.16**, showing the phase module input current $i_{1,\mathrm{i}}$ and its low-pass filtered version $\bar{i}_{\mathrm{ab}}$ with a fundamental $\bar{i}_{\mathrm{ab(1)}}$ which is a factor of $2/\sqrt{3}$ higher than the transformed output current $I_{\mathrm{o}}' = n_{\mathrm{s}}/n_{\mathrm{p}}\ I_{\mathrm{o}}$. The maximum mains input current, power and hence output voltage using 3^{rd} HCI can therefore be calculated as:

$$\hat{I}_{\mathrm{max},\Delta} = I_{\mathrm{o}}\,\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\,\frac{2}{\sqrt{3}}\,\sqrt{3}\,, \tag{6.17}$$

$$P_{\mathrm{max},\Delta} = \frac{\sqrt{3}}{2}\,\sqrt{3}\,\hat{U}\,\hat{I}_{\mathrm{max},\Delta} = 3\,\hat{U}\,I_{\mathrm{o}}\,\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\,, \tag{6.18}$$

$$U_{\mathrm{o,max},\Delta} = 3\,\hat{U}\,\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\,. \tag{6.19}$$

This increase in output voltage range typically allows a reduced turns ratio $n_{\mathrm{s}}/n_{\mathrm{p}}$ which in turn reduces the current stresses (cf. **Section 6.4.3**) and hence the conduction losses of the phase module switches. Measurement results with 3^{rd} HCI are shown in **Fig. 6.17**. It can be seen that a sinusoidal mains input current i_{a} results, even though the individual phase module input currents $\bar{i}_{\mathrm{ab}}$ and $\bar{i}_{\mathrm{bc}}$ contain a third harmonic.

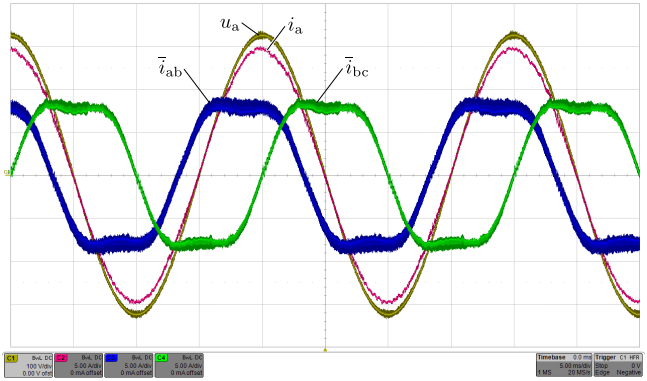

Fig. 6.17: Measurement results (5 ms/div) obtained from a prototype converter in Δ-configuration using 3rd HCI operated with $m \approx 1$. The low-pass filtered phase module input currents i_{ab} and i_{bc} (5 A/div) are non-sinusoidal due to the third harmonic current, while the converter's mains input current i_a (5 A/div) is free of low-frequency distortions and in phase with the corresponding voltage u_a (100 V/div).

6.4.2 Δ-Mode Modulation Boundaries

In order to analyze the IMD rectifiers modulation boundary and reactive power generation capabilities, its input current space vector diagram is derived in the following assuming a phase-integrated three-phase input side filter stage (as stage 2 in **Fig. 6.20**) also for stage 1. As the indirect matrix-type phase modules use an input diode rectifier, the input current $i_{k,i}$ $k \in \{1, 2, 3\}$ of each phase module can only have the same sign as the corresponding phase module input voltage $u_{k,i}$, which is defined by the respective ac mains line-to-line voltage. Furthermore, whenever the phase module's inverter switches apply a non-zero voltage $u_{k,o}$ to its transformer, the transformer's primary current $i_{k,o} \approx I'_o$ is drawn from the phase module input. This can be described as

$$i_{k,i} = \text{sign}(u_{k,i})\, I'_o\, s_k \quad s_k \in \{0, 1\}\,,\, k \in \{1, 2, 3\}\,, \tag{6.20}$$

where $s_k = 1$ if phase module k is in an active state, i.e. applying voltage to its transformer ($u_{k,o} \neq 0$), and $s_k = 0$ if it is in free-wheeling state ($u_{k,o} = 0$).

This allows to calculate the IMD rectifier's input current space vectors $\vec{i}_i$ using

$$\vec{i}_i = \frac{2}{3}\left(i_a + i_b\, e^{j2\pi/3} + i_c\, e^{-j2\pi/3}\right) \quad . \tag{6.21}$$

Tbl. 6.2: Input Current Space Vectors in Δ-Mode for Sectors 1 & 2

$(s_1\, s_2\, s_3)$	i_a/I_o'	i_b/I_o'	i_c/I_o'	i_0/I_o'	$\vec{i}_i/I_o'$
(000)	0	0	0	0	0
(100)	1	−1	0	1/3	$1 - j/\sqrt{3}$
(010)	0	1	−1	1/3	$j\,2/\sqrt{3}$
(001)	−1	0	1	−1/3	$1 + j/\sqrt{3}$
(110)	−1	0	1	2/3	$1 + j/\sqrt{3}$
(101)	2	−1	−1	0	2
(011)	1	1	−2	0	$1 + j\sqrt{3}$
(111)	2	0	−2	1/3	$2 + j\,2/\sqrt{3}$

The results for an ac mains voltage vector $\vec{u}_i$ in sectors 1 or 2 ($u_{ab} > 0$, $u_{bc} > 0$, $u_{ca} < 0$) are listed in **Tbl. 6.2** and shown in **Fig. 6.18(a)**. It can be seen from the current space vector diagram that an input current vector $\vec{i}_i$ with an amplitude up to $2\, n_s/n_p\, I_o$ can be created, which is in accordance with (6.17). Furthermore, $\vec{i}_i$ can lead or lag the mains voltage $\vec{u}_i$, which implies that the IMD rectifier can be used to create reactive power at the ac input. The input current can be phase shifted up to ±30° with respect to the mains voltage, but only for a modulation index $m < 1/\sqrt{3}$. For a higher modulation index the resulting phase shift angle, and therefore the reactive power which can be generated, reduces as shown in **Fig. 6.18(b)**. For the maximum modulation index $m = 2/\sqrt{3} \approx 1.15$ no reactive power can be generated. Note that the (buck-type) IMD rectifier's input current space vector diagram is quasi-dual to the (boost-type) VIENNA Rectifier's input voltage space vector diagram. This implies that both rectifiers have corresponding limitations on overmodulation and reactive power generation [167].

6.4.3 Semiconductor Stresses

The maximum reverse voltage applied to the input rectifier diodes and inverter switches of the phase modules depends only on the ac input voltage's amplitude $\hat{U}$. In Δ-configuration the voltage applied to a single-phase module, and therefore the voltage stress of the devices, increases by a factor of $\sqrt{3}$ as shown in **Tbl. 6.3** Similarly, the voltage applied to the output side diode rectifier depends on the input voltage and the transformer turns ratio. However, oscillations between the parasitic capacitances of the diodes and the transformers' stray inductances will create a transient overvoltage, as can be

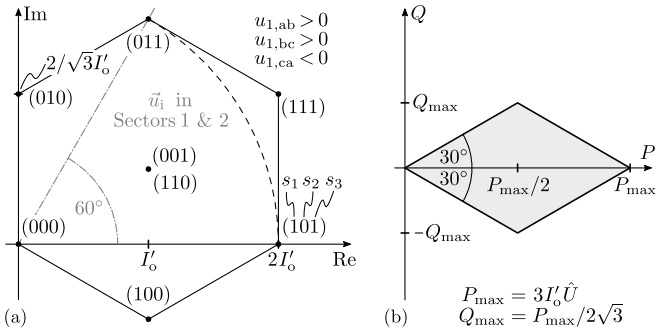

Fig. 6.18: (a) Space vector diagram of the rectifier's input current $\vec{i}_i$ in *Delta*-mode for a mains voltage in sectors 1 or 2, i.e. $u_{1,ab} > 0$, $u_{1,bc} > 0$, $u_{1,ca} < 0$, assuming a constant dc output current $I'_o = I_o\, n_s/n_p$, and a Δ-connection of the phase modules. It can be seen from geometric identities that the maximal space vector amplitude of the input current fundamental in this case is given by $|\vec{i}_i| = 2\, I'_o$. The resulting active and reactive power generation limits of the rectifier are shown in **(b)**.

Tbl. 6.3: Semiconductor Voltage Stresses

	Y-Mode	Δ-Mode
Input Rectifier	$U_{max} = \hat{U}$	$U_{max} = \hat{U}\sqrt{3}$
Inverter	$U_{max} = \hat{U}$	$U_{max} = \hat{U}\sqrt{3}$
Output Rectifier	$U_{max} = \hat{U}\frac{n_s}{n_p}2$	$U_{max} = \hat{U}\frac{n_s}{n_p}2\sqrt{3}$

seen in **Fig. 6.13**.

Note that the current stresses of all semiconductors are equal for Y- and Δ-mode as only the phase modules' input voltages change between the modes (cf. **Tbl. 6.4**). However, if the same output and input voltages are considered in both cases a lower transformer turns ratio n_s/n_p can be used in Δ-configuration compared to Y-configuration, which reduces the current stresses of the input rectifier diodes and inverter switches.

6.5 Prototype Rectifier Details

All measurement results presented in this chapter were taken on a 7.5 kW prototype rectifier built according to the specification given in **Tbl. 6.1**. The

Tbl. 6.4: Semiconductor Current Stresses

	$m_0 = 0$	$m_0 = \frac{m}{6}\sin(3\omega t)$
Input Rectifier	$I_{\mathrm{rms}} = I_{\mathrm{o}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\sqrt{\frac{m}{\pi}}$ $I_{\mathrm{avg}} = I_{\mathrm{o}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\frac{m}{\pi}$	$I_{\mathrm{rms}} = I_{\mathrm{o}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\sqrt{\frac{m}{\pi}\frac{19}{18}}$ $I_{\mathrm{avg}} = I_{\mathrm{o}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\frac{m}{\pi}\frac{19}{18}$
Inverter	$I_{\mathrm{rms}} = I_{\mathrm{o}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\frac{1}{\sqrt{2}}$ $I_{\mathrm{avg}} = I_{\mathrm{o}}\frac{n_{\mathrm{s}}}{n_{\mathrm{p}}}\frac{1}{2}$	
Output Rectifier	$I_{\mathrm{rms}} = I_{\mathrm{o}}\frac{1}{\sqrt{2}}$ $I_{\mathrm{avg}} = I_{\mathrm{o}}\frac{1}{2}$	

main components used in the prototype are listed in **Tbl. 6.5**. Pictures of the implemented prototype rectifier are shown in **Fig. 6.19** and a brief description of the main design trade-offs follows.

6.5.1 System Design

The first decision in the design of an IMY/D rectifier is whether it should be operated in Y- or Δ-configuration or both. As given in **Tbl. 6.3**, the voltage stress of the phase module semiconductors is higher in Δ-configuration by a factor of $\sqrt{3}$. For example, in Y-configuration semiconductors with a blocking voltage rating of 650 V, such as Si MOSFETs or GaN HEMTs can used in a rectifier operating from a 400 V rms to 480 V rms mains, as the blocking voltage of the phase modules' semiconductor devices is defined by the mains' line-to-neutral voltage. In Δ-configuration the maximum blocking voltage increases by a factor of $\sqrt{3}$ and 1.2 kV devices such as SiC MOSFETs or Si IGBTs have to be used, but the maximum output voltage of the phase modules increases accordingly. If the same dc output voltage has to be created, a higher turns ratio $n_{\mathrm{p}} : n_{\mathrm{s}}$ can be used, which reduces the current stresses on the phase modules' semiconductors, as can be seen from the formulas given in **Tbl. 6.4**. For rectifiers which have to operate in a wide range of mains voltages, for example 150 V-460 V line-to-line voltage, both modes can be utilized, where the system is operated in Δ-configuration for a low input voltage and in Y-configuration for high voltage.

As the IMY/D rectifier is a buck-type system, its maximum output voltage

Tbl. 6.5: Selected Components

Input Rectifier	1200 V, 45 A Si rectifier, DSP45-12A
Inverter	1200 V, 60 A, 25 mΩ SiC MOSFET, C2M0025120D
Output Rectifier	1200 V, 54 A SiC Schottky rectifier, C4D40120D
Transformer	Stack of 2 E55 N96 cores, $n_p : n_s = 14 : 7$
	1260 Strands / 2205 strands, 71 µm litz wire
	$L_\sigma = 1.25\,\mu H$, $L_m = 200\,\mu H$ w.r.t. secondary-side
Output Inductor	2 x 200 µH, 2 stacked E55 N87 cores each
	14 turns 2 mm solid copper wire
PM Filter	$L_f = 16\,\mu H$, C058206, 11 turns, 2 in series
(Stage 1)	$C_f = 1.65\,\mu F$, 2 x 3.3 µF 300 V_{rms} X2 in series
	$C_{dc} = 0.4\,\mu F$, 4 x 100 nF 1000 V MLCC parallel
EMI Filter	$L_{cm} \approx 800\,\mu H$ W422-05, 3 x 10 turns, 2 mm wire
(Stage 2)	$C_{cm} = 4.7$ nF 300 V_{rms} X2 in Y-connection
	$L_{dm} = 70\,\mu H$ C058083A2, 30 turns, 2 mm wire
	$C_{dm} = 470$ nF 300 V_{rms} X2 in Y-connection
	$L_{damp} = 9\,\mu H$ C058059A2, 15 turns, 2 mm wire
	$R_{damp} = 1\,\Omega$

is limited by the mains voltage and hence the transformer turns ratio $n_p : n_s$ has to be selected based on the lowest ac input voltage and the highest dc output voltage at which the rectifier has to be operated, using either (6.14) or (6.19) according to the selected operating mode. Note that selecting a larger $n_p : n_s$ results in a lower maximum output voltage and hence less margin for losses, mains undervoltages, etc., while at the same time reducing the conduction losses in the phase module switches. The implemented prototype uses 1.2 kV SiC MOSFETs due to their low conduction and switching losses and because they allow operation in both Y- and Δ-configuration from a 400 V rms mains. The converter is designed for Δ-configuration with a transformer turns ratio of $n_p : n_s = 2$ which results in a 22 % output voltage margin for ac input undervoltages, losses, unbalances etc.

As shown in **Fig. 6.20**, the rectifier's EMI filter stages can either be implemented as individual single-phase filters per phase module (stage 1 in **Fig. 6.20**) or as phase-integrated filter stages at the three-phase mains input (stage 2). While single-phase filter stages allow a higher degree of modularity and potentially higher flexibility in wide input voltage range designs, which are operated in either Y- or Δ-configuration, integrated three-phase filters are expected to be beneficial in terms of component volume, losses and/or cost as

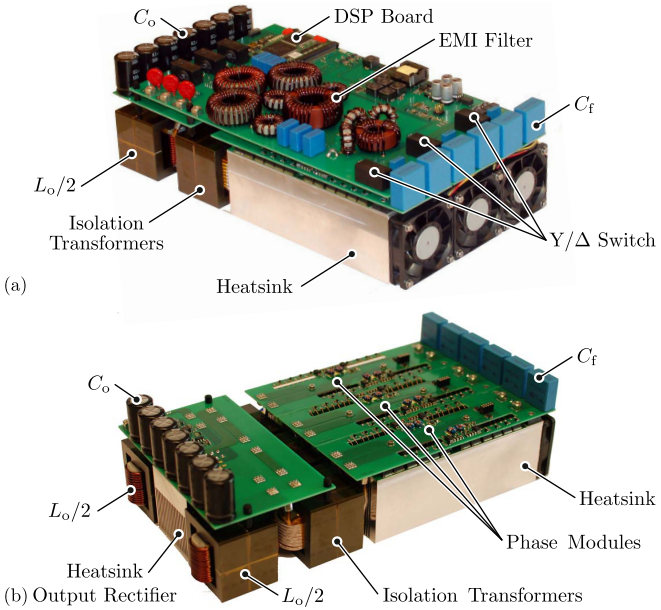

Fig. 6.19: Realized 7.5 kW IMY/D rectifier prototype, **(a)** fully assembled and **(b)** with the top PCB removed in order to show the phase modules and the output rectifier board.

they require only a single common-mode choke per stage compared to one per phase module in phase-modular filters. However, a detailed analysis of these EMI filter topologies is out of the scope of this chapter.

6.5.2 Performance

The measured efficiency for asymmetric and symmetric modulation, with and without 3rd HCI, is plotted in **Fig. 6.21**. As expected from the considerations above, the efficiency is higher for asymmetric modulation as all phase modules achieve ZVS. At rated output power the efficiency increases from 96.9 % with symmetric modulation (without 3rd HCI) to 97.2 % with asymmetric modulation which corresponds to a reduction of the losses by 22 W. Towards light load the efficiency curves converge, as even with asymmetric modulation ZVS cannot be achieved because the load current does not store sufficient energy in the leakage inductances L_σ to fully recharge all parasitic

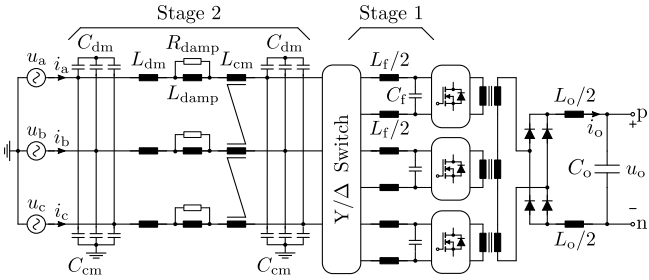

Fig. 6.20: Schematic of the EMI input filter implemented in the IMY/D rectifier prototype. Note that either separate single-phase filter stages for each phase module (as in stage 1 shown here), or phase-integrated three-phase filter stages (as in stage 2) can be used.

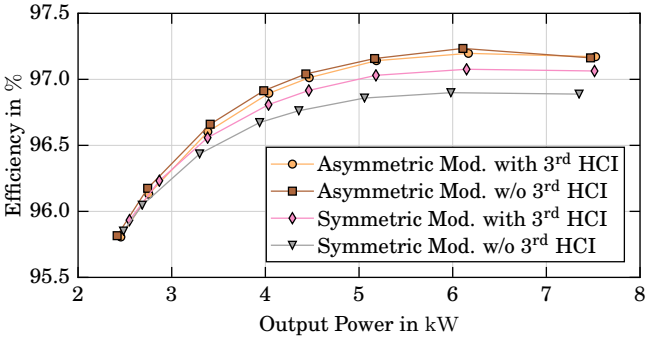

Fig. 6.21: Measured converter efficiencies in Δ-configuration as a function of output power for asymmetric (ZVS) and symmetric (hard switching) modulation and with and without 3rd HCI at nominal input and output voltages. The measurements were taken using a *Yokogawa WT3000* power analyzer.

capacitances resulting in incomplete ZVS.

As the same transformer was used for operation with and without 3rd HCI basically the same efficiency results for both cases. However, without 3rd HCI the prototype has to be operated very close to the modulation limit $m \approx 1$, which would not be feasible in an industrial application. In order to obtain the same output voltage margin as with 3rd HCI the turns ratio $n_p : n_s$ has to be reduced to $\sqrt{3}/2 \approx 87\,\%$. While this does not change the winding losses in the transformers, it increases the current in the inverter switches $S_{k,1..4}$

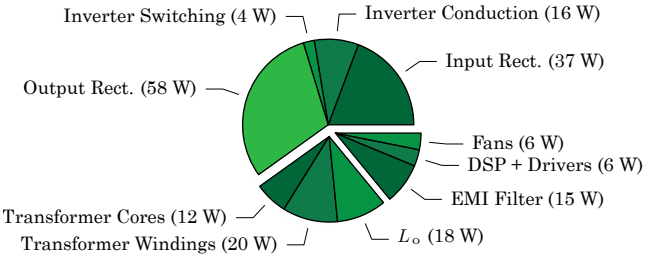

Fig. 6.22: Calculated component losses for nominal operation of the prototype converter in Δ-configuration with 3rd HCI and asymmetric modulation.

by 15 %, leading to ≈ 33 % higher conduction losses. Note that for symmetric modulation the efficiency increases with 3rd HCI due to the changed shape of the duty cycle signal.

In **Fig. 6.22** the calculated component losses for nominal operation in Δ-configuration with 3rd HCI are shown. About 30 % of the total losses occur in the SiC Schottky diodes of the output rectifier, while the input rectifiers and inverters account for another ≈ 30 %. The remaining losses are due the passive components, DSP, gate drivers, fans, etc. With outer dimensions of 35.5 cm x 18 cm x 10.5 cm, a total volume of 7.28 dm^3 and a power density of 1.03 kW/dm^3 results. However, ≈ 60 % of this volume is occupied by heatsinks, which were reused from a previous prototype based on Si MOSFET devices [164]. As these could not withstand hard-switching, which occurs for low dc output currents, an oring-configuration was used, where low-voltage Schottky diodes are connected in series with the MOSFETs, effectively suppressing the MOSFETs body diode. An additional SiC Schottky diode is than connected in antiparallel to this series connection to enable reverse current flow. This results in considerably higher conduction and switching losses than the SiC MOSFETs used in this thesis. It is estimated that a power density of ≈ 1.4 kW/dm^3, or more, could be achieved with an optimized custom heatsink.

The measured total harmonic distortion values of the ac input currents are plotted in **Fig. 6.23**. It can be seen that the prototype achieves ≤ 2 % of THD for half load and higher.

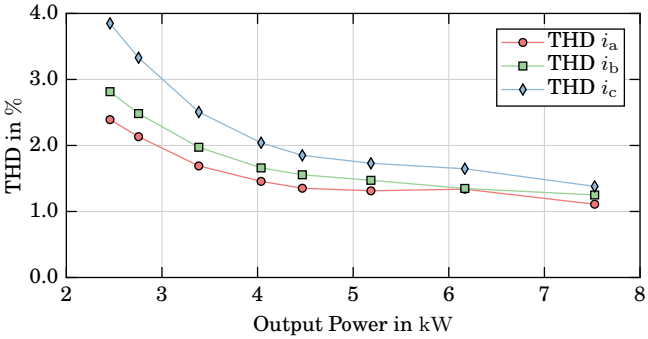

Fig. 6.23: Measurement results: THD of the IMD rectifier's input currents as a function of dc output power for operation in Δ-configuration with purely sinusoidal mains voltages. The measurements were taken using a *Yokogawa WT3000* power analyzer.

6.6 Summary

This chapter analyzes the three-phase phase-modular isolated Indirect Matrix-Type Y/Δ PFC rectifier (IMY/D rectifier), which consists of three individual isolated phase modules that can be connected to the mains in a star- or delta-configuration. Using both configurations allows a wide input voltage range and/or to adapt the voltage and current stresses of the semiconductors to the available device technologies.

Basic and advanced modulation schemes for operation in Y- or Δ-configuration are described, which enable operation with ZVS of the phase modules' inverter switches, resulting in a 10 % reduction of the overall losses in a 7.5 kW SiC MOSFET based prototype rectifier. The modulation limits for Y- and Δ-mode are described and a thrid harmonic current injection principle (3^{rd} HCI) is proposed, which allows up to ≈ 15 % higher dc output voltage and/or reduced conduction losses of the inverter switches. The prototype system achieves an efficiency of 97.2 % at full-load using the proposed ZVS modulation and 3^{rd} HCI with an mains input current THD of less than 2 %.

7

99% Efficient Isolated Three-Phase Matrix-Type DAB PFC Rectifier

In many applications that utilize a three-phase PFC rectifier, isolation is required between the mains and the load, for example due to safety reasons or different grounding schemes. A series connection of a non-isolated PFC rectifier and an isolated dc-dc converter is typically used in this case, forming a two-stage power conversion. As an alternative, this chapter describes the modulation, design and realization of a single-stage isolated three-phase PFC rectifier. The system combines a matrix converter with a dual active bridge (DAB) and is called isolated matrix-type DAB three-phase rectifier (IMDAB3R). A soft-switching modulation scheme is proposed and comprehensively analyzed, deriving closed form solutions and numerical optimization problems to calculate switching times that achieve minimal conduction losses. Based on this analysis, the design of an 8 kW, 400 V rms three-phase ac to 400 V dc prototype is discussed, striving for the highest possible efficiency. Using 900 V SiC MOSFETs and a transformer with integrated inductor, a power density of 4 kW/dm^3 is achieved. Measurement results confirm a ultra-high full-power efficiency of 99.0 % at nominal operating conditions and 98.7 % at 10 % lower input voltage.

7.1 Introduction

In recent years the number and power demand of intrinsic dc loads has increased significantly in residential areas and commercial or office buildings. These loads include electric vehicles, LED lighting, variable speed drives for energy efficient air conditioning and ventilation systems and information and communication technology equipment, such as desktop computers, servers and data centers. At the same time the amount of generated dc power increases as well, as renewable energy sources, such as photovoltaic panels and small-scale wind turbines, produce a direct current. Hence, dc distribution systems that span either only a single commercial building, industrial plant or a full residential area are expected to reduce conversion losses, improve reliability and/or lower cost. These so-called dc microgrids have received significant attention in scientific literature, research and industry [78, 84, 90, 110].

The same benefits are also expected for dc distribution systems in data centers as the number of conversion stages can be reduced [92, 93, 107, 168]. As data centers and telecommunication equipment consume significant amounts of power and are typically operated 24/7, the conversion losses of rectifiers and dc-dc converters constitute a significant share of a site's operational expenses. Therefore, circuit efforts resulting in and efficiencies as high as 99 % are economically feasible in this case [94, 133, 134].

Typically, loads of tens to hundreds of kilowatts are supplied, which implies that three-phase power factor correction (PFC) rectifiers are required to supply the dc bus from the conventional ac mains. In many applications two conversion stages are used, where a three-phase boost-type PFC front end provides an $\approx$ 800 V dc voltage which is stepped down by a dc-dc converter to the dc bus voltage of $\approx$ 400 V, yielding a two-stage system. Galvanic isolation can be included in the dc-dc converter if this is required by the application, for example due to safety reasons or grounding schemes. Alternatively, this conversion process between the mains and a dc output voltage can also be performed by different isolated matrix-type three-phase PFC rectifiers in a single-stage without an intermediate dc voltage and/or energy storage [36, 50, 52, 53, 55, 156, 170–172].

One of the simplest isolated single-stage three-phase rectifier circuits is shown in **Fig. 7.1(a)**. It consists of an input filter, a diode rectifier bridge providing the six-pulse voltage u_{xz} and a dual active bridge (DAB) arrangement used as isolated dc-dc converter. Using a DAB converter has the advantage that only a single magnetic component, the isolation transformer, is required, provided that it is designed with a sufficiently large leakage inductance L_l

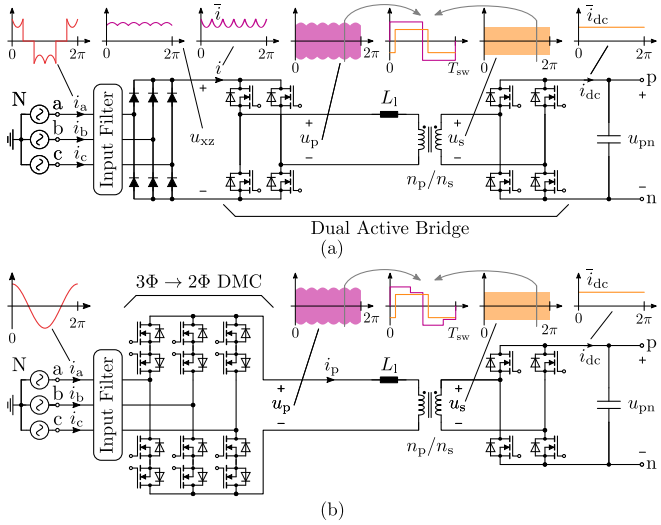

Fig. 7.1: Isolated single-stage three-phase rectifier circuits: In **(a)** a diode bridge is used to create a six-pulse voltage u_{xz} which supplies a dual active bridge (DAB) that provides galvanic isolation and creates an output voltage u_{pn} that can be higher or lower than u_{xz}. As only two diodes conduct at any time, the resulting mains currents $i_{a,b,c}$ are non sinusoidal. **(b)** By using a 3-to-2 direct matrix converter (DMC), any line-to-line mains voltage can be selected as primary-side winding voltage u_p, which enables operation with sinusoidal mains currents [59, 60, 169]. This circuit is denominated isolated matrix-type DAB three-phase rectifier (IMDAB3R) in this thesis.

and it enables both buck- and boost-operation. This means that the output voltage u_{pn} can be higher or lower than the six-pulse voltage u_{xz}. However, only two diodes of the input rectifier conduct at any time and therefore the resulting mains input currents $i_{a,b,c}$ are not sinusoidal. To overcome this, the diode rectifier and the DAB converter's primary-side full-bridge can be replaced with a direct matrix converter (DMC) as shown in **Fig. 7.1(b)**. This circuit was proposed in [59] as vehicle-to-grid interface with bidirectional power flow and in [60] and [169] as inverter. The resulting circuit is called isolated matrix-type DAB three-phase rectifier (IMDAB3R) in this thesis. The modulation schemes described in the above mentioned publications both lead to low-order harmonics in the input currents. In [169] an ac current total harmonic distortion (THD) of 12 % is reported, which is typically not acceptable for a PFC rectifier.

Tbl. 7.1: Nominal Operating Conditions & Converter Specifications

Input Voltage (Line-to-Neutral)	$U_1 = 230\,\mathrm{V}$ rms
Input Frequency	$\omega = 2\pi\,50\,\mathrm{Hz}$
Nominal DC Output Voltage	$U_{\mathrm{pn}} = 400\,\mathrm{V}$
Nominal Output Power	$P = 8\,\mathrm{kW}$
Nominal Switching Frequency	$f_{\mathrm{sw}} = 31\,\mathrm{kHz}$
Leakage Inductance	$L_1 = 36\,\mu\mathrm{H}$
Turns Ratio	$n_{\mathrm{p}}/n_{\mathrm{s}} = 22/17 \approx 1.29$

In the following, a zero voltage / zero current switching modulation scheme achieving purely sinusoidal mains currents is analyzed in **Section 7.2**, and conduction loss optimal switching times are derived. Based on this, the design procedure of an ultra-efficient 8 kW prototype rectifier and the DMC's commutation patterns are described in **Section 7.3**. Measurement results are presented in **Section 7.4**, and finally a summary of the main findings and conclusions is given in **Section 7.5**.

7.2 Modulation

In order to derive a modulation scheme for the IMDAB3R, its basic circuit topology [cf. **Fig. 7.1(b)**] is simplified by replacing the DMC MOSFETs with two one-of-three selector switches $\mathrm{S_g}$ and $\mathrm{S_h}$ that connect nodes g and h to one of the three input terminals a, b, and c. The input filter is omitted, resulting in the circuit shown in **Fig. 7.2(a)**. For the calculation of the resulting primary-side transformer current i_{p}, the circuit is simplified further by replacing the mains voltages and $\mathrm{S_g}$ and $\mathrm{S_h}$ with an equivalent voltage source u_{p}; the output voltage u_{pn}, the secondary-side full-bridge and the turns ratio are replaced with the voltage source $u'_{\mathrm{s}} = u_{\mathrm{s}} n_{\mathrm{p}}/n_{\mathrm{s}}$ as shown in **Fig. 7.2(b)**. Without loss of generality, only the first mains voltage sector with $0° \leq \omega t < 30°$ [$u_{\mathrm{a}} > 0 > u_{\mathrm{b}} \geq u_{\mathrm{c}}$, cf. **Fig. 7.2(c)**] is analyzed. The obtained results can be generalized to the remaining 11 sectors using common symmetry considerations.

7.2.1 ZVS/ZCS Switching Pattern

Transformer voltage waveforms that achieve zero voltage switching (ZVS) for a sufficiently high output power are shown in **Fig. 7.3**. For ZVS to occur, all rising edges of u_{p} must occur when i_{p} is negative an vice versa and all rising

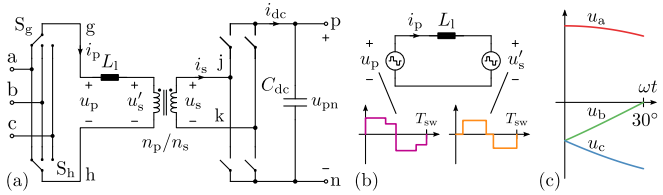

Fig. 7.2: (a) Simplified schematic of the IMDAB3R where the DMC MOSFETs are replaced by two one-of-three selector switches, S_g and S_h, and the input filter is omitted. In **(b)** the DAB-like converter model, used for the derivation of a modulation scheme achieving PFC, is shown. The input and output switches are replaced by equivalent voltage sources u_p and u'_s, referred to the transformer's primary-side. Only mains voltages in sector 1, as shown in **(c)**, are considered in the derivation.

edges of u_s must occur while i_p is positive. As a positive u_p generally results in an increasing current i_p, a staircase type pattern is used for u_p, where the mains line-to-line voltage with the highest absolute value (u_{ac} in sector 1) is selected for u_p at the beginning of the switching frequency period, when i_p is still < 0 A due to the last period. Next, the line-to-line voltage with the second largest absolute value (u_{ab}) is selected and finally 0 V are applied to the primary-side winding. Both transitions cause falling edges of u_p at positive i_p, which enables ZVS. At the beginning of the second half of every switching frequency cycle, u_p is switched to $-u_{ac}$ and the same waveform as before, but with inverted polarity of u_p, u_s and i_p, is created. This ensures that no dc voltage is applied to the transformer's primary-side winding. With the time t normalized to the period $T_{sw} = 1/f_{sw}$ of one switching cycle, u_p is defined as:

$$u_p(t) = \begin{cases} u_{ac} & \text{if } 0 \le t < \frac{1}{2} - t_2 \\ u_{ab} & \text{if } \frac{1}{2} - t_2 \le t < \frac{1}{2} - t_1 \\ 0 & \text{if } \frac{1}{2} - t_1 \le t < \frac{1}{2} \\ -u_p\left(t - \frac{1}{2}\right) & \text{if } \frac{1}{2} \le t < 1 \end{cases}, \tag{7.1}$$

where t_1 and t_2 must fulfill:

$$0 \le t_1 \le t_2 \le \frac{1}{2} \quad . \tag{7.2}$$

A pulse width modulated (PWM) square-wave ac voltage with variable duty cycle and phase shift is used for the secondary-side voltage u'_s, where the switching times of the leading edges are determined by t_3 and the lagging

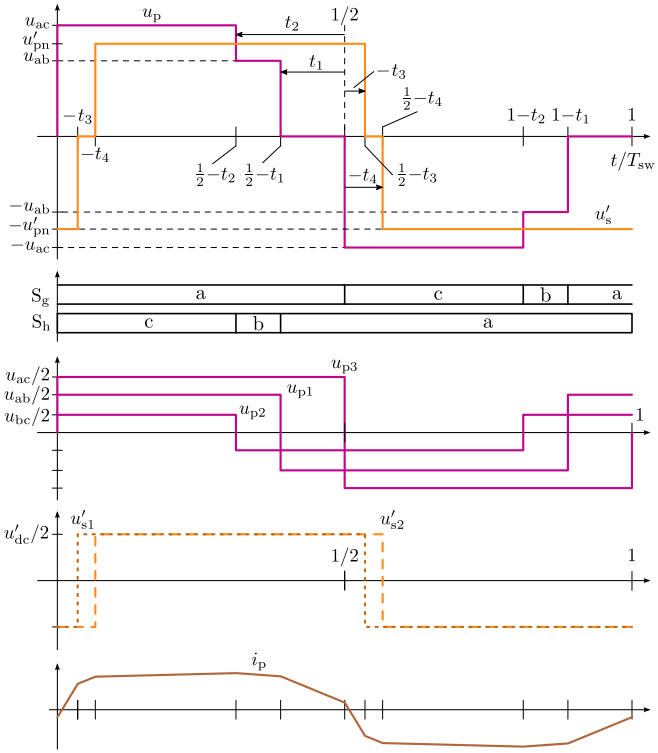

Fig. 7.3: Drawing (not to scale) of the primary (u_p) and secondary-side (u'_s) transformer voltages and the resulting primary-side current i_p for a mains voltage in sector 1, i.e. $u_a > 0 \geq u_b \geq u_c$. To achieve ZVS a staircase-shaped voltage u_p is created by first selecting the mains line-to-line voltage with largest absolute value (u_{ac}) until $t = 0.5 - t_2$, followed by the line-to-line voltage with the second largest absolute value (u_{ab}) until $t = 0.5 - t_1$ and finally 0 V until $t = 0.5$. The same shape, but with inverted polarity, is used for the negative half wave $0.5 < t \leq 1$. This voltage u_p can be modeled as sum of three, 50 % duty cycle square-waves u_{p1}, u_{p2} and u_{p3}, with amplitudes of half the ac line-to-line voltages. The secondary-side voltage u_s is split into two 50 % duty cycle signals u'_{s1} and u'_{s2}. All times are normalized to the switching period T_{sw} and all secondary-side voltages are shown with respect to the primary-side, i.e. multiplied by the turns ratio n_p/n_s.

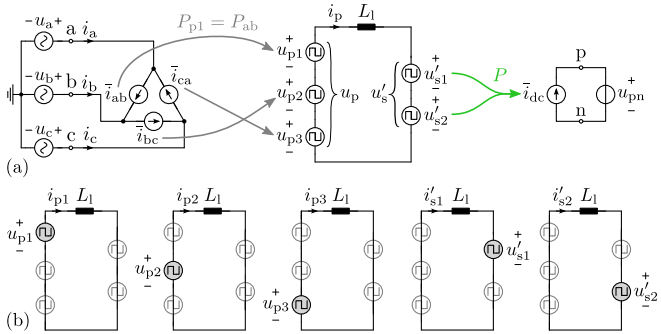

Fig. 7.4: (a) Equivalent circuit model where losses, voltage ripples and the magnetizing inductance are neglected, and all quantities are referred to the primary side. The winding voltage u_p is split into a sum of three voltages u_p1, u_p2 and u_p3 (cf. **Fig. 7.3**), which correspond to the instantaneous powers drawn from the three mains line-to-line voltages. This allows to calculate the local average values of the equivalent Δ-connection mains input currents, i.e. $\bar{i}_\mathrm{ab}$, $\bar{i}_\mathrm{bc}$ and $\bar{i}_\mathrm{ca}$. Likewise u'_s is split into u'_s1 and u'_s2, and the power received by these sources equals the power delivered to the output by the equivalent current source i_dc within a switching cycle. **(b)** The superposition principle is used to calculate i_p as sum of five components driven by the primary- and secondary-side voltage sources.

ones by t_4 as shown in **Fig. 7.3**. Like in a conventional DAB converter, u_p leads u'_s for a power transfer from the ac mains to the dc-side.

7.2.2 Calculation of Input and Output Currents

In the following derivation switching frequency voltage ripples, conduction losses and the transformer's magnetizing inductance are neglected. To calculate the transformer current i_p and the resulting mains currents $i_\mathrm{a,b,c}$, the primary-side voltage u_p is split into a sum of three 50 % duty cycle square-wave voltages u_p1, u_p2 and u_p3 as shown in **Fig. 7.4(a)**. The amplitude of u_p3 equals half of the mains line-to-line voltage with the highest absolute value (u_ac), the one of u_p2 is defined by the line-to-line voltage with lowest absolute value (u_bc) and the remaining line-to-line voltage (u_ab) determines

the amplitude of u_{p1}. This can be written as

$$u_{p1}(t) = u_{ab}\,\sigma(t + t_1) \quad , \tag{7.3}$$

$$u_{p2}(t) = u_{bc}\,\sigma(t + t_2) \quad \text{and} \tag{7.4}$$

$$u_{p3}(t) = u_{ac}\,\sigma(t) \quad \text{with} \tag{7.5}$$

$$\sigma(t) = \begin{cases} \frac{1}{2} & \text{if } 0 < (t \bmod 1) \leq \frac{1}{2} \\ -\frac{1}{2} & \text{if } \frac{1}{2} < (t \bmod 1) \leq 1 \end{cases} \quad . \tag{7.6}$$

Considering, for example, the interval $0 < t < 1/2 - t_2$ the three voltages u_{p1}, u_{p2} and u_{p3} are all positive, resulting in

$$u_p = \underbrace{\frac{u_{ac}}{2}}_{u_{p3}} + \underbrace{\frac{u_{ab}}{2}}_{u_{p1}} + \underbrace{\frac{u_{bc}}{2}}_{u_{p2}} = \frac{u_{ac}}{2} + \frac{u_{ac}}{2} = u_{ac} \quad , \tag{7.7}$$

which matches (7.1). In the same way u'_s is split into two square-waves given by

$$u'_{s1}(t) = u_{pn}\,(n_p/n_s)\,\sigma(t + t_3) \quad \text{and} \tag{7.8}$$

$$u'_{s2}(t) = \underbrace{u_{pn}\,(n_p/n_s)}_{u'_{pn}}\,\sigma(t + t_4) \quad . \tag{7.9}$$

As u_{p1} is the only voltage which depends on the mains voltage u_{ab}, the power P_{p1} delivered by u_{p1} can be used to calculate the average of the Δ-connected mains input current i_{ab} over one switching frequency period T_{sw} [cf. **Fig. 7.4(a)**]:

$$\bar{i}_{ab} = \frac{P_{ab}}{u_{ab}} = \frac{P_{p1}}{u_{ab}} = \frac{1}{u_{ab}} \int_0^1 u_{p1}(t) i_p(t)\,dt \quad . \tag{7.10}$$

In this chapter, a bar above a symbol, as in $\bar{i}_{ab}$, indicates the local average over one switching frequency period. Note that an alternative, more detailed, derivation of $\bar{i}_{ab}$ is described in **Section 7.2.3**.

Using (7.15) to (7.17), the resulting input currents for given voltages and switching times $\vec{t} = [t_1, t_2, t_3, t_4]$ can be calculated, which allows to calculate the resulting instantaneous reactive power Q [173, 174] as:

$$Q = \frac{-1}{\sqrt{3}} \left(u_a i_{bc} + u_b i_{ca} + u_c i_{ab}\right) \, . \tag{7.11}$$

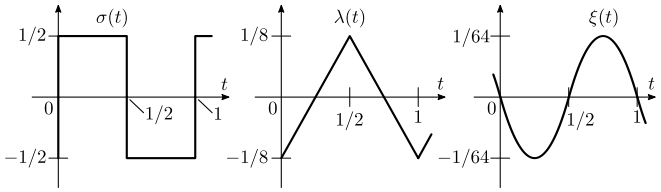

Fig. 7.5: Drawing of the auxiliary functions $\sigma(t)$, $\lambda(t)$ and $\xi(t)$ used in the derivation of mains and output current equations. Note that $\xi(t)$ is not sinusoidal, but consists of two quadratic functions.

In the ideal case, a PFC rectifier creates sinusoidal input currents, in phase with the mains voltages, which implies that no reactive power is created. Setting $Q = 0$ renders (7.11) an equality constraint that has to be fulfilled by the switching times $\vec{t}$.

The required transformer current $i_\mathrm{p}(t)$ can be found using superposition [cf. **Fig. 7.4(b)**]:

$$\begin{aligned} i_\mathrm{p}(t) = &\underbrace{\frac{u_\mathrm{ab}}{f_\mathrm{sw} L_\mathrm{l}} \lambda(t + t_1)}_{i_{\mathrm{p}1}(t)} + \underbrace{\frac{u_\mathrm{bc}}{f_\mathrm{sw} L_\mathrm{l}} \lambda(t + t_2)}_{i_{\mathrm{p}2}(t)} + \underbrace{\frac{u_\mathrm{ac}}{f_\mathrm{sw} L_\mathrm{l}} \lambda(t)}_{i_{\mathrm{p}3}(t)} \\ &+ \underbrace{\frac{-u'_\mathrm{pn}}{f_\mathrm{sw} L_\mathrm{l}} \lambda(t + t_3)}_{i'_{\mathrm{s}1}(t)} + \underbrace{\frac{-u'_\mathrm{pn}}{f_\mathrm{sw} L_\mathrm{l}} \lambda(t + t_4)}_{i'_{\mathrm{s}2}(t)} \quad , \end{aligned} \tag{7.12}$$

where each of the five individual current components has a triangular shape with 50 % duty cycle, as shown in **Fig. 7.5** and given by:

$$\begin{aligned} \lambda(t) &= \int_0^t \sigma(\tau)\, d\tau - \frac{1}{8} \\ &= \frac{1}{8} \begin{cases} -1 + 4t & \text{if } 0 < t \leq 1/2 \\ 3 - 4t & \text{if } 1/2 < t \leq 1 \end{cases} \quad . \end{aligned} \tag{7.13}$$

To solve the integral in (7.10), (7.13) can be integrated, resulting in the periodic

function $\xi(t)$ shown in **Fig. 7.5**:

$$\xi(t) = \int_0^t \lambda(\tau)\, d\tau = \frac{1}{8} \begin{cases} -t + 2t^2 & \text{if } 0 < t \leq 1/2 \\ -1 + 3t - 2t^2 & \text{if } 1/2 < t \leq 1 \end{cases}$$
$$= \frac{1}{8} \left[(t \bmod 1) - \frac{1}{2} \right] \left[1 - 2\left|(t \bmod 1) - \frac{1}{2}\right| \right] . \tag{7.14}$$

This allows to calculate the average of i_{ab} over one switching frequency period as

$$\bar{i}_{\mathrm{ab}} = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \left[u_{\mathrm{bc}}\, \xi(t_2 - t_1) + u_{\mathrm{ac}}\, \xi(0 - t_1) \right.$$
$$\left. - u'_{\mathrm{pn}}\, \xi(t_3 - t_1) - u'_{\mathrm{pn}}\, \xi(t_4 - t_1) \right] . \tag{7.15}$$

In almost the same manner, the remaining two average mains currents and the dc-side output current can be derived as

$$\bar{i}_{\mathrm{bc}} = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \left[u_{\mathrm{ab}}\, \xi(t_1 - t_2) + u_{\mathrm{ac}}\, \xi(0 - t_2) \right.$$
$$\left. - u'_{\mathrm{pn}}\, \xi(t_3 - t_2) - u'_{\mathrm{pn}}\, \xi(t_4 - t_2) \right] , \tag{7.16}$$

$$\bar{i}_{\mathrm{ca}} = \frac{2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \left[u_{\mathrm{ab}}\, \xi(t_1 - 0) + u_{\mathrm{bc}}\, \xi(t_2 - 0) \right.$$
$$\left. - u'_{\mathrm{pn}}\, \xi(t_3 - 0) - u'_{\mathrm{pn}}\, \xi(t_4 - 0) \right] \tag{7.17}$$

and

$$\bar{i}_{\mathrm{dc}} = \frac{-2}{f_{\mathrm{sw}} L_{\mathrm{l}}} \frac{n_{\mathrm{p}}}{n_{\mathrm{s}}} \left[u_{\mathrm{ab}}\, \xi(t_1 - t_3) + u_{\mathrm{ab}}\, \xi(t_1 - t_4) \right.$$
$$+ u_{\mathrm{bc}}\, \xi(t_2 - t_3) + u_{\mathrm{bc}}\, \xi(t_2 - t_4)$$
$$\left. + u_{\mathrm{ac}}\, \xi(0 - t_3) + u_{\mathrm{ac}}\, \xi(0 - t_4) \right] . \tag{7.18}$$

7.2.3 Alternative Derivation of the Mains Input Currents

An alternative and more detailed derivation of $\bar{i}_{\mathrm{ab}}$ is presented in the following. It can be seen in **Fig. 7.2(a)** and **Fig. 7.6** that switch $\mathrm{S_h}$ connects node h to the DMC's input terminal c during $0 \leq t \leq 1/2 - t_2$. This implies that the primary-side winding current i_{p} flows into terminal c during this interval.

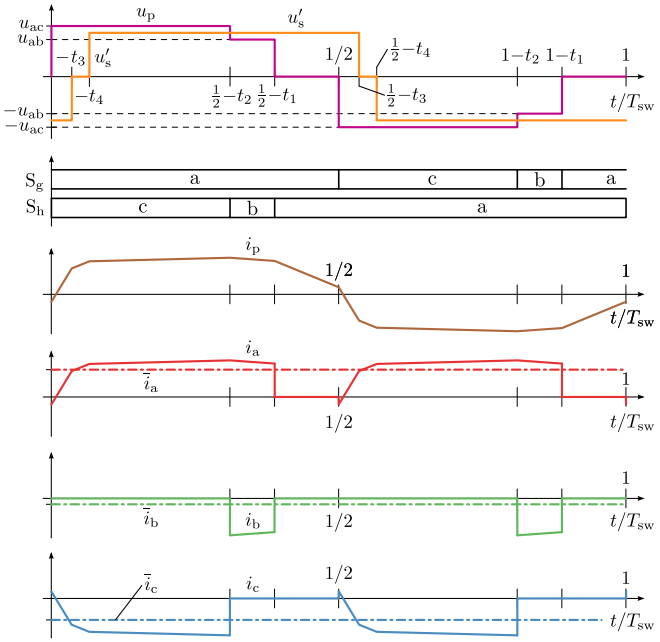

Fig. 7.6: Drawing (not to scale) of the DMC's input currents i_a, i_b and i_c during one switching frequency period. These would result as mains input currents if no EMI filter and no input filter capacitors C_f were installed. It can be seen that i_c equals $-i_p$ during $0 < t < 1/2 - t_2$ because the selector switch S_h [cf. **Fig. 7.2(a)**] connects node h to terminal c. Likewise i_b equals $-i_p$ during $1/2 - t_2 < t < 1/2 - t_1$.

Using the half-wave symmetry of i_p this allows to calculate the average of the DMC input current i_c over one switching frequency period as

$$\bar{i}_c = -2 \int_0^{1/2-t_2} i_p(t)\, dt \quad . \tag{7.19}$$

Note that the time t is normalized to the switching frequency period $T_{sw} = 1/f_{sw}$ and is therefore dimensionless. Inserting (7.12) we obtain:

$$\bar{i}_c = \frac{-2}{f_{sw} L_l} \int_0^{1/2-t_2} u_{ab}\lambda(t+t_1) + u_{bc}\lambda(t+t_2) + u_{ac}\lambda(t) - u'_{pn}\lambda(t+t_3) - u'_{pn}\lambda(t+t_4)\, dt \quad . \tag{7.20}$$

Using $\xi(t)$, the antiderivative of $\lambda(t)$ given in (7.14), integration by substitution yields:

$$\begin{aligned}\bar{i}_c = \frac{-2}{f_{\mathrm{sw}} L_1} \Bigg[& u_{\mathrm{ab}} \left(\xi(\frac{1}{2} - t_2 + t_1) - \xi(0 + t_1) \right) \\ & + u_{\mathrm{bc}} \left(\underbrace{\xi(\frac{1}{2} - t_2 + t_2)}_{\to 0} - \xi(0 + t_2) \right) \\ & + u_{\mathrm{ac}} \left(\xi(\frac{1}{2} - t_2) - \underbrace{\xi(0)}_{\to 0} \right) \\ & - u'_{\mathrm{pn}} \left(\xi(\frac{1}{2} - t_2 + t_3) - \xi(0 + t_3) \right) \\ & - u'_{\mathrm{pn}} \left(\xi(\frac{1}{2} - t_2 + t_4) - \xi(0 + t_4) \right) \Bigg] \quad . \end{aligned} \tag{7.21}$$

Considering (7.14) and **Fig. 7.5**, the following properties of $\xi(t)$ can be found:

$$\xi(0) = \xi\left(\frac{1}{2}\right) = \xi(1) = 0 \quad \text{and} \tag{7.22}$$

$$\xi\left(t + \frac{1}{2}\right) = -\xi(t) \quad . \tag{7.23}$$

This allows to write (7.21) as:

$$\begin{aligned}\bar{i}_c = \frac{2}{f_{\mathrm{sw}} L_1} \Big[& u_{\mathrm{ab}} \left(\xi(t_1 - t_2) + \xi(t_1) \right) \\ & + u_{\mathrm{bc}} \xi(t_2) \\ & + u_{\mathrm{ac}} \left(\xi(0 - t_2) \right) \\ & - u'_{\mathrm{pn}} \left(\xi(t_3 - t_2) + \xi(t_3) \right) \\ & - u'_{\mathrm{pn}} \left(\xi(t_4 - t_2) + \xi(t_4) \right) \Big] \quad . \end{aligned} \tag{7.24}$$

Using Kirchoff's current law on the left part of **Fig. 7.4(a)**, the current i_{c} can be calculated as:

$$\bar{i}_{\mathrm{c}} = \bar{i}_{\mathrm{ca}} - \bar{i}_{\mathrm{bc}} \quad . \tag{7.25}$$

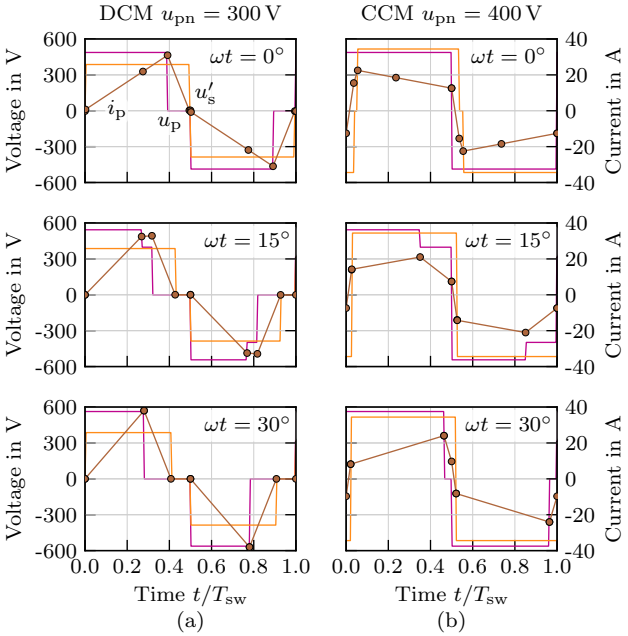

Fig. 7.7: Ideal transformer voltages and transformer current for $\bar{i}_{dc} = 20\,A$ and different mains voltage phase angles ωt. In **(a)** $u_{pn} = 300\,V$ is selected, which leads to discontinuous conduction mode (DCM) were an interval with $i_p = 0$ exists for $\omega t = 15°$ and $\omega t = 30°$. Note that u_{pn} is selected such that the plot for $\omega t = 0°$ shows the boundary case between DCM and continuous conduction mode (CCM). **(b)** Waveforms for nominal operating conditions as given in **Tbl. 7.1**, where the rectifier operates in CCM for all values of ωt.

Inserting (7.16) and (7.17) into (7.25) yields the same result as (7.24). Similar calculations can be performed for $\bar{i}_b$ and $\bar{i}_a$, but they are omitted here for the sake of brevity. This validates the results of the short derivation given above.

7.2.4 Conduction Loss Optimal PFC Modulation

It can be seen in the rectifier's schematic shown in **Fig. 7.1(b)**, that the transformer's primary winding current i_p is conducted by four DMC MOSFETs, irrespective of the DMC's conduction state. Similarly, two MOSFETs of the full-bridge conduct the secondary-side transformer current $i_s \approx i_p n_p/n_s$. Neglecting high-frequency effects such as skin and proximity losses, the semi-

conductor conduction and transformer winding losses are proportional to the square of the transformer rms current $I_{\mathrm{p,rms}}$. In the following a modulation scheme is derived which achieves sinusoidal input currents, in phase with the mains voltage, with minimal $I_{\mathrm{p,rms}}$.

The IMDAB3R's structure and its equivalent circuit [cf. **Fig. 7.2(b)**] are similar to a conventional DAB dc-dc converter for which analytic expressions of the conduction loss optimal switching times can be derived as described in [175]. Considering the special case $\omega t = 30°$, the mains line-to-neutral voltage u_{b} is zero [cf. **Fig. 7.2(c)**] and hence the rectifier must ensure $i_{\mathrm{b}} = 0$. This implies that line b is not selected by the DMC, resulting in $t_1 = t_2$. Therefore, u_{ac} is the only mains line-to-line voltage used by the DMC to create u_{p} and the rectifier operates like a conventional DAB dc-dc converter. Hence, the optimal switching times derived in [175] are also optimal for the IMDAB3R in this case. Corresponding waveforms for two different output voltages are shown in the bottom row of **Fig. 7.7**.

Discontinuous Conduction Mode

For low output currents i_{dc} and dc voltages u_{pn} higher or lower than the nominal value, these optimal switching times for $\omega t = 30°$ result in a discontinuous conduction mode (DCM) solution, where i_{p} is zero at the end of each half period at $t = 0$ and $t = 1/2$ as shown in **Fig. 7.7(a)**. Due to the similarity between the IMDAB3R and the conventional DAB dc-dc converter, it can be assumed that DCM yields the conduction loss optimal switching times for other mains phase angles ωt as well, for output currents i_{dc} below the threshold $i_{\mathrm{dc,DCM,max}}$. For the sake of clarity, DCM switching times are written as $t_{k\mathrm{D}}$, $k \in \{1, 2, 3, 4\}$, in the following.

DCM is characterized by aligned rising or falling edges of u_{p} and u'_{s} and a volt-second balance between primary and secondary-side,

$$u_{\mathrm{ab}} \left(\frac{1}{2} - t_{1\mathrm{D}} \right) + u_{\mathrm{bc}} \left(\frac{1}{2} - t_{2\mathrm{D}} \right) = u'_{\mathrm{pn}} \left(\frac{1}{2} - t_{3\mathrm{D}} - t_{4\mathrm{D}} \right), \tag{7.26}$$

which leads to $i_{\mathrm{p}}(t) = 0$ at $t = 0$ and $t = 0.5$. Note that this results in zero current switching (ZCS). For output currents i_{dc} lower than $\bar{i}_{\mathrm{dc,DCM,max}}$ an interval with i_{p} identical to zero can be inserted before $t = 0.5$ and $t = 1$ as shown in **Fig. 7.7(a)** for mains voltage phase angles $\omega t = 15°$ and $\omega t = 30°$. The calculation of $\bar{i}_{\mathrm{dc,DCM,max}}$ is described in the following. Numerical results are plotted in **Fig. 7.10** as function of ωt and the dc output voltage u_{pn}.

Depending on u_{pn}, either the rising or falling edges of u_{p} and u'_{s} have to be aligned in DCM, as shown in **Fig. 7.9(a)** to **(c)**. The boundary voltage $u'_{\mathrm{pn,b}}$,

for which rising and falling edges are aligned, can be calculated by setting $Q = 0$ to achieve PFC operation and selecting $t_{1D} = t_{3D}$ and $t_{4D} = 0$ to align rising and falling edges. Using (7.11) and (7.26) an analytic expression for $u'_{pn,b}$ can be derived as

$$u'_{pn,b} = 2\,\frac{u_{ab}^2 + u_{ab}u_{bc} + u_{bc}^2}{2u_{ab} + u_{bc}} \quad . \tag{7.27}$$

A plot of $u'_{pn,b}$ as function of ωt is shown in **Fig. 7.9(d)** for nominal mains voltage $U_1 = 230\,\mathrm{V}$ rms.

To calculate the maximum output current achievable in DCM ($\bar{i}_{dc,DCM,max}$) for low output voltage ($u'_{pn} \le u'_{pn,b}$), the duty cycle of u'_s is maximized and the rising edges of the transformer voltages are aligned by selecting $t_{3D} = t_{4D} = 0$. Equations (7.11) and (7.26) can then be solved by a computer algebra system for the required primary-side switching time t_{1D} to achieve $Q = 0$:

$$e_1 = u_{ab}^2 + u_{ab}u_{bc} + u_{bc}^2 \tag{7.28}$$

$$e_2 = u_{ab} + u_{bc} - u'_{pn} \tag{7.29}$$

$$e_3 = e_2\,(u_{ab} + 2u_{bc})\left(2e_1 - u'_{pn}\,(2u_{ab} + u_{bc})\right) \tag{7.30}$$

$$e_4 = u'_{pn}\left(2u_{ab}^2 + 3u_{ab}u_{bc} + 2u_{bc}^2\right) \tag{7.31}$$

$$t_{1D} = \frac{u_{ab}e_2\left(2e_1 - (2u_{ab} + u_{bc})u'_{pn}\right) + u_{bc}u'_{pn}\sqrt{e_3}}{4u_{ab}(u_{ab} + u_{bc})e_1 - 2(u_{ab} - u_{bc})e_4} \,, \tag{7.32}$$

where terms e_1 to e_4 are intermediate values without a physical interpretation. Finally, the remaining DCM switching time t_{2D} can be calculated as

$$t_{2D} = \frac{1}{2} - \begin{cases} \frac{1}{\sqrt{2}}\left(\frac{1}{2} - t_{1D}\right) & \text{if } u_{bc} = 0 \\ \left(\frac{u'_{pn}}{2} - u_{ab}(\frac{1}{2} - t_{1D})\right)\frac{1}{u_{bc}} & \text{if } u_{bc} > 0 \end{cases} \,, \tag{7.33}$$

which allows to evaluate (7.18) to find $\bar{i}_{dc,DCM,max}$. Example waveforms for $u_{ab} = 398\,\mathrm{V}$, $u_{bc} = 146\,\mathrm{V}$ ($\omega t = 15°$) and $u'_{pn} = 300\,\mathrm{V}$ are shown in **Fig. 7.9(a)**.

Note that in the special case $u_{pn} = 0$ the equation above results in $t_{1D} = t_{2D} = 1/2$, which results in $\bar{i}_{dc,DCM,max} = 0$. To create the desired dc output current i^*_{dc} in this case, a trapezoidal winding current i_p is created by selecting $t_2 = t_1$ as shown in **Fig. 7.8**. The secondary-side full-bridge switches are controlled with 50 % duty cycle signals that lead u_p by 1/4 (i.e. 90°):

$$t_3 = t_4 = \frac{t_1}{2} - \frac{1}{4} \quad , \tag{7.34}$$

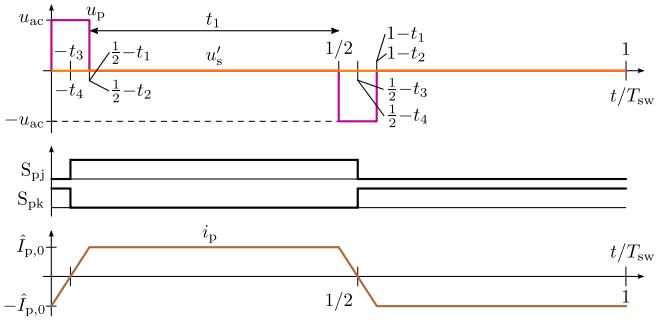

Fig. 7.8: Drawing (not to scale) of the transformer voltages u_p and u'_s and the primary-side winding current i_p for $u'_{pn} = 0$. In this case $t_1 = t_2$ and $t_3 = t_4$ is selected, irrespective of the mains voltage phase angle ωt.

and the amplitude $\hat{I}_{p,0}$ of i_p can be calculated as

$$\hat{I}_{p,0} = \frac{1}{2}\frac{u_{ac}}{f_{sw} L_1}\left(\frac{1}{2} - t_1\right) . \tag{7.35}$$

This allows to calculate the resulting dc output current as

$$\bar{i}_{dc} = \hat{I}_{p,0}\left(2\,t_1 + \frac{1}{2} - t_1\right) . \tag{7.36}$$

By setting $\bar{i}_{dc} = i^*_{dc}$, the required switching time value t_1 can be found as

$$t_2 = t_1 = \sqrt{\frac{1}{4} - 2\frac{i^*_{dc}\, f_{sw}\, L_1}{u_{ac}}} . \tag{7.37}$$

For $u'_{pn} \geq u'_{pn,b}$ the primary voltage's duty cycle is maximized by selecting $t_{1D} = 0$ and the falling edges of the transformer voltages are aligned by selecting $t_{3D} = 0$. Again (7.11) and (7.26) can be used to find analytic expression

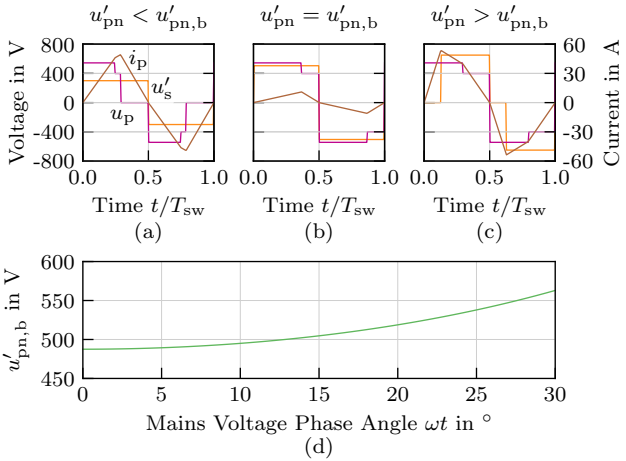

Fig. 7.9: Transformer voltages and transformer current for $\omega t = 15°$, operating with maximum output current $i_{dc,DCM,max}$ possible in DCM. In **(a)** the output voltage $u'_{pn} = 300\,V$ is lower than the boundary value $u'_{pn,b} = 505\,V$ and therefore the duty cycle of u'_s is maximal and the rising edges of u_p and u'_s are aligned. **(b)** Shows the case $u'_{pn} = u'_{pn,b}$, where both u_p and u'_s use the maximum possible duty cycle. **(c)** For $u'_{pn} = 650\,V > u'_{pn,b}$ only the duty cycle of u_p is maximal and the falling edges are aligned. In **(d)** $u'_{pn,b}$ is plotted as a function of the mains voltage phase angle ωt for nominal input voltage $U_1 = 230\,V$ rms line-to-neutral.

of the switching times t_{2D} and t_{4D} for DCM with high output voltage as

$$e_5 = u'_{pn}\,(2u_{ab} + u_{bc}) \quad , \tag{7.38}$$

$$e_6 = u'_{pn}\left(u_{ab}^2 - u_{bc}^2\right)\left(u_{ab} - u'_{pn}\right)(2e_1 - e_5) \quad , \tag{7.39}$$

$$t_{2D} = \frac{1}{2}\,\frac{u_{bc}^3 - u_{ab}^2 u_{bc} - \sqrt{e_6}}{u_{bc}^2(u_{bc} - u_{ab}) + (2u_{ab}^2 + u_{bc}^2 - e_5)u'_{pn}} \, , \tag{7.40}$$

$$t_{4D} = \frac{u_{ab}}{2u'_{pn}} + \frac{u_{bc}}{u'_{pn}}\left(\frac{1}{2} - t_{2D}\right) - \frac{1}{2} \quad . \tag{7.41}$$

This defines the four switching times for DCM operation with maximum output current for high u'_{pn} and (7.18) can be evaluated to calculate $\bar{i}_{dc,DCM,max}$ in this case. An example waveform for this case is shown in **Fig. 7.9(c)**. Note that in the corner case $u'_{pn} = u'_{pn,b}$ the solutions obtained for low and high

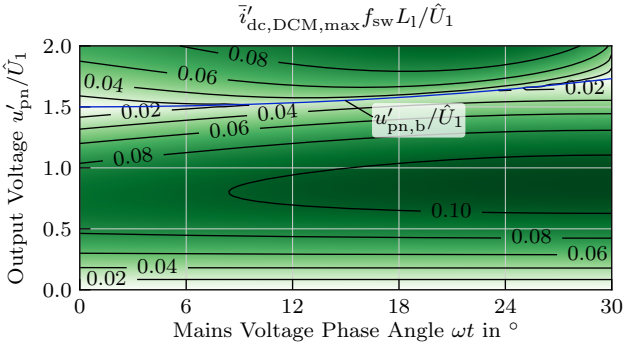

Fig. 7.10: Contour plot of the maximal output current $\bar{i}'_{\mathrm{dc,DCM,max}}$ achievable in DCM, referenced to the primary-side and normalized by multiplication with $f_{\mathrm{sw}}L_1/\hat{U}_1$, as function of the mains voltage phase angle ωt and the normalized dc voltage (w.r.t. to the primary side) $u'_{\mathrm{pn}}/\hat{U}_1$. Also shown is the boundary voltage $u'_{\mathrm{pn,b}}$, normalized to $\hat{U}_1$, as function of ωt.

output voltages coincide, yielding the waveform shown in **Fig. 7.9(b)**.

In **Fig. 7.10** $\bar{i}_{\mathrm{dc,DCM,max}}$ is plotted as function of the input output voltage ratio $u'_{\mathrm{pn}}/\hat{U}_1$ and the mains voltage phase angle ωt. To create a generic plot that is applicable to any converter, $\bar{i}_{\mathrm{dc,DCM,max}}$ is referenced to the primary side and normalized by multiplying with $f_{\mathrm{sw}}L_1/\hat{U}_1$. Additionally, the boundary voltage $u'_{\mathrm{pn,b}}(\omega t)$ is plotted, normalized to $\hat{U}_1$. It can be seen that only relatively low output currents can be achieved in DCM for low values of u'_{pn} and if u'_{pn} is close to $u'_{\mathrm{pn,b}}$, which is also the case in a conventional DAB dc-dc converter [175].

The solutions obtained above yield the switching times for the maximum dc output current in DCM. If a current i^*_{dc} lower than $i_{\mathrm{dc,DCM,max}}$ has to be created an interval with $i_{\mathrm{p}} = 0$ can be inserted before the end of each half-cycle by rescaling the switching times as

$$t_k(i^*_{\mathrm{dc}}) = \frac{1}{2} - \left(\frac{1}{2} - t_{k\mathrm{D}}\right)\sqrt{\frac{i^*_{\mathrm{dc}}}{\bar{i}_{\mathrm{dc,DCM,max}}}} \quad k \in \{1,2,3\}\,, \tag{7.42}$$

$$t_4(i^*_{\mathrm{dc}}) = t_{4\mathrm{D}}\sqrt{\frac{i^*_{\mathrm{dc}}}{\bar{i}_{\mathrm{dc,DCM,max}}}}\quad . \tag{7.43}$$

Note that the switching times are not proportional to i^*_{dc} but to its square

root. This is because introducing an interval with $i_\mathrm{p} = 0$ reduces the time during which power is transferred between primary and secondary side and simultaneously reduces the amplitude of i_p.

Continuous Conduction Mode

Output currents i_dc^* larger than $\bar{i}_{\mathrm{dc,DCM,max}}$ cannot be achieved with DCM, but by CCM. This implies that (7.26), the volt-second balance between u_p and u_s', no longer holds within a switching half-cycle. With the output current reference value i_dc^* two equality constraints are defined:

$$\bar{i}_\mathrm{dc}\left(u_\mathrm{ab}, u_\mathrm{bc}, u_\mathrm{pn}, \vec{t}\,\right) = i_\mathrm{dc}^* \quad , \tag{7.44}$$

$$Q\left(u_\mathrm{ab}, u_\mathrm{bc}, u_\mathrm{pn}, \vec{t}\,\right) = 0 \quad , \tag{7.45}$$

for four unknown switching times $\vec{t}$. Like in the conventional DAB dc-dc converter, the additional degrees of freedom offered by the modulation can be used to select a solution which achieves minimal conduction losses by minimizing the squared rms value of transformer current $I_\mathrm{p,rms}^2$. This value can be found by calculating the complex valued Fourier series coefficients c_k of i_p defined in (7.12):

$$\begin{aligned} c_k = \frac{-1}{2\pi^2 k^2 f_\mathrm{sw} L_\mathrm{1}} \big[& u_\mathrm{ab}\, e^{j2\pi k t_1} + u_\mathrm{bc}\, e^{j2\pi k t_2} + u_\mathrm{ac}\, e^{0} \\ & - u_\mathrm{pn}' \left(e^{j2\pi k t_3} + e^{j2\pi k t_4} \right) \big] \quad , \end{aligned} \tag{7.46}$$

for odd values of k. An approximation of $I_\mathrm{p,rms}^2$ can then be found by summing the first M odd harmonics:

$$I_\mathrm{p,rms}^2 \approx 2 \sum_{m=1}^{M} c_{2m-1}\, c_{2m-1}^* \quad . \tag{7.47}$$

Choosing M between 10 and 100 typically leads to sufficiently precise results. While it might be possible to minimize $I_\mathrm{p,rms}^2$ using analytical methods, no closed form solution could be obtained. Instead, numerical optimization algorithms such as Sequential Quadratic Programming (SQP) can be used to find switching times $\vec{t}$ that minimize (7.47) subject to the equality constraints (7.44) and (7.45) [176]. Resulting CCM waveforms for nominal operating conditions and different mains voltage phase angles are shown in **Fig. 7.7(b)**.

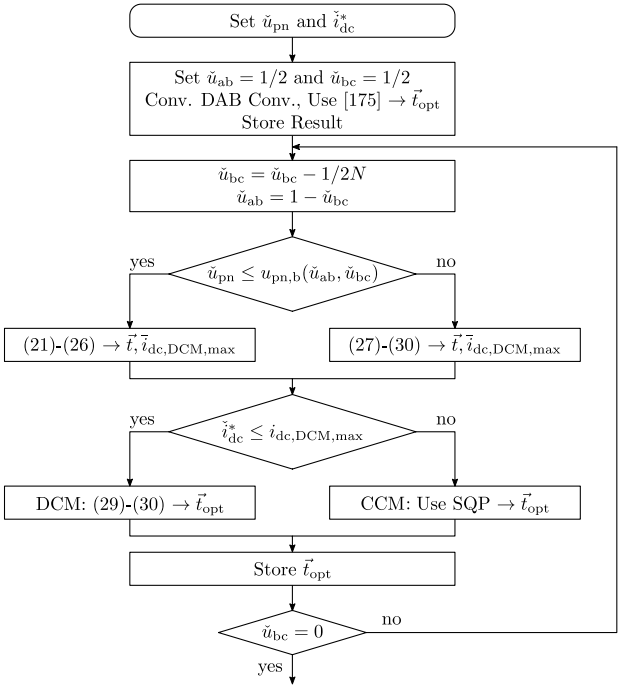

Fig. 7.11: Algorithm used to calculate the conduction loss optimal switching times $\vec{t}_{\mathrm{opt}}$ for given normalized dc voltage $\check{u}'_{\mathrm{pn}}$, a normalized output current reference $\check{i}^{*}_{\mathrm{dc}}$ and N values of $\check{u}_{\mathrm{bc}}$ in the range $[0, 1/2]$. The calculation starts with $\check{u}_{\mathrm{bc}} = 1/2$ ($\omega t = 30°$) in which case the rectifier operates like a conventional DAB dc-dc converter, using analytic equations published in [175]. For all following points DCM is used if possible ($\check{i}^{*}_{\mathrm{dc}}$ less than the maximum DCM output current $\bar{i}_{\mathrm{dc,DCM,max}}$), otherwise numerical optimization (SQP) is used to obtain a CCM solution, using the previous switching times as starting point for the optimizer.

7.2.5 Normalized Lookup Table

The computing power and memory required for numerical optimization algorithms typically render them unsuitable for real-time execution in a microcontroller used to control a PFC rectifier. Instead, the optimization is performed off-line and the resulting optimal switching times $\vec{t}_{\mathrm{opt}}$ are stored

in a lookup table (LUT). By using the normalizations:

$$\check{u}_{\mathrm{bc}} = u_{\mathrm{bc}} \frac{1}{u_{\mathrm{ac}}} \quad , \tag{7.48}$$

$$\check{u}'_{\mathrm{pn}} = u_{\mathrm{pn}} \frac{n_{\mathrm{p}}}{n_{\mathrm{s}}} \frac{1}{u_{\mathrm{ac}}} \quad , \tag{7.49}$$

$$\check{i}^*_{\mathrm{dc}} = i^*_{\mathrm{dc}} \frac{n_{\mathrm{s}}}{n_{\mathrm{p}}} \frac{1}{I_{\mathrm{nom}}} \quad I_{\mathrm{nom}} = \frac{u_{\mathrm{ac}}}{f_{\mathrm{sw}} L_{\mathrm{1}}} \quad , \tag{7.50}$$

the LUT becomes independent of converter specifications such as nominal voltage levels, $n_{\mathrm{p}}/n_{\mathrm{s}}$, f_{sw}, L_{1}, etc. Equations (7.48) to (7.50) again refer to sector 1 of the mains voltage, where $u_{\mathrm{ac}} > u_{\mathrm{ab}} \geq u_{\mathrm{bc}} \geq 0$ holds, and therefore a division by u_{ac} is possible. Equations (7.48) to (7.50) are a complete description of the rectifier's operating conditions, hence a three-dimensional LUT is required. In the following, a LUT with $N = 30$ sampling points per dimension is considered, resulting a total of 27000 entries, each consisting of four switching time values. As the measured voltages and the requested i^*_{dc} will typically not coincide exactly with the sampling points of the LUT, trilinear interpolation is used to obtain near-optimal switching times during operation.

To improve the convergence of the numerical optimizer used in CCM, the algorithm outlined in **Fig. 7.11** is used to calculate the LUT. For each pair of normalized dc voltage $\check{u}_{\mathrm{pn}}$ and output current $\check{i}^*_{\mathrm{dc}}$ values, $\omega t = 30°$ ($\check{u}_{\mathrm{ab}} = 1/2$ and $\check{u}_{\mathrm{bc}} = 0$) is considered first as the converter operates like a conventional DAB dc-dc converter in this case. The closed form solution published in [175] is used to calculate the conduction loss optimal switching times $\vec{t}_{\mathrm{opt}}$. In the next step, $\check{u}_{\mathrm{bc}}$ is reduced by $1/2N$ and the highest achievable output current in DCM $\bar{i}_{\mathrm{dc,DCM,max}}$ is calculated. If i^*_{dc} is less or equal to $\bar{i}_{\mathrm{dc,DCM,max}}$ the closed form solutions described in **Section 7.2.4** are used to calculate $\vec{t}_{\mathrm{opt}}$, otherwise a numerical optimizer (SQP) is used and the switching times $\vec{t}_{\mathrm{opt}}$ obtained for the previous point are used as initial guess. The resulting $\vec{t}_{\mathrm{opt}}$ is stored and the calculation continues with the next value $\check{u}_{\mathrm{bc}}$, until $\check{u}_{\mathrm{bc}} = 0$ is reached. The proposed algorithm was implemented in Scientific Python and requires less than five minutes to calculate a complete LUT with a resolution of $N = 30$ on a standard desktop computer [177, 178]. This implementation is available online under an open source license [179].

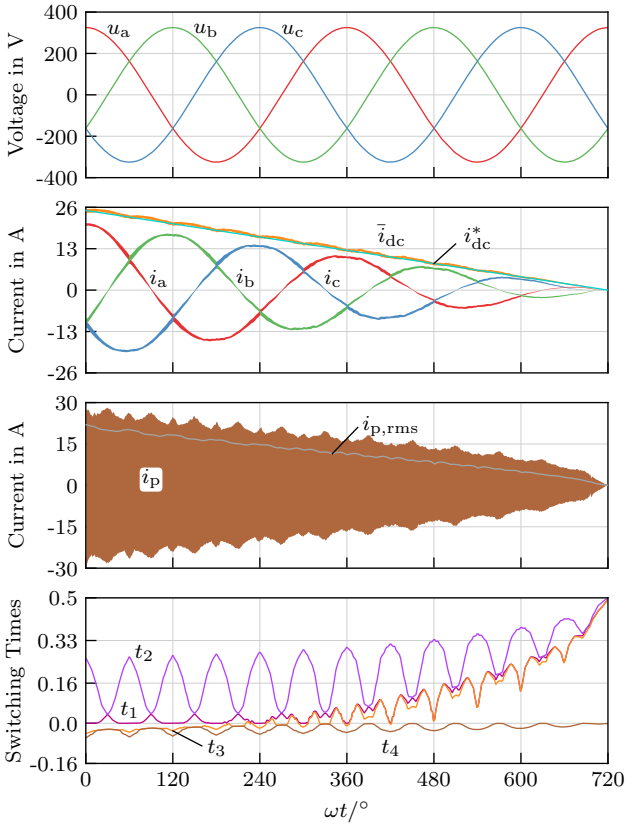

Fig. 7.12: Simulation results for a linearly decreasing output current reference signal i^*_{dc} with nominal ac and dc voltages. It can be seen that the actual output current i_{dc} tracks the reference closely and that sinusoidal mains currents i_a, i_b and i_c with a linearly decreasing amplitude result. The primary transformer current i_p, its local rms value (first-order low-pass, cut-off frequency 2.7 kHz) and the four switching times $\vec{t}$ are shown as well.

7.2.6 Properties of the Modulation Scheme

Varying DC Voltage and Current

Simulation results using the calculated LUT are shown in **Fig. 7.12** with a constant nominal dc voltage of $u_{\mathrm{pn}} = 400\,\mathrm{V}$ and a output current reference i_{dc}^{*} reducing linearly from 25 A to 0 A within two mains voltage periods. The nominal switching frequency of 31 kHz is used in this simulation. It can be seen that the first-order low-pass filtered output current $\bar{i}_{\mathrm{dc}}$ (cut-off frequency 2.7 kHz) of the secondary-side full-bridge follows the reference signal closely. Nearly sinusoidal mains currents, in phase with the mains voltages and with a linearly decreasing amplitude result. Further shown are the primary-side transformer current i_{p} (magnetizing inductance neglected) and its local rms value which also decreases almost linearly with i_{dc}^{*}.

In **Fig. 7.13** similar simulation results are shown for a fixed output current reference of $i_{\mathrm{dc}}^{*} = 20\,\mathrm{A}$, with a dc voltage ramping down linearly from $u_{\mathrm{pn}} = 500\,\mathrm{V}$ to $u_{\mathrm{pn}} = 0\,\mathrm{V}$. Again, sinusoidal mains input currents with linearly decreasing amplitude result and the first-order low-pass filtered secondary-side full-bridge output current $\bar{i}_{\mathrm{dc}}$ remains close to the set point i_{dc}^{*} independent of u_{pn}. Together **Fig. 7.12** and **Fig. 7.13** demonstrate that the proposed modulation scheme achieves sinusoidal mains input currents i_{a}, i_{b} and i_{c} for different output voltages, mains voltage phase angles and dc currents. Numerical analysis of the LUT shows that sinusoidal input currents, in phase with the mains voltage, are achieved, regardless of the input/output voltage ratio and the output current. This verifies that the modulation scheme is suitable for the implementation of a three-phase PFC rectifier.

Transformer rms Current

It can be seen in the third plot of **Fig. 7.13**, that the peak and rms values of the transformer current i_{p} change as function of u_{pn} and the mains voltage phase angle, even though the output current i_{dc} is basically constant. Relatively low peak and rms currents result for u_{pn} values close to the nominal dc voltage of 400 V, as the transformer turns ratio given in **Tbl. 7.1** is chosen accordingly. For higher ($\approx 500\,\mathrm{V}$) and lower ($\approx 200\,\mathrm{V}$) dc voltages the converter operates in DCM, resulting in triangular current waveforms [cf. **Fig. 7.7(a)**] that cause higher rms and peak currents than the trapezoidal current waveforms used in CCM [cf. **Fig. 7.7(b)**].

Assuming purely sinusoidal mains voltages and neglecting the magnetizing current, the rms value of i_{p} over a full mains voltage period can be

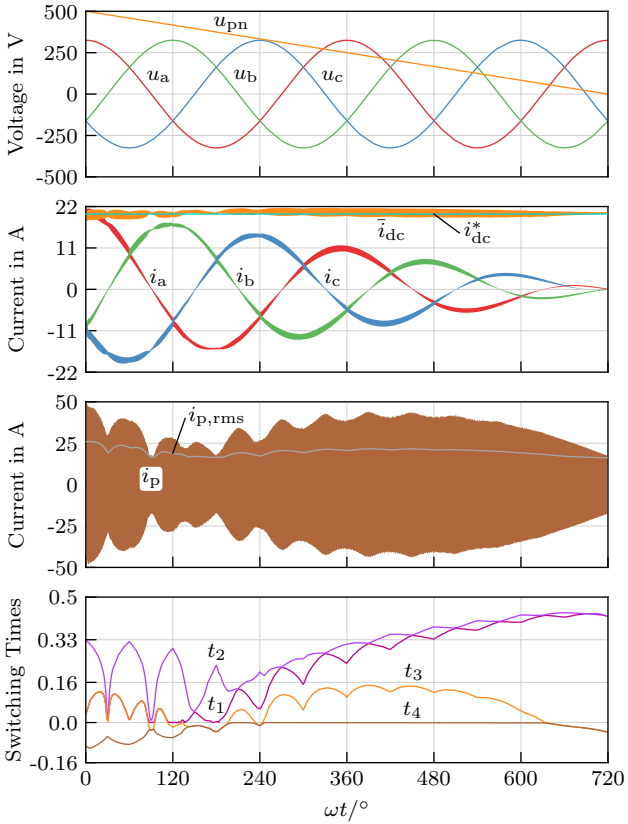

Fig. 7.13: Simulation results with a constant dc current reference $i^*_{dc} = 20$ A for a dc voltage which decreases linearly from $u_{pn} = 500$ V to 0 V. The low-pass filtered actual dc current $\bar{i}_{dc}$ (first-order, 2.7 kHz cut-off frequency) stays close to i^*_{dc} for all values of u_{pn}.

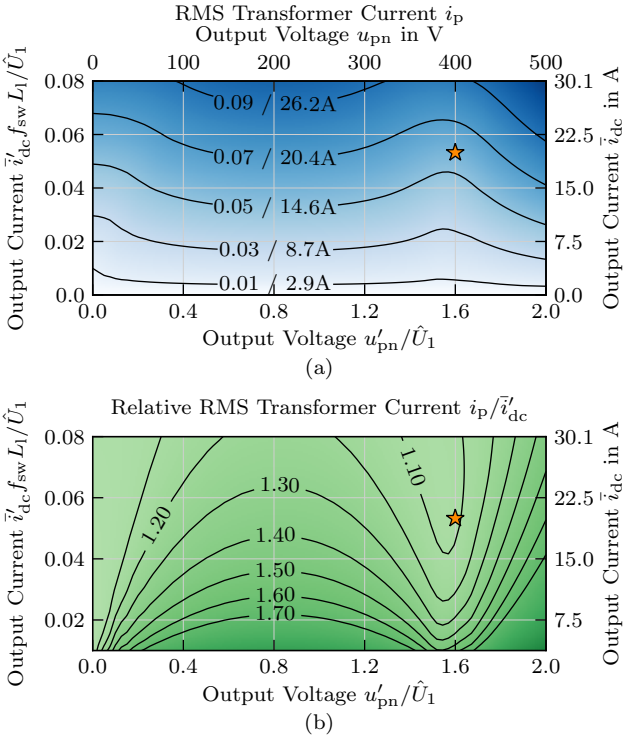

Fig. 7.14: (a) RMS value of the primary-side transformer current i_p (normalized by $f_{sw}{}^{L_1}/_{\hat{U}_1}$), as function of the normalized output voltage ${}^{u'_{pn}}/_{\hat{U}_1}$ and the output current $\bar{i}'_{dc} = \bar{i}_{dc}{}^{n_s}/_{n_p}$ (w.r.t. the primary side) normalized by $f_{sw}{}^{L_1}/_{\hat{U}_1}$. For reference, denormalized voltage and current values with $\hat{U}_1 = 325\,\mathrm{V}$ are shown at the top and right axes. **(b)** Ratio of the rms value of i_p to the dc current, w.r.t the primary side, as function of u_{pn} and output current. The orange asterisks indicate nominal operating conditions (cf. **Tbl. 7.1**).

calculated as function of two parameters: The voltage transfer ratio $u'_{pn}/\hat{U}_1$ between the dc voltage (w.r.t. to the primary side) and the mains voltage amplitude $\hat{U}_1$, and the output current with respect to the primary side $\bar{i}'_{dc} = \bar{i}_{dc}{}^{n_s}/_{n_p}$, normalized by $I_{norm} = {}^{\hat{U}_1}/_{f_{sw}L_1}$. The calculated normalized and denormalized values (for $\hat{U}_1 = 325\,\mathrm{V}$) are plotted in **Fig. 7.14(a)** with the nominal operating conditions marked by an orange asterisk. Additionally, **Fig. 7.14(b)** shows the ratio between the rms value of i_p and the output current w.r.t. the primary

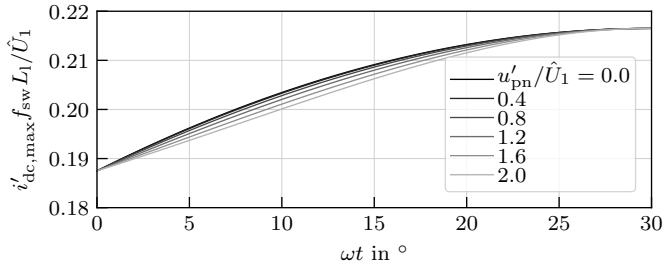

Fig. 7.15: Normalized maximum output current $\bar{i}'_{\mathrm{dc,max}}$ (w.r.t. primary side) as a function of the mains voltage phase angle ωt (only sector 1 considered) for different voltage transfer ratios $u'_{\mathrm{pn}}/\hat{U}_1$ in the range $[0, 2]$. It can be seen that for all voltage transfer ratios the minimum occurs at $\omega t = 0$ and that its value ($3/16 = 0.1875$) is independent of $u'_{\mathrm{pn}}/\hat{U}_1$.

side $\bar{i}'_{\mathrm{dc}}$, which describes the scaling of conduction losses in the switches and transformer windings with $\bar{i}_{\mathrm{dc}}$. For a given $\bar{i}'_{\mathrm{dc}}$, the transformer current i_{p} becomes minimal at $u_{\mathrm{pn}} = 0$, which is the trivial case as no power is transferred to the output, and for voltage transfer ratios $u'_{\mathrm{pn}}/\hat{U}_1$ in range the of 1.5 to 1.6. In this case the average six-pulse rectified mains voltage is close to u'_{pn}, which implies that CCM is used through most or all phase angles ωt of the mains voltage, leading to lower rms values of i_{p} than DCM which dominates for lower and higher voltage transfer ratios (cf. **Fig. 7.10**).

Output Current Limit

As in a conventional DAB dc-dc converter, the maximum power that can be transferred between primary and secondary, and hence the maximum output current, is limited and depends on the input and output voltages, L_1 and f_{sw}. This is also the case for the IMDAB3R, where the maximum output current $i_{\mathrm{dc,max}}$ also depends on the mains voltage phase angle ωt. To achieve PFC operation, only output currents less or equal to the lowest value of $\bar{i}_{\mathrm{dc,max}}$ over all ωt can be used. For given $\hat{U}_1$, u_{pn} and ωt, $\bar{i}_{\mathrm{dc,max}}$ can be found by numerically maximizing (7.18) subject to (7.45), which ensures that the input currents are in phase with the mains voltages. The resulting $\bar{i}_{\mathrm{dc,max}}$, referenced to the primary side and normalized by $f_{\mathrm{sw}} L_1/\hat{U}_1$, is plotted in **Fig. 7.15** as function of ωt for different voltage transfer ratios $u'_{\mathrm{pn}}/\hat{U}_1$. It can be seen that $\bar{i}'_{\mathrm{dc,max}} f_{\mathrm{sw}} L_1/\hat{U}_1$ reaches the minimum of $3/16 = 0.1875$ for $\omega t = 0$,

irrespective of $u'_{\mathrm{pn}}/\hat{U}_1$. This is because the largest line-to-line mains voltage (u_{ab} in sector 1) reaches its minimum of $1.5\,\hat{U}_1$ for $\omega t = 0$ [cf. **Fig. 7.2(c)**], which implies that the input voltage available for power transfer is minimal in this case. However, operation with output currents $\bar{i}'_{\mathrm{dc}}$ close to the limit $\bar{i}'_{\mathrm{dc,max}}$ is typically not feasible as, like in a conventional DAB converter, high phase shift angles close to 90° between primary and secondary side result, leading to a high reactive power due to L_1 and hence to a high rms value of i_{p}.

7.3 Design and Implementation

Conversion losses and the required operating room temperature conditioning and/or cooling are typically significant cost factors in applications that require 24/7 operation, such as data center and telecommunication power supplies. Very efficient rectifiers are therefore highly desirable in this case [133,134]. Accordingly, an IMDAB3R prototype is designed, striving for the highest possible efficiency at nominal operating conditions, to demonstrate the achievable performance and to serve as a benchmark for comparative evaluations of future research results.

It can be seen in **Fig. 7.14(b)** that the rms value of winding current i_{p} required to create a certain output current $\bar{i}_{\mathrm{dc}}$ changes significantly with the ratio between output voltage times turns ratio $u_{\mathrm{pn}}{}^{n_{\mathrm{p}}}/_{n_{\mathrm{s}}}$ and the mains voltage amplitude $\hat{U}_1$. Therefore the turns ratio should be chosen such that $u'_{\mathrm{pn}}/\hat{U}_1$ is within, or close to, the range 1.5 to 1.6 for the operating points were the highest efficiency is desired. Furthermore, it can be seen in **Fig. 7.14(b)** that higher normalized output currents $\bar{i}_{\mathrm{dc}} f_{\mathrm{sw}} L_1/\hat{U}_1$ lead to lower rms values of i_{p} for a given (denormalized) output current $\bar{i}_{\mathrm{dc}}$. This implies that the winding current's rms value decreases with increasing inductance L_1 and/or switching frequency f_{sw}. However, increasing the product $f_{\mathrm{sw}} L_1$ also reduces the maximum output current $\bar{i}_{\mathrm{dc,max}}$.

For the sake of brevity, the performed optimizations cannot be described in full detail, and instead the main steps of the design and implementation are presented in the following.

7.3.1 Considered Design

In **Fig. 7.16(a)** the schematic of the IMDAB3R considered in this section is shown and the implemented EMI input filter is shown in **Fig. 7.16(b)**. Like for conventional DAB dc-dc converters, the required inductance L_1 can either be implemented as a separate component, using an own magnetic core, or

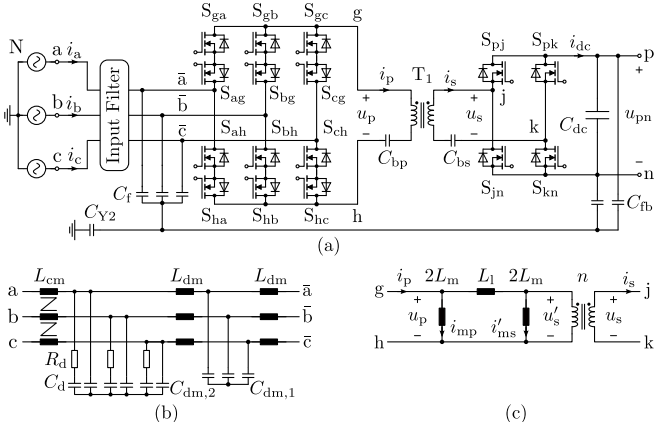

Fig. 7.16: (a) Schematic of the implemented IMDAB3R prototype, using 900 V, 10 mΩ SiC MOSFETs and an isolation transformer T_1 with built-in inductance L_l. **(b)** shows the implemented two-stage EMI filter and **(c)** shows the Π-type equivalent circuit model of the transformer, with the three parameters L_l, L_m and n. It can be used to calculate the primary- and secondary-side winding currents i_p and i_s, including the magnetizing current caused by the finite magnetizing inductance L_m.

Tbl. 7.2: Selected Components

DMC	*C3M0010090K* 900 V, 10 mΩ
Full-Bridge	*C3M0010090K* 900 V, 10 mΩ
C_{dc}	9× B32774D4106, 10 µF, 450 V
C_f	3× WE 890334026030CS, 1.5 µF, 310 V, X2 rated
C_{bp}	14× KTS500B156M55N0T00, 15 µF, 50 V
C_{bs}	10× KTS250B156M43N0T00, 15 µF, 25 V
T_1	see **Tbl. 7.3**
EMI Filter	see **Tbl. 7.4**

it can be built into the isolation transformer. The later is selected for the prototype, as this simplifies the mechanical design and eliminates the losses and volume resulting from wire terminations, screws or solder contacts etc.

Ideally, the modulation scheme described in the previous chapter creates winding voltages u_p and u_s that have no dc or low-frequency components. However, due to nonidealities such as varying delay times, voltage ripples and/or measurement errors, low-frequency components might occur. These

would lead to circulating winding currents, causing additional losses and potentially saturating the transformer. To avoid these currents, low-voltage blocking capacitors C_{bp} and C_{bs} are connected in series with the transformer windings.

Tbl. 7.2 lists the main components selected for the IMDAB3R prototype.

7.3.2 Transformer

The transformer's parameters (L_{l}, L_{m} and n) significantly influence the winding currents i_{p} and i_{s}, which determine the conducted currents and switched currents of all semiconductors. Hence, the transformer design and the resulting parameters must be calculated before the semiconductor losses can be obtained.

In the following, the Π-type equivalent circuit model of the transformer shown in **Fig. 7.16(c)** is used, as it allows a direct calculation of the winding currents i_{p} and i_{s}, including the magnetizing current components i_{mp} and i_{ms}. As the DMC and the full-bridge apply u_{p} and u_{s}, their complex valued Fourier coefficients can be calculated as

$$c_{\mathrm{mp},k} = \frac{-1}{4\pi^2 k^2 f_{\mathrm{sw}} L_{\mathrm{m}}} \left(u_{\mathrm{ab}}\, e^{j2\pi k t_1} + u_{\mathrm{bc}}\, e^{j2\pi k t_2} + u_{\mathrm{ac}}\, e^{0} \right), \tag{7.51}$$

$$c_{\mathrm{ms},k} = \frac{-n^2 u_{\mathrm{pn}}}{4\pi^2 k^2 f_{\mathrm{sw}} L_{\mathrm{m}}} \left(e^{j2\pi k t_3} + e^{j2\pi k t_4} \right) . \tag{7.52}$$

Using the Fourier coefficients c_{k}, calculated with (7.46) for the simple DAB model that neglects L_{m}, the rms value of the k-th harmonic can be calculated as

$$I_{\mathrm{p,rms},k} = \sqrt{2 \left(c_k + c_{\mathrm{mp},k} \right) \left(c_k^* + c_{\mathrm{mp},k}^* \right)} , \tag{7.53}$$

$$I_{\mathrm{s,rms},k} = \sqrt{2 \left(n c_k - c_{\mathrm{ms},k} \right) \left(n c_k^* - c_{\mathrm{ms},k}^* \right)} , \tag{7.54}$$

for odd values of k. This allows to calculate the winding losses, including those resulting from skin and proximity effect, for an operating point given by u_{ab}, u_{bc}, i_{dc} and u_{pn}. The winding currents' squared rms values $I_{\mathrm{p,rms}}^2$ and $I_{\mathrm{s,rms}}^2$

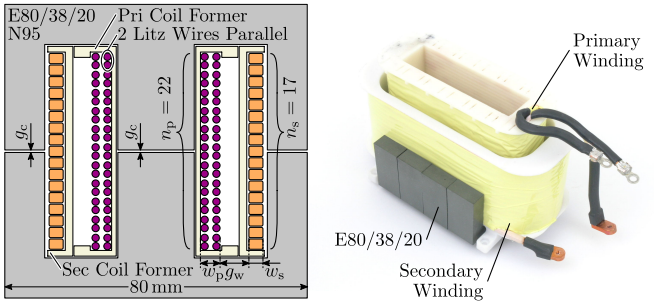

Fig. 7.17: (a) Scaled cross section drawing of the transformer. To implement the required leakage inductance L_σ, the windings are wound on individual, 3D-printed coil formers and are separated by a 7 mm wide gap g_w. **(b)** Picture of the implemented transformer, with the top half of the core removed and the inner, primary-side coil former lifted.

can be approximated by summing the squares of the first M odd harmonics as

$$I_{p,rms}^2 \approx \sum_{m=1}^{M} I_{p,rms,2m-1}^2 \,, \tag{7.55}$$

$$I_{s,rms}^2 \approx \sum_{m=1}^{M} I_{s,rms,2m-1}^2 \,. \tag{7.56}$$

Typically, selecting M in the range between 10 and 100 is sufficient. By averaging the resulting losses over approximately 10 points within one mains voltage sector, the transformer's winding losses for the considered values of U_1, u_{pn} and i_{dc} can be calculated.

The transformer's core losses are calculated using the improved Generalized Steinmetz Equation (iGSE) [138]. As L_σ is built into the transformer as leakage inductance, the voltage drop across L_σ creates a significant leakage flux. This leads to a spatially varying flux density in the core. For each operating point, this is accounted for by evaluating the iGSE twice, once for the flux density created by u_p and once for u_s and averaging the obtained losses.

A drawing of the implemented transformer's cross section is shown in **Fig. 7.17(a)** and the chosen design parameters are given in **Tbl. 7.3**. To implement a sufficiently large leakage inductance L_σ, the primary and secondary winding do not occupy the entire core window, but are separated by a gap of

Tbl. 7.3: Transformer Design

Core	EE80/38/20, Epcos TDK N95, 4 pairs stacked
Primary Winding	71 µm litz wire, 630 strands, 2 wires in parallel
Secondary Winding	100 µm litz wire, 900 strands, rectangular
Winding Widths	$w_p = 7\,\text{mm}$, $w_s = 4\,\text{mm}$
Winding Separation	$g_w = 7\,\text{mm}$
Air Gap	$g_c = 0.3\,\text{mm}$, twice in magnetic path
Turns Ratio	$n = 1.29$
Measured	$L_l = 36\,\mu\text{H}$, w.r.t. to primary
Measured	$L_m = 1.45\,\text{mH}$, w.r.t. to primary

$g_w = 7\,\text{mm}$. While this reduces the available copper cross section and therefore increases the dc resistance of the windings, it also reduces the proximity effect losses, which are approximately proportional to the winding widths w_p and w_s squared [180]. The gap between primary and secondary winding is achieved by using individual coil formers and the primary-side coil former is inserted into the center part of the secondary-side coil former, as can be seen in the picture in **Fig. 7.17(b)**.

As described, the rectifier's modulation scheme the rms value of i_p varies significantly with the voltage transfer ratio u'_{pn}/U_1. A turns ratio n_p/n_s of 1.29 is selected, which results in $u'_{pn}/U_1 \approx 1.6$, yielding low rms values of i_p for a given output current, as can be seen in **Fig. 7.14(b)**. Due to restricted availability of litz wires and to fully utilize the core window's height, two wires with 630 strands of 71 µm are connected in parallel for the primary-side winding. To avoid circulating currents, the wires are wound in parallel and in close proximity to each other. Measurements confirm a current ratio of 1 : 2, which results in losses that are, surprisingly, only 11 % higher than in the ideal case of equal current sharing. As the wires are wound in close proximity, touching each other, no significant temperature difference between the wires is expected.

The remaining transformer design parameters, such as core size and number of stacked cores, and n_p are chosen by numerical optimization to achieve the highest possible efficiency of the whole converter system at nominal operating conditions. Losses of 30 W are measured with a calorimeter in this case, confirming a 99.6 % full-load efficiency of the transformer.

7.3.3 Semiconductors

As in any direct matrix converter, the peak reverse voltage applied to the primary-side MOSFETs is defined by the ac mains line-to-line voltage amplitude. Assuming a 20 % margin for overvoltages and the switching frequency ripple of the input filter capacitor voltages $u_{\tilde{a}}$, $u_{\tilde{b}}$ and $u_{\tilde{c}}$, a peak reverse voltage of 680 V results. C3M0010090K SiC MOSFETs from Wolfspeed with a nominal on-state resistance $R_{\mathrm{DS(on)}}$ of 10 mΩ at 25 °C (+ ≈ 2 mΩ bond wire resistance) and a breakdown voltage of 900 V are selected for the DMC switches as they offer the lowest available $R_{\mathrm{DS(on)}}$ in a four-lead TO-247 package at the time of prototype realization.

The peak reverse voltage of the secondary-side switches is given by the maximum dc voltage u_{pn} and therefore devices with a breakdown voltage of 650 V, such as GaN HEMTs, could be used. To simplify the design and to avoid using different gate driver circuits, the same type of 900 V SiC MOSFETs as on the primary side is selected for the full-bridge switches.

Conduction Losses

It can be seen from the schematic in **Fig. 7.16(a)** that the primary-side winding current i_{p} is conducted by four DMC switches regardless of the DMC's switching state and that two of the four full-bridge switches conduct the secondary-side winding current i_{s}. The conduction losses can therefore be calculated as

$$P_{\mathrm{c}} = R_{\mathrm{DS(on)}} \left(4\, I_{\mathrm{p,rms}}^2 + 2\, I_{\mathrm{s,rms}}^2 \right) \quad , \tag{7.57}$$

where the primary-side and secondary-side winding current rms values $I_{\mathrm{p,rms}}$ and $I_{\mathrm{s,rms}}$ depend on the operating point and transformer parameters (as described in **Section 7.3.2**), i.e. the mains (U_{l}) and dc (U_{pn}) voltages, the output current i_{dc}, the switching frequency f_{sw} and the transformer parameters L_{l}, L_{m} and n.

Switching Losses

Calculating the DMC semiconductors' switching losses is not as straight forward, because the rectifier changes from ZCS in DCM (at low output current and/or output voltages significantly larger or lower than the nominal value), over incomplete ZVS (iZVS) to complete ZVS in CCM (cf. **Fig. 7.7**). Measured switching loss data for a half-bridge configuration of the selected SiC MOSFETs has been published in [181]. The selected devices achieve

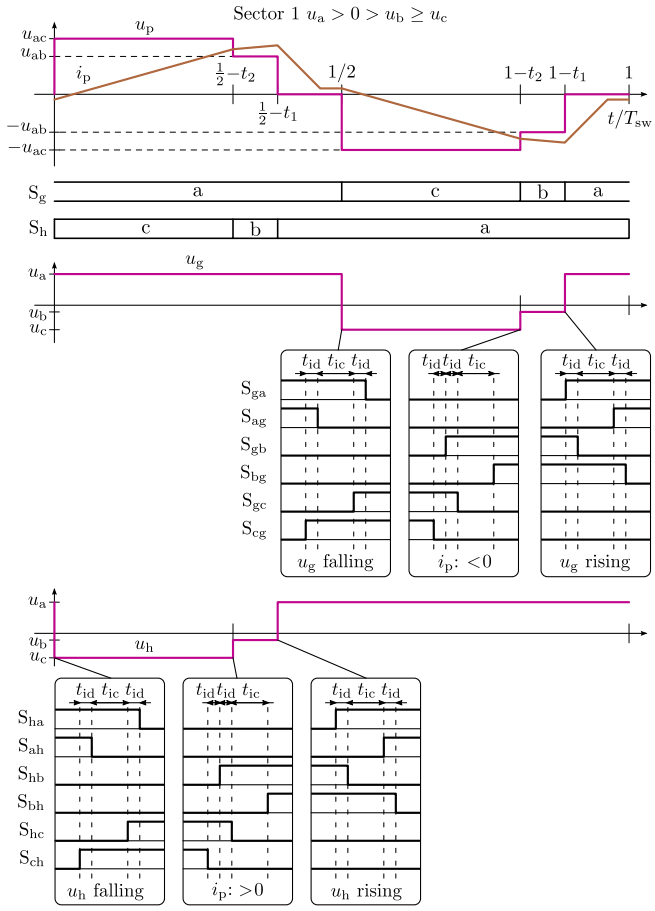

Fig. 7.18: Drawing of the DMC commutation patterns used in sector 1. In the freewheeling intervals $1/2 - t_1 \leq t < 1/2$ and $1 - t_1 \leq t < 1$ (i.e. $u_p = 0$) nodes g and h are both connected to the input terminal with the highest absolute value, i.e. input a in sector 1. Time axes not to scale. Figure continue on next page.

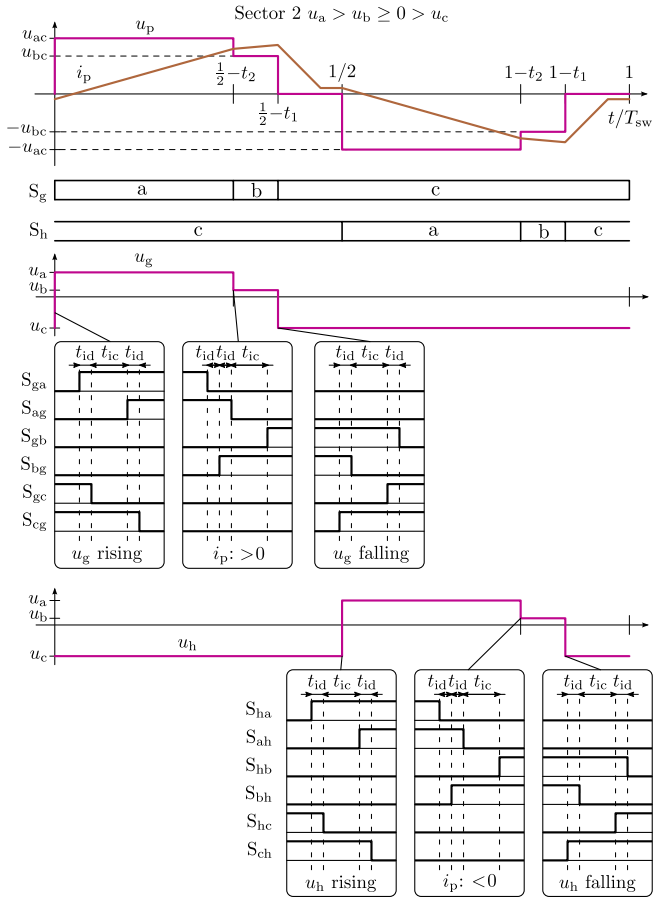

Fig. 7.18 (Cont.): Drawing of the DMC commutation patterns used in sector 2. During the free-wheeling intervals ($u_p = 0$) nodes g and h are connected to the input terminal c.

complete ZVS when switching $\approx$ 7 A or more and have ZCS losses that are more than ten times those at complete ZVS. For iZVS the losses are approximated with a quadratic dependence on the switched current [165]. Hence the transformer's magnetizing current typically has a significant impact on the occurring switching losses and it cannot be neglected. Extending the superposition (7.12) described in **Section 7.2.2** by using the transformer model shown in **Fig. 7.16(c)** the primary- and secondary-side winding currents i_p and i_s are calculated as:

$$i_\mathrm{p}(t) = i_\mathrm{p1}(t) + i_\mathrm{p2}(t) + i_\mathrm{p3}(t) + i'_\mathrm{s1}(t) + i'_\mathrm{s2}(t) + \underbrace{+ \frac{u_\mathrm{ab}\lambda(t+t_1) + u_\mathrm{bc}\lambda(t+t_2) + u_\mathrm{ac}\lambda(t)}{2\,f_\mathrm{sw}L_\mathrm{m}}}_{i_\mathrm{mp}}\,, \tag{7.58}$$

$$i_\mathrm{s}(t) = n\left(i_\mathrm{p1}(t) + i_\mathrm{p2}(t) + i_\mathrm{p3}(t) + i'_\mathrm{s1}(t) + i'_\mathrm{s2}(t)\right) - \underbrace{- n\,\frac{u_\mathrm{pn}}{2\,f_\mathrm{sw}L_\mathrm{m}}\left[\lambda(t+t_3) + \lambda(t+t_4)\right]}_{i'_\mathrm{ms}}\,. \tag{7.59}$$

Evaluating (7.58) at $1/2$, $1/2 - t_1$ and $1/2 - t_2$ yields the corresponding currents switched by the DMC MOSFETs with positive values for ZVS. Note that in ZCS and iZVS the charge stored in the output capacitances C_oss of the DMC MOSFETs which are constantly turned off during the transition causes additional losses and this has to be accounted for in the calculation of switching losses [127].

The described effects are considered in the converter design and the loss calculations presented in **Section 7.4.4**, however a detailed description of the employed models would require too many details and is therefore not discussed here.

DMC Commutation

As the DMC is comprised of six bidirectionally conducting and blocking switches, four-step commutation sequences are required to ensure that no mains line-to-line voltage is shorted and that a valid conduction path for i_p exists at all times [182]. To ensure this, either the sign of i_p, or the sign of the corresponding switching node's voltage edge needs to be known. In total, four sequences can be distinguished: $i_\mathrm{p} > 0$, $i_\mathrm{p} < 0$, u_g or u_h rising and u_g or u_h falling, where u_g and u_h are the voltages between nodes g or h and the

mains neutral. Theoretically, the voltage transition's sign can be determined from the measured mains voltages, however, the matrix converter's input voltages at nodes ā, b̄ and c̄ exhibit a switching frequency ripple that can lead to sign reversal of the voltage edge. Transitions over the line-to-line voltage with lowest absolute value therefore have to use commutation sequences for a known direction of i_p.

One switching frequency period of the commutation scheme proposed for the IMDAB3R is illustrated in **Fig. 7.18** for sector 1 and sector 2. Shown are u_g and u_h, an exemplary DCM current i_p, and the twelve MOSFETs' gate signals. At the beginning of a pulse period ($t = 0$) in sector 1 ($u_a > 0 > u_b \geq u_c$) node h is switched from mains input a to c. As u_{ac} is the largest line-to-line voltage, this results in a falling edge of u_h and the corresponding commutation sequence is used for the MOSFETs S_{ha}, S_{ah}, S_{hc} and S_{ch}, which starts by turning on S_{ch}. Assuming that i_p is below zero, which is the case under ZVS conditions, this does not cause a transition of u_h and the following interlock time t_{id} is only required to ensure a complete charging of S_{ch}'s gate and to allow for mismatched delay times between different gate drivers. A value of $t_{id} = 50$ ns is used in the prototype. The ZVS transition of u_h starts with the turn-off of S_{ah} and a sufficiently long interlock delay t_{ic} is required before the subsequent turn-on of S_{hc}. Calculations and measurements indicate that a value of $t_{ic} = 300$ ns is required to achieve ZVS or valley switching (incomplete ZVS) if currents of 7 A or lower are switched. Before the last step, the turn-off of S_{ha}, the shorter interlock delay t_{id} is used again as node h has already reached its final potential.

In the next transition at $t = 1/2 - t_2$, node h is switched from line c to line b. As u_b and u_c are almost equal at the beginning of sector 1, u_h might not be rising in this case. However, as u_p was equal to u_{ac} since the beginning of the pulse period, it is safe to assume that the primary-side winding current i_p is now positive and the corresponding commutation sequence is used. In this case the third switching event, the turn-off of S_{hc}, initiates the commutation and therefore the first two interlock delays are shorter than the last one. At $t = 1/2 - t_1$ the commutation for a rising edge on u_h is used as node h switches from input b to line a, resulting in a rising edge. In this commutation sequence the turn-off of S_{hb} starts the ZVS transition and uses the longer interlock delay t_{ic}. For the second half of the pulse period, node h remains connected to line a and node g performs the same sequence of commutations as node h during the first half period. As before, commutation sequences with known voltage edge directions are used at $t = 1/2$ and $t = 1 - t_1$ and the commutation sequence for $i_p < 0$ is used at $t = 1 - t_2$.

The second part of **Fig. 7.18** shows the same signals over one pulse period in sector 2 ($u_a > u_b \geq 0 > u_c$, i.e. $30° < \omega t \leq 60°$), which implies that different line-to-line voltages are selected for u_p. To keep the number of required switching transitions at a minimum, nodes g and h are connected to the ac mains line with the largest absolute value (c in sector 2) during the freewheeling intervals $(1/2 - t_2, 1/2)$ and $(1 - t_2, 1)$. This implies that node g is switched during the first half period and node h is switched during the second one in sector 2. In all sectors the transitions at $1/2 - t_2$ and $1 - t_2$ use sequences for known current sign and all others use those for a known voltage edge direction. Switching signals for the remaining ten mains voltage sectors can be derived from those shown in **Fig. 7.18** using symmetry considerations and permuting the mains line voltages. However, the details are not discussed here for the sake of brevity.

If an immediate shutdown of the rectifier is required, for example because the protection circuitry has detected an overcurrent, the transformer needs to be demagnetized without interrupting its winding currents. This implies that the DMC switches cannot be opened immediately. A variation of the procedure described in [183] can be implemented, which ensures that L_1 is demagnetized independent of i_p's sign.

7.3.4 Switching Frequency

The winding currents i_p and i_s, and therefore the conducted and switched currents, vary significantly with the waveforms of u_p and u_s that depend on $\hat{U}_1$, ωt, u_{pn} and i_{dc}. However, the output current i_{dc} that results for given waveforms also depends on the switching frequency f_{sw}. Increasing f_{sw} results in a higher normalized current reference $\breve{i}^*_{dc}$ (cf. (7.50)), generally leading to lower rms values for i_p and i_s as can be seen in **Fig. 7.14(b)**. Additionally, the transformer's core losses typically reduce with increasing f_{sw} due to the lower peak flux density, while the proximity and skin effect losses in the windings and the switching losses increase. Hence, an optimal value for f_{sw} can be found that minimizes the conversion losses for a given operating point. This is verified by measurement results and discussed in more detail in **Section 7.4.4**.

7.3.5 Output Voltage Control

A block diagram of the proposed dc output voltage control scheme is shown in **Fig. 7.19**. First the measured output voltage u_{pn} is compared to the set point value u^*_{pn} and fed into a controller G_u to determine the required equivalent

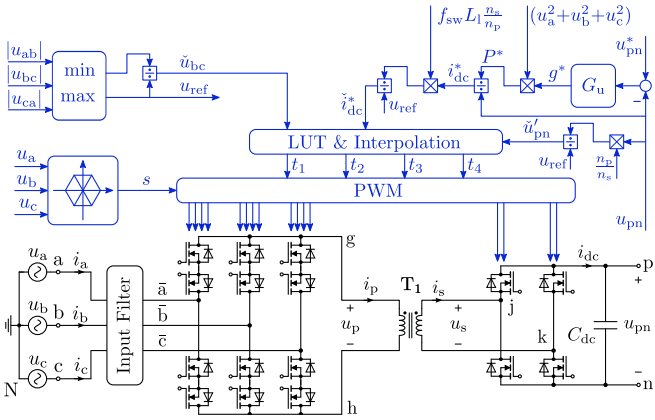

Fig. 7.19: Schematic of the IMDAB3R, including a block diagram of the implemented closed loop control. The output voltage controller G_u determines the required equivalent three-phase conductance g^* that is rescaled to the normalized dc output current reference signal $\check{i}^*_{dc}$. The measured dc voltage u_{pn} and the minimum of the measured absolute line-to-line ac voltages are normalized and fed in the lookup table (LUT). Measured mains voltages are used to determine the sector s required by the pulse width modulator (PWM).

line-to-neutral conductance value g^* of each phase that has to be created at the three-phase input. Multiplying g^* with the sum of the measured mains line-to-neutral voltages squared $(u_a^2 + u_b^2 + u_c^2)$, the required input power P^* results. Dividing P^* by u_{pn} yields the required output current i^*_{dc}, which is normalized by multiplying it with the constant $f_{sw}L_l n_s/n_p$ and dividing by u_{ref} as described in **Section 7.2.5**. The required normalization voltage u_{ref} is derived by selecting the maximum absolute value of the measured line-to-line voltages u_{ab}, u_{bc}, u_{ca}. Similarly, the minimal absolute line-to-line voltage (u_{bc} in sector 1) is divided by u_{ref} to calculate the normalized signal $\check{u}_{bc}$ required by the LUT. The measured dc voltage u_{pn} is rescaled to the primary side and divided by u_{ref} to obtain the normalized voltage $\check{u}'_{pn}$ that is also fed into the LUT. Using these normalized signals, the surrounding data points in the 3D-LUT are obtained and trilinear interpolation is used to determine the relative switching times t_1, t_2, t_3 and t_4. The measured mains voltages are also used to determine the sector s, which is fed to the pulse width modulator together with the four relative switching times to control the primary-side and secondary-side MOSFETs.

Tbl. 7.4: EMI Filter Components

C_f	4.5 µF	3× WE 890334026030CS, 1.5 µF, 310 V, X2 rated
$C_{\mathrm{dm},1}$	3.0 µF	2× WE 890334026030CS, 1.5 µF, 310 V, X2 rated
$C_{\mathrm{dm},2}$	1.5 µF	WE 890334026030CS, 1.5 µF, 310 V, X2 rated
C_d	1.5 µF	WE 890334026030CS, 1.5 µF, 310 V, X2 rated
C_fb	2.2 nF	Epcos TDK B32021A3222, 2.2 nF, 300 V, Y2 rated
R_d	3.3 Ω	2 W SMD resistor
L_dm	15 µH	WE 7443641500

As the mains input currents are created by open loop control only no current sensors are required by the proposed control scheme. This is an advantage for high-efficiency converters as corresponding sensor losses can be avoided.

7.3.6 Further Design Considerations

To allow a fair comparison in terms of volumetric power density and efficiency with other three-phase PFC rectifiers, an EMI filter is included in the prototype, however, for the sake of brevity it is not designed specifically for this converter. Instead, a filter similar to the one used for a three-phase buck-type SWISS Rectifier with the same voltage and power rating [184] is used. The schematic of the implemented filter is shown in **Fig. 7.16(b)**. The filter consists of a two-stage, fourth-order, differential-mode filter formed by L_dm, $C_{\mathrm{dm},1}$ and $C_{\mathrm{dm},2}$. Note that only the second stage contains an R-C damping element formed by R_d and C_d, to avoid the damping resistor losses due to switching frequency voltage ripples in the first filter stage [184].

Due to parasitic coupling capacitances between the transformer's primary and secondary windings, a common-mode current flows from the DMC to the full-bridge. Feedback capacitors C_fb enable this current to return to the star-point of the input capacitors C_f. A capacitor C_{Y2} is added between this star-point and the converter's aluminum base plate or casing to provide a return path for currents resulting from parasitic capacitances between switching nodes, transformer windings, etc. and the base or casing. Depending on the load's ground capacitance or grounding scheme an additional common-mode filter inductor L_cm might be required to comply with EMI regulations, but this was not implemented in the prototype. As the core of L_cm is not subject to switching frequency voltages or currents, it exhibits only mains frequency conduction losses, which are typically $\approx 1\,\mathrm{W}$.

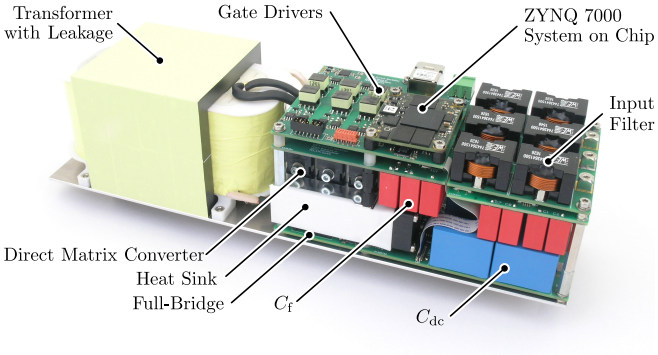

Fig. 7.20: Picture of the implemented 8 kW prototype, measuring 312 mm × 80 mm × 80 mm, which results in a power density of 4 kW/dm^3 (66 W/in^3).

As the design procedure of the IMDAB3R's EMI filter is essentially not different from that for other buck- or buck-boost-type PFC rectifiers, it is not discussed here further for the sake of brevity.

7.3.7 Designed Prototype

A picture of the hardware prototype is shown in **Fig. 7.20**: With outer dimensions of 312 mm × 80 mm × 80 mm (12.3 in × 3.15 in × 3.15 in) a total volume of 2 dm^3 results, which corresponds to a power density of 4 kW/dm^3 (66 W/in^3). The distribution of calculated losses for nominal input and output voltages, full-load (i_{dc} = 20 A) and f_{sw} = 31 kHz is shown in **Fig. 7.21(a)**. Almost half of the total losses (≈ 37 W) occur in the semiconductors, of which 8 W are switching losses and 29 W are due to current conduction. The transformer causes 28 W of losses, approximately equally split between primary winding, secondary winding and the core. The FPGA, gate driver, fans and the auxiliary power supply (three-phase mains to 5 V) consume about 7 W. Conduction losses in the EMI filter inductors cause less than 5 W of losses and other components, such as PCBs and capacitors account for approximately 3 W.

A share of 46 % of the rectifier's total volume is occupied by the transformer and ≈ 22 % by the EMI input filter. The heat sinks, fans and MOSFETs require another 16 % of the total volume. The remaining volume holds the control board and gate drivers, as well as the dc output capacitors.

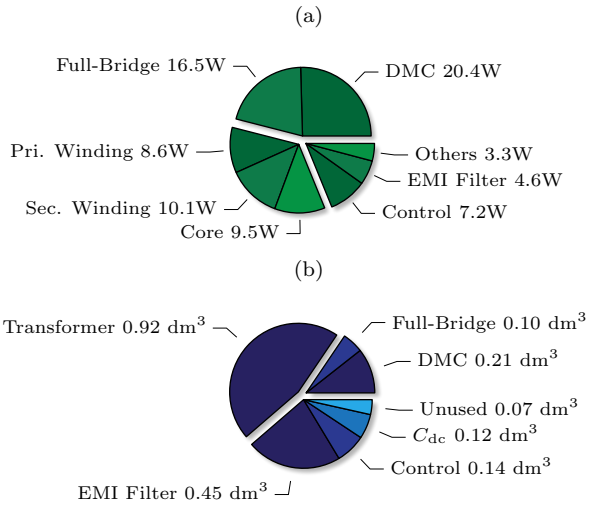

Fig. 7.21: (a) Breakdown of calculated losses for nominal operation and **(b)** boxed volumes of the corresponding components (1 dm³ = 61 in³). The control losses include an FPGA, gate drivers, cooling fans, and a 600 V to 5 V LLC-based auxiliary power supply.

7.4 Measurement Results

Measurement results taken on the 8 kW prototype rectifier shown in **Fig. 7.20** are presented in the following.

7.4.1 Mains Input Currents

In **Fig. 7.22** the measured ac mains line-to-neutral voltages u_a, u_b and u_c, as well as the corresponding ac input currents i_a, i_b and i_c are shown for nominal operating conditions as defined in **Tbl. 7.1**. The input currents are sinusoidal and in phase with the mains voltages but show slight distortions at the 30° mains voltage sector boundaries resulting in an input current total harmonic distortion (THD) of 3.0 %. The IMDAB3R acts as a current source for the input filter, causing a relatively large switching frequency voltage ripple at the input capacitors C_f. This voltage ripple affects u_p, which in turn changes the shape of i_p and causes a mismatch between actual and ideal mains input currents. Together with the change of the switching pattern at the sector boundary,

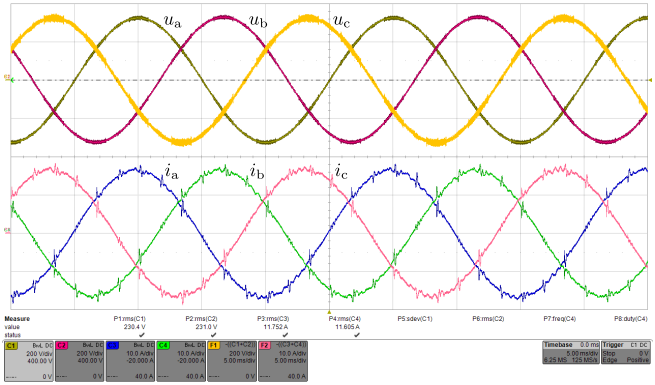

Fig. 7.22: Measured mains line voltages u_a, u_b and u_c (200 V / div, 5 ms / div) and input currents i_a, i_b and i_c (10 A / div) for nominal operating conditions and $f_{sw} = 33\,\text{kHz}$. An input current THD of 3.0 % results. Only the quantities of phases a and b are measured directly, those of phase c are created by postprocessing using $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

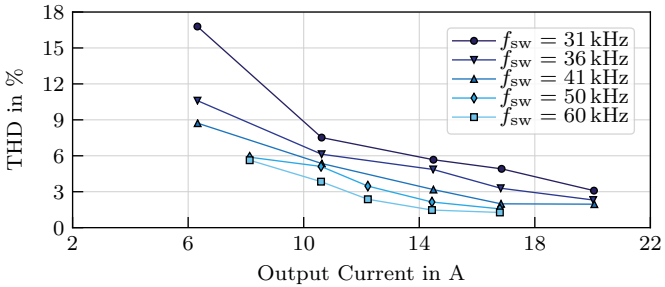

Fig. 7.23: Input current THD (maximum of phases) for different dc currents and switching frequencies, measured with a *Yokogawa WT3000* power analyzer.

this starts a short, damped ringing of the input filter. Similar ac input current distortions exist in buck-type three-phase rectifiers [113, 117, 119, 184].

Input current THD values, measured with a *Yokogawa WT3000* power analyzer for different output currents i_{dc} and switching frequencies, are shown in **Fig. 7.23**. Generally, the THD values decrease with increasing f_{sw} because errors caused by the switching frequency input voltage ripple and by the dead time between calculating $\vec{t}$ and the actual switching actions, etc. are reduced. This effect is more pronounced for low output currents i_{dc} because the rectifier

changes between CCM and DCM operation in every mains voltage sector for low switching frequencies. Relatively long interlock delays ($\approx 300\,\mathrm{ns}$) are required to achieve ZVS in CCM, which causes additional dead time and pulse width distortion in DCM and hence repeated transitions between CCM and DCM leading to input current distortions. By increasing f_{sw} the normalized current reference $\check{i}'_{\mathrm{dc}}$ increases [cf. (7.50)] and the converter operates in CCM for a longer period during each mains voltage sector. Simulation results suggest that an adaptive selection of interlock delay times, based on the operating conditions (mains voltage, u_{pn}, i_{dc}, etc.) could be used to improve THD at low output currents without loosing complete ZVS in high-load conditions. For the sake of brevity this is not discussed here further.

7.4.2 Transformer Waveforms

Measured transformer voltages u_{p} and u_{s} and the corresponding winding currents i_{p} and i_{s} are shown in **Fig. 7.24** for four different mains voltage phase angles ωt. The plots were recoded under nominal operating conditions and with 20 A load current, as specified in **Tbl. 7.1**. It can be seen that the primary-side winding voltage's falling edges and the secondary-side voltage's rising edges occur entirely with positive winding currents i_{p} and i_{s}, which implies that complete ZVS is achieved.

7.4.3 Load Step

In **Fig. 7.25** the measured mains input current i_{a}, the primary-side winding current i_{p}, the dc output voltage u_{pn} and the load current i_{load} are shown for a load step from $i_{\mathrm{load}} = 10\,\mathrm{A}$ to $i_{\mathrm{load}} = 20\,\mathrm{A}$. This step causes a transient of u_{pn} with a peak voltage drop of 15 V, which is 3.5 % of the set point value. The amplitude of i_{p} increases during the transient, but i_{p} stays balanced around zero.

7.4.4 Efficiency

Measured rectifier efficiencies and losses are plotted in **Fig. 7.26** as markers, together with calculation results shown as solid lines, for different output currents i_{dc} and nominal voltages ($U_1 = 230\,\mathrm{V}$ rms, $U_{\mathrm{pn}} = 400\,\mathrm{V}$). As the losses vary significantly with f_{sw}, five different curves are shown with switching frequencies between 31 kHz and 60 kHz.

For $i_{\mathrm{dc}} \approx 20\,\mathrm{A}$ losses of 80 W are achieved with $f_{\mathrm{sw}} = 31\,\mathrm{kHz}$, resulting in a full-load efficiency of 99 %. Increasing the switching frequency to 36 kHz

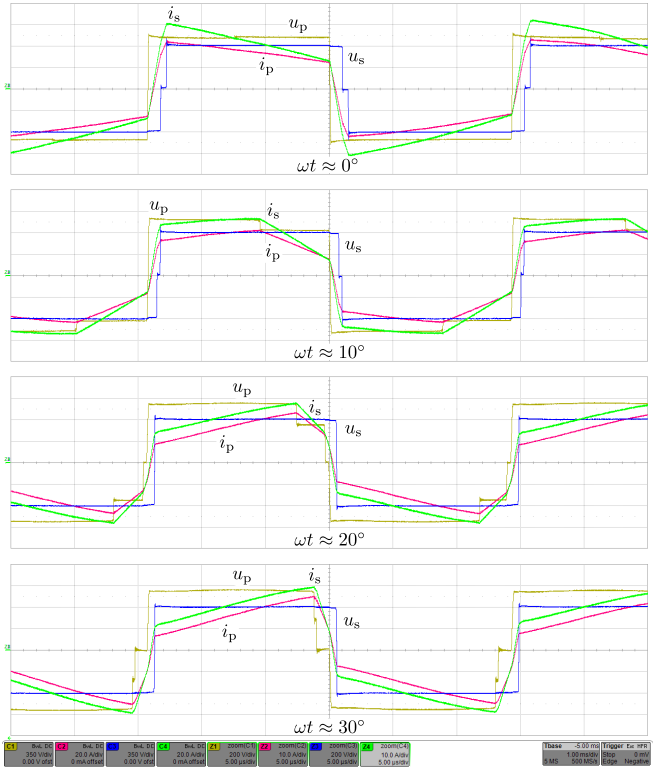

Fig. 7.24: Measured transformer voltages u_p, u_s (200 V / div, 5 µs / div) and currents i_p, i_s (10 A / div) for nominal operation, $f_{sw} = 35$ kHz and different mains phase angles ωt. It can be seen that all falling edges of u_p and all rising edges of u_s occur with positive transformer currents, which implies that ZVS is achieved. Note: Calculations show that the primary-side magnetizing current has an amplitude of ≈ 3 A.

or 41 kHz reduces the efficiency due to increasing ZVS losses. At a lower load current of $i_{dc} \approx 17$ A incomplete ZVS results for $f_{sw} = 31$ kHz and the rectifier's total losses can be reduced by increasing the switching frequency to $f_{sw} = 36$ kHz as complete ZVS is again achieved. Increasing f_{sw} even further has the contrary affect as higher switching losses result. This frequency dependence is even more pronounced for $i_{dc} \approx 10.5$ A, as the rectifier operates in DCM for almost the entire mains voltage period with $f_{sw} = 31$ kHz, but in CCM for $f_{sw} = 60$ kHz. Besides reducing the switching losses due to ZVS

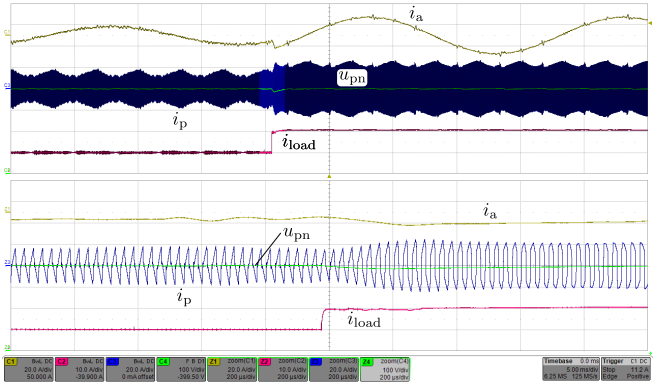

Fig. 7.25: Measurement results (5 ms / div) for a load transient from half to rated load current. Shown are the mains input current i_a (20 A / div), the primary-side transformer current i_p (20 A / div), the dc output voltage u_{pn} (100 V / div) and the load current i_{load} (10 A / div). The bottom plot (200 µs / div) shows a zoom around the load step.

instead of ZCS, this also reduces the rms value of i_p from 10.4 A to 9.1 A, which reduces the conduction losses in the MOSFETs and windings by 23 %. When i_{dc} is reduced further to $\approx$ 6.5 A, the switching frequency required to keep CCM over the whole mains period exceeds 80 kHz. The resulting ZVS switching losses and the increasing skin and proximity effect losses in the transformer windings lead to total rectifier losses that are higher than those at f_{sw} = 31 kHz, as can be seen in **Fig. 7.26**. Selecting f_{sw} for minimal losses at the required output current i_{dc}, an efficiency of 99 % results for 12 A $\leq i_{dc} \leq$ 20 A. At half the rated load ($i_{dc} \approx$ 10.6 A) an efficiency of 98.9 % is measured at f_{sw} = 60 kHz.

Measured efficiencies and losses for a 10 % lower mains voltage of U_1 = 207 V rms and u_{pn} = 400 V are shown in **Fig. 7.27** for different output currents. In each point the switching frequency which results in the highest efficiency is selected and written on top of the corresponding marker. Compared to nominal voltages, higher switching frequencies are required to achieve minimal losses for a given value of i_{dc}, as the border between DCM and CCM occurs for higher values of $\check{i}_{dc}$. This reduces the achievable peak efficiency to 98.6 % for output currents between 14.4 A and 20 A.

All loss measurements plotted in **Fig. 7.26** and **Fig. 7.27** are taken with a *Yokogawa WT3000* power analyzer. For every operating point and switching

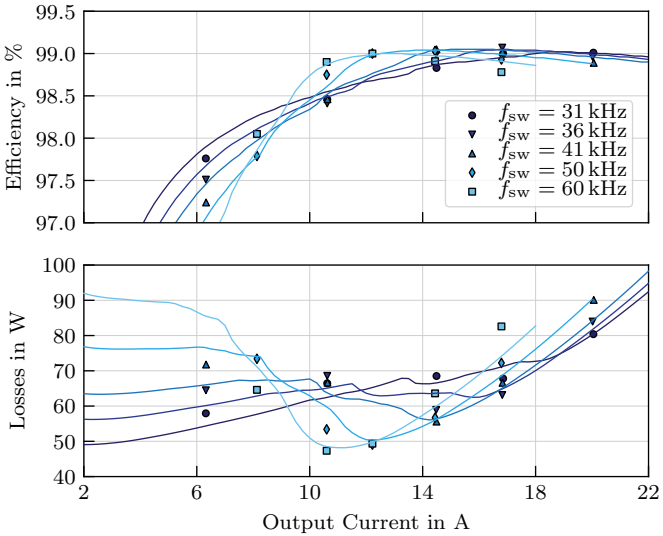

Fig. 7.26: Measured (markers) and calculated (solid lines) efficiency and losses of the rectifier as a function of the output current i_{dc}, for nominal input (U_1 = 230 V rms) and output (U_{pn} = 400 V) voltages and various switching frequencies.

frequency the rectifier was allowed to reach thermal steady state in an ambient temperature of 30 °C (±3 °C). As electrical loss measurements are difficult at such high efficiencies, two operating points, i_{dc} = 20 A at f_{sw} = 31 kHz and i_{dc} = 14.5 A at f_{sw} = 41 kHz, are verified by a calorimetric loss measurement. The converter is placed inside a calorimeter which measures the rectifier's heat dissipation thermally at a controlled ambient temperature of 40 °C with a precision of 2 % (i.e. 1.6 W) [143]; 86 W and 58 W of losses are measured, which is only 7.5 % and 5.4 % higher than the electrical measurements. As a significant amount of the rectifier's losses are due to conduction losses in the MOSFETs and transformer windings, approximately 4 % of this difference is likely due to the increased ambient temperature.

7.5 Summary and Conclusions

This chapter analyzes the isolated matrix-type DAB three-phase PFC rectifier (IMDAB3R), which was originally proposed as vehicle-to-grid interface. Due to its structural similarity to the conventional dual active bridge (DAB)

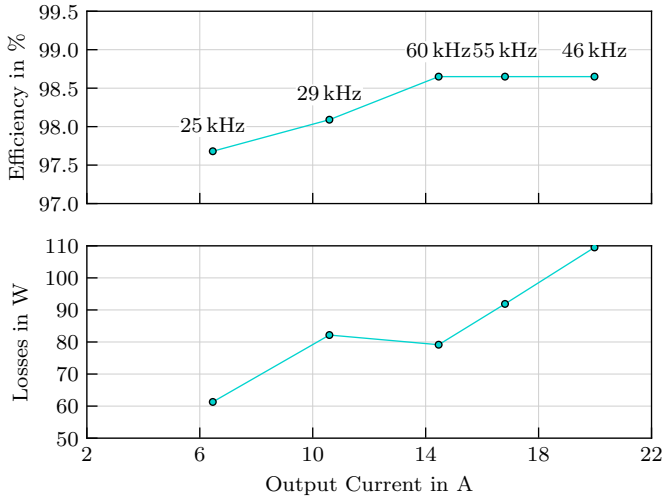

Fig. 7.27: Measured efficiency and losses as a function of the output current, for a reduced mains voltage of $U_1 = 207\,\mathrm{V}$ rms (line-to-neutral) and nominal output voltage ($U_{\mathrm{pn}} = 400\,\mathrm{V}$). The switching frequency which minimized losses is chosen in each operating point and written above the corresponding markers in the top plot.

converter, an isolation transformer with sufficiently large leakage inductance is the only magnetic component required, except for the EMI filter. This simplifies the mechanical design and potentially reduces cost and/or volume. Additionally, the IMDAB3R does not require any current sensors, as satisfactory mains input current THD values of 3 % are achieved with open loop control of the transformer current.

A conduction loss optimal modulation scheme for the IMDAB3R, achieving zero current or zero voltage switching, is proposed and thoroughly analyzed in this chapter. The required switching times are derived analytically for DCM and by numerical optimization for CCM. This allows to achieve sinusoidal mains currents, in phase with the line voltages for arbitrary dc output currents and voltages. As the time required for the switching time calculation is longer than the cycle time of a typical control loop, off-line optimized switching times for all combinations of mains and dc voltages and output current are stored in a normalized, three-dimensional lookup table. It is used by the digital control circuit to determine near optimal switching times using trilinear interpolation. An implementation of the required optimization

routines is published as open source software [179].

To verify the theoretical considerations and to provide a benchmark for the highest achievable efficiency, an 8 kW isolated three-phase PFC rectifier is designed, implemented and tested. Using novel 900 V 10 mΩ SiC MOSFETs and a transformer with litz wire windings, the prototype achieves a power density of 4 kW/dm^3. At nominal operating conditions, with 230 V rms line-to-neutral mains and 400 V dc output voltage an efficiency of 99 % is measured for load currents between 12 A and 20 A, using a load current dependent switching frequency in the range of 31 kHz to 60 kHz. A mains current THD of less than 4 % is achieved in this range, which is within usual regulatory restrictions for PFC rectifiers. At full-load 46 % of the total losses occur in the semiconductors, 35 % in the transformer and 19 % are caused by the input filter, control, gate driver, fans, PCBs and the auxiliary power supply. A 10 % lower mains voltage (207 V rms) leads to higher transformer currents, reducing the efficiency slightly to 98.7 %.

Compared to hard switching circuit topologies, the prototype rectifier's efficiency has a stronger dependence on the operating conditions (i.e. input and output voltages and currents) and the switching frequency, as the rectifier achieves complete ZVS only in a relatively narrow set of operating conditions. This implies that the switching frequency should be changed online according to the current operating conditions to achieve the best performance, which complicates the control and modulation circuit. Alternatively, the transformer's magnetizing current could be increased to extend the range of operating conditions for which ZVS is achieved with a given switching frequency, however, this also increases conduction losses under nominal operating conditions, reducing the achievable peak efficiency. Further research could address this trade-off.

Measured full-load efficiency values of other isolated three-phase rectifiers are summarized in **Tbl. 7.5**. Even though most of these were not optimized for maximum efficiency, it can be seen that the prototype presented in this chapter achieves a reduction of losses by a factor of 2 or more, also compared to systems utilizing state-of-the-art wide bandgap devices. As the isolation transformer is the only magnetic component loaded by switching frequency voltages this increase in efficiency is not at the expense of power density as can also be seen from **Tbl. 7.5**.

While this chapter focuses on rectifier operation, the derived modulation scheme and the optimized switching times could, in principle, also be used for inverter operation. To do so, the sequence of switching states would have to be reversed, creating a rising stair-case type voltage at the primary winding

Tbl. 7.5: Comparison to Other Isolated Three-Phase PFC Rectifiers

Topology	Technology	Rated Power	DC Voltage	Measured Efficiency	Power Density
Phase-Modular SEPIC [185]	Si IGBT Si Diodes	4 kW	400 V	90 %	unknown
Isolated Full-Bridge Boost [186]	Si IGBT	1.7 kW	200 V	91 %	unknown
Swiss-Forward [53]	SiC MOSFET SiC Schottky	3 kW	270 V	93.5 %	0.44 kW/dm^3
Matrix-Type Isolated Inverter [187]	SiC MOSFET	1.3 kW	400 V	94.1 %	unknown
IMDAB3R [188]	SiC MOSFET SiC Schottky	1.2 kW	180 V	94.4 %	unknown
Phase-Modular & Scott Transformer [189]	Si IGBT Si Diode	12 kW	400 V	95.1 %	1.33 kW/dm^3
Phase-Modular Ćuk [190]	SiC MOSFET Si Diode	2 kW	400 V	95.1 %	unknown
Phase-Modular PFC & LLC [191]	Si MOSFET SiC Diode	10 kW	300 V	95.5 %	unknown
IMDAB3R [169]	SiC MOSFET	1 kW	230 V	96.0 %	unknown
Isolated Matrix-Type Δ Rectifier **Chapter 6**	SiC MOSFET SiC Schottky	7.5 kW	400 V	97.2 %	1.03 kW/dm^3
Phase-Modular PFC & LLC [192]	GaN HEMT	22 kW	400 V	98 %	3.3 kW/dm^3
IMDAB3R (this Chapter)	SiC MOSFET	8 kW	400 V	99.0 %	4.0 kW/dm^3

with a phase leading secondary-side winding voltage. Further research could also address different implementation options for the inductive isolation network, such as using a separate inductor and transformer. To increase the efficiency even further the switching frequency could also be varied within the mains voltage period. Additionally the interlock delays used by the PWM modulators could be varied, ensuring valley switching under incomplete ZVS, and reducing dead time in ZCS switching. This could potentially reduce the input current THD at light-load conditions and might also enable a slight reduction of losses as the conduction times of body diodes can be reduced in certain operating points.

8

The Zurich Rectifier – An Isolated Indirect-Matrix-Type DAB PFC Rectifier

In the previous chapter an isolated matrix-type dual active bridge (DAB) three-phase PFC rectifier (IMDAB3R) is analyzed, achieving a full-load efficiency of 99 % with an 8 kW prototype rectifier. However, a relatively complex modulator is required, as four different multi-step commutation patterns are used by the direct matrix converter on the primary-side. To simplify the modulator without compromising efficiency, a new circuit topology is proposed in this chapter. The direct matrix converter is replaced by an input voltage selector and a subsequent T-type inverter, essentially forming a kind of indirect matrix converter. This mitigates the need of the multi-step commutation patterns as a valid conduction path for the transformer winding currents is guaranteed by body diodes at all times. Loss alculations indicate that the system, which is named *Zurich Rectifier* in the following, achieves the same efficiency as the IMDAB3R at nominal output voltage when using the same SiC MOSFETs. At half the rated output voltage the Zurich Rectifier's losses are 9 % lower than those of the IMDAB3R.

8.1 Introduction

In **Chapter 7** the single-stage IMDAB3R is analyzed and a conduction loss optimal modulation scheme is derived, which allows to achieve a peak efficiency of 99.0 % at full-load. This PFC rectifier uses a direct matrix converter (DMC) to apply the mains line-to-line voltages to the primary-side transformer winding of a DAB converter. The DMC requires four different multi-step commutation sequences in order to ensure that the primary-side winding current has a valid conduction path at all times and that no mains voltages are shorted at any time [182, 193]. Special commutation patterns are also required to perform a safe shutdown when an error condition, such as an over-current, an over-voltage or failing control power, is detected. Executing a wrong commutation sequence typically leads to high overvoltage or overcurrents of the DMC switches, potentially damaging the semiconductors. This is a general disadvantage of the DMC and in many applications a diode-based over-voltage clamp circuit is used [182, 193]. However, these diodes add parasitic capacitances to the DMC and therefore increase the switching losses, especially in discontinuous conduction mode (DCM) where zero current switching (ZCS) occurs.

These disadvantages can be overcome by replacing the DMC with an input voltage selector (IVS) and a T-type inverter bridge as shown **Fig. 8.1**. The IVS consists of a six-pulse diode rectifier bridge and three bidirectionally blocking and conducting switches, formed by the anti-series connection of two MOSFETs. Like in the SWISS Rectifier (cf. **Chapter 3**), the IVS diodes connect the mains input terminal $\bar{a}$, $\bar{b}$ or $\bar{c}$ with the highest potential to node x and the one with the lowest potential to node z. The two MOSFETs connected to the remaining mains input are then turned on to connect this input to node y. Therefore, the semiconductors in the IVS commutate at twice the mains frequency and exhibit only negligible switching losses. As described in **Section 3.2**, the voltages u_x, u_y and u_z between the corresponding nodes and the star-point of the mains are piecewise sinusoidal and hence form a three-phase voltage. This allows to connect the input filter capacitors C_f to these nodes as well, which leads to continuous currents in the IVS semiconductors and thereby reduces the conduction losses.

The T-type inverter bridge connects each of the two primary-side transformer nodes g and h to the IVS output nodes x, y or z. As each of these nodes is connected to a mains input terminal, the T-type inverter essentially applies a mains line-to-line voltage as primary-side winding voltage u_p, achieving the same functionality and the same degrees of freedom as the IMDAB3R's

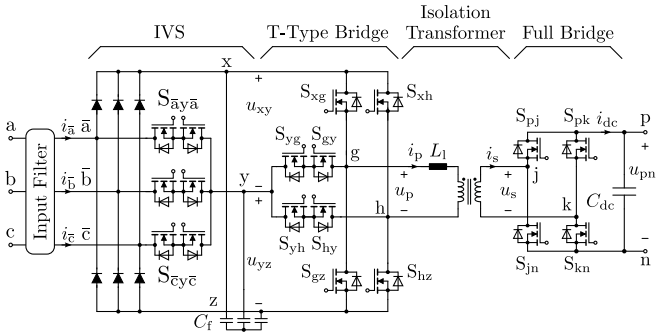

Fig. 8.1: Schematic of the single-stage, isolated indirect-matrix-type DAB three-phase rectifier. Like the SWISS Rectifier (cf. **Chapter 3**), this circuit uses an input voltage selector (IVS) to create an intermediate three-phase voltage system at nodes x, y and z. Two T-type bridge legs are used to connect the primary-side transformer winding (nodes g and h) to nodes x, y and z. Like in the IMDAB3R, any mains line-to-line voltage can be selected as primary-side winding voltage u_p and therefore the same modulation scheme can be used. This circuit is denominated as *Zurich Rectifier* in this work.

DMC. Note that the body diodes of the T-type inverter MOSFETs (S_{xg}, S_{gz}, S_{xh} and S_{hz}) and the capacitors C_f provide a valid conduction path for the primary-side winding current i_p, even if all switches are turned off simultaneously. This eliminates the need for multi-step commutation sequences in the T-type inverter.

The combination of an IVS and a T-type inverter can be interpreted as an indirect matrix converter, where the mains input voltages are first rectified by the IVS and then converted into a higher frequency ac voltage u_p by the T-type inverter bridge. To the best of the author's knowledge this circuit has not yet been published in scientific literature.

In **Section 8.2**, a commutation pattern is proposed for the Zurich Rectifier that allows to use the modulation scheme previously derived for the IMDAB3R. Equations for the T-type inverter MOSFETs' rms current stresses are derived as well. The losses calculated for a Zurich Rectifier are compared to those of a IMDAB3R in **Section 8.3**. Both systems are designed using the same semiconductor technology and the same magnetic components. The main specifications for both rectifiers are given in **Tbl. 8.1**. Finally, the main results are summarized in **Section 8.4** and conclusions are drawn.

Tbl. 8.1: Nominal Operating Conditions & Converter Specifications

Input Voltage Amplitude (Line-to-Neutral)	$\hat{U}_1 = 325\,\mathrm{V}$ rms
Input Frequency	$\omega = 2\pi\,50\,\mathrm{Hz}$
Nominal DC Output Voltage	$U_{\mathrm{pn}} = 400\,\mathrm{V}$
Nominal Output Power	$P = 8\,\mathrm{kW}$
Minimal Switching Frequency	$f_{\mathrm{sw,min}} = 25\,\mathrm{kHz}$
Maximal Switching Frequency	$f_{\mathrm{sw,max}} = 100\,\mathrm{kHz}$
Leakage Inductance	$L_1 = 36\,\mu\mathrm{H}$
Turns Ratio	$n_{\mathrm{p}}/n_{\mathrm{s}} = 22/17 \approx 1.29$

8.2 Modulation and Commutation

The Zurich Rectifier's series connection of an IVS and a T-type inverter bridge can apply any mains line-to-line voltage to the primary-side transformer winding as voltage u_{p}. Hence the same winding voltage waveforms as for the IMDAB3R can be used, which achieve zero voltage switching (ZVS) in continuous conduction mode (CCM) and ZCS in DCM. Exemplary waveforms of u_{p} and the secondary-side winding voltage u'_{s} (referred to the primary-side) are shown in **Fig. 8.2** for mains voltages in sector 1, i.e. $u_{\mathrm{a}} > 0 \geq u_{\mathrm{b}} > u_{\mathrm{c}}$ and $u_{\mathrm{x}} = u_{\mathrm{a}}$, $u_{\mathrm{y}} = u_{\mathrm{b}}$, $u_{\mathrm{z}} = u_{\mathrm{c}}$. A CCM primary-side winding current i_{p} is shown as well, however, all signals are not drawn to scale. In this chapter, all switching times are normalized to the switching period $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$.

8.2.1 Switching Pattern

To enable ZVS, a staircase shape is used for u_{p}, which can be decomposed into the two bridge output voltages u_{g} and u_{h}, measured between nodes g or h and the mains star-point. As shown in **Fig. 8.2**, the largest line-to-line voltage u_{xz} is selected for u_{p} at the beginning of the switching period ($t = 0$), by turning off S_{xh} and S_{yh} and turning on S_{hz}, which connects node h to node z. Node g is still connected to node x, due to the previous switching period. Switch S_{hy} is turned on simultaneously, even though it will not conduct any current, as this allows a natural commutation in the following transition [194]. At $t = 1/2 - t_2$, switch S_{hz} is turned off and S_{yh} is turned on to connect nodes h and y, resulting in $u_{\mathrm{p}} = u_{\mathrm{xy}}$. At $t = 1/2 - t_1$ ($t_1 \leq t_2$), switch S_{hy} is turned off and S_{xh} is turned on to connect node h to x and start a free-wheeling interval with $u_{\mathrm{p}} = 0$. Beginning at $t = 1/2$, the same switching sequence is executed on S_{xg}, S_{gy}, S_{yg} and S_{gz}, to create the same waveform for

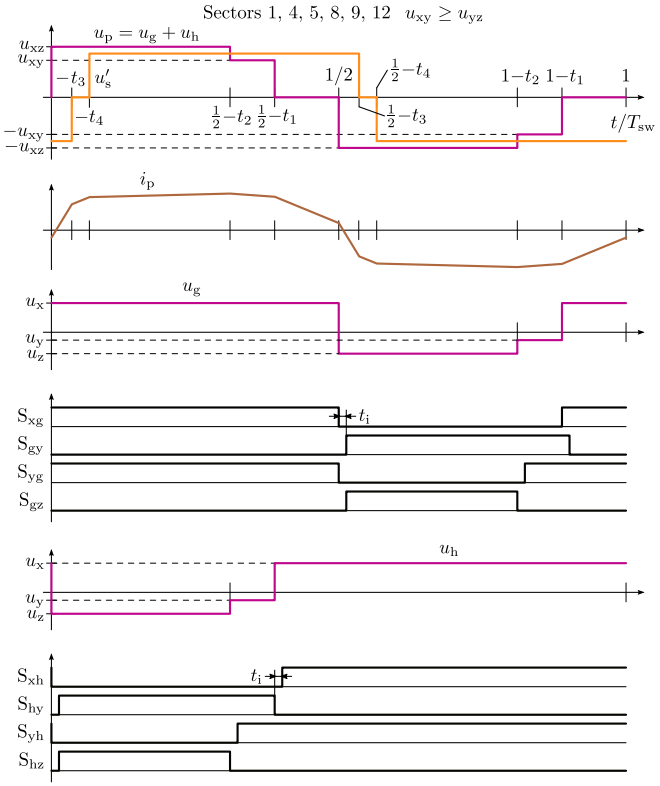

Fig. 8.2: Commutation pattern of the T-type inverter bridge used in sectors 1, 4, 5, 8, 9 and 12 where $u_{xy} \geq u_{yz}$ holds. Shown are the transformer winding voltages u_p and u'_s (w.r.t the primary-side) and the resulting primary-side winding current i_p. Also shown are the voltages u_g and u_h between the output nodes g and h of the T-type inverter and the mains star-point, as well as the control signals for the eight inverter MOSFETs. The waveforms are shown for illustration only and are not to scale.

u_p as before, but with reversed polarity. Ideally, this results in a zero-mean waveform for u_p, which is required to prevent a saturation of the transformer. An interlock time t_i is inserted between the turn-off and the following turn-on at each transition to prevent shoot through currents. Like in the IMDAB3R, a symmetric rectangular waveform with variable duty cycle and phase shift is applied as secondary-side transformer winding voltage u_s by the full-bridge S_{pj}, S_{jn}, S_{pk} and S_{kn}. This waveform is characterized by the switching times

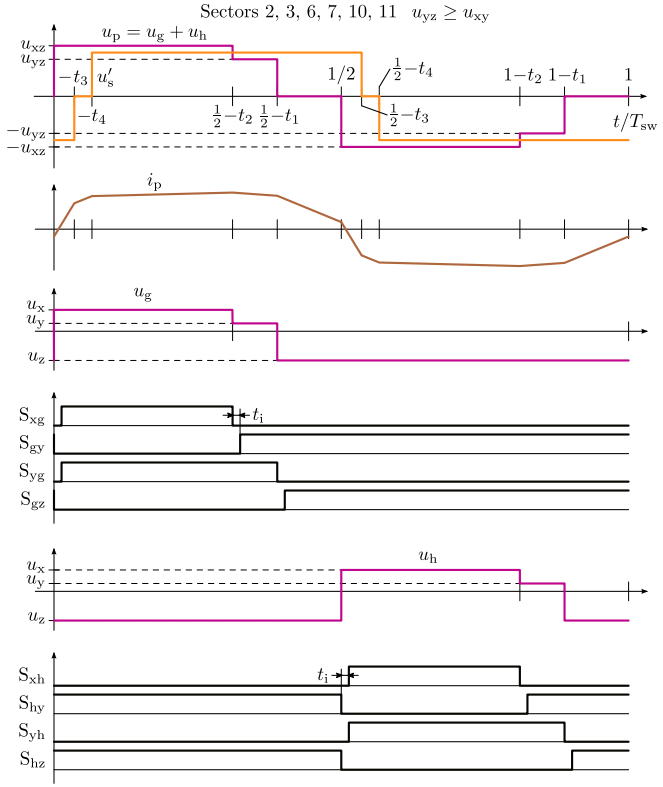

Fig. 8.3: Transformer voltage and current waveforms and commutation pattern used in sectors 2, 3, 6, 7, 10 and 11 during which $u_{yz} \geq u_{xy}$ holds. See **Fig. 8.2** for a description of the shown signals.

t_3 and t_4 as described in **Section 7.2.1**.

It can be seen in **Fig. 8.2** that both rising edges of u_g and the falling one of u_h occur when i_p is negative. Vice versa, i_p is positive at the rising edges of u_h and the falling one of u_g. Provided that i_p has a sufficient amplitude, ZVS is achieved in all transitions. To achieve ZVS also in the mains voltage sectors 2, 3, 6, 7, 10 and 11, where $u_{yz} \geq u_{xy}$ holds, a slightly different switching pattern is used as shown in **Fig. 8.3**. In these sectors, nodes g and h are connected to node z during the free-wheeling intervals ($1/2 - t_1 \geq t > 1/2$ and $1 - t_1 \geq t > 1$). At the beginning of the switching period, the switches S_{gy} and S_{gz} are turned off and the switches S_{xg} and S_{yg} are turned on. This connects node g to node

x and results in $u_p = u_{xz}$. The switch S_{xg} is turned off at $t = 1/2 - t_2$ and S_{gy} is turned on to connect node g to node y, which selects the second largest line-to-line voltage u_{yz} for u_p. At $t = 1/2 - t_1$, S_{yg} is turned off and S_{gz} is turned on, connecting node g to node z. As before, an interlock time t_i is inserted between the turn-off and and turn-on to prevent shoot through. In the second half period ($1/2 \leq t < 1$), the switches S_{xh}, S_{hy}, S_{yh} and S_{hz} are switched in the same sequence as shown in **Fig. 8.3**, to create a zero-mean waveform for u_p.

Changing from one modulation pattern to the other occurs ideally immediately after the beginning of a pulse period at $t = 0$. After executing the first transitions $u_p = u_{xz}$ results for both patterns. Therefore the modulator can continue with the new pattern once the transitions at $t = 0$ is completed.

8.2.2 Modulation

In the modulation patterns described above, the four switching times $\vec{t} = [t_1, t_2, t_3, t_4]$ represent the transformer voltages' degrees of freedom and need to be chosen such that the desired dc output currents results and that sinusoidal mains input currents, in phase with the voltages are achieved. As the waveform of u_p created by the T-type inverter is identical to the one created by the DMC in the IMDAB3R, both circuit topologies can use the same switching times $\vec{t}$. A detailed description how $\vec{t}$ can be chosen to achieve the desired input and output currents with minimal rms winding current $i_{p,rms}$ is given in **Section 7.2**.

Simulation results for a Zurich Rectifier, with $f_{sw} = 31\,\text{kHz}$ and nominal operating conditions according to the specifications listed in **Tbl. 8.1**, are plotted in **Fig. 8.4**. It can be seen that sinusoidal mains input currents i_a, i_b and i_c result, but transient distortions exist at the mains line-to-neutral voltages' intersections. Most likely, this is due to the same mechanism that causes similar distortions of the SWISS Rectifier input currents (cf. **Chapter 3**): Due to the body diodes in the T-type inverter, the IVS output voltages u_{xy} and u_{yz} cannot be negative. This would be required for their local average values to become zero when the mains line-to-neutral voltages intersect, as both voltages show a significant switching frequency voltage ripple. An analysis of this phenomenon in the Zurich Rectifier is out of scope of this thesis.

8.2.3 Calculation of Device Currents

Due to the phase-symmetry of the DMC used in the IMDAB3R, the primary-side winding current i_p is always conducted by four DMC MOSFETs and the occurring conduction losses can be calculated from the primary-side winding

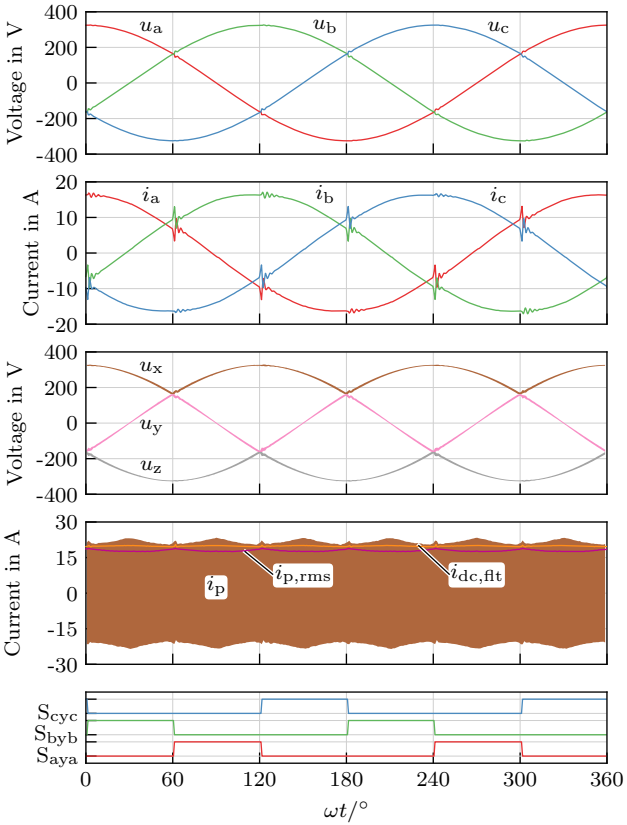

Fig. 8.4: Simulation results for an 8 kW Zurich Rectifier. The ac input currents i_a, i_b, i_c are sinusoidal with transient distortions at the intersection of mains line-to-neutral voltages u_a, u_b, u_c. These distortions are most likely due to the switching frequency voltage voltage ripple of the IVS output voltages u_x, u_y, u_z as described in **Chapter 3** for the SWISS Rectifier. Also shown are: the primary-side winding current i_p, its local rms value $i_{p,rms}$ and the low-pass filtered (first-order, cut-off frequency 2.7 kHz) dc output current $i_{dc,flt}$. The bottom plot shows the gate signals for the three bipolar switches in the IVS.

current's rms value $i_{\mathrm{p,rms}}$. This is not possible with the Zurich Rectifier, as the T-type inverter uses only a single MOSFET between nodes x and z and the output nodes g and h, but two MOSFETs, connected in series, between node y and nodes g and h.

To calculate the rms current stresses of the T-type inverter switches S_{xg}, S_{gy}, S_{yg} and S_{gz} for the operating condition defined by $\hat{U}_1$, u_{pn} and $\bar{i}_{dc}$, typically ten different mains voltage phase angles ωt are considered. For each point, the voltages u_{xy}, u_{yz}, u_{pn} and the output current reference i^*_{dc} are calculated and the corresponding switching times $\vec{t}$ are determined using a lookup table as described in **Section 7.2.5**. It can be seen in **Fig. 8.2** and **Fig. 8.3** that i_p is conducted by S_{gy} and S_{yg} either during the interval $1/2 - t_2 \leq t \leq 1/2 - t_1$ or during $1 - t_2 < t < 1 - t_1$. Assuming that the secondary-side full bride does not switch during this interval (i.e. $t_3 \leq t_1$ and $t_4 \leq t_1$), i_p changes linearly from $i_p(1/2 - t_2)$ to $i_p(1/2 - t_1)$. In this case the local rms value $\left\langle i_{S_{gyg}} \right\rangle$ over one switching frequency period can be calculated as:

$$\left\langle i_{S_{gyg}} \right\rangle = \sqrt{(t_2 - t_1)\,\zeta(i_p(\frac{1}{2} - t_2), i_p(\frac{1}{2} - t_1))} \quad , \tag{8.1}$$

where $\zeta(i_1, i_2)$ describes the mean square of a current changing linearly from i_1 to i_2 in time Δt:

$$\zeta(i_1, i_2) = \frac{1}{\Delta t} \int_0^{\Delta t} \left(i_1 + (i_2 - i_1)\frac{t}{\Delta t} \right)^2 dt = \frac{1}{3}\left[i_1^2 + i_1 i_2 + i_2^2 \right] \quad . \tag{8.2}$$

If the secondary-side full-bridge switches during the considered interval, e.g. if $1/2 - t_2 < 1/2 - t_3 < 1/2 - t_1$ holds, this can be accounted for by evaluating ζ for each linear segment of i_p as:

$$\left\langle i_{S_{gyg},\mathrm{rms}} \right\rangle = \sqrt{\begin{aligned}&(t_2 - t_3)\zeta(i_p(\frac{1}{2} - t_2), i_p(\frac{1}{2} - t_3)) \\ &\quad + (t_3 - t_1)\zeta(i_p(\frac{1}{2} - t_3), i_p(\frac{1}{2} - t_1))\end{aligned}} \quad . \tag{8.3}$$

The rms current value for one set of operating conditions, considering the whole mains voltage period, can then be found by averaging the squared current values of M (typically $M = 10$ to $M = 30$) different mains voltage phase angles ωt within one 30° mains voltage sector:

$$I_{S_{gyg},\mathrm{rms}} = \sqrt{\sum_{m=0}^{M-1} \left\langle i_{S_{gyg},\mathrm{rms}} \right\rangle^2 (\omega t = \frac{\pi}{6}\frac{m}{M-1})} \quad . \tag{8.4}$$

In the same way, the local rms values of the currents in the switches S_{xg} and S_{gz} can be calculated. Note that the local rms currents $\langle i_{S_{xg}} \rangle$ and $\langle i_{S_{gz}} \rangle$ are different, as only one of the two switches conducts during the free-wheeling periods $1/2 - t_2 < t < 1/2$ and $1 - t_2 < t < 1$. However, the two modulation schemes differ in which switch is used for free-wheeling and the modulation schemes are alternated every second mains voltage sector. Therefore, the same rms current value $I_{S_{xg},\mathrm{rms}} = I_{S_{gz},\mathrm{rms}}$ results for the switches S_{xg} and S_{gz}, when a full 2π mains period is considered. Furthermore, the currents in S_{xg}, S_{gz} and S_{gy} are orthogonal to each other, as exactly one of the switches conducts at any point in time and a Pythagorean form of Kirchoff's current law can be applied to node g:

$$I^2_{S_{xg},\mathrm{rms}} + I^2_{S_{gyg},\mathrm{rms}} + I^2_{S_{gz},\mathrm{rms}} = I^2_{\mathrm{p,rms}} \quad . \tag{8.5}$$

The rms value $I_{\mathrm{p,rms}}$ of the primary-side winding current i_p can be calculated as described in **Section 7.3.2**, which allows to calculate the rms currents in the outer T-type rectifier switches S_{xg} and S_{gz} using:

$$I_{S_{xg},\mathrm{rms}} = I_{S_{gz},\mathrm{rms}} = \sqrt{\frac{1}{2}\left(I^2_{\mathrm{p,rms}} - I^2_{S_{gyg},\mathrm{rms}}\right)} \quad . \tag{8.6}$$

Calculation results for $I_{S_{xg},\mathrm{rms}}$ and $I_{S_{gyg},\mathrm{rms}}$ are plotted in **Fig. 8.5(a)** and **(b)** respectively, as function of the dc output voltage u'_{pn} (w.r.t the primary-side) and the dc output current i'_{dc} (w.r.t. the primary-side). To obtain a plot that is independent of design specific parameters, such as the switching frequency f_{sw}, the turns ratio $n = n_\mathrm{p}/n_\mathrm{s}$ and the leakage inductance L_σ, all quantities are referenced to the primary-side. All currents are divided by a normalization current $I_{\mathrm{nom}} = \hat{U}_1/f_{\mathrm{sw}}L_\sigma$ and the output voltage is normalized by dividing it by the mains line-to-neutral voltage amplitude $\hat{U}_1$.

It can be seen in **Fig. 8.5(a)** that $I_{S_{xg},\mathrm{rms}}$ increases with increasing output current $\bar{i}'_{\mathrm{dc}}$ for all dc output voltages. Like $I_{\mathrm{p,rms}}$, $I_{S_{xg},\mathrm{rms}}$ has a minimum for $u'_{\mathrm{pn}}/\hat{U}_1 \approx 1.5$, as the dc output voltage, transformed to the primary-side, matches the average six-pulse rectified three-phase mains voltage. In most operating points, the current stress $I_{S_{gyg},\mathrm{rms}}$ of switches S_{gy}, S_{yg}, S_{hy} and S_{yh} is about half the value of $I_{S_{xg},\mathrm{rms}}$ or less [cf. **Fig. 8.5(b)**], as the free-wheeling never occurs via node y.

8.3 Comparison to the IMDAB3R

The Zurich recitifier's circuit structure is derived from IMDAB3R described in **Chapter 7**, and both create the same transformer winding voltages. Therefore,

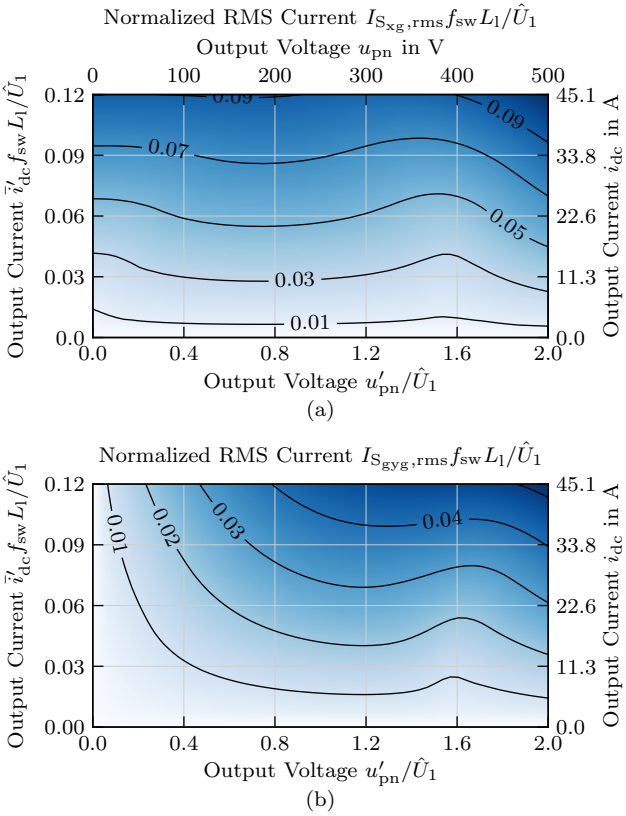

Fig. 8.5: Normalized rms currents (considering a full mains voltage period) in the T-type inverter switches (a) S_{xg} and (b) S_{gyg} as function of the dc output current $\bar{i}'_{dc}$ (w.r.t. the primary-side) and the dc output voltage u'_{pn} (w.r.t. the primary-side). All currents are multiplied with $f_{sw} L_1/\hat{U}_1$ and the output voltage is referenced to the primary-side and divided by $\hat{U}_1$ to obtain normalized quantities. For reference, the right-side and top-side axes show denormalized quantities using nominal parameters, i.e. $f_{sw} = 31\,\text{kHz}$, $L_1 = 36\,\mu\text{H}$, $n = 1.29$ and $\hat{U}_1 = 325\,\text{V}$.

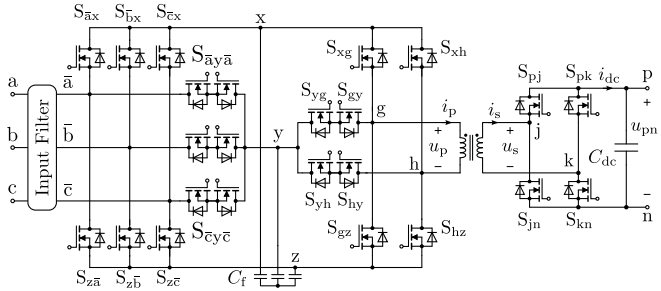

Fig. 8.6: Schematic of the Zurich Rectifier considered in the loss calculations. To reduce the IVS' conduction losses, the six-pulse diode rectifier bridge is replaced with MOSFETs $S_{\bar{k}x}$ and $S_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$, which are used as synchronous rectifiers.

the design procedure is very similar for both converters, the main difference results from the different rms current stresses of the primary-side semiconductors. A brief comparison is presented in the following.

8.3.1 Primary-Side Semiconductors

It can be seen in **Fig. 8.1** that the Zurich Rectifier requires eight MOSFETs for the T-type inverter bridge and six MOSFETs and six diodes for the IVS. For applications where a high conversion efficiency is required, the IVS diodes are typically replaced by six MOSFETs $S_{\bar{k}x}$ and $S_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$ as shown in **Fig. 8.6**. This lowers the conduction losses as described in **Section 4.3** for the SWISS Rectifier. In this case 24 MOSFETs are required for the Zurich rectifier, while 16 are sufficient to implement an IMDAB3R [cf. **Fig. 7.16(a)**].

To compare the highest possible efficiencies that can be achieved by the two circuit topologies, the same 900 V, 10 mΩ SiC MOSFETs from *Wolfspeed* (*C3M0010090K*) as used for the IMDAB3R prototype described in **Section 7.3**, are used for the Zurich Rectifier as well. These devices are considered for all eight T-type inverter switches and the outer IVS switches $S_{\bar{k}x}$ and $S_{z\bar{k}}$. As the rms currents in the IVS switches $S_{\bar{k}y\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$ are about three times lower, similar SiC MOSFET (*C2M0025120D*) form *Wolfspeed* with a higher $R_{DS(on)}$ value of 25 mΩ are considered. The selected components are summarized in **Tbl. 8.2**.

Neglecting switching frequency current ripples in the input filter and the filter's reactive power demand, the rms current stresses of the IVS switches

Tbl. 8.2: Components Considered for the Zurich Rectifier

IVS, $S_{\bar{k}x}$, $S_{z\bar{k}}$	*C3M0010090K* 900 V, 10 mΩ
IVS, $S_{\bar{k}y\bar{k}}$	*C2M0025120D* 1200 V, 25 mΩ
T-type Inverter	*C3M0010090K* 900 V, 10 mΩ
Full-Bridge	*C3M0010090K* 900 V, 10 mΩ
Transformer	same as in IMDAB3R, see **Tbl. 7.3**
EMI Filter	same as in IMDAB3R, see **Tbl. 7.4**

are defined only by the rectifier's input power. They can be calculated as:

$$I_{S_{\bar{k}x},\mathrm{rms}} = I_{S_{z\bar{k}}} = \hat{I}_1 \sqrt{\frac{\sqrt{3}}{8\pi} + \frac{1}{6}} \quad , \tag{8.7}$$

$$I_{S_{\bar{k}y\bar{k}},\mathrm{rms}} = \hat{I}_1 \sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}} \quad , \tag{8.8}$$

where $\hat{I}_1$ is the amplitude of the mains input current and can be approximated as:

$$\hat{I}_1 = \frac{2\,P_{\mathrm{in}}}{3\,\hat{U}_1} \quad P_{\mathrm{in}} = \frac{\bar{i}_{\mathrm{dc}}\,u_{\mathrm{pn}}}{\eta} \quad . \tag{8.9}$$

Note that η is the rectifier's estimated efficiency at the considered operating point.

During each switching transition of a T-type inverter half-bridge one MOSFETs is turned off and another one is turned on. However, like in the IMDAB3R, the MOSFET that is constantly turned off, also stores a charge in its nonlinear output capacitance. During the transition, its output capacitance is charged or discharged, which causes additional losses. This is considered in the calculation models but not discussed here further for the sake of brevity.

Due to the Zurich Rectifier's similarity to the IMDAB3R, the same EMI input filter, transformer and secondary-side full-bridge are assumed in the loss calculations. The Zurich Rectifier's overall losses vary significantly with the switching frequency f_{sw}, as the transformer's windings current i_{p} and i_{s} and their rms values change with the operating conditions (u_{pn}, $\bar{i}_{\mathrm{dc}}$ and f_{sw}). Furthermore the converter changes between ZCS in DCM and ZVS in CCM, causing significantly different losses. A loss-optimal f_{sw} can therefore be found for each operating point.

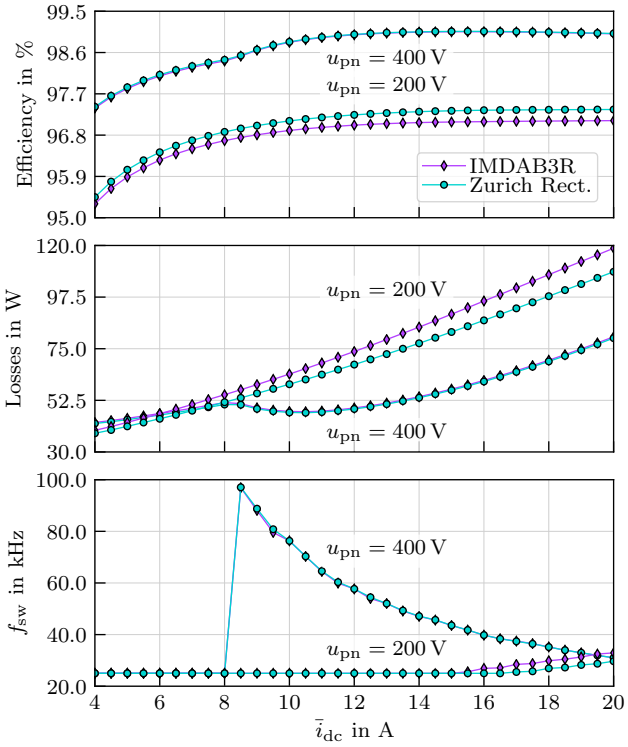

Fig. 8.7: Calculation results for an IMDAB3R and a Zurich Rectifier for the specification given in **Tbl. 8.1**. Shown are the calculated efficiency, losses and loss-optimal switching frequency f_{sw}, as a function of the dc output current $\bar{i}_{dc}$ for two different output voltages u_{pn}.

8.3.2 Calculation Results

Calculated efficiency, losses and loss-optimal switching frequency values f_{sw} for the Zurich Rectifier and the IMDAB3R are plotted in **Fig. 8.7** as function of the output current $\bar{i}_{dc}$. Two different dc output voltages $u_{pn} = 400\,V$ and $u_{pn} = 200\,V$ are shown. It can be seen that the results calculated for the two circuit topologies are almost identical for $u_{pn} = 400\,V$. In this case the conduction losses of the Zurich Rectifier's T-type inverter are lower than the conduction losses in the IMDAB3R's DMC, because only two or three MOSFETs conduct i_p in the T-type inverter, but four MOSFETs conduct i_p

in the DMC. Adding the additional conduction losses occurring in the IVS, almost identical losses result for the Zurich Rectifier and the IMDAB3R.

This is not the case for $u_{pn} = 200\,V$ as can be seen in **Fig. 8.7**. In this case, both converters operate in DCM and the primary-side winding voltage u_p is zero for about two thirds of the pulse period due to the low output voltage. In the Zurich Rectifier only two MOSFETs, either S_{xg} and S_{xh} or S_{gz} and S_{hz}, conduct i_p during this free-wheeling period. Compared to the DMC, this reduces the T-type inverter's conduction losses more than the additional conduction losses in the IVS. Hence, the Zurich Rectifier achieves approximately 9 % lower losses than the IMDAB3R when the dc output voltage u_{pn} is half the rated voltage.

8.4 Summary and Conclusions

In this chapter, a new isolated single-stage indirect matrix-type three-phase PFC rectifier circuit, denominated as Zurich Rectifier, is proposed and analyzed. The basic circuit structure is similar to a conventional DAB dc-dc converter, however, on the primary-side a mains-frequency commutated IVS and a T-type, three-level inverter bridge are used to sequentially connect the mains line-to-line voltages to the transformer's primary winding. This combination of an IVS and a T-type inverter offers the same degrees of freedom as a three-to-two line DMC that is used in the IMDAB3R. Therefore the same modulation scheme can be employed, resulting in the same transformer voltage and current stresses. Compared to the IMDAB3R, the Zurich Rectifier requires two additional MOSFETs and six additional diodes. For very high efficiencies these diodes can also be replaced by MOSFETs used as synchronous rectifiers.

As in other PFC rectifier circuits that use an IVS, the input filter capacitors are preferably installed between the IVS and the T-type inverter to reduce the conduction losses in the IVS semiconductors. This also allows to use a half-bridge-like commutation pattern for the T-type inverter that is significantly simpler to implement than the four-step sequences required by the IMDAB3R. Calculations show that the Zurich Rectifier can achieve the same efficiency as the IMDAB3R with nominal output voltage $u_{pn} = 400\,V$ when using the same 900 V SiC MOSFETs. As the Zurich Rectifier has a lower number of MOSFETs in the conduction path used during free-wheeling, its losses at $u_{pn} = 200\,V$ are about 9 % lower than those of the IMDAB3R.

In a next step, a Zurich Rectifier hardware demonstrator should be implemented to verify the benefits predicted by the theoretical considerations given

in this chapter. As the calculated semiconductor losses are almost identical to those of the IMDAB3R, a similar heat sink can be used. As the volume of the eight additional MOSFETs, which are required by the Zurich Rectifier, is small compared to the rest of the converter, it can be assumed that the Zurich Rectifier can achieve a power density similar to the IMDAB3R.

9

Conclusions and Outlook

Rectifiers are an essential part of power electronics, as in many applications a dc load needs to be supplied from an ac source. The first rectifiers precede the age of electronics and mostly used electromechanical systems of rotating or vibrating contacts to perform the rectification. Mercury arc rectifiers were discovered at the beginning of the 20th century and allowed more reliable systems as they require no moving parts. With the introduction of thyristors in the 1950's, modern power electronics started to develop and controlled rectifiers became possible, which allow to control the dc output voltage without mechanical parts such as contactors.

Loads in excess of approximately 4 kW are typically supplied from the three-phase ac mains, and not just from a single-phase voltage, due to the reduced cabling effort in the mains and because the power drawn from a single-phase ac voltage pulsates with twice the mains frequency. Furthermore, in many applications the mains currents' shape is regulated by standards such as *IEC 61000-3-2*, *IEC 61000-3-4* and *IEEE 519*, which limit the allowed amplitude of current harmonics. Usually the total harmonic distortion of the mains currents needs to be less than 5 % of the nominal input current. Corresponding circuits, which are capable to create a dc output voltage and sinusoidal input currents, in phase with the ac voltages, are usually called PFC rectifiers. They can be classified according to the allowed ac/dc voltage

ratios: For boost systems the dc output voltage needs to be at least as high as the ac line-to-line voltage's peak value. Similarly the output voltage can at most be as high as $\sqrt{3}/2 \approx 0.87$ times the ac line-to-line voltage's peak value for buck rectifiers and it can be higher or lower for buck-boost systems.

While boost-type PFC rectifiers received considerably more attention in scientific and industrial research, several applications exist where buck-type systems could be beneficial. These include the charging of electric vehicle batteries, dc microgrids that are envisaged as future power distribution concepts within office buildings and residential areas, or dc powered data centers. In these applications dc voltages of around 400 V are required with power levels of tens to hundreds of kW. Buck-type PFC rectifiers are an interesting option in this case, as they enable to power these dc loads from the three-phase ac mains with typical rms line-to-line voltages in the range of 400 V to 480 V using only a single conversion stage. For systems with high utilization, i.e. where the rectifier is operated most of the time, such as data centers, it has been shown that the cost of dissipated power has a significant impact on the total cost of ownership, which creates a need for ultra-efficient PFC rectifiers. A high efficiency is also beneficial from an ecological point of view, as about two thirds of the world's electricity production still originates from fossil fuels.

9.1 Results

This thesis begins with an overview of boost-, buck- and buck-boost-type three-phase PFC rectifier circuit topologies, stating their inventors and citing original publications wherever possible. Several isolated matrix-type PFC rectifiers, which perform a power conversion between the three-phase mains and an isolated dc voltage without a significant intermediate energy storage element, are shown as well. These systems are furthermore classified into phase-modular and phase-integrated circuits. Possible applications for buck-type PFC rectifiers are discussed and an overview of studies on the global electricity consumption of data centers is given, showing that an annual consumption of around 300 TW h is realistic. Assuming a cost of 0.1 EUR per kW h, this implies that the world's data centers have an annual power cost of 30 billion EUR.

Four circuit topologies are selected for an in-depth analysis in this thesis: The non-isolated buck-type SWISS Rectifier and the closely related Integrated Active Filter (IAF) rectifier, as well as the phase-modular isolated matrix-type Y/Δ (IMY/D) rectifier and the isolated matrix-type buck-boost DAB

three-phase rectifier.

Three chapters of this thesis focus on various aspects of the non-isolated, buck-type SWISS Rectifier. First, the limits for reactive power generation are investigated, showing that its input currents can lead or lag the corresponding mains phase voltages by up to ±30°. This implies that inductive or capacitive reactive power can be generated, however, it is limited to 57.7 % of the active power drawn from the mains. Analytical equations for the reactive power generation's impact on the semiconductor current stresses and the resulting additional conduction losses are derived as well. Furthermore, the SWISS Rectifier's operation with unsymmetrical mains voltages is analyzed, showing that the conventional modulation and control schemes generate a constant output current even for unsymmetrical mains voltages. This results in distorted mains input currents. A modification to the control circuit is proposed to achieve ohmic mains behavior, which is usually preferred, as it reduces losses in distribution lines and transformers caused by low-frequency current harmonics.

Like in other buck-type PFC rectifier circuits, the SWISS Rectifier's mains currents exhibit distortions whenever two mains voltages intersect. It is shown that the root cause for these distortions is the switching frequency voltage ripple of the input filter capacitors, which forces an additional input rectifier diode to conduct. An analytical expression is derived, which allows to estimate the resulting mains current THD for given filter parameters, mains and switching frequency. In order to mitigate these distortions, the input filter capacitors are first moved to the output side of the rectifier input stage, which allows a temporary pulse width modulation of the input stage around the line voltage intersections. Furthermore, this modifications reduces the conduction losses in the input stage and shortens the commutation paths of the switching stage. Simple analytic approximations for the optimal pulse widths are derived, which can be evaluated online by the rectifier's controller. Simulation and measurement results taken on a 7.5 kW prototype confirm that the input current THD can be reduced from 4.2 % to $\leq$ 1.6 % and show that the concept is tolerant to distortions and unbalance of the mains voltages.

Another approach to mitigate the SWISS Rectifier's input current distortions is to reduce the input filter capacitor's voltage ripple by using an interleaved switching stage. This also allows to use a larger total semiconductor die area, which reduces conduction losses without paralleling individual switches. This is usually challenging in hard switching converters, as parasitics can lead to unequal current sharing, increasing losses. The additional output inductors required for the interleaved switching stages can be com-

bined with the EMI filter's common-mode inductor into a single magnetic device called Integrated Common-Mode Coupled Inductor (ICMCI). The required core can be assembled from four conventional U cores, each carrying one winding. This structure achieves current compensation and hence allows close coupling among all windings, which reduces the output current ripple and lowers the corresponding high-frequency winding losses. Based on an analysis of the ICMCI's magnetic structure and using a common-mode / differential-mode separation matrix, a control block diagram is proposed that allows a decoupled control of all winding currents and ensures equal current sharing among the individual half-bridges.

A highly efficient interleaved SWISS Rectifier is designed by selecting SiC MOSFETs, magnetic cores, wire type and number of turns, etc. to achieve minimal losses. An 8 kW prototype system is built, which achieves a power density of 4 kW/dm^3. For 400 V rms line-to-line input and 400 V dc output voltage, a peak efficiency of 99.26 % is measured at 60 % load with electrical and high precision calorimetric methods and a full-load efficiency of 99.16 % is achieved. These measurements include the losses of the power stage, as well as those of gate drivers, control, fans and all other auxiliary components, no further power supplies besides the three-phase mains are used. This is important, as about 60 % of the total losses occur in the semiconductors and $\approx$ 20 % in the magnetic components. Approximately 10 % are caused by the EMI filter, PCBs etc and the remaining 10 % result from auxiliary systems such as gate drivers, control and fans. Compliance with the CISPR 11 Class B EMI conducted emission limit is confirmed by measurements. These results show that highly efficient three-phase buck-type PFC rectifiers can be built using commercially available SiC MOSFETs operated in hard switching, combined with ferrite and nanocrystalline cores and solid wire windings. The resulting efficiency curve as function of the output power is quite flat, an efficiency $\geq$ 99 % is achieved for $\geq$ 30 % output current and nominal voltages. This is beneficial for applications requiring high availability, such as telecommunication and data center power supplies, which typically employ two, or more, redundant rectifiers, each rated for full power. For output currents higher than half the rated value, the losses show only little dependence on the mains voltage, for a ±15 % input voltage variation the losses change by approximately ±10 %.

The fact that dissipated power constitutes a significant amount of operating costs in certain applications such as data centers, motivates the use of life cycle costs (LCC) as a metric in power converter design. In this case LCC, also known as total cost of ownership (TCO), is defined as the sum

of investment cost for buying the converter (e.g. a rectifier) plus the cost of power dissipation during the service life. Note that the latter consists not only of the raw electricty cost, but includes additional costs for cooling, power distribution and standby generators, as well as economic factors such as interest rate and discounting of future savings, and can therefore be as high as twice the raw electricity price. Considerations for a 380 V dc distribution data center with 24/7 operation and an assumed dissipation cost of EUR 0.12 per kW h show that, for a service life of 10 years or more, SiC MOSFETs used as mains frequency rectifier achieve roughly the same LCC as conventional silicon diodes, even though SiC MOSFETs have about 10 times higher first costs. Analytical design equations are derived, which allow to select cost-optimal die areas (i.e. $R_{\mathrm{DS(on)}}$ values) for MOSFETs given defined current, service life, first costs and switching frequency. A similar approach can be used to select cost-optimal core materials and sizes for all magnetic components. By carrying out these calculations for several switching frequencies, a cost-optimal frequency can be selected. Using this approach, a cost-optimal three-phase buck-type interleaved Integrated Active Filter (IAF) rectifier for 380 V dc data center applications is designed, showing that converter designs with an efficiency of 99 % and a power density of $4\,\mathrm{kW/dm^3}$ are economically feasible for a service life of 10 years or more. A prototype using these specifications and commercially available SiC MOSFETs, SiC Schottky diodes and nanocrystalline core materials is built. Measurements confirm a full-load efficiency of 99 %, an input current THD of 2 % and compliance with CISPR 11 Class B EMI emission limits.

Some applications suitable for buck-type PFC rectifiers require galvanic isolation between the ac mains and the load due to safety regulations (e.g. in electric vehicle charging) or due to different grounding schemes on the ac and dc-side (e.g. in dc data centers). Isolated matrix-type rectifier topologies are an interesting option in this case, as they allow a single-stage conversion between the mains and the dc bus and do not require any intermediate mains frequency energy storage elements such as electrolytic capacitors. One circuit analyzed in this thesis is the isolated phase-modular indirect matrix-type Y/Δ (IMY/D) rectifier, which consists of three identical phase-modules that are similar to dc-dc forward converters. These isolated phase-modules can be connected in star (Y) or delta (Δ) at the mains interface, which allows a very wide input voltage range without oversizing. Besides this, the IMY/D rectifier features a simple modulation, where each phase-module uses a phase shift modulator to create a square wave signal with a duty cycle proportional to the corresponding ac input voltage. The rectifier's control structure is equally straightforward,

as it is essentially equal to a conventional buck converter. Unlike in many other three-phase rectifiers, no coordinate transformations and/or methods to determine the mains voltage phase angle are required. It is shown that zero voltage switching (ZVS) can be achieved with sufficiently large load currents like in a conventional dc-dc forward converter. Furthermore, a third harmonic current injection method is proposed for delta-configuration, which allows to either increase the output voltage by 15 % or to reduce the conduction losses by adapting the transformer's turns ratio. Measurements taken on a hardware prototype confirm an input current THD of 1.5 % and that ZVS is achieved. The proposed ZVS modulation and the third harmonic current injection method allows a 10 % reduction of the conversion losses. An efficiency of 97.2 % results for a nominal output power of 7.5 kW.

Finally, in an attempt to create a 99 % efficient isolated three-phase PFC rectifier circuit, the matrix-type buck-boost Dual Active Bridge (DAB) three-phase PFC rectifier is analyzed. This is a promising circuit, since it requires only a single isolation transformer with sufficient leakage inductance, but no inductors. All EMI input filter inductors are operated with small voltage ripples and negligible current ripple and can hence be built with low losses. While this circuit topology has been published before, a high ac current THD of 12 % was reported, which is not suitable for PFC rectifiers. An equivalent circuit model, similar to a conventional DAB converter, is derived in this thesis that allows to analyze the modulation and to formulate an optimization problem. This is solved numerically by nonlinear programming to obtain a lookup table serving as modulation function for the converter. Using this lookup table, a mains current THD of 3.0 % was measured on a prototype rectifier, which is comparable to other PFC rectifiers. Like in a conventional DAB converter, the proposed modulation achieves ZVS for sufficiently large load currents and zero current switching otherwise. Using 900 V SiC MOSFETs and a switching frequency of 31 kHz, the 8 kW prototype rectifier achieves a power density of 4 $\mathrm{kW/dm^3}$ and was measured to have an outstanding full-load efficiency of 99.0 %.

The direct matrix converter used in this prototype requires sophisticated multi-step commutation sequences and a correspondingly complex modulator. To overcome this disadvantage, a modification of the circuit topology is proposed, which replaces the direct matrix converter by the series connection of an input rectifier stage commutated at mains frequency and a T-type three-level inverter bridge. This eliminates the need for multi-step commutation patterns, but eight additional MOSFETs are required. Calculations show that the same, or a higher efficiency results, depending on the output voltage.

9.2 Outlook

Since the beginning of power electronics, dozens of isolated and non-isolated, boost-, buck- and buck-boost three-phase PFC rectifier circuits have been proposed and analyzed in scientific literature. Presumably, this variety is the result of efforts to create circuits that perform well in a defined application, or make the best possible use of the available technology. However, various performance measures, such as efficiency, power density, weight, cost, control complexity, reliability, scalability, fault tolerance, etc. exist and their assessment depends on the considered application. It is therefore extremely unlikely that a single optimal rectifier circuit topology, which outperforms others in all measures, will be invented in the future. Rather, only gradual improvements of a few, selected performance measures can be expected from new circuits. Ideally, each one should be analyzed with respect to several aspects, in order to provide a full picture. Similarly, novel technologies and devices, such as SiC MOSFETs, GaN HEMTs or improved ferromagnetic core materials, should be seen as an incentive to re-evaluate well-known circuits, as well as unfamiliar ones, and not just as a drop-in replacement. Changing the device will likely affect several performance aspects of a circuit and might change which topology is best suited for a given application.

Regarding electric vehicle battery fast-charging as potential application for buck-type three-phase PFC rectifiers, economic challenges result from the investments required to build a fast-charging infrastructure along major highways. Further research regarding the LCC of power distribution and conversion systems would be beneficial for both industry and policy makers, to serve as an objective basis for taking decisions. Ideally, the environmental impact and other factors should be studied as well, in order to enable a fact-based discussion and to identify conflicting goals, for example between low investment cost systems leading to comparatively high conversion losses, which increase the environmental impact, e.g. due to green house gas emissions from electricity production. The situation is somewhat different for dc microgrids, as a functional ac based distribution system already exists in developed countries and it seems unlikely that this will be replaced by dc distribution solely for efficiency benefits, especially as the required investment cost is high and the service life of the employed equipment is usually several decades. However, in new installations, dc microgrids could be a viable option, provided that sufficient dc capable house hold appliances, IT equipment, lamps, etc are available.

Regarding LCC alone, the situation seems to be clear for applications

using power converters with a high utilization, such as data centers: Due to the low losses of wide bandgap semiconductors and the comparatively high costs for electricity and cooling, LCC optimal systems are required to have a very high efficiency, typically $\geq 99\,\%$ for power levels above $\approx 10\,\mathrm{kW}$. Challenges result, as investment and operational costs of data center infrastructure are usually allocated to different accounts within an organization or might even be split between two or more separate companies. This leads to a prisoner's dilemma, where the resulting overall system is not cost-optimal, even though all businesses, rationally, try to minimize their expenses. However, the ongoing trend towards cloud computing, where software, calculation power, and storage are bought as a service from a provider, might solve this issue. Assuming that the service provider owns and operates the required data center, an incentive to minimize overall LCC results.

The prototypes designed in this thesis might serve as benchmark for achievable efficiencies in three-phase buck-type PFC rectifiers with commercially available technology at the time of publication. With advances in semiconductor devices towards lower conduction and switching losses, as well as lower loss magnetic core materials, even higher efficiencies of 99.5 % and above will become possible. Recently published theoretical analyses show that these efficiencies should be achievable for 10 kW three-phase multi-level boost-type PFC rectifiers [195]. Further research and experimental verification is required to confirm this and to assess if this is also achievable with buck- and buck-boost-type PFCs.

All three converters designed in this thesis have the same volume and power rating, and hence achieve the same power density. However, it seems difficult to draw clear conclusions from this fact as the implications of any converter's volume depend heavily on the application. It is clear that if two different converters have the same power, first cost, efficiency, reliability, etc., the smaller one is generally preferable, but this is a very unlikely situation. Assuming that a Pareto front of efficiency, or first cost, versus power density is known from design calculations, how much more volume would a customer accept to get a loss or first cost reduction of, for example, 1 %? The problem with this trade-off is that usually the approximate shape of a product is specified early in the design, or is already given if a converter is designed as replacement for an existing product. In this case, any reduction in volume below the required value is basically useless. For higher power levels further restrictions arise from handling, such as the maximum weight a single person is allowed to lift by safety regulations, or from constructional restrictions: Is the customer willing to tear down a wall because the converter won't fit

through the door? So while it is of course a valid question to ask what volume (or better maximum and minimum dimensions) a converter has in order to assess its performance, power density should not be considered as a linear scale: A new converter, with the same efficiency but half the volume is not twice as good than the old one. An exception that comes to mind are data center operators in rapidly expanding markets, with a high utilization of their IT equipment. If customers cannot be served and revenue is lost because of insufficient resources, any space that is occupied by power converters instead of servers has an associated opportunity cost. This linearly translates volume into cost. However, this seems to be an exceptional case and presumably will only last for a limited amount of time, as the company and its competitors have a strong financial incentive to expand their operations and satisfy the customers' demand.

By the large, analysis, assessment and comparison of power electronic converter topologies remain an ongoing task, due to enhancements in power semiconductors and magnetic materials, as well as new circuit topologies. Such comparisons should ideally not be limited to the converter and its technical details, but include the targeted application and the resulting economical factors and environmental impacts.

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