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Low-Noise and Low-Distortion Switch-Mode Power Amplifiers for Nano-Positioning Applications

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Try not. Do, or do not. There is no try.
– Yoda

Für meine Eltern.

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Mario Mauerer

Abstract

Integrated semiconductor structures continuously shrink in size and grow in complexity, driven by the incessant digitization of our everyday lives. Likewise, the corresponding industrial manufacturing tools and processes keep pushing technological limits to achieve this feat, for example with the upcoming adoption of extreme ultraviolet lithography, which facilitates semiconductor technology node sizes below 10 nm. Thus, nanometer-precision mechatronic positioning systems are essential tools for this industry. They are used for various applications, such as the positioning and moving of semiconductor wafers in lithography, inspection, or other manufacturing processes. Different electromagnetic actuators, like permanent magnet linear motors or magnetically levitating bearings, are employed. The force- and torque-producing electric currents of these actuators must be free of noise and other unwanted signal components to prevent the generation of undesired forces that otherwise lead to positioning errors. Thus, shrinking semiconductor features and more complex manufacturing processes demand an increasing accuracy and precision of the positioning actuators and their corresponding driving currents. Similarly, the demand for a high manufacturing throughput increases the required actuator output powers.

Traditionally, the desired low-noise and low-distortion actuator currents are provided by linear amplifiers due to their inherently low output noise. However, the achievable power conversion efficiencies are limited and high output powers cannot be generated in the vicinity of precision motion systems due to thermal constraints. Hybrid amplifiers, which combine a linear amplifier with a switch-mode power electronic converter, strive to alleviate these restrictions. Nonetheless, such systems are more complex and require careful tuning to achieve the desired load current quality.

This thesis investigates output noise and distortion of high-power, digitally controlled switch-mode (Class-D) amplifiers for precision positioning and motion applications. Such power converters feature simple and scalable topologies, which reduces development time and cost. The resulting implications on important sources of noise and distortion within such systems are carefully and comprehensively analyzed. Amplifier constituents that critically affect noise and distortion are identified and optimized. Extensive measurements on small- and full-scale hardware prototypes verify the findings.

In a first step, suitable and modern wide-bandgap power electronic switching devices and converter topologies are analyzed, using detailed computer circuit simulations that model both the electrical and thermal power transistor

behavior, with the aim of identifying arrangements of inherently low distortion. Two promising power stage topologies, namely the regular interleaved half-bridge and the dual buck converter, are identified.

Next, a novel low-jitter gate driver is presented, which circumvents flaws of digital signal isolators that are commonly required in power electronic converters. It is shown how such isolators often introduce significant amounts of signal jitter, which leads to critical wideband noise in the amplifier output waveforms. Furthermore, the developed gate driver is capable of withstanding fast voltage transients across its isolation barrier, which is a necessity for the reliable control of fast-switching wide-bandgap power transistors. Measurements corroborate the functionality and effectiveness of the circuit.

Similarly, wideband noise arises from digital pulse-width modulators due to their limited amplitude resolutions. Thus, digital delta-sigma modulation is employed, in conjunction with regular PWM methods, which introduces the capability to shift this noise to higher frequencies, where it does not affect mechatronic positioning systems. A suitable modulation structure for digital implementations is identified and optimized for noise attenuation and stability. Simulations and measurements demonstrate the achievable noise reduction in the pulse-width modulated power transistor control signals.

Digital feedback control systems, characterized by a high design flexibility, improve the quality of the amplifier output waveforms significantly. However, accurate sensors for the feedback signals are essential. Consequently, all important elements of voltage and current acquisition systems are analyzed and optimized for the application in the discussed power amplifier systems. This includes shunt-based and integrated current sensors, high-voltage resistive dividers, operational amplifiers, analog anti-aliasing filters and oversampled analog-to-digital converters with their respective digital decimation filters.

The different insights and developments culminate in the construction of a full-scale power amplifier hardware demonstrator. It operates with an input voltage of 400 V DC and can provide AC and DC load currents with amplitudes up to 25 A (peak), while reaching output current signal-to-noise ratios of more than 100 dB and similarly, total harmonic distortion figures of less than −100 dB. It is capable of implementing two distinct power conversion topologies in order to thoroughly investigate their distortion performances. The utilized gallium nitride power transistors enable half-bridge interlock times as low as 30 ns, and switching frequencies reach 200 kHz. The efficacies of the discussed key amplifier elements are demonstrated with comprehensive measurements that aim to highlight the influence of individual sources of noise and distortion.

Furthermore, the demonstrator's high-performance digital processing system enables a real-time Kalman filter implementation that is executed at a rate of 100 kHz. It is used to reduce sensor noise, which consequently improves the amplifier output current signal-to-noise ratio. Interestingly, the amplifier's linearity is slightly affected by the Kalman filter and thus, important design criteria are identified to circumvent this effect.

Similarly, two real-time distortion compensation techniques are presented. The first calculates the voltage errors caused by the half-bridge interlock time in great detail and adjusts the duty cycles accordingly, which significantly reduces distortion. The second method considers the instantaneous DC supply voltage for forming the half-bridge duty cycles, which improves the system's power supply rejection.

Finally, the thesis concludes with a summary and discussion of the obtained insights. An outlook for future research possibilities is also given.

Kurzfassung

Ausgehend von der stetigen Digitalisierung in allen Bereichen unseres Alltags weisen Strukturen von integrierten Halbleiterbauelementen zunehmend kleinere und komplexere Geometrien auf. Dementsprechend werden die technologischen Grenzen der zugrunde liegenden industriellen Herstellungsprozesse zunehmend ausgelotet, zum Beispiel mit der anstehenden Einführung der EUV-Lithografie (extremes Ultraviolett), welche die Herstellung von Halbleitern mit Strukturbreiten unter 10 nm ermöglicht. Mechatronische Positioniersysteme mit Genauigkeiten im Nanometer-Bereich sind damit essenziell für diesen Industriezweig. Sie werden für verschiedene Aufgaben wie das Positionieren oder genaue Bewegen von Halbleiterwafern bei Belichtungsprozessen, der Inspektion oder anderen Herstellungsschritten eingesetzt. Verschiedene elektromagnetische Aktuatoren, wie zum Beispiel Permanentmagnet-Linearmotoren oder magnetische Schwebelager, werden dafür benötigt. Die elektrischen Ströme dieser Aktuatoren erzeugen Kräfte oder Drehmomente und müssen entsprechend frei von Rauschen und anderen unerwünschten Signalkomponenten sein, um störende Positionierungsfehler zu vermeiden. Die Entwicklung von immer kleineren Halbleiterstrukturen und komplexeren Fertigungsmethoden verlangt eine zunehmende Genauigkeit und Präzision dieser Aktuatoren und deren elektrischen Ströme. Gleichzeitig verlangt der Wunsch nach höheren Produktionsdurchsätzen eine steigende Ausgangsleistung der Aktuatoren.

Die benötigten rausch- und verzerrungsarmen Ströme werden herkömmlicherweise von linearen Verstärkern bereitgestellt, welche ein inhärent tiefes Ausgangsrauschen aufweisen. Allerdings sind die erreichbaren Leistungsumwandlungseffizienzen begrenzt und hohe Ausgangsleistungen daher in der Nähe von Präzisions-Positioniersystemen aufgrund thermischer Einschränkungen nicht realisierbar. Hybridverstärker, welche eine lineare Verstärkungsstufe mit einem Schaltkonverter kombinieren, können eingesetzt werden, um diese Einschränkungen zu umgehen. Jedoch haben solche Systeme einen komplexeren Aufbau und müssen vorsichtig abgestimmt werden, um die nötige Stromqualität zu erreichen.

Diese Dissertation untersucht das Rauschen und die Verzerrung in Ausgangssignalen von digital gesteuerten Hochleistungs-Schaltverstärkern für die Anwendung in Präzisions-Positioniersystemen. Solche Leistungskonverter bieten einfache und skalierbare Topologien, was die Entwicklungszeit und Kosten reduziert. Die Auswirkungen von wichtigen Quellen von Rauschen und Verzerrung in solchen Systemen werden präzise und tiefgreifend untersucht. Verstärkerelemente, welche diese Effekte kritisch beeinflussen,

werden identifiziert und optimiert. Umfangreiche Messungen an diversen Hardwareprototypen bestätigen die Resultate.

In einem ersten Schritt werden sowohl geeignete und moderne Leistungshalbleiter mit breitem Bandabstand, als auch verschiedene Konvertertopologien analysiert. Mit detaillierten computerbasierten Schaltungssimulationen, welche das elektrische und das thermische Verhalten modellieren, werden Schaltungskonfigurationen bestimmt, welche inhärent tiefe Verzerrungen aufweisen. Zwei vielversprechende Topologien werden identifiziert, wobei die erste auf der phasenversetzten Taktung zweier Brückenzweige basiert und die zweite als *Dual Buck* Konverter bekannt ist.

Als Nächstes wird ein neuartiger Transistor-Gatetreiber mit tiefem Jitter präsentiert. Diese Treiberschaltung kann Einschränkungen von digitalen Signalisolatoren, welche oft in leistungselektronischen Systemen benötigt werden, effektiv vermeiden. Der normalerweise beträchtliche Jitter der Isolatoren wird vom Treiber effektiv unterdrückt, wodurch Transistor-Steuersignale mit tiefem Rauschen erzeugt werden können. Der Gatetreiber ist außerdem fähig, mit schnellen Spannungstransienten über seiner Isolationsbarriere zu arbeiten, was eine essenzielle Eigenschaft für das zuverlässige und schnelle Schalten von Leistungshalbleitern mit breitem Bandabstand darstellt. Messungen bestätigen die Funktion und Effektivität der Schaltung.

Digitale Pulsbreitenmodulatoren erzeugen aufgrund ihrer begrenzten Amplitudenauflösung ebenfalls breitbandiges Rauschen. Darum wird die Delta-Sigma Modulation präsentiert, welche es, zusammen mit herkömmlichen Pulsbreitenmodulatoren, ermöglicht, das Rauschen zu höheren Frequenzen zu verschieben, wodurch es das mechatronische Positioniersystem nicht mehr beeinträchtigt. Eine geeignete Modulationsstruktur für digitale Systeme wird eingeführt und optimiert, um eine maximale Rauschunterdrückung bei einem stabilen Betrieb zu ermöglichen. Simulationen und Messungen legen die erreichte Rauschreduktion in den pulsbreitenmodulierten Transistor-Steuersignalen dar.

Digital gesteuerte Regelungssysteme sind flexibel einsetzbar und können die Qualität der Verstärker-Ausgangssignale erheblich verbessern. Sie benötigen jedoch präzise Sensoren für die rückgeführten Messsignale. Darum werden alle wichtigen Elemente von Spannungs- und Strommesssystemen für den Einsatz in den betrachteten Schaltverstärkern analysiert und optimiert, wobei sowohl Simulationen als auch Messungen zum Einsatz kommen. Dies beinhaltet die Untersuchung von widerstandsbasierten und integrierten Stromsensoren, Widerstandsteilern für hohe Spannungen, Operationsverstär-

kern, analogen Anti-Aliasing Filtern und überabgetasteten Analog-Digital-Wandlern mit deren digitalen Dezimierungsfiltern.

Die verschiedenen Resultate und Entwicklungen werden in einem realistischen Leistungsverstärker-Prototyp vereint. Der Verstärker arbeitet mit einer Eingangsspannung von 400 V DC und kann Ausgangsströme (AC und DC) von bis zu 25 A bereitstellen. Der Rauschabstand des Ausgangsstromes erreicht mehr als 100 dB und die Gesamt-Oberschwingungsverzerrung liegt bei unter −100 dB. Ausserdem kann der Verstärker mit zwei verschiedenen Konvertertopologien betrieben werden, was die genaue Untersuchung der jeweils resultierenden Ausgangsstromverzerrungen erlaubt. Die verwendeten Galliumnitrid-Leistungstransistoren ermöglichen kurze Halbbrückenverriegelungszeiten von 30 ns und Schaltfrequenzen bis zu 200 kHz. Die Leistungsfähigkeit der präsentierten Systemkomponenten wird mit umfangreichen Messungen aufgezeigt, welche auch deren individuelle Auswirkungen auf Rauschen und Verzerrung darstellen.

Das digitale Hochleistungs-Signalverarbeitungssystem des Prototyps ermöglicht des Weiteren die Implementierung eines in Echtzeit berechneten Kalman Filters, wobei eine Ausführungsfrequenz von 100 kHz erreicht wird. Dadurch wird Sensorrauschen weitestgehend unterdrückt, was den Rauschabstand des Verstärkerausgangssignals erhöht. Interessanterweise wird die Linearität des Verstärkers leicht beeinträchtigt, weshalb Auslegungsgrundsätze aufgezeigt werden, um den Effekt entsprechend zu minimieren.

Weiterführend werden zwei Vorsteuerungsmethoden präsentiert, welche ebenfalls in Echtzeit ausgeführt werden. Mit der ersten Methode können die Fehler bei der Spannungsbildung der Halbbrückenzweige, verursacht durch deren Verriegelungszeiten, detailliert berechnet und entsprechend über das Tastverhältnis korrigiert werden, was die Verzerrung der Ausgangssignale markant reduziert. Der zweite Ansatz berücksichtigt die momentane DC-Versorgungsspannung des Verstärkers bei der Bildung der Tastverhältnisse der Brückenzweige, was eine erhöhte Unterdrückung von Störungen der Versorgungsspannung mit sich bringt.

Die Dissertation endet mit einer Zusammenfassung und Diskussion der Ergebnisse, sowie einem Ausblick auf zukünftige Forschungsansätze.

Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
BTL	Bridge-Tied Load
CM	Common-Mode
CMTI	Common-Mode Transient Immunity
CPU	Central Processing Unit
DB	Dual Buck
DC	Direct Current (0 Hz)
DM	Differential-Mode
DSP	Digital Signal Processor/Processing
E-HEMT	Enhancement-Mode HEMT
EMF	Electromotive Force
EMI	Electromagnetic Interference
FDA	Fully Differential Amplifier
FEM	Finite Element Method
FF	Feedforward
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
HB	Half-Bridge
HEMT	High-Electron-Mobility Transistor
HF	High Frequency
HV	High Voltage
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
IIR	Infinite Impulse Response
IMD	Intermodulation Distortion
LV	Low Voltage
MFB	Multi-Feedback Filter Topology
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NCS	Noise-Coupled Noise Shaper
NS	Noise Shaping
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PLL	Phase-Locked Loop

PWM	Pulse-Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SINAD	Signal-to-Noise-and-Distortion Ratio
SMD	Surface-Mount Device
SNR	Signal-to-Noise Ratio
SoC	System on a Chip
STF	Signal Transfer Function
TB	Triple Buck Topology
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion plus Noise
WBG	Wide-Bandgap

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1 Introduction

Power Amplifiers are electronic devices that provide a high-power replication of a low-power control signal. They emerged with the proliferation of long-range communication and detection systems in the early twentieth century that required the undistorted generation of signals with elevated power levels [1]. Vacuum tubes, in conjunction with magnetic amplifiers, were widely used to provide amplification, both for high-frequency signals used in radio transmission or radar, and for low-frequency signals carrying human speech [2–4]. Consequently, audio amplification systems were prominent early adopters of vacuum tube amplifiers and their output signal quality was an important performance measure, due to the high sensitivity of the human auditory system [5–8].

The discovery and widespread application of the solid-state transistor in the 1950s was a milestone for power amplification due to the versatility and reliability of these fundamental contributors to power electronics [9]. However, the employed amplifiers were widely based on linear power stage topologies that limit the achievable power conversion efficiencies, to values of typically less than 70 %. Naturally, switch-mode amplifiers, characterized by higher efficiencies, emerged in lockstep [10–12].

Nowadays, such power amplifier systems are widely utilized on a large scale due favorable properties regarding power losses, reliability, versatility, scalability and cost-effectiveness. The results of this thesis are applicable to most of these systems. Hence, in the following, important applications of power amplifiers are outlined, with a special focus on ultra-high-precision mechatronic positioning and motion systems.

1.1 Power Amplifier Applications

Increased signal power levels are required in virtually any imaginable industrial and commercial electronic device. Thus, amplifiers manifest in wide frequency and power ranges, both encompassing several orders of magnitude. A typical and widespread application for such amplifiers is the audio signal amplification, where, e.g., in mobile handsets, output powers are in the milliwatt range, but can reach kilowatt levels for large-scale concert systems. Noise and distortion of such amplifiers are key characteristics, as a good signal replication is desired [13, 14]. Due to the nature of human auditory perception, the amplifier performance is critical in a frequency range from several hertz up to ≈20 kHz.

Medical imaging applications depend heavily on highly linear amplifiers with output signals of low distortion. In magnetic resonance imaging (MRI), gradient amplifiers are responsible for creating well-defined magnetic fields, for which they are required to deliver fast-changing output currents in excess of 100 A, whereas the current quality directly affects the imaging capability [15–18]. Certain computed tomography machines utilize X-rays to obtain the desired insights. The necessary high-energy radiation is generated by steering an electron beam inside a vacuum tube onto a metal target. In order to focus the X-rays, or to move the corresponding beam, the electron stream must be exactly positioned, for which power amplifiers are utilized [19, 20].

High-energy particle physics research also depends on the precise manipulation of accelerated atomic constituents. This can be achieved with electromagnetic deflection systems, whose controlling currents, which are often in excess of several hundred ampere, are provided by power amplifiers. For such applications, current noise and stability are important for an accurate alignment of the particle beams [21, 22].

Well-controlled currents are commonplace in mechanical positioning applications, which often employ electromagnetic actuators. Terrestrial telescopes require the precise positioning and tracking of their mirrors and antennas to seek the desired celestial objects [23]. Furthermore, automated industrial processes often employ robots or manufacturing machines such as mills, and increasingly, 3D printers, that require the accurate handling of the workpiece and similarly, exact actuator currents. In microscopy applications, or other tasks that involve precision optics, linear piezo actuators are commonly used and require a low-noise voltage supply to avoid positioning errors. Some optical applications rely on magnetic bearings that are supplied with well-defined currents to obtain the desired accuracy [24].

This thesis focuses on power amplifiers in the context of nano-precision positioning applications, which are accompanied by special considerations that demand exceptional properties of the employed power amplifiers, as highlighted in the following.

1.1.1 Nano-Positioning

The integrated semiconductor manufacturing industry relies heavily on high-precision mechatronic positioning systems that are essential for different processes such as lithography, wafer dicing or inspection [25]. During exposure in lithographic processes by specialized machines (wafer scanners), the semiconductor wafers, as well as the reticles, are continuously moved to apply the desired patterns. All motion must be exactly controlled to avoid errors [26–30]. Similar processes that are based on precise and continuous movements are used for the manufacturing of display panels, which requires long-stroke positioning stages [31]. Active vibration isolation systems are commonly placed between the motion system and the ground to attenuate mechanical movements and forces, caused by nearby equipment or seismic activity. They rely on short-stroke and dynamic actuators, whose output forces must be of low noise to prevent the generation of undesired movements [32–35].

Fig. 1.1 exemplarily illustrates a precision positioning stage and its active vibration isolation system. Such stages often employ single- and three-phase linear or rotary actuators like permanent magnet synchronous motors, reluctance motors, voice coils or magnetically levitating bearings, in order to provide accelerating forces or torques [36, 37]. Closed-loop control systems, which regularly use position sensors with resolutions in the sub-nanometer range, increase the positioning accuracy and disturbance rejection. They provide the reference signals for the power amplifiers that generate the desired actuator currents. Thus, the amplifiers in such applications often provide controlled output currents, in contrast to, e.g., audio amplifiers, which usually generate voltage signals. Generally, the fundamental frequencies of the actuator currents range from DC to several hundred hertz, which is defined by the specific task of the motion system (e.g., continuously moving wafer scanners or vibration isolation systems). The upper frequency limit is given by the achievable positioning speed of the motion systems, which is commonly restricted by the high-resolution position sensors. It is also influenced by the design of the electromagnetic actuators (e.g., number of magnetic pole pairs).

Fig. 1.1: High-precision mechatronic positioning system used in integrated semiconductor manufacturing [38]. The power amplifiers are located in the base. A vibration isolation system (blue color) rejects disturbances from the ground. The long-stroke actuators reach accelerations of 12 m/s^2 and speeds of 1.2 m/s. The position stability is given as ±25 nm, with a repeatability of ±400 nm.

As the defining structures of the semiconductor wafers become ever smaller and more complex, it is estimated that the signal-to-noise ratio (SNR) of the amplifier output currents needs to increase by ≈20 dB every five years to keep track with industry demands [39]. Currently, the amplifiers are expected to deliver load current SNR figures in excess of 110 dB, and the total harmonic distortion should be below −100 dB. These requirements are accentuated by the increasing adoption of extreme ultraviolet (EUV) lithography, which is also driven by the demand for more intricate semiconductor features [40, 41]. This introduces the need for precision magnetic levitation stages due to the fact that the semiconductor wafers have to reside in a vacuum to allow the efficient propagation of the EUV radiation [42–46].

Consequently, the supporting structures used in nano-precision positioning stages, such as air or magnetic bearings, are often characterized by low mechanical friction and damping. Thus, actuator forces easily translate to movements. This is especially critical in a frequency range from DC to ≈10 kHz, in which the motion systems provide little damping in the transfer functions from actuator forces to the corresponding accelerations, and in which they exhibit their critical dynamics (e.g., mechanical mass-spring-damper resonances). Thus, actuator currents must be of high precision in

this frequency band, as undesired current components otherwise generate disturbing motion.

As a consequence, linear amplifiers, regularly based on power operational amplifiers or discrete devices, are traditionally preferred for precision positioning applications, due to their inherently low output powers over wide frequency ranges, combined with low output impedances [31, 47]. Their noise and linearity can be further improved with closed-loop feedback control systems that can be implemented in the analog or digital domain, whereas the former intrinsically features low noise levels due to the absence of (digital) amplitude quantization [28, 29]. However, linear amplifiers collectively suffer from limited efficiencies and low output powers. Hybrid amplifiers strive to alleviate these restrictions by combining linear amplifiers with high-power and efficient switch-mode converters [48, 49]. Nevertheless, such topologies increase the complexity of the electrical circuit and, if utilized, the feedback control systems, as the fundamentally different characteristics of the linear and switched conversion stages, with respect to their dynamics and input/output impedances, have to be analyzed and stabilized individually. This increases cost and development effort. Furthermore, these heterogeneous systems do not scale well, i.e., inherently different systems, such as discrete amplifiers instead of integrated devices, must potentially be employed to obtain amplifiers with higher output powers. This is not the case for switch-mode power converters, as their fundamental structures and conversion principles can remain unaltered in a wide range of applications.

The power requirements of motion systems in the semiconductor manufacturing industry are continuously increasing due to growing wafer diameters that necessitate more massive positioning systems. Additionally, the desire for an increased throughput demands higher accelerations and thus, higher actuator forces. Naturally, this translates to higher amplifier output powers [39, 50]. Restrictions on the thermal dissipation in the vicinity of nanometer-precision mechanical systems, which are in place to prevent unwanted changes in length of structural components due to thermal expansion, prohibit the usage of high-power and inefficient linear or hybrid amplifiers [51, 52]. In the foreseeable future, peak actuator powers in the kilowatt range up to $\approx$10 kW are required, especially during fast movements, e.g., in inspection processes where wafers are re-positioned with high accelerations between different analysis steps, to maintain a high production throughput. Amplifier load current amplitudes of up to $\approx$50 A and output voltages in excess of 100 V are desired to support a wide range of actuator types.

Analog amplifier control systems, i.e., feedback control algorithms implemented by means of analog signal processing elements, such as operational amplifiers, require a considerable development effort as they are implemented with distinct physical systems that need to be built, tested and modified to achieve the desired performance. Digital systems, where the control laws are embodied by calculations in the digital domain, are more flexible and quickly deployed on different converter systems with only minor modifications, which reduces development time and cost. Furthermore, they allow the implementation of advanced signal processing structures such as Kalman filters, which is practically not possible with analog solutions.

Consequently, this thesis analyzes key influence factors on the output signal quality of fully digitally controlled, pulse-width modulated, switch-mode (Class-D) power amplifiers. In the following, currently achieved performance figures of various types of amplifiers are outlined with respect to their noise and distortion.

1.2 State-of-the-Art Amplifier Systems

Power amplifiers manifest with wide ranges of output powers, operating frequencies and designs. Nonetheless, output noise and distortion figures can generally be compared.

1.2.1 Noise

Amplifier output noise data of commercial or research systems is often not provided due to its more complicated definition and measurement method. **Fig. 1.2** gives an overview of the best achievable signal-to-noise ratio (SNR) figures and output powers of a selection of industrial solutions.

The noise of integrated Class-D audio amplifier circuits (ICs) [53–62, 68, 69] is given for the stand-alone circuit itself and is thus expected to deteriorate once employed in a complete amplifier system, due to the influences of other system components such as the DC supply. This is corroborated by the reduced performance of complete Class-D audio amplifier systems [63, 65]. Linear amplifiers are often limited in output power, but show low output noise levels [64, 66]. Similarly, operational amplifiers with low output noise figures are available, while also being limited in power [73]. Switch-mode MRI amplifiers can offer very high output powers, but noise is generally also elevated [16]. Hybrid amplifiers combine an analog power stage with a switch-mode converter, or provide some other analog means of correcting

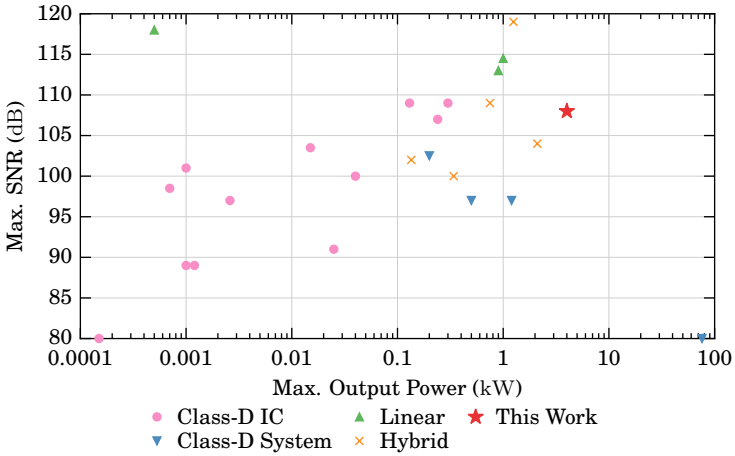

Fig. 1.2: Reported signal-to-noise ratio (SNR) performance of commercial amplifiers. Noise bandwidth for SNR figures is ≤20 kHz. Higher SNR values at higher output powers are favorable. References: [16, 53–72].

the output of a switched stage, e.g., by using an analog feedback control system. Consequently, they offer low output noise levels while also achieving high output powers. However, their efficiencies are often still less than that of switch-mode converters, and their structures are inherently more complex [70–72]. The system presented in this work achieves high SNR figures at high powers, which also exceed the performance of other switch-mode amplifiers [67].

1.2.2 Distortion

Amplifier linearity is an important characteristic and can be more conveniently apprehended than noise, which renders achieved values of industrial and research systems generally more available. **Fig. 1.3** illustrates the best reported total harmonic distortion (THD) of numerous systems.

As with the SNR figures presented above, distortion values of integrated Class-D power amplifier circuits (ICs) neglect additional sources of nonlinearity such as output filters or nonideal DC voltage supplies [53–62, 68, 69, 74, 77]. Hence, complete switch-mode audio amplifiers perform significantly worse than the stand-alone integrated circuits [63, 65, 75, 76, 78]. High-power linear gradient amplifiers for MRI applications, or laboratory-grade general-

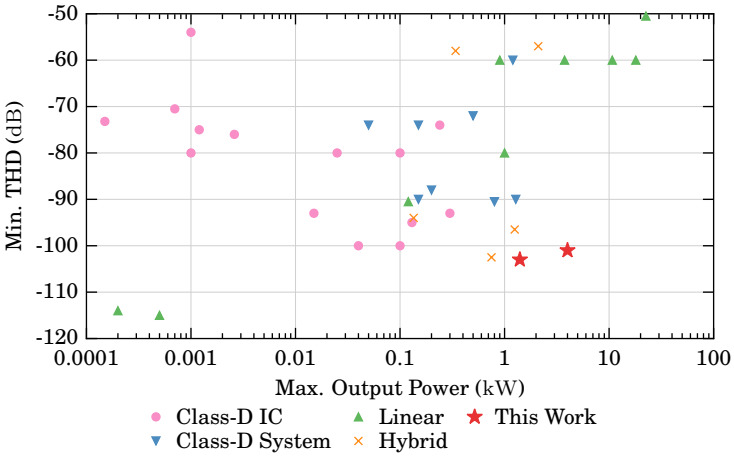

Fig. 1.3: Reported total harmonic distortion (THD) figures of common amplifiers. This work presents two power-stage topologies, differing by their distortion performance and output capability. Lower THD values at higher achievable output powers are favorable. References: [39, 53–85].

purpose systems, can supply currents in excess of 100 A, but their THD is limited [64, 66, 79–82]. Low-power operational amplifiers achieve the best output distortion [73, 84], while the linearity of power operational amplifiers deteriorates [85]. Hybrid power amplifiers show, similar to their noise levels, also low output distortion figures, at the cost of system complexity [70–72]. The dual buck switch-mode power topology, which is also investigated in this work, produces inherently low THD figures, with the disadvantage of significantly increased power semiconductor losses [39, 67, 83]. The distortion performance of the dual buck topology, as well as the regular Class-D switching stage, which are both presented in this thesis, achieve low linearity figures at the demonstrated high power levels.

1.3 Aims and Contributions

The objective of this thesis is to analyze individual sources of noise and distortion in digitally controlled, high-power switch-mode amplifiers. Different interacting nonlinear effects give rise to unwanted amplifier output signal components, which render a rigorous mathematical analysis difficult. Thus,

in order to determine the impacts of deteriorating effects within distinct amplifier subsystems, computer simulations and hardware demonstrators are employed, as they allow the analysis of noise and distortion, as well as the optimization, of individual system components. Different methods and circuits are introduced and developed in order to improve the achievable amplifier performance. Additionally, a versatile and high-power amplifier demonstrator system is built, which, due to the flexibility of its key systems, also delivers important insights into the behavior of output noise and distortion.

The central contributions of this thesis to the knowledge base of precision switch-mode power amplification are listed below:

- Evaluation of different power semiconductor transistor technologies with respect to amplifier output distortion. Extensive computer circuit simulations, which include thermal loss models, recreate the detailed transistor switching behavior. The resulting distortion, caused by the nonideal switching transitions and the modulation of important transistor on-state conduction resistances, is investigated and compared.

- Optimization of different low-distortion power stage topologies, namely the regular interleaved half-bridge and the dual buck power stages, whereas the latter can be improved and amended to further reduce distortion. Circuit simulations that employ the aforementioned transistor models facilitate a performance evaluation.

- Development of an isolated, low-jitter gate driver that is also immune to fast common-mode voltage transients across its isolation barrier. This enables low-noise amplifier output signals while also achieving high transistor switching speeds, which reduces distortion and switching losses. The findings are verified with a hardware prototype.

- Investigation of delta-sigma modulation (noise shaping) techniques that can create digital signals of low amplitude resolutions, while shifting the resulting quantization noise to high frequencies. A specific modulator implementation that is suitable for digital systems is optimized with respect to its noise attenuation capability and stability. Measurements on a hardware demonstrator verify the results.

- Analysis of voltage and current sensor technologies with respect to noise and distortion. In-depth investigations and measurements are performed on different integrated circuits and sensors, including shunt resistors, isolated current sensors, high-voltage dividers, operational

amplifiers and high-order filters, to determine their inherent noise and linearity. Digital filters for oversampled analog-to-digital (ADC) conversion systems are optimized with respect to their phase delay in order to improve the stability margins of closed-loop control systems. Signal jitter in isolated ADCs can introduce significant noise to the measurements and hence, in the application of a half-bridge current sensor, a design guideline for the respective half-bridge inductor is given.

- Design of a digital, high-gain, closed-loop control system that is capable of being executed at high frequencies, which provides a significant disturbance rejection and reference tracking performance. This lowers noise and distortion in amplifier output signals.

- Implementation of a real-time Kalman filter algorithm to reduce residual sensor noise. High execution rates are targeted to maintain the high gains of the feedback controllers. Measurements demonstrate the achievable performance.

- Development and verification of control system feedforward compensation techniques to improve amplifier linearity. The error caused by the half-bridge interlock time is calculated in real-time and the duty cycle can be adjusted accordingly. A similar approach is employed to consider variations of the amplifier DC supply voltage.

- Design and construction of a full-scale hardware demonstrator system (400 V, 25 A) to verify the aforementioned analyses and circuits of its individual system components. Extensive measurements in a well-defined setting are performed and unprecedented noise and distortion levels are achieved.

- Additional approaches and concepts for digital switch-mode power amplifiers are discussed that could enhance the achieved performance figures even more.

1.4 Enabling Technologies

The following technological contributors emerged in recent times and permit unprecedented noise and distortion performance figures of all-digital, highly efficient switch-mode power amplifiers.

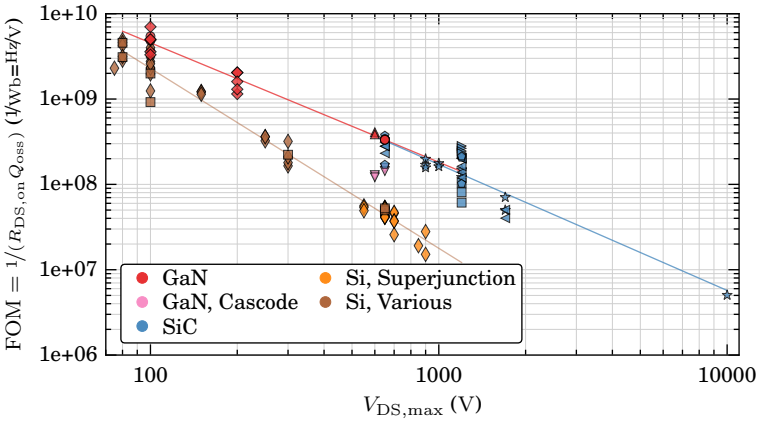

Fig. 1.4: Figures of merit (FOM) of 114 commercially available GaN, SiC and regular silicon (Si) power transistors. The 10 kV device is not yet commercial but detailed in [86]. The output charge Q_{oss} is found by numerically integrating the voltage-dependent output capacitance C_{oss} (which is commonly provided by manufacturer datasheets), up to a voltage of $2/3 V_{\mathrm{DS,max}}$ [87]. $R_{\mathrm{DS,on}}$ is the typical on-state conduction resistance at 25 °C. The GaN cascode devices are not considered for the linear fit line. The markers encode different manufacturers. Note that this performance comparison does not include reverse recovery effects.

- Wide-bandgap power semiconductors have, due to their utilization of new semiconductor materials and arrangements, significantly reduced parasitic capacitances while still achieving low conduction resistances, as **Fig. 1.4** reveals. GaN power switching transistors with suitable voltage and current ratings for the considered applications recently became commercially available. They enable fast switching transitions and high switching frequencies. The lack of reverse recovery effects further reduces losses. These are favorable attributes for low-distortion amplifier output waveforms. Furthermore, the correspondingly required high-frequency gate driving and signal isolation circuits advanced synchronously.

- High-performance digital processing systems offer the close integration of modern central processing units (CPUs) with field-programmable gate arrays (FPGAs). This allows a flexible combination of digital logic circuits and procedural programs, which empowers significant data throughput rates and short processing times. This facilitates high execution rates of digital feedback control systems and the possibility to implement advanced control methods.

- Analog-to-digital converters with high amplitude resolutions and sampling rates enable oversampled, low-noise acquisition systems that are key elements of precision power converters with digital feedback control. Furthermore, auxiliary circuits like low-jitter, high-speed and high-voltage digital signal isolators, which are capable of transmitting the resulting data at high rates from the ADC systems, allow the usage of such ADCs in the context of power electronic converters.

1.5 Thesis Outline

- **Chapter 2** first defines performance metrics related to noise and distortion, which are used throughout this work. Next, a comprehensive overview of prominent sources and mechanisms of noise and distortion in switch-mode power amplifiers is presented.

- **Chapter 3** introduces detailed power transistor circuit simulation models that cover the electrical and thermal domain to identify suitable devices and circuit topologies with respect to distortion. The dual buck power stage topology, designed to prevent distortion caused by half-bridge interlock time, is presented and extended in order to improve its

performance. Circuit simulations are performed to identify system parameters to which the achievable power stage output distortion reacts with high sensitivity.

- **Chapter 4** identifies the need for transistor gate control signals that are free of signal jitter, which otherwise introduces significant wideband noise to the switching stage power waveforms. Digital signal isolators are identified to be a considerable source of such jitter. Therefore, an isolated gate driver circuit is presented that is capable of rejecting the jitter of any signal isolator. Furthermore, it is immune against common-mode voltage transients of high slew rates, which are commonplace in fast-switching converters. Extensive measurements on small- and large-scale demonstrators prove its functionality and effectiveness.

- **Chapter 5** introduces delta-sigma modulation (noise shaping) in the context of power electronic converters. It is shown how commonly used digital pulse-width modulators create significant quantization noise due to their low amplitude resolutions. Thus, noise shaping is employed to shift the quantization noise to higher frequencies, where it is of no concern for the considered applications. The method is implemented in the digital domain and requires little resources. Computer simulations are used to optimize the achievable noise attenuation, and measurements verify the performance.

- **Chapter 6** discusses methods and possibilities for the creation of low-noise and low-distortion voltage and current sensors that are suitable for power electronic converters. First, it is shown that shunt resistors achieve a sufficiently high linearity, despite thermal self-heating. This is in contrast to integrated, isolated current sensors, which provide an insufficient noise and distortion performance, as verified with measurements. Next, noise of high-voltage dividers, employing large resistance values, is analyzed. It is demonstrated that they can achieve high SNR figures. The linearity of operational amplifiers is extensively measured and compared, as manufacturer data is often inconsistent. Furthermore, it is shown that intricate circuits based on operational amplifiers, such as higher-order filters, can achieve low noise and distortion. Oversampled analog-to-digital conversion lowers the inherent quantization noise of ADC devices. The required digital decimation filter is optimized with respect to its phase delay such that the stability margins of potentially employed feedback control systems are only

minimally affected. Finally, if the ADC is placed on an isolated potential, and the data is transmitted using (jittery) digital signal isolators, it is analytically shown, for the application of a half-bridge current measurement, how a reduction of the SNR can be prevented by designing the half-bridge inductor appropriately.

- **Chapter 7** introduces the full-scale hardware demonstrator used to verify the performance of the different system components, and to demonstrate the achievable noise and distortion figures of its output current. The power topology employs modern GaN switching transistors and allows to implement two different power stages. Furthermore, the transistor loss model is presented and used to identify the achievable load currents, and to verify that the thermal variation of the transistor junction temperatures does not significantly influence distortion. Similarly, the closed-loop feedback control system is illustrated and modeled. Extensive measurements of load current noise and distortion demonstrate the achieved performance. The influence of individual system components, such as the noise shaping modulators or the DC supply, are demonstrated.

- **Chapter 8** exhibits how a real-time Kalman filter can be used to effectively eliminate sensor noise, to which the feedback control system reacts sensitively. A high execution rate of the algorithm is made possible by the capable digital signal processing system of the hardware demonstrator. The design and implementation of the utilized steady-state Kalman filter is presented. Measurements of noise and distortion are performed to expose the method's influences.

- **Chapter 9** illustrates two approaches to reduce amplifier distortion, by adopting feedforward compensation techniques. First, the voltage errors, introduced by the half-bridge interlock intervals, are calculated in real-time and used to correct the corresponding duty cycles, which significantly reduces distortion. Similarly, the variation of the DC-link voltage can be measured to adapt the half-bridge duty cycles accordingly, which improves the amplifier's power supply rejection.

- **Chapter 10** briefly summarizes key results and findings of this thesis. An outlook on future research is also given.

1.6 List of Publications

Key insights presented in this thesis have been published at international conferences, at workshops and in reputable scientific journals, while some contributions are covered by corresponding patents.

Journal Papers

- M. Mauerer and J. W. Kolar, "Noise Minimization for Ultra-High SNR Class-D Power Amplifiers," *CPSS Transactions on Power Electronics and Applications*, accepted for publication.
- M. Mauerer and J. W. Kolar, "Distortion Minimization for Ultra-Low THD Class-D Power Amplifiers," *CPSS Transactions on Power Electronics and Applications*, accepted for publication.
- M. Mauerer, A. Tüysüz and J. W. Kolar, "Low-Noise Isolated Digital Shunt for Precision Class-D Power Amplifiers," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1907–1910, Mar. 2018.
- M. Mauerer, A. Tüysüz and J. W. Kolar, "Low-Jitter GaN E-HEMT Gate Driver With High Common-Mode Voltage Transient Immunity," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9043–9051, Nov. 2017.

Conference Papers

- M. Mauerer, A. Tüysüz and J. W. Kolar, "Voltage/Current Measurement Performance and Power Supply Rejection in All-Digital Class-D Power Amplifiers," in *Proc. of the IEEE Industrial Electronics Society Conference (IECON)*, pp. 666–673, Oct. 2016.
- M. Mauerer, A. Tüysüz and J. W. Kolar, "Gate Signal Jitter Elimination and Noise Shaping Modulation for High-SNR Class-D Power Amplifiers," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1198–1205, Mar. 2016.

  Outstanding Presentation Award

- M. Mauerer, A. Tüysüz and J. W. Kolar, "Distortion Analysis of Low-THD/High-Bandwidth GaN/SiC Class-D Amplifier Power Stages," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2563–2571, Sept. 2015.

  Best Overall Poster Award

Workshops

- M. Mauerer and J. W. Kolar, "Minimization of Switching Stage Non-Idealities for Ultra-Low THD Class-D Power Amplifiers," presented at the *IEEE Power Electronics Society Workshop: "Interlock Times – Necessary, Useful or Not Needed at All?,"* Warsaw, Poland, Sept. 2017.

Patents

- M. Mauerer and J. W. Kolar, "Electrical Power Converter and Method for Controlling an Electrical Power Converter," EU Patent EP18207576, 2018.
- M. Mauerer and J. W. Kolar, "Circuit Arrangement for Controlling Power Transistors of a Power Converter," US Patent US20170149428A1, 2017.
- M. Mauerer and J. W. Kolar, "Schaltungsanordnung zur Ansteuerung von Leistungstransistoren eines Umrichters (in German)," EU Patent EP3171516A1, 2015.

Further Scientific Contributions

- L. Schrittwieser, M. Mauerer, D. Bortis, G. Ortiz and J. W. Kolar, "Novel Principle for Flux Sensing in the Application of a DC + AC Current Sensor," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 4100–4110, Sept. 2015.

- L. Schrittwieser, M. Mauerer, D. Bortis, G. Ortiz and J. W. Kolar, "Novel Principle for Flux Sensing in the Application of a DC + AC Current Sensor," in *Proc. of the International Power Electronics Conference (IPEC ECCE Asia)*, pp. 1291–1298, May 2014.

2

Noise and Distortion in Power Amplifiers

Different sources of noise and distortion in power amplifier systems originate from nonlinear effects that can resist a rigorous mathematical modeling approach. This fact contributes to the motivation of this thesis, which investigates the impacts of distinct causes of noise and distortion on the amplifier output signal quality with detailed computer simulations and hardware prototypes. Critical system components are identified, which can then be specifically optimized for the desired performance.

Fig. 2.1 illustrates a generic switch-mode power amplifier conversion system that is operated with digital control methods. Common sources of noise and distortion are indicated. Such a system serves as a digital-to-analog converter, as the power stage replicates the digital control signals in the analog domain. As this replication is never ideal, due to the rectangular waveforms of the reference signals, which are difficult, if not impossible, to accurately form with power electronic switches, noise and distortion are introduced. Throughout this thesis, the term *digital* characterizes a system that operates with signals that are updated only at distinct, regularly spaced time steps, and that are described by a set of discrete (i.e., quantized) amplitude levels (which are usually also regularly spaced). This is in contrast to the *analog* domain, where signals vary continuously in time and their amplitudes are not subject to a defined set of levels (neglecting quantum physical effects).

In the following, important sources of noise and distortion in the discussed amplifier systems are described in more detail. However, **Sec. 2.1** first introduces noise and distortion metrics used throughout this work. **Sec. 2.2** then presents sources of noise and **Sec. 2.3** introduces nonlinear effects that cause harmonic distortion.

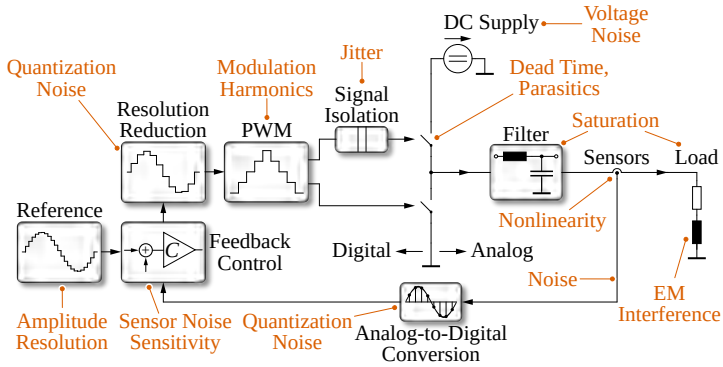

Fig. 2.1: Important sources of noise and distortion in a generic, digitally controlled power amplifier system that essentially serves as a digital-to-analog converter.

2.1 Performance Metrics

Varying methods are commonly used to classify noise and distortion of signals. Thus, this section introduces the definitions that are employed throughout this thesis, which enables consistent comparisons of measurements and performance figures.

Regularly used metrics are based on frequency spectra of signals, as they often contain information that is relevant for precision amplification in a more suitable form than time-domain measurements. The signal-to-noise ratio (SNR) relates the power of desired signal components to the power of unwanted noise, which is commonly also present in the signal, and is a widely used metric for any amplifier. The linearity of an amplification system is independent of noise, and is usually qualified by relating spectral signal components that are caused by nonlinear amplifier transfer characteristics to the desired output signal component, resulting in the figure of the total harmonic distortion.

In the following, the two metrics are defined and described in detail.

2.1.1 Total Harmonic Distortion

Amplifier output distortion is caused by a nonlinear amplification of the input signal s_{in}, which results in a distorted output s_{out}. The corresponding amplifier transfer characteristic from its input to the output does thus not only contain the amplifier gain G, but also nonlinear terms. In a first approximation, such

a transfer characteristic could exemplarily be given as

$$s_{\text{out}} = G s_{\text{in}} + c_1 s_{\text{in}}^2 + c_2 s_{\text{in}}^3. \tag{2.1}$$

If the input signal is assumed to be sinusoidal, with a fundamental frequency ω_{F} such that $s_{\text{in}} = a \sin(\omega_{\text{F}} t)$, the following amplifier output results:

$$\begin{aligned} s_{\text{out}} = \underbrace{Ga \sin(\omega_{\text{F}} t)}_{\text{Desired Output}} + \underbrace{\frac{1}{2} c_1 a^2}_{\text{DC Offset}} + \underbrace{\frac{3}{4} c_2 a^3 \sin(\omega_{\text{F}} t)}_{\text{Freq. } \omega_{\text{F}}} - \\ \underbrace{\frac{1}{2} c_1 a^2 \cos(2\omega_{\text{F}} t)}_{\text{Freq. } 2\omega_{\text{F}}} - \underbrace{\frac{1}{4} c_2 a^3 \sin(3\omega_{\text{F}} t)}_{\text{Freq. } 3\omega_{\text{F}}}. \end{aligned} \tag{2.2}$$

Simplifying results in

$$s_{\text{out}} = s_0 + s_1 \sin(\omega_{\text{F}} t) - s_2 \cos(2\omega_{\text{F}} t) - s_3 \sin(3\omega_{\text{F}} t). \tag{2.3}$$

Consequently, the amplifier nonlinearity is reflected in the amplitudes of the signal components at integer multiples of ω_{F}. This is commonly used to classify amplifier distortion, with the measure of the total harmonic distortion (THD), defined as follows:

$$\text{THD} = 20 \log_{10} \frac{\sqrt{s_2^2 + s_3^2 + \cdots + s_k^2}}{s_1}. \tag{2.4}$$

Note that s_1 is the signal amplitude of the fundamental component (at frequency ω_{F}) and $s_{2\ldots k}$ are the amplitudes of the first $k-1$ integer harmonics of the fundamental (at frequencies $k\omega_{\text{F}}$, with $k \in \{2, 3, \ldots\}$) [88]. In practical low-distortion amplifiers, only the first few harmonics significantly affect distortion and thus, harmonics are considered up to $k = 9$ for the calculation of the THD in this work, unless otherwise specified.

In order to measure the amplifier output THD, a sinusoidal reference signal with negligibly small distortion and fundamental frequency $\omega_{\text{F}} = 2\pi f_{\text{F}}$ is applied to the amplifier input (or provided as a digital reference for the amplifier control system). The amplifier then generates a nearly sinusoidal output waveform whose frequency spectrum contains the amplitudes $s_1 \ldots s_k$ of the desired fundamental signal and its integer harmonics. The spectrum is usually obtained by calculating the (discrete) fast Fourier transform (FFT) of the obtained time-domain output waveform measurements [89, 90]. By

varying the amplifier gain or the input signal amplitude, the behavior of the THD can be recorded at different operating points, which provides insights into the amplifier's distortion mechanisms.

2.1.2 Signal-to-Noise Ratio

Noise behaves differently than ordinary signals in the sense that it does not occur at distinct frequencies, but rather its power is distributed over a certain frequency band. Furthermore, noise is often caused by random processes or interference. Consequently, to compare figures of noise, the respective frequency band in which the noise power is considered, must be given.

Throughout this thesis, the term *noise* encompasses all undesired components of a signal, except the harmonics that are caused by amplifier nonlinearities, as shown in Sec. 2.1.1 above. Thus, distinct signals like spectral components at 50 Hz, which are prominently caused by electromagnetic interference (EMI) originating from the power grid, are also accounted to the noise power [91].

A signal can be decomposed into its individual spectral components. If it is nearly sinusoidal (with fundamental frequency ω_F and some integer harmonics), this decomposition could be given as

$$s = \underbrace{s_1}_{\text{Desired Component}} \underbrace{+ s_2 + s_3 + \cdots + s_k}_{\text{Harmonics}} + \underbrace{s_\mathrm{n}}_{\text{Noise}}. \tag{2.5}$$

The signal-to-noise ratio (SNR) is a common metric to classify a signal's desired power in relation to its noise power and is defined as

$$\mathrm{SNR} = 10 \log_{10} \frac{P(s_1)}{P(s_\mathrm{n})}. \tag{2.6}$$

$P(s_1)$ is the power of the desired signal component. If it is a sinusoidal signal (which is not a necessary condition), it has the fundamental frequency ω_F. $P(s_\mathrm{n})$ encompasses the power of the signal's noise components. Note that any potential harmonics of the desired signal (s_k), e.g., caused by amplifier nonlinearity, are, like $P(s_1)$, not attributed to the power of the noise. Similarly, the DC component s_0 is also not considered [88]:

$$P(s_\mathrm{n}) = \int_{\mathrm{DC}}^{10\,\mathrm{kHz}} P(s)\mathrm{d}f - \sum_{k=0}^{\infty} P(s_k). \tag{2.7}$$

Fig. 2.2 further illustrates this. It is essential that the frequency band, in which the noise power is accounted for, is stated when SNR values are provided, due to the fact that a noise signal generally distributes its power over wide frequency ranges. In this work, which considers power amplifiers for precision mechatronic systems, the noise power is critical in a frequency range from DC (0 Hz) to 10 kHz and thus, this is the frequency range used for the SNR figures, unless otherwise indicated.

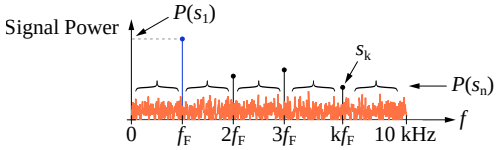

Fig. 2.2: Noise power considered for the SNR excludes the power of the signal at the fundamental frequency f_F and its harmonics. The frequency band from DC to 10 kHz is critical for mechatronic motion systems.

2.1.3 Other Metrics

Although not further considered, other common metrics for the classification of noise and distortion are briefly presented for the sake of completeness.

- SINAD is the signal-to-noise-and-distortion ratio, which is similar to the SNR definition presented in (2.6), but also includes the power of the integer harmonics in conjunction with the noise power. It is the inverse of the THD+N.
- THD+N represents the total harmonic distortion and noise. Unlike the THD definition in (2.4), it not only considers the power of the harmonics, but also the noise power. It is the inverse of the SINAD.
- IMD stands for intermodulation distortion and represents another method to quantify amplifier linearity. Instead of a single-frequency input signal, as used in the THD definition (see Sec. 2.1.1), an input signal with two distinct frequencies is used. Due to system nonlinearities, harmonics will also arise at the sum and differences of the two input frequencies, whose amplitudes are used to form the IMD figure [88]. This method allows quantifying amplifier distortion at higher frequencies, which could be impossible with the THD measurement method introduced above, as the integer harmonics of high-frequency fundamental

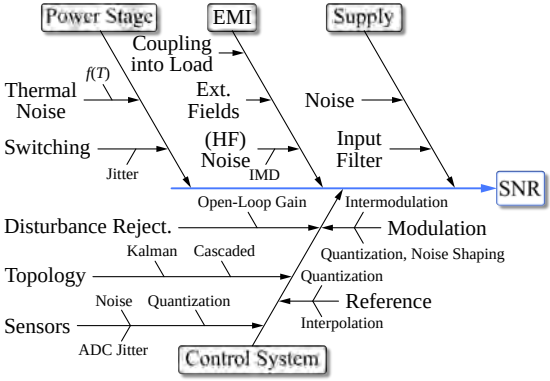

Fig. 2.3: Nonidealities of system components and parameters that affect the SNR of the output quantities of digitally controlled power amplifier systems.

signals can be outside the bandwidth of the measuring device. The two frequencies of the input signals in an IMD measurement are usually selected such that the intermodulation products are placed within the measurement bandwidth. However, modern measuring equipment provides sufficiently wide bandwidths, and in mechatronic positioning systems, for which the investigated amplifiers are intended, common actuator fundamental frequencies typically do not exceed several hundred hertz. Consequently, the THD measurement method described in Sec. 2.1.1 is sufficient.

2.2 Noise Sources in Power Amplifiers

Noise is often generated by random processes and its energy is distributed in a certain frequency band [92, 93]. Such processes, among others, are also found throughout digitally controlled power amplifiers as illustrated in **Fig. 2.3**, which lists important factors and system components that influence amplifier output noise power.

Digital control of power electronic converters gives rise to different important sources of noise, mostly caused by the inherent amplitude quantization of digital signals. The resulting quantization noise generally has a uniform power density in a frequency band from DC to the Nyquist frequency (which is half of the sampling rate of the digital system) [88]. The noise power depends

on the available number of quantization levels, as they define the magnitudes of the amplitude errors when a continuous signal is quantized [88, 94]. Consequently, this source of noise is reduced by selecting a sufficiently high amplitude resolution for digital signals.

Pulse-width modulators (PWM) are often used to create the binary switching transistor control signals in power electronic converters [95]. They are generally implemented using digital counters, whose counting rates are limited by the performance of digital circuits. As shown in Ch. 5, this limitation leads to the fact that common digital PWM is often constrained to amplitude resolutions below ≈12 bit with pulse repetition frequencies that are normally used in power conversion systems. Thus, even when high-resolution digital signals are used throughout the system (e.g., 32 bit), their resolution must be substantially reduced before they can be supplied to the digital modulators, which increases the resulting quantization noise power. This results in pulse-width modulated signals whose duty cycles are quantized with the same, comparably small resolution. As this noise is present in the switch control signals, it is recreated by the power stage and hence also introduced to the analog domain, where it becomes measurable in the amplifier output waveforms. This source of noise is critical in open-loop amplifier systems, while still affecting closed-loop systems as shown in this thesis. Ch. 5 presents a digital method to shift the quantization noise energy, caused by the limited-resolution PWM, to higher frequencies. Such methods are commonly applied in the audio industry and collectively named delta-sigma modulation, or noise shaping [96].

Digital signal isolators are regularly used in power electronic applications to transmit switch control signals across an isolation barrier (e.g., for a high-side switch in a half-bridge (HB) power stage configuration). As the entire signal information is encoded (modulated) into the time instants of the transitions of the binary switch control signals, any temporal displacement of these edges (i.e., jitter [97]) leads to the addition of unwanted signal information, which often manifests as noise. This noise is then also transferred to the analog domain by the switch-mode power conversion stage, where it influences the amplifier output quality [98, 99]. As shown in this work in Ch. 4, digital signal isolators commonly introduce significant amounts of jitter. Consequently, a new gate driving method is presented, which is able to eliminate this signal jitter almost completely. Jitter of digital signal isolators is also relevant for isolated analog-to-digital converters (ADCs), where it introduces unwanted measurement noise, as shown in Sec. 6.5.

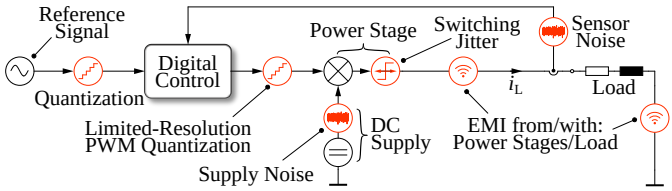

Fig. 2.4: Important amplifier noise sources can be modeled as series-connected voltage or signal sources.

Sensor noise is critical for any closed-loop feedback system and hence, care must be taken to limit the impact of this effect [100]. Consequently, voltage and current sensor systems must be designed accordingly. As reliable manufacturer noise data of commercial sensors is often unavailable, Ch. 6 presents viable approaches and measurements to create low-noise sensors that are applicable to power electronic converters. Furthermore, it is shown how oversampling of ADCs can be used, in conjunction with optimized digital filters, to reduce ADC quantization noise. The remaining sensor noise can be further reduced by employing a Kalman filter [101], which is demonstrated in Ch. 8.

Some circuit topologies of switch-mode power converters are subject to a limited power supply rejection, which results in noise from the DC supply propagating to the amplifier output with little or no attenuation [102–104]. Consequently, the spectral content of the DC supply must be carefully considered, or additional circuit components, such as low-pass filters, have to be employed. In Sec. 9.2, a compensation method is presented that is capable of rejecting unwanted signals originating from the DC supply.

Electromagnetic interference from external sources such as the power grid, or other switch-mode converters operating nearby, can also affect the quality of the converter output, either by interacting with the load or with circuits within the amplifier itself. Even if the noise is outside the amplifier's critical frequency band, intermodulation distortion (IMD) can create noise components in sensitive bandwidths [105, 106]. Electromagnetic shielding or a feedback control system can be used to attenuate such sources of noise, as shown in Sec. 7.2.

Fig. 2.4 summarizes the mentioned key sources of noise in digital switch-mode power amplifiers.

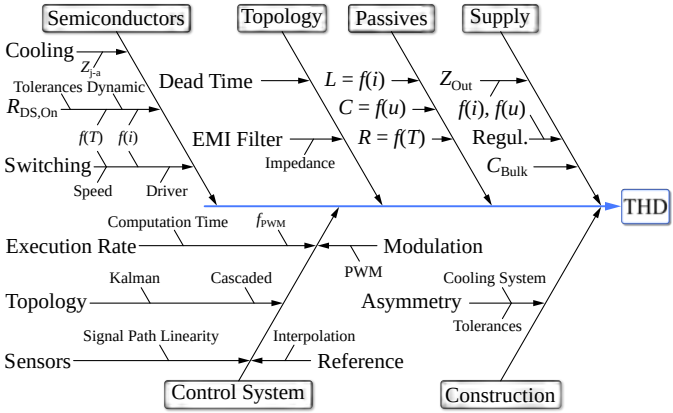

Fig. 2.5: Nonidealities of system components and parameters that affect the THD of the output quantities of digitally controlled power amplifier systems.

2.3 Distortion Sources in Power Amplifiers

Harmonic distortion arises from nonlinear elements in the paths of control or power signals within the amplifier system. **Fig. 2.5** lists prominent sources of nonlinearities in the context of switch-mode power converters with digital control systems.

The power switching stages, which are the key elements of a switch-mode amplifier that transfer the digital switch control signals to the analog domain, are a prominent source of distortion, as the recreation of the binary digital switch control signals, which carry the information with ideal rectangular waveforms, is not possible with a physical system, as the signal rise and fall times would have to approach zero. Parasitic elements of the power switching devices, such as transistor output capacitances, or undesired inductances of main current paths, limit the achievable signal transition speeds in practical settings, which thus causes distortion [13, 98, 102, 107–109]. Furthermore, the switching behavior of the power transistors is also affected by the properties of their driving circuits, which hence further influence the achievable distortion. The parasitic elements of the switching stages often give rise to high-frequency voltage or current oscillations, which can cause undesired electromagnetic interference with sensitive measurement equipment, or it renders the compliance with common norms for radiated and conducted emissions more demanding. The emergence of wide-bandgap (WBG) power

transistors with inherently low parasitic elements improves the achievable switching speeds and reduces undesired parasitic effects.

Dead time (also named interlock time), which is the time required between subsequent switching actions of power transistors in a HB arrangement to prevent shorting the DC-link (shoot-through), is a considerable source of distortion in many switch-mode power amplifiers, as it introduces a current-dependent voltage error to the switched HB voltage output [102, 107, 109]. The interaction of the HB current during the dead time interval with parasitic capacitances (e.g., the transistor output capacitances), also affects distortion nonlinearly [110]. Consequently, such phenomena are analyzed with detailed computer models in this work to take all effects into account, as done in Ch. 3, which also presents the performance of a power stage topology that considerably reduces distortion related to the dead time interval. Furthermore Sec. 9.1 presents a real-time compensation method to reduce the error introduced by dead time in a regular HB topology, which markedly improves the amplifier's linearity. The short switching times of modern WBG power transistors enable a considerable and reliable reduction of HB dead times, reducing distortion.

The on-state conduction resistances ($R_{\mathrm{DS,\,on}}$) of power MOSFETs or WBG transistors, or forward voltage drops of diodes placed in main conduction paths, are additional parasitic elements which can cause harmonic distortion [39, 102]. These circuit properties strongly depend on the temperatures of the corresponding semiconductor junctions, which can vary significantly during converter operation. Furthermore, they are influenced by the specific types of power semiconductors, their manufacturing tolerances and the employed thermal cooling solutions. Consequently, this work investigates to what extent the modulation of power transistor conduction resistances influences amplifier THD, for systems operated with and without a closed-loop control system. Ch. 3 presents the results for open-loop power converters and Sec. 7.3 investigates this source of distortion with consideration of a closed-loop feedback control system.

Digital pulse-width modulation is, apart from being a source of quantization noise, further known to introduce undesired modulation harmonics, which generally manifest at high frequencies, but low-order harmonics are also a common occurrence, especially if the ratio of the PWM carrier frequency to the fundamental frequency of the modulated signal is low [95]. This nonlinear behavior of the modulator is extensively described in literature [95, 111–113], and several methods are proposed to linearize this key element [111, 114, 115]. WBG switching transistors enable high PWM frequencies and thus, the low-order modulation harmonics can generally be neglected,

as they are dominated by other nonlinear effects such as dead time or nonideal switching waveforms. PWM can also introduce a varying time delay, which reduces the stability margins of closed-loop feedback control systems, as shown in Sec. 7.2 and [116–119].

Passive circuit elements, such as filter inductors or load resistors, can exhibit nonlinear effects, which is prominently experienced with saturating inductors (i.e., the inductance value is a (nonlinear) function of the inductor current). Similarly, many types of resistors show a significant thermal dependency of their resistance. As shown in [99, 120], and with measurements in this work, such effects can cause considerable distortion in the amplifier output waveforms and thus, these elements must be carefully designed.

If the amplifier drives a single-phase load, its input power is infamously subject to a significant ripple (which is not the case for a three-phase load). This often leads to a corresponding variation of the DC supply voltage due to a nonzero series impedance or a nonideal output voltage control of the amplifier's DC supply. Due to the limited power supply rejection, this leads to harmonic distortion in the amplifier output signals [98, 103, 104, 121, 122]. Sec. 9.2 presents a control system method to compensate variations in the DC supply voltage, which reduces distortion.

A closed-loop feedback control system provides an effective method to reject undesired signal components. However, if the sensors used to provide the required measurements are not capable of detecting erroneous signal components, or introduce them to the measurements due to nonlinearities in their signal paths (e.g., caused by nonlinear operational amplifiers), the control system cannot correct the amplifier output, or likewise, it generates faulty signals [100]. Consequently, Ch. 6 presents methods to obtain linear voltage and current sensors required for high-power amplifiers. The achievable disturbance rejection of a digital closed-loop control system depends on its execution rate, which is often proportional to the converter's switching frequency. Consequently, modern low-loss WBG power transistors enable high-frequency, high-gain controllers that provide a significant disturbance rejection capability. In order to reduce sensor noise, a Kalman filter can be employed, as mentioned in the previous section. However, its linear system model can reject harmonic signal components from the estimates and consequently, the amplifier linearity deteriorates. Ch. 8 provides details of this effect.

2.4 Summary

Important sources of noise and distortion in power output waveforms of switch-mode power amplifiers are presented. The metrics used to quantify the effects, namely the signal-to-noise ratio and the total harmonic distortion, are introduced and used consistently throughout this thesis.

Next, a detailed listing of noise sources is given. The quantization noise originating from the digital nature of the control system, or the pulse-width modulators, is a prominent contributor. Digital signal isolators, required for gate control signals, can add significant time-domain jitter to their outputs, which adds wideband noise. Additionally, sensor noise is critical when a feedback control system is employed. Due to the amplifier's limited power supply rejection, noise components of the amplifier supply voltage can affect its output waveforms, which is also the case for electromagnetic interference.

Nonlinear effects that lead to harmonic distortion are discussed similarly. The waveform of a switched HB output voltage, which replicates the digital signal in the physical domain, must show short rise and fall times, and little deviation from the ideal rectangular shape, to prevent distortion. With the regular HB power stage topology, the required interlock time between transistor switching actions is a significant source of distortion. Resistances and voltage drops of main power devices can be modulated by amplifier output signals, which constitutes a nonlinearity of the amplifier. PWM can introduce low-order modulation harmonics, which corroborates the need for high pulse repetition frequencies. Furthermore, passive elements, such as inductors or load resistors, can be nonlinear. As with noise, the amplifier's power supply rejection is limited and a varying supply voltage thus causes distortion. High-gain, closed-loop feedback controllers are desired for their disturbance rejection capability. However, they require, apart from low-noise feedback signals, also highly linear sensors.

3

Low-Distortion Switching Stage

The power stage is the core element of any switch-mode conversion system as it is responsible of converting the (digital) power transistor control signals into physical quantities such as voltages or currents. An ideal power stage replicates its control signals without adding undesired signal components like noise or harmonic distortion. However, as outlined in Sec. 2.3, different power stage characteristics, many of which are nonlinear in nature, affect the distortion of switching stage output signals. Consequently, this chapter presents extensive computer simulation models in order to analyze the distortion performance of the regular half-bridge (HB) power stage and the dual buck (DB) topology, which is specifically designed to reduce distortion related to the HB interlock time. Different types of modern WBG power semiconductors are considered as main switching elements, whereas detailed electrical and thermal models are employed to correctly identify distortion.

Only a computer simulation can be used to isolate the distortion components originating from the switching stage, as it can render all other required elements, such as the pulse-width modulators or the reference signals, ideal.

Sec. 3.1 first introduces the low-distortion DB topology and its important features. Furthermore, the circuit arrangement is extended such that its main power devices are arranged symmetrically, which increases its linearity. In **Sec. 3.2**, the computer simulation approach is presented alongside the utilized electrical and thermal semiconductor models. A method is presented that enables a significant reduction of simulation time. Finally, **Sec. 3.3** illustrates the simulation results for the analyzed circuit arrangements and WBG power semiconductors. Circuit parameters are identified to which the power stage distortion reacts especially sensitive.

3.1 The Dual Buck Topology

This section describes the DB power stage topology. It has emerged for precision amplifiers during the 1980s and was also named *opposed current converter* or *balanced current amplifier* [13, 39, 67, 83, 123–126]. Its key characteristic is the significantly reduced harmonic distortion that is otherwise caused by interlock/dead time, which, in a HB power stage configuration, is the time interval during which both transistors are turned off. This is required to prevent a short-circuit of the DC-link or high shoot-through currents between subsequent switching actions of the HB transistors. Furthermore, the basic DB implementation is also immune against HB shoot-through, which is possible in a regular HB topology by (inadvertently) turning on both power switches.

It is well-known that HB interlock/dead time is a significant source of distortion in Class-D amplifiers or DC/AC inverters (see Sec. 2.3). **Fig. 3.1** illustrates the underlying nonlinear mechanism in HB switching arrangements subject to dead time. The shape and time instants of the switched HB output voltage transitions in u_{SN} depend on the instantaneous magnitude and polarity of the HB current i_{HB}, which is proportional to the load current. Consequently, due to this load current dependent switch-node voltage modulation, indicated with the colored areas, harmonic distortion is introduced. In the illustrated example, the first switching action undergoes a hard-switched transition whereas the second one is either fully soft (i.e., zero voltage switching) or achieves partial soft-switching, which depends on the magnitude of i_{HB}, the power transistor capacitances, the DC-link voltage (due to the nonlinear transistor capacitances), as well as other parasitic circuit capacitances [127].

Fig. 3.2 (a) illustrates a regular HB power stage. By connecting the load to a split DC-link, or a second HB, a load current i_{L} such as shown in **Fig. 3.2 (c)** can be generated (note that current ripple components caused by the switching actions are neglected). As positioning systems often rely on sinusoidal actuator currents, this waveform, with a fundamental period T_{F}, is used for the following analysis, but the conversion systems can equally operate with any waveform shape. Due to the low fundamental frequencies of typically tens or hundreds of hertz, reactive currents caused by the HB filter capacitor C_{HB} are neglected.

The DB topology is also based on HB switching transistor arrangements, but enforces unidirectional HB output currents to avoid the generation of distortion. **Fig. 3.2 (b)** presents the basic DB topology. By introducing a

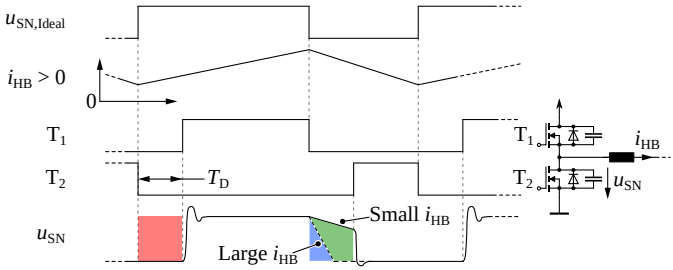

Fig. 3.1: Time-domain waveforms illustrating the cause of dead time related distortion in a HB configuration. Depending on the magnitude and direction of the HB current i_{HB}, the switch-node voltage u_{SN} deviates from the ideal shape as indicated with the colored areas. Note that the low-frequency waveform of i_{HB} is not visible during one PWM cycle as illustrated here, where the behavior for $i_{HB} > 0$ is exemplarily chosen.

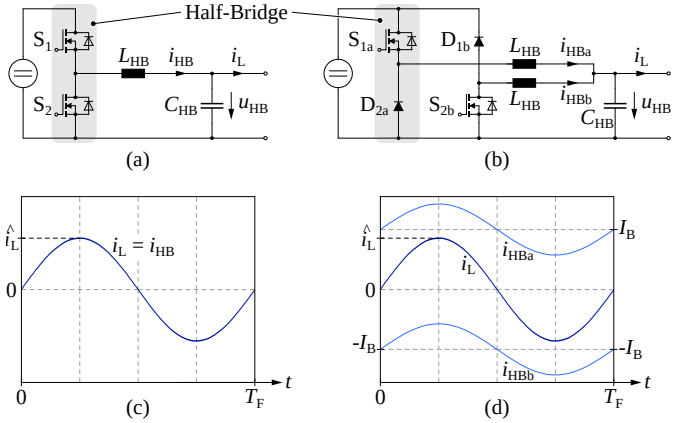

Fig. 3.2: **(a)** Regular HB topology. **(b)** DB topology. **(c)** Load current waveform of the regular HB power stage. Negative currents and voltages u_{HB} are possible by connecting the load to a split DC-link or, as a bridge-tied load, to a second HB. **(d)** DB current waveforms. The individual HB currents are unidirectional.

second HB, a circulating current can be generated between the two HBs such that the currents i_{HBa} and i_{HBb} are always unidirectional. This prevents the output voltage error of the HBs that would otherwise occur due to the changing current polarity. Due to the unidirectional HB currents, one HB transistor can be replaced by a diode as shown in **Fig. 3.2 (b)**, which renders the HB immune to shoot-through, as it is not possible to create a short-circuit of the DC-link by faulty transistor switching actions. The desired circulating current can be generated by introducing a corresponding voltage offset to the HB modulation signals [39], or by means of a closed-loop control system (see Sec. 7.2).

The HB currents i_{HBa} and i_{HBb}, whose sum is the load current i_{L}, are determined as

$$i_{\mathrm{HBa,HBb}}(t) = \frac{i_{\mathrm{L}}(t)}{2} \pm I_{\mathrm{B}}. \tag{3.1}$$

In order to preserve the unidirectional nature of the HB currents, the bias current I_{B} has to be selected with respect to the peak load current amplitude $\hat{i}_{\mathrm{L}}$ that can occur during operation:

$$I_{\mathrm{B}} \overset{!}{>} \frac{\hat{i}_{\mathrm{L}}}{2}. \tag{3.2}$$

This necessitates the prior knowledge of the load current waveform, which is usually given in amplifiers for mechatronic actuators or MRI machines. If the load current can be arbitrary, such as in audio amplifiers, a sufficient margin for the bias current has to be taken into account.

The DB topology employs two HBs that are generally controlled by PWM. By interleaving the modulator carriers, the effective switching frequency can be doubled, which reduces ripple amplitudes and relaxes output filter constraints [102, 125]. Hence, this topology is compared to the very similar regular interleaved HB topology, illustrated in **Fig. 3.3**, and in which both HB currents are identical: $i_{\mathrm{HB}}(t) = {}^{i_{\mathrm{L}}(t)}/_{2}$. Additional pairs of HBs can be interleaved similarly in both the DB and the regular interleaved topology in order to increase the load current capability and the effective switching frequency [83].

As the power transistor conduction and switching losses strongly depend on the HB currents, a comparison of the regular interleaved HB and the DB topology is required. The HB RMS currents for the two topologies, assuming a sinusoidal load current with amplitude $\hat{i}_{\mathrm{L}}$ and frequency $f_{\mathrm{F}} = {}^{1}/_{T_{\mathrm{F}}}$, are given,

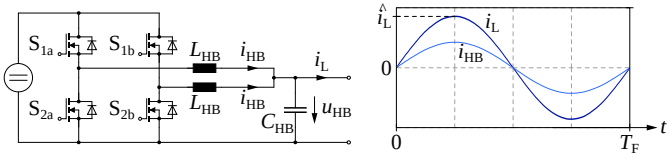

Fig. 3.3: Regular interleaved HB topology. The two HB currents are ideally identical and their sum results in the load current.

using (3.1) for the DB topology, as follows:

$$I_{\mathrm{HB,RMS,HB}} = \sqrt{\frac{1}{T_\mathrm{F}} \int_0^{T_\mathrm{F}} \left(\hat{i}_\mathrm{L}/2 \sin(2\pi f_\mathrm{F} t)\right)^2 \mathrm{d}t} = \frac{\hat{i}_\mathrm{L}\sqrt{2}}{4}, \tag{3.3}$$

$$I_{\mathrm{HB,RMS,DB}} = \sqrt{\frac{1}{T_\mathrm{F}} \int_0^{T_\mathrm{F}} \left(I_\mathrm{B} + \hat{i}_\mathrm{L}/2 \sin(2\pi f_\mathrm{F} t)\right)^2 \mathrm{d}t} = \frac{\sqrt{2(8I_\mathrm{B}^2 + \hat{i}_\mathrm{L}^2)}}{4}. \tag{3.4}$$

Assuming the minimally required I_B to preserve HB current unidirectionality as given by (3.2), the following DB HB RMS current results:

$$I_{\mathrm{HB,RMS,DB}}\left(I_\mathrm{B} = \hat{i}_\mathrm{L}/2\right) = \frac{\hat{i}_\mathrm{L}\sqrt{6}}{4}. \tag{3.5}$$

From this, it is evident that the HB RMS currents are at least by a factor $\sqrt{3} \approx 1.73$ higher in the DB topology than when the HBs are operated in the regular interleaved fashion. This affects transistor losses significantly, as it is revealed with models and measurements of the hardware demonstrator in Ch. 7. Consequently, a minimization of I_B in accordance with the expected amplitudes of i_L is desired to reduce losses. Note that I_B can also be modulated to reduce losses as shown in [39]. However, this increases distortion and is thus not further considered.

By increasing I_B, the HB currents become less modulated by the load current i_L, as the ratio of the amplitude of the sinusoidal current component to the absolute current value decreases. This renders the HB switching behavior less modulated by the load current and thus, the variation in the switching behavior is reduced (e.g., rise/fall times of the HB output voltage or transient voltage overshoots caused by parasitic inductances), which further eliminates distortion. However, the HB current RMS values increase according to (3.4). Thus, the bias current provides a degree of freedom that controls the trade-off between converter distortion and losses, as long as (3.2) is satisfied.

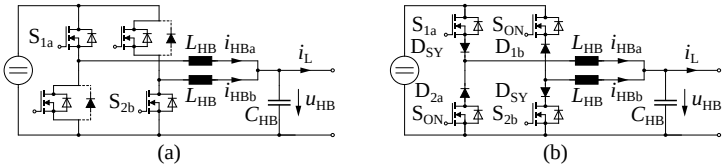

Fig. 3.4: Extended DB topologies. **(a)** Synchronously rectified DB (DB_{SR}) topology. The diodes are replaced with power switches. **(b)** Symmetrized DB (DB_{SY}) power stage. Additional power MOSFETs (permanently turned on) and diodes are connected in series to the main DB switches (cf. **Fig. 3.2 (b)**) to render the HBs symmetrical.

Due to the elevated HB currents of the DB topology, it is desirable to replace its HB diodes D_{2a} and D_{1b} (cf. **Fig. 3.2 (b)**) with power semiconductor switches with reduced conduction losses. The resulting synchronously rectified DB (DB_{SR}) topology is illustrated in **Fig. 3.4 (a)**. The power stage arrangement of this topology is now identical to the regular interleaved HB (cf. **Fig. 3.3**). It only differs by the control of the HB currents, which is identical to the DB topology and results in reduced distortion. However, this arrangement requires HB dead time (not directly affecting distortion) and is susceptible to shoot-through. In order to avoid the large voltage drops of WBG devices when operated in reverse conduction mode (which, in the case of GaN transistors, can exceed ≈5 V [128]), small free-wheeling diodes (e.g., SiC Schottky diodes) can be connected in parallel to the power transistors. They have a lower voltage drop and only conduct the HB current during the dead time interval which generally lasts less than 100 ns in fast-switching, MOSFET-based converters.

As shown in [39], the symmetry of the HB switching elements, with respect to conduction resistances or forward voltage drops, affects distortion. Thus, the DB topology from **Fig. 3.2 (b)** can be rendered symmetrical by adding the corresponding diodes and power transistors as illustrated in **Fig. 3.4 (b)**. Note that two transistors (S_{ON}) are permanently turned on as the series diodes provide the blocking capability. Similarly, the diodes D_{SY} are redundant and only added for symmetry reasons. This topology still benefits from shoot-through immunity, but the increased number of elements in the main conduction paths increase losses and complexity.

In the following, extensive computer simulations are used to evaluate the distortion performance of the presented topologies with consideration of different power semiconductors.

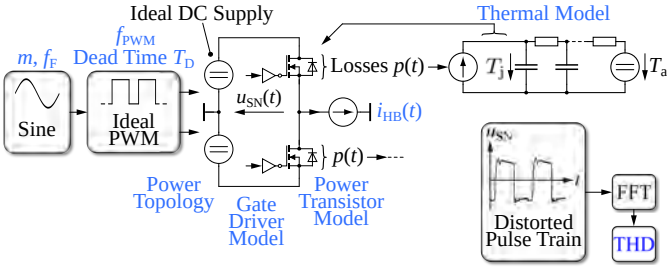

Fig. 3.5: Computer simulation setup for the switching stage distortion analysis. Different circuit topologies, switch technologies and thermal systems are modeled such that the main nonlinearities are well accounted for. All functional blocks except the switching stage are assumed ideal.

3.2 Computer Simulation Description

With the goal to identify power stage arrangements and wide-bandgap semiconductor switches suitable for low-distortion power amplifiers, computer simulation models are employed as they allow the consideration of ancillary power converter system components, such as the pulse-width modulator or the DC supply, as nearly ideal entities, which is not possible with an experimental prototype. Furthermore, all important nonlinear effects can be considered. The investigated topologies encompass the DB topology (and its symmetrical variants) as well as the regular interleaved HB power stage, as presented in the previous section.

The simulation method is illustrated in **Fig. 3.5**. The switching behavior of the power stage is recreated with detailed electrical and thermal models, whereas the gate driver circuits are also considered as they significantly influence the transistor switching behavior. In order to isolate the nonlinear effects of the switching stage, the reference signal, the PWM signal generation and the DC supply are assumed ideal. The HB current is impressed by an ideal sinusoidal current source and consequently, the distortion of the power stage is reflected in the switch-node voltage u_{SN}, whose frequency spectrum contains the low-order integer harmonics caused by the nonideal switching waveform of the HB arrangement. As low-frequency spectral components are considered in this investigation, switching ripple currents are neglected, which justifies the sinusoidal current sources.

The power transistor switch control signals are created by an idealized pulse-width modulator, i.e., it has a nearly ideal amplitude resolution (floating-

point arithmetic) and its reference is naturally sampled [95]. However, the (regular) time step of the circuit simulation software limits the accuracy of the detection of the intersection between the reference signal and the PWM carrier [129]. Despite short time steps (≈300 ps), this introduces wideband quantization noise that can potentially mask low-level harmonics in the frequency spectrum. Details of this source of noise are provided in Ch. 5. Consequently, a simple noise shaping modulator is employed to reduce quantization noise at low frequencies, which enables the reliable detection of low-level harmonics [130]. This modulation technique is also further detailed in Ch. 5, where it is also shown that it does not affect distortion. The modulator input signal has a sinusoidal waveform with fundamental frequency f_F and modulation index (i.e., amplitude relative to the PWM carrier) of $m \in [0, 1]$. The phase φ between the modulator signal and i_HB can also be adjusted.

The spectrum of the HB switch-node voltage $u_\mathrm{SN}(t)$ is calculated numerically using the FFT. In order to accurately detect harmonics with potentially low-level amplitudes, an FFT window with a sufficiently high dynamic range is used (i.e., a window with a high side lobe attenuation such as a Kaiser window with $\beta = 38$) [89]. This window selection and the requirement for a reliable detection of low-level harmonics necessitates the simulation of several fundamental output periods due to the window's spectral leakage and wide main lobe [90]. From the resulting spectrum, the THD is then calculated according to (2.4), whereas the harmonic number is limited to $k = 4$ for this analysis (i.e., the first three harmonics are considered for the distortion).

An alternative computer simulation approach, which does not require the time-consuming evaluation of several fundamental periods, is described in [131]. However, the inclusion of thermal models, which influence the transistor switching actions and conduction behavior, is not possible.

High switching speeds are desired for precision amplifier power stages in order to reduce distortion originating from the finite rise- and fall-times of the switch-node voltage u_SN. Furthermore, switching losses can be reduced in hard-switched topologies like the ones analyzed here. Therefore, fast-switching SiC and GaN transistors are evaluated in the course of this analysis [132]. WBG semiconductors are also considered for the power diodes of the DB topologies, as such devices also enable fast switching transitions due to significantly reduced reverse recovery effects and small parasitic capacitances.

The investigation considers open-loop amplifier power stages and aims at a detailed comparison of different power stage topologies and switching

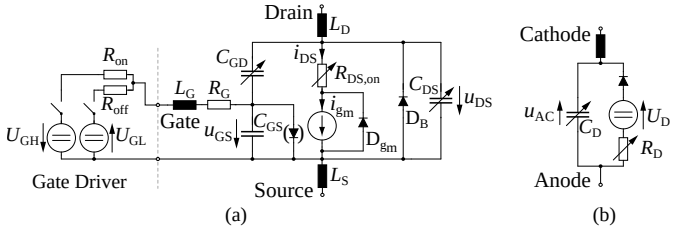

Fig. 3.6: (a) Functional electrical transistor model incorporating the gate driver circuit [133]. The $R_{DS,on}$ depends on the transistor junction temperature. Some WBG transistors show diode characteristics between their gate and source contacts. **(b)** Corresponding diode model. All parameters are derivable from datasheet specifications.

devices. The analysis presented in Sec. 7.3, which is similar to the approach used here, also considers a closed-loop feedback control system.

In the following, the detailed electrical and thermal models of the analyzed power transistors, which are required to obtain a realistic switching and conduction behavior, are presented. All model parameters are either derived from manufacturer datasheets or are based on simple FEM simulations.

3.2.1 Electrical Model for Regular Power MOSFETs and Wide-Bandgap Devices

Fig. 3.6 illustrates the equivalent circuit models used to recreate key characteristics of the switching and conduction behavior of the investigated power transistors and diodes [133]. The circuit functionality of the power transistor model is implemented with the following set of dependencies:

$$\begin{aligned} u_{\mathrm{Th}},\, g_{\mathrm{m}} &= f(T_{\mathrm{j}}), \\ R_{\mathrm{DS,on}} &= f(T_{\mathrm{j}},\, i_{\mathrm{DS}}), \\ C_{\mathrm{DS}},\, C_{\mathrm{GD}} &= f(u_{\mathrm{DS}}), \\ i_{g_{\mathrm{m}}} &= (u_{\mathrm{GS}} - u_{\mathrm{Th}}) g_{\mathrm{m}}, \text{ for } u_{\mathrm{GS}} > u_{\mathrm{Th}}, \\ U_{\mathrm{D}_{\mathrm{gm}}},\, R_{\mathrm{D}_{\mathrm{gm}}} &= f(u_{\mathrm{GS}},\, u_{\mathrm{Th}}), \end{aligned}$$

where u_{Th} is the transistor threshold voltage, g_{m} its transconductance, T_{j} the junction temperature and $R_{\mathrm{DS,on}}$ the on-state resistance which also depends on the instantaneous drain-source current i_{DS}. Similarly, the transistor's nonlinear capacitances are modeled as a function of the corresponding voltages. The transistor current conduction is recreated by the current source $i_{g_{\mathrm{m}}}$, which

is controlled by the gate-source voltage u_{GS}, the threshold voltage and the transconductance [133]. Consequently, the diode D_{gm} is required to provide a freewheeling path for the controlled current source $i_{\mathrm{g_m}}$. If the transistor is turned on ($u_{\mathrm{GS}} > u_{\mathrm{Th}}$), the forward voltage ($U_{\mathrm{D_{gm}}}$) and drift resistance ($R_{\mathrm{D_{gm}}}$) of this diode are set to zero such that it conducts the excess current of the controlled source $i_{\mathrm{g_m}}$, without affecting the rest of the circuit.

Power transistors can exhibit differing characteristics during reverse conduction. In regular power MOSFETs and SiC transistors, the body diode $\mathrm{D_B}$ is present and provides a current path for reverse conduction. Consequently, during the transistor turn-off state (i.e., $u_{\mathrm{GS}} < u_{\mathrm{Th}}$), the forward voltage and resistance of the freewheeling diode D_{gm} are set to sufficiently high values such that $\mathrm{D_B}$ is the only available conduction path. GaN devices, on the contrary, do not contain a body diode $\mathrm{D_B}$. During reverse conduction, their main conduction channel is turned on and thus, the reverse current flows through $R_{\mathrm{DS,on}}$ [128]. Consequently, during transistor turn-off, the diode D_{gm} is used to provide a current path through $R_{\mathrm{DS,on}}$. Its drift resistance $R_{\mathrm{D_{gm}}}$ is therefore set to zero. As the reverse voltage drop of GaN transistors is generally a strong function of the gate voltage u_{GS}, the forward drop $U_{\mathrm{D_{gm}}}$ is adapted accordingly by considering the instantaneous gate-source voltage. Finally, some GaN devices exhibit a diode characteristic between their gate and source contacts, which can also be incorporated in the model [134].

The gate driver significantly affects the switching behavior of power transistors and thus, as shown in **Fig. 3.6 (a)**, it is an integral part of the transistor model. Its key elements are two turn-on/off resistors R_{on}, R_{off}, and two voltage sources such that a negative gate voltage can be applied, which is often required in fast-switching HB applications to prevent the parasitic turn-on of a transistor due to currents flowing through the gate-drain capacitance that can potentially cause a sufficient voltage drop at the gate resistors to lift the gate voltage above u_{Th}.

The power diodes are modeled similarly. **Fig. 3.6 (b)** illustrates the utilized equivalent circuit and the following characteristics are embedded in the simulation software:

$$\begin{aligned} R_{\mathrm{D}}, U_{\mathrm{D}} &= f(T_{\mathrm{j}}), \\ C_{\mathrm{D}} &= f(u_{\mathrm{AC}}). \end{aligned}$$

The necessary transistor and diode properties to implement the described circuit functionality can generally be extracted from manufacturer datasheet values, which renders this model easy to use, while still covering all important characteristics. The implementation in the simulation software is also straight-

forward as the described equations and correlations can be implemented as simple algorithms [129].

Many circuit properties, like the $R_{\mathrm{DS,on}}$, that affect the linearity of the power stage, are a strong function of T_j and consequently, a thermal model is required. This allows the accurate determination of the time-domain behavior of T_j, and the depending parameters, for all investigated power semiconductors. It is presented in the following.

3.2.2 Thermal Model

Commonly used switching transistors in power electronic converters, such as silicon (carbide) MOSFETs, as well as GaN E-HEMTs, exhibit a nonlinear behavior of the on-state resistance $R_{\mathrm{DS,on}}$ as a function of the junction temperature [128,135]. Naturally, the instantaneous transistor losses and hence, T_j and $R_{\mathrm{DS,on}}$, are a function of the converter operating point (e.g., its output current or switching frequency), which causes a corresponding variation (modulation) of the main conduction path resistances and hence, harmonic distortion. Even as modern WBG semiconductors show a reduced temperature dependency of the $R_{\mathrm{DS,on}}$ compared to their silicon counterparts [128], this nonlinear effect has to be considered for highly linear amplifiers.

Thus, the thermal system is comprehensively modeled and takes the cooling methods of different power semiconductor packages into account. **Fig. 3.7** illustrates the considered heat dissipation methods that are commonly used in power electronic applications. Some PCB-mounted devices require a cooling path through the PCB itself using thermal vias (see **Fig. 3.7 (a)** and **(b)**) [136]. On the other hand, as **Fig. 3.7 (c)** illustrates, some SMD devices offer a path of significantly lower thermal resistance when cooled directly at the case [128]. Finally, through-hole devices are regularly mounted onto a heat sink with an electrically isolating pad, as **Fig. 3.7 (d)** shows. The characteristics of the power device's thermal system between junction and case are described by the (complex) impedance Z_jc of the thermal equivalent circuit model. Similarly, the behavior of the external cooling components between the case and the ambient are summarized by Z_ext.

The thermal model, which is implemented for each switching device in the simulation software, is illustrated in **Fig. 3.8 (a)**. It consists of the two thermal impedances Z_jc and Z_ext which also cover the transient thermal behavior by incorporating important thermal capacitances. From manufacturer datasheets, a step response plot of Z_jc is usually available. Thus, by using system identification techniques, the corresponding transfer function model of Z_jc can

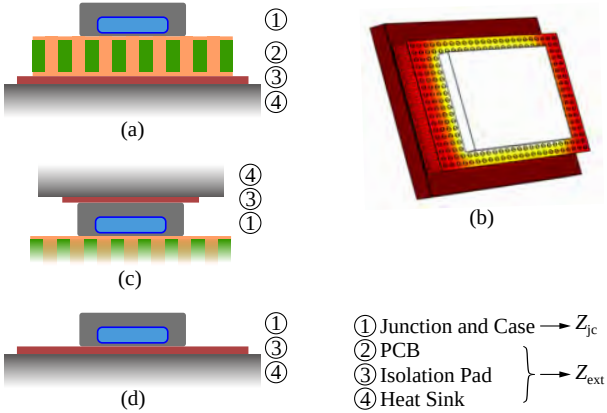

Fig. 3.7: Different power device cooling methods and thermal modeling process. **(a)**, **(b)** Surface-mounted device cooled through the PCB. **(c)** SMD cooled through its case. **(d)** Through-hole device mounted on a heat sink (PCB not shown).

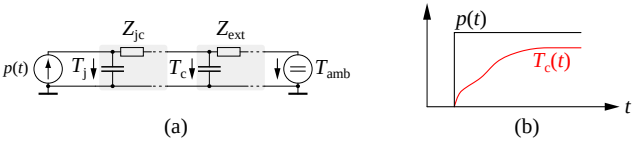

Fig. 3.8: (a) Thermal equivalent circuit model of the power semiconductors and their cooling arrangement. **(b)** Thermal step response to determine key thermal characteristics.

be identified and directly implemented in the simulation software [129, 137]. However, for the thermal impedance Z_{ext} from case to ambient, such data is not available, as it strongly depends on the employed cooling approach.

Consequently, Z_{ext} is identified from temperature step responses that are obtained with thermal FEM simulations which incorporate important thermal properties of the external cooling components (see **Fig. 3.7 (b)**). As **Fig. 3.8 (b)** illustrates, a power loss step is applied in the FEM simulation to the case of the power device and the subsequent time-domain behavior of the case temperature T_c is recorded, from which Z_{ext} can be identified using system identification methods, like it is described for Z_{jc} above. This approach is used to obtain the thermal models for the three considered cooling solutions as illustrated in **Fig. 3.7**.

In order to avoid harmonic distortion due to circuit asymmetry (i.e., unevenly heated switching devices) and temperature-dependent transistor on-state resistances, it is important that the temperature differences between the devices vary as little as possible. Consequently, the thermal impedances between the devices and the ambient must be minimized. This can be achieved by using the appropriate cooling solution for each device as illustrated in **Fig. 3.7**. For this analysis, the heat sink is modeled as an ideally thermally conductive plate being held at a constant temperature T_{amb}, which is justified as the important thermal properties are covered by Z_{jc} and Z_{ext}.

The thermal loss of each power device is the sum of its conduction and switching losses. The knowledge of each device's momentary resistance in the simulation model allows for a simple evaluation of the corresponding conduction losses. In order to assess the switching losses, which strongly depend on the switched current and voltage, as well as the gate driver configuration, data from manufacturer datasheets, publications, or estimates from SPICE simulation models are used [138–140]. In each simulation time step, the momentary losses of the devices are provided to the corresponding thermal models and the resulting junction temperatures are used to vary the device parameters accordingly. This enables a realistic simulation of the time-varying $R_{\mathrm{DS,on}}$, which allows the investigation and comparison of the resulting distortion.

Simulation Time Reduction

In the discussed mechatronic applications, fundamental amplifier output frequencies f_{F} are typically in the range of DC to several hundred hertz. As mentioned above (see Sec. 3.2), the simulation of multiple (typically ≈15) fundamental periods is necessary to correctly obtain the spectrum of the power stage output voltage, such that the THD can be reliably calculated. However, the inclusion of a thermal model, which typically contains comparably large thermal capacitances, and hence, slow dynamics, requires the simulation of more fundamental periods such that it reaches its steady-state. As a small simulation time step (≈300 ps) has to be chosen to correctly represent the fast switching transitions, and to reduce quantization noise of the PWM, the resulting simulation data becomes intolerably large and the simulations require significant amounts of time (in the order of days).

Consequently, a method is presented that allows a faster simulation of the thermal system. Simulations show that distortion caused by electrical effects (e.g., switching overshoot, rise/fall times), and distortion components caused by the thermal behavior (e.g., time-varying $R_{\mathrm{DS,on}}$), can be decoupled.

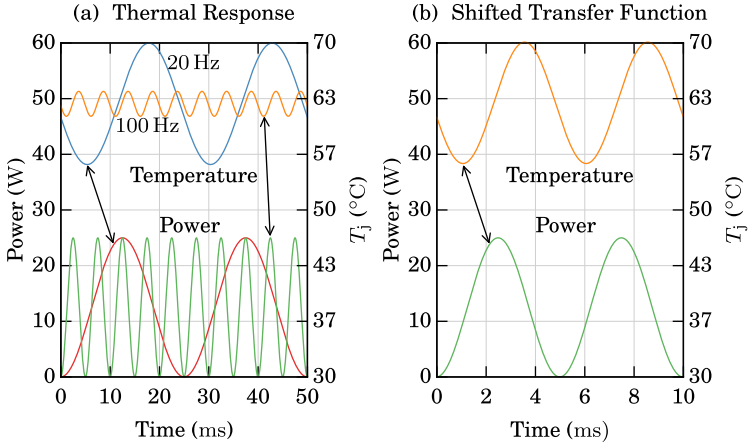

Fig. 3.9: Behavior of the thermal system of a power semiconductor at different fundamental frequencies. **(a)** Device loss power with f_F of 20 Hz and 100 Hz, and the corresponding variation in junction temperature T_j. **(b)** With the frequency-shifted thermal transfer function, the response of T_j at 100 Hz is identical to the behavior at 20 Hz (cf. (a)).

If thermal effects are not considered (i.e., T_j is considered constant), the resulting distortion components are independent of the fundamental frequency f_F, as long as $f_{PWM} >> f_F$, such that the low-order integer harmonics introduced by the PWM remain negligible [95]. Thus, the number of simulation steps can be reduced by increasing f_F, while still correctly accounting for the distortion caused by the electrical switching behavior. However, the thermal transfer functions must be adapted for the higher fundamental frequency such that the thermal behavior of the system is identical as if a smaller f_F was used. **Fig. 3.9 (a)** illustrates this exemplarily. It shows the time-domain waveform of a power device's T_j for two fundamental frequencies of 20 Hz and 100 Hz as a consequence of the indicated power losses of the device. A thermal model as described in Sec. 3.2.2 is used and the simulation has reached its steady. As expected, the variation of T_j is larger at a smaller fundamental period, as the thermal capacitances provide higher impedances. The objective is to render the waveform of T_j at the elevated loss power fundamental frequency of 100 Hz identical to the one at 20 Hz with respect to the waveform of the loss power. This is achieved as follows: It is assumed that the transfer function of

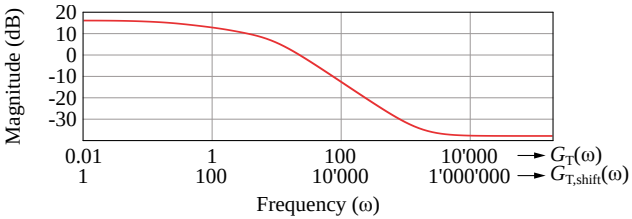

Fig. 3.10: Magnitude plot of an exemplary thermal transfer function and the effect of the frequency shift. $f_{HF} = 100\, f_F$

the thermal system, G_T, is of the following form:

$$G_T(s) = \frac{a_0 + a_1 s + \cdots + a_n s^n}{b_0 + b_1 s + \cdots + b_n s^n}. \tag{3.6}$$

This transfer function can be shifted in the frequency domain by modifying the terms containing the complex frequency parameter s:

$$G_{T,\,shift}(s) = \frac{a_0 + (f_F/f_{HF})a_1 s + \cdots + (f_F/f_{HF})^n a_n s^n}{b_0 + (f_F/f_{HF})b_1 s + \cdots + (f_F/f_{HF})^n b_n s^n}, \tag{3.7}$$

where f_F is the desired low fundamental frequency, and f_{HF} is the elevated simulation frequency. **Fig. 3.10** exemplarily illustrates such a frequency-shifted transfer function. The usage of the thermal transfer function $G_{T,\,shift}$ results in an identical behavior of T_j when the simulation is performed with the elevated fundamental amplifier output signal frequency f_{HF}, as when the simulation is done using G_T and with f_F. This is shown in **Fig. 3.9 (b)**. Despite the fundamental frequency of $f_{HF} = 100\,\text{Hz}$, the variation of T_j is identical with respect to the loss waveform when compared to the simulation at $f_F = 20\,\text{Hz}$. The distortion components of the output waveform, caused by the thermal variation of the $R_{DS,\,on}$ and other circuit parameters, can now be correctly accounted for, despite the elevated simulation frequency f_{HF}. Note that this approach is only valid as long as the distortion components caused by the circuit's electrical behavior (e.g., switching transition shape, ringing etc.) are not affected by the increased fundamental frequency, which is the case for $f_{HF} <\approx 5\,\text{kHz}$, as experimentally determined with the considered PWM frequencies. The utilized fundamental frequencies in the simulations are indicated with the results below, but are generally selected at $f_{HF} = 2\,\text{kHz}$. This reduces simulation data and duration.

3.3 Results

Following the introduction of the simulation approach and the description of the electrical and thermal models, the results of the simulations are presented. To identify components that critically affect THD, sensitivity analyses are performed, which reveal how strongly the output THD reacts to variations of different system parameters. The sensitivity is defined as the partial derivative of the THD with respect to a single parameter x (e.g., dead time or type of transistor), at a given nominal operating point X_0:

$$S(x)\big|_{X_0} = \left.\frac{\partial\,\mathrm{THD}}{\partial x}\right|_{X_0}. \tag{3.8}$$

In order to determine S, all model parameters are kept at their nominal values, whereas the parameter being analyzed (i.e., x) is swept over a certain range and the resulting THD is plotted against it.

Tab. 3.1 lists important properties of the investigated transistors and diodes, together with their appropriate cooling solutions. Switches with different characteristics (i.e., capacitances or thermal properties) are selected in order to cover a broad field of commonly used WBG power semiconductors. The device $\mathrm{GaN}_{\mathrm{T1}}$ is modeled after an E-HEMT from *GaN Systems*, while $\mathrm{GaN}_{\mathrm{T2}}$ is a gate injection transistor with a diode characteristic at its gate [138, 141], and $\mathrm{GaN}_{\mathrm{T3}}$ is a device from *EPC*. The SiC devices are closely related to offerings from *Wolfspeed*.

The regular interleaved HB topology (see **Fig. 3.3**) consists of two identical HBs, each conducting (ideally) the same current. Furthermore, the output filter of interleaved power stages simply creates the arithmetic mean of the individual switch-node voltages of each HB, which does not affect THD. Consequently, an analysis of both HBs is redundant and only a single HB is considered, which also reduces simulation complexity. For the DB topologies, it is also sufficient to simulate only one HB, as both operate symmetrically. The sinusoidal current source (cf. **Fig. 3.5**) then simply injects the unipolar DB current waveform. The utilized load current amplitude $\hat{i}_{\mathrm{L}}$ is given with the simulation results below. For the DB topologies, (3.1) is used to determine the resulting HB currents with the indicated bias currents I_{B}. In the case of the regular HB topology, the HB current is equal to the load current i_{L}, as only one HB is considered. Thus, it is necessary to regard the two topologies at their corresponding operating points with doubled current amplitudes in order to compare the results.

The harmonic distortion of the switch-node voltage u_{SN} is calculated as described in Sec. 2.1.1 (the first three harmonics are considered). The

Tab. 3.1: Different WBG transistors and diodes used in the simulations. U_{BD} is the breakdown voltage.

Transistor Material	Abbrev.	U_{BD}	$R_{DS,on}$ 25 °C	$I_{DS,Max}$ 25°C	Cooling (cf. **Fig. 3.7**)
GaN	GaN_{T1}	650 V	55 mΩ	30 A	PCB (a)
GaN	GaN_{T2}	600 V	56 mΩ	20 A	PCB (a)
GaN	GaN_{T3}	200 V	25 mΩ	22 A	Top (c)
SiC	SiC_{T1}	1200 V	80 mΩ	36 A	Heat sink (d)
SiC	SiC_{T2}	1200 V	25 mΩ	90 A	Heat sink (d)
Diode Material	Abbrev.	U_{BD}	Q_j (3-300 V)	I_{Max} 125 °C	Cooling (cf. **Fig. 3.7**)
SiC	SiC_{D1}	650 V	17 nC	10 A	PCB (a)
SiC	SiC_{D2}	650 V	35 nC	20 A	Heat sink (d)
SiC	SiC_{D3}	1200 V	37 nC	15 A	Heat sink (d)

simulation time step T_{step} is chosen such that the quantization noise does not affect the outcome of the simulation (i.e., $T_{step} < 300\,ps$), and the ambient temperature T_{amb} is set to 40 °C.

Tab. 3.1 lists the abbreviations of the power devices and Sec. 3.1 presents the different DB topology designations. This analysis is a comparison of different power devices and topologies and the indicated THD figures cannot be related to realistically achievable values, as important system components like the DC supply or the pulse-width modulator are simulated as ideal entities in order to isolate the distortion effects caused by the switching stage.

3.3.1 Gate Driver Parameter Selection

As the gate driver directly influences the transistor switching behavior, sensitivity analyses of its parameters (i.e., U_{GH}, U_{GL}, R_{on}, R_{off}, as shown in Sec. 3.2.1) are performed. **Fig. 3.11** shows the results for the GaN_{T1} transistor in both the regular HB and DB topology.

The HB topology shows higher sensitivities to the gate driver parameters, whereas R_{on} is especially of significance. This corroborates the necessity of fast switching transitions, achievable with small R_{on} in the HB topology to achieve low distortion. Consequently, in all simulations the gate driver

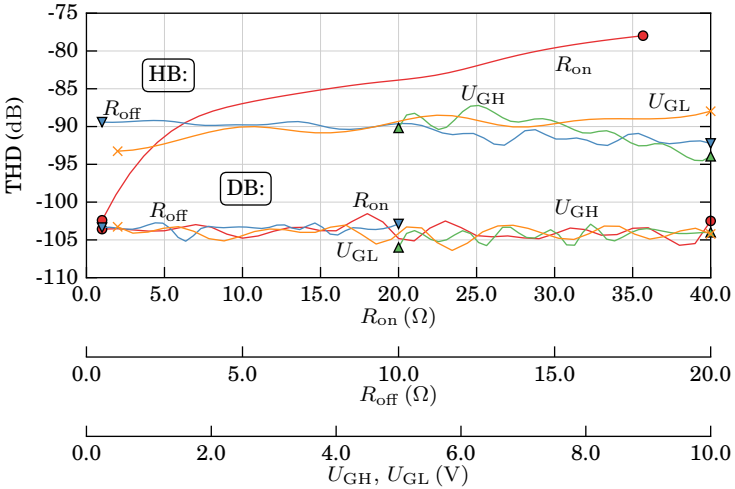

Fig. 3.11: Sensitivities to the gate driver parameters for the DB and the HB topology with GaN_{T1} and SiC_{D1} as switch and diode. $f_{\text{PWM}} = 100\,\text{kHz}$, $f_{\text{F}} = 50\,\text{Hz}$, $f_{\text{HF}} = 2\,\text{kHz}$, $m = 0.75$, $\hat{i}_{\text{L}} = 3\,\text{A}$, $\varphi = 0°$, $T_{\text{D}} = 15\,\text{ns}$, $I_{\text{B}} = 6.5\,\text{A}$, $U_{\text{DC}} = 400\,\text{V}$. The nominal parameters are: $R_{\text{on,nom}} = 5\,\Omega$, $R_{\text{off,nom}} = 2\,\Omega$, $U_{\text{GH,nom}} = U_{\text{GL,nom}} = 7\,\text{V}$.

parameters are chosen with the help of such a sensitivity analysis in order to find a configuration which is both low in distortion and stable in all operating points (i.e., no erroneous switching actions at fast switch-node voltage transients with high values of $\mathrm{d}u_{\mathrm{SN}}/\mathrm{d}t$).

3.3.2 Topology Comparison

In **Fig. 3.12**, the different power stage topologies are analyzed with sweeps of the modulation index m and the output current i_{L}, using the $\mathrm{GaN}_{\mathrm{T1}}$ transistor. Additionally, the results from an ideal HB topology (i.e., ideal switches, no parasitic elements and dead time $T_{\mathrm{D}} = 0$) are plotted to illustrate the simulation limit, caused by the nonzero simulation time step of $T_{\mathrm{step}} = 233\,\mathrm{ps}$. Interestingly, if the idealized HB is operated with dead time (e.g., 15 ns), its THD performance is worse than that of its realistically modeled counterpart (which operates with the same dead time). This is due to the output capacitance of the transistors which can improve the distortion in topologies that require dead time, as shown in [110] and also further below.

This analysis reveals that the DB topologies are subject to less output distortion than the HB topology, even when simulated with a low value for the dead time of $T_{\mathrm{D}} = 15\,\mathrm{ns}$. A further reduction of dead time, which would reduce the THD of the HB topology, is considered difficult in a real system in order to safely prevent the erroneous simultaneous turn-on of both HB transistors, even with fast-switching WBG transistors. This is further detailed in Sec. 7.6.1.

For the DB topologies that employ a diode in their main power path (i.e., the DB and $\mathrm{DB}_{\mathrm{SY}}$ topologies, as shown in **Fig. 3.2 (b)** and **Fig. 3.4 (b)**), the THD is improved when the diode $\mathrm{SiC}_{\mathrm{D1}}$ is used instead of $\mathrm{SiC}_{\mathrm{D2}}$ or $\mathrm{SiC}_{\mathrm{D3}}$, as this diode has a smaller junction capacitance (but higher conduction losses compared to the other two). This allows faster switching transitions at the cost of higher temperature swings, which nonetheless results in a lower THD in the considered operating ranges.

The synchronously rectified DB topology ($\mathrm{DB}_{\mathrm{SR}}$, see **Fig. 3.4 (a)**) requires dead time, as it is topologically identical to the regular interleaved HB topology. Simulations show that there is little sensitivity of the THD to this dead time. This is expected due to the use of SiC freewheeling diodes in parallel to the main power transistors which limit the forward voltage drop during the short dead time intervals. The presented sensitivity sweep in **Fig. 3.12** indicates that this topology achieves the best distortion figures. This is due to its low conduction losses, as there are no diodes in the main power paths, and its

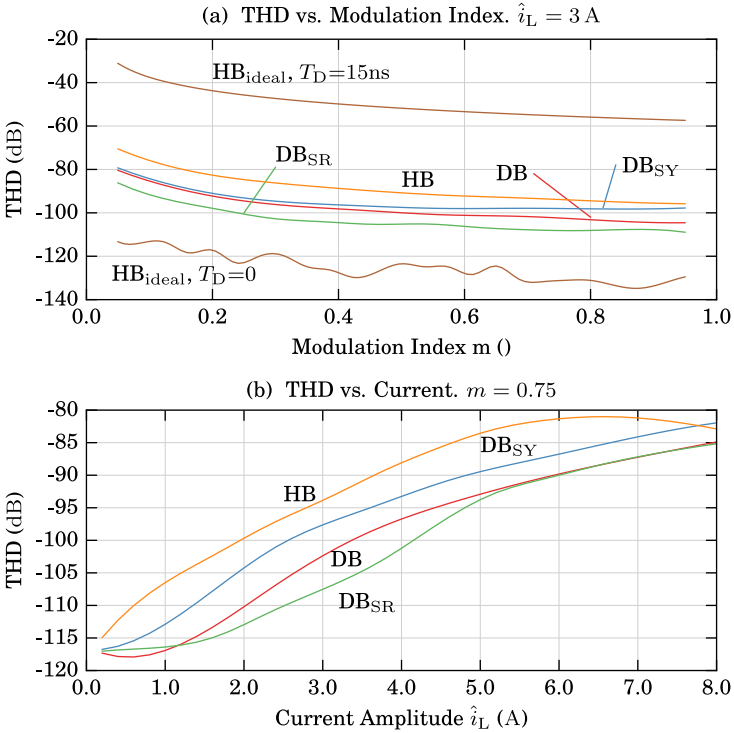

Fig. 3.12: Comparison of different circuit topologies with the GaN_{T1} switch and the SiC_{D1} diode. THD is shown as a function of: **(a)** The modulation index m and **(b)** the output current amplitude i_L. $f_{PWM} = 100$ kHz, $f_F = 50$ Hz, $f_{HF} = 2$ kHz, $m_{nom} = 0.75$, $\hat{i}_{L,nom} = 3$ A, $\varphi = 0°$, $T_{D,HB} = 15$ ns, $T_{D,DB_{SR}} = 15$ ns, $I_B = \hat{i}_L/2 + 5$ A, $U_{DC} = 400$ V.

inherently high symmetry. Although the DB_{SY} topology is also symmetrical, it performs slightly worse than the regular DB topology. This is caused by the increased number of power semiconductors in its main conduction paths, which undergo distortion-inducing thermal variations of their resistances and voltage drops.

3.3.3 Power Transistor Comparison

The THD performance of the different considered power transistors is illustrated with the synchronously rectified DB (DB_{SR}) topology in **Fig. 3.13**. As a comparison, the HB topology with the GaN_{T1} switch is also illustrated.

It shows that power transistors which have a low thermal impedance to the ambient, that generally correlates with the semiconductor die area and the $R_{DS,on}$, create less distortion, as their junction temperature variation is reduced. Hence, the parameters that affect the nonlinearity (e.g., the $R_{DS,on}$) remain more constant during a fundamental output period. However, this effect can be offset by higher achievable switching speeds, which is featured by low-capacitance switches that commonly show elevated conduction resistances due to the smaller semiconductor die areas (and thus, higher thermal impedances). Thus, due to the interaction of these nonlinear effects, a detailed thermal and electrical simulation must be performed in order to determine the best achievable distortion for a given amplifier configuration and operating point.

The analysis also reveals the limited performance of the GaN_{T2} transistor, which is mainly caused by its gate configuration that features a diode behavior between the gate and source, which affects the switching speed.

3.3.4 Sensitivity to the Dead Time

It is well-known that the dead time T_D, required in the regular HB topology, has a significant influence on the THD. **Fig. 3.14** illustrates this for the investigated power transistors. It is noteworthy that the THD often shows a local minimum at certain values of T_D. This is due to the fact that in topologies with dead time, the transistor output capacitance can reduce distortion as it renders the voltage transitions within a switching cycle more symmetrical (i.e., the rising and falling switch-node transitions). However, this strongly depends on the operating point and the (parasitic) capacitances, as corroborated by this analysis and [110]. The position and extent of this local distortion minimum depends on the output capacitance of the switch (and potentially other

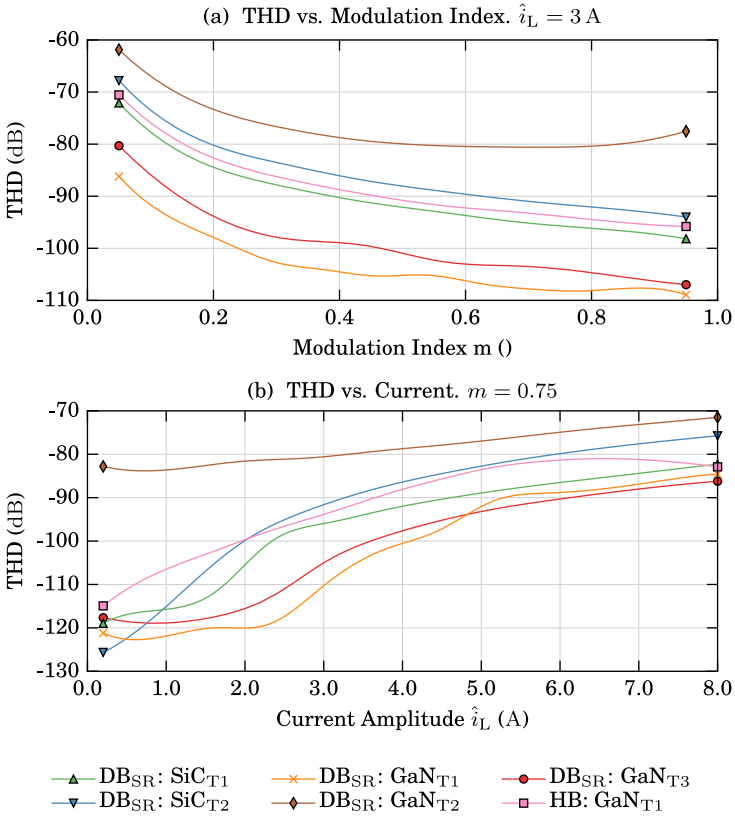

Fig. 3.13: Comparison of different switch technologies. THD as a function of: **(a)** The modulation index m and **(b)** the output current amplitude i_L. $f_{PWM} = 100$ kHz, $f_F = 50$ Hz, $f_{HF} = 2$ kHz, $m_{nom} = 0.75$, $\hat{i}_{L,nom} = 3$ A, $\varphi = 0°$, $T_{D,HB} = 15$ ns, $T_{D,DB_{SR}} = 20$ ns, $I_B = \hat{i}_L/2 + 5$ A, $U_{DC} = 400$ V (150 V with GaN$_{T3}$).

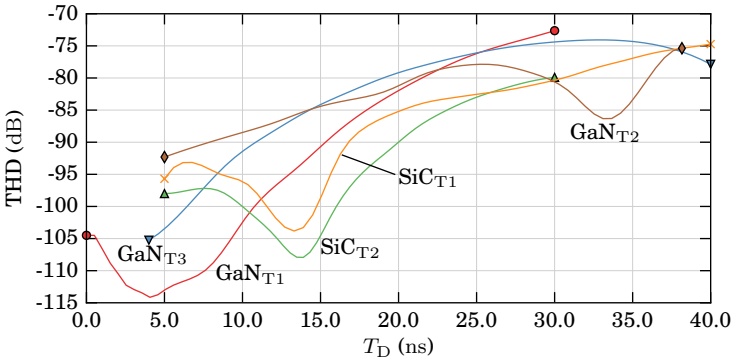

Fig. 3.14: Influence of the dead time T_D with different switches in the HB topology. $f_{PWM} = 100\,\text{kHz}$, $f_F = 50\,\text{Hz}$, $f_{HF} = 2\,\text{kHz}$, $m = 0.75$, $\hat{i}_L = 3\,\text{A}$, $\varphi = 0°$, $U_{DC} = 400\,\text{V}$ (150 V with GaN_{T3}).

parasitic capacitances, e.g., caused by PCB tracks), as well as the gate driver configuration, as it also influences the shape of the switching transitions.

3.3.5 Sensitivity to the Dual Buck Bias Current

Similar than the dead time in the HB topology, the bias current I_B of the DB topology influences the THD as shown in **Fig. 3.15**. In the DB and DB_{SY} topologies, the THD initially decreases with increasing I_B, which is expected since a higher bias current leads to faster and less modulated switching transitions. However, at a certain magnitude of I_B, the thermal variation of the devices leads to an undesired deterioration of the THD. Consequently, it is important to select the bias current in conjunction with the utilized power switches to minimize distortion.

The synchronously rectified DB topologies (DB_{SR}) that employ GaN transistors are less sensitive to the bias current than the configurations which utilize SiC devices. This is attributed to their reduced parasitic switch capacitances and low thermal impedances.

3.3.6 Sensitivity to the Switching Frequency

The influence of the switching frequency f_{PWM} on the open-loop modulated power stages is illustrated in **Fig. 3.16** for the HB and DB topologies. At higher switching frequencies, the relative duration of the switch-node voltage

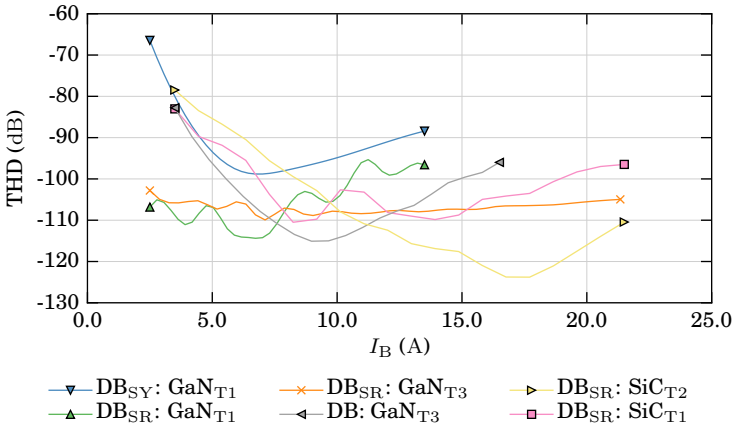

Fig. 3.15: Influence of the bias current I_B with different switches in the analyzed DB topologies. $f_{PWM} = 100\,\text{kHz}$, $f_F = 50\,\text{Hz}$, $f_{HF} = 2\,\text{kHz}$, $m = 0.75$, $\hat{i}_L = 3\,\text{A}$, $\varphi = 0°$, $T_{D,DB_{SR}} = 15\,\text{ns}$.

transition time to the switching period increases, which affects distortion. Furthermore, the transistor switching losses are elevated, which increases the average junction temperatures. Thus, the average conduction resistances shift to points on the thermal $R_{DS,on}$ curves, which are often nearly quadratic, with steeper slopes. This leads to a stronger modulation of the on-state resistances.

However, a low switching frequency might not be desired as the amplifier's output bandwidth strongly depends on f_{PWM}, as shown in [125] and Sec. 7.2. A possible solution for this trade-off between distortion and bandwidth can be obtained by operating several power stages with interleaved PWM signals, which results in a higher effective switching frequency. Another possibility are multi-cell systems which are also based on an interleaved operation [125].

3.3.7 Summary

The presented sensitivity sweeps provide valuable insights into the behavior of the investigated power switches and circuit topologies. In order to summarize the important results concisely, the averaged THD values of selected simulations are evaluated for the parameter ranges listed in **Tab. 3.2** and given in **Tab. 3.3** below.

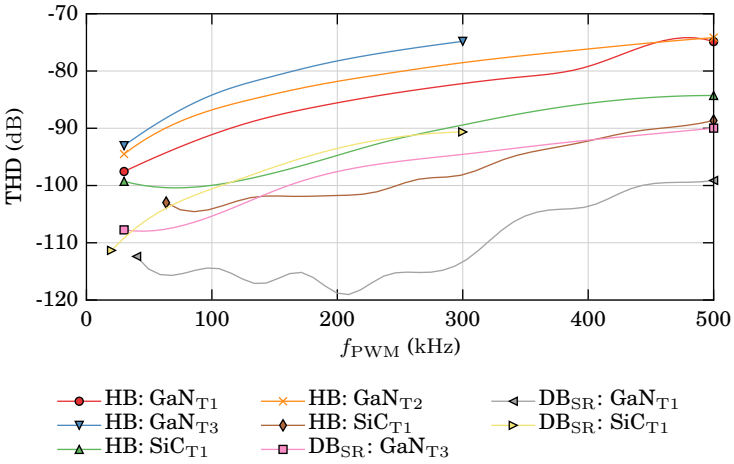

Fig. 3.16: Influence of the switching frequency f_{PWM} with different switches in different HB and DB topologies. $f_F = 50\,Hz$, $f_{HF} = 2\,kHz$, $m = 0.75$, $\hat{i}_L = 3\,A$, $\varphi = 0°$, $T_{D,HB} = 15\,ns$.

Generally, it can be concluded that the DB topologies effectively eliminate dead time related distortion, which results in a highly linear behavior of these topologies. Due to the high losses of the symmetrical DB topology (DB_{SY}), and the fact that the synchronously rectified DB topology (DB_{SR}) performs better, its usage cannot be recommended. Furthermore, the regular DB topology is less linear than the DB_{SR} topology. This is attributed to the fact that the HB of the DB topology is not symmetrical, in contrast to the construction of the DB_{SR}.

However, the DB_{SR} configuration is not robust against HB short-circuits, which can be a requirement in certain applications. If the shoot-through immunity is not critical, the regular HB topology also offers a viable alternative to the DB variations, as the occurring RMS currents are significantly reduced and hence, the power conversion efficiency is substantially better. This is especially important if high PWM switching frequencies, that inherently increase the switching losses, are required to obtain a high-gain closed-loop control system (see Sec. 7.2).

All simulations presented in this chapter are obtained with a single HB leg. However, the DB topology requires two HBs and thus, in order to fairly compare the simulation results of the DB and HB topologies, the distortion

values of the HB topology that are obtained at half the load current have to be used (see the beginning of this section). This boosts the performance of the investigated HB topology to the level of the DB arrangements. For the HB topology, it is desirable to reduce dead time as much as possible, and the gate driver should also be constructed such that it achieves fast power device switching actions, while still being robust against erroneous transistor turn-on/off behavior, as the simulations in this chapter have revealed.

For open-loop amplifier applications, there exists a trade-off between switching speed (which correlates with the parasitic switch capacitances) and thermal performance. Generally, small parasitic transistor capacitances are desired to achieve fast switching speeds that result in reduced losses and distortion due to the good recreation of the switch control signals in the physical domain. This, however, often increases the device's thermal impedance to the ambient (due to smaller semiconductor die areas) and the conduction losses and hence, its junction temperature variation increases, which introduces thermal-related distortion. Due to the nonlinear nature of these effects and interactions, a detailed simulation such as the one performed in this work is often the only method to reliably evaluate the required switch technology for the intended application.

Based on the insights gained with these sensitivity analyses, the hardware demonstrator, presented in Ch. 7, is constructed such that it supports both the synchronously rectified DB and the regular interleaved HB topology. This allows a realistic comparison of the two power stage layouts. GaN power transistors (GaN_{T1}) are used as they achieve comparably low THD values in the presented simulations. Furthermore, their packages enable low-parasitic HBs characterized by fast switching transitions and little undesired behavior such as voltage overshoots or excessive ringing.

Tab. 3.2: Parameters ranges in which the THD sweeps are evaluated. Results are shown in **Tab. 3.3** below.

Parameter		Considered Range
Modulation Index	m	$0.05 \cdots 0.95$
Output Current Amplitude	$\hat{i}_\mathrm{L}$	$1\,\mathrm{A} \cdots 3\,\mathrm{A}$
Switching Frequency	f_PWM	$50\,\mathrm{kHz} \cdots 500\,\mathrm{kHz}$
Dead Time	T_D	$5\,\mathrm{ns} \cdots 40\,\mathrm{ns}$
Bias Current	I_B	$\hat{i}_\mathrm{L}/2 + (1\,\mathrm{A} \cdots 15\,\mathrm{A})$
Output Phase Angle	φ	$-90° \cdots 90°$
DC-Link Voltage	U_DC	$0.3 \cdots 1.5 \cdot U_\mathrm{DC,nom}$

Tab. 3.3: Averaged THD values (unit: dB) from the sweep ranges given in **Tab. 3.2**. The rightmost column contains the averages of the other columns. The nominal values used for the parameters except the swept parameters are: $m = 0.75$, $\hat{i}_\mathrm{L} = 3\,\mathrm{A}$, $f_\mathrm{PWM} = 100\,\mathrm{kHz}$, $T_\mathrm{D} = 15\,\mathrm{ns}$, $I_\mathrm{B} = \hat{i}_\mathrm{L}/2 + 5\,\mathrm{A}$, $\varphi = 0°$, $U_\mathrm{DC} = 400\,\mathrm{V}$ or $150\,\mathrm{V}$ (for $\mathrm{GaN_{T3}}$).

		Swept Parameter							
Topology	Switch	m	i_L	f_PWM	T_D	I_B	φ	U_DC	Total
$\mathrm{DB_{SR}}$	$\mathrm{GaN_{T1}}$	−103	−111	−110	n/a	−104	−113	−105	−107.7
	$\mathrm{GaN_{T2}}$	−76	−82	−79	n/a	−98	−94	−91	−86.7
	$\mathrm{GaN_{T3}}$	−99	−113	−103	n/a	−107	−109	−110	−106.8
	$\mathrm{SiC_{T1}}$	−90	−106	−90	n/a	−102	−96	−96	−96.7
	$\mathrm{SiC_{T2}}$	−87	−99	−87	n/a	−103	−92	−92	−93.3
$\mathrm{DB_{SY}}$	$\mathrm{GaN_{T1}}$	−94	−102	−93	n/a	−89	−102	−97	−96.2
DB	$\mathrm{GaN_{T1}}$, $\mathrm{SiC_{D1}}$	−96	−110	−96	n/a	−99	−103	−103	−101.2
	$\mathrm{GaN_{T3}}$, $\mathrm{SiC_{D1}}$	−100	−112	−99	n/a	−104	−107	−106	−104.7
HB	$\mathrm{GaN_{T1}}$	−88	−100	−84	−89	n/a	−94	−93	−91.3
	$\mathrm{GaN_{T3}}$	−78	−92	−82	−92	n/a	−90	−84	−86.3
	$\mathrm{SiC_{T1}}$	−95	−100	−92	−86	n/a	−101	−102	−96.0
	$\mathrm{SiC_{T2}}$	−77	−85	−97	−91	n/a	−91	−91	−88.7

4

Low-Jitter Gate Driver

Transistor gate drivers are an integral part of the power stage and fundamentally define the switching waveforms. As the gate control signals contain the entire information of the desired switching stage output signal that is to be transferred by the power stage to the analog domain, care must be taken to preserve the integrity of these signals. In power electronics, the gate control signals often have to be transported across an isolation barrier as the control entity's reference potential is different, which is, e.g., the case for the high-side switch in a half-bridge (HB) configuration. Digital signal isolators, or methods based on high-impedance signal paths, are commonly used to achieve this. However, as shown in this chapter, they alter the information of the transmitted gate control signals unfavorably through time-varying propagation delays (jitter), which adds noise to the gate control signal that is then also replicated by the power stage.

Sec. 4.1 further explains signal isolator jitter and its ramifications in the context of power electronic converters. Sec. 4.1.1 also illustrates jitter measurements of different types of digital signal isolators. **Sec. 4.2** presents a novel isolated gate driver circuit that is capable of eliminating jitter from any isolator, while also being robust against fast common-mode (CM) transients across its isolation barrier, which is a necessity for reliably operating fast-switching WBG transistors. Measurements on a small-scale prototype verify the functionality. Finally, **Sec. 4.3** examines the gate driver performance in a full-scale, open-loop power amplifier with SNR measurements that confirm the theoretical impact of the gate signal jitter on the amplifier output SNR.

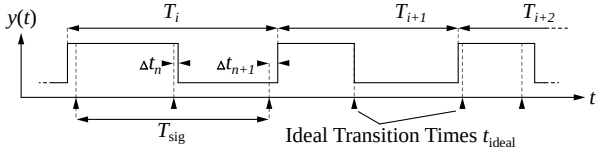

Fig. 4.1: A binary periodic signal is subject to jitter if its edges are shifted by Δt_n away from their ideal transition times, which often follows a stochastic distribution.

4.1 Jitter in Power Electronics

A common switch configuration in power converters is a pair of transistors that act complementary (e.g., arranged in a HB configuration) in order to amplify their rectangular control waveforms. The switching states are generally controlled by a single binary (i.e., 1-bit) signal which encodes the on/off state of the two switches. If this control signal originates from a digital processing system (as opposed to, e.g., an analog pulse-width modulator), the power switch arrangement can be regarded as a digital-to-analog converter, as their switching actions convert the binary, digital control signal into a physical quantity. In this case, the idealized switch-node voltage is an (amplified) copy of the binary control signal, whereas the entire information of the signal is embodied solely in the time-instants of its transitions [142]. In power electronics, the encoding from the information contained in the reference signal (which represents the desired output of the HB) to a binary switch control signal is often achieved using a pulse-width modulator [95].

As described in Sec. 2.2 and Sec. 2.3, the replication of the binary control signal in the physical domain is, due to nonideal properties associated with power electronic switches, such as nonzero switching times or on-state resistances, or clock frequency limitations in digital processing systems, among others, not ideal. Thus, noise and distortion are added to the converter's power output waveforms.

In the following, signal jitter, another undesired phenomenon which especially affects binary signals and limits their achievable SNR, is investigated. In the time domain, it can be regarded as a stochastically varying delay in a signal path. Consequently, in a binary signal, this effect shifts the signal transitions away from their ideal time instants and thus alters its information content [97,143,144]. If the jitter is of stochastic nature, noise is usually added to the signal's spectrum, e.g., jitter following a normal probability distribution usually introduces white noise [145]. In common digital systems, the time

shifts of the signal transitions are usually less than 1 ns. Precision ADC circuits require jitter values of the sampling signals well below 100 ps, which is also detailed in Sec. 6.5 and [88].

Fig. 4.1 shows a jittery periodic binary signal that could be the gate control signal of a HB's high-side switch (which is identical to the signal waveform of the idealized HB switch-node voltage). The jitter expresses itself as the time-dependent deviations Δt_n of the signal's edge positions from their ideal instants t_{ideal}. Note that the jitter changes the signal's period T_{sig} such that each subsequent period has a slightly different duration T_i. Throughout this thesis, jitter is measured by acquiring the durations T_i of randomly selected periods of such a signal. The RMS value of the jitter, given that N periods are recorded, and under the assumption of a Gaussian distribution, can then be given as

$$T_{\text{Jit,RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(T_i - T_{\text{avg}})^2}, \tag{4.1}$$

with

$$T_{\text{avg}} = \frac{1}{N}\sum_{i=1}^{N} T_i \approx T_{\text{sig}}. \tag{4.2}$$

Note that $T_{\text{Jit,RMS}}$ is the standard deviation of the randomly sampled periods T_i [97]. As the periods T_i follow a stochastic process, a sufficient number of samples N must be recorded in order to correctly assess the RMS value. Often, $1000 < N < 10000$ is sufficient [146].

As shown in [99], $T_{\text{Jit,RMS}}$ can be used to derive the best achievable SNR (in a bandwidth f_{BW}) of a sinusoidal, pulse-width modulated signal:

$$\text{SNR}_{\text{max}} = 20\log_{10}\left(\frac{m}{4\sqrt{2}\cdot T_{\text{Jit,RMS}}}\sqrt{\frac{T_{\text{sig}}}{f_{\text{BW}}}}\right)\ \text{dB}, \tag{4.3}$$

where m is the modulation index of the normalized input signal of the pulse-width modulator: $0 \leq m \leq 1$. **Fig. 4.2** illustrates this equation for different common pulse repetition frequencies in power electronic converters. It is evident that even signal jitter values in the picosecond-range can limit the achievable SNR to values below 100 dB. This effect is also discussed in Sec. 6.5, where the signal jitter influences the SNR of an ADC. Consequently, the origins and magnitudes of jitter in power converters must, depending on the application, be carefully analyzed to be able to obtain low-noise power amplifier output waveforms.

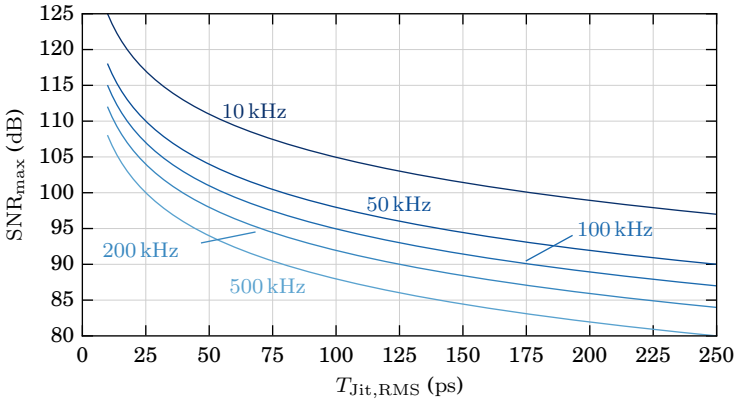

Fig. 4.2: Plots of (4.3) that visualize the best achievable SNR of a jittery PWM signal, for different pulse repetition rates f_{PWM}. The assumed modulation index is $m = 1$ and the SNR bandwidth f_{BW} is 10 kHz.

A digital signal often accumulates jitter as it passes through integrated circuits like DSPs, FPGAs, logic gates or signal buffers. However, these contributions are usually small and only significant for high-speed data transmission systems [97]. Electromagnetic interference can also contribute to signal jitter, usually through crosstalk with closely located digital signals. In power converters, fast-changing switch-node voltages can be a substantial source of jitter-inducing EM fields. Careful signal routing must be employed to minimize the influence from such sources [147]. However, the most prominent source of jitter in power converters are signal isolation circuits, such as commonly used optocouplers or non-optical digital signal isolators, which are used to transmit a digital signal across a galvanic isolation barrier. **Fig. 4.3** depicts a HB switching leg, which is a typical building block of power converters, and consists of two power transistors, T_1 and T_2, and their respective gate driver circuits. In order to allow any control system reference potential between the potentials U_{POS} and U_{NEG} of the DC-link rails, T_1 and T_2 require galvanically isolated gate driver circuits, as the driver reference potentials (i.e., the transistor source contacts) are not identical to the control circuit reference potential, and may also change rapidly upon switching transitions of the HB switch-node output $u_{SN}(t)$.

Digital signal isolators feature shorter propagation delay times, stricter time tolerances and higher CM transient withstand capabilities across their

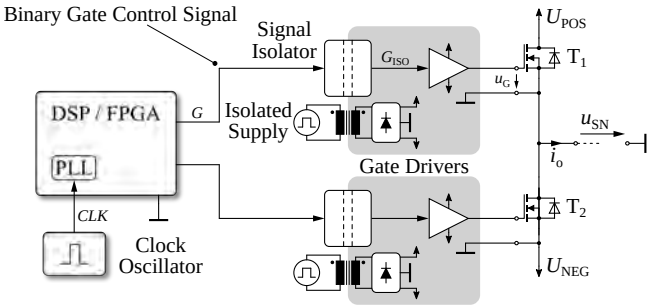

Fig. 4.3: Conventional HB switch arrangement with two power transistors, their gate drivers and a digital gate signal source. The signal isolator adds jitter to the isolated signal G_{ISO}.

isolation barriers than optocouplers and are thus expected to perform better in low-distortion applications where the signal integrity is of importance [148, 149]. The usage of discrete signal isolation transformers is discouraged as they cannot transmit DC signals, are prone to malfunctioning when subject to fast (CM) voltage transients across their isolation barriers and tend to become bulky when operating at low frequencies. Likewise, integrated HB drivers typically have the disadvantages of low CM transient withstand capabilities, are not galvanically isolated and are susceptible to latch-up conditions [150, 151].

Jitter data of digital isolators is rarely provided and if available, it often lacks a clear definition or measurement description. Consequently, the following section presents measurements of jitter figures of commonly used commercial signal isolation techniques. It shows that the amount of jitter varies significantly, not only between, but also within different isolator technologies, which renders their selection process difficult and encourages the design of a gate driver that is immune to the jitter of any isolator, which is presented afterwards in Sec. 4.2.

4.1.1 Jitter Figures of Common Signal Isolators

Different commonly used signal isolators for power electronic applications, with isolation ratings up to 5 kV RMS, are compared experimentally with respect to their jitter performance, as such data is scarcely provided by manufacturers.

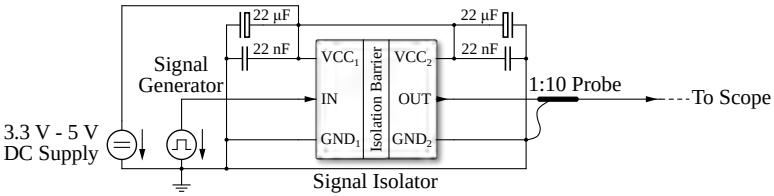

Fig. 4.4: Circuit for the signal isolator jitter measurement. All components and the oscilloscope probe are directly placed at the device package. The signal generator is internally terminated with 50 Ω. When possible, 3.3 V is used as supply voltage.

The output jitter of the isolators is measured by generating a low-jitter rectangular voltage waveform with a fixed period using a precision signal generator (*Tektronix AFG3102*), and feeding it to the input of the considered signal isolator (with the appropriate signal level), whose supply is sufficiently bypassed and filtered. **Fig. 4.4** illustrates the circuit configuration. At the isolator output, the durations of randomly sampled periods are obtained with an oscilloscope (*Rohde&Schwarz RTO1014*) and the RMS jitter of the output signal is approximated with the standard deviation of the measured periods (see (4.1)). More than 5000 period durations are recorded for each measurement in order to reliably record the standard deviation. For all measurements, the input waveform has a frequency of 200 kHz, which is a value close to regularly used sampling or switching frequencies in power electronic applications. The waveform generator's inherent RMS jitter is 7.3 ps and the oscilloscope's jitter contribution is below 5 ps [152], which, by considering these (uncorrelated) standard deviations, results in a lower measurement boundary of $\sqrt{5^2\text{ps} + 7.3^2\text{ps}} = 8.8\,\text{ps}$ RMS for this jitter measurement method.

Fig. 4.5 illustrates the measurement results for the analyzed signal isolators which feature different signal propagation times and a wide range of CM transient immunities (CMTI). The figure indicates how fast the voltage across the device's isolation barrier may change without producing erroneous output signals or entering a nonrecoverable latched-up state. Note that the propagation times and CMTI values are obtained from datasheets. Isolators based on a capacitive isolation method often modulate the input signal to increase its frequency (and to be able to transmit DC signals) and then transfer it via capacitive coupling across a dielectric to the isolated side, where it is demodulated and output [148, 167, 168]. Depending on the detailed implementation of the internal (de-)modulator, significant amounts of jitter can be added to the transmitted signal. Magnetic isolators use a similar approach, but the signal

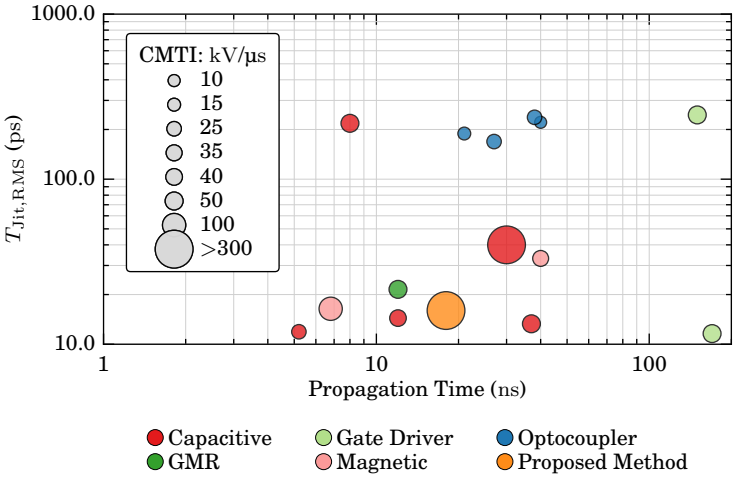

Fig. 4.5: RMS jitter of different types of digital signal isolators. CMTI: CM transient immunity. GMR: Giant magnetoresistive effect. Note that the (high-side) gate drivers do not provide a galvanically isolated interface, as they use a high-impedance signal path to the high-voltage potential. Capacitive isolators: [153–157]. Gate drivers: [158, 159]. Optocouplers: [160–163]. GMR: [164]. Magnetic isolators: [165, 166].

is inductively coupled to the isolated output side [169]. Another method of magnetic coupling is based on the giant magnetoresistive effect (GMR) [170]. For the sake of completeness, high-side gate drivers are also investigated, even though they do not provide a galvanic isolation as they transfer the signal through a high-impedance path [171].

The measurements indicate that different isolators, providing a wide range of propagation times and CMTIs, show a wide spread of jitter values, even when utilizing a similar isolation technology. This renders the selection process for a low-jitter signal isolator, required for the low-noise transmission of the gate control signals, more complex and necessitates a careful analysis. Consequently, the following section introduces a robust gate driver capable of rejecting jitter from any signal isolator in order to achieve low-noise switched amplifier waveforms.

4.2 Proposed Low-Jitter Gate Driver

As shown in the previous section, the selection of a low-jitter isolator is complicated by the lack of manufacturer data, and similar isolation technologies show jitter figures that can vary by an order of magnitude. Additionally, signal isolators with a sufficient CMTI, which is required for fast-switching WBG power transistors, are scarce. Thus, a robust isolated gate driver is presented that rejects even large amounts of jitter introduced by the gate signal isolator. There are several methods to reduce the jitter of a periodic digital clock signal, among them are jitter filters based on phase locked loops (PLLs) or controlled oscillators, which are usually employed in isolated analog-to-digital converters to produce the low-jitter sampling clock signals [88,172,173]. However, these methods are only applicable to periodic clock signals with a fixed duty cycle, which is not the case for modulated gate control signals.

Hence, this work proposes the circuit depicted in **Fig. 4.6** to eliminate the jitter introduced to the gate signal by the isolator. It provides a very low-jitter gate control signal to the switching transistor and thus, eliminates the corresponding source of noise. The circuit utilizes a basic concept proposed in [174], but improves it by not using an isolated clock generation device, which reduces complexity. Furthermore, the circuit is rendered immune to fast CM voltage transients, i.e., it prevents a faulty turn-on or turn-off of the power transistor in case the signal isolator emits erroneous signals during switch-node voltage transients of high $\mathrm{d}u_{\mathrm{SN}}/\mathrm{d}t$.

The key component of this gate driver is a clock-edge triggered D-type flip-flop which is used to re-synchronize the jittery gate control signal G_{ISO}

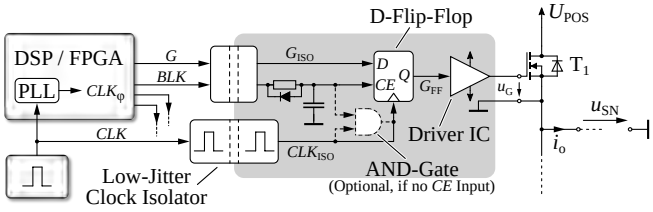

Fig. 4.6: Proposed gate driver which significantly reduces jitter and is immune to output voltage transitions with a high $\mathrm{d}u_{SN}/\mathrm{d}t$. The driver is illustrated for a high-side transistor in a HB switching arrangement, but it is not limited to this power stage configuration. If the flip-flop does not provide a clock-enable (*CE*) input, a logic AND-gate can be used to gate the flip-flop's clock signal. The isolated supply and the identical driver of the second transistor T_2 of the bridge leg are not shown.

after the signal isolator onto a low-jitter clock signal CLK_{ISO}, which is synchronous to the system's global clock signal *CLK*, and supplied to the isolated gate driver using a small signal transformer which is capable of operating with frequencies in excess of 100 MHz. The clock isolation transformer is driven by a high-speed, low-voltage differential signal (LVDS) driver, and an LVDS receiver is used to recover CLK_{ISO} from the transformer's secondary [175]. As shown in Sec. 4.2.3, Tab. 4.2 below, this technique adds ≈6 ps of RMS jitter to CLK_{ISO}. The *CLK* signal, which is derived from an integrated precision oscillator, achieves ≈3.3 ps RMS jitter. As mentioned in Sec. 4.1, this transformer-based clock isolator cannot be used to transmit the gate control signal, as it is only capable of transmitting AC signals, and it has an insufficient CM transient rejection. The functionality of the logic AND-gate and the flip-flop's clock-enable (*CE*) input, as illustrated in **Fig. 4.6**, is explained in Sec. 4.2.1 below.

Fig. 4.7 depicts the timing waveforms of the different signals used in the gate driver circuit. Note that the functionality of the *BLK* signal is explained afterwards in Sec. 4.2.1. In order to fulfill the flip-flop's setup/hold timing requirements to prevent a potentially unstable flip-flop output, the clock used for the DSP/FPGA, CLK_φ, must potentially be shifted in phase relative to the isolated clock CLK_{ISO}, such that, ideally, a signal transition of G_{ISO} coincides with the falling edge of CLK_{ISO}. As G_{ISO} is a jittery signal, its worst-case transition instants must be used to assess the flip-flop timing. Discrete flip-flops typically have setup/hold times below 500 ps [176]. The required phase shift, which mainly depends on the propagation delay of the gate signal isolator $T_{pd,ISO}$ and the clock isolator, can be accomplished by, e.g., using on-

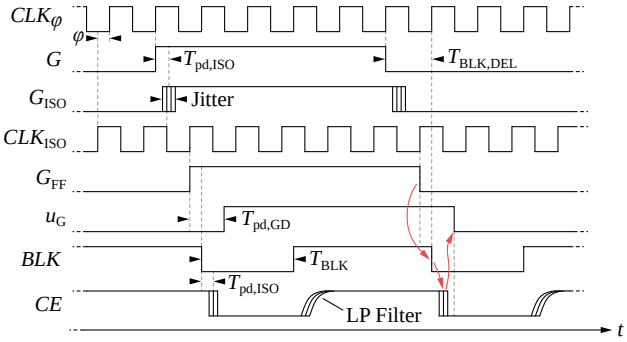

Fig. 4.7: Timing waveforms of the proposed circuit. CLK_φ is used by the digital control system. *BLK* and *CE* are used to render the system immune to bridge leg output transitions with a high $\mathrm{d}u/\mathrm{d}t$. $T_{\mathrm{pd,ISO}}$ and $T_{\mathrm{pd,GD}}$ are the propagation delays of the signal isolator and the gate driver IC. The required sequencing of G_{FF}, *BLK* and *CE* is indicated with arrows.

chip digital clock managers of the gate signal generating FPGA [177]. If such an integrated phase-shifting feature is not available, an external configurable delay line circuit can be utilized. As multiple such gate drivers may be present in a power electronic converter, it is necessary that the signal propagation delays of the clock and gate control signals are matched between different gate drivers, such that the setup/hold timings are as similar as possible for all flip-flops in order to prevent timing violations. This may necessitate length matching of the signal traces and may restrict the worst-case device-to-device propagation delay skew of the signal isolators. If the flip-flop's timing cannot be guaranteed by such measures, it is possible to place a second flip-flop after the first one in order to significantly reduce the possibility of an unstable output of the second flip-flop [178]. The maximum frequency of the clock signal *CLK* at which the circuit can operate depends only on the limitations of the used devices like the flip-flop or LVDS drivers/receivers. Experiments show that 100 MHz poses no problems, whereas at 200 MHz, the output signal integrity of the LVDS receivers used in the clock isolation circuit decreases significantly, which prohibits a reliable operation of the flip-flop [179].

In the following, it is shown how the flip-flop's clock-enable input can be used to render the circuit immune to faulty outputs of the signal isolator which can emerge during fast switching actions of the power transistors.

4.2.1 Common-Mode Transient Immunity

In typical power converter circuits, the switch-node voltage also appears across the isolation barrier of the high-side transistor gate driver signal isolator, i.e., with reference to **Fig. 4.3**, the signal isolator of T_1, whose output side is connected to the source contact of T_1, is subjected to $u_{SN}(t)$ across its isolation barrier. Unfavorably, signal isolators are only rated for a certain maximum $^{du}/_{dt}$ of their isolation barrier voltage (usually 50 kV/µs to 100 kV/µs), without producing faulty output signals [149, 168, 180, 180]. These values are regularly exceeded, at least during portions of the voltage transitions, with fast-switching GaN or SiC power transistor HB circuits [141]. The proposed gate driver of **Fig. 4.6** is also designed to prevent the transmission of faulty control signals from the signal isolator output through the flip-flop to the gate driver IC during, and shortly after, switch-node transients, and thus avoids an undesired and potentially destructive turn-on (or turn-off) of the associated power transistor.

The central concept is a second control signal (the blanking signal *BLK*), which is used to disable the flip-flop, i.e., it conserves its output G_{FF} regardless of a potentially faulty data input *D* (see **Fig. 4.6**). A passive RC low-pass filter in the blanking signal's path prevents temporary (nanosecond range) erroneous signals, that are potentially emitted by the signal isolator during fast switch-node transients, from re-enabling the flip-flop during the ongoing voltage transition. In order to be able to quickly disable the flip-flop before a switch-node transient is initiated by the switching transistor, a signal diode is placed across the resistor of the low-pass filter. In order to disable the flip-flop, its clock-enable (*CE*) input can be used or, if such an input is not available, a logic AND-gate controlled by the *BLK* signal can disable the flip-flop's clock signal as illustrated with dotted lines in **Fig. 4.6**. The required control of the *BLK* signal is identical in both configurations.

The corresponding waveforms of the *BLK* and *CE* signals are also illustrated in **Fig. 4.7**. Note that the required sequencing of the control signals G_{FF}, *BLK* and *CE* is indicated with red arrows. The flip-flop must be disabled (*CE* pulled low) before the gate driver initiates the switch-node transition by changing the gate voltage u_G. Additionally, **Fig. 4.8** illustrates the blanking sequence and the required timing for both gate drivers of a HB configuration. The blanking delay time $T_{BLK,DEL}$ ensures that the flip-flop can update its output before it is disabled by pulling *BLK* low. As common gate drivers have a propagation delay in the range of 5 ns to 50 ns, and the charging/discharging of the transistor's gate capacitance also takes some time, $T_{BLK,DEL}$ is usually smaller than $\approx$ 30 ns in order to disable the flip-flop before the fast

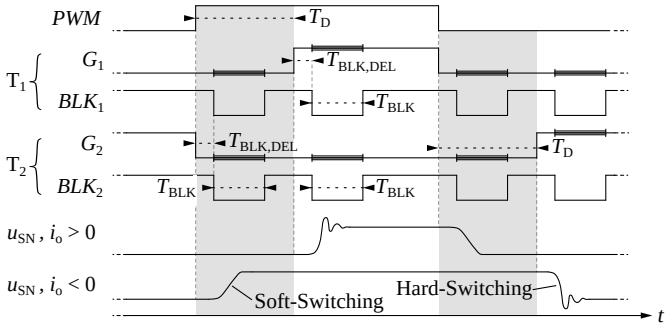

Fig. 4.8: Blanking signal control for the two HB transistors T_1 and T_2, controlled by a binary PWM signal. The blanking delay time $T_{BLK,DEL}$ ensures that the flip-flop can update its output. During the blanking time T_{BLK}, the switch-node voltage transition occurs and *BLK* is held low to disable the flip-flop. After the dead time T_D, the complementary transistor is switched. The switch-node voltage $u_{SN}(t)$ is drawn for both polarities of the HB output current.

switching transition takes place. The flip-flop is disabled during the blanking time T_{BLK}, in which the switch-node potential undergoes its transition. After the dead time T_D has elapsed, which is the amount of time required to prevent a simultaneous turn-on of both HB transistors and/or a short-circuit of the DC-link rails, the complementary transistor's gate signal is toggled and another blanking cycle is initiated. Both gate drivers go through a blanking cycle if any of the two gate signals change, which is required as the polarity of the output current defines which gate signal (G_1 or G_2) finally initiates the switch-node transition. A state-machine in the gate signal generating FPGA can be used to control the timing of the gate and blanking signals.

This system limits the minimum dead time and switch-node voltage pulse widths, as time must be allotted for the blanking cycle ($T_{BLK,DEL} + T_{BLK}$) and the low-pass filter in the path of the *BLK* signal, during which the bridge leg's output state cannot be changed. Timing parameters that proved viable for the measurements presented in the following section are listed in **Tab. 4.1**.

Additionally, the flip-flop introduces a time delay of one digital clock period $1/f_{CLK}$ to the gate signal's path. However, as the digital clock frequency is usually >100 MHz, this delay is negligible. Furthermore, due to the repeated and fast voltage transients, the dielectric of the signal isolator can be subject to accelerated aging due to dielectric losses, which potentially reduces its lifetime or insulation capability [181]. In order to reduce the dielectric stress, a

Tab. 4.1: Viable timing parameters for the low-jitter gate driver. Some time is required for the blanking sequence that prevents faulty switching actions. This limits the minimum dead time T_{D}.

CLK_{φ}, CLK_{ISO}	Max. Frequency	100 MHz to 150 MHz
T_{D}	Min. Time	50 ns to 70 ns
T_{BLK}	Time	≈30 ns
$T_{\mathrm{BLK,DEL}}$	Time	≈20 ns

small CM inductor can be placed in series to the signal isolator, which reduces the dynamics of the CM transients [182].

The presented gate driver works with any kind of power electronic switch (e.g., silicon, SiC or GaN enhancement-mode MOSFETs, or IGBTs), as the creation of the low-jitter isolated signal is decoupled from the driving circuitry that is directly connected to the switch and provides the appropriate signal levels and powers for its control.

4.2.2 Simplified Circuit Variants

The comparison of isolator jitter measurements in **Fig. 4.5** reveals the availability of low-jitter digital signal isolators. These devices, however, are not robust against fast CM transients and thus, faulty outputs during, or shortly after high-speed switch-node transients are experienced. However, such an isolator could be used in the simplified gate driver circuit depicted in **Fig. 4.9**. A re-synchronization to a low-jitter clock is not necessary due to the low-jitter isolator. By employing a digital latch with a dedicated enable input (*LE*), the faulty isolator outputs can be prevented from reaching the gate driver IC in the same way as it is done for the flip-flop-based driver described above. This results in a simplified circuit. The approach has been tested with a *Nexperia 74AUP1G373GW,125* latch and a *Texas Instruments ISO7220* digital isolator and worked as expected (note that measurements of the previously presented re-synchronizing gate driver are given in the next section).

Unfortunately, this approach still exposes the digital isolator to fast-changing voltage transients across its isolation barrier, which can potentially lead to a permanent latch-up of the digital signal isolator due to its low CMTI rating, which cannot be reliably prevented. Therefore, this circuit is only

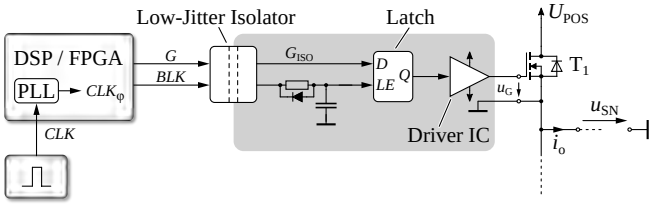

Fig. 4.9: Simplified gate driver that is immune to faulty outputs of the signal isolator, as the latch enable input can be used to retain the output of the latch during switching actions. However, the digital signal isolator is prone to permanent latch-up, as low-jitter devices are often not robust against fast CM voltage transients.

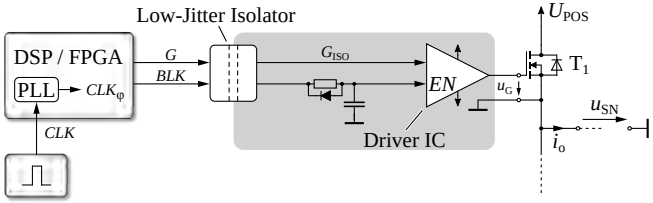

Fig. 4.10: The blanking signal directly disables the gate driver and ensures a reliable turn-off of the power transistor. However, this does not prevent the parasitic turn-off of the transistor, caused by short-lived faulty digital signal isolator outputs.

encouraged if the avoidance of a permanent signal isolator latch-up condition can somehow be ensured.

As shown in **Fig. 4.10**, some gate driver ICs provide an enable input (*EN*) that could be controlled directly by the blanking signal *BLK* in order to disable the gate driver (i.e., turn the corresponding power transistor off), which prevents a parasitic turn-on and potential short-circuit of the DC-link, caused by faulty isolator output signals. However, this circuit does not prevent a parasitic turn-off of the power transistor, which can occur some nanoseconds after its turn-on, caused by faulty digital signal isolator outputs that can propagate through the diode of the low-pass filter. This behavior has in fact been observed and the circuit is thus also not encouraged, as the HB switch-node voltage is significantly distorted by the short parasitic turn-off of one of its power transistors.

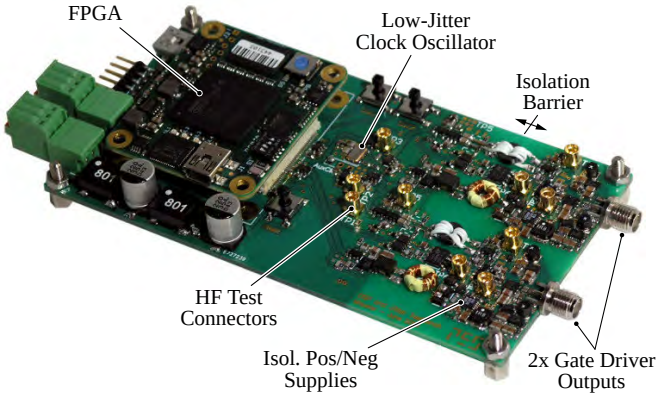

Fig. 4.11: Hardware demonstrator featuring two isolated gate drivers with the jitter reduction circuitry. The clock isolator comprises a *Fair-Rite 5943000101* toroidal core with $N_1 = N_2 = 4$ turns, being driven by an LVDS driver. The (jittery) digital signal isolator is an *SI8620*, the gate driver IC is an *LM5114* and the clock oscillator is an *FXO-HC536R-100*. The flip-flop is a *74LVC1G79GV* and its *CE* functionality is implemented with an AND-gate at its clock input.

Therefore, in the following, the jitter rejection capability of the initially presented flip-flop-based gate driving circuit is validated with measurements on a small-scale demonstrator, whereas the subsequent Sec. 4.3 also performs the corresponding high-power and SNR measurements that link the low-jitter gate driver signals to low-noise output waveforms in a realistic amplifier setting.

4.2.3 Jitter Rejection Measurements

The low-jitter gate driver circuit shown in **Fig. 4.6** is implemented in a small-scale hardware demonstrator in order to verify its basic functionality. **Fig. 4.11** shows the system which features two isolated, low-jitter gate drivers (capable of driving a HB switch arrangement), an FPGA and a low-jitter clock oscillator that also serves as the FPGA's clock source.

Using this prototype, the RMS jitter along the gate signal path is measured. **Fig. 4.12** illustrates such a measurement in the time domain for the rising edges of the (periodic) signals G_{ISO} and G_{FF} (cf. **Fig. 4.6**) after one period, with each edge transition being made visible using the oscilloscope's infinite screen persistence and the oscilloscope trigger being set to the previous rising

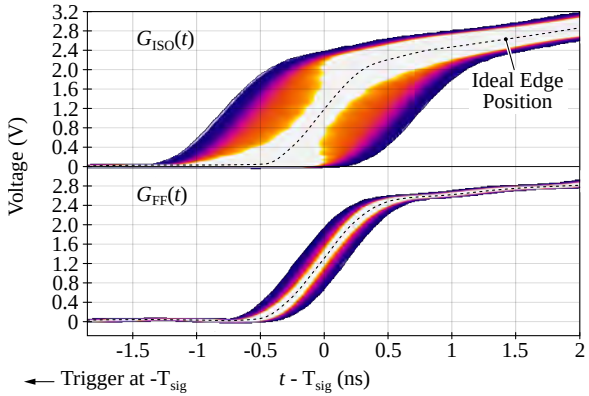

Fig. 4.12: Persistent oscilloscope waveforms of two key gate driver signals, visualizing their jitter. Brighter colors represent more signal transitions. The oscilloscope has a 1 GHz analog bandwidth and samples with 10 GHz (*R&S RTO1014*).

edge. A high-bandwidth oscilloscope must be used to minimize the influence of its own time base jitter, which is usually in the single-digit picosecond range, as described in Sec. 4.1.1.

Tab. 4.2 lists the RMS jitter values of different signals along the gate signal path, measured using the method presented in Sec. 4.1 and Sec. 4.1.1. For these measurements, a rectangular voltage waveform is created by the FPGA and transmitted to the gate drivers. The clock frequency of the low-jitter oscillator is 100 MHz. Using (4.3), the maximum achievable SNR is also exemplarily listed for the corresponding jitter values (using f_{PWM} = 100 kHz and f_{BW} = 10 kHz). It is evident that the signal isolator adds the most jitter (i.e., 215 ps) to the gate signal. The clock isolator only contributes 5.7 ps of RMS jitter. The remaining contributions arise from the re-synchronization flip-flop and the gate driver IC.

Due to the stochastic nature of jitter, a visualization with a histogram is done. **Fig. 4.13** depicts the measured time deviations of G_{ISO} and G_{FF} from their ideal transition instants. It reveals that the jitter of G_{FF} can be approximated by a normal distribution with a standard deviation of 24.7 ps. This does not apply to the distribution of G_{ISO}, which shows a more triangular shape, caused by internal processes of the digital signal isolator.

These measurements verify the basic functionality of the low-jitter gate driver in the sense that it is capable of rejecting the jitter of the digital signal isolator. Furthermore, it confirms the isolator as the only significant source

Tab. 4.2: Measured RMS jitter values of signals along the gate signal path in the low-jitter gate driver. The max. achievable SNR is derived from (4.3) for a PWM frequency of 100 kHz and a bandwidth of 10 kHz

Signal	$T_{\mathrm{Jit,RMS}}$ (ps)	$\mathrm{SNR}_{\mathrm{max}}$ (dB)
CLK	3.3	124.6
CLK_{ISO}	9.0	115.9
G	33.5	104.4
G_{ISO}	248.0	87.1
G_{FF}	24.7	107.1
u_{G}	25.1	107.0

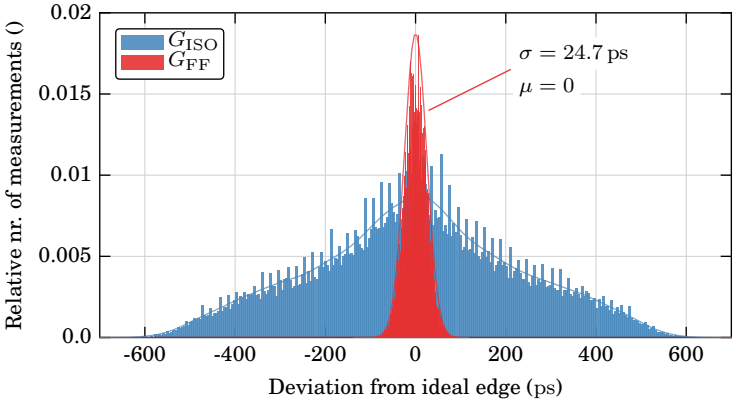

Fig. 4.13: Histogram of two jittery signals as measured on the small-scale hardware demonstrator. G_{ISO} is the signal after the digital isolator and G_{FF} is the same signal after the re-synchronization flip-flop.

of jitter, as other digital logic elements and the high-frequency clock isolator contribute only marginally to the jitter of the transistor gate signal.

The following section performs similar measurements, but on the high-voltage switch-node of a HB power stage, employed in a realistic amplifier setting. The beneficial effects of the low-jitter gate driver signals on the amplifier's output SNR are also presented.

4.3 High-Power and Noise Measurements

A switch-mode power amplifier is used to assess and verify the low-jitter gate driver in a realistic setting. The system is presented in full detail in Ch. 7, whereas for this analysis, it is operated in an open-loop fashion to illustrate the noise in the output waveforms that results from gate signal jitter (i.e., no feedback control is used). Furthermore, the system contains only two independent HBs, comprising four top-cooled *GanSystems GS66508T* E-HEMT GaN transistors, operated at a DC-link voltage of up to 400 V (as opposed to operating with four HBs, which is the system's full capacity, as shown in Ch. 7). In order to enable a direct comparison, one HB operates with a regular, jittery gate driver, while the other HB uses the proposed low-jitter driver. **Fig. 4.14** illustrates the hardware demonstrator as configured for this analysis.

4.3.1 Measurement Setup

The two utilized HBs are denoted as HB A and B, respectively. Both gate drivers of HB A are configured in such a way that the low-jitter feature is disabled. Thus, they behave as regular, jittery gate driver circuits. Hereby, the blanking signal *BLK* is used to keep the gate driving IC's output permanently low during switch-node transitions, utilizing a second control input of the gate driver IC, which prevents a parasitic turn-on of the power transistor, and the jittery signal isolator output is directly routed to the gate driver IC. Otherwise, the two HBs are operated identically. **Fig. 4.15** depicts the circuit configuration for the measurements and **Tab. 4.3** lists relevant component values. The gate drivers apply a voltage of +6 V between gate and source of the E-HEMT transistors in order to turn them on and a voltage of −3.3 V to ensure a reliable turn-off. The digital clock frequency is set to 100 MHz and for the low-jitter gate drivers, the blanking delay time $T_{\mathrm{BLK,DEL}}$ is set to 20 ns, the blanking time T_{BLK} to 30 ns and the dead time T_{D} to 70 ns.

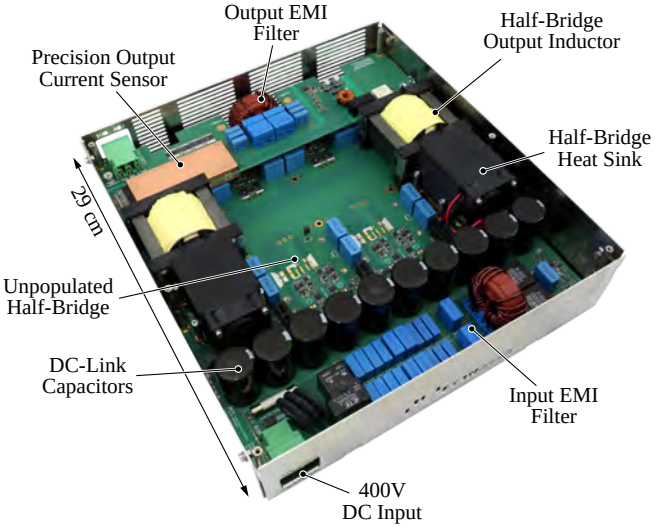

Fig. 4.14: Power amplifier demonstrator with the control board removed. Two of the four HBs are populated, which employ top-cooled *GS66508T* GaN E-HEMT transistors. This allows a direct comparison of the low-jitter gate driver with a regular approach.

To measure the SNR of the filtered HB output voltages $u_{\mathrm{L,A}}$ and $u_{\mathrm{L,B}}$, a high-precision, two-channel spectrum analyzer (*Rohde&Schwarz UPV*) is used [183]. Furthermore, to reduce the otherwise significant quantization noise of the PWM signals, the optimized noise shapers, as presented in Ch. 5, are employed. This significantly reduces HB output noise caused by the PWM, in a band from DC to 10 kHz, which renders the noise contribution from the jittery gate signals observable. The digital pulse-width modulators are clocked with 100 MHz and have (configurable) counter resolutions of 9, 8 and 7 bit, which results in pulse repetition frequencies f_{PWM} of 97.8 kHz, 196.1 kHz and 393.7 kHz respectively, as symmetric triangular PWM counters are employed (see (5.2) in Sec. 5.1) [95]. As the two HBs are operated in an open-loop fashion, a low-noise 400 V power supply is required as such a switch-mode amplifier is characterized by a low power supply rejection [102–104]. Otherwise, too much additional noise is introduced to the HB output voltages, which renders the noise contributions from the gate drivers unobservable. For these experiments, an *HP 6035A* power supply is used (0-500 V, max. 5 A or 1 kW).

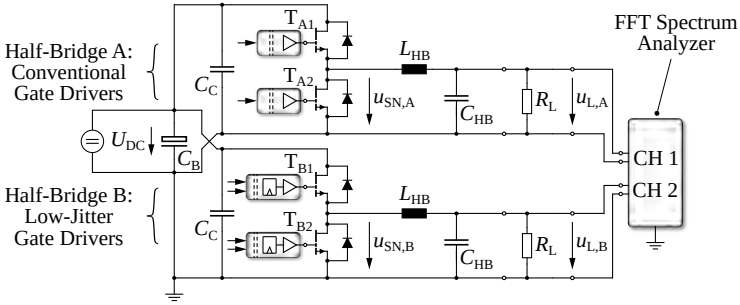

Fig. 4.15: Circuit configuration for the measurements. HB A features a conventional, jittery gate driver whereas the low-jitter gate driver is used in HB B. The SNR of the HB output signals $u_{\mathrm{L,A}}$ and $u_{\mathrm{L,B}}$ is measured using a *Rohde&Schwarz UPV* high-precision FFT spectrum analyzer.

Tab. 4.3: Amplifier configuration of the measurement setup (see **Fig. 4.15** for the corresponding circuit diagram).

C_B	Bulk DC-Link Capacitors (Electrolytic)	1 mF
C_C	HB Commutation Capacitors (Ceramic)	2 µF
L_{HB}	HB Inductors (Ferrite, N87)	700 µH
C_{HB}	HB Filter Capacitors (Film)	12 µF
R_L	Load Resistor	Variable

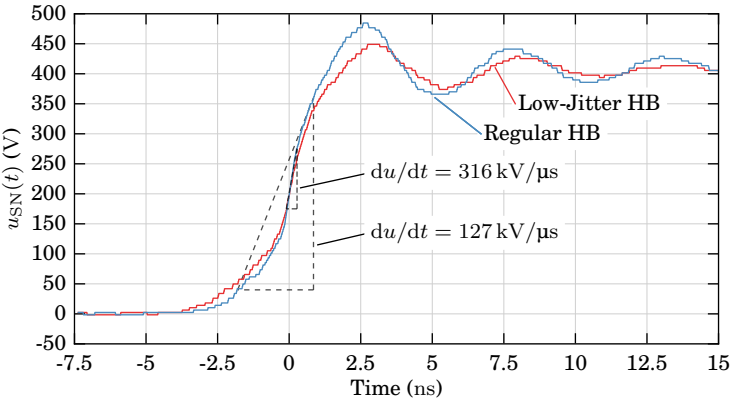

Fig. 4.16: Hard-switched turn-on transients of the two HBs, recorded during steady-state operation with a switching frequency of 100 kHz. $U_{DC} = 400\,V$, $P_{HB} = 1\,kW$.

In the following, the jitter of the high-voltage switch-node output of the HB is measured, as opposed to the jitter of the gate driver signals which is presented in Sec. 4.2.3 above.

4.3.2 Switch-Node Jitter Measurement

The RMS jitter of randomly sampled periods (according to (4.1) and (4.2)) is measured directly at the switch-node voltage $u_{SN}(t)$ with different converter operating conditions. For that purpose, both HBs are operating as independent DC/DC buck converters with a fixed duty cycle $d = 0.5$, and switching frequencies ranging from 100 kHz to 400 kHz. Consequently, $u_{L,x} \approx U_{DC}/2$, and R_L is used to define the DC load power of each HB: $P_{HB} = u_{L,x}^2/R_L$.

Fig. 4.16 illustrates a measurement of $u_{SN}(t)$ of the two HBs at their hard-switching turn-on instant. The fast slew rates corroborate the necessity of a gate driver that is capable of reliably operating with high CM transient stresses across its isolation barrier.

Fig. 4.17 shows oscilloscope measurements of rising edges of $u_{SN}(t)$ of the two HBs after one period, measured for ≈5000-7000 periods, whereas the oscilloscope's screen persistence illustrates recurring transitions with red-shifted colors. The period durations T_i are recorded with the oscilloscope by measuring the elapsed time between two trigger instants (rising edges of $u_{SN}(t)$), whereas the trigger level is set to $U_{DC}/2$. The inherent jitter contri-

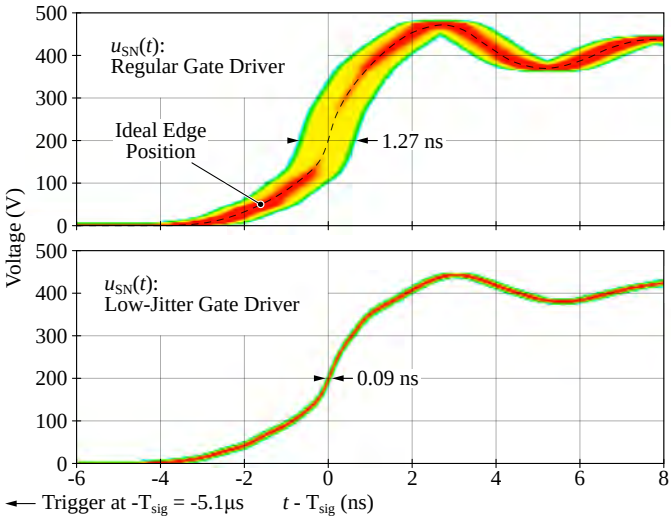

Fig. 4.17: Persistent oscilloscope waveforms of $u_{SN}(t)$, recorded during DC/DC operation of the two HBs at 400 V, 196.1 kHz and 500 W each. The oscilloscope has a 1 GHz analog bandwidth and samples with 10 GHz (*R&S RTO1014*). Between ≈5000 to 7000 signal transitions are recorded.

bution of the oscilloscope itself is expected to be less than 5 ps [152]. This measurement reveals that the low-jitter gate driver reduces the peak-to-peak jitter by a factor of ≈14.

Each period's deviation from the ideal duration is also plotted in a histogram in order to illustrate the underlying stochastic distribution, as shown in **Fig. 4.18** for a selection of different operating conditions of the two HBs. The jitter (of both HBs) is independent of the converter's operating condition such as DC-link voltage, switching frequency or output load, which enables the usage of the low-jitter driver in different applications without the necessity of circuit alterations. The distribution of the regular gate driver's jitter resembles a triangular distribution, whereas the remaining jitter of the improved driver can be approximated with a normal distribution ($\mu = 0, \sigma = 18$ ps).

Using this method, RMS jitter values of u_{SN} from both HBs are recorded for different operating conditions. **Tab. 4.4** lists the measurement results, which show the significant jitter reduction of the high-powered switch-node voltage achieved by the low-jitter gate driver. This is in accordance with the measurements performed on the gate driver circuit alone, as shown

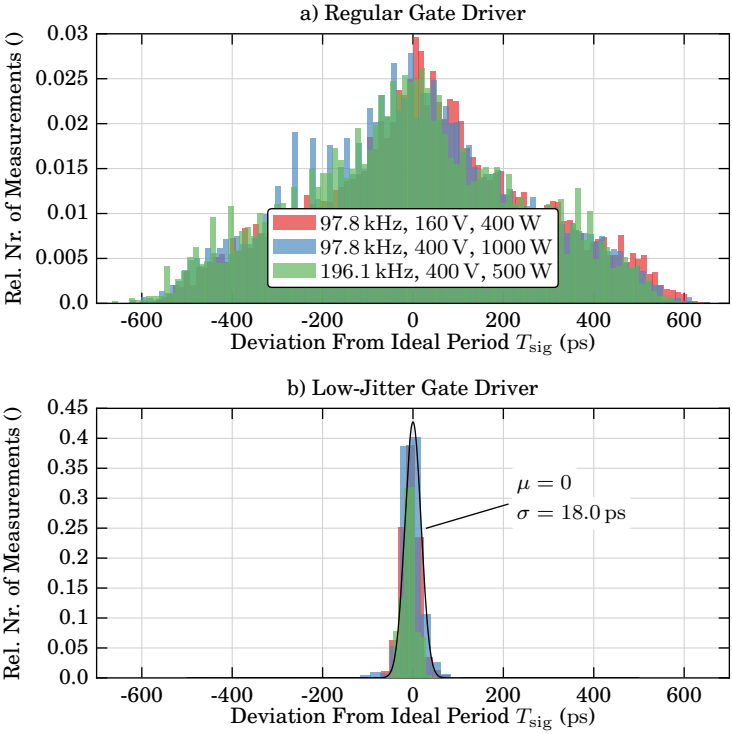

Fig. 4.18: Histograms of (T_{sig} – T_{avg}) of the two HBs operating as DC/DC buck converters with different PWM frequencies and output loads. The legend is valid for both plots. Each histogram incorporates ≈5k-7k measurements. **(a)** Conventional gate driver, 100 bins. **(b)** Low-jitter gate driver, 10 bins.

Tab. 4.4: RMS jitter measured during DC/DC buck converter operation in $u_{SN}(t)$ of the HB with the regular gate drivers (HB A) and the low-jitter drivers (HB B) at different power converter operating points.

U_{DC} (V)	f_{PWM} (kHz)	P_{HB} (W)	$T_{Jit,RMS,A}$ (ps)	$T_{Jit,RMS,B}$ (ps)
160	97.8	100	235.1	18.2
160	97.8	400	236.3	17.9
160	196.1	400	239.2	15.1
160	393.7	400	235.8	30.3
400	97.8	100	230.8	19.0
400	97.8	1000	237.0	19.7
400	196.1	500	238.4	13.5

previously in Sec. 4.2.3. Furthermore, the jitter values remain consistent over a wide range of operating conditions. The RMS jitter recorded at a switching frequency of 393.7 kHz is slightly elevated (30.3 ps) compared to the other values (≈15 ps to 20 ps), which is attributed to thermal effects in the gate driving circuit, as its power dissipation increases at higher frequencies and the integrated circuits (e.g., flip-flop, AND-gate, gate driver IC) are introducing more jitter. Nonetheless, the low-jitter gate driver reduces the RMS jitter on average across the different measurements by a factor of ≈12.

In the following, the SNR of the HB output voltages, with applied sine-modulation, is measured. The results corroborate the necessity for low-jitter gate drivers.

4.3.3 SNR Measurements

Similar to the previous section, the two HBs are operated independently as buck converters, but now, the duty cycles are modulated according to

$$d(t) = m_{DC} + m \sin(2\pi f_F t), \tag{4.4}$$

which creates sinusoidal output voltages with DC offsets, whose SNR is investigated. The selection of $m_{DC} = 0.5$ and $m = 0.42$ leads to a minimum duty cycle of 0.08 and a maximum duty cycle of 0.92. This is done as the noise shapers, which are required to eliminate noise from the PWM, are

optimized for stable operation up to $d = 0.95$, which leaves some safety margin (see Ch. 5). The fundamental frequency f_F is set to 33 Hz as there is no integer ratio with the 50 Hz mains frequency, whose (fundamental and harmonic) components can be visible in the spectra of the measurements due to the amplifier's open-loop operation and the nonideal power supply. The selection of the fundamental frequency does not influence the SNR, as (4.2) shows and measurements confirm.

As with the previous analysis, the converter is operated at different output power levels according to

$$P_{\mathrm{HB,AVG}} = \frac{1}{T_F} \int_0^{T_F} \frac{u_{L,x}(t)^2}{R_L} dt, \tag{4.5}$$

with $T_F = 1/f_F$ and

$$P_{\mathrm{HB,Pk}} = \frac{(U_{DC}(m_{DC} + m))^2}{R_L}, \tag{4.6}$$

while the reactive power resulting from the output filter capacitor C_{HB} is neglected due to the low fundamental frequency f_F. The *Rohde&Schwarz UPV* spectrum analyzer is directly connected to the filtered HB output voltages $u_{L,x}$. As this unit accepts an input voltage of up to 160 V, the DC-link voltage is set to $U_{DC} = 160$ V for these measurements.

Fig. 4.19 shows spectra of the two HBs at $P_{\mathrm{HB,AVG}} = 400$ W and with a switching frequency of 196.1 kHz. As expected, the noise floor of the low-jitter HB is significantly lower. The harmonic distortion of both waveforms is due to the dead time in the HBs, nonzero transistor on-state resistances and nonzero switching times, among others, as described in Sec. 2.3. However, as only the SNR is investigated in this analysis, the harmonic spectral components are of no concern as they are not considered when calculating the noise power (see Sec. 2.1.2). The SNR is measured for different operating conditions of the converter, which **Tab. 4.5** summarizes. As the DC power supply injects some noise and spectral spurs up to ≈300 Hz, which adds to the HB output noise, the SNR is evaluated in a frequency band ranging from 300 Hz to 10 kHz. In **Fig. 4.19**, this supply-related noise contribution is well visible between the harmonics of the 33 Hz fundamental.

These measurements show that the achieved SNR figures are, as expected from the static jitter measurements presented earlier, not significantly dependent on the load power. Note that for the low-jitter gate driver, the SNR values can only be compared for matching PWM frequencies, as different noise shapers are used for each frequency, which affects the noise content of the HB output signals (see Ch. 5).

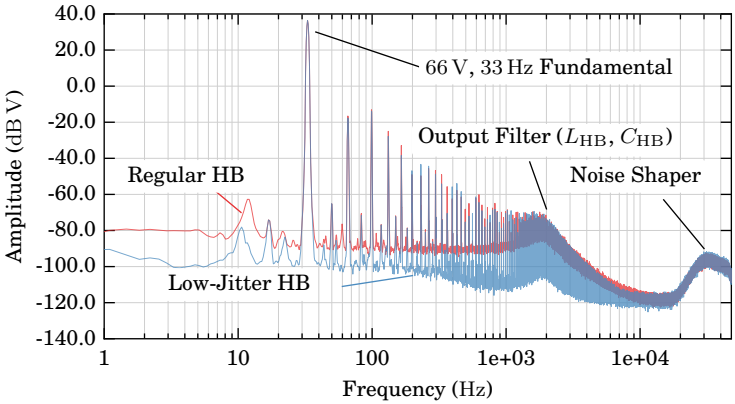

Fig. 4.19: Spectra (AC coupled) of the two filtered HB output voltages $u_{L,x}(t)$. The PWM switching frequency is 196.1 kHz, U_{DC} = 160 V and $P_{HB,AVG}$ = 400 W. The SNR of the regular HB output is 88.3 dB, whereas the low-jitter HB achieves 105.9 dB. Y-axis shows the voltage amplitude in dB relative to 1 V.

Tab. 4.5: SNR measurements for the two HBs at different operating conditions. U_{DC} = 160 V. The SNR is evaluated in a frequency band from 300 Hz to 10 kHz.

f_{PWM} (kHz)	$P_{HB,AVG}$ (W)	$P_{HB,Pk}$ (W)	$SNR_{HB\,A}$ (dB)	$SNR_{HB\,B}$ (dB)
97.8	100	250	87.6	98.8
97.8	400	1000	89.5	99.6
196.1	100	250	86.1	107.1
196.1	400	1000	88.3	105.9
393.7	100	250	84.5	95.4
393.7	400	1000	84.9	90.5

Tab. 4.6: Jitter values (averaged) from different converter loads, the corresponding best possible SNR according to (4.3), evaluated in a bandwidth from 300 Hz to 10 kHz, in comparison to the measured SNR values, which are also averaged from different converter operating points. The relative error compares the theoretical SNR from (4.3) with the measurement.

f_{PWM} (kHz)	$T_{\mathrm{Jit,RMS,A}}$ (ps)	$\mathrm{SNR}_{\mathrm{Max,Calc.}}$ (dB)	$\mathrm{SNR}_{\mathrm{Meas,HB\,A}}$ (dB)	Relative Error (%)
97.8	235.2	86.2	88.6	2.8
196.1	238.8	83.1	87.2	4.9
393.7	235.8	83.2	84.7	1.8
f_{PWM} (kHz)	$T_{\mathrm{Jit,RMS,B}}$ (ps)	$\mathrm{SNR}_{\mathrm{Max,Calc.}}$ (dB)	$\mathrm{SNR}_{\mathrm{Meas,HB\,B}}$ (dB)	Relative Error (%)
97.8	18.7	108.2	99.2	−8.3
196.1	14.3	107.6	106.5	−1.0
393.7	30.3	101.0	93.0	−7.9

Correspondingly, **Tab. 4.6** summarizes the measured RMS jitter and SNR values as arithmetic means from different operating conditions in order to compare them to the best achievable SNR according to (4.3), with $f_{\mathrm{BW}} = 9700\,\mathrm{Hz}$ and $m = 0.84$, as this corresponds to the configuration of this measurement. The acquired jitter values follow the theoretical predictions accurately for the conventional gate driver with the jittery switch-node signal, despite its triangular-shaped distribution (cf. **Fig. 4.18**; note that (4.3) assumes a normal distribution). As the low-jitter HB achieves significantly better SNR figures, it can be concluded that the SNR of the conventional HB output is in fact limited by the jitter of the signal isolators. Regarding the low-jitter HB, the measurement with $f_{\mathrm{PWM}} = 196.1\,\mathrm{kHz}$ also matches well with the theoretical prediction (i.e., −1 % relative error). The increased relative errors of the low-jitter HB operated with the other two PWM frequencies are due to the fact that, at such low noise levels, other noise sources are of similar power, e.g., the residual noise of the noise shaping pulse-width modulators, which strongly depends on their execution rate (see Ch. 5), or the DC amplifier supply.

4.4 Summary

Signal jitter and its deteriorating effect on the output noise of switched power amplifiers is introduced. Measurements of commercial gate signal isolators, which are ubiquitously required in power electronic converters, show significantly varying jitter figures that differ by more than a factor of 10, even within similar signal isolation technologies. Furthermore, digital isolators that provide both low jitter and high CM voltage transient withstand capabilities, are rare.

This corroborates the need for the proposed low-jitter gate driver, which is capable of rejecting jitter from any type of isolator. It uses a high-frequency signal transformer to provide a low-jitter clock to the isolated gate driver circuit, where it is used to re-synchronize the jittery output of the digital signal isolator. Furthermore, by utilizing a second digital signal, the circuit is rendered robust against faulty switching actions during high-speed voltage transients that are common with modern WBG semiconductors and regularly exceed slew rates in excess of 300 kV/µs, as shown with measurements.

The effectiveness of the proposed gate driver is verified on a full-scale open-loop power amplifier at different operating conditions. The measurements confirm the theoretically expected noise values in the amplifier output and demonstrate the desired performance gain when operating with the improved gate driver. Compared to a conventional method, the SNR can be increased by 20 dB, reaching values of 107 dB in a 10 kHz bandwidth. Thus, the presented method reduces a significant source of noise in switch-mode power amplifiers.

5

Noise Shaping ΔΣ Modulation

Pulse-width modulation (PWM) is frequently used in power electronic converters to generate gate control signals for the switching transistors and, like the converter control system, often implemented in the digital domain. Due to practical clock frequency limitations of digital systems, pulse-width modulators can only generate a defined set of values for their output signals. This corresponds to a limited resolution of the modulated signals, which introduces wideband quantization noise that restricts the achievable PWM output SNR. Therefore, conventional PWM is a significant source of noise and thus undesired for precision power amplifiers.

Consequently, the principles of ΔΣ modulation, or noise shaping, are employed, which encompass signal processing techniques that ultimately enable the creation of low-noise PWM output signals. In the discussed application, the required structures are implemented fully digitally. They shift the quantization noise of the limited-resolution pulse-width modulator to higher frequencies, where it is of no concern, as mechatronic positioning systems are only sensitive to noise below a certain frequency (e.g., 10 kHz). They are thus a valuable contribution to low-noise power amplifiers, as they effectively eliminate a considerable source of noise.

First, **Sec. 5.1** explains the fundamental limits and the resulting quantization noise of digital PWM implementations. Next, **Sec. 5.2** introduces digital noise shaping in the context of power electronics. An optimization method is used to maximize the achievable SNR and stability of the noise shaper implementation. Simulations and measurements verify the functionality and effectiveness of the proposed modulation method. Finally, **Sec. 5.3** presents a summary of the results.

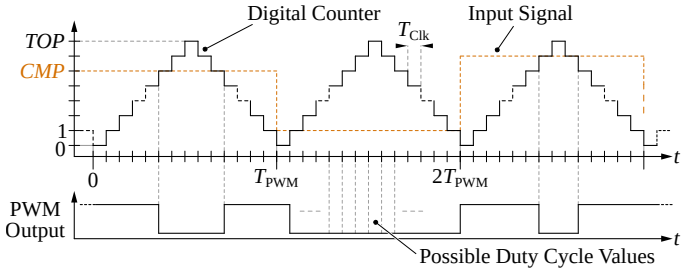

Fig. 5.1: Principle of digital PWM, illustrated with regular symmetrical sampling and a triangular carrier. Each counter step also represents a possible duty cycle, which gives rise to duty cycle quantization and the corresponding wideband noise.

5.1 Limits of Digital PWM

Pulse-width modulators are ubiquitously used in digital control systems of switch-mode converters to generate the required binary switch control signals (which encode the on/off states of the power transistors). Such modulators are well understood, simple to use and applicable to the majority of power stage topologies [95]. As shown in **Fig. 5.1**, digital PWM signals are commonly created with a counter that increments its value with integer step sizes, during one switching period $T_{PWM} = 1/f_{PWM}$, from zero to a predefined value (*TOP*) and, in the case of a triangular carrier, subsequently counts back down to zero [95]. The counting rate usually corresponds to the digital clock frequency f_{Clk}. Whenever the counter value is smaller than the input signal *CMP* (for compare), the binary PWM output signal is set to its high value and otherwise, it is set low. This transfers the information of the *CMP* signal to the binary PWM output. The ratio of the time during which the PWM output signal is high to the duration of a switching period T_{PWM} is the duty cycle. The *CMP* signal is commonly updated once (symmetrical sampling, as illustrated in **Fig. 5.1**) or twice (asymmetrical sampling) per PWM cycle, at the bottom and/or top value of the counter [95]. Note that the range of the *CMP* signal must be identical to the range of possible counter values in order to prevent modulation errors.

The PWM signal generation process is not linear, as the spectrum of the modulated output signal contains frequency components that are generated by nonlinear effects. This behavior is influenced by the carrier waveform and the updating method of the *CMP* signal, which affect high-frequency spectral

components and low-order baseband harmonics of the *CMP* signal in the PWM output [95].

For this work, a regularly and symmetrically sampled PWM implementation with a triangular carrier (cf. **Fig. 5.1**) is used, where the *CMP* value is updated once per PWM period, which leads to symmetrical PWM pulses with respect to the carrier waveform [95]. Compared to a sawtooth carrier, the use of a triangular carrier reduces both low- and high-frequency harmonics [95].

As **Fig. 5.1** illustrates, each counter step represents a possible PWM duty cycle and hence, the duty cycle can only take values from a discrete set (i.e., it is quantized), with the number of available counter steps representing the respective duty cycle resolution [184]. Thus, the achievable SNR of the PWM output signal is limited due to quantization errors that are common to signals of finite amplitude resolution [94]. The SNR of a sinusoidal, amplitude-quantized signal with a resolution of n bits can be approximated by

$$\mathrm{SNR} \approx 6.02n + 1.76 \text{ dB}. \tag{5.1}$$

The representation of digital signals with binary numbers (i.e., in the base-2 numeral system) is common and thus, an amplitude resolution of n bits results in 2^n possible amplitude levels that the quantized signal can be represented with. If the signal is sampled (i.e., updated only at regular time instants), the quantization noise occurs in a frequency band from DC to half the sampling frequency (i.e., the Nyquist frequency) [88].

Consequently, as the digital PWM counter values are also described with binary numbers, the following relations are given, with reference to **Fig. 5.1**:

$$TOP = 2^n - 1 = \frac{T_{\mathrm{PWM}}}{2T_{\mathrm{CLK}}}, \tag{5.2}$$

$$n = \frac{\ln(TOP + 1)}{\ln(2)} = \frac{\ln\left(f_{\mathrm{CLK}}/2f_{\mathrm{PWM}} + 1\right)}{\ln(2)}. \tag{5.3}$$

These equations relate the amplitude quantization with the digital counter frequency and the PWM period. To obtain low-noise digital signals, a sufficient number of amplitude levels is mandatory (cf. (5.1)). Thus, as (5.3) shows, in order to achieve a certain duty cycle resolution for a given PWM frequency $f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}}$, a high digital clock frequency $f_{\mathrm{CLK}} = 1/T_{\mathrm{CLK}}$ is required. For example, to obtain a PWM signal with $f_{\mathrm{PWM}} = 50\,\mathrm{kHz}$ and a duty cycle resolution of $n = 17$ bits, a clock frequency $f_{\mathrm{Clk}} \approx 13.1\,\mathrm{GHz}$ is necessary. However, the physical implementation of high-resolution counters operating at such high clock rates is unfeasible with state-of-the-art digital logic circuits. The limit for configurable logic is usually below 500 MHz for f_{CLK} [185]. This

limits the achievable output resolution of digital pulse-width modulators to usually ≈7–14 bits, as they have to operate with certain minimum values for f_{PWM} that are common to switch-mode power converters (e.g., ≈10 kHz to 1000 kHz). This is insufficient to obtain power transistor gate control signals with a high SNR.

Due to the desired digital control of the amplifiers discussed in this work, analog modulators are not considered. Additionally, high-resolution PWM generators that are available in some digital signal processors, which are usually based on configurable delay lines, also do not provide a sufficiently high resolution [186]. By using high-speed digital serializers, effective PWM counter clock rates up to several GHz can be achieved [187]. However, as shown above, this is not sufficient to achieve PWM signals with a satisfactory SNR. Therefore, the following section presents a digital signal processing technique that can create digital signals of low noise in certain (definable) frequency ranges, despite relying on the low-resolution signals.

5.2 Digital Noise Shaper

As shown above, practical clock frequency limitations restrict the usage of high-resolution PWM in power electronics. However, in Class-D audio amplifiers, high-resolution signals with up to 24 bits of quantization levels need to be converted by such modulators, which can operate with switching frequencies in excess of 300 kHz, in order to obtain the power switch control signals [114, 188, 189]. This would require an unrealistically high digital clock frequency for the PWM counter (cf. (5.2)). Consequently, the counter resolution must be reduced to achieve the desired PWM frequency, which introduces undesired quantization noise. However, as the human hearing is generally limited to a frequency range below ≈20 kHz, a signal processing technique named delta-sigma (ΔΣ) modulation, or noise shaping, has been developed for audio amplification, which can be employed in conjunction with limited-resolution PWM [96, 190]. The noise shaping technique shifts the quantization noise, that is generated when low-resolution digital signals are created from high-resolution references, to frequencies, e.g., in the application of audio amplifiers, above 20 kHz, where it is not perceivable by humans and thus, of no concern. This allows the unaltered replication of the high-resolution reference signals with limited-resolution PWM in a certain frequency band (the baseband). **Fig. 5.2** illustrates this concept.

This technique is also applicable for power amplifiers in mechatronic positioning systems, where actuator current noise is critical in the low-frequency

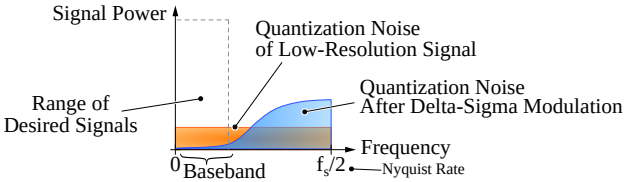

Fig. 5.2: Illustration of spectral densities of quantization noise of digital, sampled signals (sampling rate f_s), both with and without delta-sigma modulation. Quantization noise can be shifted to higher frequencies to obtain a low-noise baseband.

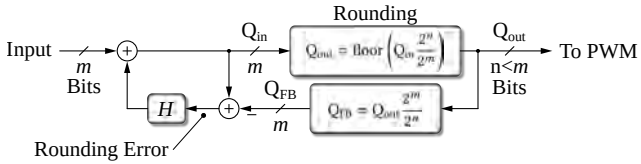

Fig. 5.3: Simplified noise shaping principle. The rounding error is fed back into the system whereas its frequency components are shaped by the transfer function H. Signals are binary and based on signed or unsigned fixed-point arithmetic.

baseband below ≈10 kHz. At higher frequencies, noise is generally negligible due to the sufficient attenuation of the motion systems at these frequencies, and a potentially employed amplifier output filter would also reject high-frequency noise.

The basic concept behind a noise shaping signal conversion system that is used to reduce the resolution of digital signals, and can provide low quantization noise in a certain baseband, is illustrated in **Fig. 5.3**. The digital reference input signal is based on binary fixed-point numbers (which can be signed or unsigned) and has a high amplitude resolution of m bits, whereas the low-resolution output, which, in the discussed application can be used as input for the subsequent pulse-width modulator, is generated by rescaling and truncating the input signal as indicated. This maps the input signal to the (smaller) range of the output signal. The integer nature of the output signal is preserved by rounding towards negative infinity, which is performed by the indicated floor function. This corresponds to the behavior of binary fixed-point numbers subject to sign-extended shift operations (see Sec. 5.2.1 below). In order to obtain the rounding error, the output Q_{out} is simply rescaled to the range of the input signal, with which the difference can be taken to obtain the desired quantization error. The error is fed back into the

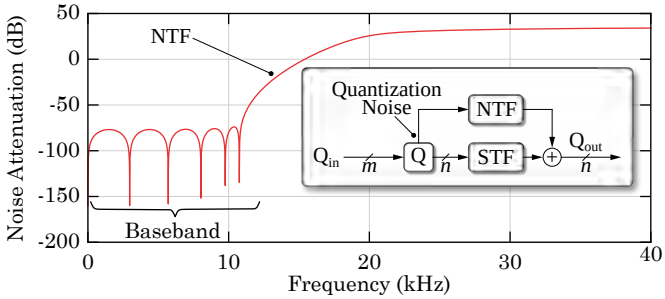

Fig. 5.4: Amplitude plot of an arbitrary noise transfer function (NTF) with 11 poles and 11 zeros. The high-pass characteristic shifts the quantization noise to higher frequencies. The signal transfer function is usually unity and does hence not affect the desired signal, whose resolution is being reduced by the noise shaping system.

system, which is only exemplarily illustrated in **Fig. 5.3**, and its spectrum is shaped by a transfer function H such that the quantization noise is significantly reduced in the low-frequency baseband. The output signal can be used with a corresponding pulse-width modulator that has a digital counter resolution of n bits. Consequently, the execution frequency of the digital noise shaper, f_{NS}, is identical to the update rate of the modulator, e.g., in the case of regular symmetric sampling [95], the noise shaper is executed with the PWM frequency f_{PWM}, as the modulator updates its reference once per PWM cycle.

The influence of a noise shaping system on its output can be described by two distinct transfer functions, which is enabled by the knowledge of the rounding error. The quantization noise behavior is described by the noise transfer function (NTF), whereas the influence of the noise shaper on the desired output signal is defined by the signal transfer function (STF) [96]. This concept is visualized by the block diagram in **Fig. 5.4**. These transfer functions are implemented by the internal structure of the noise shaper, whereas the STF is commonly selected to be unity, as the noise shaper should not affect the signal itself, only its quantization noise that results from the reduction of signal resolution. Consequently, a noise shaper does not introduce harmonic distortion. In the discussed applications, the quantization noise is attenuated in the baseband and shifted to higher frequencies. In the illustrated example of the NTF, the baseband ranges from DC to 10 kHz in which the rounding

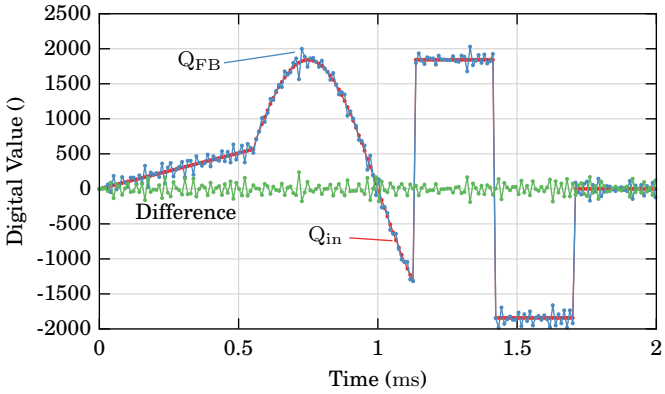

Fig. 5.5: Exemplary time-domain behavior of noise shaper signals. The input signal has an amplitude resolution of 12 bits and the output of the noise shaper is 9 bits wide. The output is rescaled (i.e., multiplied by 2^{12-9}) such that the input and output are directly comparable.

noise gets attenuated by ≈75 dB. At higher frequencies, the quantization noise increases, whereas the total noise energy is unchanged [96].

In order to illustrate the concept of a signal transfer function that is unity, **Fig. 5.5** depicts the simulated response of a noise shaper output signal to an arbitrary, varying input signal in the time domain. The ideal tracking performance of the noise shaper output and the lack of any dynamics corroborate STF = 1. The indicated difference is taken between the input and (rescaled) output, and it reflects the quantization error whose spectrum is shaped by the NTF.

As a noise shaper employs a feedback signal path, the system can potentially become unstable. Due to nonlinear processes common to digital signals, such as quantizer rounding, saturation or overflow effects, noise shapers can only be investigated to the full extent by using comprehensive numerical computer simulations that enable the assessment of their performance and stability with different input signals and amplitudes.

Noise shaping can be employed in different ways to obtain the switch control signals. **Fig. 5.6** illustrates two possible signal paths in a noise shaping modulation system. In the first option, the noise shaper outputs a low-resolution signal which is directly used as the switch control signal, e.g., a signal with a resolution of $k = 1$ bit in the case of a two-level (e.g., half-bridge (HB)) switching stage. Hence, the pulse-width modulator can be

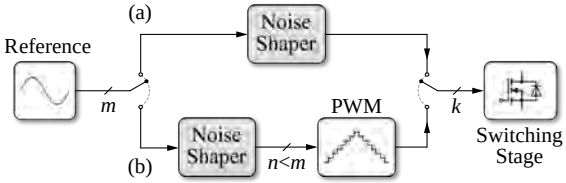

Fig. 5.6: Two possible signal paths in a digital, noise shaping modulation system for power electronic converters. **(a)** The noise shaper directly creates the switching signals. **(b)** The noise shaper feeds a pulse-width modulator.

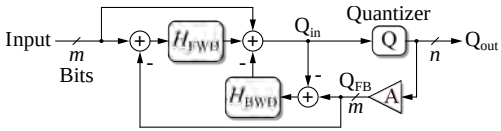

Fig. 5.7: The noise-coupled noise shaping structure (NCS) used in this work due to its suitability for digital designs. The transfer functions H_{FWD} and H_{BWD} define the noise and signal transfer functions.

omitted. In the other option, as illustrated in **Fig. 5.6 (b)**, the noise shaper forms an output signal with a resolution of several bits (e.g., $n = 8$), which is fed to a regular, counter-based modulator that creates the desired power switch control signals. However, the stability and performance of noise shapers with very low output resolutions (e.g., 1 bit as illustrated) is generally insufficient and hence, the approach in **Fig. 5.6 (a)** is discouraged [191, 192]. This is corroborated by computer simulations with different noise shaper topologies [96].

In the following, the structure of the noise shaper implementation chosen for this work, and its performance, are presented in detail.

5.2.1 Implementation Details

There is a noise shaping topology which is especially well suited for the use in digital systems, as the rounding error can be accurately determined and fed back, which improves stability. The structure is named noise-coupled noise shaper (NCS) and illustrated in **Fig. 5.7** [193–195]. The gain block A simply rescales the output such that the rounding error can be formed (cf. **Fig. 5.3**). The signal transfer function of this structure is STF = 1, whereas the NTF is

given by two transfer functions as follows:

$$\mathrm{NTF} = \frac{1 - H_{\mathrm{BWD}}}{1 + H_{\mathrm{FWD}}}. \tag{5.4}$$

Generally, a discrete-time NTF can be given in the frequency domain as [96]:

$$\mathrm{NTF}(z) = \frac{\sum_{k=0}^{N} b_k z^{-k}}{\sum_{k=0}^{N} a_k z^{-k}}. \tag{5.5}$$

By comparing the coefficients of the numerators and denominators of (5.5) and (5.4), the following terms result for the transfer functions that define the NTF:

$$H_{\mathrm{BWD}} = -\sum_{k=0}^{N} b_k z^{-k} + 1 = (-b_0 + 1) - b_1 z^{-1} - b_2 z^{-2} - \cdots - b_N z^{-N}, \tag{5.6}$$

$$H_{\mathrm{FWD}} = \sum_{k=0}^{N} a_k z^{-k} - 1 = (a_0 - 1) + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_N z^{-N}. \tag{5.7}$$

Thus, H_{FWD} and H_{BWD} can be implemented with digital FIR filters [196]. The order of the noise shaper is given by N, whereas higher-order noise shapers show a better noise suppression, but are more susceptible to unstable behavior [96].

Fig. 5.8 reveals details of the digital implementation of the NCS. The two required transfer functions are implemented with simple digital FIR filters that require few resources, as N is generally less than 15. The reduction in signal resolution is achieved by the division by 2^{m-n}, which corresponds to a binary right-shift of the digital data $m - n$ times, where the discarded least significant bits (LSBs) indicate the loss of signal precision. Likewise, the rescaled value $\mathrm{Q_{FB}}$ used to determine the rounding error is found by the corresponding binary left-shift operation, where the newly created LSB are set to zero.

In the following, numerical optimization is used to find an optimal and stable NTF for a given noise shaper configuration. This is done using computer simulations due to the nonlinear nature of the analyzed system.

5.2.2 Noise Shaper Optimization

The poles and zeros of the NTF, which is essentially a high-pass filter, can be optimally arranged such that the noise level is minimized in the desired

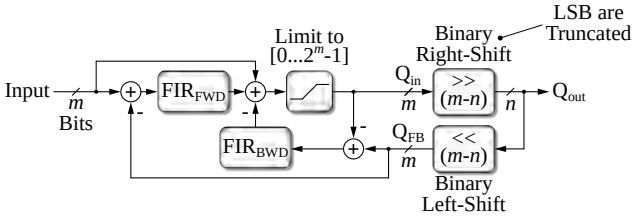

Fig. 5.8: Implementation details of the noise-coupled delta-sigma modulator. The limiter is illustrated for the case of unsigned signals, but the structure works equally for signed data, as long as the most significant bit is correctly padded during the binary right-shift operation to maintain the sign of the two's complement number.

baseband [96]. The order of the noise shaper is an additional degree of freedom which influences its performance. However, the stability of different NS configurations undergoing varying input signals must be assessed using computer simulations due to the inherent nonlinear nature of the noise shapers. Such optimizations and stability assessments are performed for the noise-coupled shaper considered in this work, with the aim of finding stable configurations with the best possible quantization noise suppression (i.e., the best achievable SNR) from DC to 10 kHz. The utilized method optimizes the order and placement of the zeros and poles of the NTF, numerically simulates the NCS structure with the selected NTF, checks for stability and evaluates the achievable SNR at the output signal Q_{out} [197, 198].

Fig. 5.9 illustrates the best achievable SNR of the noise-coupled shapers as found by this optimization routine, for different noise shaper execution frequencies f_{NS} and output resolutions n. The NTFs are designed by the optimization algorithm to achieve the best possible noise suppression from DC to 10 kHz for each investigated configuration. The orders of the noise shapers range from 7 to 14, and all indicated results represent a stable noise shaper for input signals with a modulation index of $m = 0.9$ (which is the amplitude normalized to the input signal range). This maximum modulation index at the noise shaper input is selected such that the noise shaper retains some headroom at the output that allows it to correct the quantization error. If the input signal exceeds this amplitude, the noise shaper usually becomes unstable and cannot recover. It is thus essential that the signal amplitude at the noise shaper input is limited appropriately. The optimization results indicate that naturally, higher output resolutions translate to less quantization noise and thus, a higher achievable SNR. The same holds for the noise shaper

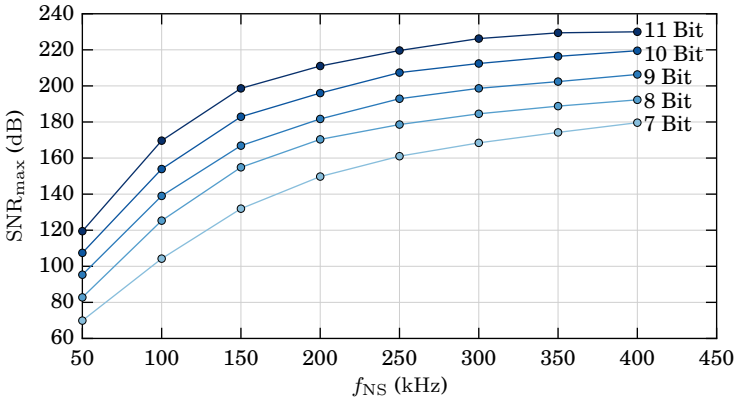

Fig. 5.9: Achievable SNR of stable noise-coupled shapers with different output resolutions n. The SNR is evaluated from DC to 10 kHz. The reference input is a 80 Hz sinusoidal signal with an amplitude resolution of 39 bits and a modulation index of $m = 0.9$. The noise shaper is executed with f_{NS}.

execution frequency f_{NS}, as a higher ratio of f_{NS} to the bandwidth of the baseband (i.e., the oversampling ratio) also enables a better performance [96].

5.2.3 Verification Measurements

The NCS structure presented above has been implemented in an FPGA in order to verify its performance. The small-scale demonstrator hardware presented in Sec. 4.2.3 is used, as it provides low-jitter (i.e., low-noise) gate drivers. Two GaN E-HEMT transistors (*GaN Systems GS66508T*) are connected to the two gate driver outputs to obtain a HB power stage that can provide low-noise and low-distortion output signals. The supply of the HB is provided by batteries (9 V) to minimize external noise sources.

The selected noise shaper for the verification has an order of $N = 11$ and an output signal resolution of $n = 9$ bit, which is identical to the resolution of the digital PWM counter, which counts with $f_{CLK} = 100$ MHz and thus, a PWM switching frequency of $f_{PWM} = 97.8$ kHz results (cf. (5.3)). The PWM input is updated once per PWM cycle and hence, the noise shaper execution rate is $f_{NS} = f_{PWM}$. The digital reference signal is sinusoidal with a fundamental frequency of 170 Hz and an amplitude resolution of 26 bits. A modulation index of $m = 0.85$ is selected to ensure the stability of the noise shaper (as shown in Sec. 5.2.2, the noise shaper is stable up to $m = 0.9$). Due to the

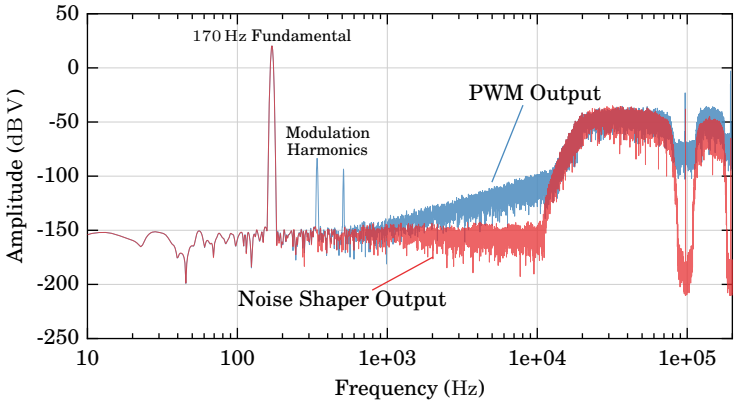

Fig. 5.10: Simulated amplitude spectra of the digital noise shaper output signal and the 1-bit binary PWM output. The spectra are rescaled in amplitude to match the fundamentals. The NS output achieves an SNR of 137.9 dB, which is reduced in the PWM output signal to 97.8 dB due to intermodulation distortion. The THD of the PWM signal is −103.5 dB.

intended application in mechatronic systems, the NTF is optimized to achieve a low-noise baseband from DC to 10 kHz. The reference signal is provided with f_{NS} to the noise shaper input in order to eliminate the need for an upsampling and interpolation stage.

Fig. 5.10 shows the computer simulated amplitude spectra of both the 9-bit noise shaper output signal and the binary PWM output. The spectra are rescaled such that the fundamentals match in amplitude. At frequencies above 10 kHz, the quantization noise increases significantly, as designed. The SNR of the noise shaper output signal is 137.9 dB (DC to 10 kHz), whereas the theoretically achievable value with a 9-bit signal in this bandwidth is given, using (5.1), as

$$\mathrm{SNR} \approx 6.02 \cdot 9 + 1.76 + 10 \log_{10}\left(\frac{f_{\mathrm{PWM}}/2}{10\,\mathrm{kHz}}\right) \approx 62.8\,\mathrm{dB}, \tag{5.8}$$

which takes the reduced bandwidth into account (the quantization noise is evenly distributed from DC to $f_{\mathrm{PWM}}/2$) [88]. Note that the spectrum of the PWM output signal contains two harmonics that originate from the regularly sampling PWM, which is slightly nonlinear (the THD is −103.5 dB in this example) [95]. The amplitudes of these harmonics depend on the ratio of the PWM frequency to the fundamental frequency [95]. Pre-distortion

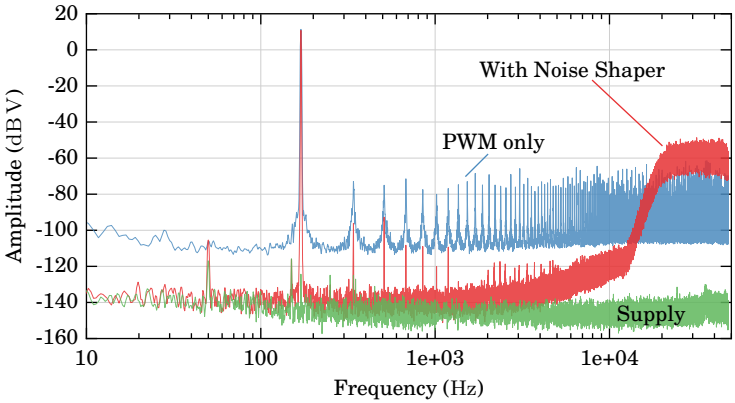

Fig. 5.11: Voltage spectra measured at a switched HB output (which replicates the PWM output), operated with and without the noise-coupled noise shaper. The supply spectrum is measured at the DC supply of the HB. The SNR with the noise shaper reaches 97 dB, whereas the regular PWM method only achieves 65.8 dB.

techniques can potentially be used to reduce these harmonics [114, 115, 199]. However, such methods are often complex and offer limited performance gains. Furthermore, other nonlinear effects in a realistic amplifier setting, such as HB dead time, generally dominate these harmonics. The nonlinear pulse-width modulator also causes the noise floor of the PWM output signal to rise at frequencies lower than 10 kHz. This is an effect caused by intermodulation distortion (IMD) at the modulator's nonlinearity, which leads to high-frequency noise being folded back into the baseband [105, 114, 200]. The mentioned pre-distortion techniques can potentially also mitigate this effect. Furthermore, this IMD is significantly increased when using asymmetric regular sampling of the modulator (i.e., the PWM reference is updated twice per PWM cycle instead of only once), which increases the noise of the PWM output signal in the baseband. This is due to the fact that this sampling method increases the modulator's nonlinearity, as compared to regular symmetric sampling where the reference is only updated once per PWM period, and is thus not employed [95]. Regarding noise, the SNR of the PWM output in this example is 97.8 dB (DC to 10 kHz), which is still significantly higher than what a regular pulse-width modulator, whose performance is compared in the following, can achieve (see (5.8)).

Fig. 5.11 depicts a measurement performed with the hardware demonstrator at the switched HB voltage output, using a precision audio analyzer (*R&S UPV*) [183]. Note that the HB switching stage is simply used to recreate the digital PWM output with a low-noise voltage signal in order to measure it. If only a regular 9-bit modulator is used without noise shaping, the quantization noise is significant and the SNR in the baseband from DC to 10 kHz is only 65.8 dB, which matches with the approximation in (5.8). As expected from the simulation results, the noise shaper considered in this experiment can increase this figure to 97 dB, which is very close to the simulated value of 97.8 dB. There are, however, more harmonics in the noise-shaped spectrum than predicted by the simulations. This is due to the nonzero switching times of the power transistors, dead time and the nonideal supply (see Sec. 2.3). The THD of the noise-shaped signal is −102 dB (considering only the first two harmonics), which is also a close match with the simulation. Note that an RMS jitter of ≈25 ps is still present in the switched output waveform, despite using the low-jitter gate drivers. This limits the best achievable SNR in the 10 kHz baseband to ≈107 dB (see Sec. 4.1), which defines the limit for the achievable SNR with this setup.

In order to compare the measurement with the simulation, **Fig. 5.12** shows the power spectral densities of the measured signal and the simulation, which allows a direct comparison of the noise levels, as the measured spectra are obtained with a different FFT window and length [90]. At frequencies from DC to ≈2 kHz, the noise floor of the measurement is higher than what the simulation suggests due to the remaining HB RMS jitter of ≈25 ps and noise from the HB DC supply. Otherwise, the measurement matches well with the simulation, which verifies the expected functionality.

This investigation utilizes an open-loop power stage, i.e., there is no feedback control involved, which could also attenuate the PWM quantization noise. This is done to be able to analyze the effectiveness of the ΔΣ modulator. The impact of the noise shaper in a closed-loop amplifier system is presented in Sec. 7.6.2 with a full-scale power amplifier system.

5.3 Summary

The limits of digital PWM with respect to the achievable output noise are outlined. The discrete digital counter used for the modulation quantizes the duty cycle of the switch control signal, which introduces undesired wideband quantization noise. Sufficient noise levels could be achieved if it was possible to operate a high-resolution PWM counter with a frequency of several GHz,

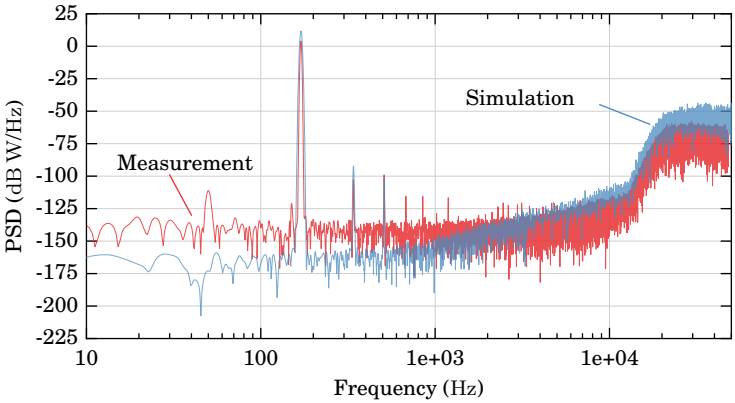

Fig. 5.12: Power spectral densities of the measured HB output and the corresponding computer simulation. Reference impedance: 1 Ω.

which is infeasible with state-of-the-art technology. Other approaches, such as analog modulators or high-resolution PWM techniques based on delay lines, or digital serializers, also achieve an insufficient performance.

Consequently, digital ΔΣ modulation (noise shaping) is presented in the context of the power electronic switching stage. This simple signal processing technique is capable of shifting quantization noise to higher frequencies by considering the rounding error that results from a reduction of signal amplitude resolution. Thus, a regular limited-resolution pulse-width modulator can be utilized, which then achieves low-noise output signals in the critical baseband (i.e., DC to 10 kHz for the discussed mechatronic power amplifiers).

A noise shaping topology, the noise-coupled noise shaper, is well suited for digital-to-analog conversion, as it is capable of accurately determining the rounding error of the quantizer. Its simple digital implementation, whose main complexity is covered by two FIR filters, is presented in detail. The structure is numerically optimized with respect to noise attenuation and stability, which determines the achievable performance for different configurations (i.e., PWM frequencies and modulator amplitude resolutions).

Measurements are presented on a small-scale, open-loop demonstrator, which match well with numerical simulations. The selected 9-bit noise shaper, executed at a rate of 100 kHz, is able to improve the SNR of the pulse-width modulated HB output voltage by more than 30 dB to 97.8 dB. The performance can be further increased with higher execution frequencies or PWM resolu-

tions. This demonstrates the effectiveness of the presented method, as it is capable of eliminating a significant source of noise in any digital pulse-width modulated power converter.

6

Precision Voltage and Current Sensors

Closed-loop feedback control systems require flawless sensors that precisely acquire the desired signals in a given frequency band. If noise or other unwanted signal components are added to measurements, feedback systems treat them like reference input signals and thus, introduce them to the controlled physical systems. Similarly, if measurements do not reflect the entire signal content, the control systems cannot reject potential errors.

In power electronic converters, current sensors commonly feature bandwidths into the megahertz range and measure currents of tens of ampere. Similarly, the voltages that need to be acquired in such systems can also be in the range of several hundred volts. However, the output signal of any voltage or current sensor is usually a voltage with only several volts of magnitude, that is subsequently processed with common signal electronics or analog-to-digital converters (ADCs). Thus, such elements are an integral part of any acquisition system and are also considered in this chapter, which deals with the analysis of all relevant sensor system components.

First, **Sec. 6.1** investigates noise and distortion of commonly used current sensors. The linearity of shunt resistors is analyzed with a detailed thermal simulation as well as a simplified approximation. Next, integrated isolated current sensors are evaluated with a low-distortion linear current source, which reveals their insufficient noise and distortion performance for precision feedback systems. Similarly, **Sec. 6.2** presents the noise of high-voltage dividers that are used to measure voltage levels up to several hundred volts. **Sec. 6.3** then analyzes the linearity and noise of operational amplifiers, which are key components of analog signal paths, as they can be employed flexibly as amplifiers, buffers or filters. As a digital control system is considered for

the power amplifiers in this thesis, **Sec. 6.4** presents a method to reduce the quantization noise of ADCs, based on oversampling. The required digital low-pass filter is optimized with respect to its delay, which is critical as it potentially resides in the feedback path of a control system. If the ADC is placed on an isolated potential, its sampling jitter must be considered as it is a significant source of noise, which is revealed in **Sec. 6.5**. The investigation considers a half-bridge (HB) current measurement setup and consequently, a design guide for its filter inductor with respect to the ADC sampling jitter is given.

6.1 Current Sensors

Different types of current sensors are commercially available and widely utilized in power converters for feedback control or supervision. They can be divided into galvanically isolated or nonisolated types, whereas the latter usually comprise methods using shunt resistors, and the former employ different effects and technologies such as magnetic cores with Hall effect sensors or transducers based on the giant magnetoresistive effect, to name a few [201, 202]. However, consistent linearity or noise data is hardly available for any type of sensor. Hence, this section analyzes different current sensors with respect to these properties. Suitable types for low-noise and low-distortion power amplifiers in mechatronic positioning applications, where the load current quality is particularly critical, are identified.

6.1.1 Shunt Resistors

A shunt resistor provides a simple means of measuring a current, as the voltage drop across it is, ideally, proportional to the resistor current i_S. Furthermore, the intrinsic noise of shunt resistors is generally negligible due to the small resistance values that are selected to limit thermal losses and distortion, as shown in this section [93].

Consequently, the noise of a shunt-based current sensor is generally dominated by subsequent amplification or filtering circuits, which necessitates low-noise analog designs. For example, an amplifier based on operational amplifiers (op-amps) with a voltage gain of 10 can be designed with a total output voltage noise of ≈30 µV RMS in the respective bandwidth of the subsequent analog ADC front-end (e.g., 500 kHz in this example), as illustrated in **Fig. 6.1** [84]. Assuming a shunt resistance value R_S of 20 mΩ and a current of 20 A RMS, an SNR at the output of the amplifier of 102.5 dB results, which

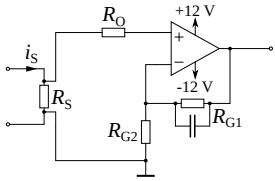

Fig. 6.1: Amplifiers for shunt voltages require low-noise designs. Exemplary configuration for an amplifier with a gain $G \approx 10\,\mathrm{V/V}$ and a total output noise of 30 µV RMS in a 500 kHz bandwidth: Op-amp: *LT1028A*, $R_{G1} = 2940\,\Omega$, $R_{G2} = 324\,\Omega$, $R_O = 294\,\Omega$ (used for op-amp offset current compensation).

can be further increased by using a shunt resistance of higher value. Additionally, by reducing the bandwidth (i.e., attenuating high-frequency noise), which is done in an oversampled ADC system as shown in Sec. 6.4, the SNR is further increased.

To prevent harmonic distortion, the shunt resistance R_S cannot be increased arbitrarily. As most resistive materials show a temperature dependence of R_S, the shunt voltage $u_S = R_S i_S$ also depends on the associated thermal loss $p(t) = R_S i_S^2(t)$, as it alters the shunt temperature T_S. However, T_S is considerably influenced by the thermal impedance from the resistive element to the ambient [203].

Thus, in order to comprehensively investigate the linearity of a shunt resistor, the thermal system has to be considered. In a first step, 3D FEM models of different shunt resistors are used to identify their thermal capacitances and resistances, which results in their thermal equivalent circuit. Next, numeric computer simulations that include the identified thermal models are performed in order to evaluate the linearity of the investigated resistors. This approach allows to take the nonlinear interactions between the instantaneous power loss in the resistor and the thermal behavior of the resistive material, including its thermal capacitance and resistance, into account. This approach is similar to the method used in Sec. 3.2, where the linearity of different power transistors is determined.

Resistor Thermal Model

3D FEM simulations are used to identify the relevant thermal properties of the considered shunt resistors. **Fig. 6.2** illustrates the thermal model. The resistive element of the shunt is assumed to be a thin foil of *Manganin* alloy, mounted on an electrically isolating substrate. This is a common resistive material for

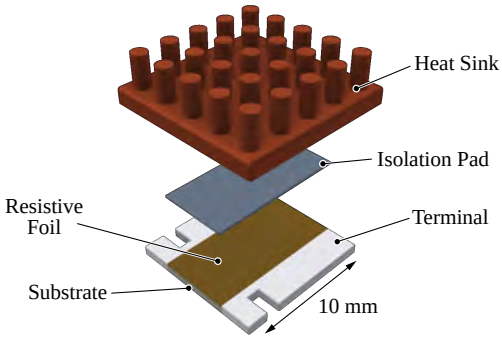

Fig. 6.2: Thermal configuration of the shunt resistor. The resistive element is mounted on a substrate and is cooled with a heat sink through an electrically isolating pad. This figure illustrates a *CSM3637* resistor [205].

shunts due to its nearly constant thermal coefficient of resistance [204]. The dimension of the foil is given by the size of the shunt resistor's package and its thickness is set such that the desired resistance is obtained. In order to limit the temperature variation of the shunt (which increases its linearity), a heat sink is used to cool the resistive element through an electrically isolating, thermally conductive isolation pad. In the FEM simulation, a power loss step is applied to the resistive foil and its temperature is recorded. From the resulting temperature step response, the thermal model is identified [137]. This is done identically in Sec. 3.2.2 for power transistors and their cooling solutions. It is assumed that the heat sink is held constantly at T_a which, due to its comparably large thermal capacitance, holds. The material characteristics of the isolation pad are identical for each simulation and its dimension is given by the size of the resistive foil, except for its thickness, which is fixed at 0.4 mm. **Tab. 6.1** lists thermal properties of *Manganin* and the isolation pad. The thermal behavior of the substrate is not considered, as its material is generally not known. However, its thermal capacitance would only reduce the temperature variation of the resistive foil and thus, the employed approach potentially overestimates the distortion of the shunt resistors.

Tab. 6.2 lists the shunt resistors that are investigated in this analysis. Various resistor package sizes (that correspond to different masses of the resistive foils) are chosen in order to demonstrate the effect of different thermal characteristics. The resistance values are selected to reflect commonly used values in applications with currents ranging from ≈1 A to 30 A.

Tab. 6.1: Thermal properties of *Manganin* and the considered isolation pad, as implemented in the FEM simulation.

Material	κ (W/(m K))	C (J/(kg K))	σ (25 °C) (S/m)	ρ (kg/m^3)
Manganin	22	410	2.33×10^6	8400
Isolation Pad	1.0	880	–	2500

Tab. 6.2: Evaluated shunt resistors. The resistive element is assumed to be *Manganin* and its thickness t is chosen such that the desired resistance value results, given the element's length l and width w.

Type	R_S (mΩ)	Resistive Element Dimension $l \times w \times t$ (mm)
CSM2512 [205]	10	$4.8 \times 3.2 \times 0.065$
CSM3637 [205]	5	$4.8 \times 9.4 \times 0.044$
	10	$4.8 \times 9.4 \times 0.022$
	50	$4.8 \times 9.4 \times 0.0044$
SMD 1206	10	$3.0 \times 1.6 \times 0.0806$
Burster 1282 [206]	10	$300 \times 20 \times 0.645$

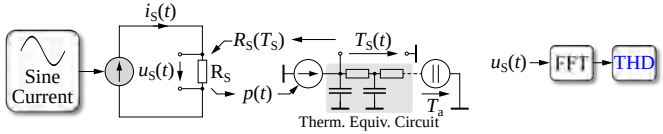

Fig. 6.3: Simulation setup to determine the linearity of the shunt resistor R_S. The thermal equivalent circuit is identified using thermal FEM simulations.

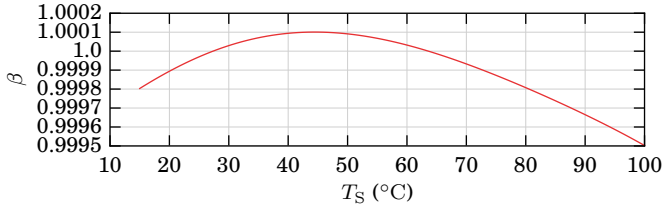

Fig. 6.4: Temperature coefficient of the alloy *Manganin*, which is commonly used for shunt resistors. $R = R_{\text{nom}}\beta$.

In the following, the identified thermal impedances Z_{ST} of each shunt are used to determine the shunt linearity in numerical simulations.

Linearity Simulation

A computer simulation is used to identify the distortion of different shunt resistors, including their thermal models that are identified in the previous section. **Fig. 6.3** illustrates the simulation approach. The considered shunt resistors are listed in **Tab. 6.2**. Additionally, **Fig. 6.4** illustrates the thermal coefficient of resistance of *Manganin* as incorporated in the thermal simulation software [129]. The resistor current is sinusoidal, $i_S(t) = \hat{i}_S \sin(2\pi f_F t)$, and naturally, the output of the simulation model is the shunt voltage $u_S(t)$. From this voltage, the THD is determined via the fast Fourier transform (FFT). In each simulation time step, the momentary shunt resistor loss $p(t)$ is supplied to the thermal model (implemented as an equivalent circuit), which returns the shunt temperature T_S. Consequently, the instantaneous shunt resistance R_S and thus, u_S, are given in each simulation step.

Fig. 6.5 visualizes the best achievable THD for the considered shunts. Two different simulations are performed. In **Fig. 6.5 (a)**, the frequency f_F of the sinusoidal shunt current is fixed at 10 Hz and the current amplitude is swept. In **Fig. 6.5 (b)**, the RMS current is fixed at 1 A and the frequency

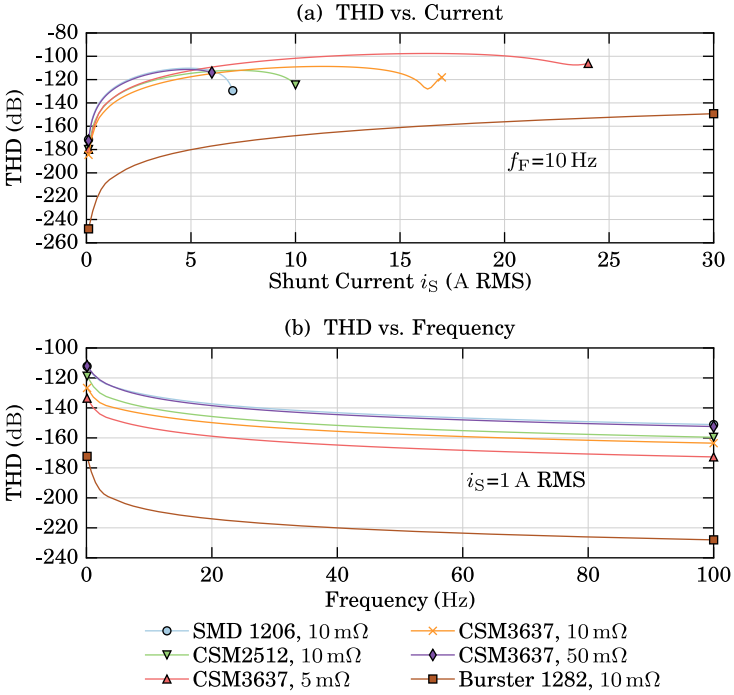

Fig. 6.5: Achievable THD of the investigated shunt resistors, limited by the self-heating of the resistive foils. **(a)** Frequency of the reference current fixed at 10 Hz. **(b)** Shunt current amplitude fixed at 1 A RMS. T_a = 25 °C.

is varied. The maximum currents are selected such that the loss ratings of the individual resistors are not exceeded. At increased current amplitudes, it is possible for the THD to improve again. This is due to the fact that the temperature of the resistive element approaches ≈45 °C, at which its thermal coefficient of resistance is nearly constant (cf. **Fig. 6.4**). Furthermore, at higher fundamental current frequencies f_F, the linearity improves. This is expected because the thermal capacitances present less impedance at higher frequencies, which reduces the thermal variation.

The results demonstrate a sufficient linearity for the investigated shunt resistors, as their THD is generally less than −110 dB at low currents. The large *Burster 1282* resistor shows the best performance, as its resistive element is extensive and well cooled. Due to the lack of a detailed knowledge of

shunt resistor constructions, this analysis does not include the electro-thermal properties of the interface between the shunt resistor terminals and the resistive foil itself, which, due to the usage of different materials at different temperatures, can give rise to voltage drops that affect the shunt linearity negatively [207]. Furthermore, manufacturers potentially use different resistive materials than the analyzed *Manganin*, which can also be arranged with a different geometry than the considered uniform foil. Nonetheless, the presented analysis gives an approximation of the achievable distortion performance of shunt resistors.

Assuming a purely resistive thermal impedance $Z_{ST} = R_{ST}$, a simpler estimation of the THD can be obtained, as shown in the following.

Shunt Model Considering Only a Thermal Resistance

The shunt voltage u_s can be given with a simple analytical expression, assuming a constant thermal resistance R_{ST} from the resistive element to the ambient (and neglecting thermal capacitances), such that $T_S(t) = p(t)R_{ST} + T_a$, where $p(t) = R_S i_S^2$. With a linear thermal coefficient of resistance α such that

$$R_S = R_{nom}(1 + \alpha(T_S - T_a)), \tag{6.1}$$

the shunt voltage $u_S = R_S i_S$ is then given as

$$u_S(t) = \frac{R_{nom} i_S(t)}{1 - \alpha R_{nom} R_{ST} i_S^2(t)}. \tag{6.2}$$

This expression can be employed in a numerical analysis by considering a sinusoidal shunt current i_S and evaluating the integer harmonics of u_S. For example, with a sinusoidal current $i_S(t) = 10\,\mathrm{A}\sin(\omega t)$, and $R_{ST} = 2\,\mathrm{K/W}$, $\alpha = 2 \times 10^{-6}$ and $R_{nom} = 10\,\mathrm{m\Omega}$, which are values achieved by commercial shunt resistors, the resulting THD of u_S is $-120\,\mathrm{dB}$ [208]. This is in the same range as the results from the 3D FEM simulations, which corroborates the accuracies of the approximations. In reality, the thermal capacitances neglected for this simplification further improve this result, as they limit the shunt's temperature variation.

Shunt Resistors Summary

With low-noise analog amplifiers used to process the voltage drop of shunt resistors, it is possible to obtain high-bandwidth (several hundred kilohertz) current measurements with SNR values in excess of 100 dB, that can be further

improved when the bandwidth of the measured signal is reduced, e.g., by downsampling and decimation (see Sec. 6.4).

The thermal coefficient of resistance, although usually small for shunt resistors, gives rise to harmonic distortion. Two analysis methods are used to investigate the linearity of current sensing shunt resistors. Both approaches reveal that shunts can achieve sufficiently low inherent distortion figures with current levels common in precision power amplifiers for mechatronic applications. The estimated THD figures are below ≈ -110 dB, which is similar than what the subsequent signal processing systems (e.g., analog amplifiers or filters) can achieve (see Sec. 6.3).

Thus, a shunt resistor provides a simple and effective method to obtain a current measurement of very low noise and distortion. A potential disadvantage is the missing galvanic isolation of the measurement circuit, which is often desired in power electronic converters. Consequently, the following section investigates the performance of isolated current sensors.

6.1.2 Integrated Isolated Current Sensors

If a galvanically isolated current measurement is required, a substantial variety of sensors is available. These sensors regularly include integrated processing electronics and the underlying sensing principle often relies on magnetic effects [201, 202]. For example, in open-loop type current sensors, the magnetic flux density in a sensing core is measured using a Hall effect sensor and directly used as output signal. Similarly, closed-loop sensors can employ an additional winding to actively drive the core flux to zero, which is expected to result in a more linear sensor. Unfortunately, there is typically no consistent distortion data of such sensors available and hence, the following analysis investigates noise and distortion of different types of galvanically isolated current sensors, as listed in **Tab. 6.3**.

Therefore, a precision linear current source is used to provide a sinusoidal reference current for the investigated sensors. Their output signal frequency spectra are then evaluated to determine the THD and SNR. **Fig. 6.6** depicts the schematic of the utilized source. An industrial linear voltage amplifier (*AE Techron 7224*) provides the reference current i_{Ref}. An analog feedback system, comprising a low-distortion shunt resistor R_{Ref} (*Burster 1282*, 10 mΩ) and a type-III (lead-lag) compensator, is used to attenuate harmonics and noise in i_{Ref} that originate from the nonideal power amplifier. R_{L} is used to bias the power amplifier into a suitable operating point (i.e., stable and low harmonics). The low-distortion reference signal u_{Ref} is provided by a

Tab. 6.3: Isolated current sensors with different sensing principles such as the anisotropic magnetoresistive effect (AMR) or open/closed-loop (OL/CL) circuits involving Hall effect sensors. The fluxgate principle excites a magnetic core and utilizes its saturation in combination with compensation windings [202]. f_{BW} is the sensor measurement bandwidth. Linearity is the integral nonlinearity error, i.e., the max. deviation from the ideal transfer curve, as given by the datasheet.

Nr.	Ref.	Technology	Output Type	I_{nom} (A RMS)	f_{BW} (kHz)	Linearity (% I_{nom})
1	[209]	AMR, CL	Voltage	15	200	±0.1
2	[210]	AMR, CL	Current	15	400	±0.2
3	[211]	Hall, OL	Voltage	20	50	±1
4	[212]	Hall, CL	Voltage	15	200	< 0.1
5	[213]	Hall, CL	Current	25	200	< 0.2
6	[214]	Fluxgate, CL	Current	60	800	±0.0001

high-precision FFT spectrum analyzer, which is also used to measure the THD and SNR of the amplified shunt voltage $u_{S,A}$ and the current sensor output voltage u_{Sens} [183]. The shunt resistor R_{Ref} is, like the employed operational amplifiers (*LT1028A*), highly linear (see Sec. 6.1.1 above and Sec. 6.3.1 below).

Fig. 6.7 illustrates the THD (first 4 harmonics considered) and SNR (in a frequency band from 100 Hz to 20 kHz) of the different sensor output voltages u_{Sens} as a function of the measured sinusoidal current. The fundamental current frequency is 35 Hz, which is in the range of common precision mechatronic actuator frequencies. Furthermore, the integer sensor output signal harmonics do not overlap with harmonics of the 50 Hz grid that are present in the reference current spectrum due to the insufficient power supply rejection of the linear power amplifier.

The measurements show that the investigated current sensors can achieve a THD of no less than ≈−90 dB, whereas their output SNR is also significantly reduced. For the sake of completeness, the same current source was also used to investigate different shunt resistors. As expected from the analysis in Sec. 6.1.1, neither THD nor SNR of the shunt output voltage are affected. Note that for this measurement, the fluxgate sensor was operated, like the other sensors, with only one primary winding. By using multiple turns and also optimizing its burden resistance, its performance can be increased to higher values than determined here, which is shown in Sec. 7.5. Furthermore,

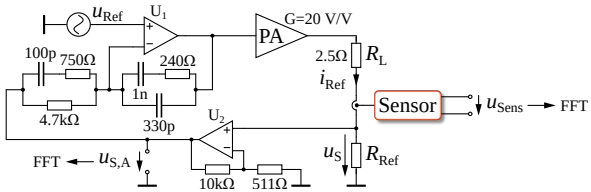

Fig. 6.6: Precision linear current source with analog closed-loop control. U_1 operates as a type-III compensator to reduce the distortion of the commercial linear power amplifier. U_2 provides the amplified feedback signal $u_{S,A}$. All op-amps are *LT1028A* and the reference shunt R_{Ref} is highly linear.

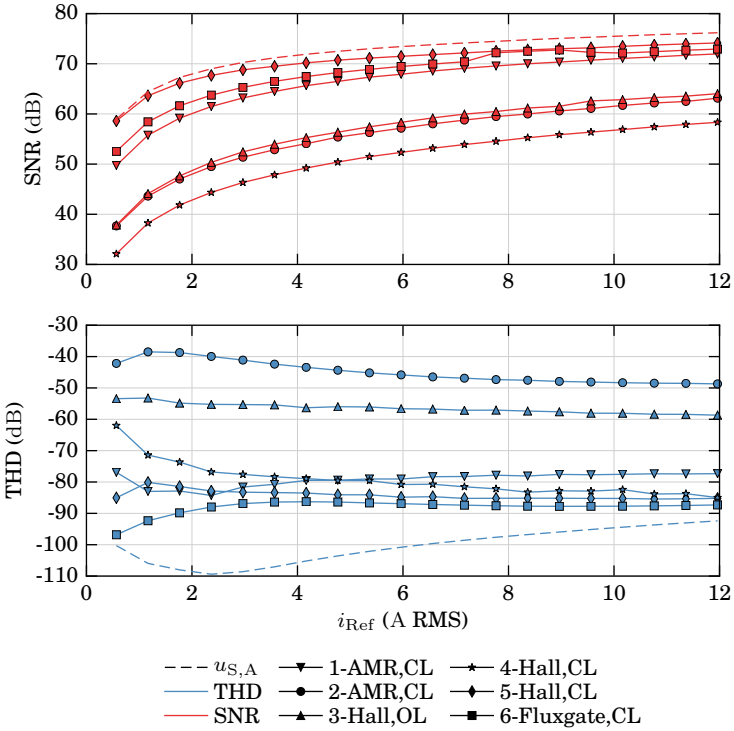

Fig. 6.7: THD (first 4 harmonics) and SNR (100 Hz–20 kHz) of different galvanically isolated current sensors as listed in **Tab. 6.3**. A low-distortion linear current source supplies the reference current (indicated with $u_{S,A}$, cf. **Fig. 6.6**).

this sensor is, compared to the others, considerably larger in volume, which is also reflected in its cost.

Consequently, if an application such as the discussed power amplifiers requires current measurements of low noise and distortion, shunt resistors should be utilized, as they deliver a superior performance over integrated, galvanically isolated sensors.

6.1.3 Summary

Shunt-based current sensors are characterized by low inherent noise due to the generally small resistance values and the availability of low-noise analog circuits used to amplify or filter the shunt voltages. However, the analysis of their linearity requires the consideration of the resistor's thermal behavior, as the temperature-dependent resistance variation introduces harmonic distortion. Consequently, thermal models of selected shunt resistors are extracted using 3D FEM simulations and employed in conjunction with computer simulations to determine the linearity of current sensing resistors. It is revealed that a THD of less than −110 dB can be achieved, given a sufficiently low thermal coefficient of resistance, which is commonly the case for shunt resistors intended for current sensing applications.

Distortion data of integrated, isolated current sensors, which are convenient to use in power electronic setups due to their inherent galvanic isolation, is rarely consistently available. Therefore, a low-distortion linear current source is used to analyze different devices. It is revealed that their output signal noise and distortion is insufficient for the application in precision feedback systems. Hence, shunt resistors must be used to acquire currents with low noise and distortion.

6.2 High-Voltage Resistive Dividers

Voltage signals with magnitudes in excess of several volts are commonly processed with resistive dividers, as most signal processing elements (e.g., op-amps or ADCs) operate with signal voltages below ≈12 V. If the power dissipation of the utilized resistors and hence, their resistance variation is kept low (i.e., several milliwatts), such dividers achieve a sufficiently high linearity, which can be verified with the approximation of the resistor's thermal behavior by a thermal resistance, as presented for the shunt sensing resistors at the end of Sec. 6.1.1.

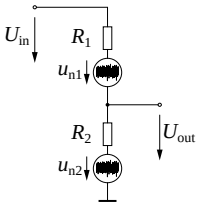

Fig. 6.8: Noise model for a resistive divider used to determine the achievable SNR at the output. Resistor noise is modeled with series-connected voltage sources.

However, with sensing voltages in the range of several hundred volts, high resistance values are required to reduce the thermal loss power. This can introduce considerable electrical noise by the resistors themselves, which mainly expresses itself as thermal noise and excess/flicker noise [93]. The achievable SNR at the output of a resistive divider is then limited. **Fig. 6.8** illustrates the noise model of such a circuit arrangement. The RMS voltage noise at the output of the divider is given by [93]

$$u_{\mathrm{no}} = \sqrt{\frac{(R_2 u_{\mathrm{n1}})^2 + (R_1 u_{\mathrm{n2}})^2}{(R_1 + R_2)^2}}, \tag{6.3}$$

where u_{n1} and u_{n2} are the corresponding resistor RMS voltage noise sources that consider excess noise u_{ex} and thermal noise u_{th}, in a bandwidth that spans from f_1 to f_2 (with $f_{\mathrm{BW}} = f_2 - f_1$), as follows:

$$u_{\mathrm{n1,2}} = \sqrt{u_{\mathrm{ex}}^2 + u_{\mathrm{th}}^2}, \tag{6.4}$$

$$u_{\mathrm{ex}} = 1 \times 10^{-6} 10^{\mathrm{NI}/20} u_{\mathrm{R_{1,2}}} \sqrt{\log_{10}(f_2/f_1)}, \tag{6.5}$$

$$u_{\mathrm{th}} = \sqrt{4kTR_{1,2} f_{\mathrm{BW}}}, \tag{6.6}$$

where NI is the resistor noise index in dB [93, 215], u_{R} the voltage across the resistor, k the Boltzmann constant, T the temperature in Kelvin, and R the resistance value. The noise index is a method to quantify excess resistor current noise [93, 215]. If several resistors are connected in series, their noise voltages u_{n} are to be added using the root of the sum of the squares of the individual voltages to obtain the voltage of the equivalent noise source. Consequently, the best achievable SNR at the output of the resistive divider is given as

$$\mathrm{SNR}_{\mathrm{div}} = 10 \log_{10} \left(\frac{U_{\mathrm{out}}^2}{u_{\mathrm{no}}^2} \right). \tag{6.7}$$

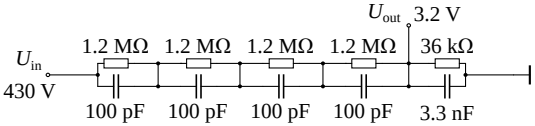

Fig. 6.9: A compensated high-voltage divider with an SNR of 119.9 dB and a maximum power loss of 10 mW per resistor.

Fig. 6.9 exemplarily illustrates a frequency-compensated divider that allows the measurement of voltages up to 440 V with signal processing circuits operating at 3.3 V. The divider achieves an output SNR according to (6.7) of ≈119.9 dB (DC–10 kHz), whereas a resistor noise index of NI = −10 dB is assumed, which is worse than what can be expected for common metal film resistors. This provides some margin, as this figure can significantly vary between different resistors and manufacturers [93, 215]. The linearity of the divider is ensured by the low thermal dissipation of less than 10 mW per resistor. Furthermore, the parallel capacitors are used to dominate parasitic capacitances such that the divider achieves a flat frequency response in a wide bandwidth [216]. Note that these capacitors, in combination with the resistors, limit the noise bandwidth, which further improves the SNR of the divider (the noise in RC arrangements is described as $^{kT}/_{C}$ noise [93, 217]).

The divider output voltage is commonly buffered by an op-amp before it is applied to the input of an ADC, due to the high impedance of the divider. Despite the fact that the measured voltages are often only unipolar (e.g., an AC signal with a DC offset), it is important that the buffer op-amp is supplied with a symmetric bipolar voltage with respect to signal ground, e.g., ±5 V, in order to prevent harmonic distortion, which is otherwise considerable, even in op-amps advertised for the usage with unipolar supply voltages. Furthermore, high-impedance dividers are susceptible to EMI, which can require the placement of an electromagnetic shield to prevent the pickup of faulty signals.

6.3 Analog Amplifiers and Filters

Analog-to-digital converters are ubiquitously used to transfer measurements of physical quantities such as voltages or currents into the digital domain, where the acquisitions are processed (e.g., filtered or analyzed) with more flexibility, robustness and less cost as it would be possible with analog signal processing circuits. Nonetheless, some analog circuitry is often still

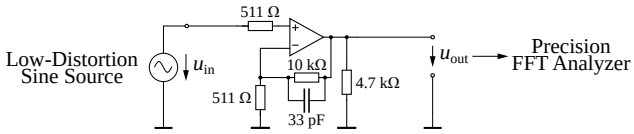

Fig. 6.10: Noninverting amplifier circuit for the evaluation of different op-amp devices. The supply voltages are symmetric with respect to ground and set according to the datasheet specifications (e.g., ±15 V). The input signal source and FFT analyzer are provided by a *Rohde&Schwarz UPV Audio Analyzer*.

required to convert the measured signals into suitable amplitude ranges for the subsequent ADC systems and/or to modify their spectral content. This is conveniently achieved using operational amplifiers, which are key circuit components of amplifiers, filters and signal buffers. Consequently, their noise and distortion performance in the context of widely used amplifier and filter circuits is analyzed in the following.

Noise in op-amp circuits is regularly modeled with equivalent voltage or current sources, which enables traditional circuit analysis methods [93]. Additionally, the noise performance of op-amp circuits can generally be determined from manufacturer datasheets. Furthermore, common circuit simulation software (e.g., SPICE) can also offer the capability to analyze circuit noise. Due to the wide availability of low-noise op-amp devices and the good understanding of the underlying noise models, it is generally possible to design analog amplifier or filter circuits of sufficiently low noise, as it was demonstrated for the shunt amplifier in Sec. 6.1.1, and is also shown later in Sec. 6.3.2 for the case of an anti-aliasing filter. However, the linearity of op-amps is generally not conveniently established, as shown in the following.

6.3.1 Operational Amplifier Linearity

In contrast to op-amp noise, harmonic distortion in their outputs signals is caused by a multitude of nonlinear effects that depend on the internal construction of the devices, the external circuit configuration, or input and output impedances [218]. Furthermore, manufacturers often provide no consistent data or measurement methods. These factors render the design of op-amp-based circuits with regard to their linearity inherently more difficult than their noise analysis.

Therefore, the linearity of different precision op-amp devices, employed in a common noninverting amplifier configuration, is evaluated experimentally

with the aim to determine the achievable THD. **Fig. 6.10** illustrates the utilized circuit. The gain $G = u_{\text{out}}/u_{\text{in}}$ is fixed at 20 V/V. The input signal is provided by an ultra-low-distortion sinusoidal signal generator (THD ≈ -120 dB), which is incorporated in a precision FFT analyzer that is also used to evaluate the distortion of the output voltage u_{out} [183]. Note that the noninverting amplifier configuration is more susceptible to distortion than the inverting variant, as both op-amp inputs swing with the input signal, which changes the operating point of the op-amp input stage, whereas in the inverting configuration, they are fixed at $\approx$0 V [219]. The investigated op-amps are selected with a focus on precision devices (i.e., low (advertised) distortion/noise and low offset errors and bias currents). Furthermore, their gain-bandwidth-product is in excess of 10 MHz.

Fig. 6.11 shows the resulting THD measurements of the amplifier output waveforms (22 op-amps are evaluated, but only the best devices are shown). For input voltages $u_{\text{in}} < 0.3$ V, a THD of the amplified signal below -110 dB can be achieved with certain devices, which is sufficiently low for the considered applications. Interestingly, the THD at the amplifier output can be less than the THD at the input in such a measurement. This is due to the interaction of two series-connected (slightly) nonlinear systems, in this case the low-distortion signal generator and the op-amp. The harmonics of the input signal can destructively interfere with the harmonics introduced by the nonlinearities of the op-amp, due to differing phase relations [220, 221]. This behavior is not desired as the harmonics, which are present in the amplifier's input, are not amplified and hence vanish from the output signal, which reflects an incomplete measurement. This reveals the necessity for an individual analysis of such circuits in a realistic setting in order to determine the behavior, interaction and influence of the main nonlinearities in the signal path.

Note that a reduction of amplifier gain improves the circuit's linearity, as shown in Sec. 6.3.2 below for the case of a unity-gain filter. Furthermore, fully differential amplifiers (FDAs), which are specialized op-amps that provide differential signal paths, are expected to perform even better with respect to their output THD than the analyzed devices, due to their differential nature which can reduce the generation of even-order harmonics [222].

Having established the availability of low-distortion op-amps with a simple amplifier circuit, the next section investigates a higher-order analog low-pass filter.

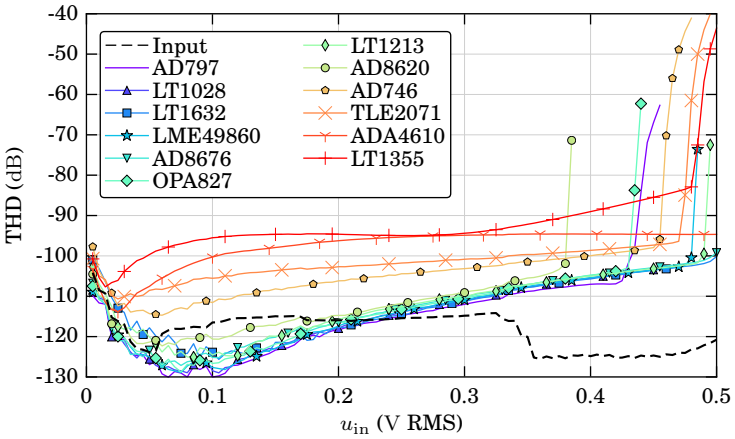

Fig. 6.11: THD of sinusoidal amplifier output signals, considering the first 5 harmonics. The low-distortion amplifier input is provided by a precision signal generator. The prominent increase in THD shown by some op-amps at higher output levels is due to limited op-amp output swing capabilities.

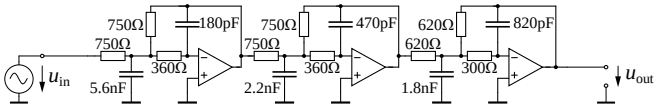

Fig. 6.12: 6^{th}-order Butterworth filter circuit that can be used as an anti-aliasing filter of an ADC that samples with 5 MHz. $G = 1\,V/V$, $f_{pass} = 300\,kHz$, $f_{stop} = 2.5\,MHz$, $A_{Stop} = 100\,dB$. Op-amp: *AD8620*.

6.3.2 Anti-Aliasing Filter

Op-amp circuits are commonly used in analog filters, where they act as signal buffers or amplifiers. **Fig. 6.12** exemplarily illustrates a 6^{th}-order Butterworth low-pass filter implemented with the multi-feedback (MFB) filter topology. With regard to distortion, the MFB topology is better suited than the also widely used Sallen-Key filter topology, as the op-amps are employed in the inverting configuration, which keeps both op-amp inputs near signal ground [219]. Such a filter can be used as the analog anti-aliasing filter of an ADC and hence, it should add only little distortion or noise to the filtered output signal. **Fig. 6.13** illustrates the THD and SNR at the input and output of the filter for different amplitudes and frequencies. The figures were

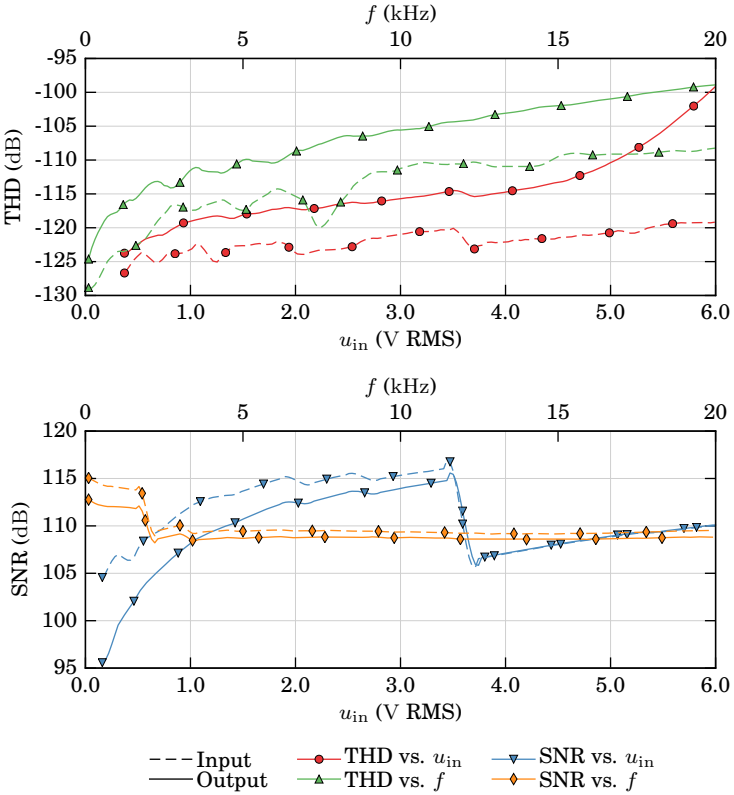

Fig. 6.13: THD and SNR at the output of the MFB low-pass filter. THD includes the first 9 harmonics and SNR is evaluated from 100 Hz to 20 kHz. The frequency for the input voltage sweep is 1 kHz and the input RMS amplitude for the frequency sweep is 2 V. The decreasing SNR at ≈ 3.5 V is due to a range switch in the source.

established with the same method as used for the linearity measurements of single op-amps in Sec. 6.3.1 above. The filter adds ≈5 dB to the THD of its output signal over a wide amplitude range. On the other hand, the SNR is nearly identical at the input and output, due to the low-noise nature of the employed op-amps.

This demonstrates the sufficiently high noise and distortion performance of more complex op-amp circuits. Note that the noise of such a circuit can also be analyzed with circuit simulation software, as manufacturers often provide accurate device models. This is, however, usually not possible with linearity and hence, a dedicated analysis, such as the approach presented here, is necessary.

6.3.3 Summary

The measurements in this section demonstrate the achievable noise and distortion of analog amplifiers and higher-order filters, which is sufficient for the application in sensor circuits of high-precision power converters. The output THD of op-amp signal amplifiers (with a gain of 20) is less than −110 dB for certain devices. Similarly, an analog filter comprising three op-amps (with a gain of 1) reliably demonstrates THD values below −115 dB. The op-amps required for such low distortion figures must be carefully selected, as datasheet information is often lacking. Noise in op-amp circuits is analyzed more conveniently, as it can be modeled with linear equivalent circuits. The mentioned analog filter adds only little noise to the output signal and achieves SNR values that reach 115 dB (DC–20 kHz).

After analog signal processing circuits, a digital acquisition system is often employed in the signal path. Its performance is discussed in the following.

6.4 Analog-to-Digital Conversion

Integrated ADC devices are widespread and quantize analog voltage signals to obtain digital signals with amplitude resolutions of n bits at (often constant) sampling rates f_S. This results in 2^n available quantization levels. Because of the limited amplitude resolution, wideband quantization noise is added to the digitized signals, which limits the best achievable SNR [88]. The SNR in a frequency band from DC to $f_S/2$ of a sampled digital signal with a resolution of n bits can be approximated by [88]

$$\mathrm{SNR} \approx 6.02n + 1.76 \text{ dB}. \tag{6.8}$$

Tab. 6.4: Performance figures of selected precision ADCs. SNR as specified by the datasheet is given by $\mathrm{SNR_{ADC}}$, and in a bandwidth from DC to $f_S/2$. The achieved SNR figures of the devices are generally less than expected from the theoretical maximum given by (6.8), whereas distortion is sufficiently low.

Part	Bits n	f_S (MHz)	THD (dB)	$\mathrm{SNR_{ADC}}$ (dB)	SNR (dB) cf. (6.8)
ADS1675	24	2	−103	97	146.2
ADS9110	18	2	−118	100	110.1
AD7960	18	5	−117	99	110.1
AD7961	16	5	−116	95.5	98
AD7915	16	1	−118.5	94	98
ADS8881	18	1	−115	100	110.1
LTC2378-18	18	1	−124	102	110.1
LTC2377-20	20	0.5	−125	104	122.2

However, commercial ADC devices generally show SNR figures worse than what (6.8) suggests, due to additional noise sources and fabrication constraints of integrated circuits. **Tab. 6.4** lists datasheet values of selected high-resolution ADCs. The best achievable SNR is ≈100 dB (from DC to $f_S/2$), whereas the linearity is sufficiently high, with THD figures below −115 dB. In the following, it is shown how oversampling, i.e, the acquisition of samples at a higher frequency than strictly necessary, can be used to significantly increase the achievable SNR of an ADC. The therefore required digital decimation filter is then optimized to minimize its delay, which affects closed-loop control systems that potentially utilize the ADC data, negatively.

In a basic ADC acquisition system, as illustrated with **Fig. 6.14**, the aim is to replicate the analog signals in the frequency band from DC to f_B (i.e., the baseband) in the digital domain, with an ADC sampling frequency f_S. In order to prevent unwanted signal components due to aliasing, an analog low-pass filter (LPF) with an attenuation A, which should exceed the ADC's dynamic range at $f_S/2$, is placed at the input of the ADC [88]. Thus, the sampling frequency must generally be higher than $2f_B$ such that the analog anti-aliasing filter can roll off in the frequency interval from f_B to $f_S/2$. The quantization noise, caused by the limited ADC amplitude resolution of n bits,

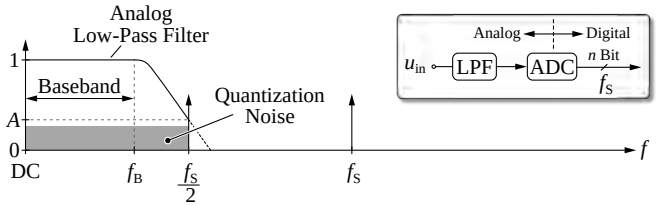

Fig. 6.14: Basic ADC conversion system using Nyquist-sampling, where the required sampling rate f_S is chosen only slightly higher than $2f_B$ (to allow the analog low-pass filter to roll off). The quantization noise is introduced by the ADC and not affected by the analog low-pass filter.

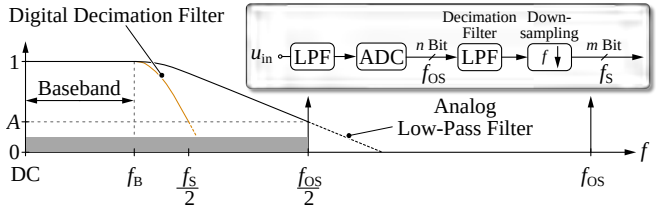

Fig. 6.15: Oversampling employs a higher than necessary ADC sampling frequency f_{OS} to increase the achievable SNR of the acquisition system by spreading the quantization noise energy over a wider frequency band. Furthermore, the order of the analog filter can be significantly reduced, as the filter complexity is shifted to the digital domain. Note that the digital decimation filter affects the quantization noise (not illustrated).

is usually evenly distributed in a band from DC to $f_S/2$, and the resulting achievable SNR can be approximated with (6.8).

If the SNR of a given ADC is insufficient, or cost constraints require the usage of a low-resolution device, oversampling, where f_S is chosen higher than necessary, can be employed to increase the SNR of the digitized signal [88]. **Fig. 6.15** illustrates this approach. As the sampling frequency is now higher ($f_{OS} > f_S$), the energy of the quantization noise, which is unchanged as compared to the Nyquist-sampled system of **Fig. 6.14** due to the assumed identical amplitude resolution of the ADC, is spread over a wider frequency band (i.e., from DC to $f_{OS}/2$) and hence, the noise energy in the baseband is reduced. Furthermore, the analog anti-aliasing low-pass filter can roll off in a wider frequency band to achieve the same attenuation A and can thus be of a smaller order, requiring fewer components (e.g., op-amps), which reduces signal distortion and noise.

However, as only the baseband, which now contains less quantization noise energy, is required for the subsequent data processing system, a (digital) low-pass filter is needed to reject the noise above f_B. Its digital nature allows the implementation of stable, high-order, low-noise and low-distortion filters. Thus, by oversampling, the filter complexity is shifted from the analog to the digital domain [88, 196]. As the subsequent digital processing system might only operate at the lower frequency f_S (which, e.g., corresponds to the execution rate of a digital feedback control system), the oversampled rate f_{OS} can be too high and thus, the sampling rate must be reduced with downsampling. In order to prevent aliasing, a low-pass filter is required, which is the same digital filter used to isolate the baseband as mentioned above (which is, in this context, named decimation filter) [196]. The resulting decimated and downsampled digital signal is sampled at the frequency f_S and achieves a higher amplitude resolution of $m > n$ bits that results from the lower quantization noise energy in the baseband. Consequently, the achievable SNR (SNR_{OS}) is increased. The ratio of the two sampling rates is the oversampling ratio (OSR) and given by: $OSR = f_{OS}/f_S$. The resulting SNR_{OS} in an oversampled ADC system can be estimated with

$$SNR_{OS} \approx SNR_{ADC} + 10\log_{10}(OSR)\ \text{dB}, \tag{6.9}$$

which holds from DC to $f_{OS}/(2\,OSR) = f_S/2$ [88]. For simplicity reasons, it is assumed that the noise energy is subject to an ideal "brick wall" digital low-pass filter, as otherwise, the equivalent noise bandwidth of the specific digital decimation filter has to be considered, due to the fact that the quantization noise is affected by this filter [93].

For oversampling to work, some (uncorrelated) noise must be present in the analog (and digitized) signal in order to be able to build a higher-resolution average with the decimation filter [88]. This noise is usually provided inherently by the circuit components of the analog front-end of the ADC (e.g., the anti-aliasing filter).

The disadvantage of an oversampled ADC conversion system is the requirement for an ADC that is capable of sampling with f_{OS}, and the need for the corresponding digital processing system (i.e., the digital decimation filter and downsampling unit) that must handle the samples at f_{OS}.

In the following section, the digital decimation filter is optimized with regard to its phase lag, which reduces the stability margins of closed-loop control systems, if the acquisition arrangement is part of such.

6.4.1 Digital Decimation Filter Optimization

The digital low-pass decimation filter in an oversampled ADC system, which ideally provides an attenuation of $\mathrm{SNR}_{\mathrm{OS}}$ at $f_{\mathrm{OS}}/(2\,\mathrm{OSR})$ in order to fully prevent aliasing, can add a considerable phase lag to its output signal [196]. Consequently, this section analyzes different digital filters in order to minimize their delay.

Digital IIR filters are preferred for this application as they can realize a given filter specification with fewer stages than FIR filters and consequently, they show a smaller phase lag, which, at low frequencies (i.e., in the baseband), increases nearly linearly with frequency. Thus, the performance of different filters is assessed by the signal delay T_{IIR} that corresponds to this linear phase lag [196].

For the analysis, an ADC with a given amplitude resolution and sampling rate f_{OS} is chosen. Next, a set of integer oversampling ratios is selected, as this is conveniently achievable in digital systems, by simply omitting the desired number of samples. Each oversampling ratio defines the stopband frequency of the corresponding digital decimation filter as $f_{\mathrm{Stop}} = f_{\mathrm{OS}}/(2\,\mathrm{OSR}) = f_{\mathrm{S}}/2$ (see **Fig. 6.15**). The filter's stopband attenuation is fixed at 80 dB, which is a value selected to minimize aliasing and provide stable filter configurations [196]. For each configuration, the passband frequency f_{B} of the decimation filter is then varied in a range from (an arbitrarily selected) $f_{\mathrm{B}} = 20\,\mathrm{kHz}$ to f_{Stop}, while the order of the ensuing filters are limited to 30, which still results in stable digital filter implementations. The filter delay T_{IIR} is evaluated in the frequency baseband from DC to 20 kHz. Where applicable, the passband ripple of the investigated filters is set to 0.0001 dB. Thus, for each

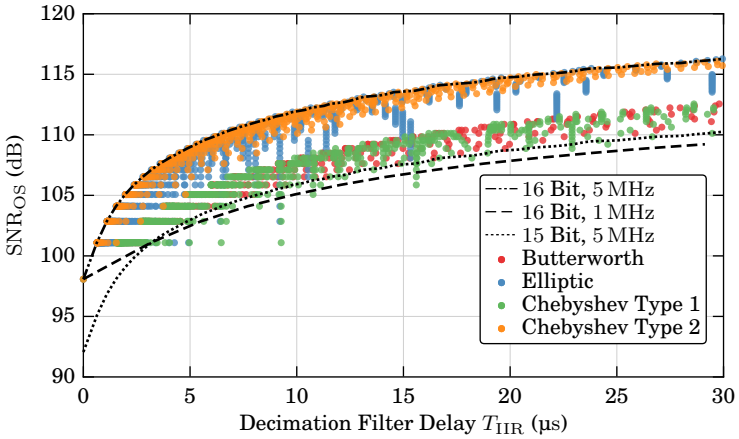

Fig. 6.16: Oversampled SNR and the delay of the required digital decimation filters for different OSR. The colored points correspond to the decimation filters used with the 16-Bit, 5 MHz ADC. The dashed lines are the Pareto fronts of the indicated ADC configurations.

selected OSR, the resulting SNR can be estimated using (6.9), whereas the intrinsic SNR of the ADC is calculated with the approximation (6.8).

Fig. 6.16 plots the evaluated filter selections and the resulting $\mathrm{SNR}_{\mathrm{OS}}$, in correspondence with the delay of the respective digital filter. Each point corresponds to a possible decimation filter for a 16-bit ADC, sampling at a rate of $f_{\mathrm{OS}} = 5\,\mathrm{MHz}$. The Pareto fronts of two other ADCs are also illustrated. For example, considering the 16-bit, 5 MHz ADC and a consecutive control system that operates at a frequency of $f_{\mathrm{S}} = 200\,\mathrm{kHz}$, an OSR of 25 results. Assuming an intrinsic SNR of the ADC of 98 dB, the SNR of the decimated digital signal can, according to (6.9), achieve 112 dB in a band from DC to 100 kHz. According to **Fig. 6.16**, the best digital decimation filter for this configuration (with a filter order up to 30) results in a phase lag that corresponds to a delay of ≈12 µs.

The analysis shows how, with an increased OSR (and hence, a higher $\mathrm{SNR}_{\mathrm{OS}}$), the delay of the filter increases accordingly, which corresponds to the increasing filter order. Furthermore, the Chebyshev Type 2 filter offers the best performance while also featuring no passband ripple [196]. The resulting filter complexities are considerable, with orders up to 30, and thus, digital processing systems that are capable of implementing such filters at the oversampled frequency f_{OS} are required (e.g., FPGAs).

In Sec. 7.2, the delay of the digital decimation filter is considered in the feedback path of a closed-loop control system, as it reduces its stability margin.

6.4.2 Summary

Integrated ADC devices, which are regularly used for feedback control, rarely achieve SNR figures of more than 100 dB (DC–$f_S/2$). However, they are often capable of sampling at frequencies in excess of several megahertz, which is more than required for the control of common power electronic converter systems. Thus, the SNR-limiting quantization noise is distributed over a wider frequency range and the analog low-pass filter can be of reduced complexity, which limits noise, distortion and cost. A digital decimation filter then reduces the bandwidth of the oversampled digital signal to the desired range, hereby rejecting undesired quantization noise. SNR figures in excess of 110 dB are achieved for downsampled rates that are common in the considered control systems. Additionally, the digital decimation filter is optimized such that it adds only a minimum phase delay to the digital signal.

6.5 Isolated ADC Acquisition Jitter

Power electronic conversion systems regularly require sensors (and their ADCs) on reference potentials that are different from the one of the control system, where the data is processed. This necessitates the transfer of the digital data across galvanic isolation barriers. **Fig. 6.17** illustrates such a circuit configuration, which performs a galvanically isolated current measurement in a HB switching arrangement. This is a typical power electronic topology and sensing application. The shunt resistor R_S offers low noise and a high linearity compared to other integrated, isolated current sensors, as demonstrated in Sec. 6.1. Compared to a low-side shunt placement, which would obviate the isolated sensing circuitry, the illustrated setup allows the quick detection of faulty output currents at all times [201, 223].

Placing the ADC on the isolated potential offers the benefit that only its digital signals need to cross the isolation barrier, which is effortlessly achievable with integrated digital isolator devices that preserve the signal integrity. However, the ADC control signal that starts the acquisition process, whereby the ADC samples its input voltage prior to its digitization, is also transmitted through the signal isolator. This device can add significant amounts of jitter to it, which expresses itself as a time-dependent and stochastically varying signal propagation delay of the isolator, as shown in Sec. 4.1.1. It is well-

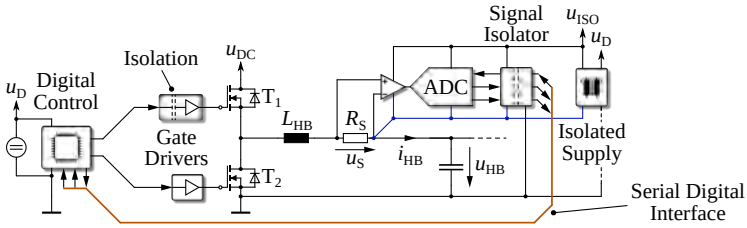

Fig. 6.17: Typical setup of a digitally controlled HB switching stage employing a shunt resistor and an isolated ADC circuit in order to measure the HB output current i_{HB} with low noise and distortion.

known that this jitter, even if it is in the picosecond range, severely limits the ADC's achievable SNR, as it introduces wideband noise to the sampled signal [88, 224]. This source of HB current measurement noise is relevant for ultra-low-noise applications and has been discovered as a deteriorating effect in earlier work, but not described in detail [223].

In the following, the implications of ADC sampling jitter on the SNR and the design of a synchronously sampling HB current sensor are presented. Note that the ramifications of the sampling jitter are identical for any ADC system and not restricted to the discussed current measurement, which is selected here due to its applicability in Class-D power amplifier topologies that require a low-noise HB current sensor.

In order to evaluate the impact of the ADC sampling jitter on the HB output current measurement SNR, the circuit configuration of **Fig. 6.17** is considered in a single-phase DC/AC converter. **Fig. 6.18** illustrates the related waveforms. It is assumed that the time-average of i_{HB} over a switching period T_{PWM}, denoted as $\langle i_{HB} \rangle$, and u_{HB}, are both sinusoidal (with fundamental frequency $f_F = 1/T_F$) and in phase to each other, which is valid for resistive loads and small HB output filter capacitances C_{HB}. In the following analysis, the load is resistive (R_L) and connected to a second, identical HB. This constitutes a full-bridge Class-D amplifier topology with a bridge-tied load (BTL), as shown in **Fig. 6.18 (a)**. Note that the following analysis is independent of the load configuration, it can be performed equally with any type of load (e.g., inductive-resistive), and other load connections (e.g., to a DC-link mid-point instead of the considered BTL). In order to be able to provide a load current of both polarities, a constant CM voltage $u_{CM} = u_{DC}/2$ is added to the HB output voltages. **Fig. 6.18 (b)** illustrates the resulting waveforms for one fundamental period. The duty cycle of the HB PWM gate control

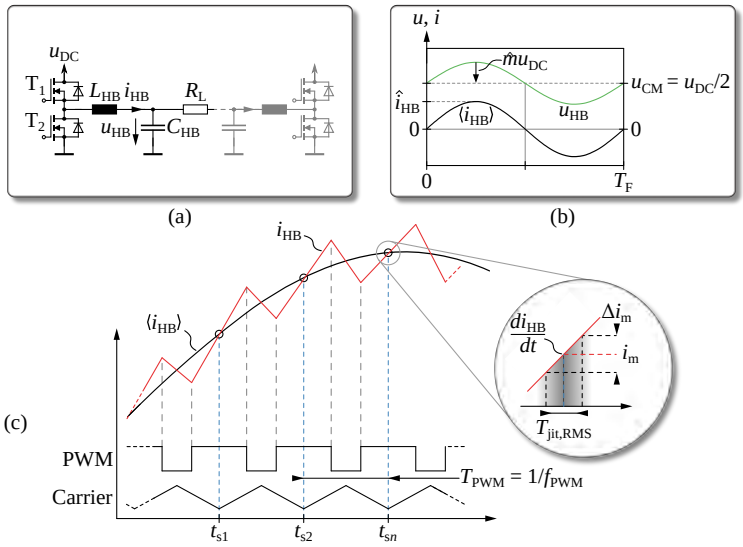

Fig. 6.18: (a) Discussed HB conversion stage. **(b)** Sinusoidal waveforms of relevant signals. **(c)** HB current waveform subject to ripple. The current-sensing ADC samples once per PWM period at sampling instants t_{sn}. Due to jitter, t_{sn} is varied stochastically around its ideal time instant. The current slope at t_{sn} defines the current measurement error Δi_m that reduces the SNR of the current measurement.

signal, which is the relative turn-on time of the high-side transistor T_1 during a PWM switching period T_{PWM}, is thus given as $d(t) = 1/2 + m(t)$, with the modulation index being $m(t) = \hat{m}\sin(2\pi f_F t)$. Neglecting switching frequency ripple components and the voltage drop at L_{HB}, this results in

$$u_{HB}(t) = u_{DC}\left(1/2 + \hat{m}\sin(2\pi f_F t)\right), \tag{6.10}$$

$$\langle i_{HB}\rangle(t) = \hat{i}_{HB}\sin(2\pi f_F t). \tag{6.11}$$

During the turn-on time of T_1, the slope of the HB output current is then given as

$$\frac{\mathrm{d}i_{HB}(t)}{\mathrm{d}t} = \frac{u_{DC} - u_{HB}(t)}{L_{HB}} = \frac{u_{DC}\left(1 - 2\hat{m}\sin(2\pi f_F t)\right)}{2L_{HB}}. \tag{6.12}$$

As illustrated in **Fig. 6.18 (c)**, the ADC is sampling once per PWM period when the carrier reaches its bottom value, at time instants t_{sn}, which is the case with regularly sampled, symmetric PWM [95]. This ensures that no HB switching action takes place during the signal acquisition, which, due to the fast voltage transients occurring at the switch-node, can introduce spurious error voltages to the measurement. The sampling could equally take place at the top value of the PWM carrier.

The jitter of the sampling signal moves the ADC acquisitions away from the ideal instants, which would result in the current measurement i_m, as illustrated in the enlarged portion of **Fig. 6.18 (c)**. Consequently, the resulting measurement error Δi_m depends on the current slope $\mathrm{d}i_{HB}/\mathrm{d}t$ and is, due to the stochastic nature of the jitter, also behaving like noise and hence reduces the SNR of the current measurement. The jitter-induced current error can thus be given as

$$\Delta i_m(t) = \frac{\mathrm{d}i_{HB}(t)}{\mathrm{d}t} T_{jit,RMS}. \tag{6.13}$$

In order to calculate the SNR of the current measurement, the RMS value of the current error is determined over the fundamental period T_F [88] with

$$\Delta i_{m,RMS} = \sqrt{\frac{1}{T_F}\int_0^{T_F} \Delta i_m^2(t)\mathrm{d}t} = \frac{T_{jit,RMS}\, u_{DC}\sqrt{2\hat{m}^2 + 1}}{2L_{HB}}. \tag{6.14}$$

By relating this RMS error current to the RMS value of the load current i_{HB}, the SNR is found as

$$\mathrm{SNR}_{DC-f_S/2} = 20\log_{10}\left(\frac{\hat{i}_{HB}/\sqrt{2}}{\Delta i_{m,RMS}}\right). \tag{6.15}$$

Note that the SNR is valid in the frequency band ranging from DC to half of the sampling frequency f_S. In this case, $f_S = f_{PWM}$, as one sample is acquired per PWM period. The presented derivation of the SNR can be easily modified to also incorporate ADC sampling twice during a PWM period, at the top and bottom values of the PWM carrier. Assuming a uniform noise density, the SNR can be calculated for a narrower frequency band $f_{BW} < f_S/2$ by accounting for the noise energy only in this bandwidth [88]:

$$\mathrm{SNR}_{\mathrm{DC}-f_{BW}} = \mathrm{SNR}_{\mathrm{DC}-f_S/2} + 10\log_{10}\left(\frac{f_S/2}{f_{BW}}\right). \tag{6.16}$$

This is of interest in, e.g., mechatronic positioning applications that are sensitive to noise in a frequency range from DC to ≈10 kHz.

Considering additional (uncorrelated) noise sources that are not related to jitter, e.g., ADC quantization or noise from the ADC's input amplifiers/filters, which can be expressed by an equivalent RMS noise current i_n, the SNR is then given by extending (6.15):

$$\mathrm{SNR}_{\mathrm{DC}-f_S/2} = 20\log_{10}\left(\frac{\hat{i}_{HB}/\sqrt{2}}{\sqrt{\Delta i^2_{m,RMS} + i^2_n}}\right). \tag{6.17}$$

Fig. 6.19 illustrates this equation exemplarily, where i_n is selected such that it corresponds to the quantization noise of the indicated ADC resolutions [88]. **Fig. 6.19 (a)** sets the HB inductance value L_{HB} constant while sweeping $T_{Jit,RMS}$ and **Fig. 6.19 (b)** fixes $T_{Jit,RMS}$ while varying L_{HB} in order to illustrate the sensitivity of the SNR to these important design parameters. The results of numeric computer simulations, which recreate selected operating points of the presented measuring configuration in a circuit simulation by sampling a HB current signal (which naturally also contains the corresponding current ripple components) at jittery time instants, are also illustrated. They verify the validity of the presented analysis. The time step used for the computer simulations is 13.33 ps, which provides a sufficient temporal resolution to cover RMS jitter values below 50 ps, as the simulations show. This requires large amounts of computer memory and was thus performed on a high-performance computing cluster.

The following example demonstrates the impact of this analysis on the design of the HB inductor. Precision power amplifiers for mechatronic positioning applications can operate at DC-link voltages up to 400 V with a pulse repetition frequency of 100 kHz and a peak output current of $\hat{i}_{HB} = 20$ A.

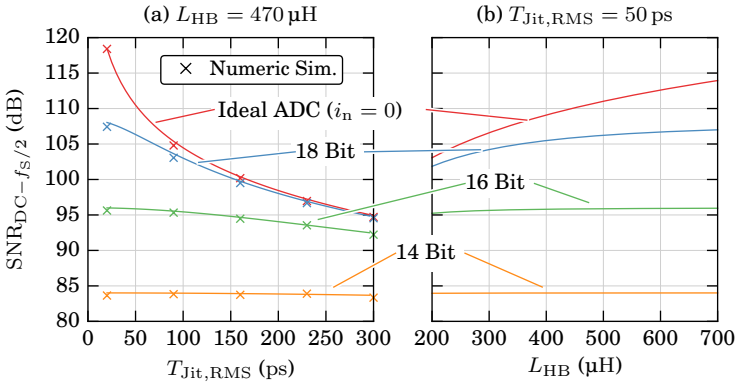

Fig. 6.19: Best achievable SNR (DC–$f_S/2$) of the HB output current measurement. **(a)** Dependence on the ADC conversion signal's RMS jitter and **(b)** the HB inductance. The analysis is done for different levels of additional noise i_n that corresponds to the ADC's quantization noise. $u_{DC} = 400\,V$, $R_L = 5\,\Omega$, $\hat{i}_{HB} = 10\,A$ (assuming that this is also the ADC's full-scale input).

The HB inductance value is usually chosen such that the peak-to-peak current ripple is limited to ≈20 % of the current amplitude, which results in a value of $L_{HB} = 250\,\mu H$ for this example. Assuming an ADC conversion jitter of 100 ps, which is caused by the signal isolator, and a low-noise acquisition system with an effective resolution of 18 bits (i.e., ≈108 dB intrinsic SNR), as well as a bridge-tied (full-bridge Class-D topology) resistive load of 10 Ω, the best achievable measurement SNR of 102.8 dB results (DC–50 kHz). If, however, the HB inductance value is selected as 680 µH, the SNR can be increased to 106.8 dB, which is equivalent to a reduction of sensor current noise power by a factor of 0.63, in this example.

6.5.1 Summary

The analysis shows how low-noise, high-resolution acquisition systems are sensitive to the ADC's conversion jitter which, in power electronic converters, is often caused by digital signal isolators that are required for the galvanic isolation of the ADC.

In the demonstrated application of a low-noise, shunt-based HB current measurement, the HB inductance value offers a degree of freedom to improve

the achievable SNR for a given ADC conversion jitter, as the slope of the current ripple determines the measurement error.

With the presence of uncorrelated noise sources such as ADC quantization or noise from analog signal processing circuits, the sensitivity of the measurement SNR to the ADC sampling jitter is, together with the best achievable SNR, reduced. Nonetheless, the presented derivation can be used as a design guideline for the HB inductance value if the HB current is acquired with an isolated ADC system.

7 Hardware Demonstrator

Based on the analyses presented in this thesis so far, which investigates and optimizes key components of low-noise switch-mode power amplifiers, a full-scale hardware demonstrator is built for verification purposes and further explorations. The amplifier operates with a 400 V DC input and provides a controlled output current of up to 25 A (peak) to a single-phase load. GaN power transistors are used as they promise a good distortion performance, which is revealed in Ch. 3. The same analysis also identifies two promising power stage topologies that feature low distortion, namely the synchronously rectified dual buck (DB) and the regular interleaved half-bridge (HB) topology. The demonstrator system is capable of implementing both power stages such that they can be comprehensively compared.

The design and construction of the power amplifier is presented. Measurement results demonstrate its performance and identify sensitivities of noise and distortion to amplifier system components and operating parameters.

First, **Sec. 7.1** introduces the circuit layout of the power topology. It then presents the semiconductor loss model which is confirmed by measurements. This model is used to investigate the achievable amplifier output current such that maximally admissible transistor junction temperatures are not destructively exceeded. Similarly, the optimal number of paralleled transistors is derived as a function of the amplifier's nominal output current. **Sec. 7.2** presents the closed-loop feedback control system employed to improve the disturbance rejection and reference tracking performance of the amplifier. Its sensors, digital signal processors and modulators are outlined. The detailed plant model is given and used to optimize the stability margins and gains of the controllers. Next, the closed-loop feedback system is used in **Sec. 7.3** in conjunction with the power transistor loss model to investigate the distortion caused by the thermal variation of the transistor junction temperatures.

Sec. 7.4 provides details of the amplifier's construction and **Sec. 7.5** introduces the measurement methods and reference sensors used for assessing its performance. Experimental results are provided in **Sec. 7.6**, which investigates the achieved output current SNR and THD, as well as the influences of different system parameters such as the DC supply, dead time, the power stage topology or the noise shaping modulators.

Finally, a summary of key components and performance figures is given in **Sec. 7.7**.

7.1 Power Stage Topology

The two switching stages that are intended for further analysis (based on the results obtained in Ch. 3), specifically the synchronously rectified DB and the regular interleaved HB, are topologically identical and only differ in the waveforms of the HB currents. Thus, only a single power stage layout is required. The DB topology is characterized by a circulating bias current which enforces unidirectional HB currents, hereby reducing distortion (see Sec. 3.1 for details). This increases the HB currents significantly and thus, the transistor losses must be carefully considered for this topology, which is done in Sec. 7.1.1 below.

Fig. 7.1 illustrates the main components of the demonstrator system's power stage topology. It provides two output phases, each comprising two interleaved HBs, which enables the operation as the DB and the regular interleaved topology. The single-phase load is connected between the two phase outputs as a bridge-tied load (BTL), which increases the available load voltage and power supply rejection [58, 102]. The converter is designed for an input voltage of $\leq$400 V DC and the load current amplitude $\hat{i}_\mathrm{L}$ can reach 25 A (e.g., peak value of a sinusoidal signal).

As with most switch-mode power converters, EMI filters are employed at the input and output. A single-stage, passively damped common-mode (CM) and differential-mode (DM) filter is used at the DC input to ensure compliance with common EMI norms, such as *CISPR 11 A/B*. The output filter consists of two stages. Its main purpose is the reduction of HF emissions that can potentially radiate from the actuators in precision motion systems, which are often placed near sensitive measuring equipment. Note that, by changing the phase shifts between the PWM carriers of the four HBs, the high-frequency spectral content, i.e., the CM and the DM components of the load voltage, can be influenced [102].

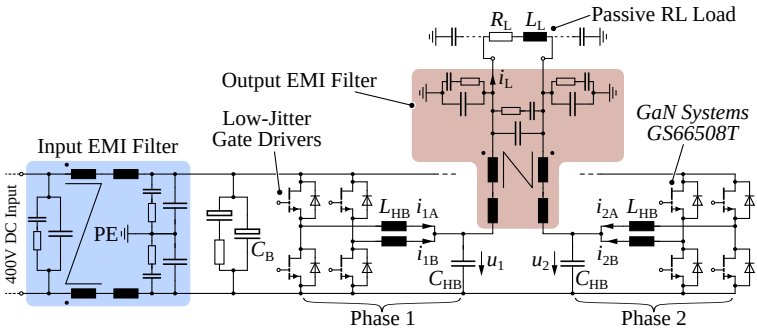

Fig. 7.1: Power circuit of the hardware demonstrator. It comprises two individually interleaved phases that drive a single-phase bridge-tied load (BTL). EMI filters at the DC input and AC output ensure compliance and limit electromagnetic emissions from the actuators near potentially sensitive equipment in the positioning system.

The first output filter stage comprises the HB inductor L_{HB} and the filter capacitor C_{HB}. As shown in Sec. 6.5, the conversion jitter of the isolated ADC that is used to measure the HB current imposes a lower boundary for the inductance of L_{HB} in order to achieve a certain SNR of the HB current measurement. A value of $L_{HB} = 700\,\mu H$ is selected to reduce the HB ripple current amplitude to ≈10 % of the peak HB current. The linearity of these inductors, characterized by the stability of the inductance values as a function of the inductor currents, is important to obtain an inherently low amplifier output distortion. Consequently, gapped ferrite cores are used for L_{HB} (*EPCOS ETD59* with a 4 mm air gap in the center core leg). The inductor provides a constant inductance value up to currents of ≈13 A until saturation effects emerge. This is sufficient for the intended output currents of up to 25 A due to the usage of two interleaved HBs. The winding is made from HF litz wire (630 wires with a diameter of 0.071 mm each) to reduce high-frequency losses [225].

The HB filter capacitor C_{HB} defines the cutoff frequency of the first filter stage. Due to the cascaded feedback control system, which is presented in Sec. 7.2 below, the selection of this capacitance value does not influence the dynamic performance of the control system (if no current or voltage limits are exceeded during transients). However, large HB filter capacitances can result in considerable reactive currents at elevated fundamental frequencies, which lowers the power conversion efficiency and the available load current. On the other hand, a low filter cutoff frequency results in a better attenuation of noise, which increases the achievable amplifier output signal SNR. For

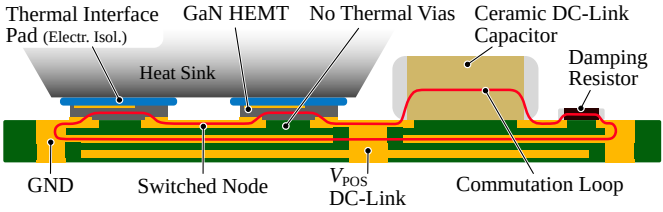

Fig. 7.2: Simplified circuit board cross-section illustrating the layout of a top-cooled HB. The lack of thermal vias allows low-inductance vertical commutation loops. Only the top two copper layers are shown (a six layer PCB is used). Geometric proportions are altered for better visualization.

the demonstrator, a value of $C_{\mathrm{HB}} = 12\,\mu\mathrm{F}$ is selected, which places the cutoff frequency of the first filter stage at 1.7 kHz. This first HB filter section is actively damped by means of the feedback control system, whereas the second stage of the EMI output filter comprises a passively damped high-frequency CM/DM filter.

The single-phase nature of the load results in a significant power ripple at the input and output of the amplifier when operating with AC load currents. In order to stabilize the DC-link voltage, electrolytic capacitors with a total value of $C_{\mathrm{B}} = 1.8\,\mathrm{mF}$ are employed. These capacitors are also an integral part of the EMI input filter.

As shown in Ch. 3, GaN transistors enable power stages with very low inherent distortion due to the comparably small values of their parasitic elements. They achieve fast switching transitions and provide low conduction resistances. Thus, the *GS66508T* GaN enhancement-mode high-electron-mobility (E-HEMT) power transistor from *GaN Systems* is selected for the hardware demonstrator. It features a blocking voltage of 650 V, a nominal on-state conduction resistance of 50 mΩ, a current rating of 30 A and no reverse recovery losses, which makes it well suited for hard-switched inverter applications [226]. The loss model of this power device is presented in Sec. 7.1.1 below. As the switching transistors are cooled from the top side, no thermal circuit board vias, that would disrupt the commutation loop of the two HB transistors, are required, which enables fast HB switching transitions with little voltage overshoot and ringing. **Fig. 7.2** illustrates the circuit board cross-section of a top-cooled HB, featuring a heat sink and a 40 mm fan for forced air cooling. Short HB switching times are favorable, as they enable brief HB interlock/dead times, which is beneficial for low-distortion power

outputs as outlined in Sec. 2.3. Values as low as 30 ns are reliably achieved with the demonstrator system.

In order to reduce the voltage drops across the power transistors during reverse conduction, which in case of GaN transistors with negative gate voltages during turn-off can be substantial (i.e., several volts), small SiC power diodes (*CREE C3D1P7060Q*, 600 V, 3.3 A) are connected anti-parallel and in close proximity to each E-HEMT. These diodes only conduct during the dead time interval, which is usually shorter than 100 ns and consequently, they dissipate little power and their pulse current rating is sufficient.

Each transistor is driven by a *Texas Instruments LM5114* gate driver with separate turn-on/off resistors of 6.7 Ω and 3.3 Ω, respectively [227]. These values are selected to obtain fast HB switching transitions without parasitic transistor switching actions, and provide some damping in the gate loop. The gate drivers apply a voltage of 6 V to turn the power E-HEMTs on and a voltage of −3.3 V during turn-off. The negative gate voltage is required due to the low threshold voltages of the power transistors in order to prevent the parasitic turn-on of a power device during fast HB switching transitions. Each gate driver circuit is supplied by a low-power (2.5 W), high-frequency (1 MHz) isolated forward converter that employs a toroidal ferrite core transformer (6.3 mm) with reinforced isolation between the primary and secondary windings to reduce the parasitic capacitance, which otherwise adds to the capacitance of the switch-node and increases switching losses. The gate control signals are galvanically isolated using low-jitter digital isolators/gate drivers (*Si8271*; 40 ps RMS jitter [153]), which are required to reduce wideband noise in the switched HB voltage outputs as demonstrated in Ch. 4. Also, this isolator is robust against high CM voltage transients across its isolation barrier (typically 300 kV/µs), which is a necessity for fast-switching GaN transistors. Initially, the demonstrator was built and tested with the low-jitter gate driver presented in Ch. 4. Later, the integrated driver (*Si8271*) became available and was also tested with the demonstrator. Both solutions achieve a nearly identical noise performance in the gate signals and the switched HB voltages, despite the fact that the commercial solution (*Si8271*) has an output signal jitter of twice the magnitude (40 ps RMS) than the presented low-jitter driver, as other sources of noise, such as the DC supply of the amplifier, begin to dominate the overall noise power at the achievable low levels of jitter-related HB voltage noise.

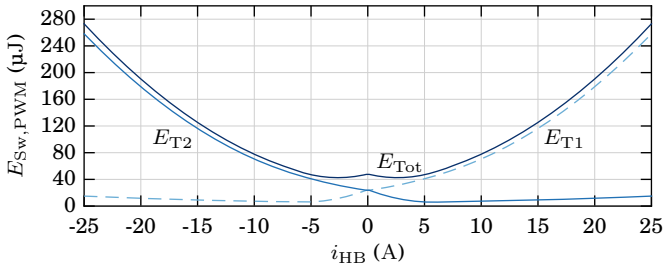

Fig. 7.3: Measured transistor switching loss energies for a HB consisting of a high-side (T_1) and low-side (T_2) transistor (*GaN Systems GS66508T*) [228]. The indicated energies are dissipated once per PWM cycle (i.e., two switching actions). Positive HB currents i_{HB} flow out of the HB (i.e., hard turn-on of T_1) and negative currents flow into it (i.e., (partially) soft turn-on of T_1). $u_{\mathrm{DC}} = 400\,\mathrm{V}$. Gate driver: *LM5114*. Turn-on/off resistors: 6.7 Ω/3.3 Ω. Turn-on/off voltages: 6 V/−3.3 V. Dead time: 50 ns. Numeric fitting data provided in **Tab. 7.1**.

7.1.1 Power Transistor Loss Model

In the following, the loss model of the selected power switching transistor (*GaN Systems GS66508T*), comprising switching and conduction losses, is presented, which is then used to derive the achievable amplifier output currents (see Sec. 7.1.2), and to gain insights into the distortion caused by thermal modulation of the on-state resistance (see Sec. 7.3).

The evaluation of the transistor switching losses is aggravated by the fact that they depend significantly on the gate drive configuration and sufficient data is rarely found in datasheets. Loss measurements of the utilized GaN power transistors, for soft- and hard-switching transitions, are provided in [228], which are used here to derive the transistor losses occurring during a PWM period as a function of the HB current. The loss model is extended by incorporating parasitic capacitances that cause additional switching losses (e.g., due to the PCB routing or the HB inductors). Losses during the HB dead time interval, when the transistors (with their SiC diodes connected anti-parallel) may operate in reverse conduction, are also considered. A dynamic behavior of the transistor on-state conduction resistance $R_{\mathrm{DS,on}}$ has not been observed and is thus not modeled [229, 230]. The resulting loss energies for each HB transistor during one PWM cycle (i.e., two switching transitions per transistor, one turning the device off and one turning it on) are illustrated in **Fig. 7.3** for a DC-link voltage of 400 V and under the assumption

Tab. 7.1: Polynomial fitting coefficients for the switching energy E_{T1} dissipated during one PWM cycle (cf. **Fig. 7.3**). It is assumed that the HB current i_{HB} is constant during the PWM period. Unit: µJ.

$E_{T1} = c_0 + c_1 i_{HB} + c_2 i_{HB}^2 + c_3 i_{HB}^3 + \cdots + c_6 i_{HB}^6$							
i_{HB} in:	c_0	c_1	c_2	c_3	c_4	c_5	c_6
[0, 25] A	24.17	1.943	0.2544	0.001716	0	0	0
[−25, 0] A	25.43	8.29	1.303	0.09475	0.003415	5.322e−5	1.985e−7

of a constant HB current during the PWM period. Polynomial fitting parameters for the high-side transistor (T_1) switching losses are listed in **Tab. 7.1**. Measurements of the overall losses of the demonstrator system corroborate the accuracy of this transistor loss model as shown in **Fig. 7.5** below.

In order to accurately model the transistor conduction losses, with consideration of the temperature-dependent $R_{DS,on}$, a computer simulation, which incorporates a comprehensive thermal model of each power transistor and its cooling solution, is employed [129]. This allows to track the thermal variation of the junction temperature T_j during converter operation with fundamental output frequencies f_F of several tens of cycles per second, which are common for mechatronic positioning applications. Note that a thermal model that consists only of thermal resistances is insufficient to correctly recreate the behavior of T_j during a fundamental period, as the converter is not operated with a constant load current and hence, the thermal capacitances of both the transistor junction and cooling solution influence the dynamics of T_j. This approach is identical to the modeling and simulation performed in Sec. 3.2, where the junction temperatures of different power devices are considered to identify suitable low-distortion topologies.

In the following, this approach is employed for the hardware demonstrator's topology in order to investigate its losses, achievable output currents and distortion caused by transistor on-state conduction resistance modulation. **Fig. 7.4** illustrates the simulation model, which is employed for each transistor. Once per PWM cycle, the individual and instantaneous conduction and switching losses (P_C, P_{Sw}) are evaluated and applied to the respective thermal model that consists of two capacitances and resistances that implement the important thermal dynamics. The capacitance C_j and resistance R_{jc} model the thermal behavior of the transistor chip. Their values are provided by manufac-

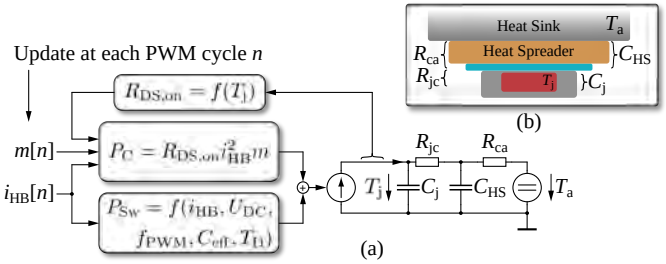

Fig. 7.4: (a) Thermal model used to simulate the thermal variation of $R_{DS,on}$ during amplifier operation, including transistor conduction and switching losses. **(b)** The model uses the thermal junction-case resistance R_{jc}, the thermal junction capacitance C_j, as well as the thermal resistance of the isolation pad and the heat spreader to ambient, R_{ca}, and the thermal capacitance of the isolation pad and heat spreader, C_{HS}. The modulation index m is the relative on-time of the high-side HB transistor during one PWM cycle.

turers or can be extracted from the transient thermal impedance curve often found in power transistor datasheets. C_{HS} and R_{ca} represent the heat spreader and the thermal resistance from transistor case to ambient (cf. **Fig. 7.4**). It is assumed that the heat sink base plate and fins are fixed at the ambient temperature T_a, and the thermal capacitance C_{HS} models the capacitance of the heat spreader, which connects the transistor case thermally to the base plate and fins of the heat sink, and the isolation pad. This covers all relevant thermal elements. The values of this capacitance/resistance are found using a thermal 3D FEM simulation which incorporates the utilized geometries and required material properties. Values for the investigated configuration are given in **Fig. 7.6**. The temperature dependence of the $R_{DS,on}$ is usually provided by manufacturer datasheets and it often obeys a quadratic function of T_j, also in modern WBG semiconductors, which facilitates the evaluation of the transistor conduction losses, as the dependencies can effortlessly be implemented in the simulation software [128, 135]. Note that, as this model incorporates the important nonlinearities, it is capable of predicting thermal runaway which can be caused by high transistor losses and the fact that the currents are often impressed by the feedback control system in amplifiers for mechatronic applications. The disadvantage of this approach is that the thermal system requires time to reach its steady-state value, which prolongs simulations. This can be alleviated by initializing the thermal model to the expected steady-state temperatures. The modification of the thermal transfer

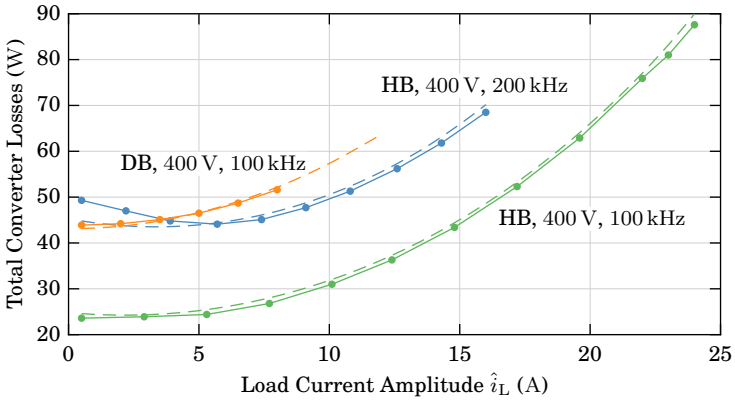

Fig. 7.5: Measured overall power conversion losses of the hardware demonstrator and the corresponding model predictions (dashed), for the regular interleaved HB and the DB topology. Load: 5 Ω+2.5 mH (losses are practically identical for all considered load configurations). $f_F = 35\,\text{Hz}$, $I_B = 5.5\,\text{A}$ (DB topology bias current).

functions to reduce the simulation complexity, as explained in Sec. 3.2.2, is not required for this approach, as the circuit simulation does not incorporate detailed parasitic elements and hence, the simulation time step is not selected as small as in the analysis of Sec. 3.2.

This semiconductor loss model is used to predict the overall power conversion losses of the hardware demonstrator. **Fig. 7.5** compares measurements performed on the amplifier system using a power analyzer with the results of the computer simulation model, which match well. The illustrated losses include not only the losses of the eight HB transistors of the hardware demonstrator, but also inductor (winding and core) losses as well as conduction losses in shunt resistors, PCB tracks and EMI filters. Power for the digital control logic and cooling fans (≈15 W) is not considered. Note that the DB topology is generating approximately twice the loss power as the regular interleaved topology, which constitutes its major drawback. The resulting power conversion efficiencies are listed in Sec. 7.6.3 below.

7.1.2 Amplifier Operating Range

Using the discussed comprehensive loss model of the power converter, the detailed transistor thermal behavior can be investigated for both analyzed power stage topologies. **Fig. 7.6** exemplarily illustrates simulation wave-

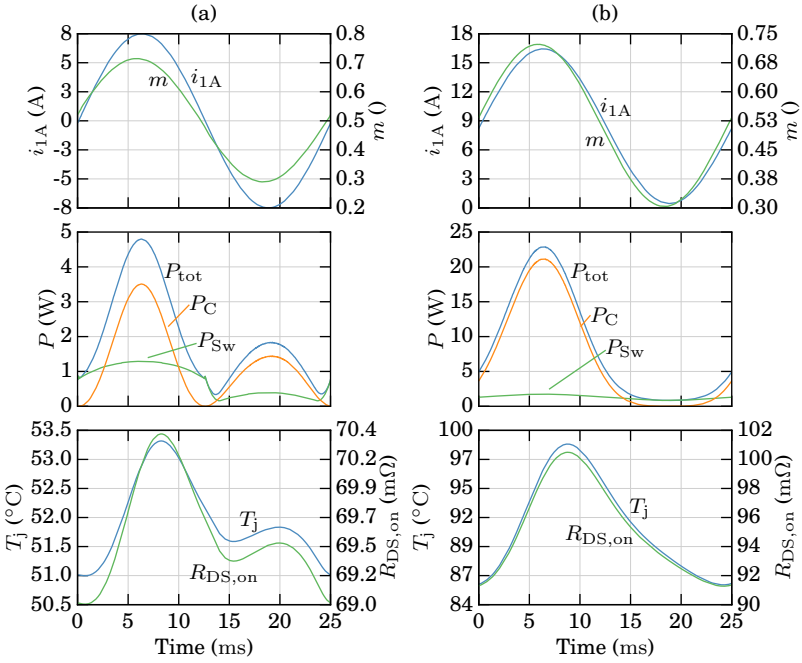

Fig. 7.6: Simulation results of the thermal behavior of a high-side HB transistor during one fundamental load current period. **(a)** Regular interleaved topology. **(b)** DB operation. m: HB modulation index. Middle plots: transistor losses, $P_{tot} = P_C + P_{Sw}$. $\hat{i}_L = 16\,A$, $f_F = 40\,Hz$, $I_B = 8\,A$, $f_{PWM} = 100\,kHz$, $u_{DC} = 200\,V$, $L_L = 2.5\,mH$, $R_L = 5\,\Omega$, $T_a = 40\,°C$, $R_{jc} = 0.5\,K/W$, $C_j = 2.4\,mF$, $R_{ca} = 5.5\,K/W$, $C_{HS} = 10\,mF$.

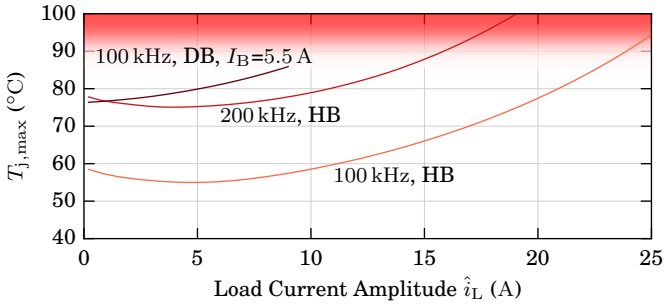

Fig. 7.7: Simulated peak junction temperatures during converter operation with PWM frequencies of 100 kHz and 200 kHz for the regular interleaved HB and DB configurations (with a constant bias current of 5.5 A). This is valid for all considered load configurations and for fundamental load current frequencies below ≈40 Hz.

forms. The load current i_L in this example is sinusoidal with an amplitude $\hat{i}_L$ of 16 A and a fundamental frequency of 40 Hz. In **Fig. 7.6 (a)**, the converter is operated with the regular, interleaved power stage topology where each HB conducts a current of amplitude $i_L/2$. The simulation model allows a detailed insight into the behavior of the transistor junction temperatures, which in this case, vary by ≈2.3 K. On the other hand, if the converter is operated with the DB mode, as shown in **Fig. 7.6 (b)**, which results in higher HB currents as indicated, a variation of T_j of ≈12 K occurs, which consequently also leads to a higher variation of the $R_{DS,on}$. Thus, after the introduction of the closed-loop feedback control system, this simulation model is used in Sec. 7.3 to investigate the harmonic distortion resulting from the variation of the transistor on-state resistances, with consideration of the feedback controllers.

In the following, the simulation is used to investigate the converter's highest allowable load current amplitude for a given operating configuration. The load current limit is set such that the peak junction temperatures of the power transistors does not exceed ≈90 °C, to prevent thermal runaway and to provide some safety margin. Note that the operating point illustrated in **Fig. 7.6 (b)** exceeds this constraint, as the peak junction temperature reaches 98 °C. **Fig. 7.7** illustrates the load current limits for different operating modes of the discussed amplifier demonstrator. The transistor losses are practically independent of the chosen load resistor/inductor values, as they mainly depend on the switched current and not on the HB duty cycles. The same applies for the fundamental frequency f_F of the sinusoidal load current,

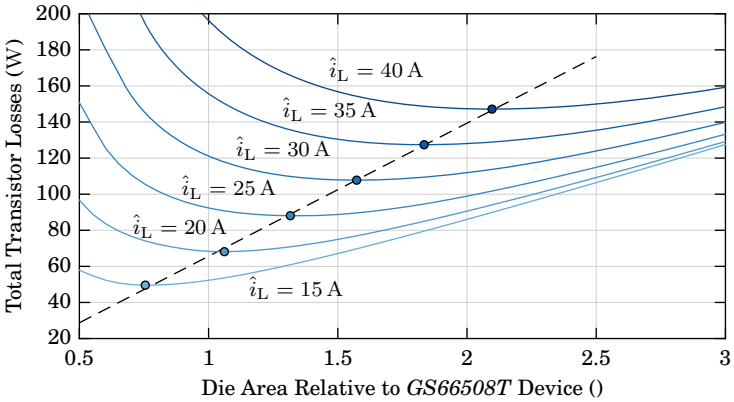

Fig. 7.8: Total transistor losses (conduction and switching) of the demonstrator system, averaged over a fundamental period of the load current, for different load current amplitudes $\hat{i}_L$. The active transistor area is scaled relative to a single *GaN Systems GS66508T* transistor used in the demonstrator system. $f_{PWM} = 200$ kHz, $u_{DC} = 400$ V. Regular interleaved power stage topology.

as the reactive power (caused by the HB filter capacitors) is negligible at the considered frequencies.

It is evident that the DB topology, due to its circulating bias current I_B and thus, the increased transistor losses, can provide less load current before the junction temperatures reach critical values, which is an inherent limitation of this power stage topology. The high losses could be lowered by dynamically adapting I_B during converter operation to the momentarily occurring load current amplitudes, while still maintaining an acceptable distortion performance. Similarly, by modulating the bias current as shown in [39], the losses can be reduced, but distortion is increased which is thus not a favorable operating mode.

7.1.3 Transistor Paralleling

As the power transistor losses limit the achievable amplifier load current, it is illustrated in the following how the load current range can be optimally extended by changing the active areas of the power transistors (e.g., by connecting power transistors in parallel). This reduces the currents of the individual transistors and hence, the associated losses and junction temperatures.

As the losses P_T of a single *GS66508T* transistor are known in detail (see **Fig. 7.3**), the losses $P_{\mathrm{T,Tot}}$ of n paralleled transistors, operating with a total HB current i_HB, can be derived with

$$P_{\mathrm{T,Tot}} = nP_\mathrm{T}(i_\mathrm{HB}/n). \tag{7.1}$$

This assumes that each transistor has its individual gate driver and cooling system, such that for each transistor, the same losses as presented in the previous section occur for the same current. Note that n does not necessarily have to be integer, as long as the gate drivers and cooling systems are scaled accordingly.

The resulting total transistor losses (conduction, switching) of the eight switches employed in the hardware demonstrator (which can now consist of several paralleled devices) are illustrated in **Fig. 7.8** for different n and amplitudes $\hat{i}_\mathrm{L}$ of the sinusoidal load current, and a DC-link voltage of 400 V with a PWM frequency of 200 kHz. Note that these are the averaged transistor losses over one load current fundamental period. From this analysis, it emerges that a single *GS66508T* transistor is the optimal selection for the operation with $\hat{i}_\mathrm{L} \approx 20$ A at the indicated DC-link voltage and switching frequency. The extension of load current capability can similarly be achieved by introducing more interleaved HBs instead of paralleled transistors [125].

7.2 Feedback and Control System

In order to increase the amplifier's reference tracking and disturbance attenuation performance, a closed-loop digital feedback control system is used [231]. Its structure is illustrated in **Fig. 7.9**. To stabilize this multiple-input and multiple-output system, three cascaded controllers are employed as shown. A type-III (lead-lag) controller acts on the amplifier's precision output load current. It provides the two phase voltage references for the two proportional-integral (PI) phase voltage controllers. The innermost control loop consists of proportional (P) controllers that regulate the four HB currents. The models of the dynamic systems are given in Sec. 7.2.3 below.

Such linear controllers are quickly understood and tuned, and can be stabilized well during critical operating conditions, e.g., by using integrator anti-windup techniques, when voltages or currents in the plants (i.e., the controlled dynamic systems) saturate. This can, e.g., be the case if the HB duty cycles reach 0 or 1 [100]. Furthermore, the controller tuning objectives with respect to bandwidth and stability are simple to formulate and optimize, as

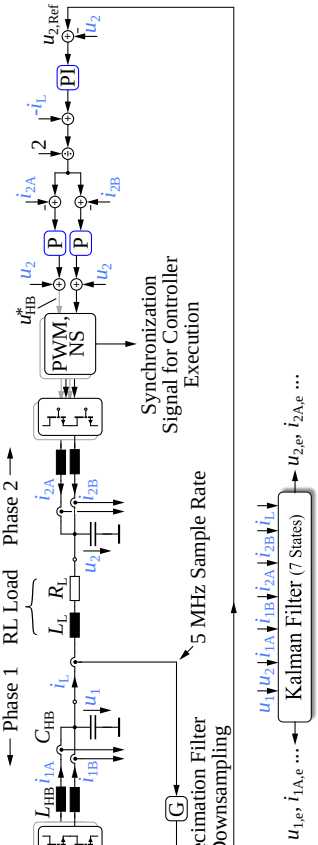

Fig. 7.9: Control system structure of the hardware demonstrator. The control topology consists of three cascaded controllers with feedforward (FF) compensation. Proportional (P) current controllers are used for the four HB currents, proportional-integral (PI) voltage controllers for the two phase voltages and a type-III (lead-lag) controller for the load current. The Kalman filter provides low-noise estimates of the measured values, and can be disabled. The pulse-width modulators employ digital noise shapers (NS) for quantization noise reduction. A feedforward path is also used for the requested load voltage to improve the tracking performance.

shown in Sec. 7.2.3 below. This is harder to achieve with other control schemes such as state-space controllers (e.g., linear-quadratic regulators). Furthermore, the performance of the utilized cascaded controllers is expected to be similar with respect to disturbance rejection and reference tracking to what a state-space controller design can achieve [100, 232, 233]. Advanced mathematical methods for controller tuning, such as H_∞-methods, are not considered due to the required complexity to appropriately form the optimization goals and to find the corresponding solutions. A model predictive controller (MPC) would be well suited due to its capability of considering constraints [234]. However, the required computational complexity renders it difficult to employ in systems that must be controlled with high execution rates (e.g., 200 kHz in the demonstrator system).

In the described cascaded control system, the intricacies of the employed controllers increase with the dynamics of the controlled plants, i.e., the HB current controller is a simple P-controller, whereas the load current lead-lag controller, whose plant dynamics include the responses of the two inner control loops as well as the load, contains more poles/zeros to be able to provide sufficient stability and open-loop gain, which improves reference tracking and disturbance rejection.

Sensor noise is critical in any feedback control system and hence, a Kalman filter, which is capable of reducing residual sensor noise, can be employed to provide the feedback signals for the controllers. Its details and implementation, as well as performance results, are further presented in Ch. 8.

The control algorithms are implemented using digital logic circuits (provided by an FPGA) as a discrete-time system. They are executed synchronously to the converter PWM, i.e., at the start of a new PWM period, all required measurements for the feedback controllers are obtained, their outputs are calculated, the noise shapers are updated and finally, new duty cycles are applied in the subsequent PWM cycle (regular symmetric PWM sampling [95]). In the following, details of the utilized modulators and noise shapers are given.

7.2.1 Gate Control Signal Modulation

The power switch control signals are generated with digital pulse-width modulators that are based on triangular carriers and regular symmetric sampling once per cycle (see Sec. 5.1 and [95]). Compared to asymmetric sampling, where the modulator reference is updated twice in each PWM period, symmetric sampling results in a less nonlinear modulator, which reduces baseband noise when its reference input is supplied by a noise shaper, as discussed

in Sec. 5.2. In contrast to other modulation methods such as self-oscillating concepts [235] or click modulation [236], this proven approach provides a constant pulse repetition rate (which is advantageous for the digital control system, as it is then executed regularly) and the high-frequency spectrum of the power stage output signals can be determined analytically, which facilitates the design of the converter's EMI filter [95]. Furthermore, modulated signals with a sufficiently low harmonic distortion (in the low-frequency baseband) can be created with this method, due to the fact that the ratio of the PWM frequency (up to 200 kHz) to the fundamental frequency of the modulated signal is generally high (>500). Details of this modulation method are also shown in Sec. 5.1, where its fundamental resolution limits that deteriorate the achievable SNR of the modulated waveforms, are revealed.

Consequently, digital noise shapers, which provide low-resolution input signals for each pulse-width modulator, are used to shift quantization noise to frequencies above 10 kHz, where it is of no concern to the discussed mechatronic applications. The details of this method and the employed digital implementation are given in Ch. 5. In the amplifier demonstrator, the noise shapers can be bypassed to investigate the noise performance of regular PWM. Unless otherwise stated with the measurement results below, they are always activated.

Each HB is controlled by its own set of noise shaper and pulse-width modulator, which are both implemented in an FPGA and operated with a digital clock frequency of 200 MHz. The pulse-width modulators employ digital counters with signal widths of 9 bits and 10 bits, which correspond to counter top values of 511 and 1023. Due to the triangular carrier (i.e., the counter counts from zero to top and back to zero during one PWM cycle), this results in pulse repetition frequencies f_{PWM} of 195.7 kHz and 97.8 kHz, respectively (cf. (5.2) in Sec. 5.1). For the remainder of this work, these frequencies are rounded and referred to as 100 kHz and 200 kHz. The feedback control system is executed with the same frequency, except when the Kalman algorithm is enabled with $f_{\mathrm{PWM}} = 200\,\mathrm{kHz}$, where it updates the PWM references at a rate of 100 kHz (e.g., every second PWM cycle), as the Kalman algorithm requires more time to compute (see Ch. 8).

7.2.2 Sensors and Signal Processing

To increase the control system's flexibility with respect to different control topologies, and to decouple the cascaded control loops dynamically, each

system state, i.e., the four HB currents, the two phase voltages and the load current, as well as the DC supply voltage, are measured.

Sensor noise critically affects the closed-loop feedback system and hence, low-noise voltage and current sensors with optimized signal processing circuits (filters/amplifiers) are used, as described in Ch. 6. All analog-to-digital converters feature amplitude resolutions of 16 bits and maximum sample rates of 1 MHz, except for the load current ADC, which is an 18-bit device capable of sampling at a rate of 5 MHz. To minimize the intrinsic noise of this sensor, oversampling with an optimized decimation filter, as shown in Sec. 6.4, is employed. The 16-bit, synchronously sampling ADCs are selected to reduce circuit complexity. As shown in Ch. 8, a Kalman filter is effective, as it can further reduce sensor noise. Oversampled high-resolution, high-frequency ADCs could be used for all measurements, which would, however, increase the system cost and complexity markedly.

All currents are measured using shunt resistors (with isolated ADCs), as they show a superior noise and distortion performance compared to other, integrated solutions (see Sec. 6.1). The four sensors for the HB currents are galvanically isolated as illustrated in Sec. 6.5. The utilized signal isolators for the data transmission of these ADCs are *Analog Devices ADuM131E*, which feature a low RMS jitter of 16.4 ps (cf. **Fig. 4.5**). Thus, they effectively eliminate jitter-related sampling noise, as shown in Sec. 6.5. This isolator cannot be used to isolate gate control signals due to its insufficient CM transient immunity, which is however of no concern for the HB current measurement ADCs, as they are placed after the first HB filter stage (see **Fig. 7.9**). The DC-link and phase voltages, which can reach values up to 400 V, are measured with resistive dividers that are optimized for low noise and distortion, as derived in Sec. 6.2.

The ADCs for the four HB currents, the two phase voltages and the DC-link voltage sample synchronously with the PWM carriers, with the result that the acquisition of their input voltages occurs once every PWM period at time instants where no switching actions of the power converter take place, which can potentially influence the measurements with high-frequency radiated or conducted emissions. Consequently, no anti-aliasing filters are used for these ADCs, as it is assumed that there is no high-frequency signal content in their input voltages that could create aliasing artifacts in the digitized signals [184]. This also improves the dynamics of the closed-loop feedback system, as there are no phase delays in the feedback paths. Furthermore, the ripple component of the HB currents and phase voltages are not recorded with this sampling method.

Conversely, the oversampled load current ADC acquires its samples asynchronously to the converter switching actions and thus, it employs an analog anti-aliasing filter (6^{th}-order Butterworth with an attenuation of −3 dB at 430 kHz), and the sensing circuit is placed in a shielding enclosure. This shunt-based sensor utilizes four paralleled 50 mΩ shunt resistors to reduce their thermal distortion (cf. Sec. 6.1) and is capable of measuring THD down to a level of ≈−110 dB, which is mainly limited by the operational amplifiers used to provide the required gain and buffering in the anti-aliasing filter (*LT1028A* and *AD8620*, see Sec. 6.3.1). This is sufficient for the demonstrated performance, as the achievable load current THD of the power converter is limited by other influence factors, such as HB dead time.

An FPGA is well suited to acquire and process the high-speed, high-resolution data streams from the individual ADCs, which results in an overall data rate of 112 Mbit/s when operating with $f_{\text{PWM}} = 200$ kHz. However, some control tasks, like a Kalman filter, are implemented with less complexity as a procedural program that also achieves a high numerical accuracy due to the usage of floating-point arithmetic. Consequently, the converter's digital processing system employs a *Xilinx Zynq Z-7020* system on a chip (SoC), which combines an FPGA with two 666 MHz *ARM Cortex-A9* CPUs, and which features high-performance floating-point coprocessors. As shown with the Kalman filter implementation in Ch. 8, fast data transfers between the FPGA and the CPUs are important to achieve a good control performance, which is facilitated by the possibility of the *Zynq* to transfer data coherently between the FPGA fabric and the CPU L2-cache, hereby minimizing latency [237]. A 1 GiB DDR3 memory is connected to the processing system, which allows the recording of large amounts of internal data, such as ADC samples. Furthermore, a 100 Mbit/s optical Ethernet link (100BASE-FX) facilitates the transmission of such data to an external computer for further analysis and processing. An additional optically isolated serial interface is used for the transfer of commands that control the amplifier, e.g., to set load current references or to start/stop converter operation.

The feedback controllers of the demonstrator system are implemented with digital logic in the processing system's FPGA and are based on fixed-point arithmetic. This is done to achieve high control system execution rates (400 kHz are achieved as shown with measurements below). However, it requires a more complex design process as compared to a control system implementation based on procedural programs, as digital logic circuits must be carefully tested and verified to ensure their functionality. In the following, the design of the feedback controllers is presented in detail.

7.2.3 Control System Model

The discussed switch-mode power converter comprises a continuous-time, analog power stage and a discrete-time digital control system. This constitutes a mixed continuous/discrete system, whose rigorous analysis requires specialized tools and methods, and is often done with numeric system simulations. In order to be able to apply traditional linear control system analysis methods, which are sufficient to reveal important dynamics and performance figures, the control system and the description of the physical plants are approximated and modeled as continuous-time systems. The controllers are tuned with the methods described below, and then transformed into discrete-time representations that can be implemented digitally. Due to the synchronous sampling of the sensors, the acquired measurements closely follow the averaged waveforms over a switching period and hence, ripple components of waveforms that are relevant for control, caused by the switch-mode nature of the power stage, are not measured. This is according to the *small-aliasing approximation* described in [184]. Thus, a continuous-time averaged model of the converter is used for its linear description, which considers system dynamics well below the switching frequency [87, 184]. After modeling, tuning and time-discretization of the controllers, the performance of the mixed continuous/discrete system is verified using computer circuit simulations that can consider both the discrete- and continuous-time systems in order to verify the expected performance and the validity of the approximations [129].

The delay of the PWM and the control system calculation time contribute to the loop delay of the dynamic system, which reduces the phase margins of the controllers and must be considered to obtain a sufficiently accurate approximation of the averaged converter models, as shown in the following [184].

PWM Delay

Fig. 7.10 illustrates a simplified and reduced model of the demonstrator feedback control system. The gain of the proportional HB current controller could be selected arbitrarily high if there was no delay in this controller's plant (which comprises the pulse-width modulator, the HB power stage and its inductor). This is due to the fact that this controller's plant exhibits only a first-order integrative characteristic (see (7.2) below). However, the time delay in the forward path of this control loop, which is caused by the PWM sampling action, directly limits the achievable gain of the P-type current controller, as it reduces its phase margin [100, 184]. As indicated in **Fig. 7.10** with a

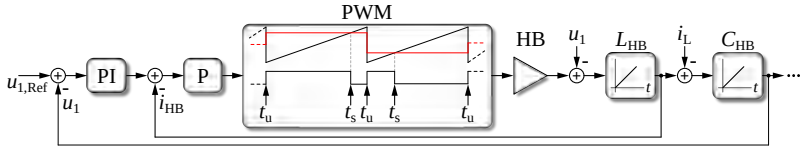

Fig. 7.10: Simplified and reduced control system structure (cf. **Fig. 7.9**). At time instants t_u, the PWM input signal is updated (regular sampling with a sawtooth carrier [95]). At t_s, the HB switches the first time after t_u and changes its output voltage. With this modulation method, the delay $t_s - t_u$ depends on the duty cycle.

sawtooth carrier, this delay, $T_{D,PWM}$, depends on the momentary modulator duty cycle, as indicated with the varying time difference $t_s - t_u$, where t_u denotes the time instants where the PWM reference is updated (regular sampling), and t_s indicates the points in time when the HB changes its output for the first time after the start of the PWM period. This amplitude dependency renders the delay behavior of the PWM nonlinear. The detailed modeling and description of this delay depends on the type of modulator and has been extensively analyzed [116–119, 184]. However, in the demonstrator system, which features a symmetrical modulator (i.e., a triangular PWM carrier), this modulation delay is constant and equivalent to one half of the PWM period time: $T_{D,PWM} = T_{PWM}/2$ [184].

Total Forward Path Delay

Apart from the PWM delay $T_{D,PWM}$, the time required for the control system to calculate the updated duty cycles according to the control laws, $T_{D,Ctrl}$, also has to be considered to properly approximate the phase response of the dynamic system. The sum $T_{D,PWM} + T_{D,Ctrl} = T_{Fwd}$ is the total delay in the forward path of the control system plant.

As the control algorithms are implemented with digital logic, they can be executed at a high frequency. If the Kalman filter is disabled, the calculation of the updated duty cycles requires less than one PWM cycle (for the considered PWM frequencies up to 200 kHz). **Fig. 7.11 (a)** illustrates the process. At the time instant t_{u1}, the measurements of the required voltages and currents are obtained. This provides the errors for the individual controllers, whose calculation starts subsequently and finishes before the next time instant t_{u2}. At that instant, the newly calculated duty cycles are available and the pulse-width modulator inputs are updated accordingly, while the measurements for the next control cycle are obtained. Consequently, $T_{D,Ctrl} = T_{PWM}$. This

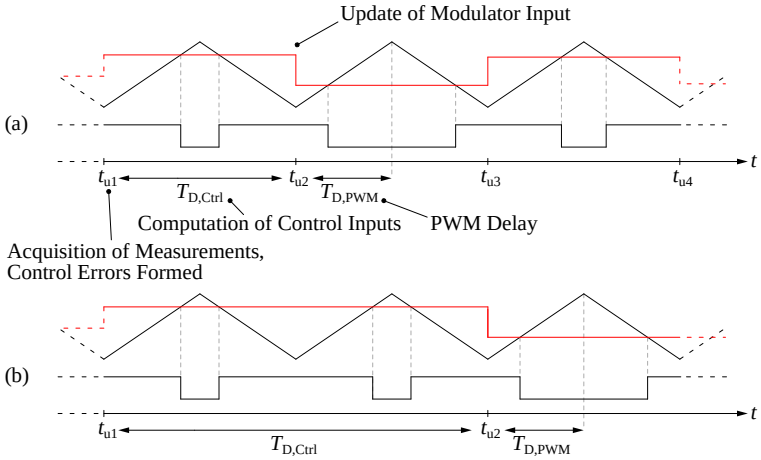

Fig. 7.11: Time delay model for the control system. The total delay is $T_{\mathrm{Fwd}} = T_{\mathrm{D,Ctrl}} + T_{\mathrm{D,PWM}}$. **(a)** The controller implementations require less than one PWM period to calculate the next duty cycles. **(b)** If the Kalman filter algorithm is executed with $f_{\mathrm{PWM}} = 200\,\mathrm{kHz}$, two PWM cycles are required to provide the next control inputs.

also applies if the Kalman filter is enabled and the PWM frequency is set to 100 kHz. However, if $f_{\mathrm{PWM}} = 200\,\mathrm{kHz}$ and the Kalman algorithm is executed, which requires more time, the control system is executed as illustrated in **Fig. 7.11 (b)**, where two PWM periods are required for $T_{\mathrm{D,Ctrl}}$. **Tab. 7.2** summarizes the resulting delays as used for the control system model in the hardware demonstrator system.

Consequently, the execution rate of the control system affects the achievable control performance and should be maximized. This corroborates the use of fast-switching GaN power transistors that facilitate high-frequency operation due to their comparably low losses, and a capable digital signal processing unit. In the following, the derived delays are employed in the models of the linear systems that are used to design the feedback controllers.

Controller and Plant Models

As all system states (i.e., capacitor voltages and inductor currents) are available to the control system, the individual control loops can be dynamically

Tab. 7.2: Control system operating modes as used in the hardware demonstrator system and for the tuning of its feedback control systems. The Kalman filter requires less than 8 µs for the computation of the estimates.

$f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}}$	Kalman	$T_{\mathrm{D,Ctrl}}$	$T_{\mathrm{D,PWM}}$	T_{Fwd}
100 kHz	OFF	T_{PWM}	$T_{\mathrm{PWM}}/2$	$3/2 T_{\mathrm{PWM}} = 15\,\mu\mathrm{s}$
100 kHz	ON	T_{PWM}	$T_{\mathrm{PWM}}/2$	$3/2 T_{\mathrm{PWM}} = 15\,\mu\mathrm{s}$
200 kHz	OFF	T_{PWM}	$T_{\mathrm{PWM}}/2$	$3/2 T_{\mathrm{PWM}} = 7.5\,\mu\mathrm{s}$
200 kHz	ON	$2T_{\mathrm{PWM}}$	$T_{\mathrm{PWM}}/2$	$5/2 T_{\mathrm{PWM}} = 12.5\,\mu\mathrm{s}$

decoupled, which simplifies controller tuning and increases the achievable control bandwidths.

Consequently, as illustrated in **Fig. 7.9**, the dynamic system description of the plant of each proportional HB current controller is given in the Laplace domain, where s is the complex frequency parameter, as

$$G_1 = \frac{1}{sL_{\mathrm{HB}}} \mathrm{e}^{-sT_{\mathrm{Fwd}}}. \tag{7.2}$$

The output of the P controller is, due to the knowledge of the phase voltage (u_1 or u_2), directly the required voltage across the inductor L_{HB}. Due to the small-signal approximation described above, the HB power stage is modeled as an ideal voltage source. T_{Fwd} comprises the aforementioned PWM delay and the time required for the execution of the control algorithms (cf. **Tab. 7.2**). As the control system is executed synchronously with the PWM carriers, and the HB current sensors, as well as the phase voltage sensors, do not incorporate anti-aliasing filters, no phase delay is assumed in the feedback path of this control loop. Hence, the open- and closed-loop transfer functions of the proportional HB current controller are given as

$$G_{\mathrm{Pctrl,OL}} = K_{\mathrm{P}} G_1, \tag{7.3}$$

$$G_{\mathrm{Pctrl,CL}} = \frac{G_{\mathrm{Pctrl,OL}}}{1 + G_{\mathrm{Pctrl,OL}}}, \tag{7.4}$$

where K_{P} is the controller gain.

As the load current is also known to the control system, the plant of the PI phase voltage controller can be dynamically decoupled, and its description

is as follows:

$$G_2 = G_{\mathrm{Pctrl,CL}} \frac{1}{sC_{\mathrm{HB}}}. \tag{7.5}$$

Similarly, as with the P-controllers, there is no dynamics in the feedback path of this controller due to the lack of sensor anti-aliasing filters and hence, the open- and closed-loop transfer functions of the PI phase voltage controller are given as

$$G_{\mathrm{PIctrl,OL}} = K_{\mathrm{PI}} \left(1 + \frac{1}{sT_{\mathrm{PI}}}\right) G_2, \tag{7.6}$$

$$G_{\mathrm{PIctrl,CL}} = \frac{G_{\mathrm{PIctrl,OL}}}{1 + G_{\mathrm{PIctrl,OL}}}, \tag{7.7}$$

with K_{PI} and T_{PI} being the PI controller parameters.

Finally, the type-III load current controller requests, through the PI phase voltage controllers, the desired load voltage in order to fulfill its control objective. The dynamic system description of its plant incorporates the dynamics of the inner control loops and the load:

$$G_3 = G_{\mathrm{PIctrl,CL}} \frac{1}{R_{\mathrm{L}} + sL_{\mathrm{L}}}. \tag{7.8}$$

The transfer function of the type-III controller is given by [87]

$$G_{\mathrm{TIIIctrl}} = K_{\mathrm{TIII}} \frac{\left(1 + \frac{T_{\omega z1}}{s}\right)\left(1 + \frac{s}{T_{\omega z2}}\right)}{\left(1 + \frac{s}{T_{\omega p1}}\right)\left(1 + \frac{s}{T_{\omega p2}}\right)}, \tag{7.9}$$

with K_{TIII}, $T_{\omega z1}$, $T_{\omega z2}$, $T_{\omega p1}$ and $T_{\omega p2}$ being the controller's five tuning parameters. Consequently, the open- and closed-loop transfer functions of this control loop are as follows:

$$G_{\mathrm{TIIIctrl,OL}} = G_{\mathrm{TIIIctrl}} G_3 G_{\mathrm{AA}} \mathrm{e}^{-sT_{\mathrm{Decim}}}, \tag{7.10}$$

$$G_{\mathrm{TIIIctrl,CL}} = \frac{G_{\mathrm{TIIIctrl}} G_3}{1 + G_{\mathrm{TIIIctrl,OL}}}. \tag{7.11}$$

This controller's load current sensor incorporates an oversampled ADC that operates asynchronously to the PWM cycles of the power converter, with a sampling rate of 5 MHz. Consequently, an analog anti-aliasing filter is required for the ADC to prevent the acquisition of undesired radiated or conducted spurious signals caused by the fast switching transitions of the

HBs. The transfer function G_{AA} of this filter is given by the Butterworth filter of 6^{th} order, a $-3\,\mathrm{dB}$ passband frequency of 430 kHz and a $-90\,\mathrm{dB}$ stopband attenuation reached at 2.5 MHz, which corresponds to the employed physical analog filter. Furthermore, a digital Chebyshev Type 2 IIR low-pass decimation filter is used, as described in Sec. 6.4.1. This filter is modeled with a constant time delay of T_{Decim} due to its nearly linear phase behavior at low frequencies. If the converter operates at $f_{\mathrm{PWM}} = 200\,\mathrm{kHz}$, which corresponds to an oversampling ratio of $\mathrm{OSR} = {}^{5\,\mathrm{MHz}}/_{200\,\mathrm{kHz}} = 25$, the decimation filter adds a phase delay of $T_{\mathrm{Decim}} \approx 12\,\mu\mathrm{s}$, which is obtained by optimizing the filter as shown in Sec. 6.4.1, with a maximum filter order of 30. Similarly, with $f_{\mathrm{PWM}} = 100\,\mathrm{kHz}$, the delay is given as $T_{\mathrm{Decim}} \approx 24\,\mu\mathrm{s}$.

To reduce the steady-state tracking error of the load current, the load voltage is also determined by a feedforward term, whose value is derived (also during converter operation synchronously with the entire control system) from the requested load current and the load inductance L_{L} and resistance R_{L}, which is also illustrated in **Fig. 7.9**.

Controller Tuning

The individual feedback loops are tuned, using loop shaping, to achieve an open-loop phase margin of at least 50° and a gain margin of more than 6 dB, which ensures fast dynamic responses without excessive transients [87, 100]. While this is possible to be done manually (e.g., with the symmetrical optimum method [238]), numeric optimization methods can achieve a better overall performance, as the presented control system incorporates numerous dynamics that render a manual tuning approach exhaustive. Additionally, complex optimization goals and constraints can be formulated and pursued. Consequently, the eight tuning parameters of the controllers, as described above, are determined using numerical optimization algorithms [198, 239]. The optimization objective is the maximization of the integral of the open-loop transfer function magnitude of the load current controller and its plant, over a frequency interval from 1 Hz to the crossover frequency, while respecting the aforementioned phase and gain margins. **Fig. 7.12** illustrates this with the shaded area. This ensures high open-loop gains, which is a measure of a controller's disturbance rejection capability, and high crossover frequencies (i.e., the frequency at which the open-loop magnitude falls below 0 dB) [87]. Apart from the mentioned stability margins, another controller tuning constraint is given by a requirement on the crossover frequencies of two adjacent control loops, which are to be separated by at least a factor of 2, e.g., the crossover frequency of the PI phase voltage control loop must be

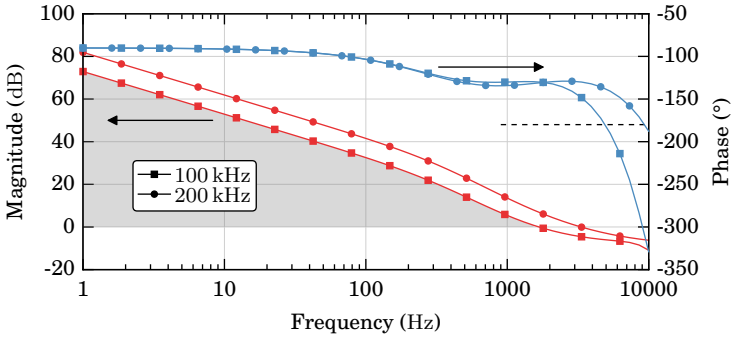

Fig. 7.12: Open-loop bode plots of the type-III load current controller and its plant ($G_{\mathrm{TIIIctrl,OL}}$) for PWM frequencies of 100 kHz and 200 kHz (which correspond to the control system execution frequencies). 5 Ω+2.5 mH load configuration. The shaded area is maximized by controller tuning.

at least twice as high as the crossover frequency of the type-III load current controller and its plant. This factor is chosen experimentally and ensures some dynamic separation of the control loops, which reduces overshoot of the step responses and gain peaking of the closed-loop transfer functions to values below ≈2 dB. The tuned continuous-time controllers are then discretized such that they can be implemented as digital control algorithms.

As shown above, the PWM frequency of the power converter influences the achievable performance of the feedback control system, as with a reduced PWM delay at higher pulse repetition frequencies, an increased open-loop gain can be achieved for a given required phase margin. **Fig. 7.12** exemplarily shows the difference in achievable control system performance when the type-III controller is tuned for a PWM rate of 100 kHz and 200 kHz. The open-loop gain is ≈9 dB larger when the converter (and the control system) operate at 200 kHz instead of 100 kHz. **Tab. 7.3** lists the crossover frequencies, as determined by the described controller tuning method, of the open-loop transfer functions that comprise the controllers and the respective system plants, with the three different loads that are used with the demonstrator system (see Sec. 7.5 below for further details on the load selection).

In the following, the closed-loop feedback control system is used in a comprehensive computer circuit simulation of the hardware demonstrator to determine the impact of thermal transistor on-state resistance modulation on the amplifier load current THD.

Tab. 7.3: Achieved open-loop controller crossover frequencies for the different control system execution rates of the hardware demonstrator. For example, the open-loop transfer function of the type-III controller is given by $G_{\mathrm{TIIIctrl,OL}}$, as shown with (7.10).

Load	f_{PWM}	f_{Ctrl}	Controller Crossover Frequencies P-Ctrl	PI-Ctrl	T-III
2 Ω+10 mH	100 kHz	100 kHz	7.2 kHz	3.6 kHz	1.7 kHz
2 Ω+10 mH	200 kHz	100 kHz	8.7 kHz	4.0 kHz	2.0 kHz
2 Ω+10 mH	200 kHz	200 kHz	14.4 kHz	6.2 kHz	3.1 kHz
5 Ω+2.5 mH	100 kHz	100 kHz	7.2 kHz	3.4 kHz	1.7 kHz
5 Ω+2.5 mH	200 kHz	100 kHz	8.7 kHz	4.3 kHz	2.2 kHz
5 Ω+2.5 mH	200 kHz	200 kHz	14.4 kHz	6.7 kHz	3.3 kHz
10 Ω+100 µH	100 kHz	100 kHz	7.2 kHz	3.3 kHz	1.6 kHz
10 Ω+100 µH	200 kHz	100 kHz	8.7 kHz	4.3 kHz	2.2 kHz
10 Ω+100 µH	200 kHz	200 kHz	14.4 kHz	6.9 kHz	3.5 kHz

7.3 Distortion due to Thermal Modulation of Transistor $R_{\mathrm{DS,on}}$

The switching and conduction losses, as well as the thermal model of the utilized power transistor, as presented in Sec. 7.1.1, enable detailed insights into the time-domain behavior of each transistor's junction temperature. Consequently, the variation of the $R_{\mathrm{DS,on}}$ is also determinable, which allows the investigation of the distortion caused by this effect in the amplifier output current. This approach is similar to the analysis performed in Sec. 3.2, however, in the following, the closed-loop control system of the power amplifier, as described in Sec. 7.2, is also considered. Furthermore, this investigation includes the complete circuit of the demonstrator amplifier. Time-domain waveforms that are obtainable with the simulation model are illustrated in **Fig. 7.6** above.

Fig. 7.13 (a) visualizes the simulated load current THD of the hardware demonstrator. In order to visualize the effect of the $R_{\mathrm{DS,on}}$ modulation, the simulations are also performed with constant, temperature-independent on-state resistances. Both the regular interleaved HB and the DB topologies are considered. Note that, to reduce simulation complexity, the power semiconductor switching actions are assumed ideal. Consequently, the indicated

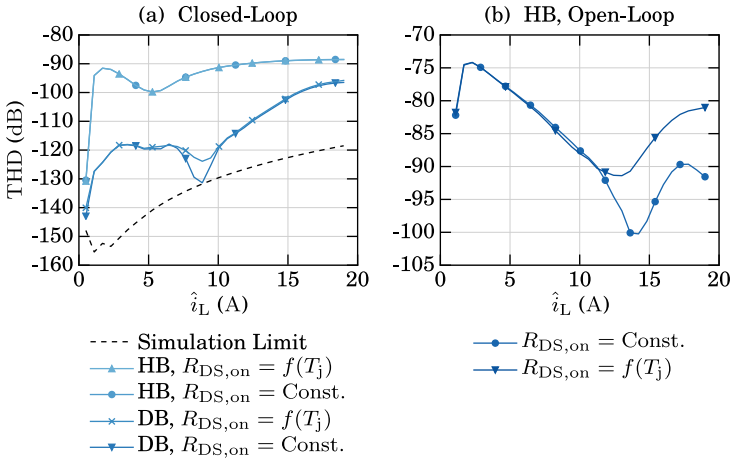

Fig. 7.13: Simulated THD of the hardware demonstrator load current, considering the regular interleaved HB and DB topologies, and incorporating thermal $R_{\mathrm{DS,on}}$ modulation. **(a)** Enabled closed-loop feedback control, $T_{\mathrm{D}} = 40\,\mathrm{ns}$. **(b)** Open-loop operation, $T_{\mathrm{D}} = 10\,\mathrm{ns}$. The simulation limit is the best achievable THD with an ideal amplifier model, only restricted by the simulation time step.

THD values are not directly comparable to measurements obtained from the hardware system, but they reflect the influence of the variation of the $R_{\mathrm{DS,on}}$ on the load current THD, which is the aim of this analysis.

It shows that the variation of the junction temperature and the resulting change in $R_{\mathrm{DS,on}}$ has only a negligible effect on the distortion of the closed-loop converter system, even at high load currents and with the DB topology, which causes a significantly larger $R_{\mathrm{DS,on}}$ variation, as shown in Sec. 7.1.1. The influence of the thermal on-state resistance modulation on THD manifests only when the closed-loop control system is not utilized, as **Fig. 7.13 (b)** illustrates. However, in order to visualize the minuscule effects on THD during open-loop operation at all, the dead time is reduced in the simulation to a very low value of 10 ns, as otherwise, the harmonic distortion related to the HB dead time dominates.

Thus, it can be concluded that the thermal dependency of the $R_{\mathrm{DS,on}}$ does not significantly contribute to the output THD in the load current range of the demonstrator system, even during open-loop operation, as other non-linearities, most notably dead time, give rise to more prominent distortion components.

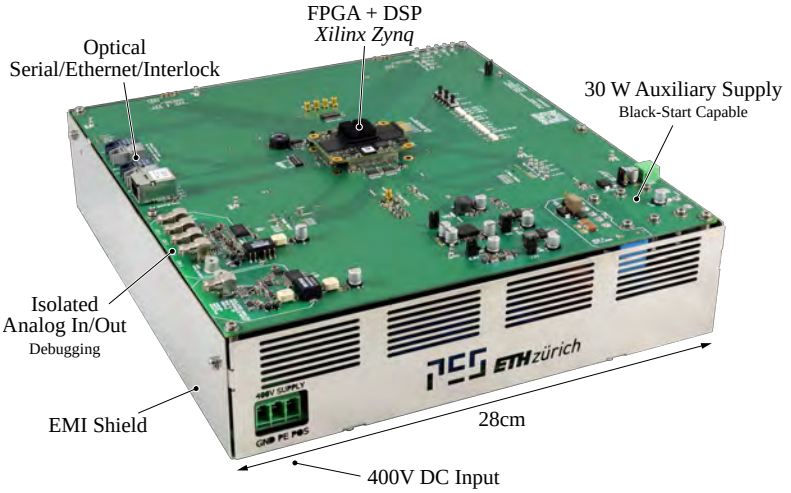

Fig. 7.14: Hardware demonstrator system. It operates with an input voltage up to 400 V DC and is capable of driving a single-phase bridge-tied load with a maximum current amplitude of 25 A. GaN power transistors facilitate high switching frequencies up to 200 kHz while achieving low losses and low distortion. A high-performance digital signal processing system enables high-gain feedback controllers.

7.4 Construction

The hardware demonstrator is depicted in **Fig. 7.14**. A sheet metal housing is used to provide shielding against external sources of electromagnetic noise and to define the parasitic capacitances from the switching stages to protective earth, which are important influence factors for the conducted EMI performance [240]. Digital fiber optical links enable galvanically isolated communication channels with the amplifier, which also facilitates the possibility for high-speed data download (100 Mbit/s). A black-start capable integrated auxiliary supply (*VICOR V375C15C75BL*) is connected to the 400 V DC input and provides ≈15 W of power for the four cooling fans and the digital control and acquisition systems.

In **Fig. 7.15**, the housing and the control PCB are removed to reveal the power stage. Each HB is cooled from the top side with a spring-loaded heat sink that comprises a copper base plate and aluminium fins. Four 40 mm fans provide air flow. The 18-bit load current sensor is placed on a separate PCB in a copper shielding enclosure. A considerable amount of volume is required

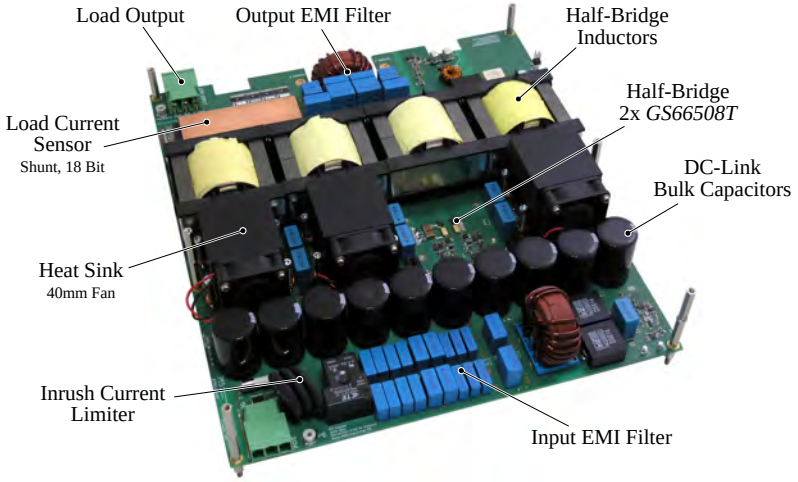

Fig. 7.15: The hardware demonstrator without the control board and the EMI shielding case. The heat sink of one HB is removed. The isolated load current ADC resides on a separate PCB and is contained in its own EMI shielding case, as it acquires data asynchronously to the converter's switching actions.

for the highly linear HB inductors that comprise gapped ferrite cores. The communication between the power board and the control PCB is achieved through five small individual PCBs that can be plugged vertically into *PCI Express* connectors between the two boards. This ensures the signal integrity of the serial high-speed ADC data interfaces and the gate control signals. Various safety features such as the detection of excessive currents, voltages or temperatures, as well as a fiber optical interlock loop, are provided.

7.5 Measurement Methods

The methods described in the following are used to obtain all measurements of the hardware demonstrator. The presented amplifier is capable of supplying an output current with very low distortion and noise. Consequently, a sufficiently linear and low-noise sensor is required to accurately obtain a reference current measurement for verification purposes. Thus, a *LEM IT 65-S* flux-gate current transducer is used to accurately obtain the amplifier load current THD and SNR [214]. Three primary winding turns enable the full uti-

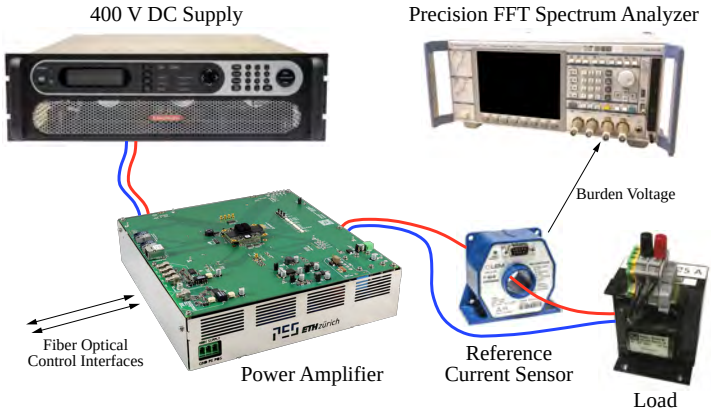

Fig. 7.16: Measurement arrangement used to obtain amplifier performance figures. The *LEM IT 65-S* reference current sensor is a highly linear low-noise device. The *Rohde&Schwarz UPV* spectrum analyzer measures the output voltage of the precision current sensor and calculates the SNR and THD of the load current.

lization of the sensor's range. Its burden resistor, which is used to transform the sensor's current output to a measurable voltage, has a value of 47 Ω and consists of ten paralleled through-hole metal film resistors to minimize their power dissipation and thus, maintain linearity. Note that this sensor was also considered in the current sensor analysis of Sec. 6.1.2. There, its recorded performance is not as high as in the configuration used here due to the fact that only one primary turn was used to directly compare it to similar sensors, and the burden resistor was more nonlinear, which emphasizes the necessity of a careful sensor selection process.

The sensor's burden voltage is measured with a *Rohde&Schwarz UPV* audio analyzer, which is a low-noise high-precision spectrum analyzer with a high input impedance (100 kΩ) [183]. The THD and SNR are measured as described in Sec. 2.1, whereas for the THD, the first 8 harmonics are considered, and the SNR figure includes noise in a frequency band from 10 Hz to 10 kHz. This setup can accurately measure THD levels as low as ≈−108 dB (that are dominated by odd harmonics caused by the sensor itself), which is sufficiently accurate for the presented measurements. Considering only even harmonics, the sensor is capable of measuring THD of less than −110 dB. This current transducer is also able to measure SNR values in excess of ≈108 dB. These performance figures are similar to what current sensing shunt resistors can

achieve (cf. Sec. 6.1.1). However, the cost, volume and power consumption of the integrated sensor are considerably higher than that of a shunt-based solution, which is the reason why this transducer is only used as reference current sensor and not within the amplifier itself. The measurement setup is illustrated in **Fig. 7.16**.

In order to measure the amplifier output THD and SNR, a digital sinusoidal load current reference is created ($i_{\mathrm{L,Ref}}$, see **Fig. 7.9**), with a fundamental frequency f_{F} of either 35 Hz or 210 Hz. The amplifier then also creates a load current with the same fundamental frequency. This selection of f_{F} ensures that its low-order integer harmonics do not interfere with the 50 Hz grid harmonics that are being coupled into the *LEM* reference current sensor through external stray fields, but are not present in the actual load current (as determined by experimental validations). Furthermore, these frequencies are in the range of common actuator current frequencies used in positioning applications. In the digital signal processing system, the numeric values of the digital load current reference waveforms are represented as µA in fixed-point arithmetic, and quantized with an amplitude resolution of 32 bits. They contain no significant harmonics or noise. Unless otherwise stated, the digital noise shapers are enabled and the Kalman filter algorithm is not executed. Furthermore, the regular interleaved power stage topology with a nominal dead time of 30 ns is employed for most measurements.

The amplifier is loaded with different passive resistive-inductive loads that model common actuators, such as linear motors with or without iron cores, in slowly moving mechatronic positioning systems (i.e., actuator back-EMF is not considered). The load resistors and inductors need to be highly linear as they otherwise introduce undesired distortion components that prevent an accurate evaluation of the converter's inherent linearity. Consequently, for the load resistors, thick film high-power resistors with a low thermal coefficient are used (*Vishay LPS 600*). They implement three different load resistance values of 2 Ω, 5 Ω and 10 Ω. The three corresponding load inductors have values of 10 mH, 2.5 mH and 100 µH respectively. The magnetic cores of the load inductors are made from laminated silicon steel in case of the 2.5 mH and 10 mH inductors (designed for low-frequency power grid applications), whereas the core of the 100 µH inductor is a gapped ferrite. The inductors have a sufficient current and saturation rating in excess of 25 A RMS. Their individual linearities are demonstrated with the measurements below. Note that the load resistors have a limited power dissipation capability which limits the achievable load currents in certain measurement settings.

Two different high-power laboratory DC supplies are employed to provide the amplifier's DC input voltage, an *HP 6035A* (500 V, 5 A) unit and a *Sorensen SGI 600-17* (600 V, 17 A). The *HP* supply has a slightly reduced output noise as compared to the *Sorensen* unit. However, the load current SNR measurements of the amplifier differ by less than ≈1 dB when supplied by either of the two devices (with closed-loop amplifier operation). Similarly, due to the higher output current rating of the *Sorensen* supply, it stabilizes its DC output voltage better. Nonetheless, the THD measurements of the amplifier output current also differ by less than ≈1 dB between the two supplies.

The described measurement method and load configurations are used throughout the following sections and chapters to obtain the amplifier's characterizing noise and distortion figures.

7.6 Experimental Results

In this section, distortion and noise measurements of the demonstrator system are presented. The utilized reference sensors and measurement methods, as well as the load configurations, are outlined in Sec. 7.5 above. As the underlying causes of noise and distortion are generally fundamentally different and independent, the investigation is regarding the noise and distortion of the power amplifier output separately. More experiments, that demonstrate the performance of the Kalman filter and two distortion compensation methods, are presented in Ch. 8 and Ch. 9, respectively.

7.6.1 Distortion Performance

Fig. 7.17 shows the load current THD of the amplifier, operating with the regular interleaved power stage topology, for the three considered loads and different PWM frequencies. The controller gains are adapted for each load configuration and execution frequency as explained in Sec. 7.2. As expected, the load current THD is significantly reduced with higher controller execution frequencies due to the improved open-loop gains of the control loops, which correspond to their disturbance rejection capabilities. However, this only applies for the load configurations that utilize the 2.5 mH or 10 mH laminated iron core inductors. They are less linear (i.e., they show a more current-dependent inductance variation) than the 100 µH gapped ferrite core inductor. This nonlinearity manifests itself as a disturbance to the control system (through the generated harmonics), which is rejected more effectively with higher control gains and consequently, with higher PWM and controller

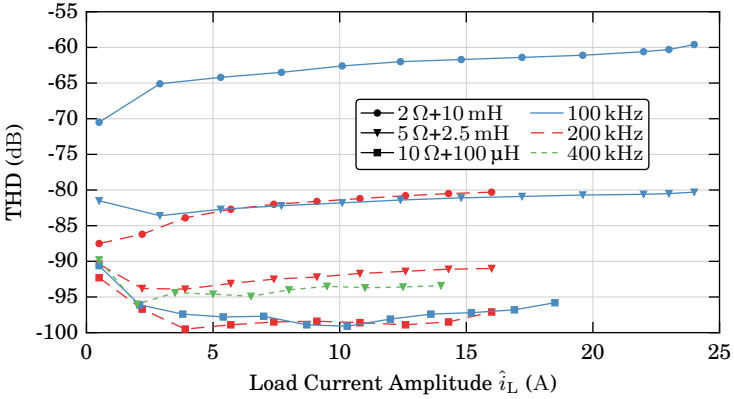

Fig. 7.17: Measured THD of three different loads for control system execution frequencies of 100 kHz, 200 kHz and 400 kHz. Regular interleaved power stage topology. f_F=35 Hz, u_{DC}=400 V, T_D=30 ns. PWM frequencies are (correspondingly) 100 kHz and 200 kHz, whereas the 400 kHz control system rate is achieved by updating the PWM reference twice per switching period. Load currents are limited by the power transistor losses or the load resistor dissipation capabilities.

execution frequencies. The feedback sensors do not limit the achievable THD, as the DB topology, demonstrated below, achieves THD figures below −100 dB. The linearity of the load resistors is also of significance. Wirewound load resistors, which can show a significant thermal coefficient of resistance, introduce considerable harmonics also at high fundamental frequencies (>100 Hz) and thus, precision thick film resistors are used as described in Sec. 7.5. The demonstrated THD figures are independent of the utilized DC-link voltage, e.g., the same results are obtained with a DC-link voltage of 200 V.

In order to double the control system execution rate and correspondingly increase the achievable controller gains, asymmetric regular sampling, where the PWM references are updated twice per PWM cycle, can also be employed [95]. Note that this reduces the effectiveness of the digital noise shapers significantly and is hence not a preferred operating mode (see Sec. 5.2.3). Nonetheless, **Fig. 7.17** also illustrates the controller performance with asymmetric regular sampling, which results in a control system execution frequency of 400 kHz when operating with f_{PWM} = 200 kHz. For this configuration, the feedback controllers have also been tuned as described in Sec. 7.2.3. However, as seen from the measurements, the THD cannot be significantly improved anymore, despite the reduction of the control delay. This is due

to limits of the digital implementation of the controllers in the FPGA fabric as logic circuits based on fixed-point arithmetic. Specifically, the type-III load current controller is realized as an IIR filter that implements this controller's transfer function. As the clock frequency of the FPGA design is set to 200 MHz, to achieve short controller calculation times, it prevents the usage of complex (i.e., wide bit-width) multipliers and adders in order to achieve timing closure of the digital logic. Consequently, for high-gain controller implementations, which are enabled if the control system can be executed with high rates such as 400 kHz, digital signals can saturate or overflow, which subsequently renders the controller unstable. Due to the implementation as IIR filter, it is also difficult to employ stabilizing structures such as anti-windup elements. This further decreases the controller's stability. Consequently, its gains have to be reduced in order to render it stable and hence, the control performance cannot increase arbitrarily. This is a fundamental limitation of controller implementations that are based on digital circuits. It could be overcome by utilizing an FPGA that is capable of processing signals with a sufficient number of bits to prevent saturation or overflow effects, while still utilizing a high digital clock rate of 200 MHz, or even more. An other approach is to implement the controllers with digital logic that handles floating-point numbers, at the cost of an increased digital resource utilization. Similarly, the control algorithms could be executed with a procedural program based on floating-point arithmetic whereas, however, the achievable controller execution rates would be significantly reduced as compared to what is achievable with digital logic designs.

If the fundamental frequency f_F is increased to 210 Hz, the integer harmonics are shifted correspondingly to higher frequencies where the open-loop gains of the controllers are reduced (cf. **Fig. 7.12**). Thus, their disturbance rejection at these frequencies is also diminished, which results in higher harmonic distortion. **Fig. 7.18** reveals measurements of this matter for $f_\mathrm{F} = 210\,\mathrm{Hz}$ and $f_\mathrm{PWM} = 200\,\mathrm{kHz}$, which is compared to the corresponding measurements obtained with $f_\mathrm{F} = 35\,\mathrm{Hz}$ from **Fig. 7.17** above.

These measurements reveal a high sensitivity of the load current distortion to the control system's open-loop gains, which, due to digital implementation limits, cannot be arbitrarily increased. The necessity for linear loads, that otherwise introduce additional undesired distortion, is also demonstrated. The HB dead time for this experiment was set to 30 ns. In the following, the sensitivity of the load current distortion to this key property is measured and discussed.

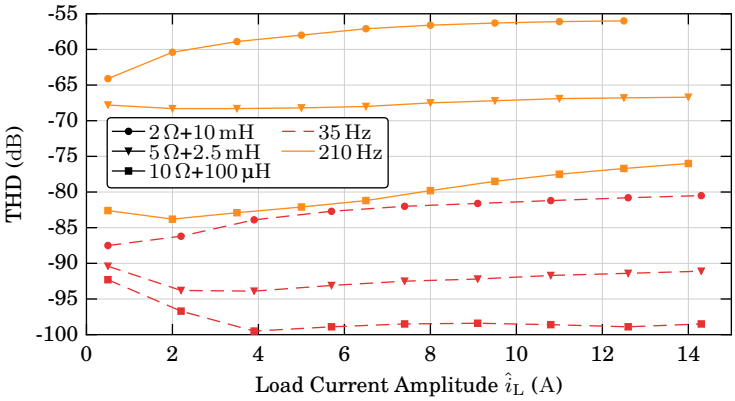

Fig. 7.18: THD measurements at an increased fundamental load current frequency f_F = 210 Hz. f_{PWM} = 200 kHz. The f_F = 35 Hz measurements are the corresponding results from **Fig. 7.17**.

Distortion Due to Dead Time

Using the demonstrator system, the effect of dead time on the amplifier output current distortion, when operating with the regular interleaved HB topology, is investigated. **Fig. 7.19** illustrates the THD for different dead times as a function of the load current amplitude of the 10 Ω+100 µH load. As expected, dead time only affects odd harmonics, as the HB output waveform error is a function of the current polarity, which renders it half-wave symmetrical (see Sec. 2.3). The amplitudes of the even harmonics are constant and independent of dead time, as the indicated logarithmic fit matches well. The odd-order harmonics, which dominate the THD, depend significantly on dead time, which corroborates the expected high sensitivity to this cause of distortion, despite operating the amplifier with the closed-loop control system.

As **Fig. 7.19** illustrates, 30 ns of dead time results in a THD of ≈−100 dB over a wide load current range. Such short dead times are facilitated by the fast HB switching transitions, which take less than 5 ns at a DC-link voltage of 400 V (cf. **Fig. 4.16**). As a high-side HB power transistor requires an isolated gate control signal, the propagation delay skew of the two HB gate control signal paths for the high- and low-side transistor, i.e., the propagation delay difference (and its variation, e.g., due to temperature), which is mostly caused by the digital signal isolators, imposes a practical lower limit to dead

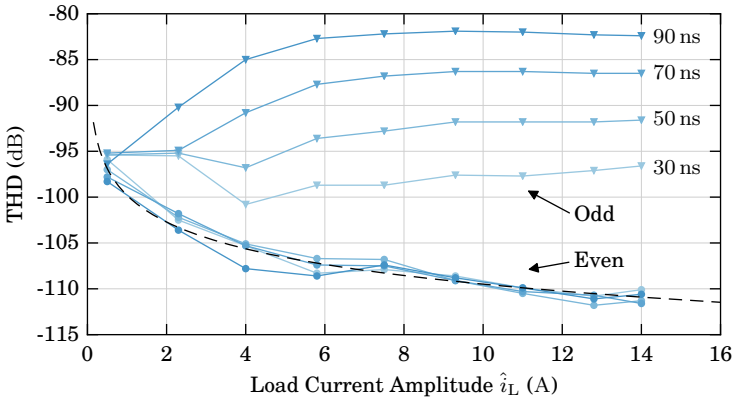

Fig. 7.19: Measured THD for different dead times of the regular interleaved power stage topology as indicated. Load: 10 Ω+100 µH. Odd harmonics: 3, 5, 7, 9. Even harmonics: 2, 4, 6, 8. The THD of the even harmonics follows a logarithmic fit (of the dB values, dashed curve). $f_F = 35\,\text{Hz}$, $u_{DC} = 400\,\text{V}$, $f_{PWM} = 200\,\text{kHz}$.

time, as it must be guaranteed that a minimum interlock interval is always ensured to prevent HB shoot-through. With current digital signal isolators and gate drivers, the practical lower dead time limit is ≈30 ns to 60 ns [153]. Another option to further reduce dead time are special gate drivers that couple the two gate voltages and make sure that always only one transistor is conducting, while minimizing dead time at the same time [241]. However, this approach increases circuit complexity and affects the gate loop parasitic inductance, which, due to the fast switch-node transitions of the HBs and the low GaN HEMT gate threshold voltages, can lead to parasitic transistor turn-on switching actions [128]. Other approaches supervise the conduction state of a transistor and communicate it to the complementary gate driver that can then control the switching state accordingly [242, 243]. Nonetheless, this method also requires more circuit elements and a high-speed, low-skew communication channel to the isolated gate driver, which also has to be robust against fast CM transients.

In the following, the performance of the DB topology, which inherently eliminates distortion related to dead time, is presented experimentally.

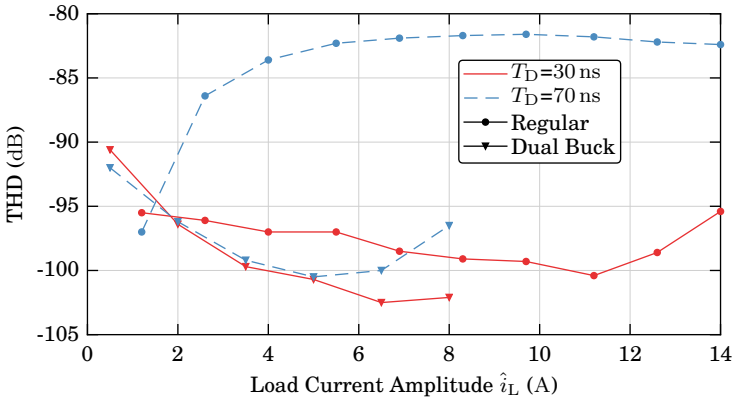

Fig. 7.20: THD improvement using the DB topology to reduce dead time related distortion, compared to the regular interleaved power stage. Load: 10 Ω+100 µH. u_{DC} = 400 V, f_{PWM} = 100 kHz, f_F = 35 Hz. I_B = 5.5 A for the DB topology.

Distortion of the Dual Buck Topology

As the demonstrator system supports the DB topology which is designed to eliminate distortion related to HB dead time (see Sec. 3.1 for details), its effect on the load current THD can be investigated experimentally. **Fig. 7.20** illustrates the results. By introducing the bias current (I_B = 5.5 A), the THD can be significantly lowered, especially when operating with considerable dead times. The linearizing effect of the DB topology is less pronounced with shorter dead times, as it reduces the magnitude of distortion components related to dead time in the first place. Note that the indicated HB dead times are identical for both power stage topologies, as an interlock time interval is also required for the synchronously rectified DB topology that is employed here (see Sec. 3.1).

The bias current is selected according to the results from the thermal amplifier model in Sec. 7.1.2, which is used to determine the achievable load current that is limited by the peak transistor junction temperatures. In any case, I_B must be larger than $\hat{i}_L/2$ to ensure unidirectional HB currents.

As the allowable load current amplitude of the DB topology is severely limited, Sec. 9.1 presents a duty cycle compensation method that achieves a similar distortion performance than the DB, without suffering from increased losses and reduced output current capabilities.

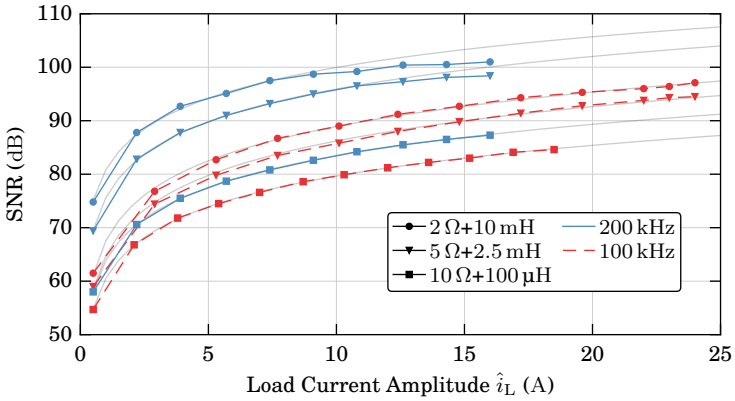

Fig. 7.21: SNR measured for different loads at different f_{PWM}, which correlates with the achievable disturbance rejection performance of the closed-loop controllers. Regular interleaved HB topology. At high currents and high SNR figures, noise from the DC supply affects the SNR unfavorably. Gray lines are least-squares fits: $\mathrm{SNR(dB)} = c_0 \ln(\hat{i}_L) + c_1$. $u_{DC} = 400\,\mathrm{V}$, $f_F = 35\,\mathrm{Hz}$. DC supply: *Sorensen SGI 600-17*.

7.6.2 Noise Performance

The amplifier load current SNR of the three considered loads is illustrated in **Fig. 7.21**, both for a PWM pulse repetition frequency (and the correspondingly tuned closed-loop control systems) of 100 kHz and 200 kHz, and with the regular interleaved power stage. The Kalman filter algorithm is not used for these measurements, but its effect is demonstrated in Ch. 8. Naturally, load configurations with a higher inductance value show less current noise due to the fact that the power amplifier operates as a voltage source, whose output noise components translate to noise currents in accordance with the presented load impedance. As expected, the control topology with the higher open-loop gains rejects noise disturbances better and hence, SNR is improved by up to 10 dB with $f_{PWM} = 200\,\mathrm{kHz}$. However, similar as with the THD measurements presented above, the SNR performance with high-inductance loads is more sensitive to the gain of the controllers. This is due to the fact that the 10 mH and 2.5 mH iron core inductors are significantly larger and contain more winding turns than the 100 µH ferrite core inductor. Thus, they are more susceptible to EMI and pick up more noise from the environment. Such noise components act as dominating disturbances and hence, high controller gains

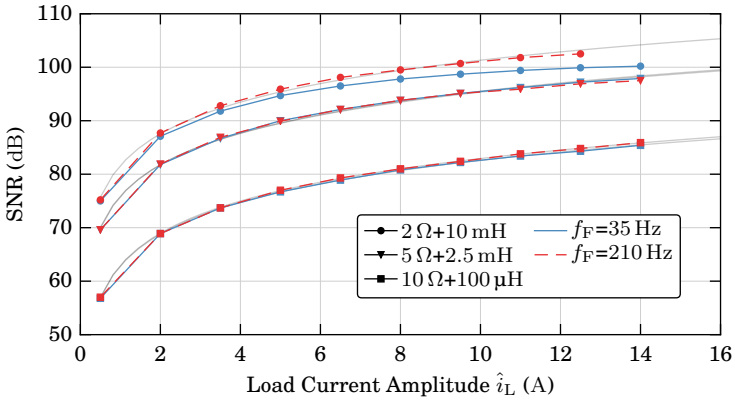

Fig. 7.22: SNR measured for different loads and fundamental frequencies f_F. Regular cascaded control system. $u_{DC} = 400\,V$, $f_{PWM} = 200\,kHz$. Supply: *HP 6035A*.

result in a more effective attenuation, which improves SNR. The 100 µH load is not introducing significant noise and hence, higher performing controllers do not increase SNR as much as with the other two load configurations, as other sources of noise, such as PWM quantization or sensor noise, are of similar power levels.

The gray lines in **Fig. 7.21** are logarithmic least-squares fits of the SNR values of each corresponding amplifier configuration (the formula is given in the figure caption). As given by (2.6), the SNR exhibits a logarithmic behavior as a function of the load current, if the noise power remains constant. This is behavior of the SNR is experienced with the measurements in **Fig. 7.21**, which hence implies that the load current noise is not affected by the magnitude of i_L. This is expected, as key noise sources, e.g., the PWM or gate drive signal isolation, operate independently of the output current amplitude.

Consequently, the achievable SNR is limited by the load current capability of the power amplifier, as the noise power remains, ideally, constant. However, at increased load currents, the SNR measurements deviate from their fitted values (cf. the 2 Ω+10 mH load curves in **Fig. 7.21**). This is attributed to the fact that noise originating from the DC laboratory power supply increases at high output powers. The deteriorating effects of increasing DC supply noise is also visible in the current amplitude sweeps shown in **Fig. 7.22**, which shows similar measurements, but performed at two different fundamental load current frequencies f_F. The degrading effect on the SNR is, again, only visible

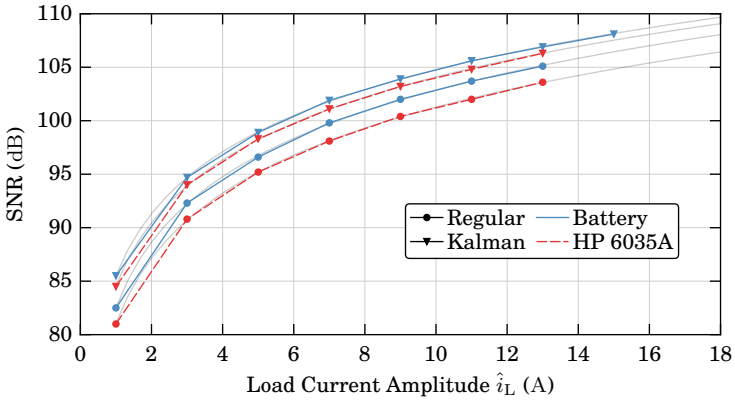

Fig. 7.23: Load current SNR improves with a battery supply compared to a switch-mode, high-power laboratory supply (*HP 6035A*). Regular cascaded control system executed with 200 kHz, Kalman controller executed with 100 kHz (see Ch. 8). f_{PWM} = 200 kHz, u_{DC} = 75 V, f_F = 35 Hz, Load: 2 Ω + 10 mH.

with the 2 Ω+10 mH load and for f_F = 35 Hz, whereas the measurements performed with f_F = 210 Hz follows its expectation well (i.e., do not derive from its logarithmic fit line). This distinction of load current SNR between the different fundamental frequencies is owed to the fact that the amplifier's DC-link buffer capacitors (C_B=1.8 mF in the demonstrator system) present less impedance for the single-phase load ripple current at higher f_F and consequently, it is shunted from the DC-link supply, whose output current is thus experiencing less variation. This improves its voltage regulation and hence, noise is reduced. The DC-link voltage could be measured and used in conjunction with a feedforward compensation method to mitigate the impacts of the DC-link voltage variations. However, as shown in Sec. 9.2, this approach can potentially introduce further noise and thus, deteriorate the SNR.

Generally, however, the SNR is independent of f_F, which is expected as the disturbance rejection of the feedback controllers is not affected by the frequency of their reference signals. This is not the case for harmonic distortion as shown in **Fig. 7.18** above, as the control system provides less open-loop gain at higher frequencies to attenuate the harmonics at integer multiples of f_F.

In order to further illustrate the influence of the DC supply on the load current noise, **Fig. 7.23** shows measurements where the switch-mode laboratory supply is exchanged with a battery comprising six individual series-connected 12 V lead-acid cells, that typically features a negligible output voltage noise. For this measurement, the DC-link voltage is set to 75 V for both supply types. By eliminating the noise of the switch-mode laboratory supply, SNR improves slightly (≈1 dB) and does not deteriorate at high load currents. Furthermore, the SNR reaches values up to 108 dB, which corresponds to an equivalent current noise of 42 µA RMS in the 10 kHz baseband. In this figure, the performance with an enabled Kalman filter is also demonstrated. Details are given in Ch. 8.

The presented SNR figures in this section are slightly deteriorated from what the open-loop system in Sec. 4.3 achieved (≈107 dB), where the low-jitter gate drivers are investigated. This is due to the fact that sensor noise does not affect open-loop systems. Furthermore, the SNR measurements in Sec. 4.3 are obtained with a reduced DC-link voltage of 160 V (due to limitations of the measurement equipment), and with correspondingly reduced output powers, which improves the noise of the DC supply. However, due to the open-loop operation, the harmonic distortion is significantly worse than what is demonstrated above in this section (cf. **Fig. 4.19**).

The observed sensitivity to supply noise emphasizes the requirement for a low-noise DC voltage source, especially during amplifier operation with single-phase loads that are characterized by a large power ripple. This demands a good output voltage tracking performance of the DC supply. If a switch-mode power converter is used, a good rejection of voltage components related to the corresponding switching frequency is also required, even if these frequencies are outside the noise-sensitive baseband, as intermodulation distortion, e.g., caused by the EMI input filter of the amplifier or the feedback control of the DC supply, can shift harmonics of the switching frequency into sensitive frequency bands, where they appear as undesired noise.

Noise Shaper Performance

To reduce the PWM quantization noise, digital noise shapers, as presented in Ch. 5, are utilized at the input of the four modulators. **Fig. 7.24** illustrates this (disengageable) system as used in the hardware demonstrator. During open-loop operation of the power converter, when no closed-loop feedback system is active, this noise shaper significantly increases the output signal SNR by more than 30 dB as shown in Sec. 5.2.3.

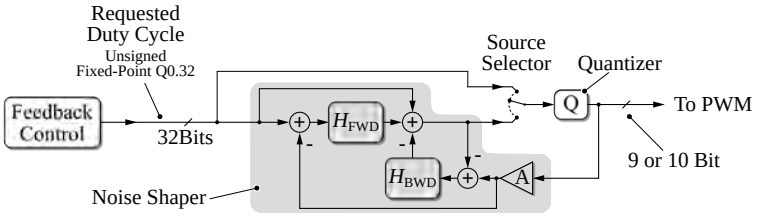

Fig. 7.24: Noise shaping in the demonstrator system reduces the PWM quantization noise from DC to 10 kHz. Each noise shaper consists mainly of two FIR filters $H_{FWD/BWD}$ and can be bypassed to investigate its effect.

Fig. 7.25 illustrates the influence of the noise shapers on the amplifier load current SNR during closed-loop operation. With bypassed noise shapers, the regular quantizers create significant noise due to rounding errors and thus, the load current SNR degrades by up to 5 dB. This effect is less pronounced if the higher-gain control system (f_{PWM} = 200 kHz) is utilized, as it is capable of rejecting more quantization noise than the controllers that are executed with 100 kHz. Again, at high load powers, the increasing noise of the DC supply becomes evident, as described previously.

In the same measurement, the THD of the load current is also acquired and, from **Fig. 7.25**, it is evident that the noise shaping modulator does not affect amplifier linearity, which is expected due to its unity signal transfer function (the noise shaper only affects the rounding error of the digital quantizer, see Sec. 5.2 for details).

It can be concluded that a noise shaping modulator is a valuable addition to any low-noise PWM conversion system, as it is capable of eliminating a significant noise source. This is especially relevant for power converters without a feedback control system as shown with measurements in Sec. 5.2.3. Nonetheless, the noise shaper benefits are still evident in high-performance closed-loop systems. The digital implementation of the utilized noise shaper only requires two comparably small FIR filters (whose orders are usually smaller than 15) that require little additional logic and can be conveniently implemented with an FPGA. Furthermore, the Kalman filter relies on the noise shaping modulators, as the PWM quantization noise otherwise dominates sensor noise and renders the Kalman filter ineffective, as further described in Ch. 8.

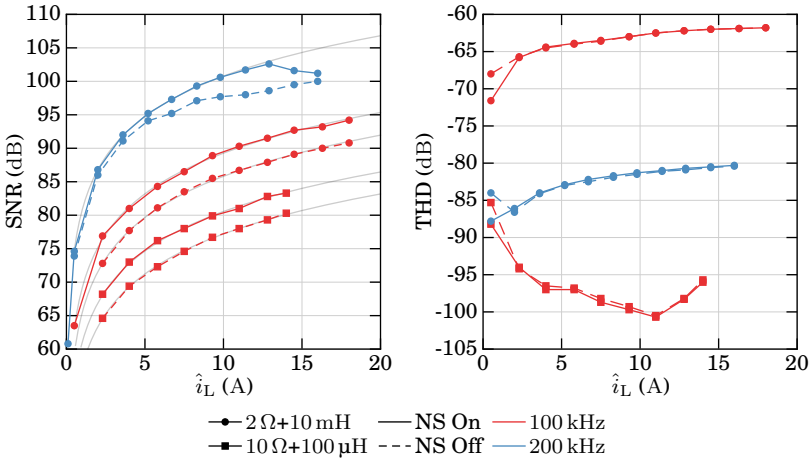

Fig. 7.25: Measured effects of the noise shapers on load current SNR with closed-loop converter operation. Regular interleaved power stage, f_{PWM} = 100 kHz and 200 kHz. At high load currents, the DC supply increasingly injects noise. THD is not affected by the noise shapers. u_{DC} = 400 V, f_F = 35 Hz.

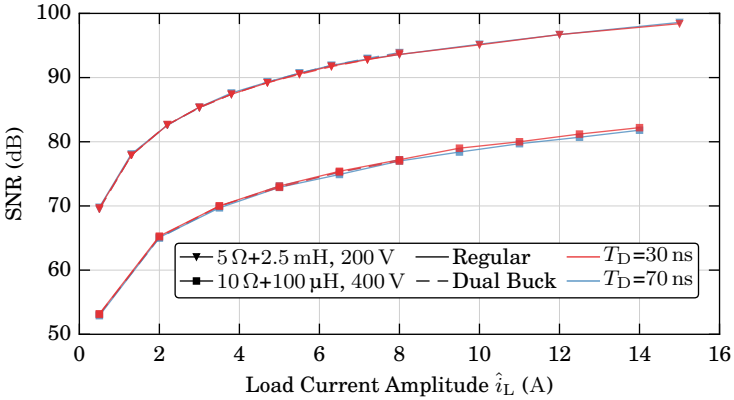

Fig. 7.26: The measured SNR is independent of HB dead time T_D and power stage topology. 200 V measurements taken with f_{PWM} = 200 kHz, 400 V measurements with f_{PWM} = 100 kHz. f_F = 35 Hz. I_B = 5.5 A.

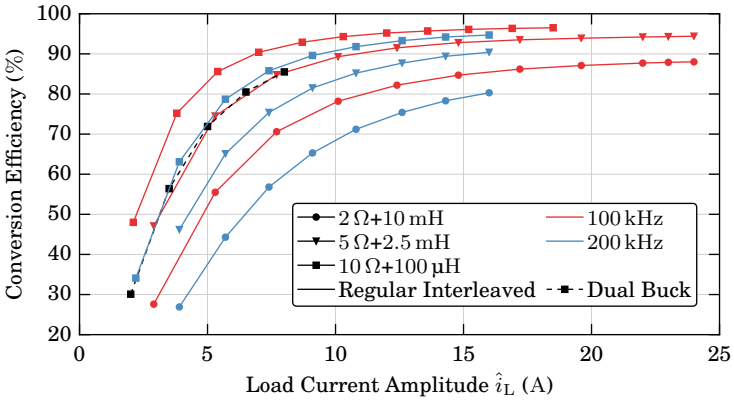

Fig. 7.27: Measured power conversion efficiencies for different loads and amplifier configurations. Power for control system and cooling fans (≈15 W) is excluded. The DB stage is operated with $f_{PWM} = 100\,\text{kHz}$. $u_{DC} = 400\,\text{V}$, $f_F = 35\,\text{Hz}$. More details in **Tab. 7.4**.

Noise of the Dual Buck Topology

The DB power stage differs from the regular interleaved HB topology in how the individual HB currents are controlled, as detailed in Sec. 3.1. Its effect on distortion is presented in Sec. 7.6.1 above. Similarly, **Fig. 7.26** shows SNR measurements for both converter operating modes and two different HB dead times. It reveals that the SNR is neither affected by the power stage topology nor the employed dead time. This is expected as the dead time is constant and introduces no source of noise. Furthermore, the DB behavior of the power converter is achieved by altering the current references of the four HB current controllers in the feedback control system, such that the desired circulating bias current I_B is introduced. Likewise, this does not provide an additional source of noise. Thus, the only significant disadvantage of the DB topology is given by its increased transistor losses and hence, a reduced amplifier output current capability.

The measurement also illustrate SNR figures of the amplifier operating with a DC-link voltage of 200 V, which do not differ from values obtained at 400 V.

Tab. 7.4: Measured power conversion efficiencies of the demonstrator system for different loads and amplifier configurations. More details in **Fig. 7.27**.

u_{DC}	f_{PWM}	$R_L + L_L$	$\hat{i}_L$	P_L	η
Regular Interleaved Topology:					
400 V	100 kHz	10 Ω+100 µH	18.5 A[1]	1.7 kW	96.5 %
		5 Ω+2.5 mH	24.0 A	1.4 kW	94.4 %
		2 Ω+10 mH	24.0 A	576 W	88.0 %
400 V	200 kHz	10 Ω+100 µH	16 A	1.3 kW	94.7 %
		5 Ω+2.5 mH	16 A	640 W	90.4 %
		2 Ω+10 mH	16 A	256 W	80.3 %
DB Topology (I_B = 5.5 A):					
400 V	100 kHz	10 Ω+100 µH	8 A	320 W	85.4 %

[1] Limited by load resistor dissipation capability

7.6.3 Power Conversion Efficiency

The achieved overall power conversion efficiencies of the demonstrator system are illustrated in **Fig. 7.27**, whereas the peak values and further details are given in **Tab. 7.4**. The data is obtained using a power analyzer to measure the active power at the converter's DC input and at the load (P_L). Note that the auxiliary power of the control logic and the cooling fans is not included. Depending on the fan speed, the converter requires ≈10 W to 30 W of auxiliary power. The achieved conversion efficiencies demonstrate the advantage of switch-mode power converters as compared to hybrid or linear solutions. Furthermore, the output powers also exceed typical values of precision amplifiers (cf. Sec. 1.2). The loss model, presented in Sec. 7.1.1, reveals that with an ohmic load of 14 Ω, a DC supply voltage of 400 V and a PWM frequency of 100 kHz, a load power of 4 kW is feasible without destructive peak transistor junction temperatures (sinusoidal load current with $\hat{i}_L$ = 24 A). However, this is not verified with the demonstrator due to the limited power dissipation capability of the utilized load resistors.

7.7 Summary and Discussion

The power amplifier system is introduced in detail and its THD and SNR performance is demonstrated with measurements. Its flexible power stage arrangement allows the implementation of the regular interleaved HB and the DB topology, which enables experimental comparisons. Top-cooled GaN power transistors are employed, which reduce parasitic circuit elements and facilitate high switching speeds. The gate driving and isolation circuits, which are key power stage elements, are also outlined. The amplifier is designed for a DC-link voltage of 400 V and a peak load current of 25 A (peak), while switching frequencies reach 200 kHz.

A comprehensive loss model of the power transistors is developed, which covers switching and conduction losses. The dynamics of the thermal systems are also considered to correctly recreate the modulation of the power transistor on-state resistances. This is used to determine the achievable amplifier load currents, which are limited by the transistor's peak junction temperatures. The analysis shows that the DB topology, due to its bias current, can only provide a third of the load current as compared to the regular interleaved topology. Furthermore, it is shown how for a given load current capability of the amplifier, power transistors can be optimally paralleled to minimize losses.

Regular PWM, combined with digital noise shapers that are used to mitigate quantization noise, is employed. The high-performance digital processing system is capable of executing the feedback control algorithms at least once per PWM period, up to control system execution frequencies of 400 kHz. An FPGA and modern a CPU, combined in a single integrated circuit, are used to process the high-resolution ADC data and the feedback control algorithms at such rates. Furthermore, they enable complex control schemes such as real-time Kalman filters.

The closed-loop cascaded feedback controllers, as well as the corresponding dynamic systems, are modeled with time-continuous representations and consider important delays, namely the PWM delay and the time required for the execution of the control algorithms, in order to accurately determine stability margins. All feedback controllers are tuned using loop shaping to maximize the controller gains and bandwidths. Using the closed-loop controllers in a detailed circuit simulation of the power converter, which includes the transistor losses and thermal models, it is shown that distortion arising from the variation of the transistor on-state conduction resistances

is negligible for the load current range that is achievable with the hardware demonstrator.

Experiments are performed to demonstrate the load current THD and SNR, and to identify amplifier system parameters to which these key performance figures react with high sensitivities. Harmonic distortion acts as disturbance for the closed-loop controllers and hence, it is shown how higher control system execution rates, enabled by the correspondingly increased converter switching frequencies, improve the achievable THD. The load current harmonic distortion depends on the linearity of the utilized load inductors and resistors, but is generally independent of the load current amplitude. Values as low as −99.5 dB (0.001 06 %) are achieved despite using the regular interleaved HB topology that relies on distortion-inducing dead time (the amplifier is operated with $T_D = 30$ ns). The high sensitivity to the HB interlock time is further demonstrated with measurements that corroborate the need for fast HB switching speeds that enable short dead times. Practical lower dead time limits are given by propagation delay tolerances between different gate signal isolator devices or gate drivers. Consequently, the DB topology is also investigated, and its load current THD reaches −102.5 dB (0.000 75 %), whereas the maximum load current is limited to 8 A (instead of 25 A with the regular interleaved topology).

The amplifier output current THD is mainly limited by the linearity of the utilized load inductors and resistors, the remaining HB dead time, the (temperature-dependent) power transistor on-state resistances, the restricted open-loop gain of the feedback controllers and the varying DC-link supply voltage (caused by the single-phase load power ripple). In Sec. 9.2, a method is presented which can improve the amplifier's power supply rejection. Furthermore, the outlook in Sec. 10.2 presents potential approaches to further increase the amplifier's linearity. The best obtainable THD is ≈−110 dB, which is determined by the measurement limit of the employed highly linear load current sensor.

The amplifier's achievable load current SNR is investigated similarly. As with distortion, high-gain controllers are capable of rejecting undesired noise and thus, the SNR also improves with the converter's PWM frequency and the correspondingly tuned controllers. The effectiveness of increased controller gains are more prominent with load inductors that are susceptible to external EMI sources and hence, are picking noise up from the environment. The load current noise power remains constant over wide operating ranges. Only at high currents, noise originating from the DC supply increases, which can limit the achievable SNR. Nonetheless, values as high as 102 dB are recorded.

By using a low-noise battery supply, which eliminates this source of noise, SNR figures up to 105 dB are demonstrated with the regular cascaded control system. By enabling the Kalman filter (see Sec. 8 for details), an SNR of 108.1 dB is achieved.

Remaining noise sources include the pulse-width modulators and the noise shapers, sensor noise, external noise introduced through EMI with the load inductor and resistor, as well as the mentioned DC supply noise, which dominates at high amplifier output powers. If the tested DC supplies were ideal, i.e., maintained their output noise also at high powers, the SNR could be increased with a higher load current of the amplifier. For example, by regarding the noise level of the 10 mH load illustrated in **Fig. 7.22** (at a fundamental load current frequency of 210 Hz), the SNR would increase to 111 dB with a load current amplitude $\hat{i}_\mathrm{L}$ of 30 A. As shown in Sec. 7.1.3, the obtainable amplifier load current can be raised by paralleling transistors or interleaving more HBs.

With the closed-loop feedback system enabled, the noise shaping modulators are still able to improve the load current SNR by ≈5 dB. Due to their simple digital design, they are thus a valuable addition for such amplifiers. The measurements also demonstrate that the THD is not affected by the noise shapers. Similarly, the DB topology achieves the same SNR figures as the regular interleaved topology, which also holds for varying DC-link voltages of both topologies.

Power conversion efficiencies, which strongly depend on the utilized load resistance, are recorded up to values of 96.5 %, with a DC-link voltage of 400 V and a PWM frequency of 100 kHz. At 200 kHz, an efficiency of 94.7 % is demonstrated. These figures are enabled by the fast switching actions and low on-state resistances of the GaN power transistors.

8

Real-Time Kalman Filter

A closed-loop feedback control system is an essential contribution for high-performance output waveforms of any amplifier system, as it is capable of significantly rejecting disturbances such as noise or harmonic distortion, and also improves the reference tracking performance. **Fig. 8.1** illustrates the simplified block diagram of the closed-loop cascaded feedback control system as employed in the hardware demonstrator, whose details are given in Ch. 7 (redundant elements like the second phase and the interleaved half-bridge (HB) are omitted for simplicity, see **Fig. 7.9** for a complete illustration). Dominant sources of noise are illustrated, whereas the sensor noise coupling is only shown for the load current measurement i_{L}, despite all measurements containing sensor noise that is generally caused by the sensors themselves, analog filters or amplifiers, or the subsequent ADC acquisition stage. Design considerations for low-noise sensors are presented in Ch. 6.

Sources of noise that act on the plants of the dynamic system (e.g., the supply noise) appear as disturbances to the control system and are thus effectively attenuated with the open-loop gains of the feedback loops, which are defined by the transfer functions of the controllers and their corresponding plants, as shown in Sec. 7.2. This disturbance rejection is an important feature of closed-loop feedback control systems. On the other hand, a fundamental impediment is their high sensor noise sensitivity, as this noise source is basically amplified by the high gains of the controllers. Thus, the control system reacts equally sensitive to sensor noise than to its reference input [100, 244], which corroborates the necessity for advanced control techniques such as a Kalman filter. It describes an estimation method that is capable of effectively reducing sensor noise. As measurements will show, the Kalman filter can further improve the achievable load current SNR, despite the low-noise sensors of the hardware demonstrator.

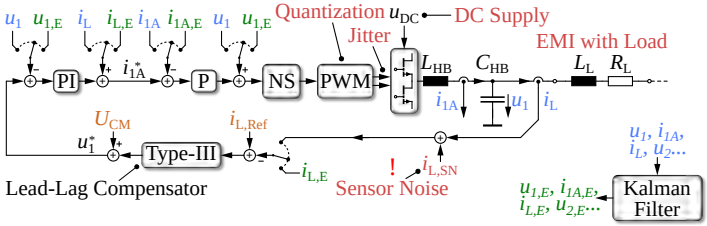

Fig. 8.1: Simplified diagram of the cascaded control system of the hardware demonstrator (second phase and second HB of the shown bridge leg omitted). Important sources of noise are outlined (sensor noise only shown for i_L, despite every sensor being subjected to noise). Sensor noise, as opposed to the other sources, cannot be rejected by closed-loop feedback control. The feedback controllers can either directly use the sensor measurements or the Kalman estimates.

Sec. 8.1 presents the Kalman filter design and tuning methods in the context of the discussed power amplifier system. **Sec. 8.2** then discusses the implementation of the algorithm in the digital signal processing system, which is characterized by short processing times. **Sec. 8.3** demonstrates the reduction of load current noise with measurements on the demonstrator system. Due to the linear system model of the Kalman filter, the linearity of the amplifier can be affected, as shown in **Sec. 8.3.1**. Finally, **Sec. 8.4** summarizes the results.

8.1 Kalman Filter Design

Generally, the Kalman filter presents an approach to provide estimates of unknown or noisy states of a dynamic system (e.g., voltage, current, position, speed etc.), given some knowledge about the dynamic system itself, and usually (noisy) measurements of some (or all) states [101]. Kalman filters, which can manifest in different implementations that are often tailored for specific applications (e.g., with linear or nonlinear dynamic system models), are commonly used in guidance or navigation. Such applications do not require high execution rates of the required calculations due to their limited dynamics. However, as shown in Sec. 7.2.3 for the control system modeling and in Sec. 7.6 with measurements, the execution rate of the feedback controllers in the considered precision power amplifier is critical for achieving output waveforms of low noise and distortion. In the intended application, the Kalman filter is used to attenuate sensor noise and hence, it must be computed with the same

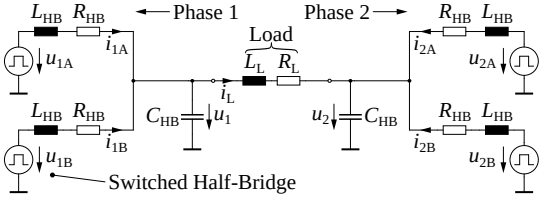

Fig. 8.2: Linear dynamic system model of the demonstrator system power stage used for the Kalman filter. Switching ripple components are disregarded as all sensors (except the load current sensor) sample synchronously with the switching actions and thus, the switch-mode HBs are modeled as controlled voltage sources [184]. $L_{HB} = 700\,\mu H$, $R_{HB} = 70\,m\Omega$, $C_{HB} = 12\,\mu F$.

rate as the feedback control system (i.e., in *real-time*), in order to provide the updated low-noise estimates of the measurements for each control cycle.

Due to their computational complexity, real-time Kalman filters in power electronic applications usually do not exceed execution rates in excess of 5 kHz to 30 kHz, which is insufficient for precision amplifiers due to the accompanying reduction of achievable control gain [245–249]. By implementing the Kalman algorithm using configurable logic (i.e., with an FPGA), the execution rates can be increased to more than 150 kHz [250, 251]. However, this comes at the cost of a significantly increased implementation complexity and a loss of design flexibility. Consequently, this chapter presents a real-time Kalman filter implementation, executed as a procedural program that is calculated by a conventional processor. It is part of the demonstrator's feedback control system and it can provide low-noise estimates of the sensor data at a rate of 100 kHz, while featuring seven system states and four inputs in its underlying dynamic model, as presented in the following.

8.1.1 Dynamic System Model

The Kalman algorithm requires a dynamic model of the physical system that also describes the relevant sources of noise. In order to reduce the computational complexity, a linear model of the power amplifier system, illustrated in **Fig. 8.2**, is utilized. The switched HBs are modeled as controlled voltage sources to obtain a linear system. Its description, including the state vector $\boldsymbol{x}$, the input vector $\boldsymbol{u}$, and a vector $\boldsymbol{w}$ that models noise, can be given by

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} + \boldsymbol{G}\boldsymbol{w}, \tag{8.1}$$

with the system matrices as follows:

$$\boldsymbol{A} = \begin{bmatrix} -R_{\mathrm{HB}}/L_{\mathrm{HB}} & 0 & 0 & 0 & 0 & -1/L_{\mathrm{HB}} & 0 \\ 0 & -R_{\mathrm{HB}}/L_{\mathrm{HB}} & 0 & 0 & 0 & -1/L_{\mathrm{HB}} & 0 \\ 0 & 0 & -R_{\mathrm{HB}}/L_{\mathrm{HB}} & 0 & 0 & 0 & -1/L_{\mathrm{HB}} \\ 0 & 0 & 0 & -R_{\mathrm{HB}}/L_{\mathrm{HB}} & 0 & 0 & -1/L_{\mathrm{HB}} \\ 0 & 0 & 0 & 0 & -R_{\mathrm{L}}/L_{\mathrm{L}} & 1/L_{\mathrm{L}} & -1/L_{\mathrm{L}} \\ 1/C_{\mathrm{HB}} & 1/C_{\mathrm{HB}} & 0 & 0 & -1/C_{\mathrm{HB}} & 0 & 0 \\ 0 & 0 & 1/C_{\mathrm{HB}} & 1/C_{\mathrm{HB}} & 1/C_{\mathrm{HB}} & 0 & 0 \end{bmatrix}, \tag{8.2}$$

$$\boldsymbol{B} = \begin{bmatrix} 1/L_{\mathrm{HB}} & 0 & 0 & 0 \\ 0 & 1/L_{\mathrm{HB}} & 0 & 0 \\ 0 & 0 & 1/L_{\mathrm{HB}} & 0 \\ 0 & 0 & 0 & 1/L_{\mathrm{HB}} \\ \multicolumn{4}{c}{\boldsymbol{O}_{3\times 4}} \end{bmatrix}, \tag{8.3}$$

$$\boldsymbol{x} = \begin{bmatrix} i_{1\mathrm{A}} & i_{1\mathrm{B}} & i_{2\mathrm{A}} & i_{2\mathrm{B}} & i_{\mathrm{L}} & u_1 & u_2 \end{bmatrix}^\top, \tag{8.4}$$

$$\boldsymbol{u} = \begin{bmatrix} u_{1\mathrm{A}} & u_{1\mathrm{B}} & u_{2\mathrm{A}} & u_{2\mathrm{B}} \end{bmatrix}^\top, \tag{8.5}$$

with $\boldsymbol{O}$ being the zero matrix where its indices define the number of its rows and columns. The state vector $\boldsymbol{x}$ includes all capacitor voltages and inductor currents, and the input vector $\boldsymbol{u}$ contains the four HB voltages. In the demonstrator system, all seven states are measured by sensors and consequently, the measurement equation, including the measurement noise term $\boldsymbol{v}$, is given by

$$\boldsymbol{y}_m = \boldsymbol{I}\boldsymbol{x} + \boldsymbol{v}, \tag{8.6}$$

with $\boldsymbol{I}$ being the identity matrix.

Noise is described by the process noise $\boldsymbol{w}$, which accounts for sources of noise within the dynamic system, and measurement noise $\boldsymbol{v}$, generated by the sensors. The noise is assumed to have a Gaussian probability distribution and a white (i.e., uniform) power spectral density. The corresponding noise covariance matrices $\boldsymbol{Q}$ and $\boldsymbol{R}$ are given as $\boldsymbol{Q} = E(\boldsymbol{w}\boldsymbol{w}^\top)$ and $\boldsymbol{R} = E(\boldsymbol{v}\boldsymbol{v}^\top)$, where E is the expected value. In this work, the process noise model is based on the assumption that the four HB voltages are the only sources of noise within the dynamic system (apart from the measurement noise). This is given in the demonstrator hardware, in which the quantization noise of the low-resolution pulse-width modulators, or the HB switching jitter, are injecting such process noise into the plant. Other sources of noise within the system, such as EMI with the load, are neglected due to their comparably small noise powers and often parasitic natures. Consequently, $\boldsymbol{G}$ is modeled such that the

process noise only affects the four HB currents:

$$\boldsymbol{G} = \left[\begin{array}{c|c} \boldsymbol{I}_{4\times4} & \boldsymbol{O}_{4\times3} \\ \hline \boldsymbol{O}_{3\times4} & \boldsymbol{O}_{3\times3} \end{array}\right]. \tag{8.7}$$

The process noise (co)variances are modeled as

$$\boldsymbol{Q} = \left[\begin{array}{cccc|c} \sigma^2_{\mathrm{HB}} & 0 & 0 & 0 & \\ 0 & \sigma^2_{\mathrm{HB}} & 0 & 0 & \boldsymbol{O}_{4\times3} \\ 0 & 0 & \sigma^2_{\mathrm{HB}} & 0 & \\ 0 & 0 & 0 & \sigma^2_{\mathrm{HB}} & \\ \hline \multicolumn{4}{c|}{\boldsymbol{O}_{3\times4}} & \boldsymbol{O}_{3\times3} \end{array}\right], \tag{8.8}$$

with σ^2_{HB} being the noise variance of the HB voltages. The diagonal nature of this matrix reflects the fact that these four noise sources are independent. Similarly, the measurement noise covariance matrix is

$$\boldsymbol{R} = \mathrm{diag}\left(\begin{bmatrix} \sigma^2_{i_{\mathrm{HB}}} & \sigma^2_{i_{\mathrm{HB}}} & \sigma^2_{i_{\mathrm{HB}}} & \sigma^2_{i_{\mathrm{HB}}} & \sigma^2_{i_{\mathrm{L}}} & \sigma^2_{u_{\mathrm{HB}}} & \sigma^2_{u_{\mathrm{HB}}} \end{bmatrix}\right), \tag{8.9}$$

which incorporates the noise variances of the three different types of voltage/current sensors of the demonstrator system (HB currents, load current and phase voltages). Again, the diagonal matrix reflects the independence of the sensor noise sources, as each sensor is a self-contained unit which cannot influence the noise of other sensors. The corresponding sensor noise standard deviations, measured during converter operation with no applied voltages or currents, are given as $\sigma_{i_{\mathrm{HB}}} = 2.0\,\mathrm{mA}$, $\sigma_{i_{\mathrm{L}}} = 83.0\,\mu\mathrm{A}$ and $\sigma_{u_{\mathrm{HB}}} = 25.0\,\mathrm{mV}$. For each measurement, 5×10^6 samples are obtained. As shown in Ch. 6, the sensor noise levels remain constant in their operating ranges. The low value for $\sigma_{i_{\mathrm{L}}}$ reflects the effort to create a low-noise measurement for the load current i_{L} (i.e., oversampled, high-resolution ADC with optimized analog processing circuitry, see Sec. 6.4).

8.1.2 Steady-State Kalman Filter

Using the presented system and noise covariance matrices (i.e., $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{G}$, $\boldsymbol{Q}$ and $\boldsymbol{R}$), the Kalman filter can be designed. In order to reduce the required computations during converter operation and thus, to maximize the Kalman filter execution rate, a steady-state implementation of the Kalman estimation method is chosen. It is based on the assumption of constant noise covariance matrices ($\boldsymbol{Q}$, $\boldsymbol{R}$) and hence, does not require the time-consuming calculation of inverse matrices or matrix factorizations [101]. This assumption holds

in the considered power converter, as sensor noise and the system's input noise sources (e.g., PWM or HB switching jitter) maintain a constant and independent noise behavior during operation.

In the presented application, the Kalman filter is implemented in a sampled system and consequently, the discrete-time process noise covariance matrix is determined using Van Loan's method [101], whereas the continuous-time system description can be converted to a sampled model using common discretization methods such as zero-order hold or Tustin's method. The design process is well documented and common engineering tools can be used to effortlessly determine the optimal solution of the Kalman estimation problem [101, 252].

For the case of the considered steady-state Kalman filter, the algorithm, which provides the required low-noise measurement estimates, reduces to the calculation of a dynamic system of the following form, where the filtered measurements at each execution step n are given by $\boldsymbol{y}_e$, and $\boldsymbol{x}_n$ is an internal state that is continuously updated:

$$\boldsymbol{x}_n = \boldsymbol{A}_k \boldsymbol{x}_{n-1} + \boldsymbol{B}_k \begin{bmatrix} \boldsymbol{u}_{n-1} \\ \boldsymbol{y}_{m,n} \end{bmatrix}, \tag{8.10}$$

$$\boldsymbol{y}_e = \boldsymbol{C}_k \boldsymbol{x}_n + \boldsymbol{D}_k \begin{bmatrix} \boldsymbol{u}_{n-1} \\ \boldsymbol{y}_{m,n} \end{bmatrix}. \tag{8.11}$$

Note that the solution of the Kalman estimation problem is embedded in the matrices $\boldsymbol{A}_k, \boldsymbol{B}_k, \boldsymbol{C}_k$ and $\boldsymbol{D}_k$ [252]. The vector $\boldsymbol{y}_{m,n}$ contains the measurements at step n and $\boldsymbol{u}_{n-1}$ is the system input as applied in the previous step. The two equations contain only multiplications and additions, and no complex matrix operations such as finding an inverse. Thus, the computations can be performed in a comparably short time.

In the following, it is briefly explained how the remaining sensor noise in the estimates of the Kalman filter can be affected through a tuning parameter, before details of the implementation in the demonstrator system are given.

8.1.3 Kalman Filter Tuning

A key parameter of the Kalman filter is the *Kalman gain* [101]. Using the system model as described above, the Kalman filter algorithm calculates predictions for the true states of the dynamic system in each execution step. The Kalman gain is then used to weight these predictions relative to the measurements in order to form a weighted estimate of the system states, which in this case, is also the Kalman filter's output. Consequently, this presents a

tuning opportunity. The Kalman gain is determined during the design process as optimal solution of the Kalman estimation problem, and affected by the assumed process noise standard deviation σ_{HB} (see (8.8)) [101, 252]. By increasing this value, the filter increases the weight on the measurements compared to the predictions from its linear model, as there is a high uncertainty in the dynamic system (i.e., increased process noise). Consequently, the noise content of the estimates increases. On the other hand, by choosing smaller values for σ_{HB}, which leads to a Kalman gain that weights the measurements less, as the filter then trusts its predictions more, noise in the estimates can be reduced. In summary, the behavior of the Kalman filter can be tuned with the noise covariance matrices, which affect the resulting Kalman gain. As shown in Sec. 8.3.1 further below, the Kalman gain also affects the linearity of the amplifier due to the utilization of a linear system model in conjunction with a slightly nonlinear physical system. For the demonstrator system, values for σ_{HB} are experimentally determined in order to maximize the achievable SNR, while still obtaining stable Kalman filters. Values between 1 and 15 result, depending on the utilized load configuration.

8.2 Implementation

Due to the availability of a modern and fast CPU with floating-point units in the demonstrator system, the Kalman algorithm, as described by (8.10) and (8.11), is implemented as a procedural program based on floating-point arithmetic. Compared to a solution based on digital logic provided by an FPGA, which often requires manufacturer-specific logic designs such as wide multipliers, memories or floating-point cores, a procedural algorithm offers more design flexibility, as it is quickly changed, which is more demanding with digital hardware designs. This also reduces development time and cost, and the design can be quickly deployed on other systems, as no hardware-specific constructs are required. Furthermore, potential Kalman filter instabilities, related to the numerical precision of the calculations, are circumvented by the use of floating-point arithmetic [101, 252].

Fig. 8.3 illustrates the implementation of the Kalman algorithm and the signal paths inside the demonstrator's *Xilinx Zynq Z-7020* processing system. At the beginning of each PWM cycle (if $f_{\mathrm{PWM}} = 100\,\mathrm{kHz}$, or every second cycle if $f_{\mathrm{PWM}} = 200\,\mathrm{kHz}$), the sensors measure all seven system states and transmit the data to the FPGA fabric, where the raw ADC measurements are rescaled to 32 bit wide fixed-point data vectors that represent the physical quantity in µA or µV, which is sufficient to cover the dynamic ranges of

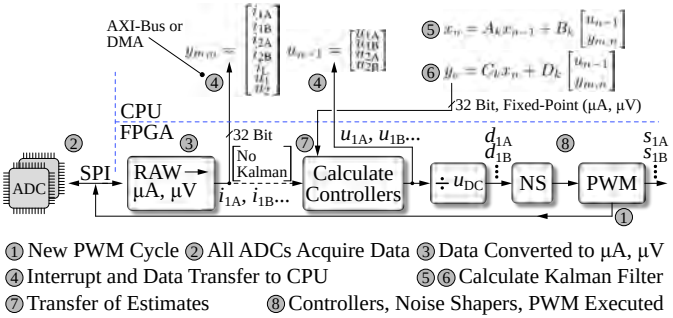

Fig. 8.3: Data paths for the calculation of the steady-state Kalman filter in the demonstrator system. The entire algorithm can be executed with 100 kHz (two PWM cycles if $f_{\mathrm{PWM}} = 200\,\mathrm{kHz}$). If the Kalman filter is not used, the measured data is sent directly to the feedback controllers.

the measurements, while also providing sufficiently low quantization noise. If the Kalman filter is enabled, an interrupt is raised in the CPU and the measurements, together with the previously requested HB voltages $\boldsymbol{u}_{n-1}$, are transferred from the FPGA fabric to the cache of one of the *ARM Cortex* CPUs. Due to the small data payload (44 bytes), this transfer requires approximately the same amount of time with register-based CPU bus transfers (*AXI4-Lite*) as with a cache-coherent direct memory access. Next, the transferred data is converted to a floating-point representation and the Kalman filter algorithm is computed, using the processor's floating-point unit, according to (8.10) and (8.11). The matrices $\boldsymbol{A}_k$, $\boldsymbol{B}_k$, $\boldsymbol{C}_k$ and $\boldsymbol{D}_k$ are stored as floating-point arrays in the processor memory. The updated estimates $\boldsymbol{y}_e$ of the system states are then transferred back to the FPGA fabric (again, as 32-bit fixed-point numbers), where the cascaded controllers are executed using the estimates instead of the measurements. Subsequently, the delta-sigma noise shapers (NS) and pulse-width modulators are updated with the new duty cycles as requested by the control system, and the process, whose execution requires ≈8 µs, is complete and repeated with the start of the next PWM cycle.

8.3 Performance Measurements

Fig. 8.4 shows two frequency spectra of the load current i_{L} at the amplifier output under closed-loop operation, to demonstrate the influence of the Kalman filter, as the only difference between the two measurements is the

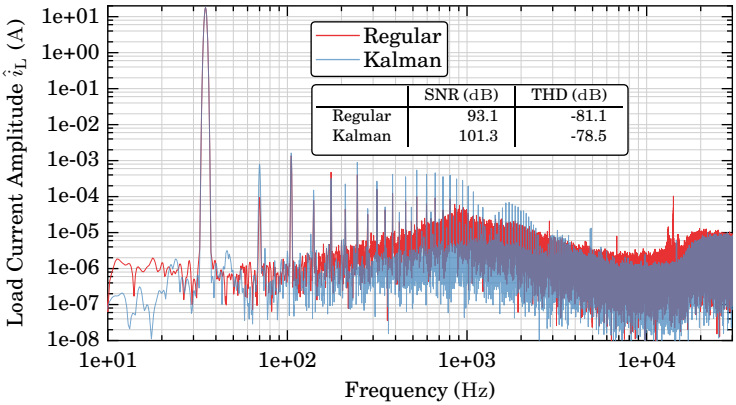

Fig. 8.4: Measured spectra of the load current obtained from the amplifier's load current sensor, with and without the use of Kalman estimates for the feedback control system. $f_{PWM} = 100\,\text{kHz}$, $u_{DC} = 400\,\text{V}$, $\hat{i}_L = 18\,\text{A}$, $f_F = 35\,\text{Hz}$, Load: $5\,\Omega + 2.5\,\text{mH}$. FFT window: Kaiser, 38^{th}-order. Nr. of samples: 20e6. Sampling rate: 5 MHz. Kalman filter and feedback control system executed with 100 kHz.

utilization of either the Kalman estimates or the unaltered measurements for the feedback control system. As illustrated, with the Kalman filter enabled, the load current SNR increases significantly, which is also evident from the lower noise floor in the spectrum (both spectra are recorded with the same number of samples and FFT window function). As explained in Sec. 8.3.1 below, the Kalman filter affects THD unfavorably. Note that for the Kalman algorithm to function effectively, the noise shaping modulators of the demonstrator system must be enabled. Otherwise, the HB quantization noise dominates the noise components that relate to sensor noise and hence, the Kalman algorithm achieves only a vanishing SNR improvement.

Fig. 8.5 illustrates SNR measurements with the Kalman filter for the three analyzed loads, with a controller update rate of $f_{PWM} = 100\,\text{kHz}$. As observed in Sec. 7.6.2, at very high SNR values, the achievable performance is limited by the noise of the DC supply. Nonetheless, the SNR can be improved in excess of 10 dB by the presented steady-state Kalman filter. However, despite employing a sophisticated processing platform, the Kalman filter execution rate is limited to 100 kHz, which is mainly due to the time required to perform the floating-point operations for the calculation of (8.10) and (8.11), and the data transfer between the FPGA fabric and the CPU memory. The execution time

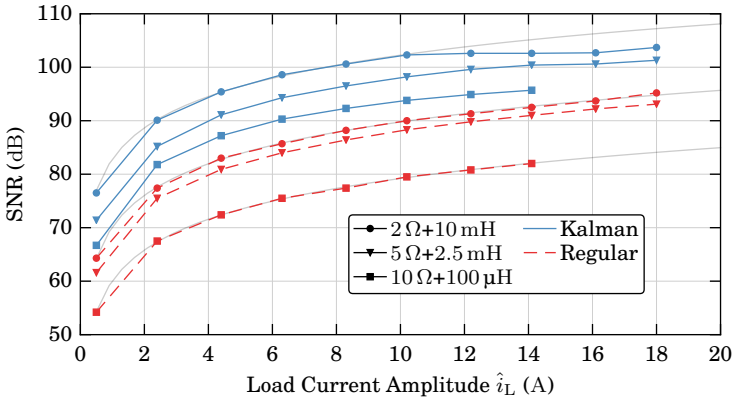

Fig. 8.5: Measurement of the load current SNR improvement by the Kalman filter. Deviation from fitted line at high SNR is due to DC supply noise at high powers. All controllers and the Kalman filter algorithm are executed with $f_{PWM} = 100\,kHz$. $u_{DC} = 400\,V$, $f_F = 35\,Hz$.

could be lowered by implementing the entire algorithm in the FPGA fabric as a digital design. This, however, substantially increases complexity, prolongs development times and reduces design flexibility, as explained previously.

A similar noise performance than what is achievable with an enabled Kalman algorithm can also be obtained with the regular control system, but executed with $f_{PWM} = 200\,kHz$. This facilitates controllers with higher open-loop gains and thus, improved disturbance rejections, which reduces the influence of noise sources such as the DC supply or the pulse-width modulators. **Fig. 8.6** illustrates this by comparing the relevant measurements as indicated. If the Kalman filter would also be executed at a rate of 200 kHz, the SNR would even further improve. Note that the Kalman filter is especially effective at improving the SNR of the 100 µH load, despite the reduced control gains. This load inductor is not subject to significant external noise due to its few winding turns and small size. Thus, sensor noise is a dominant contributor to the amplifier's overall output noise and hence, the control system with the enabled Kalman filter can effectively reduce this noise source. Higher control gains can only marginally improve the SNR of this load, as sensor noise dominates (cf. **Fig. 7.21**). The two other load inductances generally achieve a better SNR due to their higher impedances, but sensor noise is not dominating as these inductors are subjected to noise related to EMI sources

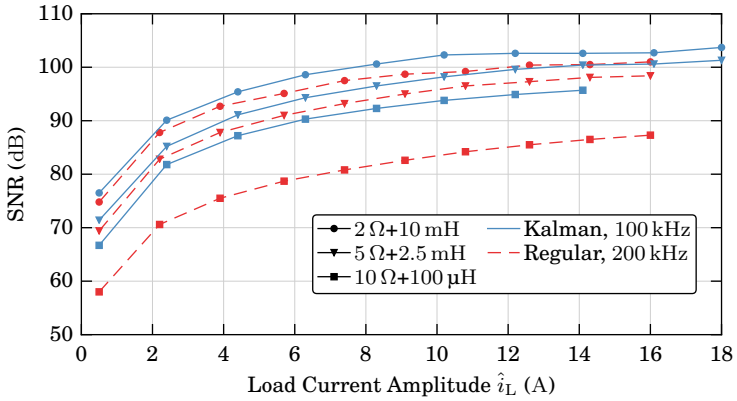

Fig. 8.6: Measured load current SNR performance comparison between the control system with the enabled Kalman algorithm, calculated at a rate of 100 kHz, and the regular controllers that use the unmodified measurements, but tuned for an execution rate of 200 kHz. The PWM frequencies correspond to the controller execution rates. This plot combines the data from **Fig. 8.5** and **Fig. 7.21**.

and hence, the Kalman filter is not as effective. This susceptibility to external noise sources of the selected load inductors is also discussed in Sec. 7.6.2.

In summary, the effectiveness of the Kalman algorithm depends on the noise environment of the amplifier. If the load current noise is dominated by sensor noise, the Kalman filter can provide a significant improvement. If, however, other sources of noise, which act as disturbances to the control system dominate, it can be advantageous to refrain from utilizing a Kalman filter and instead select a higher controller execution rate (which requires an increased converter switching frequency), with the correspondingly improved disturbance rejection.

8.3.1 Distortion Due to the Linear Model

The employed Kalman filter utilizes a linear system model of the converter and the load in order to estimate the true values of its voltages and currents. As outlined in Sec. 8.1.3, the Kalman filter provides a tuning parameter (the Kalman gain) that weights its predictions, which are based on its linear model, against the measurements to produce a new estimate of the system states. If the filter prediction is weighted more, sensor noise is effectively attenuated since less emphasis is put on the (noisy) measurements to create the new

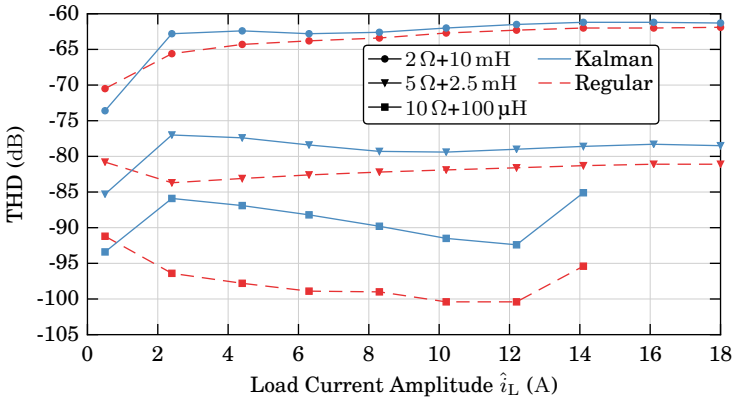

Fig. 8.7: Effect of the Kalman filter on the measured load current THD. The trade-off between noise filtering and deterioration of the THD is affected by a tuning parameter of the Kalman filter. The sudden increase of THD at high load currents with the 10 Ω load is due to the DC supply output current limit. $u_{DC} = 400\,V$, $f_{PWM} = 100\,kHz$, $f_F = 35\,Hz$.

estimates. On the other hand, by weighting the measurements more than the predictions from the linear model, the estimates become more noisy. As a linear system model is used to create the filter predictions, nonlinearities, such as current-dependent inductances or thermal coefficients of load resistors, are not modeled and hence, the filter predictions do not contain any harmonics. Consequently, if the Kalman gain is tuned with emphasis on the predictions, harmonics, like noise, are attenuated in the filter estimates, as the linear model allows for neither. This has the adverse effect that the actual harmonics present in the output current are then not supplied through the error signals to the feedback controllers and thus, the THD deteriorates. Consequently, the Kalman gain can be used to tune the trade-off between the reduction of load current noise and the allowable deterioration of the THD.

Measurements shown in **Fig. 8.7** illustrate this effect. With the Kalman filter enabled, the THD degrades while at the same time, the load current noise is significantly reduced (not shown here, see Sec. 8.3 above). The THD could potentially be improved by employing a Kalman system model that incorporates the nonlinearities of the physical system (e.g., current-dependent inductances). However, this requires an accurate model of the nonlinearities and potentially increases the computation time of the Kalman algorithm, with

the result of decreasing the achievable controller execution rate. This also affects the THD adversely due to the corresponding reduction of controller gain.

A similar effect potentially influences the noise rejection of the amplifier when the Kalman filter is used, as the filter's linear model cannot consider external disturbances, like EMI that couples directly into the load, e.g., into the windings of an actuator. Consequently, such signal components are attenuated by the Kalman estimator and not present in its output. Thus, they do not appear at the inputs of the feedback control system and cannot be rejected by it. Due to the often parasitic nature of such external noise sources, an application-specific tuning of the Kalman gain is required in order to optimize the overall noise rejection of the amplifier, or an inclusion of such sources, if they can be modeled with sufficient accuracy, in the process noise matrix. Again, the effectiveness of the Kalman filter depends on the noise environment of the power amplifier system.

8.4 Summary

The high sensor noise sensitivity of the closed-loop amplifier feedback control system is demonstrated by the effectiveness of a Kalman filter algorithm that serves as an estimator to further reduce sensor noise. Due to the static noise conditions in the power converter (i.e., the sensor and process noise (co)variances do not change over time), a steady-state Kalman filter implementation can be employed, which provides comparably little computational complexity and enables its execution with a frequency of 100 kHz. This is also facilitated by the high-performance processing system of the hardware demonstrator, and is required to maintain high controller gains. Measurements demonstrate that the load current SNR can be increased by more than 10 dB when the Kalman filter is employed, reaching levels that approach 104 dB (DC–10 kHz). With low-noise amplifier supplies, load current SNR figures in excess of 108 dB are obtained (see **Fig. 7.23** in Sec. 7.6). The Kalman filter is especially effective if sensor noise dominates the load current SNR, as an increased gain of the feedback controllers cannot be used to reduce this source of noise.

However, the linear system model, upon which the algorithm bases its predictions, does not allow for harmonic distortion and hence, such components are, unfavorably, also attenuated by the Kalman filter. This prevents their rejection by the closed-loop control system. However, the Kalman filter can be tuned to take this effect into account, and a trade-off between sensor noise attenuation and the deterioration of the amplifier's linearity can be found. The

same applies for external noise sources that are difficult to model as process noise, due to their often parasitic or intermittent nature. Consequently, the noise environment of the amplifier must be considered and the Kalman filter must be tuned accordingly to obtain the optimal performance.

This chapter reveals that a Kalman filter provides a viable and simple method to attenuate sensor noise in closed-loop precision power electronic converters, and only a sufficiently capable digital signal processing system is required. Thus, it is also possible to reduce the cost and complexity of the voltage and current sensors, as the Kalman filter can partly compensate their noise-related deficiencies. Furthermore, if the switching frequency of a converter cannot be further increased, which would enable feedback controllers with higher gains, a Kalman filter can potentially be employed to increase the SNR.

9 Feedforward Distortion Compensation

The inherent distortion of output power waveforms created by regular half-bridge (HB) power topologies (i.e., no dual buck (DB) operation) can be reduced with methods that compensate the errors caused by the underlying nonlinearities, by correcting the HB output voltages accordingly. This is achieved by modeling the nonlinear behavior of the switching stage, from which the required corrective actions can be derived. With the regarded amplifier systems, this results in the continuous adjustment of the HB duty cycles during operation. This approach can significantly reduce sources of distortion in this power stage arrangement, which is favorably characterized by a simple structure and high efficiency, as compared to the low-distortion DB topology.

In this chapter, two fundamental imperfections of the HB switching topology are addressed: the HB interlock time required to prevent a short-circuit of the DC-link, and the inherently low power supply rejection. First, **Sec. 9.1** models the HB switching behavior during the dead time interval in real-time, from which the resulting voltage error is derived and used to compensate the duty cycle accordingly. The effectiveness of the method is presented with the hardware demonstrator system. Second, **Sec. 9.2** measures the variation of the HB DC supply voltage and compensates the duty cycle such that the requested voltage is effectively obtained at the output of the power stage. As shown with measurements, the power supply rejection of the amplifier is increased.

9.1 Dead Time Compensation

The measurements with the hardware demonstrator in Sec. 7.6.1 confirm the expected high sensitivity of the amplifier output waveform distortion to the HB interlock time, when operated with the regular interleaved power stage topology. As shown in **Fig. 7.19**, the THD improves from −82 dB to −98 dB when the dead time is lowered from 90 ns to 30 ns, despite closed-loop feedback control. The DB converter topology, detailed in Sec. 3.1 is designed to avoid this source of distortion, with the fundamental disadvantage of considerably increased conduction and switching losses of the main power conversion components. Sec. 7.6.3 illustrates the losses of the two power stage topologies with measurements.

Consequently, this section presents a method that calculates the erroneous output voltages of each HB in the regular interleaved power stage topology. They are caused by the current-dependent behavior of the HB switch-node voltage during the dead time interval (see Sec. 2.3 and Sec. 3.1). This effect is modeled in real-time, i.e., during converter operation, by the control system and the HB duty cycles are corrected correspondingly to obtain the desired switching stage output signals. In the past, different methods to reduce dead time induced distortion by means of a feedback or feedforward system have been presented [95, 253–259].

However, an extensive dead time compensation method that considers different effects, such as ripple currents or detailed switching waveforms, can be employed in the demonstrator system due to the availability of all HB current and voltage measurements, and a high-performance digital processor. Its key feature is the real-time calculation of the deviating voltage-time areas introduced by dead time (see the colored areas in **Fig. 9.1 (d)**, which is similar to **Fig. 3.1**). Thus, the duty cycle of each HB is independently corrected such that the desired voltage-time area is applied to the HB inductor, hereby reducing distortion caused by the dead time intervals. To further enhance the performance, the HB current ripple is also calculated and considered.

Fig. 9.1 illustrates the algorithm. In order to model the HB switching behavior, especially with respect to the soft- and partially soft-switched transitions, resulting in the varying voltage-time areas A_S or A_{PS} that depend on the instantaneous HB output current at the switching instant, the algorithm assumes a (linear) equivalent HB capacitance $C_{HB,Eq}$, comprising the parasitic power transistor capacitances C_{oss} as well as parasitic capacitances of the PCB layout and the HB inductor. During the switching transition, it is assumed that $C_{HB,Eq}$ is charged/discharged by a constant current, which,

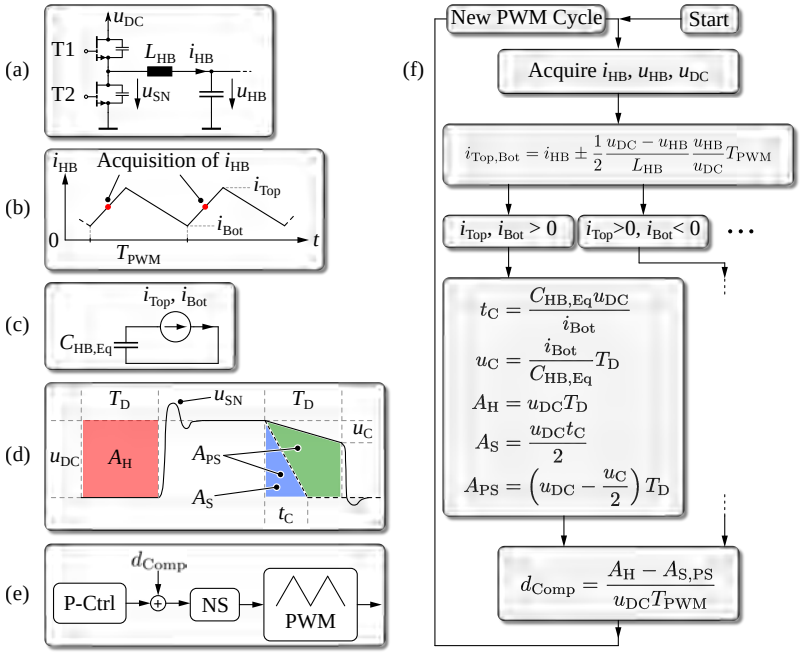

Fig. 9.1: Dead time compensation algorithm used for each HB. **(a)** Considered HB arrangement. **(b)** Synchronous sampling of the HB current sensors once per PWM cycle, and denomination of the current ripple. **(c)** Equivalent circuit and linear capacitance used to model the soft-switched transitions. **(d)** HB switch-node voltage waveform with error-areas due to dead time T_D (cf. **Fig. 3.1** in Sec. 3.1). **(e)** The compensation value d_{Comp} is added to the requested HB duty cycles of the P-current controllers. NS: Noise shaper, for high-resolution PWM generation (see Ch. 5). **(f)** Flow diagram and utilized equations of the compensation algorithm. Note that the algorithm is shown for $i_{Top,Bot} > 0$. For the other cases, the method works accordingly. The algorithm is not necessarily executed every PWM cycle, as the calculation can take more than one cycle.

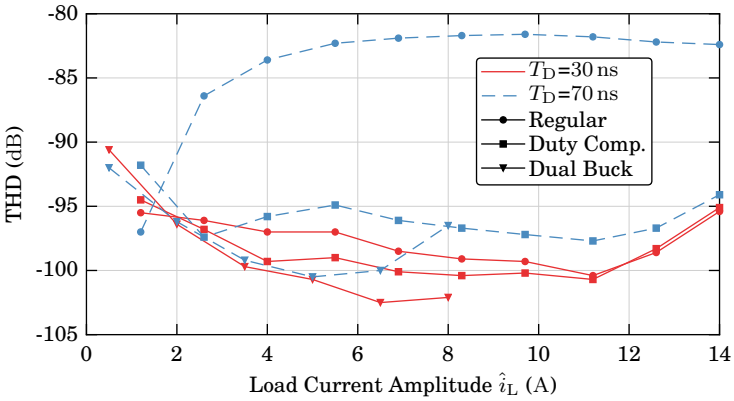

Fig. 9.2: Measured THD improvement with the duty cycle compensation method, compared to the regular interleaved power stage and the DB topology. Load: 10 Ω+100 µH, f_F = 35 Hz, u_{DC} = 400 V, f_{PWM} = 100 kHz, I_B = 5.5 A for the DB topology.

due to the large energy storage provided by L_{HB} compared to the energies stored in $C_{HB,Eq}$, is valid for a wide current range [127]. Consequently, the soft-switched transition times of the switch-node voltage u_{SN} can be conveniently calculated, as shown in **Fig. 9.1**. The value of $C_{HB,Eq}$ can be estimated from the output capacitances of the power transistors, the PCB layout and the HB inductors. It can also be tuned during converter operation such that the THD of the amplifier output is minimized. Due to the nonlinearity of the power transistor parasitic capacitances, the value for $C_{HB,Eq}$ depends on the DC-link voltage. In the demonstrator system, this value ranges from ≈300 pF to 400 pF (u_{DC}=200 V to 400 V).

The effectiveness of the method on the load current THD of the amplifier demonstrator system is illustrated with measurements in **Fig. 9.2**, which repeats some results of **Fig. 7.20**. If the system operates with T_D = 70 ns, the benefits of the presented method are clearly observable and it reaches THD levels close to what the DB topology can achieve, with the added benefit that the allowable load current is not limited, as the converter losses are not affected by the compensation method. The presented compensation algorithm is not subject to any dynamic behavior and works equally during amplifier load steps or changes in the operating conditions, as all required variables (e.g., the HB current) are known at all times. Furthermore, mea-

surements show that the load current SNR is not affected by the presented method.

The algorithm is executed regularly and synchronously with the converter switching frequency at a rate of 50 kHz, which is limited by the capability of the digital signal processor of the demonstrator system (the algorithm is implemented as a procedural program). Due to the comparably slowly varying HB currents, with fundamental frequencies of usually less than ≈300 Hz in mechatronic positioning systems, the achieved execution rate of the algorithm is sufficient. Its execution speed could be increased by employing a lookup table instead of calculating the compensation values in real-time. Measurements show that its performance is independent of the selected load current fundamental frequency. Nonetheless, an implementation of this method with digital logic circuits within an FPGA could substantially increase the execution rate and render it identical to the PWM frequency. However, care must then be taken to avoid numerical errors due to the fixed-point arithmetic that is commonly used in such implementations, which increases complexity and development effort.

The DB topology still achieves a slightly better performance, which is mainly attributable to the fact that a linear equivalent capacitance is used to model the switching behavior, whereas the shape of the HB voltage transitions is determined by the highly nonlinear power transistor capacitances. Additionally, the assumption of a constant current during the HB transition to charge/discharge the capacitances also breaks down at small current amplitudes [127]. Furthermore, the actual dead time can also be slightly different from what the algorithm assumes, due to propagation delay skews between different gate signal paths, mostly caused by the propagation timing tolerances of the employed digital signal isolators that transmit the gate control signals to the corresponding power devices.

9.1.1 Summary

The presented duty cycle compensation method can significantly lower distortion caused by HB dead time, without affecting converter losses and the achievable load current magnitude, or the SNR of the amplifier output waveform. This is enabled by a comprehensive model of the switching transitions, which also considers the soft and partially soft transistor switching actions in real-time during operation. This is enabled by the measurement of all relevant quantities such as HB currents or output voltages by the feedback control system. With a dead time of 70 ns, THD can be improved by up to 15 dB, reach-

ing values close to −100 dB. With a dead time of 30 ns, distortion is already significantly reduced and the presented method yields a THD improvement of up to 2 dB. The DB topology, which can only achieve a significantly reduced output current due to its increased losses, improves the THD at this selection of dead time by ≈4 dB, to values below −102 dB.

Thus, the presented compensation method, which is implemented without effort as a procedural program in a digital processing system, is especially effective with commonly used dead times of ≈100 ns or more, whereas neither the DB topology nor the presented feedforward approach result in a significant improvement of THD when ultra-low dead times are used.

9.2 DC-Link Voltage Compensation

The supply voltage is a potential source of undesired signal components in the power output of a switch-mode amplifier, as it directly affects the switched HB voltages during the turn-on intervals of the high-side transistors. Open-loop Class-D amplifiers in principle have an insufficient power supply rejection and/or limited applicability for precision applications [102–104]. If the power converter drives a bridge-tied load, as it is the case with the demonstrator system, where the load is connected between the two converter output phases (see Sec. 7.1), the (differential-mode) load voltage u_L, averaged over a switching period, is given as

$$u_\mathrm{L} = u_1 - u_2 = u_\mathrm{DC}\,(d_1 - d_2)\,, \tag{9.1}$$

whereas $d_{1,2}$ are the HB duty cycles of the two phases (assuming operation with the regular interleaved HB topology):

$$d_1 = d_\mathrm{CM} + m\sin(\omega_\mathrm{F} t), \tag{9.2}$$

$$d_2 = d_\mathrm{CM} - m\sin(\omega_\mathrm{F} t), \tag{9.3}$$

and d_CM is the common-mode (CM) component of the duty cycles to enable bidirectional load voltages ($d_\mathrm{CM} = 1/2$). Thus, as u_L is a function of u_DC, and $d_1 \neq d_2$ due to the AC output waveforms commonly used for actuators in positioning systems, the sensitivity to variations in the DC supply is generally high. This is especially the case at low frequencies, where the HB filter stage and the high-frequency EMI filter do not provide significant attenuation. The closed-loop feedback control system reduces this sensitivity considerably, but nonetheless, if the DC-link voltage variation correlates to the converter output current, harmonic distortion is introduced. This is, e.g., the case with

a single-phase load that is characterized by a fluctuating power and hence, an accordingly varying amplifier input current. The DC power supply, which usually has a given output series impedance $Z_s \neq 0$, and a limited disturbance rejection, cannot maintain a constant output voltage and hence, the DC-link voltage varies correspondingly. This variation is usually less than several volts and is finally attenuated by the closed-loop control system, but has to be considered for low-distortion power converters. Additionally, uncorrelated spectral components originating from the DC supply, such as 50 Hz spurs from the grid, or other noisy components, are also not ideally rejected by the amplifier and thus transmitted through the switching stage to the load.

In the demonstrator system, the required HB duty cycle d is normally calculated from the P-type current controller output, which is the requested HB voltage u^*_{HB}, by assuming a constant DC-link voltage value: $d = u^*_{\mathrm{HB}}/u_{\mathrm{DC,Const}}$. However, since the system is capable of measuring u_{DC} during operation, the instantaneous value of u_{DC} can be used for the determination of the duty cycle: $d = u^*_{\mathrm{HB}}/u_{\mathrm{DC,Meas}}(t)$. Consequently, the duty cycle is compensated in real-time during converter operation to take any variation of the HB DC supply voltage, which can be caused by the single-phase power ripple or the DC supply system itself, into account. The DC-link voltage at the HBs is measured once per PWM period and the duty cycles are adjusted correspondingly. Such feedforward methods are also applied in audio amplifiers [121], with the disadvantage of requiring an additional voltage sensor.

The performance of this simple method is explored in the following by adding a series resistance to the DC supply in order to introduce a load current dependent variation to the amplifier's DC-link voltage, caused by the single-phase power ripple. The sensitivity of the load current THD to the DC supply series output resistance is shown in **Fig. 9.3** with the demonstrator system, with and without the mentioned duty cycle compensation. It is evident that a DC supply series impedance deteriorates the load current THD, especially at high amplitudes, and despite the usage of closed-loop feedback control. However, when utilizing the feedforward compensation method, the THD is not affected by the varying supply voltage. Note that the presented compensation method is also effective at attenuating other undesired signal components from the DC-link voltage, which are potentially originating from the supply, like voltage variations at 50 Hz caused by the grid voltage that is insufficiently attenuated by the DC supply system.

Note that in **Fig. 9.3**, at low currents, the THD seems deteriorated by the usage of the feedforward compensation method. This is an artifact, as the measurement of u_{DC} introduces noise to the duty cycle (through sensor

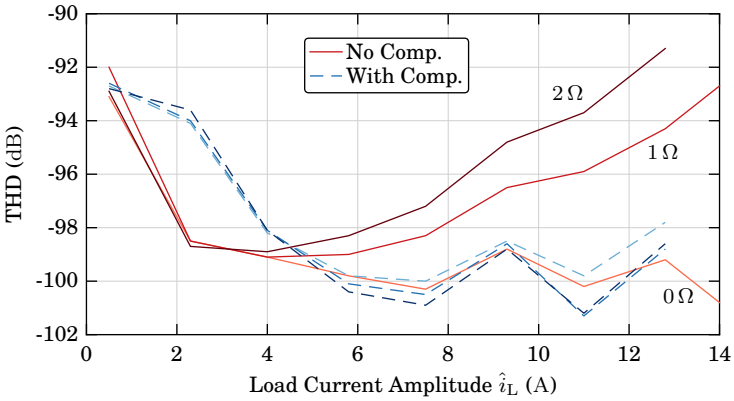

Fig. 9.3: Measured influence of an (ohmic) series impedance of the DC supply on the THD. Measuring the varying DC-link voltage and compensating the HB duty cycles accordingly improves the THD. $u_{DC} = 200\,V$, $f_{PWM} = 200\,kHz$, $f_F = 35\,Hz$. Load: 10 Ω+100 µH

noise), which consequently increases the load current noise and thus, some harmonics are masked in the spectrum. This renders the THD measurement inaccurate at low load currents. A low-pass filter could reject some noise from the DC supply voltage measurement and reduce this effect. Nonetheless, a disadvantage of this compensation method is revealed, as it potentially increases the load current noise in the described manner.

9.2.1 Summary

This analysis corroborates the need for a stable and low-noise DC amplifier supply system. Any DC-link voltage variation is generally reflected in the amplifier output waveforms, as the converter has a limited power supply rejection. Even though the closed-loop feedback control system significantly improves the supply rejection, a compensation method is presented to further increase the system's resilience to varying supply voltages.

This is accomplished by measuring the instantaneous amplifier DC-link voltage during converter operation and compensating the duty cycles accordingly, such that the desired output voltages are produced. Measurements are performed that demonstrate the effectiveness of this simple solution for the case of an increased supply series impedance that leads, due to the single-phase current ripple, to a corresponding variation of the amplifier's supply

voltage. This is especially critical at high load powers, where it is shown that the amplifier maintains the same distortion performance when utilizing the real-time duty cycle compensation, as with a nearly ideal supply impedance. However, the method potentially introduces noise to the duty cycles through a noisy voltage acquisition of u_{DC}, which can result in a reduced output SNR.

10 Conclusion and Outlook

Precision power amplifiers, characterized by power output signals of low noise and low distortion, are required in important medial, scientific and industrial applications, in which power levels and signal frequencies span several orders of magnitude. This thesis focuses on amplifiers that generate well-controlled output currents for electromagnetic actuators in nanometer-precision mechatronic positioning and motion systems. They are commonly used in the integrated semiconductor manufacturing industry, for processes like wafer lithography or inspection. Different actuators, such as levitating magnetic bearings, voice coils or permanent magnet synchronous motors are normally employed, but all require currents of extremely low noise and distortion to prevent the generation of erroneous forces or torques that would lead to inaccuracies in the position or speed of the mechanical systems. Such positioning systems provide little (mechanical) damping at frequencies below 10 kHz and thus, actuator current noise and distortion is critical in this range.

Linear or hybrid amplifiers are traditionally used to provide the required currents for the employed electromagnetic actuators of the motion systems. However, they generally suffer from limited output powers and efficiencies, and do not scale well due to heterogeneous power stage designs, which increases cost and development effort.

Therefore, this thesis analyzes and optimizes key sources of noise and distortion in digitally controlled, switch-mode power amplifiers, which can provide high efficiencies and considerable output powers. Likewise, the digital nature of the control system provides flexibility and it can be employed in a wide range of amplifier systems. The obtained results are applicable for any type of switch-mode conversion arrangement.

In the past, different sources of noise and distortion in such systems have been described in literature, as these types of amplifiers are in use for more than 40 years. However, the nonlinear nature of many important sources of noise and especially, distortion, renders a rigorous mathematical analysis difficult. Therefore, this thesis comprehensively investigates important amplifier components with detailed computer simulation models and hardware prototypes. Causes of noise and distortion are identified and compared, and core power conversion and control elements are optimized in order to render them suitable for ultra-high-precision amplifiers.

10.1 Conclusions and Results

The analysis and design efforts are reflected by unprecedented noise and distortion figures that are achieved with an exhaustive hardware demonstrator system. It operates with DC-link voltages up to 400 V and provides load currents that reach 25 A (peak). Modern GaN power transistors facilitate fast switching transitions, leading to low distortion and low losses. Pulse-width modulation (PWM) frequencies up to 200 kHz are achieved, which enables high-gain feedback control systems. In the following, key results are summarized.

10.1.1 Low-Distorion Amplifier Power Stages

This work compares the regular interleaved half-bridge (HB) power stage and the dual buck (DB) topology, both with simulations and measurements. The latter is designed to avoid distortion caused by HB interlock time, through the introduction of a bias current that linearizes the power stage switching behavior. In the regular HB topology, this dead time is confirmed to be a considerable contributor to the harmonic distortion of the amplifier load current. Hence, the DB topology is capable of effectively rejecting this source of nonlinearity, which results in a load current total harmonic distortion (THD) of less than −102 dB (0.000 79 %), as demonstrated with the demonstrator system. However, the DB converter induces considerable transistor losses due to its bias current. This results in a reduced amplifier output current capability to prevent the thermal destruction of the switching devices, and a correspondingly limited power conversion efficiency.

However, due to the usage of modern GaN power transistors, which enable fast switching transitions, the interlock time of the regular HB power stage can be reliably reduced to values as low as 30 ns. This effectively

decreases harmonic distortion and it is shown how the achievable THD of this topology is diminished by less than 5 dB as compared to the DB power stage. Advantageously, the regular HB arrangement achieves considerably higher output currents (by a factor of 3), due to the lack of a bias current. THD values of ≈−100 dB (0.001 %) are achieved over wide load current ranges.

The fast switching speeds of the GaN transistors, exceeding 300 kV/µs at the HB switch-nodes, reduce distortion originating from the switching stage, as the switched output voltages approach the rectangular shape of the reference waveforms (i.e., the PWM output signals). Modern power transistor packages (which provide cooling paths through the top side of surface-mounted devices) lead to circuit designs with low parasitic elements, which further improves the voltage-forming qualities of the switching stages. The low losses of the employed devices facilitate high switching frequencies and correspondingly high open-loop gains of potentially employed feedback controllers (200 kHz at a DC-link voltage of 400 V are achieved with the hard-switching amplifier demonstrator).

The residual sources of harmonic distortion within the amplifier power stage comprise the remaining HB dead time, the nonideal switching transitions and the variation of the amplifier DC supply voltage, which is especially of concern when operating with single-phase loads, due to the resulting power ripple. The thermal modulation of the power transistor on-state resistances is shown to be of negligible influence and does not deteriorate the load current THD. Similarly, the pulse-width modulators, which can also cause low-frequency harmonics, are operated at sufficiently high pulse repetition frequencies such that modulated sinusoidal signals with fundamental frequencies below ≈500 Hz, which is a common frequency range of actuator currents in positioning systems, do not contain significant harmonics. Measurements have demonstrated that the linearity of the amplifier filter and load inductors, as well as the load resistors, is of significance. Hence, highly linear parts (i.e., high saturation currents, constant inductance values and low thermal coefficients of resistance) are required.

10.1.2 Low-Noise Switch Control Signal Generation

Signal jitter, which can be caused by the stochastic variation of a signal path's propagation delay, adds wideband noise and thus limits the signal's achievable signal-to-noise ratio (SNR). Power electronic converters, whose switching actions are controlled by rectangular waveforms, are especially susceptible to jitter, which is mainly introduced by the signal isolators that are required

for the propagation of power transistor gate control signals to galvanically isolated potentials, as measurements demonstrate. Thus, a low-jitter gate driver circuit is developed, which is capable of reducing jitter of the isolated gate control signals to values below 20 ps RMS, while at the same time being immune to fast common-mode (CM) voltage transients across its isolation barrier. Measurements demonstrate its functionality and performance. It is capable of increasing the SNR of a 400 V, open-loop power amplifier by 20 dB, as compared to a regular (jittery) gate driver, to 107 dB (DC–10 kHz).

It is also shown how digital PWM introduces significant quantization noise due to the fact that it must be implemented with limited-resolution digital counters in order to achieve the desired pulse repetition frequencies. Thus, digital delta-sigma modulation (noise shaping) is utilized, which is a digital signal processing technique that can shift quantization noise to higher frequencies, where it does not affect the considered mechatronic actuators. An implementation of such a structure, which is specifically favorable for digital designs, is introduced and optimized for noise attenuation and stability. Simulations and measurements confirm the effectiveness of the method, as the SNR of PWM output signals can be increased by more than 30 dB in contrast to traditional PWM signal generation approaches.

Despite the introduction of low-noise techniques, the discussed amplifier system still contains some sources of noise. This is, in part, caused by residual noise from the digital pulse-width modulators and the noise shapers. The presented delta-sigma modulators can achieve lower noise levels with higher converter switching frequencies, which corroborates the need for low-loss, high-frequency GaN power transistors. The low-jitter gate drivers achieve jitter figures below 20 ps and do not significantly contribute to noise originating from the switched HBs. However, the DC supply can inject significant noise powers and undesired signal components into the amplifier system, whose power supply rejection is limited. This is confirmed by multiple measurements with the hardware demonstrator. Thus, stable, low-noise amplifier supplies are necessitated. Likewise, load inductors and resistors can be subject to external sources of EMI, which creates undesired load current noise. A high-gain feedback control system is capable of rejecting these noise sources and is thus an integral part of such power amplifiers.

10.1.3 Feedback Control

Closed-loop control systems provide disturbance rejection and improve reference tracking, which reduces undesired signal components in the amplifier

output waveforms. However, a significant limitation is their inherently high sensitivity to faulty or noisy measurements.

Thus, circuits and methods to obtain low-noise and low-distortion current and voltage sensors for power converters are introduced, analyzed and compared. It is shown that shunt resistors are effectively the only current sensing technique for achieving low-noise (≈110 dB SNR, DC–10 kHz) and low-distortion (<−110 dB THD) current measurements, as integrated, isolated sensors only provide a sufficient performance with a considerable sensor volume and cost. Similarly, high-voltage resistive dividers reach SNR figures in excess of 120 dB, if the resistors are carefully selected. The linearity of operational amplifiers is individually analyzed as consistent data is, in contrast to their noise models, often not available. It is shown how single-stage amplifiers achieve THD figures below −110 dB (with a gain of 20), and that higher-order analog filters can be designed without significantly affecting the SNR and THD of the corresponding signal path. Furthermore, oversampled analog-to-digital conversion is employed to reduce ADC quantization noise, whereas the required digital decimation filter is optimized with respect to its phase delay. ADC sampling jitter introduces noise and thus, digital signal isolators, which potentially are a considerable source of jitter, and which are regularly used in power electronic converters where galvanically isolated measurements are required, must be carefully analyzed.

Due to the high-performance digital processing system of the demonstrator amplifier, the influence of a real-time Kalman filter is investigated, which is capable of further reducing sensor noise, and operates with an update rate of 100 kHz. Despite the low-noise sensors, the load current SNR can be increased by more than 10 dB, and amplifier load current SNR figures as high as 108 dB are recorded. Due to the linear model of the estimator and the slightly nonlinear physical system, the amplifier's harmonic distortion can be affected when the Kalman filter provides the low-noise sensor data for the feedback controllers. The trade-off between sensor noise reduction and increased THD can, however, be tuned.

Model-based feedforward compensation techniques are employed to further improve the load current quality. They only require sufficient computational resources. The voltage-forming errors of the HBs, caused by dead time, can be calculated in real-time during converter operation, which enables corresponding duty cycle corrections. The achieved THD figures approach the performance of the DB topology, without limiting the amplifier's output current capability. Similarly, the instantaneous DC-link voltage can be con-

sidered when forming the HB duty cycles, which improves the amplifier's power supply rejection.

High converter switching frequencies minimize delay and enable high-gain feedback controllers, which is tantamount to their effectiveness in reducing load current noise and distortion. If the control algorithms are implemented with digital logic based on fixed-point arithmetic, to obtain low control system calculation times (e.g., with an FPGA), controllers with high gains can become unstable due to numerical saturation or overflow effects, which limits the achievable performance of such feedback control system implementations.

10.2 Opportunities and Outlook

In the following, different concepts are presented which could potentially further improve the SNR and THD of the discussed switch-mode power amplifiers.

Note that the already achieved performance cannot be arbitrarily increased due to restrictions regarding noise and linearity of available current and voltage sensing technologies. The state-of-the-art equipment used to obtain the reference measurements can acquire SNR and THD figures up to $\approx \pm 120\,\mathrm{dB}$.

10.2.1 Hybrid Switch-Mode Power Converters

The achieved THD of the presented amplifier system ($\approx -100\,\mathrm{dB}$ over wide load current ranges) is, at least in parts, limited by the finite gain of the control system. The performance of the feedback controllers is closely linked to their execution frequency and hence, as demonstrated with measurements, high converter PWM rates increase the controller's disturbance rejection capabilities and thus, the THD and SNR improve. Due to switching losses, an arbitrary increase of the controller execution frequency is not possible.

Thus, a hybrid amplifier, comprising two distinct switch-mode converters, could be employed to overcome this limitation. This approach, however, significantly increases the complexity and heterogeneity of the power conversion system. The basic concept is illustrated in **Fig. 10.1**. The main power converter delivers the majority of the load power and is limited in its switching frequency and control gains. Thus, a low-voltage, high-frequency auxiliary converter can provide a corrective influence to reduce the error of the load current. Due to its low operating voltage and output power, its switching

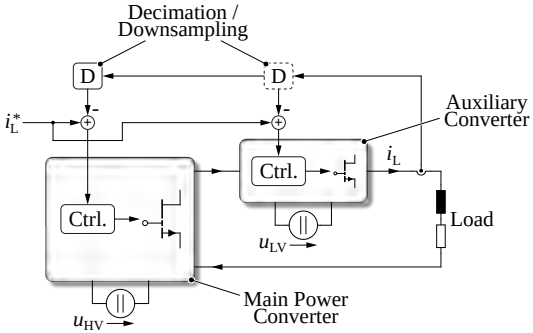

Fig. 10.1: Hybrid switch-mode amplifier concept comprising two different power converters. The main converter delivers most of the load power and operates with a high DC-link voltage, which consequently limits its switching frequency. A low-power, high-frequency auxiliary converter is used to further improve the load current.

frequency can be considerably increased, which enables a high-gain control system of the auxiliary converter. Different hybrid converter structures are possible [48, 49, 260, 261].

This approach requires a load current sensor that delivers its measurements at a sufficiently high rate and low noise level. In the demonstrator system, an 18-bit ADC, sampling at 5 MHz, is employed. Thus, the auxiliary converter could operate at a switching frequency of also 5 MHz, or at a lower rate, which then necessitates decimation and downsampling (see Ch. 6.4).

Fig. 10.2 illustrates a possible circuit constellation that integrates such an auxiliary converter with the power topology of the presented hardware demonstrator. Two buck converters are connected in series to the phase filter capacitors and can thus directly influence the load voltage in order to generate the necessary correcting load currents [125]. Their low-voltage supply u_{LV} (e.g., 20 V) can be generated from the main converter's 400 V DC-link.

However, the addition of the auxiliary converter complicates the dynamic system and it must be considered for the tuning of all feedback controllers. Furthermore, the interaction between the main and the auxiliary converter, e.g., during transient load current steps, must be analyzed in order to ensure stability and appropriate dynamic responses (e.g., overshoot or damping). These aspects complicate the design process. Hybrid amplifiers that incorporate a linear and a switch-mode power stage suffer from similar restrictions, whereas their power conversion efficiencies are reduced due to

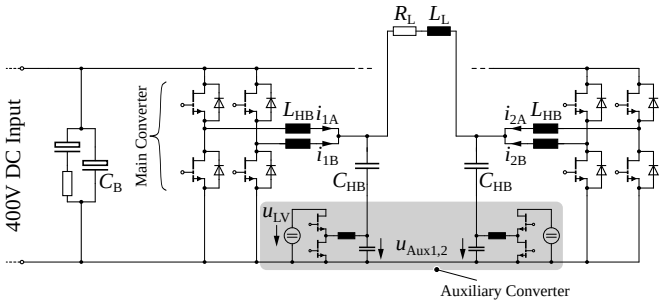

Fig. 10.2: Possible circuit topology of a hybrid switch-mode power amplifier, based on the demonstrator system used in this thesis. The two auxiliary buck converters can directly influence the load voltage. Their low-voltage supply can be generated from the 400 V DC supply of the main converter.

the linear amplifier, as compared to the combination of two switch-mode power stages.

Below, in Sec. 10.3, a novel switch-mode hybrid system is presented that combines two parallel connected power-stage topologies to incorporate the benefits of either topology.

10.2.2 High-Speed Digital Signal Processing

A state-of-the-art digital signal processing circuit, which comprises an FPGA and two CPUs, is adopted for controlling the presented hardware demonstrator. It allows the implementation of a high-frequency, real-time Kalman filter with a procedural program due to its fast floating-point processing units. Nonetheless, in order to achieve control system execution rates up to 400 kHz, the cascaded feedback controllers are implemented in its FPGA as digital logic based on fixed-point arithmetic. As demonstrated in Sec. 7.6.1, this can limit the achievable gain of the controllers due to numerical overflow and saturation effects, which destabilize the control loops.

Driven by the ongoing "smartphone revolution", which continuously increases the computational power of integrated processors, the capabilities of digital signal processing elements suitable for the control of power electronic converters are constantly extended. This will enable the implementation of high-frequency control systems with procedural programs based on floating-point precision arithmetic, which renders the controllers numerically more stable and simpler to develop. Furthermore, this might facilitate the imple-

mentation of computationally extensive controllers, such as methods that are based on model predictive control.

10.2.3 Amplifier Supply

The switch-mode laboratory power supplies used to provide the input voltage of the precision amplifier are identified as considerable sources of noise and undesired signal components that propagate through the DC-link to the load current, attenuated only by the amplifier's power supply rejection. Measurements show how this limits the achievable load current SNR, especially at high power levels.

Thus, in order to eliminate this source of noise, a high-power switch-mode supply that utilizes low-noise techniques as presented in this thesis could be employed to provide a stable DC supply for the subsequent amplifier. This essentially constitutes the series-connection of two precision amplifiers, whereas the first serves as a DC/DC converter and the second operates, e.g., as a precision inverter. A communication channel between the two converters could further improve the stabilization of the DC-link voltage, as it enables feedforward control techniques to improve the dynamic response of the supply converter.

A power pulsation buffer, based on a power electronic converter, could also be employed to provide the power ripple of a single-phase amplifier load, which leads to a constant input power of the amplifier [262]. This improves the voltage stability of any DC supply.

10.2.4 Power Transistor Technology

Ongoing development efforts continuously improve wide-bandgap power devices, which will render a wide variety commercially available. Their switching behavior with respect to speed and undesired effects, such as parasitic turn-on or ringing, will further improve. This allows the precise replication of the digital switch control signals in the physical domain, which reduces distortion and noise. Gate drivers are increasingly closely integrated within the switching transistor packages, or even the same power semiconductor dies, which simplifies the circuits of the power stages and enables fast switching transitions that also result in reduced switching losses.

10.3 The Triple Buck Converter

In the following, another novel approach to achieve high converter output powers and low distortion is presented. It is a hybrid switch-mode converter system that combines a Class-D power stage and a DB converter. It can benefit from the advantages of each topology, and as it utilizes three HBs, it is referred to as the triple buck (TB) converter.

The regular Class-D power amplifier topology, essentially comprising one or several (paralleled, interleaved) HB power stages, is commonly employed due to its low power conversion losses. However, as shown in this work, the HB interlock/dead time significantly deteriorates the achievable output signal THD. Even with interlock times below 50 ns, the THD of Class-D amplifiers is often limited to values higher than −90 dB.

The DB power stage alleviates this significant drawback of the Class-D topology (cf. Sec. 3.1). Its key characteristics are the two individual HBs and the fact that the HB currents are unidirectional and dominated by the circulating bias current I_B. Note that I_B must be selected in consideration of the expected peak output current amplitudes $\hat{i}_\mathrm{o}$ to always ensure current unidirectionality. The two HB currents i_1 and i_2 of the DB stage can be characterized by their CM and DM components: $i_\mathrm{CM} = i_1 + i_2$ and $i_\mathrm{DM} = i_1 - i_2$. Note that i_DM characterizes the circulating bias current between the two DB HBs and i_CM is the effective output current. The bridge-leg diodes can also be replaced by synchronously rectifying transistors. This improves the achievable THD further due to the equal on-state voltage drops of each HB side.

The major disadvantage of the DB converter is introduced by the fact that the HB RMS current amplitudes are, given the modulation method shown in Sec. 3.1, at least by a factor of $\sqrt{3}$ higher than with a regular, two-phase parallel interleaved Class-D topology that provides an identical output current. This significantly reduces the achievable power conversion efficiency, which, even with modern wide-bandgap semiconductors, is limited to values below 90 % (in a 400 V system as used in this work).

Hence, in the following, the combination of a Class-D power stage with a DB converter is introduced in order to benefit from the unique characteristics of each topology. Additionally, the feedback control system structure is outlined and computer circuit simulations verify the functionality of the design.

The circuit of the proposed power conversion topology is illustrated in **Fig. 10.3**. Its name arises from the fact that it employs three HBs. It combines a regular Class-D power amplifier with a DB power stage, i.e., both

converters are connected through a coupled inductor as shown. Note that a single HB is shown for either the Class-D and the DB stage, whereas it is possible to interleave several paralleled HBs for the individual conversion stages in order to increase the output power capability and/or to increase the effective switching frequency, hereby mitigating output EMI filtering efforts.

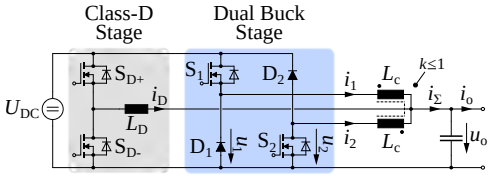

Fig. 10.3: Proposed new TB topology. The Class-D power stage provides a high conversion efficiency, while the DB stage can generate low-distortion output signals. As for the DB topology, synchronously rectified transistors could be employed instead of the freewheeling diodes D_1, D_2.

The key concept behind the TB topology is that significant output power levels, up to several kilowatts, can be provided by the efficient Class-D stage. As this topology introduces considerable distortion components due to its HB interlock time intervals, a DB stage, which can provide the desired output signals (voltage) with low error, is also employed as illustrated.

The magnetically coupled inductors are characterized by the turns ratio $N_1/N_2 = 1$, the self inductances $L_{c1} = L_{c2} = L_c$, the coupling factor $k \in [0, 1]$, and the resulting mutual inductance $M = kL_c$. The inductor arrangement fulfills two purposes: First, it provides an impedance for the circulating DM current of the DB stage, which is required for its control and to limit the DM ripple current amplitude. Second, it dynamically decouples the DB stage from the Class-D stage, which facilitates the design of the feedback control system that is commonly employed to further improve the output signal quality. Note that the magnetic coupling of the DB inductors can also reduce their overall volume [39].

The proposed converter does not utilize the Class-D stage to provide the circulating bias current of the DB stage, which is another concept to augment the DB converter as shown in [263].

In the following, a feedback control topology of the TB converter is briefly outlined and its functionality demonstrated with computer simulations.

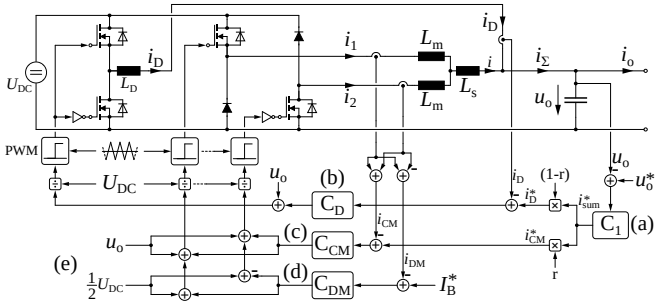

Fig. 10.4: Possible TB feedback control topology, employing cascaded controllers (C_X). **(a)** Output voltage control. **(b)** Class-D output current (i_D) control. **(c)** CM current control of the DB stage. **(d)** DM bias current control of the DB stage. **(e)** Feedforward compensation.

10.3.1 Control and Functional Verification

The TB converter provides a controlled output voltage $u_o(t)$ (or, by employing an additional feedback loop, a controlled output current $i_o(t)$). **Fig. 10.4** illustrates the proposed control topology. Note that, for the sake of clarity, the coupled inductors, as shown in **Fig. 10.3** with $k \leq 1$, are replaced by an equivalent circuit that provides the DM iductance (L_m) for the circulating current, and a series inductance L_s that decouples the DB stage from the Class-D stage.

The compensator C_1, which is typically a proportional-integral (PI) or proportional-integral-derivative (PID) type, provides feedback for the output voltage u_o, as **Fig. 10.4 (a)** depicts. Its output is the reference for the combined current i_Σ of the two converter stages. Note that an asterisk (*) indicates a controller reference signal.

The current i_Σ is formed as $i_\Sigma = i_D + i$ and thus, by introducing an (arbitrarily selectable) weighting factor $r \in [0,1]$, the current references of the Class-D stage and the DB stage can be given as $i_D^* = (1-r)i_\Sigma^*$ and $i^* = r i_\Sigma^*$, respectively. Thus, if $r = 0$, the entire output current is provided solely by the Class-D stage, and if $r = 1$, the DB converter provides the entire load current. This allows an optimization of the typical trade-off between power conversion losses and output THD in real-time during converter operation.

The Class-D output current i_D is controlled by C_D, which can also be a proportional (P), PI-or PID-compensator (cf. **Fig. 10.4 (b)**). Similarly, the output current i of the DB stage is controlled by C_{CM}. The circulating bias

current of the DB stage is, as outlined above, the difference of the two DB HB currents $i_{1,2}$. It can be controlled independently of the current i as illustrated in **Fig. 10.4 (d)**. The outputs of the CM and DM current controllers of the DB stage are combined as illustrated in order to obtain the desired reference output voltages of the two DB HBs, u_1^* and u_2^*.

To improve the transient response of the control system and to decouple the cascaded control loops, the measured output voltage u_o can be used as a feedforward compensation term, as **Fig. 10.4 (e)** shows. Finally, the required duty cycles of the three HBs are formed by pulse-width modulators, which can also be enhanced by delta-sigma modulators (noise shapers) to reduce quantization noise and to increase the output signal-to-noise ratio.

The operation of the TB converter is demonstrated in **Fig. 10.5** with a computer circuit simulation (*GeckoCIRCUITS*) that incorporates all important circuit elements and time-discrete control systems, corresponding to the diagram in **Fig. 10.4**. The output voltage reference u_o^* is sinusoidal with an arbitrarily selected frequency of 600 Hz, which results in a sinusoidal output current i_o, with a purely resistive load of 3 Ω.

As illustrated, the sharing of the output current by each converter stage can be arbitrarily selected during operation, and the currents are adjusted seamlessly according to the selection of r, which is changed during operation in **Fig. 10.5 (d)** from 0.2 to 0.6, while at the same time, I_B^* is also changed from 4 A to 11 A to ensure the unidirectinality of the currents of the DB stage.

This behavior is especially useful for converters/amplifiers in nanometer-scale mechatronic positioning applications, where the power loss of nearby converters and motor drives must be limited to avoid a thermal distortion of the sensitive positioning stages. Thus, during high-speed positioning movements, which often do not require a high output signal quality of the amplifiers, r can be selected close to 0 such that the efficient Class-D stage of the TB converter provides the desired high-power output. The achievable THD figures are then limited by the dead time of the Class-D stage, commonly to values above −90 dB, while the converter can achieve high power conversion efficiencies of typically more than 96 %, as demonstrated in this thesis. Similarly, when the positioning stage must be moved with low THD of the driving signals (often at reduced power levels), r can be selected close to 1 such that only the low-distortion DB stage provides the desired output. THD values below −100 dB can be achieved, while the conversion efficiencies are limited to values lower than 90 % (cf. Sec. 7.6.3). If r is selected between 0 and 1, the inductive voltage divider formed by L_D and L_s (cf. **Fig. 10.4**) determines

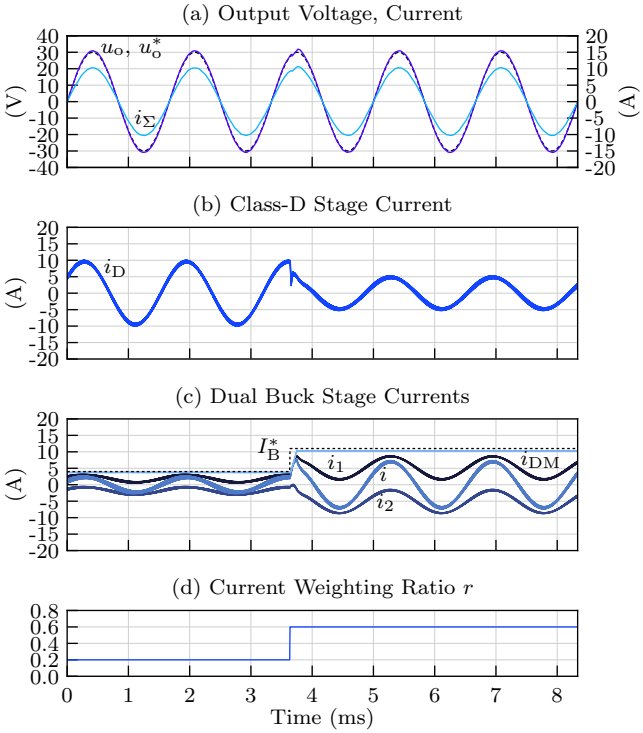

Fig. 10.5: Computer circuit simulation of the TB converter. The current sharing ratio and DB bias current are changed to demonstrate the topology's interoperability. $L_D = L_s = L_m = 100\,\mu H$, $U_{DC} = 100\,V$, $f_{PWM} = 200\,kHz$. C_1 is a PI-controller and the other compensators are of P-type.

the weighting of the contribution of the Class-D and DB stages to the overall TB converter output distortion and power conversion efficiency.

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