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Three-Phase PFC Rectifier and High-Voltage Generator for X-Ray Systems

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Abstract

MEDICAL X-ray systems have been under steady development since the discovery of X-rays by Röngten in 1895. However, the principle of X-ray generation has remained the same. Electrons are accelerated within an evacuated tube by a high-voltage difference from the cathode towards the anode. X-rays are emitted when electrons hits the anode. However, most of the energy of the electrons is dissipated by the anode in form of heat. Therefore, an X-ray power supply needs to provide not only voltages up to 150 kV but also a peak power of up to 100 kW. Since the cooling capability of the vacuum tube is typically only in the range of 1 kW, the power supply has to deliver high peak but only low average power.

In the development of X-ray systems there are three major trends affecting the high-voltage generator. First, nowadays X-ray systems use passive three-phase rectifiers which limit the application with weak power grids, emit low-frequency current harmonics and usually require adaption transformers for use with different nominal mains voltages. It is desired to use an active rectifier instead in order to provide a wide input voltage range that allows world-wide use of the device without modifications to the hardware. Second, currently available high-voltage generators typically provide rise- and fall-times of the tube voltage in the range of 500 µs. In pulsed fluoroscopy applications short rise- and fall-times of the tube voltage would eliminate the need for the cathode control grid which is necessary to keep the patient dose at a minimum. In dual energy computer tomography shorter fall- and rise-times could replace nowadays systems using two X-ray tubes at two different voltage levels by a single tube which is alternating between two voltage levels. Finally, the additional features should be achieved in a cost effective manner in order to make the technology affordable for all patients.

In order to achieve cost reductions the design of the inductive components is of particular importance. The high peak power but low average power of the application allows to reduce the volume and material cost of inductors and transformers substantially without exceeding the thermal limit. One basic element for the design of inductive components is the winding loss model which needs to take into account skin effect and proximity effect losses within the winding. An easy to use winding loss model is presented based on asymptotic approximations of the exact analytic equations for skin effect and proximity effect. Using appropriate asymptotic solutions for the low-frequency and for the high-frequency range, is usually sufficient. The error introduced by the approximations is only significant at the border between low-frequency and high-frequency range which is located approximately at the frequency where the conductor dimension equals twice the skin depth. It can be shown that windings with conductor dimensions close to this border should be avoided since they exhibit a higher AC resistance than windings with thicker or thinner conductors than twice the skin depth. Furthermore, the low-frequency asymptotic approximation allows to show that due to the proximity effect there is an optimum operating frequency of transformers which is inversely proportional to the conductor dimension and the winding width.

Based on the winding loss model an active three-phase rectifier is optimized for minimum total cost of ownership, which is the sum of material cost and loss energy cost. Due to the high peak-to-average load profile a high power density (9.56 kW/dm^3) and moderate efficiency (97.3 %) design results. The prototype is designed for 65 kW nominal power and provides stabilized 800 V DC for the required input voltage range of 290 V-530 V line-to-line RMS. Due to their competitive price, silicon IGBTs provide a lower total cost of ownership for the considered application than silicon carbide MOSFETs while also providing high reliability and availability. The Vienna rectifier as a unidirectional system exhibits a discontinuous conduction mode which is usually entered only at very low power levels. Due to the high power density of the boost inductors a relatively high current ripple occurs and discontinuous conduction occurs already at 20 % load. Since the duty cycle to voltage relationship is no longer linear in discontinuous conduction mode, high input current distortion is encountered with traditional closed-loop current controllers. Therefore, a special control scheme is presented that maintains sinusoidal input currents also with low load. The duty cycle values to obtain sinusoidal input currents can be directly expressed by analytic equations depending on the mains voltages, the DC-link voltage and the current set value. The control scheme is demonstrated on a 65 kW rectifier prototype.

In order to reach a high tube voltage control bandwidth a non-resonant high-voltage generator topology is proposed. The topology extends a single active bridge converter using two coupled transformers which are feeding two series connected rectifier stages at the output. Compared to commonly used resonant converter solutions the proposed topology mainly provides the advantage of zero voltage switching with constant switching frequency and high output voltage control bandwidth. Compared to a conventional single active bridge, which also shares these advantages, the proposed topology additionally provides lower inverter RMS currents and a higher maximum output current. The concept is demonstrated on a 60 kW DC-DC converter prototype. With two interleaved inverters using silicon IGBTs operating at 50 kHz output voltage rise-times and fall-times of $\approx 100\,\mu s$, i.e. five switching cycles, are achieved.

The conclusion of the thesis summarizes the main findings and contributions and provides an outlook on future research topics emanating mainly from the construction of the high-voltage transformer.

Kurzfassung

Seit der Entdeckung der Röntgenstrahlen 1895 wurde der Funktionsumfang medizinischer Röntgengeräte ständig weiterentwickelt. Unverändert blieb jedoch das grundlegenden Prinzip der Röntgenstrahlerzeugung. In einer Vakuumröhre werden Elektronen durch eine hohe Beschleunigungsspannung von einer Kathode in die Anode geschleudert. Beim Auftreffen auf die Anode wird Röntgenstrahlung in Form von Bremsstrahlung ausgesendet. Ein Grossteil der Energie bleibt jedoch in Form von Wärme ungenutzt. Der Hochspannungserzeuger muss daher nicht nur eine Spannung von bis zu 150 kV sondern auch eine Spitzenleistung von bis zu 100 kW bereitstellen. Die Kühlleistung der Anode in der Vakuumröhre ist jedoch stark begrenzt sodass die durchschnittlich aufzubringende Leistung in der Grössenordung von 1 kW liegt.

Die Entwicklung des Hochspannungserzeugers bestimmen zur Zeit drei wesentliche Trends. Einerseits weisen heute übliche passive Diodengleichrichter relativ hohe Oberschwingungsströme auf, erlauben einen Einsatz mit verschiedenen Netzspannungen nur mit Hilfe von Anpasstransformatoren und sind mit weichen Netzen nicht kompatibel. Um einen weltweiten Einsatz des Geräts ohne Anpassungen gewährleisten zu können ist der Einsatz eines aktiven Pulsgleichrichters von grossem Interesse. Eine weitere Schwäche aktueller Hochspannungserzeuger sind die relativ langen Anstiegs- und Abfallzeiten der Röhrenspannung von etwa 500 µs. Kürzere Anstiegs- und Abfallzeiten würden das bei Fluoroskopie heute übliche Steuergitter der Röhre überflüssig machen. Zudem könnten für *Dual Energy* Computer Tomographie Anwendungen eingesetzte, mit zwei verschiedenen Spannungen arbeitende Zweiröhrensysteme mit nur einer Röhre auskommen die schnell zwischen zwei Spannungsniveaus wechselt. Schlussendlich sollen die gewünschten Zusatzfunktionen kostengünstig umgesetzt werden um die Technologie allgemein zugänglich zu machen.

Besonders die Auslegung der induktiven Komponenten des Hochspannungsgenerators birgt grosses Einsparpotential. Durch die hohe Spitzen- aber niedrige Durchschnittsleistung können Baugrösse und Materialkosten stark reduziert werden ohne das thermische Limit zu überschreiten. Ein wichtiges Element für die Berechung induktiver Komponenten ist das Modell der Hochfrequenzwicklungsverluste. Basierend auf den exakten Gleichungen zur Bestimmung der Wirbelstromverluste in Wicklungen werden asymptotische Näherungen hergeleitet die sich durch einfache Anwendbarkeit auszeichnen. Es muss dabei zwischen zwei Näherungen für Nieder- und Hochfrequenzbereich unterschieden werden. Der maximale Fehler entsteht an der Bereichsgrenze welche etwa bei der Frequenz erreicht wird bei der die Abmessung eines Einzelleiters der doppelten Skintiefe entspricht. Es lässt sich jedoch zeigen, dass Leiterabmessungen der doppelten Skintiefe vermieden werden sollten, da der AC Widerstand der Wicklung sowohl für kleinere als auch für grössere Leiterabmessungen niedriger ist. Die asymptotische Näherung für den Niederfrequenzbereich erlaubt ausserdem die Herleitung der optimalen Betriebsfrequenz von Transformatoren welche indirekt proportional zum Produkt aus Einzelleiterabmessung und Wicklungsbreite ist.

Basierend auf dem Wicklungsverlustmodell wird ein Dreiphasenpulsgleichrichter für minimale Lebenszykluskosten, also der Summe von Betriebs- und Investitionskosten, optimiert. Aufgrund des hohen Verhältnisses von Spitzen- zu Durchschnittsleistung wird eine hohe Leistungsdichte von 9.56 kW/dm^3 bei einem Wirkungsgrad von 97.3 % erreicht. Der Prototyp weist eine Nennleistung von 65 kW auf und stellt eine konstante Ausgangsspannung von 800 V bei einem Eingangsspannungsbereich von 290 V - 530 V (Aussenleiterspannung effektiv) zur Verfügung. Für die gegebene Anwendung sind die Lebenszykluskosten bei Verwendung kostengünstiger Silizium IGBTs geringer als beim Einsatz von Siliziumkarbid MOSFETs. Ausserdem erweist sich die hohe Zuverlässigkeit und Verfügbarkeit als vorteilhaft. Unidirektionale Systeme wie der verwendete *Vienna Rectifier* weisen einen lückenden Betrieb auf welcher typisch nur bei sehr niedrigen Leistungen auftritt. Aufgrund der hohen Leistungsdichte ergibt sich jedoch ein relativ grosser Stromrippel in den Boost-Induktivitäten was dazu führt, dass der lückende Betrieb bis zu 20 % der Nennleistung vorherrscht. Da im lückenden Betrieb der Zusammenhang zwischen Tastverhältnis und Brückenzweigspannung nicht mehr linear ist, entsteht bei Verwendung eines herkömmlichen Stromreglers eine relativ hohe Eingangsstromverzerrung. Es wird gezeigt dass durch Verwendung eines speziellen Steuerverfahrens auch im lückenden Betrieb sinusförmige Eingangsströme erreichbar sind. Die nötigen Tastverhältnisse lassen sich direkt aus den Phasenspannungen, der Zwischenkreisspannung und der geforderten Leistung berechnen. Das Steuerverfahren wird an einem 65 kW Prototyp gezeigt.

Um die geforderte Dynamik der Ausgangsspanungsregelung zu erreichen wird eine neuartige nicht-resonante Schaltungsstruktur des Hochspannungserzeugers verwendet. Die Schaltung verbessert die Eigenschaften des *Single Active Bridge* Konverters mittels zweier Transformatoren mit gekoppelten Wicklungssystemen und in Serie geschalteten Ausgangsgleichrichtern. Im Vergleich zu häufig eingesetzten Resonanzkonvertern bietet die vorgeschlagene Struktur die Vorteile weichen Schaltens bei konstanter Schaltfrequenz sowie höherer Bandbreite der Ausgangsspannungsregelung. Im Vergleich zum ursprünglichen *Single Active Bridge* Konverter ist dabei der Effektivwert des Wechselrichterstroms geringer und die, bei gegebener Baugrösse der Transformatoren, übertragbare Leistung höher. Das Konzept wird an einem 60 kW Prototyp demonstriert. Mit zwei phasenversetzt mit jeweils 50 kHz betriebenen Wechselrichtern können Anstiegs- und Abfallzeiten der Ausgangsspannung im Berich von $\approx 100\,\mu s$, also der Dauer von fünf Schaltperioden, erreicht werden.

Abschliessend werden die wesentlichen Resultate und Beiträge der Arbeit zusammengefasst. Ausserdem werden weitere Forschungsthemen die sich vor allem aus der Konstruktion des Hochspannungstransformators ableiten diskutiert.

Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
AVG	Average
CCM	Continuous Conduction Mode
CCM1	Continuous Conduction Mode 1
CCM2	Continuous Conduction Mode 2
CCM3	Continuous Conduction Mode 3
CISABC	Coupled Interleaved Single Active Bridge Converter
CISPR	Comité International Spécial des Perturbations Radioélectriques
CM	Common Mode
CT	Computer Tomography
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCM1	Discontinuous Conduction Mode 1
DCM2	Discontinuous Conduction Mode 2
DCM3	Discontinuous Conduction Mode 3
DECT	Dual Energy CT
DS-ADC	Delta-Sigma ADC
DSP	Digital Signal Processor
DM	Differential Mode
DUT	Device Under Test
EMI	Electro Magnetic Interference
ESL	Equivalent Series Inductance
FFT	Fast Fourier Transform
FEM	Finite Element Method
FOM	Figure Of Merit
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GSE	Generalized Steinmetz Equation
HET	High Efficiency Transformer
HF	High-Frequency
HVT	High-Voltage Transformer
IC2OC	Inverter Current RMS to DC Output Current
IGBT	Insulated Gate Field Effect Transistor
iGSE	Improved Generalized Steinmetz Equation
IPOS	Input Parallel Output Series

ISABC	Interleaved Single Active Bridge Converter
ISOS	Input Series Output Series
LF	Low-Frequency
LISN	Line Impedance Stabilization Network
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPC	Neutral Point Clamped
OTC	Optimum Trajectory Control
PCB	Printed Circuit Board
PFC	Power Factor Correction
PK	Peak
PWM	Pulse Width Modulation
QP	Quasi Peak
RMS	Root Mean Square
SABC	Single Active Bridge Converter
SiC	Silicon Carbide
SRC	Series Resonant Converter
TCM	Triangular Current Mode
TCO	Total Cost of Ownership
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VR	Vienna Rectifier
ZCS	Zero Current Switching
ZMPC	Zero Midpoint Current
ZVS	Zero Voltage Switching
PES	Power Electronic Systems Laboratory

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1

Introduction

On the evening of Friday, November 8, 1895, Wilhelm Conrad Röntgen discovered *a new kind of rays.* At that time he was Director of the Physical Institute of the University of Würzburg and conducted experiments using a Hittorf-Crookes tube, an evacuated glass tube, connected to a *relatively large Ruhmkorff* high-voltage generator [1]. While applying voltage to the tube that he covered with black cardboard he noticed fluorescence of bariumtetracyanoplatinate coated paper located on a nearby table. He soon ruled out his initial assumption that the rays would be a different kind of light, similar to ultraviolet light because he observed that rays are passing through a wide varity of materials without being able to observe the phenomena of deflection or refraction. However, he noted that with increasing density and thickness of the material that the rays are passing through absorption increases. He published the results of his thorough examinations first in German on December 28, 1895, in *Sitzungsberichte der Physikalisch-Medizinischen Gesellschaft in Würzburg* [2], English translations in Nature [3] and Science [4] followed early in 1896. In his report he coined the term X-rays, after the unknown variable x. The discovery soon lead to widespread use, not only in medicine but also for entertainment purposes. However, it took years until the actual physical nature of X-rays as high energy photon beams was theoretically described.

1.1 X-Ray Generators

X-rays used for imaging purpose originate mostly as Bremsstrahlung, which is emitted when an electron is deflected and slowed down by the positively charged core of an atom of the anode.

1.1.1 X-Ray Tube

The electron is accelerated within an evacuated tube using a high-voltage applied between a negative cathode and a positive anode. The accelerated electron hits the target, which is part of the anode and usually made of tungsten for its high melting point. The energy spectrum of the photon beam emitted from the target as Bremsstrahlung is continuous since only a few electrons still have their initial energy when being slowed down by an atom's core. Most of the electrons already lost part of their energy due to other Coulomb interactions within the anode. The maximum energy of a photon is thus limited to the initial energy eU the electron has when reaching the target. Increasing the tube voltage U, therefore, increases the mean energy of the photon beam. According to the Beer-Lambert law X-rays entering into matter are exponentially attenuated with increasing depth [5]. The attenuation decreases with increasing photon energy and decreasing material density. Therefore, in order to obtain a high contrast X-ray image the tube voltage needs to be selected depending on the volume and density of the object.

Röntgen's experiment and early X-ray tubes employed cold cathodes where the free electrons for acceleration are generated from discharge ionization of residual gas atoms in the tube. In 1913 William Coolidge invented a tube using a glowing tungsten filament as cathode [6,7]. The thermionic electron emission at the surface of the filament allows higher tube currents and offers the possibility to control the tube current by adjusting the filament temperature and, since the photon generation rate is proportional to the tube current, the intensity of the emitted X-ray beam. This improvement allowed to reduce the exposure time from several minutes or even hours to seconds or less.

The principle of modern X-ray sources is still the same. A tungsten filament, which is part of the cathode and therefore on negative potential, is supplied with an adjustable heating current. The electrons emitted from the filament are accelerated with the tube voltage towards the anode. A large share of the electrons, equivalent to approximately 40 % of the energy, is scattered back from the target. Most of the electrons entering the target transfer their energy to phonons, causing the anode to heat up. Only $\approx 1\,\%$ of the energy is actually emitted as

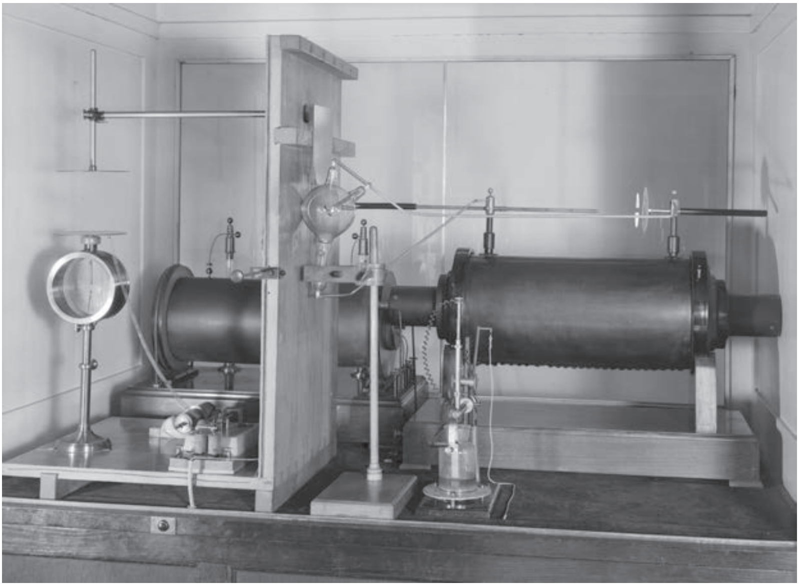


Fig. 1.1: X-ray tube (center) and high-voltage generator (right) used by Röntgen to investigate ionization of air by X-rays between two electrodes (left). (Photo: Deutsches Museum)

Bremsstrahlung which can be used for diagnostic and also for therapy purposes [5]. Since the vacuum tube only provides limited heat transfer to the ambient, the average power that can be supplied to the tube is given by the maximum temperature of the anode and its thermal resistance to the ambient and it typically amounts to less than 1 kW. The peak-power however is only limited by the internal thermal resistance of the anode which is typically a composite of tungsten and copper or molybdenum [8]. Therefore, the peak-power can be considerably higher reaching values up to 100 kW. The duration of such a full power pulse is limited by the total amount of energy which can be stored in the thermal capacitance of the anode at its maximum temperature, thus usually full-load pulses are limited to less than 10 s.

1.1.2 High-Voltage Supply

Röntgen's *Ruhmkorff* shown in Fig. 1.1 is a high-voltage generator similar to a fly back converter. An accumulator provided current to the primary coil wound around an iron core, lacking the back iron. A switch interrupts the primary current as soon as it reaches a certain level, igniting an arc. The high arc voltage drives the current rapidly back to zero while a secondary winding provides a high-voltage to the tube [1]. Besides electro mechanical switches also versions using mercury and electrolytic (Wehnelt) contacts were in use [9]. Due to the high duty-cycle, i.e. the relative time the switch is closed, the negative voltage that is applied to the tube is much lower than the positive voltage. Therefore, no rectifier is necessary and X-rays are primarily emitted at one electrode of the tube only.

With the upcoming electrification and AC grids transformers started to replace these early induction coils. The at that time commonly used Coolidge tube exhibits self-rectifying behaviour. It could therefore be directly supplied with AC and acted as half-wave rectifier. However, the self-rectifying property of the tube is lost as soon as the anode heats up to a point where thermionic emission starts and electrons are conducted in both ways. Two-way conduction must be avoided since two X-ray sources would lead to blurred images and destruction of the cathode due to overheating. Therefore, self-rectifying tubes are only found in dental and low power portable units. Early high power X-ray systems employed contacts rotated by a synchronous machine and later rectifier tubes to provide full-wave high-voltage rectification.

Nowadays X-ray high-voltage supplies mainly use full-wave rectification using series connected diode strings, although there are still a few dental systems employing self-rectification. The high-voltage transformer is usually supplied by an Insulated Gate Field Effect Transistor (IGBT) based inverter switching in the tens of Kilohertz range in order to reduce its size and weight [6]. The high switching frequency also allows to reduce the size of the high-voltage DC-link capacitors. Therefore, Cockcroft-Walton voltage multipliers, which employ a large number of capacitors, are a cost effective solution because they reduce the voltage stress on the transformer's secondary winding, allowing a small and simple construction. However, due to their slow dynamic response their application is limited [10].

1.2 Applications

In medicine, apart from radiation therapy which typically employs linear accelerators, X-rays are mainly used for diagnostic purposes. The classic two-dimensional whole body multi-purpose radiography devices are complemented with specialised equipment for diagnosis of breast cancer (mammography), dental X-ray systems and portable units for use during surgery. Additionally to bones and cavities, such as the lung, also blood vessels can be visualised (angiography) by injecting a contrast medium [11].

Other than single-shot radiography fluoroscopy provides a live X-ray video. The term comes from the fluorescent screens used in early days, nowadays digital detectors capture the video. Fluoroscopy is used to view the functioning of inner organs in motion and also to provide a live view to the surgeon during operations. Due to the long exposure time during fluoroscopy the patient dose is relatively high ranging between 1 mSv to 5 mSv, which is the equivalent of up to two years of natural background radiation exposure (2.4 mSv/y) [12]. Compared to that the dose from a single extremity or intra-oral X-ray image equals the natural radiation exposure of merely one day. In order to limit the patient dose the beam is typically pulsed at an adjustable rate of usually around ten pulses per second (pulsed fluoroscopy) [13].

Following the work of Godfrey Hounsfield the first Computer Tomography (CT) was carried out in 1971 [14]. Since then X-rays can be used to obtain three-dimensional images as well. In principle a CT consists of an X-ray tube with a digital detector which is rotating around the patient to capture one slice, while the patient is moved laterally through the machine to obtain slices of all body parts of interest [15]. For each slice images are taken at evenly spaced angular intervals. The one-dimensional Fast Fourier Transform (FFT) of each projection at a certain angle equals one row through the center of the two-dimensional Fourier transform of the image of the slice at the same angle. The density, or more accurately attenuation coefficient image of the slice, is finally reconstructed by carrying out the inverse FFT [16]. Due to the high number of X-ray images taken during a CT scan, the effective dose to the patient ranges from 2 mSv to 12 mSv which is equivalent to two to five years of natural background ration exposure [12].

1.3 Recent Developments

One recent advancement in X-ray technology is the use of two energy levels (dual energy). The attenuation of the X-ray beam for a specific element shows a spike at the energy corresponding to the binding energy of the K-shell [17]. Since the K-shell energy depends on the atomic number, dual energy scans provide better contrast. Dual energy images are already widely used for bone densitometry but also Dual Energy CT (DECT) is employed more often due to the better soft tissue contrast. There are still three competing DECT technologies [18]. Dual source DECT uses two tubes and two detectors working at different voltages, typically 80 kV and 140 kV. Single source DECTs use only one tube which is either switching between two voltage levels at approximately 1 kHz (rapid kVp switching) or which uses two detectors sensitive to different parts of the spectrum (dual detector layer).

Another development aims at the reduction of the patient dose by reducing the rise times and fall times of the tube voltage caused by the charging and discharging of the high-voltage capacitors. This is of particular concern with pulsed fluoroscopy which exhibits relatively high dose per treatment and high pulse frequency [13]. Although the relative duration of the rising and falling voltage edges is short, during that time low energy X-rays are emitted which is, compared with higher energy X-rays, mostly absorbed by the patient and therefore contributes a significant share of the dose. Most nowadays systems use an additional anode control grid to rapidly pulse the beam since the high-voltage rise-times and fall-times are too long. By increasing the bandwidth of the high-voltage generator the control grid on the tube could be eliminated.

1.4 Objective and Contributions

The objective of this work is to optimize an X-ray power supply providing 60 kW to the tube at up to 150 kV DC voltage with rise-times and fall-times of less than 500 µs from a three-phase mains with line-to-line RMS input voltage range of 290 V to 530 V. The specified voltage range results from the requirement to deal with 400 V and 480 V mains voltages with 10 % over- and 20 % under-voltage tolerance. Nowadays X-ray power supplies are using six-pulse passive diode rectifiers supplying a DC voltage which is depending on the mains voltage. high-voltage generators connected to passive rectifiers therefore either have to be able to cope with a wide input voltage range, while also providing a wide output voltage range of typically 50 kV to 150 kV to the tube, or are equipped with a mains frequency transformers stepping down the 480 V mains to 400 V. Furthermore, six-pulse diode rectifiers exhibit considerable harmonic current emissions which may require additional low-frequency harmonic filtering depending on the utility grid regulations [19]. This work presents an active mains interface which provides a stable DC-link voltage to the high-voltage generator and sinusoidal currents to the mains.

1.4.1 Three-Phase PFC Rectifier

While highly efficient active three-phase Power Factor Correction (PFC) rectifiers are common for Uninterruptible Power Supply (UPS) and telecommunication supplies, a design optimized for use with X-ray systems faces different challenges. Because of the high peak-to-average load ratio and the low amount of full-load operating hours, one can take advantage of the relatively low average power. The primary objective is to reach lowest material cost instead of highest efficiency, while maintaining high reliability despite the thermal cycling of the components [20]. Optimizing the trade-off between material cost and loss energy cost during operation, i.e. minimizing the total cost of ownership, results in relatively small boost inductors of the rectifier, exhibiting high current ripple. The Vienna rectifier, a unidirectional three-phase three-level rectifier, provides stable DC-link voltage and sinusoidal input currents and compared to the two-level six-switch rectifier [21] the power semiconductors only need to block half of the DC-link voltage which can be as low as the line-to-line peak voltage. Therefore, low switching loss 650 V IGBTs in combination with low reverse recovery charge 650 V free-wheeling diodes can be employed which match the low-cost, high reliability design target. However, due to its unidirectional structure the Vienna rectifier exhibits a Discontinuous Conduction Mode (DCM) which occurs when the current ripple is in the range of the amplitude of the input current fundamental. For light load, which would be a common use case for fluoroscopy, the Vienna rectifier mainly operates in DCM. However, due to the different duty-cycle to voltage relationship conventional Continuous Conduction Mode (CCM) current control schemes in DCM result in distorted input currents. The main scientific contribution, resulting from the design of the rectifier, is the derivation of a control scheme that allows to maintain sinusoidal currents in DCM which is presented in Chapter 3.

1.4.2 High-Voltage Generator

On the output side the primary challenge, apart from the high-voltage and power demand, is to reach low-voltage rise-times and fall-times. Most nowadays high-voltage generators for X-ray systems use a resonant converter, allowing to integrate the high stray inductance and winding capacitance of the high-voltage transformer into the resonant tank and achieve either zero current or zero voltage switching on the inverter. However, the two main drawbacks of resonant converters are the variable switching frequency which is required to maintain zero voltage switching for all operating conditions and the slow dynamic response of the resonant tank which slows down the output voltage control. Therefore, a non-resonant interleaved approach is proposed which features zero voltage switching with constant switching frequency and fast output voltage control employing two low winding capacitance multi-rectifier high-voltage transformers. The main contribution to the high-voltage generator is the invention of an interleaved circuit which employs two coupled transformers, allowing to reduce the inverter RMS current compared to an uncoupled variant which is presented in Chapter 4.

1.5 List of Publications

Different parts of the research findings presented in this thesis have already been published or will be published in international scientific journals, conference proceedings and tutorials, or have been protected by multi-national patents. The publications and patents developed in the course of this thesis are listed below.

Journal Papers

- M. Leibl, G. Ortiz, and J. W. Kolar, ”Design and Experimental Analysis of a Medium Frequency Transformer for Solid-State Transformer Applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 110–123, March 2017. DOI: 10.1109/JESTPE.2016.2623679

- M. Leibl, J. W. Kolar, and J. Deuringer, ”Sinusoidal Input Current Discontinuous Conduction Mode Control of the VIENNA Rectifier,” *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8800–8812, November 2017. DOI: 10.1109/TPEL.2016.2641502

- M. Leibl, O. Knecht, and J. W. Kolar, ”Inductive Power Transfer Efficiency Limit of a Flat Half-Filled Disc Coil Pair,” accepted for publication in *IEEE Transactions on Power Electronics*, 2018. DOI: 10.1109/TPEL.2018.2797366

- M. Leibl, J. W. Kolar, and J. Deuringer, ”High Bandwidth Non-Resonant High Voltage Generator for X-Ray Systems,” under review at *CPSS Transactions on Power Electronics and Applications*, 2018.

Conference Papers

- M. Leibl, and J. W. Kolar, ”Comparative Analysis of Inductor Concepts for High Peak Load Low Duty Cycle Operation,” in *Proceedings of the International Power Electronics Conference (IPEC - ECCE Asia)*, Hiroshima, Japan, May 2014, pp. 899–906. DOI: 10.1109/IPEC.2014.6869694

- M. Leibl, M. Darani, J. Deuringer, and J. W. Kolar, ”New Boundary Mode Sinusoidal Input Current Control of the VIENNA Rectifier,” in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Pittsburgh, PA, USA, September 2015, pp. 1240–1247. DOI: 10.1109/ECCE.2014.6953543

- M. Leibl, J. Deuringer, and J. W. Kolar, ”New Current Control Scheme for the Vienna Rectifier in Discontinuous Conduction Mode,” in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Pittsburgh, PA, USA, September 2014, pp. 201–209. DOI: 10.1109/ECCE.2015.7309689

Patents

- M. Leibl, ”Verfahren zur Steuerung eines Mehrpunkt-Gleichrichters,” German Patent Application No. DE102014214276A1, Filed Jul. 22, 2014, published Jan. 28, 2016.

- M. Leibl, ”Hochspannungsgenerator für ein Röntgengerät,” German Patent Application No. DE102016215765, filed Aug. 23, 2016.

Further Scientific Contributions

- G. Ortiz, M. Leibl, J. W. Kolar, and O. Apeldoorn ”Medium Frequency Transformers for Solid-State-Transformer Applications - Design and Experimental Verification,” in *Proceedings of the 10th IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Kitakyushu, Japan, April 2013, pp. 1285–1290. DOI: 10.1109/PEDS.2013.6527217
- G. Ortiz, M. Leibl, J. Huber, and J. W. Kolar, ”Design and Experimental Testing of a Resonant DC-DC Converter for Solid-State Transformers,” in *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7534–7542, October 2017. DOI: 10.1109/TPEL.-2016.2637827
- L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar, and T. Soeiro ”99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems” in *Proceedings of the 32nd Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, March 2017, pp. 2173–2178. DOI: 10.1109/APEC.2017.7931000
- J. Azurza Anderson, L. Schrittwieser, M. Leibl, and J. W. Kolar, ”Multi-Level Topology Evaluation for Ultra-Efficient Three-Phase Inverters” in *Proceedings of the IEEE International Telecommunications Energy Conference (INTELEC)*, Broadbeach, QLD, Australia, October 2017, pp. 456–463. DOI: 10.1109/INTLEC.2017.-8214178

2

Optimized Design of Inductive Components

Optimization of transformers and inductors, referred to as inductive components, can be time consuming due to the multitude of available parameters. First, the designer can choose between different core topologies, such as shell-type, core-type, toroidal and pot cores. Second, the geometric dimensions have to be specified which alone amount to four variables: width and height of core area and winding area. In case of an inductor also the air gap needs to be determined. Third, the structure of the winding needs to be specified as well by setting the number of turns, the conductor profile (rectangular or round), the type of conductor (solid or stranded) and if stranded the number of strands. Finally, the core material needs to be selected from different kinds of ferrite and iron powder materials, amorphous and nanocrystalline tapes and laminated silicon steel. Together all this parameters form the so-called design space. In practice this design space is heavily reduced by the limited availability of cores and conductors.

The core component of the optimization process is the model which maps the design space to the so-called performance space. The losses of an inductive component is the dimension of the performance space which is always present. Additionally a binary dimension is often used which indicates if the maximum values of winding and core temperature, core flux density and isolation electric field are within the limits given by the material. Volume, weight and material cost are also common dimensions of the performance space.

In order to find the best design, a cost function has to be applied to the performance space which assigns a price to each member of the design space. A simple example of a cost function evaluates, for a given number of operating hours and energy cost, the sum of the energy cost during the component life and its initial material cost. This is known as Total Cost of Ownership (TCO) optimization. Depending on the application other dimensions can be taken into account as well. In case of inductive components for aircraft for example one may want to add a price for the weight of the device. Finally, the design with the lowest cost can be considered optimal with respect to the given cost function.

Prior to applying the cost function, the performance space can be reduced to the Pareto front which always includes the best design. The Pareto front consists of all elements of the performance space which are *better* in at least one dimension than all the other elements of the performance space. Implicitly the relation *better* assumes a part of the cost function which is usually possible. For example, lower values of loss, weight, volume and material cost are always better than higher ones. Often the Pareto front is used to illustrate trade-offs and when a cost function cannot be specified due to the lack of reliable prices.

Applying the cost function only to the Pareto front reduces the computational effort for evaluating the cost function. However, the additional effort for finding the Pareto front usually outweighs this benefit. Instead, in order to reduce the computational effort the design space can be confined to include only *optimized designs* using analytically found optimality criteria, such as the optimum number of turns of a transformer.

2.1 High-Frequency Winding Losses

One essential part of the loss model of an inductive component is the winding loss model which needs to take into account the eddy current losses within the winding. Often the eddy current loss in a single conductor of the winding is separated into two parts, the skin effect losses and the proximity effect losses. While the skin effect describes the eddy current loss due to the magnetic field of the current in the conductor itself, the proximity effect describes the extra losses due to eddy currents induced by an external magnetic field, i.e. the magnetic field of all other conductors constituting the winding. For the two common cases of windings consisting of foil and round conductors analytic solutions for the eddy current losses due to skin and proximity effect are known. This Section provides an overview of the existing analytic solu-

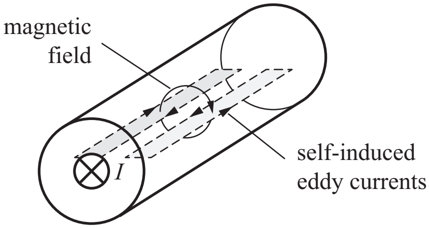


Fig. 2.1: Skin effect in a round conductor.

tions for the calculation of skin and proximity effect and a comparison to Finite Element Method (FEM) simulations. Furthermore, simplified approximations of the exact solutions for conductor dimensions much smaller or much larger than skin depth are derived. Finally, the loss expressions for foil and round conductors are used to derive the losses in typical winding arrangements and the results are again compared to FEM simulations.

2.1.1 Skin Effect

A current flowing in a conductor also creates a magnetic field within the conductor. If the current is varying over time (AC) this magnetic field induces a voltage that causes eddy currents inside the conductor itself. The direction of these eddy currents is such that they counteract the current density in the interior of the conductor and add to the current density at the surface of the conductor as shown in Fig. 2.1. Therefore, High-Frequency (HF) currents are concentrated mainly within a layer beneath the conductor surface called the skin depth. In the following the skin effect for a half-space boundary and for foil conductors is derived and the solution for round conductors is reviewed. It is shown that the simple result of the half-space boundary can be used to approximate the skin effect for the cases of foil- and round conductor as well.

Skin Effect at Half-Space Boundary

It is assumed that a current per unit length (in y-direction) I' flows distributed within a conductor filling the half-space $x > 0$. The current is oriented in z-direction. The half-space $x < 0$ is electrically isolating. The situation is shown in Fig. 2.2a. If the current is sinusoidal with am-

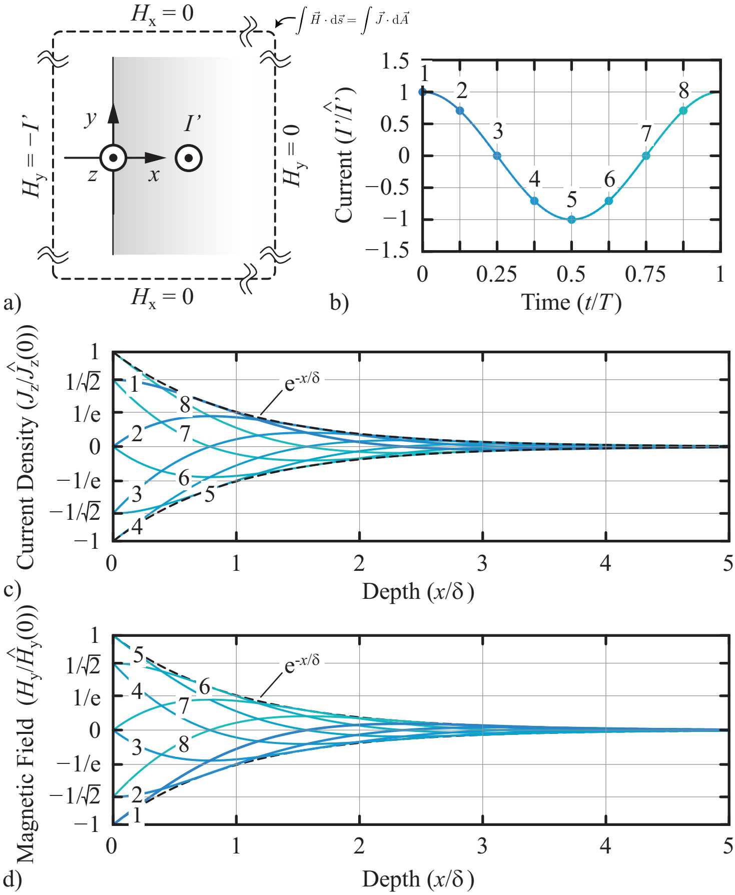


Fig. 2.2: One-dimensional skin effect at the boundary (yz plane) between an isolating half-space and a conductive half-space.

plitude $\hat{I}'$ and frequency $\omega = 2\pi f$, it is distributed such that Ampère's law

$$\vec{\nabla} \times \vec{H} = \vec{J} \tag{2.1}$$

and Faraday's law

$$\vec{\nabla} \times \vec{E} = -\frac{\mathrm{d}\vec{B}}{\mathrm{dt}} \tag{2.2}$$

are fulfilled. Because of the infinite extension in y- and z-direction there are only current density components in z-direction and magnetic field components in y-direction. Furthermore, since the current is sinusoidal complex analysis can be used. Therefore, (2.1) and (2.2) simplify to

$$\frac{\mathrm{d}\underline{\hat{H}}_y}{\mathrm{dx}} = \underline{\hat{J}}_z \tag{2.3}$$

and

$$\frac{\mathrm{d}\underline{\hat{E}}_z}{\mathrm{dx}} = j\omega\underline{\hat{B}}_y. \tag{2.4}$$

Using the material relationships $E = \frac{J}{\sigma}$ and $B = \mu H$ (2.3) and (2.4) can be combined to obtain the homogeneous second order differential equation for the magnetic field inside the conductor

$$\frac{\mathrm{d}^2\underline{\hat{H}}_y}{\mathrm{dx}^2} = j\omega\mu\sigma\underline{\hat{H}}_y. \tag{2.5}$$

The fundamental solution of this kind of differential equation is any constant multiple of $\mathrm{e}^{\lambda x}$, which leads to the characteristic equation $\lambda^2 = j\omega\mu\sigma$ and it's solutions

$$\lambda = \pm\sqrt{\omega\mu\sigma} = \pm\frac{1+j}{\delta} \tag{2.6}$$

with the skin depth

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu}}. \tag{2.7}$$

Using both possible values of λ leads to the general solution for the magnetic field inside the conductor

$$\underline{\hat{H}}_y = C_1\mathrm{e}^{\frac{1+j}{\delta}x} + C_2\mathrm{e}^{-\frac{1+j}{\delta}x} \tag{2.8}$$

with the constants C_1 and C_2 still to be determined by boundary conditions. For the half-space boundary it is assumed that deep inside the conductor, i.e. for $x \to \infty$, the magnetic field and the current density approach zero, thus

$$\underline{\hat{H}}_y(\infty) \to 0 \Rightarrow C_1 = 0. \tag{2.9}$$

Applying Ampère's law in the integral form on a loop as shown in Fig. 2.2a shows that the magnetic field at the conductor surface equals the total current flow per unit length in y-direction but with opposite sign, therefore

$$\underline{\hat{H}}_y(0) = -\underline{\hat{I}}' \Rightarrow C_2 = -\underline{\hat{I}}. \tag{2.10}$$

The magnetic field inside the conductive half-space is finally found to be

$$\underline{\hat{H}}_y(x) = -\underline{\hat{I}}' \mathrm{e}^{-\frac{1+j}{\delta}x}. \tag{2.11}$$

Using (2.3), the current density can be derived from the magnetic field as

$$\underline{\hat{J}}_z(x) = \underline{\hat{I}}' \frac{1+j}{\delta} \mathrm{e}^{-\frac{1+j}{\delta}x}. \tag{2.12}$$

The solutions show, that current density and magnetic field are attenuated in amplitude by a factor e and phase-shifted by −90° per skin-depth δ. For different times during the current period marked in Fig. 2.2b the instantaneous values of current density and magnetic field are shown in Fig. 2.2c and d. The instantaneous ohmic loss per unit area of the yz-plane inside the conductive half-space is calculated as

$$p'' = \vec{S}(0) \cdot \vec{e}_x = -E_z(0)H_y(0) \tag{2.13}$$

using the Poynting vector $\vec{S} = \vec{E} \times \vec{H}$. Therefore, the time average ohmic loss per unit area is

$$P'' = \frac{1}{2}\Re\{-\underline{\hat{E}}_z(0)\underline{\hat{H}}_y(0)^*\} = \frac{1}{2}\frac{\hat{I}'^2}{\sigma\delta}. \tag{2.14}$$

According to (2.14) in terms of losses it is equivalent to assume that instead of the actual current density distribution shown in Fig. 2.2c the current I' flows uniformly distributed in a layer of thickness δ. This result, although only exact for the case of a conductor filling one half-space, can be used with good accuracy also in situations of practical interest as will be shown in the following.

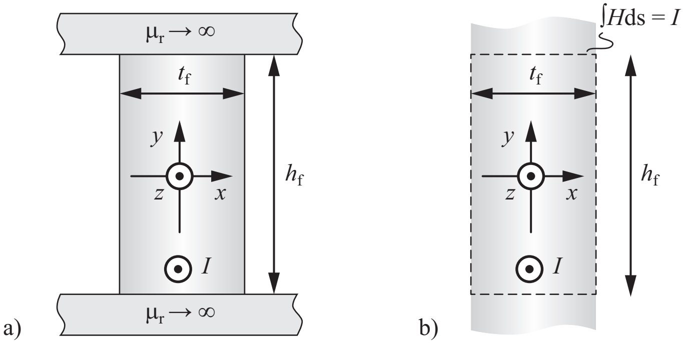


Fig. 2.3: Dimensions and coordinate systems for derivation of skin effect in a piece of foil terminated by two highly permeable parts (a) and equivalent piece of a foil conductor, extending infinitely in y- and z-direction (b).

Skin Effect in Foil Conductors

In order to obtain a simple closed form expression, the skin effect for foil conductors is described for the special case of the foil conductor being terminated by two infinitely permeable pieces as shown in Fig. 2.3a. This situation is equivalent to the one of a (finite) piece of a foil conductor, infinitely extending in y-direction (Fig. 2.3b) and can therefore be described one-dimensionally, with the magnetic field oriented in y- and the current density in z-direction. These are exactly the assumptions that resulted in (2.8), which will be used as a starting point for the derivation of the skin effect loss in a foil conductor. In order to determine the constants C_1 and C_2, Ampère's law is applied at the integration path indicated in Fig. 2.3b. With the origin of the coordinate system placed at the center of the conductor, the boundary conditions for the magnetic field,

$$\underline{\hat{H}}_y\left(\frac{t_\mathrm{f}}{2}\right) = \frac{\underline{\hat{I}}}{2h_\mathrm{f}} \quad \text{and} \quad \underline{\hat{H}}_y\left(-\frac{t_\mathrm{f}}{2}\right) = -\frac{\underline{\hat{I}}}{2h_\mathrm{f}}, \tag{2.15}$$

are obtained. Because of the odd symmetry $\underline{\hat{H}}_y(\frac{t_\mathrm{f}}{2}) = -\underline{\hat{H}}_y(-\frac{t_\mathrm{f}}{2})$, $C_2 = -C_1$, and thus

$$C_1 = \frac{\underline{\hat{I}}}{2h_\mathrm{f}} \frac{1}{\mathrm{e}^{\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}} - \mathrm{e}^{-\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}}} \tag{2.16}$$

is valid. Therefore, the magnetic field within the foil conductor is

$$\underline{\hat{H}}_y(x) = \frac{\underline{\hat{I}}}{2h_\mathrm{f}} \frac{\mathrm{e}^{\frac{1+j}{\delta}x} - \mathrm{e}^{-\frac{1+j}{\delta}x}}{\mathrm{e}^{\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}} - \mathrm{e}^{-\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}}}. \tag{2.17}$$

From that the current density is derived using (2.3) as

$$\underline{\hat{J}}_z(x) = \frac{\underline{\hat{I}}}{2h_\mathrm{f}} \frac{1+j}{\delta} \frac{\mathrm{e}^{\frac{1+j}{\delta}x} + \mathrm{e}^{-\frac{1+j}{\delta}x}}{\mathrm{e}^{\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}} - \mathrm{e}^{-\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}}}. \tag{2.18}$$

The time average ohmic loss in a piece of unit area of the foil conductor is obtained by evaluating the Poynting vector at both conductor surfaces. Due to symmetry it is sufficient to multiply the result obtained for one surface by two. Therefore, the average ohmic loss within a piece of unit area of a foil conductor due to skin effect is

$$P'' = \Re\left\{\underline{\hat{E}}_z\left(\frac{t_\mathrm{f}}{2}\right)\underline{\hat{H}}_y^*\left(\frac{t_\mathrm{f}}{2}\right)\right\} = \frac{\hat{I}^2}{8\sigma\delta h_\mathrm{f}^2} \frac{\sinh(\frac{t_\mathrm{f}}{\delta}) + \sin(\frac{t_\mathrm{f}}{\delta})}{\cosh(\frac{t_\mathrm{f}}{\delta}) - \cos(\frac{t_\mathrm{f}}{\delta})}. \tag{2.19}$$

A common expression for the skin effect losses of foil windings uses a factor F_f which expresses the ratio of AC to DC resistance due to the skin effect as function of the ratio of foil thickness to skin depth. Thus, the skin effect losses of a foil conductor per unit length (z-direction) are

$$P'_\mathrm{f,skin} = R'_\mathrm{dc} F_\mathrm{f}(\nu) \hat{I}^2 \tag{2.20}$$

with

$$R'_\mathrm{dc} = \frac{1}{\sigma h_\mathrm{f} t_\mathrm{f}} \tag{2.21}$$

and

$$F_\mathrm{f} = \frac{\nu}{4} \frac{\sinh(\nu) + \sin(\nu)}{\cosh(\nu) - \cos(\nu)}, \quad \nu = \frac{t_\mathrm{f}}{\delta}. \tag{2.22}$$

The skin effect factor for foil conductors F_f is compared to a FEM simulation in Fig. 2.4. As expected the simulated values agree with the analytic solution. The logarithmic scale reveals that the factor F_f could also be approximated using two asymptotes. For the LF range, where the foil is thinner than twice the skin depth ($\nu < 2$), the skin effect is negligible and the factor F_f approaches the value $\frac{1}{2}$ since (2.20) uses the amplitude not the RMS value of the current. For the HF range ($\nu > 2$) where the foil is thicker than twice the skin depth it can be assumed that the current is concentrated only within a layer of the skin depth beneath

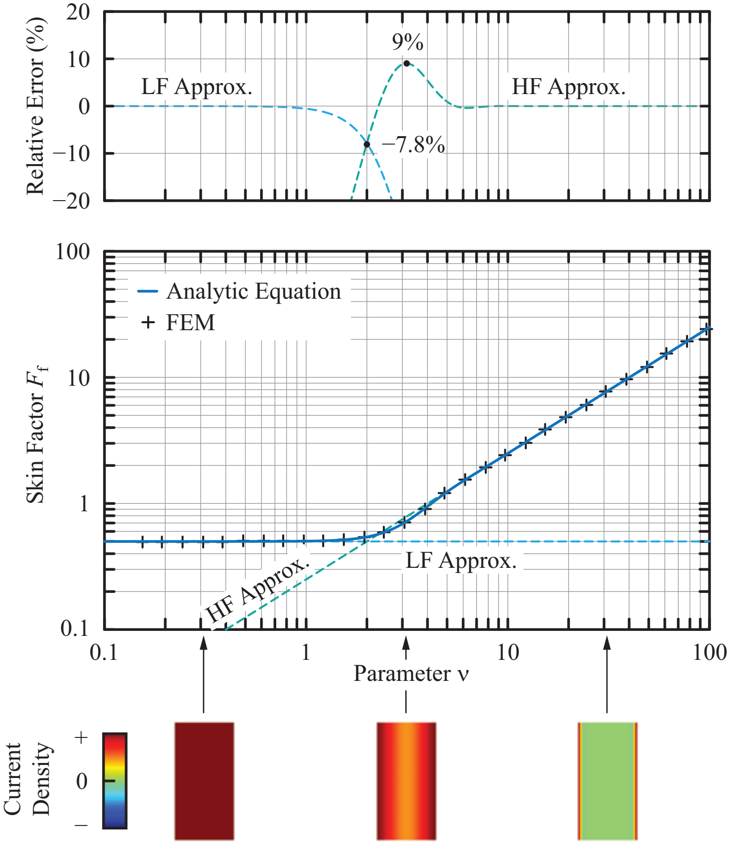


Fig. 2.4: Comparison of analytic solution, FEM simulation and LF and HF approximations of the skin effect factor F_f of foil conductors.

the two surfaces of the foil. Therefore, the ratio of AC resistance to DC resistance equals approximately the ratio of foil thickness to twice the skin depth. Therefore, instead of the exact expression, the asymptotic approximation

$$F_\mathrm{f} \approx \begin{cases} \frac{1}{2}, & \text{if } t_\mathrm{f} < 2\delta \\ \frac{t_\mathrm{f}}{4\delta}, & \text{if } t_\mathrm{f} \geq 2\delta \end{cases} \tag{2.23}$$

can be used with a maximum error of ±9 %.

Skin Effect in Round Conductors

Due to the rotational symmetry, the AC current density distribution in a cylindrical conductor with circular cross section, referred to as round conductor in the following, can also be expressed as a one-dimensional problem. However, the solution to the differential equation is a modified Bessel function of the first kind with index zero, making the derivation of the power loss due to skin depth more complicated than that for a foil conductor. For the sake of brevity only the solution is presented here, a detailed recently published derivation of the solution can be found in [22], although according to that the first exact solution of the skin effect in a round conductor goes back to Heaviside [23]. Using a factor F_r [24] similar as with foil conductors the power loss per unit length due to skin effect in a round conductor of diameter d_r can be expressed as

$$P'_\mathrm{r,skin} = R'_\mathrm{dc} F_\mathrm{r}(\xi) \hat{I}^2 \tag{2.24}$$

with

$$R'_\mathrm{dc} = \frac{4}{\sigma d_\mathrm{r}^2 \pi}, \quad \xi = \frac{d_\mathrm{r}}{\sqrt{2}\delta} \tag{2.25}$$

and

$$\begin{aligned} F_\mathrm{r} = \frac{\xi}{4\sqrt{2}} \Bigg(& \frac{\mathrm{ber}_0(\xi)\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \\ & - \frac{\mathrm{bei}_0(\xi)\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \Bigg) . \end{aligned} \tag{2.26}$$

Fig. 2.5 shows the factor F_r with the corresponding data points obtained from a FEM simulation verifying the solution. For conductor dimensions less than 4δ, the skin effect is almost negligible. For conductor diameters larger than 4δ it is possible to approximate F_r by assuming the current only flows within a layer of thickness δ beneath

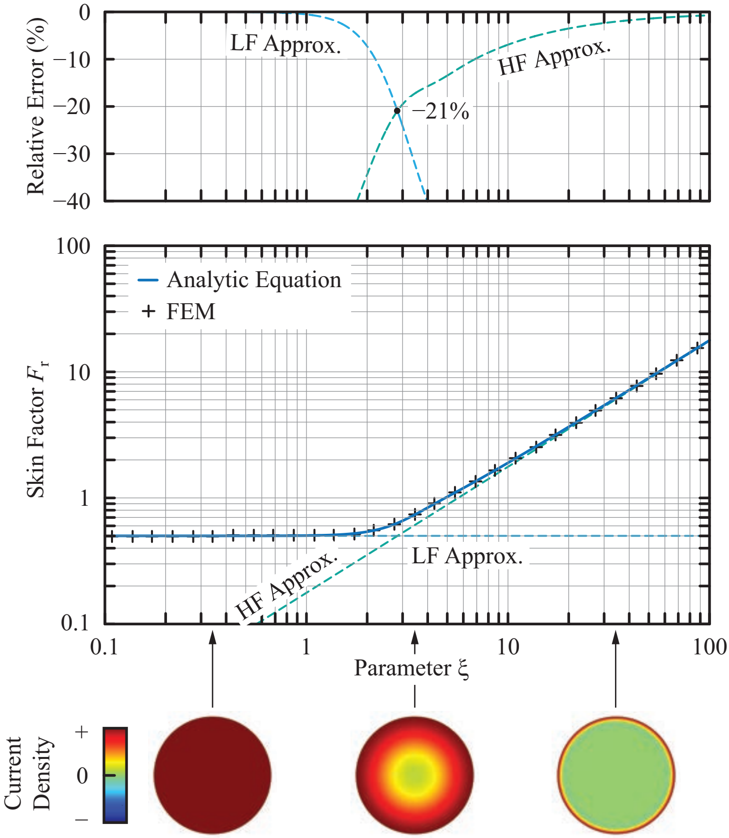


Fig. 2.5: Comparison of analytic solution, FEM simulation and LF and HF approximations of the skin effect factor F_r of round conductors.

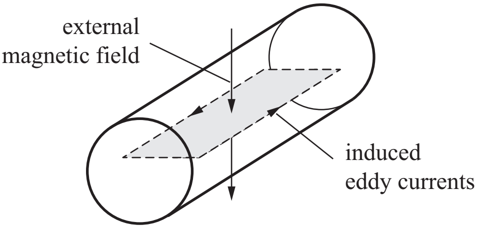


Fig. 2.6: Proximity effect in a round conductor.

the surface. If the cross section of the conductor is related to the cross section of the skin depth tube, which is approximately $\pi d_\mathrm{r}\delta$, the approximate value of F_r for conductor dimensions larger than 4δ is obtained. Therefore,

$$F_\mathrm{r} \approx \begin{cases} \frac{1}{2}, & \text{if } d_\mathrm{r} < 4\delta \\ \frac{d_\mathrm{r}}{8\delta}, & \text{if } d_\mathrm{r} \geq 4\delta \end{cases} \tag{2.27}$$

with a maximum error of $-21\,\%$ at $d_\mathrm{r} = 4\delta$.

2.1.2 Proximity Effect

According to Faraday's law time varying (AC) magnetic fields induce a voltage within a closed loop. In conductive parts this induced voltage leads to eddy currents counteracting the external magnetic field as shown for the case of a round conductor in Fig. 2.6. Often the external field is caused by currents in conductors in the proximity, therefore this effect is called proximity effect. In windings of inductive components the proximity losses usually outweigh the losses caused by the skin effect.

Proximity Effect in Foil Conductors

In order to obtain a simple one-dimensional solution, it is assumed that a piece of foil is either terminated by two cores or part of an infinitely extending sheet as shown in Fig. 2.7a. Assuming that the considered piece of foil is exhibited to an external magnetic field

$$\vec{H} = H\vec{e}_y \tag{2.28}$$

the current density due to the infinite extension in z direction only consists of a z component. Therefore, the solution for the magnetic

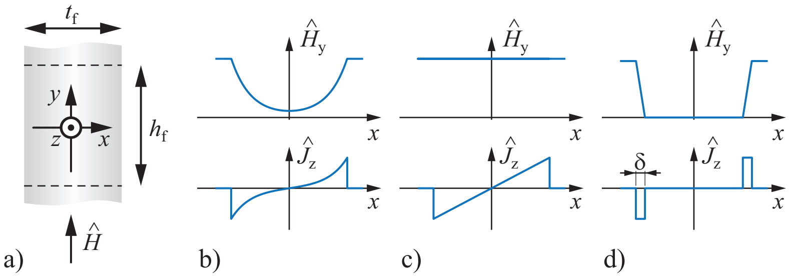


Fig. 2.7: Dimensions of a foil conductor exhibited to an external magnetic field (a); distribution of magnetic field and current density amplitude inside the foil for $\nu = 3$ (b); approximative distribution of current density and magnetic field for LF (c) and for HF (d).

field within the foil is given as (2.8) with the constants C_1 and C_2 to be determined by boundary conditions. Since the total current in the conductor is zero, the magnetic field at the conductor surfaces equals the externally applied magnetic field, i.e.

$$\underline{\hat{H}}_y\left(\frac{t_\mathrm{f}}{2}\right) = \underline{\hat{H}}_y\left(-\frac{t_\mathrm{f}}{2}\right) = \underline{\hat{H}}. \tag{2.29}$$

Therefore, $C_1 = C_2$ and the magnetic field is obtained as

$$\underline{\hat{H}}_y = \underline{\hat{H}} \frac{\mathrm{e}^{\frac{1+j}{\delta}x} + \mathrm{e}^{-\frac{1+j}{\delta}x}}{\mathrm{e}^{\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}} + \mathrm{e}^{-\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}}}. \tag{2.30}$$

Using (2.3), the current density

$$\underline{\hat{J}}_z = \underline{\hat{H}} \frac{1+j}{\delta} \frac{\mathrm{e}^{\frac{1+j}{\delta}x} - \mathrm{e}^{-\frac{1+j}{\delta}x}}{\mathrm{e}^{\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}} + \mathrm{e}^{-\frac{1+j}{\delta}\frac{t_\mathrm{f}}{2}}} \tag{2.31}$$

is derived from the magnetic field. The distribution of magnetic field and current density inside a foil conductor due to proximity effect is shown in Fig. 2.7b. Comparing the current density in a foil conductor due to skin effect (2.18) and due to proximity effect (2.31) shows that the first is an even, the second an odd function of x. Since even and odd functions are orthogonal to each other the losses due to the proximity effect can be simply added to the losses caused by the skin effect [25].

The losses per unit area of the foil can be expressed by evaluating the Poynting vector, considering both surfaces by applying a factor two.

Therefore, the loss per unit area of a foil is

$$P'' = \Re\left\{\underline{\hat{E}}_z\left(\frac{t_\mathrm{f}}{2}\right)\underline{\hat{H}}_y^*\left(\frac{t_\mathrm{f}}{2}\right)\right\} = \frac{\hat{H}^2}{2\sigma\delta}\frac{\sinh(\frac{t_\mathrm{f}}{\delta})-\sin(\frac{t_\mathrm{f}}{\delta})}{\cosh(\frac{t_\mathrm{f}}{\delta})+\cos(\frac{t_\mathrm{f}}{\delta})}. \tag{2.32}$$

In analogy to the expression for the loss due to the skin effect, a factor G_f is commonly used to describe the proximity loss in a foil of thickness t_f per unit length as

$$P'_\mathrm{f,prox} = R'_\mathrm{dc}G_\mathrm{f}(\nu)\hat{H}^2 \tag{2.33}$$

with

$$R'_\mathrm{dc} = \frac{1}{\sigma h_\mathrm{f} t_\mathrm{f}} \tag{2.34}$$

and

$$G_\mathrm{f} = h_\mathrm{f}^2\nu\frac{\sinh(\nu)-\sin(\nu)}{\cosh(\nu)+\cos(\nu)}, \quad \nu = \frac{t_\mathrm{f}}{\delta}. \tag{2.35}$$

The exact analytic result of $G_\mathrm{f}(\nu)$ is shown together with the results obtained numerically using a FEM simulation in Fig. 2.8. The numerical results verify the analytic solution. Asymptotic approximations for the cases of LF and HF can be identified from this plot.

In case of LF, i.e. if the foil thickness is much smaller than the skin depth, the induced eddy currents inside the foil do not change the total amplitude of the magnetic field in the foil significantly. In this case it can be assumed that the magnetic field inside the conductor equals the externally applied homogeneous magnetic field. By integrating Faraday's law in the form of (2.4), the electric field inside the foil is obtained as a function of the external magnetic field $\underline{\hat{H}}$ as

$$\underline{\hat{E}}_z(x) = \int_0^x j\omega\mu\underline{\hat{H}}_y\mathrm{d}x' = j\omega\mu\underline{\hat{H}}x. \tag{2.36}$$

This approximation is illustrated in Fig. 2.7c. The electric field, due to $J = \sigma E$, results in eddy current losses. Therefore, the time average proximity loss per unit length (z-direction) within a foil of thickness t_f and height h_f subjected to a magnetic field amplitude $\hat{H}$ is

$$P'_\mathrm{f,prox,LF} = h_\mathrm{f}\int_{-\frac{t_\mathrm{f}}{2}}^{\frac{t_\mathrm{f}}{2}}\frac{1}{2}\sigma E_z(x)^2\mathrm{d}x = \frac{1}{24}\sigma\mu^2\omega^2\hat{H}^2h_\mathrm{f}t_\mathrm{f}^3. \tag{2.37}$$

In case of HF, i.e. if the foil thickness is much larger than the skin depth, the magnetic field at the interior of the foil is almost zero. It is therefore

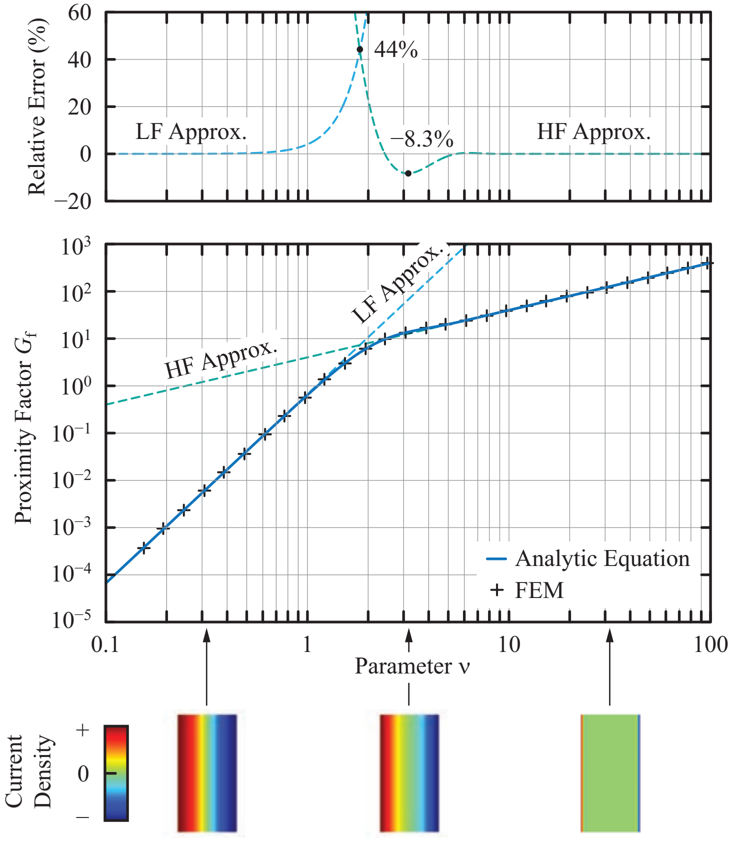


Fig. 2.8: Comparison of analytic solution, FEM simulation and LF and HF approximations of the proximity effect factor G_f of foil conductors.

assumed that a current is flowing within the skin depth beneath the surfaces of the foil such that the external magnetic field inside the foil is compensated as shown in Fig. 2.7d. The current amplitude per y-unit length beneath each of the two surface is

$$\hat{I}' = \hat{H} h_\mathrm{f}. \tag{2.38}$$

Assuming the current is uniformly distributed within the skin-depth, the HF approximation for the proximity loss per z-unit length within a piece of foil with height h_f is

$$P'_\mathrm{f,prox,HF} = \frac{h_\mathrm{f}}{\sigma\delta}\hat{H}^2. \tag{2.39}$$

At this point it is interesting to note that for LF the proximity losses increase with f^2 and t_f^3, while for HF they only increase with $\sqrt{f}$ and are independent on the foil thickness. Using the notation as in (2.33), the approximations for the factor G_f can be summarized as

$$G_\mathrm{f} \approx \begin{cases} \frac{h_\mathrm{f}^2 t_\mathrm{f}^4}{6\delta^4}, & \text{if } t_\mathrm{f} < 6^{\frac{1}{3}}\delta \\ \frac{h_\mathrm{f}^2 t_\mathrm{f}}{\delta}, & \text{if } t_\mathrm{f} \geq 6^{\frac{1}{3}}\delta \end{cases}. \tag{2.40}$$

In order to obtain a continuous function, the boundary, $\nu = 6^{\frac{1}{3}} \approx 1.8$, is selected. As shown in Fig. 2.8 the approximation results in a maximum error of $+44\,\%/-8.3\,\%$.

Proximity Effect in Round Conductors

The exact expression for the proximity loss in a round conductor of diameter d_r subjected to a homogeneous external magnetic field of amplitude $\hat{H}$ is

$$P'_\mathrm{r,prox} = R'_\mathrm{dc} G_\mathrm{r}(\xi)\hat{H}^2, \tag{2.41}$$

with

$$R'_\mathrm{dc} = \frac{4}{\sigma d_\mathrm{r}^2 \pi}, \quad \xi = \frac{d_\mathrm{r}}{\sqrt{2}\delta}, \tag{2.42}$$

and

$$\begin{aligned} G_\mathrm{r} = \frac{\xi\pi^2 d_\mathrm{r}^2}{2\sqrt{2}} \Bigg(& \frac{\mathrm{bei}_2(\xi)\mathrm{ber}_1(\xi) - \mathrm{ber}_2(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \\ & - \frac{\mathrm{ber}_2(\xi)\mathrm{bei}_1(\xi) + \mathrm{bei}_2(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \Bigg). \end{aligned} \tag{2.43}$$

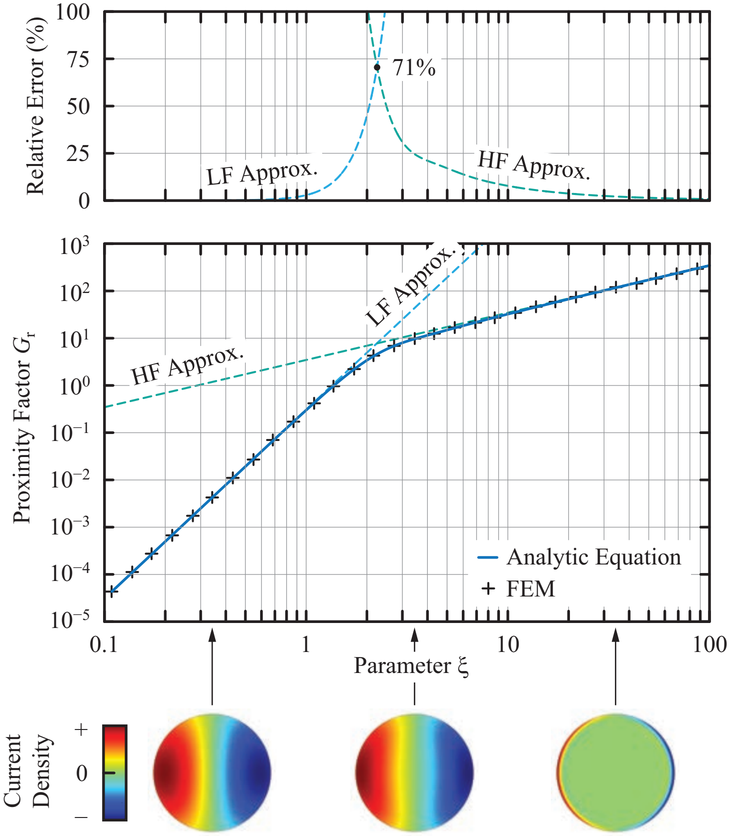


Fig. 2.9: Comparison of analytic solution and FEM simulation of the proximity effect factor G_r of round conductors.

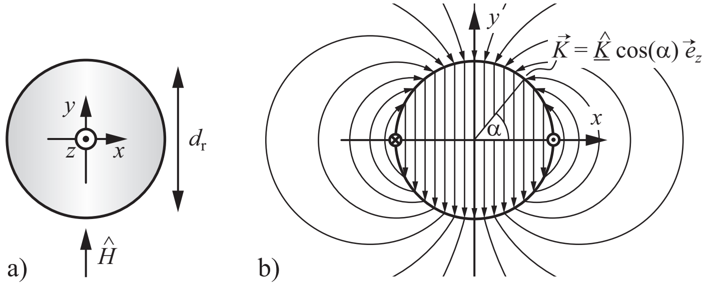


Fig. 2.10: Round conductor with coordinate system and dimensions as used for the derivation of the LF and HF asymptotes (a) and surface current distribution $\vec{K}(\alpha)$ resulting in a homogeneous magnetic field within a cylinder (b).

The accurate analytical solution, based on a modified Bessel function, is stated in [25]. A more detailed derivation can be found in [26]. The analytic expression is shown in Fig. 2.9 and compared to a FEM simulation. As expected the simulation agrees with the analytic solution. The logarithmic scale reveals that there are two asymptotes for $\xi \to 0$ (LF) and $\xi \to \infty$ (HF). For the case of LF, the external magnetic field penetrates the conductor and is only weakly affected by the eddy currents flowing in the conductor. It is thus assumed that the magnetic field inside the conductor is constant and equals the externally applied magnetic field $\underline{\hat{H}}$ oriented in y-direction as shown in Fig. 2.10a. Since there is no variation in z-direction Faraday's law (2.2) simplifies to the one-dimensional expression

$$\frac{\mathrm{d}\underline{\hat{E}}_z}{\mathrm{dx}} = j\omega\mu\underline{\hat{H}}, \tag{2.44}$$

and therefore the electric field for the LF approximation is

$$\underline{\hat{E}}_z(x) = j\omega\mu\underline{\hat{H}}x. \tag{2.45}$$

By integrating the loss density within the conductor $p = \frac{1}{2}\sigma\hat{E}^2$ using $x = r\cos(\alpha)$ the average loss per unit length is obtained as

$$P'_{\mathrm{r,prox,LF}} = \int_0^{\frac{d_\mathrm{r}}{2}} \int_0^{2\pi} \frac{1}{2}\sigma\omega^2\mu^2\hat{H}^2(r\cos(\alpha))^2 r\mathrm{d}\alpha\mathrm{dr} = \frac{\pi\sigma\mu^2\omega^2\hat{H}^2 d_\mathrm{r}^4}{128}. \tag{2.46}$$

For the case of HF, the eddy currents induced within the conductor counteract the external magnetic field such that the magnetic field inside the conductor is virtually zero. For the derivation of the HF asymptote it is assumed that a current $\vec{K} = K_z\vec{e}_z$ is flowing at the surface of the conductor such that the magnetic field inside the conductor is zero. A surface current distribution,

$$\underline{\hat{K}}_z = \underline{\hat{K}}\cos(\alpha), \tag{2.47}$$

at the surface of a cylinder with α as shown in Fig. 2.10b results in a homogeneous magnetic field $\underline{\vec{H}} = -\frac{\hat{K}}{2}\vec{e}_y$ inside the cylinder. It is now assumed that the surface current is flowing in a layer of skin-depth beneath the surface. Due to the local and temporal sinusoidal distribution the RMS value of the current within this skin depth tube is

$$I_{\mathrm{rms}} = \frac{1}{\sqrt{2}}\frac{1}{\sqrt{2}}2\hat{H}\pi d_{\mathrm{r}}. \tag{2.48}$$

Therefore, the losses per unit length due to the proximity effect in a round conductor for HF are

$$P'_{\mathrm{r,prox,HF}} = I^2_{\mathrm{rms}}\frac{1}{\sigma\delta\pi d_{\mathrm{r}}} = \hat{H}^2\frac{\pi d_{\mathrm{r}}}{\sigma\delta}. \tag{2.49}$$

Summarizing the proximity loss asymptotes for LF and HF using the notation as in (2.41), the factor G_{r} can be approximated as

$$G_{\mathrm{r}} \approx \begin{cases} \frac{\pi^2 d_{\mathrm{r}}^6}{128\delta^4}, & \text{if } d_{\mathrm{r}} < 32^{\frac{1}{3}}\delta \\ \frac{\pi^2 d_{\mathrm{r}}^3}{4\delta}, & \text{if } d_{\mathrm{r}} \geq 32^{\frac{1}{3}}\delta \end{cases} \tag{2.50}$$

with a maximum error of 71 % at the boundary of LF and HF, which is chosen at $d_{\mathrm{r}} = 32^{\frac{1}{3}}\delta \approx 3.17\delta$ in order to obtain a continuous function for G_{r}.

2.1.3 Winding of Foil or Round Conductors

In a winding consisting of multiple conductors of foil, round wire or litz wire, the losses in each individual conductor are caused by the skin effect within the conductor and the proximity effect caused by the magnetic field of all other conductors of the winding. As long as the magnetic field that each conductor is exposed to is an even function

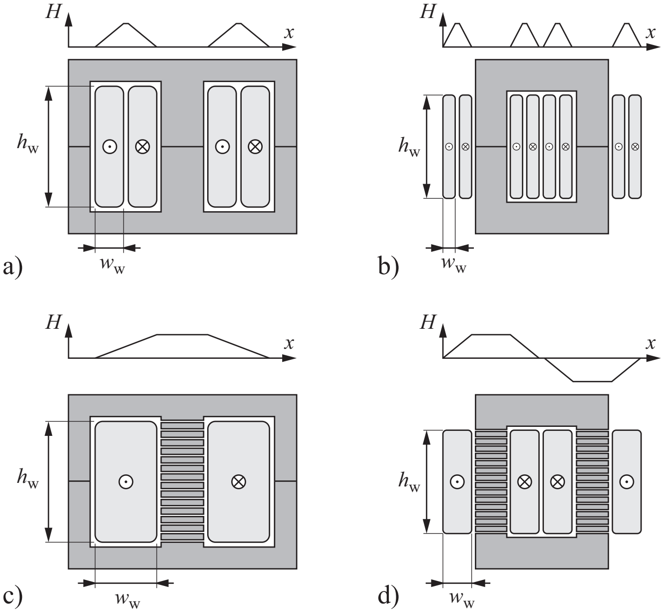


Fig. 2.11: Approximative magnetic field distribution in typical winding arrangements. (a) Transformer windings on an E-core. (b) Transformer windings on a U-core. (c) Inductor winding on an E-core with distributed gap. (d) Inductor winding on a U-Core with distributed gap.

with respect to the conductor center, the eddy current density induced by this magnetic field is an odd function. Since the current density distribution due to skin effect is always an even function, the current densities due to skin effect and due to proximity effect are orthogonal. Therefore, skin- and proximity losses can be simply added to obtain the total losses per unit length,

$$P' = P'_{\text{skin}} + P'_{\text{prox}} = R'_{\text{dc}}(F\hat{I}^2 + G\hat{H}^2), \tag{2.51}$$

in a single conductor of the winding. Since the part of the proximity losses is proportional to the magnetic field squared, the average power dissipated in the conductors of the winding due to eddy currents is obtained by using the spatial RMS value

$$\hat{H}_{\text{srms}} = \sqrt{\frac{1}{V}\int_{\mathscr{V}} \hat{H}^2 \mathrm{dV}} \tag{2.52}$$

of the magnetic field within the winding volume $\mathscr{V}$. In case of transformer windings and distributed gap inductor windings the magnetic field in the winding can be approximated as linearly increasing as shown in Fig. 2.11. If the different turn lengths within a winding are neglected, for a linearly increasing magnetic field the spatial RMS value is

$$\hat{H}_{\text{srms}} = \frac{N\hat{I}}{\sqrt{3}h_{\text{w}}}. \tag{2.53}$$

Due to its triangular shape (Fig. 2.11), the ratio of the magnetic field maximum value $\frac{N\hat{I}}{h_{\text{w}}}$ in the winding to its spatial RMS value is $\sqrt{3}$, same as the ratio between peak and RMS value of a triangular waveform in time domain. The number of conductors N is not necessarily equal to the number of turns, instead it is the total number of round conductors or strips of foil within the cross section of the winding. It is assumed that each conductor is carrying the same current $\hat{I}$. The partitioning of the conductors into turns is not relevant at this point because the total amount of proximity losses only depends on the RMS magnetic field within the winding and, assuming all conductors carry the same amount of current, the magnetic field distribution within the winding is the same no matter if the conductors are connected in series as in a single conductor winding or (partly) in parallel as in a litz wire winding. In case of a parallel connection however, the homogeneous current

$$\text{Foil:}\quad \frac{R_\mathrm{ac}}{R_\mathrm{dc}} \approx \begin{cases} 1+\frac{1}{9}\frac{k_\mathrm{cu}^2 w_\mathrm{w}^2 t_\mathrm{f}^2}{\delta^4} & : t_\mathrm{f} < 6^{\frac{1}{3}}\delta \\ \frac{1}{\delta}\left(\frac{t_\mathrm{f}}{2}+\frac{2k_\mathrm{cu}^2 w_\mathrm{w}^2}{3t_\mathrm{f}}\right) & : t_\mathrm{f} \geq 6^{\frac{1}{3}}\delta \end{cases}$$

$$\text{Round:}\quad \frac{R_\mathrm{ac}}{R_\mathrm{dc}} \approx \begin{cases} 1+\frac{1}{12}\frac{k_\mathrm{cu}^2 w_\mathrm{w}^2 d_\mathrm{r}^2}{\delta^4} & : d_\mathrm{r} < 32^{\frac{1}{3}}\delta \\ \frac{1}{\delta}\left(\frac{d_\mathrm{r}}{4}+\frac{8k_\mathrm{cu}^2 w_\mathrm{w}^2}{3d_\mathrm{r}}\right) & : d_\mathrm{r} \geq 32^{\frac{1}{3}}\delta \end{cases}$$

Tab. 2.1: Approximations for the $\frac{R_\mathrm{ac}}{R_\mathrm{dc}}$ ratio of foil- and round conductor windings with $\delta = \frac{1}{\sqrt{\pi\mu_0\sigma f}}$.

distribution between the conductors has to be guaranteed by continuously transposing the conductors, i.e. each conductor in a litz wire has to take each place in the cross section of the wire. The number of conductors in the winding,

$$N = \frac{k_\mathrm{cu} h_\mathrm{w} w_\mathrm{w}}{A_\mathrm{con}}, \tag{2.54}$$

is expressed by introducing the copper filling factor k_cu that relates the total conductor cross sectional area NA_con (copper area) to the winding area $h_\mathrm{w} w_\mathrm{w}$ with the conductor cross section of a single foil conductor $A_\mathrm{con,f} = h_\mathrm{f} t_\mathrm{f}$ or round conductor $A_\mathrm{con,r} = \frac{d_\mathrm{r}^2\pi}{4}$. By inserting (2.54) and (2.53) into (2.51) the ratio of AC resistance to DC resistance of the winding

$$\frac{R_\mathrm{ac}}{R_\mathrm{dc}} = \begin{cases} 2\left(F + \frac{k_\mathrm{cu}^2 w_\mathrm{w}^2}{3h_\mathrm{f}^2 t_\mathrm{f}^2} G\right) & : \text{foil} \\ 2\left(F + \frac{16k_\mathrm{cu}^2 w_\mathrm{w}^2}{3\pi^2 d_\mathrm{r}^4} G\right) & : \text{round} \end{cases} \tag{2.55}$$

is found. It can be observed that the proximity effect part of the AC-to-DC resistance ratio increases with the product of filling factor and winding width squared. Since for a low DC resistance a high filling factor is desired, reducing the winding width is always a very effective measure to reduce the proximity losses in a winding. Narrow windings can be achieved by using a core with a narrow but high window and/or by using interleaved windings. Inserting the approximations (2.23), (2.40), (2.27) and (2.50) for F and G as found for foil and round conductors into the ratio of AC resistance to DC resistance of the winding (2.55) results in the approximative expressions given in Tab. 2.1. The actual boundary between LF and HF region for the winding AC-to-DC resistance ratio results as root of a third degree polynomial and is too complex for practical use. Therefore, it is suggested to use the boundaries determined for the asymptotic approximations of G since the proximity losses in a winding are usually dominating over the skin effect losses. The resulting asymptotic approximations allow to calculate the AC-to-DC resistance ratio of transformer windings, including interleaved arrangements (Fig. 2.11), and distributed gap inductor windings with minimal effort, based only on the winding filling factor, the winding width and the conductor dimension and the skin depth. However, by using the spatial RMS value (2.53) of the magnetic field in the winding it is not considered that the turn length at the location where the magnetic field is low is usually not the same as the turn length where the magnetic field is high. This usually leads to an underestimation of the AC resistance of windings with the maximum value of the magnetic field appearing at the longest turn (inner windings in Fig. 2.11) and to an overestimation of the AC resistance of windings with the maximum of the magnetic field appearing at the shortest turn (outer windings in Fig. 2.11). However, for concentric winding arrangements as in Fig. 2.11 this effect cancels out in total, if both windings use the same strand diameter or foil thickness. The only further simplifications are to assume that the magnetic field distribution in the winding is triangular and one-dimensional. The simplicity of this approach also prevents errors in the implementation, and is therefore generally recommended for cases when the conductor dimensions are smaller than skin depth or much larger than skin depth, resulting in very accurate results. At the boundary of LF and HF region, the winding AC resistance is overestimated due to the overestimation of the proximity losses. However, it is shown in the following that this region should be avoided in practice by using appropriate conductor dimensions.

FEM Verification

The derived winding loss model is verified using a 2D FEM simulation of a winding of foil conductors and a winding of round wires. In order to reduce the calculation time, only a horizontal slice of the foil winding as shown in Fig. 2.12 and a single row of round conductors as shown in Fig. 2.13 are simulated. For this example, the strand diameter and the foil thickness are set to 1 mm. Each winding consists of 20 conductor layers with a distance of 1 mm. The simulated AC/DC resistance ratio k_{ac} of the foil winding is shown in Fig. 2.12. The foil winding is assumed to reach the core at the top and at the bottom, therefore the use of the

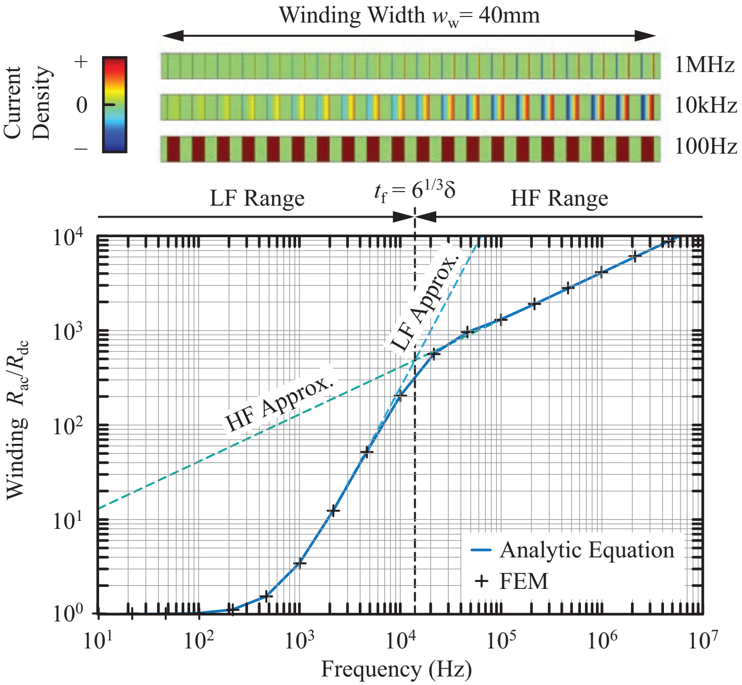


Fig. 2.12: Current distribution and ratio of AC-to-DC resistance of a 20 layer foil winding simulated using a FEM compared to the exact analytic solution and the asymptotic approximations for LF and HF range.

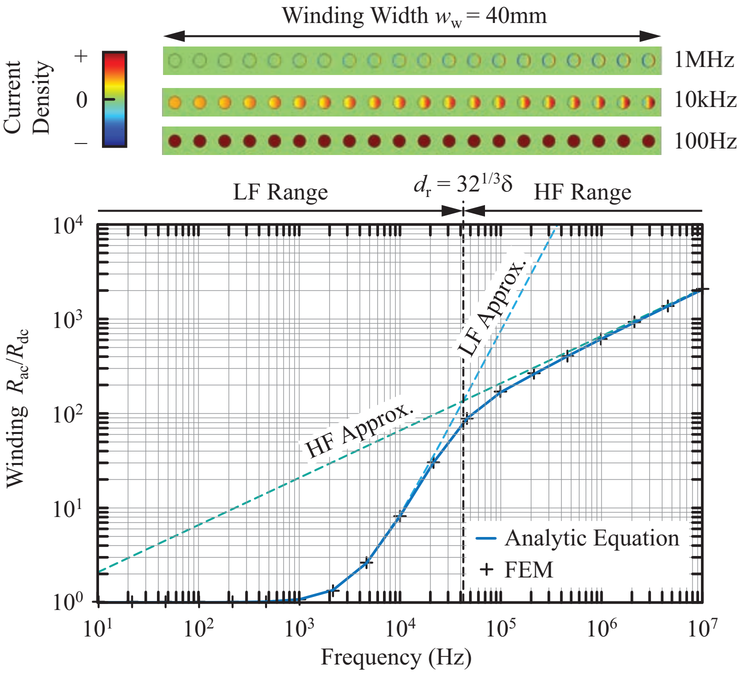


Fig. 2.13: Current distribution and ratio of AC-to-DC resistance of a 20 layer round wire winding simulated using a FEM compared to the exact analytic solution and the asymptotic approximations for LF and HF range.

one-dimensional solution is justified and the AC-to-DC resistance ratio produced by the FEM simulation matches perfectly with the exact analytic solution (2.55). The asymptotic approximations for the LF range introduce an error of less than 1 % up to frequencies where the skin depth reaches the foil thickness. At the boundary of LF and HF range the AC resistance is overestimated but the exact solution quickly converges to the HF asymptote. In practice there is always a gap between foil winding and core, causing an additional orthogonal component of the magnetic field in the winding [27] not covered by this model.

The simulated AC-to-DC resistance ratio k_{ac} of the round conductor winding is shown in Fig. 2.13. The FEM results confirm very accurately the AC-to-DC resistance ratios obtained using (2.55). For conductor diameters smaller than skin depth, the LF approximation provides an error of less than 1 %. The maximum error is observed at the boundary of LF and HF range where the proximity loss overestimation leads to an overestimation of the total winding loss. For the HF range the exact solution converges to the approximation as expected. For the case at hand the distance to the next row of conductors is chosen such that a filling factor of 10 % results. For higher filling factors the analytic result overestimates the losses by up to 66 % in the HF range compared to the values resulting from the FEM simulation. For better accuracy in densely packed windings there is a modified version of the Dowell model [28]. Due to the complexity of this modified Dowell model and because the HF range is usually avoided the model derived in this work, which is conservative, is considered sufficient.

Optimum Choice of Conductor Dimension

In order to reduce the eddy current losses in a winding the obvious choice is to reduce the strand diameter of the litz wire or the thickness of the foil. In the LF range this strategy is correct since the proximity losses are proportional to the strand diameter or foil thickness respectively squared. In the HF range however, the asymptotic approximations in Tab. 2.1 reveal that the proximity loss term actually decreases with the inverse of strand diameter or foil thickness. At the same time the skin effect term increases proportional to strand diameter or foil thickness. For the case that the filling factor of a winding and the operating frequency are given and the available cross section for the winding, i.e. the core window, is completely filled the AC-to-DC resistance ratio of the winding is shown in Fig. 2.14. The filling factor is set to 35 %, which

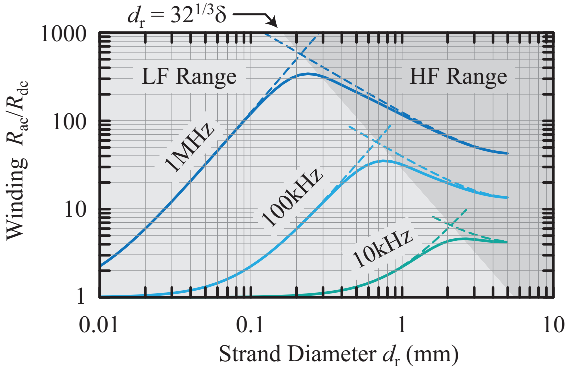


Fig. 2.14: Winding AC-to-DC resistance ratio of a round wire winding with 35 % filling factor and 5 mm winding width as function of the strand diameter for different frequencies. Solid lines mark exact analytic solution, dashed lines the asymptotic approximations.

is a typical value for round profile litz wire windings, and the winding width is set to 5 mm. It can be observed that for small strand diameters the AC resistance increases quadratically up to the point where the HF range is entered. At this point the AC resistance starts to drop with increasing strand diameter. For the case of 1 MHz that means that a 5 mm solid wire has the same AC resistance as a 60 µm litz wire. The explanation for this behaviour is that in the HF range the interior of the conductors is held field free by eddy currents on the surface of the conductors and that it is more efficient to have one eddy current circulating around one large inductor instead of many eddy currents circulating around many small conductors. This effect can be useful in (boost-) inductor windings where the dominant DC current component profits from the high filling factor of the solid conductor winding and the relatively small AC current component sees an AC resistance which is equivalent to the one of a more expensive litz wire winding.

In general the rule is to avoid round conductors with a diameter close to $32^{\frac{1}{3}}\delta \approx 3.2\delta$ and foil conductor with a thickness close to $6^{\frac{1}{3}}\delta \approx 1.8\delta$, i.e. a dimension close to the LF-HF boundary.

There are not many cases when a winding is operated in the HF range. But inductors with relatively small current ripple and dominant DC/50 Hz/60Hz current component are a typical example. In this case

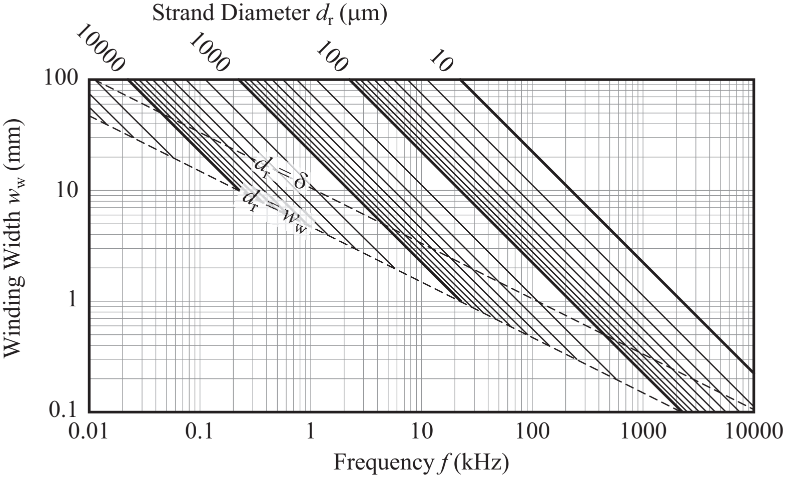


Fig. 2.15: Necessary strand diameter to reach $\frac{R_{ac}}{R_{dc}} = 1.25$ depending on the winding width and the operating frequency for litz (or round) copper wire windings with 35 % filling factor.

it is beneficial to maximize the conductor dimension such that it fills the available winding width.

Another important case are applications with dominant HF current components such as transformer- or Triangular Current Mode (TCM) inductor windings. In these situations small conductor dimensions should be selected such that the operating frequency is in the LF range. For a given winding width, operating frequency, filling factor and AC-to-DC resistance ratio the conductor dimension results from the appropriate LF relationship in Tab. 2.1. As will be shown in the following, transformer windings typically use AC-to-DC resistance ratios in the range of 1.2 - 1.8. Based on the LF approximation for round wire windings for the case of a 35 % filling factor litz (or round) copper wire winding with $\frac{R_{ac}}{R_{dc}} = 1.25$ the necessary strand diameter depending on winding width and operating frequency is shown in Fig. 2.15. Therefore, for these assumptions a 71 µm litz wire allows a winding width of 10 mm at 30 kHz, of 3 mm at 100 kHz and of only 0.3 mm at 1 MHz. This example illustrates the important fact that in the LF range for a given AC-to-DC resistance ratio the product of operating frequency, winding width and strand diameter is constant. Therefore, without increasing the AC resistance the switching frequency cannot be increased without decreasing either the winding width or the strand diameter. Since the strand diameter is limited in practice to values in the range of 50 µm large (high power) inductive components (with wide windings) have to be operated at low frequencies.

2.2 Core Loss Model

Since the core losses in an inductive component are usually approximately equal to the winding losses, modelling the loss density in the core material is equally important as modelling the winding losses. In theory loss mechanisms in ferro-magnetic materials are often categorized into three parts [29, 30]:

Hysteresis losses describe the static energy lost in one cycle of the B-H loop as function of the flux density amplitude. It is assumed that this energy is frequency independent, therefore the hysteresis loss density,

$$p_{\mathrm{h}} = k_{\mathrm{h}} f B^{\alpha}, \tag{2.56}$$

scales linear with frequency and uses a material specific exponent α to describe the scaling with the flux density.

Eddy current loss in the sheets or grains of conductive material that the core consists of can be described based on the expressions derived for the proximity loss within windings. Since conductivity and dimensions of the sheets or grains of core material are usually selected such that the skin depth is much larger than the sheet or grain dimension, the LF approximation applies and the eddy current loss density,

$$p_{\mathrm{e}} = k_{\mathrm{e}} f^2 B^2, \tag{2.57}$$

is thus assumed to scale quadratically with f and B.

Excess losses or anomalous losses account for the error due to loss mechanisms not completely understood such as the frequency dependence of the hysteresis energy and additional eddy current losses due to domain wall motion. The loss density due to the excess losses,

$$p_{\mathrm{a}} = k_{\mathrm{a}} f^{\gamma} B^{\gamma}, \tag{2.58}$$

scale with fB using the exponent γ which, depending on the assumptions used for modelling the eddy current loss due to domain wall motion, amounts to either 1.5 or 2 [31]. The concept of loss separation allows to decouple the losses of the material, i.e. sort of steel, from its structure, i.e. sheet thickness or grain size. However, in power electronics applications these kind of physics-based models have been abandoned due to the limited accuracy of the excess loss model, which can dominate the total losses in ferrite, and due to the high number of typically unknown parameters. Instead experimental data, provided by manufacturers or by own measurements, in combination with logarithmic-scale interpolation (like the Steinmetz equation) is typically used. This kind of loss-map based core loss calculation provides best accuracy and in combination with the improved generalized Steinmetz equation also allows to calculate losses for arbitrarily shaped flux density waveforms based only on loss maps recorded for sinusoidal flux density.

2.2.1 Magnetic Materials

The most common core materials used in power electronics can be categorized in five groups:

Grain oriented electrical steel is usually used in mains frequency transformers and electric machines and due to the excessive HF losses only of minor importance for application in power electronics. However it provides the highest saturation flux density of $\approx 1.9\,\mathrm{T}$.

Amorphous tape wound cores are made of thin ($\approx 25\,\mu\mathrm{m}$) layers of amorphous steel tape produced by means of fast solidification [32]. The specific losses of amorphous iron are lower than the ones of electrical steel but also the saturation flux density of 1.56 T is lower. Applications include transformers with frequencies ranging up to a few kHz as well as Differential Mode (DM) Electro Magnetic Interference (EMI) filter inductors and buck/boost inductors up to tens of kHz. Metglas from Hitachi Metals is a widely used product.

Iron powder cores consist of isolated grains of an alloy of iron silicon and aluminum which are pressed to form the desired core shape. The loss density is comparable but usually a bit higher than that of amorphous cores. The saturation process is soft, i.e. the permeability reduces to about 50 % its initial value at ≈ 0.5 T until the material saturates completely at flux densities in the range of 0.8 - 1.2 T. The main advantage of powder cores is that they are the only material available in various relative permeabilities typically in the range of 10 to 100. The low permeability eliminates the need for an airgap. Instead the core material acts as distributed airgap, greatly reducing the winding losses of buck/boost inductors. The advantage of the material is therefore not its loss density, which is typically higher than for all other materials with the exception electrical steel, but the low winding loss in inductor and flyback transformer applications. Suppliers of powder core materials include Magnetics and Micrometals.

Nanocrystalline tape wound cores are similarly produced as amorphous tapes but additional annealing greatly reduces the core loss density while also lowering the saturation flux density to 1.2 T. The low loss density and high saturation flux density makes nanocrystalline cores the preferred choice for transformers and Common Mode (CM) inductors for operating frequencies in the range from 5 to 50 kHz. Manufacturers include Vacuumschmelze (Vitroperm 500F) and Hitachi Metals (Finemet).

Ferrites used in power electronics are usually MnZn ferrites. NiZn ferrites are also available but typically used for applications requiring frequencies above 5 MHz. Power ferrites (MnZn) provide low loss densities even at high frequencies but the saturation flux density is only ≈ 0.4 T. The loss density is typically temperature dependent, reaching a minimum at ≈ 100 °C. Due to the low HF loss ferrite is the preferred choice for operating frequencies above 50 kHz. The probably most popular material group is covered by EPCOS N87 and the similar Kaschke K2008 and Ferroxcube 3C94.

The loss densities provided by the manufacturers for Magnetics KoolMu 26, Metglas 2605SA1, Vacuumschmelze Vitroperm 500F and EPCOS N87 are compared for frequencies ranging from 10 kHz to 1 MHz and flux densities ranging from 0.01 to 1.3 T. The core material with minimum loss is selected and the loss densities are plotted in Fig. 2.16. It is shown, that the powder core material KoolMu 26 does not show up in this map, since its loss density is higher than the one of all other materials on the full frequency and flux density range. The amorphous core

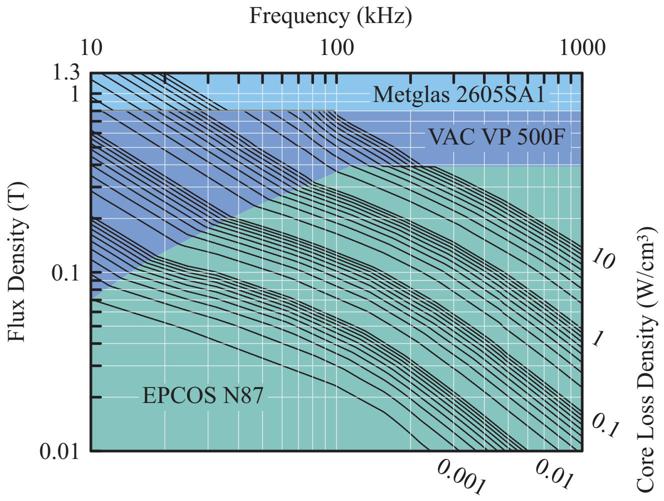


Fig. 2.16: Preferred frequency and flux density ranges for minimum loss with common core materials and according core loss density.

material Metglas 2605SA1 is preferable only for flux densities exceeding 0.78 T which is the *effective* saturation flux density of Vacuumschmelze's Vitroperm 500F. This nanocrystalline material is preferred for flux densities ranging from 0.39 to 0.78 T on the full frequency range but it is even the best choice at lower flux density values down to 80 mT at frequencies less than 100 kHz. The remaining range down to lowest flux density values is covered by the ferrite material EPCOS N87. Therefore, it depends on the targeted power density which material is the best choice at a certain frequency. Highly efficient and thus low loss density devices tend to use ferrite cores while with increasing power density nanocrystalline cores or even amorphous cores are getting more attractive.

2.2.2 Sinusoidal Flux-Waveforms

Core loss data is usually provided by manufacturers for sinusoidal flux density waveforms with amplitude $\hat{B}$ in the form of diagrams as shown in Fig. 2.17 for EPCOS N87 (a), for Vacuumschmelze Vitroperm 500F (b), for Metglas 2605SA1 (c) and for Magnetics KoolMu 26 (d). Addi-

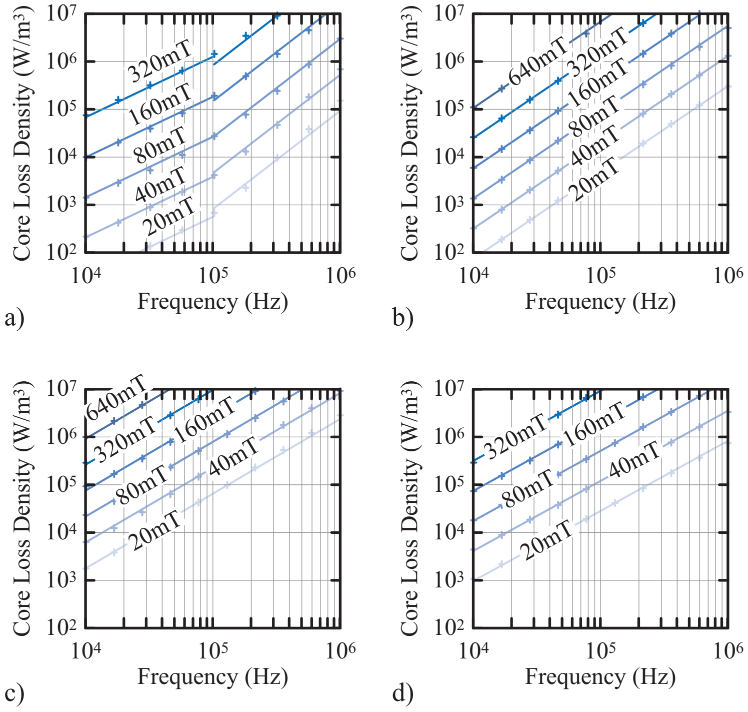


Fig. 2.17: Core loss data provided by manufacturers (+) and interpolation using the Steinmetz equation with parameters obtained from least-square fitting of the manufacturer data for EPCOS N87 100 °C(a), for Vacuumschmelze Vitroperm 500F (b), for Metglas 2605SA1 (c) and for Magnetics KoolMu 26 (d).

Material	f (kHz)	B (T)	k $(\frac{\mathrm{Ws}^{\alpha}}{\mathrm{m}^3\mathrm{T}^{\beta}})$	α	β	Error (%)
EPCOS N87 100 $^\circ C$	10 - 100	< 0.39	$1.53 \cdot 10^{1}$	1.26	2.79	-19/+18
	100 - 1000		$7.88 \cdot 10^{-4}$	2.05	2.50	-46/+23
VAC VP 500F	100 - 1000	< 0.78	$1.57 \cdot 10^{-2}$	1.81	2.10	-13/+15
Metglas 2605SA1	100 - 1000	< 1.28	1.11	1.57	1.80	-22/+16
KoolMu 26	100 - 1000	< 0.5	4.53	1.47	2.09	-12/+11

Tab. 2.2: Steinmetz parameters obtained from a least-squares fit of manufacturer provided core loss data.

tionally to the points obtained from manufacturers loss curves log-space linearly interpolated lines are shown which show the evaluation of the Steinmetz equation for the average loss density of a core material

$$\bar{p}_{\mathrm{c}} = k f^{\alpha} \hat{B}^{\beta} \tag{2.59}$$

with parameters k, α, β obtained from a least-squares fit of the manufacturer data to the equation. For EPCOS N87 the loss density data points are not perfectly linear with frequency but slightly bent. This is accounted for by splitting the frequency range into two parts separated at 100 kHz. The Steinmetz parameters obtained from this least-square fit are provided in Tab. 2.17 together with maximum relative error that occurs on the specified frequency and flux density range. Manufacturers often specify effective or magnetic core cross section and core volume values. These values are supposed to be used for the calculation of flux density and total losses of the core. While for ferrite and iron powder materials the effective values of core cross section and volume only differ by a few percent from the actual geometric dimensions, the effective core cross sections specified for Vitroperm 500F are in average only 65 % of the geometric cross section and the effective volume is only 75 % of the actual volume. This is explained by the low stacking factor of the thin tape ([33],p. 103). In order to make the different core materials comparable the loss data has been scaled such that the actual geometric dimensions can be used for all materials. Therefore, also the saturation flux density of Metglas 2605SA1 reduces from 1.56 to the effective value 1.28 T and the one of Vitroperm 500F reduces from 1.2 to 0.78 T. As shown in Tab. 2.2 the reduction of the loss data to only three parameters introduces some error, which is in the range of $\approx \pm 20\,\%$ for all materials except for ferrite at frequencies higher than 100 kHz where the error varies between -46 and 23 %. In order to avoid this error the

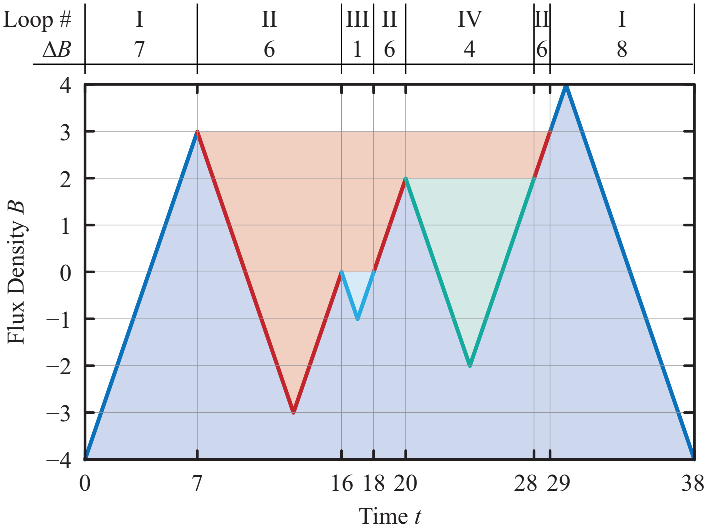


Fig. 2.18: Flux density waveform split in one major loop (I) with one sub-loop (II) with two sub-sub-loops (III & IV) according to the iGSE loop separation scheme.

complete loss data has to be used, however the Steinmetz equation still serves as an interpolation function.

2.2.3 Arbitrary Flux-Waveforms

A widely used method to estimate the core losses of arbitrarily shaped flux density waveforms using only loss data in the form of Steinmetz parameters obtained from measurements with sinusoidal flux density waveforms is the iGSE [34]. It specifies the instantaneous core loss density depending on the time derivative of the flux density and the ΔB of the current loop as

$$p_{\mathrm{c}}(t) = k_{\mathrm{i}} \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (\Delta B)^{\beta-\alpha} \tag{2.60}$$

with

$$k_{\mathrm{i}} = \frac{k}{2^{\beta-1}\pi^{\alpha-1}\int_0^{2\pi}|\cos(\theta)|^{\alpha}\mathrm{d}\theta} \approx \frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)}. \tag{2.61}$$

The average core loss density is obtained as the average, i.e. $\bar{p}_{\mathrm{c}} = \frac{1}{T}\int_0^T p_{\mathrm{c}}(t)\mathrm{d}t$.

Loop Separation

The value of ΔB is in general not constant over time, instead it has to be obtained by splitting up the flux density waveform into loops. One loop is defined to consist of one or more segments with positive flux density slope followed by one ore more segments with negative flux density slope. The process for separating a flux density waveform into subloops is:

1. Identify minimum and maximum of the waveform, the part after the minimum and before the maximum is the rising part, the rest is the falling part.

2. Go through the rising part starting at the minimum value. If the slope of the waveform turns to negative, remove everything until the level where the slope has changed is reached again. Store the removed part of the waveform and repeat this process each time the slope turns to negative until the maximum value of the waveform is reached.

3. Go through the falling part starting at the maximum value. If the slope of the waveform turns to positive, remove everything until the waveform falls below the value where the slope has changed. Store the removed part of the waveform and repeat this process each time the slope turns to positive until the minimum value of the waveform is reached.

After step 3 a complete loop is extracted from the waveform. Steps 1 to 3 are applied recursively for each of the parts which have been removed and stored during steps 2 and 3. The procedure is applied to an example waveform in Fig. 2.18. The outermost loop I ranges between -4 and 4, therefore the value of ΔB is 8. The rising part of the outermost loop is interrupted by loop II with a ΔB of 6. The rising part of loop II is again interrupted by loops III and IV, each having an individual value of ΔB.

Frequency/Flux Density Scaling

The process of loop splitting complicates the application of the iGSE, in particular in situations when the fundamental frequency of the flux density signal is many times smaller than the switching frequency, as it is the case for the flux density in the boost inductor of a PFC rectifier. In order to avoid unnecessary computational overhead, in particular in optimization routines, the f, B scaling law for the iGSE can be applied. Assuming that the average core loss density $\bar{p}_{\mathrm{c0}}$ at a frequency f_0 and a flux density peak value $\hat{B}_0$ of the boost inductor of a PFC rectifier is known. Then the core loss density for a different frequency f and flux density peak value $\hat{B}$ simply equals

$$\bar{p}_{\mathrm{c}} = \bar{p}_{\mathrm{c0}} \left(\frac{f}{f_0} \right)^{\alpha} \left(\frac{\hat{B}}{\hat{B}_0} \right)^{\beta} \tag{2.62}$$

as can be shown by inserting $B = B_0 \frac{\hat{B}}{\hat{B}_0}$ and $t = t_0 \frac{\hat{f}_0}{\hat{f}}$ into (2.60). Exploiting this scaling property allows to save considerable computation time when performing multi-objective optimizations where a high number of elements in the design space has to be mapped to the performance space.

Triangular Waveforms

The most important flux density shape in power electronics is the triangular waveform. Due to the f,B scaling property of the iGSE the core loss density for a triangular flux density with peak value $\hat{B}_{\mathrm{tri}}$ can be expressed in the form of the Steinmetz equation

$$p_{\mathrm{c,tri}} = k_{\mathrm{tri}} f^{\alpha} \hat{B}_{\mathrm{tri}} \tag{2.63}$$

with

$$k_{\mathrm{tri}} = \frac{k \left(\frac{2}{\pi} \right)^{\alpha - 1}}{0.2761 + \frac{1.7061}{\alpha + 1.354}} \tag{2.64}$$

accounting for the triangular shape. The relationship (2.64) can therefore be used to convert between Steinmetz parameters for sinusoidal and for triangular flux density waveforms.

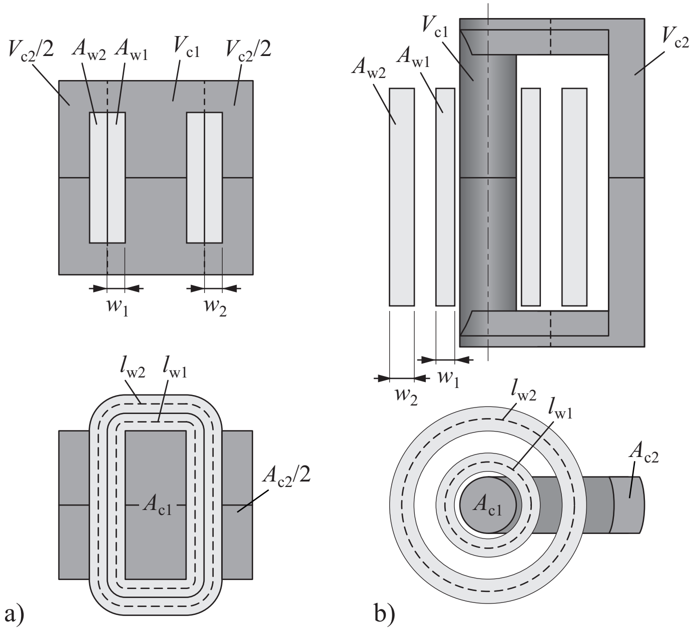


Fig. 2.19: Necessary dimensions for optimized transformer design for the example of two stacked E cores (a) and for a High-voltage transformer with UR core (b).

2.3 Optimized Transformer Design

In order to reduce the computation time of a multi-objective optimization the number of turns and the operating frequency of a transformer with a given geometry, core material and winding material can be determined analytically. The relevant expressions are derived in the following.

2.3.1 Losses in a Transformer

The total loss in a transformer consist of the losses of the two (or more) windings and the losses in the corresponding parts of the core. The core is partitioned in as many parts as there are windings assigning each core part the flux which is obtained as integral of the corresponding winding voltage per turn. Therefore, the total losses of a transformer are

$$P_{\mathrm{tot}} = \underbrace{N_1^{-\beta} f^{\alpha-\beta} \sum_i P_{\mathrm{c0}i}}_{\text{total core loss } P_{\mathrm{c}}} + \underbrace{N_1^2 \sum_i (1 + a_i f^2) P_{\mathrm{w0}i}}_{\text{total winding loss } P_{\mathrm{w}}} \tag{2.65}$$

with the normalized expressions for the core and the winding loss in each winding-core pair,

$$P_{\mathrm{c0}i} = k_{\mathrm{tri}} V_{\mathrm{c}i} \left(\frac{U_i}{4 n_i A_{\mathrm{c}i}} \right)^{\beta} \tag{2.66}$$

and

$$P_{\mathrm{w0}i} = \frac{l_{\mathrm{w}i}}{k_{\mathrm{cu}i} \sigma_i A_{\mathrm{w}i}} (n_i I_i)^2 \tag{2.67}$$

which are independent of the number of primary turns N_1 and the operating frequency f and the turns ratio of each winding i

$$n_i = \frac{N_i}{N_1}. \tag{2.68}$$

The windings AC-to-DC resistance ratios are included in the term $1 + a_i f^2$ expressing the AC-to-DC resistance ratio of each winding i using the LF winding resistance approximations (2.55) for foil and round conductors with

$$a_i = \begin{cases} \frac{1}{9}(\pi \sigma_i \mu_0 k_{\mathrm{cu}i} w_{\mathrm{w}i} t_{\mathrm{f}i})^2 & : \text{foil} \\ \frac{1}{12}(\pi \sigma_i \mu_0 k_{\mathrm{cu}i} w_{\mathrm{w}i} d_{\mathrm{r}i})^2 & : \text{round} \end{cases}. \tag{2.69}$$

It is assumed, that a 50 % duty cycle $\pm U_i$ rectangular voltage is applied to each winding i and a RMS current I_i flows through each winding's N_i turns. In Fig. 2.19 the geometric dimensions used in the expressions are shown on the basis of two examples. In Fig. 2.19a two stacked E-cores completely filled with two windings are shown, except the different average turn lengths of the windings the geometry is symmetric with respect to primary-secondary side. In Fig. 2.19b the geometry of the high-voltage transformer used in this work is shown with substantial primary-secondary asymmetry.

2.3.2 Optimum Number of Turns

With the number of turns of all windings of the transformer referred to the number of turns N_1 of the primary winding, this number can

	HET	HVT
Output Power	3 kW	30 kW
Core Geometry	2×E55/28/21	UR72/65/39
Core Material	EPCOS N87	EPCOS N87
Primary Conductor	71 µm litz	500 µm foil
Primary Filling Factor	35 %	50 %
Secondary Conductor	71 µm litz	250 µm round
Secondary Filling Factor	35 %	24 %
Primary Voltage	400 V	400 V
Primary Duty Cycle	50 %	25 %
Secondary Voltage	400 V	100 kV
Secondary Duty Cycle	50 %	50 %
Current Shape	triangular	triangular
Maximum Inverter Frequency	200 kHz	100 kHz

Tab. 2.3: Case studies for optimized transformer design.

be chosen freely to minimize the losses. Since with increasing number of turns the flux density is reduced the core losses decrease with N_1^β. Proportional to the number of turns the conductor length and the conductor cross section increase, therefore the winding losses increase with N_1^2. The total loss (2.65) is therefore minimized at

$$N_{1\mathrm{opt}} = \left(\frac{\beta}{2} \frac{f^{\alpha-\beta} \sum_i P_{\mathrm{c}0i}}{\sum_i (1 + a_i f^2) P_{\mathrm{w}0i}} \right)^{\frac{1}{2+\beta}}. \tag{2.70}$$

Inserting this value in the expressions for winding and core loss from (2.65) shows, that at the optimum number of turns the ratio of the total core loss to the total winding loss is

$$\frac{P_\mathrm{c}}{P_\mathrm{w}} = \frac{2}{\beta}. \tag{2.71}$$

The number of turns optimization is demonstrated by means of two case studies with the specifications listed in Tab. 2.3. The first example, the High Efficiency Transformer (HET), could be part of an isolated DC supply and is using a relatively large core in order to achieve high efficiency as it is suitable for continuous operation. The second example, the High-Voltage Transformer (HVT), resembles the transformer used

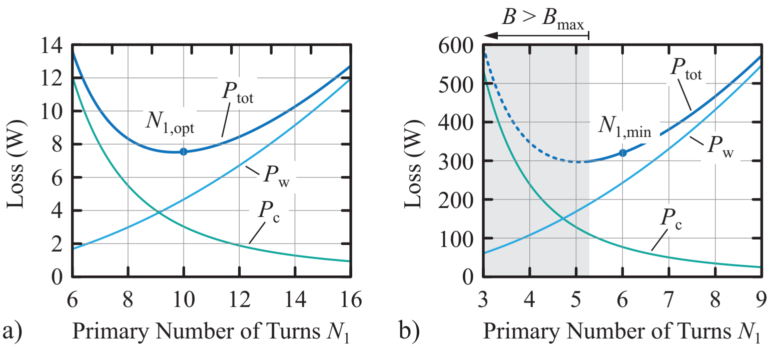


Fig. 2.20: Losses in a transformer as function of the number of turns for the High Efficiency Transformer design (a) and the High-Voltage Transformer design (b).

for the high-voltage generator constructed in this work. It is only used in pulsed operation and therefore optimized for high power density. The total loss of the HET is shown in Fig. 2.20a as function of the number of turns. It is shown that the optimum is relatively narrow because of the relatively large exponents 2 and β of winding and core loss. For the second example shown in Fig. 2.20b the optimum number of turns cannot be reached since the maximum flux density in the core would be exceeded. Therefore, the number of turns has to be set to the minimum value not exceeding the maximum flux density B_{max} (set to $0.8B_{\mathrm{sat}}$) which, for 50 % duty cycle $\pm U_i$ voltages at the windings is

$$N_{1\mathrm{min}} = \max\left(\frac{U_i}{4fA_{ci}B_{\mathrm{max}}}\right). \tag{2.72}$$

2.3.3 Optimum Operating Frequency

For a particular transformer core with a certain number of turns, the flux density amplitude is reduced with increasing operating frequency. Since usually $\beta > \alpha$, the overall core losses are reduced with increasing operating frequency. As long as the frequency is low enough and the AC-to-DC resistance ratio of the winding is close to one, the winding losses are only weakly affected by the frequency increase. Therefore, with increasing frequency the number of turns is reduced to keep the core-to-winding loss ratio at the optimum value and the total transformer losses are also reduced. However, if the operating frequency is further increased at some point the quadratic increase of the proximity losses in the winding starts to dominate and the total losses of the transformer increase with increasing frequency. The frequency where the losses reach a minimum can be found by expressing the total losses with the number of turns set to the optimum value as

$$P_{\mathrm{tot}} = P_{\mathrm{c}}\left(1+\frac{\beta}{2}\right) = \left(\frac{\beta}{2}\frac{f^{2(1-\frac{\alpha}{\beta})}}{\sum_i (1+a_i f^2) P_{\mathrm{w}0i}}\right)^{\frac{-\beta}{2+\beta}} \left(\sum_i P_{\mathrm{c}0i}\right)^{\frac{2}{2+\beta}}. \tag{2.73}$$

Differentiating and setting this expression to zero leads to the optimum operating frequency for the transformer with optimum number of turns

$$f_{\mathrm{opt,I}} = \sqrt{\left(\frac{\beta}{\alpha}-1\right)\frac{\sum_i P_{\mathrm{w}0i}}{\sum_i a_i P_{\mathrm{w}0i}}}. \tag{2.74}$$

Rearranging this expression leads to

$$\frac{P_{\mathrm{w,ac}}(f_{\mathrm{opt,I}})}{P_{\mathrm{w,dc}}} = \frac{\sum_i (1+a_i f_{\mathrm{opt,I}}^2) P_{\mathrm{w}0i}}{\sum_i P_{\mathrm{w}0i}} = \frac{\beta}{\alpha}, \tag{2.75}$$

i.e. if the number of turns and the operating frequency of a transformer are both set to their optimum values the ratio of the total winding losses to the winding losses calculated for DC equals the ratio of β to α. There are two special cases in which the formulation of the optimum operating frequency can be simplified:

1. If the values of $P_{\mathrm{w}0i}$ are all equal, which is the case if the total copper cross sections and average turn lengths of all N_{w} windings are the same and the winding RMS currents are all inversely proportional to the winding turns ratios

$$f_{\mathrm{opt,I}} = \sqrt{\left(\frac{\beta}{\alpha}-1\right)\frac{1}{\frac{1}{N_{\mathrm{w}}}\sum_i a_i}} \quad \text{and} \quad \frac{1}{N_{\mathrm{w}}}\sum_i \frac{R_{\mathrm{w}i,\mathrm{ac}}(f_{\mathrm{opt,I}})}{R_{\mathrm{w}i,\mathrm{dc}}} = \frac{\beta}{\alpha}. \tag{2.76}$$

2. If all windings of the transformer are made of the same litz wire or foil with the same filling factor and winding width, thus have the same constant a,

$$f_{\mathrm{opt,I}} = \sqrt{\left(\frac{\beta}{\alpha}-1\right)\frac{1}{a}} \quad \text{and} \quad \frac{R_{\mathrm{ac}}(f_{\mathrm{opt,I}})}{R_{\mathrm{dc}}} = \frac{\beta}{\alpha}. \tag{2.77}$$

If all windings of the transformer have the same width w_w and are made of litz wire with the same strand diameter d_r, filling factor k_cu and conductivity σ

$$f_\mathrm{opt,I} = \frac{\sqrt{12}}{\pi \sigma \mu_0 k_\mathrm{cu} w_\mathrm{w} d_\mathrm{r}} \sqrt{\frac{\beta}{\alpha} - 1}. \tag{2.78}$$

For this special, but common case one important observation is made: For a given set of Steinmetz parameters α, β, winding filling factor and conductivity the product of strand diameter, winding width, and optimum operating frequency is constant. This property can be exploited as a design criterion for the dimensioning of the strand diameter.

Up to this point it has been assumed that the optimum operating frequency is determined while the primary number of turns of the transformer is set to the optimum value N_1opt. However, there are cases when this optimum cannot be reached because the maximum flux density in the core would be exceeded. For these flux density limited cases another optimum of the operating frequency $f_\mathrm{opt,II}$ exists, assuming that the primary number of turns is set to the minimum N_1min such that the core flux density is always at its maximum value. In this case the number of turns is inversely proportional to the frequency and thus the winding losses are inversely proportional to the frequency squared. At the same time, due to the constant flux density amplitude, the core losses are increasing with f^α. The optimum frequency with minimum number of turns is therefore found by inserting (2.72) into (2.65), differentiating by f and setting to zero. It amounts to

$$f_\mathrm{opt,II} = \left(\frac{2}{\alpha} \max \left(\frac{U_i}{4 A_{\mathrm{c}i} B_\mathrm{max}} \right)^{2+\beta} \frac{\sum_i P_{\mathrm{w0}i}}{\sum_i P_{\mathrm{c0}i}} \right)^{\frac{1}{\alpha+2}}. \tag{2.79}$$

The total transformer losses as function of the operating frequency are shown in Fig. 2.21a for the HET example from Tab. 2.3. The losses are shown for the two situations: (I) $N_1 = N_\mathrm{1opt}$, and (II) $N_1 = N_\mathrm{1min}$. As expected the losses with N_1min are higher than with N_1opt for all frequencies except for the frequency where minimum and optimum number of turns are equal and the two total loss curves are tangent to each other. At frequencies below this value the optimum number of turns would exceed the maximum flux density and the optimum number of turns is therefore not feasible. In this example $f_\mathrm{opt,I}$ is at the right side of the tangent point and is therefore feasible and preferred over $f_\mathrm{opt,II}$. In the

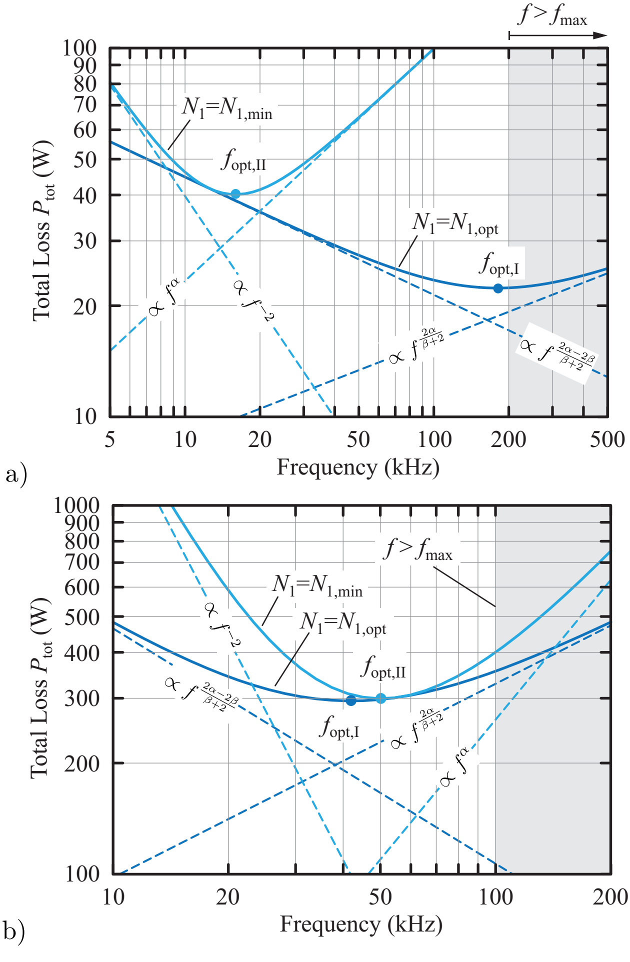


Fig. 2.21: Transformer loss as function of frequency for the number of turns either set to the minimum to not exceed the maximum flux density, or to the optimum for minimum loss. The HET example is shown in (a), the HVT example is shown in (b).

HVT example shown in Fig. 2.21b this is no longer the case, $f_{\mathrm{opt,I}}$ is at the left side of the tangent point where the optimum number of turns cannot be set and is therefore not feasible. Therefore, the frequency should be set to $f_{\mathrm{opt,II}}$ with the number of turns set to the minimum value. In general $f_{\mathrm{opt,I}}$ is feasible if the frequency at the tangent point is lower than $f_{\mathrm{opt,I}}$. This is only the case if $f_{\mathrm{opt,I}} > f_{\mathrm{opt,II}}$. Therefore, deciding between $f_{\mathrm{opt,I}}$ and $f_{\mathrm{opt,II}}$ means simply to chose the higher of the two. Usually there is an upper limit to the operating frequency depending mainly on the inverter switching losses. A good choice for selecting the maximum frequency f_{max} is the frequency where conduction and switching losses of the inverter are equal. With the constraints f_{max} and B_{max} and a given transformer geometry, core material and conductor dimensions the following optimization procedure is proposed.

1. Determine the optimum operating frequency:

$$f = \min\left(f_{\mathrm{max}}, \max\left(f_{\mathrm{opt,I}}, f_{\mathrm{opt,II}}\right)\right) \tag{2.80}$$

2. Determine the optimum number of primary turns:

$$N_1 = \max\left(\mathrm{ceil}(N_{1\mathrm{min}}), \mathrm{round}(N_{1\mathrm{opt}})\right) \tag{2.81}$$

By applying these simple steps the optimum number of turns and operating frequency can be determined without exceeding the limits set for maximum flux density in the core and maximum switching frequency of the inverter. The design could still be thermally not feasible, which remains to be checked in a following step.

2.3.4 Transformer Scaling Laws

The geometry of the HET example of Tab. 2.3 is now scaled with respect to power and box volume, while all geometric proportions of the core are kept constant. The resulting efficiency is shown in Fig. 2.22 together with the optimum switching frequency. Since the strand diameter of the litz wire is not changed during scaling, the optimum frequency $f_{\mathrm{opt,I}}$ according to (2.74) is inversely proportional to unit length ($L = V^{\frac{1}{3}}$). However this relationship is only true in region I marked in Fig. 2.22 where neither the flux density nor the operating frequency are limited by their maximum values and can thus are set optimally. Therefore, the core to winding loss ratio in region I is $\frac{2}{\beta}$ and the ratio of AC-to-DC

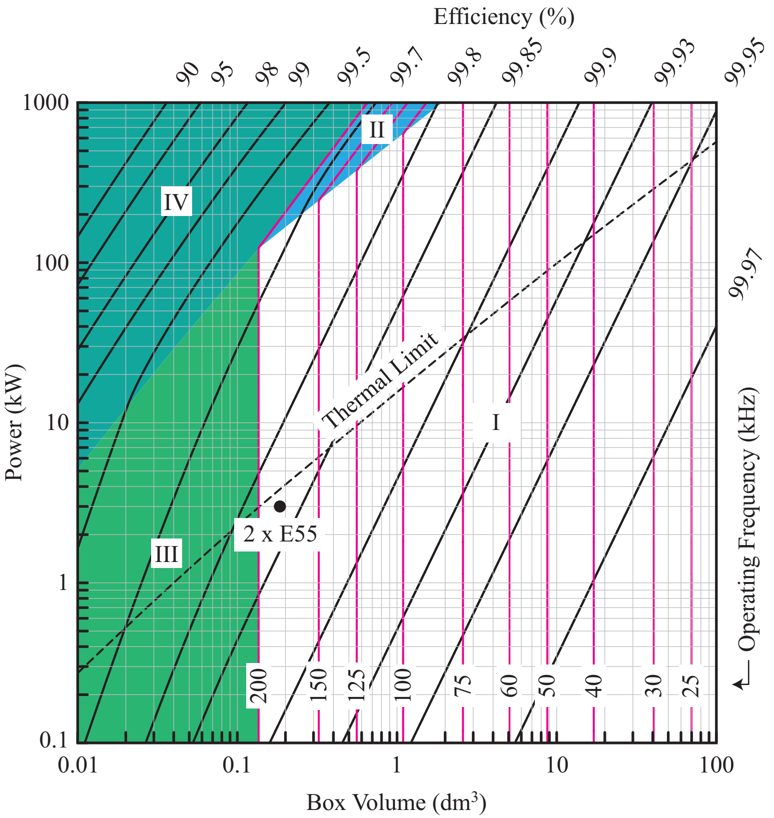


Fig. 2.22: Optimum operating frequency and efficiency as function of power and boxed volume of a transformer. It is assumed that the core's dimensions are proportional to the ones of two stacked E55 cores of N87 with 71 µm litz wire and 35 % filling factor. In region I the switching frequency and the number of turns are set to their optimum values, in region II the number of turns is set to the minimum value to not exceed the maximum flux density of $B_{\max} = 0.3\,\mathrm{T}$, the operating frequency is set to its optimum value. In region III the frequency reaches the maximum value $f_{\max} = 200\,\mathrm{kHz}$ and only the number of turns is set to the optimum value. In region IV the frequency is at the maximum value and the number of turns at the minimum to not exceed the maximum flux density.

winding resistance is $\frac{\beta}{\alpha}$. If the power of a design in region I is increased, both the current density and the flux density increase while the operating frequency remains unchanged. At the point where the flux density reaches the maximum value, region II is entered. In this region the optimum operating frequency $f_{\mathrm{opt,II}}$ (2.79) applies which is, at the same box volume, higher than $f_{\mathrm{opt,I}}$. Transformer designs for continuous operation are unlikely to lie within regions II. However, designs operating with pulse power only, such as the HVT designed in this work, are typically located in region II. In addition to the flux density limit, the limit of the operating frequency f_{max} is responsible for two more regions. If the volume of a transformer design in region I is reduced while keeping the power constant, the optimum operating frequency increases until it reaches the maximum frequency and region III is entered. Within this region, the flux density is still below its maximum value, thus the number of turns is set to the optimum value and the ratio of core to winding losses is $\frac{2}{\beta}$, but the operating frequency is fixed. If, at constant box volume, the power in region III is increased flux density and current density increase until the flux density reaches the maximum value. At this point region IV is entered where both frequency and flux density equal their maximum values. The power for a given box volume in region IV is still variable but only by means of varying the current density. Therefore, the ratio of core to winding loss in region IV is smaller than $\frac{2}{\beta}$. Region IV is also entered if the box volume of a design in region II is reduced while keeping the power constant. Due to the thermal limit shown in Fig. 2.22, which is calculated for natural convection and radiation cooling, transformer designs for continuous operation are usually located within regions I or III, depending on the value of the maximum inverter frequency which is set to 200 kHz in this example. In these regions the ratio of core to winding losses is constant with $\frac{2}{\beta}$ and therefore simple scaling laws for the transformer losses as function of volume and power can be derived.

Region I

Inserting the optimum values of number of turns (2.70) and frequency (2.74) in region I into the expression for the total loss of the transformer (2.65) results in

$$P_{\mathrm{tot,I}} = (2+\beta)\left(\frac{\sum_i P_{\mathrm{c0}i}}{2}\right)^{\frac{2}{2+\beta}}\left(\frac{\sum_i P_{\mathrm{w0}i}}{\alpha}\right)^{\frac{\beta}{2+\beta}} f_{\mathrm{opt,I}}^{\frac{2(\alpha-\beta)}{2+\beta}}. \qquad (2.82)$$

Considering only the geometric dimensions of the core and the power the scaling law for the losses in region I

$$P_{\mathrm{tot,I}} \propto \left(\frac{V_{\mathrm{c}}^{\frac{1}{\beta}} V_{\mathrm{w}}^{\frac{1}{2}}}{A_{\mathrm{c}} A_{\mathrm{w}}} w_{\mathrm{w}}^{1-\frac{\alpha}{\beta}} P \right)^{\frac{2\beta}{2+\beta}} \propto L^{\frac{6-3\beta-2\alpha}{2+\beta}} P^{\frac{2\beta}{2+\beta}} \tag{2.83}$$

can be derived. The exponent for the power ranges between 0.95 for Metglas, 1.02 for Vitroperm 500F and 1.16 for N87 ($< 100\,\mathrm{kHz}$). Therefore, the losses scale almost linearly with the power, i.e. the efficiency is only weakly depending on the transferred power. The exponent for the unit length L however ranges between -0.67 for Metglas, -0.96 for Vitroperm 500F and -1.02 for N87 ($< 100\,\mathrm{kHz}$). The losses therefore scale approximately inversely proportional to the unit length for ferrite and nano-crystalline materials. The scaling law for the losses in region I allows to optimize a core geometry for minimum losses without the need to know operating frequency or power, i.e. without knowing the application by simply minimizing the term $\frac{V_{\mathrm{c}}^{\frac{1}{\beta}} V_{\mathrm{w}}^{\frac{1}{2}}}{A_{\mathrm{c}} A_{\mathrm{w}}} w_{\mathrm{w}}^{1-\frac{\alpha}{\beta}}$ for a given box volume. This way for a given core material the core geometry that results in the lowest losses for a given box volume can be found. The expression $\frac{V_{\mathrm{c}}^{\frac{1}{\beta}} V_{\mathrm{w}}^{\frac{1}{2}}}{A_{\mathrm{c}} A_{\mathrm{w}}} w_{\mathrm{w}}^{1-\frac{\alpha}{\beta}}$ can also be used as a Figure Of Merit (FOM) that completely describes the influence of the core dimensions on the losses. A similiar FOM has been proposed in [35] but without considering the part $w_{\mathrm{w}}^{1-\frac{\alpha}{\beta}}$ for the influence of the winding width on the HF winding resistance.

Region III

For the frequency limited, but number of turns optimal case of region III inserting the optimum number of turns (2.70) into (2.65) results in

$$P_{\mathrm{tot,III}} = (2+\beta) \left(\frac{\sum_i P_{\mathrm{c}0i}}{2} \right)^{\frac{2}{2+\beta}} \left(\frac{\sum_i (1 + a_i f_{\mathrm{max}}^2) P_{\mathrm{w}0i}}{\beta} \right)^{\frac{\beta}{2+\beta}} f_{\mathrm{max}}^{\frac{2(\alpha-\beta)}{2+\beta}} . \tag{2.84}$$

Therefore, the losses in region III approximately scale with

$$P_{\mathrm{tot,III}} \propto \left(\frac{V_{\mathrm{c}}^{\frac{1}{\beta}} V_{\mathrm{w}}^{\frac{1}{2}}}{A_{\mathrm{c}} A_{\mathrm{w}}} P \right)^{\frac{2\beta}{2+\beta}} \propto L^{\frac{6-5\beta}{2+\beta}} P^{\frac{2\beta}{2+\beta}} . \tag{2.85}$$

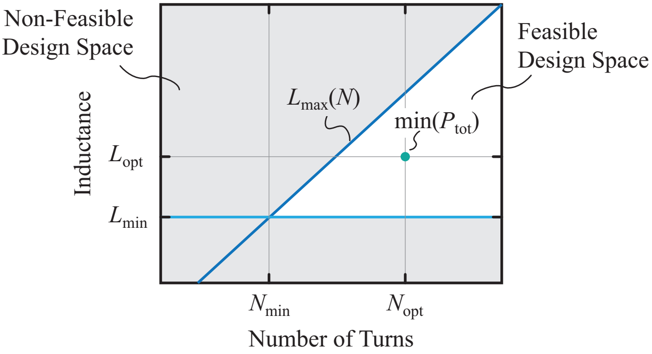


Fig. 2.23: Feasible design space for the degrees of freedom N and L of a buck/boost inductor, assuming a given magnetic core.

The scaling law with power in regions I and III is therefore the same, the exponent of the unit length L however is different and ranges between -0.79 for Metglas, -1.1 for Vitroperm 500F and -1.66 for N87 ($<$ 100 kHz).

2.4 Optimized Inductor Design

Assuming an inductor in a boost or buck converter shall be realized with a given core with adjustable air gap and a given type of winding. In this case the the number of turns N and the air gap g have to be specified, desirable to the values that minimize the total loss P_{tot} of the inductor in its nominal operating point or a weighted average of multiple operating points. Since the inductance is a function of the number of turns and the air gap, instead of using N and g as parameters, equivalently N and L can be used as degrees of freedom with the air gap being a dependent variable. The resulting design space N,L is illustrated in Fig. 2.23. For a given number of turns N there is a maximum achievable value of L_{max} which appears at the minimum air gap which is possible without exceeding the specified maximum flux density in the core. Independently of the number of turns one usually wants to specify a minimum value of the inductance L_{min} (i.e. a maximum current ripple) due to EMI filter requirements or due to limitations of the current controller. Within the remaining feasible design space $N > N_{\text{min}}$ and

$L_{\text{max}}(N) > L > L_{\text{min}}$ the number of turns and the inductance may be varied to minimize the total losses P_{tot}.

2.4.1 Losses in an Inductor

Assuming that the inductance of a boost inductor can be varied, the current in the boost inductor may be split into a LF- and a HF-part,

$$i = i_{\text{lf}} + i_{\text{hf}} = i_{\text{lf}} + \frac{\psi_{\text{hf}}}{L}. \tag{2.86}$$

The LF-part is independent of L since it is forced by the current controller. The HF-part, sometimes referred to as ripple, is inversely proportional to the inductance. The total losses in an inductor are therefore partitioned into three parts

$$P_{\text{tot}} = N^{-\beta} P_{\text{c0}} + N^2 P_{\text{wlf0}} + N^2 P_{\text{whf0}}, \tag{2.87}$$

with the core loss constant according to the iGSE,

$$P_{\text{c0}} = \frac{V_{\text{c}}}{A_{\text{c}}^{\beta}} \frac{1}{T} \int_0^T k_i \left| \frac{\mathrm{d}\psi_{\text{hf}}}{\mathrm{d}t} \right|^{\alpha} (\Delta\psi_{\text{hf}})^{\beta-\alpha} \mathrm{d}t, \tag{2.88}$$

the LF winding loss constant,

$$P_{\text{wlf0}} = \frac{l_{\text{w}}}{k_{\text{cu}} \sigma A_{\text{w}}} I_{\text{lf}}^2, \tag{2.89}$$

and the HF winding loss constant including the switching frequency harmonics k,

$$P_{\text{whf0}} = \frac{l_{\text{w}}}{k_{\text{cu}} \sigma A_{\text{w}} L^2} \frac{1}{2} \sum_k \frac{R_{\text{ac}}(k)}{R_{\text{dc}}} \hat{\psi}_{\text{hf}(k)}^2. \tag{2.90}$$

The LF-part of the core losses is usually very small for 50 Hz applications and therefore neglected in this loss calculation.

2.4.2 Optimum Inductance and Number of Turns

The analysis shows that only the HF winding losses depend on the inductance value, with high values of inductance reducing the losses.

Therefore, with this simple model for the losses of an inductor the maximum possible inductance,

$$L_{\max} = \frac{N A_{\mathrm{c}} B_{\max} - \Psi_{\mathrm{hf,max}}}{I_{\mathrm{lf,max}}}, \tag{2.91}$$

which minimizes the current ripple, is considered to be optimal, i.e. $L_{\mathrm{opt}} = L_{\max}$. This simplification is not considering the LF core losses and the DC bias related core loss increase. Both increase with increasing inductance. The maximum inductance value, for a given number of turns, is in any case limited by the saturation flux density of the core and the maximum LF current value, including overload scenarios. Therefore, a high saturation flux density indirectly reduces the HF winding losses same as a low LF peak current as it is the case in current compensated inductors (common mode chokes). Rearranging expression (2.91) allows to calculate the minimum number of turns $N_{\min}$ such that the minimum required inductance $L_{\min}$ is reached without exceeding the maximum core flux density as indicated in Fig. 2.23. Assuming that the maximum possible inductance value, i.e. the smallest possible air gap, with a given number of turns minimizes the losses, inserting $N_{\max}$ for N into (2.90) results in an expression for P_{tot} only depending on the number of turns. It is not possible to analytically specify the number of turns that minimizes the total loss, therefore this minimum has to be found numerically. However it shall be pointed out that the dependence of the HF winding losses on the number of turns is relatively weak if $N A_{\mathrm{c}} B_{\max} \gg \Psi_{\mathrm{hf,max}}$ since in this case

$$\frac{N}{L} = \frac{N I_{\mathrm{lf,max}}}{N A_{\mathrm{c}} B_{\max} - \Psi_{\mathrm{hf,max}}} \approx \frac{I_{\mathrm{lf,max}}}{A_{\mathrm{c}} B_{\max}}. \tag{2.92}$$

For this low ripple case the optimum value of the number of turns can be approximated as

$$N_{\mathrm{opt}} \approx \left(\frac{\beta P_{\mathrm{c0}}}{2 P_{\mathrm{wlf0}}} \right)^{\frac{1}{2+\beta}}. \tag{2.93}$$

For the three-phase three-level rectifier designed in this work the losses within one of the three boost inductors as function of the inductance are analysed in Fig. 2.24 for three different core sizes. The number of turns is set to the minimum possible value according to (2.91), such that $L = L_{\max}$. It is shown that the HF-part of the winding losses is only

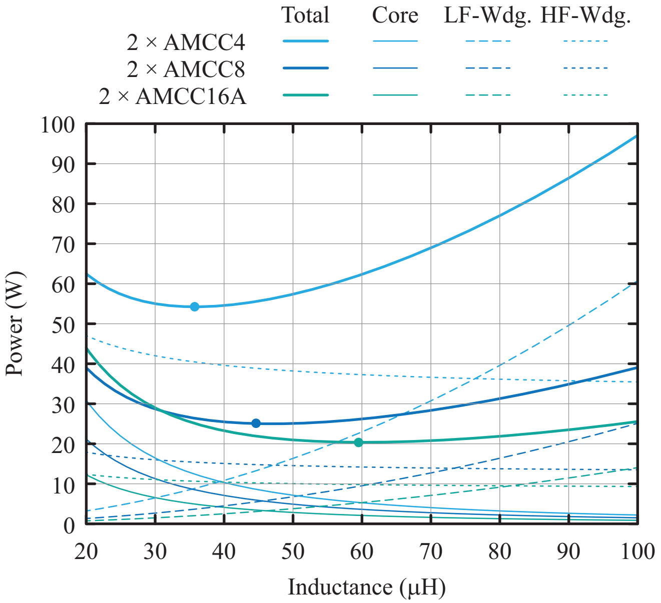


Fig. 2.24: Average loss components in one of three boost inductors of the three-phase three-level rectifier built in this work for the average of the two nominal operating points of 12 kW and 65 kW for three different amorphous cut cores as function of the inductance.

weakly affected by the selected inductance value since a higher value of inductance results in a higher number of turns and thus higher winding resistance but also in a lower ripple current. The main trade-off is observed between high core losses at low inductance values and high LF winding losses at high inductance values. Unsurprisingly with increasing core size the losses at the optimum value of inductance decrease. However it is interesting to note that with increasing core volume also the inductance at the optimum number of turns increases. The reason for that is, that with increasing volume the loss density in both core and winding is reduced and thus the flux density HF component must be decreased, resulting in a lower relative current ripple, i.e. in a higher inductance value. Therefore, the optimum inductance value of a boost inductor is a function of its size and should not be determined arbitrarily by specifying a certain relative current ripple. A high power density inductor with low volume automatically leads to a small optimum inductance value and high current ripple, while a highly efficient large inductor geometry results in a relatively large optimum inductance value and small relative current ripple.

2.4.3 Total Cost of Ownership Optimization

It has been shown that both, the optimum number of turns and the optimum inductance of a boost or buck inductor are defined by the volume of the core. The question which core volume to select still remains. A simple answer is: the cheapest. However, to find the cost minimum not only the material costs have to be taken into account since there is a trade-off between volume and losses as shown for the three-phase rectifier designed in this work in Fig. 2.26.

By assigning a cost to the losses using the price of electric energy and the specified operating hours of the device the trade-off between loss and volume, i.e. between energy- and material cost is resolved. The sum of energy and material cost is the total cost of ownership. Assuming an electricity price of 0.15 EUR/kWh, operation for eight hours per day during 20 years and with the material prices published in [19] the total costs of ownership are calculated as shown in Fig. 2.27.

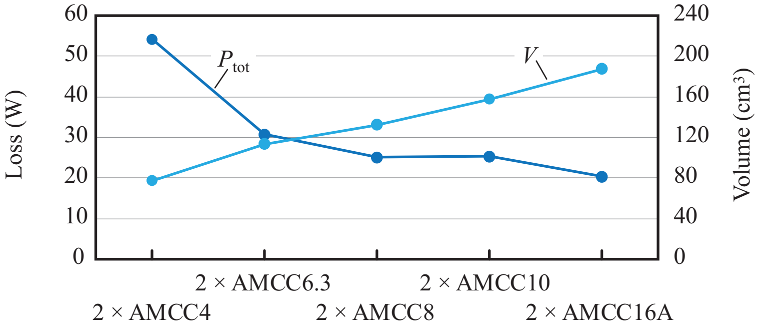


Fig. 2.25

Fig. 2.26: Volume and loss trade-off of the boost inductors of the three-phase three-level rectifier built in this work for five different amorphous cut cores.

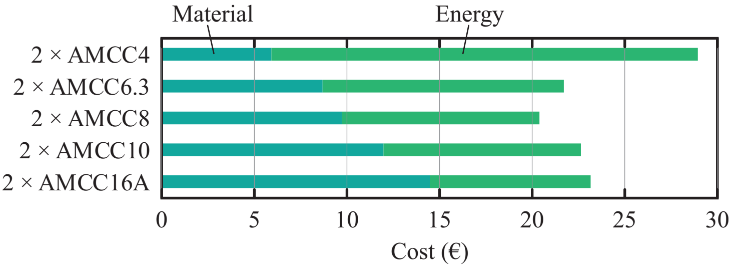


Fig. 2.27: Material- and energy cost trade-off for the boost inductors of the three-phase three-level rectifier built in this work for five different amorphous cut cores.

2.5 Summary of the Chapter

It is shown that the calculation of skin- and proximity losses in windings can be greatly simplified using two asymptotic approximations for LF and HF range. The error introduced compared to the exact solution is always positive and occurs only for conductor dimensions close to two times the skin depth which should be avoided anyway since conductor dimensions in that range maximize the winding AC resistance.

In the LF range the proximity losses of a winding increase with the square of the product of winding width, operating frequency and conductor dimension (strand diameter or foil thickness). For transformers, which are usually operated in LF range, it is shown that an optimum operating frequency can be derived from this rule which appears at $\frac{R_{\mathrm{ac}}}{R_{\mathrm{dc}}} = \frac{\beta}{\alpha}$ and can be analytically expressed. This optimum operating frequency is inversely proportional to the winding width and may not be realisable for small transformers because of the semiconductor switching losses, however for large transformers it places an upper limit to the desired semiconductor switching frequency. In addition to the operating frequency also the number of turns of a transformer need to be to the optimum value which appears if the ratio of core- to winding losses equals $\frac{2}{\beta}$ and can be expressed analytically as well.

On the contrary no optimum operating frequency exists for CCM inductor. Since, assuming a particular core with a certain number of turns, higher operating frequency leads to lower core losses (as long as $\beta > \alpha$) and to lower winding losses due to the reduced current ripple. However, the inductance and the number of turns of an inductor both need to be optimized. It is shown that the optimum inductance depends on the volume of the core, resulting in a loss minimum at low inductance and high ripple for high power density designs.

3

Vienna Rectifier with High Peak-to-Average Load Ratio

Power supplies of X-ray systems can be designed to take advantage of the relatively low average power but also need to handle the peak-power. The specifications of the three-phase rectifier prototype constructed within this work define 65 kW peak-power but only 800 W average power. Two typical load profiles as shown in Fig. 3.1 are specified for the rectifier output. The single-shot mode shown in Fig. 3.1a is used to capture one image, releasing the maximum permissible amount of energy to the tube. The pulse duration at 65 kW is thus 2.3 s. After that the tube needs to cool down for approximately three minutes. The other mode, pulsed fluoroscopy, shown in in Fig. 3.1b is used to capture live X-ray video during surgery and is therefore used continuously. The pulse power is 12 kW for 2 ms with 30 ms repetition time. For the design and optimization of the prototype it is assumed that the utilization of the two modes is equal. Since, the average power of both modes is only 800 W the number of full-load operating hours is low.

For the rectifier prototype the Vienna Rectifier (VR) topology is selected since it allows the use of 600 V semiconductors with 800 V DC-link voltage. Therefore, offering high switching frequency and three-levels using low-cost components. Since the circuit is only unidirectional a Discontinuous Conduction Mode (DCM) exists. Due to the low number of full-load operating hours the total cost of ownership optimization of the boost inductors leads to a high power density design with small inductance value and high current ripple. Therefore, the DCM is entered already at relatively high power levels, i.e. at 20 % of nominal power.

This chapter comprises a review of the different VR topologies in

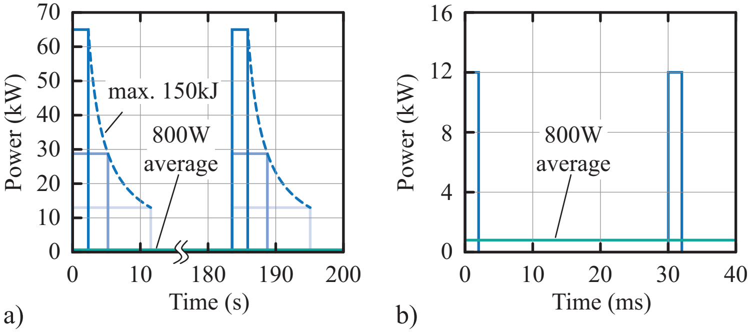


Fig. 3.1: Typical load patterns the rectifier of the X-ray system needs to supply. (a) Single-shot mode, (b) pulsed fluoroscopy.

Sec. 3.1 and a summary of operating limits and control in Continuous Conduction Mode (CCM) in Sec. 3.2. In Sec. 3.3 the control scheme for operation in DCM is introduced, which is particularly useful for the given but also other high peak-to-average load ratio applications. A step-by-step procedure for the design of the EMI filter is provided in Sec. 3.4, covering also the implications of the DCM control scheme. Finally, measurements of load steps, efficiency and EMI noise emission of the prototype are provided in Sec. 3.5.

3.1 Circuit Variants

The so-called Vienna rectifier is a three-phase, three-level PFC rectifier originally proposed in [36]. It is distinguished from other three-phase three-level topologies mainly by its unidirectional circuit, allowing to get along with a minimum of only three active switches. There are three main variants of the circuit, all having in common a split DC-link and three identical bridge legs. The AC terminal of each bridge leg can be controlled to connect to the DC-link midpoint or, depending on the current direction, to the positive or negative DC-link rail. Employing Pulse Width Modulation (PWM) modulation the switching period (local) average voltage at each bridge leg is adjusted to control the currents in the three boost inductors to sinusoidal reference values.

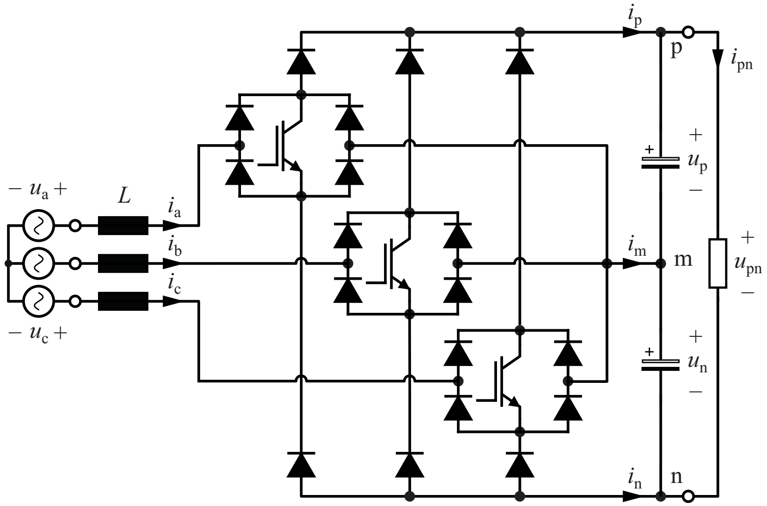


Fig. 3.2: Three-switch circuit variant of the VR. Together with four diodes each unidirectional switch forms a bidirectional switch facilitating midpoint connection if turned on.

3.1.1 Three-Switch Topology

The circuit, as shown in Fig. 3.2, employs only three transistors. Each transistor forms a bidirectional switch using four rectifier diodes which are only commutating with mains frequency. Because of the low commutation frequency of the rectifier diodes, low-cost, low forward voltage drop devices can be used [37]. While the switch of a bridge leg is turned on the according boost inductor is connected to the DC-link midpoint M via two of the four rectifier diodes. While the switch is turned off, the current still flows through one of the rectifier diodes and through one of the free-wheeling diodes into the positive (P) or negative (N) rail of the DC-link, depending on the current direction. All semiconductors are only subjected to half the DC-link voltage and by replacing at least one in each group of four rectifier diodes by a thyristor a DC-link precharging circuit can be integrated [38]. Using only three switches and gate driver circuits is the main advantage of this variant. The disadvantages are that there are three elements in the conduction path when the current is flowing into the midpoint and that the switching frequency commutation loop also includes the stray inductance of three elements.

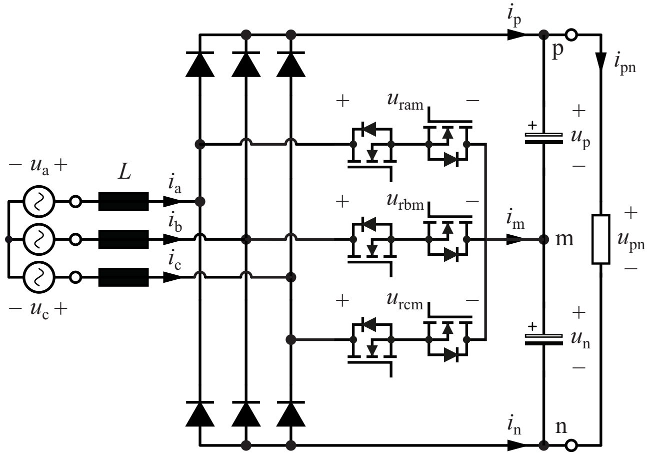


Fig. 3.3: T-type circuit variant of the VR using three bidirectional switches to facilitate the midpoint connection.

3.1.2 T-Type Topology

The T-type circuit variant of the VR as shown in Fig. 3.3 minimizes the total number of semiconductors and reduces the conduction loss by allowing the current to reach the positive and negative DC-link rail through only one element. The midpoint connection is realized using two series connected switches forming the bidirectional switch. The switches are only subjected to half the DC-link voltage while the diodes need to block the full DC-link voltage. Silicon PiN diodes that are able to block the full DC-link voltage typically release unacceptably high reverse recovery charge and would generate high turn-on losses in the switches. Therefore, Silicon Carbide (SiC) Schottky-barrier diodes in combination with Metal Oxide Semiconductor Field Effect Transistor (MOSFET)s or bidirectional IGBTs [39] are the preferred choice. For that reason a pre-charging circuit using a thyristor cannot be integrated.

3.1.3 Neutral Point Clamped Topology

The Neutral Point Clamped (NPC) circuit variant of the VR as shown in Fig. 3.4 is similar to the classic NPC three-level inverter structure. Six mains frequency commutating rectifier diodes conduct the positive

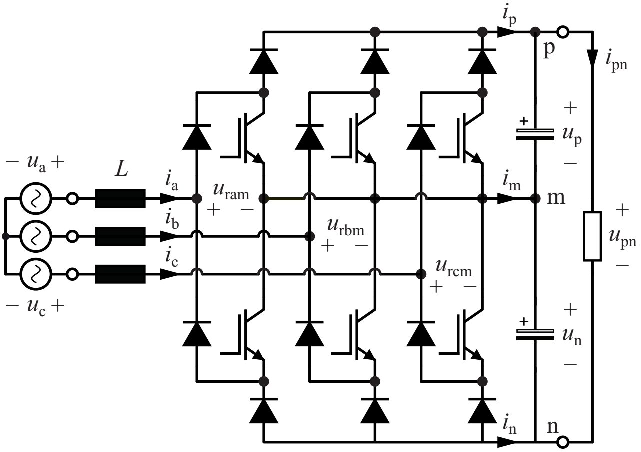


Fig. 3.4: NPC circuit variant of the VR with six mains frequency commutating rectifier diodes and three positive and three negative switching frequency commutating boost stages.

mains currents to the boost stages connected to the positive half of the DC-link and the negative mains currents to three boost stages connected to the negative half of the DC-link. Switching frequency commutation only occurs within the boost stages with only two semiconductors included in each commutation loop, allowing a simple Printed Circuit Board (PCB) or power module layout. All elements only need to block half the DC-link voltage and by replacing half of the rectifier diodes with thyristors DC-link pre-charging can be integrated. Compared to the three-switch variant there are only two semiconductors in the conduction path per phase, typically reducing conduction loss. Due to these practical advantages the NPC variant is selected for the VR constructed in this work.

3.2 Continuous Conduction Mode

At high power levels the boost inductor current i_k of each phase k only contains a small amount of ripple. The direction of each boost inductor current, therefore, remains constant throughout the switching period - except for narrow intervals around the current zero crossings. With the directions of the boost inductor currents known from measurements, the local average values $\langle u_{\mathrm{r}k\mathrm{m}} \rangle$ of the rectifier input voltages $u_{\mathrm{r}k\mathrm{m}}$ can be set directly via the duty cycles of the switches. Using closed-loop control sinusoidal boost inductor currents are maintained.

3.2.1 Space Vector Diagram

Space vectors are often used aiming for better understanding of relationships in three-phase systems when the zero component is not relevant. Using space vector representations of the rectifier input voltages for all possible switching states the limits of amplitude and phase shift of the rectifier AC input voltage are derived in the following.

A space vector is a linear transformation of three corresponding phase quantities (a,b,c), voltage or current, to a two-dimensional α,β plane. With $\underline{a} = \exp(j\frac{2\pi}{3})$ the mains voltages are transformed into the space vector

$$\underline{u} = u_\alpha + ju_\beta = \frac{2}{3}(u_\mathrm{a} + \underline{a}u_\mathrm{b} + \underline{a}^2 u_\mathrm{c}), \tag{3.1}$$

and the rectifier input voltages at the AC terminals of the bridge legs into the space vector

$$\underline{u}_\mathrm{r} = u_{\mathrm{r}\alpha} + ju_{\mathrm{r}\beta} = \frac{2}{3}(u_\mathrm{ram} + \underline{a}u_\mathrm{rbm} + \underline{a}^2 u_\mathrm{rcm}), \tag{3.2}$$

and the boost inductor currents into the space vector

$$\underline{i} = i_\alpha + ji_\beta = \frac{2}{3}(i_\mathrm{a} + \underline{a}i_\mathrm{b} + \underline{a}^2 i_\mathrm{c}). \tag{3.3}$$

Three-Level Inverter

The possible voltage space vectors that the VR rectifier is able to apply at its input terminals for all switching states can be derived from the general voltage space vector diagram of a three-level three-phase inverter as shown in Fig. 3.5. In total $3^3 = 27$ different switching states are available, each phase leg may switch between positive rail P, midpoint M and negative rail N. Due to redundant switching states producing the same voltage space vectors 19 different voltage space vectors can be applied.

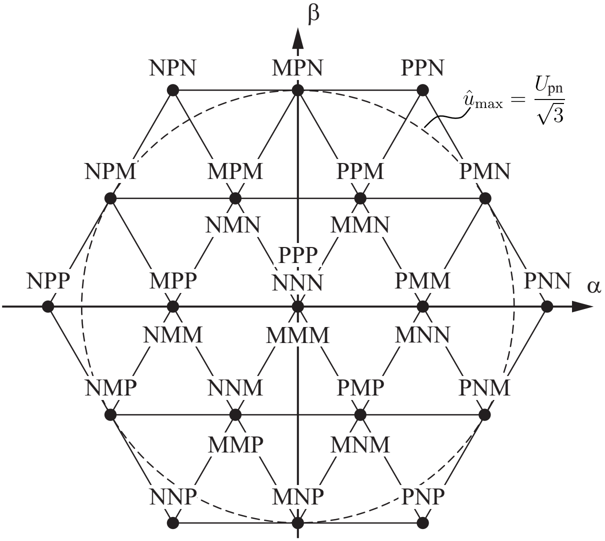

β
α
NPN
MPN
PPN
$\hat{u}_{\max} = \frac{U_{\mathrm{pn}}}{\sqrt{3}}$
NPM
MPM
PPM
PMN
NMN
MMN
PPP
NNN
NPP
MPP
PMM
PNN
NMM
MMM
MNN
NMP
NNM
PMP
PNM
MMP
MNM
NNP
MNP
PNP

Fig. 3.5: General voltage space vector diagram of a three-level three-phase inverter. The switching states describe the switching states of the three phases, each being either P for positive rail, M for midpoint and N for negative rail of the DC-link.

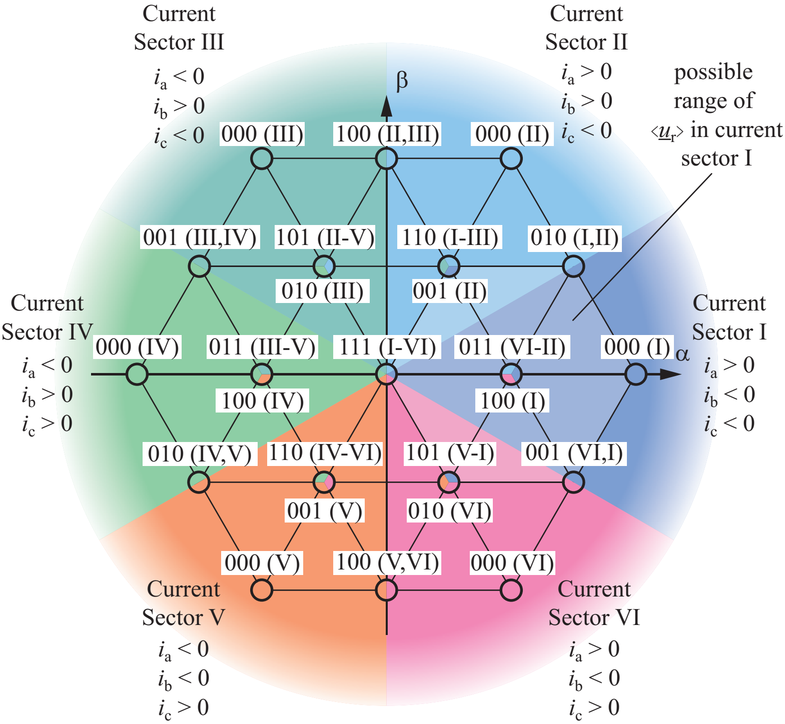

Current
Sector III
$i_a < 0$
$i_b > 0$
$i_c < 0$
Current
Sector II
$i_a > 0$
$i_b > 0$
$i_c < 0$
possible range of $\langle \underline{u}_r \rangle$ in current sector I
β
α
000 (III)
100 (II,III)
000 (II)
001 (III,IV)
101 (II-V)
110 (I-III)
010 (I,II)
010 (III)
001 (II)
Current
Sector IV
$i_a < 0$
$i_b > 0$
$i_c > 0$
000 (IV)
011 (III-V)
111 (I-VI)
011 (VI-II)
000 (I)
Current
Sector I
$i_a > 0$
$i_b < 0$
$i_c < 0$
100 (IV)
100 (I)
010 (IV,V)
110 (IV-VI)
101 (V-I)
001 (VI,I)
001 (V)
010 (VI)
000 (V)
100 (V,VI)
000 (VI)
Current
Sector V
$i_a < 0$
$i_b < 0$
$i_c > 0$
Current
Sector VI
$i_a > 0$
$i_b < 0$
$i_c > 0$

Fig. 3.6: Available rectifier voltage space vectors $\underline{u}_r$ of the VR depending on the sector (I-VI) the boost inductor space vector $\underline{i}$ is located in.

Vienna Rectifier

Whereas a three-level three-phase inverter is able to apply any of the 19 voltage space vectors at any time, the available voltage space vectors of the VR depend on the directions of the phase currents. Instead of three states P,M and N each phase leg can only apply two different states: P or M for positive and M or N for negative currents. The six different combinations of phase current directions partition the α, β current plane into six sectors. For each of these sectors the state of each phase leg can be either on (1), i.e. connected to the midpoint or off (0), i.e. positive current flows to P, negative to N, resulting in $2^3 = 8$ switching states. As shown in Fig. 3.6 the eight switching states of each sector result in seven different voltage space vectors, one switching state always being redundant.

The seven available voltage space vectors within each current sector are located at the corners and in the center of a hexagon. By applying combinations of the space vectors during one switching period, any local average of the rectifier voltage space vector inside the hexagon can be generated. In order to minimize the current ripple it is advantageous to generate the local average of the rectifier input voltage using only the three closest voltage space vectors located at the corners of the triangle that encloses the desired rectifier input voltage local average value. If the rectifier voltage space vector $\underline{u}_r$ is in phase with the boost inductor current space vector $\underline{i}$ this is always possible since the hexagons of two neighbouring current sectors are overlapping. Therefore, all 27 voltage space vectors of the general three-level space vector diagram are available in the course of one mains period.

Since there are more voltage space vectors (27) than switching states (8), only voltage space vectors with the same color as the currently prevailing current space vector sector are available (Fig. 3.6). After a transition from one current sector to the next, the voltage space vectors assigned to four of the eight switching states change while the other four switching states still generate the same voltage space vectors as in the current sector before. Consider the case of a sector transition from I to II. While the switching state 011 generates the same voltage space vector in both current sectors the redundant switching state 100 generates two different voltage space vectors. This can be critical in applications with high current ripple, since at a current sector boundary the ripple leads to sector transitions during one switching period.

Vienna Rectifier Modulation Limit

The outer hexagon with the switching state 000 defining its corners spans the maximum range of the rectifier input voltage local average space vector $\langle \underline{u}_\mathrm{r} \rangle$. The maximum PWM phase voltage amplitude $\hat{u}_\mathrm{max}$ equals the radius of the largest circle contained by that range (see Fig. 3.5) which equals

$$\hat{u}_\mathrm{max} = \frac{U_\mathrm{pn}}{\sqrt{3}} \tag{3.4}$$

with the total DC-link voltage U_pn.

Vienna Rectifier Phase Shift Limit

Since two of the seven voltage space vectors are located ±30° outside the according 60° current sector it is possible to operate the VR with up to $-30° < \varphi < 30°$ phase shift between boost inductor current and rectifier voltage space vectors. However, as the rectifier input voltage amplitude $\hat{u}_\mathrm{r}$ approaches its maximum value $\frac{U_\mathrm{pn}}{\sqrt{3}}$ the maximum phase shift decreases until it reaches zero at the maximum possible rectifier input voltage amplitude. Using the modulation index

$$M = \frac{2\hat{u}_\mathrm{r}}{U_\mathrm{pn}}, \tag{3.5}$$

the maximum phase shift (radian measure) between rectifier voltage and boost inductor current

$$|\varphi|_\mathrm{max} < \begin{cases} \frac{\pi}{6} & \text{if } M \leq \frac{2}{3} \\ \frac{\pi}{3} - \arccos\left(\frac{1}{\sqrt{3}M}\right) & \text{if } M > \frac{2}{3} \end{cases} \tag{3.6}$$

can be derived. In practice the ability of the VR to operate with non-zero phase shift, i.e. to generate or consume reactive power, is of minor interest since the DC-link voltage is usually selected as small as possible to be able to use semiconductors with best conduction and switching properties. Therefore, the modulation index typically reaches high values up to 1.08 (480 V mains with 10 % over-voltage and 800 V DC-link voltage) allowing a maximum phase shift of only 2.3°.

3.2.2 Output Voltage Control

The control objective is to maintain a stable DC voltage at the output side of the rectifier and to emulate a symmetric resistive load to the

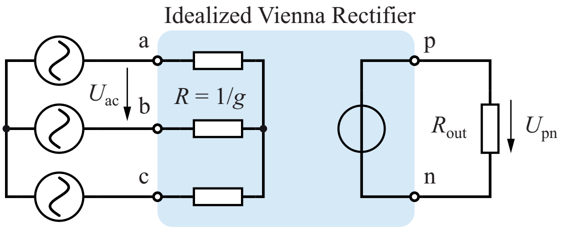

Idealized Vienna Rectifier
a
b
c
p
n
U_{ac}
$R = 1/g$
R_{out}
U_{pn}

Fig. 3.7: Idealized equivalent circuit of the rectifier.

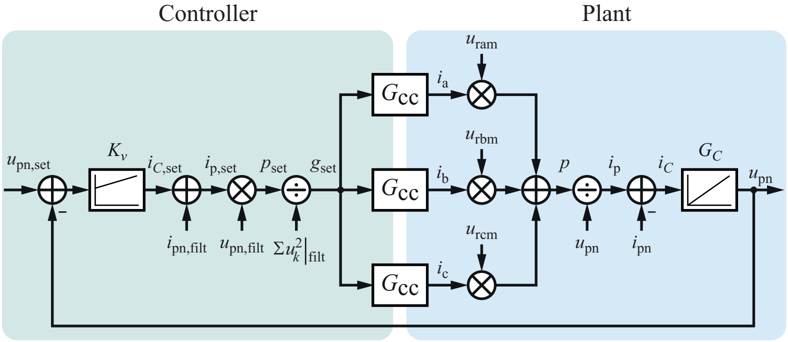

Controller
Plant
$u_{\mathrm{pn,set}}$
K_v
$i_{C,\mathrm{set}}$
$i_{\mathrm{p,set}}$
p_{set}
g_{set}
$i_{\mathrm{pn,filt}}$
$u_{\mathrm{pn,filt}}$
$\Sigma u_k^2|_{\mathrm{filt}}$
G_{CC}
G_{CC}
G_{CC}
i_{a}
i_{b}
i_{c}
u_{ram}
u_{rbm}
u_{rcm}
p
i_{p}
i_C
G_C
u_{pn}
u_{pn}
i_{pn}
−
−

Fig. 3.8: Voltage control loop.

grid at the input side (Fig. 3.7). The actual controller is realized as cascaded control, split in a governing voltage controller that specifies the emulated input resistance or rather its inverse, the conductivity g in order to maintain constant DC-link voltage. The input current controllers derive the phase current set values,

$$i_{k,\mathrm{set}} = g \cdot u_k, \tag{3.7}$$

for each phase k from the conductivity g and the phase voltage u_k. The structure of the voltage control loop is shown in Fig. 3.8. The voltage controller itself sets the current $i_{C,\mathrm{set}}$ which is to be injected into the series connection of the two DC-link capacitors, each with a capacitance of C. Using the low-pass filtered measurement of the output current $i_{\mathrm{dc,filt}}$, the set value of the power that has to be supplied by the rectifier and the resulting conductivity which has to be applied to the grid, g_{set}, are calculated. A PI-type voltage controller is selected to eliminate

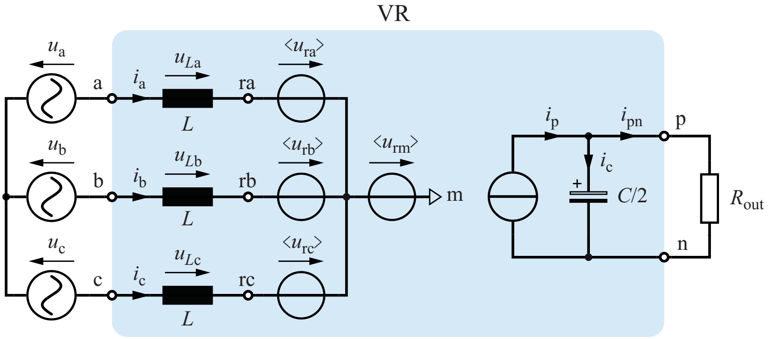


Fig. 3.9: Control equivalent circuit schematic of the Vienna Rectifier

steady state output voltage error.

3.2.3 Input Current Control

In order to simplify the analysis the input side of the rectifier is replaced by a set of controllable voltage sources representing the local average values of the rectifier input voltages. At the output side a current source i_p is feeding the series connection of the two DC-link capacitors C (Fig. 3.9). The local average values of the rectifier input voltages $\langle u_{\mathrm{r}k\mathrm{m}} \rangle$ can be split into the CM component

$$\langle u_\mathrm{rm} \rangle = \frac{\langle u_\mathrm{ram} \rangle + \langle u_\mathrm{rbm} \rangle + \langle u_\mathrm{rcm} \rangle}{3} \tag{3.8}$$

and the DM components

$$\begin{aligned} \langle u_\mathrm{ra} \rangle &= \langle u_\mathrm{ram} \rangle - \langle u_\mathrm{rm} \rangle && (3.9) \\ \langle u_\mathrm{rb} \rangle &= \langle u_\mathrm{rbm} \rangle - \langle u_\mathrm{rm} \rangle && (3.10) \\ \langle u_\mathrm{rc} \rangle &= \langle u_\mathrm{rcm} \rangle - \langle u_\mathrm{rm} \rangle. && (3.11) \end{aligned}$$

Since $\langle u_\mathrm{ra} \rangle + \langle u_\mathrm{rb} \rangle + \langle u_\mathrm{rc} \rangle = 0$ and also $u_\mathrm{a} + u_\mathrm{b} + u_\mathrm{c} = 0$ the voltages which are applied at the boost inductors

$$u_{L\mathrm{k}} = u_k - \langle u_{\mathrm{r}k} \rangle \tag{3.12}$$

are only depending on elements of the according phase. Therefore, the current controller of each phase may be considered independently [40].

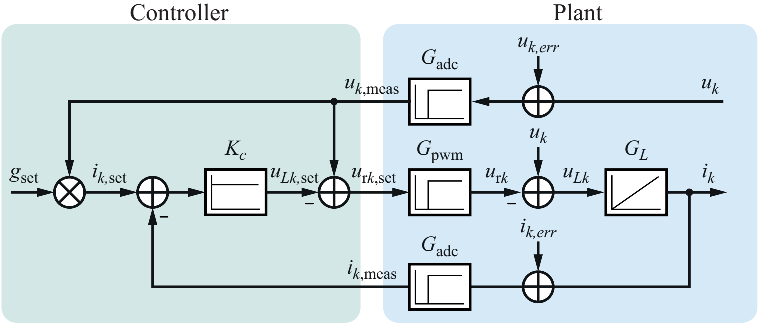

Controller
Plant
G_{adc}
$u_{k,err}$
$u_{k,\mathrm{meas}}$
u_k
K_c
G_{pwm}
u_k
G_L
g_{set}
$i_{k,\mathrm{set}}$
$u_{Lk,\mathrm{set}}$
$u_{\mathrm{r}k,\mathrm{set}}$
$u_{\mathrm{r}k}$
u_{Lk}
i_k
$-$
$-$
$-$
$i_{k,err}$
G_{adc}
$i_{k,\mathrm{meas}}$

Fig. 3.10: P current control loop for undamped input filters with band pass filtered input voltage feed-forward.

The local average of the rectifier input voltage CM component $\langle u_{\mathrm{rm}} \rangle$ is not employed in closed loop control since no LF CM current path exists and, therefore, no CM current control is required. The control loop of one phase current controller is shown in Fig. 3.10.

Plant Transfer Functions

The plant behaviour of the current control loop is mainly determined by the delays of PWM and Analog to Digital Converter (ADC) and by the inductance of the boost inductor. The PWM delay time T_{pwm} with triangular carriers equals half a switching period $T_{\mathrm{s}} = \frac{1}{f_{\mathrm{s}}}$. With synchronous sampling at the center of the switching period. The delay for measuring, T_{adc}, also amounts to half a switching period - including the time for calculating the new duty cycles and writing them into the shadow registers of the PWM unit of the Digital Signal Processor (DSP). The transfer functions for the delays are expressed as

$$G_{\mathrm{pwm}} = \mathrm{e}^{-sT_{\mathrm{pwm}}} \text{ and } G_{\mathrm{adc}} = \mathrm{e}^{-sT_{\mathrm{adc}}}. \tag{3.13}$$

The boost inductors are modelled as integrators with the transfer function

$$G_L = \frac{1}{sL}. \tag{3.14}$$

Since the current controller should be acting directly on the inductor the controller output is subtracted from the mains voltage, or rather the voltage at the first differential mode filter capacitor. This type of input voltage feed-forwarding requires that the input filter is equipped with damping resistors [41], otherwise filter oscillations could occur.

Controller Gain

The phase currents are controlled using simple proportional controllers as proposed in [40]. With a proportional controller gain of k_{pc} the loop transfer function is given as

$$K_c G_{\mathrm{pwm}} G_L G_{\mathrm{adc}} = k_{\mathrm{pc}} \mathrm{e}^{-s(T_{\mathrm{pwm}}+T_{\mathrm{adc}})} \frac{1}{sL}. \tag{3.15}$$

Assuming a desired phase-margin of the current controller of φ_{c}, the maximum current controller gain

$$k_{\mathrm{pc}} = \frac{L}{T_{\mathrm{pwm}} + T_{\mathrm{adc}}} \left(\frac{\pi}{2} - \varphi_{\mathrm{c}} \right) \tag{3.16}$$

can be directly calculated.

Step Response

With the assumed delays $T_{\mathrm{adc}} + T_{\mathrm{pwm}} = \frac{1}{f_{\mathrm{s}}}$ and a phase margin of $\varphi_{\mathrm{c}} = 60°$, i.e. a controller gain of $k_{\mathrm{pc}} = \frac{\pi f_{\mathrm{s}} L}{6}$, the reference step response of the current control loop exhibits $\approx 6\,\%$ overshoot as shown in Fig. 3.11a. Because of the integrating plant behaviour there is no steady-state error in the reference step. The 90 % rise-time of the current for this case is $\approx \frac{2.45}{f_{\mathrm{s}}}$. The rise-time of the reference step therefore only depends on the switching frequency or more accurately on the inherent delays T_{pwm} and T_{adc}. The response of the current to a step of the error in the measurement of the phase voltage $u_{k,\mathrm{err}}$ for the same situation is shown in Fig. 3.11b. Since only a proportional controller is used a steady-state error of $\Delta i_k = \frac{\Delta u_{k,\mathrm{err}}}{k_{\mathrm{pc}}}$ persists. Therefore, this current deviation due to the voltage measurement error is proportional to $T_{\mathrm{pwm}} + T_{\mathrm{adc}}$ and inversely proportional to the value of the boost inductance. Therefore, high current ripple and high delays both result in low disturbance rejection. Minimizing the delays is thus essential for low input current Total Harmonic Distortion (THD).

3.2.4 DC-Link Balancing

As shown in Sec. 3.2.3 the local average of the rectifier input voltage $\langle u_{\mathrm{r}k\mathrm{m}} \rangle$ of each phase can be split into a DM part $\langle u_{\mathrm{r}k} \rangle$ which is set by

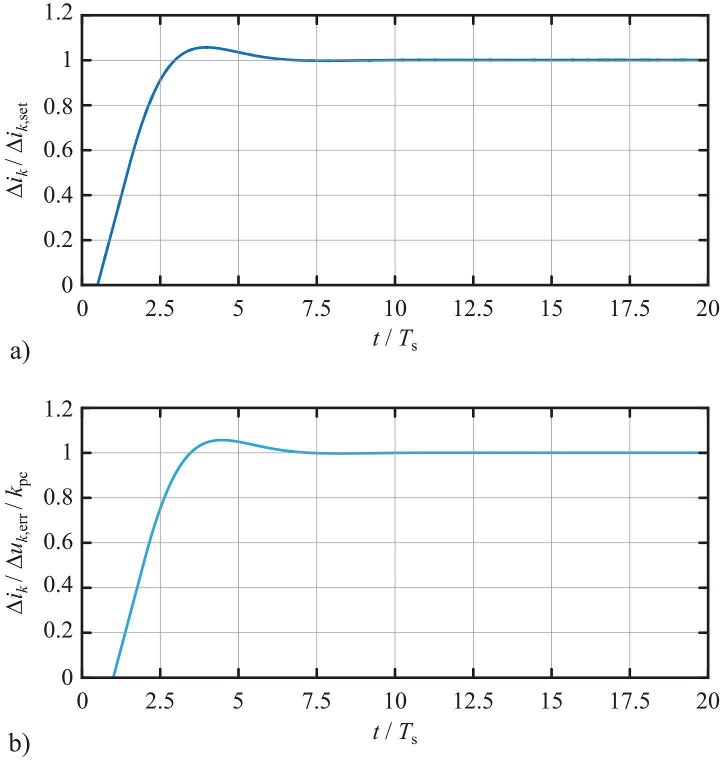


Fig. 3.11: Reference current step response (a) and phase voltage measurement error step response (b) of the current control loop with the proportional gain set to reach 60° phase margin.

the current controller and a CM part $\langle u_{\mathrm{rm}}\rangle$ which has no effect on the input currents, instead it affects the distribution of the power flow from the mains to the two parts of the DC-link and is, therefore, used to balance the DC-link voltages.

Common Mode Voltage Limits

The rectifier input CM voltage local average $\langle u_{\mathrm{rm}}\rangle$, referred to as CM voltage in this Section, is the offset of the virtual star point of the three rectifier input DM voltage local average values with respect to the midpoint of the DC-link. However, this CM voltage is limited since the rectifier input voltage local average value $\langle u_{\mathrm{r}k\mathrm{m}}\rangle$ of each phase k is limited between 0 and $\mathrm{sign}(i_{\mathrm{k}})\frac{U_{\mathrm{pn}}}{2}$. The CM voltage boundaries

$$u_{\mathrm{rm,max}} = \min\left(\frac{U_{\mathrm{pn}}}{4}(\mathrm{sign}(i_k)+1) - \langle u_{\mathrm{r}k}\rangle\right) \tag{3.17}$$

$$u_{\mathrm{rm,min}} = \max\left(\frac{U_{\mathrm{pn}}}{4}(\mathrm{sign}(i_k)-1) - \langle u_{\mathrm{r}k}\rangle\right) \tag{3.18}$$

respect the limits for all rectifier input DM voltage local average values set by the current controller and all boost inductor current directions. The resulting available range of the CM voltage is shown in Fig. 3.12a for $U_{\mathrm{ac}} = 400\,\mathrm{V}$, $U_{\mathrm{pn}} = 800\,\mathrm{V}$, $P = 65\,\mathrm{kW}$ and zero reactive power. It is shown that the CM voltage range reduces to a single point at each zero crossing of one of the inductor currents.

Midpoint Current Limits

The duty cycle, the relative on-time, of each switch k,

$$d_k = \left(1 - \frac{2|\langle u_{\mathrm{r}k\mathrm{m}}\rangle|}{U_{\mathrm{pn}}}\right), \tag{3.19}$$

represents the relative time interval with respect to the switching period when the current of the corresponding phase is flowing into the midpoint. Therefore, the midpoint current local average

$$\langle i_{\mathrm{m}}\rangle = -\frac{2}{U_{\mathrm{pn}}}\sum_k |\langle u_{\mathrm{r}k\mathrm{m}}\rangle| i_k \tag{3.20}$$

is obtained. While this expression also applies to the general three-level inverter with split DC-link, for the VR $\mathrm{sign}(\langle u_{\mathrm{r}k\mathrm{m}}\rangle) = \mathrm{sign}(i_k)$ is true if

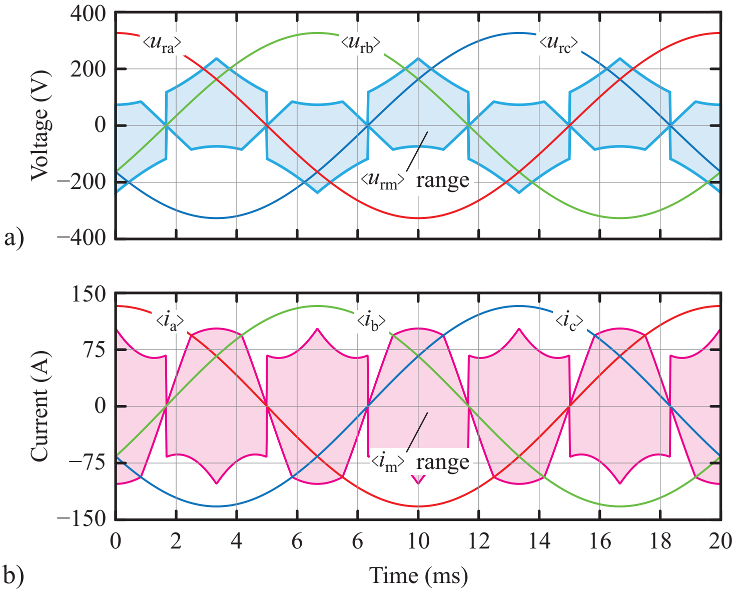


Fig. 3.12: Maximum range for setting the rectifier input CM voltage local average $\langle u_{\mathrm{rm}} \rangle$ (a) and resulting maximum range of the midpoint current local average $\langle i_{\mathrm{m}} \rangle$ (b) for $U_{\mathrm{ac}} = 400\,\mathrm{V}$, $U_{\mathrm{pn}} = 800\,\mathrm{V}$, $P = 65\,\mathrm{kW}$ and zero reactive power.

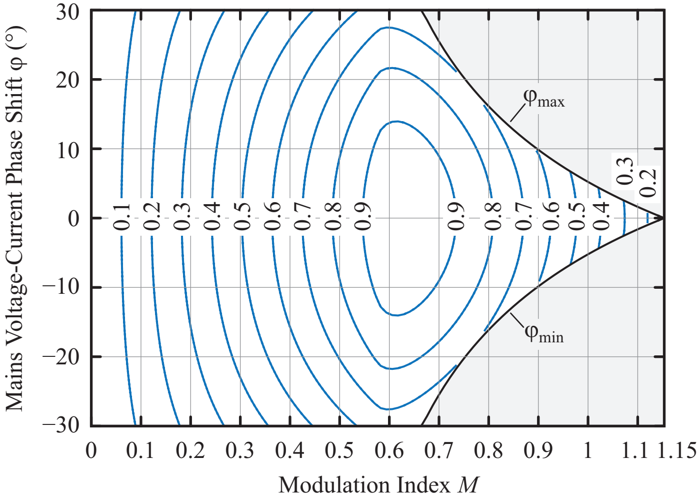


Fig. 3.13: Maximum average midpoint current during one mains period related to the phase current RMS value as function of rectifier input voltage phase shift φ with respect to the rectifier input current and modulation index M.

the rectifier input CM voltage local average limits (3.17) and (3.18) are met. In this case $|\langle u_{\mathrm{r}k\mathrm{m}}\rangle|i_k = \langle u_{\mathrm{r}k\mathrm{m}}\rangle|i_k|$ and thus (3.20) becomes

$$\langle i_{\mathrm{m}}\rangle = -\frac{2}{U_{\mathrm{pn}}}\sum_k(\langle u_{\mathrm{r}k}\rangle + \langle u_{\mathrm{rm}}\rangle)|i_k|. \tag{3.21}$$

Therefore, increasing the rectifier input CM voltage local average reduces the midpoint current local average. The available rectifier input CM voltage local average range of Fig. 3.12a translates into the midpoint current local average range shown in Fig. 3.12b. Since the midpoint current local average range at each zero crossing of one of the phase currents narrows down to zero a continuous non-zero current flow to the midpoint is not possible. However, on average through the mains period a midpoint current of any direction can be supplied to the midpoint. The value of this maximum average midpoint current depends on the modulation index and the phase shift between rectifier input voltage and current fundamentals and can only be calculated numerically as it is shown in Fig. 3.13 with the maximum average midpoint

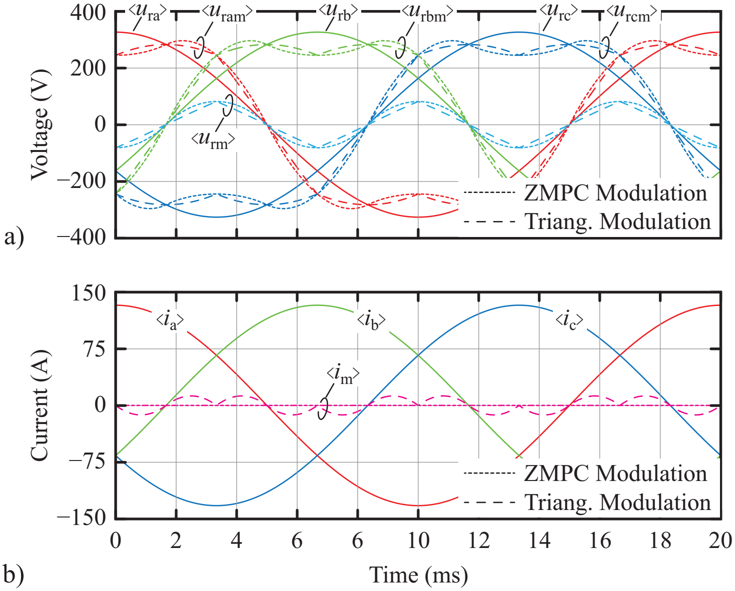


Fig. 3.14: Rectifier input voltage local average values (a) and rectifier input current local average values and midpoint current average values (b) for Zero Midpoint Current (ZMPC) modulation and triangular CM voltage modulation for $U_{ac} = 400\,\text{V}$, $U_{pn} = 800\,\text{V}$, $P = 65\,\text{kW}$ and zero reactive power.

current related to the phase RMS current.

In practice the maximum midpoint current that can be supplied to the DC-link is typically limited by the value reached at the highest modulation index. In a typical worst case of $M = 1.08$ (480 V mains with 10 % over-voltage and 800 V DC-link voltage) with $\varphi = \varphi_{max}$ the maximum midpoint current is still 21 % of the rectifier input current RMS value.

Zero Mipdpoint Current Modulation

In order to minimize the LF output voltage ripple it is desirable to reduce the LF-part of the midpoint current as much as possible. As shown in Fig. 3.12b it is possible to keep the midpoint current local average value at zero throughout the mains period if the rectifier input voltage-current phase shift is zero. The necessary value of the rectifier

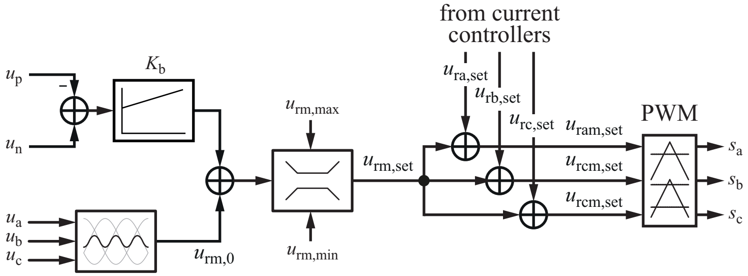

from current controllers
u_{p}
−
u_{n}
K_{b}
u_{a}
u_{b}
u_{c}
$u_{\mathrm{rm,0}}$
$u_{\mathrm{rm,max}}$
$u_{\mathrm{rm,min}}$
$u_{\mathrm{rm,set}}$
$u_{\mathrm{ra,set}}$
$u_{\mathrm{rb,set}}$
$u_{\mathrm{rc,set}}$
$u_{\mathrm{ram,set}}$
$u_{\mathrm{rcm,set}}$
$u_{\mathrm{rcm,set}}$
PWM
s_{a}
s_{b}
s_{c}

Fig. 3.15: DC-link balancing control loop.

input CM voltage local average

$$\langle u_{\mathrm{rm,0}} \rangle = -\frac{\sum_k \langle u_{\mathrm{r}k} \rangle |i_k|}{\sum_k |i_k|} \tag{3.22}$$

results from (3.21). It is assumed that the phase current i_k of each phase is proportional to the corresponding phase voltage and that the rectifier input DM voltage local average $\langle u_{\mathrm{r}k} \rangle$ approximately equals the corresponding phase voltage. If the phase voltages are sorted by their absolute values such that $|u_{\mathrm{max}}| > |u_{\mathrm{mid}}| > |u_{\mathrm{min}}|$ expression (3.22) can be further simplified to

$$\langle u_{\mathrm{rm,0}} \rangle = u_{\mathrm{min}} \left(\frac{u_{\mathrm{min}}}{u_{\mathrm{max}}} + 1 \right). \tag{3.23}$$

Using this Zero Midpoint Current (ZMPC) third harmonic injection function allows to reduce the LF output voltage ripple to zero. The function can be derived directly from the phase voltages and can therefore be used similar to the triangular third harmonic injection which simply uses half of the phase voltage with minimum absolute value as third harmonic injection function. The two ways of setting the rectifier input CM voltage local average are compared in Fig. 3.14, showing that the LF midpoint current is indeed eliminated using Zero Midpoint Current (ZMPC) modulation whereas with triangular CM voltage modulation a considerable LF midpoint current remains.

Balancing Control Loop

After the rectifier input voltage DM components are determined by the current controllers as shown in Sec. 3.2.3 and the rectifier input voltage

CM component is calculated for zero LF midpoint current according to (3.23) a few more steps remain. First, the difference between lower and upper DC-link voltage, $(u_\mathrm{n} - u_\mathrm{p})$, is fed into the balancing controller, which is usually of PI-type to avoid steady state offset. The output of the balancing controller is added to the CM voltage for zero midpoint current $\langle u_\mathrm{rm,0} \rangle$ and the result is capped by the limits $\langle u_\mathrm{rm,max} \rangle$,$\langle u_\mathrm{rm,min} \rangle$ according to (3.17) and (3.18). Finally, the capped result is added to the rectifier input voltage DM components as determined by the current controllers. The resulting rectifier input voltage set values now have to be translated to gate signals by the PWM unit. The signal flow is illustrated in Fig. 3.15. Capping the rectifier input CM voltage set value guarantees that, if the rectifier input DM voltages requested by the current controllers meet amplitude (3.4) and phase shift limit (3.6), the resulting rectifier input voltage set values can actually be generated by the PWM, i.e. $\mathrm{sign}(\langle u_{\mathrm{r}k\mathrm{m}} \rangle) = \mathrm{sign}(i_k)$.

3.2.5 Pulse Width Modulation

After the set values of DM and CM components of the rectifier input voltage local average values are determined the gate signals are generated. The PWM modulation of the three phases offers another degree of freedom - the phase shifts between the three carriers. Since the carrier phase shift has no effect on the local average values of rectifier input voltages or DC-link currents it is usually set to minimize the boost inductor current ripple.

Minimum Differential Mode Modulation

Fig. 3.16 shows the preferred way of generating the gate signals from two 180° phase shifted triangular carriers for the rectifier input voltage space vector local average $\langle \underline{u}_r \rangle$ shown in the space vector diagram in Fig. 3.16a. The DM rectifier input voltage local average values $\langle u_{\mathrm{r}k} \rangle$ are calculated from the α,β components of the given space vector. The CM rectifier input voltage local average $\langle u_\mathrm{rm} \rangle$ is determined such that zero midpoint current results. Since the current space vector is in phase with the desired rectifier input voltage space vector (3.23) is used. The resulting rectifier input voltage local average values $\langle u_{\mathrm{r}k\mathrm{m}} \rangle$ are shown in Fig. 3.16b. The rectifier input voltage local average values are compared to two triangular carriers with a peak-to-peak value of half the DC-link

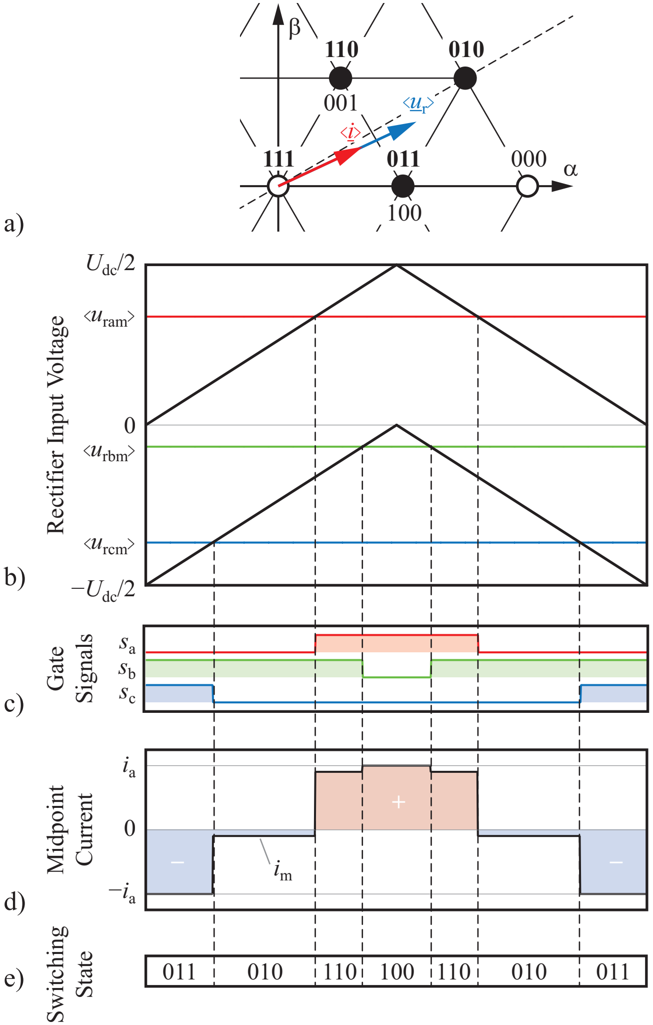

a)
β
110
010
001
⟨u_r⟩
⟨i⟩
111
011
000
α
100
b)
Rectifier Input Voltage
U_dc/2
⟨u_ram⟩
0
⟨u_rbm⟩
⟨u_rcm⟩
−U_dc/2
c)
Gate Signals
s_a
s_b
s_c
d)
Midpoint Current
i_a
0
−i_a
+
−
i_m
e)
Switching State
011
010
110
100
110
010
011

Fig. 3.16: PWM generation of the VR in CCM with 180° phase shifted carriers for positive and negative rectifier input voltages.

voltage each. While the local average value of a rectifier input voltage is less than the upper triangular carrier and greater than the lower triangular carrier, the corresponding switch is turned on (Fig. 3.16c). The switching states resulting from this modulation scheme are shown in Fig. 3.16e, showing that only the three closest voltage space vectors are employed with each vector being applied twice per switching period. This type of modulation, therefore, minimizes the DM current ripple. The state of each switch is always inverted at the center of the switching period compared to the state at the begin of the switching period. Therefore, the switching period always starts at one of the voltage space vectors with two redundant switching states, using one of the two states at the beginning and the end and the other at the middle of the switching period. Between these two redundant switching states a maximum of two more states is applied. Since these two additional states can only differ in one bit compared to one of the two redundant states and compared to each other it is guaranteed that only the closest three space vectors are employed (compare Fig. 3.6).

If the rectifier input CM voltage local average $\langle u_{\mathrm{rm}} \rangle$ is reduced, all rectifier input voltage local average values $\langle u_{\mathrm{r}k\mathrm{m}} \rangle$ are reduced by the same amount. As it becomes clear from Fig. 3.16b this does not affect the duration of the switching states 010 and 110 in the given example, but it increases the duration of the redundant switching state 100 while reducing the duration of the other redundant switching state 011 at the same time. During the redundant switching states the midpoint current equals

$$|i_{\mathrm{m}}| = \max(|i_k|) \tag{3.24}$$

with the sign being different for the two redundant switching states (compare Fig. 3.6). Therefore, reducing the rectifier input CM voltage local average $\langle u_{\mathrm{rm}} \rangle$ increases the midpoint current.

Minimum Common Mode Modulation

With two 180° phase shifted triangular carriers the High-Frequency HF CM component of the rectifier input voltages is maximized and thus the HF DM components of the rectifier input voltages are minimized. By using synchronized carriers for all three phases the opposite, i.e. minimum CM and maximum DM HF components of the rectifier input voltages results. This is shown in Fig. 3.17. The switching period now always starts and ends with switching state 000. At the middle of the

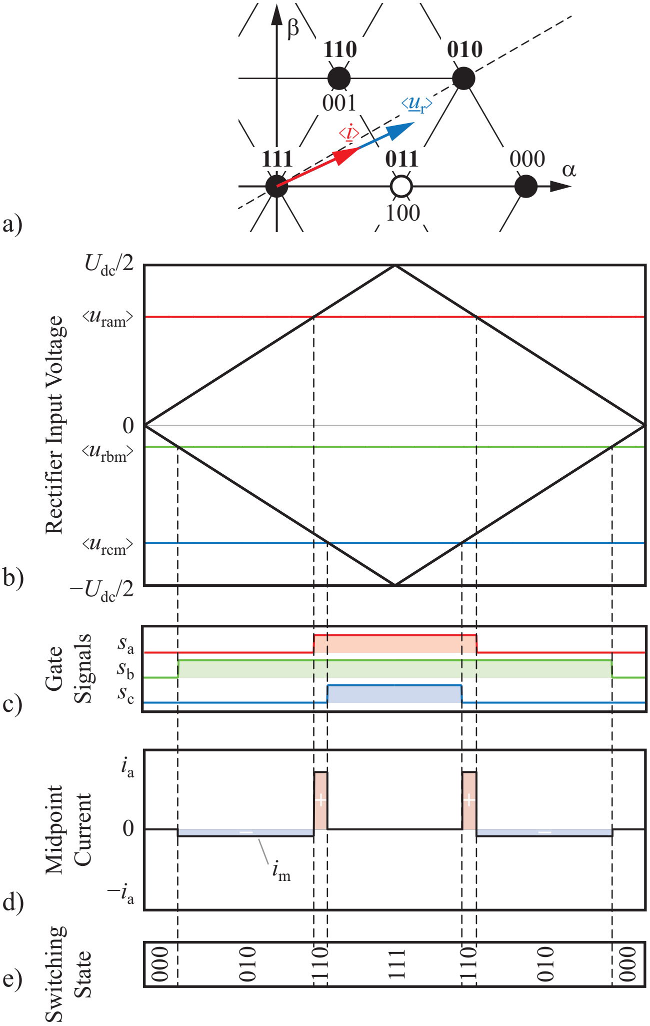

a)
β
110
010
001
⟨u_r⟩
⟨i⟩
111
011
000
α
100
b)
Rectifier Input Voltage
U_dc/2
⟨u_ram⟩
0
⟨u_rbm⟩
⟨u_rcm⟩
−U_dc/2
c)
Gate Signals
s_a
s_b
s_c
d)
Midpoint Current
i_a
0
−i_a
+
−
i_m
e)
Switching State
000
010
110
111
110
010
000

Fig. 3.17: PWM generation of the VR in CCM with synchronized carriers.

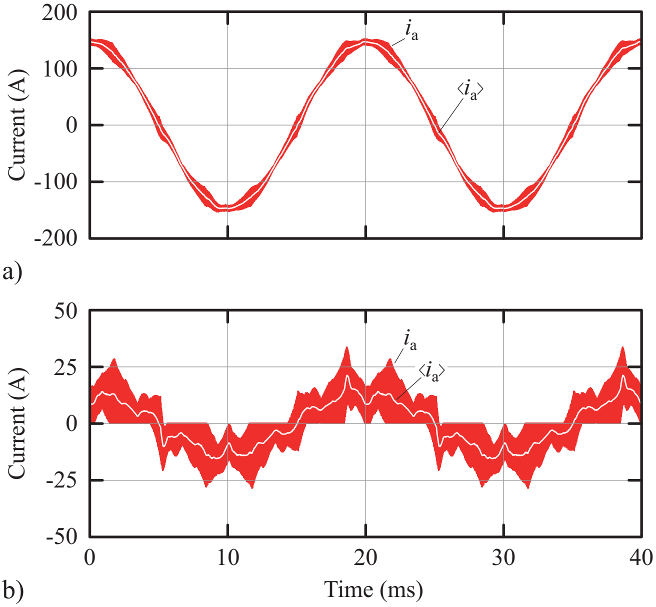


Fig. 3.18: Simulated current in one of the boost inductors of the VR and its local average with 400 V RMS line-to-line input voltage, 800 V DC output voltage, 50 µH boost inductance per phase, 28 kHz switching frequency and 65 kW output power (a). Reducing the power to 6.5 kW (b) results in a distorted shape of the local average due to DCM.

switching period switching state 111 is always set. This way the rectifier input voltage local average space vector is not composed of the closed available space vectors (Fig. 3.17a,e) and unnecessary current ripple in the boost inductors results. However, the HF-part of the midpoint current (Fig. 3.17d) is considerably reduced compared to minimum DM modulation, while its local average is not affected.

3.3 Discontinuous Conduction Mode

Unidirectional converter systems such as the VR exhibit a Discontinuous Conduction Mode (DCM) at light load, i.e. when the input current local average value is less than the ripple amplitude. With high power density, as resulting from the TCO optimization [42] of the system, also the loss densities in core and winding of the boost inductors are high, and therefore the HF flux density amplitude is high. The high HF flux density results in a relatively high current ripple of $\frac{\Delta i}{i} \approx 25\,\%$ for the considered system. In Fig. 3.18a the inductor current and its local average are shown for 65 kW load; the relative current ripple is in the range of 25 % in this case. At 6.5 kW, which is considered light load, the absolute inductor current ripple is still the same but the relative peak-to-peak inductor current ripple is already $> 200\,\%$ as shown in Fig. 3.18b. Therefore, DCM occurs and the current measurement which relies on synchronous sampling becomes inaccurate and the relationship between duty cycle of the switch and average rectifier input voltage is changed. As a result, the local average of the current waveform is no longer sinusoidal. Solutions to this problem for single-phase rectifiers exist [43], however they can not be directly applied to the VR due to the coupling of the three phases.

Two control schemes to operate the VR in DCM are already known. In the first control scheme [44] all switches are turned on and off at the same time (single-switch rectifier control scheme, [45]). The currents have approximately triangular shape but their local average value is not varying sinusoidally. However, the control is simple because the duty cycle is directly set by the output voltage controller and no current sensors are required. Furthermore, the switch that carries the highest current can be turned off a little earlier or later than the other two switches. This allows to actively balance the DC-link voltages.

The second solution, proposed in [46], extends the DCM control loop by an adaptive compensator. The currents in the boost inductors are modeled using an observer and compared to the measured values. The error of the local average of each current is then fed into a PI-controller, whose integral part is inverted at each zero crossing of the according phase voltage. This way the error voltage of each phase, which is the difference between the voltage set according to the duty cycle and the actually applied voltage because of current discontinuity, can be compensated. However, after a load step the controller takes considerable time, approximately 10 ms, to adapt to the new error voltages. Furthermore, the control scheme relies on current measurements during DCM control, which are not as easy to obtain as in CCM, since the time when the instantaneous value of the current equals its local average is not known in advance. However, it offers the advantage that no change between different control schemes occurs throughout the whole power range.

A control scheme that prevents input current distortion at light load based on the exact analytic solution for the duty cycles of the VR in DCM is presented in the following. Aiming for a better understanding of the behaviour of the VR in DCM space vector representations for voltages and currents can be used [45]. For the following considerations a switching period at a mains voltage angle of $\varphi = 10\,°$ of a symmetric three-phase system with $u_\mathrm{a} = \hat{u}\cos(\varphi)$, $u_\mathrm{b} = \hat{u}\cos(\varphi - \frac{2\pi}{3})$, $u_\mathrm{c} = \hat{u}\cos(\varphi - \frac{4\pi}{3})$ is considered. The values of the mains voltages, which are assumed to be constant during the switching period, therefore satisfy the condition $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$. It is also assumed that at the start of the switching period $T_\mathrm{s} = \frac{1}{f_\mathrm{s}}$ the boost inductor currents are zero.

3.3.1 Synchronous Switching DCM

One option to control the VR in DCM is to operate all switches synchronously, i.e. to turn them on and off at the same time setting the duty cycle such that the required power is transferred into the DC-link. However, this operating principle results in non-sinusoidal input currents as can be easily shown using space vector representation. After turning on all switches at $t = 0$ each current is rising at a rate proportional to its according phase voltage, as shown in interval $\boxed{1}$ in Fig. 3.19a. The space vector representation of this interval shown in Fig. 3.19b reveals that according to

$$\frac{\mathrm{d}\underline{i}}{\mathrm{dt}} = \frac{1}{L}(\underline{u} - \underline{u}_\mathrm{r}) \tag{3.25}$$

the current space vector is moving along the indicated trajectory $\boxed{1}$ in the direction of the mains voltage space vector, since the rectifier voltage space vector $\underline{u}_\mathrm{r}(111)$ is zero. After turning off all switches at the same time, the phase currents commutate to the free-wheeling diodes and thus during this interval $\boxed{3}$ all phase currents are decreasing. The voltage space vector applied to the boost inductors now is the difference between the rectifier voltage space vector $\underline{u}_\mathrm{r}(000)$, which is applied during this switching state, and the mains voltage space vector. The boost inductor current space vector therefore moves along the trajectory $\boxed{3}$ during this state. As soon as the phase current with the smallest absolute value (i_b) reaches zero, state $\boxed{4}$ is entered. Now, the differ-

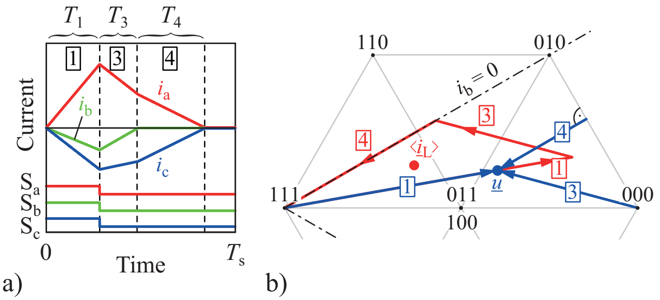


Fig. 3.19: Boost inductor currents during one switching period in DCM with synchronously operated switches while $u_a > 0 > u_b > u_c$ (a) and space vector representation of the same situation (b).

ence between the rectifier voltage space vector $\boxed{3}$ projected to the line $i_b = 0$ and the mains voltage space vector is applied to the boost inductors. The boost inductor current space vector moves along the line $i_b = 0$ until it reaches the origin where it remains until the end of the switching period. This investigation shows that, the local average of the boost inductor current with synchronous switching is located somewhere within the triangle $\boxed{1}$-$\boxed{3}$-$\boxed{4}$ which is aligned with the mains voltage space vector with one side. Therefore, the local average of the boost inductor current space vector is generally not in phase with the mains voltage space vector. Since the phase shift between the mains voltage space vector and the local average of the boost inductor current space vector varies throughout the mains period, taking positive and negative values, a non-sinusoidal shape of the input current is observed with synchronously controlled switches. This is confirmed by the simulated waveform shown in Fig. 3.20.

3.3.2 Proposed Sinusoidal Current DCM Pattern A

In order to achieve sinusoidal input currents, the phase shift between the local average of the boost inductor current space vector and the mains voltage has to be constant throughout the mains period. Achieving zero phase shift, i.e. resistive mains behaviour, is intended in the following. For zero phase shift in the considered example an additional voltage space vector has to be applied as shown in Fig. 3.21b. Turning off the switch of phase c earlier than the others, inserts the state

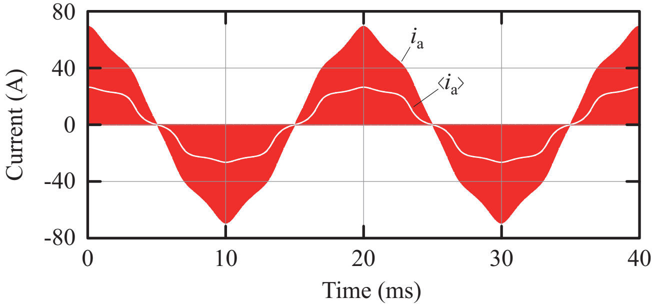


Fig. 3.20: Simulated boost inductor current of one phase and its local average value in DCM with synchronously operated switches. Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2} \cdot 230\,\mathrm{V}$, $U_{\mathrm{pn}} = 800\,\mathrm{V}$, $P = 13\,\mathrm{kW}$, $f_{\mathrm{s}} = 28\,\mathrm{kHz}$, $L = 50\,\mu\mathrm{H}$.

$\boxed{\text{2A}}$ with the according voltage space vector that shifts the boost inductor current space vector into the appropriate direction to eliminate the phase shift between mains voltage and boost inductor current. The phase current waveforms during one switching period applying to this situation are shown in Fig. 3.21a and it can be observed that during state $\boxed{\text{2A}}$ the absolute value of the current of the phase with the smallest absolute voltage increases. At the same time a current i_{m} is injected into the DC-link midpoint with opposite sign as the phase voltage with smallest absolute value. By adjusting the duration of state $\boxed{\text{2A}}$ such that zero phase shift is maintained throughout the mains period the simulated waveform of the boost inductor current of one phase shown in Fig. 3.22 is obtained. The local average of the boost inductor current is sinusoidal and it can be observed that the local average of the midpoint current varies with three times the mains frequency and contains no DC-component.

3.3.3 Proposed Sinusoidal Current DCM Pattern B

Although when using the switching pattern described in Section 3.3.2 the generated midpoint current contains no DC-component, it is desired to be able to provide a small DC midpoint current to counteract asymmetric leakage currents or small asymmetric loads connected to the output that would otherwise cause unbalanced DC-link voltages. Using the

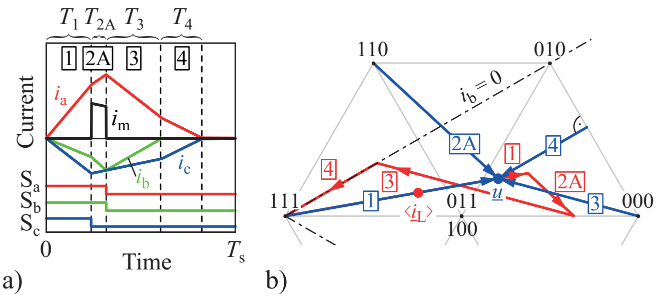

T_1
T_{2A}
T_3
T_4
1
2A
3
4
Current
i_a
i_m
i_b
i_c
S_a
S_b
S_c
0
Time
T_s
a)
110
010
$i_b = 0$
2A
1
4
4
3
2A
1
3
111
011
100
000
u
$\langle i_L \rangle$
b)

Fig. 3.21: Boost inductor currents during one switching period in DCM employing switching state $\boxed{\text{2A}}$ while $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$ (a) and space vector representation of the same situation (b). The duration of the switching state $\boxed{\text{2A}}$ is chosen such that the phase shift between mains voltage space vector and boost inductor current space vector is zero.

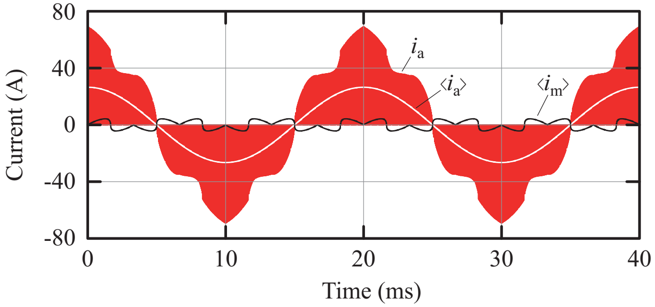


Fig. 3.22: Simulated boost inductor current of one phase, its local average value and the local average value of the midpoint current in DCM employing switching state $\boxed{\text{2A}}$ to reach resistive mains behaviour. Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2} \cdot 230\,\mathrm{V}$, $U_\mathrm{pn} = 800\,\mathrm{V}$, $P = 13\,\mathrm{kW}$, $f_\mathrm{s} = 28\,\mathrm{kHz}$, $L = 50\,\mathrm{\mu H}$.

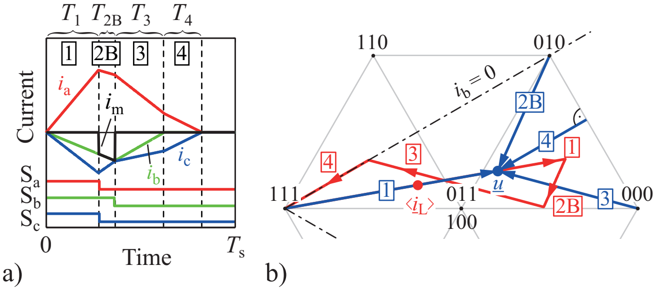


Fig. 3.23: Boost inductor currents during one switching period in DCM employing switching state $\boxed{\text{2B}}$ while $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$ (a) and space vector representation of the same situation (b). The duration of the switching state $\boxed{\text{2B}}$ is chosen such that the phase shift between mains voltage space vector and boost inductor current space vector is zero.

switching state 010 in the aforementioned example as shown in Fig. 3.23 allows exactly that. By leaving the switch of the phase with the smallest absolute voltage turned on longer than the two others, switching state $\boxed{\text{2B}}$ is inserted between states $\boxed{1}$ and $\boxed{3}$. The space vector diagram in Fig. 3.23b shows that this switching state also allows to achieve zero phase shift between mains voltage and local average of the boost inductor current, if the duration of the state is chosen correctly. The current waveforms during one switching period (Fig. 3.23a) reveal that the absolute value of the current of the phase with the smallest absolute voltage is also rising, as it is when state $\boxed{\text{2A}}$ is applied. However, since the midpoint current during state $\boxed{\text{2B}}$ equals the current of the phase with the smallest absolute value of the voltage the direction of the midpoint current during state $\boxed{\text{2B}}$ is opposite to its direction during state $\boxed{\text{2A}}$. If the duration of state $\boxed{\text{2A}}$ is chosen correctly to eliminate the phase shift between mains voltage and boost inductor current throughout the mains period, the local average of the boost inductor current is also sinusoidal as shown in Fig. 3.24. By comparing Fig. 3.22 and Fig. 3.24 it is observed that the local average of the midpoint current has opposite sign in the two different switching patterns A and B.

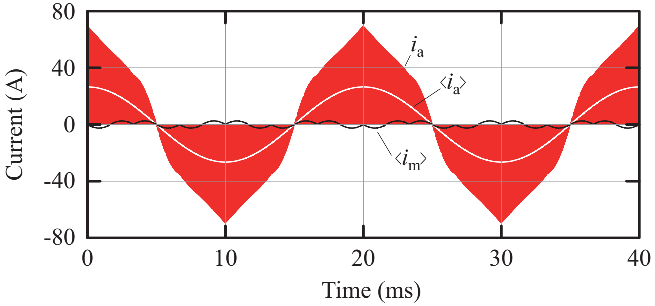


Fig. 3.24: Simulated boost inductor current of one phase, its local average value and the local average value of the midpoint current in DCM employing switching state $\boxed{2\text{B}}$ to reach resistive mains behaviour. Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2} \cdot 230\,\text{V}$, $U_{\text{pn}} = 800\,\text{V}$, $P = 13\,\text{kW}$, $f_{\text{s}} = 28\,\text{kHz}$, $L = 50\,\mu\text{H}$.

3.3.4 Calculation of the Duty Cycles

In order to actually achieve sinusoidal currents using the switching patterns described in Sections 3.3.2 and 3.3.3, the durations of switching states $\boxed{1}$, $\boxed{2\text{A}}$ and $\boxed{2\text{B}}$ have to be set correctly, depending on the amount of power to be transferred, the values of the phase voltages and the DC-link voltage. As shown in the the following the required expressions can be found analytically. For each of the described five switching states n the equivalent circuit, the current change Δi_{kn} in each mains phase k and the duration T_n are given in Tab. 3.1. Using these equations the local average values of the currents in the boost inductors are calculated as

$$\begin{aligned} \langle i_k \rangle = \frac{1}{2} & (\Delta i_{k1} T_1 + (\Delta i_{k1} + \Delta i_{k2x}) T_{2x} + (\Delta i_{k1} + \Delta i_{k2x} \\ & + \Delta i_{k3}) T_3 + (\Delta i_{k1} + \Delta i_{k2x} + \Delta i_{k3} + \Delta i_{k4}) T_4) \, f_{\text{s}}, \end{aligned} \tag{3.26}$$

with x being either A or B. In order to obtain sinusoidal input currents the rectifier has to act like a symmetric three-phase resistive load concerning the local current average values $\langle i_k \rangle$. Therefore, it is required that for each phase k the resistance $r_k = \frac{u_k}{\langle i_k \rangle}$ is the same, i.e. $r_k = r$. Assuming $\sum_k u_k = 0$ and $\sum_k i_k = 0$, this condition is guaranteed if the resistances of two phases are the same. Therefore, solving the equation

$$\frac{u_\mathrm{a}}{\langle i_\mathrm{a}\rangle} = \frac{u_\mathrm{b}}{\langle i_\mathrm{b}\rangle}, \tag{3.27}$$

with the local average values of the currents inserted from (3.26), yields the value of D_2A or D_2B (as defined in Tab. 3.1) that is necessary for resistive behaviour, i.e. sinusoidal input currents after filtering switching frequency components. The value of D_1 follows by inserting the values D_2A or D_2B obtained from (3.27) into any of the equations $r = \frac{u_k}{\langle i_k\rangle}$ for a required resistance r at the mains side. In order to normalize the resistance r emulated to the mains and the phase voltages, and in order to include the 30 ° symmetry of the three phase system, the variables

$$\begin{aligned} D_0 &= \sqrt{\frac{f_\mathrm{s}L}{r}}, && (3.28)\\ m_\mathrm{max} &= \frac{2\cdot\max(|u_\mathrm{a}|,|u_\mathrm{b}|,|u_\mathrm{c}|)}{U_\mathrm{pn}}, && (3.29)\\ m_\mathrm{min} &= \frac{2\cdot\min(|u_\mathrm{a}|,|u_\mathrm{b}|,|u_\mathrm{c}|)}{U_\mathrm{pn}}, && (3.30) \end{aligned}$$

are introduced. Using these definitions the duty cycles for switching pattern B are obtained as

$$D_\mathrm{1B} = D_0\sqrt{2 - 2m_\mathrm{max} + m_\mathrm{min}}, \tag{3.31}$$

$$D_\mathrm{2B} = D_0\sqrt{2 - 3m_\mathrm{min}} - D_\mathrm{1B}. \tag{3.32}$$

For switching pattern A, the relative duty cycles are

$$\begin{aligned} D_\mathrm{1A} = \frac{D_0}{\sqrt{y}} \cdot \big((9m_\mathrm{min}^2 + 6m_\mathrm{min} + 2)m_\mathrm{max} \\ -(6m_\mathrm{min} + 2)m_\mathrm{max}^2 - 3m_\mathrm{min}^3 - 4m_\mathrm{min}^2\big) \end{aligned} \tag{3.33}$$

and

$$\begin{aligned} D_\mathrm{2A} = D_\mathrm{1A} \cdot (9m_\mathrm{min}^2 m_\mathrm{max} - 2m_\mathrm{min}^2 - \sqrt{x} \\ -6m_\mathrm{min}m_\mathrm{max}^2 + 4m_\mathrm{max}m_\mathrm{min} - 3m_\mathrm{min}^3) \\ \div(3m_\mathrm{min}^3 - 9m_\mathrm{min}^2 m_\mathrm{max} + 4m_\mathrm{min}^2 - 2m_\mathrm{max} \\ +6m_\mathrm{min}m_\mathrm{max}^2 - 6m_\mathrm{max}m_\mathrm{min} + 2m_\mathrm{max}^2), \end{aligned} \tag{3.34}$$

with

$$\begin{aligned} x = (2m_{\max} - 2 - m_{\min})m_{\min}(3m_{\min} - 2) \\ \cdot(2m_{\max} - m_{\min})(m_{\max}^2 - m_{\min}^2) \end{aligned} \tag{3.35}$$

and

$$\begin{aligned} y = 3m_{\min}^5 + m_{\min}^4(7 - 15m_{\max}) \\ +m_{\min}^3(24m_{\max}^2 - 23m_{\max} + 2) \\ +m_{\min}^2(20m_{\max}^2 - 8m_{\max} - 12m_{\max}^3) \\ +m_{\min}(\sqrt{x} - 4m_{\max}^3 + 6m_{\max}^2) \\ +m_{\max}(\sqrt{x} + 2m_{\max} - 2m_{\max}^2). \end{aligned} \tag{3.36}$$

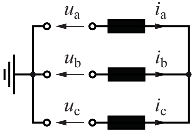
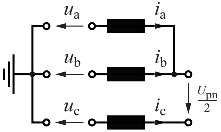
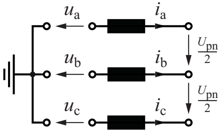
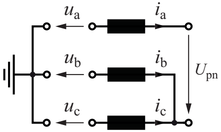
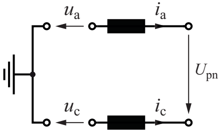
Because of the complexity of the terms for switching pattern A a realization of the control scheme in hardware is only possible using look-up tables for the relative duty cycles $d_{1\mathrm{A}} = \frac{D_{1\mathrm{A}}}{D_0}$, $d_{2\mathrm{A}} = \frac{D_{2\mathrm{A}}}{D_0}$ and $d_{1\mathrm{B}} = \frac{D_{1\mathrm{B}}}{D_0}$, $d_{2\mathrm{B}} = \frac{D_{2\mathrm{B}}}{D_0}$. With the modulation index $M = \frac{2\hat{u}}{U_{\mathrm{pn}}}$ the relative duty cycles are shown in Fig. 3.25. It is observed, that the functions are smooth and continuous and therefore well-suited for implementation using look-up tables. For high values of the modulation index, the duty cycle functions (3.33,3.34,3.31,3.32) result in negative values. Numerical investigations show that all duty cycle values are valid for modulation indices up to $M \leq 1.12$ which is slightly less than the maximum modulation index of $M_{\max,ccm} = \frac{2}{\sqrt{3}} \approx 1.15$ that the rectifier could theoretically be operated with in CCM [47]. However, also in CCM this modulation index cannot be reached since a small voltage reserve is necessary to maintain current control.

3.3.5 DCM/CCM Threshold

Since the rectifier is operating at constant switching frequency, the total on-time T for all states is limited to

$$T = T_1 + T_{2x} + T_3 + T_4 < \frac{1}{f_{\mathrm{s}}}. \tag{3.37}$$

According to (3.28) the duration of each state is proportional to $\frac{1}{\sqrt{r}}$. Therefore, the resistance which can be emulated for the mains in DCM is limited. This resistance value marks the threshold between CCM and

State	s_{a},s_{b},s_{c}	Equivalent circuit	Changes of inductor currents	Duration of state
$\boxed{1}$	1 - 1 - 1	 u_{a} i_{a} u_{b} i_{b} u_{c} i_{c}	$\Delta i_{\mathrm{a1}} = \frac{T_1}{L} \cdot u_{\mathrm{a}}$ $\Delta i_{\mathrm{b1}} = \frac{T_1}{L} \cdot u_{\mathrm{b}}$ $\Delta i_{\mathrm{c1}} = \frac{T_1}{L} \cdot u_{\mathrm{c}}$	$T_1 = \frac{D_1}{f_{\mathrm{s}}}$
$\boxed{2A}$	1 - 1 - 0	 u_{a} i_{a} u_{b} i_{b} $\frac{U_{\mathrm{pn}}}{2}$ u_{c} i_{c}	$\Delta i_{\mathrm{a2a}} = \frac{T_{\mathrm{2A}}}{L} \cdot (u_{\mathrm{a}} - \frac{U_{\mathrm{pn}}}{6})$ $\Delta i_{\mathrm{b2a}} = \frac{T_{\mathrm{2A}}}{L} \cdot (u_{\mathrm{b}} - \frac{U_{\mathrm{pn}}}{6})$ $\Delta i_{\mathrm{c2a}} = \frac{T_{\mathrm{2A}}}{L} \cdot (u_{\mathrm{c}} + \frac{U_{\mathrm{pn}}}{3})$	$T_{\mathrm{2A}} = \frac{D_{\mathrm{2A}}}{f_{\mathrm{s}}}$
$\boxed{2B}$	0 - 1 - 0	 u_{a} i_{a} $\frac{U_{\mathrm{pn}}}{2}$ u_{b} i_{b} $\frac{U_{\mathrm{pn}}}{2}$ u_{c} i_{c}	$\Delta i_{\mathrm{a2b}} = \frac{T_{\mathrm{2B}}}{L} \cdot (u_{\mathrm{a}} - \frac{U_{\mathrm{pn}}}{2})$ $\Delta i_{\mathrm{b2b}} = \frac{T_{\mathrm{2B}}}{L} \cdot u_{\mathrm{b}}$ $\Delta i_{\mathrm{c2b}} = \frac{T_{\mathrm{2B}}}{L} \cdot (u_{\mathrm{c}} + \frac{U_{\mathrm{pn}}}{2})$	$T_{\mathrm{2B}} = \frac{D_{\mathrm{2B}}}{f_{\mathrm{s}}}$
$\boxed{3}$	0 - 0 - 0	 u_{a} i_{a} u_{b} i_{b} U_{pn} u_{c} i_{c}	$\Delta i_{\mathrm{a3}} = \frac{T_3}{L} \cdot (u_{\mathrm{a}} - \frac{2U_{\mathrm{pn}}}{3})$ $\Delta i_{\mathrm{b3}} = \frac{T_3}{L} \cdot (u_{\mathrm{b}} + \frac{U_{\mathrm{pn}}}{3})$ $\Delta i_{\mathrm{c3}} = \frac{T_3}{L} \cdot (u_{\mathrm{c}} + \frac{U_{\mathrm{pn}}}{3})$	$T_3 = -\frac{L \cdot (\Delta i_{\mathrm{b1}} + \Delta i_{\mathrm{b2x}})}{u_{\mathrm{b}} + \frac{U_{\mathrm{pn}}}{3}}$
$\boxed{4}$	0 - 0 - 0	 u_{a} i_{a} U_{pn} u_{c} i_{c}	$\Delta i_{\mathrm{a4}} = \frac{T_4}{2L} \cdot (u_{\mathrm{a}} - u_{\mathrm{c}} - U_{\mathrm{pn}})$ $\Delta i_{\mathrm{b4}} = 0$ $\Delta i_{\mathrm{c4}} = \frac{T_3}{2L} \cdot (u_{\mathrm{c}} - u_{\mathrm{a}} + U_{\mathrm{pn}})$	$T_4 = -\frac{2L \cdot (\Delta i_{\mathrm{a1}} + \Delta i_{\mathrm{a2x}} + \Delta i_{\mathrm{a3}})}{u_{\mathrm{a}} - u_{\mathrm{c}} - U_{\mathrm{pn}}}$

Tab. 3.1: Switching states of the proposed sinusoidal current DCM control scheme, assuming $u_{\mathrm{a}} > 0 > u_{\mathrm{b}} > u_{c}$.

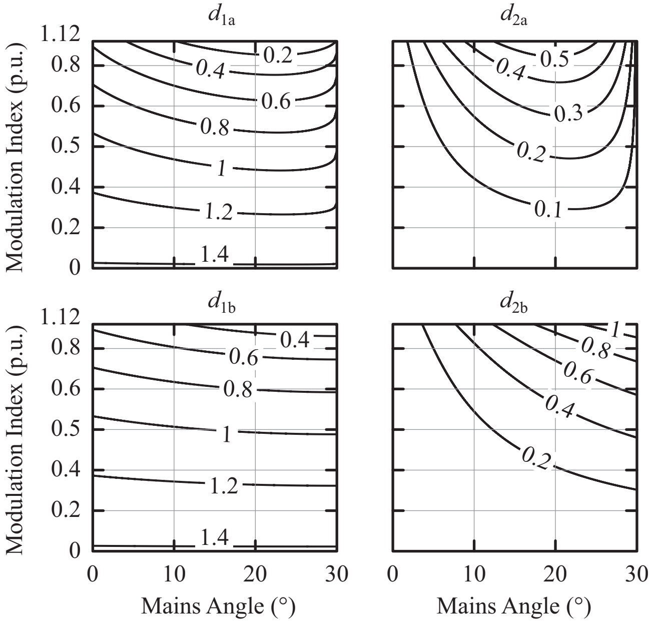


Fig. 3.25: Relative duty cycles $d_k = \frac{D_k}{D_0}$ for resistive behaviour of the VR in DCM for switching patterns A and B as function of modulation index and mains angle.

DCM operation. By solving (3.37), the minimum resistance which can be emulated for the mains during a switching period with pattern B is obtained as

$$r_{\mathrm{min,B}} = \frac{4 f_{\mathrm{s}} L}{2 + m_{\mathrm{min}} - 2 m_{\mathrm{max}}}, \tag{3.38}$$

with the switching frequency f_{s}, the boost inductance L and m_{max} and m_{min} as defined in (3.30) and (3.29). It is possible to find an analytic expression for $r_{\mathrm{min,A}}$ for pattern A using symbolic math software, however, the result is too complicated to be shown here. Instead it shall be mentioned that numerical investigations reveal that

$$r_{\mathrm{min,A}} < 1.1 r_{\mathrm{min,B}}. \tag{3.39}$$

However, one is usually only interested in the minimum resistance which is achievable with both patterns A and B throughout the whole mains period at a certain modulation index M. The exact value,

$$R_{\mathrm{min}}(M) = \max_{\varphi \in [0°, 30°]} (r_{\mathrm{min,A}}(M, \varphi), r_{\mathrm{min,B}}(M, \varphi)), \tag{3.40}$$

is shown in Fig. 3.26. It can be approximated with less than 1 % error as

$$R_{\mathrm{min}}(M) \approx \frac{4 f_{\mathrm{s}} L}{2 - \sqrt{3} M}. \tag{3.41}$$

Therefore, the maximum power that can be transferred using both patterns A and B throughout the whole mains period is estimated with less than 1 % error as

$$P_{\mathrm{max}} \approx \frac{3 \hat{u}^2}{4 f_{\mathrm{s}} L} \left(1 - \frac{\sqrt{3} \hat{u}}{U_{\mathrm{pn}}} \right), \tag{3.42}$$

with the mains phase voltage amplitude $\hat{u}$, the switching frequency f_{s}, the boost inductance L and the DC-link voltage U_{pn}. The minimum resistance which is achievable in DCM marks the threshold for the phase current controllers to switch to DCM. To avoid that the controller constantly switches between CCM and DCM a hysteresis has to be implemented, so that DCM is only entered if the voltage controller requires a resistance of, e.g. $2R_{\mathrm{min}}$, and CCM is only re-entered if the required resistance drops below R_{min}. Using such a hysteresis for the selection of the current control mode requires that the operating ranges for DCM and CCM are overlapping. That is actually the case since at the value

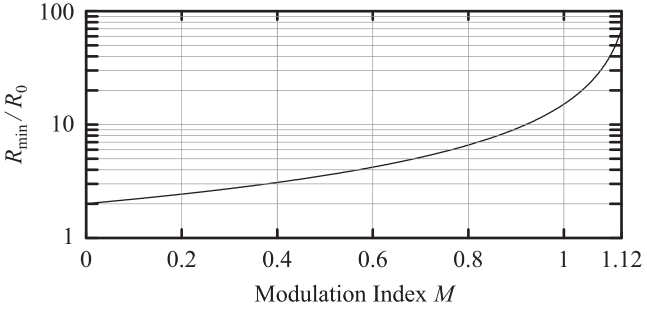


Fig. 3.26: Minimum resistance that can be emulated for the mains throughout the whole mains period using the DCM patterns A or B related to the base $R_0 = f_\mathrm{s}L$.

$R = R_\mathrm{min}$ the current ripple in DCM is approximately twice as high than it is in CCM. Therefore, operation in CCM with satisfactory input current quality is possible for emulated mains resistance values up to $2R_\mathrm{min}$.

3.3.6 DC-Link Balancing & Midpoint Current Limit

Since the direction of the current injected into the DC-link midpoint (midpoint current i_m) differs between switching patterns A and B, the ratio between the two DC-link voltages can be controlled by selecting the appropriate switching pattern. For equal voltage sharing between the two parts of the DC-link bang-bang control can be used with the rule for selecting the switching pattern as specified in Tab. 3.2. Applying this control in an idealized circuit simulation results in a boost inductor current waveform as shown in Fig. 3.27a. By comparing the shape of the current ripple with Figs. 3.22 and 3.24, the continuous alternation of the switching pattern can be observed. Also the (low-pass filtered) midpoint current is virtually eliminated. If the two parts of the DC-link are loaded with slightly different loads or if there are different parasitic leakage currents present, the VR has to supply a steady-state average midpoint current throughout the mains period I_m. In CCM the amount of midpoint current that can be supplied is proportional to the phase current amplitude and reduces with increasing modulation index [48]. At a modulation index $M = 1$ approximately 45 % of the phase rms current amplitude can be supplied into the midpoint. In DCM the current

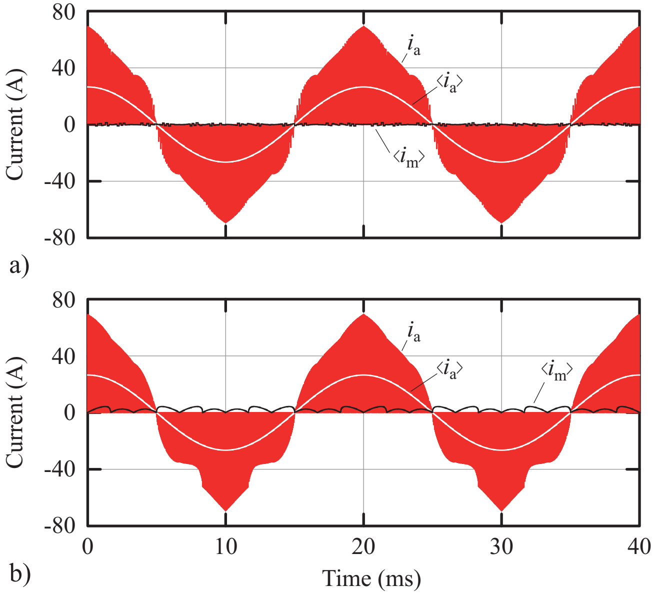


Fig. 3.27: Simulated boost inductor current, its local average value and the low-pass filtered midpoint current with output voltage balancing control and symmetric loading of the two DC-links (a) and with maximum permissible asymmetric loading (more load on negative DC-link) (b). Operating condition and parameters used for the simulation: $\hat{u} = \sqrt{2} \cdot 230\,\mathrm{V}$, $U_{\mathrm{pn}} = 800\,\mathrm{V}$, $f_{\mathrm{s}} = 28\,\mathrm{kHz}$, $L = 50\,\mu\mathrm{H}$, $P = P_{\mathrm{p}} + P_{\mathrm{n}}$ with $P_{\mathrm{p}} = P_{\mathrm{n}} = 6.5\,\mathrm{kW}$ in (a) and $P_{\mathrm{p}} = 5.6\,\mathrm{kW}$ and $P_{\mathrm{n}} = 7.4\,\mathrm{kW}$ in (b).

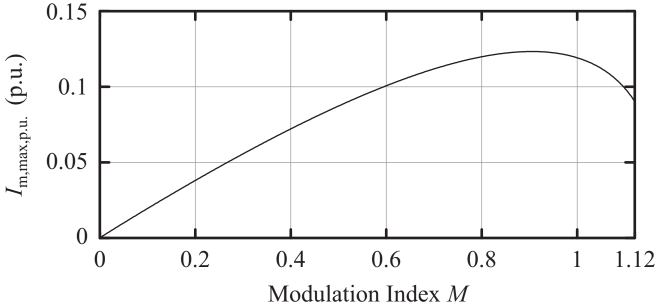


Fig. 3.28: Maximum average midpoint current that can be supplied into the midpoint of the DC-link relative to the phase current fundamental RMS value.

which can be supplied to the midpoint by switching between patterns A and B is also limited. The maximum positive midpoint current is generated if state 2A is always used while the phase voltage with the smallest absolute value is negative and state 2B is always used while the phase voltage with the smallest absolute value is positive. The boost inductor current waveform for this situation is shown in Fig. 3.27b. An asymmetry in the shape between positive and negative half-period of the boost inductor current can be observed but the local average value is sinusoidal. The average value related to the mains period of this maximum midpoint current can be found only numerically. Using the RMS value of the phase current fundamental I_{p} for normalization, the maximum relative midpoint current $I_{\mathrm{m,max,p.u.}} = \frac{I_{\mathrm{m,max}}}{I_{\mathrm{p}}}$ results which is shown in Fig. 3.28 as a function of the modulation index M. It is observed that the maximum midpoint current for typically used modulation indices in the range of $M \in [0.6, 1.1]$ amounts to at least $10\,\%$ of the phase current rms value. This is substantially less than the value which is possible in CCM (cf. [48]), but sufficient to cover asymmetric leakage currents and to recover from a transient DC-link voltage unbalance. In the following either pattern A or B is selected according to Tab. 3.2, which is the proposed control scheme of the VR in DCM with equal DC-link voltages. A circuit simulation of the prototype constructed within this work is used to demonstrate the functionality of the proposed balancing scheme to maintain symmetric output voltages with asymmetric load. The situation is shown in Fig. 3.29. At 400 V mains voltage and

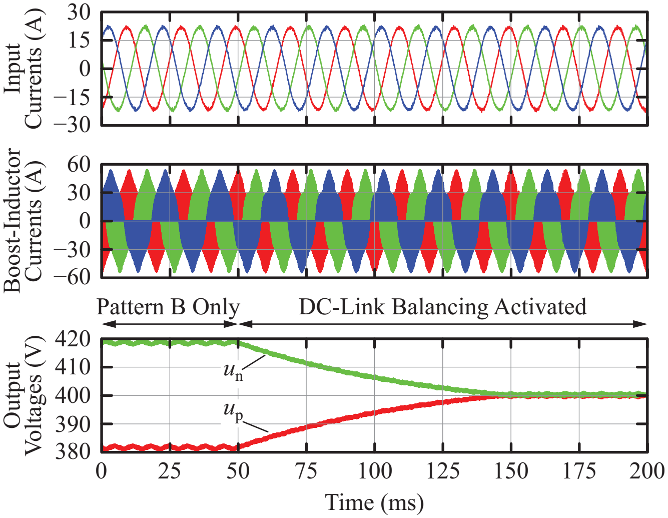


Fig. 3.29: Effect of proposed DCM DC-link balancing scheme, activated at $t = 50\,\text{ms}$, with $30.4\,\Omega$ on the upper and $33.6\,\Omega$ on the lower DC-link after initial operation using pattern B only.

Tab. 3.2: DC-Link Voltage Balancing Control Rule

	$u_\mathrm{p} > u_\mathrm{n}$	$u_\mathrm{p} < u_\mathrm{n}$
$\max(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) + \min(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) > 0$	Pattern A	Pattern B
$\max(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) + \min(u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}) < 0$	Pattern B	Pattern A

800 V DC-link voltage the rectifier is loaded with 30.4 Ω on the upper and 33.6 Ω on the lower DC-link (32 Ω ± 5 %). Initially pattern B is applied constantly, i.e. the DC-link balancing scheme is turned off. At $t = 50\,\mathrm{ms}$ the balancing scheme is activated, symmetrizing the output voltages within $\approx 100\,\mathrm{ms}$ with $2 \times 2.3\,\mathrm{mF}$ DC-link capacitance. The shape of the mains currents is not affected during the transition, however the boost inductor current ripple shape changes slightly as soon as the DC-link balancing control is activated.

3.4 Input Filter Dimensioning

Switching transients of power converters can lead to electro magnetic disturbance of communication or other electronic equipment. In order to prevent that various regulations for EMI are defined that converter systems connected to the public utility grid have to comply with [19]. The EMI filter, usually comprising several *LC* low-pass filter stages, attenuates the conducted noise emission of the converter to the mains to meet specified limits. Although comprehensive literature on this topic exists [41], this Section aims to summarize the fundamentals necessary to design a filter for a VR with special focus on the effect of the DCM control scheme proposed in Sec. 3.3.

3.4.1 Emission Regulations and Limits

Conducted electromagnetic emission is measured using a Line Impedance Stabilization Network (LISN) as shown in Fig. 3.30. The LISN is connected between the mains and the Device Under Test (DUT), i.e. the power converter. It includes one 50 Ω measurement resistor per phase and a two-stage filter that blocks HF currents from entering the mains and instead guides them through the measurement resistors. This filter also works the other way around and prevents HF currents coming

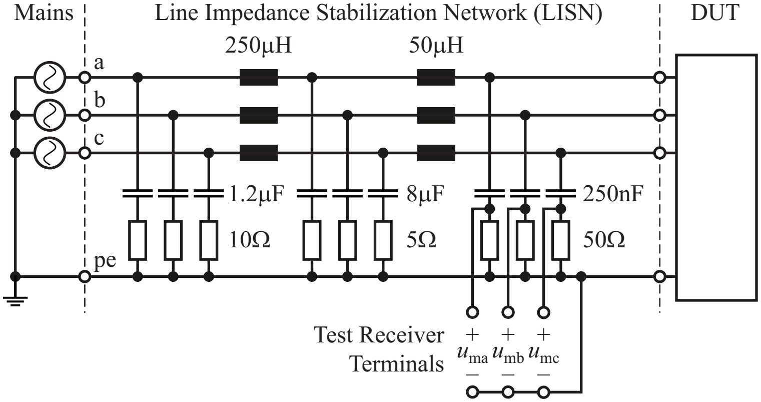

Mains
Line Impedance Stabilization Network (LISN)
DUT
250µH
50µH
a
b
c
pe
1.2µF
10Ω
8µF
5Ω
250nF
50Ω
Test Receiver Terminals
+ + +
u_{ma} u_{mb} u_{mc}
– – –

Fig. 3.30: Internal structure of a 50 Ω/50 µH LISN according to CISPR16.

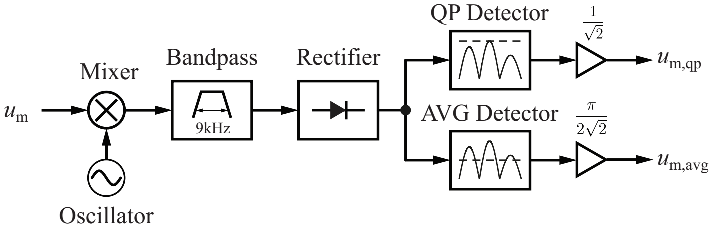

QP Detector
$\frac{1}{\sqrt{2}}$
$u_{m,qp}$
Mixer
Bandpass
Rectifier
u_m
9kHz
AVG Detector
$\frac{\pi}{2\sqrt{2}}$
$u_{m,avg}$
Oscillator

Fig. 3.31: Principle block diagram of a CISPR QP and AVG detector.

from noisy mains from flowing through the measurement resistors and influencing the measurement.

The HF voltage signal measured at the measurement resistors of the LISN is fed into a detector which is illustrated in principle in Fig. 3.31. Both, the detector and the LISN are defined in detail in CISPR-16-1-1 [49]. The detector tunes to each measurement frequency in the range of 150 kHz to 30 MHz using a mixer and a bandpass of 9 kHz bandwidth. This frequency band of the signal is rectified and fed into two different kinds of low-pass filters. The QP detector and the AVG detector. Both detectors are followed by a gain which is set such that if the input signal u_s is sinusoidal and its frequency is above 150 kHz both output signals $u_{m,qp}$ and $u_{m,avg}$ equal the input signal RMS value. A typical conducted noise emission, however, contains components at the

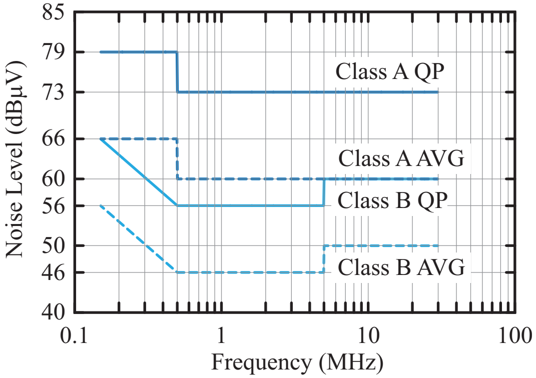


Fig. 3.32: CISPR conducted noise emission limits.

switching frequency harmonics and their side-bands, resulting in different outputs of QP and AVG detector since the QP detector implements a non-linear low-pass with a charging time constant of 1 ms and a discharging time constant of 160 ms, while the AVG detector indicates the average of the rectified signal [49].

The CISPR defines two device Classes for conducted electromagnetic emission. All equipment *suitable for use in domestic establishments and in establishments directly connected to a low-voltage power supply network which supplies buildings used for domestic purposes* [50] is categorized in Class B, which defines the more stringent limits for conducted noise emission. Slightly relaxed limits are specified for Class A equipment which is *suitable for use in all establishments other* than the ones defined for class B. Usually industrial equipment is categorized in Class A. For the studied X-ray system it is specified to comply with Class B limits. The maximum voltage levels for QP and AVG detected signals according to CISPR 11 are provided in Fig. 3.32 in dB related to 1 µV (e.g. 60 dbµV = 1 mV).

3.4.2 Vienna Rectifier Noise Emission Model

The conducted noise emission of a power converter is usually modelled by replacing half bridges with controlled voltage sources at the switching node and controlled current sources at the DC-link side. Applying this rule to the circuit of the VR with a single-stage DM filter and a single-

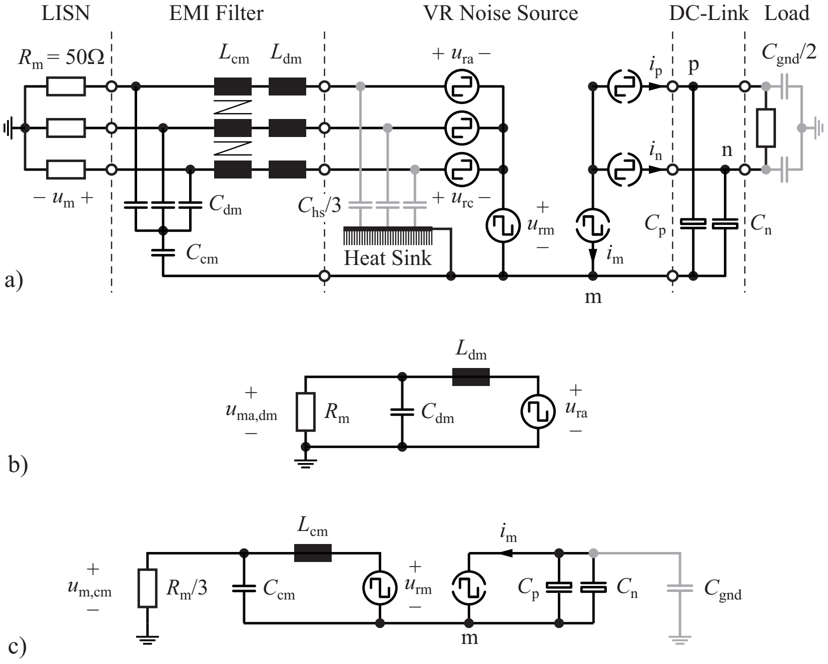

LISN
EMI Filter
VR Noise Source
DC-Link
Load
$R_m = 50\Omega$
L_{cm}
L_{dm}
$+ u_{ra} -$
i_p
p
$C_{gnd}/2$
i_n
n
$- u_m +$
C_{dm}
$C_{hs}/3$
$+ u_{rc} -$
u_{rm}
C_p
C_n
C_{cm}
Heat Sink
i_m
a)
m
L_{dm}
$u_{ma,dm}$
R_m
C_{dm}
u_{ra}
b)
L_{cm}
i_m
$u_{m,cm}$
$R_m/3$
C_{cm}
u_{rm}
C_p
C_n
C_{gnd}
m
c)

Fig. 3.33: (a) Complete VR equivalent circuit for noise emission calculations with the CM capacitor connected to the midpoint, comprising of the LISN measurement resistors, one EMI filter stage, DM and CM noise voltage sources at the AC side with parasitic capacitors connected to the heat sink, DM and CM noise current sources at the DC side, the DC-link and the load including its parasitic ground capacitance. (b) Derived DM equivalent circuit. (c) Derived CM equivalent circuit, neglecting the DM inductors and the DM capacitors.

stage CM filter with capacitive feedback to the midpoint results in the equivalent circuit shown in Fig. 3.33a. The three switching nodes of the rectifier which connect to the boost inductors are controlled by three DM voltage sources and one CM voltage source already introduced in Sec. 3.2.3. The currents injected into the DC-link (see Fig. 3.4) are modelled by the current sources i_p, i_m and i_n. At the rectifier input the first EMI filter stage is shown, consisting of the boost inductors which contribute the differential mode inductance of the stage L_dm and one CM inductor providing the CM inductance L_cm. The LISN circuit is reduced to the measurement resistors R_m only since it can be assumed that all HF current is passing through them. The capacitors C_hs represent the capacitances between semiconductors and heat sink. With a low-inductance connection between heat sink and DC-link these capacitors are connected in parallel to the noise voltage sources and, therefore, do not need to be considered.

Following the principle of superposition, the voltage at the measurement resistance of phase a,

$$u_\mathrm{ma} = u_\mathrm{ma,dm} + u_\mathrm{m,cm}, \tag{3.43}$$

can be expressed as the sum of a DM part $u_\mathrm{ma,dm}$ according to the equivalent circuit shown in Fig. 3.33b, and a CM part according to the equivalent circuit shown in Fig. 3.33c. While the DM component of the voltage at the measurement resistor,

$$\hat{\underline{u}}_\mathrm{ma,dm} = \frac{\hat{\underline{u}}_\mathrm{ra}}{1 + j\omega\frac{L_\mathrm{dm}}{R_\mathrm{m}} - \omega^2 L_\mathrm{dm} C_\mathrm{dm}}, \tag{3.44}$$

is easily derived, the CM component deserves a bit more attention. According to Fig. 3.33c the voltage source u_rm and the current source i_m contribute to the measurement resistor voltage CM component. Assuming the worst case $C_\mathrm{p} \to \infty$ and $C_\mathrm{n} \to \infty$ for the contribution of u_rm and the worst case $C_\mathrm{cm} \to \infty$ for the contribution of i_m results in the approximate CM component of the voltage at the measurement resistor,

$$\hat{\underline{u}}_\mathrm{ma,cm} = \frac{\hat{\underline{u}}_\mathrm{rm}}{1 + \frac{j\omega L_\mathrm{cm}}{\frac{R_\mathrm{m}}{3} + \frac{1}{j\omega C_\mathrm{gnd}}} - \omega^2 L_\mathrm{cm} C_\mathrm{cm}} + \frac{\frac{R_\mathrm{m}}{3}\hat{\underline{i}}_\mathrm{m}}{1 + \frac{C_\mathrm{p}+C_\mathrm{n}}{C_\mathrm{gnd}} + j\omega\frac{R_\mathrm{m}}{3}(C_\mathrm{p} + C_\mathrm{n})}. \tag{3.45}$$

The CM noise contribution of the midpoint current in (3.45) can only be reduced by increasing the DC-link capacitance, since the ground capacitance and the measurement resistance are external parameters. The actual CM filter does not affect this component if the CM capacitors are connected to the DC-link midpoint as in Fig. 3.33a.

In order to avoid the CM noise caused by the midpoint current the CM capacitors can be connected to the outputs p and n instead of the midpoint m as shown in Fig. 3.34a. The resulting CM equivalent circuit for this case (Fig. 3.34b) can be further simplified by replacing the noise current source with a Thevenin equivalent noise voltage source as shown in Fig. 3.34c. The amplitude of the noise voltage source $\frac{1}{C_\mathrm{p}+C_\mathrm{n}}\int i_\mathrm{m}\mathrm{d}t$, which equals the voltage ripple between the DC-link midpoint and the average potential between p and n, is usually at least one order of magnitude smaller than the CM voltage source u_rm and can, therefore, be neglected.

Assuming the worst case $C_\mathrm{gnd}\to\infty$ and that the CM capacitors are connected to the outputs, the voltage at the measurement resistor R_m of phase a can be expressed as

$$\underline{\hat{u}}_\mathrm{ma}\approx\frac{\underline{\hat{u}}_\mathrm{ra}}{1+j\omega\frac{L_\mathrm{dm}}{R_\mathrm{m}}-\omega^2L_\mathrm{dm}C_\mathrm{dm}}+\frac{\underline{\hat{u}}_\mathrm{rm}}{1+j\omega\frac{L_\mathrm{cm}}{R_\mathrm{m}}-\omega^2L_\mathrm{cm}C_\mathrm{cm}} \tag{3.46}$$

A further simplification of (3.46) can be introduced by only considering the highest order of ω in the denominator of (3.46) and disregarding the phase information, instead assuming the worst case of DM and CM component being in phase. This HF asymptotic approximation can be generally expressed for N_dm and N_cm filter stages as

$$|\underline{\hat{u}}_\mathrm{ma}|\approx\frac{|\underline{\hat{u}}_\mathrm{ra}|}{A_\mathrm{dm}}+\frac{|\underline{\hat{u}}_\mathrm{rm}|}{A_\mathrm{cm}} \tag{3.47}$$

with the DM and CM attenuations

$$A_\mathrm{dm}=\omega^{2N_\mathrm{dm}}\prod_{k=1}^{N_\mathrm{dm}}L_{\mathrm{dm}k}C_{\mathrm{dm}k},\ A_\mathrm{cm}=\omega^{2N_\mathrm{cm}}\prod_{k=1}^{N_\mathrm{cm}}L_{\mathrm{cm}k}C_{\mathrm{cm}k}. \tag{3.48}$$

Therefore, the DM and CM components of the input voltage of the test receiver can be simply calculated by dividing the DM and CM components of the rectifier input voltages by the corresponding attenuations of the filter.

3.4.3 Vienna Rectifier Noise Emission Spectrum

The QP detected DM and CM noise spectra of the VR in DCM and CCM are shown in Fig. 3.35 assuming that no filter is present ($A_\mathrm{dm}=A_\mathrm{cm}=$

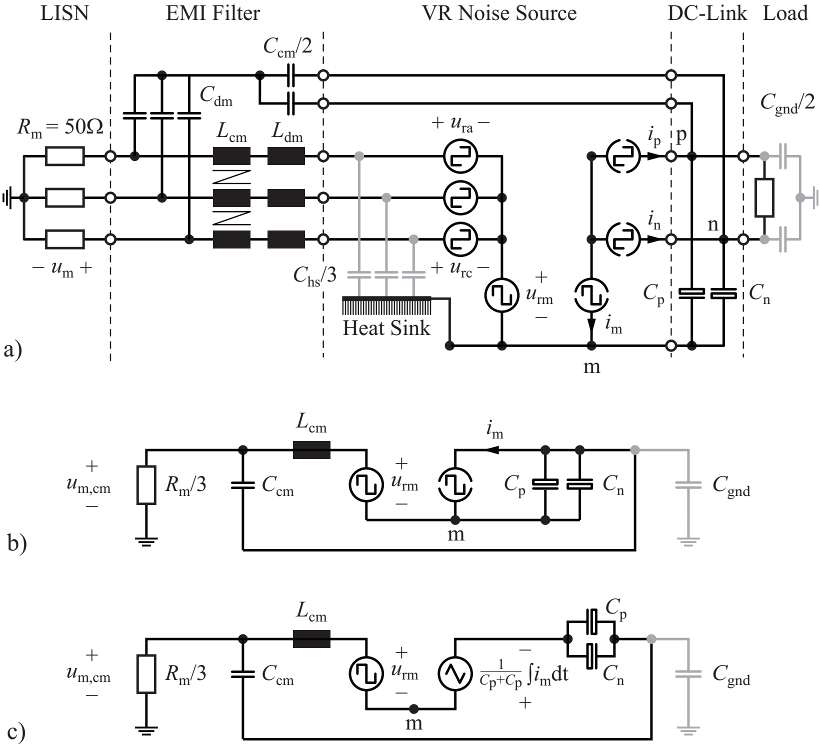

LISN
EMI Filter
VR Noise Source
DC-Link
Load
$C_{cm}/2$
C_{dm}
$C_{gnd}/2$
$R_m = 50\Omega$
L_{cm}
L_{dm}
$+ u_{ra} -$
i_p
p
i_n
n
$- u_m +$
$C_{hs}/3$
$+ u_{rc} -$
$+$
u_{rm}
$-$
C_p
C_n
Heat Sink
i_m
m
a)
L_{cm}
i_m
$+$
$u_{m,cm}$
$-$
$R_m/3$
C_{cm}
u_{rm}
C_p
C_n
C_{gnd}
m
b)
L_{cm}
C_p
$u_{m,cm}$
$R_m/3$
C_{cm}
u_{rm}
$\frac{1}{C_p+C_p}\int i_m dt$
C_n
C_{gnd}
m
c)

Fig. 3.34: (a) Complete VR equivalent circuit for noise emission calculations with the CM capacitor connected to the outputs. (b) Derived CM equivalent circuit, neglecting the DM inductors and the DM capacitors. (c) CM equivalent circuit with noise current source replaced by Thevenin equivalent noise voltage source.

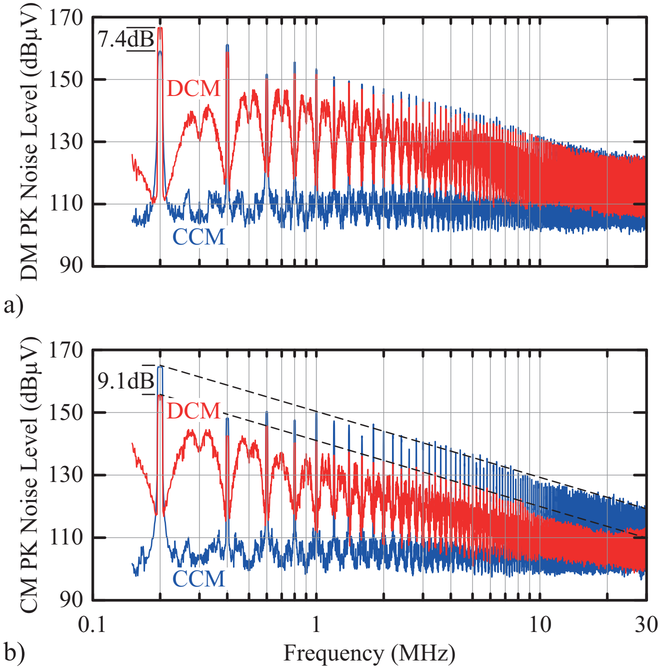


Fig. 3.35: Simulated noise emission detected with a CISPR11 peak receiver for the VR operating in CCM (blue) and in DCM (red). The DM noise with peak (PK) detection is shown in (a). It is observed that the DM noise in DCM at switching frequency is higher than in CCM. However, the noise levels at higher frequencies in DCM are the same or a little lower than in CCM. The CM noise with PK detection is shown in (b). It is shown that the CM noise level in DCM is lower than in CCM at all frequencies.

1). The switching frequency is set to 200 kHz to include the complete spectrum within the CISPR range of 150 kHz to 30 MHz. The resistance that the rectifier applies to the mains in DCM is set to the lowest value (R_{min}) which represents the case of highest noise emission. Both switching patterns A and B are used to balance the output voltage using bang-bang control. The nominal values $U_{\mathrm{ac}} = 400\,\mathrm{V}$, $U_{\mathrm{dc}} = 800\,\mathrm{V}$ are used for this simulation.

It is observed that the DM noise level at switching frequency is $\approx 7.4\,\mathrm{dB}$ higher than in CCM (Fig. 3.35a), therefore if the switching frequency is selected above 150 kHz this peak marks the worst case and defines the required DM attenuation. However, if the switching frequency is below 150 kHz this peak is located outside the limited range. Since all but the switching frequency component of the DM spectrum are approximately equal for DCM and CCM control it is no disadvantage to use the proposed DCM control scheme in this case.

The CM QP noise level is shown in Fig. 3.35b, showing that the CM noise in DCM is lower by $\approx 9.1\,\mathrm{dB}$ than in CCM for all harmonics of the switching frequency. This shifting of noise emission from CM to DM in DCM is explained by the modulation. With the proposed DCM control scheme all switches are turned on at the same time, whereas in CCM operation the switches of positive and negative boost stages are operated with 180° PWM carrier phase shift. Therefore, higher DM and lower CM conducted noise emission results in DCM compared to CCM.

3.4.4 Filter Design Procedure

A feasible filter design requires that the the total asymptotic attenuations of all CM and DM filter stages (3.48) are sufficient such that the detected QP and AVG voltages are below the allowed limits $u_{\mathrm{max,qp}}(\omega)$ and $u_{\mathrm{max,avg}}(\omega)$ at all frequencies within the range defined by CISPR.

Filter Structure

In principle two possible input filter structures could be used as shown for one filter stage in Fig. 3.36.

1. Separated DM and CM filter stages as shown in Fig. 3.36a use a dedicated CM inductor with capacitive feedback paths to the DC-link outputs and additionally a DM filter stage consisting of three

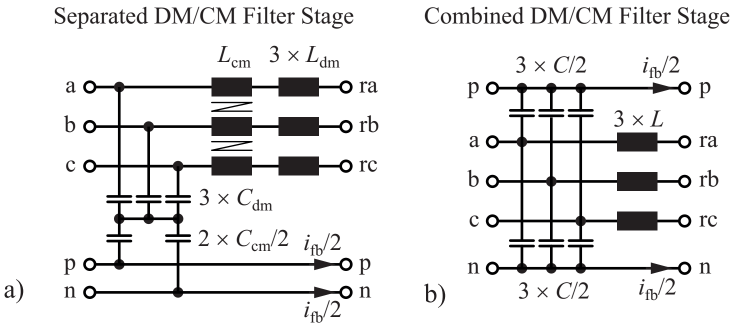

Separated DM/CM Filter Stage
Combined DM/CM Filter Stage
L_{cm}
$3 \times L_{\mathrm{dm}}$
a
b
c
ra
rb
rc
$3 \times C_{\mathrm{dm}}$
$2 \times C_{\mathrm{cm}}/2$
$i_{\mathrm{fb}}/2$
p
n
p
n
$i_{\mathrm{fb}}/2$
a)
$3 \times C/2$
$i_{\mathrm{fb}}/2$
p
p
$3 \times L$
a
b
c
ra
rb
rc
n
n
$3 \times C/2$
$i_{\mathrm{fb}}/2$
b)

Fig. 3.36: Possible filter stage structures: a separated DM&CM filter stage features less internally circulating feedback current i_{fb} (a), a combined DM&CM filter stage offers minimum component count.

DM inductor/capacitor pairs. The DM and CM attenuations (3.48) can be set independently.

2. Combined filter stages as shown in Fig. 3.36b attenuate both DM and CM by $A = \omega^{2N} \prod_{k=1}^{N} L_k C_k$. Although the structure minimizes the component count it is usually only an option with bidirectional topologies because of the high internally circulating feedback current that occurs within the capacitive filter feedback path to the DC-link due to the third harmonic LF CM voltage (Sec. 3.2.4).

The effect of the capacitive third harmonic current is shown in Fig. 3.37. Depending on the total amount of capacitance in the feedback path of the filter, the three times mains frequency capacitive current shifts the rectifier current local average zero crossing such that it cannot be supplied by the VR. The ratio

$$\frac{\hat{i}_{\mathrm{fb}(3)}}{\hat{i}_{(1)}} = \frac{3\pi}{2} f_{\mathrm{l}} C_{\mathrm{m}} R \qquad (3.49)$$

with the mains fundamental frequency f_{l}, the total input filter capacitance C_{m} connected to the DC-link and the (Y-connected) resistance R that the rectifier applies to the mains is particularly high in cases of high mains voltage and low load. Since the maximum VR phase shift reduces with increasing mains voltage, high mains and low load is the critical

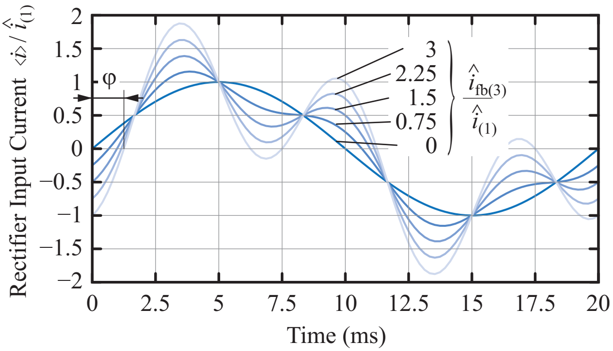


Fig. 3.37: Phase shift φ resulting between rectifier input current fundamental $\hat{i}_{(1)}$ zero crossing and rectifier input current local average $\langle i \rangle$ zero crossing for different ratios of the feedback current third harmonic amplitude $\hat{i}_{\mathrm{fb}(3)}$.

case (Sec. 3.2.1). Therefore, in order to not exceed the possible phase shift limit the total capacitance connected to the DC-link needs to be limited, which is easier to achieve with a separated DM&CM filter since only the CM capacitors, which are typically a factor of ten smaller than the DM capacitors, are connected to the DC-link in this case. Therefore, for the prototype a separated filter structure is selected.

For ratios $\frac{\hat{i}_{\mathrm{fb}(3)}}{\hat{i}_{(1)}} < 0.5$ the resulting phase shift (radian measure) due to a third harmonic feedback current between the zero crossings of the rectifier input current fundamental and the zero crossings of the rectifier input current local average can be approximated with less than +10 % error as

$$\varphi = \sqrt{9\left(\frac{\hat{i}_{(1)}}{\hat{i}_{\mathrm{fb}(3)}}\right)^2 + 2} - 3\frac{\hat{i}_{(1)}}{\hat{i}_{\mathrm{fb}(3)}}. \tag{3.50}$$

Filter Stage Time Constant

Since only the product $\prod_{k=1}^{N} L_k C_k$ of all filter stages is relevant for the asymptotic attenuation of a filter with a certain number of stages at a certain frequency and not its distribution to the values L_k, C_k of the individual stages, the geometric average filter stage (cut-off) time constant

$$T_\mathrm{c} = \left(\prod_{k=1}^{N} L_k C_k\right)^{\frac{1}{2N}} \tag{3.51}$$

which expresses this product is defined. To reach an attenuation A at a frequency ω with a N-stage filter, a filter stage time constant $T_\mathrm{c} = \frac{A^{\frac{1}{2N}}}{\omega}$ is required. Therefore, for sufficient DM QP filter attenuation at least a filter stage time constant

$$T_\mathrm{c,qp,dm} = \max_{\omega} \left(\frac{1}{\omega} \left(2 \frac{u_\mathrm{m,qp}(u_\mathrm{ra}, \omega)}{u_\mathrm{max,qp}(\omega)} \right)^{\frac{1}{2N_\mathrm{dm}}} \right) \tag{3.52}$$

is required. Since this only includes the DM part of the noise spectrum, twice the detected voltage $u_\mathrm{m,qp}$ is used in this expression to leave half of the available noise amplitude for the CM contribution. This is a worst case approximation considering the case that DM and CM noise voltages are in phase. For sufficient DM AVG filter attenuation at least a filter stage time constant

$$T_\mathrm{c,avg,dm} = \max_{\omega} \left(\frac{1}{\omega} \left(2 \frac{u_\mathrm{m,avg}(u_\mathrm{ra}, \omega)}{u_\mathrm{max,avg}(\omega)} \right)^{\frac{1}{2N_\mathrm{dm}}} \right) \tag{3.53}$$

is necessary. Furthermore, the cut-off frequency of all filter stages has to be well below the switching frequency. Assuming a factor of four between switching frequency and filter cut-off frequency and that the cut-off frequencies of all filter stages are equal, a minimum filter stage time constant

$$T_\mathrm{c,min} = \frac{4}{2\pi f_\mathrm{s}} \tag{3.54}$$

is required. Therefore, to comply with both QP and AVG limits and leave sufficient margin between filter cut-off and switching frequency the minimum DM filter stage time constant is

$$T_\mathrm{c,dm} = \max(T_\mathrm{c,min}, T_\mathrm{c,qp,dm}, T_\mathrm{c,avg,dm}). \tag{3.55}$$

By replacing *dm* with *cm* in the indices of expressions (3.52)-(3.55) and u_ra with u_rm in (3.52) and (3.53) the expressions can be used to determine the CM filter stage time constant as well.

Number of Filter Stages

Before going into detail on how to determine the component values L_k, C_k of the individual stages the optimum number of filter stages shall be discussed. If it is assumed that the component values of all filter stages are equal, i.e. $L_k = L$ and $C_k = C$, the values L and C are proportional to the filter stage time constant T_c. In order to minimize volume, loss and cost of the filter it is usually a good idea to minimize $\sum_k L_k$ and $\sum_k C_k$ which, under the given assumptions is achieved by sweeping the number of filter stages N to find the minimum

$$\min_N (N T_\mathrm{c}) \Rightarrow N_\mathrm{opt}, T_\mathrm{c,opt}. \tag{3.56}$$

Determining this optimum number of stages N_opt and the corresponding filter stage time constant $T_\mathrm{c,opt}$ can be a time consuming task. For three-level rectifiers (or inverters) operating in CCM only this process has been carried out for a DC-link voltage of 800 V and all switching frequencies in the range from 1 kHz to 10 MHz. The resulting product $N_\mathrm{opt} T_\mathrm{c,opt}$ is shown in Fig. 3.38. The modulation index has been swept within the possible range, considering the worst case. The indicated DM filter designs found in literature closely agree with the number of stages and the required filter stage time constant. The filter stage time constant is determined for a filter stage structure with separate DM and CM filter (Fig. 3.36a) as it is also used for the prototype and for a combined DM&CM filter (Fig. 3.36b). For the combined filter structure $N T_\mathrm{c}$ is shown as solid line, for the separate filter structure the dashed line indicates $N_\mathrm{dm} T_\mathrm{c,dm}$ and the dotted line indicates $N_\mathrm{cm} T_\mathrm{c,cm}$. If both CCM and the proposed DCM control scheme shall be used the filter needs to exhibit a filter stage time constant as shown in Fig. 3.39. Compared to Fig. 3.38 a higher DM filter stage time constant is necessary if the proposed DCM control scheme is used and the switching frequency is higher than 150 kHz.

For reference also the necessary filter stage time constants for multilevel rectifiers/inverters with 1,2,4 and 8 interleaved bridge legs (realized either as flying capacitor or coupled inductor as shown in Fig. 3.40) are provided in Fig. 3.41.

This analysis shows that the optimum number of filter stages, i.e. the number of stages with the lowest total amount of inductance and capacitance, is increasing with increasing switching frequency. Up to $\approx$ 10 kHz a single-stage filter is sufficient, followed by two-stage filters

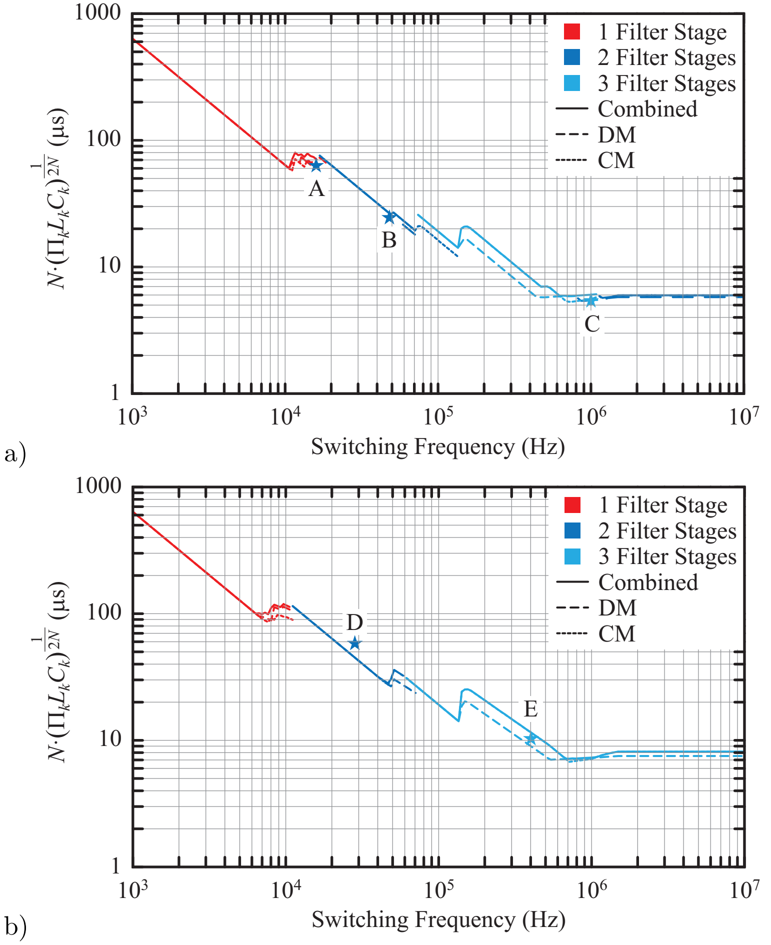
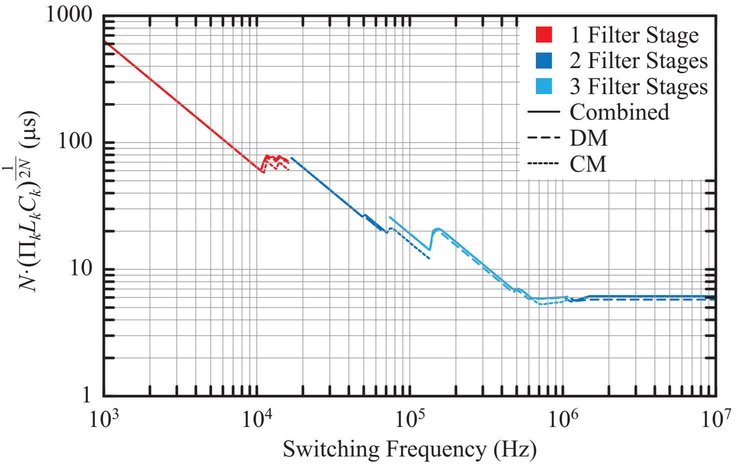
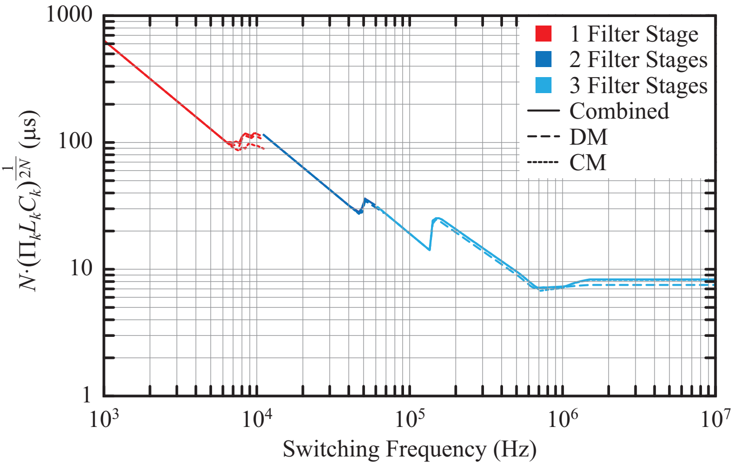


Fig. 3.38: Optimum number of filter stages (indicated by color) and minimum required filter stage time constant multiplied by the number of stages for three-level rectifiers or inverters operating in CCM with 800 V DC-link voltage for CISPR Class A (a) and Class B (b). Stars indicate DM filter designs found in literature (A, [51]; B, [52]; C, [53]; E, [54]) and the filter designed in this work (D).



a)



b)

Fig. 3.39: Optimum number of filter stages (indicated by color) and minimum required filter stage time constant multiplied by the number of stages for three-level rectifiers operating in both DCM and CCM with 800 V DC-link voltage for CISPR Class A (a) and Class B (b).

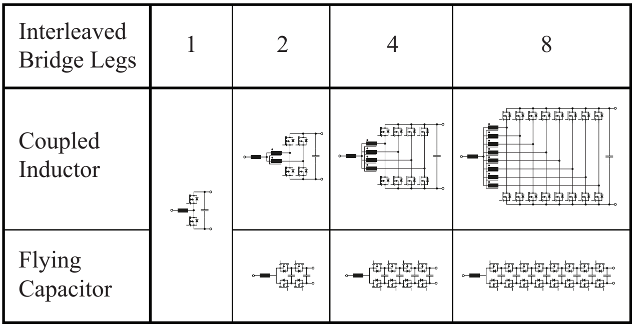


Fig. 3.40: Circuits of multi-level half-bridges using multiple interleaved two-level half-bridges either in parallel, using a coupled inductor, or in series, using flying capacitors.

up to $\approx$ 60 kHz and three-stage filters for even higher switching frequencies. The filter volume is decreasing approximately with $\frac{1}{f_\mathrm{s}}$, except for some bumps when a switching frequency harmonic reaches 150 kHz. At $\approx$ 700 kHz the noise floor of $\approx$ 110 dBµV caused by the carrier side bands defines the required filter stage time constant [53]. Exceeding the switching frequency above this limit, therefore, does not reduce the filter stage time constant further. However, increasing the switching frequency still reduces the losses in the boost inductor.

Component Values

After the filter stage time constants $T_\mathrm{c,dm}$ and $T_\mathrm{c,cm}$ and the numbers of stages N_dm and N_cm are determined, the individual component values can be defined. First the maximum value of DM capacitance per phase

$$C_\mathrm{dm,tot} = \frac{Q_\mathrm{max}}{2\pi f_\mathrm{l,max} U^2_\mathrm{ac,max}} \tag{3.57}$$

is determined by specifying the maximum reactive power Q_max that the filter is allowed to consume during no load conditions at the maximum line-to-line RMS voltage $U_\mathrm{ac,max}$ and the maximum mains frequency $f_\mathrm{l,max}$. Specifying $Q_\mathrm{max} = 5\,\%P_\mathrm{max}$ for the prototype system with 480 V/60 Hz a maximum total DM capacitance of 37 µF results. With the boost inductance $L_\mathrm{dm1} = 44\,\mu\mathrm{H}$ obtained from the optimization in Sec. 2.4.3 and the filter stage time constant $T_\mathrm{c} = 25\,\mu\mathrm{s}$ as read

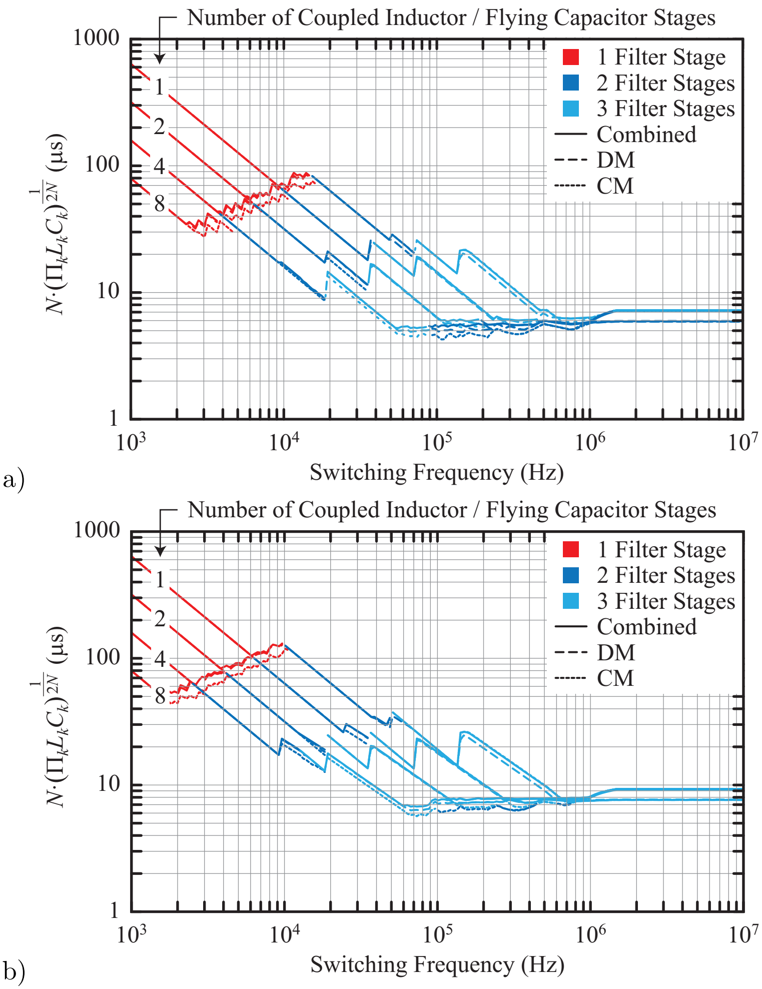


Fig. 3.41: Optimum number of filter stages (indicated by color) and minimum required filter stage time constant multiplied by the number of stages for two-level rectifiers or inverters operating in CCM with 800 V DC-link voltage for CISPR Class A (a) and Class B (b) with different numbers of interleaved bridge legs.

from Fig. 3.39b for a switching frequency of 28 kHz the DM capacitance of the first filter stage is obtained as

$$C_{\mathrm{dm1}} = \frac{T_{\mathrm{c}}^2}{L_{\mathrm{dm1}}} = 14\,\mu\mathrm{F}. \tag{3.58}$$

The remaining DM capacitance would be distributed equally in case of a three-stage filter. However, for the given switching frequency $N_{\mathrm{dm}} = 2$ results from Fig. 3.39b and thus

$$C_{\mathrm{dm2}-N_{\mathrm{dm}}} = \frac{C_{\mathrm{dm,tot}} - C_{\mathrm{dm1}}}{N_{\mathrm{dm}} - 1} = 23\,\mu\mathrm{F}. \tag{3.59}$$

The remaining DM inductance(s)

$$L_{\mathrm{dm2}-N_{\mathrm{dm}}} = \frac{T_{\mathrm{c}}^2}{C_{\mathrm{dm2}-N_{\mathrm{dm}}}} = 27\,\mu\mathrm{H} \tag{3.60}$$

follow from the filter stage time constant. Since the filter stage time constant is selected such that each filter stage cut-off frequency is a factor of four lower than the switching frequency (3.54), the asymptotic approximations (3.48) can be applied which are only determined by the product of all filter inductances and capacitances [41].

For the design of the CM filter the total CM capacitance connected to the outputs C_{m} is selected such that the maximum phase shift is not exceeded at maximum mains voltage $U_{\mathrm{ac,max}}$, mains frequency $f_{\mathrm{l,max}}$ and 10 % load. According to (3.6) the maximum phase shift $\varphi_{\mathrm{max}} = 2.3°$ results. Therefore, according to (3.50) the ratio

$$\frac{\hat{i}_{\mathrm{fb(3)}}}{\hat{i}_{(1)}} = \frac{6\varphi}{2 - \varphi^2} \approx 0.12 \tag{3.61}$$

must not be exceeded in the given case. From (3.49), the maximum filter capacitance connected to the DC-link results as

$$C_{\mathrm{m}} = \frac{2}{3\pi f_{\mathrm{l}} R} \frac{\hat{i}_{\mathrm{fb(3)}}}{\hat{i}_{(1)}} \approx 5\,\mu\mathrm{F}. \tag{3.62}$$

The value of the first CM inductance usually is a result of the number of turns optimization for minimum losses for the given core. For the sake of a simple mechanical construction the same core size (2 × F3CC8) as for the DM choke is selected but with nano-crystalline instead of amorphous tape. With the optimum number of turns an inductance of $L_{\mathrm{cm1}} = 500\,\mu\mathrm{H}$ results. With the filter stage time constant $T_{\mathrm{c,cm}} = 25\,\mu\mathrm{s}$ from Fig. 3.39b, the CM capacitance of the first stage

$$C_{\mathrm{cm1}} = \frac{T_{\mathrm{c,cm}}^2}{L_{\mathrm{cm1}}} \approx 1.25\,\mu\mathrm{F} \tag{3.63}$$

is obtained. The remaining capacitance is distributed to the remaining $N_{\mathrm{cm}} - 1$ stages, with N_{cm} according to Fig. 3.39b. Therefore,

$$C_{\mathrm{cm2}-N_{\mathrm{cm}}} = \frac{C_{\mathrm{m}} - C_{\mathrm{cm1}}}{N_{\mathrm{cm}} - 1} = 3.75\,\mu\mathrm{F}. \tag{3.64}$$

The remaining CM inductance(s)

$$L_{\mathrm{cm2}-N_{\mathrm{cm}}} = \frac{T_{\mathrm{c,cm}}^2}{C_{\mathrm{cm2}-N_{\mathrm{dm}}}} = 167\,\mu\mathrm{H} \tag{3.65}$$

follow from the filter stage time constant. Finally, after some manual tweaking in order to reach compact dimensions of the filter, the component values indicated in Fig. 3.42a are used. Although the prototype is built with the CM capacitors connected to the midpoint as shown in 3.42a, it is recommended to connect the CM capacitors to the outputs instead as shown in 3.42b in order to avoid the CM noise contribution of the midpoint current (see Sec. 3.4.2).

3.5 Experiments

The prototype constructed for the experiments is optimized for the high peak, low average load scenario of an X-ray system as shown in Fig. 3.1. The specifications of the system are provided in Tab. 3.3. The wide input voltage range is required since the system shall be used with weak grids even at 20 % under-voltage and with 10 % over-voltage with 400 V or 480 V nominal voltage. Although the application only requires the full power for 2.3 s and only 800 W continuously, for better comparability the system is thermally designed for full power continuous operation. Thus, for the actual application the semiconductor heat sink could be much smaller. The inductor size however is determined by a TCO optimization which considers the loss energy cost during the

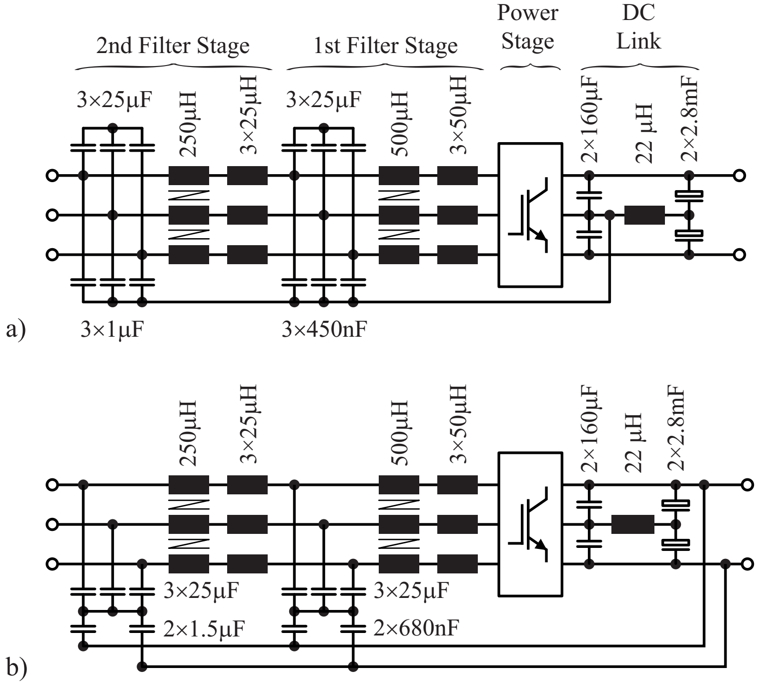

Power
Stage
DC
Link
2nd Filter Stage
1st Filter Stage
3×25μF
250μH
3×25μH
3×25μF
500μH
3×50μH
2×160μF
22 μH
2×2.8mF
a)
3×1μF
3×450nF
250μH
3×25μH
500μH
3×50μH
2×160μF
22 μH
2×2.8mF
3×25μF
2×1.5μF
3×25μF
2×680nF
b)

Fig. 3.42: Structure and component values of the EMI filter of the prototype with CM capacitors connected to the midpoint (a) and proposal to improve CM attenuation by connecting CM capacitors to the outputs (b). In order to reach a compact filter design, components with the same height are selected, resulting in higher than necessary DM capacitance. The DC-link is realized using a combination of film capacitors and electrolytic capacitors with a small inductance connecting the two midpoints that reduces the RMS current in the electrolytic capacitors.

Tab. 3.3: Prototype Specifications

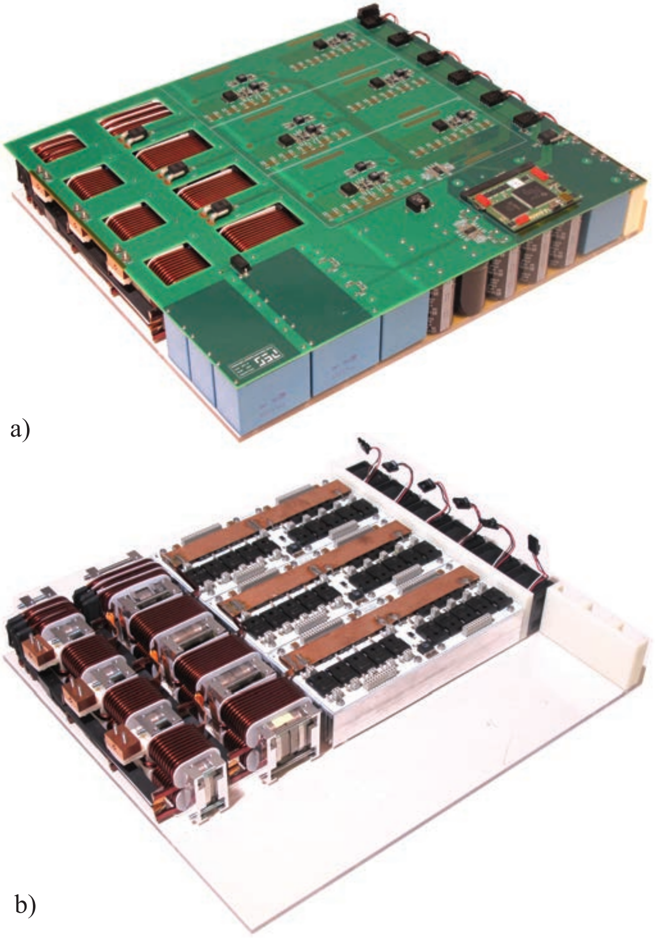
Input Voltage Range	290 V - 530 V
Output Voltage	800 V
Output Power	65 kW
Ambient Temperature	45 °C

expected system life time of 20 years, assuming that pulses with full power are generated during 4 h each day and pulses with 20 % power are carried out also during 4 h per day. Because of the low average power of 800 W this results in 360 operating hours at 65 kW and 1800 operating hours at 13 kW. In order to allow sufficient cooling, the semiconductors are directly soldered to aluminium core PCBs (isolated metal substrate) which are mounted to the heat sinks as shown in Fig. 3.43b. Helically wound rectangular conductor profile windings are used for boost and filter inductors due to the excellent filling factor and high-frequency performance of this type of winding and also since they allow efficient cooling. The inductors are connected using busbars in order to avoid that the input currents, which can amount to up to 135 A RMS at the lowest input voltage, are conducted through the PCB which only carries the DC output currents.

3.5.1 Switching Period Waveforms in DCM

The measured waveforms of boost inductor current and rectifier input voltage for a mains voltage angle of 10° (phase displacement relative to the start of the 30° sector $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$) at 4.8 kW with 400 V line-to-line RMS input voltage and 800 V DC output voltage are shown in Fig. 3.44. The measurement shows a switching period of pattern A followed by a switching period with pattern B, the selection of the switching pattern is performed by the DSP in order to balance the output voltages according to Tab. 3.2. In pattern A phase c, the one with middle absolute voltage, is turned off first, in pattern B phases a and c are turned off before phase b, the one with minimum absolute value. During the current zero interval ringing of the IGBT output capacitance with the boost inductance is observed which is initiated by the reverse recovery current of the free-wheeling diode.

Displaying the measured data of the boost inductor currents with


a)

b)

Fig. 3.43: 65 kW/28 kHz VR prototype used for the measurements to verify the proposed DCM control scheme (a) and inside view showing CM and DM inductors of the two-stage EMI filter (including the boost inductors) and semiconductors mounted to the heat sink using isolated metal substrate PCBs (b). Width × length × height = 33.6 cm × 37.4 cm × 5.4 cm (13.2 in × 14.7 in × 2.13 in), power density $\varrho = 9.56\,\mathrm{kW/dm^3}$ ($157\,\mathrm{W/in^3}$).

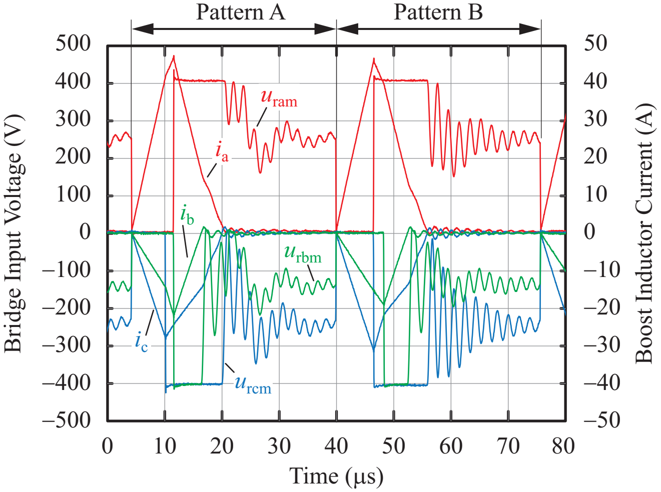


Fig. 3.44: Measured waveforms of the boost inductor currents and the rectifier input voltages with reference to the DC-link midpoint at the mains voltage sector $u_{\text{a}} > 0 > u_{\text{b}} > u_{\text{c}}$ with 4.8 kW output power, 400 V line-to-line RMS input voltage and 800 V DC output voltage.

switching pattern A in α,β-coordinates results in the trajectory shown in Fig. 3.45a and for pattern B in the trajectory shown in Fig. 3.45b. The switching state of each part of the trajectory is indicated. During state $\boxed{1}$ the boost inductor current space vector moves from the origin into the direction of the mains voltage space vector. As can be seen the local average of the measured boost inductor current space vector $\langle \underline{i} \rangle$ is located on this part of the trajectory and therefore has the same angle as the mains voltage space vector, indicating that the desired resistive behaviour is achieved.

The controller used is a TI TMS320f28335 DSP which calculates the duty cycles in DCM using four look-up tables created offline using the expressions (3.33),(3.34),(3.31) and (3.32) evaluated for 12 values of m_{max} and 7 values of m_{min}. Bilinear interpolation is carried out on the DSP to reduce the error when retrieving values from the look-up tables.

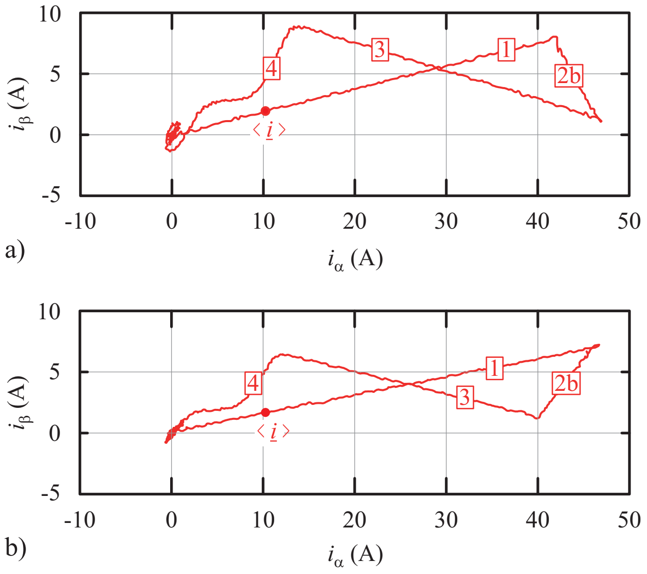


Fig. 3.45: Measured trajectories of the boost inductor currents with pattern A (a) and pattern B (b) displayed in α,β-coordinates and the local average of each trajectory $\langle \underline{i} \rangle$ at the mains voltage sector $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$ with 4.8 kW output power, 400 V line-to-line RMS input voltage and 800 DC output voltage.

3.5.2 Load Step Response

The high-voltage generator which is connected to the DC-link of the rectifier usually applies load pulses with durations ranging from 1 ms to 2.3 s at full power. Continuous load only applies with 800 W or less. The controller is implemented in the cascaded structure as described in Section 3.2.2. The outer loop contains the DC-link voltage controller which sets the resistance to be emulated to the mains by the current controller, using the output current measurement for feed-forward. In CCM the boost inductor currents are closed loop controlled using the input voltage measurements for feed-forward; in DCM, however, they are open loop controlled as described in Section 3.3. A measured load pulse with 13 kW output power and 100 ms duration at 400 V mains voltage with 800 V output voltage set value is shown in Fig. 3.46. As can be seen the rectifier is still operating in DCM at this power level, although it is close to the threshold to CCM since the input current local average is almost half the peak value of the boost inductor current. At full power, the rectifier is operating in CCM, the load pulse measured for this situation is shown in Fig. 3.47. The output voltage shows an under- and overshoot of $\approx 5\,\%$ at the beginning respectively the end of the load pulse. A negligible low-frequency output voltage ripple is observed during the pulse, caused by the non-constant power flow resulting for the resistive behaviour of the rectifier with not perfectly sinusoidal mains voltages.

3.5.3 Input Current THD

With the applied control schemes, the input currents in DCM and in CCM are ideally proportional to the phase voltages. Therefore, the input current THD is ideally the same as the voltage THD. However, in CCM the THD increases if the load is reduced due to two reasons. First, the DCM occurring at the current zero crossings causes disturbances in the current control loop due to inaccurate current measurements and the change in duty cycle voltage relationship. Second, the necessary low-pass filtering of the input voltage measurements leads to a difference between the actual and the feed-forwarded input voltage, in particular if the input voltage THD is high. This error in the feed-forwarded input voltage acts as disturbance in the current control loop. Both reasons combined lead to the increase in current THD in CCM at light load. With a mains voltage THD of 2.2 %, the measured input current THD is shown

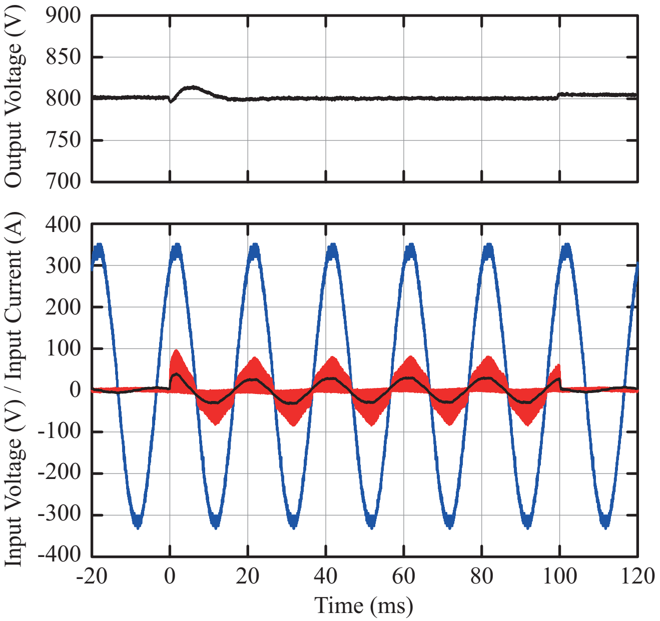


Fig. 3.46: Measured waveforms of input voltage, boost inductor current and mains current of one phase in DCM using both patterns A and B according to Tab. 3.2 during a 100 ms load pulse with 13 kW output power (no load otherwise) at 400 V mains voltage and 800 V output voltage.

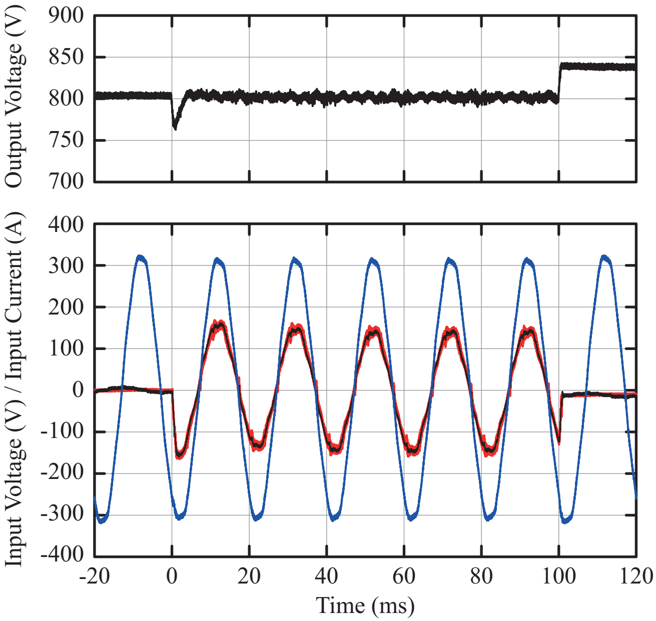


Fig. 3.47: Measured waveforms of input voltage, boost inductor current and mains current of one phase in CCM during a 100 ms load pulse with 65 kW output power (no load otherwise) at 400 V mains voltage and 800 V output voltage.

in Fig. 3.48. At 400 V line-to-line RMS voltage, 800 V output voltage and 66 kW load the input current THD amounts to 4.5 %. In order to be able to use a linear three-phase AC power source that provides 0.4 % voltage THD but features only 20 kW output power, the power is reduced to $\frac{1}{4}$ of the rated value using 200 V line-to-line RMS voltage and 400 V output voltage. Since the load impedance represented to the mains remains unchanged, the relative current ripple is the same as with full power and nominal voltages. In this case with 16.5 kW load, which represents the full-load condition, the input current THD is reduced to 2.7 %.

At load levels of 15 kW or less the rectifier can be operated using the closed loop CCM current control or the proposed open loop DCM control scheme (dashed line). The improvement of the input current THD with the proposed control scheme is significant, allowing to reduce the input current THD at nominal voltages and 15 kW from 26.9 % to 6.5 % with 2.2 % input voltage THD and with half the nominal voltages and 3.75 kW load at 0.4 % voltage THD from 21 % to 3.5 %.

At medium power levels the input current THD however is still high, owing to the synchronous sampling with twice the switching frequency. In order to reduce the THD further without increasing the value of the boost inductance or the switching frequency would require changes to the hardware such as using ADCs with higher sampling rates.

3.5.4 Conducted EMI Measurement

From the simulations discussed in Section 3.4.2 it is expected that the noise emission in DCM is lower than in CCM due to the lower CM noise level. The measurements shown in Fig. 3.49 taken at 5 kW in DCM and at 20 kW in CCM with nominal voltages basically confirm this statement except for the frequency range from 400 kHz to 600 kHz. This is explained by the oscillation of the output capacitance of the IGBTs with the boost inductance in DCM as it is observed in Fig. 3.44, which is taking place at a frequency of ≈ 500 kHz. The power level for CCM operation had to be selected higher than the one for DCM operation to make sure the converter actually operates fully in CCM and no unwanted DCM as in Fig. 3.18 occurs. Except for the noise emissions due to the parasitic ground capacitances of the IGBTs which are determined by the $\frac{\mathrm{d}v}{\mathrm{d}t}$ of the switching edges, the noise emission does not depend on the power level in CCM. Initially a two-stage DM and CM filter has been designed as shown in Fig. 3.50. In the initial design process the

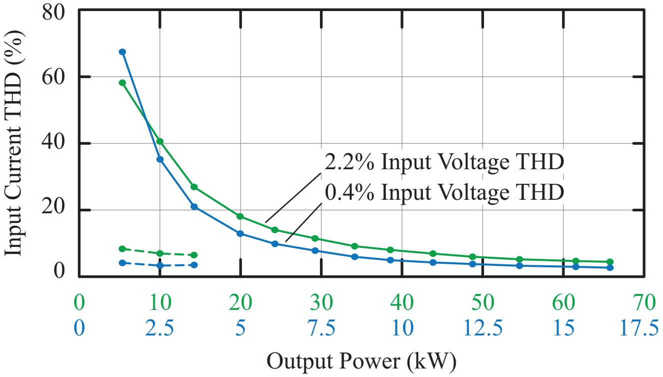


Fig. 3.48: Measured mains current THD at nominal voltage (green: 400 V line-to-line input voltage, 800 V output voltage) with 2.2 % voltage THD and at half nominal voltage (blue: 200 V line-to-line input voltage, 400 V output voltage) with 0.4 % voltage THD. Solid lines indicate measurements taken with closed loop CCM current control, dashed lines with the proposed open loop DCM current control.

contribution of the midpoint current to the CM noise (see Fig. 3.33c) and the reduction in permeability of the nano-crystalline cores for frequencies higher than 100 kHz which were not considered. Therefore, an additional toroidal CM inductor of 390 µH had to be added at the mains side of the filter to comply with CISPR Class A. To reach the intended Class B compliance a redesign with the filter structure as proposed in Fig. 3.42b is necessary.

3.5.5 Loss Distribution and Efficiency

Operation of the VR with the proposed DCM scheme has two major effects on the losses. First, turning on the switches at the same time, leads to a higher DM voltage component at switching frequency and thus to a higher current ripple. The helical windings used for the boost inductors suffer from a high AC resistance to DC resistance ratio at switching frequency, which amounts to $\frac{R_\mathrm{ac}(28\,\mathrm{kHz})}{R_\mathrm{dc}} \approx 38$ according to a FEM simulation. While, this is acceptable in CCM due to the low current ripple, the high current ripple in DCM leads to a significant increase in winding loss. This effect is observed in the calculated loss distribution shown in Fig. 3.51 for the operating point at 13 kW which

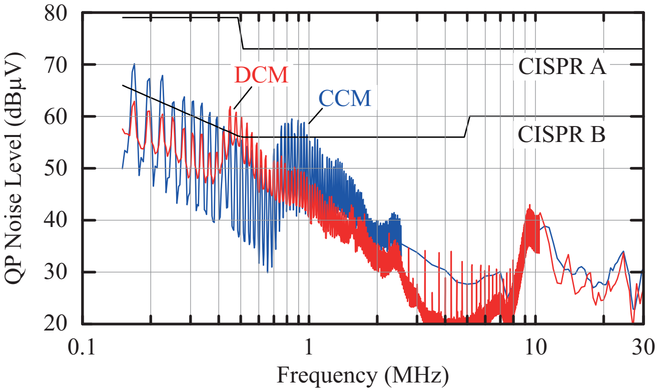


Fig. 3.49: Measured CISPR QP noise level at nominal voltages and a load of 20 kW in CCM and 5 kW in DCM. The measurements are conducted using an additional 390 µH CM inductor at the mains side of the filter to compensate for the loss of permeability of the nano-crystalline inductors at high frequencies not considered during the filter design.

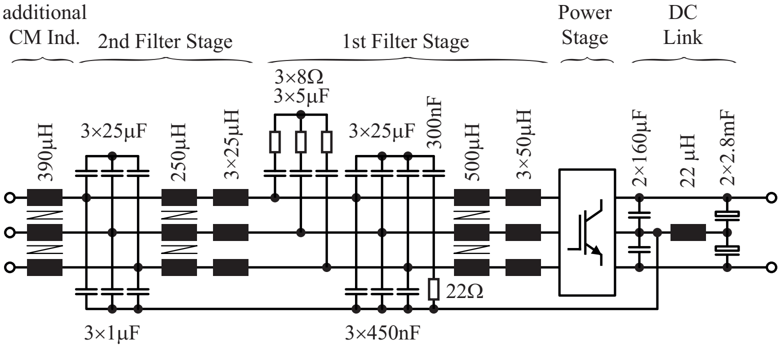

additional CM Ind.
2nd Filter Stage
1st Filter Stage
Power Stage
DC Link
390µH
3×25µF
250µH
3×25µH
3×8Ω
3×5µF
3×25µF
300nF
500µH
3×50µH
2×160µF
22 µH
2×2.8mF
22Ω
3×1µF
3×450nF

Fig. 3.50: Structure and component values of the two-stage CM and DM EMI filter of the prototype using a capacitive CM return path to the DC-link midpoint with damping resistors. The additional CM inductor at the mains side of the filter is necessary to comply with CISPR Class A.

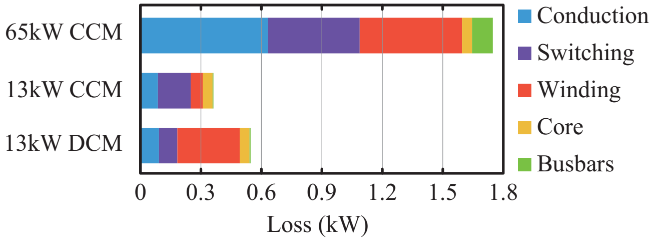


Fig. 3.51: Loss distribution at nominal voltages (400 V line-to-line RMS input voltage, 800 V output voltage) for selected operating points.

is shown for CCM and DCM operation. On the other hand in CCM the CM voltage component is higher. Because of the high CM inductance virtually no CM current ripple is observed, but the higher CM voltage causes higher core losses in the CM inductor of the first filter stage than in DCM. The core losses in the DM inductors are however higher in DCM than in CCM due to the higher DM voltage component in DCM. Therefore, in DCM, the core losses are shifted from the CM inductor of the first filter stage into the boost inductors and, according to the calculations presented in Fig. 3.51, remain approximately the same in total. The second effect on the losses in DCM concerns the switching losses. Since the transistors are turned on at zero current lower turn-on losses result compared to CCM. Since the turn-on losses are higher than the turn-off losses with the IGBTs [55] and the free-wheeling diodes [56] used, the total switching losses in DCM are lower than in CCM as shown in Fig. 3.51. The measured efficiency at nominal voltages depending on the load is shown for CCM and DCM in Fig. 3.52 and compared to the calculated values. The calculations are based on data sheet values for forward voltage drop and switching losses of the semiconductors, core loss data provided by the manufacturers adapted for the actual flux density waveform using the iGSE [34] and FEM simulations of the windings for the AC resistance to DC resistance ratio. With CCM the measured efficiency fits the calculated value with less than 0.3 % deviation at medium to high load reaching 97.2 % at full-load and a peak of 97.6 % at 24 kW. At low load the error with CCM control is growing which can be explained by the partially occuring DCM in this region not covered by the loss model. With the proposed open loop DCM control scheme the measured efficiency is lower by up to 1.3 % due to the

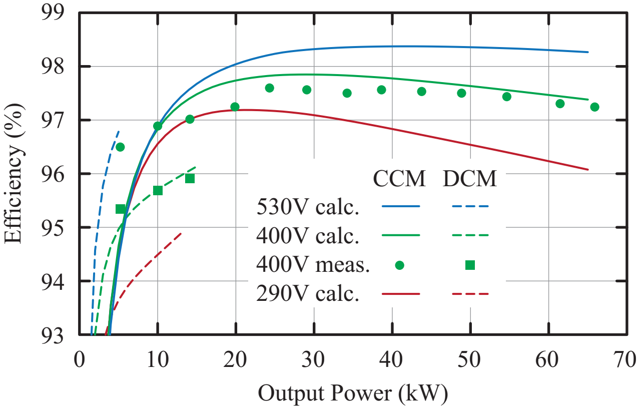


Fig. 3.52: Measured efficiency in DCM and CCM compared to the calculated values as function of the output power with nominal output voltage of 800 V.

increased current ripple. Temperature measurements are carried out using a infrared camera. The first filter stage inductor temperatures demonstrate the effect of high DM voltage with DCM control and high CM voltage with CCM control. With 10 kW in DCM the thermal image is shown in Fig. 3.53. Due to the high current ripple the DM inductor windings heat up to 97 °C in the vicinity of the airgap, which is relatively wide with 4.5 mm. The CM inductor (L_{dm1}) in this situation only heats up to 46 °C winding temperature. In CCM with 32 kW output power the picture changes as shown in Fig. 3.54. As expected the higher CM voltage causes the CM inductor core to heat up to 87 °C, due to the low current ripple the temperature of the DM inductor winding drops to 61 °C even though the load is higher than in the situation of Fig. 3.53. The heatsink temperature at 32 kW is still low with 47 °C at 25 °C ambient temperature. However, power levels higher than 40 kW could not be tested in continuous operation since the PCB close to the DC terminals would have heated up excessively.

3.6 Summary of the Chapter

It has been shown that an open loop DCM current control scheme for the VR exists, that allows resistive DCM mains behaviour. The expressions for the duty cycles can be derived analytically and are suitable for

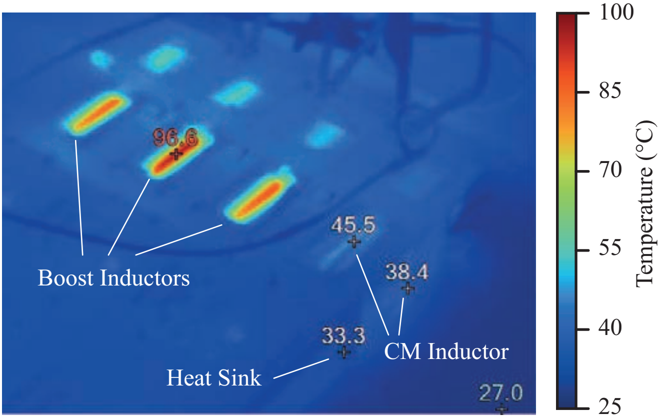

96.6
45.5
38.4
33.3
27.0
Boost Inductors
CM Inductor
Heat Sink
100
85
70
55
40
25
Temperature (°C)

Fig. 3.53: Thermal image of the prototype running at 10 kW in DCM with nominal voltages. The hotspots are observed at the windings of the boost inductors near the airgap due to the high DM current ripple. The CM inductor and the heat sink temperatures are low.

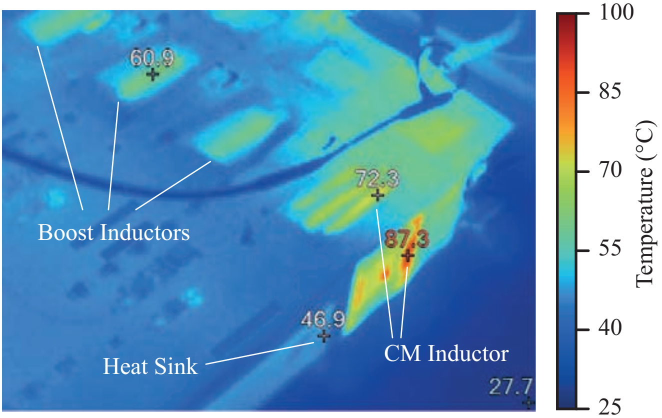

60.9
72.3
87.3
46.9
27.7
Boost Inductors
CM Inductor
Heat Sink
100
85
70
55
40
25
Temperature (°C)

Fig. 3.54: Thermal image of the prototype running at 32 kW in CCM with nominal voltages. The hotspot is moved to the core of the CM inductor (L_{dm1}), due to the higher CM voltage amplitude in CCM.

hardware implementation using look-up tables. Simulations and measurements show that a substantial reduction of input current THD is possible at light load, which for the prototype with $\approx 25\,\%$ inductor current ripple at nominal load can be considered as less than $20\,\%$ of nominal load. Compared to conventional PI current control the proposed DCM control scheme achieves a THD reduction from $20\,\%$ to less than $5\,\%$. The proposed control scheme does not rely on current measurements. Therefore, it is not necessary to resolve the actual local average of the inductor current in DCM. Other than common light load handling approaches, such as burst mode operation or increasing the switching frequency at light load, the proposed control scheme allows to operate continuously, therefore with minimum output voltage ripple, and due to the constant switching frequency the requirements for the EMI filter are not affected if the switching frequency is less than the CISPR threshold of 150 kHz. If the switching frequency is higher, 7.4 dB more DM attenuation is required. Balancing of the output voltages is possible with the proposed control scheme by selecting the appropriate pattern from two redundant switching patterns and for typical modulation indices a DC current of $10\,\%$ of the phase current RMS value can be delivered to the DC-link midpoint. The higher current ripple of the proposed control scheme leads to higher HF winding losses in the inductors of the first filter stage. However, zero current turn-on reduces the switching losses. The proposed control scheme is implemented and verified on a 65 kW prototype optimized for pulse load reaching $97.2\,\%$ efficiency at nominal load and $9.56\,\mathrm{kW/dm^3}$ power density using only low-cost Si components with 28 kHz switching frequency.

4

High Bandwidth Non-Resonant High Voltage Generator

X-RAY tubes used for diagnostic purposes require accelerating voltages of up to 150 kV but are at the same time relatively inefficient. Therefore, the power demand of medical X-ray tubes ranges from a few kW for dental imaging to more than 100 kW for CT applications. Due to the surrounding vacuum, the cooling capability of the tube is limited and thus also the average power that needs to be provided by the high-voltage supply is typically less than 1 kW. Consequently the high-voltage transformer is usually not constructed for continuous full power operation. Instead high power density transformer designs are common, resulting in a relatively high leakage inductance due to the high number of turns and the required winding isolation distance.

Despite the high output voltage, high power transfer and high transformer leakage inductance fast output voltage dynamics are desired. Short output voltage rise- and fall times also allow short pulses to be generated which is beneficial to reduce the patient dose in pulsed fluoroscopy [57] and enables single source DECT [58, 59].

Although recent achievements in SiC semiconductor technology offer diode breakdown voltages up to 35 kV [60, 61], the secondary side of the high-voltage DC-DC converter is typically involving multiple diode rectifier stages connected in series in order to reduce the winding capacitance. Therefore, topologies employing transistors on the secondary side are not feasible due to the excessive gate driver and isolation circuit overhead. The only way to achieve a short fall-time of the output voltage with unidirectional topologies is to reduce the output capacitance. For a given voltage ripple specification this can be achieved by increas-

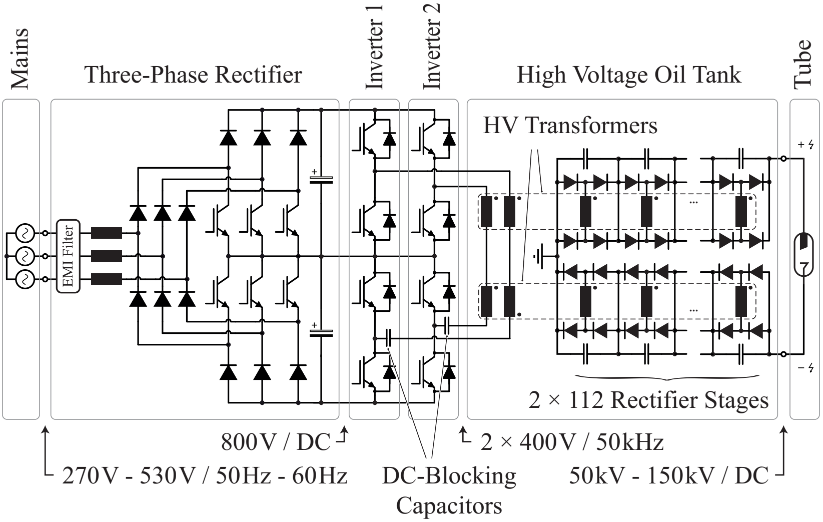

Mains
Three-Phase Rectifier
Inverter 1
Inverter 2
High Voltage Oil Tank
Tube
HV Transformers
EMI Filter
+
−
2 × 112 Rectifier Stages
800V / DC
2 × 400V / 50kHz
270V - 530V / 50Hz - 60Hz
DC-Blocking Capacitors
50kV - 150kV / DC

Fig. 4.1: Circuit of the proposed high-voltage generator, consisting of a wide input voltage range active three-phase mains rectifier, providing a stabilized DC voltage for two interleaved inverters, feeding two transformers, each equipped with 112 series connected secondary winding-rectifier units, supplying up to 150 kV and up to 60 kW to the X-ray tube.

ing the switching frequency or by using interleaving [10]. Therefore, in order to reach a high switching frequency a low switching loss Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) topology is required for the high-voltage generator. Besides providing the possibility of interleaving, the circuit needs to work with high transformer leakage inductance, and should exhibit favorable dynamics for output voltage control.

In this Chapter a coupled interleaved variant of the single active bridge converter (CISABC) is proposed that meets these demands. In Section 4.1 the topology is derived first from the uncoupled interleaved single active bridge converter (ISABC) and the steady state operation is analysed in detail. Experimental results obtained on a full-scale hardware prototype are provided in Section 4.4 verifying the analysis. Analytic expressions for the duty cycle - output current relationship are given in the Appendix.

4.1 Steady-State Analysis

The complete circuit of the high-voltage generator proposed in this work is shown in Fig. 4.1 together with an active three-phase rectifier providing a stabilized DC-link voltage to the inverter and sinusoidal input currents to the mains [62]. At the primary side each of the two inverters, which are operating with 90° phase shift, feeds a series connection of two primary windings, wound on two different transformer cores. Each inverter consists of two series connected half-bridges which, with an additional DC-blocking capacitor, are working as a full-bridge. The separation and series connection of the half-bridges is advantageous for the given application, since it allows the use of low switching loss, low-cost 650 V IGBTs for the inverters. At the secondary side each of the two transformers uses 112 secondary windings, each connected to an individual rectifier stage. As for diode split transformers used in CRT monitors this approach reduces the AC winding capacitance to a negligible value [63]. The winding capacitance is therefore not considered in the analysis and an equivalent secondary winding is used for the following circuit analysis. The proposed high-voltage generator uses a coupled interleaved version of the Single Active Bridge Converter (SABC). Before analysing the steady-state operation of the CISABC in detail the ISABC, i.e. the converter without the additional coupling of the CISABC is analysed.

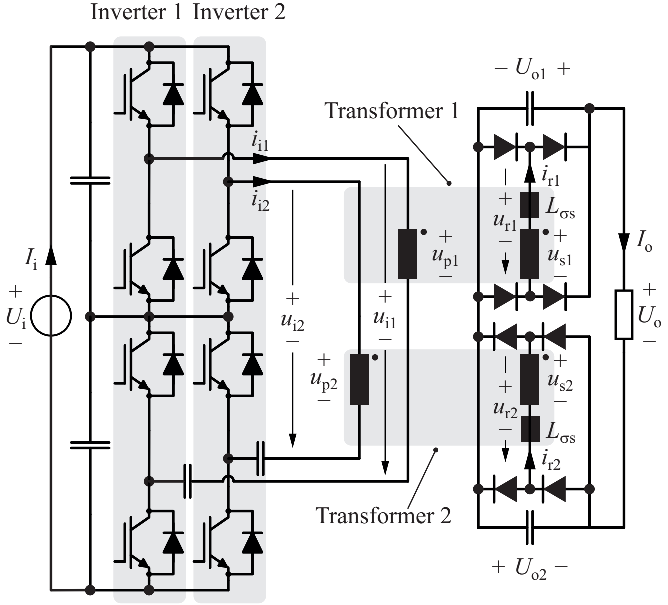


Fig. 4.2: ISABC circuit in Input Parallel Output Series (IPOS) configuration with the two half-bridges of each full-bridge inverter distributed on two split DC-links and two full-bridge diode rectifiers connected to two series connected DC-links on the secondary side, linked via two transformers with leakage inductances $L_{\sigma s}$ (reflected to the secondary side).

4.1.1 Interleaved Single Active Bridge Converter

The circuit of the ISABC is shown in Fig. 4.2, consisting of two full-bridge inverters at the primary and two full-bridge diode rectifiers at the secondary side. The two half-bridges of each inverter are distributed on the two parts of the primary DC-link, using DC-blocking capacitors. Therefore, the two inverters can be considered as parallel connected. The two rectifiers are connected to two series connected DC-links at the secondary side. Therefore, an Input Parallel Output Series connection results. Each of two independent transformers links one inverter with one rectifier. The inverters are operated with 90° phase-shift. The first harmonics of the two secondary side DC-link voltage ripples, which occur at twice the switching frequency f_s, are phase shifted by 180° and, therefore, cancel out due to the series connection. Accordingly,

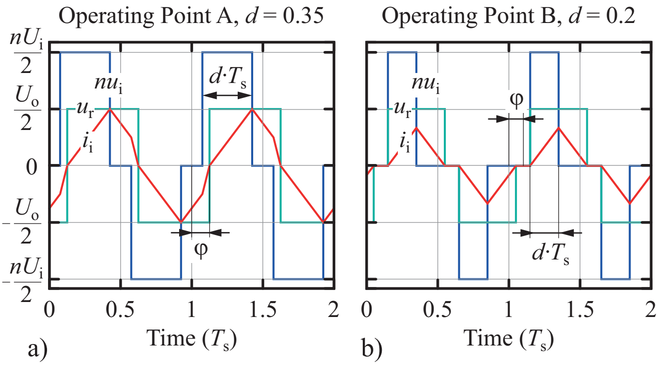


Fig. 4.3: Steady-state waveforms of one of the two SABCs of the ISABC in CCM (a) and DCM (b) for $\frac{U_o}{nU_i} = 0.5$.

the total output voltage U_o only contains ripple components with $4f_s$ and higher. Therefore, a relatively small DC-link capacitance can be used.

As mentioned above, the described ISABC can be considered as an Input Parallel Output Series connection of two independent SABCs although the inverter half-bridges are distributed on two DC-links. The steady state behaviour of the SABC as described in [64, 65] is briefly reviewed in the following for the case of the ISABC since it serves as reference for the comparison with the CISABC which is introduced in Sec. 4.1.2.

Operating Principle

The only passive elements relevant for the operation of the ISABC are the two leakage inductances of the transformers, represented as lumped elements $L_{\sigma s}$ on the secondary sides. Otherwise, the transformers are considered ideal, i.e. the magnetizing inductances are neglected, since they are not essential for the operation. The inverter switching frequency is assumed to be constant, although it could also be employed as control variable [66]. However, a constant switching frequency is desired since the projected system is operating at a, for IGBTs relatively high, switching frequency of 50 kHz. The output voltage control is therefore solely achieved by varying the inverter duty cycle $d \in [0, 0.5]$. With the notation of Fig. 4.2 the rectifier current in each SABC k is described by

$$\frac{\mathrm{d}i_{\mathrm{r}k}}{\mathrm{d}t} = \frac{1}{L_{\sigma\mathrm{s}}}(nu_{\mathrm{i}k} - u_{\mathrm{r}k}) \tag{4.1}$$

with the corresponding inverter output voltage $u_{\mathrm{i}k}$, the turns ratio n and the corresponding rectifier input voltage

$$u_{\mathrm{r}k} = \mathrm{sign}(i_{\mathrm{r}k})\frac{U_\mathrm{o}}{2}, \tag{4.2}$$

which is determined by the total output voltage U_o and the corresponding rectifier current direction.

Output Current Characteristic

It is assumed that both SABCs of the ISABC operate with the same duty cycle. At high duty cycle values each of the two SABCs operates in CCM with typical waveforms as shown in Fig.4.3a. In this conduction mode a phase shift φ between inverter and rectifier voltages results such that the average of the inverter voltage between two current zero crossings equals the output voltage. This phase shift depends on the duty cycle of the inverter and cannot be selected freely. In CCM the steady state DC output current of the ISABC is derived as

$$I_{\mathrm{o,ccm}} = \frac{nU_\mathrm{i}}{16 f_\mathrm{s} L_{\sigma\mathrm{s}}}\left(4d(1-d) - \left(\frac{U_\mathrm{o}}{nU_\mathrm{i}}\right)^2\right). \tag{4.3}$$

If the duty cycle is reduced, the phase shift reduces too until DCM is entered as soon as the rising edge of the rectifier voltage coincides with the second rising edge of the inverter voltage. This point marks the boundary between CCM and DCM at

$$d = \frac{U_\mathrm{o}}{2nU_\mathrm{i}}. \tag{4.4}$$

In DCM as shown in Fig.4.3b, the rectifier voltage exhibits a zero interval such that the voltage time integrals of inverter voltage half-cycle and rectifier voltage half-cycle are equal. Therefore, the steady-state output current in DCM is derived as

$$I_{\mathrm{o,dcm}} = \frac{nU_\mathrm{i}}{2 f_\mathrm{s} L_{\sigma\mathrm{s}}}\left(\frac{nU_\mathrm{i}}{U_\mathrm{o}} - 1\right) d^2. \tag{4.5}$$

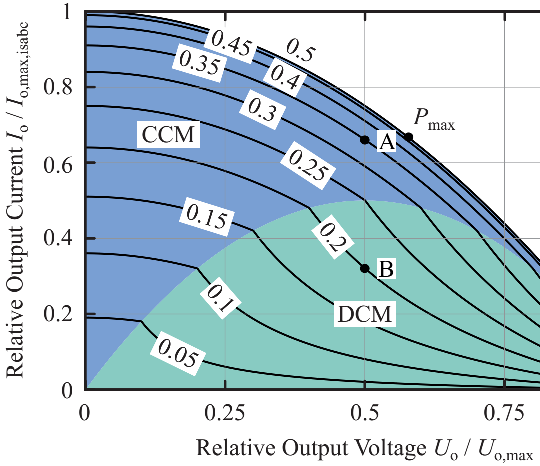


Fig. 4.4: ISABC output current - output voltage characteristic for different values of duty cycle including the operating points A and B for the waveforms shown in Fig. 4.3.

The steady state output current - output voltage characteristic of the ISABC is shown in Fig. 4.4 for different duty cycles. The regions of CCM and DCM are highlighted showing that a wide operating range is covered by DCM operation. The maximum output current is supplied at the maximum duty cycle $d = 0.5$ and zero output voltage (short circuit), and amounts to

$$I_{\mathrm{o,max,isabc}} = \frac{nU_{\mathrm{i}}}{16 f_{\mathrm{s}} L_{\sigma \mathrm{s}}}. \tag{4.6}$$

The maximum output voltage $U_{\mathrm{o,max}} = nU_{\mathrm{i}}$ is reached at zero output current (open circuit). Due to the steep decline of the deliverable output voltage with increasing output current, the maximum power that can be transferred,

$$P_{\mathrm{max}} = \frac{(nU_{\mathrm{i}})^2}{\sqrt{3}24 L_{\sigma \mathrm{s}}}, \tag{4.7}$$

is reached at $U_{\mathrm{o,max}} = \frac{n}{\sqrt{3}} U_{\mathrm{i}}$.

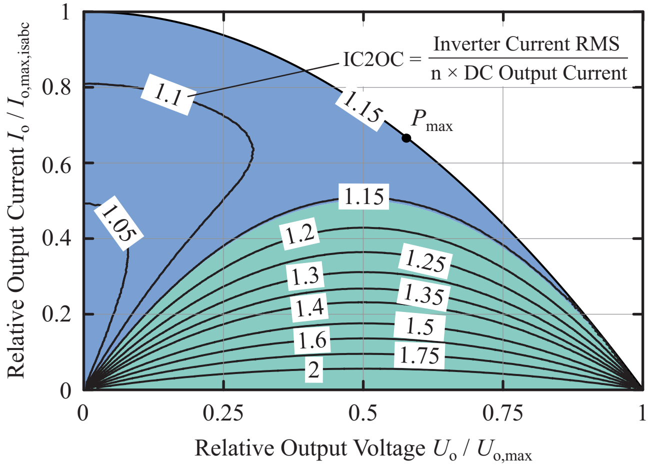


Fig. 4.5: ISABC Inverter Current RMS to DC Output Current ratio.

Inverter RMS Current

For the calculation of the inverter conduction loss and the transformer winding loss, the inverter RMS current is essential. Fig. 4.5 shows the Inverter Current RMS to DC Output Current ratio of the ISABC. In the CCM region, the ratio is less than $\frac{2}{\sqrt{3}} \approx 1.15$, less than the value reached with a Dual Active Bridge (DAB) converter in triangular current mode [67]. A rectangular current shape as it results with the ISABC if $I_o \rightarrow 0$ and $U_o \rightarrow 0$ or with a DAB if $L_\sigma \rightarrow 0$ and $U_o = nU_i$, results in the minimum possible ratio of 1. In DCM the inverter RMS current to DC output current ratio increases dramatically causing high conduction loss. Together with the fact that the maximum output power is reached at relatively low output voltage, therefore at relatively high output- and inverter current, this is the major drawback of the ISABC. This disadvantage can be overcome using a Series Resonant Converter (SRC) [68]. However, the SRC, due to its integrating plant [69], requires more sophisticated control such as cascaded control which is relatively slow, or Optimum Trajectory Control (OTC) which is relatively complex [70], compared to that the direct duty cycle - output current relationship (4.3),(4.5) of the ISABC allows direct (single control loop) output voltage control. Another solution to reduce the output RMS current of the

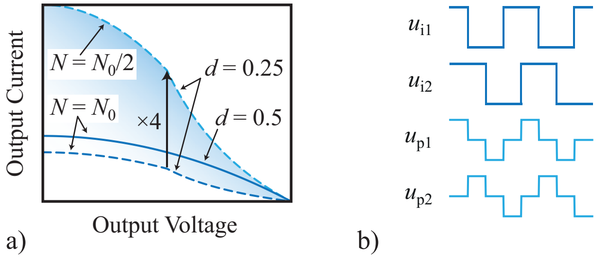


Fig. 4.6: a) Reducing the duty cycle of the ISABC from 50 % to 25 % allows to reduce the number of turns by a factor of two, increasing the maximum output current. b) Inverter voltages u_{i1}, u_{i2} and winding voltages u_{p1}, u_{p2} of the CISABC.

ISABC is to use an inductive output filter [71]. However, due to the high output voltage the filter inductor needs to be split up into one inductor per rectifier stage which is not feasible due to the high number of rectifier stages.

Inverter Switched Current

The ISABC offers ZVS on both inverter half-bridges in CCM. In DCM ZVS is only achieved on the leading half-bridge, i.e. the half-bridge which is the one causing the first of the two rising and falling edges of the transformer primary voltage (Fig. 4.3b). The lagging half-bridge achieves still ZCS in DCM at constant switching frequency. In comparison, the switching frequency of an SRC would need to be varied by a factor of two to obtain ZVS or at least ZCS over the full operating range [72].

4.1.2 Coupled Interleaved Single Active Bridge Converter

The CISABC provides a solution to maintain the advantages of the ISABC over the SRC, i.e. ZVS with constant switching frequency and direct output voltage control, while reducing the inverter RMS current. The basic idea is illustrated in Fig. 4.6. By limiting the inverter duty cycle of a ISABC to 25 % the numbers of turns on both sides of the transformers can be cut in half, thus reducing the stray inductances and increasing the output current at 25 % duty cycle by a factor of four (Fig. 4.6a) - without increasing the peak flux density in the core. Compared to the

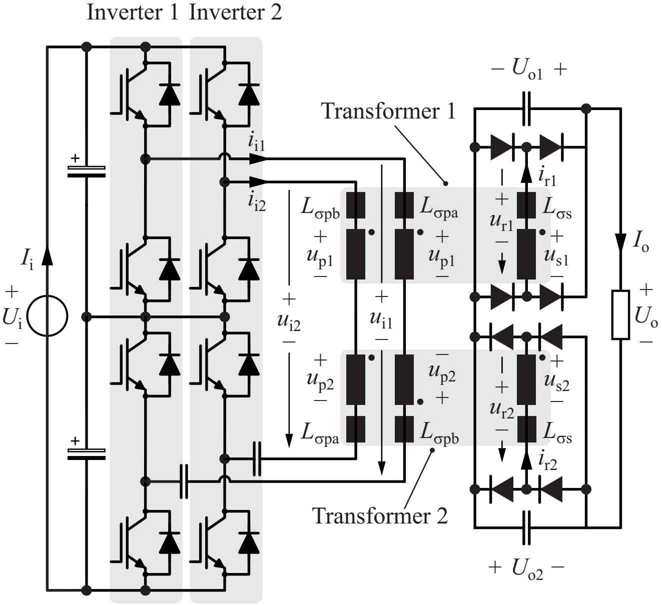

Inverter 1
Inverter 2
Transformer 1
Transformer 2
i_{i1}
i_{i2}
I_i
$+ U_i -$
$L_{\sigma pb}$
$L_{\sigma pa}$
$+ u_{p1} -$
$+ u_{i2} -$
$+ u_{i1} -$
$+ u_{p2} -$
$- u_{p2} +$
$- U_{o1} +$
i_{r1}
$+ u_{r1} -$
$L_{\sigma s}$
$+ u_{s1} -$
I_o
$+ U_o -$
$+ u_{s2} -$
$+ u_{r2} -$
i_{r2}
$+ U_{o2} -$

Fig. 4.7: Basic CISABC circuit in IPOS configuration with the two half-bridges of each inverter distributed on two split DC-links.

maximum output current with 50 % duty cycle more output current can be transferred if the duty cycle is limited to 25 % for all output voltages.

The CISABC achieves these 25 % duty cycle voltages at the transformer primary windings using two primary windings on each transformer and connecting them to the inverters as shown in Fig. 4.7. Because, inverter voltage 1 is the difference and inverter voltage 2 the sum of the two transformer primary voltages, the transformer primary voltages have to exhibit a 25 % duty cycle shape as shown in Fig. 4.6b (neglecting the primary leakage inductances for the meantime). The advantage of this circuit is that the secondary side amp-turns are now shared by the two primary windings. Since, the secondary currents, as well as the voltages, are 90° phase shifted this does not cut the inverter currents in half but still reduces them by a factor of $\sqrt{2}$. The following analysis proves this point and considers also the primary leakage inductances which have been neglected up to now.

Operating Principle

All three windings of one transformer are wound around the same magnetic path with N_p turns on each primary winding and $N_\mathrm{s} = nN_\mathrm{p}$ on each secondary winding. The windings of the high-voltage transformer are coaxially arranged with one primary winding closest to the core, directly enclosed by the next primary winding and finally with 12.5 mm isolation distance surrounded by the secondary winding. Therefore, the transformer model includes two slightly different primary leakage inductances $L_{\sigma\mathrm{pa}}$ and $L_{\sigma\mathrm{pb}}$ and the dominating secondary leakage inductance $L_{\sigma\mathrm{s}}$.

Due to the symmetry (two inverters, transformers and rectifiers) of the circuit, voltage and current pairs are summarized using vector notation. E.g., the inverter and the rectifier current vectors with the notation of Fig. 4.7 are expressed as

$$\vec{i}_\mathrm{i} = \begin{bmatrix} i_\mathrm{i1} \\ i_\mathrm{i2} \end{bmatrix}, \quad \vec{i}_\mathrm{r} = \begin{bmatrix} i_\mathrm{r1} \\ i_\mathrm{r2} \end{bmatrix}. \tag{4.8}$$

The secondary current of transformer 1 is the sum of the two primary currents divided by the turns ratio and the secondary current of transformer 2 is the difference of the second primary current and the first primary current divided by the turns ratio. Therefore, the rectifier current vector is expressed as

$$\vec{i}_\mathrm{r} = \frac{1}{n} \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \vec{i}_\mathrm{i}, \tag{4.9}$$

and by inverting the matrix the inverter current vector

$$\vec{i}_\mathrm{i} = \frac{n}{2} \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \vec{i}_\mathrm{r} \tag{4.10}$$

follows. Considering the voltages at the leakage inductance elements, the inverter voltage vector equals

$$\vec{u}_\mathrm{i} = (L_{\sigma\mathrm{pa}} + L_{\sigma\mathrm{pb}}) \frac{\mathrm{d}\vec{i}_\mathrm{i}}{\mathrm{dt}} + \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \vec{u}_\mathrm{p}, \tag{4.11}$$

and at the secondary side, the rectifier voltage vector is expressed as

$$\vec{u}_\mathrm{r} = \vec{u}_\mathrm{s} - L_{\sigma\mathrm{s}} \frac{\mathrm{d}\vec{i}_\mathrm{r}}{\mathrm{dt}}. \tag{4.12}$$

With $\vec{u}_\mathrm{s} = n\vec{u}_\mathrm{p}$, combining (4.10), (4.11) and (4.12) the time derivative of the secondary side currents is obtained as

$$\frac{\mathrm{d}\vec{i}_\mathrm{r}}{\mathrm{dt}} = \frac{1}{L_{\sigma\mathrm{s,tot}}} \left(\vec{u}_\mathrm{r0} - \vec{u}_\mathrm{r}\right), \tag{4.13}$$

with the total leakage inductance referred to the secondary side

$$L_{\sigma\mathrm{s,tot}} = \frac{n^2}{2}(L_{\sigma\mathrm{pa}} + L_{\sigma\mathrm{pb}}) + L_{\sigma\mathrm{s}}, \tag{4.14}$$

and the no-load rectifier voltage vector

$$\vec{u}_\mathrm{r0} = \frac{n}{2}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \vec{u}_\mathrm{i}. \tag{4.15}$$

In case of no-load ($\frac{\mathrm{d}\vec{i}_\mathrm{r}}{\mathrm{dt}} = 0$) the rectifier voltage vector equals the no-load rectifier voltage vector. From (4.13) it is evident that the rectifier currents result from the difference between the no-load rectifier voltages and the rectifier voltages. Only the sum of the three, possibly different leakage inductances $L_{\sigma\mathrm{pa}}$, $L_{\sigma\mathrm{pb}}$ and $L_{\sigma\mathrm{s}}$ is effectively influencing the current. Therefore, different leakage inductances of the two primary windings because of asymmetric construction due to the coaxial primary winding arrangement still lead to equal current sharing between the inverters. However, the two transformers have to be identical and each inverter needs to connect in series to two different types (a,b) of primary windings, i.e. an outer and an inner one of the coaxial arrangement. The CISABC can, therefore, be modelled by replacing transformers and inverters by two controlled voltage sources with the values of the no-load rectifier voltages (4.15). Together with the total leakage inductance referred to the secondary side (4.14) this voltage sources can be imagined to be connected to the output rectifier as shown in Fig. 4.8. This simplified model allows to study the full steady-state and dynamic behaviour of the CISABC. The no-load rectifier voltage waveforms are shown in Fig. 4.9 for different values of inverter duty cycle. With maximum duty cycle ($d = 0.5$) the no-load rectifier voltage actually looks like a 25 % duty cycle signal. If the inverter duty cycle is reduced to $d = 0.375$ a five-level stepped no-load voltage occurs. The voltage time integral of this waveform however is still the same as with maximum inverter duty cycle. In case of $d = 0.25$ the

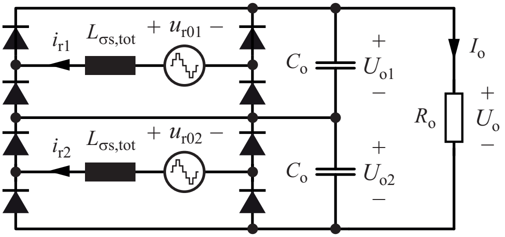

i_{r1}
$L_{\sigma s,tot}$
$+ u_{r01} -$
i_{r2}
$L_{\sigma s,tot}$
$+ u_{r02} -$
C_o
C_o
$+$
U_{o1}
$-$
$+$
U_{o2}
$-$
I_o
R_o
$+$
U_o
$-$

Fig. 4.8: Equivalent CISABC circuit employing two voltage sources representing the rectifier no-load voltages acting on the total leakage inductances referred to the secondary side.

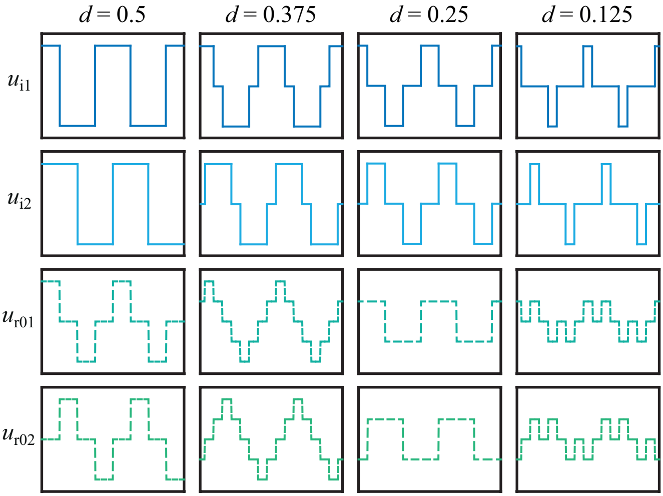


Fig. 4.9: Inverter voltages u_{i1} and u_{i2} and resulting no-load rectifier voltages u_{r01} and u_{r02} (dashed) for different values of inverter duty cycle d.

highest level vanishes and a full block rectangular waveform at the half level remains, still having the same voltage time integral as with maximum inverter duty cycle. If the duty cycle is further reduced, the zero level is entered four times per switching period, and a gap is inserted in the full block voltage. The voltage time integral is now reduced. It is pointed out that the CISABC actually provides five voltage levels to the transformer, potentially allowing a low RMS current in the transformer at low output voltage levels. Simulated waveforms of the CISABC for 50 %, i.e. maximum, duty cycle on both inverters with $U_\mathrm{o} = 0.75nU_\mathrm{i}$ are shown in Fig. 4.10. According to (4.15), with turns ratio $n = 1$ as in this simulation, the first no-load rectifier voltage u_r01 equals half of the sum of the two inverter voltages (25 % duty cycle no-load rectifier voltage waveform). With $n = 1$, the peak value of this waveform equals the peak value of the inverter voltages. The RMS value, however, is smaller by a factor $\sqrt{2}$. During the time when the no-load rectifier voltage of one transformer equals n times the inverter peak voltage, the rectifier current is building up. As soon as the no-load voltage returns to zero, the rectifier current drops too eventually reaching zero. On the secondary side this particular case is similar to the DCM of the ISABC. On the primary side, according to (4.10), with $n = 1$ the first inverter current equals half the difference between the first and the second rectifier current and the second inverter current equals half the sum of the two rectifier currents. The rectifier currents show half-cycle symmetry and, therefore, all even harmonics are zero. The two rectifier currents are also identically shaped but 90° phase shifted. If a signal is 90° phase shifted, with respect to its fundamental component, the third component is phase shifted by −90°, the fifth component by 90°, the seventh again by −90° and so on. Therefore, a phase shift of either 90° or −90° exists between each harmonic of one rectifier current and the harmonic with the same order of the other rectifier current. This means that the rectifier currents are orthogonal and, therefore, each harmonic amplitude of the sum (or difference) of the two rectifier currents equals the square root of the sum of the two corresponding rectifier harmonics squared. The RMS value of the first inverter current is, therefore, calculated as

$$\mathrm{rms}(i_\mathrm{i1}) = \frac{n}{2}\mathrm{rms}(i_\mathrm{r1} - i_\mathrm{r2}) = \frac{n}{2}\sqrt{\mathrm{rms}(i_\mathrm{r1})^2 + \mathrm{rms}(i_\mathrm{r2})^2} \qquad (4.16)$$

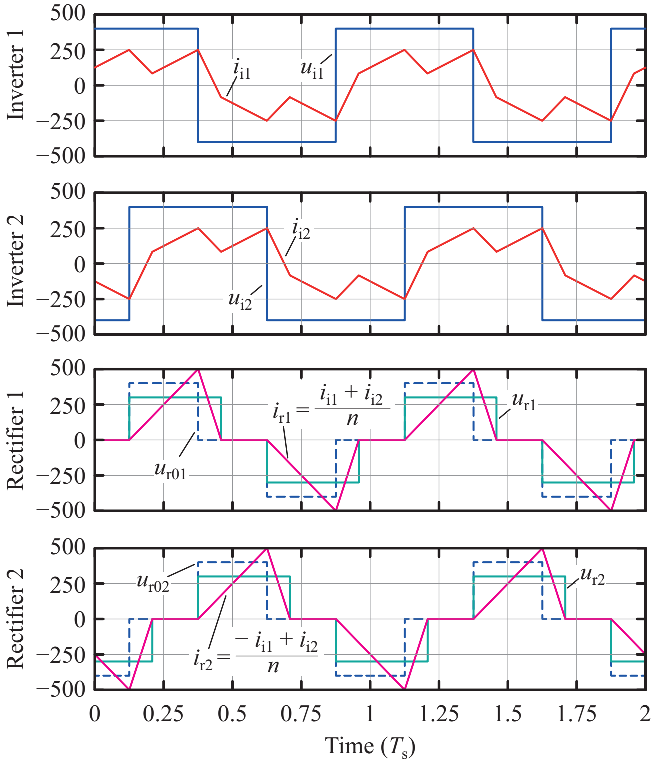


Fig. 4.10: Simulated primary- and secondary- side voltage and current waveforms of the CISABC according to Fig. 4.7 with turns ratio $n = 1$ (no-load rectifier voltage shown dashed), total leakage inductance referred to the secondary side $L_{\sigma\mathrm{s,tot}} = 1\,\mu\mathrm{H}$, switching frequency $f_\mathrm{s} = 50\,\mathrm{kHz}$, input voltage $U_\mathrm{i} = 800\,\mathrm{V}$, output voltage $U_\mathrm{o} = 600\,\mathrm{V}$ and duty cycle $d = 0.5$.

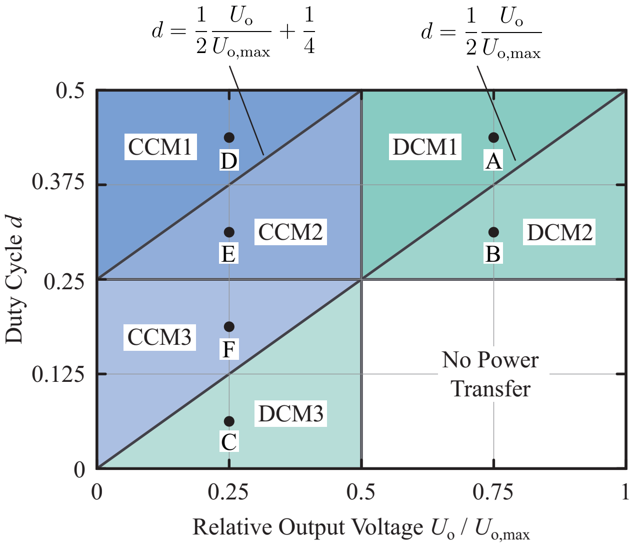


Fig. 4.11: CISABC conduction modes as function of duty cycle and output voltage relative to maximum output voltage.

and since $\mathrm{rms}(i_{r1}) = \mathrm{rms}(i_{r2})$, the RMS value of the inverter currents is

$$\mathrm{rms}(i_i) = \frac{n}{\sqrt{2}}\mathrm{rms}(i_r). \tag{4.17}$$

Therefore, with the proposed transformer configuration and turns ratio $n = 1$, the RMS value of the inverter currents is by a factor $\sqrt{2}$ lower than the RMS value of the rectifier currents, while the peak value of the rectifier no-load voltage equals the peak value of the inverter voltage. Compared to the ISABC this property allows a significant reduction of the inverter conduction loss. Furthermore, for the case shown in Fig. 4.10, the peak value of one rectifier current occurs when the other is zero, resulting in only half the current peak value being switched by the inverter.

Conduction Modes

Due to the five-level characteristic (Fig. 4.9) of the rectifier no-load voltage three different DCMs and also three CCMs have to be distinguished

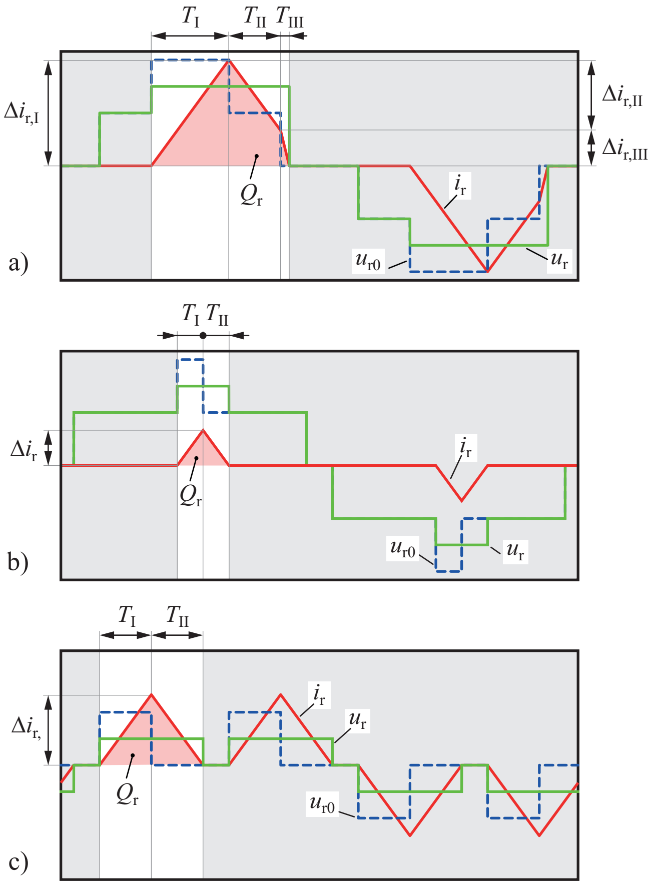


Fig. 4.12: Rectifier current, rectifier voltage and rectifier no-load voltage waveforms of the CISABC for DCM1 in working point A of Fig. 4.11/4.14 (a), for DCM2 in working point B of Fig. 4.11/4.14 (b) and for DCM3 in working point C of Fig. 4.11/4.14 (c).

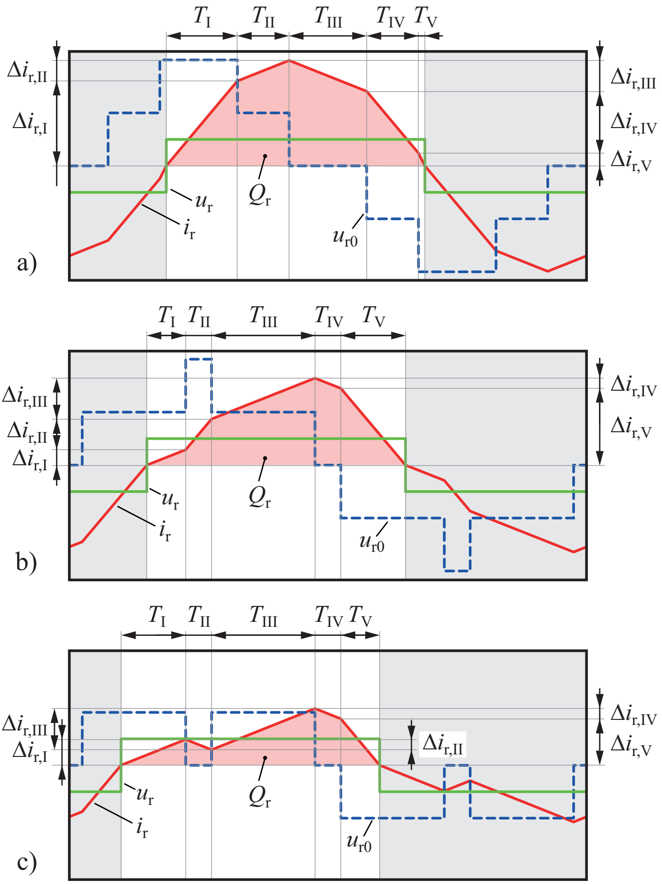


Fig. 4.13: Rectifier current, rectifier voltage and rectifier no-load voltage waveforms of the CISABC for CCM1 in working point D of Fig. 4.11/4.14 (a), CCM2 in working point E of Fig. 4.11/4.14 (b), CCM3 in working point F of Fig. 4.11/4.14 (c).

when aiming to describe the output current - duty cycle relationship. As shown in Fig. 4.11 it depends on the duty cycle and the relative output voltage which conduction mode occurs. Power transfer for output voltages higher than half the maximum output voltage is only possible in DCM and only if $d > 0.25$.

For the working points A,B, and C in Fig. 4.11, representing the three DCMs, the waveforms of no-load voltage, rectifier current and rectifier voltage of one rectifier are shown in Fig. 4.12. The working points D, E and F in Fig. 4.11 serve as examples for the three CCMs with the according waveforms shown in Fig. 4.13. From these waveforms the output current as function of the duty cycle for the six different conduction modes can be derived as

$$\begin{aligned}
I_{\mathrm{o,dcm1}} &= \frac{nU_\mathrm{i}}{2f_\mathrm{s}L_{\sigma\mathrm{s,tot}}}\left(\left(\frac{nU_\mathrm{i}}{4U_\mathrm{o}}-\frac{1}{2}\right)d^2+\frac{d}{4}-\frac{1}{16}\right), && (4.18)\\
I_{\mathrm{o,dcm2}} &= \frac{nU_\mathrm{i}}{2f_\mathrm{s}L_{\sigma\mathrm{s,tot}}}\frac{nU_\mathrm{i}-U_\mathrm{o}}{2U_\mathrm{o}-nU_\mathrm{i}}\left(d-\frac{1}{4}\right)^2, && (4.19)\\
I_{\mathrm{o,dcm3}} &= \frac{nU_\mathrm{i}}{2f_\mathrm{s}L_{\sigma\mathrm{s,tot}}}\left(\frac{nU_\mathrm{i}}{2U_\mathrm{o}}-1\right)d^2, && (4.20)\\
I_{\mathrm{o,ccm1}} &= \frac{nU_\mathrm{i}}{4f_\mathrm{s}L_{\sigma\mathrm{s,tot}}}\left(d-d^2-\frac{1}{16}-\left(\frac{U_\mathrm{o}}{2U_\mathrm{i}}\right)^2\right), && (4.21)\\
I_{\mathrm{o,ccm2\&3}} &= \frac{nU_\mathrm{i}}{8f_\mathrm{s}L_{\sigma\mathrm{s,tot}}}\left(d-\left(\frac{U_\mathrm{o}}{nU_\mathrm{i}}\right)^2\right). && (4.22)
\end{aligned}$$

For CCM2 and CCM3 the same expression results. The full derivation of the analytic expressions for the output current and the boundaries between the different conduction modes is provided in the Appendix.

Output Current Characteristic

The output current as function of the output voltage of the CISABC is plotted for different values of duty cycle in Fig. 4.14 together with the conduction mode boundaries. CCM1 only appears at very high output currents and low output voltages and is therefore not relevant for many applications because of thermal limitations. Therefore, because of the identical relationship between duty cycle and output current of CCM2 and CCM3 (4.22), it is practically sufficient to distinguish between four operating regions for hardware implementation.

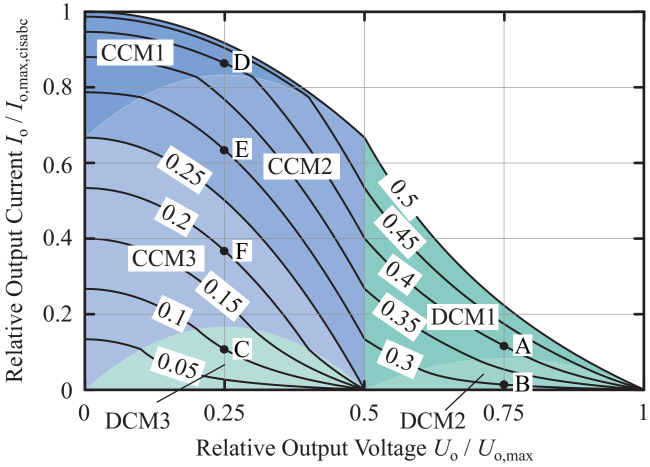


Fig. 4.14: CISABC output current as function of output voltage for different values of duty cycle with exemplary operating points used for analysing the different conduction modes in Section 4.1.2.

The output current characteristic of the CISABC looks similar as the one of the ISABC. The output current decreases with increasing output voltage for a given duty cycle and with increasing duty cycle the output current is monotonously increasing. The shape of the characteristic at 50 % duty cycle resembles the one of the ISABC at 25 % duty cycle (cf. Fig. 4.4).

From (4.21) the maximum output current (at $U_o = 0$) of the CISABC can be expressed as

$$I_{o,max,cisabc} = \frac{3nU_i}{64 f_s L_{\sigma s,tot}}. \tag{4.23}$$

At first sight, this value seems to be smaller than the maximum output current of the ISABC (4.6). However, for the given application the transformers are designed for maximum power density, and are therefore operating at the maximum flux density allowed by the core material. Because of the 25 % duty cycle shape of the rectifier no-load voltage, the maximum voltage time integral at the primary winding of the CISABC is only half the one of the ISABC. Therefore, the number of turns necessary to reach the same flux density with the CISABC is only half that of

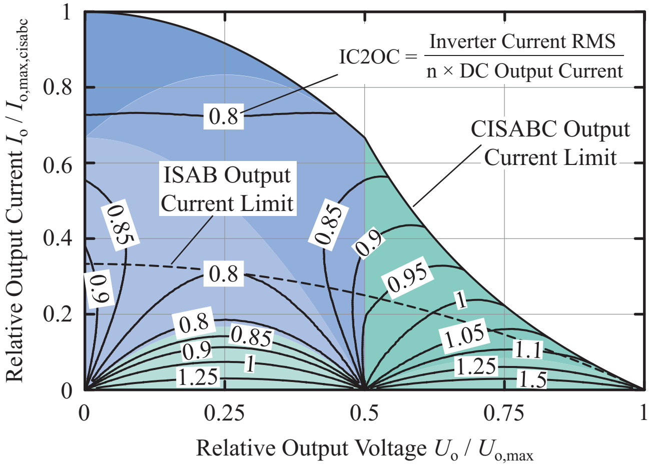


Fig. 4.15: Inverter Current RMS to DC Output Current (IC2OC) ratio of the CISABC and output current limit compared to the output current limit of the ISABC.

the ISABC, resulting in a four times lower leakage inductance as already mentioned above. If this is taken into account when dividing (4.23) by (4.6), it follows that the maximum output current of the CISABC at zero output voltage is three times higher than the one of the ISABC.

Inverter RMS Current

Apart from the higher power transfer capability, the fact that the primary side RMS current value is only $\frac{n}{\sqrt{2}}$ times the secondary side RMS value (4.17) suggests that the primary side RMS currents of the CISABC are lower than the ones of the ISABC. The Inverter Current RMS to DC Output Current (IC2OC) ratio of the CISABC is shown in Fig. 4.15. As can be seen the IC2OC ratio is less than one on a wide operating range. The plot also shows the output current limit of the CISABC compared to the output current limit of the ISABC, demonstrating that the achievable output current with the CISABC is higher than with the ISABC for all values of output voltage. A direct comparison of the inverter RMS currents of CISABC and ISABC is provided in Fig. 4.16 showing the inverter current RMS value of the CISABC related to the one of the

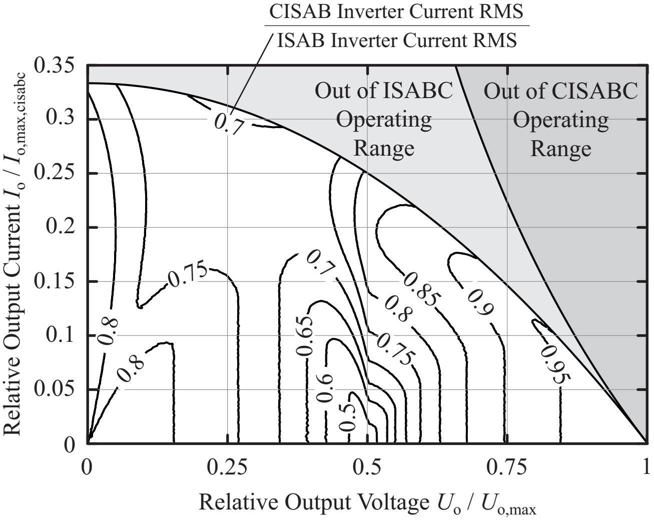


Fig. 4.16: Inverter current RMS value of the CISABC related to the one of the ISABC for the part of the operating range covered by both topologies.

ISABC. This plot shows that the inverter RMS current with the CISABC is smaller over the whole operating range covered by the ISABC. At high output voltages the inverter current RMS values are comparable but a significant reduction is achieved in particular at medium output voltage levels. As a return for the higher circuit complexity, the CISABC therefore provides lower RMS current stress on the inverter side. At the same time higher power transfer is possible with the CISABC than with the ISABC.

Inverter Switched Current

Similar to the ISABC, the CISABC inherently provides ZVS or at least ZCS in the full operating range. The condition for ZVS is that all rising edges of each inverter voltage u_i occur while the corresponding inverter current i_i is negative and that all falling edges of each inverter voltage u_i occur while the corresponding inverter current i_i is positive (voltage and current directions as in Fig. 4.2). There is also a short formulation of this condition: For a ZVS commutation the power supplied by a half-bridge port, which includes the switching node, before the commutation must be higher than after the commutation. Furthermore, a ZCS commutation is characterized by the power supplied by a half-bridge not changing during the commutation and a hard commutation is characterized by the power supplied by a half-bridge increasing during the commutation. Using (4.9) and (4.15) it can be shown that the instantaneous power supplied by both inverters p_i equals the instantaneous power p_r0 supplied by the fictive no-load rectifier voltage sources of the CISABC equivalent circuit (Fig. 4.8), i.e.

$$p_\mathrm{r0} = \vec{u}_\mathrm{r0}^\top \vec{i}_\mathrm{r} = \vec{u}_\mathrm{i}^\top \vec{i}_\mathrm{i} = p_\mathrm{i}. \tag{4.24}$$

Considering the steps of the power supplied by one no-load rectifier voltage source at the commutations in CCM1 (Fig. 4.13a) reveals that they are all negative. This is also true for the other continuous conduction modes CCM2 and CCM3 (Fig. 4.13b, c). Therefore, also all inverter power steps at the commutations in the continuous conduction modes are negative and consequently ZVS is achieved. For the discontinuous conduction modes the situation is not so clear since in DCM1 (Fig. 4.12a) half of the steps of the power $u_\mathrm{r01} i_\mathrm{r1}$ supplied by *one* no-load rectifier voltage source at the commutation times is negative but the other half is zero. However, when one of the two power steps supplied by the two no-load rectifier voltage sources is zero the other is negative. Therefore, all total inverter power steps are negative and thus ZVS is obtained at all commutations in DCM1. In DCM2 (Fig. 4.12b) only one of four commutations per half-cycle results in a reduction of the power supplied by the according rectifier no-load voltage source. Thus, only two of four commutations result in a reduction of the total inverter power p_i and are thus ZVS commutations while the other two result in no change of the inverter power and are thus ZCS commutations. In DCM3 two of four commutations per half-cycle result in a reduction of the power supplied by each rectifier no-load voltage source. The other two result in no change. Since the commutations that do not affect the power supplied by the rectifier no-load voltage occur with 90° phase-shift, half of the commutations in DCM3 are ZVS and the other half are ZCS. In summary this analysis shows that in all continuous conduction modes and in DCM1 the CISABC is operating with ZVS on all inverter half-bridges. In DCM2 and DCM3 the leading half-bridges operate in ZVS while the lagging half-bridges operate in ZCS, similarly as in the DCM of the SABC.

The currents that are switched by the leading and the lagging half-bridge of each inverter are shown in Fig. 4.17 related to the output DC current. ZVS is obtained on the full operating range, although the lagging half-bridge has to switch at zero current at lower output currents. This might be an issue for highly efficient Si MOSFET designs with large output capacitances, but from a thermal perspective the losses that occur from discharging the output capacitance of the switch are typically not critical, in particular with Si IGBTs and Gallium Nitride (GaN) and SiC MOSFETs.

4.2 Dynamic Analysis

4.2.1 Linear Model

In order to model the dynamic behaviour of the CISABC a simple linear equivalent circuit as shown in Fig. 4.18b is used. The inverter is represented by a voltage source, controlled by the duty cycle d and the leakage inductance by a virtual internal resistance

$$R_\sigma = \frac{U_{\mathrm{o,max}}}{I_{\mathrm{o,max}}} = \frac{64}{3} f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}. \tag{4.25}$$

As shown in Fig. 4.18a this simple model approximates the actual output current - output voltage characteristic only roughly in terms of steady-state value. It could be improved, at the price of higher complexity and only piece-wise linearity, by adapting the values of the internal resistance and the gain of the controlled voltage source depending on the working point. However, the dynamic behaviour is not only determined by inverter and leakage-inductance. Instead the total DC-link capacitance C_{o} of the rectifiers and the load connected to the output also contribute to the dynamic system behaviour. The complete dynamic equivalent circuit of the CISABC shown in Fig. 4.18 is represented by the transfer function

$$G(s) = \frac{U_{\mathrm{o}}(s)}{d(s)} = \frac{k_1}{T_1 s + 1} \tag{4.26}$$

with

$$k_1 = \frac{2nU_{\mathrm{i}}R_{\mathrm{o}}}{R_{\mathrm{o}} + R_\sigma}, \quad T_1 = \frac{C_{\mathrm{o}}}{2}\frac{R_{\mathrm{o}}R_\sigma}{R_{\mathrm{o}} + R_\sigma}. \tag{4.27}$$

Therefore, the CISABC dynamic behaviour is approximately described by a first-order (PT1) system with a characteristic time constant T_1 proportional to the output capacitance and the parallel connection of

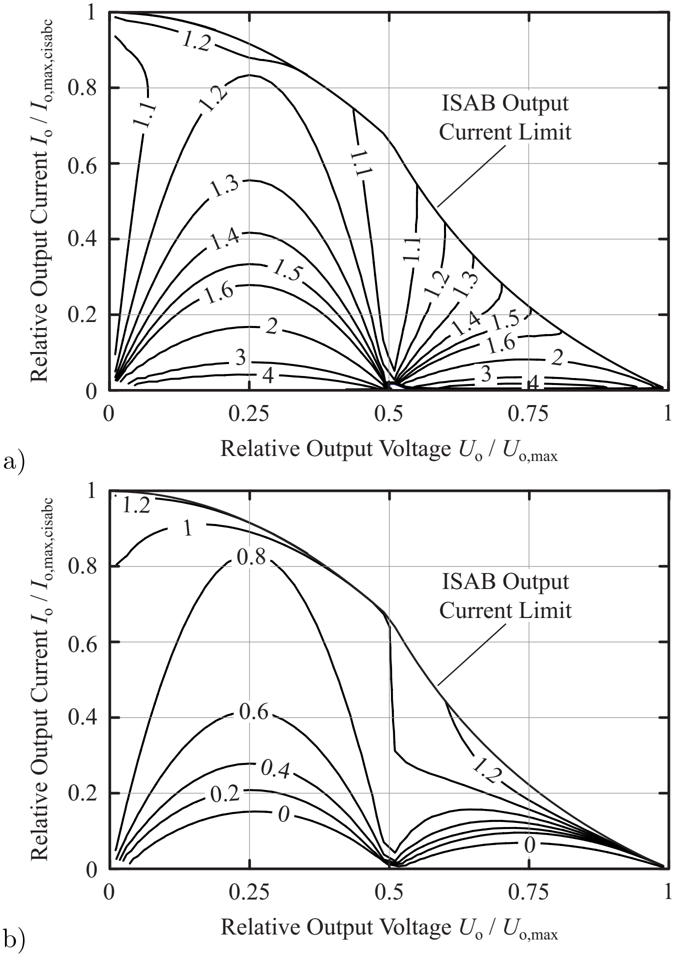


Fig. 4.17: Currents switched in leading switch (a) and lagging switch (b) of the inverter of an CISABC related to output DC current reflected to primary side.

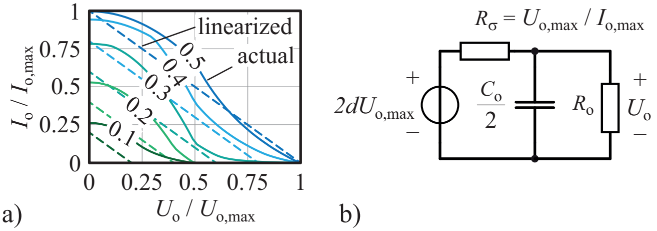


Fig. 4.18: Comparison of linear model and actual output characteristic of the ISABC (a) and equivalent circuit of the linear model (b).

the load resistance R_o and the virtual internal resistance R_σ. This first-order behaviour is a significant advantage of the CISABC (and the ISABC) compared to the SRC which, at resonance frequency, exhibits a second order system [69].

4.2.2 Output Voltage Closed-Loop Control

The phase shift of the described linearised plant transfer function $G(s)$ is less than -90 °, therefore an integral controller $K(s) = \frac{k_\mathrm{d}}{s}$ which is directly acting on the duty cycle can be used for controlling the output voltage. The according closed-loop block diagram is shown in Fig. 4.19. The resulting closed-loop transfer function

$$G_2(s) = \frac{k_2}{T_2^2 s^2 + 2d_2 T_2 s + 1} \tag{4.28}$$

is identified as a second order (PT2) system. Its parameters are identified as

$$k_2 = 1, \quad d_2 = \frac{1}{2\sqrt{k_\mathrm{d} k_1 T_1}}, \quad T_2 = \sqrt{\frac{T_1}{k_\mathrm{d} k_1}}. \tag{4.29}$$

The required fastest output voltage rise-time without overshoot is reached if the system is critically damped, i.e. if $d_2 = 1$. This is achieved by setting the controller integral gain to

$$k_\mathrm{d} = \frac{(R_\sigma + R_\mathrm{o})^2}{4nU_\mathrm{i} R_\sigma C_\mathrm{o} R_\mathrm{o}^2}. \tag{4.30}$$

The resulting time constant T_2 is given as

$$T_2 = C_\mathrm{o} \frac{R_\mathrm{o} R_\sigma}{R_\mathrm{o} + R_\sigma}, \tag{4.31}$$

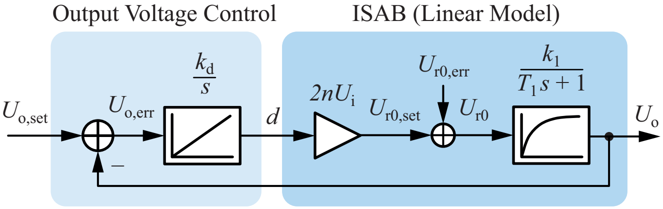


Fig. 4.19: Output voltage control loop block diagram with the ISABC replaced with its linear model and a pure integral controller acting directly on the duty cycle.

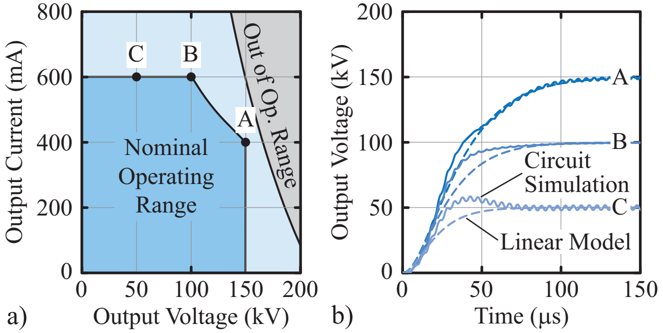


Fig. 4.20: Specified high-voltage generator operating range and characteristic working points (a) and set value step response of the linear control model compared to the circuit simulation (b).

and the output voltage set value step response, thus achieves a 99 % rise-time of $T_r \approx 6.6T_2$. The operating range for the targeted X-ray system is limited by the maximum output power of 60 kW and the maximum output current of 600 mA, as shown in Fig. 4.20a. The high-voltage transformer's leakage inductance is dimensioned, such that the maximum output current of the ISABC is 50 % higher than the specified limit. For the three operating points A (maximum power, maximum voltage), B (maximum power, maximum current) and C (maximum current, minimum voltage) the set value step response of the linear model is compared to the one of a circuit simulation. The controller integral gain is set to the maximum value for no overshoot (4.30). The circuit simulation shows that for working points A and B this control gain, found using the linear model, is actually a good choice and the linear model agrees reasonably well with the simulation. In working point C, however, overshoot of the output voltage is observed. This is due to the error introduced by the linear model (Fig. 4.18a) and the delay of the PWM not included in the model. The minimum rise-time of 6.6 T_2, therefore should only be used to approximately describe the relationship between output voltage rise-time, switching frequency, leakage inductance, output capacitance and load resistance. The actual output voltage controller gain has to be found by tuning a circuit simulation using the analytically found value (4.30) as initial point. Since the optimum controller gain depends on the working point, gain scheduling has to be employed to cover the full operating range.

4.2.3 Midpoint Balancing Closed-Loop Control

Until now only symmetrically loaded outputs of the ISABC have been considered. Due to the IPOS structure, the two output voltages are self-stable and if loaded symmetrically also self-balanced. However, with certain types of X-ray tubes not all electrons emitted by the filament are collected by the anode. Instead a small part of the electrons is attracted by the metallic shielding of the tube. Since the shield is connected to the midpoint of the high-voltage output an asymmetric load appears and the two partial voltages $U_{\mathrm{o}1}$, $U_{\mathrm{o}2}$ (see Fig. 4.7) are loaded with different currents. Without any counter measures, unequal currents also lead to unequal voltages $U_{\mathrm{o}1}$, $U_{\mathrm{o}2}$. Since, the isolation of each of the two high-voltage transformer-rectifier stages is only rated for half the maximum output voltage, unequal voltage sharing could damage the isolation. Therefore, active output voltage midpoint balancing control is necessary to guarantee equal output voltages also with asymmetric loads. As shown in Fig. 4.21 using the fundamental component phasors of inverter voltages and rectifier no-load voltages, this is possible by varying the phase shift between the two primary side inverters. With the nominal value of 90° phase shift (Fig. 4.21a) the two rectifier no-load voltage fundamentals are equal. If the phase shift is reduced (Fig. 4.21b), the first rectifier no-load voltage fundamental is increased, while the second is decreased, allowing to transfer more current to the first and less to the second output voltage half. The opposite situation (Fig. 4.21c) with a phase shift of more than 90° results in a lower first and a higher second rectifier no-load voltage fundamental, resulting in lower current to the

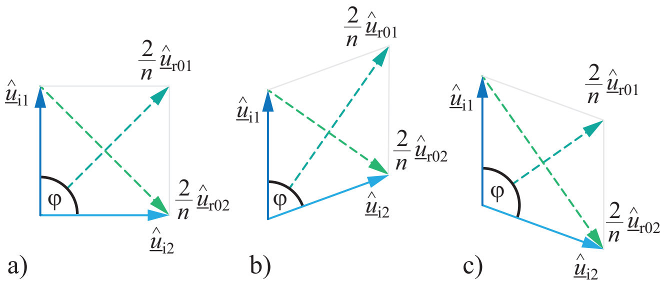

$\hat{\underline{u}}_{i1}$
$\frac{2}{n}\hat{\underline{u}}_{r01}$
$\frac{2}{n}\hat{\underline{u}}_{r02}$
$\hat{\underline{u}}_{i2}$
φ
a)
b)
c)

Fig. 4.21: Effect of phase-shift variation on the rectifier no-load voltage fundamental amplitude, showing $\hat{u}_{r10} = \hat{u}_{r20}$ with nominal phase shift $\varphi = 90\,°$ (a), $\hat{u}_{r10} > \hat{u}_{r20}$ with phase shift $\varphi < 90\,°$ (b) and $\hat{u}_{r20} > \hat{u}_{r10}$ with phase shift $\varphi > 90\,°$ (c).

first and higher current to the second half of the output. Using basic trigonometric relationships, and the phase shift deviation $\Delta\varphi = \varphi - \frac{\pi}{2}$ it can be shown that

$$\hat{u}_{r01} + \hat{u}_{r02} \propto \cos(\frac{\Delta\varphi}{2}) \quad \text{and} \quad \hat{u}_{r01} - \hat{u}_{r02} \propto -\sin(\frac{\Delta\varphi}{2}). \tag{4.32}$$

Therefore, small phase-shift deviations $\Delta\varphi$ affect the sum of the two no-load rectifier voltage fundamentals and thus the total output voltage only weakly while the difference of the two no-load rectifier voltage fundamentals and thus the difference of the two partial output voltages is strongly influenced. A separate output voltage balancing controller, acting on the phase shift deviation $\Delta\varphi$, is therefore introduced which is only weakly coupled with the main output voltage controller, acting on the duty cycle. The complete controller block diagram with the proposed output voltage balancing controller is shown in Fig. 4.22. The balancing controller is also realised as an integral controller acting on the normalized phase shift deviation $g = \frac{\Delta\varphi}{2\pi}$. The gain of g acting on the plant is chosen in a first order estimation such that for $d = 0.5$ and $g = -0.5$, i.e. maximum duty cycle and $0\,°$ inverter phase shift, $U_{r20} = 0$ and for $d = 0.5$ and $g = 0.5$, i.e. maximum duty cycle and $180\,°$ inverter phase shift, $U_{r10} = 0$.

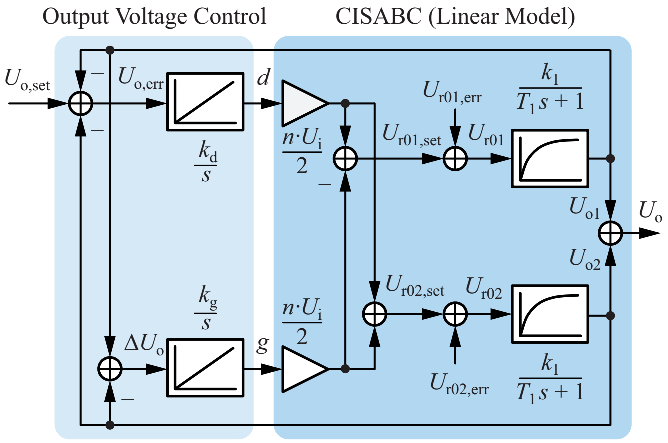

Output Voltage Control
CISABC (Linear Model)
$U_{\mathrm{o,set}}$
$U_{\mathrm{o,err}}$
d
$\frac{k_{\mathrm{d}}}{s}$
$\frac{n \cdot U_{\mathrm{i}}}{2}$
$U_{\mathrm{r01,err}}$
$U_{\mathrm{r01,set}}$
U_{r01}
$\frac{k_1}{T_1 s + 1}$
U_{o1}
U_{o}
U_{o2}
$U_{\mathrm{r02,set}}$
U_{r02}
$\frac{k_{\mathrm{g}}}{s}$
ΔU_{o}
g
$U_{\mathrm{r02,err}}$
–

Fig. 4.22: Complete linearised ISABC control model employing an integral output voltage controller acting on both inverter duty cycles d and a separate output voltage balancer acting on the deviation g of the inverter phase shift from the nominal value of 90 °.

4.2.4 Input Voltage Balancing

Exploiting the phase shift variation between the two inverters allows to compensate load asymmetries on the output voltage halves but in case of asymmetric output load the load distribution on the two inverters is also asymmetric. To maintain balanced input and output voltage even under heavy load asymmetries that could exceed the midpoint control capability of the VR, the two half-bridges of each inverter are distributed on the two input DC-links and DC blocking capacitors are introduced in the primary current path (Fig. 4.23a). The capacitance needs to be selected sufficiently high such that the resonance frequency with the total leakage inductance is approximately ten times lower than the switching frequency:

$$C_{\mathrm{dcblock}} > \frac{10}{(2\pi f_{\mathrm{s}})^2 L_{\sigma\mathrm{s,tot}}}. \tag{4.33}$$

This results in a relatively large (76 µF) capacitance for the case at hand, since it also needs to conduct the full primary current.

Another option is to use two LC resonant tanks that are fed by one of the inverter half-bridges and rectified by additional diodes (Fig. 4.23b).

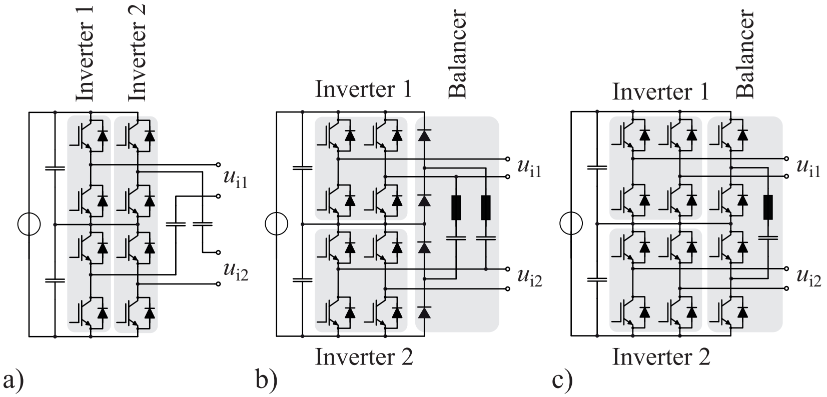


Fig. 4.23: Three options for balancing the input DC-links. (a) DC-blocking capacitors and each inverter is distributed on both DC-links. (b) Two resonant balancers fed by one inverter half-bridge and rectified using additional diodes. (c) Active resonant balancer.

Each of this balancing circuits is unidirectional, and therefore there is always only one of them operating, depending on the type of load asymmetry. A third option employing only one resonant balancing circuit is the active circuit shown in Fig. 4.23c which involves two additional half-bridges. The main advantage of the *LC* balancer circuits is that they are also able to balance the input DC-links during no load conditions, which otherwise would have to be achieved using two small balancing resistors.

Taking into account the additional components of the resonant balancing circuits, the first option still seems to be the most efficient solution. Especially, since DC-blocking capacitors are anyway necessary to avoid DC current that may occur in the primary winding because of small duty cycle errors. (Although they could be built using ceramic capacitors with a voltage rating of only a few volts if both half-bridges are connected to the same DC-link.)

4.2.5 PWM Generation

The gate signals for the inverter half-bridges have to be generated such that duty cycle updates are carried out as fast as possible to reduce the dead time to a minimum. At the same time it has to be guaranteed that no DC component is generated, as it could occur if the duty cycle is alternating between two values from one half-cycle to the next. The modulation scheme shown in Fig. 4.24 achieves both goals. The duty cycle is updated each half-cycle and each half-cycle contains always a positive and a negative output voltage part of equal duration. Therefore, the time integral of each inverter voltage contains no DC offset as shown for u_i in Fig. 4.24. The carrier is a triangular counter at two times the switching frequency. The duty cycle is updated every time the counter reaches zero. As soon as the counter reaches the current duty cycle level, the free-wheeling state is entered. After the counter has changed its direction the duty cycle level is reached a second time and the inverter output voltage is turned on with the inverse polarity as at the beginning of the pulse. A linear duty cycle ramp-up from 0 to 0.5 within two switching cycles is shown in Fig. 4.24. Although the average delay of each inverter is half a switching cycle, the delay of the no load rectifier voltage, which is a combination of both inverter voltages, is merely one fourth of the switching cycle, allowing high controller gain due to the small dead time. Since each inverter half voltage never contains a DC offset, also the combination of both inverter voltages which is applied to the transformer is pure AC at all times.

The phase shift also needs to be adjusted while the PWM is running to establish output voltage balancing. In order to avoid any DC offset the phase shift update is achieved by increasing the duration of the zero inverter voltage state (free-wheeling state) such that the required phase shift results. In Fig. 4.25 a change from zero phase shift to a positive value back to a negative value and finally back to zero is shown. Since for each phase shift change it only makes sense to delay one of the two inverter carriers, the average delay for a phase shift change is half a switching cycle.

4.2.6 Sampling Delay Reduction with Delta-Sigma ADCs

To minimize the measurement delay, Delta-Sigma ADCs (DS-ADCs) can be used for the hardware realisation of the output voltage controller and the output voltage midpoint balancing controller. The output of a DS-ADC is only a single bit (1-bit resolution) at high sampling frequency, which is 20 MHz with the employed DS-ADC [73]. The digital signal, therefore, is similar to a PWM of the analog signal [74]. Because of the

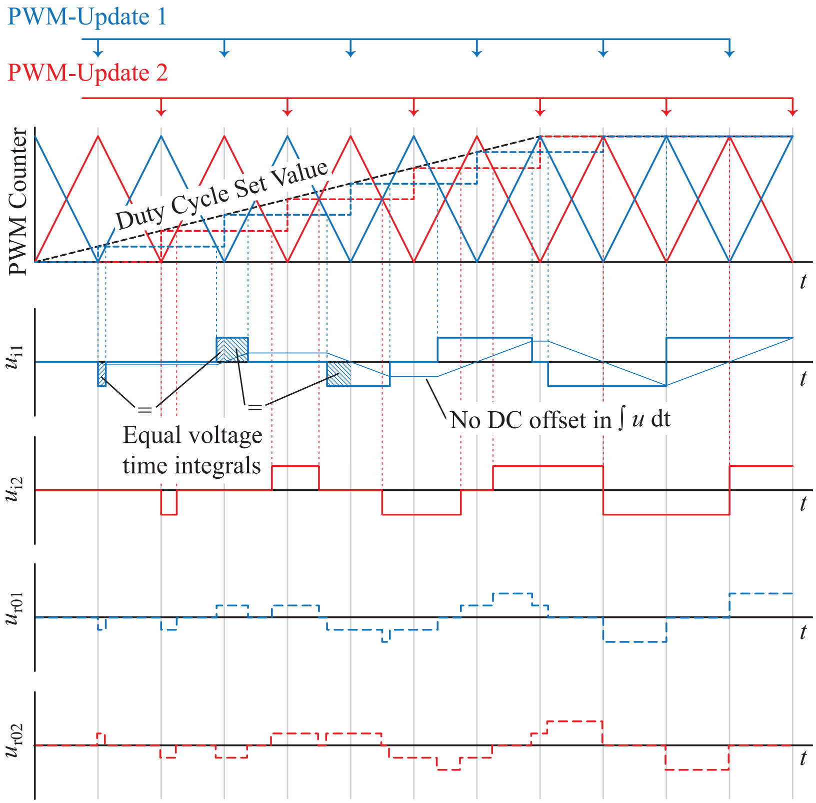

PWM-Update 1
PWM-Update 2
PWM Counter
Duty Cycle Set Value
t
u_{i1}
Equal voltage time integrals
=
=
No DC offset in $\int u\,\mathrm{d}t$
u_{i2}
u_{r01}
u_{r02}

Fig. 4.24: PWM modulation scheme for the ISAB with an update rate of twice the switching frequency and guaranteed DC-free inverter voltages. The duty cycle is ramped up from 0 to 0.5 within two switching periods. Each update of duty cycle on any inverter affects both no load rectifier voltages. Therefore, the effective delay for duty cycle updates is only one fourth of a switching cycle.

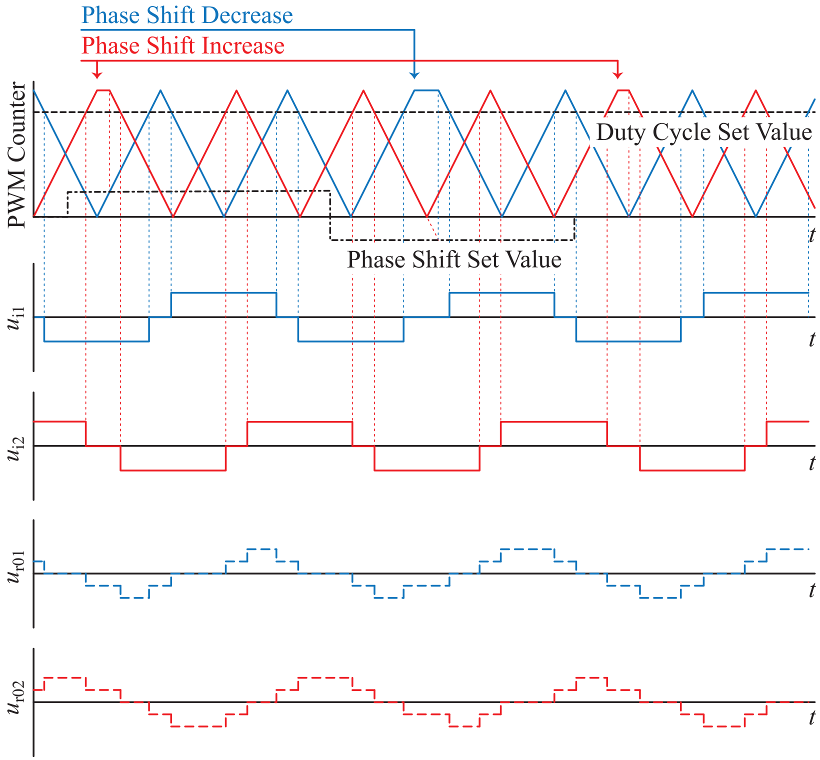

Phase Shift Decrease
Phase Shift Increase
PWM Counter
Duty Cycle Set Value
Phase Shift Set Value
t
u_{i1}
t
u_{i2}
t
u_{r01}
t
u_{r02}
t

Fig. 4.25: Implementation of phase shift changes for the ISAB PWM modulation scheme. A positive phase shift change is achieved by delaying the second inverter counter at its top value, effectively increasing the duration of the zero inverter output voltage state. Vice versa a negative phase shift change is achieved by delaying the first inverter carrier.

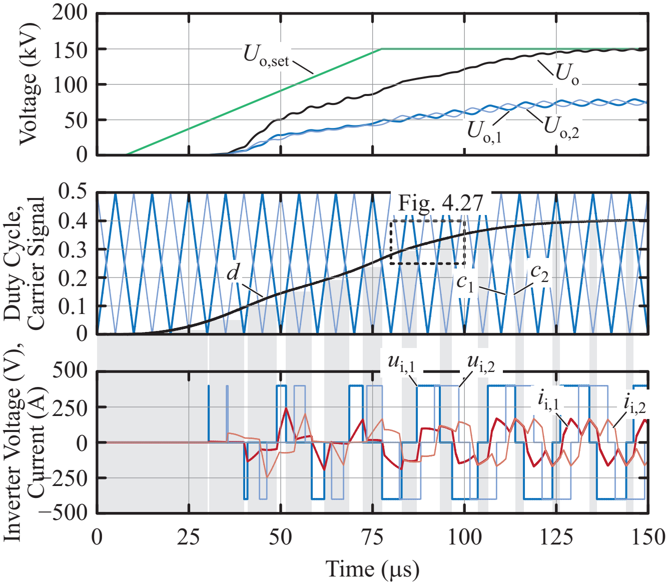


Fig. 4.26: Simulated output voltage set value ramp (step) showing the modulation using one triangular carrier with twice the switching frequency for each inverter, allowing to update each inverter voltage twice per switching period.

1-bit width the signal can be easily transmitted through isolators and single-bit transmission errors only have a small influence. Therefore, the signal is inherently noise resistant. In order to obtain a higher resolution, the bit-stream could be fed into a digital filter, typically a sinc3 [75]. Increasing the length of the filter increases the resolution, but also increases the delay. However, if the controller only consists of integrators, the measured output voltage bit-stream can be directly subtracted from a bit-stream of the output voltage set value and the difference can be directly fed into the integrator (counter). This way the measurement delay can be eliminated and the integrator output, which for the CISABC output voltage controller represents the inverter duty cycle, is updated at the full sampling rate of the DS-ADC.

The duty cycle, therefore, varies throughout one switching period. Fig. 4.26 shows a simulated step of the output voltage set value. In order to limit the inverter current positive output voltage set value changes are slew rate limited, resulting in a ramp. As the output voltage set value starts to rise, also the duty cycle set value for both inverters starts to increase. Note that each inverter updates its actual set duty cycle twice per switching period, i.e. once each half-period. Within each half-period the triangular carrier signal is incremented from 0 to 0.5 and then decremented back to 0 (see 4.26). At the beginning of a half-period the inverter output voltage is maintained as it is, i.e. either positive or negative. As soon as the rising carrier reaches the set duty cycle, the free-wheeling state is entered and the duty cycle is stored. When the carrier returns to the stored value of the duty cycle the inverter output voltage is switched to the opposite value as it was at the beginning of the half-period. This modulation scheme guarantees to avoid any DC inverter output voltage component since each inverter half-period contains a positive and a negative pulse with same duration. Furthermore, the duty cycle which is actually applied is the latest possible value, minimizing the PWM delay. Since both inverters are updated with twice the switching frequency and interleaved, updates for the total output voltage are processed at four times the switching frequency. Therefore, the output voltage rise-time of five switching cycles actually includes 20 duty cycle updates. A detailed view of the duty cycle calculation as it is actually implemented in a FPGA is shown in Fig. 4.27. First, the output voltage set value is also converted into a 1-bit stream $U_{\mathrm{o,set},\Delta\Sigma}$. By subtracting the output voltage bit-streams obtained from the DS-ADCs the output voltage error $U_{\mathrm{o,err},\Delta\Sigma}$ is calculated. Integrating this error by cumulative adding or subtracting a certain increment, which is proportional to the applied integral controller gain, the duty cycle set value is obtained. Due to the low resolution of the output voltage error the duty cycle set value still contains some ripple, the quantization noise of the DS-ADC. In order to prevent multiple switching actions per half-cycle or a DC component of the inverter voltage the first duty cycle value that is greater or equal than the rising carrier is locked-in for the rest of the half-cycle.

4.3 Loss Distribution

The DC-DC conversion efficiency is calculated for the full operating range for a high-voltage generator with the CISABC topology and with a conventional SRC operated at constant switching frequency. The specifications and component values of the circuits are shown in Fig. 4.29; the

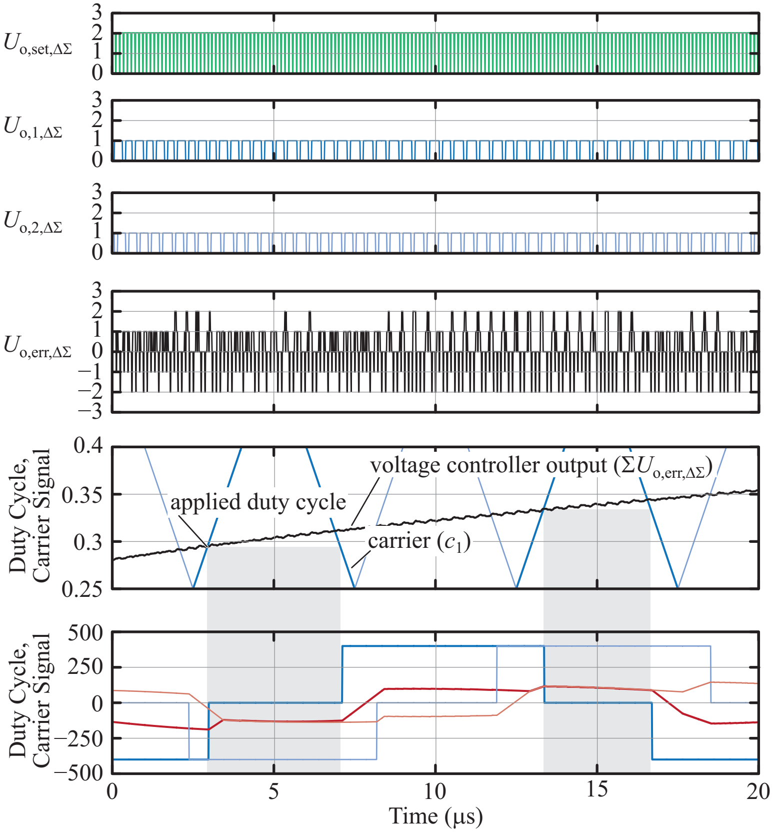


Fig. 4.27: Detailed view of the duty cycle calculation by integrating the difference between output voltage set value bit-stream and measured output voltage bit-streams during one switching period as implemented on a FPGA.

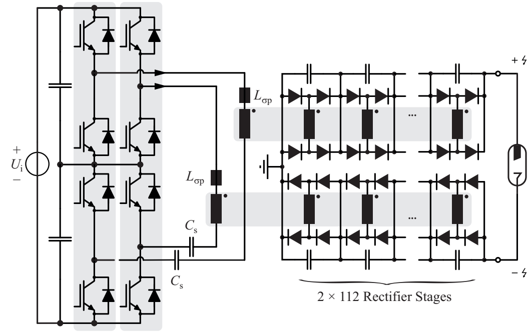

+
U_i
−
$L_{\sigma p}$
$L_{\sigma p}$
C_s
C_s
...
...
+ ⚡
− ⚡
2 × 112 Rectifier Stages

Fig. 4.28: Circuit of the SRC considered in the efficiency comparison shown in Figs. 4.30, 4.31.

CISABC		SRC	
U_i	800V	U_i	800V
$U_{o,max}$	150kV	$U_{o,max}$	150kV
P_{max}	60kW	P_{max}	60kW
f_s	50kHz	f_s	50kHz
N_p	2×6	N_p	12
N_s	112×14	N_s	112×14
$L_{\sigma p}$	1.25μH	$L_{\sigma p}$	5μH
$C_{dcblock}$	74μF	C_s	2μF

Fig. 4.29: Component values and specifications of the CISABC and SRC considered in the efficiency comparison.

circuit of the SRC is shown in Fig. 4.28. The inverter is using five 650 V IGBTs [76] in parallel, and the high-voltage rectifier consists of 112 full-bridge rectifiers per transformer equipped with 1 kV diodes [77]. The numbers of turns are determined for a maximum flux density of 0.3 T with a UR72/65/39 N87 ferrite core for a switching frequency of 50 kHz. The result is shown in Fig. 4.30. The SRC allows higher efficiency at the highest output voltage, but lower efficiency at the maximum output current. Therefore, the maximum inverter losses with the CISABC are $\approx 1450\,\mathrm{W}$ but $\approx 1900\,\mathrm{W}$ with the SRC.

A detailed break up of the losses at different operating points for the CISABC and the SRC is shown in Fig. 4.31. The SRC only provides low losses at high output voltages due to the low switching losses because of (almost) zero current switching. At lower output voltages the switching losses increase drastically resulting in considerably higher total losses than with the CISABC.

4.4 Experimental Results

In order to demonstrate the functionality of the proposed CISABC circuit and control scheme without requiring high-voltage equipment the prototype uses transformers with a lower ($n = 9 : 6$) turns ratio. The transformer core is the same as will be used for the high-voltage version including also the number of turns of the primary windings and the isolation distance between primary and secondary. A photograph of the test set-up is shown in Fig. 4.32. Since only short ($< 1\,\mathrm{ms}$) pulses are required to demonstrate the functionality, the two inverters are supplied by a 23.5 mF, 400 V electrolytic capacitor bank. All inverter half-bridges are connected in parallel to this capacitor bank. The inverters are operated with 50 kHz using 650 V IGBTs [78]. The transformers use N87 ferrite cores, two six-turns 0.5 mm foil primary windings and one nine-turn 820 × 200 µm litz wire secondary winding that resembles the geometry of the 112 14-turn secondary windings that are used on the high-voltage version. The low winding capacitance of the equivalent transformer is justified, since the total winding capacitance of the high-voltage transformer will be comparable, due to the partitioning of the winding into 112 parts each connected to a separate rectifier stage. The AC winding voltage is therefore only 670 V at 150 kV output voltage. The secondary windings of the equivalent transformers used in the low-voltage test set-up are connected to two rectifier

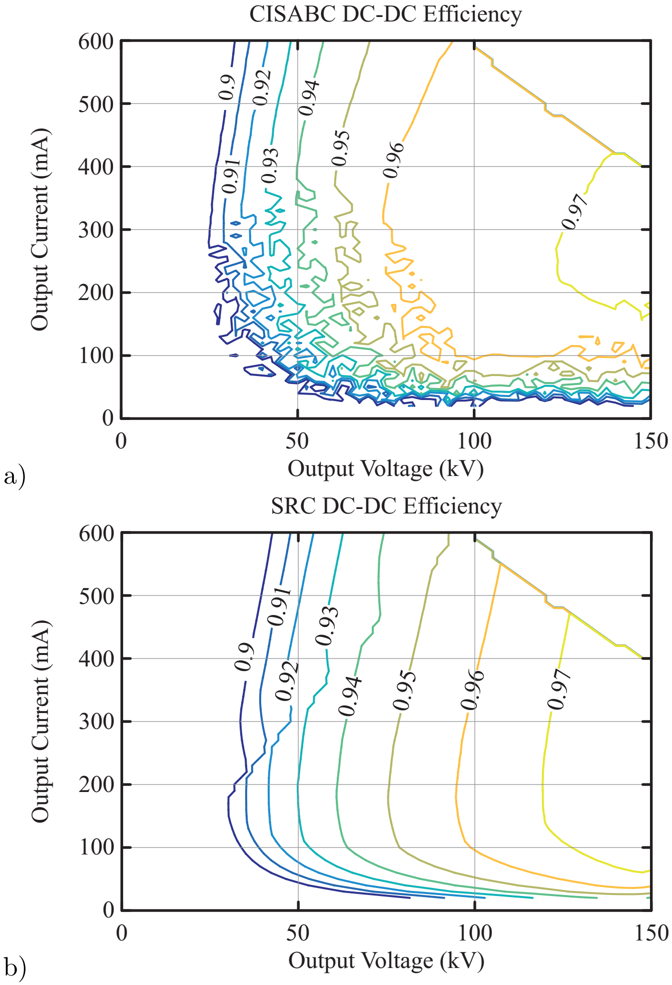


Fig. 4.30: DC-DC conversion efficiency of high-voltage generator with CISABC topology (a) and SRC topology (b). The corresponding pie charts (see Fig. 4.31) are scaled to represent the absolute loss value.

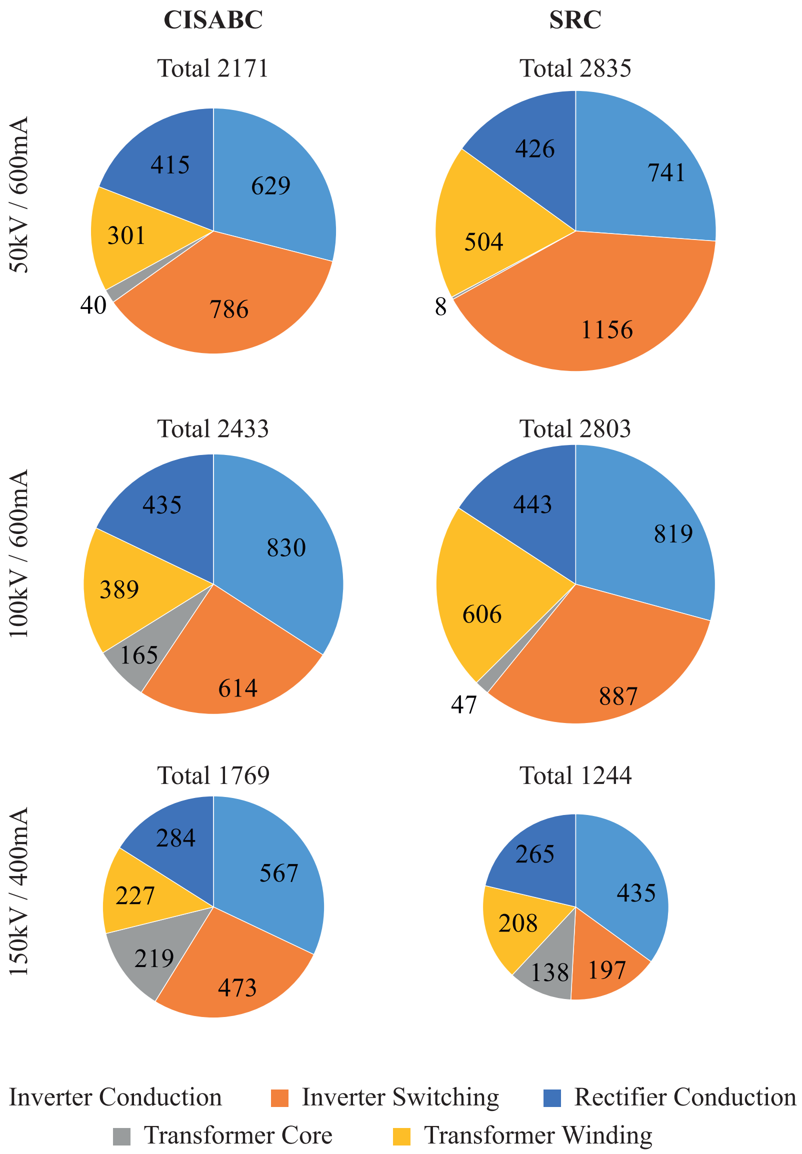


Fig. 4.31: Distribution of the losses on the components of the high-voltage generator with CISABC and SRC topology at different output voltages and maximum output current.

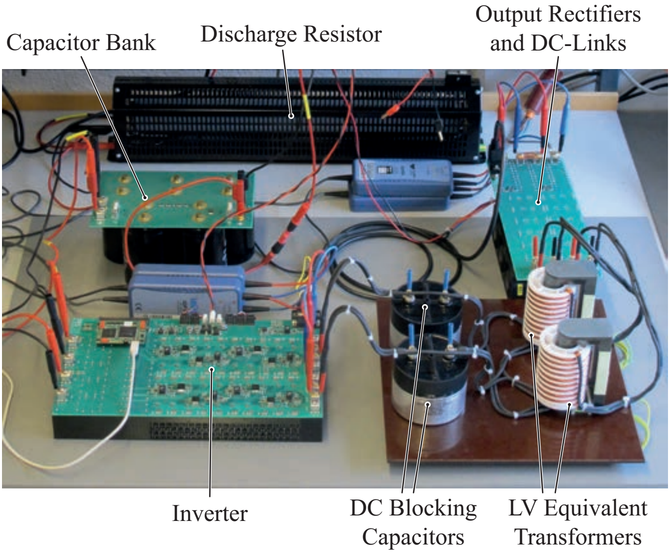

Capacitor Bank
Discharge Resistor
Output Rectifiers and DC-Links
Inverter
DC Blocking Capacitors
LV Equivalent Transformers

Fig. 4.32: Experimental set-up of the high-voltage generator equipped with $n = 9 : 6$ low-voltage transformers using same cores and winding geometry as in the projected high-voltage transformers.

stages using 650 V Si diodes [79] with 7.6 µF output capacitors. The load resistor connected to the output is not shown in the photograph.

4.4.1 Inverter Testing

The CISABC normally allows soft switching under all load and output voltage conditions. However, the peak currents that have to be turned off can be relatively high. For the designed 60 kW inverter the highest currents appear at low output voltage and high output current. When the tube voltage is set to 50 kV and the tube current is 600 mA each inverter turns off a current of ≈ 250 A. Due to the relatively short turn-off times of the Infineon IGBT5 series the switching loss is only 3.5mJ at that current level using five 50A rated devices in parallel. However, since the employed IGBTs have no avalanche rating low-inductance commutation loop design is essential to keep the switching overvoltage below the breakdown voltage of 650 V, without increasing the gate resistor to a value higher than the one used for the switching loss measurements specified in the data sheet.

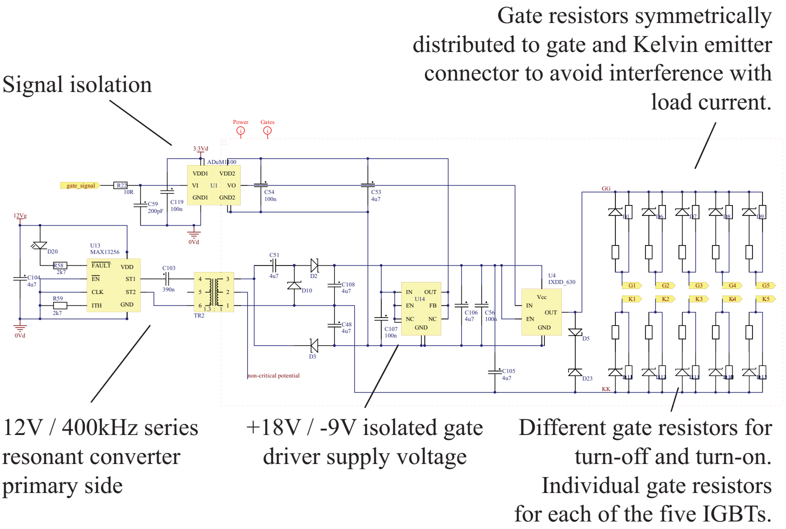
Gate Resistor Selection

The gate driver uses a bipolar voltage supply with -9 V for the off-state and 18 V for the on-state. The gate resistor values in the data sheet [78] are specified for a 15 V / 0 V supply. In order to reach similar switching losses as specified in the data sheet, the gate resistor values for turn-off and turn-on have to be calculated such that the typical current fall-time (23 ns) and rise-time (8 ns) as specified in the data sheet is obtained. The current fall-time is the time that it takes the gate voltage to fall from the Miller voltage U_{mill} to the threshold voltage U_{th}. After the Miller plateau the gate voltage follows

$$u_{\text{g,off}}(t) = (U_{\text{on}} - U_{\text{off}}) \cdot \mathrm{e}^{-\frac{t}{R_{\text{g,off}} C_{\text{g}}}} + U_{\text{off}} \tag{4.34}$$

with the on-state supply voltage U_{on}, the off-state supply voltage U_{off}, the turn-off gate resistor $R_{\text{g,off}}$ and the gate capacitance C_{g}, which can be used to calculate the required gate resistor for a given fall-time. For $t_{\text{f}} = 23\,\text{ns}$, $C_{\text{g}} = 3.1\,\text{nF}$, $U_{\text{th}} = 4\,\text{V}$ and $U_{\text{mill}}(50A) = 6.5\,\text{V}$ the turn-off gate resistor per TO-247 IGBT is

$$R_{\text{g,off}} = \frac{t_{\text{f}}}{C_{\text{g}} \ln(\frac{U_{\text{mill}} - U_{\text{off}}}{U_{\text{th}} - U_{\text{off}}})} = 42.2\,\Omega. \tag{4.35}$$



Signal isolation

Gate resistors symmetrically distributed to gate and Kelvin emitter connector to avoid interference with load current.

12V / 400kHz series resonant converter primary side

+18V / -9V isolated gate driver supply voltage

Different gate resistors for turn-off and turn-on. Individual gate resistors for each of the five IGBTs.

Power
Gates
3.3Vd
ADuM1100
VDD1
VDD2
VI
U1
VO
GND1
GND2
gate_signal
R22
10R
C59
200pF
C119
100n
0Vd
C54
100n
C53
4u7
12Vg
D20
U13
MAX13256
R58
2k7
FAULT
VDD
EN
ST1
CLK
ST2
ITH
GND
C104
4u7
R59
2k7
0Vd
C103
390n
4
5
6
3
2
1
1.3 : 1
TR2
C51
4u7
D2
D10
C108
4u7
C48
4u7
D3
non-critical potential
IN
OUT
U14
EN
FB
NC
NC
GND
C107
100n
C106
4u7
C56
100n
U4
IXDD_630
Vcc
IN
OUT
EN
GND
C105
4u7
D5
D23
GG
KK
D1
D6
D7
D8
D9
G1
G2
G3
G4
G5
K1
K2
K3
K4
K5

Fig. 4.33: Gate driver circuit schematic.

At turn-on the gate voltage rises according to

$$u_{\mathrm{g,on}}(t) = (U_{\mathrm{on}} - U_{\mathrm{off}}) \cdot (1 - \mathrm{e}^{-\frac{t}{R_{\mathrm{g,off}} C_{\mathrm{g}}}}) + U_{\mathrm{off}}. \qquad (4.36)$$

Therefore, the gate resistor for the typical current rise-time of $t_{\mathrm{r}} = 8\,\mathrm{ns}$ as specified in the datasheet can be calculated as

$$R_{\mathrm{g,on}} = \frac{t_{\mathrm{r}}}{C_{\mathrm{g}} \ln(\frac{U_{\mathrm{on}} - U_{\mathrm{th}}}{U_{\mathrm{on}} - U_{\mathrm{mill}}})} = 13.1\,\Omega. \qquad (4.37)$$

Finally, the selected gate resistor values are $R_{\mathrm{g,off}} = 44\,\Omega$ and $R_{\mathrm{g,on}} = 22\,\Omega$ since this allows to use only $44\,\Omega$ resistors for the gate driver circuit (see Fig. 4.33). Each of the five parallel IGBTs is connected via individual gate resistors. Furthermore the gate resistors of each IGBT are split in two halves placed on the gate and on the emitter pin. This way load and gate current are separated as good as possible, also due to the 4-pin package that provides a Kelvin emitter pin.

Commutation Loop Layout

In order to limit the switching overvoltage at turn-off to a given level $U_{\mathrm{ov}} = 100\,\mathrm{V}$ at a current fall-time of $t_{\mathrm{f}} = 23\,\mathrm{ns}$ at a switched current of $I = 300\,\mathrm{A}$, the commutation loop inductance must not exceed the value of

$$L_{\mathrm{com,max}} = \frac{U_{\mathrm{ov}} t_{\mathrm{f}}}{I} = 7.67\,\mathrm{nH}. \tag{4.38}$$

Since the inductance of one TO-247 is $L_{247} = 13\,\mathrm{nH}$, the contribution of one half-bridge consisting of two groups of five TO-247 packages parallel is $L_{\mathrm{hb}} = 2\frac{L_{247}}{5} = 5.2\,\mathrm{nH}$. Therefore, only 2.47 nH are available for the DC-link and the PCB tracks, demanding for wide co-planar tracks placed on two adjacent layers of the PCB and a large number of film capacitors placed in parallel to reduce the total Equivalent Series Inductance (ESL) which is in the range of 25 nH for a single capacitor.

Another issue is the current sharing between the paralleled IGBTs. This is achieved by placing the AC connection on one side of the half-bridge and the DC link on the other side as illustrated in Fig. 4.34. Note, that by placing the components in a row with AC connection on one side and DC connection on the other side, the current path lengths are the same for all IGBTs. The two half-bridges have to be supplied by individual plus and minus rails in order to guarantee equal current path lengths also during the free-wheeling state (zero output voltage). In order to minimize the inductance of the two commutation loops, the plus and minus rails of each half-bridge have to be on two layers next to each other as shown in Fig. 4.34.

The arrangement of the switches of the two full-bridges on the PCB is shown in Fig. 4.35. Although the DC-link planes are only $w = 62\,\mathrm{mm}$ wide and at most $l = 215\,\mathrm{mm}$ of average length, due to the distance of only $d = 0.2\,\mathrm{mm}$ given by the 8 layer PCB, the inductance introduced by the PCB planes is only

$$L_{\mathrm{pcb}} = \mu_0 \frac{ld}{w} = 0.87\,\mathrm{nH}. \tag{4.39}$$

Therefore, the value that remains for the total ESL of the DC-link is $\mathrm{ESL}_{\mathrm{max}} = L_{\mathrm{com,max}} - L_{\mathrm{hb}} - L_{\mathrm{pcb}} = 1.6\,\mathrm{nH}$. The ESL per capacitor is usually around 25 nH [80]. Therefore, at least 16 film capacitors in parallel are required. Finally, $24 \times 4\,\mu\mathrm{F}$ EPCOS B32794D2405K capacitors are selected to form a DC-link with $C = 96\,\mu\mathrm{F}$, $\mathrm{ESL} = 1.04\,\mathrm{nH}$ and $I_{\mathrm{max}} = 144\,\mathrm{A}$ per full-bridge.

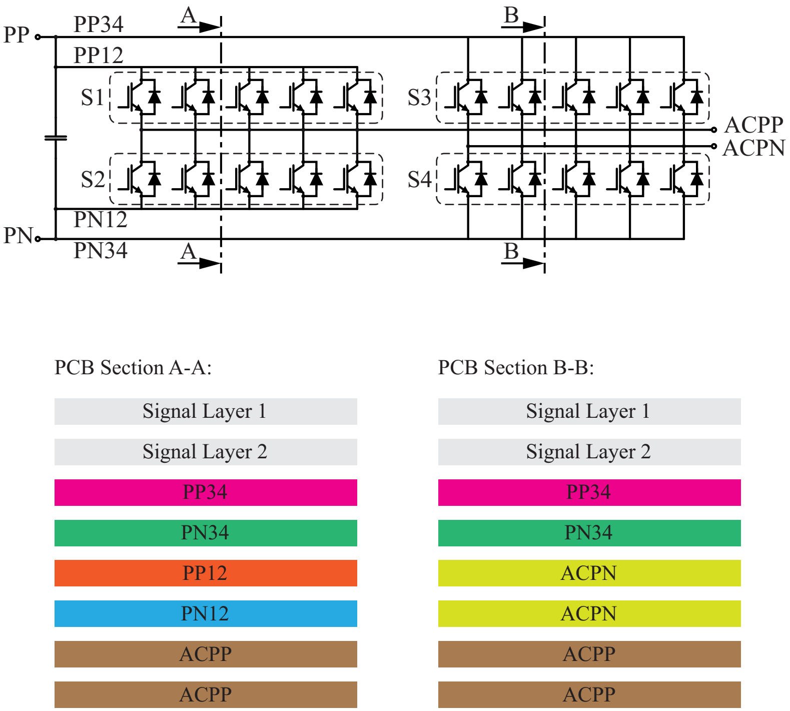

PP
PP34
PP12
A
B
S1
S3
ACPP
ACPN
S2
S4
PN12
PN
PN34
A
B
PCB Section A-A:
Signal Layer 1
Signal Layer 2
PP34
PN34
PP12
PN12
ACPP
ACPP
PCB Section B-B:
Signal Layer 1
Signal Layer 2
PP34
PN34
ACPN
ACPN
ACPP
ACPP

Fig. 4.34: Power circuit schematic with five IGBTs in parallel and cross section of the PCB planes at two locations.

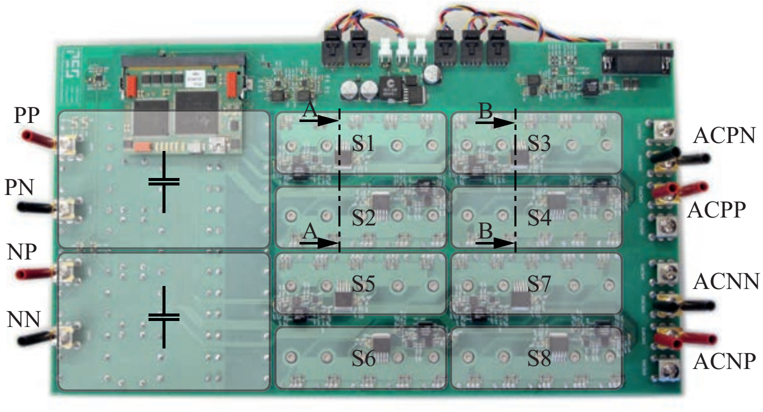


Fig. 4.35: Arrangement of the power components on the inverter PCB.

Switching Test

The total commutation loop inductance of the half-bridge farthest from the DC-link sums up to $L_{\text{com}} = 7.11\,\text{nH}$. Theoretically, with the selected gate resistors this results in an overvoltage of $U_{\text{ov}} = 93\,\text{V}$ at 300 A switched current. The experiment shows that the actual overvoltage is slightly higher, namely 132 V on the half-bridge S3-S4 and 149 V on the half-bridge S7-S8. The waveforms are shown in Fig. 4.36. Although, the overvoltage is slightly higher than expected, there is still a sufficient margin to the breakdown voltage of 650 V.

4.4.2 Steady-State Operation

Measured waveforms of the inverter and rectifier side voltages and currents representing working point A of the nominal operating range (Fig. 4.38) are shown in Fig. 4.37. Note, that the rectifier currents are obtained only mathematically using (4.9) from the measurements taken on the primary side. With the equivalent transformer used, the set voltage for this operating point of 853 V at 71 A represents an output voltage of 150 kV at 400 mA with the real system. This point of maximum voltage and maximum power (60 kW) is located in the region of DCM1. Therefore, the current on the rectifier side is discontinuous while the current on the inverter side is continuous. The measurement

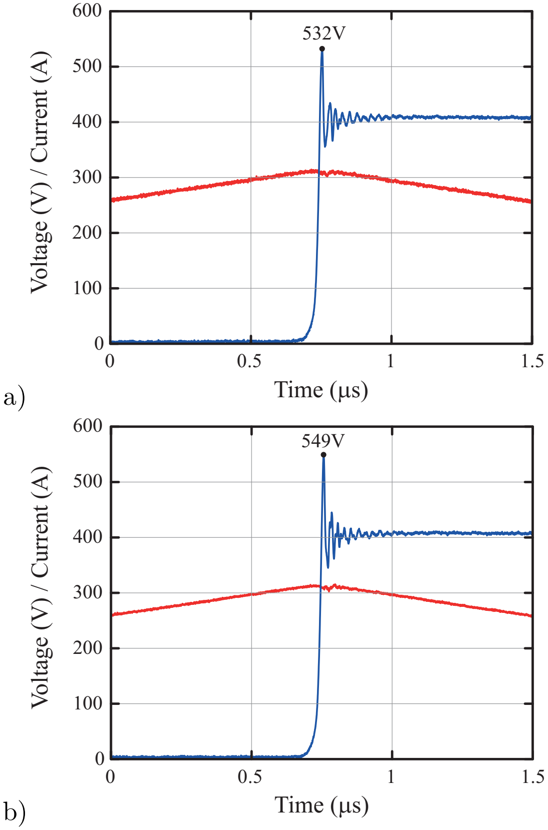


Fig. 4.36: Inductive switching test of 300 A at 400 V with half-bridge S3-S4 (a) and half-bridge S7-S8 (b).

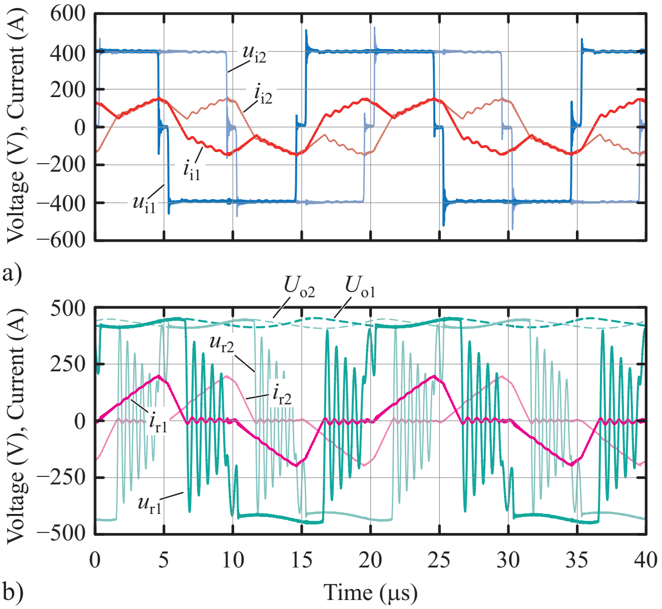


Fig. 4.37: Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point A of Fig. 4.38 with 853 V output voltage and 60 kW output power.

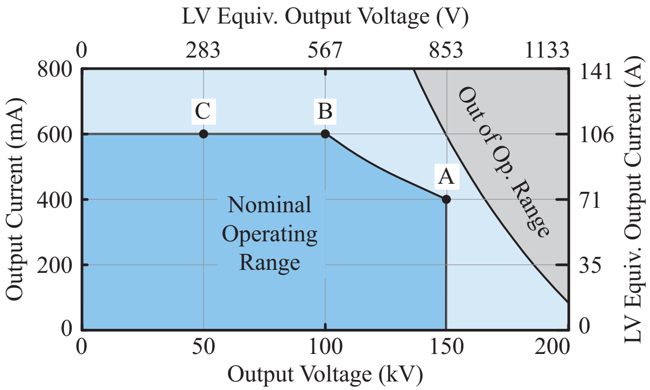


Fig. 4.38: Nominal operating range and experimentally tested working points shown with separate scales for voltage and current for the high-voltage and the low-voltage equivalent transformers.

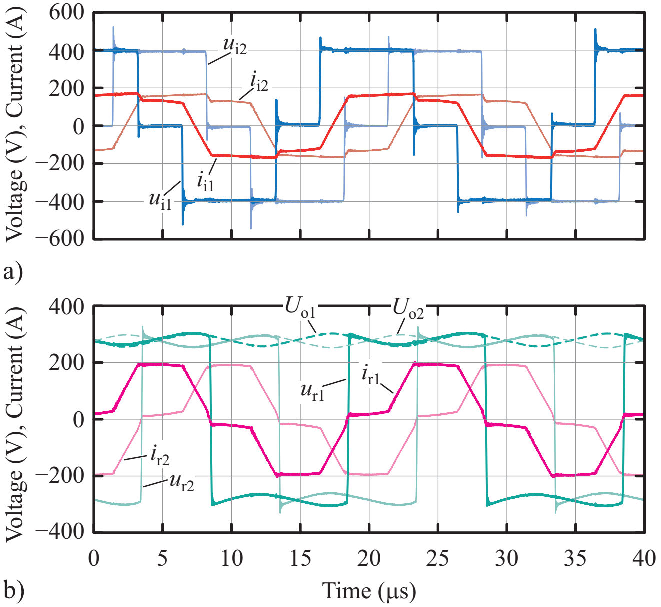


Fig. 4.39: Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point B of Fig. 4.38 with 567 V output voltage and 60 kW output power.

also shows the typical ringing of the rectifier capacitance with the transformer leakage inductance during the current zero state causing small oscillations also in the inverter currents. However, as expected ZVS is obtained in both inverters. The waveforms representing operating point B, i.e. 567 V output voltage and 106 A output current, are provided in Fig. 4.39. This operating point marks the lowest voltage, equivalent to 100 kV, at which the maximum power of 60 kW has to be transferred. The rectifier current waveform is still continuous and resembles the shape of CCM2. The inverter duty cycle in this measurement is $d = 0.35$ and with $U_{\mathrm{o,max}} = nU_{\mathrm{i}} = 1200\,\mathrm{V}$ the ratio $\frac{U_{\mathrm{o}}}{U_{\mathrm{o,max}}} = 0.47$. Therefore, this agrees with the conduction mode boundaries specified in Fig. 4.11. Also in this mode both inverters operate with ZVS. The waveforms representing operating point C, i.e. maximum specified output current at $\frac{1}{3}$ of the maximum output voltage are shown in Fig. 4.40. With the low-voltage equivalent transformer the voltage set value is 283 V at 106 A

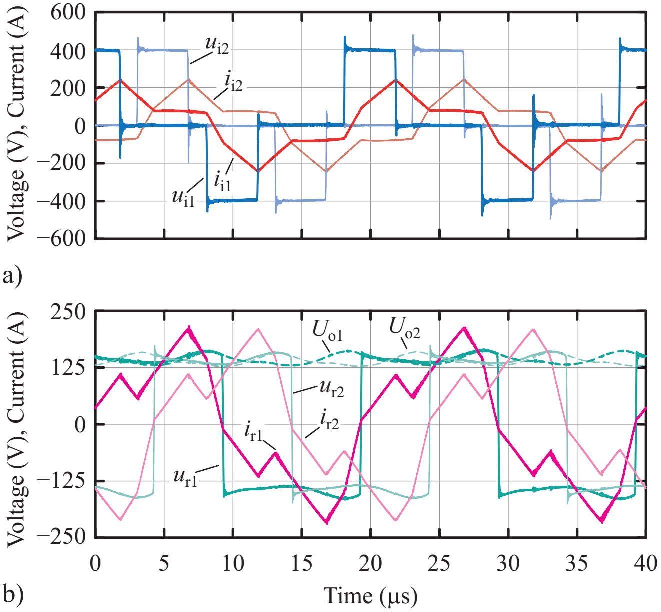


Fig. 4.40: Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point C of Fig. 4.38 with 283 V output voltage and 30 kW output power.

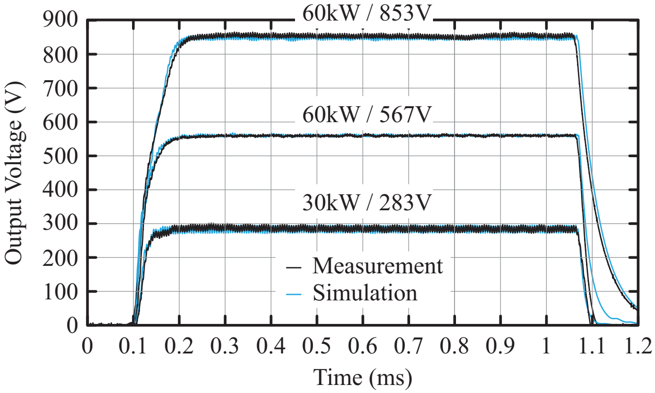


Fig. 4.41: Measured closed-loop controlled set value pulses for the low-voltage equivalent operating points corresponding to Fig. 4.38a compared to circuit simulations.

output current, corresponding to 50 kV, 600 mA with the high-voltage transformer. With a ratio of $\frac{U_\text{o}}{U_\text{o,max}} = 0.24$ and a duty cycle of $d = 0.19$, according to Fig. 4.11, this operating point is located within the region of CCM3 as the shape of the rectifier current proves. The measurement also confirms ZVS for this operating point.

4.4.3 Output Voltage Control

For the three operating points investigated in the previous section also set value step responses are measured. The results are shown in Fig. 4.41 and compared to the results obtained from a circuit simulation. As it is shown there is little deviation from the simulation, i.e. it is likely that all relevant parasitic elements are modelled correctly. Note, that the simulation applies exactly the same control algorithm as implemented in the FPGA, including models of the DS-ADCs used for the output voltage measurements. Of the passive components only the leakage inductance $L_{\sigma\text{s,tot}} = 2.8\,\mu\text{H}$, the output capacitance $C_\text{o} = 7.6\,\mu\text{F}$ and the load resistance R_o equaling $12\,\Omega$ in operating point A, $5.4\,\Omega$ in operating point B and $2.7\,\Omega$ in operating point C are modelled. Switches and diodes are modelled ideally. As can be seen, the output voltage rise-time for all operating points is less than 100 µs (5 switching cycles). The achievable

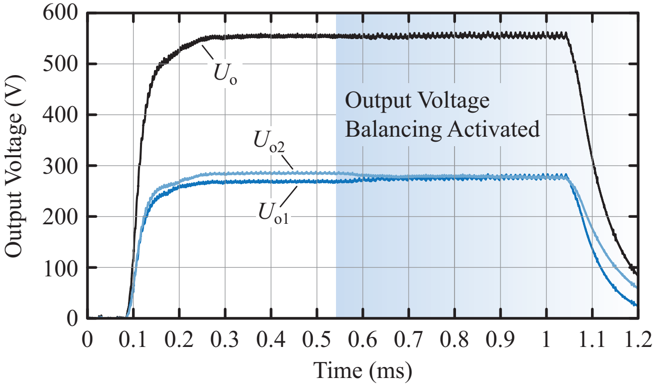


Fig. 4.42: Measured output voltage pulse with asymmetric load ($R_{o1} = 7.5\,\Omega$, $R_{o2} = 12.5\,\Omega$) and delayed activation of the balancing controller.

rise-time is lower for lower values of load resistance.

4.4.4 Output Voltage Balancing

The effect of the proposed output voltage balancing control by varying the phase shift is shown in Fig. 4.42. With an output voltage set value of 560 V and the two rectifier stages loaded with $R_{o1} = 7.5\,\Omega$ on the upper and $R_{o2} = 12.5\,\Omega$ on the lower DC-link, the output voltage is ramped up with the balancing controller disabled. A slight deviation of the two output voltages due to the negative slope of the output current - output voltage characteristic (Fig. 4.14) results. Activating the output voltage balancing controller equalizes the output voltages within $< 100\,\mu s$. The total output voltage value is not affected due to the low coupling between the total output voltage controller and the balancing controller.

4.5 Summary of the Chapter

A novel interleaved circuit variant, the CISABC, is proposed. The circuit connects two transformers, or at least one transformer with two magnetic paths, such that the no-load secondary voltages are obtained proportional to the sum and/or the difference of the two inverter voltages.

The circuit exhibits in total six continuous and discontinuous conduction modes which are analysed in detail with analytic expressions for the output current - duty cycle relationship and the boundaries between the conduction modes provided. A robust to noise and yet fast digital control based on Delta-Sigma ADCs is proposed and implemented on an FPGA. Furthermore, it is shown that the output voltages can be actively balanced employing the phase shift between the inverters in case of asymmetric load. The control strategy is demonstrated on a 60 kW, 50 kHz prototype, achieving 100 µs (five switching cycles) output voltage rise- and fall times.

The CISABC features several advantages over the ISABC and the SRC. Compared to the ISABC, the main advantage is the lower inverter RMS current. Depending on the operating point the inverter current of the CISABC can be as low as half the value obtained with the ISABC. Furthermore, the maximum possible output current which is limited by the leakage inductance is up to three times higher with the CISABC than with the ISABC at the same core peak flux density. Compared to the SRC the CISABC mainly provides the advantage of ZVS (or at least ZCS) over the full operating range with constant switching frequency. Additionally, the non-resonant structure of the CISABC exhibits only a first-order system compared to the second-order system of the SRC, allowing fast output voltage control. Finally, compared to non-interleaved circuits the low output voltage ripple of the CISABC allows a small output capacitance which is necessary to achieve short output voltage fall-times with passive rectifiers.

One main disadvantage of the proposed solution is that it requires two transformers, or at least a transformer with two flux paths. For the given application this is acceptable since using two transformers allows to reduce the 150 kV isolation requirement to only 75 kV between winding and core. Further, the CISABC exhibits slightly higher RMS currents on the rectifier side than the ISABC on parts of the operating range. However, since the losses in the rectifier diodes are mainly caused by the average current, which is the same as the one of the ISABC, this is only a minor downside.

In summary the low inverter RMS currents and the ZVS or at least ZCS inverter commutation on the full operating range allow to keep the inverter losses low while constant switching frequency guarantees low control complexity. The interleaved operation allows to reduce the output capacitance, and double the duty cycle update rate, such that in combination with the first-order dynamic behaviour of the CISABC high output voltage control bandwidth is achieved. The proposed circuit and control structure is, therefore, a good choice for applications that allow only a passive secondary side (diode) rectifier but require fast output voltage rise- and fall times, as demonstrated on a prototype for a high-voltage X-ray power supply.

5

Conclusions and Outlook

Current improvements of X-ray-based medical imaging systems are driven by the demand for increased image quality, lower patient dose and lower system cost. These three main aspects are targeted by the research presented in this work. Finding the balance between increased functionality and performance on the one side and overall system cost reduction on the other side is crucial. In many industrialized nations, the market for medical equipment resides in an environment of ageing societies and consequently stressed health care budgets. At the same time emerging countries, are aiming to provide health care services to a wider population but are also struggling with limited financial resources. Low-cost systems are therefore required by a wide range of customers in order to guarantee affordable medical care for all people. However, compromises in image quality and functionality are not accepted by existing costumers. Instead, at the same time additional functionality is requested such as the ability to work with weak power grids and different nominal voltages as well as short tube voltage rise- and fall-times in order to reduce the patient dose and enable dual energy applications.

5.1 Results and Conclusion

The system investigated within this work has to provide a wide input voltage range at the mains side, allowing to operate with weak grids and 400 V or 480 V nominal voltages of the three-phase mains. On the high-voltage side up to 150 kV and 60 kW have to be supplied to the tube with shortest possible voltage rise- and fall-times.

For the design of the rectifier a TCO analysis has been carried out to find the optimum trade-off between material cost and loss energy cost by properly dimensioning the passive components. The high peak-to-average load ratio, which is limited by the maximum average cooling power of the tube of only $\approx 800\,\mathrm{W}$, enables extremely high peak power density of the passive components. However, it turned out that the minimum TCO is not obtained at the highest power density (thermal limit) but obtained as optimum from the trade-off between material cost and loss energy cost.

At the time of the analysis silicon IGBTs in combination with the VR topology resulted as most advantageous combination due to the three-level characteristic and the low cost and high reliability of the semiconductors. Because of the IGBTs relatively high switching energy loss, only a moderate switching frequency of 28 kHz results. Due to the high peak-to-average power ratio, however, a power density of $9.56\,\mathrm{kW/dm^3}$ is achieved by exploiting the thermal capacitance of the inductors. The measured efficiency of the rectifier is 97.3 % at nominal load. Due to the low boost inductor volume a high current ripple results which creates input current distortions with conventional control schemes. One main contribution presented in this work solves this issue by applying pre-calculated duty cycle values from look-up tables to maintain sinusoidal input currents also during light load operation, which is a common use case for X-ray high-voltage generators. Measurements of the constructed prototype show that the input current THD can be reduced from 26.9 % to 6.5 % at 25 % load.

On the output side a novel DC-DC converter topology is shown in this work. Using an interleaved coupled arrangement of two high-voltage transformers the series resonant capacitors used within nowadays high-voltage generators can be eliminated. The proposed topology enables ZVS on the inverters with constant switching frequency, rendering it particularly well-suited for possible design updates employing MOSFETs. Also with the employed low turn-off loss IGBTs a switching frequency of 50 kHz is possible resulting in an output voltage rise-time of only 100 µs. The short rise-time of five switching cycles is a result of the fast dynamics of the non-resonant topology and the low output capacitance of the series interleaved arrangement.

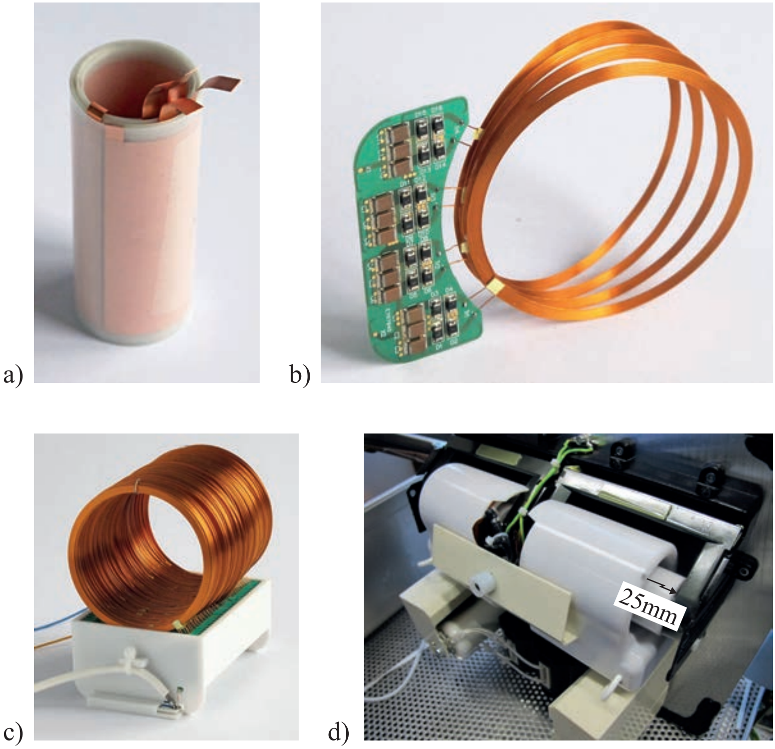


Fig. 5.1: High-voltage transformer prototype. a) Primary windings; b) four secondary windings with rectifier stages; c) 112 rectifier stages and secondary windings assembly; d) assembly of two transformers in oil tank with location of break-down at 150 kV total voltage.

5.2 Future Research and Outlook

This work is focused on the three-phase rectifier and the inverter part of the high-voltage generator. Future investigations need to pay more attention to the high-voltage transformer design. A first prototype (Fig. 5.1) constructed within this work, based on the same core as used in existing systems, exhibited an isolation failure while testing with a total output voltage of 150 kV. The reason for that is most likely a cavity present in the 3D-printed coil former. Therefore, the construction needs to be adapted in order to avoid 3D-printed parts and possibly need to employ an electric field shielding structure that covers the high-voltage edge of the winding stack. Yielding at the same time a cost-effective, easily manufacturable design is another challenging aspect of this task.

First tests with the high-voltage transformer also revealed that the high-voltage measurement dividers used in nowadays systems cannot be fully compensated, therefore only provide limited bandwidth which is too low to achieve the same output voltage rise- and fall-times as presented in this work. A voltage divider which is integrated on the PCBs of the rectifier stage is proposed to meet this requirement.

If necessary, e.g. for dual energy CT, the output voltage rise- and fall-times of 100 µs achieved with 50 kHz could be further improved at the price of using SiC MOSFETs for the inverters. However, assuming a switching frequency of 200 kHz could be reached with the inverter, the required high-voltage DC capacitance is only 30 pF. This value is however already reached with 40 cm of the currently used high-voltage cable that connects the high-voltage generator to the tube. Therefore, with unidirectional systems a further increase of the switching frequency also implies changes to the mechanical construction, i.e. the arrangement of oil tank and X-ray tube in order to minimize the load capacitance.

A

Conduction Modes of the Coupled Interleaved Single Active Bridge Converter

THE derivation of the duty cycle - output current relationships for the different conduction modes of the CISABC and the boundaries between the different conduction modes are presented in the following.

A.1 Discontinuous Conduction Modes

A.1.1 Discontinuous Conduction Mode 1

For high values of duty cycle and high output voltage, as in working point A indicated in Fig. 4.14, the CISABC operates in DCM1. The characteristic waveforms of rectifier current, rectifier voltage and rectifier no-load voltage for this case are shown in Fig. 4.12a. It is assumed, that the outputs are loaded symmetrically, therefore only the situation of one of the two rectifier sides is considered. Furthermore, because of the half-cycle symmetry of the signals, only the positive rectifier current half-cycle is regarded. Assuming $0.5 > d > 0.25$ the rectifier no-load voltage varies between all five values. If it is also assumed that $nU_\mathrm{i} > U_\mathrm{o} > \frac{nU_\mathrm{i}}{2}$, the rectifier current is only rising while the rectifier no-load voltage equals nU_i, its full-level. Hence, assuming the rectifier current as actually discontinuous, the rectifier current has to be zero when the rectifier no-load voltage value changes from half-level to full-level and this last rising edge of the rectifier no-load voltage marks the beginning of the positive current half-cycle. Each current half-cycle is partitioned into three conduction intervals. During the first interval the rectifier current rises for

$$T_{\mathrm{I}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}} \tag{A.1}$$

with the switching period $T_{\mathrm{s}} = \frac{1}{f_{\mathrm{s}}}$. As soon as the rectifier no-load voltage changes to half its positive maximum level, interval II begins and the rectifier current changes for

$$T_{\mathrm{II}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,II}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \tag{A.2}$$

For DCM1 it is assumed, that the current does not reach zero during interval II. Therefore, after T_{II} has passed and the rectifier no-load voltage has changed to zero, the final conduction interval III is maintained until the current reaches zero. The total voltage-time-product applied to the leakage inductance between two current zero crossings is zero, i.e. the voltage-time-products of rectifier voltage and rectifier no-load voltage during the three conduction intervals have to be equal, i.e.

$$nU_{\mathrm{i}} T_{\mathrm{I}} + \frac{nU_{\mathrm{i}}}{2} T_{\mathrm{II}} = U_{\mathrm{o}}(T_{\mathrm{I}} + T_{\mathrm{II}} + T_{\mathrm{III}}) \Rightarrow T_{\mathrm{III}}. \tag{A.3}$$

This expression yields the duration of the third conduction interval when the current decreases to zero for

$$T_{\mathrm{III}} = \left(\frac{nU_{\mathrm{i}}}{2U_{\mathrm{o}}} d - \frac{1}{4}\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,III}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \tag{A.4}$$

Using expressions (A.1)-(A.4), the total charge Q_{r} transferred to the output during one half-cycle (Fig. 4.12a) is calculated which, multiplied by twice the switching frequency, finally leads to the average current transferred to the output in DCM1,

$$I_{\mathrm{o,dcm1}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}} \left(\left(\frac{nU_{\mathrm{i}}}{4U_{\mathrm{o}}} - \frac{1}{2} \right) d^2 + \frac{d}{4} - \frac{1}{16} \right). \tag{A.5}$$

For the derivation of the output current in DCM1 it is assumed that the rectifier current does not reach zero during interval 2. However, reducing the duty cycle in DCM1 also reduces the duration T_{III}, until interval 3 vanishes. With the assumed output voltage range, requiring that the rectifier current rises only when the full-level rectifier no-load voltage applies, and by requiring $T_{\mathrm{III}} > 0$, the conditions for DCM1,

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} < d < \frac{1}{2} \quad \text{and} \quad \frac{nU_{\mathrm{i}}}{2} < U_{\mathrm{o}} < nU_{\mathrm{i}}, \tag{A.6}$$

are obtained.

A.1.2 Discontinuous Conduction Mode 2

If the duty cycle at high output voltage ($U_{\mathrm{o}} > \frac{nU_{\mathrm{i}}}{2}$) is reduced below the minimum value for DCM1 the positive rectifier current half-cycle reaches zero already before the second no-load rectifier voltage falling edge. The rectifier-side waveforms for this situation, DCM2, are shown in Fig. 4.12b for working point B of Fig. 4.14. As in DCM1, the positive rectifier current half-cycle begins with the last no-load rectifier voltage rising edge. During the first conduction interval the rectifier current rises for

$$T_{\mathrm{I}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{A.7}$$

After the first rectifier no-load voltage falling edge the current decreases until it reaches zero. The duration of this second conduction interval is obtained by setting the voltage-time-products of rectifier no-load voltage and rectifier voltage during the two conduction intervals equal, i.e.

$$nU_{\mathrm{i}}T_{\mathrm{I}} + \frac{nU_{\mathrm{i}}}{2}T_{\mathrm{II}} = U_{\mathrm{o}}(T_{\mathrm{I}} + T_{\mathrm{II}}) \Rightarrow T_{\mathrm{II}}, \tag{A.8}$$

yielding the duration of conduction interval II,

$$T_{\mathrm{II}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2U_{\mathrm{o}} - nU_{\mathrm{i}}} \left(2d - \frac{1}{2}\right) T_{\mathrm{s}}. \tag{A.9}$$

With expressions (A.7) and (A.9) the average current transferred to the output in DCM2,

$$I_{\mathrm{o,dcm2}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}} \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2U_{\mathrm{o}} - nU_{\mathrm{i}}} \left(d - \frac{1}{4}\right)^2, \tag{A.10}$$

is obtained. Reducing the duty cycle to values less than $\frac{1}{4}$ while $U_{\mathrm{o}} > \frac{n}{2}U_{\mathrm{i}}$ results in a no-load rectifier voltage waveform not reaching the full-level (compare Fig. 4.9). Therefore, no interval is left with the rectifier current increasing and thus no power is transferred to the output. The conditions for DCM2 are consequently specified as

$$\frac{1}{4} < d < \frac{U_\mathrm{o}}{2nU_\mathrm{i}} \quad \text{and} \quad \frac{nU_\mathrm{i}}{2} < U_\mathrm{o} < nU_\mathrm{i}. \tag{A.11}$$

A.1.3 Discontinuous Conduction Mode 3

With low values of both output voltage and duty cycle as in operating point C in Fig. 4.14, DCM3 occurs. The characteristic waveforms for operating point C are shown in Fig. 4.12c. The rectifier no-load voltage consists of two pulses with same width and same polarity followed by two pulses of opposite polarity. Since the durations of all pulses are the same and also the durations of all four zero intervals of the rectifier no-load voltage are equal; assuming that the current is discontinuous means that there are four symmetric rectifier current pulses separated by four current zero intervals. One such triangular current pulse is described by

$$T_\mathrm{I} = dT_\mathrm{s} \quad \text{and} \quad \Delta i_\mathrm{r} = \frac{nU_\mathrm{i} - 2U_\mathrm{o}}{4L_{\sigma\mathrm{s,tot}}} T_\mathrm{I}. \tag{A.12}$$

Requiring equal voltage-time-products of rectifier voltage and rectifier no-load voltage during the current pulse,

$$\frac{nU_\mathrm{i}}{2} T_\mathrm{I} = U_\mathrm{o}(T_\mathrm{I} + T_\mathrm{II}) \Rightarrow T_\mathrm{II}, \tag{A.13}$$

yields the duration of the current decrease during interval II,

$$T_\mathrm{II} = \left(\frac{nU_\mathrm{i}}{2U_\mathrm{o}} - 1\right) dT_\mathrm{s}. \tag{A.14}$$

Multiplying four times the charge transferred during one such pulse to the output with the switching frequency leads to the average current transferred to the output in DCM3,

$$I_\mathrm{o,dcm3} = \frac{nU_\mathrm{i}}{2f_\mathrm{s}L_{\sigma\mathrm{s,tot}}} \left(\frac{nU_\mathrm{i}}{2U_\mathrm{o}} - 1\right) d^2. \tag{A.15}$$

Two conditions have to be fulfilled for DCM3 to occur. First, for the considered shape of the rectifier no-load voltage, the output voltage must be lower than half the input voltage reflected to the secondary side. Second, the duty cycle must be small enough such that the current is actually decreasing to zero during the rectifier no-load voltage zero interval, i.e. $T_\mathrm{I} + T_\mathrm{II} < \frac{T_\mathrm{s}}{4}$. Therefore, the conditions for DCM3 are

$$0 < d < \frac{U_\mathrm{o}}{2nU_\mathrm{i}} \quad \text{and} \quad 0 < U_\mathrm{o} < \frac{nU_\mathrm{i}}{2}. \tag{A.16}$$

A.2 Continuous Conduction Modes

A.2.1 Continuous Conduction Mode 1

A high duty cycle value together with low output voltage as in working point D indicated in Fig. 4.14 results in continuous current conduction, i.e. CCM. The waveforms of rectifier side voltages and current for this working point are shown in Fig. 4.13a. The positive current half-cycle consists of two intervals with rising current (T_I, T_II) followed by three intervals with falling current (T_III, T_IV, T_V). While the durations of intervals T_II, T_III, T_IV are defined by the inverter duty cycle, the durations of the first and the last interval are determined by the current zero crossings. The voltage-time-products of rectifier no-load voltage and rectifier voltage between two current zero crossings have to be equal. Assuming that the rising edge current zero crossing is located between the last rectifier no-load voltage rising edge and the first rectifier no-load voltage falling edge this condition can be expressed as

$$nU_\mathrm{i}\left(T_\mathrm{I} - \left(d - \frac{1}{4}\right)\frac{T_\mathrm{s}}{2}\right) = U_\mathrm{o}\frac{T_\mathrm{s}}{2} \Rightarrow T_\mathrm{I}, \tag{A.17}$$

yielding T_I. During interval I the full rectifier no-load voltage level is applied and the resulting rectifier current increase is described by

$$\Delta i_\mathrm{i,I} = \frac{nU_\mathrm{i} - U_\mathrm{o}}{2L_{\sigma\mathrm{s,tot}}}T_\mathrm{I}, \quad T_\mathrm{I} = \left(\frac{d - \frac{1}{4}}{2} + \frac{U_\mathrm{o}}{4nU_\mathrm{i}}\right)T_\mathrm{s}. \tag{A.18}$$

The following interval durations are all directly derived from the inverter duty cycle (compare Fig. 4.9). For interval II only half of the maximum level of the rectifier no-load voltage applies, thus the rectifier current rises slower described by

$$\Delta i_\mathrm{r,II} = \frac{nU_\mathrm{i} - 2U_\mathrm{o}}{4L_{\sigma\mathrm{s,tot}}}T_\mathrm{II}, \quad T_\mathrm{II} = \left(\frac{1}{2} - d\right)T_\mathrm{s}. \tag{A.19}$$

During the third interval the rectifier no-load voltage is zero and the rectifier current is thus changing during

$$T_{\mathrm{III}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,III}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \tag{A.20}$$

During the fourth interval the rectifier current decreases faster with the rectifier no-load voltage now taking its half negative level.

$$\Delta i_{\mathrm{r,IV}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{IV}}, \quad T_{\mathrm{IV}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}} \tag{A.21}$$

Finally, during interval V the negative full-level of the rectifier no-load voltage drives the rectifier current back to zero for

$$T_{\mathrm{V}} = \left(\frac{d - \frac{1}{4}}{2} - \frac{U_{\mathrm{o}}}{4nU_{\mathrm{i}}}\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}}. \tag{A.22}$$

Using (A.18)-(A.22) the charge transferred to the output during one current half-cycle is calculated. Multiplied with twice the switching frequency, the average current transferred to the output in CCM1,

$$I_{\mathrm{o,ccm1}} = \frac{nU_{\mathrm{i}}}{4f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}} \left(d - d^2 - \frac{1}{16} - \left(\frac{U_{\mathrm{o}}}{2U_{\mathrm{i}}}\right)^2\right), \tag{A.23}$$

is obtained. By reducing the duty cycle in CCM1, according to (A.22), the duration of interval V is also reduced, until the current zero crossings coincide with the last rising and falling edges of the rectifier no-load voltage. For lower values of duty cycle, the assumption of the positive slope current zero crossing being located between the last rising and first falling edge of the rectifier no-load voltage is no longer true. Setting $T_{\mathrm{V}} > 0$ yields the minimum duty cycle for CCM1, which reaches the maximum possible value of $d = 0.5$ at $U_{\mathrm{o}} = \frac{nU_{\mathrm{i}}}{2}$. Therefore, also the maximum output voltage for CCM1 results from $T_{\mathrm{V}} > 0$ and the conditions for CCM1 can be summarized as

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} + \frac{1}{4} < d < \frac{1}{2} \quad \text{and} \quad 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{A.24}$$

A.2.2 Continuous Conduction Mode 2

Reducing the duty cycle to values lower than the minimum for CCM1 (A.24) results in rectifier voltage and current waveforms as shown in

Fig. 4.13b simulated for working point E in Fig. 4.14. In this CCM2 the rectifier no-load voltage, same as in DCM1, utilizes all five levels, i.e. $d > 0.25$, but the positive slope current zero crossing is located between the third and the fourth (last) rectifier no-load voltage rising edge. Each current half-cycle can be partitioned into five conduction intervals. The beginning of the first interval, i.e. the time of the positive slope current zero crossing, is located such that the voltage-time-product of the rectifier no-load voltage equals the voltage-time-product of the rectifier voltage during the positive rectifier current half-cycle, i.e.

$$(T_\mathrm{I} + T_\mathrm{II}) n U_\mathrm{i} = U_\mathrm{o} \frac{T_\mathrm{s}}{2} \Rightarrow T_\mathrm{I}, \tag{A.25}$$

which yields the duration T_I of the first interval. During that time the rectifier no-load voltage is at its half-level and the rectifier current is described by

$$\Delta i_{\mathrm{r,I}} = \frac{nU_\mathrm{i} - 2U_\mathrm{o}}{4L_{\sigma\mathrm{s,tot}}} T_\mathrm{I}, \quad T_\mathrm{I} = \left(\frac{1}{4} + \frac{U_\mathrm{o}}{2U_\mathrm{i}} - d \right) T_\mathrm{s}. \tag{A.26}$$

The duration of the following intervals is determined solely by the edges of the rectifier no-load voltage, i.e. by the inverter duty cycle. During interval II, the full-level of the rectifier no-load voltage applies and the rectifier current rises during

$$T_\mathrm{II} = \left(d - \frac{1}{4} \right) T_\mathrm{s} \quad \text{by} \quad \Delta i_{\mathrm{r,II}} = \frac{nU_\mathrm{i} - U_\mathrm{o}}{2L_{\sigma\mathrm{s,tot}}} T_\mathrm{II}. \tag{A.27}$$

During interval III, the rectifier current continues to rise but the rectifier no-load voltage is back at its half-level. The interval is thus described by

$$T_\mathrm{III} = \left(\frac{1}{2} - d \right) T_\mathrm{s}, \quad \Delta i_{\mathrm{r,III}} = \frac{nU_\mathrm{i} - 2U_\mathrm{o}}{4L_{\sigma\mathrm{s,tot}}} T_\mathrm{III}. \tag{A.28}$$

During interval IV the rectifier no-load voltage is zero and the rectifier current decreases for

$$T_\mathrm{IV} = \left(d - \frac{1}{4} \right) T_\mathrm{s} \quad \text{by} \quad \Delta i_{\mathrm{r,IV}} = -\frac{U_\mathrm{o}}{2L_{\sigma\mathrm{s,tot}}} T_\mathrm{IV}. \tag{A.29}$$

Finally, during interval V the negative half-level of the rectifier no-load voltage applies and the current decreases to zero,

$$T_\mathrm{V} = \left(\frac{1}{4} - \frac{U_\mathrm{o}}{2nU_\mathrm{i}} \right) T_\mathrm{s}, \quad \Delta i_{\mathrm{r,V}} = \frac{-nU_\mathrm{i} - 2U_\mathrm{o}}{4L_{\sigma\mathrm{s,tot}}} T_\mathrm{V}. \tag{A.30}$$

Combining (A.26)-(A.30) allows to calculate the charge transferred to the output during one rectifier current half-cycle, multiplied with twice the switching frequency yielding the average current transferred to the output in CCM2,

$$I_{\mathrm{o,ccm2}} = \frac{nU_{\mathrm{i}}}{8f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}}\left(d - \left(\frac{U_{\mathrm{o}}}{nU_{\mathrm{i}}}\right)^2\right). \tag{A.31}$$

The region of CCM2 is limited by three conditions. First, (A.30) shows that with increasing output voltage the duration of interval V decreases until it reaches zero at $U_{\mathrm{o}} = \frac{nU_{\mathrm{i}}}{2}$. This limit marks the boundary to DCM1. Second, for the rectifier no-load voltage to utilize all five levels it is required (compare Fig. 4.9) that $d_{\mathrm{ccm2}} > \frac{1}{4}$. Finally, with increasing duty cycle the duration of interval I (A.26) approaches zero. Requiring $T_{\mathrm{I}} > 0$ places an upper bound on the duty cycle identical with the minimum duty cycle for CCM1 (A.24). The conditions for CCM2 are summarized as

$$\frac{1}{4} < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} + \frac{1}{4} \quad \text{and} \quad 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{A.32}$$

A.2.3 Continuous Conduction Mode 3

With duty cycle and output voltage as in working point F in Fig. 4.14, CCM3 is entered. The corresponding waveforms of rectifier side current and voltages are shown in Fig. 4.13c. The rectifier no-load voltage, as in DCM3, consists of two half-level voltage pulses with same polarity followed by two pulses of opposite polarity. As in CCM1 and CCM2 five conduction intervals are identified for one rectifier current half-cycle. The first interval starts with the positive slope current zero crossing, located between rising and falling edge of the first positive rectifier no-load voltage pulse, and ends with the falling edge of the first rectifier no-load voltage pulse. The duration of the first interval is determined by the condition of equal voltage-time-products of rectifier-no-load voltage and rectifier voltage between two rectifier current zero crossings, i.e.

$$T_{\mathrm{I}} nU_{\mathrm{i}} = U_{\mathrm{o}}\frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}. \tag{A.33}$$

During the first interval the positive half-level of the rectifier no-load voltage applies and the rectifier current changes during

$$T_{\mathrm{I}} = \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}}T_{\mathrm{I}}. \tag{A.34}$$

During the zero interval between the two positive pulses of the rectifier no-load voltage, interval II, the rectifier current decreases for

$$T_{\mathrm{II}} = \left(\frac{1}{4} - d\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,II}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \tag{A.35}$$

During the following interval III, the current rises at the same rate as in interval I for

$$T_{\mathrm{III}} = dT_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,III}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \tag{A.36}$$

The duration and the rectifier current change rate of interval IV are identical as in interval II, i.e.

$$T_{\mathrm{IV}} = T_{\mathrm{II}}, \quad \Delta i_{\mathrm{r,IV}} = \Delta i_{\mathrm{r,II}}. \tag{A.37}$$

During interval V the rectifier current decreases, while the negative half-level of the rectifier no-load voltage applies, for

$$T_{\mathrm{V}} = \left(d - \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right) T_{\mathrm{s}} \quad \text{by} \quad \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}} \tag{A.38}$$

until it reaches zero. Using expressions (A.34)-(A.38) the charge transferred to the output during one positive current half-cycle is calculated and multiplied with twice the switching frequency to obtain the average current transferred to the output in CCM3,

$$I_{\mathrm{o,ccm3}} = \frac{nU_{\mathrm{i}}}{8f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}} \left(d - \left(\frac{U_{\mathrm{o}}}{nU_{\mathrm{i}}}\right)^2\right). \tag{A.39}$$

Surprisingly, identical expressions for the output current in CCM2 (A.31) and CCM3 are obtained. Therefore, the boundary, $d = 0.25$, between CCM2 and CCM3 could also be discarded. However, additionally a second condition limits the region of CCM3, since reducing the duty cycle also reduces the duration of interval V (A.38) until it vanishes completely. If the duty cycle is reduced further the current reaches zero before the first negative pulse of the rectifier no-load voltage begins and DCM3 is entered (compare Fig. 4.12c). Therefore, setting $T_{\mathrm{V}} > 0$ yields the minimum duty cycle for operation in the region of CCM3, which coincides with the maximum duty cycle for operation in DCM3. Therefore, the conditions for CCM3 can be summarized as

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} < d < \frac{1}{4} \quad \text{and} \quad 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{A.40}$$

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