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Hybrid Amplifiers for AC Power Source Applications

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Abstract

AC test sources are essential equipments for testing electric systems which are connected to ac mains. These ac test sources are required to have low output impedance, clean output voltage and highly dynamic behavior. Presently LPAs are mainly employed in ac test sources because of their high fidelity and excellent dynamic behaviour. However, these LPAs have very high losses in their output stages, which make the systems bulky and expensive. Therefore, there are growing research interests in realizing high efficiency and high bandwidth ac test sources by combining linear power amplifiers and switch-mode converters, which results in the reduction of the system losses while keeping the high dynamic performance of the LPAs. The main objective of this work is to develop novel highly dynamic hybrid power amplifiers with high efficiency for ac power source applications.

Firstly in Chapter 1, a short description of the motivation for this work is given. Then a number of hybrid power amplifiers presented in the recent literature are collected and categorised to three types according to their configurations.

Chapter 2 presents the first hybrid power amplifier (Type I), which employs a 3-level buck-boost converter with adjustable output voltages for generating the supply voltages of a linear power amplifier. The idea is to reduce the voltage drop across the LPA power transistors. The losses calculation, sys-

tem dimensioning and the control design are treated in detail. A 1 kW laboratory prototype specified for aircraft ac voltage application is then built to verify the analysis.

Chapter 3 introduces the second hybrid power amplifier that belongs to Type II. It is a so called Hybrid Multi-Cell Amplifier (H-MCA) which connects a high slew rate LPA and a multi-cell inverter in series. The multi-cell inverter outputs the large-scale voltage and the LPA only generates a small correction voltage. Therefore the losses of LPA are limited to a minimum level for high voltage applications. The system modulation, analytical system losses calculation, and control design are described. In addition, an isolated bi-directional multi-output resonant dc-dc converter with open-loop control is presented to provide the dc supplies for all the inverter cell units as well as for the LPA.

In recent years, the switch-mode amplifiers, characterised by high efficiency, have attracted many research interests in various applications. Therefore, it is certainly interesting to compare the performance of the switch-mode amplifiers with the hybrid power amplifier for ac power source applications. In Chapter 4, two pure switch-mode amplifiers, AM + PWM Multi-Cell Amplifier (AP-MCA) and PWM Multi-Cell Amplifier (P-MCA), are analyzed and designed.

Chapter 5 presents a universal laboratory prototype with a compact and symmetric design. This prototype is able to perform three topologies: H-MCA, AP-MCA, and P-MCA, by proper selection of jumpers and different digital control coding. The system performances of these three topologies measured from this prototype are compared.

Finally the work done is summarized in Chapter 6 and an outlook is given for further developments.

Kurzfassung

Wechselspannungsquellen sind für das Testen von netzbetriebenen elektronischen Geräten essentiell. Diese Spannungsquellen müssen eine niedrige Ausgangsimpedanz und eine hochdynamisch geregelte Ausgangsspannung aufweisen. Momentan werden hierfür hauptsächlich lineare Leistungsverstärker (linear power amplifier, LPA) aufgrund ihrer hohen Zuverlässigkeit und ausgezeichneten Dynamik eingesetzt. Andererseits treten in den Ausgangsstufen dieser Verstärkerschaltungen sehr hohe Verluste auf, was ein grosses Bauvolumen und hohe Kosten mit sich bringt. Daher werden nun zunehmend Konzepte für Wechselspannungsquellen mit hohem Wirkungsgrad und hoher Bandbreite untersucht, die aus einer Kombination von Linearverstärkern mit getakteten Konvertern (switch-mode converter) entstehen. Damit sollen die Verluste unter Beibehaltung der hohen dynamischen Performance des Linearverstärkers deutlich reduziert werden. Das Ziel der vorliegenden Arbeit ist daher die Untersuchung und Entwicklung eines neuartigen hybriden Leistungsverstärkers mit hoher Dynamik und hohem Wirkungsgrad für die Anwendung als Wechselspannungsquelle.

Zunächst wird im 1. Kapitel die Motivation für diese Arbeit kurz erläutert. Anschliessend werden aus der Literatur bekannte Topologien für Leistungsverstärker präsentiert und in drei Gruppen kategorisiert.

In Kapitel 2 wird Typ I des hybriden Leistungsverstärkers näher vorgestellt, der einen 3-Level-Tief-Hochsetzsteller mit regelbarer Ausgangsspannung zur Erzeugung der Versorgungsspannung des nachfolgenden Linearverstärkers benutzt. Die Idee hierbei ist, durch entsprechende Vorgabe der Versorgungsspannung den Spannungsabfall über den Leistungstransistoren des Linearverstärkers zu reduzieren. Die Verlustberechnung, die Auslegung des Systems sowie die regelungstechnische Analyse und Auslegung werden hier im Detail behandelt. Zur Verifikation der theoretischen Analyse wird abschliessend ein 1 kW Labor-Testsystem entwickelt und aufgebaut.

In Kapitel 3 wird Typ II des hybriden Leistungsverstärkers vorgestellt, der sogenannte Hybrid Multi-Cell Amplifier (H-MCA). Bei dieser Topologie wird ein linearer Leistungsverstärker mit hoher Flankensteilheit mit einem Mehrzellen-Wechselrichter in Serie geschaltet. Der Mehrzellen-Wechselrichter gibt dabei das Grosssignal an den Ausgang, während der lineare Verstärker lediglich eine Korrekturspannung ausgibt. Somit können die Verluste auch für Hochspannungsanwendungen minimiert werden. In diesem Kapitel werden die Ansteuerung des Systems, die Herleitung der Verluste sowie die regelungstechnische Auslegung detailliert beschrieben. Weiters wird ein bidirektionaler Resonanz-Gleichspannungs-Konverter mit Potenzialtrennung und mehreren Ausgängen beschrieben, der im unregelt betrieben wird. Dieser Konverter dient zur Versorgung der Wechselrichterzellen und des Linearverstärkers mit den benötigten Gleichspannungen.

Da im Verlauf der letzten Jahre auch reine Schaltverstärker (switch-mode amplifiers) aufgrund ihres hohen Wirkungsgrades zunehmend Forschungsinteresse geweckt haben, werden in dieser Arbeit auch diese untersucht und mit den hybriden Topologien verglichen. Daher werden in Kapitel 4 zwei interessante Topologien analysiert und dimensioniert: AM + PWM Multi-Cell Amplifier (AP-MCA) und PWM Multi-Cell Amplifier (P-MCA).

Kapitel 5 beschreibt schliesslich einen universellen Testaufbau mit einem sehr kompakten Design, der es erlaubt drei verschiedene Topologien nur

durch Setzen von Drahtbrücken und Verwendung passender Regelungssoftware zu implementieren: H-MCA, AP-MCA, and P-MCA. Die Performance der drei Systeme wird messtechnisch ermittelt und verglichen.

Abschliessend werden in Kapitel 6 die wesentlichen Erkenntnisse dieser Arbeit zusammengefasst und ein Ausblick auf weitere Forschungen in diesem Bereich gegeben.

List of Symbols

C_i	capacitors, $i \in N$
C_{Fi}	filter capacitors, $i \in N$
C_{gs}	gate-to-source capacitance
C_{gd}	gate-to-drain capacitance
C_{dom}	dominated capacitor in LPA model
C_r	lumped capacitance in the resonant loop
D_i	power diodes, $i \in N$
f_o	output frequency
f_n	natural resonant frequency
f_s	switching frequency
f_{sw}	switching frequency for switching losses calculation
f_{bk}	switching frequency of buck stage transistor
f_{bt}	switching frequency of boost stage transistor
f_{sm}	switching frequency of inverter cell in P-MCA
f_{spwm}	switching frequency of the PWM inverter cell in AP-MCA
F_M	triangular carrier amplitude
g_m	MOSFET transconductance
i_L	instantaneous inductor current
I_L	constant inductor current

I_{RM}	diode reverse recovery peak current
I_{sw}	switching current
i_o	instantaneous output current
I_{op}	output peak current
k_{tt}	switching losses coefficient
L_i	inductors, $i \in N$
L_{Fi}	filter inductors, $i \in N$
L_r	lumped inductance in the resonant loop
K_{FB}	inductor current feedback coefficient
K_{FF}	feed-forward coefficient
Q_{rr}	diode reverse recovery charge
P_{in}	input power
P_{lpa}	losses of output transistors in LPA
P_o	output power of the linear amplifier
r_o	MOSFET output impedance
R_i	resistors, $i \in N$
R_{di}	filter damping resistors, $i \in N$
R_s	MOSFET source resistance
R_o	output resistance
R_r	lumped resistance in the resonant loop
R_L	load resistance
$R_{s,u}$	shunt resistor presenting the switching losses
$R_{s,i}$	series resistor presenting the switching losses
S^*	normalization basis for the power
T_{on}	switch on time
T_{off}	switch off time
u_{C+}	upper boost capacitor voltage of tracking power supply
u_{C-}	lower boost capacitor voltage of tracking power supply
u_{p+}	positive supply voltage for LPA
u_{p-}	negative supply voltage for LPA

u_o	instantaneous output voltage
u_{mo}	multi-cell inverter output voltage
u_{lo}	linear power amplifier output voltage
u_{g1}	gate voltages (1)
u_{g2}	gate voltages (2)
u_{vas}	driver signal generated by PA97
U_{op}	output peak voltage
U_{ds}	drain-to-source voltage
U_{sw}	switching voltage
U_z	dc supply voltage for each inverter cell
U_a	LPA dc supply voltage generated by dc-dc converter
U_L	low voltage level of gate voltage
U_H	high voltage level of gate voltage
U_M	gate miller voltage
U_{th}	gate threshold voltage
V_{CC}	constant supply voltage for conventional LPAs
V_a	voltage remaining across a conducting power transistor
V_b	width of the hysteresis band
Z_L	magnitude of the load impedance
$Z_G(s)$	impedance of the drive stage
$Z_{pa}(s)$	output impedance of the PA97 with the designed negative feedback
$Z_o(s)$	system output impedance
α	ratio between inductor constant current I_L and LPA output current I_{op}
φ	phase angle of the load current
η	efficiency
τ_{zi}	time constant of a zero in control systems, $i \in N$
τ_{pi}	time constant of a pole in control systems, $i \in N$
 Index	
avg	average value

<i>bk</i>	buck stage
<i>bt</i>	boost stage
<i>cls</i>	closed-loop
<i>con</i>	conduction
<i>lin</i>	linear
<i>max</i>	maximum value
<i>on</i>	“on” state of a switch
<i>off</i>	“off” state of a switch
<i>open</i>	open-loop
<i>rms</i>	root mean square value
<i>sim</i>	simulated
<i>smp</i>	sample
<i>sw</i>	switched
<i>tot</i>	total

Other designations

x^*	reference value of a control signal x
\tilde{x}	small signal variation of a state variable x

Abbreviation

AM	Amplitude Modulation
DSP	Digital Signal Processing
ESR	Equivalent Series Resistance
AP-MCA	AM + PWM Multi-Cell Amplifier
H-MCA	Hybrid Multi-Cell Amplifier
P-MCA	PWM Multi-Cell Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCT	Pseudo Continuous Time
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation

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THD Total Harmonic Distortion

ZOH Zero Order Hold

Chapter 1.

Introduction

AC test sources are essential equipments for testing electric systems which are connected to ac mains. These ac test sources are required to have low output impedance, clean output voltage and highly dynamic behaviour so that they are able to simulate different mains conditions in order to perform different tests for the electric systems. Some typical standardized EMC emissions & immunity tests are: limits for harmonic current emissions (IEC 61000-3-2), limitation of voltage fluctuations and flicker (IEC 61000-3-3), voltage variations immunity (IEC 61000-4-11), harmonics and inter-harmonics immunity (IEC 61000-4-13), voltage fluctuations immunity (IEC 61000-4-14), and variation of power frequency immunity (IEC 61000-4-28) etc.

Presently linear power amplifiers are mainly employed in ac test sources because of their high fidelity and excellent dynamic behaviour. However, these linear power amplifiers have very high losses in their output stages, which make the systems bulky and expensive due to the large heatsinks that are required. For example, an ac power source PA1000 from Spitzenberger has an output power rating of 1 kVA, but weights 45 kg [1]. In recent years switch-mode power amplifiers, mainly class-D and class-E amplifiers, have replaced linear power amplifiers in various applications where high fidelity

is not required. The main reason for their use is that they have a much higher efficiency, which results in a compact and low cost design realization. However, switch-mode power amplifiers produce additional EMI and a suitable low pass filter is necessary between amplifier and load. This results in two disadvantages, firstly the system bandwidth is limited by the low pass filter, and secondly the output impedance of the amplifier is significantly increased at the natural frequency of the low pass filter.

Therefore, there are growing research interests in realizing high efficiency and high bandwidth ac power sources by combining linear power amplifiers (LPA) and switch-mode converters which results in the reduction of the system losses while keeping the high dynamic performance of the linear power amplifiers.

Since the power losses of LPA are determined by the voltage drop across the power transistors and the current flowing through the power transistors, there are only two approaches to lower the power losses, i.e. decreasing the voltage drop across the power transistors or reducing the transistors currents. All the hybrid topologies are based on these two considerations. The author of [2] classifies the composite amplifiers in four groups: series voltage, parallel voltage output, parallel current and series current output. However this classification does not include another hybrid topology which employs a tracking power supply (TPS) to adjust the supply voltages according to the required linear amplifier output voltage. This topology can significantly reduce the voltage drop across the linear amplifier power transistors, which results in a reduction of the amplifier power losses. Furthermore, voltage sources are typically required for ac power source applications as well as other industrial applications like stage acoustic amplifiers, etc.

Based on the aforementioned considerations, the voltage source hybrid power amplifiers are classified to three types as shown in Figure 1.1. In the following contents, we are to discuss the details of each type hybrid power amplifier and sort the hybrid power amplifiers from the collected literature into these three categories.

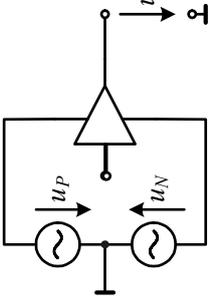
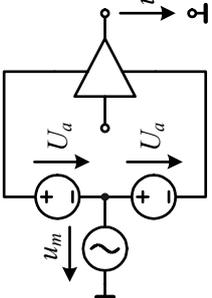
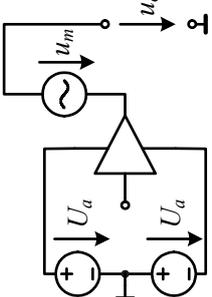
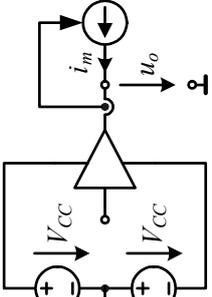
<p>Type I</p> <p>Envelope Configuration</p>	<p>Type II</p> <p>Series Configuration</p>	<p>Type II</p> <p>Series Configuration</p>	<p>Type III</p> <p>Parallel Configuration</p>
			
<p>Reduce voltage drops across LPA power transistors</p>	<p>Reduce voltage drops across LPA power transistors</p>		<p>Reduce output current of LPA power transistors</p>

Figure 1.1: Classification of hybrid power amplifiers.

Type I: Envelope Configuration [2]-[15]

In contrast to the conventional class-AB amplifiers that are usually supplied by constant dc supplies, for this type of hybrid amplifiers these constant dc supplies are replaced by switch-mode power supplies that are able to vary their output voltages according to the instantaneous LPA output voltages. Therefore LPA power losses are dramatically reduced because the voltage drop across LPA power transistors is kept to a minimum level. The representative key waveforms of this approach are demonstrated in Figure 2.1. However the disadvantage of this configuration is that the linear power amplifier should deliver the full output power and sustain the full output voltage stress. This makes it difficult to design the linear power amplifier for high voltage applications.

There are two types of converters that are used for TPSs in the literature, buck-type and boost-type. In [4], two buck converters, which have series connected their output voltages, are proposed for achieving a variable amplifier supply voltage. And this buck-type TPS is widely employed in RF power amplifier applications [8]-[14]. A buck-type TPS with an isolated push-pull boost converter is proposed in [5]. Multiphase buck converters have been employed as TPS for RF power amplifiers [14]. A boost dc-dc converter with a switching frequency of 10 MHz is presented for Code Division Multiple Access (CDMA) applications. In [13], a buck-boost type converter is proposed to adaptively supply the PA in CDMA application in order to increase the battery life.

Type II: Series Configuration [2], [16]-[18]

In this type of topology, a main ac voltage source that delivers the bulk of the output voltage is connected in series with a LPA that only outputs the small amount of a correction voltage that supplements the voltage difference between output voltage u_o and main voltage u_m . Therefore, LPAs with low voltage supplies can be employed in high voltage applications, which significantly reduces the voltage drop across LPA power transistors. There are two possibilities to connect these two parts. One possibility is to connect the main ac voltage source to the ground of the LPA dc power supplies [16],

[17], and the other is to connect it with the LPA output voltage in series [2], [18].

In the earlier days, a hybrid configuration of LPAs was proposed [16], where the class-AB LPA that has higher efficiency served as the main ac voltage source and the class-A LPA that is characterised by better output voltage quality is employed as the correction voltage source. In [17], the class-AB LPA in the previous topology is replaced by a class-D amplifier that acts as the main ac voltage source. A “Quasi-Linear Amplifier” topology has been proposed in [18]. The “Quasi-Linear Amplifier” consists of low switching frequency inverters connected in series with a LPA to generate gradient coil currents with fast ramp time for magnetic resonance imaging (MRI) systems. Another transformer coupled series voltage output topology is proposed in [2], where the switch-mode amplifier is to provide the main output power and the transformer coupled LPA is used to remove the output ripple and higher frequency deficiencies of the main amplifier.

Type III: Parallel Configuration [19]-[27]

A LPA and a current controlled switch-mode amplifier are connected in parallel at the output. There the switch-mode amplifier contributes the main load current and the linear amplifier generates the difference current. With this topology a relatively small current is flowing through the linear power amplifier so that the losses can be significantly reduced and the output impedance is defined by the linear power amplifier stage. However, a high voltage linear power amplifier is still required for a mains simulation application and switching noise can appear in the output voltage due to the increased output impedance of linear power amplifiers at high frequencies. This type of topology is especially preferred for audio amplifier applications

Work Objectives

The main objective of this work is to develop novel highly dynamic hybrid power amplifiers of high efficiency for ac test source applications. Based on the ideas to combine linear and switch-mode technologies, two new topologies of hybrid power amplifiers are proposed and analyzed.

The first hybrid power amplifier, which belongs to Type I, employs a three-level buck-boost converter with adjustable output voltages for generating the supply voltages of a linear power amplifier. The supply voltages can then be modulated according to the required instantaneous linear power amplifier output voltage so that the voltage drop across the output power transistors can be significantly reduced; this results in a significant power loss reduction.

The second hybrid power amplifier, which belongs to Type II, is a so-called Hybrid Multi-Cell Amplifier (H-MCA) which comprises a high slew rate linear power amplifier and H-bridges cell units. The output of the linear amplifier and of the cell units are connected in series. A simple modulation is applied which determines how many cell units are switched into the output loop according to the instantaneous output voltage reference signal. There, a low voltage commercial linear power amplifier can be applied.

Both systems will be analyzed in detail and the performance, e.g. system losses and dynamics, will be compared to a conventional linear power amplifier. According to a typical specification, the components will be selected and a robust control will be designed for both systems. The final objective is to build compact laboratory prototypes to verify the theoretical analysis and to show the systems efficiency improvement over conventional ac test sources.

Besides these two hybrid systems, two other switch-mode amplifiers, AM + PWM Multi-Cell Amplifier (AP-MCA) and PWM Multi-Cell Amplifier (P-MCA), are analyzed and designed. The system performances of efficiency, power bandwidth, dynamic behavior, output voltage THD and output impedance measured from a universal laboratory prototype are compared with H-MCA.

Contributions

The main contributions of this work are briefly listed in the following.

1. A novel hybrid amplifier topology, which connects a buck-boost type envelope tracking converter in series with a linear power amplifier, is proposed, analysed and verified in a laboratory prototype.
2. Another novel hybrid amplifier topology, which combines a high slew rate linear power amplifier and H-bridges cell units followed by a dv/dt filter, is proposed, analysed and verified in a laboratory prototype.
3. A comparative study is performed on three different types of multi-level amplifier. A universal prototype, which can perform all these three multi-level amplifiers, is built and provides a fair basis for the performance comparison.

Most of these results have been published in IEEE transactions or conference proceedings as listed below.

- G. Gong, H. Ertl, and J. W. Kolar, "Novel power supply for linear power amplifiers," *IEEE Trans. on Industrial Electronics*, Vol. 55, pp. 684-698, Feb. 2008.
- G. Gong, H. Ertl, and J. W. Kolar, "A multi-cell cascaded power amplifier," in *Proc. 2006 Applied Power Electronics Conference*, pp. 1550-1556.
- G. Gong, S. Round, and J. W. Kolar, "Design, Control and Performance of Tracking Power Supply for a Linear Power Amplifier," in *Proc. 2005 Power Electronics Specialists Conference*, pp. 2841 – 2847.
- G. Gong, H. Ertl, and J. W. Kolar, "High-Frequency Isolated DC/DC Converter for Input Voltage Conditioning of a Linear Power Amplifier," in *Proc. 2003 IEEE Power Electronics Specialists Conference*, Vol. 4, pp. 1929 – 1934.

Chapter 2.

Novel Tracking Power Supply for Linear Power Amplifiers

2.1 Introduction

Conventional linear power amplifiers (LPAs), as schematically shown in Figure 2.1(a), are widely employed in industry because of their high output voltage quality and excellent *dynamic* behaviour. As shown in Figure 2.1(b) such amplifiers are usually supplied with constant voltages. The time behaviour of the current, voltage and instantaneous power of the output power transistor T_{p1} of a LPA is shown in Figure 2.1 (c) for class-AB operation. High losses occurring in the transistors result in a low efficiency, especially for supplying reactive loads. This constitutes a serious problem in particular for high power systems, which tend to be very bulky and expensive because of the large heat sinks required and the large power consumption. Consequently, there is a growing interest in increasing the efficiency of high power linear amplifier systems.

As described in the Introduction, a very efficient way to avoid the aforementioned drawbacks is conditioning the supply voltage, i.e. varying the supply voltages of the LPA by using a tracking power supply (TPS) that adjusts the supply voltages according to the required linear amplifier output voltage [2]-[15]. With this, the voltage drop across the linear amplifier power transistors could be reduced considerably resulting in a corresponding reduction of the amplifier power losses.

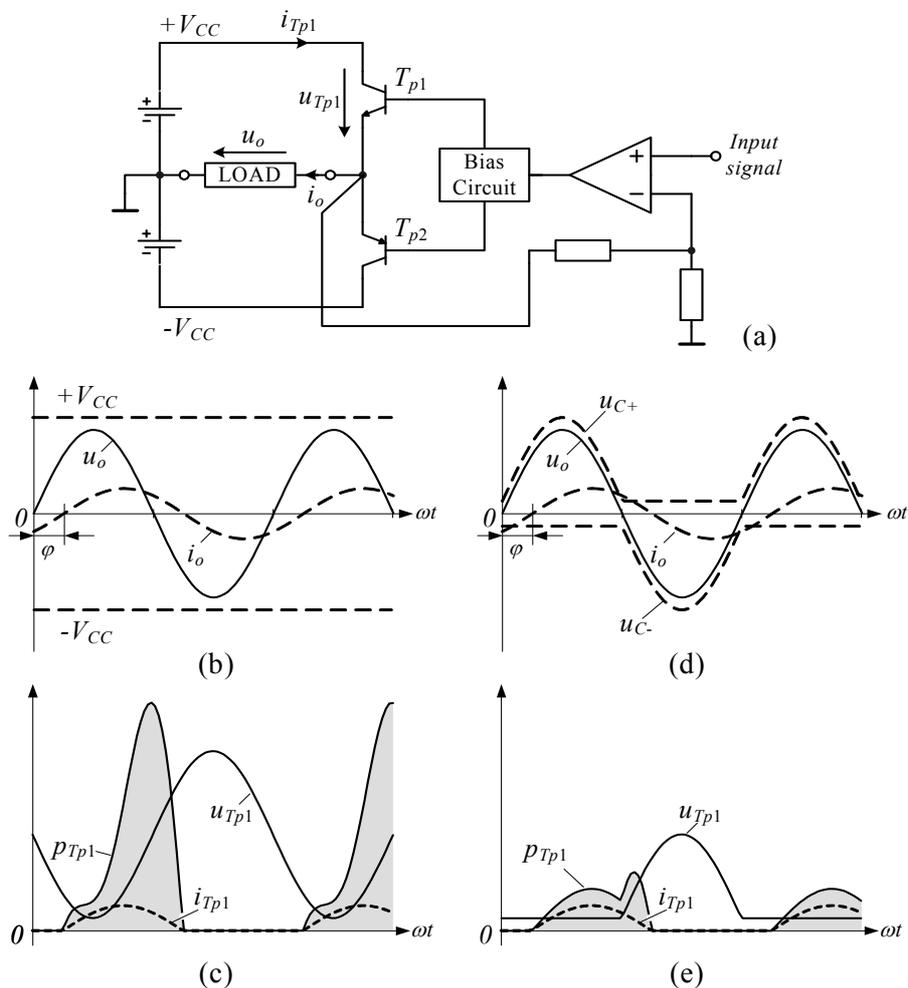


Figure 2.1: (a) Conventional LPA; (b) basic waveforms for constant supply voltage; (c) current, voltage and instantaneous power loss of transistor T_{p1} for constant supply voltage; (d) variation of the supply voltage according to the time behaviour of the voltage to be generated by the LPA; (e) current, voltage, and instantaneous power loss of transistor T_{p1} for conditioned supply voltage.

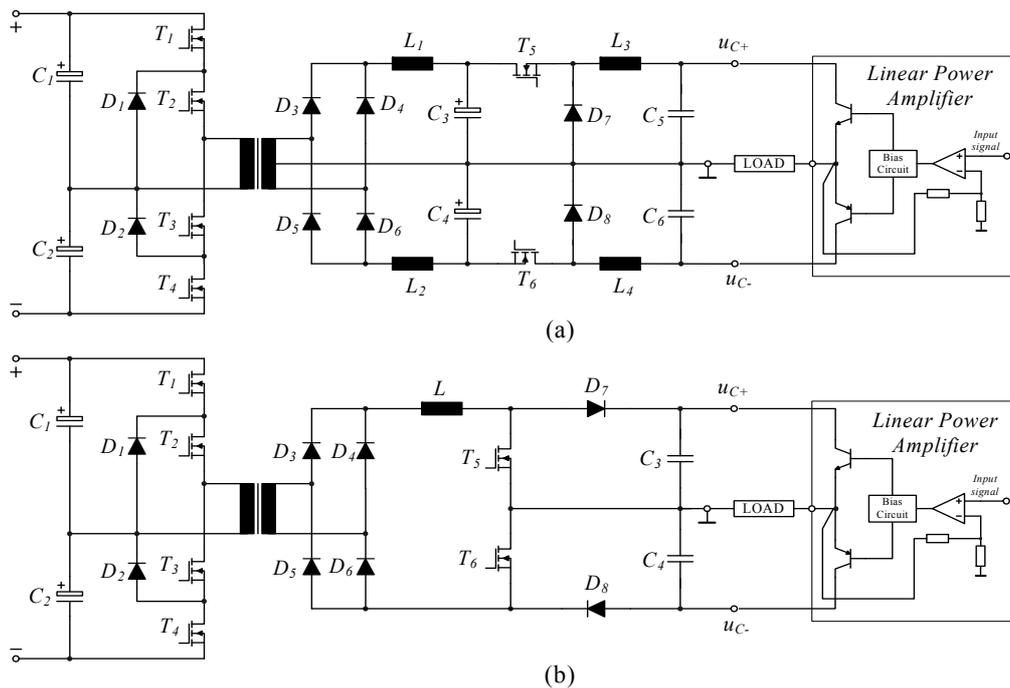


Figure 2.2: TPS topologies for a LPA; (a) conventional realization 0; (b) proposed system [30].

While the Type I hybrid topologies in [2]-[11] are all based on buck-type converters, in this chapter a new isolated boost-type TPS topology is proposed for controlling the supply voltage of a LPA according to Figure 2.1(d) [30]-[31].

In principle, a TPS as shown in Figure 2.2(a) could be employed for realizing a variable supply voltage according to Figure 2.1(d). There, the input stage is formed by a three-level dc-dc converter topology [32], which reduces the blocking voltage stress on the primary side power transistors as compared to a full-bridge topology. Therefore, the concept is especially advantageous for high input voltage applications. The system output stage is formed by two buck converters with series connected outputs. The control of the power amplifier supply voltages could be implemented with underlying current control. However, the system shows a high realization effort as a centre-tapped transformer, four inductors and four capacitors are employed on the secondary side. A further drawback is the limitation of the maximum rate of change of the output voltage by the output filter.

In this chapter a novel boost-type topology for realizing a TPS with comparably low effort is proposed and depicted in Figure 2.2(b). Only a single inductor and two capacitors are required on the secondary side, although in a practical implementation an additional high frequency output filter might be required. However, the size of this filter is much smaller than the output filter of the buck-type converter (Figure 2.2a) for the same LPA supply voltage ripple value. In this topology, a control loop is provided for impressing the secondary inductor current. Based on this, a tolerance band control of the supply voltages of the linear amplifier is performed by proper gating of the power transistors T_5 and T_6 , and an excellent dynamic behaviour of the voltage control is achieved.

There are different possible applications for this novel approach. Here we are aiming to use this system as a single-phase testing voltage source for aircraft equipment, the considerations will however be as far as possible in general terms. The power level is selected as 1kW, which is used for low power experimental systems. The system operation specifications are defined as

$$U_{o,rms} = 115 \text{ V} \pm 15\% \approx 98 \text{ V} \sim 132 \text{ V}$$

$$f_o = \text{DC} \sim 1 \text{ kHz}$$

$$I_{op,max} = 10 \text{ A}$$

where $U_{o,rms}$ is the RMS value of the output voltage, f_o is the output frequency and $I_{op,max}$ is the maximum output peak current. The output voltage range covers the abnormal single-phase voltage range, 97 V \sim 134V, of the 115 Vrms ac mains in aircraft according to DO-160D Change No.2. The specified output frequency is selected with respect to the widest abnormal mains frequency range, 360 Hz \sim 800 Hz, which is defined for testing A(WF) catalog equipment as well as referring to DO-160D Change No.2.

In the following analysis, firstly the LPA transistor losses will be compared in the case of different input voltage conditions in section 2. Then the key issues of the TPS design will be discussed in section 3. In section 4, the output filter will be designed to limit the switching noise of the output voltage.

Furthermore, a current loop design with feed-forward control based on the derived small signal model of the TPS will be treated in section 5. Finally, section 6 shows the simulation and experimental results.

2.2 LPA Transistor Losses for Different Input Voltage Conditions

For the following calculations we assume the output voltage of the LPA to be

$$u_o = U_{op} \sin \omega t . \quad (2.1)$$

Assuming a linear load, the resulting output (load) current is

$$i_o = \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) = I_{op} \sin(\omega t - \varphi). \quad (2.2)$$

where Z_L is the magnitude of the load impedance and $\varphi \in (-\pi, +\pi)$ is the phase angle of the load current. The output power of the linear amplifier is then

$$P_o = \frac{U_{op}^2}{2Z_L} \cos \varphi. \quad (2.3)$$

For a LPA operating in class-AB mode, the low quiescent current can be neglected for the losses calculation. Therefore, the losses resulting for transistor T_{p1} (see Figure 2.1(c)) are

$$\begin{aligned} P_{T_{p1},tra} &= \frac{1}{2\pi} \int_{\varphi}^{\varphi+\pi} (V_{CC} - U_{op} \sin \omega t) \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t \\ &= \frac{U_{op}}{2\pi \cdot Z_L} \left(2V_{CC} - \frac{1}{2}\pi \cdot U_{op} \cos \varphi \right). \end{aligned} \quad (2.4)$$

If the class-AB power amplifier is supplied by the proposed converter, we have for the power losses of transistor T_{p1} (see Figure 2.1(e)) and $\varphi \in (0, +\pi)$

$$\begin{aligned}
P_{T_{p1},pro} &= \frac{1}{2\pi} \left[\int_{\varphi}^{\pi} V_a \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t \right. \\
&\quad \left. + \int_{\varphi}^{\varphi+\pi} (V_a - U_{op} \sin \omega t) \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t \right] \quad (2.5) \\
&= \frac{U_{op}}{2\pi \cdot Z_L} \left[2V_a + \frac{1}{2} U_{op} (\sin \varphi - \varphi \cos \varphi) \right].
\end{aligned}$$

where $V_a = V_{CC} - U_{op}$ denotes the voltage remaining across a conducting power transistor. For $\varphi \in (-\pi, 0)$, the power losses in transistor T_{p1} are

$$\begin{aligned}
P_{T_{p1},pro} &= \frac{1}{2\pi} \left[\int_{\varphi}^0 (V_a - U_{op} \sin \omega t) \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t \right. \\
&\quad \left. + \int_0^{\pi+\varphi} V_a \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t \right] \quad (2.6) \\
&= \frac{U_{op}}{2\pi \cdot Z_L} \left[2V_a + \frac{1}{2} U_{op} (\varphi \cos \varphi - \sin \varphi) \right].
\end{aligned}$$

By combining (2.5) and (2.6) the power losses of transistor T_{p1} for $\varphi \in (-\pi, +\pi)$ result in

$$P_{T_{p1},pro} = \frac{U_{op}}{2\pi \cdot Z_L} \left[2V_a + \frac{1}{2} U_{op} |\varphi \cos \varphi - \sin \varphi| \right]. \quad (2.7)$$

In Figure 2.3 the normalized transistor losses, the input power $P_{in} = P_o + 2P_{Tp}$, the output power P_o and the efficiency η of the linear class-AB power amplifier are given for different load conditions for the assumed operating parameters of $V_{CC} = 230$ V, $V_a = 30$ V, $U_{op} = 200$ V, and $Z_L = 20$ Ω . Here, the normalization basis for the power is defined as

$$S_{base} = \frac{U_{op}^2}{2Z_L}; \quad (2.8)$$

and P_{Tp} denotes the losses of a power transistor. By employing the proposed concept the transistor power losses can be significantly reduced in comparison to constant supply voltage, resulting in a significant improvement of the

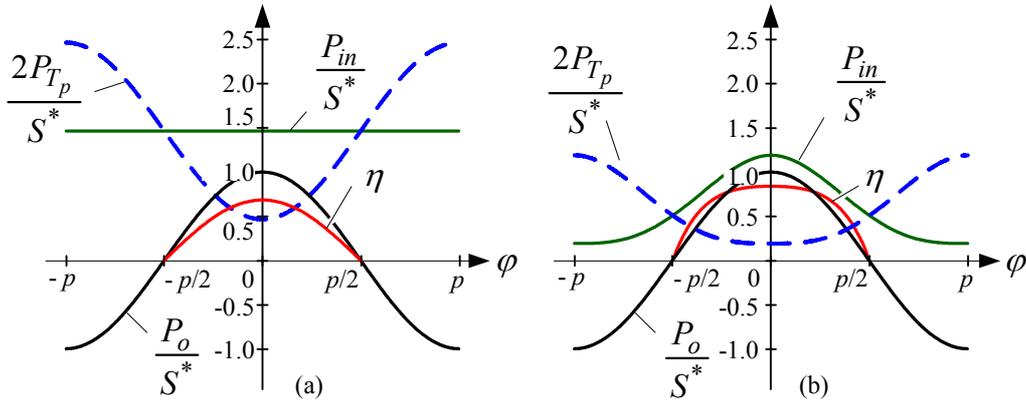


Figure 2.3: Dependency of the normalized transistor losses (normalization with reference to S_{base} as defined in (8)), input power, output power, and efficiency of a linear class-AB power amplifier on the load phase angle for constant supply voltage (a) and for the proposed supply voltage conditioning (b).

amplifier efficiency (in Figure 2.3, the efficiency is only shown for passive loads, i.e., for phase angle values $\varphi \in (-\pi/2, +\pi/2)$).

In Figure 2.4 the normalized transistor power losses are depicted in dependence on the normalized output voltage amplitude, where the normalization basis is the maximum output voltage amplitude $U_{op,max}$; the operating parameters are $V_{CC} = 230$ V, $V_a = 30$ V, $U_{op,max} = 200$ V, and $Z_L = 20$ Ω . Evidently, the losses are reduced significantly due to the conditioning of the

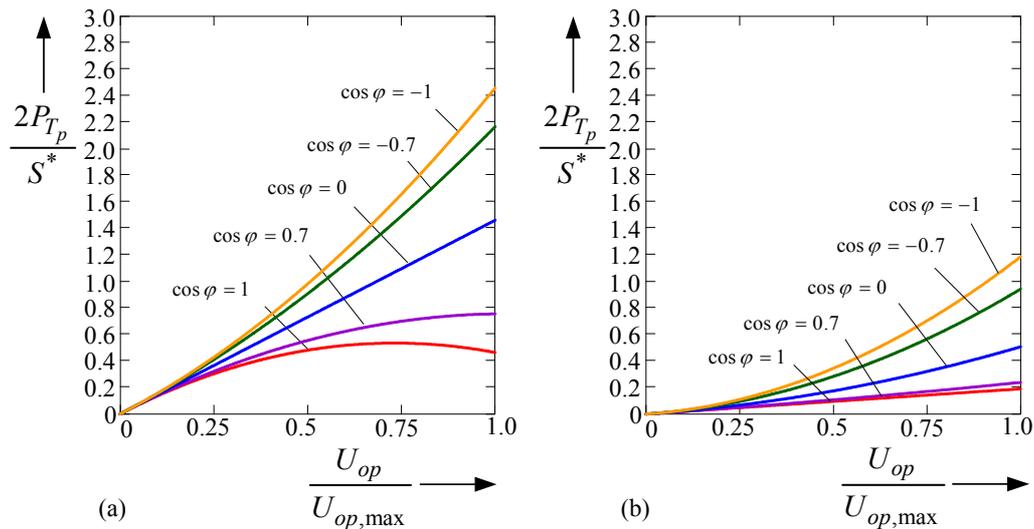


Figure 2.4: Dependency of the normalized transistor power losses on the normalized amplifier output voltage amplitude for constant supply voltage (a) and for supply voltage conditioning (b) according to Figure 2.1(d).

supply voltage.

2.3 Tracking Power Supply Design

Firstly, the operating principle of the TPS will be described in this section, then the switching frequency of the boost stage MOSFET is analyzed and the dimensioning of the output capacitors is explained. Furthermore, the equations for calculating the current stresses on the components are given and the calculated results are verified by numerical simulation, and finally the components are selected according to the defined specifications.

2.3.1 Basic Operating Principle

In order to simplify the analysis of the system and to focus on the main aspects, the three-level isolated dc-dc converter is replaced by a buck converter in the following analysis. The control structure of the proposed TPS is shown in Figure 2.5. The proposed converter consists of: (i) a buck stage, in which the main inductor is split into two inductors L_1 and L_2 in order to have the same common-mode noise rejection in both paths and the inductor current i_L is controlled to a constant value and where constant-frequency, average current-mode control and feed-forward of the local average value of the voltage across the power transistors T_2 and T_3 are employed, (ii) a boost stage where a tolerance band control is performed to achieve high dynamics with a low realization effort, and (iii) an output filter that reduces the supply voltage switching ripple to guarantee a good output voltage THD figure of the LPA.

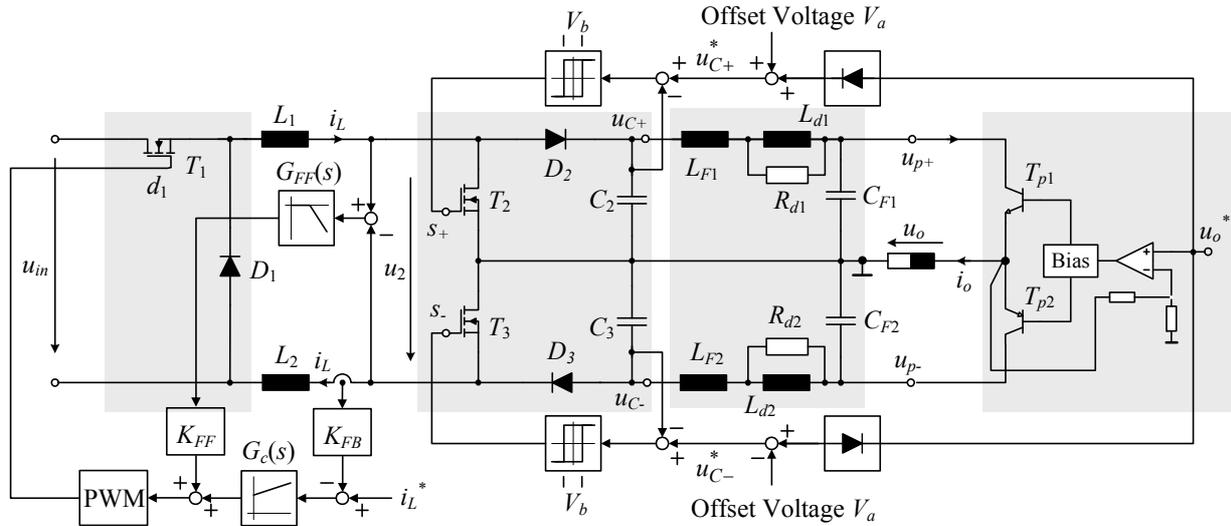


Figure 2.5: Structure of the proposed TPS using a buck converter as the input stage instead of a three-level isolated dc-dc converter. V_a is the offset voltage; V_b is the width of the tolerance band.

The conduction states of the output stage are shown in Figure 2.6 for positive load current. There, the buck-type input stage is represented by a current source i_L and the output filter is neglected. For realizing the control of the supply voltages of the LPA according to Figure 2.5, T_3 remains in the on-state in the case that u_{C-} is higher than the reference value $u_{C-}^* - \frac{1}{2}V_b$, where V_b is the width of the tolerance band. When the positive supply voltage u_{C+} due to the current consumption of the linear amplifier (see Figure 2.6(a)) reaches the lower boundary of the tolerance band $u_{C+}^* - \frac{1}{2}V_b$, T_2 is turned off (see Figure 2.6(b)) and the current i_L commutates into D_2 and recharges the

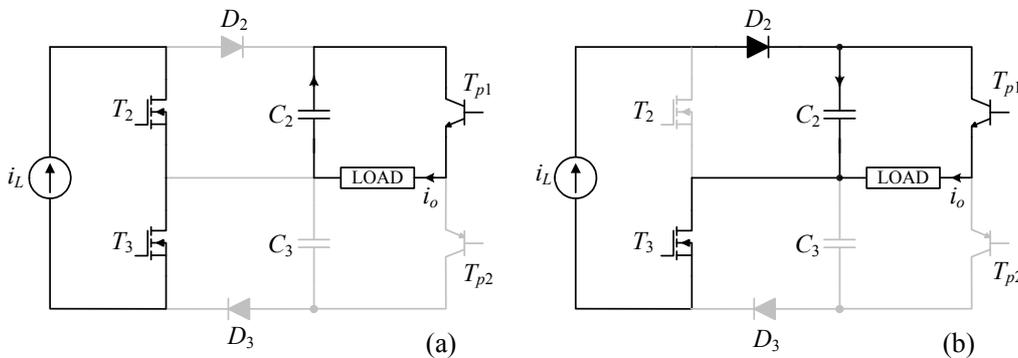


Figure 2.6: Simplified equivalent circuit of the proposed converter and conduction states of the output stage for positive load current.

output capacitor C_2 . If u_{C+} reaches the upper boundary of the tolerance band $u_{C+}^* + \frac{1}{2}V_b$, T_2 is turned on, accordingly diode D_2 blocks (see Figure 2.6(a)), and i_L free-wheels through T_2 and T_3 .

2.3.2 Switching Frequency Analysis

The switching frequency range of the boost switches is now analyzed and this information is used for calculating the switching losses and designing the output filter. Since the switching frequency is much higher than the output current frequency, a balanced charge flow of the output capacitors is assumed over a switching period. The charge flow balance of the capacitor C_2 is given by

$$[I_L - I_{op} \sin(\omega t - \varphi)]T_{on} = I_{op} \sin(\omega t - \varphi)T_{off}, \quad (2.9)$$

where $\omega t \in (\varphi, \pi + \varphi)$. The discharge time can be calculated as

$$T_{off} = C \frac{V_b}{I_{op} \sin(\omega t - \varphi)}, \quad (2.10)$$

where $C = C_2 = C_3$. Therefore, the local switching frequency f_s can be derived as

$$f_s = \frac{1}{T_{on} + T_{off}} = \frac{\sin \omega t (\alpha - \sin \omega t)}{\alpha C V_b} I_{op}, \quad (2.11)$$

where α denotes the current ratio $\alpha = I_L / I_{op}$. The maximum switching frequency therefore is given by

$$f_{s,max} = \frac{\alpha I_{op}}{4C V_b} = \frac{I_L}{4C V_b} \quad (2.12)$$

and the average switching frequency is

$$f_{s,avg} = \frac{1}{2\pi} \int_0^\pi f_s d\omega t = \frac{I_{op}}{2\alpha C V_b} \left(\frac{2\alpha}{\pi} - \frac{1}{2} \right). \quad (2.13)$$

As shown in (2.12) and (2.13), the switching frequency of the boost stage is inversely proportional to the width of the hysteresis band V_b . For selecting the width of the hysteresis band we need a compromise between the boost stage switching frequency and the output switching noise. For example, if we reduce V_b , the switching frequency of the boost stage will be increased, which results in higher switching losses, but on the other hand the switching noise contained in the output voltage of the converter is lowered, which decreases the attenuation requirement of the output filter.

2.3.3 Dimensioning of the Output Capacitors C_2 and C_3

The capacitance C of the output capacitors C_2 and C_3 has a significant influence on the required current source value I_L and the switching frequency of the boost stage. Decreasing the capacitance of C_2 and C_3 can bring the benefit of a lower required value of I_L that will reduce the current stresses of the power components (see (2.16)), but increases the switching frequency of the boost stage as given in (2.12) and (2.13). A practical selection of the output capacitor value is to limit the maximum capacitor current value to 20% of the peak current of the LPA. The capacitor value then can be calculated as

$$C \approx \frac{0.2I_{op}}{2\pi f_o U_{op}}, \quad (2.14)$$

where f_o is the output frequency.

2.3.4 Constant Inductor Current I_L

In order to ensure the good performance of the supply voltages conditioning, the constant inductor current I_L must always be higher than the summed current I_{sum} needed by the LPA and output capacitors, which is

$$I_{sum} = I_{op} \sin(\omega t - \varphi) + \omega C U_{op} \cos \omega t. \quad (2.15)$$

The required maximum value $I_{sum,max}$ of the inductor current (which occurs for capacitive loading of the amplifier) can be calculated as

$$I_{sum,max} = I_{op} + \omega C U_{op} . \quad (2.16)$$

With respect to the switching ripples in the inductor current and for providing a modulation margin for T_2 and T_3 , the constant inductor current is set to

$$I_L^* = 1.4 I_{sum,max} . \quad (2.17)$$

2.3.5 Current Stresses on the Components

For the calculation of the current stresses it is assumed that the circuit is operating symmetrically, i.e. the current stresses of T_2 , D_2 and C_2 are same as the current stresses of T_3 , D_3 and C_3 respectively, and all components are ideal, i.e. the output power of the system is equal to the input power. With this, we have for the average and rms value of the current through transistor T_1

$$I_{T_1,avg} = \frac{P_O + 2P_{T_{p1},pro}}{U_{in}} , \quad (2.18)$$

$$I_{T_1,rms} = \sqrt{I_{T_1,avg} I_L} . \quad (2.19)$$

Furthermore, the diode D_1 values are

$$I_{D_1,avg} = I_L - I_{T_1,avg} , \quad (2.20)$$

$$I_{D_1,rms} = \sqrt{I_{D_1,avg} I_L} . \quad (2.21)$$

The average and rms values of the current through D_2 are

$$I_{D_2,avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} I_{op} \sin(\omega t - \varphi) d\omega t = \frac{I_{op}}{\pi} , \quad (2.22)$$

$$I_{D_2,rms} = \sqrt{\frac{I_{op}I_L}{\pi}}. \quad (2.23)$$

Finally, we have for the average value and the rms value of the current through the boost transistors T_2

$$I_{T_2,avg} = I_L - I_{D_2,avg} = \left(\alpha - \frac{1}{\pi}\right) I_{op}. \quad (2.24)$$

$$I_{T_2,rms} = \sqrt{\left(\alpha - \frac{1}{\pi}\right) I_{op}I_L}. \quad (2.25)$$

For calculating the rms value of the currents through C_2 and C_3 , it is assumed that the current through the output capacitor C_2 (or C_3) only occurs when the corresponding transistor T_{p1} (or T_{p2}) is conducting, and the output current i_o is constant during the switching period. Here the square of the local rms value of the capacitor current i_c in a single switching period is defined as

$$i_{cs}^2 = \frac{1}{T_s} \int_0^{T_s} i_c^2 dt = \frac{1}{T_s} \left\{ [I_L - I_{op} \sin(\omega t - \varphi)]^2 T_{on} + [I_{op} \sin(\omega t - \varphi)]^2 T_{off} \right\}. \quad (2.26)$$

By combining (2.26) with (2.9) and (2.10) we have

$$i_{cs}^2 = I_{op} \sin(\omega t - \varphi) [I_L - I_{op} \sin(\omega t - \varphi)]. \quad (2.27)$$

Therefore the rms value of the output capacitor current during one output period can be calculated as

$$I_{C_2,rms} = \sqrt{\frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} i_{cs}^2 d\omega t} = I_{op} \sqrt{\frac{\alpha}{\pi} - \frac{1}{4}}. \quad (2.28)$$

The stresses on the components have to be calculated for the worst operation point, i.e., the output voltage $U_{o,rms} = 132$ V and the output current $I_{op} = 10$ A for a resistive load. The calculated components current stresses are

compared to the simulated results, as shown in **Tab.I**; there, for the operating parameters $U_{in} = 200$ V, $V_a = 25$ V, $I_L = 15$ A, $U_{op,rms} = 132$ V, $I_{op} = 10$ A, $R_L = 18.6$ Ω and $f_o = 400$ Hz have been selected. The simulated results show a very good correspondence to the calculated values. According to the components current stresses listed in Tab.I, the main power devices are selected (see Tab.II in Section VI).

Table 2.1: Comparison of the Calculated and Simulated Component Stresses.

		Current [A]	
		Calculated	Simulated
T1	avg	5.46	5.48
	rms	9.05	9.05
D1	avg	9.54	9.52
	rms	11.96	11.99
T2,3	avg	11.82	11.82
	rms	13.31	13.34
D2,3	avg	3.18	3.19
	rms	6.91	6.90
C2,3	rms	4.77	4.82

2.3.6 Switching Losses Measurement

Proper system design requires correct information on the semiconductor switching losses employed in the system. This information is used for determining the system losses distribution, small signal modelling and selecting the heat sink. Since the switching losses are highly dependent on the parasitic parameters in the hardware, e.g. the commutation loop inductance (ESR of the film capacitor, device lead inductances, and PCB track inductances), gate driver etc. The same semiconductors might have very different switching losses in different hardware. The way regarded as most accurate is to directly measure the switching losses in the hardware setup [33].

In Figure 2.7, the switching losses measurement setups are depicted for the buck stage (a) and the boost stage (b). Here the components are the same as the ones listed in Table 2.4. Only one extra external capacitor 2.2 mF / 450 V is added to the system in Figure 2.7(b), in order to keep the switching voltage stable for the boost stage switching losses measurement. The switching currents are measured with an AC current transformer with a turns ratio of 1:50 (A in Figure 2.7). This current sensor comprises a R6.3/N30 toroidal ferrite core, a burden resistor of 5 Ω and an impedance matching network to a 50 Ω coaxial cable. Another current sensor, B in Figure 2.7, is measured by the Tektronix TCP202 used for monitoring the inductor current. The switching voltages are measured by a LeCroy voltage differential probe DXC100A in conjunction with the differential amplifier D1855A. Before starting the switching losses measurement, it is vital to calibrate the delay between the current sensor and voltage probe. For the equipments employed here, the voltage measurement has a delay of 7.6 ns with reference to the current measurement.

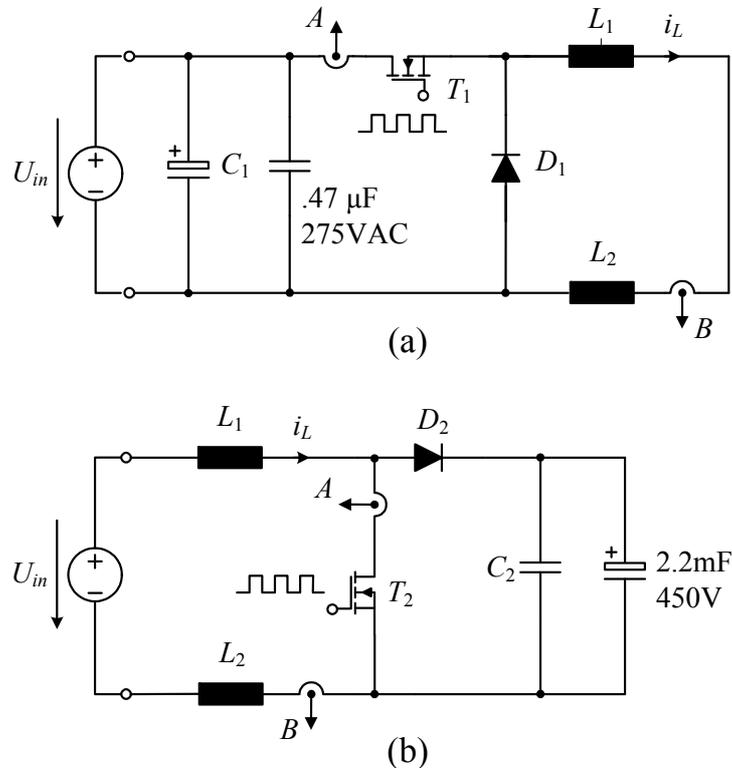


Figure 2.7: Switching losses measurement setup for the buck stage (a) and the boost stage (b).

The measured switching behavior of the switch unit T_1 and D_1 in the buck stage is shown in Figure 2.8. Here the turn-on behavior is measured at junction temperatures of 120°C (a) and 30°C (b) respectively. The switching voltage and current are 200 V and 17 A . The turn-on power losses p_{on} and turn-on energy w_{on} (which is integrated from p_{on}) are calculated from the measured switching voltage u_{sw} and switching current i_{sw} . It is shown from Figure 2.8(a) that the turn-on peak current reaches 34 A , which is twice the switching current I_{sw} . This is caused by the reverse recovery current of the freewheeling diode D_1 . The measured turn-on energy loss at the junction

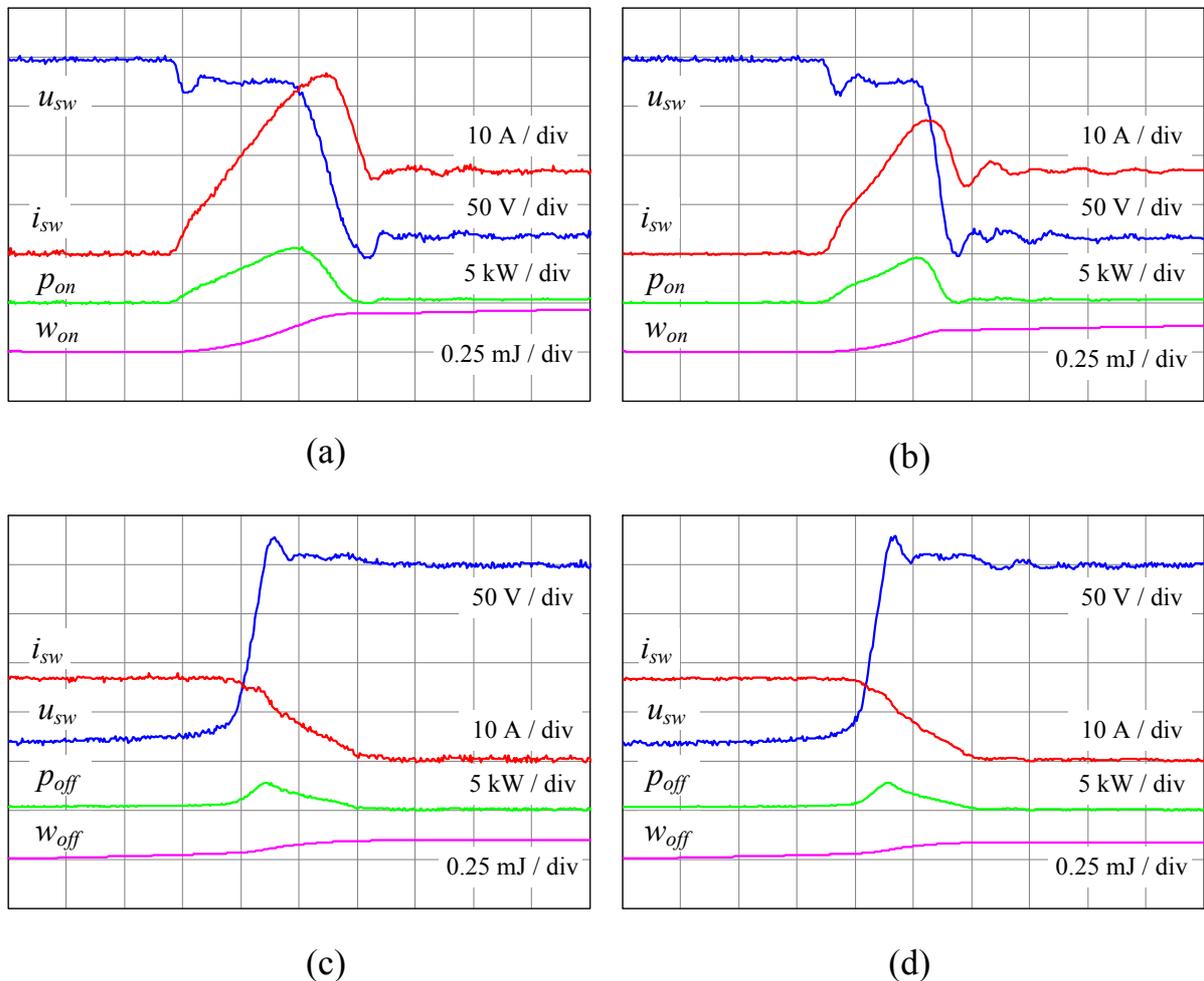


Figure 2.8: Measured switching behavior of the switch unit consisting of T_1 , SPW20N60C3, and D_1 , RHRG3060, in the buck stage: turn on at $17\text{ A} / 200\text{ V}$ with device junction temperature of 120°C (a) and 30°C (b); turn off at $17\text{ A} / 200\text{ V}$ with device junction temperature of 120°C (c) and 30°C (d); Time scale: 20 ns/div .

temperature of 120°C is 238 μJ which is almost double the one measured at the junction temperature of 30°C, 147 μJ . This is because the reverse recovery character of D1, RHRG3060, is much worse at high junction temperature. The buck stage turn-off behavior at junction temperatures of 120°C and 30°C is shown in (c) and (d) respectively. From the measurement, the turn-off energy losses at 120°C and 30°C are 75 μJ and 66 μJ respectively. In contrast to the turn-on energy losses, the turn-off energy losses are only slightly increased at higher junction temperature because there is no influence of the diode reverse recovery current.

In the laboratory, the turn-on energy loss w_{on} , turn-off energy loss w_{off} and reverse recovery energy loss w_{rr} in the buck and boost stages are measured at each testing condition over junction temperatures of 30°C, 60°C, 90°C and 120°C, switching voltages of 100V, 150V and 200V, and for five switching currents evenly selected from 1A to 20A. Each energy loss measurement is performed three times and the average value is finally used for data fitting.

The measured switching losses in the buck stage and boost stage at 120°C junction temperature are depicted in Figure 2.9 and Figure 2.10 respectively. For a least-square fitting of the turn-on and turn-off energy losses we use [34] - [35]

$$w = k_1 u^2 + k_2 u \cdot i + k_3 u^2 i + k_4 u i^2 + k_5 u^2 i^2, \quad (2.29)$$

and for the free-wheeling diode reverse recovery energy losses we use

$$w = k_2 u \cdot i + k_3 u^2 i + k_4 u i^2 + k_5 u^2 i^2 + k_6 i. \quad (2.30)$$

The calculated polynomial coefficients are listed in Table 2.2¹. In order to embed the switching losses information into the system small signal model to be derived later and for the calculation of the switching losses in the

¹ It is also possible to include the temperature variable into the fitting function [36]. In this case the approximation function including variables of voltage, current and temperature should perform a three-dimensional fitting to the measured data.

boost stage, another least-squares approximation which simply regards the switching losses as proportional to the product of the switching current and voltage as given below,

$$w = k_7 u \cdot i. \quad (2.31)$$

The employed coefficient k_7 is calculated and compiled in Table 2.3. Figure 2.9 (b), (d), (f) and Figure 2.10(b), (d), (f) show the measured data and re-

Table 2.2: Polynomial coefficients of the least-square approximation of the measured switching losses.

Switching Losses Parameters							
		k_1	k_2	k_3	k_4	k_5	k_6
Buck Stage	On	0.76	56	$7.5 \cdot 10^{-4}$	0.27	$-3.99 \cdot 10^{-6}$	
	Off	$2.58 \cdot 10^{-2}$	14	$-2.49 \cdot 10^{-3}$	0.56	$-3.2 \cdot 10^{-5}$	
	R. R.	-	15	$-9.21 \cdot 10^{-3}$	-0.76	$1.48 \cdot 10^{-3}$	1156
Boost Stage	On	0.79	11	$2.87 \cdot 10^{-3}$	0.96	$-1.76 \cdot 10^{-5}$	
	Off	$3.43 \cdot 10^{-2}$	15	$-3.2 \cdot 10^{-3}$	1.18	$-2.3 \cdot 10^{-5}$	
	R. R.	-	13	$-2.71 \cdot 10^{-3}$	-0.32	$-3.93 \cdot 10^{-5}$	172
	Units	$nJ(V^2)^{-1}$	$nJ(VA)^{-1}$	$nJ(V^2A)^{-1}$	$nJ(VA^2)^{-1}$	$nJ(V^2A^2)^{-1}$	$nJ(A)^{-1}$

Table 2.3: Simplified least-square approximation of the measured switching losses.

Switching Losses Parameters		
		k_7
Buck Stage	On	71.5
	Off	20.7
	R. R.	14.3
Boost Stage	On	36.4
	Off	30.6
	R. R.	8.9
	Units	$nJ(VA)^{-1}$

sulting fitted curves. There the fitted curves for the turn-on and turn-off energy losses are close to the measured data, but for the free-wheeling diode reverse recovery energy loss, the fitted curves disagree with the measurement data (Figure 2.9(f) and Figure 2.10(f)). However the reverse recovery energy loss only contributes a small fraction of the total switching losses compared to the turn-on and turn-off losses.

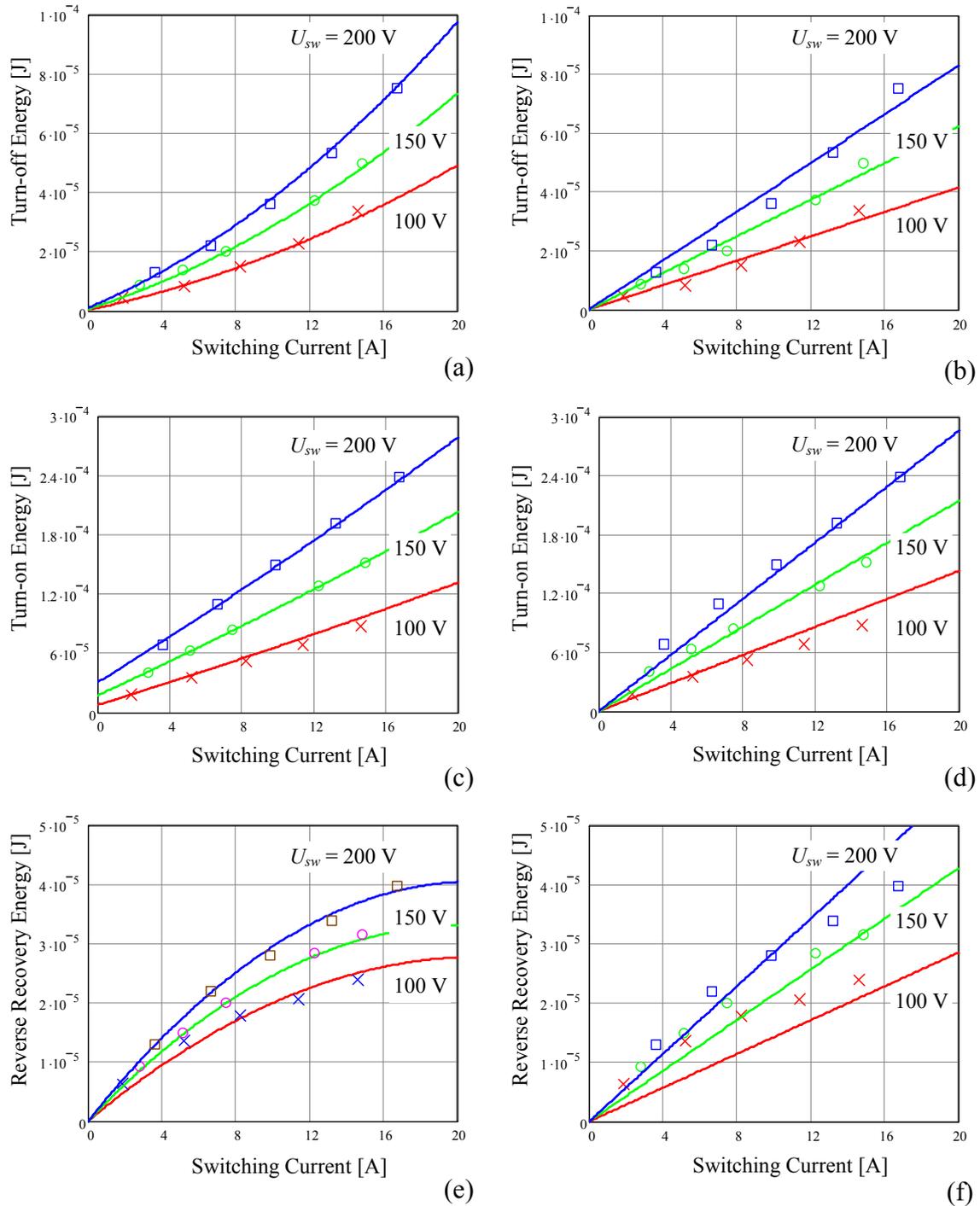


Figure 2.9: Least-square fittings of the measured switching losses in the buck stage operated at junction temperature of 120°C : MOSFET turn-off energy loss (a) MOSFET turn-on energy loss (c) and freewheeling diode reverse recovery energy loss (e) approximated by fitting function (2.29) and (2.30); MOSFET turn-off energy loss (b), MOSFET turn-on energy loss (d) and freewheeling diode reverse recovery energy loss (f) approximated by fitting function (2.31).

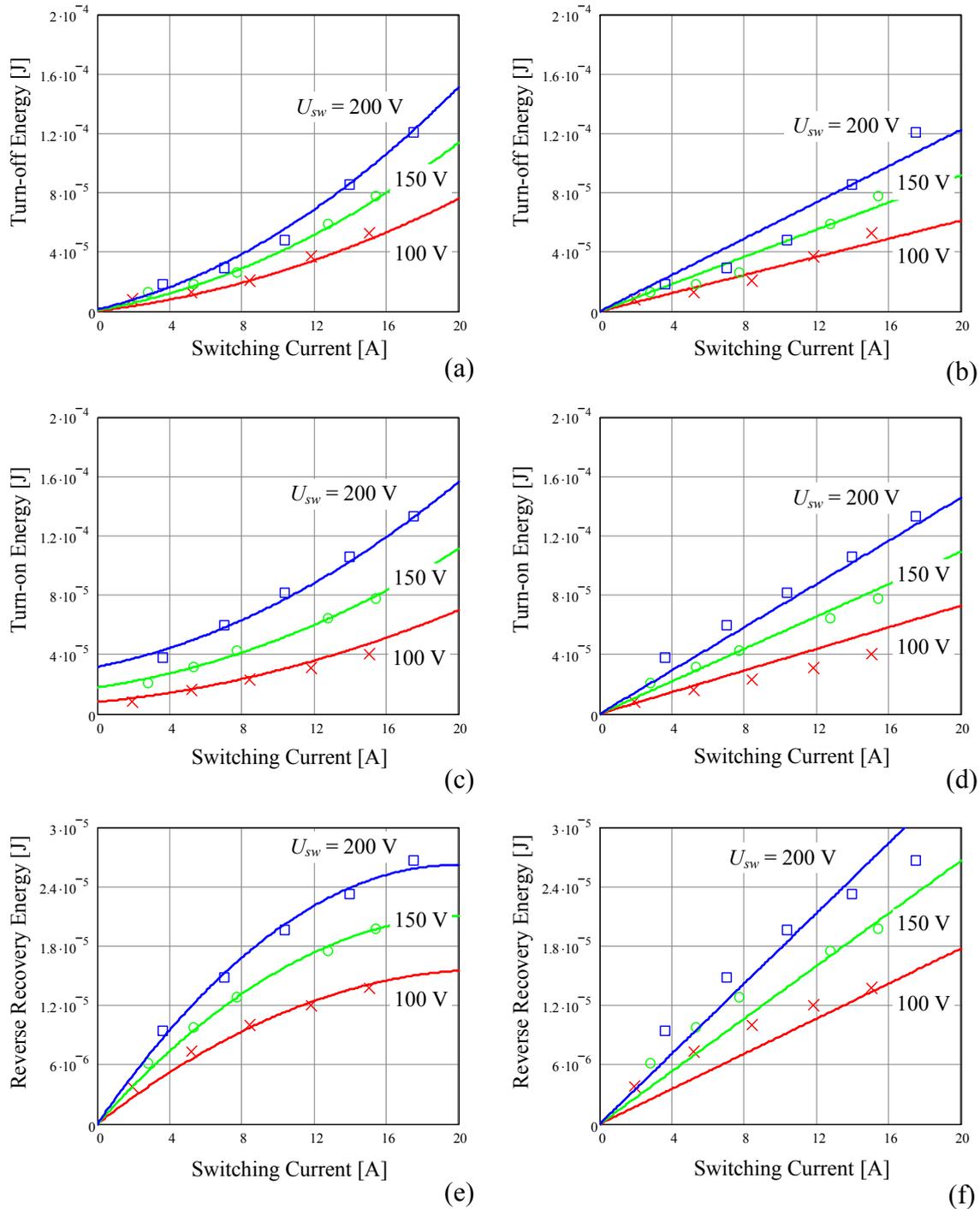


Figure 2.10: Least-square fittings of the measured switching losses in the boost stage operated at junction temperature of 120°C : MOSFET turn-off energy loss (a) MOSFET turn-on energy loss (c) and freewheeling diode reverse recovery energy loss (e) approximated by fitting function (2.29) and (2.30); MOSFET turn-off energy loss (b), MOSFET turn-on energy loss (d) and freewheeling diode reverse recovery energy loss (f) approximated by fitting function (2.31).

2.4 Output Filter Design

The power supply voltages for the LPA include switching frequency ripples which could reduce the quality of the output voltage due to the non-ideal power supply rejection ratio (PSRR) of the LPA. Therefore, a filter is placed between the converter and the LPA in order to limit the switching noise. However, the cut-off frequency of this filter should not be made too low as it could reduce the performance of the output voltage tracking.

In this section, a small signal model of a feed-forward controlled LPA is considered in order to derive the PSRR. Then, for a given THD+N limitation, a guideline to specify the harmonics of the supply voltages is calculated by using the derived PSRR. Finally, the output filter is designed to meet the harmonic requirement of the supply voltages for the LPA.

2.4.1 PSRR Consideration of the LPA

Firstly the PSRR of a simplified LPA is analyzed to specify the ripple limitation of the power supply voltage. The PSRR is very dependent on the configuration and on component parameters of the LPA [37]-[38]. For verifying the proposed TPS, a simple class-AB power amplifier using feed-forward control is experimentally analyzed. The schematic of the amplifier is shown in Figure 2.11. An integrated, high voltage, power amplifier device, APEX PA97, is employed to amplify the input voltage and provide the driver signal u_{vas} for the output power stage. After biasing the driver signal u_{vas} , two gate voltages u_{g1} and u_{g2} are generated and applied to the output power stage, which is a typical push-pull complementary stage.

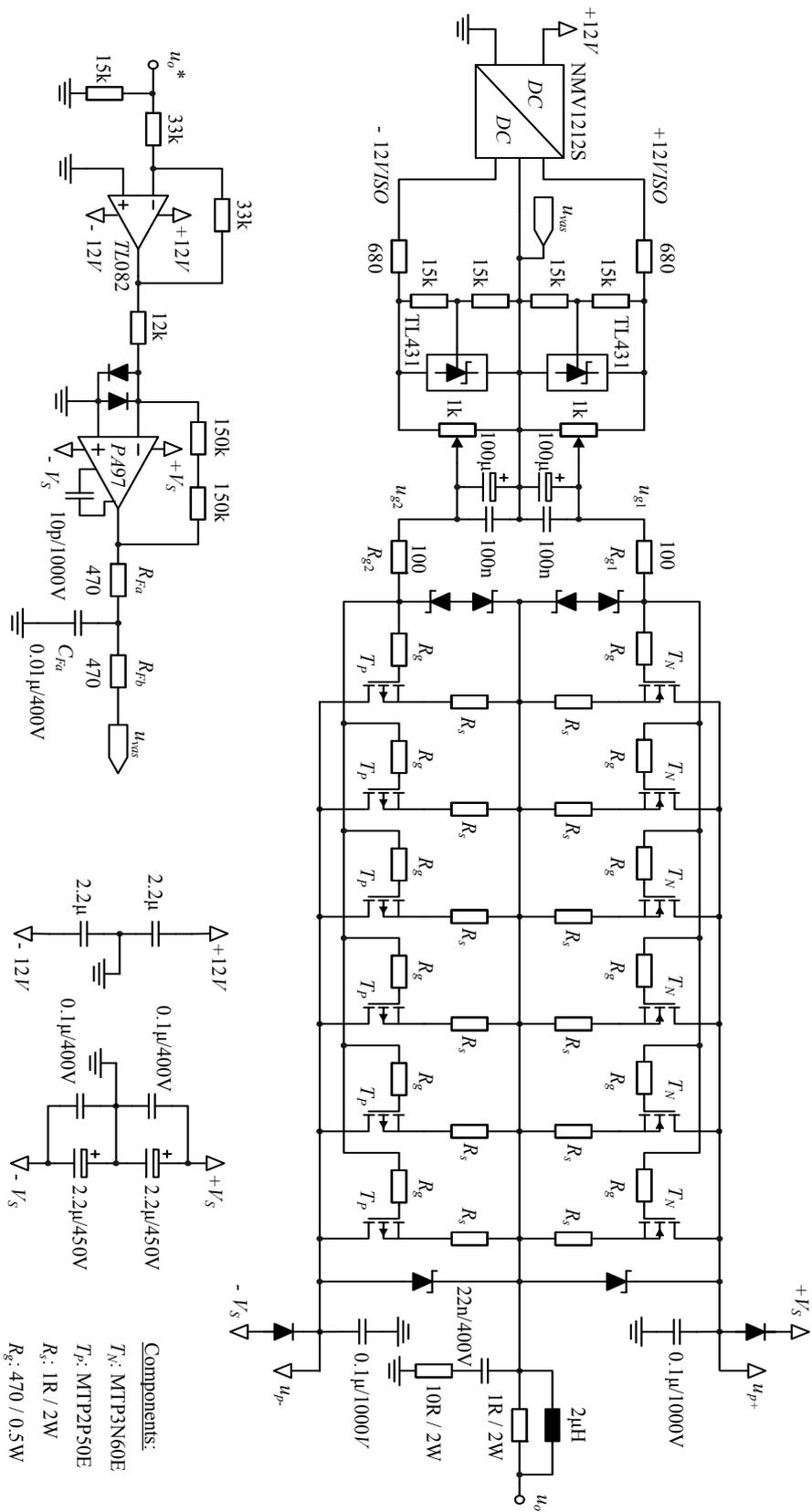


Figure 2.11: Circuit schematic of a simple laboratory class-AB power amplifier employing feed-forward control.

In the experimental system, only the output power stage is supplied by the TPS while the voltage gain stage is supplied by additional constant power supplies V_{S+} and V_{S-} (see Figure 2.11). Therefore, the noise in the supply is coupled to the system only through the output power stage of the LPA. In order to simplify the derivation of the PSRR of the LPA, we assume during the following analysis: i) the current is equally distributed in the power MOSFETs both in positive and negative power stages; ii) all the passive components are ideal.

Figure 2.12 shows the simplified small signal model for deriving the positive PSRR. In this model the gate-to-source capacitance is defined as C_{gs} ; C_{gd} is the gate-to-drain capacitance; g_m and r_0 are the transconductance and output impedance of the MOSFET respectively; R_s is the source resistance; R_L is the load resistance; $Z_G(s)$ is the impedance of the drive stage (shaded grey area in Figure 2.12), where the impedance of the bias stages is neglected since it is smaller compared to the other series connected components in this branch, and $Z_{pa}(s)$ is the output impedance of the PA97 with the designed negative feedback (parameters given in Figure 2.11).

The negative PSRR can be deduced analogously. The calculated and measured PSRR for positive supply-rail and negative supply-rail are compared in Figure 2.13. The calculated PSRRs show good matching with the measured results from the laboratory hardware. Furthermore, the results show that

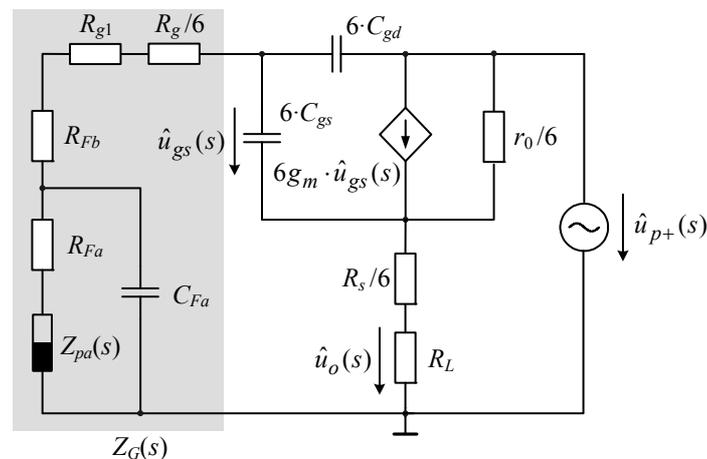


Figure 2.12: Simplified small signal model for deriving the positive PSRR. (refer to Figure 2.11)

the negative PSRR is less than the positive PSRR. The main reason is that the gate-to-drain capacitance of P-channel MOSFET MTP2P50E employed in the negative power stage is higher than that of N-channel MOSFET MTP3N60E used in the positive power stage, since the PSRR can be approximated as

$$F_{PSRR}(s) = \frac{\hat{u}_{p+}(s)}{\hat{u}_o(s)} \approx \frac{sC'_{gd}Z_G(s) + 1}{sC'_{gd}Z_G(s)}, \quad (2.32)$$

where $C'_{gd} = 6 \cdot C_{gd}$. It has been verified numerically that this approximated function closely matches the calculated PSRR resulting from the model given in Figure 2.12. Therefore, the dominant parameters of the output stage for determining the PSRR are the gate-to-drain capacitance C_{gd} and the driver stage impedance $Z_G(s)$. In Figure 2.13, it is shown that the PSRR has a slope

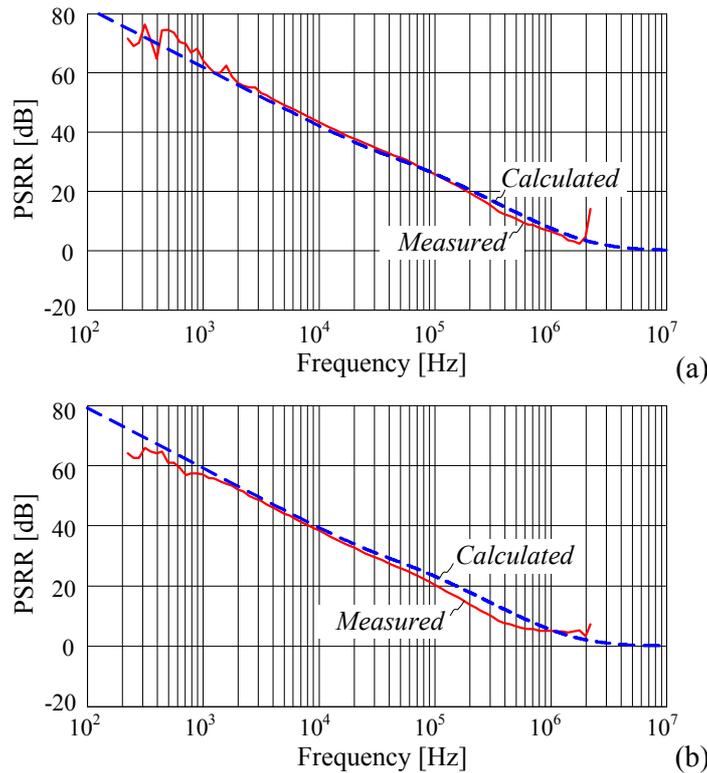


Figure 2.13: Comparison of calculated and measured PSRR for positive supply rail (a) and negative supply rail (b). The parameters for testing positive PSRR are: $U_o = 100V$, $U_{ds} = 25V$, $R_L = 30\Omega$, $C_{gs} = 751pF$, $C_{gd} = 19pF$, $g_m = 0.8S$, $r_o = 1.8M\Omega$ [39]; the parameters for testing negative PSRR are: $U_o = -100V$, $U_{ds} = -25V$, $R_L = 30\Omega$, $C_{gs} = 819pF$, $C_{gd} = 26pF$, $g_m = 0.9S$, $r_o = 1.6M\Omega$ [40].

of -20dB/decade for low frequencies, and if the frequency increases beyond the certain value, the LPA can no longer attenuate the supply voltage ripple and the ripple appears directly on the output voltage of the LPA.

As seen in (2.32), the gate-to-drain capacitance C_{gd} has a strong impact on the PSRR; however C_{gd} is highly dependent on the drain-to-source voltage U_{ds} of the power MOSFET. For a higher U_{ds} across the MOSFET, a higher PSRR can be achieved in the LPA, but on the other hand, this increases the voltage drop across of the MOSFET and results in higher power losses. Moreover, the closed-loop control of the LPA output voltage can increase the low frequency PSRR, but this is limited by the bandwidth of the control loop.

2.4.2 Output Filter Design

For LPAs, the required THD+N figure that characterizes the output voltage quality (output distortion due to the non-linearities in the signal path of amplifiers [41]) is dependent on the application, and in this chapter a value of 0.1% is assumed to be suitable. The aim of the filter design is to limit the output voltage noise caused by the switching frequency ripple of the supply voltages so as not to significantly influence the THD+N figure.

The simulated spectrum of the switching frequency voltage ripple in the output voltage of the TPS without a filter is shown in Figure 2.14. The spectrum illustrates that the switching noise is mainly between 100kHz and 300kHz.

Before undertaking the filter design a guideline for the rms amplitude of any output voltage harmonic component caused by the switching power supply must be specified, and in this case a value of less than 10% THD is used. The guideline is given by (2.33) and is shown in Figure 2.14, where the THD is assumed to be 0.1% for testing power supply applications

$$U_{gui}(s) = 10\% \cdot 0.1\% \cdot U_{op} F_{PSRR}(s) . \quad (2.33)$$

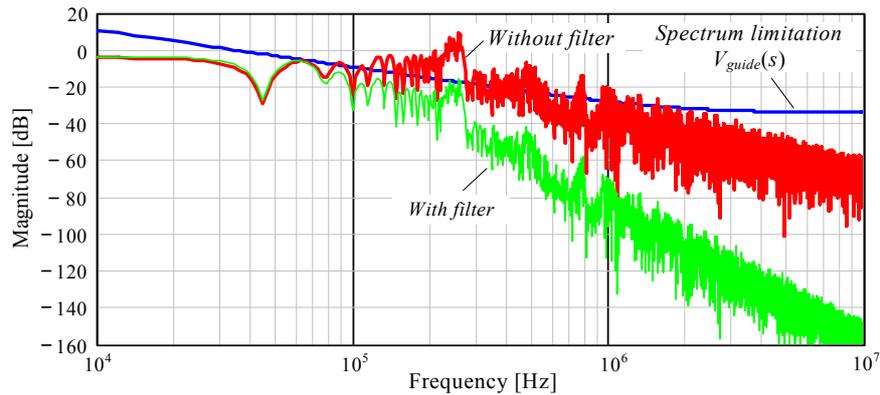


Figure 2.14: Simulated TPS voltage spectrum with/without filter. Simulation parameters are: $I_L=15\text{A}$, $V_b=25\text{V}$, $U_{o,rms}=115\text{V}$, $f_o=400\text{Hz}$, $R_L=16.2\ \Omega$.

In the previous equation, the negative supply-rail rejection ratio is used since it is worse than the positive supply-rail rejection ratio. A filter topology is selected and the parameters of the components are calculated to fulfil the criteria, as shown in Figure 2.15. The design of the filter parameters uses the procedure referred to in [42] and [43]. The spectrum of the filtered output voltage of the TPS is shown in Figure 2.14, where all the frequency components are lower than the required level. The total noise in the output voltage caused by the supply switching noise in the case of no output filter is about 0.6% of the output fundamental for the nominal operating point; with the output filter the noise figure is significantly reduced to 0.05%.

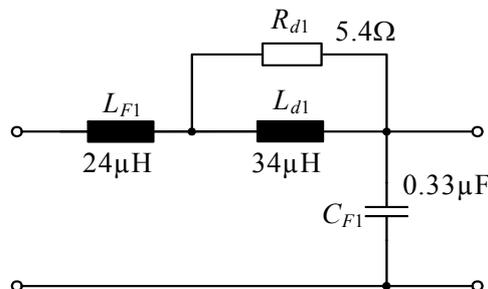


Figure 2.15: The topology and parameters of the output filter.

2.5 Controller Design

In this section, the small signal model of the TPS is first derived, then feed-forward control is implemented to improve the stability of the system, and finally the design of the constant current controller is described.

2.5.1 Linearized Small Signal Model

The equivalent circuit of the TPS when the upper output stage is operating is given in Figure 2.16(a), and the corresponding linearized small signal model including the main damping resistance is shown in Figure 2.16(b) [44]. The damping resistances include the equivalent resistances R_{e1} and R_{e2} of the semiconductors in the buck stage and boost stage, and the resistances $R_{s,u1}$, $R_{s,i1}$ and $R_{s,u2}$, $R_{s,i2}$ which represent the switching losses of the buck stage and boost stage; the resistance R_{LM} is the summation of the equivalent series resistances of the inductor L_1 and L_2 ; R_{LF1} and R_{Ld1} are the equivalent series resistances of the output filter inductors. The equivalent semiconductor resistances R_{e1} and R_{e2} representing the semiconductor conduction losses can be determined from

$$R_{e1} = D_{bk}R_{T_1} + (1 - D_{bk})r_{D_1} \quad (2.34)$$

$$R_{e2} = D_{bt}R_{T_2} + (1 - D_{bt})r_{D_2}, \quad (2.35)$$

where D_1 and D_2 are the static duty cycles of the buck stage and boost stage, R_{T_1} and r_{D_1} are the on-resistances of the switch and diode of the buck stage, and R_{T_2} and r_{D_2} are the on-resistances of the switch and diode of the boost stage. The voltage sources U_{e1} and U_{e2} denote the equivalent voltage drops of the diodes in the buck stage and boost stage. These voltage sources do not influence the small signal model but slightly alter the DC operating point of the system.

The influence of the switching losses in the buck stage (or the boost stage) on the small signal model can be represented by damping resistors $R_{s,u}$ and $R_{s,i}$ [45]. This consideration is based on an approximation that the switching

losses including turn-on losses, turn-off losses and reverse recovery losses are proportional to the product of the switching voltage U_{sw} and switching current I_{sw} at a given operating point as given by

$$P_{sw} = k_{tt} f_{sw} U_{sw} I_{sw} , \quad (2.36)$$

where k_{tt} is the switching losses coefficient which can be obtained by using (2.31) to fit the switching losses measurement results, and f_{sw} is the switching frequency. The damping resistors $R_{s,u}$ and $R_{s,i}$ can be calculated as [45]

$$R_{s,u} = \frac{2U_{sw}}{k_{tt} f_{sw} I_{sw}} , \quad (2.37)$$

$$R_{s,i} = \frac{k_{tt} f_{sw} U_{sw}}{2I_{sw}} . \quad (2.38)$$

By applying (2.37) and (2.38) to the switches of buck and boost stages respectively, the damping resistances $R_{s,u1}$, $R_{s,i1}$, $R_{s,u2}$ and $R_{s,i2}$ can be calculated as

$$R_{s,u1} = \frac{2U_{in}}{k_{tt1} f_{bk} I_L} , R_{s,i1} = \frac{k_{tt1} f_{bk} U_{in}}{2I_L} ; \quad (2.39)$$

$$R_{s,u2} = \frac{2U_{C+}}{k_{tt2} f_{bt} I_L} , R_{s,i2} = \frac{k_{tt2} f_{bt} U_{C+}}{2I_L} , \quad (2.40)$$

where f_{bk} is the switching frequency of buck stage, f_{bt} is the average switching frequency of the boost stage for the considered operating point, k_{tt1} and k_{tt2} are measured switching losses coefficients of buck stage and boost stage respectively.

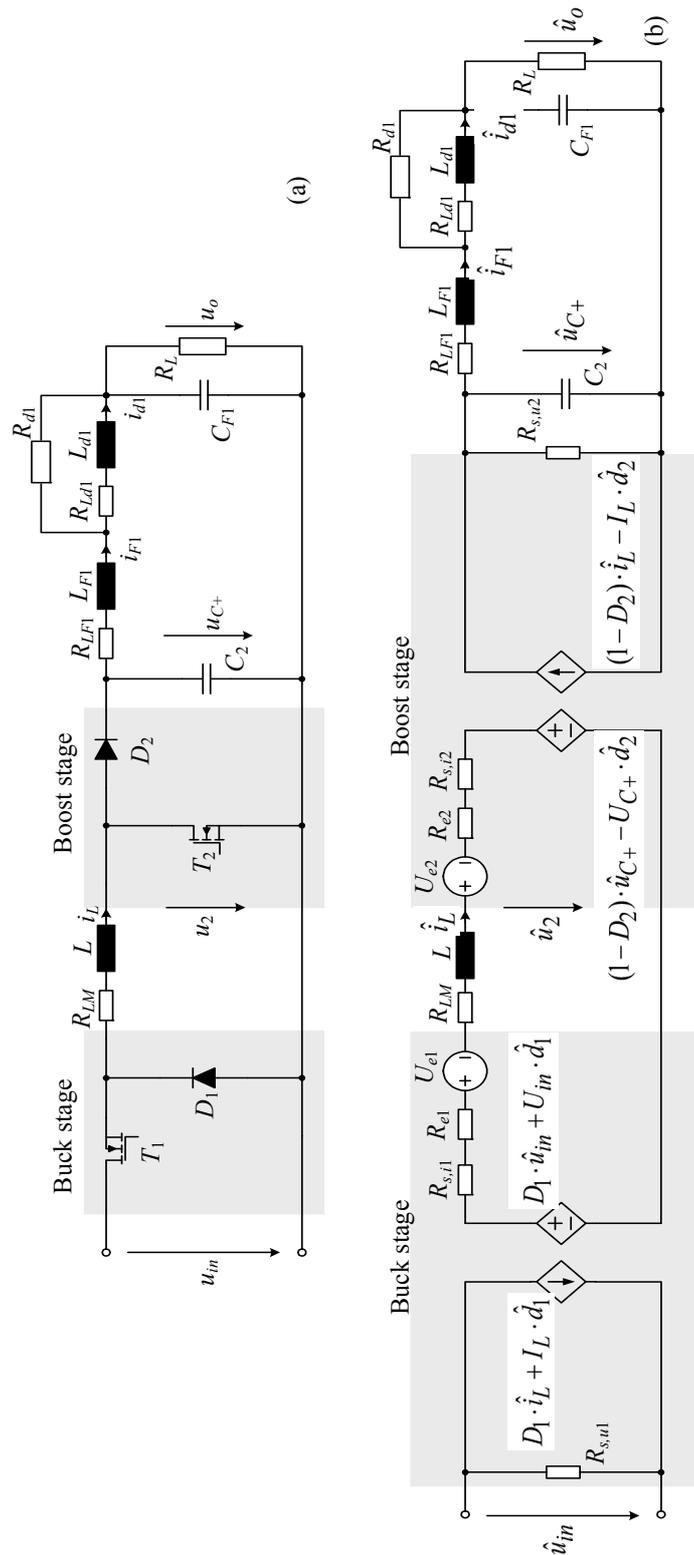


Figure 2.16: Equivalent circuit of the TPS when the upper output stage is operating (a), and corresponding linearized small signal model including the main damping resistances (b).

The step responses of the inductor current, i_L , for a small change in the buck-stage duty cycle ($\Delta d_1 = 8\%$) are shown in Figure 2.17. The results from two typical operating points, a buck-boost mode ($D_{bk} = 0.5$ and $D_{bt} = 0.5$) and buck mode ($D_{bk} = 0.5$ and $D_{bt} = 0$), are measured experimentally and compared with the theoretical responses. Here the semiconductor parameters employed to perform the theoretical calculation are obtained from the data-sheets of the components, assuming a junction temperature of 125°C . These parameters are: $R_{T1} = 0.29 \Omega$, $r_{D1} = 0.037 \Omega$, $k_{tt1} = 1.0 \cdot 10^{-7} \text{ s}$, $R_{LM} = 0.03 \Omega$, $R_{T2} = 0.11 \Omega$, $r_{D2} = 0.06 \Omega$, $k_{tt2} = 7.8 \cdot 10^{-8} \text{ s}$. The calculated damping resistances in buck mode are: $R_{s,u1} = 12 \text{ k}\Omega$, $R_{s,i1} = 0.3 \Omega$, $R_{e1} = 0.16 \Omega$, $R_{e2} = 0.06 \Omega$, $R_{s,i2} = 0.09 \Omega$, $R_{s,u2} = 9.7 \text{ k}\Omega$. And in buck-boost mode these resistances are: $R_{s,u1} = 3 \text{ k}\Omega$, $R_{s,i1} = 0.075 \Omega$, $R_{e1} = 0.16 \Omega$, $R_{e2} = 0.085 \Omega$, $R_{s,i2} = 0.05 \Omega$, $R_{s,u2} = 4.9 \text{ k}\Omega$. The figure shows that the theoretical model closely predicts the actual response. It can also be seen that the buck-boost mode of operation has higher damping and a longer rise time compared to the buck mode of operation.

2.5.2 Feed-forward Control and Current Loop Design

From the system small signal model, the transfer function $G_{d_{bki}}(s)$ from buck stage duty cycle variations, $\tilde{d}_{bk}(s)$, to the inductor current small signal

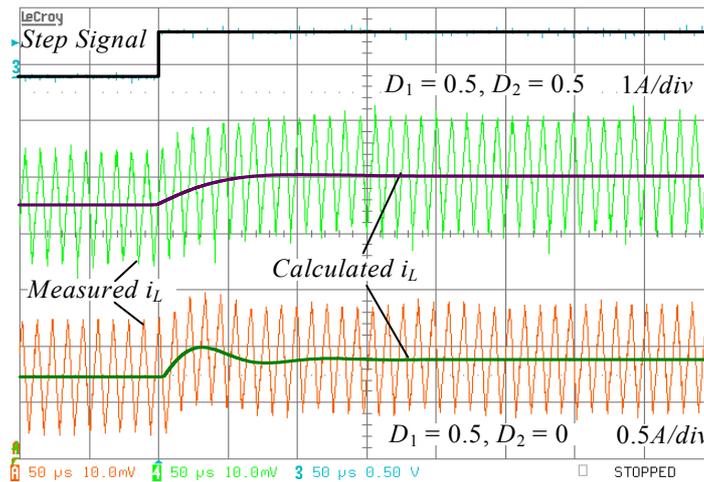


Figure 2.17: Comparison of the step responses between measurement results and calculation results, at operating points of $D_{bk} = 0.5$ and $D_{bt} = 0.5$ (buck-boost mode) and $D_{bk} = 0.5$ and $D_{bt} = 0$ (buck mode). The operating parameters are: input voltage $U_{in} = 100\text{V}$, $R_L = 30\Omega$, $f_{bk} = 100\text{kHz}$, $f_{bt} = 100\text{kHz}$, $U_{C+} = 100\text{V}$ (buck-boost mode) / 50V (buck mode).

variations, $\tilde{i}_L(s)$, and the transfer function $G_{ui}(s)$ from the output voltage variations of the boost stage, $\tilde{u}_{C+}(s)$, to $\tilde{i}_L(s)$ can be derived. Since the boost stages utilize hysteresis control, the output voltage u_{C+} can be assumed to be identical to the reference voltage (ignoring the switching ripple and small time delays). The boost stage output voltage variation, $\tilde{u}_{C+}(s)$, can be considered as a disturbance to $\tilde{i}_L(s)$ and therefore the focus is on analyzing $G_{d_{bki}}(s)$ in order to design the proper controller $G_c(s)$ for the constant current control. The control block diagram for inductor current control in the schematic of Figure 2.5 is illustrated in Figure 2.18, where the inductor current feedback coefficient K_{FB} is 0.2; $G_{FF}(s)$ is the low pass filter for the feed-forward voltage u_2 (voltage across the boost transistors T_2 and T_3 as shown in Figure 2.5), $K_{FF} = 1/U_{in}$ is the feed-forward coefficient, and F_M is the triangular carrier coefficient, which is the reciprocal value of the peak-to-peak amplitude of the triangular carrier of the PWM. From Figure 2.16 the small signal derivative equation of \tilde{i}_L can be written as (with $U_{in} = \text{const}$ and $U_{C+} = \text{const}$)

$$L \frac{d\tilde{i}_L}{dt} + R_{tot} \cdot \tilde{i}_L = U_{in} \tilde{d}_{bk} + U_{C+} \tilde{d}_{bt}, \quad (2.41)$$

where $R_{tot} = R_{s,i1} + R_{e1} + R_{LM} + R_{e2} + R_{s,i2}$. Since $\tilde{u}_{C+} = 0$, there should be no change in the local average output current and/or on-current through C_2 , hence we have

$$(1 - D_{bt})\tilde{i}_L - I_L \tilde{d}_{bt} = 0. \quad (2.42)$$

By combining (3.43), (3.53) and performing a Laplace transformation, the transfer function $G_{d_{bki}}(s)$ can be derived as

$$G_{d_{bki}}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}_{bk}(s)} = \frac{U_{in}}{sL + R_{tot} - \frac{U_{C+}(1 - D_{bt})}{I_L}}. \quad (2.43)$$

For most operating points, the transfer function $G_{d_{bki}}(s)$ has a pole in the right half plane, but by using feed-forward control (see Figure 2.5) the poles can be shifted to the left half plane. Here the feed-forward voltage variation $\tilde{u}_2(s)$ is

$$\tilde{u}_2(s) = (R_{e2} + R_{S,i2})\tilde{i}_L(s) - U_{C+}\tilde{d}_{bt}(s). \quad (2.44)$$

By employing the feed-forward control, as shown in Figure 2.18, the control duty cycle variation $\tilde{d}_{bk}(s)$ is changed to

$$\tilde{d}_{bk}(s) = \tilde{d}'_{bk}(s) + K_{FF}\tilde{u}_2(s), \quad (2.45)$$

where the low pass filter $G_{FF}(s)$ is considered as a unity gain since the pole frequency is higher than the current control loop bandwidth. Furthermore, combining equations (2.42), (2.43), (2.44), and (2.45) the new plant transfer function $G_{d'_{bki}}(s)$, inside the dashed frame shown in Figure 2.18, can be obtained as

$$G_{d'_{bki}}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}'_{bk}(s)} = \frac{U_{in}}{sL + R_{S,i1} + R_{e1} + R_{LM}}, \quad (2.46)$$

where we can see that the feed-forward control effectively cancels the influence of DC operating value U_{C+} on the plant transfer function.

A PI-controller with an additional pole at high frequency $G_c(s)$ is employed to compensate the system in order to guarantee a good performance of the

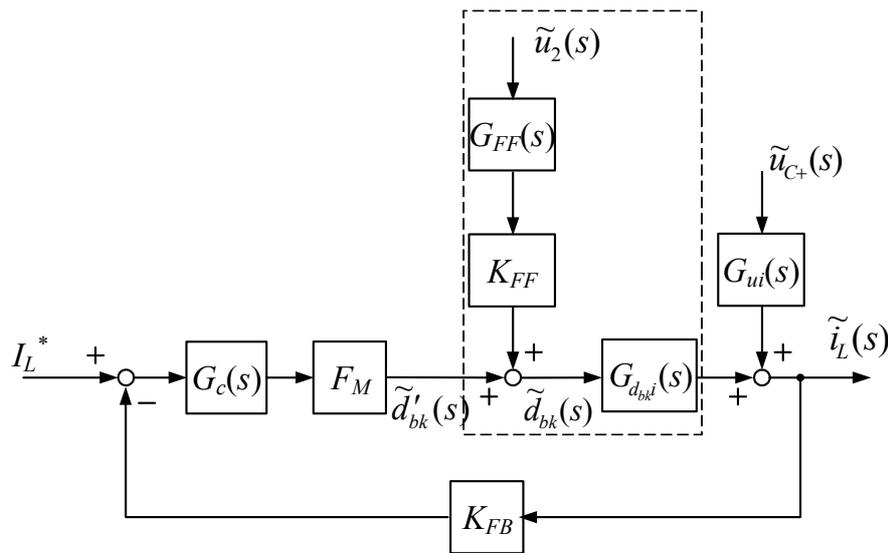


Figure 2.18: Small signal block diagram for inductor current control.

system at all operating points. The transfer function of $G_c(s)$ is

$$G_c(s) = \frac{K_p(1 + s\tau_{z1})}{s(1 + s\tau_{p1})}, \quad (2.47)$$

where $K_p = 50 \text{ A}^{-1}\cdot\text{s}^{-1}$, $\tau_{z1} = 4 \cdot 10^{-3} \text{ s}$, $\tau_{p1} = 1.6 \cdot 10^{-6} \text{ s}$. With the designed controller, the inductor current loop has a phase margin of around 70° and an overall crossover frequency of 10 kHz, which is 10% of the switching frequency, as shown in Figure 2.19.

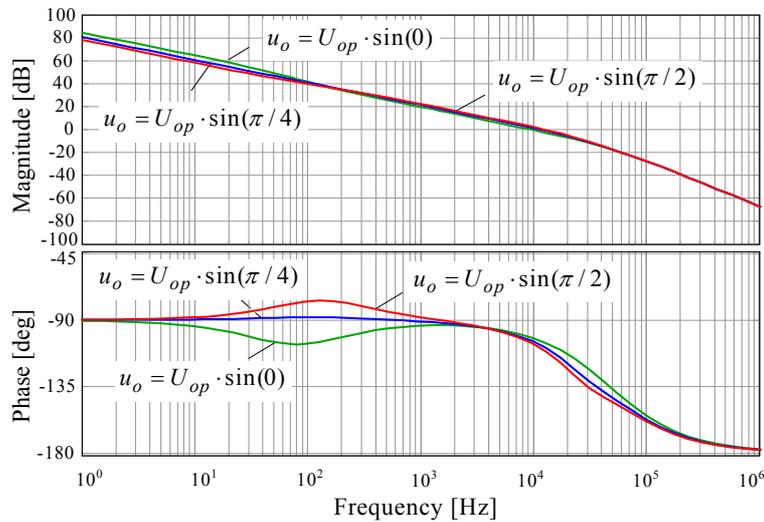


Figure 2.19: Bode plots of the compensated current loop at three typical operating points.

2.5.3 Variable Current Control

For controlling the output current I_L of the buck-stage to a constant value according to the maximum load current and the maximum charging current of the capacitors C_2 and C_3 a highly dynamic control of the linear amplifier supply voltage is achieved; however, higher conduction losses do occur.

In order to reduce the conduction losses, an inductor current control as depicted in Figure 2.20 could be employed [30]. There, the current reference value i_L^* is formed by the rectified linear amplifier load current i_o , the charging current of C_3 and/or C_4 dependent on the rate of change of the linear amplifier output voltage reference value u_o^* , and by an offset signal which guarantees a sufficient control margin. In case the duty cycle of T_2 or T_3

voltage source u_{ad} . This controlled voltage source in the frequency domain $u_{ad}(s)$ is depicted as

$$u_{ad}(s) = K_A \frac{1}{1 + s \cdot a} s \cdot L_{F1} i_{F1}(s) \quad (2.48)$$

According to

$$Z_{ad}(s) = \frac{u_{ad}(s)}{i_{F1}(s)} = K_A \frac{s \cdot L_{F1}}{1 + s \cdot a} = \frac{s \cdot a}{1 + s \cdot a} R_a, \quad (2.49)$$

this active damping scheme acts as a virtual variable impedance $Z_{ad}(s)$ in series with the inductor L_{F1} as shown in Figure 2.21 (c). This virtual impedance has a very low absolute value at low frequencies in order not to impact the DC character of the output filter and has a purely resistive behaviour with a resistance of R_a for high frequencies, which covers the natural frequency of the output filter so that a higher damping factor can be performed. Furthermore, the resistance R_a can be derived from (2.49) as

$$R_a = \frac{K_A L_{F1}}{a} \quad (2.50)$$

which shows its dependence on the parameters K_A , L_{F1} and a .

When designing the parameters of the active damping, the three main following points should be considered. First of all, the active damping must not increase the output impedance of the output filter. Secondly, a sufficient damping should be provided at natural frequency of the output filter. Lastly, the phase shift occurring in the supply voltages at output frequency caused by the active damping must be minimized. According to the three requirements above, the active damping parameters are designed to be: $R_a = 5.8 \Omega$ and $a = 1.7 \cdot 10^{-5} \text{ s}$. Figure 2.22 compares the transfer function from u_{ref} to u_o (when R_L is $5 \text{ k}\Omega$) with the case of active damping and without active damping. This figure shows that the damping of the system at the frequencies around the natural frequency of the output filter is significantly increased. For further reducing the phase shift of the supply voltages while keeping the same damping factor, a higher order filter $G_{ad}(s)$ can be applied, which can

lower the virtual variable impedance in the low frequency range. Moreover, the reason that we can not only use active damping in the output filter is that the active damping just works when the switches are operating; however, sufficient passive damping is still required when the switches are not switching in the case of very light load current.

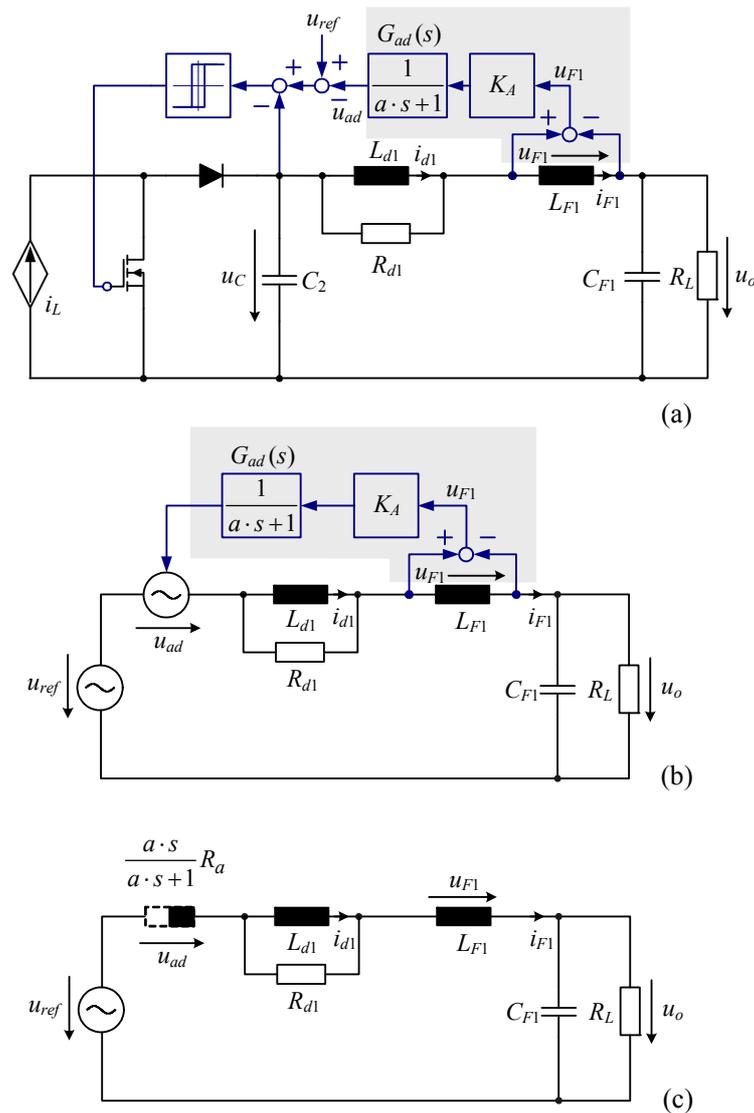


Figure 2.21: Structure for implementing active damping of the output filter (a); equivalent circuit by assuming ideal hysteresis control (b) and equivalent circuit with inserted virtual variable impedance $(a \cdot s / (a \cdot s + 1)) \cdot R_a$ to increase the system damping factor (c).

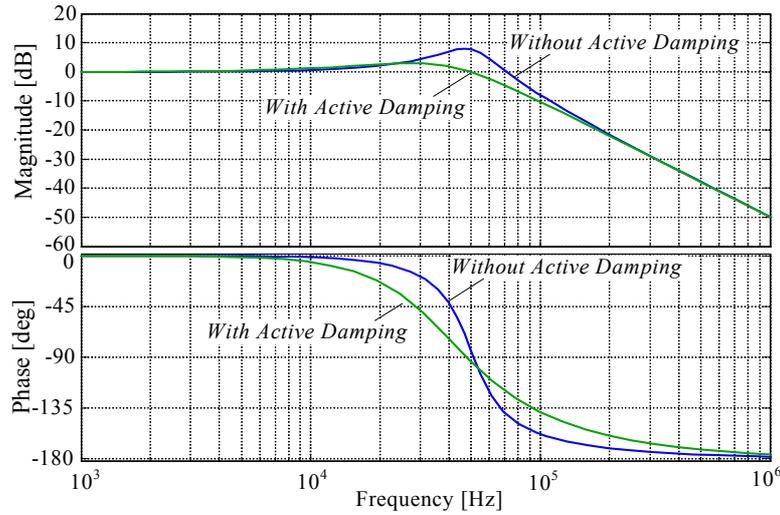


Figure 2.22: Comparison of the Bode plots of the transfer function from u_{ref} to u_o with active damping and without active damping ($R_L = 5k\Omega$).

2.6 Experimental Results

For verifying the theoretical considerations a 1.5kW prototype of the TPS shown in Figure 2.5 has been realized for feeding a 1kW LPA. The main components employed in the TPS are listed in Table 2.4.

Table 2.4: Power Components of the TPS.

Components	Denomination	Type
Input Electrolytic Capacitor	C_1	2 x 470 μ F/220VDC
CoolMOS	T_1	SPW20N60C3
Power Diode	D_1	RHRG3060
Inductor	L_1, L_2	120 μ H, 58439-A2, AWG13, 38 turns
CoolMOS	T_2, T_3	SPW47N60C3
Power Diode	D_2, D_3	ISL9R1560P2
Film Capacitor	C_2, C_3	0.47 μ F/275VAC
Output Filter Inductor	L_{F1}, L_{F2}	24 μ H, 58550-A2, AWG15, 30 turns
Damping Inductor	L_{d1}, L_{d2}	34 μ H, 58550-A2, AWG15, 37 turns
Output Filter Capacitor	C_{F1}, C_{F2}	0.33 μ F/275 VAC

The experimental results, measured from the laboratory prototype, are shown in Figure 2.23 and compared to the system performance with and without feed-forward control. It is shown that with the help of feed-forward control the shape of the inductor current I_L (Figure 2.23 b)) shows a significant improvement in the rejection of the variation of output voltage compared to the inductor current I_L without feed-forward control (Figure 2.23(a)).

Experimental results are shown in Figure 2.24 to compare the system performance without active damping (a) and with active damping (b). It is shown that the oscillations occurring in Figure 2.24(a) are no longer present in Figure 2.24 (b) due to the active damping.

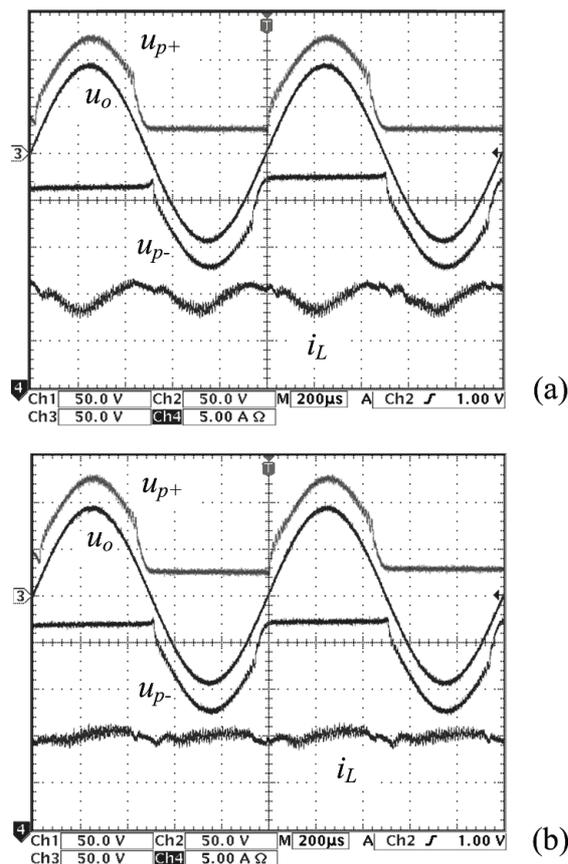


Figure 2.23: Performance comparison without feed-forward control (a) and with feed-forward control (b). Operating parameters are: $U_{in} = 100$ V, $I_L = 10$ A, $V_b = 30$ V, $U_{op} = 100$ V, $f_o = 1$ kHz, $R_L = 30$ Ω , and buck stage switching frequency $f_{bk} = 100$ kHz. Voltage scale: 50V / div; current scale: 5A / div.

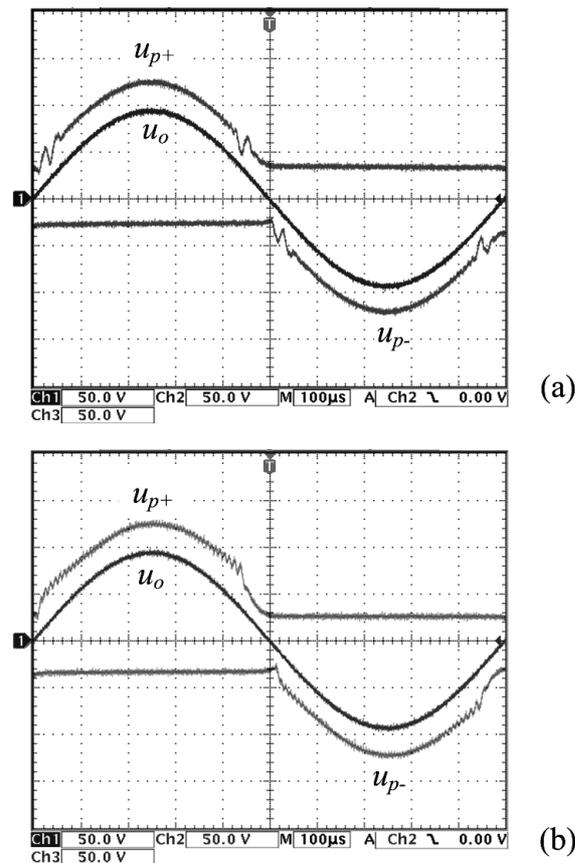


Figure 2.24: Comparison of the measured performance of the output voltages of the TPS without active damping (a) and with active damping (b). The operation parameters are: $U_{in} = 100$ V, $I_L = 10$ A, $V_b = 30$ V, $U_{op} = 100$ V, $f_o = 1$ kHz, $f_{bk} = 100$ kHz, and $R_L = 30\Omega$. Voltage scale: 50V / div.

The experimental verification has also been performed for three different loads, i.e., ohmic load ($\varphi = 0^\circ$), 16Ω , ohmic-inductive load ($\varphi = 45^\circ$), $10\Omega/2\text{mH}$ in series, and ohmic-capacitive load ($\varphi = -45^\circ$), $12\Omega/10\mu\text{F}$ in series, for nominal output voltage $U_{o,rms} = 115$ V, maximum output current $I_{op} = 10$ A and maximum output frequency $f_o = 400$ Hz. The time behaviour of the LPA supply voltages, u_{p+} and u_{p-} , and the amplifier output voltage, u_o , is shown in Figure 2.25 for ohmic and ohmic-reactive loads. As the output current of the buck input stage (see Figure 2.5) is controlled to a constant value, the LPA supply voltage can respond to variations with high dynamics. In Figure 2.25(b), it can be seen that there are discrete steps in the supply voltage when the output capacitor voltage of the upper/lower stage is charged and no-load current is supplied by the upper/lower stage. Each step duration is one switching period, therefore the active damping cannot help

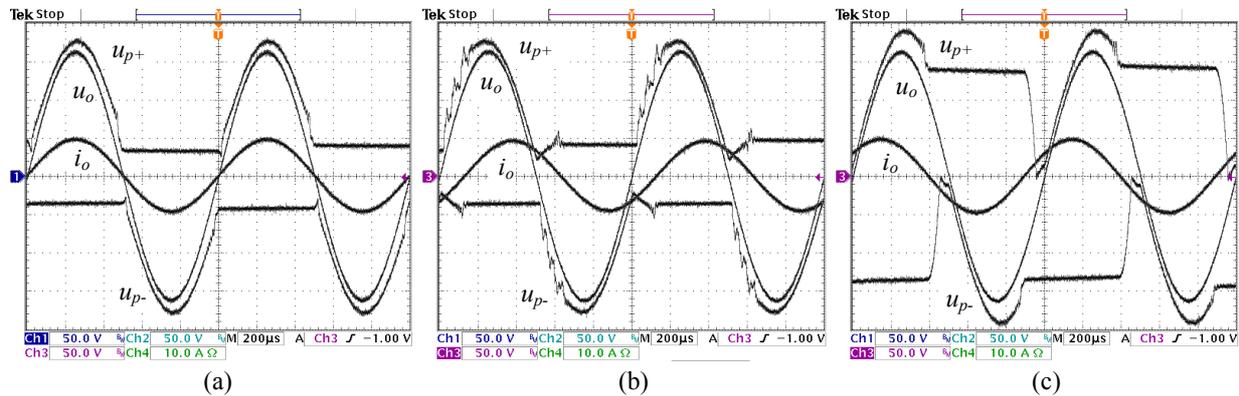


Figure 2.25: Experimental results for different loads; Operating parameters are: $U_{in} = 200$ V, $I_L = 15$ A, $V_a = 25$ V, $V_b = 25$ V, $U_{op} = 162$ V, $I_{op} = 10$ A, $f_o = 1$ kHz, $f_{bk} = 100$ kHz; ohmic load, $Z_L = R_L = 16 \Omega$ (a); inductive load, $10\Omega / 2\text{mH}$ in series (b); capacitive load, $12\Omega / 15\mu\text{F}$ in series (c). Voltage scale: $50\text{V} / \text{div}$; current scale: $10\text{A} / \text{div}$.

to reduce this ringing; however, an output filter with a higher damping factor can eliminate this ringing (see Figure 2.14(e) in [31]) but has a greater volume and losses. In case of capacitive load (see Figure 2.25(c)) the supply voltages u_{p+} and u_{p-} of the linear amplifier cannot follow the reference value because there is no current for discharging the capacitor C_2 or C_3 . However, this does not affect the losses of the LPA as the corresponding transistors do not carry load current.

The excellent transient behaviour of the system is clearly shown in Figure 2.26 where a sawtooth-shaped output signal with a slope of the trailing edge of $\approx 6\text{V}/\mu\text{s}$ is generated and the switch-mode stage adjusts the supply voltage such that some voltage margin is left and no distortion in the linear amplifier output signal occurs.

Figure 2.27 compares the power losses and efficiencies of the proposed TPS + LPA system and of a class-AB LPA. The testing conditions are that both systems output 400 Hz, and 10 A peak value sinusoidal currents over the full range of the specified output voltage. The efficiencies and power losses of the class-AB LPA supplied by constant voltages are calculated by using (2.4) and are not measured from the hardware, since the maximum allowed power dissipation of the experimental LPA is only 280W. However, it has been verified that the calculation results of (2.4) closely match the measured results of the experimental LPA operating at lower power levels. It is shown in Figure 2.27 that the proposed TPS + LPA system has an overall

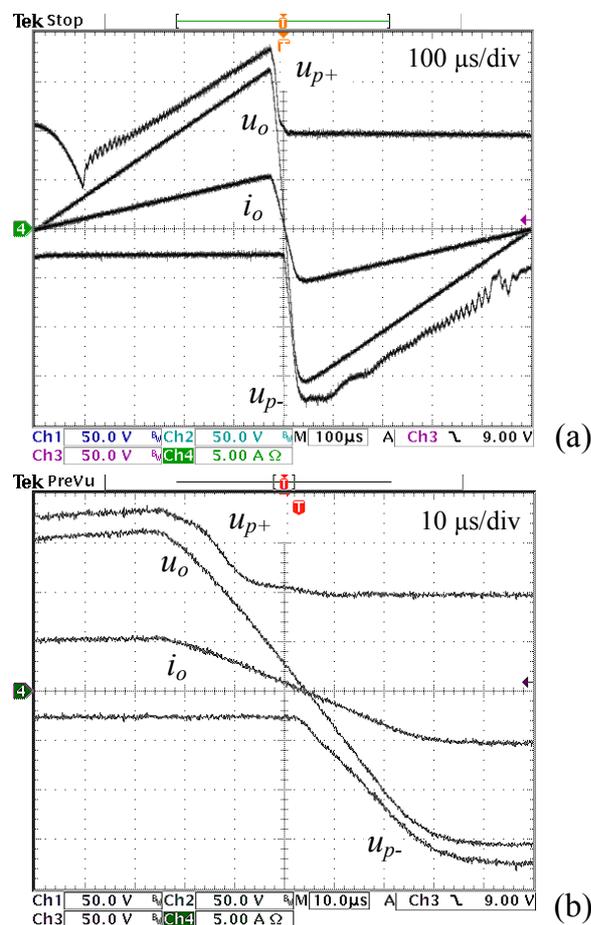


Figure 2.26: Experimental results for generating a sawtooth-shaped 1kHz linear amplifier output u_o ; ratio of rise-time to fall time is 19:1; (a) waveforms for one output period, (b) zoom in at the falling edge of the output voltage. Operating parameters are: $U_{in} = 200$ V, $I_L = 15$ A, $V_a = 25$ V, $V_b = 25$ V, $U_{op} = 162$ V, and $R_L = 30$ Ω . Voltage scale: 50V / div; current scale: 5A / div.

higher efficiency compared to the conventional class-AB LPA in the full output voltage range. The power losses reduction advantage for the proposed system is most obvious when generating lower output voltages. There, the full output current capacity is available, while conventional class-AB LPAs often require downgrading their output current capacity in the lower voltage region because of the dramatically increased power losses as illustrated in Figure 2.27. Furthermore, the calculated efficiencies of the proposed system have good matching with the measured results (maximum difference of 2.5% at $U_{o,rms} = 98$ V).

The power losses distribution of the proposed TPS + LPA system at maximum output power is demonstrated in Figure 2.28, where TPS and LPA each

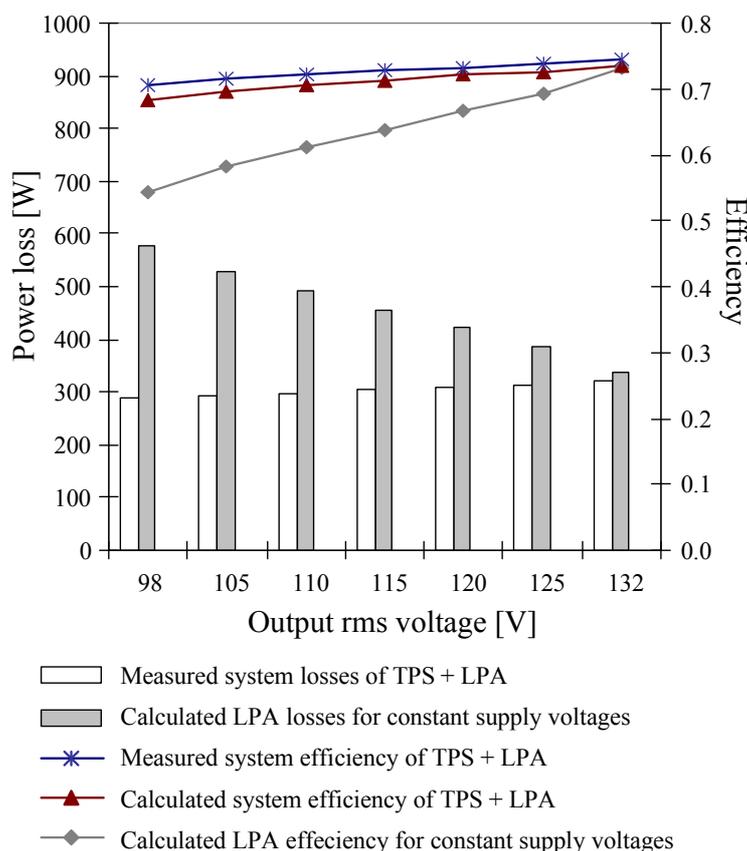


Figure 2.27: Power loss and efficiency comparison of the proposed system, TPS + LPA, and the LPA with constant supply voltages. Operation parameters of TPS + LPA are: $U_{in} = 200$ V, $I_L = 15$ A, $V_a = 25$ V, $V_b = 25$ V, $I_{op} = 10$ A, $f_o = 400$ Hz, $f_{bk} = 100$ kHz, while the operation parameters of LPA with constant supply voltages are: $V_{CC} = \pm 200$ V, $I_{op} = 10$ A, $f_o = 400$ Hz.

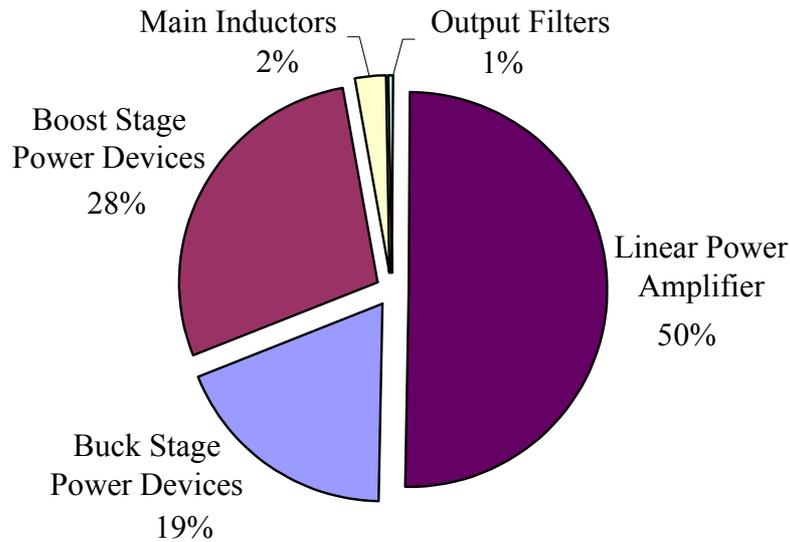


Figure 2.28: Calculated power loss distribution of the proposed TPS + LPA system at maximum output power. The operation parameters of TPS + LPA are: $U_{in} = 200$ V, $I_L = 15$ A, $V_a = 25$ V, $V_b = 25$ V, $U_{o,rms} = 132$ V, $I_{op} = 10$ A, $f_o = 400$ Hz, $f_{bk} = 100$ kHz.

produces about 50% of the total system losses. Here the efficiency of the TPS stage is relatively low (about 87%) due to the high current stresses on the components and hard switching of the MOSFETs. However, the current stresses on the components can be reduced by applying the variable current control scheme proposed in [31] and the hard switching losses could be lowered by employing soft switching techniques.

2.7 Conclusions

A new TPS topology for conditioning the supply voltages of a LPA has been proposed which reduces the voltage drops across the linear amplifier power transistors to low values and therefore considerably lowers the amplifier power losses. This proposed boost-type TPS has some major advantages over the existing buck-type tracking power supplies, such as no requirement for dc bus voltage higher than the output voltage, small output filter and high output voltage dynamic. These benefits make the boost-type TPS more suitable for high output voltage applications, e.g., testing power sources.

However, the maximum output current is limited by the constant inductor current value.

In this chapter, the theoretical calculations demonstrate that the power transistor losses in the LPA are significantly reduced when employing variable supply voltages. The current stresses on the power semiconductors of the proposed system are calculated analytically. The output filter is implemented and dimensioned according to the PSRR of the LPA to ensure a high output voltage quality of the system. Furthermore, the small signal model of the TPS is derived, and based on this model the constant current loop and feed-forward control are designed to insure that the inductor current remains constant even when the output power is varying at high frequency. An active damping strategy for the output filter which is easy to implement is designed. As an example for the testing application of single-phase aircraft equipment, a 1kW laboratory prototype including TPS and LPA is built to verify the theoretical analysis. The experimental system shows a clear system efficiency improvement compared to a conventional class-AB LPA and a high output voltage dynamic $6\text{V}/\mu\text{s}$ is achieved. As a result, the proposed system is applicable for linear amplifiers generating large amplitude output signals in the kHz range.

In the course of further research the experimental hardware could be extended to the topology shown in Figure 2.2(b), i.e. an isolated three-level buck-type dc-dc converter could be employed as input stage. The output filter could be substituted by a higher order circuit in order to reduce the supply voltage phase shift when outputting a high frequency signal. Furthermore, the adaptive current control scheme depicted in Figure 2.11 [31] could be implemented in order to further reduce the system losses. When the TPS+LPA system is used to perform specific equipment testing, where the output voltage waveform shape is known, it is possible to lower the system losses by pre-shaping the inductor current. Therefore, we could calculate the required inductor current reference such that the inductor current can ramp up to a high current level before the load requires the high current. In this way, we could lower the inductor current slew rate requirement and reduce the system losses.

The proposed TPS+LPA system has shown an obvious system losses reduction over the conventional class-AB LPA in high output voltage applications (see Figure 2.27). The other future option for this application is to use pure switching mode power amplifiers. By employing advanced semiconductor devices, e.g. SiC schottky diodes in combination with superjunction silicon MOSFETs, to increase the switching frequency or applying interleaving and/or multi-level methods to increase the equivalent switching frequency, it is possible to realize a high bandwidth, high voltage power amplifier of similar performance.

Chapter 3.

Hybrid Multi-Cell Amplifier

In this chapter, a multi-cell cascaded power amplifier, which belongs to hybrid Type II, with a high output voltage capability, wide load range and high bandwidth is presented. The cascaded power amplifier is formed by combining a low-voltage linear power amplifier in series with multiple inverter cells. A high output voltage and bandwidth is achievable by using very simple modulation and feedback control design. The dc voltages for the inverter cells and linear power amplifier are provided by an isolated, bidirectional dc-dc resonant converter. Finally the measurements for the compact prototype verify the theoretical analysis of the amplifier.

3.1 Introduction

As described in Chapter 2, we employ a boost-type TPS with an adjustable output voltage to replace the constant DC power supply for a conventional class-AB power amplifier. The supply voltages can then be modulated according to the required instantaneous output voltage, so that the voltage drop across the output power transistors can be significantly reduced, resulting in a power loss reduction [48]-[49]. However, a low pass filter is still necessary between the power supply and the linear power amplifier to re-

duce the switching noise in the output voltage of the linear power amplifier and this limits the total system's dynamic performance. Furthermore, the linear power amplifier should deliver the full output power and sustain the full output voltage stress. This makes it difficult to design the linear power amplifier for mains simulation applications, especially those that require $\pm 400\text{V}$ for generating a single phase system. In [19]-[27] various switch-mode assisted linear power amplifiers are presented that are basically a class-D converter connected in parallel with a linear power amplifier. The switch-mode amplifier contributes the main load current and the linear amplifier generates the difference current. With this topology a relatively small current is flowing through the linear power amplifier so that the losses can be significantly reduced and the output impedance is defined by the linear power amplifier stage. However, a high voltage linear power amplifier is still required for a mains simulation application and switching noise can appear in the output voltage due to the increased output impedance of the linear power amplifier at high frequencies.

A "Quasi-Linear Amplifier" topology has been proposed in [18] and is similar to the topology presented in this chapter. The "Quasi-Linear Amplifier" consists of low switching frequency inverters connected in series with a linear power amplifier to generate gradient coil currents with fast ramp time for magnetic resonance imaging (MRI) systems. However this "Quasi-Linear Amplifier" acts as a current source, while the topology in this chapter operates as a voltage source that has very low output impedance and includes an isolation stage.

The topology of the multi-cell cascaded power amplifier is shown in Figure 3.1(a), and consist of: (i) a high slew rate linear power amplifier, (ii) a multi-cell inverter, which is connected in series with the linear power amplifier to generate the output voltage, (iii) a bidirectional, multi-output, isolated dc-dc converter that provides the dc voltages for the cell units and the linear power amplifier and allows bidirectional energy flow in the case of non-resistive loads. The multi-cell cascaded power amplifier has the advantages of a high bandwidth, high efficiency, no output filter, and utilizes a low voltage commercial linear power amplifier. The representative waveforms

of a 10-cell cascaded power amplifier are shown in Figure 3.1(b), where the multi-cell inverter generates the stepped high voltage u_{mo} according to the reference output voltage u_o^* and the switching frequency of the cells is low. Furthermore, the output voltage of the linear power amplifier u_{la} is regulated to compensate for the small voltage difference between u_{mo} and u_o . Therefore, a low voltage linear power amplifier can be employed. The grey area between $u_{mo} - U_a$ and $u_{mo} + U_a$ is the voltage range that can be achieved by the multi-cell cascaded power amplifier for the reference voltage u_o^* .

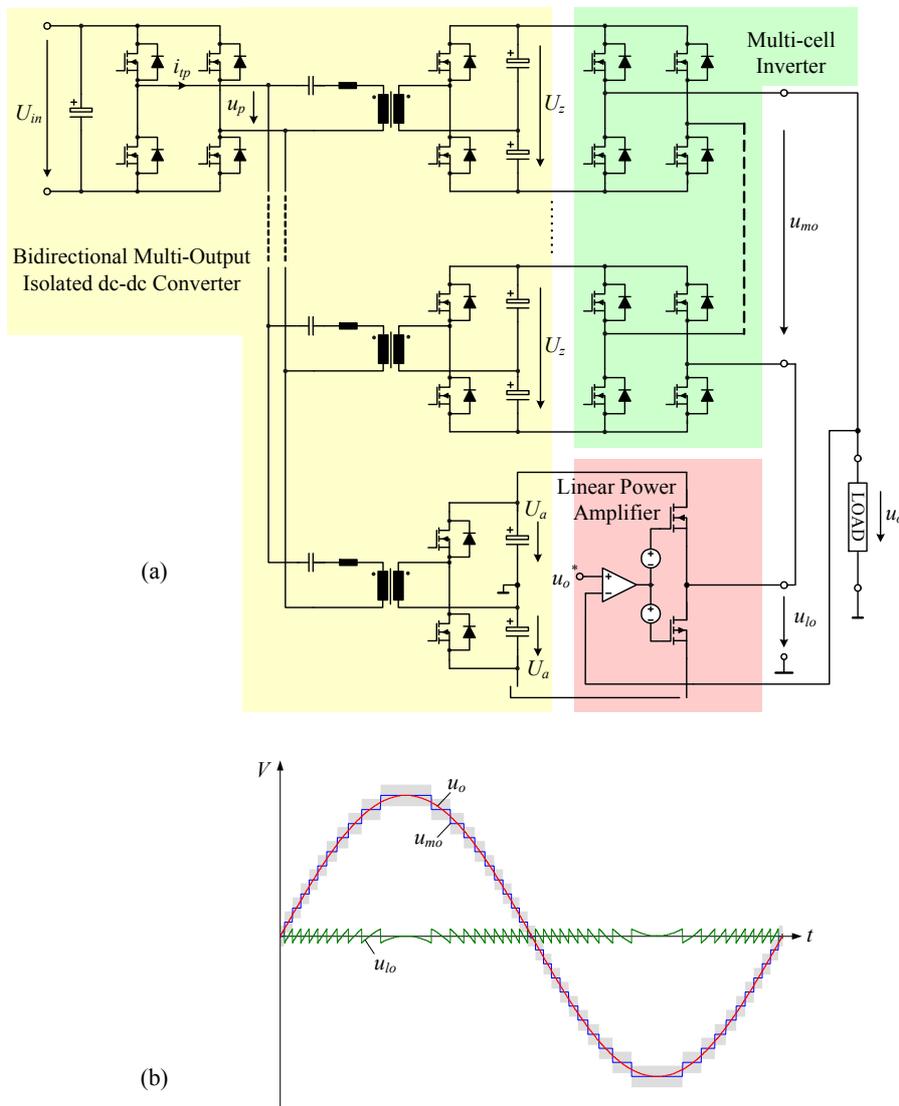


Figure 3.1: Topology of an isolated multi-cell cascaded power amplifier (a) and representative waveforms of the output voltage u_o , multi-cell output voltage u_{mo} and linear power amplifier output voltage u_{lo} of a 10-cell cascaded power amplifier (b).

3.2 Operating Principle

3.2.1 Modulation and Control

The control scheme of a simplified two-cell cascaded power amplifier is shown in Figure 3.2. Here two H-bridges are connected in series with the linear power amplifier to form the output voltage. The H-bridge units are controlled in an open loop manner and each H-bridge cell can output three possible voltage, U_z , $0V$ and $-U_z$, where U_z is the DC supply voltage of the cell units. The different switching states for generating these three different output voltages levels are shown in Figure 3.3. The linear power amplifier is operated in a closed loop with a high bandwidth, so that it can compensate for the voltage difference between output voltage u_o and multi-cell voltage u_{mo} .

The control signals of the H-bridge units are directly generated by comparing the reference output voltage u_o^* and step voltages $-3/2U_z$, $-1/2U_z$, $+1/2U_z$ and $+3/2U_z$. For instance the output voltage of unit 1 is $0V$, i.e., T_3

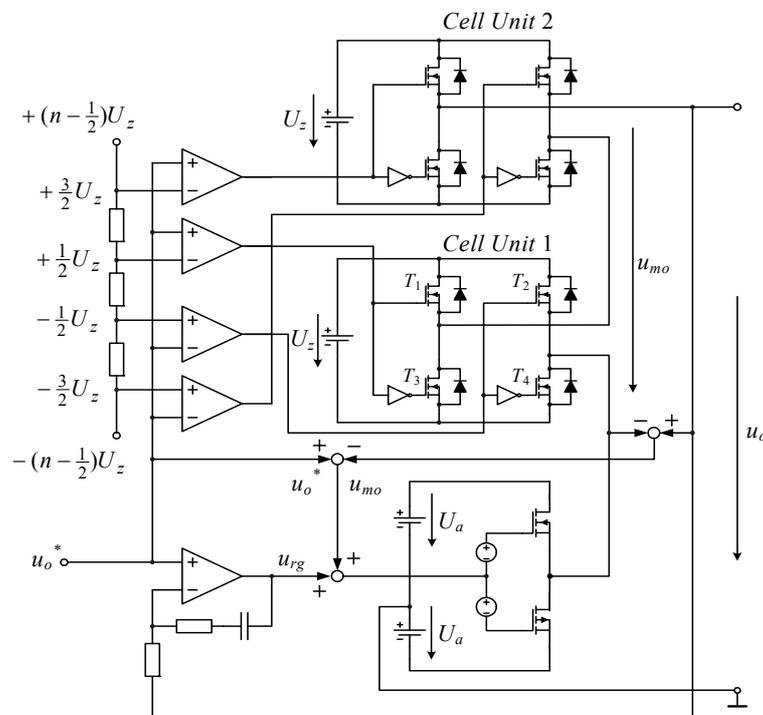


Figure 3.2: Control scheme of two-cell cascaded power amplifier.

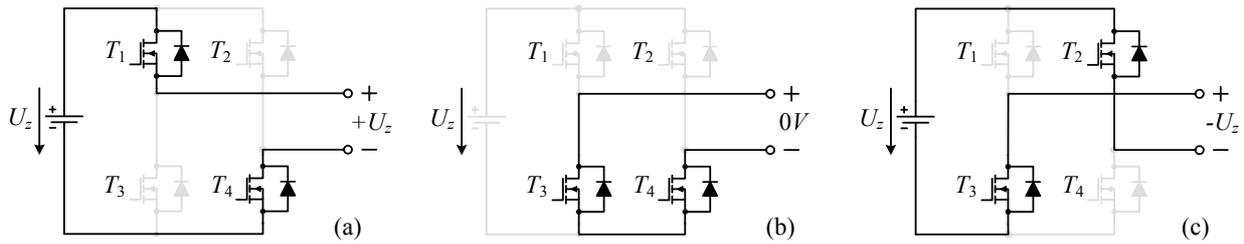


Figure 3.3: Three different possible cell output voltage states: $+U_z$ (a), 0 V (b), and $-U_z$ (c).

and T_4 are on, when u_o^* is between $-1/2U_z$ and $+1/2U_z$. If u_o^* increases and reaches $+1/2U_z$, T_3 is turned off and T_1 is turned on, thus unit 1 outputs $+U_z$. Alternatively, unit 1 will produce an output voltage $-U_z$ when u_o^* decreases and reaches $-1/2U_z$. The total multi-cell voltage u_{mo} is dependent on the reference output voltage u_o^* as is demonstrated in Figure 3.4. Furthermore this topology can be easily expanded to an n-cell cascaded power amplifier with very low effort.

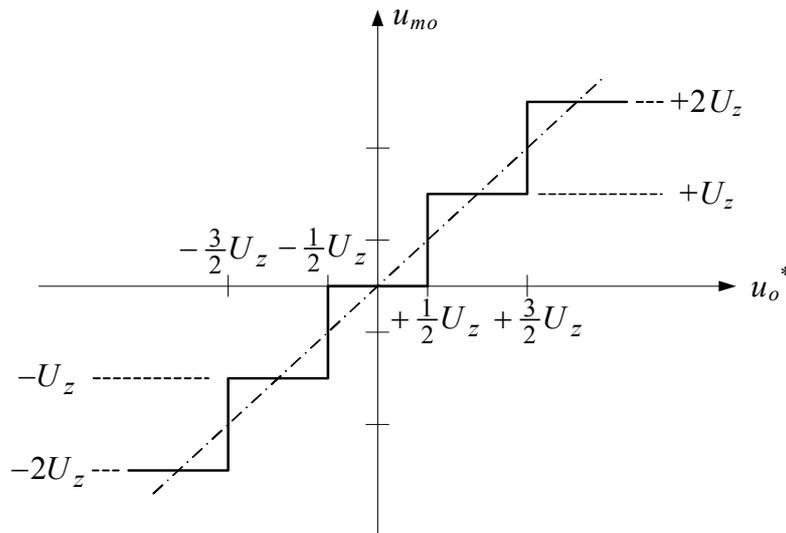


Figure 3.4: Multi-cell voltage u_{mo} in dependency on the reference output voltage u_o^* .

In Figure 3.2, the DC voltage of the linear power amplifier U_a is required to be higher than $1/2U_z$ in order to have sufficient voltage regulation margin. The system just uses a single voltage loop control and the control signal of the linear power amplifier is formed by summing the feed forward voltage $u_o^* - u_{mo}$ and the output of the voltage regulator u_{rg} .

3.2.2 Slew Rate Limit

It must be pointed out that the output voltage slew rate of the linear power amplifier needs to be high enough to compensate for the voltage slope during the rising or falling steps produced by the multi-cell inverter. Therefore, a slew rate control must be applied to the gate driver of the MOSFETs in the inverter cells.

As the switching voltage dv/dt is determined by the miller capacitance and gate driver current. Consequently the dv/dt can be limited either by increasing the gate resistance or by adding an external miller capacitor. Since increasing the gate resistance will result in significant switching delays, the simple way to limit the switching slew rate is to add an external capacitor connected between gate and drain. E.g., to limit the slew rate of the high side MOSFET, an external capacitor C_M in parallel with the intrinsic capacitor C_{gd} is employed as shown in Figure 3.5(a). It is shown in Figure 3.5(b) that the theoretical output voltage of the multi-cell inverter u_{mo} is ramping up with a limited dv/dt .

However, the resulting drawback of adding C_M is worsening the shoot-through and/or cross conduction problem which is a well known phenomenon occurring often in half bridge configuration [55]. This happens under the circumstances that the off-state switch is momentarily turned on by the high dv/dt when the other switch in the same leg is turned on. Since the drain-to-gate capacitance is increased, the crossing current $(C_M + C_{gd})dv/dt$ is therefore enlarged which can cause the off-state switch gate voltage to exceed the turn-on threshold voltage. This shoot-through can increase the switching losses, or even lead to a failure of the semiconductor because of the overload current. Typically a negative off-state gate voltage is used to prevent shoot-through. In [60], an active miller clamp circuit is implemented to prevent this problem which provides a low impedance path from the gate to source of the off-state switch when the other switch in the same leg is turned on.

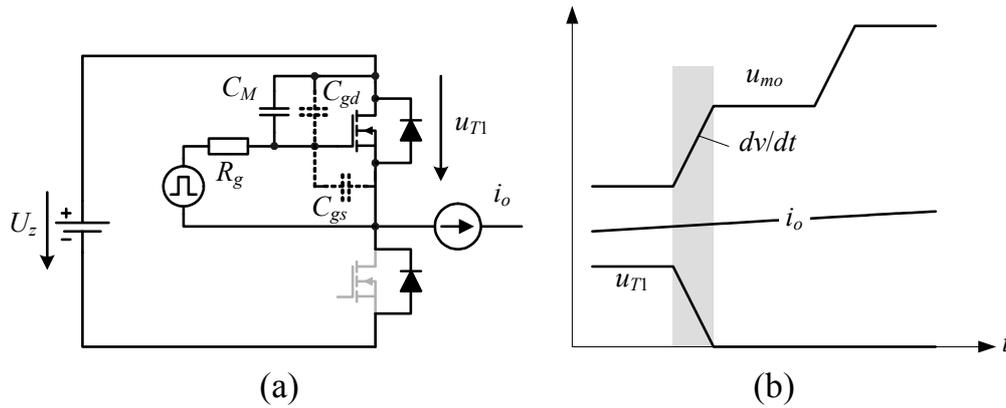


Figure 3.5: Scheme of gate driver for controlling the turn-on slew rate of high side MOSFET (a) and the key waveforms of a cell unit when it's output changes from 0V to $+U_z$.

In order to analyse the condition to avoid the shoot-through in the case of adding external miller capacitors to the MOSFETs, the circuit schematic of a bridge leg of an inverter cell is demonstrated in Figure 3.6. There U_H is the high voltage level of the gate voltages, U_L is the low voltage level of the gate voltages, R_{on} is the turn-on gate resistor, R_{off} is the turn-off gate resistor, C_{gd} is the intrinsic gate-to-drain capacitor, and C_{gs} is the intrinsic gate-to-source capacitor.

For limiting both the turn-on and turn-off slew rate to be SR, the turn-on and turn-off resistors should be selected as

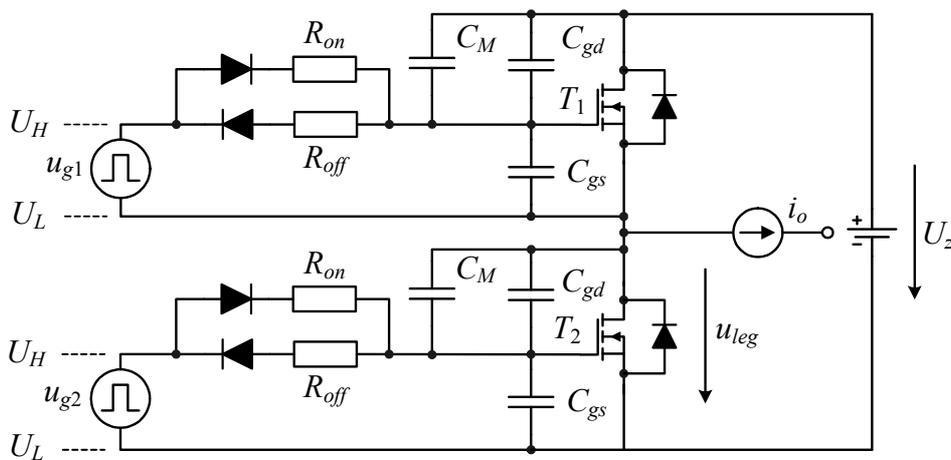


Figure 3.6: Circuit scheme of a bridge leg of an inverter cell that uses an external miller capacitor C_M for each MOSFET to limit the slew rate of switching voltages.

$$R_{on} = \frac{U_H - U_M}{SR \cdot (C_M + C_{gd})} \quad (3.1)$$

and

$$R_{off} = \frac{U_M - U_L}{SR \cdot (C_M + C_{gd})}, \quad (3.2)$$

where SR is the limited slew rate of the drain-to-source voltages and U_M is defined as the miller voltage value. In order to prevent the shoot-through, the voltage across the R_{off} in parallel with C_{gs} caused by the step current $SR(C_M + C_{gd})$ during the time period $T_{SR} = U_z / SR$ should not exceed the threshold voltage U_{th} , as given below

$$(U_M - U_L) \left(1 - e^{-\frac{1}{R_{off}C_{gs}}T_{SR}} \right) < U_{th} - U_L. \quad (3.3)$$

Combining (3.2) and (3.3), we find that the required capacitance C_{gs} should fulfil the following condition,

$$C_{gs} > \frac{U_z(C_M + C_{gd})}{U_M - U_L} \cdot \frac{1}{\ln \frac{U_M - U_L}{U_M - U_{th}}}. \quad (3.4)$$

For the aforementioned analysis, the conditions to avoid the shoot-through are:

- Add an external capacitor between the gate and source of the MOS-FETs so that the total gate-to-source capacitance can fulfil the criteria defined in (3.4).
- Use negative gate supply voltages to lower the required value for the external gate-to-source capacitor.

However, there are some significant disadvantages of this simple implementation for limiting the slew rate. The switching delay time is increased because of the required external gate-to-source capacitor which can impair the system bandwidth. Extra circuits have to be implemented in the gate circuit

Table 3.1: Output voltage delay or distortion of a bridge leg in dependency on the switching state and the direction of i_o .

	Level "1" ($T_2 \rightarrow \text{off}, T_1 \rightarrow \text{on}$)	Level "0" ($T_1 \rightarrow \text{off}, T_2 \rightarrow \text{on}$)
$i_o > 0$	Dead time delay Diode reverse recovery	No dead time delay No diode reverse recovery
$i_o < 0$	No dead time delay No diode reverse recovery	Dead time delay Diode reverse recovery

to reduce the turn-on and turn-off delays, e.g., a small resistor in series with a Zener diode network. Furthermore, the interlock delay time has to be set longer than T_{SR} , which can cause a long time delay in the cell output voltage under some circumstances. As mentioned before, each bridge leg can generate two voltage levels: U_z (level "1") and 0V (level "0"), and the current i_o might have a positive or negative direction; hence there are four different possible switching situations for each leg as listed in Table 3.1. This implementation has problems with dead time delay and diode reverse recovery at the specific situations when u_{leg} changes to U_z in the case of $i_o > 0$ and u_{leg} changes to 0V in the case of $i_o < 0$. Let us take the latter case as an example to explain the problems. At first the gate signal is set to U_L and therefore T_1 is turned off, but u_{leg} is still U_z because the i_o flows through the body diode of T_1 . Then T_2 is turned on, u_{leg} has a voltage jump with ringing because of the current commutation from the body diode of T_1 to T_2 . After that, u_{leg} rises with the limited slew rate. The voltage spikes caused by the reverse recovery behaviour of the body diode would be impossible for LPA to compensate.

There are also other active circuits which can limit or control the switching slew rate. Figure 3.7 shows a collection of different implementations for turn-off dv/dt limit or control from the literature, and turn-off dv/dt limit or control can be realized in similar ways. They are used typically for connecting IGBTs in series, for reduction of overshoot voltages, or lessening EMI. In [56], a closed-loop control is implemented which uses u_{ds} as the feedback signal, therefore u_{ds} is controlled to follow the reference voltage that defines the switching slew rate, as shown in Figure 3.7(a). This requires careful con-

trol loop design in order to guarantee the high loop bandwidth and system stability [57]. Another method is to feed forward the differentiated value of u_{ds} by using an external capacitor C_M of some picofarads [58], as shown in Figure 3.7(b). The advantage of this method in contrast to the conventional method of increasing gate resistance is that it does not increase the gate resistance; therefore it is still possible to charge and discharge the gate very fast. In some applications which require the flexibility to adjust the slew rate in order to find the compromised slew rate concerning switching losses and complying to the EMC standard [59]. A controllable current source is implemented to electronically adjust the Miller capacitance C_M , as illustrated in Figure 3.7(c). However, this method needs two individual circuits to control the turn-on and turn-off slew rates since two current sources with different directions are required. In Figure 3.7(d) a two-level active gate voltage control circuit is implemented that senses the differentiated value of u_{ds} as a trigger signal to determine the gate voltage level, i.e., to set the gate voltage to a lower level when the u_{ds} is rising [60]-[61].

These circuits can achieve the switching voltages slew rate limitation without having the problem of increased switching delay time. However they are much more complex to implement with discrete components, especially implementing the slew rate limit for thirty six MOSFETs of the proposed system. Furthermore, in order to limit the reverse recovery voltage in some situations (see Table 3.1), di/dt limit circuits have to be implemented for each MOSFETs, which even further increases the system complexity.

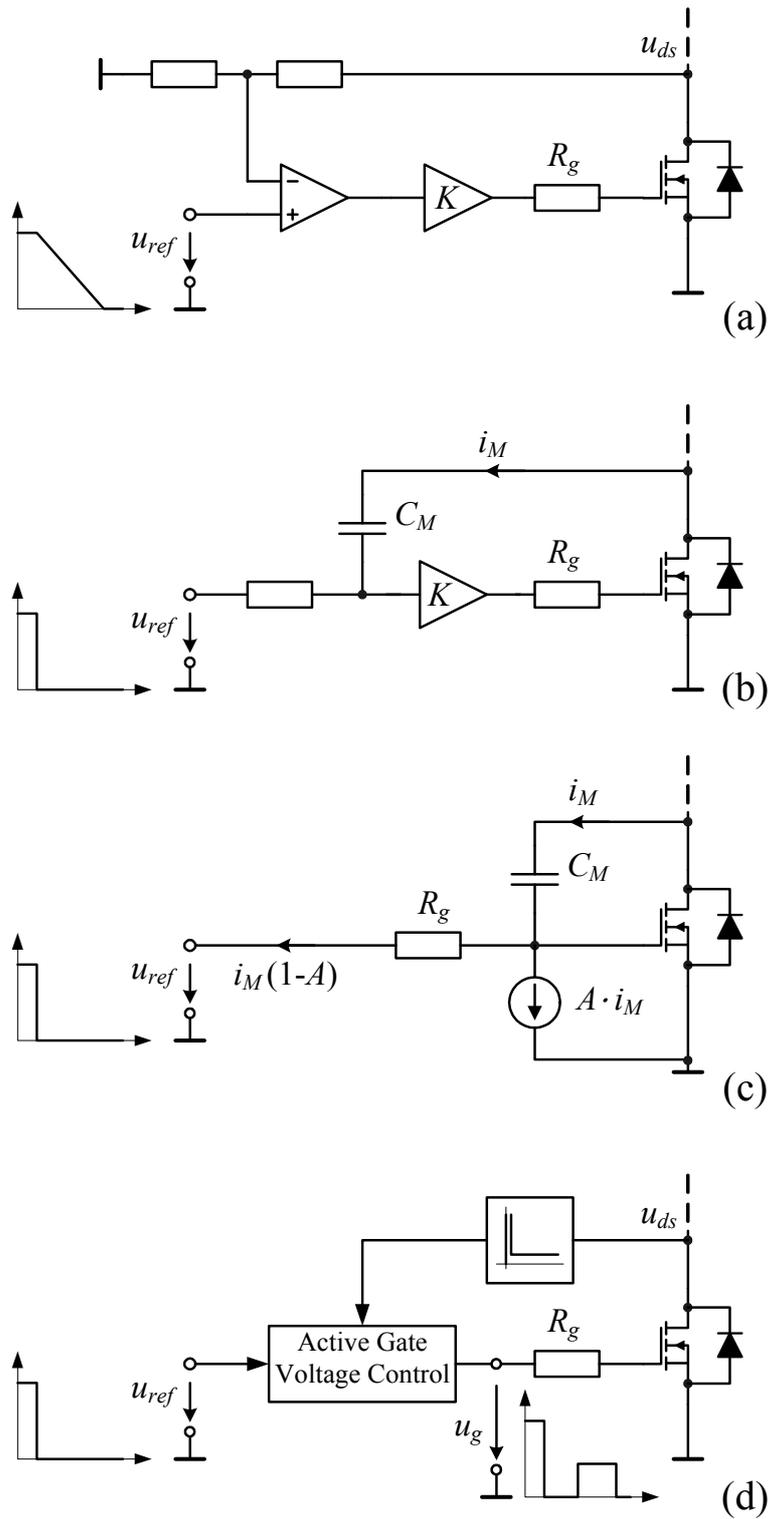


Figure 3.7: Collection of different implementations for turn-off dv/dt limit or control. Use the gate reference voltage with a certain slew rate and negative feedback of u_{ds} (a), feedback of the differentiated value of u_{ds} and use a high current amplifier (b), flexible dv/dt control by electronically adjusting C_M (c), and two-level active gate voltage control (d).

For simplicity of the system, a simple LC filter with a LR damping network is used to limit the dv/dt of the inverter cell output voltage, as shown in Figure 3.8. Since all nine inverter cells are connected in series, only one dv/dt limit filter is needed for the complete system. There is an approximation between the 10%-90% rise time t_r and the corner frequency f_n for a second-order system, which is [62]

$$t_r = \frac{0.286}{f_n}. \quad (3.5)$$

In this system the slew rate limit is set to 15 V/ μ s, and then f_n is calculated as

$$f_n = \frac{0.29}{\frac{U_z(0.9 - 0.1)}{SR}} = \frac{0.286}{\frac{40 \text{ V}(0.9 - 0.1)}{15 \text{ V}/\mu\text{s}}} = 134 \text{ kHz}. \quad (3.6)$$

As seen in Figure 3.8 C_F has to sustain the full amplitude of u_o and we have to limit the current i_{CF} flowing through C_F because i_{LF} carries the sum of i_{CF} and i_o . Here a practical choice is to limit the peak current $I_{CF,pk}$ to 50% of the output peak current I_{op} in the case of the system operating at the maximum frequency. Thus the limitation of C_F is written as

$$C_F < \frac{0.5I_{op}}{2\pi f_{o,max}U_{op}} = \frac{0.5}{2\pi f_{o,max}R_L} = \frac{0.5}{2\pi \cdot 5 \cdot 10^3 \text{ Hz} \cdot 70\Omega} \quad (3.7)$$

$$= 225 \text{ nF}.$$

Also considering that the output impedance of the filter must be low enough compared to the load impedance and the filter must have sufficient damping for the no-load situation, the parameters of the dv/dt filter are designed to be

$$C_F = 220 \text{ nF}, L_F = 6.8 \mu\text{H}, L_d = 66 \mu\text{H}, R_d = 6 \Omega. \quad (3.8)$$

In order to check the design results, the frequency response of the input-to-output voltage transfer ratio and step response for $R_L = 70 \Omega$ and $R_L = \infty$ are shown in Figure 3.9 and Figure 3.10 respectively. For the step responses,

the dv/dt of the rising area are $14.7 \text{ V}/\mu\text{s}$ for $R_L = 70 \Omega$ and $15.7 \text{ V}/\mu\text{s}$ for $R_L = \infty$ in the case that the cell dc voltage $U_z = 40 \text{ V}$. Maximum overshoot for the no-load case is 23%, which is inside the voltage area where the LPA is able to compensate the voltage difference. And the frequency responses of the input-to-output voltage transfer ratio for the nominal load impedance of 70Ω but with different phase angle of 0° , 45° and -45° are also shown in Figure 3.11, where the peak amplitude for the inductive load $\varphi = 45^\circ$ is only 0.5dB higher than the one for the resistive load.

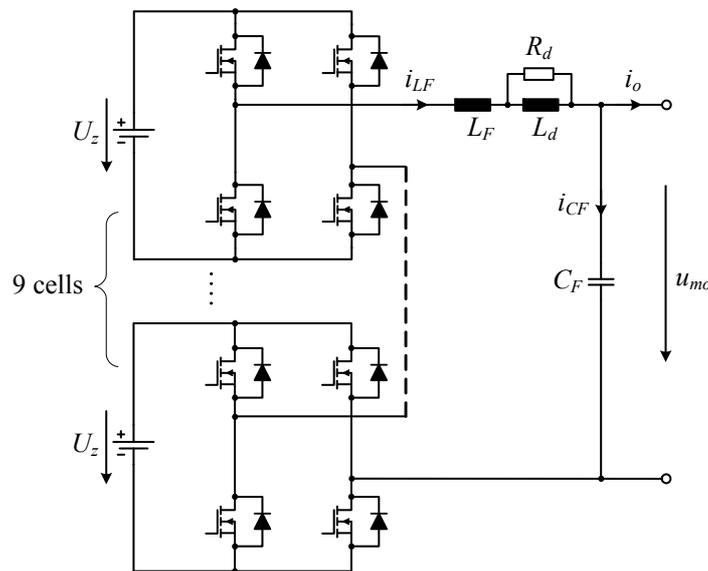


Figure 3.8: Employment of a simple LC filter with a LR damping network to limit the dv/dt of the inverter cell output voltage. The filter parameters are: $L_F = 6.8 \mu\text{H}$, $L_d = 66 \mu\text{H}$, $R_d = 6 \Omega$, and $C_F = 220 \text{ nF}$.

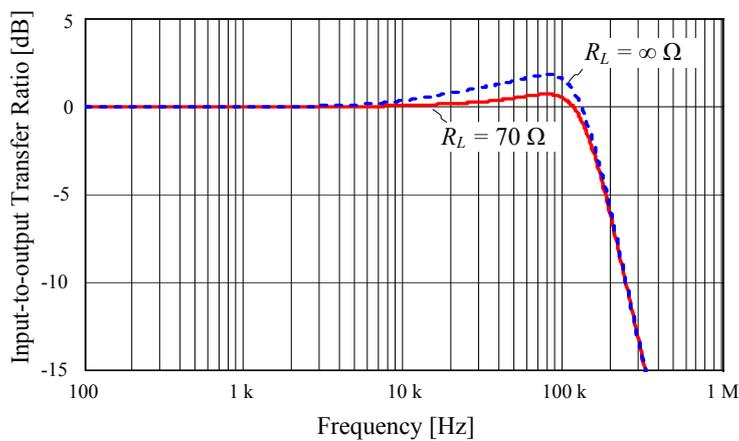


Figure 3.9: Comparison of the frequency response of the input-to-output voltage transfer ratio for $R_L = 70 \Omega$ and $R_L = \infty$.

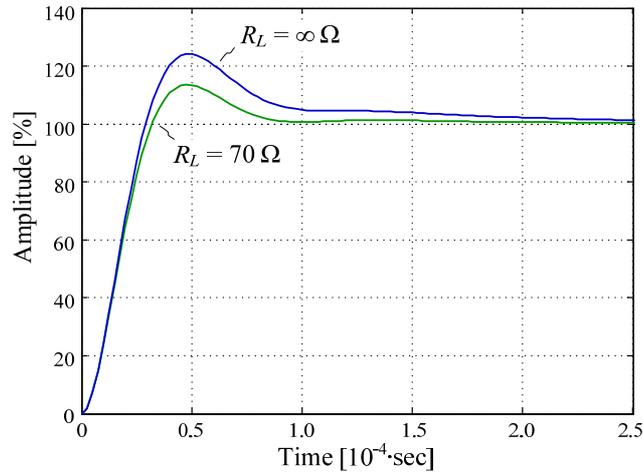


Figure 3.10: Step response of the dv/dt limit filter for nominal load 70Ω and no-load situations.

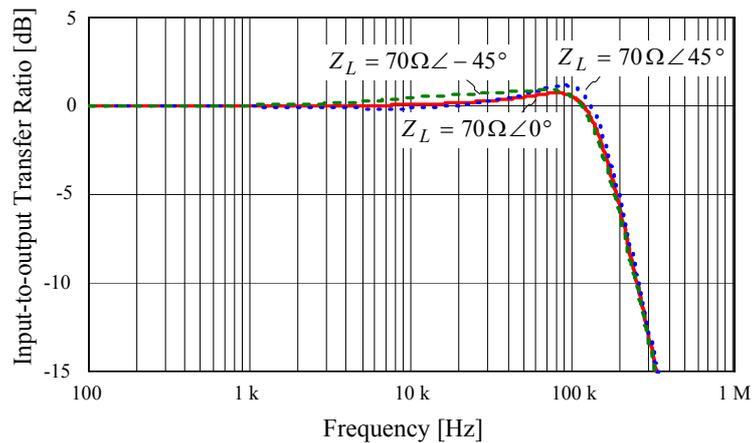


Figure 3.11: Comparison of the frequency response of the input-to-output voltage transfer ratio for the nominal load impedance of 70Ω but with different phase angles of 0° , 45° and -45° .

3.3 Uncontrolled Bidirectional dc-dc Converter

A mains simulator requires electrical isolation and bi-directional power flow in the case where reactive power is required at the output. Therefore, an isolated bi-directional dc-dc converter has to be used to provide the DC voltages for the H-bridge units and linear power amplifier. In order to reduce the complexity of the circuit, an uncontrolled bi-directional multi-output dc-dc converter is employed (see Figure 3.1). An H-bridge is utilized

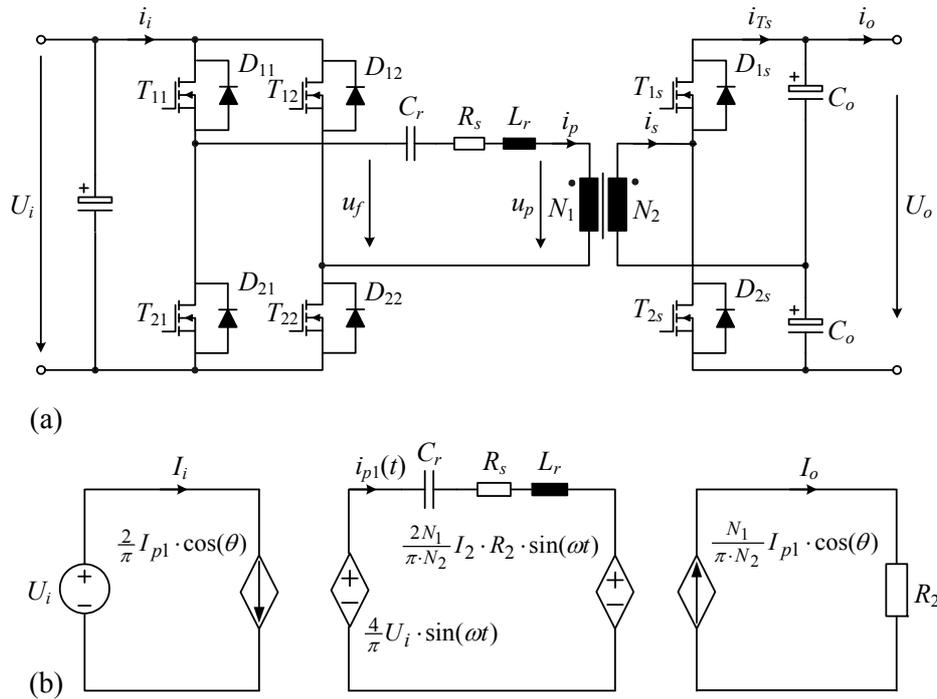


Figure 3.12: Topology of the uncontrolled bi-directional dc-dc converter (a) and corresponding steady-state equivalent circuit (b).

as a common input stage, and an individual transformer, LC tank and half bridge rectifier are used for each output stage. It is also possible to use a single transformer with multiple secondary windings to further simplify the system; however this can cause current oscillations between the different cell units in case they operate at different power levels. Moreover, this results in higher losses and makes the system inflexible when the number of the cells is to be extended.

The topology of a single output, bi-directional dc-dc converter is shown in Figure 3.12(a) [51]-[53], where synchronized 50% fixed duty cycle control is used for both the primary side H-bridge and secondary side half bridge. With this operation the converter can still guarantee an output voltage accuracy of $\pm 5\%$ without closed-loop control.

3.3.1 Steady-state Analysis

For deriving the dc voltage conversion ratio, here the following analysis is carried out which only considers the fundamental components of the voltages and currents in the converter. Through this analysis, a steady-state equivalent circuit is shown in Figure 3.12(b) where the capacitor C_r is the series resonant capacitor, L_r is the lumped inductance consisting of the leakage inductance of the transformer and other parasitic inductances in the resonant loop, R_r is the lumped resistance that includes all the parasitic resistance in the resonant loop, e.g., the on-resistance of the semiconductors, winding resistance and PCB track resistance etc., θ is the phase shift between full bridge output voltage u_f and the primary current i_p , U_i and i_i are

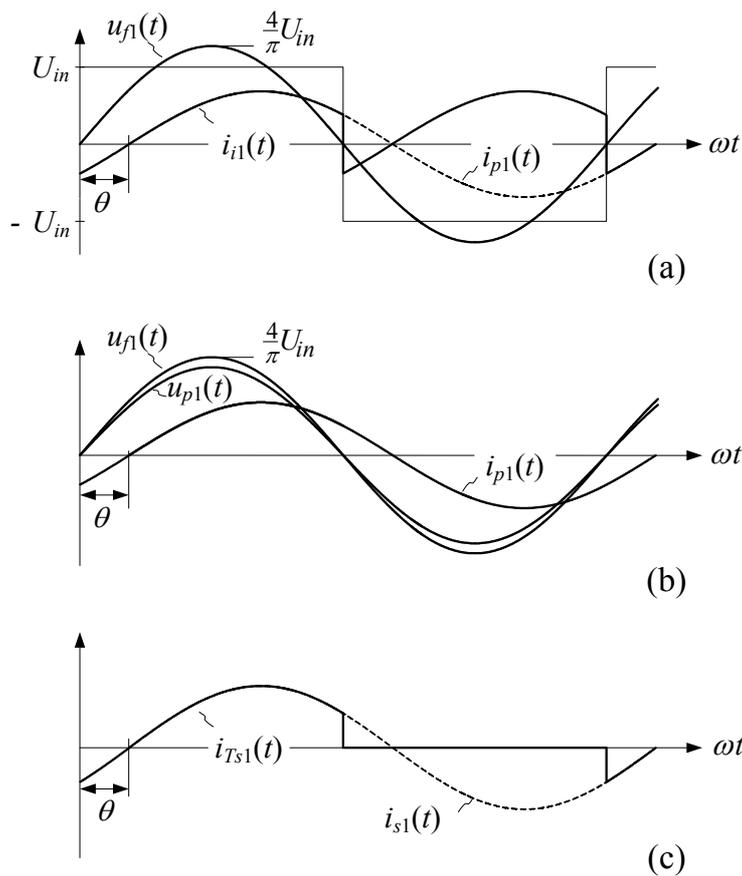


Figure 3.13: Fundamental components of the key waveforms in the bi-directional resonant converter. (a): full bridge output voltage $u_{b1}(t)$ and the input current $i_{i1}(t)$; (b): full bridge output voltage $u_{b1}(t)$, transform primary voltage $u_{p1}(t)$, and the primary current $i_{p1}(t)$; (c): secondary transistor T_{1s} current $i_{T_{1s}}(t)$.

the input voltage and current respectively, and u_p is the transformer primary voltage, and i_{T1} is the current of the secondary transistor T_{1s} .

Figure 3.13 shows the fundamental components of the key waveforms of the converter. Since the full bridge voltage u_f is a square waveform with the amplitude of U_i , its fundamental component is

$$u_{f1}(t) = \frac{4}{\pi} U_i \sin(\omega t). \quad (3.9)$$

The input dc current I_i is the integral value of the input current $i_{i1}(t)$ as shown in Figure 3.13(a) over a switching period, which can be calculated as

$$I_i = \frac{1}{T_s} \int_0^{T_s} i_{i1}(t) dt = \frac{1}{\pi} \int_0^{\pi} I_{p1} \sin(\omega t - \theta) d\omega t = \frac{2I_{p1} \cos \theta}{\pi}. \quad (3.10)$$

Since the secondary switching signals are synchronized with the primary side switches, the voltage u_f before the resonant tank is in phase with the voltage u_p after the resonant tank. The fundamental component of u_p can be written as

$$u_{p1}(t) = \frac{2N_1}{\pi N_2} I_2 R_2 \sin(\omega t). \quad (3.11)$$

Therefore the amplitude of the resonant current $i_{p1}(t)$ is

$$I_{p1} = \frac{\frac{4}{\pi} U_i - \frac{2N_1}{\pi N_2} I_2 R_2}{|j \cdot X_L - j \cdot X_C + R_r|}, \quad (3.12)$$

where $X_L = \omega \cdot L_r$ is the impedance of the series inductor, $X_C = 1/(\omega \cdot C_r)$ is the impedance of the resonant capacitor. And the resonant current $i_{p1}(t)$ is

$$i_{p1}(t) = I_{p1}(\omega t - \theta), \quad (3.13)$$

where the phase angle θ is defined as

$$\theta = \arctan \frac{X_L - X_C}{R_r} \quad (3.14)$$

Lastly the dc output current I_2 can be obtained by averaging the current $i_{Ts1}(t)$ over one switching period (see Figure 3.13(c)):

$$\begin{aligned} I_2 &= \frac{1}{T_s} \int_0^{T_s} i_{Ts1}(t) dt = \frac{1}{2\pi} \int_0^\pi \frac{N_1}{N_2} I_{p1} \sin(\omega t - \theta) d\omega t \\ &= \frac{N_1}{\pi N_2} I_{p1} \cos \theta. \end{aligned} \quad (3.15)$$

The average output voltage is given as

$$U_2 = I_2 R_2. \quad (3.16)$$

By combining equations (3.12), (3.15) and (3.16), the normalized input-to-output voltage conversion ratio can be derived as

$$\frac{U_2}{\frac{2N_2}{N_1} U_i} = 1 - \frac{\pi^2 N_2}{4N_1} \cdot \frac{|j \cdot X_L - j \cdot X_C + R_r|^2}{R_r U_i} I_2. \quad (3.17)$$

In Figure 3.14, the normalized input-to-output voltage transfer ratio, with dependency on the output current I_2 , is depicted for the case of different switching frequencies. It is shown that when the switching frequency is $f_s = 1.2\omega_0 / (2\pi)$, the normalized input-to-output voltage transfer ratio is $(100 \pm 1)\%$ when the output current changes from -5A to $+5\text{A}$. The points marked with “x” come from simulation and they show a very good match with the calculated results. The load regulation from digital simulation is shown in Figure 3.15, and it can be seen that no overshoot occurs in the case of a sudden load change and that the static output voltage error is $\pm 1\%$. Here the normalization base of the output voltage U_2 is defined as the open circuit output voltage $U_2^* = (2N_2/N_1) \cdot U_{in} = 40 \text{ V}$.

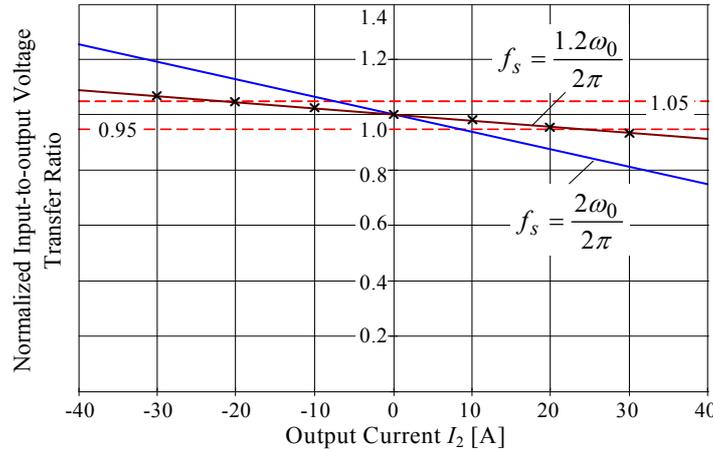


Figure 3.14: Normalized input-to-output voltage transfer ratio in dependency on the output current I_2 . Circuit parameters are: $U_{in} = 400V$, $N_1:N_2 = 20:1$, $C_r = 0.25\mu F$, $R_s = 6.2\Omega$, $L_r = 10\mu H$, $C_o = 1mF$.

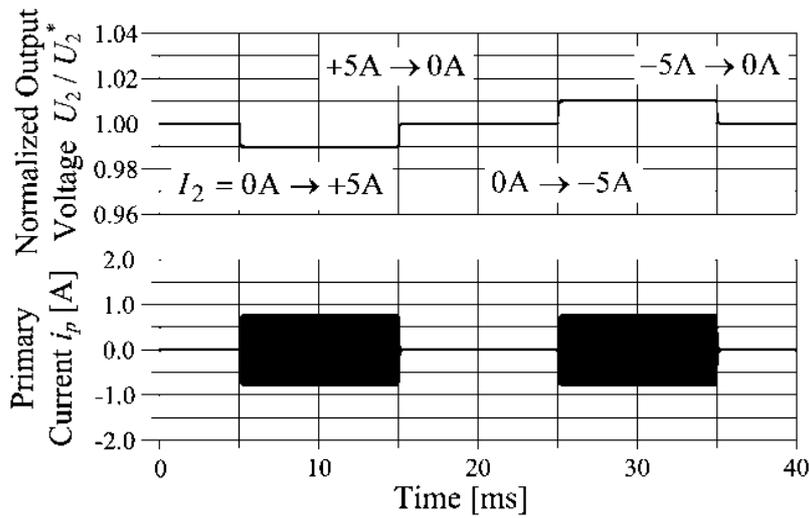


Figure 3.15: Simulated load regulation of the dc/dc converter. The output voltage normalization base is the open circuit output voltage $U_2^* = (2N_2/N_1) \cdot U_{in}$. Circuit parameters are: $U_{in} = 400V$, $N_1:N_2 = 20:1$, $C_r = 0.25\mu F$, $R_r = 6.2\Omega$, $L_r = 10\mu H$, $C_o = 1mF$, $f_s = 120\text{ kHz}$.

3.3.2 Output Impedance Optimization

In order to guarantee the output voltage regulation of the dc-dc converter without feedback control, it is necessary to optimize the converter output impedance. We can rewrite (3.17) to

$$U_2 = \frac{2N_2}{N_1} U_i - \frac{\pi^2 N_2^2}{2N_1^2} \cdot \frac{|j \cdot X_L - j \cdot X_C + R_r|^2}{R_r} I_2, \quad (3.18)$$

which shows the dependency of the output voltage U_2 on the output current I_2 . Obviously the converter output impedance is

$$\begin{aligned} R_o &= \frac{\pi^2 N_2^2}{2N_1^2} \cdot \frac{|j \cdot X_L - j \cdot X_C + R_r|^2}{R_r} \\ &= \frac{\pi^2 N_2^2}{2N_1^2} \cdot \frac{(X_L - X_C)^2 + R_r^2}{R_r}. \end{aligned} \quad (3.19)$$

The minimum output impedance value is derived as

$$R_{o,\min} = \begin{cases} \frac{\pi^2 N_2^2}{2N_1^2} \cdot R_r, & |X_L - X_C| = 0 \\ \frac{\pi^2 N_2^2}{2N_1^2} \cdot 2R_r, & |X_L - X_C| \neq 0 \end{cases}. \quad (3.20)$$

For the equation above, we can see that the converter has its minimum output impedance when the converter is switched at the natural frequency of the resonant tank. Figure 3.16 shows the dependency of the converter output impedance R_o on the normalized switching frequency f_s / f_0 . There the minimum output impedance values occur when the switching frequency f_s is equal to the natural frequency f_0 , i.e., $X_L = X_C$, regardless of the value of the resistor R_r . However in the circuit, the switching frequency is usually set to a frequency which is higher than the natural frequency f_0 in order to achieve the ZVS for primary transistors. The converter output impedance R_o in dependency on different values of the lumped resonant loop resistor R_r is illustrated in Figure 3.17, where the switching frequency f_s is selected to be $1.1f_0$, $1.2f_0$, and $1.3f_0$. It is shown that the minimum output impedance $R_{o,\min}$ occurs at $R_r = |X_L - X_C|$ and the minimum value is given in (3.20).

Unfortunately the lumped resonant loop resistance R_r is not flexible to adjust for a given circuit. However we can optimize the resonant inductance L_r that is mainly the leakage inductance of the transformer. Figure 3.18 shows the dependency of the converter output impedance R_o on the normalized

switching frequency f_s/f_0 for different resonant tanks that have the same natural frequency. It is shown that the output impedance R_o reduces with decreasing the resonant inductance L_r . Furthermore, we have noticed that the output impedance curve in dependency on the normalized switching frequency f_s / f_0 is flatter for lower quality factor Q_r , which is similar to the input-to-output voltage conversion ratio of the series resonant converter [52]-[53]. The difference is that Q_r in this converter is defined as

$$Q_r = \frac{\sqrt{L_r}}{R_r} \sqrt{C_r}. \quad (3.21)$$

In the series resonant converter, the equivalent load resistance is used in defining Q_r instead of using R_r here.

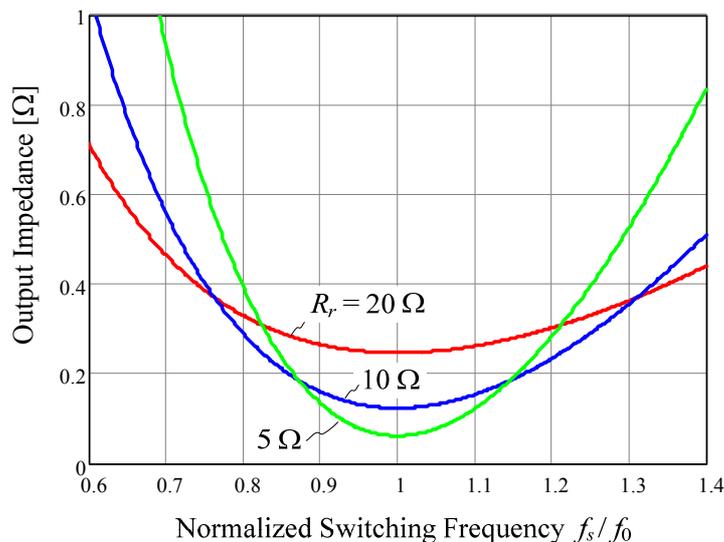


Figure 3.16: Dependency of the converter output impedance R_o on the normalized switching frequency f_s / f_0 for different lumped resonant loop resistor R_r . Calculation parameters are: $N_1:N_2 = 20:1$, $C_r = 45$ nF, $L_r = 30$ μ H.

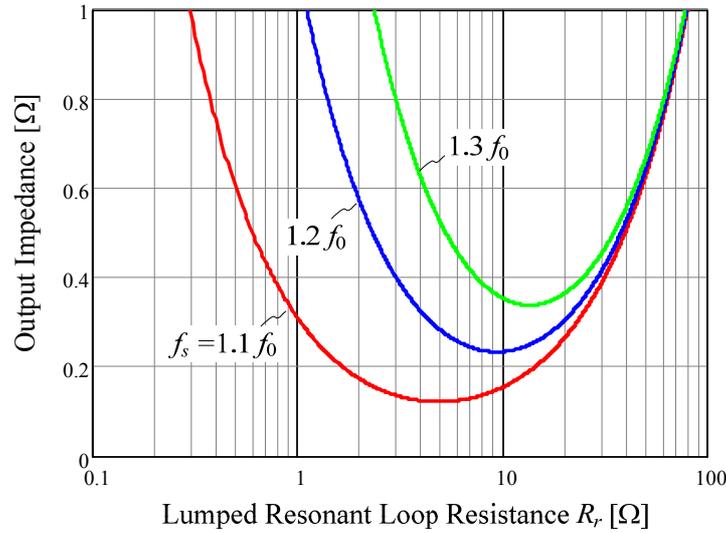


Figure 3.17: Dependency of the converter output impedance R_o on the different lumped resonant loop resistance R_r for different switching frequencies f_s . Calculation parameters are: $N_1:N_2 = 20:1$, $C_r = 45$ nF, $L_r = 30$ μ H.

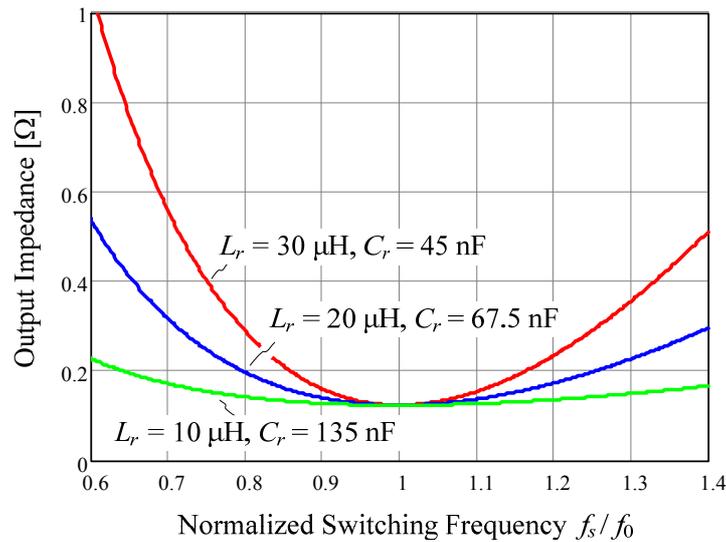


Figure 3.18: Dependency of the converter output impedance R_o on the normalized switching frequency f_s / f_0 for different resonant tanks having the same natural frequency f_0 . Calculation parameters are: $N_1:N_2 = 20:1$, $R_r = 10$ Ω .

3.3.3 Hardware Considerations

Based on the output impedance analysis in the section above, in order to achieve the low converter output impedance, we have to minimize the

lumped inductance L_r and resistance R_r in the resonant loop when designing the hardware and determine the right switching frequency. Firstly it is necessary to find out the composition of the L_r and R_r in the circuit.

The resonant circuit scheme is shown in Figure 3.19(a) and the component parameters are given in Table 5.3. The equivalent circuit of the resonant loop is shown in Figure 3.19(b). There R_{k1} is the lumped resistance in the primary conducting resonant loop which includes the ESR of the input capacitor C_{i1} (the film capacitor C_{i2} is neglected since its impedance is much higher than C_{i1} at the converter resonant frequency), the on-resistance of the conducting MOSFETs, and the parasitic resistance in the PCB tracks. R_w and L_{lk} are the lumped transformer resistance and inductance including both primary and secondary windings. Analogously, R_{k2} and L_{k2} are the lumped resistance and inductance in the secondary conducting loop. Therefore the lumped RLC parameters shown in Figure 3.12(b) can be written as

$$\begin{aligned}
 R_r &= R_{k1} + R_w + \frac{N_1^2}{N_2^2} R_{k2}; L_r = L_{k1} + L_{lk} + \frac{N_1^2}{N_2^2} L_{k2}; \\
 C_r &= \frac{C_p \frac{N_2^2}{N_1^2} 2C_{o1}}{C_p + \frac{N_2^2}{N_1^2} 2C_{o1}}.
 \end{aligned} \tag{3.22}$$

Since R_{k1} and L_{k1} are comparably smaller than the other two terms in (3.22), the work of minimizing L_r and R_r is mainly focused on the transformer and the secondary side circuit.

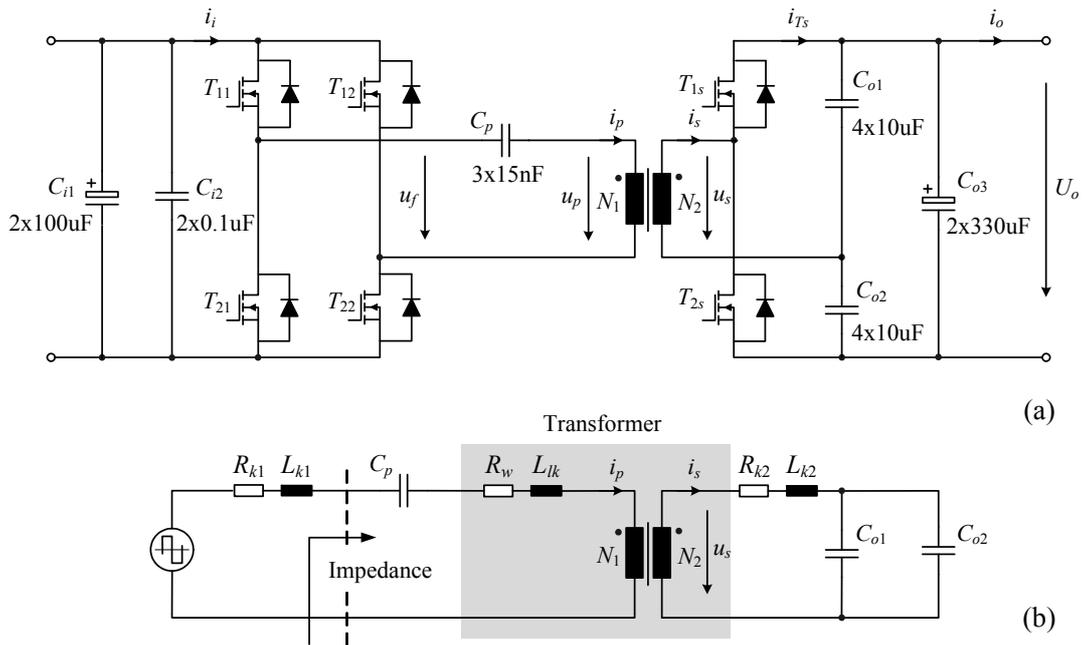


Figure 3.19: Circuit schematic of the bi-directional resonant converter (a) and equivalent circuit of the resonant loop for deriving the resonant parameters (b).

Minimizing the leakage inductance of the transformer

Figure 3.20 shows the transformer windings structure. In order to reduce the leakage inductance, the three aspects listed below have been considered when designing the transformer:

- A typical sandwich structure is used for the transformer windings which not only reduces the leakage inductance but also lowers the winding losses because of lessening the proximity effects.
- The air space in the windings and between the different windings is minimized in order to reduce the leakage flux. E.g., sixty turns of primary windings exactly fit two layers in the foil; copper tapes are used for the secondary windings to maximize the utilization of the winding window; and extremely thin isolation material is employed.

The measured impedance from the measurement point (see Figure 3.19) when the secondary winding of the transformer is shorted is shown in Figure 3.21, where the dotted curve is from measurement and the continuous curve is the fitted curve using the series RLC model. The leakage inductance L_{lk} and lumped winding resistance R_w are given as

$$R_w = 5.47 \Omega, L_{lk} = 25.6 \mu\text{H}, \tag{3.23}$$

where L_{lk} is only about 0.1% of the primary magnetizing inductance, 29 mH.

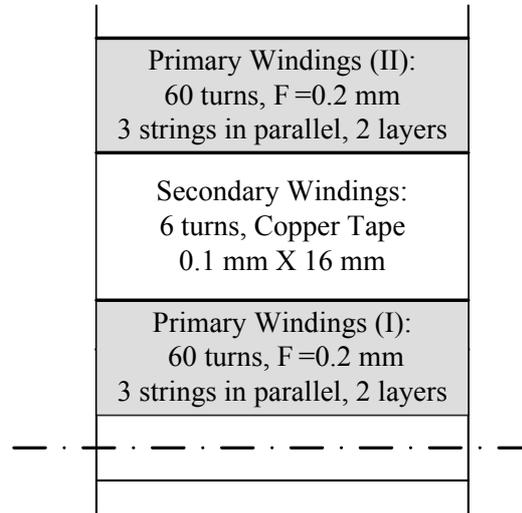


Figure 3.20: Structure of transform windings

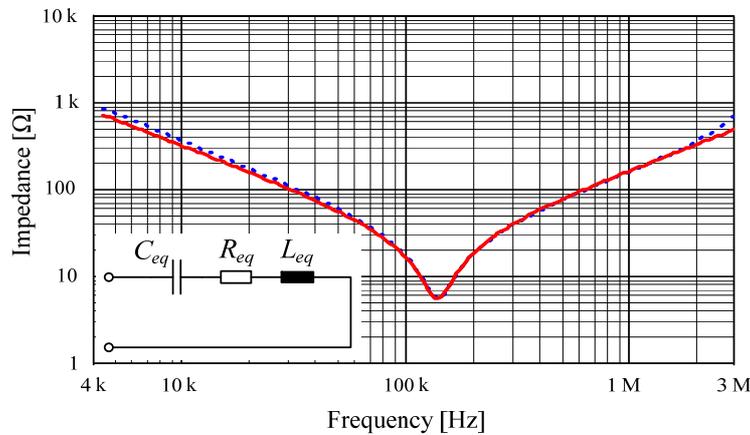


Figure 3.21: Measured impedance form the measurement point (see Figure 3.19) when the secondary winding of the transformer is shorted (dotted) and the impedance curve of the equivalent RLC resonant tank (continuous). The circuit parameters are calculated through fitting the measurement curve: $C_{eq} = 49.86 \text{ nF}$, $R_{eq} = 5.47 \Omega$, $L_{eq} = 25.6 \mu\text{H}$.

Minimizing parasitic inductance and resistance in the secondary side

Because the transformer has a high turns ratio of 20:1, the secondary side inductance and resistance will be multiplied by 400 when the values are converted to the primary side. There are mainly two actions that have been carried out to minimize them:

- IRF6648 with DirectFET™ package is selected for realization of the secondary side MOSFETs. The inductance in the source mounted DirectFET™ package is only about 1 nH at 1 MHz. This value is significantly reduced compared to the inductance of a DPAK, 2.4nH, and of a D²PAK, 5 nH measured at the same frequency [54]. At the same time, the board mounted resistance of the DirectFET™ package is only about 1 mΩ measured at 1 MHz. Furthermore, IRF6648 on-resistance is only 10 mΩ at the junction temperature of 125°C and gate-to-source voltage of 10 V.
- For designing the PCB layout, the secondary side conducting loop is minimized. And a big polygon is placed to connect the transformer to the central point of the output capacitor leg, in order to guarantee a low impedance loop whether T_{1s} or T_{2s} is conducting.

In order to determine the RLC parameters in the resonant loop, the Agilent impedance analyzer 4294A is used to measure the impedance from the measurement point (see Figure 3.19) while T_{1s} is on, T_{2s} is off and the DC capacitor C_{o3} is shorted. The measured impedance is depicted in Figure 3.22. By curve fitting the measured data, the equivalent RLC parameters are found as: $C_{eq} = 37.02$ nF, $R_{eq} = 10.80$ Ω, $L_{eq} = 29.22$ μH. Compared to the measurement while the transformer secondary winding is shorted (Figure 3.21), the inductance and resistance in the secondary conducting loop are calculated as

$$R_{k2} = 13 \text{ m}\Omega, L_{k2} = 9 \text{ nH.} \quad (3.24)$$

The primary loop resistance R_{k1} is mainly dominated by the MOSFET on-resistance that is 0.42 Ω at a junction temperature of 125°C and a gate-to-source voltage of 10 V. The inductance L_{k1} is estimated by a simple rule of thumb, 10 nH/cm, for the PCB tracks and device leads. Therefore these two parameters are approximated as

$$R_{k1} = 0.9 \text{ }\Omega, L_{k1} = 600 \text{ nH.} \quad (3.25)$$

Combining equations (3.22), (3.23), (3.24), and (3.25), the resulting RLC parameters in the total resonant loop are

$$R_r = 11.7 \Omega, L_r = 29.82 \mu\text{H}, C_r = 37 \text{ nF}. \quad (3.26)$$

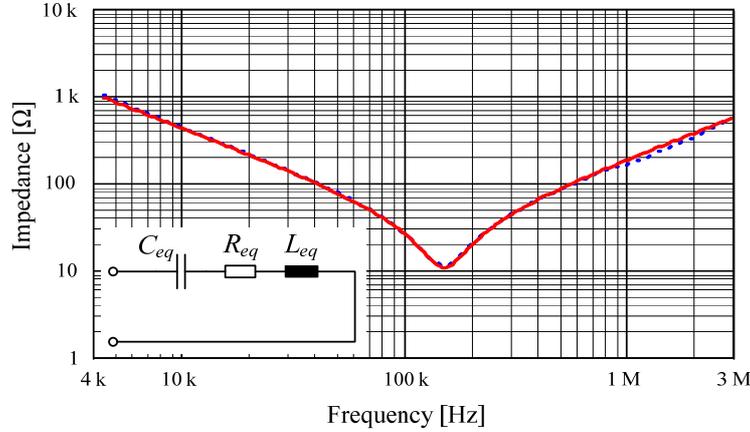


Figure 3.22: Measured impedance from the measurement point (Figure 3.19) when the secondary dc capacitor C_{o3} is shorted (dotted) and the impedance curve of the equivalent RLC resonant tank (continuous). The circuit parameters are calculated through fitting the measurement curve: $C_{eq} = 37.02 \text{ nF}$, $R_{eq} = 10.80 \Omega$, $L_{eq} = 29.22 \mu\text{H}$.

3.3.4 Experimental Results

In order to determine the optimized switching frequency, a series of tests has been carried out to measure the output voltage U_2 in dependency on the switching frequency f_s for the constant output dc current $I_2 = 3 \text{ A}$. As mentioned above, the optimized switching frequency must be slightly higher than the natural resonant frequency f_0 , so that the switches in the primary side can be turned on under ZVS and the resonant current amplitude I_{p1} is limited (according to (3.15), I_{p1} is inversely proportional to $\cos \theta$).

Figure 3.23 shows the measured waveforms of the primary current i_p , transformer primary voltage u_p , and secondary voltage u_s for three different switching frequencies, 110 kHz, 140 kHz and 180 kHz. At 110 kHz switching frequency i_p is leading u_p and u_s , which means this frequency is smaller than f_0 . Analogously 180 kHz is larger than f_0 because i_p lags behind u_p and u_s . Figure 3.23(b) shows that 140 kHz seems to be a good choice for the optimized switching frequency which is only slightly higher than f_0 . And the primary current amplitudes, 0.76 A at 110 kHz and 0.8 A at 180 kHz, are larger than the one at 140 kHz. This relation is in line with (3.15). Moreover,

Figure 3.23 also shows that a sharp step in i_p , about 0.5 A, always occurs when the polarities of u_p and u_s change. There are two factors which can cause the sharp current step in i_p : different delay times from the FPGA signal to the switch action of primary and secondary sides, and the different behaviours of the switching voltage of primary MOSFETs and secondary MOSFETs. The first factor is compensated in FPGA programming. However for the second factor, there are few chances for compensation because they are dependent on the MOSFET device parameters, gate driver unit, layout and operating points. If we want to completely eliminate the current step, the voltage shapes of u_p and $\frac{N_1}{N_2}u_s$ are required to be identical, which is not realistic in the hardware. However the current step amplitude has been minimized after the delay time compensation during the hardware testing.

The comparison of the measured and calculated curves of the output voltage in dependence on the switching frequency is depicted in Figure 3.24. There the measured f_0 is about 138 kHz while the calculated f_0 is 152 kHz which indicates ten percent difference. The possible reasons for the difference are:

- Influence of current, voltage and temperature on the component parameters. Since in the analysis the circuit parameters are obtained through small signal impedance measurements and data-sheets, these values could vary when we put the circuit into power operation.
- The steady-state equivalent circuit model shown in Figure 3.12 of the converter is not accurate enough. It is fundamental to the analysis of the converter steady-state characteristic that we consider i_p to have a sinusoidal shape; however in the hardware i_p is not sinusoidal any more especially due to the sharp current step. For a more accurate model, we could modify the steady-state model.

The discussion above also points out that this converter is sensitive to device parameters, operating point, hardware delay times, and tolerances of component values etc. Therefore it is not easy to achieve a very accurate design. However analysis of the converter gives a good design guideline which has about 10% tolerance for this laboratory prototype.

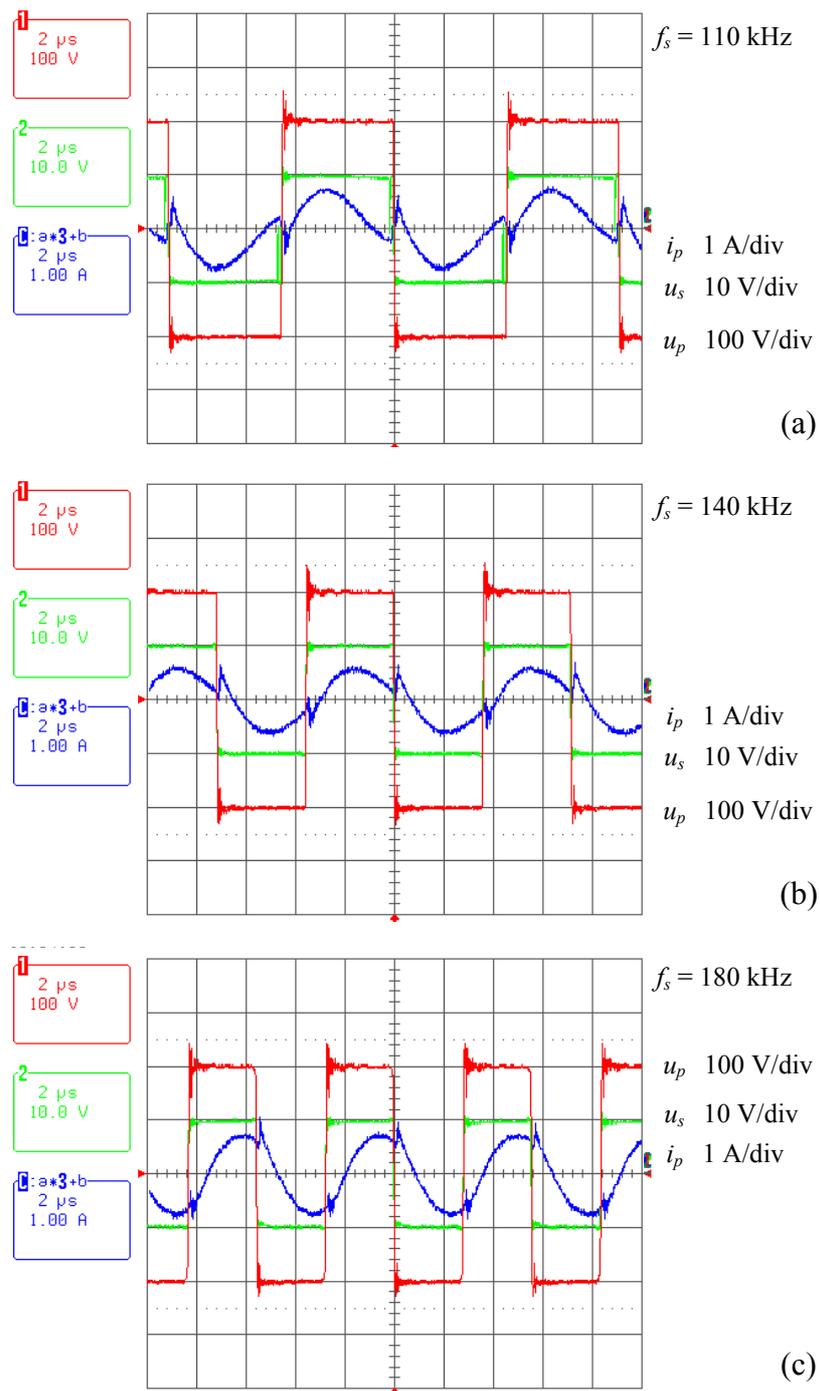


Figure 3.23: Measured time behaviour of the primary current i_p , transformer primary voltage u_p , and secondary voltage u_s for three different switching frequencies: 110 kHz (a), 140 kHz (b) and 180 kHz (c). Operation parameters: $U_{in} = 200\text{ V}$, $I_2 = 3\text{ A}$.

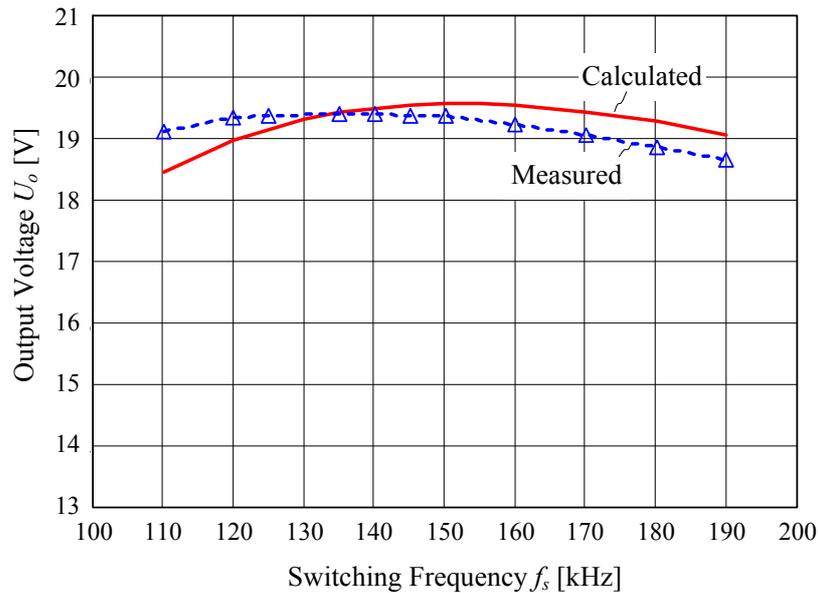


Figure 3.24: Output voltage in dependency on the switching frequency. Operation parameters: $U_{in} = 200$ V, $I_2 = 3$ A.

As explained before, the aim of the design of this converter is to achieve the output voltage regulation tolerance of $\pm 5\%$ without closed-loop control for bi-directional power flow. Figure 3.25 shows the experimental results for forward power flow operation. This figure demonstrates the measured time behaviours of the primary current i_p , transformer primary voltage u_p , and secondary voltage u_s for different output dc currents, 1 A, 3 A and 5 A. In these measurements, the input voltage is fixed to $U_{in} = 200$ V and the load resistance is adjusted to control the dc output current value. All voltage and current values are measured with high precision Fluke multi-meters. The measured and calculated V-I curves for forward power flow operation are illustrated in Figure 3.27. The calculated output resistance, 0.17Ω , is about 20% less than the measured output resistance, 0.22Ω . However we can still achieve $\pm 5\%$ regulation error at nominal output current 4.5 A for forward power flow.

For measuring the reverse power flow, the output is connected to a regulated dc voltage source and the input voltage U_{in} and input current I_{in} are measured. Figure 3.26 shows the measured waveforms of the primary current i_p , transformer primary voltage u_p , and secondary voltage u_s for different input dc currents, -0.1 A, -0.3 A and -0.5 A. If we compare i_p in Figure

3.26(c) with i_p in Figure 3.25(c), the current phase is about 180° shifted because of the reverse power flow. Furthermore, for a similar level of power flow, the amplitude of i_p for reverse power flow, 1.2 A, is relatively higher than the one for forward power flow, 0.9 A. The reason has been mentioned before: it is due to the voltage switching behavior difference of the primary MOSFETs and secondary MOSFETs. This difference effectively creates a small leading phase shift of u_s against u_p . Therefore, i_p always steps to negative direction when the polarity of u_p and u_s changes from negative to positive and analogously i_p steps to positive direction when the polarity of u_p and u_s changes from positive to negative. This phenomena is not dependant on the direction of power flow. Because of this, the amplitude of i_p is reduced for forward power flow while it is increased for the reverse power flow. In addition, this small phase shift also affects the static voltage transfer ratio, i.e., the secondary side dc voltage U_2 is slightly raised. Figure 3.27 shows that $U_2 = 20.1$ V which is supposed to be 20 V at zero power flow condition. Consequently U_{in} is brought down for reverse power flow operation as shown in Figure 3.28. On the other hand, we could control the phase shift to control the output voltage, but this comes at the cost of an increased current sudden step in i_p .

The measured and calculated V-I curves for reverse power flow operation are illustrated in Figure 3.28. There the measured output resistance is 24Ω while the calculated output resistance is 17Ω . From the V-I measurements for forward power flow, an output resistance of 0.22Ω is determined. Theoretically the output resistance for reverse power flow should be $100 \times 0.22 \Omega = 22 \Omega$. However the measured value is 24Ω which is about 10% higher. This is because of the higher resistive losses due to the relatively higher current amplitude for reverse power flow operation as discussed in the previous paragraph. In Figure 3.28, one sees a voltage regulation error of 7.5% at nominal current of 0.45 A. However, these measurements are done for 135V output voltage range. For 270 V output voltage range operation, the input voltage is increased to 400 V and the nominal output current stays the same. This will effectively reduce the regulation error by a factor of two, i.e., 2.5% for forward power flow and 4% for reverse power flow.

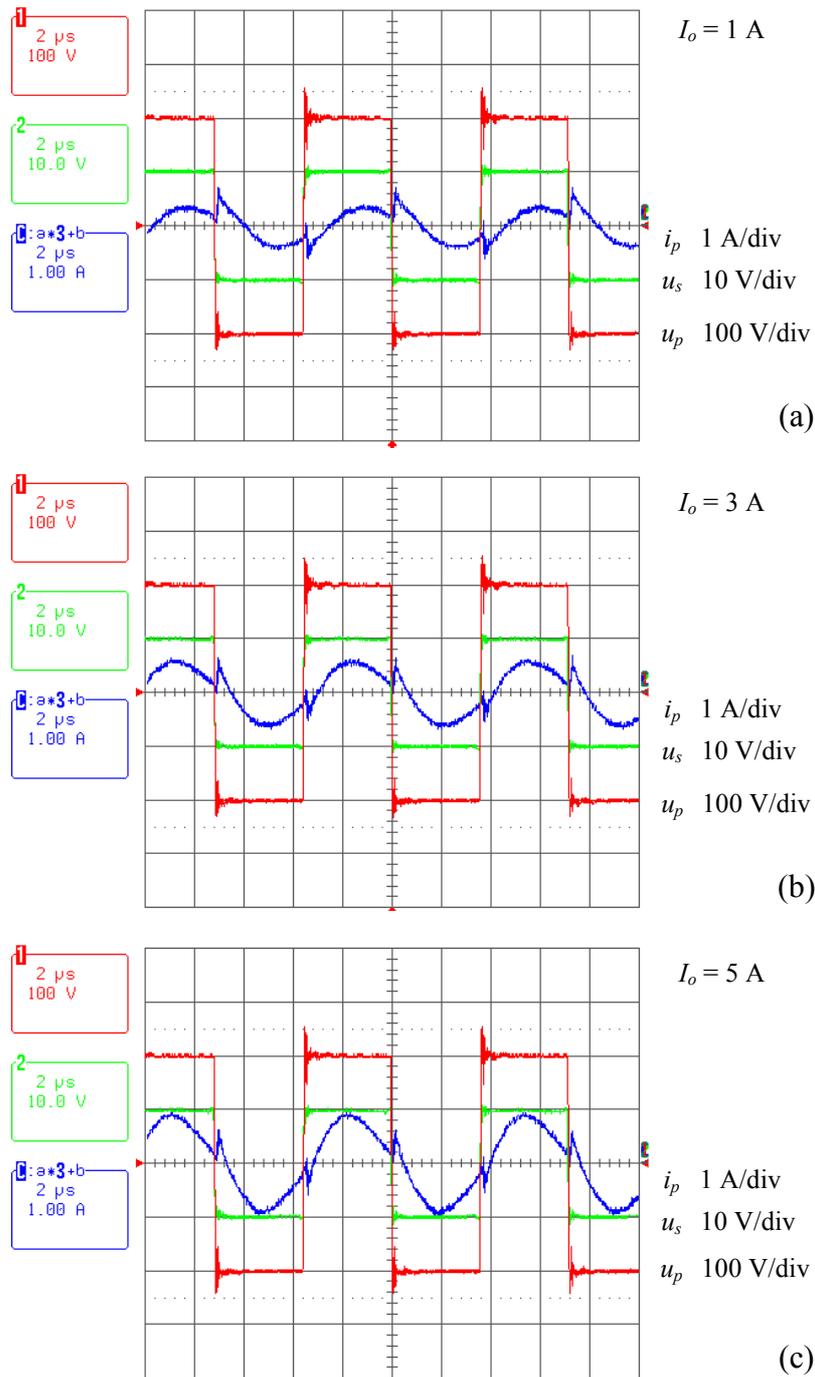


Figure 3.25: Experimental results for forward power flow operation. Measured time behaviours of the primary current i_p , transformer primary voltage u_p , and secondary voltage u_s for different output dc current: 1 A (a), 3 A (b) and 5 A (c). Operation parameters: $U_{in} = 200 \text{ V}$, $f_s = 140 \text{ kHz}$.

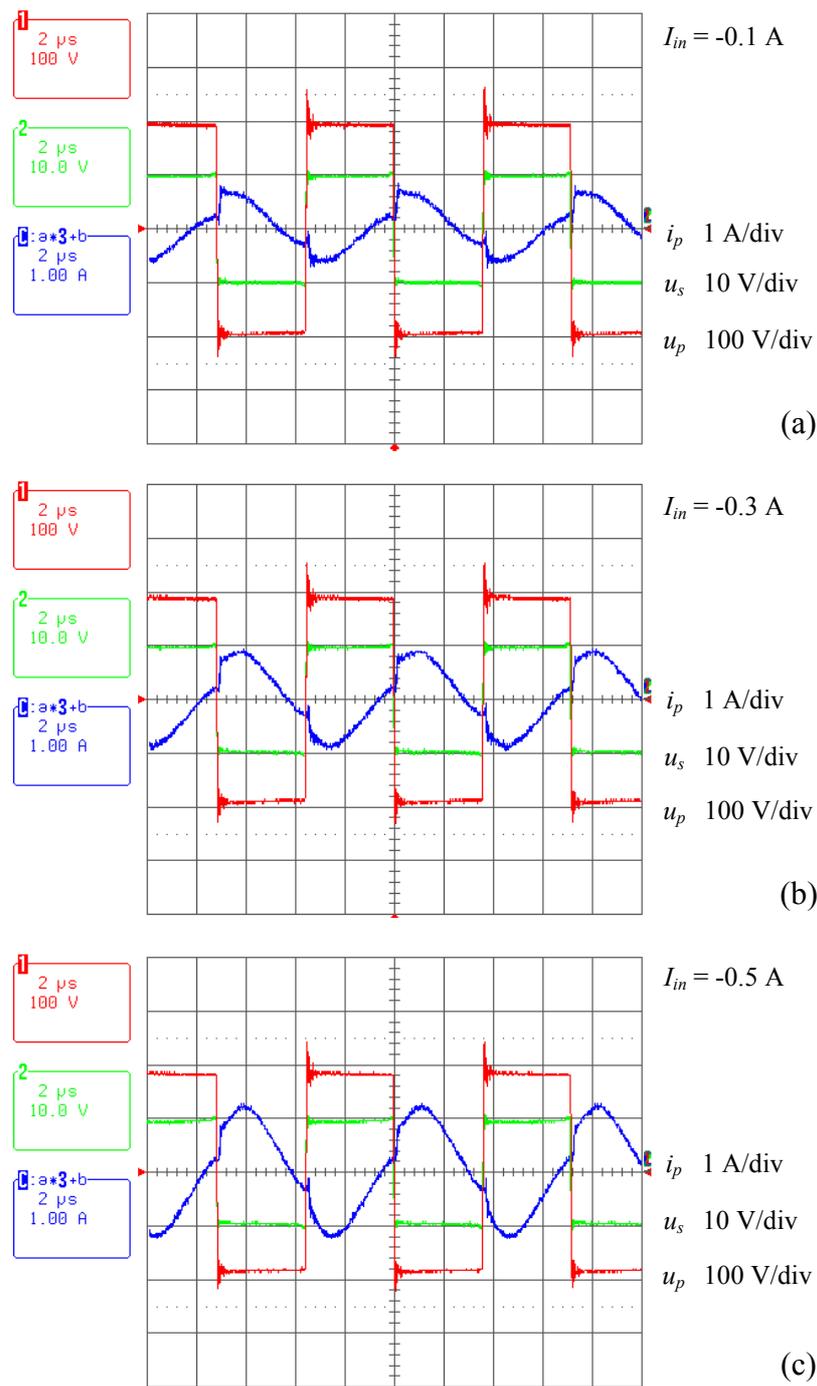


Figure 3.26: Experimental results for reverse power transfer operation. Measured time behaviours of the primary current i_p , transformer primary voltage u_p , and secondary voltage u_s for different input dc current: -0.1 A (a), -0.3 A (b) and -0.5 A (c). Operation parameters: $U_2 = 20$ V, $f_s = 140$ kHz.

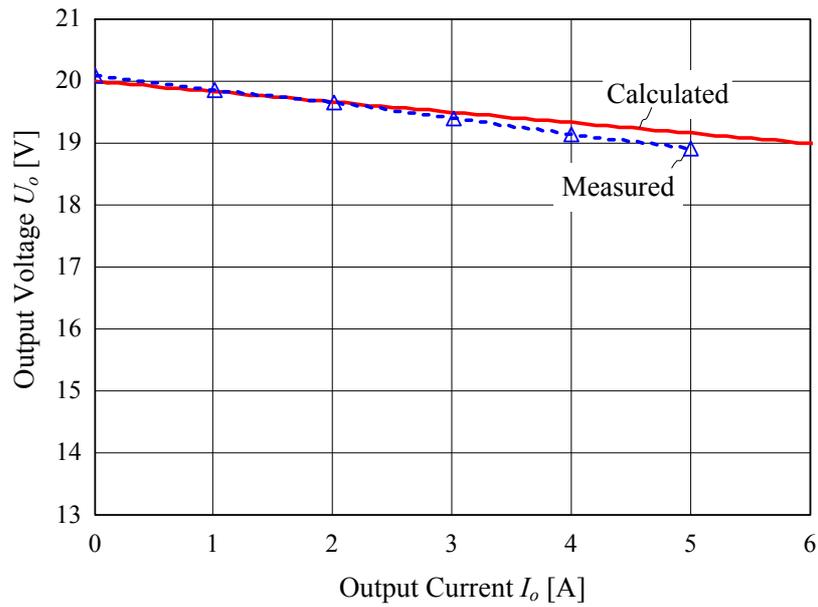


Figure 3.27: V-I curve for forward power flow operation. Operation parameters: $U_{in} = 200$ V, $f_s = 140$ kHz.

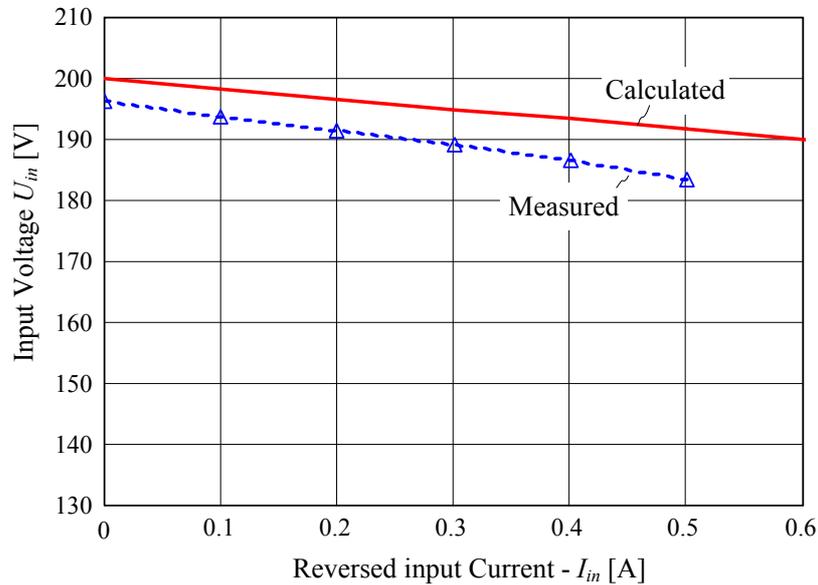


Figure 3.28: V-I curve for reverse power flow operating. Operation parameters: $U_2 = 20$ V, $f_s = 140$ kHz.

3.4 System Loss Calculation

3.4.1 LPA Losses

For the loss calculations it is assumed that the output voltage of the linear power amplifier is

$$u_o = U_{op} \sin \omega t \quad (3.27)$$

and results in an output (load) current of

$$i_o = \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) = I_{op} \sin(\omega t - \varphi), \quad (3.28)$$

where Z_L is the magnitude of the load impedance and $\varphi \in (-\pi/2, +\pi/2)$ is the phase angle of the load current. The output power of the linear amplifier is then given by

$$P_o = \frac{U_{op}^2}{2Z_L} \cos \varphi. \quad (3.29)$$

In the case where the linear power amplifier is operating in a class-AB mode and the quiescent current is neglected, the losses of the output transistors in the linear power amplifier are calculated as

$$P_{lpa} = 2 \frac{1}{2\pi} \int_{\varphi}^{\varphi+\pi} (U_a - u_{lo}) \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t. \quad (3.30)$$

The equation above can be approximated by using U_a to replace $U_a - u_{la}$ considering that the voltage drop occurring across the power transistor of LPA is constant

$$P_{lpa,sim} = \frac{1}{\pi} \int_{\varphi}^{\varphi+\pi} U_a \frac{U_{op}}{Z_L} \sin(\omega t - \varphi) d\omega t = \frac{2}{\pi} U_a I_{op}. \quad (3.31)$$

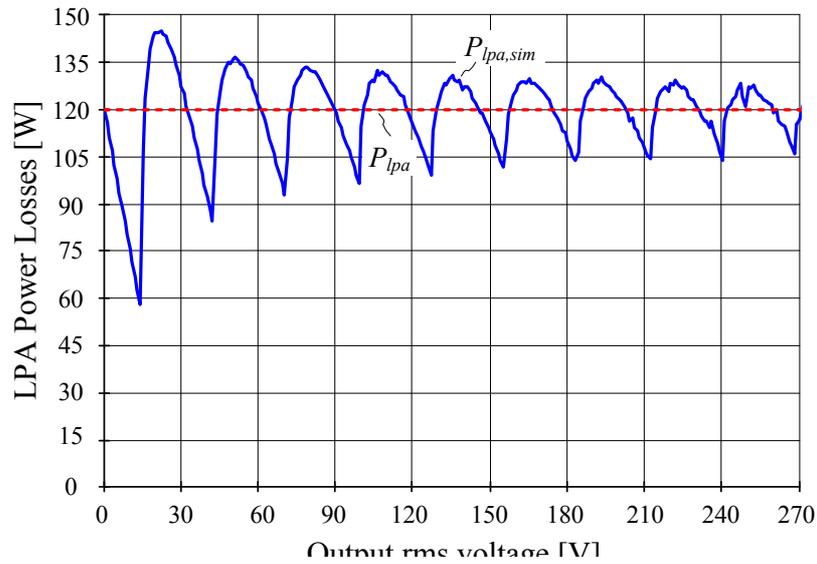


Figure 3.29: Comparison of LPA losses P_{lpa} with simplified LPA losses $P_{lpa,sim}$ in dependency on output rms voltage U_o . Operating parameters: $I_{o,rms} = 4.5$ A, $\varphi = 0^\circ$, $f_o = 5$ kHz, $U_z = 40$ V, $U_a = 30$ V.

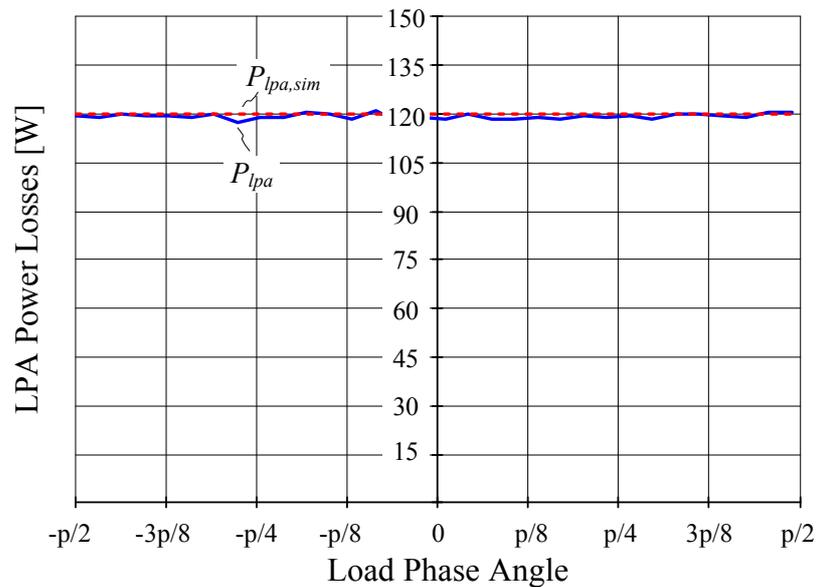


Figure 3.30: Comparison of LPA losses P_{lpa} with simplified LPA losses $P_{lpa,sim}$ in dependency on load phase angle φ . Operating parameters: $U_{o,rms} = 270$ V, $I_{o,rms} = 4.5$ A, $f_o = 5$ kHz, $U_z = 40$ V, $U_a = 30$ V.

The comparison of LPA losses P_{lpa} with the simplified LPA losses $P_{lpa,sim}$ in dependency on the output rms voltage U_o is depicted in Figure 3.29. There the higher the output voltage, the less difference there is between P_{lpa} and

$P_{lpa,sim}$. This is because more inverter cells are switched on for higher output voltage. If an infinite number of inverter cells are switched on, P_{lpa} and $P_{lpa,sim}$ would be the same. And this also shows that $P_{lpa,sim}$ is a good approximation of P_{lpa} in general.

Figure 3.30 shows the comparison of the LPA losses P_{lpa} with the simplified LPA losses $P_{lpa,sim}$ in dependency on load phase angle φ ; the LPA losses are almost independent of the load phase angle.

3.4.2 Multi-cell Inverter Losses

Since the multi-cell inverter is connected in series with the load, there are always two transistors conducting the load current for each cell unit. The conduction losses of the multi-cell inverter $P_{mci,con}$ are

$$P_{mci,con} = 2N \cdot R_{on} \left(\frac{U_{op}}{\sqrt{2}Z_L} \right)^2, \quad (3.32)$$

where N is the number of the cells, and R_{on} is the on-resistance of a single transistor in the multi-cell inverter.

For the calculation of the switching losses of the multi-cell inverter, the switching sequence and condition of each inverter unit must be known. Figure 3.31 shows the switching sequence of one inverter cell in one output period and how the three different output voltages $+U_z$, $0V$ and $-U_z$ are generated according to the corresponding switching patterns. For instance at t_1 , T_s is turned off and afterwards T_1 is turned on, with the result that the cell output voltage is changed from $0V$ to $+U_z$. Summarizing the switching patterns of one inverter cell shows that for one output voltage period two switch-on and two switch-off actions of each operating cell unit occur.

The typical turn-on and turn-off switching behaviour of a MOSFET in a bridge leg is depicted in Figure 3.32, where the body diode reverse recovery is considered during the turn-on of the MOSFET [64]. The switching time, including turn-on and turn-off, is divided into six periods. These periods are defined in Table 3.2, where the time behaviours of gate voltage u_{gs} , switch-

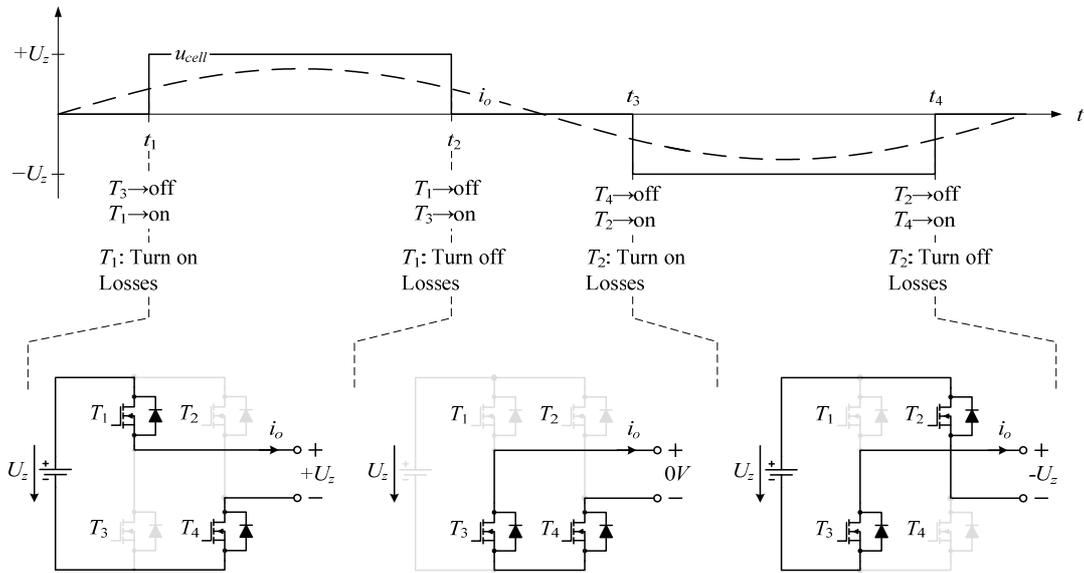


Figure 3.31: Switching sequence of one inverter cell in one output period and corresponding inverter output voltage status for a resistive load.

ing current i_{sw} and switching voltage u_{sw} in each period are described. By integrating i_{sw} and u_{sw} over the switching time the switching energy can be calculated.

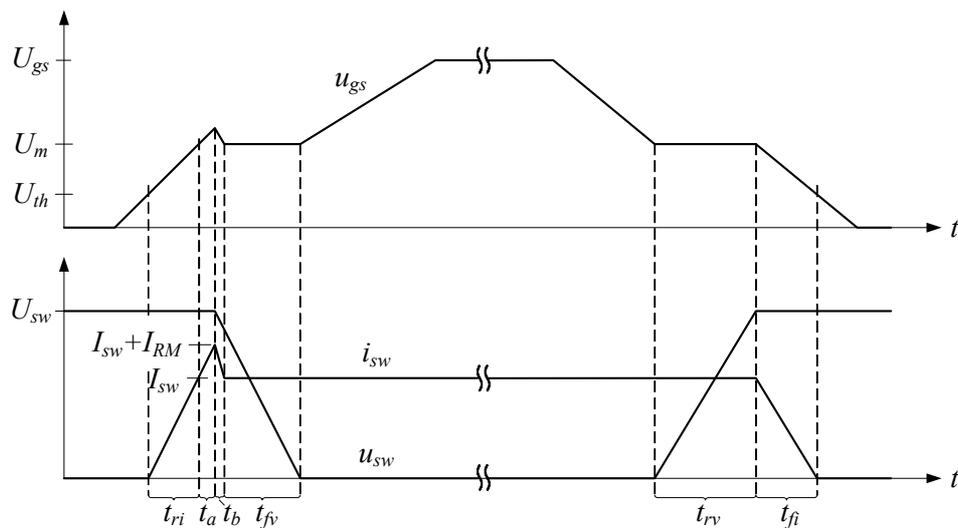


Figure 3.32: Typical turn-on and turn-off switching behaviour of a MOSFET in a half bridge leg.

Table 3.2: Periods and behaviour description of a switching period

	Switching Periods	Denotation	Gate Voltage u_{gs}	Switching Current i_{sw}	Switching Voltage u_{sw}
Turn-on	Current rising period	t_{ri}	Rises from U_{th} to U_m	Rises from 0 A to I_{sw}	Stays at U_{sw}
	Reverse recovery period I	t_a	Rises slightly	Rises from I_{sw} to $I_{sw} + I_{RM}$	Stays at U_{sw}
	Reverse recovery period II	t_b	Falls to U_m	Falls to I_{sw}	Falls slightly
	Voltage falling period	t_{fv}	Stays at U_m	Stays at I_{sw}	Falls to 0 V
Turn-off	Voltage rising period	t_{rv}	Stays at U_m	Stays at I_{sw}	Rises from 0 V to U_{sw}
	Current falling period	t_{fi}	Falls from U_m to U_{th}	Falls to 0 A	Stays at U_{sw}

In the following analysis, the duration of each period will be derived. The current rise period t_{ri} is calculated as

$$t_{ri} = \frac{Q_{m1} - Q_{th}}{U_m - U_{th}} R_{on} \ln \left(\frac{U_{gs} - U_{th}}{U_{gs} - U_m} \right), \quad (3.33)$$

where Q_{th} is the MOSFET gate charge when the gate voltage is increased to U_{th} , and Q_{m1} is the MOSFET gate charge when the gate voltage rises to U_m . This rise time is usually very small. In practice the current rise time is limited by the parasitic inductance of the commutation loop. However the employed DirectFET package has only 0.5 nH inductance. With careful layout design, here we neglect the influence of the commutation loop inductance.

As given in [63], diode reverse recovery time t_{rr} is proportional to the square root of the forward current divided by the current slew rate. Therefore, t_{rr} can be calculated from

$$t_{rr} = \frac{\sqrt{\frac{I_{sw}}{I_{sw}}}}{\sqrt{\frac{I_{F,spec}}{didt_{spec}}}} t_{rr,spec} = \frac{\sqrt{t_{ri}}}{\sqrt{\frac{I_{F,spec}}{didt_{spec}}}} t_{rr,spec}. \quad (3.34)$$

There $I_{F,spec}$, $didt_{spec}$ and $t_{rr,spec}$ are the specified values from the device datasheet. The reverse recovery charge Q_{rr} is proportional to the forward current [63]. We can derive Q_{rr} as

$$Q_{rr} = \frac{I_{sw}}{I_{F,spec}} Q_{rr,spec}. \quad (3.35)$$

The diode reverse recovery current can be approximated to have a triangular shape. Then the peak value of the reverse recovery current I_{RM} is computed as

$$I_{RM} = \frac{2Q_{rr}}{t_{rr}}. \quad (3.36)$$

On the first part of the reverse recovery period t_a , the reverse recovery current is continuously rising until the peak value. Thus t_a is obtained from

$$t_a = \frac{I_{RM}}{\frac{I_{sw}}{t_{ri}}} = \frac{I_{RM} t_{ri}}{I_{sw}}. \quad (3.37)$$

Therefore the other part of the reverse recovery period t_b is

$$t_b = t_{rr} - t_a. \quad (3.38)$$

During the voltage drop period t_{fv} , the gate voltage stays at U_m . Then this period is calculated as

$$t_{fv} = \frac{(Q_{m2} - Q_{m1}) R_{on}}{U_{gs} - U_{th}} \quad (3.39)$$

where Q_{m2} is the MOSFET gate charge needed at the end of the Miller effect stage. During the turn-off period, there are only two stages: voltage rising period t_{rv} and current falling time t_{fi} . And there is no diode reverse recovery in this period. Then t_{rv} and t_{fi} are analogously derived as

$$t_{rv} = \frac{Q_{m2} - Q_{m1}}{U_m/R_{off}}; \quad (3.40)$$

$$t_{fi} = \frac{Q_{m1} - Q_{th}}{U_m - U_{th}} R_{off} \ln\left(\frac{U_m}{U_{th}}\right). \quad (3.41)$$

According to Figure 3.32, the switching energy losses of one inverter cell in one output voltage period are

$$\begin{aligned} E_{sloss} = & 2 \left(\frac{1}{2} U_{sw} (I_{sw} + I_{pm}) (t_{ri} + t_a) \right. \\ & + \frac{1}{2} U_{sw} (2I_{sw} + I_{RM}) t_b \\ & \left. + \frac{1}{2} U_{sw} I_{sw} (t_{fv} + t_{rv} + t_{fi}) + \frac{1}{2} C_{oss} U_{sw}^2 \right), \end{aligned} \quad (3.42)$$

where C_{oss} is the output capacitance of MOSFETs and $\frac{1}{2} C_{oss} U_{sw}^2$ represents the energy losses because the capacitor energy dissipates through the MOSFET during hard turn-on. Since the switching voltage is constant, i.e., $U_{sw} = U_z$, the switching energy is mainly dependent on the switching current (the junction temperature is considered to be 125°C for the calculation). Therefore the E_{sloss} can be regarded as a function of I_{sw} .

As we have seen in Figure 3.1 the switching current is different for each cell, and this can be calculated for resistive load as

$$I_{sw(i)} = I_{op} \sin \left(\sin^{-1} \left(\frac{(2i-1)U_z}{2U_{op}} \right) \right), \quad (3.43)$$

where $i \in (1, n)$ and $n = \text{trunc}(U_{op} / U_z + 1/2)$ is the number of the actual operating cells according to the amplitude of the output voltage to be generated. E.g., $I_{sw(1)}$ is the switching current of the first switch-on inverter unit. By combining equations (3.42) and (3.43), the switching losses of the complete multi-cell inverter can be derived as

$$P_{mci,sw} = 2f_o \sum_{i=1}^n E_{sloss}(I_{sw(i)}). \quad (3.44)$$

where f_o is the frequency of the output voltage. When there is a large number of inverter cells, we can use the average value of output current in a half output period as switching current for all the cells, i.e.,

$$P_{mci,sw,sim} = 2nf_o E_{sloss} \left(\frac{2}{\pi} I_{op} \right). \quad (3.45)$$

The total losses of the multi-cell cascaded power amplifier is summed to be

$$P_{mci} = P_{mci,con} + P_{mci,sw}. \quad (3.46)$$

3.4.3 Isolated dc-dc Converter Losses

Since each inverter cell outputs a different power, as we have seen from Figure 3.1, this consequently determines the power drawn from each dc link provided by the isolated dc-dc converter. The power required for each inverter cell is

$$P_{inv,out(i)} = \frac{1}{\pi} \int_{\sin^{-1}\left(\frac{(2i-1)U_z}{2U_{op}}\right)}^{\pi - \sin^{-1}\left(\frac{(2i-1)U_z}{2U_{op}}\right)} U_z I_{op} \sin(t - \varphi) dt. \quad (3.47)$$

If we only consider the fundamental component of the resonant current (key waveforms as shown in Figure 3.13), the conduction losses of the primary MOSFETs are

$$P_{idc,con,pri} = 4 \left(\frac{\pi}{4} \frac{1.15 P_o}{U_{in}} \frac{1}{\cos(\theta)} \right)^2 R_{on,inf}, \quad (3.48)$$

where the factor 1.15 is added to consider the additional power needed for covering the system losses. The conduction losses of the MOSFETs on the secondary side are calculated as

$$P_{idc,con,sec} = 2 \sum_{i=1}^n \left(\frac{\pi}{2} \frac{P_{inv,out(i)}}{U_z} \frac{1}{\cos(\theta)} \right)^2 R_{on,irf}. \quad (3.49)$$

The calculation of the switching losses is similar to multi-cell inverter losses calculation. With reference to the lumped winding resistance of the transformer determined in (3.23), hence the transformer conduction losses are

$$P_{idc,tr,Cu} = \sum_{i=1}^n \left(\frac{N_2}{N_1} \frac{\pi}{\sqrt{2}} \frac{P_{inv,out(i)}}{U_z} \frac{1}{\cos(\theta)} \right)^2 R_w. \quad (3.50)$$

According to the material datasheet of Epcos N87, the core losses of EFD 30/15/9 at 140 kHz and $\Delta B = 173$ mT are 0.4 W. Thus the total core losses are

$$P_{idc,tr,Fe} = 10 \times 0.4W = 4 W. \quad (3.51)$$

Once the transformer is defined, the core losses are only dependant on the amplitude and shape of the applied voltage. In this circuit, we use a fixed input voltage and a fixed 50% duty cycle, hence the core losses stay constant.

3.4.4 Circuit Parameters

The circuit parameters used for system losses calculation are listed in Table 3.3. Most of them are given in the device datasheets [65]-[66]. The MOSFETs employed in the secondary side of the dc-dc converter are same as the MOSFETs employed in the multi-cell inverter, therefore for the converter secondary side only the gate resistances of the MOSFETs are listed.

Table 3.3: Circuit Parameters for System Losses Calculation.

	Parameters	Denotation	Values	Comments
LPA	LPA supply voltage	U_a	30 V	For 270 V output voltage range
	MOSFET on resistance	R_{on}	10 m Ω	
Multi-cell Inverter	Gate supply voltage	U_{gs}	12 V	
	MOSFET turn-on threshold voltage	U_{th}	4 V	IRF6648
	MOSFET Miller voltage	U_m	5.6 V	IRF6648
	Gate turn-on resistor	R_{gon}	6.6 Ω	Including output resistor of gate driver IC LM101AM
	Gate turn-off resistor	R_{goff}	6.6 Ω	Including output resistor of gate driver IC LM101AM
	Total gate charge	Q_{th}	6.5 nC	Gate voltage rises to U_{th} , IRF6648, $U_{ds} = 48$ V
	Total gate charge	Q_{m1}	9 nC	Gate voltage rises to U_m , IRF6648, $U_{ds} = 48$ V
	Total gate charge	Q_{m2}	27 nC	Gate voltage at end of Miller effect, IRF6648, $U_{ds} = 48$ V
	Output capacitance	C_{oss}	420 pF	IRF6648, $U_{ds} = 40$ V
	Specified reverse recovery time	$t_{rr,spec}$	47 ns	Body diode of IRF6648
	Specified reverse recovery charge	$Q_{rr,spec}$	56 nC	Body diode of IRF6648
	Specified forward current	$I_{F,spec}$	17 A	Body diode of IRF6648
	Specified di/dt	$didt_{,spec}$	100 A/ μ s	Body diode of IRF6648

	Switching frequency	f_{sw}	140 kHz	
dc-dc convert (primary)	Gate supply voltage	U_{gs}	12 V	
	MOSFET turn-on threshold voltage	U_{th}	4 V	SPP20N60CFD
	MOSFET Miller voltage	U_m	7 V	SPP20N60CFD
	Gate turn-on resistor	R_{gon}	11 Ω	Including output resistor of gate driver IC LM101AM
	Gate turn-off resistor	R_{goff}	6 Ω	Including output resistor of gate driver IC LM101AM
	Total gate charge	Q_{th}	17 nC	Gate voltage rises to U_{th} , SPP20N60CFD
	Total gate charge	Q_{m1}	30 nC	Gate voltage rises to U_m , SPP20N60CFD
	Total gate charge	Q_{m2}	80 nC	Gate voltage at end of miller effect, SPP20N60CFD
	Output capacitance	C_{oss}	70 pF	SPP20N60CFD, $U_{ds} = 400$ V
	Specified reverse recovery time	$t_{rr,spec}$	150 ns	Body diode of SPP20N60CFD
	Specified reverse recovery charge	$Q_{rr,spec}$	1 μ C	Body diode of SPP20N60CFD
	Specified forward current	$I_{F,spec}$	20.7 A	Body diode of SPP20N60CFD
	Specified di/dt	$didt_{,spec}$	100 A/ μ s	Body diode of SPP20N60CFD
dc-dc convert (secondary)	Gate turn-on resistor	R_{gon}	11 Ω	Including output resistor of gate driver IC LM101AM
	Gate turn-off resistor	R_{goff}	6 Ω	Including output resistor of gate driver IC LM101AM

3.5 System Dimensioning

3.5.1 System Loss Comparison with Class-AB Power Amplifier

To show the system loss reduction of the H-MCA over the conventional class-AB mode power amplifier, the losses of these two systems have to be compared. Here when calculating the losses of a class-AB power amplifier,

the input isolated dc supply stage losses are not counted. Therefore the losses of the isolated dc-dc converter are also not included in the H-MCA losses for reasons of fair comparison.

The losses in the output power transistors of a conventional class-AB mode power amplifier are [49]

$$P_{loss,lin} = \frac{U_{op}}{\pi Z_L} \left(2V_{CC} - \frac{1}{2} \pi U_{op} \cos \varphi \right), \quad (3.52)$$

where V_{CC} is the positive DC power supply voltage of a conventional class-AB mode power amplifier.

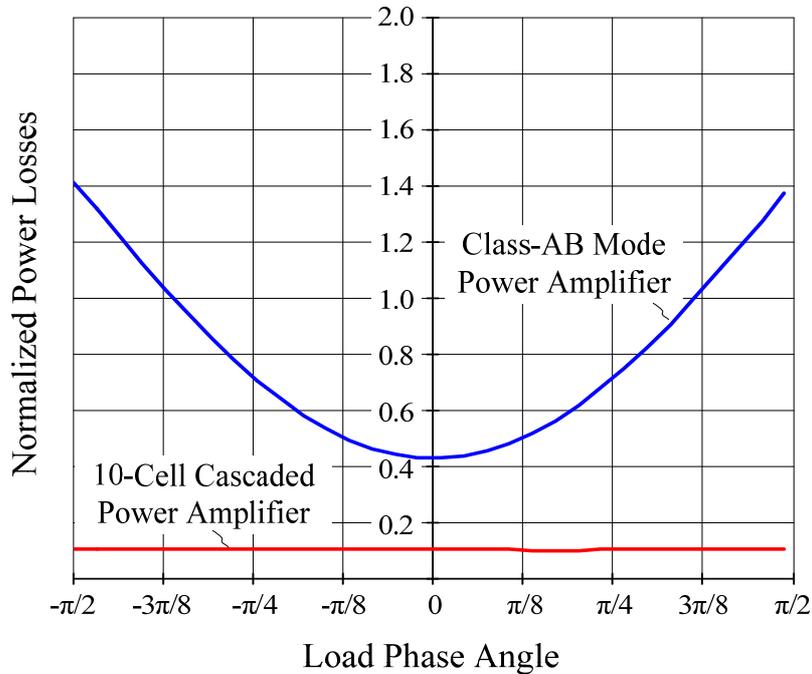


Figure 3.33: Comparison of the calculated normalized power losses, P_{loss} / P_o^* , of class-AB mode power amplifier and 10-cell cascaded power amplifier in dependency on load phase angle φ . Operating parameters: $U_{o,rms} = 270\text{V}$, $Z_L = 60 \Omega$, $f_o = 5\text{kHz}$, $U_z = 40 \text{V}$, $U_a = 30 \text{V}$, $V_{CC} = 400 \text{V}$. For circuit parameters refer to Table 3.3.

Figure 3.33 compares the calculated normalized power losses (P_{loss} / P_o^*) of a class-AB power amplifier and a 10-cell cascaded power, where the normalization base of the power is $P_o^* = U_{op,max}^2 / (2Z_L)$ and $U_{op,max} = 382 \text{V}$. It is shown that the cascaded power amplifier has a significant loss reduction in

contrast to a class-AB power amplifier, furthermore the power losses of the class-AB power amplifier increase dramatically in the case of inductive or/and capacitive loads, while the losses of the cascaded power amplifier are nearly constant.

The dependency of the normalized power losses on the output rms voltage U_o is depicted in Figure 3.34. For the complete range of the output voltage the losses of the cascaded power amplifier are not higher than one-third of the losses of the class-AB power amplifier.

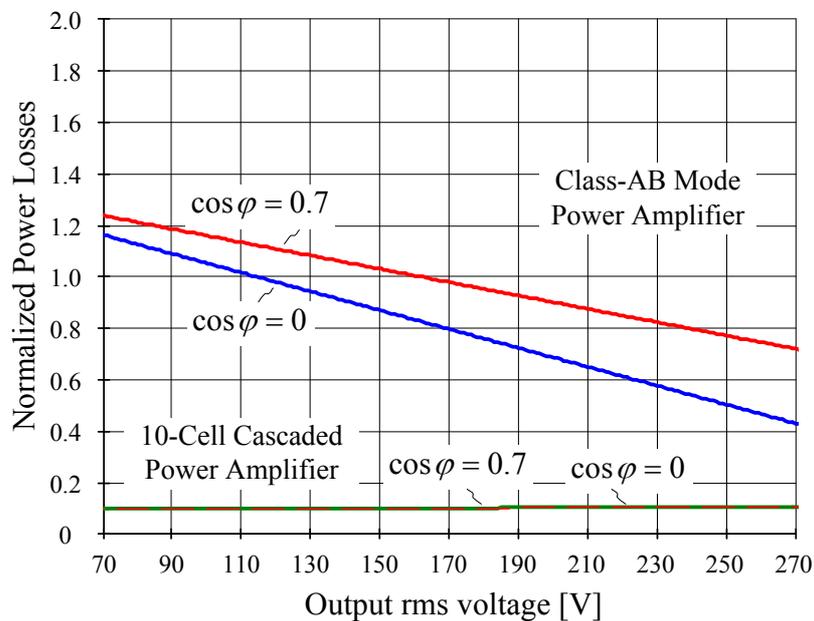


Figure 3.34: Comparison of the calculated normalized power losses, P_{loss} / P_o^* , of class-AB mode power amplifier and 10-cell cascaded power amplifier in dependency on output rms voltage U_o . Operating parameters: $I_{o,rms} = 4.5$ A, $f_o = 5$ kHz, $U_z = 40$ V, $U_a = 30$ V, $V_{CC} = 400$ V. For circuit parameters refer to Table 3.3.

3.5.2 System Efficiency

According to the selected components, the calculated efficiency (dependent on output rms voltage U_o) of a 10-cell cascaded power amplifier is shown in Figure 3.35. It is shown that the cascaded power amplifier has a good efficiency over a wide output voltage range while a conventional linear power amplifier will only have a maximum efficiency of 78.5% theoretically.

The calculated power loss distribution in the 10-cell cascaded power amplifier system is shown in Figure 3.36. The LPA losses are dominant, i.e., 66% of the total system losses. The losses of the multi-cell inverter are very small: the conduction losses are the main losses since the switching losses at 5 kHz are so small that they can be even neglected.

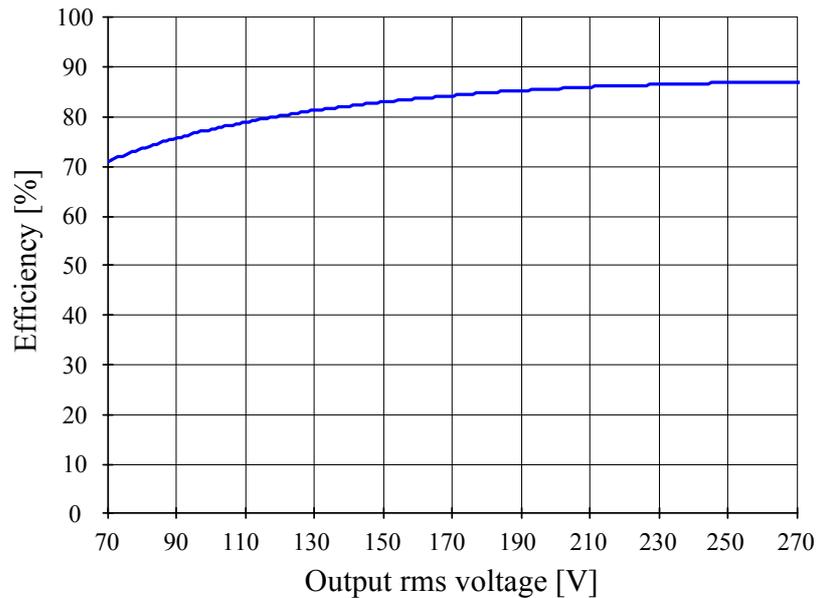


Figure 3.35: Calculated efficiency of the 10-cell cascaded power amplifier in dependency on output rms voltage U_o . The operation parameters are: $I_{o,rms} = 4.5$ A, $\varphi = 0^\circ$, $f_o = 5$ kHz, $U_z = 40$ V, $U_a = 30$ V. For circuit parameters refer to Table 3.3.

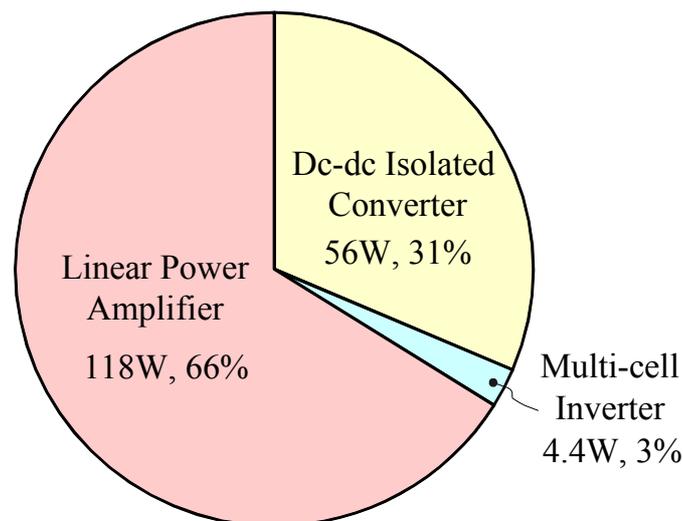


Figure 3.36: Calculated power losses distribution of the 10-cell cascaded power amplifier. The operation parameters are: $U_{o,rms} = 270$ V, $Z_L = 60 \Omega$, $\varphi = 0^\circ$, $f_o = 5$ kHz, $U_z = 40$ V, $U_a = 30$ V. For circuit parameters refer to Table 3.3.

3.5.3 Thermal Balance

Since the H-bridge cells are not simultaneously switched to the load (see Figure 3.1), the output power requirement of each cell is different. The comparison of the output power of the different cells for the 10-cell inverter is illustrated in Figure 3.37, where it is clearly shown that the earlier the cell unit is switched on the more power it contributes. Since the thermal stresses of the cells and the corresponding dc-dc converter stages are different, a thermal management strategy must be utilized to equalize the thermal stresses among the cells. A simple management strategy, which does not require any additional hardware, can be employed. The main idea is to derive a simplified thermal model of the cell, and then calculate the power losses of each cell unit by using a central digital signal processor. The sequencing of the cells is made based on the estimated semiconductor junction temperatures, such that the cell units are switched in the inverse sequence to the semiconductor junction temperature during the next output period.

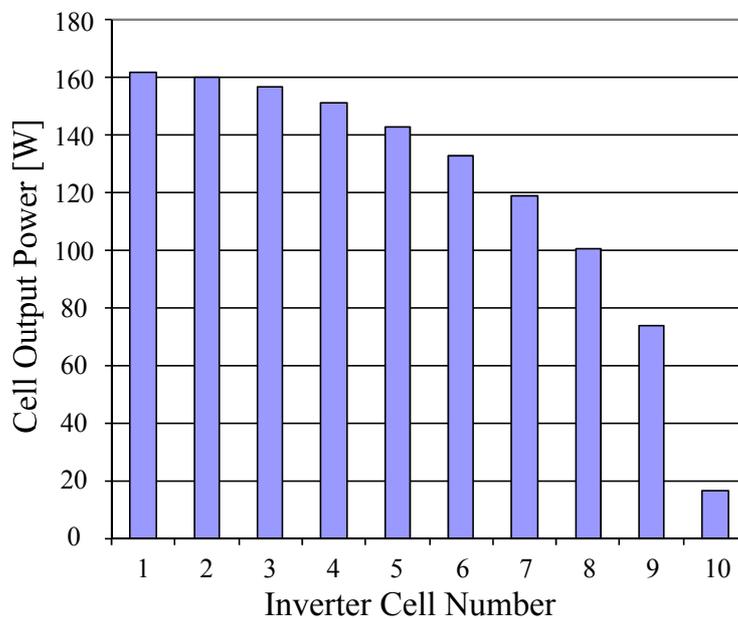


Figure 3.37: Comparison of the output power of the different cells of the 10-cell inverter. The operation parameters are: $Z_L = 60 \Omega$, $\varphi = 0^\circ$, $f_o = 5\text{kHz}$, $U_{o,rms} = 270 \text{V}$, $U_z = 40 \text{V}$, $U_a = 30 \text{V}$.

3.6 Control Design

3.6.1 Overview of System Control

The H-MCA system control scheme realized in the hardware is shown in Figure 3.38. The power components are listed in Table 5.3. The complete system employs mixed mode control: analog control and digital control. The analog control part contains the output voltage control and the multi-cell inverter switching signals determination. Since a commercial linear power amplifier APEX MP111 with the power bandwidth of 500 kHz is employed, as shown in Figure 5.6, the complete feedback for the output voltage control loop utilizes the analog circuit in order not to impair the system dynamic performance. The reason to use the fast analog comparators which directly compare the reference signal with threshold voltage levels is to minimize the delay time. On the other hand, many functions like PWM generation, protection and monitoring etc., are realized digitally, which provides great flexibility and convenience to operate and/or modify the system. The input signals of all the 49 gate driver units are directly connected to the buffer arrays which are connected to the FPGA output signals. Functionally also the gate driver input signals of the multi-cell inverter could be connected to the outputs of the analog comparators. However advantages of having a FPGA board controlling all the gate signals are: (i) the control strategy is compatible with the control implementation of the other two amplifier topologies and (ii) the system is able to turn off all the gating signals in the case of a protection signal. Furthermore the comparator threshold reference levels are generated by TrimDAC which can be digitally set from the DSP.

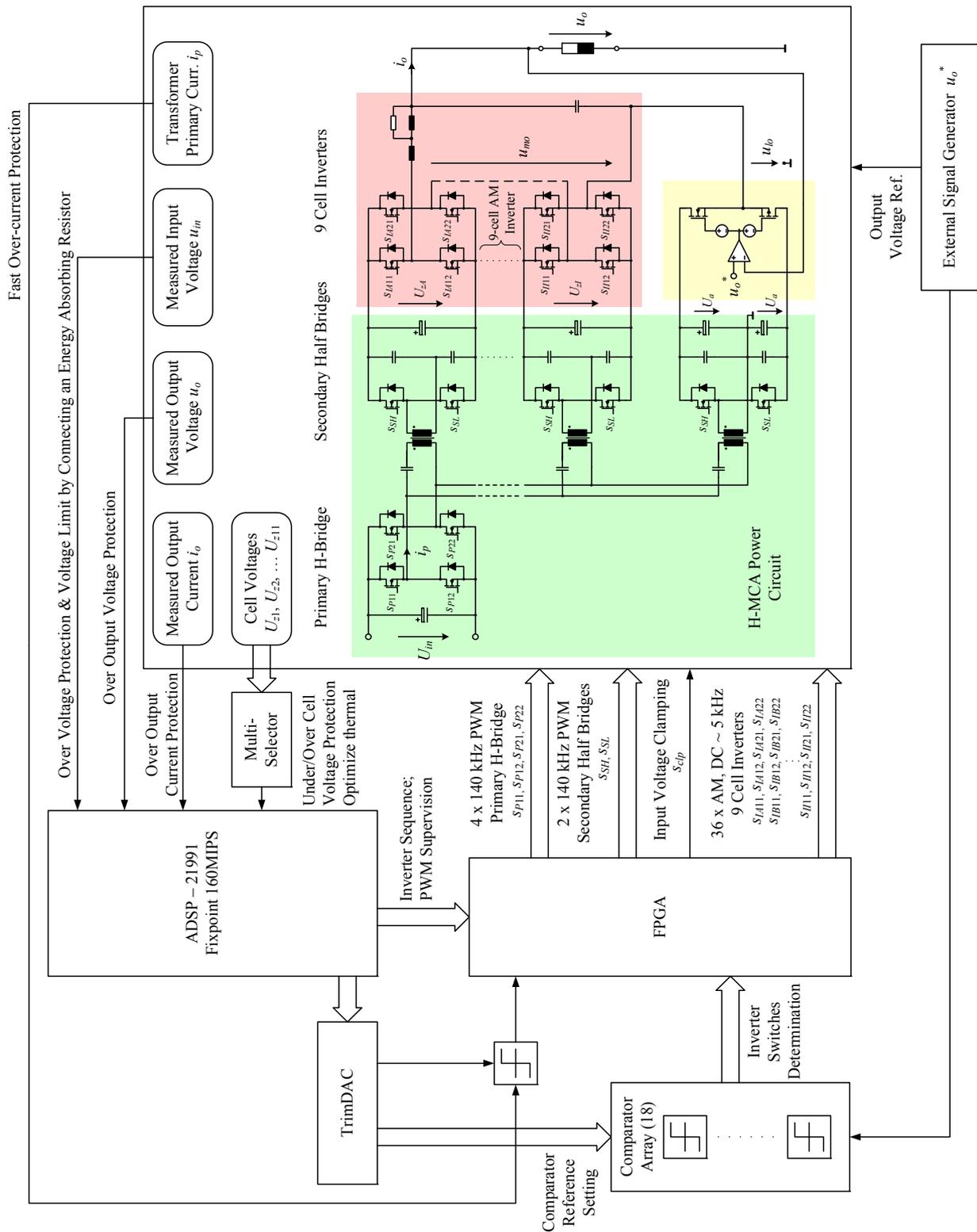


Figure 3.38: System control scheme of a H-MCA. Mixed control: output voltage control by analog; system protection and monitoring are realized digitally.

3.6.2 Apex MP111D Model

Before designing the system feedback loop, first the open-loop function of MP 111D, which is defined from the differential input voltage u_{ed} to the amplifier output voltage u_{lo} , has to be measured. As mentioned the analog amplifier small signal characters are highly dependent on the devices parameters and dc operating points, e.g., the drain-to-source voltage of the transistors in the output stage. Therefore the open-loop function $v_g(s)$ is measured for different output voltages at the fixed supply voltages.

The measured Bode plots of the open-loop function $v_g(s)$ for positive output

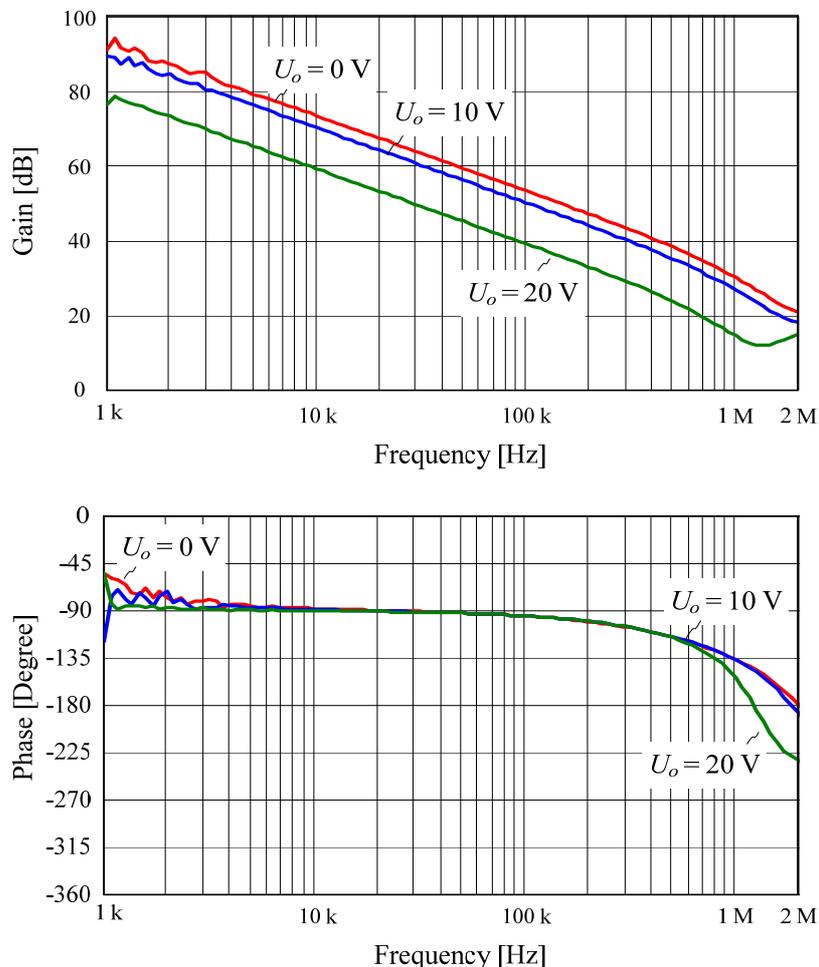


Figure 3.39: Comparison of measured APEX MP111D open-loop transfer function for three different positive output voltages: 0 V, 10 V and 20 V. Operation parameters: $V_{cc} = \pm 30$ V, $C_{dom} = 11$ pF, $R_L = 3.3$ k Ω .

voltages, i.e., when the upper N-channel MOSFET is conducting, are illustrated in Figure 3.39. There the gain of $v_g(s)$ is decreased for higher output voltage, i.e., less voltage drop occurs across the conducting transistor. E.g., the gain of $v_g(s)$ for $U_o = 20$ V is about 15 dB less than that when $U_o = 0$ V. Figure 3.40 depicts the measured Bode plots of the open-loop function $v_g(s)$ in the case of negative output voltage, i.e., the lower side P-channel MOSFET is conducting. Interestingly the open-loop function shows a very similar character for the different output voltages, 0 V, -10 V and -20 V.

Regarding the measurements above, we have to consider the open-loop transfer function when $U_o = 0$ V that has the highest gain for control loop

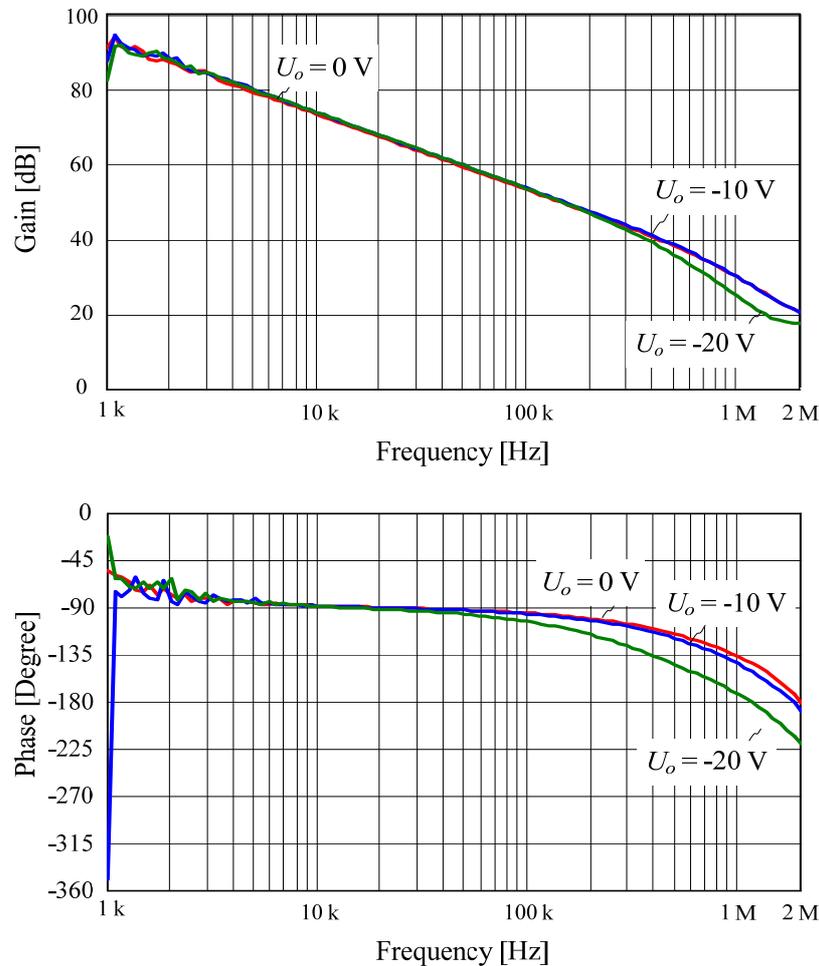


Figure 3.40: Comparison of measured APEX MP111D open-loop transfer function for three different negative output voltages: 0 V, -10 V and -20 V. Operation parameters: $V_{cc} = \pm 30$ V, $C_{dom} = 11$ pF, $R_L = 3.3$ k Ω .

design in order to guarantee system stability for the full output voltage range. The open-loop transfer function has been measured also for different load conditions; however it shows that the load in the range from 30Ω to $10 \text{ k}\Omega$ has very limited influence and therefore it is neglected.

As described in [37], the dominant factors affecting the open-loop transfer function are the input stage transconductance g_i and the so-called dominant capacitor C_{dom} . The value of g_i is determined by the input differential stage design. The capacitor C_{dom} is the negative feedback capacitor of the voltage amplifying stage. For MP 111D, C_{dom} can be varied by external capacitors. Therefore the open-loop transfer function can be defined as

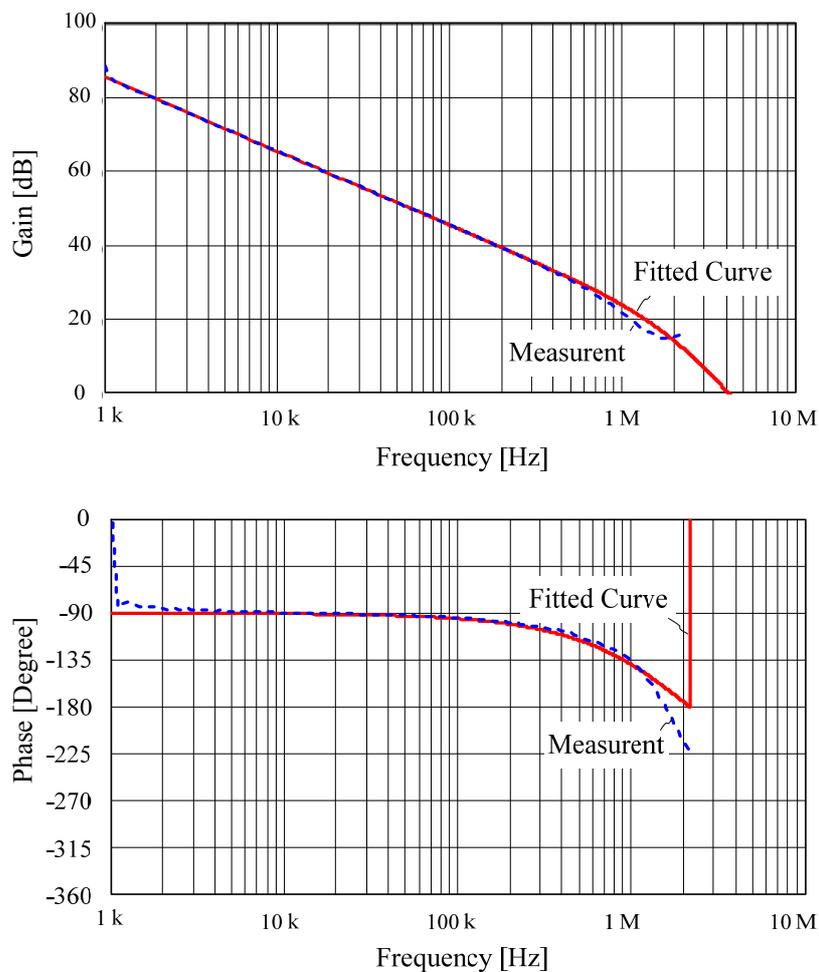


Figure 3.41: Comparison of measured and fitted Bode plots of APEX MP111D open-loop transfer function $v_g(s)$. Operation parameters: $V_{cc} = \pm 30 \text{ V}$, $C_{dom} = 34 \text{ pF}$, $R_L = 3.3 \text{ k}\Omega$.

$$v_g(s) = \frac{g_i}{C_{dom}s} \frac{1}{\tau_1 s + 1} \frac{1}{\tau_2 s + 1}, \quad (3.53)$$

where the τ_1 and τ_2 represent the high frequency poles caused by the parasitic circuit parameters of the output stage.

The comparison of measured and fitted Bode plots of the APEX MP111D open-loop transfer function $v_g(s)$ by using (3.53) are illustrated in Figure 3.41, where $g_i = 3.9$ mA/V, $C_{dom} = 34$ pF, and $\tau_1 = \tau_2 = 0.46$ μ s. The fitted curve shows a good match with the measured curve up to 1 MHz.

3.6.3 dv/dt Filter

For use in high frequency applications, particular attention has to be put on the component parasitic parameters when selecting the dv/dt filter components. The output impedance of the multi-cell inverter (including the dv/dt filter) is considered as a part of the system feedback loop as shown in Figure 3.45. The equivalent circuit diagram of the output impedance of the complete multi-cell inverter is shown in Figure 3.42(a), where $R_{mc} = 9 \times 2 \times R_{on,irf}$ is the total on-resistance of the inverter MOSFETs and the isolated dc-dc converter is only considered as an ideal dc source because of the large dc link capacitors. This circuit diagram with the parasitic parameters of the dv/dt filter is depicted in Figure 3.42(b). These parameters are obtained by fitting the impedance of the lumped RLC circuit models to the data measured by HP 4294A precision impedance analyzer. The output impedance Z_{mo} of the complete multi-cell inverter can be derived as

$$Z_{mo}(s) = (Z_{LF}(s) + Z_{Ld}(s) \parallel R_d + R_{mc}) \parallel Z_{CF}(s). \quad (3.54)$$

The impedances of all the LC components of the dv/dt filter, C_F , L_F , and L_d , are shown in Figure 3.43; the first resonant frequency of each component is higher than 2 MHz. Therefore the parasitic parameters of the dv/dt filter should not impact the system control design.

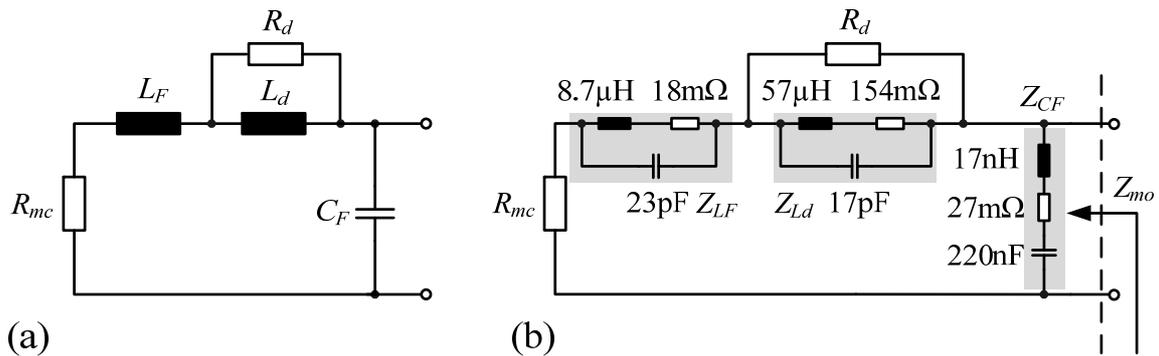


Figure 3.42: Schematic components which dominate the output impedance of the complete multi-cell inverter: neglecting the parasitic parameters of dv/dt filter (a) and including the parasitic parameters of dv/dt filter (b).

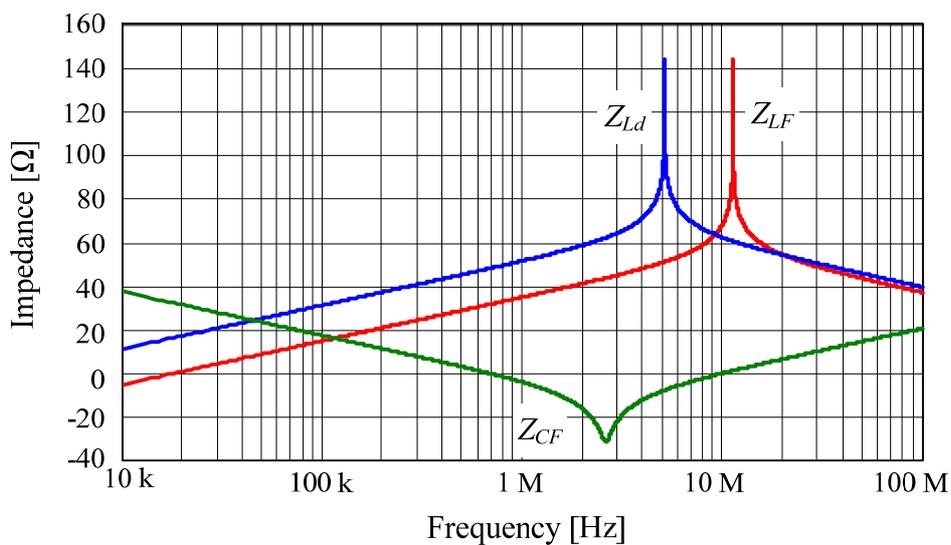


Figure 3.43: Impedance of each LC component of dv/dt filter, C_F , L_F , and L_d .

3.6.4 Control Design

For system control design, at first ideal voltage sources are assumed to substitute the dc-dc isolated converter because the output impedance of the dc-dc converter is negligible considering the system control design. The simplified H-MCA circuit scheme is shown in Figure 3.44, where we see actually the multi-cell inverter is in the feedback loop and therefore the output im-

pedance of the complete multi-cell inverter including the dv/dt filter has to be considered for the control design.

In the hardware realization, the electric path from the system output voltage to the negative input pin of MP 111D including R_2 should be well shielded. Here, a coaxial cable with the embedded resistor R_2 to connect these two points directly is used.

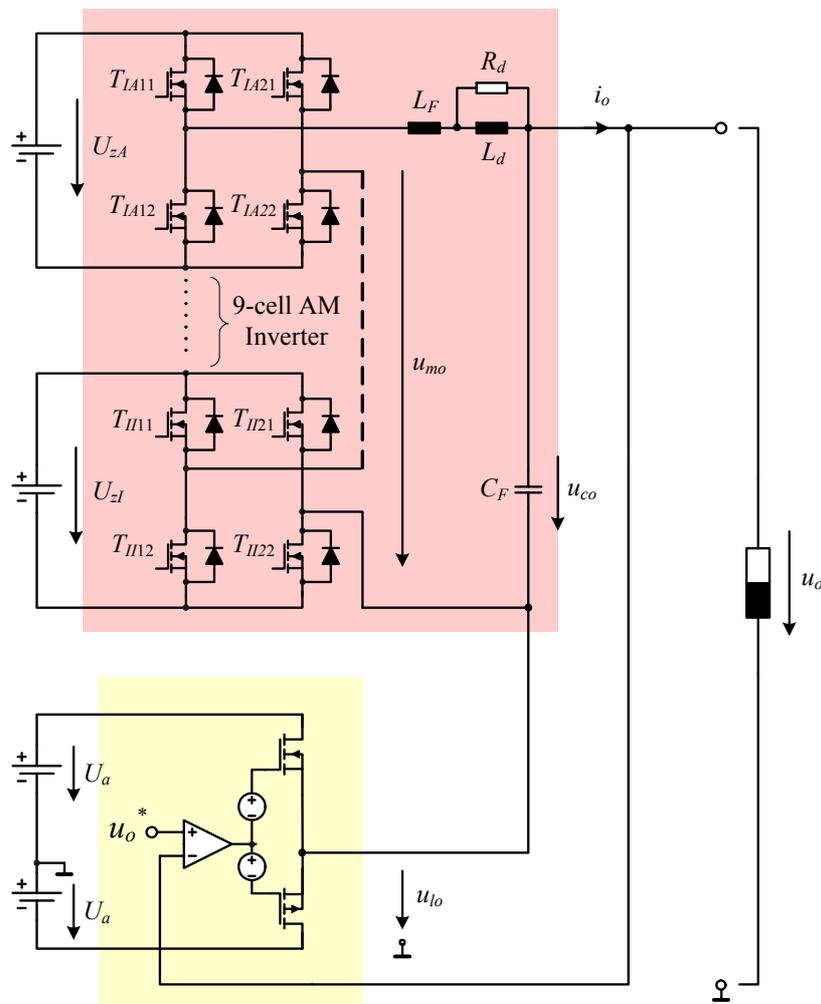


Figure 3.44: Simplified H-MCA scheme by replacing the dc-dc isolated converter with ideal voltage sources.

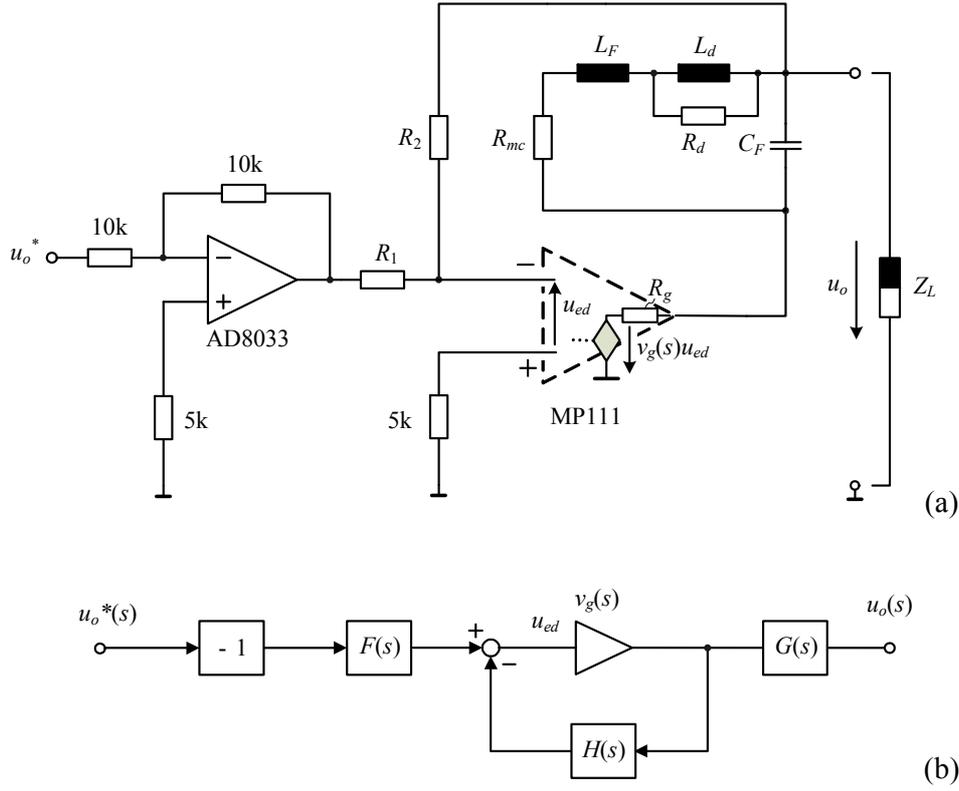


Figure 3.45: Circuit scheme (a) and control block scheme (b) for H-MCA output voltage control design.

The circuit scheme for the H-MCA output voltage control design is shown in Figure 3.45 (a), where the multi-cell inverter is replaced by the output impedance network Z_{mo} and the MP 111D is replaced by a voltage-controlled voltage source with its output resistance $R_g = 3 \Omega @DC$ [67]. The front-end inverter is used to provide the inverting function and possible scaling function if needed for the reference voltage u_o^* . Since AD8033 has such a high bandwidth of 80 MHz, this inverter is considered to be ideal. For the circuit diagram shown in Figure 3.45 (a), the control block diagram as depicted in Figure 3.45 (b) is derived [68]. In this diagram, the feed-forward transfer function $F(s)$ is defined as

$$F(s) = -\frac{R_2 + Z_{mo}(s) + R_g}{R_1 + R_2 + Z_{mo}(s) + R_g}, \quad (3.55)$$

and the feedback transfer function $H(s)$ is

$$H(s) = \frac{R_1}{R_1 + R_2 + Z_{mo}(s) + R_g}. \quad (3.56)$$

Even the MP 111D output and system output are only coupled via a relatively low impedance network Z_{mo} compared to R_2 ; there is a small voltage difference considering the small signal values. Therefore a correction function $G(s)$ is given as

$$G(s) = \frac{R_1 + R_2}{R_1 + R_2 + Z_{mo}(s) + R_g}. \quad (3.57)$$

The system open-loop function with feedback loop G_{open} is

$$G_{open}(s) = v_g(s)H(s). \quad (3.58)$$

Finally the closed-loop input-to-output transfer function $G_{io,cls}$ is calculated as

$$G_{io,cls}(s) = \frac{u_o(s)}{u_o^*(s)} = -F(s)G(s) \frac{v_g(s)}{1 + v_g(s)H(s)}. \quad (3.59)$$

The closed-loop output impedance $Z_o(s)$ is

$$Z_o(s) = \frac{Z_{mo}(s) + R_g}{1 + v_g(s)H(s)} \quad (3.60)$$

When the load Z_L is connected, the closed-loop transfer function $G_{io,cls}$ should be modified because of the system output impedance. Therefore $G_{io,cls}$ is rewritten as

$$G_{io,cls}(s) = -F(s)G(s) \frac{v_g(s)}{1 + v_g(s)H(s)} \frac{Z_L(s)}{Z_L(s) + Z_o(s)}. \quad (3.61)$$

The control design for H-MCA is quite simple because one only has to vary the following parameters:

- The external capacitor C_{dom}

- Feedback factor determined by R_1 and R_2 .

For a practical trade-off between system stability and dynamic behaviour, $C_{dom} = 33$ pF, $R_1 = 5$ k Ω and $R_2 = 200$ k Ω are selected for the control design. The Bode plot of the system open-loop transfer function $G_{open}(s)$ is shown in Figure 3.46, where the design control system achieves a crossover frequency of 460kHz and a phase margin of 68°.

The measured and calculated Bode plots of the system closed-loop input-to-output transfer function are compared in Figure 3.47. These two curves are perfectly matching up to 2 MHz. From the measured data, we can see that the closed-loop control system has a bandwidth of 570 kHz (at 32dB – 3dB =

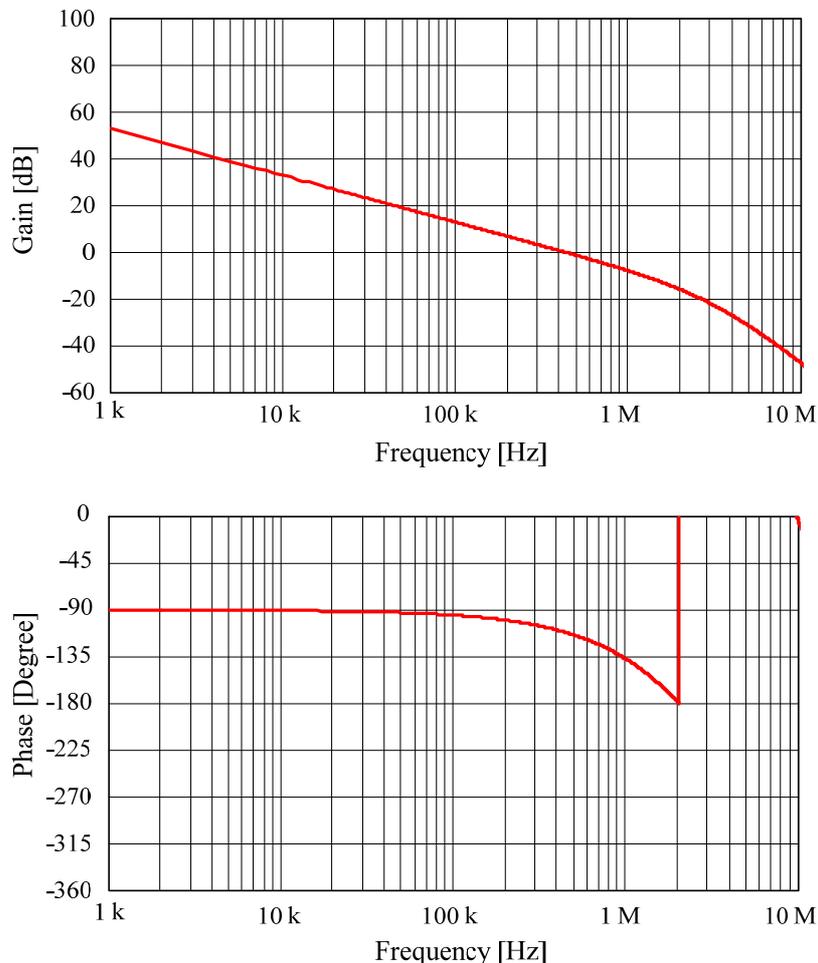


Figure 3.46: Bode plot of system open-loop transfer function. The controlled system has a crossover frequency of 460kHz and phase margin of 68°. Operation parameters: $V_{cc} = \pm 30$ V, $U_o = 0$ V.

29 dB).

Figure 3.48 compares the calculated and measured system small-signal output impedance, and verifies a very good matching of the both Bode plots.

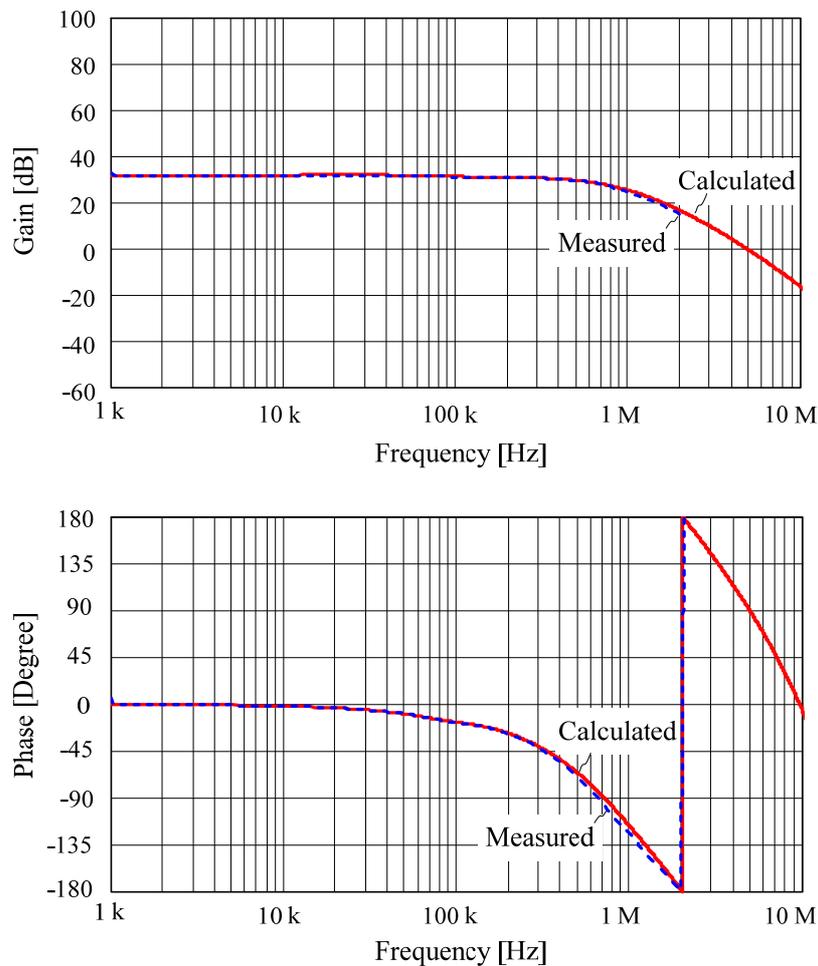


Figure 3.47: Comparison of measured and calculated Bode plots of system closed-loop small signal input-to-output transfer function. Operation parameters: $U_o = 120$ V, $C_{dom} = 34$ pF, $R_L = 35$ Ω , $U_a = 30$ V.

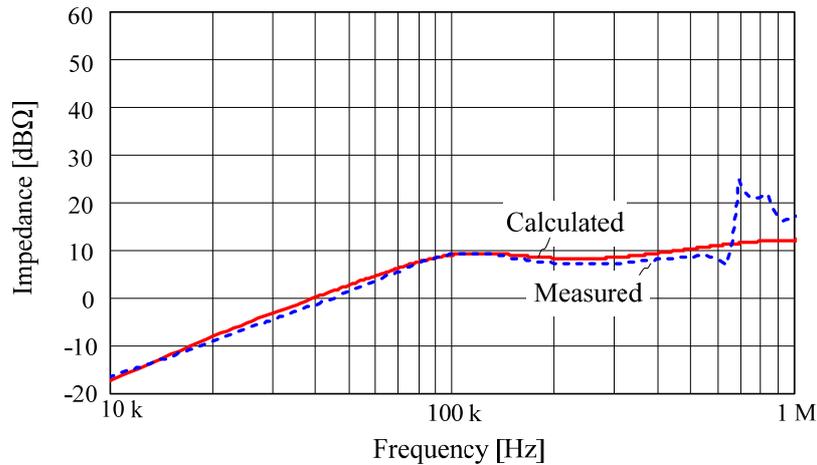


Figure 3.48: Comparison of measured and calculated Bode plots of system output impedance. Operation parameters: $U_o = 120$ V, $C_{dom} = 34$ pF, $R_L = 35$ Ω, $U_a = 30$ V.

3.7 Experimental Results

For verifying the system analysis, a laboratory prototype was built. The descriptions of the prototype and components list are given in Chapter 5. For the measurements, the test conditions comply with the 135 V output voltage range as specified in Table 5.1. The principal concept of the H-MCA is to use a high slew rate LPA to compensate the voltage difference between the output voltage and the stair-shaped voltage generated by the multi-cell inverter.

Figure 3.49 shows the zoom in measurement of u_{co} , u_{lo} and u_o for the nominal operating point. As demonstrated in this figure, each time u_{co} generates the stepped voltage, u_{lo} responds immediately with an inverse voltage step. Therefore, by summing these two voltages we can have a smooth output voltage u_o . Due to the limited system bandwidth of 580 kHz, the compensation cannot be perfect. The small ditches occurring in output voltage are caused by system regulation. A custom-designed LPA with higher bandwidth and feed-forward control could improve the regulation performance.

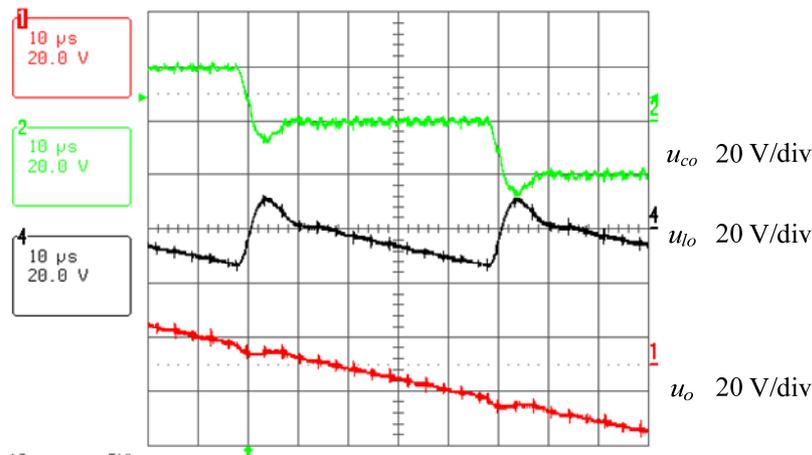


Figure 3.49: Measured performance of the LPA output voltage u_{lo} compensating the stepped shape of dv/dt filter output voltage u_{co} . Operation parameters: $U_{in} = 200$ V, $f_s = 140$ kHz, $U_{o,rms} = 115$ V, $R_L = 35$ Ω , $f_o = 1$ kHz, $U_a = 30$ V.

The measured time behaviours of the LPA output voltage u_{lo} , dv/dt filter output voltage u_{co} , output voltage u_o , and output current i_o for the three different rms output voltages $U_{o,rms}$, 70 V, 100 V and 130 V, are shown in Figure 3.50. In the full output voltage range, H-MCA is able to produce clear sinusoidal output voltages. And the measurements show the number of switch-on inverter cells in dependency on the amplitude of the output voltage, i.e., 5 switch-on inverter cells and/or 11 levels for $U_{o,rms} = 70$ V, 7 switch-on inverter cells and/or 15 levels for $U_{o,rms} = 100$ V, and 9 switch-on inverter cells and/or 19 levels for $U_{o,rms} = 130$ V. This relation is in line with the analysis.

Experimental results of the H-MCA generating a nominal output voltage 115 V for different load conditions, ohmic, inductive and capacitive loads, are shown in Figure 3.51, where it is seen that H-MCA can supply non-ohmic loads without any system stability problem.

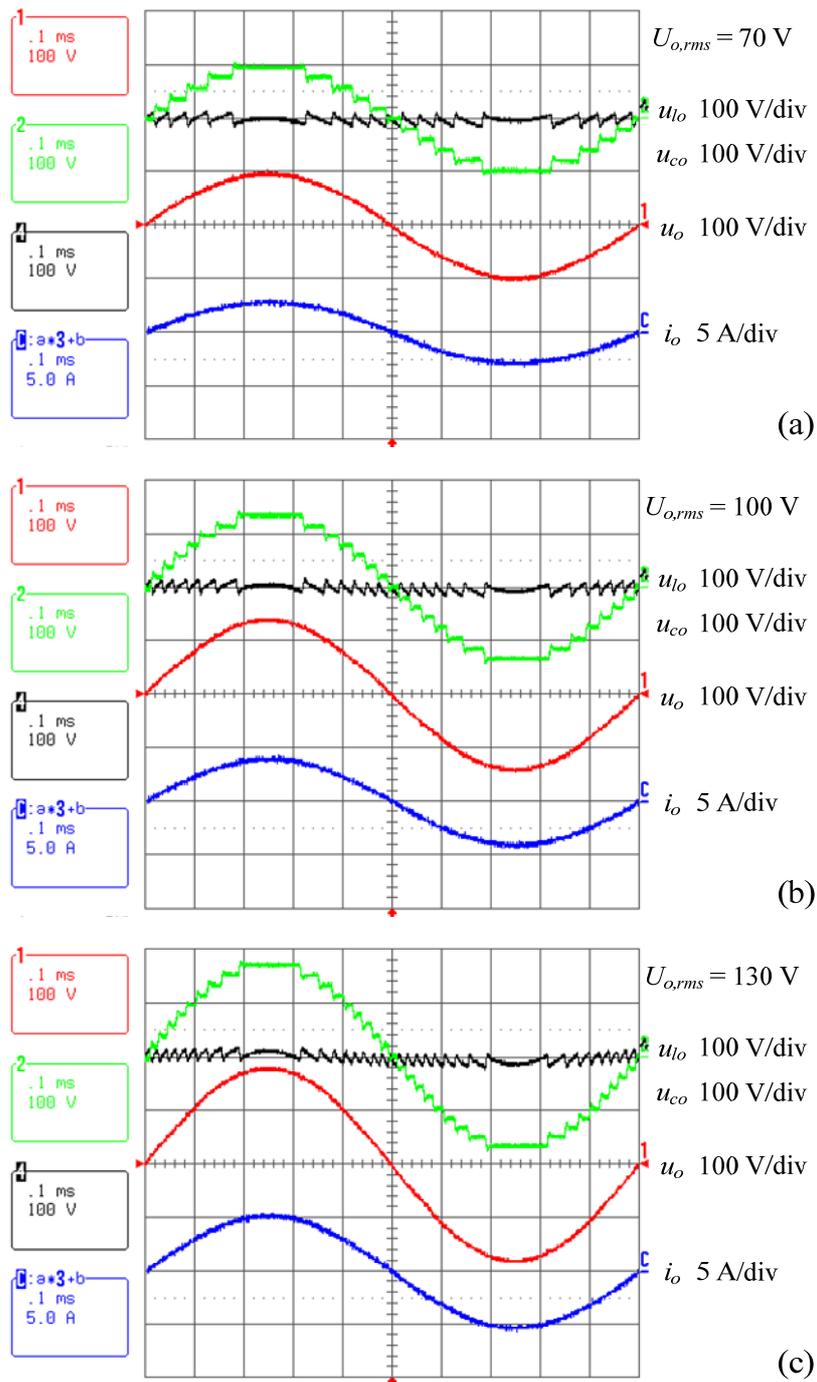


Figure 3.50: Measured time behaviours of the LPA output voltage u_{lo} , dv/dt filter output voltage u_{co} , output voltage u_o , and output current i_o for three different rms output voltage $U_{o,rms}$: 70 V (a), 100 V (b) and 130 V (c). Operation parameters: $U_{in} = 200 \text{ V}$, $f_s = 140 \text{ kHz}$, $R_L = 35 \Omega$, $f_o = 1 \text{ kHz}$, $U_a = 30 \text{ V}$.

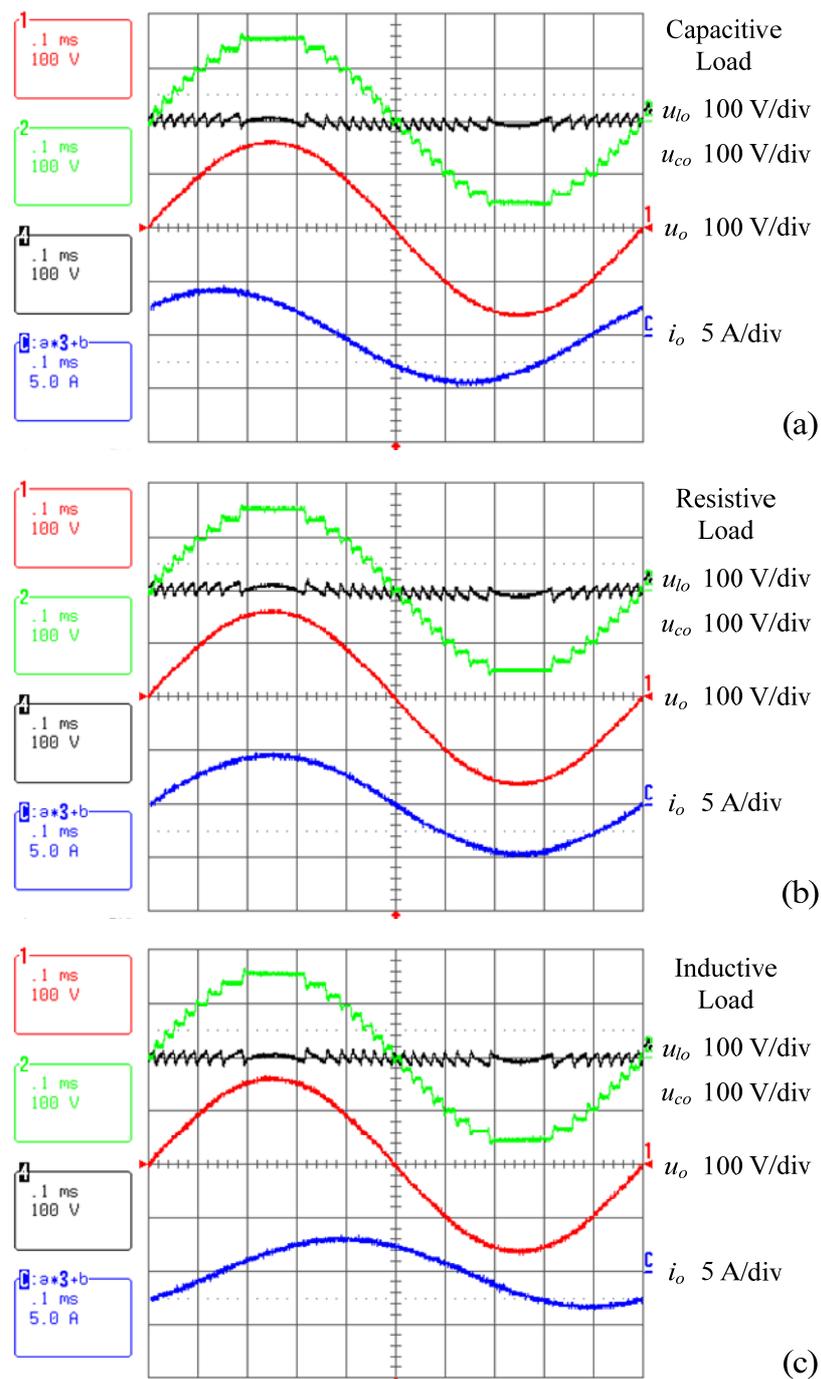


Figure 3.51: Measured time behaviours of the LPA output voltage u_{lo} , dv/dt filter output voltage u_{co} , output voltage u_o , and output current i_o for three different load conditions: capacitive load, 6.6 μF and 35 Ω in series (a), ohmic load, $R_L = 35 \Omega$ (b) and inductive load 2.5 mH and 35 Ω in series (c). Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_s = 140 \text{ kHz}$, $f_o = 1 \text{ kHz}$, $U_a = 30 \text{ V}$.

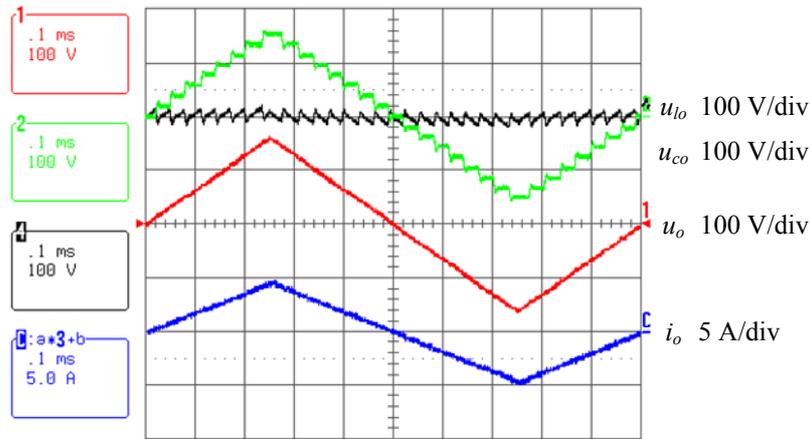


Figure 3.52: Experimental results for generating a triangular output waveform. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{op} = 162 \text{ V}$, $f_s = 140 \text{ kHz}$, $R_L = 35 \Omega$, $f_o = 1 \text{ kHz}$, $U_a = 30 \text{ V}$.

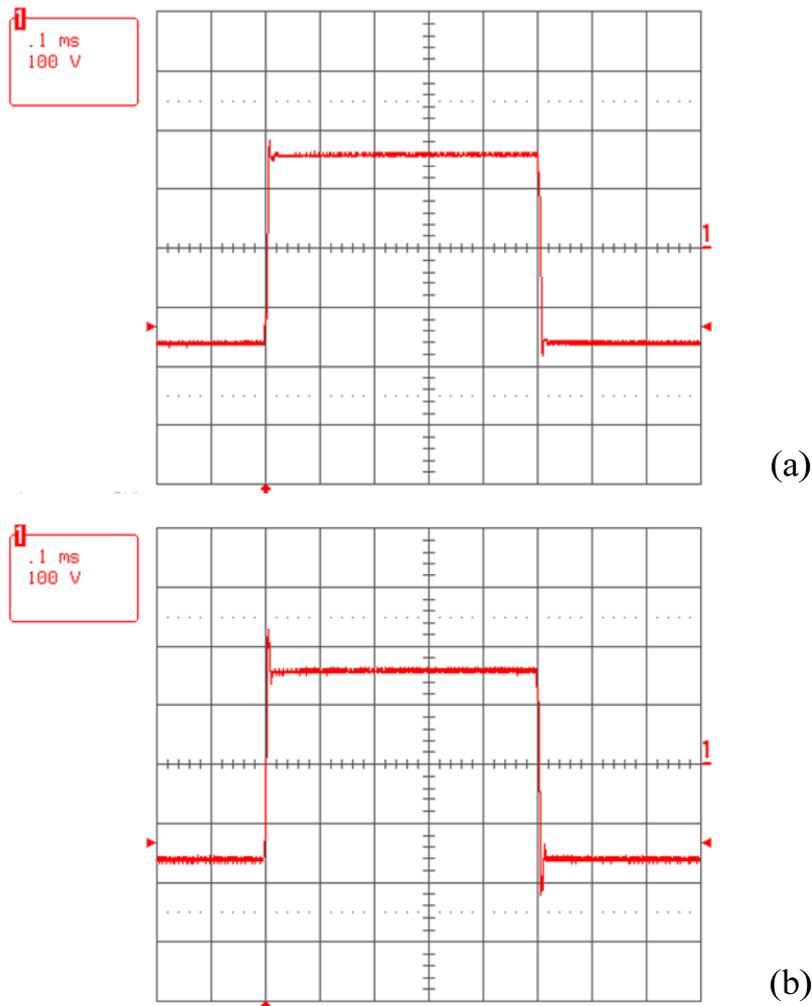


Figure 3.53: Experimental results for generating square-shaped output waveform connected with nominal load, $R_L = 35 \Omega$ (a) and no-load (b). Operation parameters: $U_{in} = 200 \text{ V}$, $U_{op} = 162 \text{ V}$, $f_s = 140 \text{ kHz}$, $f_o = 1 \text{ kHz}$, $U_a = 30 \text{ V}$.

In order to check if the H-MCA is able to generate random waveforms, triangular and rectangular signals are selected. Figure 3.52 demonstrates the experimental results for generating a 1 kHz triangular output waveform, where the system outputs a crisp triangular waveform with sharp corners.

The measured rectangular output waveforms are shown in Figure 3.53. There the voltage overshoot for nominal load, $R_L = 35 \Omega$ is about 20 V and for the no-load condition about 60 V. The overshoot voltage can be reduced by employing a dv/dt filter with higher damping effect.

In testing power source applications, it is usual to test a non-linear load, e.g., with computer power supplies, etc.. The experimental results for supplying a non-linear load are shown in Figure 3.54, where the output current surges to 9 A and the output voltage quality is not impaired. For this test, a circuit of a full bridge rectifier followed by a 2.5 mH inductor in series with a parallel-connected 100 μ F capacitor and 35 Ω resistor is employed.

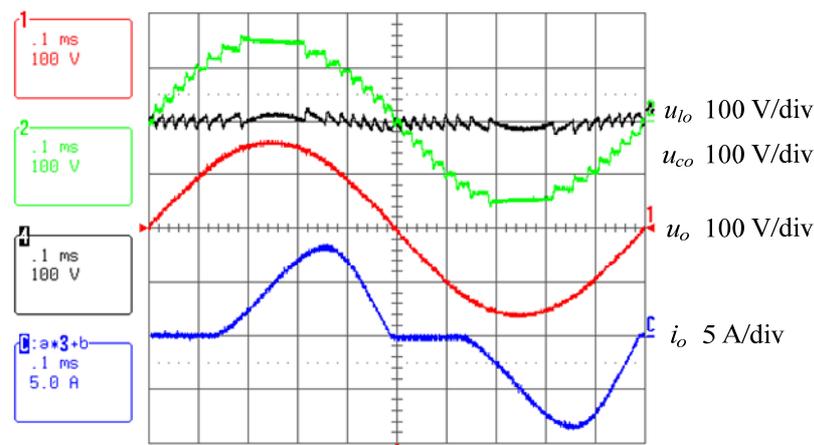


Figure 3.54: Experimental results for supplying a non-linear load. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_s = 140 \text{ kHz}$, $f_o = 1 \text{ kHz}$, $U_a = 30 \text{ V}$.

Figure 3.55 depicts the measured output voltage THD in dependency on the output frequency. The THD is about 0.3% up to 500 Hz and 3% at the worst frequency, i.e., at 10 kHz. In the THD calculation, harmonics up to 40 times the fundamental frequency are taken into consideration according to IEC 61000-3-2.

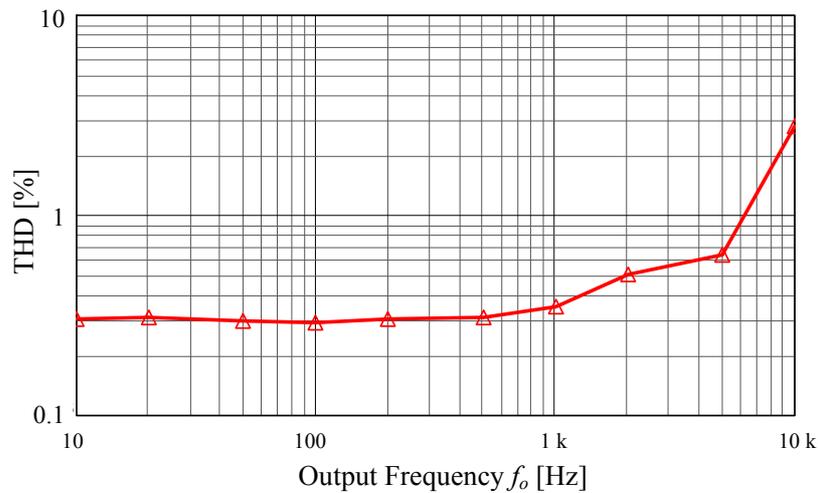


Figure 3.55: Measured output voltage THD in dependency on the output frequency f_o . Operation parameters: $U_{in} = 200$ V, $U_{o,rms} = 115$ V, $f_s = 140$ kHz, $R_L = 35$ Ω , $f_o = 1$ kHz, $U_a = 30$ V.

The prototype efficiency curves are shown in Figure 3.56, where the green curve marked with diamond points is measured from hardware for $U_a = 30$ V. The maximum efficiency at $U_{o,rms} = 130$ V is only 76%. The main losses originate from the LPA, 112 W, and the losses of the complete multi-cell inverter including the dv/dt filter are only 34 W. $U_a = 30$ V is selected for the 270 V output range where the dc link voltage of each cell is $U_z = 40$ V, but for the 135 V output voltage range the inverter cell dc voltage halved, $U_z = 20$ V, is used. Also as shown in Figure 3.49, the output voltage range u_{lo} is from -12 V to 12 V. Therefore, the LPA supply voltage could be reduced to, e.g., $U_a = 20$ V. This would significantly improve the system efficiency, by about 8%, as depicted in Figure 3.56. However reducing U_a would lower some of the system performances, e.g., overload current, non-linear load test, etc. There LPA needs a large output voltage range to compensate the cell dc link voltage drop due to the sudden surge current.

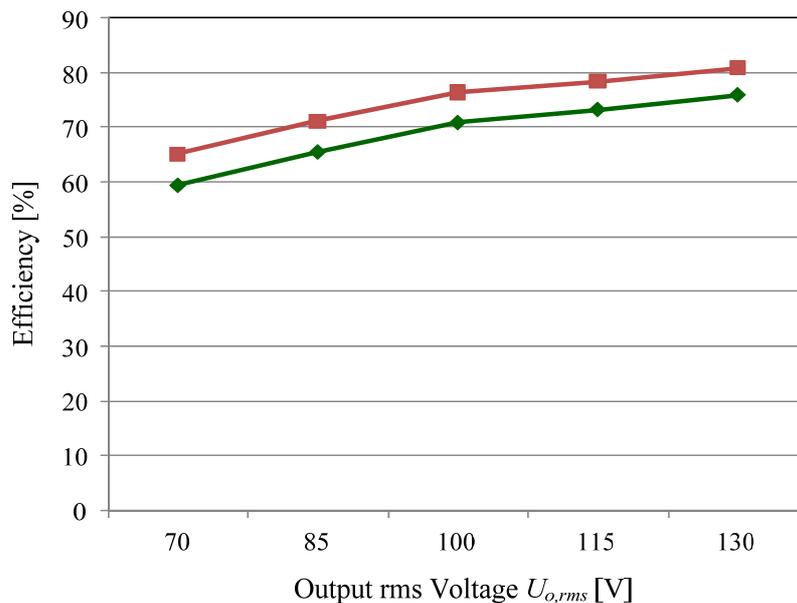


Figure 3.56: Measured system efficiency for $U_a = 30$ V, marked with diamond block and derived system efficiency for $U_a = 20$ V, marked with square block. Operation parameters: $U_{in} = 200$ V, $f_s = 140$ kHz, $R_L = 35$ Ω , $f_o = 1$ kHz, $U_a = 30$ V.

3.8 Conclusions

An isolated multi-cell cascaded power amplifier with high efficiency, high bandwidth, and wide load displacement range is presented. The cascaded power amplifier is realized by connecting a linear power amplifier and multi-cell inverter in series.

Different slew rate control schemes are compared, and finally a simple method to limit the slew rate of the inverter output voltage is developed, which utilizes a dv/dt filter composed of a LC filter with a LR damping network.

Loss calculations show a significant efficiency improvement compared to a conventional class-AB power amplifier. Furthermore, it is shown that the major system losses come from the LPA part and the power losses of the multi-cell inverter can be almost neglected because it operates at the output frequency.

An isolated, bidirectional dc-dc converter with open loop control and $\pm 5\%$ load regulation provides the power for the inverter cells and the linear power amplifier.

Based on the measured small signal model of the APEX MP 111 and the dv/dt filter, the feedback loop is designed. A system bandwidth of 570 kHz is achieved.

For the measured data from the laboratory prototype under the test condition of 135 V output voltage range specifications, H-MCA shows the performances of 570 kHz system bandwidth, 60 V/ μ s maximum slew rate, 0.6% THD up to 5 kHz and 76% system efficiency at $U_{o,rms} = 130$ V, $R_L = 35 \Omega$ which by the way can be further improved.

Chapter 4.

Multi-Cell Switch-Mode Power Amplifier

4.1 Introduction

In recent years, multi-level inverters have become increasingly popular in high-power applications. The main advantages of multi-level converters are voltage stress reduction of the power devices, low Electromagnetic Interference (EMI), low switching losses and high quality output waveform. These make multi-level inverters particularly welcome for such industrial applications as medium-voltage drivers, Static Var Compensator (SVC), STATCOMs, and grid interfaces for renewable energy like solar photovoltaic.

Mainly three types of topologies have been proposed for multi-level inverters: diode-clamped, flying-capacitor and cascaded multi-level inverters [69]-[70].

A diode-clamped three-level inverter is proposed in [71], and later this concept has been extended into a multi-level inverter [69]. This topology uses a single dc voltage that is subdivided into a number of small equal voltage levels by a series of capacitors. By appropriately arranging the power

switches and diodes, each leg can be connected to any of these dc levels. However the disadvantages of this topology are that a large number of clamping diodes are required and complex modulation has to be applied for balancing the dc-link capacitor voltages.

The flying-capacitor multi-level inverter is proposed in [72]. The main reason to develop this topology is to get rid of the large number of clamping diodes in the diode-clamped inverters. However this topology introduces many flying capacitors that are commonly regarded as less reliable components in industry. Furthermore, the voltages of the flying capacitors require a rather complicated modulation to balance.

The cascaded multi-level inverter, which is known as a multi-cell inverter in some other literature, is presented in [73]. This topology connects H-bridge inverters in series that are supplied by separated dc voltage sources to boost the output voltage range. Since each H-bridge inverter is supplied by separated dc voltage sources, there is no voltage balancing strategy needed for this topology. However the requirement for separated dc sources increases the complexity of the power circuit.

There are two different configurations for the multi-cell inverter: symmetric and asymmetric. The symmetric multi-cell inverter employs an equal dc voltage for each cell [74]-[75], while in the asymmetric multi-cell inverter the dc voltages for the cells are set to different levels [76]-[88]. In this way the multi-cell inverter can achieve a much higher number of levels by using the same number of cells as the symmetric multi-cell inverter.

In this chapter, the symmetric multi-cell inverter is selected for AP-MCA and P-MCA. The main reasons are:

- The isolation stages are anyway required for ac power source applications.
- The symmetric topology gives great freedom to increase or decrease the output voltage range with minimum effort.
- The component dimensioning is identical for each cell unit.

Many studies about the modulation of multi-level inverters have been carried out [89]-[93]. For the multi-cell inverters, phase-shifted carrier PWM is regarded as the most common PWM strategy [77]. This PWM strategy is also implemented for P-MCA in this chapter.

Two multi-cell switch-mode amplifiers, AP-MCA and P-MCA, are presented in this chapter. These two amplifiers have exactly the same power circuits but different modulation and control implementations. The operating principle, control design and experimental results are described for each system.

4.2 AM + PWM Multi-Cell Amplifier

In Chapter 3 H-MCA shows its performance of wide bandwidth, high output voltage quality and low output impedance; however, the system efficiency is impaired by the LPA that contributes around 60% of the total system losses. In order to achieve higher system efficiency, a PWM inverter cell with 500 kHz switching frequency is used to substitute the LPA unit in H-MCA. Consequently the dv/dt limit filter has to be replaced by another designed filter aiming for eliminating the switching ripple sufficiently. Afterwards, this system turns out to be a pure switch-mode amplifier with mixed AM and PWM control, hence the system is a so-called AM + PWM Multi-Cell Amplifier (AP-MCA).

4.2.1 Operation Principle

The circuit diagram of the AP-MCA is shown in Figure 4.1, where the AM inverter as well as the dc-link power supplies are the same as the H-MCA. However the LPA together with its isolation dc supply stage are replaced by a PWM inverter and its dc power supply. The AM inverter and PWM inverter are connected in series for generating the total inverter output voltage u_{mo} . As in any other switch-mode amplifier, an output filter has to be employed to eliminate the switching ripples.

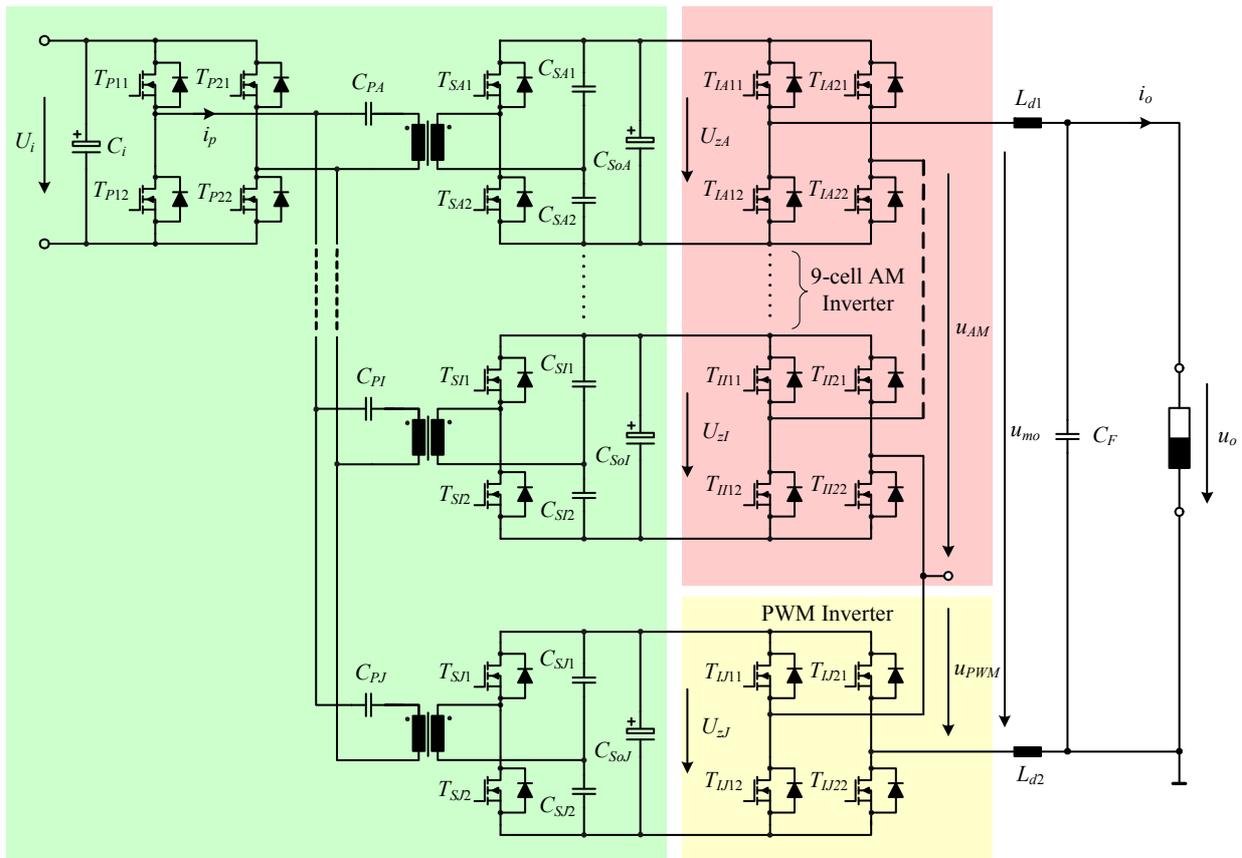


Figure 4.1: AP-MCA circuit diagram.

The modulation of the AM inverter is completely same as for H-MCA (see Figure 3.4). Also the principle of the system control is identical. Figure 4.2 demonstrates the key waveforms of AP-MCA, where the AM inverter produces the large scale voltage u_{AM} , and the PWM inverter is regulated to generate the small compensation signal. The total multi-cell inverter voltage u_{mo} is formed by the summation of u_{AM} and u_{PWM} . The sinusoidal output voltage u_o is achieved by low-pass filtering of u_{mo} .

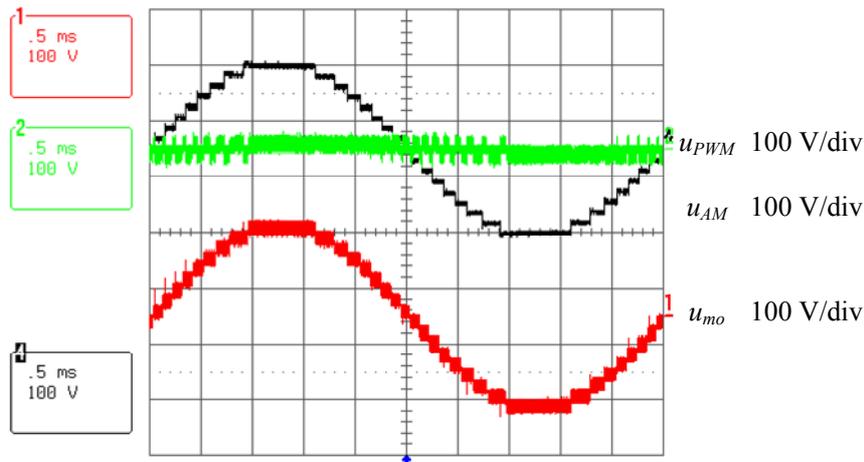


Figure 4.2: Measured key waveforms of AP-MCA.

4.2.2 Control Design

Overview of System Control

As described before, in contrast to H-MCA, the AP-MCA uses a high switching frequency class-D amplifier to replace the LPA of the H-MCA. Therefore the control system implementation for AP-MCA has to be modified. Figure 4.3 shows the system control scheme of the AP-MCA implemented in the prototype. The main difference in AP-MCA is that digital control is employed for the output voltage control that is realized by analog means in H-MCA. The output voltage u_o and its reference signal u_o^* are measured through the analog interface circuits and are converted to digital signals by the ADCs integrated in the DSP. Then the DSP calculates the output of the digital PI-controller and converts it to a count number which is to be sent to FPGA. The 500 kHz PWM signals are generated by FPGA by comparing the received count number to the digital internal 500 kHz triangular carrier.

The multi-cell inverter uses the same amplitude modulation as the H-MCA shown in Figure 3.4. And also the implementation in the hardware for determining the switching signals of the multi-cell inverter is the same as in H-MCA, where fast analog comparators are used to directly compare the reference signal with threshold voltage levels set by the TrimDAC.

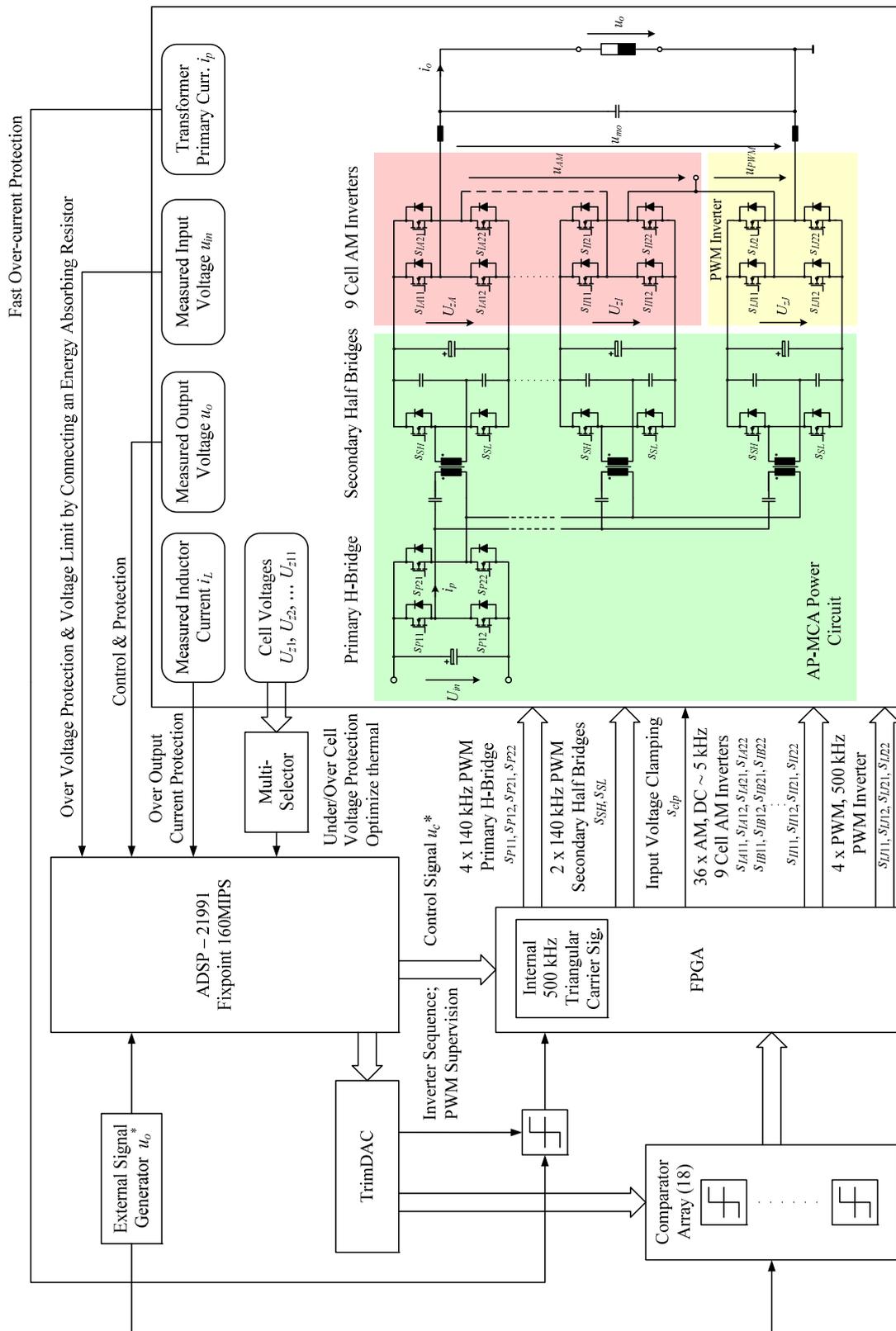


Figure 4.3: System control scheme of AP-MCA implemented in the prototype.

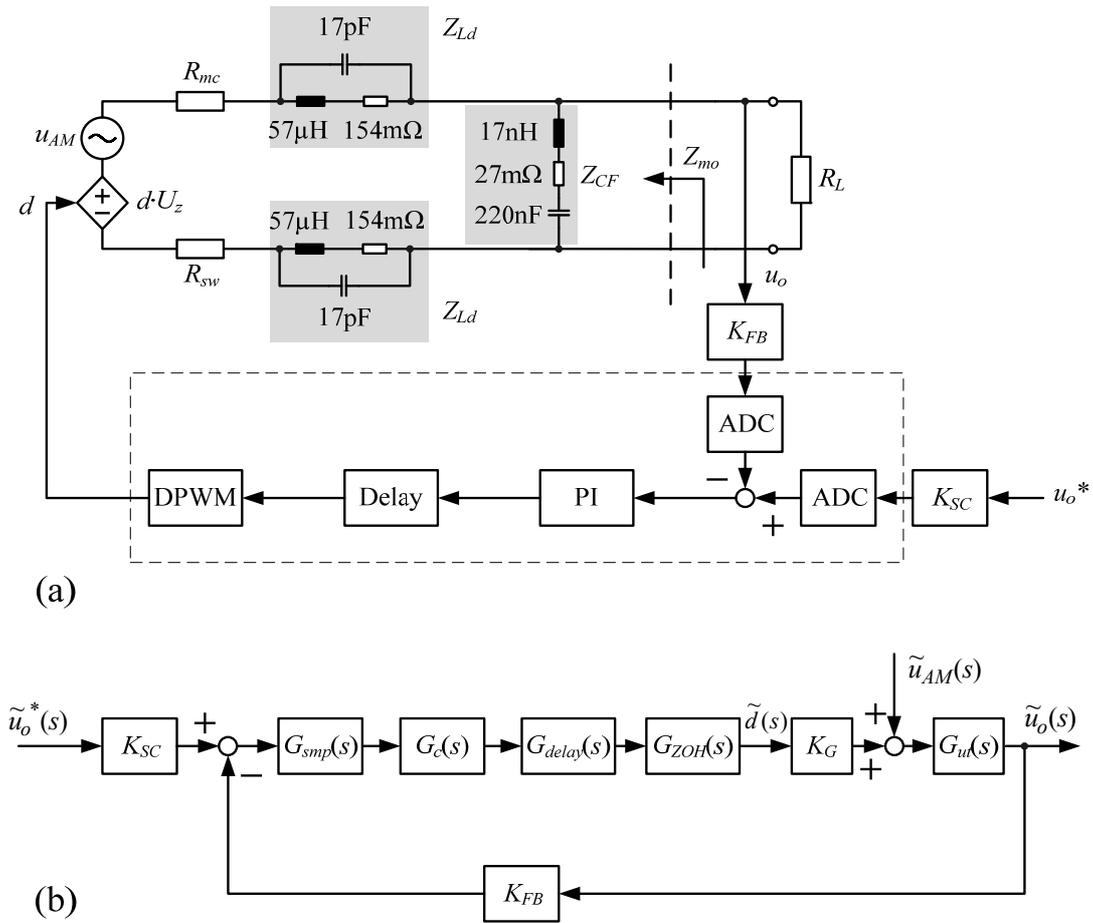


Figure 4.4: Simplified AP-MCA system control scheme (a) and the according control system block diagram (b).

System Modelling

The simplified AP-MCA control system scheme is shown in Figure 4.4(a), where the digital control part is inside the dashed frame, and outside the frame are the analog parts including the power circuit and measurement circuits. The PWM inverter is considered as a controlled voltage dU_z that is proportional to the duty cycle ratio d [94]. The AM multi-cell inverter is regarded as a disturbance voltage source u_{AM} that is connected in series with dU_z .

The output filter is calculated to ensure switching ripples of the output voltage smaller than 0.5%. Furthermore, the output inductor is split into two inductors. This provides the benefits of the same common mode impedance in both paths, and using the damping inductor of the dv/dt filter of the H-

MCA as one of the output inductors, therefore to save space in the hardware implementation.

Here R_{mc} is the total on-resistance of the inverter MOSFETs in the output conducting loop, and there are always twenty MOSFETs conducting at the same time. Therefore, this is calculated as

$$R_{mc} = 20 \times R_{on,irf} = 0.2 \Omega. \quad (4.1)$$

The switching losses of the PWM inverter can be derived as

$$P_{sw} = 2f_s E_{sloss}, \quad (4.2)$$

where the switching energy losses are from (3.42). Since the switching voltage is constant $U_{sw} = U_z$, the switching losses are approximated as

$$P_{sw} = k_{sw} I_{sw}. \quad (4.3)$$

On the other hand, the switching losses can be represented by inserting a virtual resistor R_{sw} in the circuit as shown in Figure 4.4(a). Consequently the switching losses can be also expressed as

$$P_{sw} = R_{sw} I_{sw}^2. \quad (4.4)$$

By differentiating (4.3) and (4.4) with I_{sw} , we have

$$\frac{dP_{sw}}{dI_{sw}} = k_{sw} = 2R_{sw} I_{sw}. \quad (4.5)$$

Therefore the virtual resistor R_{sw} is derived as

$$R_{sw} = \frac{k_{sw}}{2I_{sw}}. \quad (4.6)$$

Since digital control is employed for AP-MCA, we have to treat the system as a sampled-data control system. There are two approaches that may be used in analyzing a sampled-data control system: the direct (DIR) or the digitization (DIG) control design technique. The DIR design is based on z -domain

and its main advantage is that less constraints on the controller parameters are required to meet the system specifications. Furthermore, the switch-mode converter is inherently a sampled-data system. The disadvantage of this method is that there is a limited amount of experience in designing a suitable digital controller in z -domain. On the other hand, the DIG design is to use s domain transfer functions to express the digital units, hence we can utilize the well established s domain knowledge to design the appropriate controllers. Afterwards the s -domain controllers are transformed to z -domain by use of the Tustin algorithm for the digital implementation in DSP [95].

For designing the controller of AP-MCA, the DIG method is used. The functional block diagram of AP-MCA control system, which is a so-called pseudo-continuous-time (PCT) system, is demonstrated in Figure 4.4(b). In the following, each control block will be described.

Firstly the control block units in continuous-time domain are introduced. Based on Figure 4.4(a), the small-signal transfer function from $\tilde{u}_{PWM}(s)$ or $\tilde{u}_{AM}(s)$ to the output voltage $\tilde{u}_o(s)$ is

$$G_{ut}(s) = \frac{R_L \parallel Z_{CF}(s)}{R_{mc} + R_{sw} + 2Z_{Ld}(s) + R_L \parallel Z_{CF}(s)}. \quad (4.7)$$

The gain K_G is equal to the dc-link supply voltage of the PWM inverter, i.e.,

$$K_G = U_z. \quad (4.8)$$

The output voltage feedback factor $K_{FB} = 0.01$ and the scaling factor of the reference voltage $K_{SC} = 0.4$.

The following control block units to be introduced are in the discrete-time domain, i.e., implemented in DSP+FPGA. As described before, the measured signals of u_o and u_o^* are sampled by the ADC incorporated in the DSP. The PCT approximation of the sampler is given as [95]

$$G_{smp}(s) = \frac{1}{T_{smp}}, \quad (4.9)$$

where T_{smp} is the sampling time. Since FPGA receives the discrete PI-control value that is a normalized count number in the hardware implementation and updates the PWM signal at sampling frequency, this digital PWM (DPWM) effectively embeds a Zero Order Hold (ZOH) which converts the discrete signal to the analog signal. The s-domain transfer function of the ZOH is [95]

$$G_{ZOH}(s) = \frac{1 - e^{-T_{smp}s}}{s}. \quad (4.10)$$

$G_{smp}(s)$ and $G_{ZOH}(s)$ can be combined together to form the transfer function of the sample and hold element,

$$G_{SZOH}(s) = \frac{1 - e^{-T_{smp}s}}{T_{smp}s}. \quad (4.11)$$

The system delay time is defined as the time interval between the moment the data is sampled and the updating action of the duty cycle. During system operation, this interval is actually changing. Here the maximum delay time, T_{smp} , is assumed for this system,

$$G_{delay}(s) = e^{-T_{smp}s}. \quad (4.12)$$

If the root locus method is utilized for the compensation design, the Padé approximation has to be applied to $G_{SZOH}(s)$ and $G_{delay}(s)$. E.g., the second-order Padé approximation of $G_{SZOH}(s)$ is

$$G_{SZOH,PA}(s) = \frac{12}{12 + 6T_{smp}s - T_{smp}^2s^2}. \quad (4.13)$$

This approximation is good for the frequency range up to $T_{smp}/3$. However, the frequency-response compensation method based on Bode plots is employed for the controller design in this system. In this case, the Padé approximations for $G_{SZOH}(s)$ and $G_{delay}(s)$ are not necessary.

PI-controller Design

Based on the aforementioned modelling analysis, the open-loop plant transfer function is

$$G_{plant}(s) = K_G G_{ut}(s) G_{SZOH}(s) G_{delay}(s). \quad (4.14)$$

Figure 4.5 compares the Bode plots of $G_{ut}(s)$, $G_{SZOH}(s)$, and $G_{delay}(s)$, where $G_{delay}(s)$ shows the largest impact on the system phase angle. For PCT system control design, the bandwidth is typically limited to one-twentieth of the sampling frequency [96]. Therefore, a simple PI-controller is designed to compensate $K_{FB} G_{plant}(s)$ shown in Figure 4.6. The transfer function of the

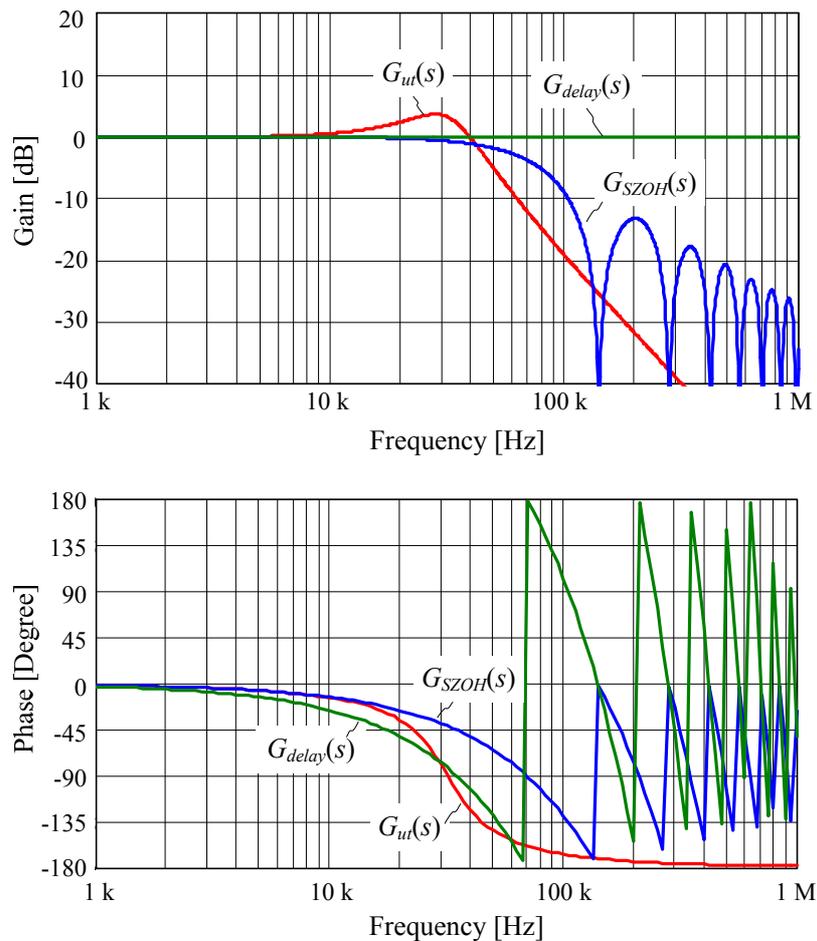


Figure 4.5: Bode plots comparison of the three transfer functions in the control plant. Operation parameters: $R_L = 35 \Omega$, $T_{smp} = 7 \mu s$.

PI-controller is given as

$$G_c(s) = K_{PI} \left(1 + \frac{1}{T_{PI}s} \right). \quad (4.15)$$

where the calculated PI parameters are: $K_{PI} = 0.45$ and $T_{PI} = 3.2 \times 10^{-6}s$. The open-loop transfer function of the compensated system is written as

$$G_{open}(s) = K_{FB}G_{plant}(s)G_c(s). \quad (4.16)$$

Figure 4.6 shows that the compensated system achieves a bandwidth of 4.5 kHz and a phase margin of 70° for the nominal load.

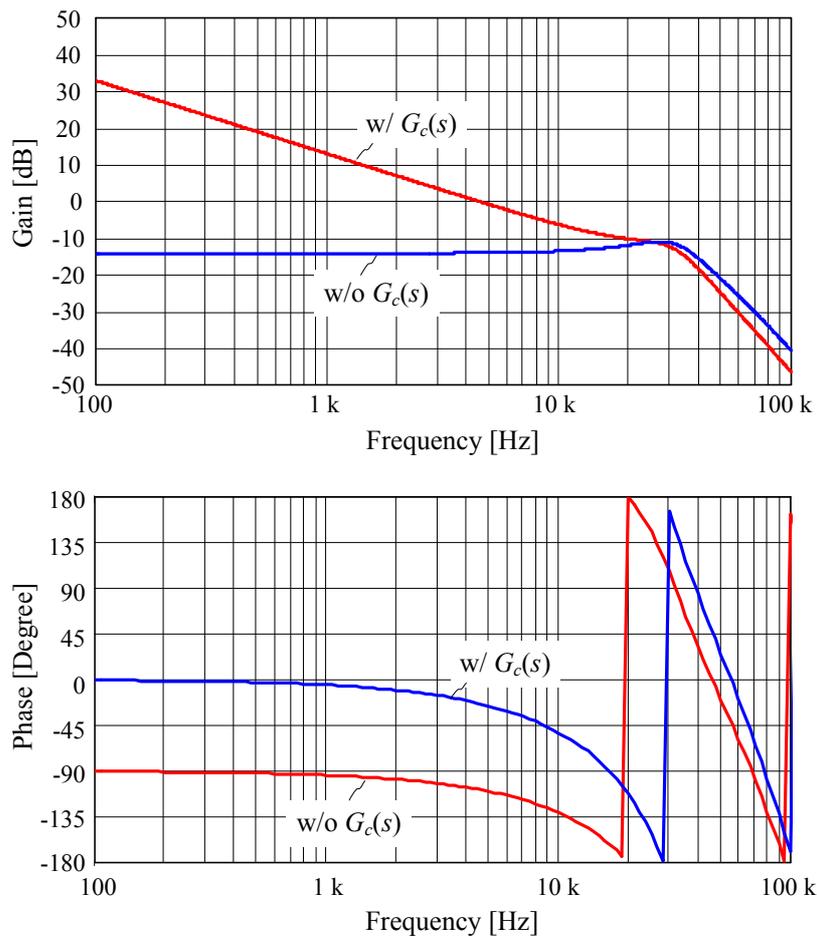


Figure 4.6: System open-loop Bode plots with and without the controller $G_c(s)$.

System Transfer Functions

Obviously the closed-loop input-to-output transfer function can be derived as

$$G_{io,cls}(s) = K_{SC} \frac{G_{plant}(s)G_c(s)}{1 + G_{open}(s)}. \quad (4.17)$$

The closed-loop transfer function from the disturbance voltage $\tilde{u}_{AM}(s)$ to $\tilde{u}_o(s)$ is

$$G_{do,cls}(s) = \frac{u_{ut}(s)}{1 + G_{open}(s)}. \quad (4.18)$$

According to Figure 4.4, the output impedance without closed-loop control is

$$Z_{mo}(s) = (R_{mc} + R_{sw} + 2Z_{Ld}(s)) \parallel Z_{CF}(s). \quad (4.19)$$

Therefore the closed-loop system output impedance can be derived as

$$Z_o(s) = \frac{Z_{mo}(s)}{1 + G_{open}(s)}. \quad (4.20)$$

Verifications

The small-signal frequency response of AP-MCA is measured from the laboratory prototype to verify the theoretical analysis. The calculated small signal parameters and system operating parameters are listed in Table 4.1.

Table 4.1: System Parameters for Small-signal Model Verification

Name	Denotation	Value
Total on-resistance	R_{mc}	0.2 Ω
Switching energy losses	E_{sloss}	2.4 μJ
Switching frequency of PWM inverter	f_s	500 kHz
Virtual resistor representing switching losses	R_{sw}	0.1 Ω
Output voltage feedback factor	K_{FB}	0.01
Reference signal scaling factor	K_{SC}	0.4
Sampling time	T_{smp}	7 μs
DC-link voltage of PWM inverter	U_z	20 V
Output voltage	U_o	120 V
Nominal load resistor	R_L	35 Ω

Figure 4.7 shows the calculated and measured Bode plots of the open-loop transfer function of AP-MCA, where these two plots match very well until 20 kHz and the measured crossover frequency and phase margin are close to the calculated values. However the measurement result shows higher damping factor in the system. This is mainly because the resistances of many contactors and PCB track impedances in the large output power loop are not considered in the small signal modelling for the sake of simplify.

The PI-controller is designed for the nominal load condition. The worst operating point concerning the system stability for the buck-type derived converters is when no-load is connected to the output. Therefore one has to check the system stability for the no-load condition. The measured Bode plots of $G_{open}(s)$ for nominal load and no-load conditions are compared in Figure 4.8, where the system still fulfils the stability criteria for the no-load condition because of the sufficient damping in the hardware.

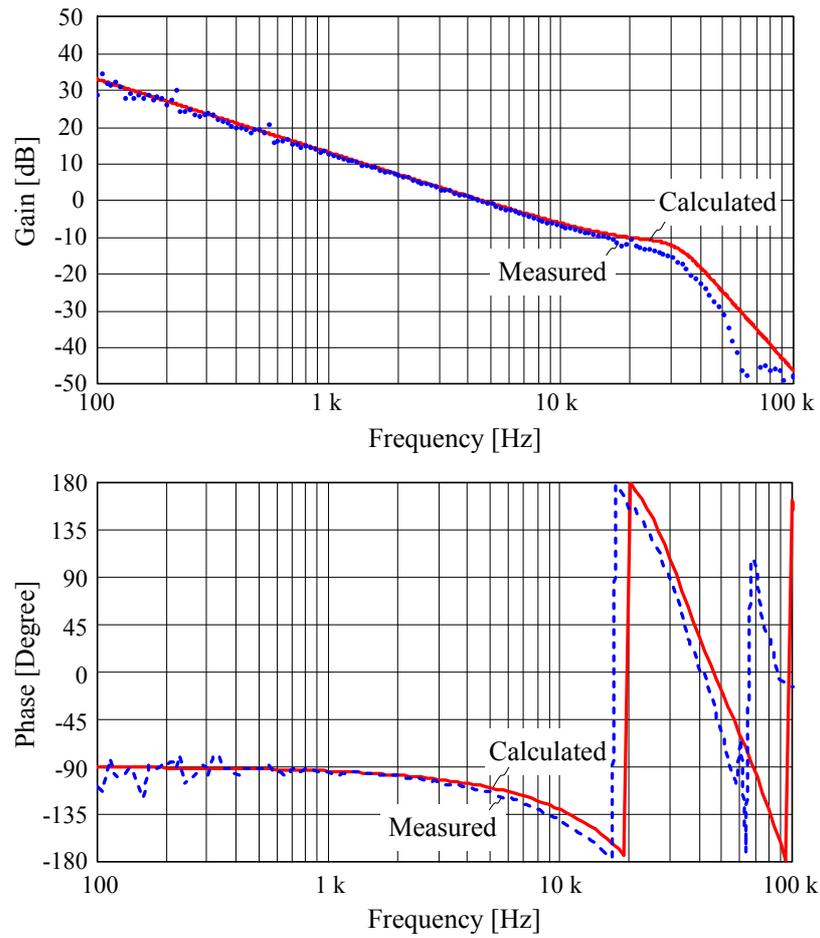


Figure 4.7: Comparison of the calculated and measured Bode plots of the open-loop transfer function of AP-MCA. The controlled system has a crossover frequency of 4.5kHz and a phase margin of 70°.

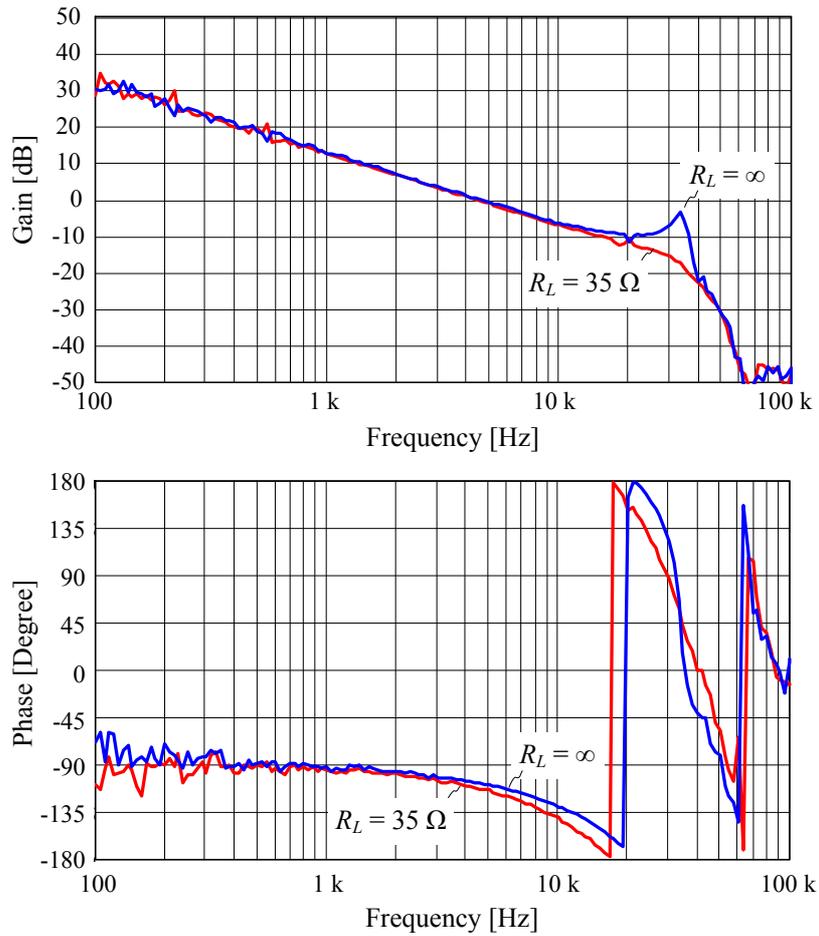


Figure 4.8: Comparison of the measured Bode plots of the open-loop transfer function of AP-MCA for nominal load and no-load conditions.

The calculated and measured Bode plots of the closed-loop transfer function, as shown in Figure 4.9, match well up to 10 kHz. The comparison of the calculated and measured Bode plots of the system output impedance are depicted in Figure 4.10, where the curves coincide except that the calculated curve shows less damping.

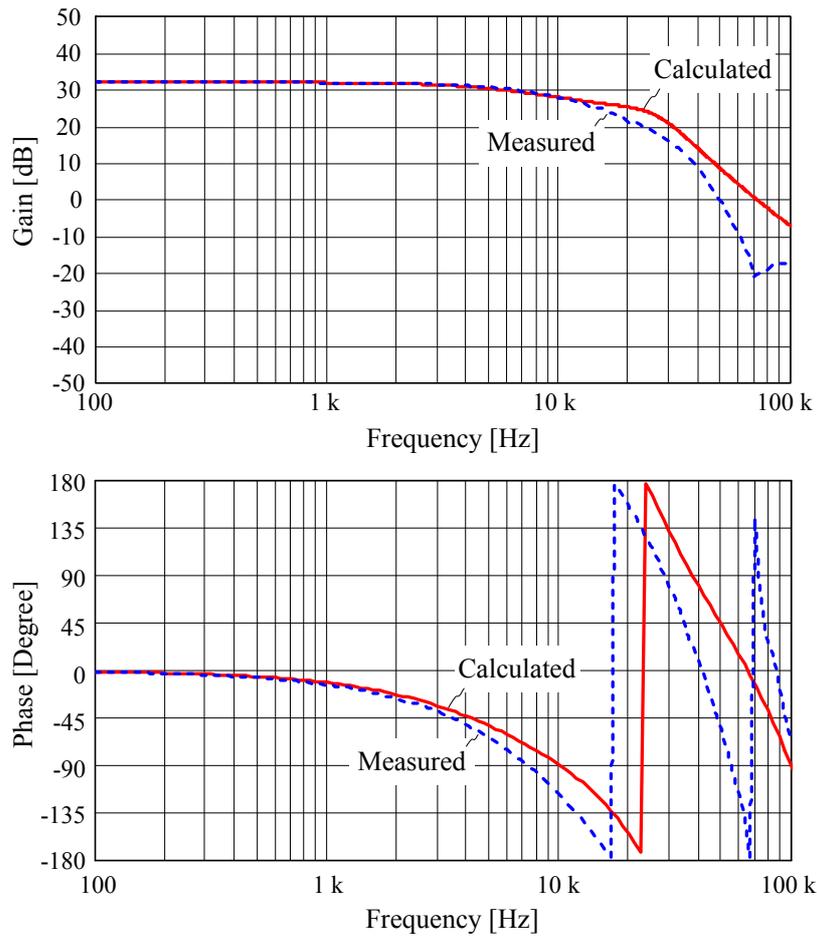


Figure 4.9: Bode plots of AP-MCA closed-loop transfer function.

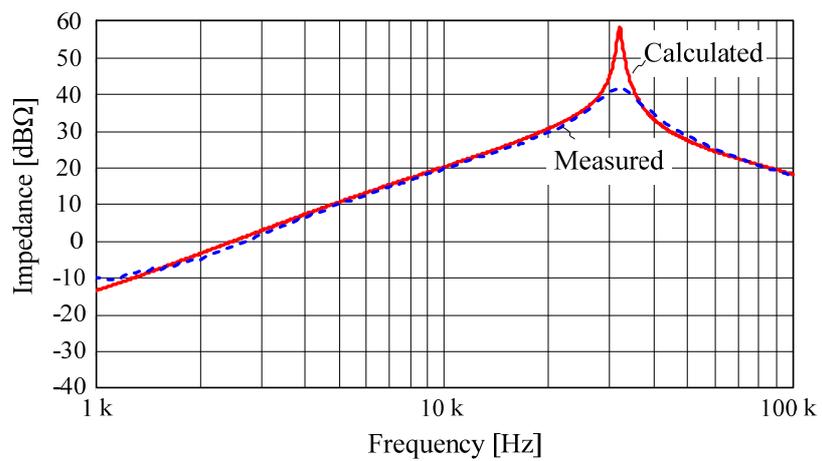


Figure 4.10: Comparison of the calculated and measured Bode plots of AP-MCA output impedance $Z_o(s)$.

4.2.3 System Performance Improvement

PWM Inverter Rotating Operation

In the hardware realization (see Chapter 5), a AP-MCA comprised of a nine-cell AM inverter and a single-cell PWM inverter is employed, where all the inverter cell circuits are identical. However, only the MOSFETs in the PWM inverter cell are switching at 500 kHz while the MOSFETs in the other nine inverter cells are switching at output frequency f_o , maximum at 5 kHz. Therefore a rotating operating scheme for the PWM inverter is developed to balance the thermal stress on the MOSFETs in the inverter cells. The idea is not to fix one inverter cell to the dedicated PWM operation. Instead, we program such that the PWM operating is rotating through all the inverter cells and each inverter cell is operating as a PWM inverter for one second after the next inverter is turned to PWM operation, and the previous inverter cell is switched to AM operation. E.g., Figure 4.11 shows the switching of the PWM operation between two inverter cells, where channel 1 and channel 2 illustrate the output voltages of inverter cell 1 and inverter cell 2. Before t_0 both cells are operating in AM mode. Cell 1 is switched to PWM operation at t_1 . Afterwards a second cell 2 is switched to PWM operation and cell 1 is turned back to AM operation.

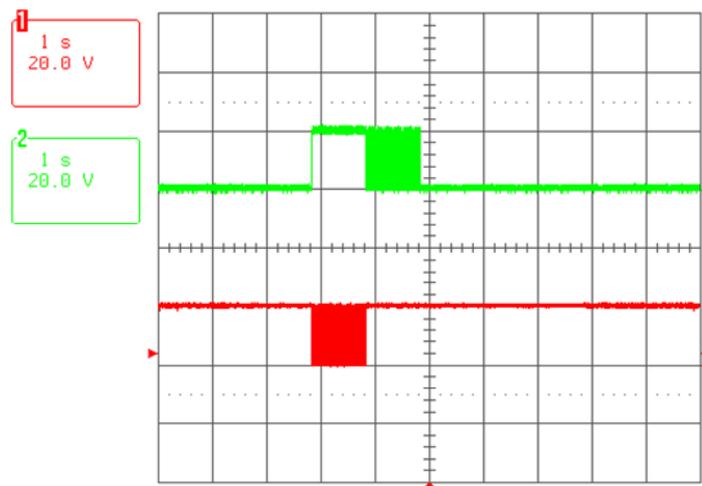


Figure 4.11: Rotating operation of PWM cells.

Feed-forward Control

As described in section 4.2.2, the nine-cell AM inverter acts as a disturbance voltage source in AP-MCA. The Bode plot of the calculated transfer function from $\tilde{u}_{AM}(s)$ to $\tilde{u}_o(s)$ is depicted in Figure 4.12, and shows that the system has no more amplitude attenuation for $\tilde{u}_{AM}(s)$ when the disturbance frequency is larger than 4.5 kHz, and even worse the amplitude of $\tilde{u}_{AM}(s)$ is excited by the output filter. Since the disturbance frequency is $18f_o$ for the maximum output voltage, this means the system has no attenuation for $\tilde{u}_{AM}(s)$ when the output frequency is larger than 250 Hz.

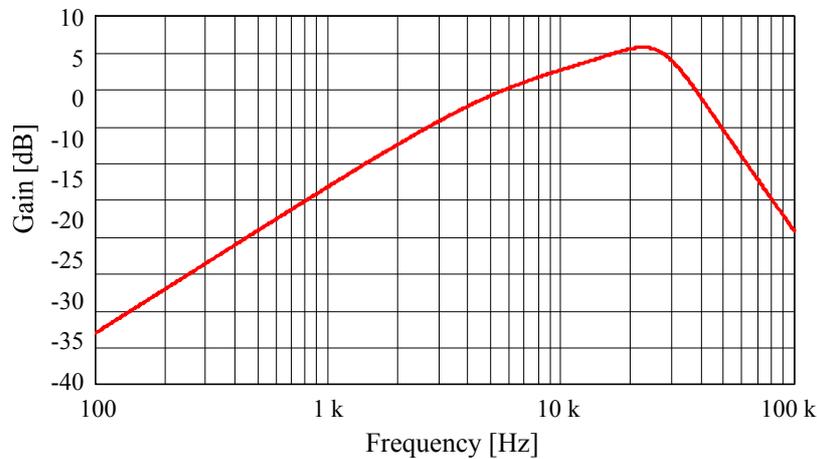


Figure 4.12: Calculated Bode plots of the transfer function from $\tilde{u}_{AM}(s)$ to $\tilde{u}_o(s)$.

In the following this disturbance behaviour is briefly analysed in the time domain. When any of the AM inverter cells changes its output voltage level, this effectively disturbs the control system with a stepped voltage. Of course the PWM inverter with only 4.5 kHz bandwidth is not able to compensate the disturbance immediately. Therefore this results in a significant distortion in the output voltage as shown in Figure 4.13(a) due to the limited control system dynamics.

There is a very simple way to eliminate the output voltage distortion by feed-forward control. I.e., every time when any inverter cell changes its output voltage, e.g., from 0 V to U_z , the duty cycle is reduced by 0.5 and thereby compensates the voltage difference. The measured waveforms with feed-forward control are shown in Figure 4.13(b), where the voltage distortion is

significantly reduced. However the disturbance is not completely eliminated since the duty cycle adjustment only changes the average voltage during one switching period.

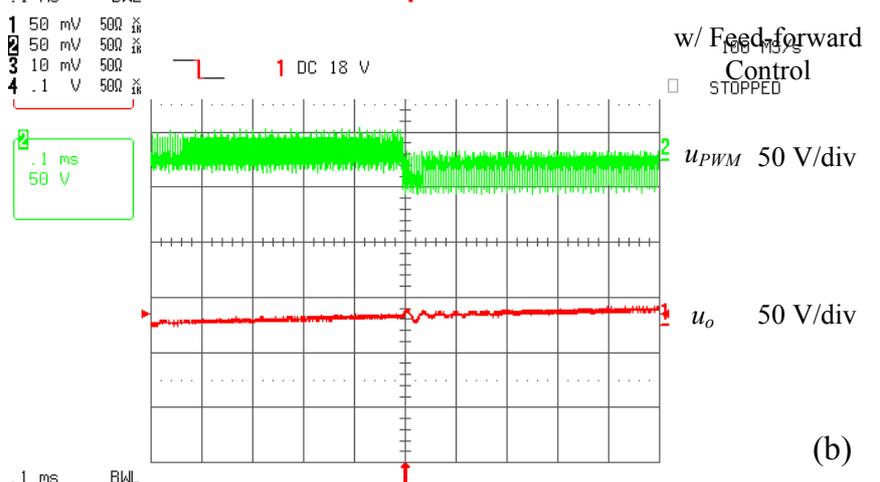
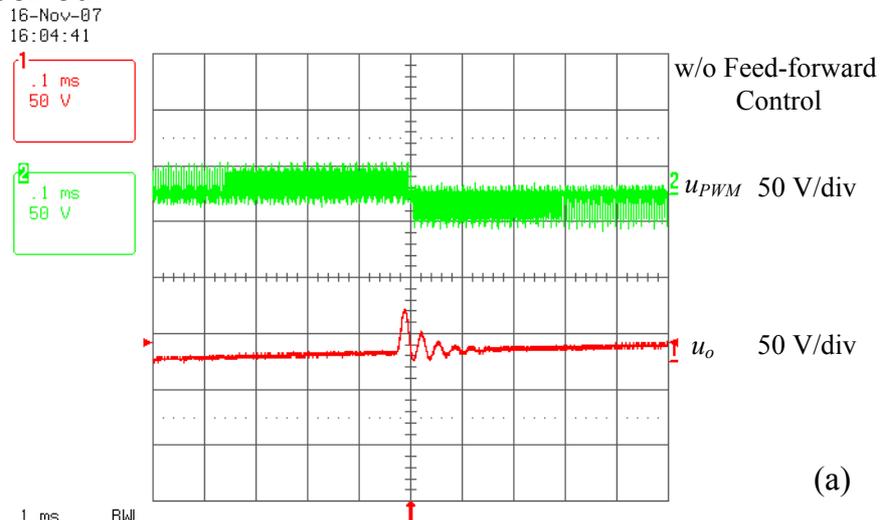


Figure 4.13: (a) without feed-forward control and (b) with feed-forward control and

4.2.4 Experimental Results

For testing the system performance, a series of measurements is carried out on the same laboratory prototype as for H-MCA. The descriptions of the prototype and components list are given in Chapter 5. The test conditions are according to the 135 V output voltage range as specified in Table 5.1.

The output voltage of AP-MCA shows a visible distortion at 1 kHz, and therefore the default test frequency for the following measurements is set to 200

Hz. The measured time behaviours of the multi-cell inverter output voltage u_{mo} , output voltage u_o , and output current i_o for three different rms output voltages $U_{o,rms}$, 70 V, 100 V and 130 V, are shown in Figure 4.14. The output voltage shows a clean sinusoidal shape for the full output voltage range. Furthermore, the measurements show the same relationship of the number of the switch-on AM inverter cells in dependence on the amplitude of the output voltage as for AP-MCA.

Experimental results of AP-MCA generating nominal output voltage 115 V for different load condition are depicted in Figure 4.15, where it is shown that AP-MCA can supply non-ohmic loads without any system stability problem.

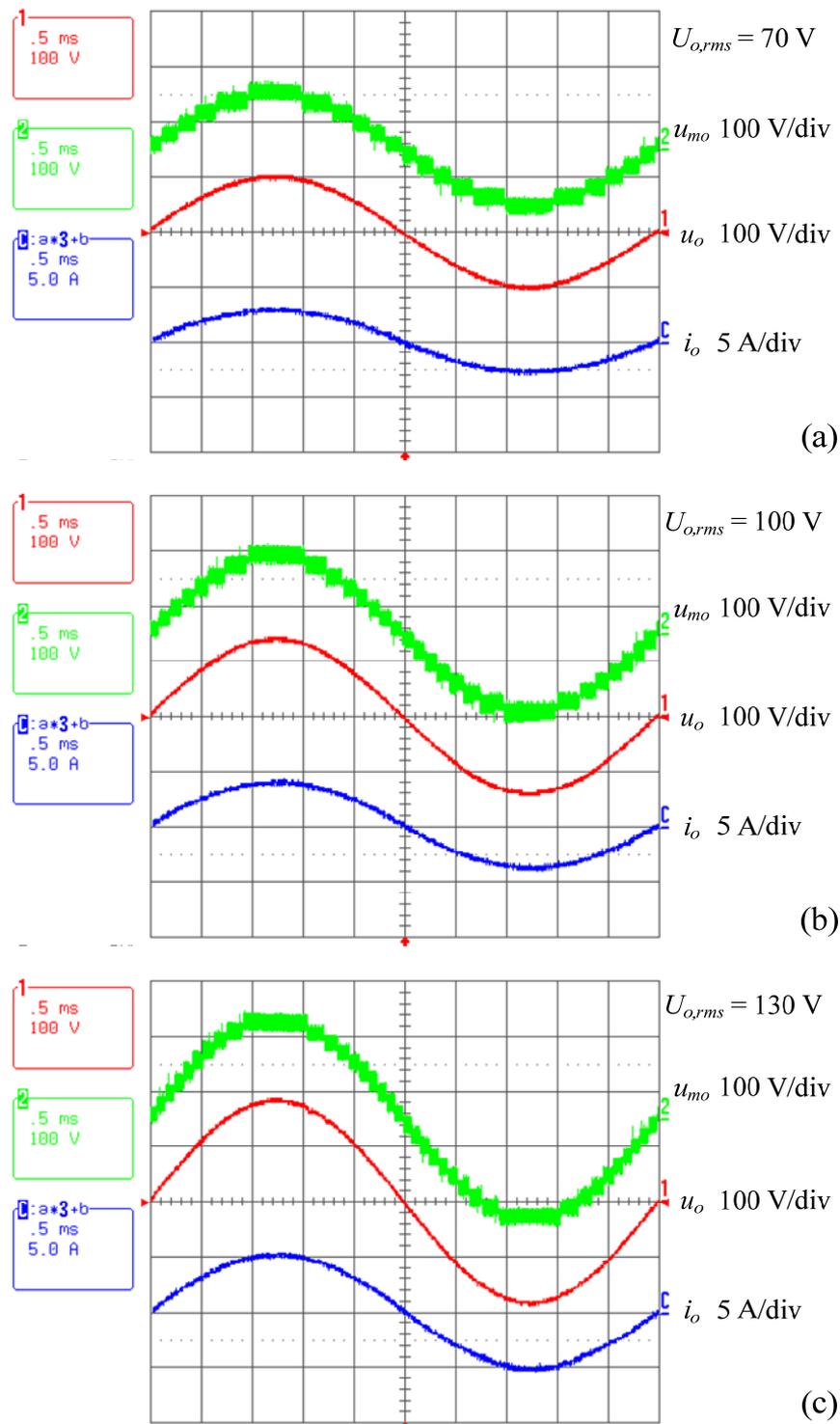


Figure 4.14: Measured time behaviours of the multi-cell inverter output voltage u_{mo} , output voltage u_o , and output current i_o for three different rms output voltages $U_{o,rms}$: 70 V (a), 100 V (b) and 130 V (c). Operation parameters: $U_{in} = 200$ V, $f_{spwm} = 500$ kHz, $U_{o,rms} = 115$ V, $R_L = 35$ Ω , $f_o = 200$ Hz.

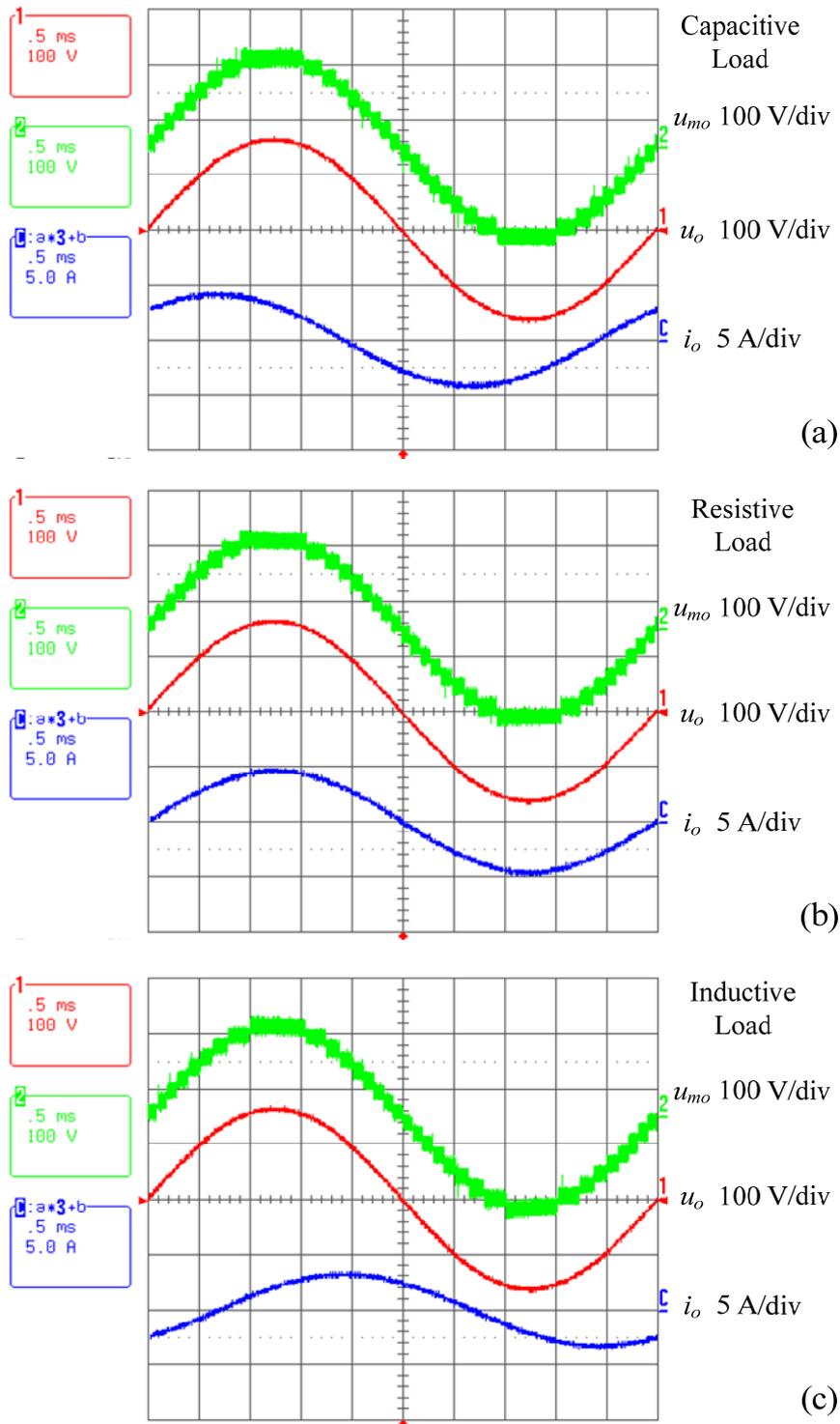


Figure 4.15: Measured time behaviours of the multi-cell inverter output voltage u_{mo} , output voltage u_o , and output current i_o for three different load conditions: capacitive load, $6.6 \mu\text{F}$ and 35Ω in series (a), ohmic load, $R_L = 35 \Omega$ (b) and inductive load 2.5 mH and 35Ω in series (c). Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_{spwm} = 500 \text{ kHz}$, $f_o = 200 \text{ Hz}$.

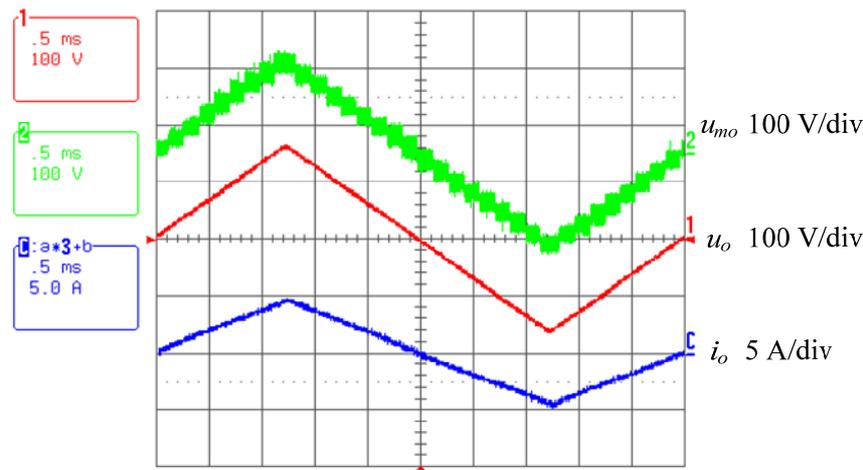


Figure 4.16: Experimental results for generating a triangular output waveform. Operation parameters: $U_{in} = 200$ V, $U_{op} = 162$ V, $f_{spwm} = 500$ kHz, $R_L = 35$ Ω , $f_o = 200$ Hz.

Figure 4.16 demonstrates the experimental results for generating a 200 Hz triangular output waveform, where the system outputs an excellent triangular waveform.

The measured rectangular output waveforms are shown in Figure 4.17. There the voltage overshoot for nominal load, $R_L = 35$ Ω , is quite large, i.e. 80 V. For the no-load condition, the overshoot is about 160 V from the simulation. This is because there is no damping in the output filter and the PWM

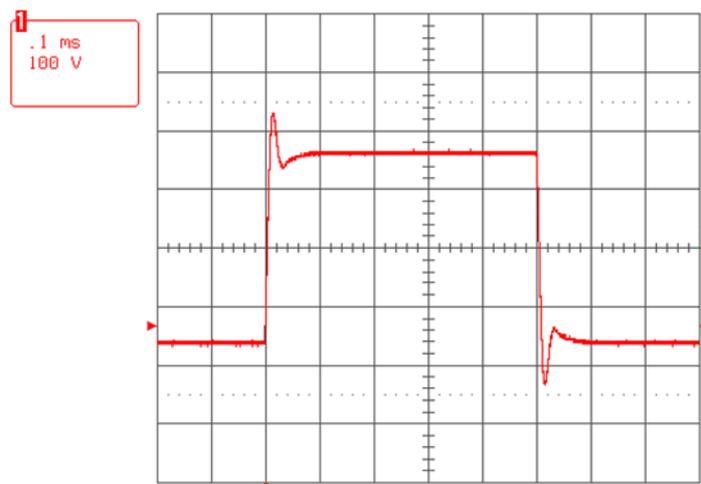


Figure 4.17: Experimental results for generating a rectangular output waveform connected with nominal load, $R_L = 35$ Ω . Operation parameters: $U_{in} = 200$ V, $U_{op} = 162$ V, $f_{spwm} = 500$ kHz, $f_o = 200$ Hz.

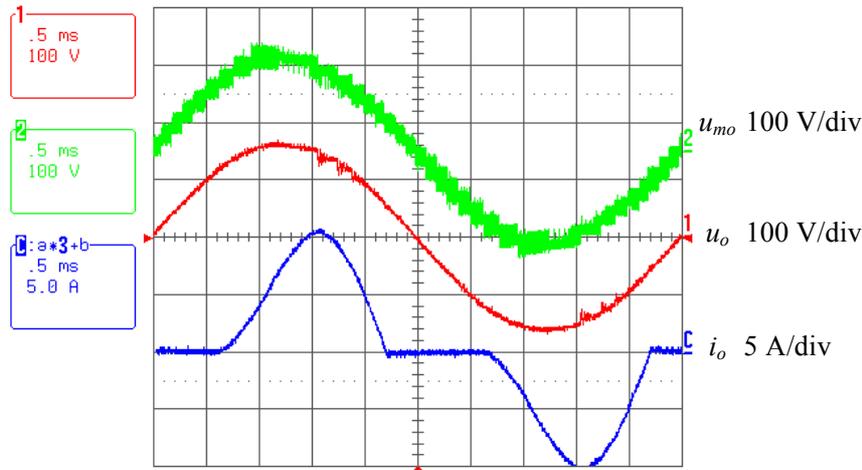


Figure 4.19: Experimental results for supplying a non-linear load. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_{spwm} = 500 \text{ kHz}$, $f_o = 200 \text{ Hz}$.

inverter is only able to compensate the voltage range from $-U_z$ to $+U_z$, which is from -20 V to $+20 \text{ V}$ in this test.

The experimental results for supplying non-linear load are shown in Figure 4.19, where the output current surges to 11 A but the output voltage is slightly distorted when the output current reaches its highest value. For this test, the load is a circuit of a full bridge rectifier followed by a 2.5 mH inductor in series with the parallel-connected $100 \mu\text{F}$ capacitor and 35Ω resistor.

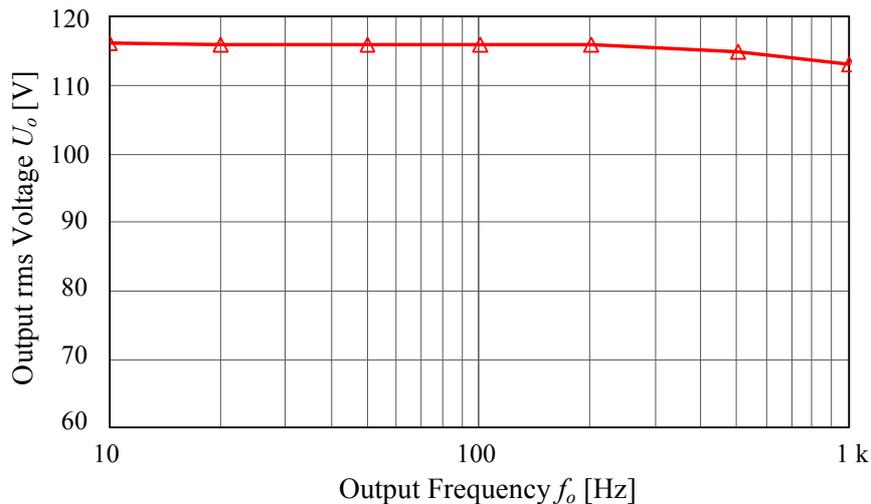


Figure 4.18: Measured large-signal output voltage in dependency on the output frequency f_o . Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms,ref} = 115 \text{ V}$, $f_{spwm} = 500 \text{ kHz}$, $R_L = 35 \Omega$.

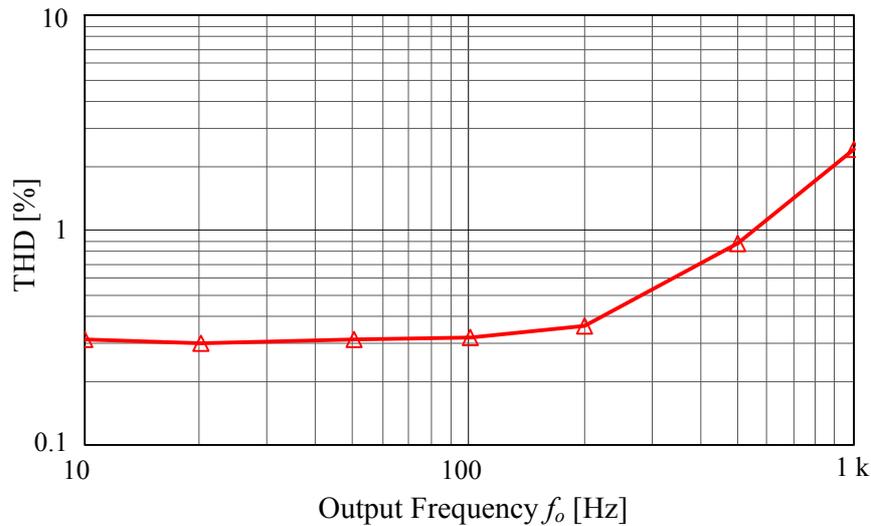


Figure 4.20: Measured output voltage THD in dependency on the output frequency f_o . Operation parameters: $U_{in} = 200$ V, $U_{o,rms,ref} = 115$ V, $f_{spwm} = 500$ kHz, $R_L = 35$ Ω .

The measured large-signal output voltage in dependency on the output frequency is depicted in Figure 4.18, where the input voltage $U_{in} = 200$ V and the output voltage reference is fixed to $U_{o,rms,ref} = 115$ V. Based on these measurements, the output voltage THD in dependency on the output frequency is demonstrated in Figure 4.20. The THD is about 0.3% up to 100 Hz and 2.4% at the measured highest frequency, i.e., at 1 kHz. In the THD calculation, harmonics up to 40 times the fundamental frequency are taken into consideration according to IEC 61000-3-2.

The prototype efficiency curves are shown in Figure 4.21, where the efficiency at $U_{o,rms} = 130$ V is 89%; that is significantly higher than that of H-MCA (76%) at the same operating point.

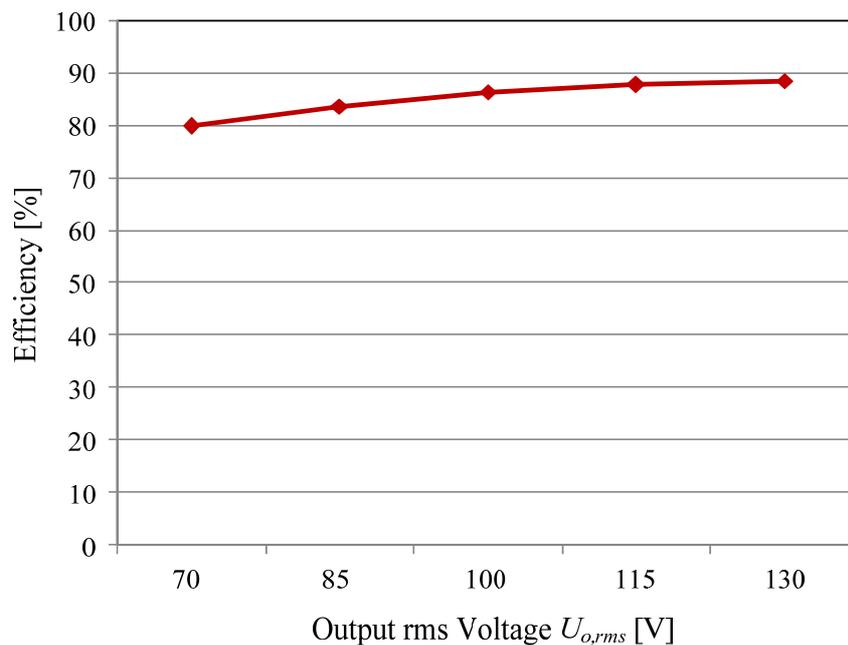


Figure 4.21: Measured system efficiency. Operation parameters: $U_{in} = 200$ V , $f_{spwm} = 500$ kHz, $R_L = 35$ Ω , $f_o = 200$ Hz.

4.3 PWM Multi-Cell Amplifier

4.3.1 Operation Principle

The circuit diagram of P-MCA is shown in Figure 4.22 which has exactly the same power circuit as AP-MCA. In the P-MCA all the inverters are operating in PWM mode, but in AP-MCA only one inverter cell is running in PWM mode and other cells are in AM operation. The switching frequency of each cell is set to 50 kHz, hence the effective switching frequency of the ten-cell system is 500 kHz, that is the same as the switching frequency of a PWM inverter cell in the AP-MCA system. This provides fair conditions for system efficiency comparison later.

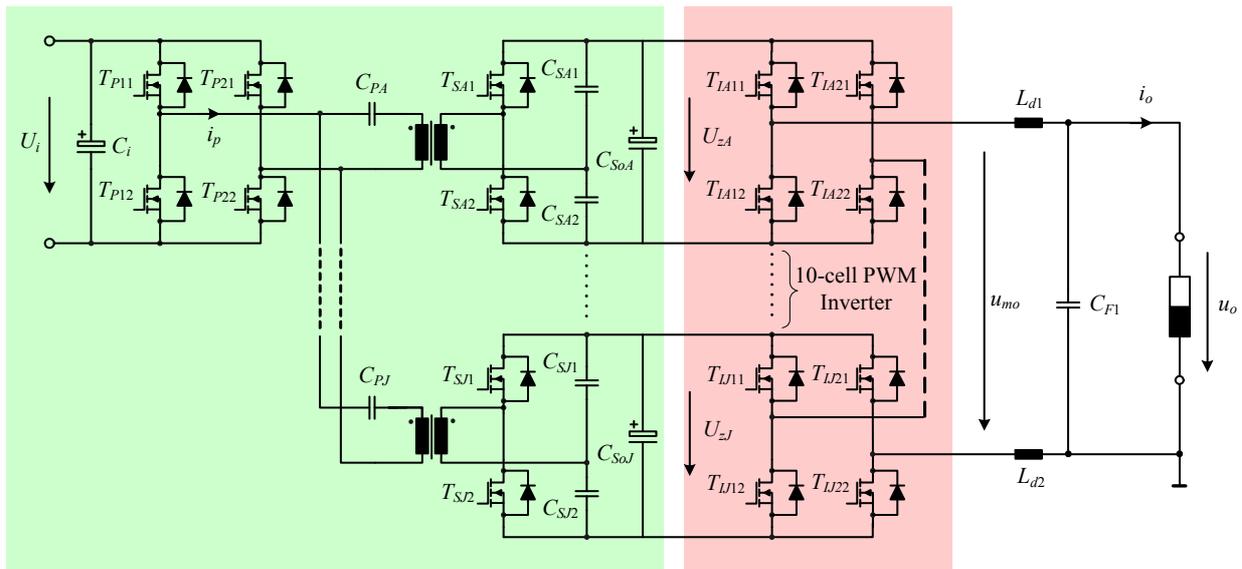


Figure 4.22: P-MCA circuit diagram.

Figure 4.2 demonstrates the key waveforms of P-MCA. There the 10-cell series-connected inverter using SPWM control produces the total output voltage u_{mo} , and the sinusoidal output voltage u_o is achieved after low-pass filtering of u_{mo} .

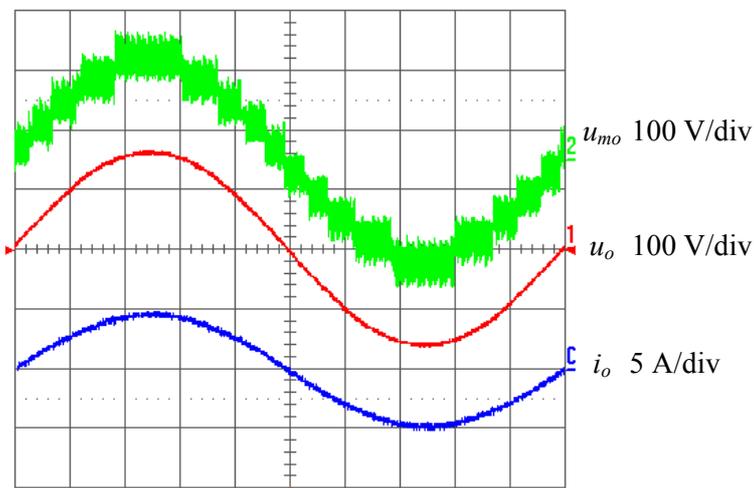


Figure 4.23: Measured key waveforms of P-MCA.

The phase shift between the output voltages of two adjacent inverter cells is demonstrated in Figure 4.24. Since a 10-cell inverter is employed in hardware and each inverter is switching at 50 kHz, the phase shift should be $2 \mu\text{s}$ and/or 36° .

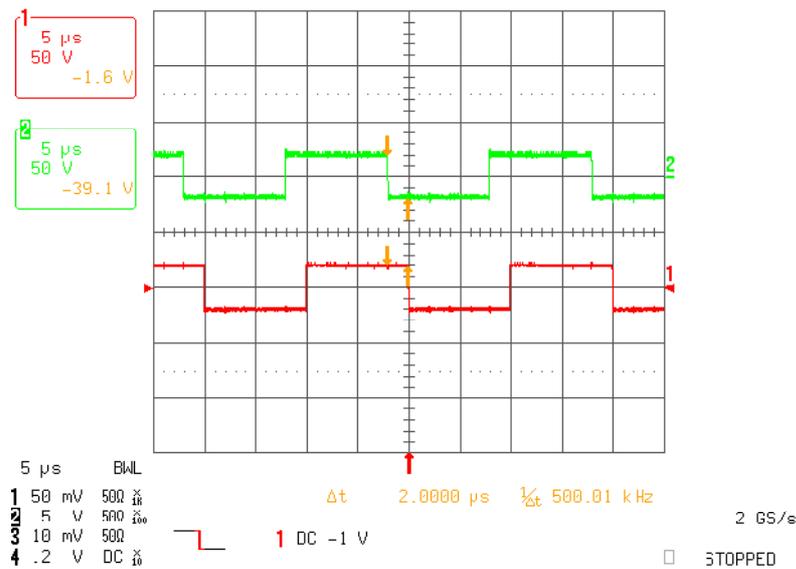


Figure 4.24: Phase shift between the output voltages of two adjacent inverter cells, 36° (2μ s). Operation parameters: $U_{in} = 200$ V, $f_{sm} = 50$ kHz, $U_{o,rms} = 115$ V, $R_L = 35 \Omega$, $f_o = 1$ kHz.

4.3.2 Control Design

The only difference between AP-MCA and P-MCA is the modulation method. AP-MCA utilizes a hybrid modulation that combines AM and PWM, while P-MCA only employs PWM modulation. The fast analog comparator arrays designed for AM modulation are not needed for P-MCA, and this makes P-MCA the only system which is fully digitally controlled among H-MCA, AP-MCA and P-MCA. A well-known phase-shifted scheme for generating the carrier signals is implemented, which increases the system switching frequency by a factor of 10 for P-MCA.

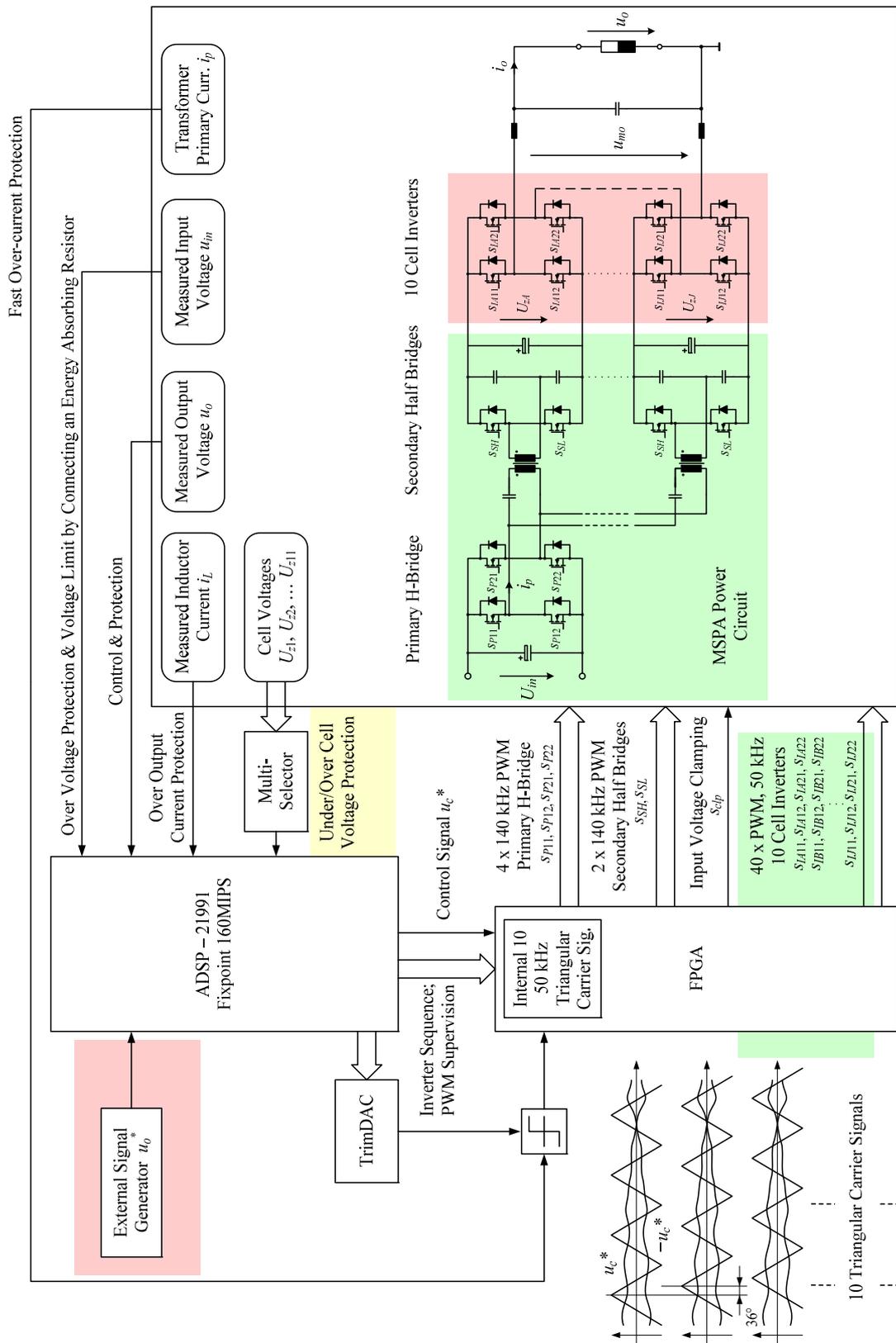


Figure 4.25: System control scheme of P-MCA implemented in the prototype.

The system small-signal modelling and control design are very similar to AP-MCA. Therefore the control design for P-MCA will be not treated in detail. When designing the compensator for P-MCA, the functional block diagram of AP-MCA shown in Figure 4.4(b) can be still used with few parameter modifications. These changes are:

- The disturbance voltage $\tilde{u}_{AM}(s)$ is no longer present;
- Gain K_G is changed from U_z to $10U_z$ because all ten cells inverter are operating in PWM mode and this effectively increases the inverter dc-link voltage by a factor of 10;
- The parameter K_{PI} of the controller is reduced to $0.1K_{PI}$, hence the designed system crossover frequency can remain at 4.5 kHz.

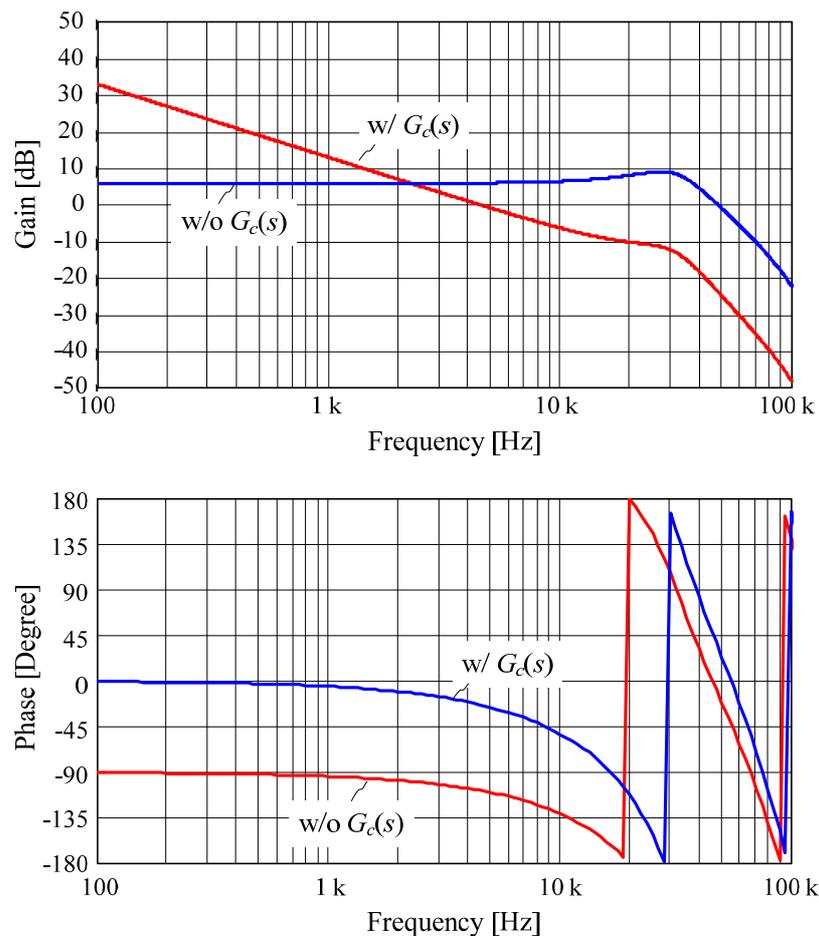


Figure 4.26: P-MCA open-loop Bode plots with and without the controller $G_c(s)$.

Figure 4.26 depicts the P-MCA system open-loop Bode plots with and without the PI-controller. It shows the gain of the system open-loop transfer function before compensation is 20 dB higher than that of AP-MCA. After the compensation, the controlled P-MCA system has a crossover frequency of 4.5kHz and phase margin of 70° , which are exactly same as in AP-MCA.

A series of measurements for the system small-signal frequency response has been made and compared to the calculated models. The calculated and measured Bode plots of the open-loop transfer function of P-MCA are compared in Figure 4.27, where both curves match quite well up to 20 kHz. Similarly to AP-MCA, the measurements show that the implemented P-MCA has a higher damping factor than that of the calculated model.

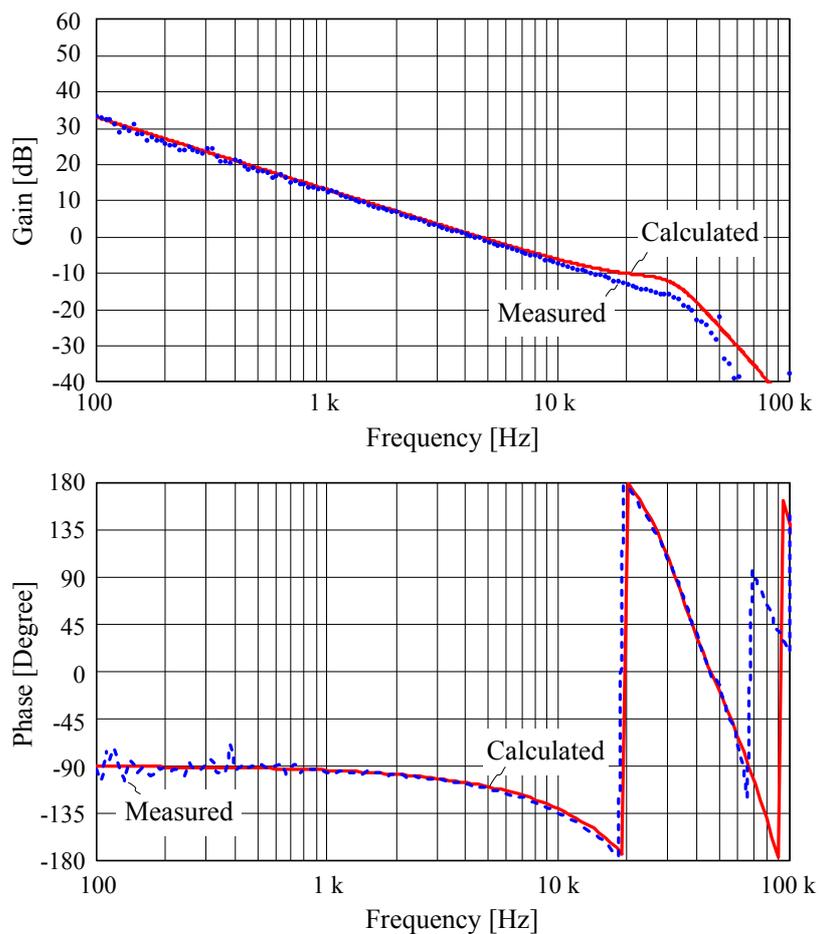


Figure 4.27: Comparison of the calculated and measured Bode plots of the open-loop transfer function of P-MCA.

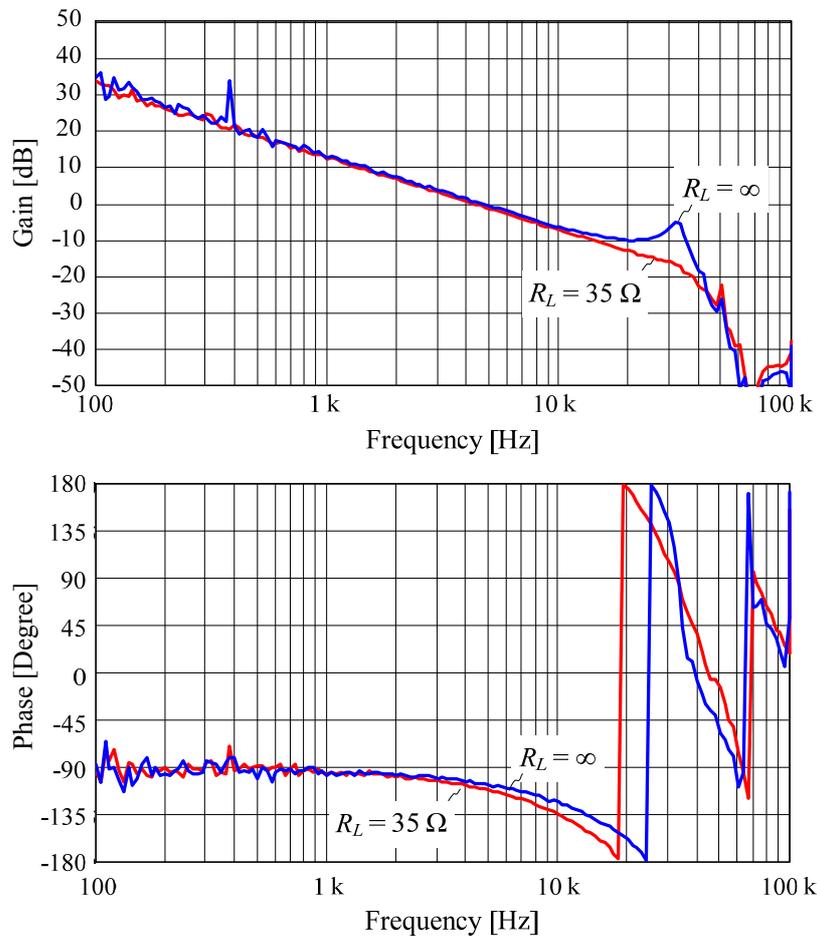


Figure 4.28: Measured Bode plots of the open-loop transfer function of P-MCA for nominal load and no-load conditions.

Figure 4.28 demonstrates the measured Bode plots of the open-loop transfer function of P-MCA for the nominal load and no-load conditions. It shows the system to be stable even for no-load operation.

The measured Bode plots of the closed-loop transfer function of P-MCA for the nominal load and no-load conditions are illustrated in Figure 4.29. The “-3 dB frequency” is about 7 kHz.

Finally, the calculated and measured Bode plots of the P-MCA output impedance are shown in Figure 4.30, which are almost identical with curves measured from AP-MCA (see Figure 4.10).

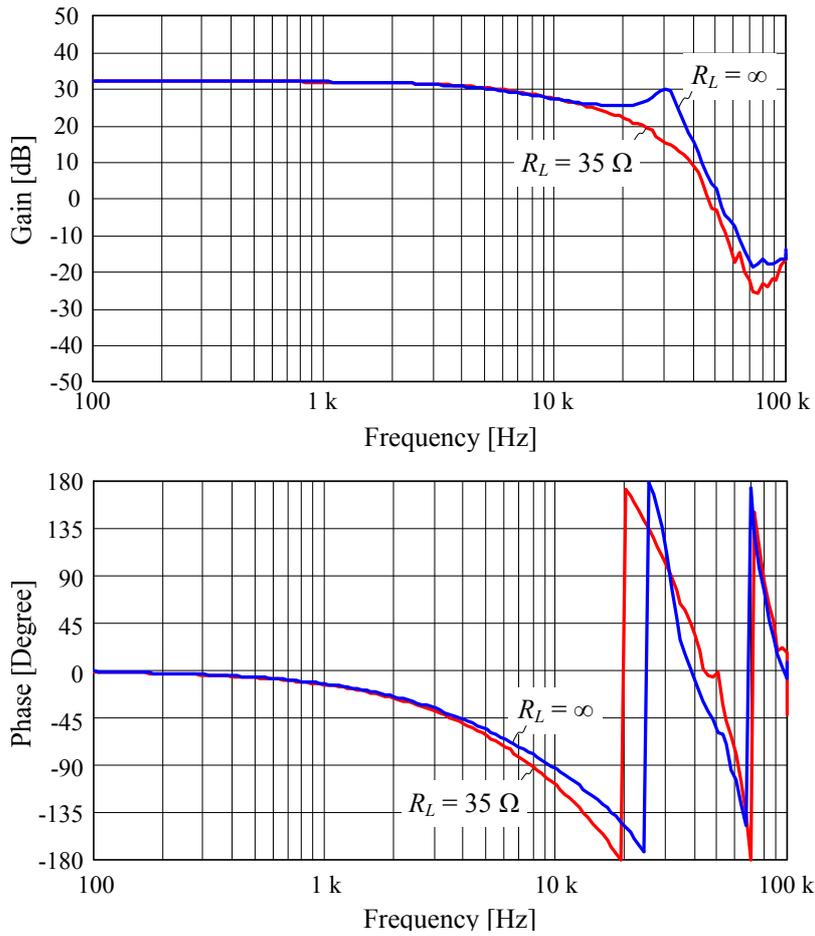


Figure 4.29: Measured Bode plots of the closed-loop transfer function of P-MCA for the nominal load and no-load conditions.

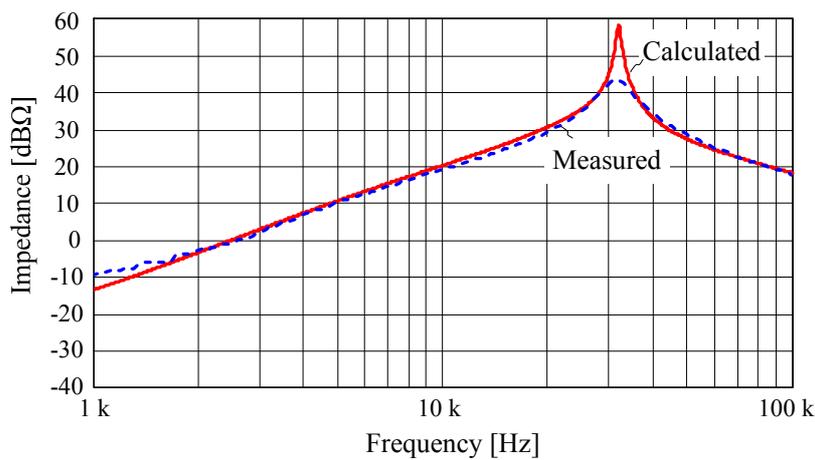


Figure 4.30: Comparison of the calculated and measured Bode plots of P-MCA output impedance.

4.3.3 Experimental Results

In order to have a fair comparison among H-MCA, AP-MCA, and P-MCA later, the same test conditions are selected which is according to the 135 V output voltage range as specified in Table 5.1. The laboratory prototype for testing is described in Chapter 5.

The measured time behaviours of the multi-cell inverter output voltage u_{mo} , output voltage u_o , and output current i_o for three different rms output voltages $U_{o,rms}$, 70 V, 100 V and 130 V, are shown in Figure 4.31. In the full output voltage range, a clean sinusoidal output voltage waveform is achieved. Figure 4.32 depicts the experimental results of P-MCA outputting the nominal output voltage 115 V for different load condition, where it shows that P-MCA can supply non-ohmic loads without any system stability problem.

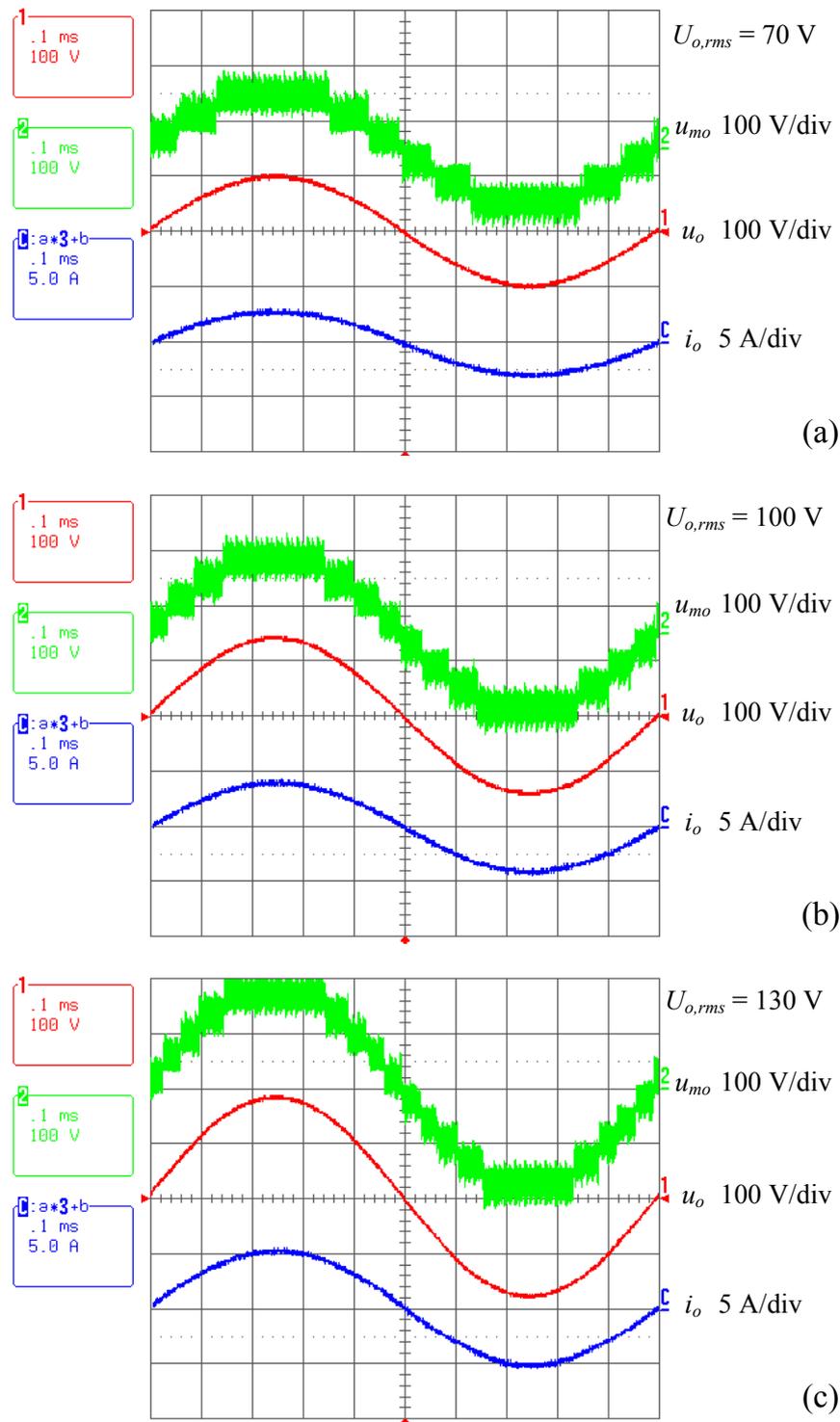


Figure 4.31: Measured time behaviours of the multi-cell inverter output voltage u_{mo} , output voltage u_o , and output current i_o for three different rms output voltages $U_{o,rms}$: 70 V (a), 100 V (b) and 130 V (c). Operation parameters: $U_{in} = 200$ V, $f_{sm} = 50$ kHz, $U_{o,rms} = 115$ V, $R_L = 35$ Ω , $f_o = 1$ kHz.

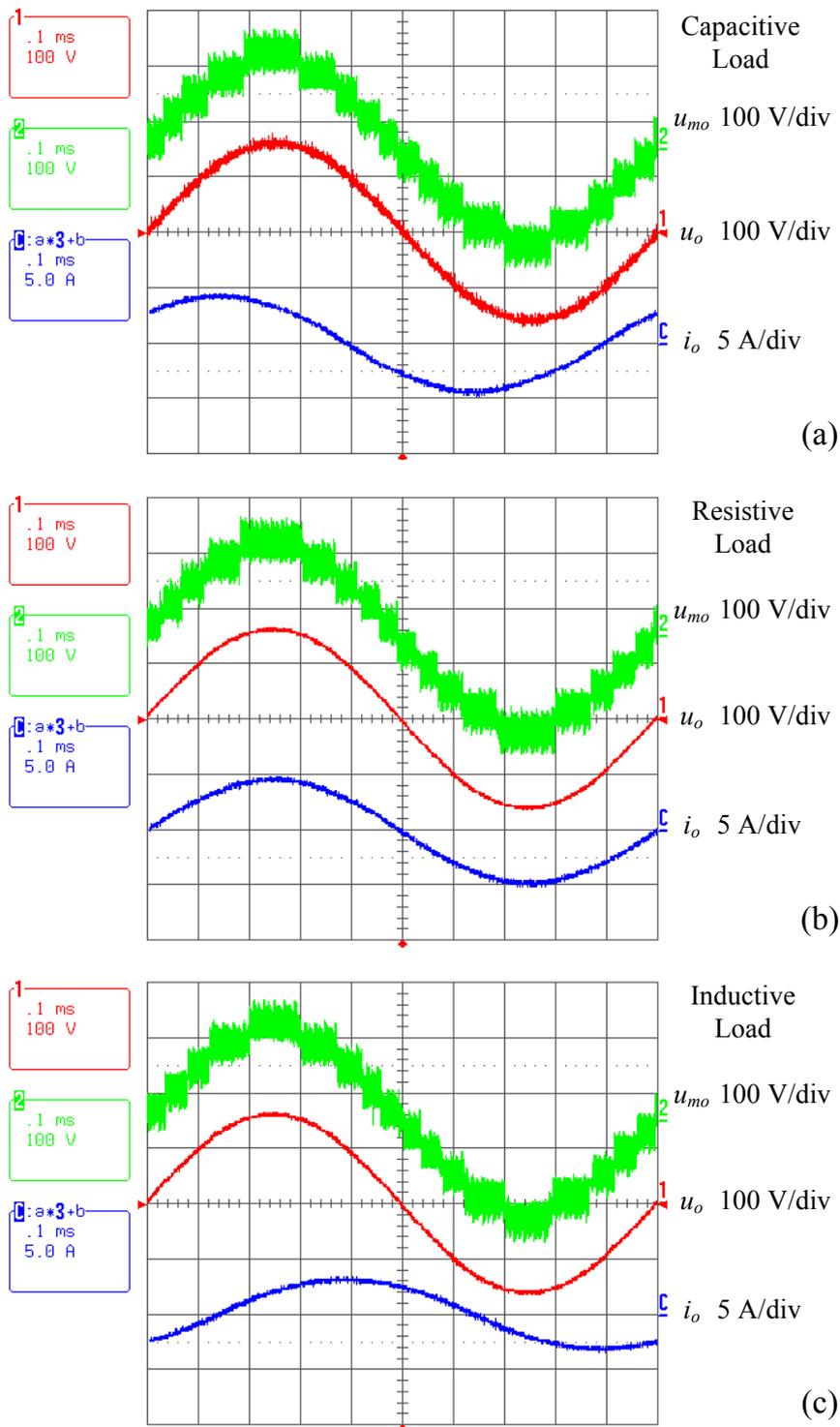


Figure 4.32: Measured time behaviours of the multi-cell inverter output voltage u_{mo} , output voltage u_o , and output current i_o for three different load conditions: capacitive load, $6.6 \mu\text{F}$ and 35Ω in series (a), ohmic load, $R_L = 35 \Omega$ (b) and inductive load 2.5 mH and 35Ω in series (c). Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_{sm} = 50 \text{ kHz}$, $f_o = 1 \text{ kHz}$.

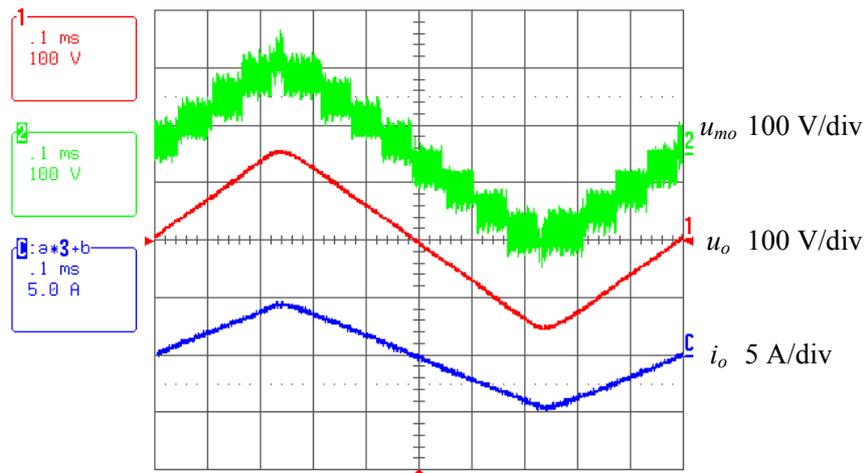


Figure 4.33: Experimental results for generating triangular output waveform. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{op} = 162 \text{ V}$, $f_{sm} = 50 \text{ kHz}$, $R_L = 35 \Omega$, $f_o = 1 \text{ kHz}$.

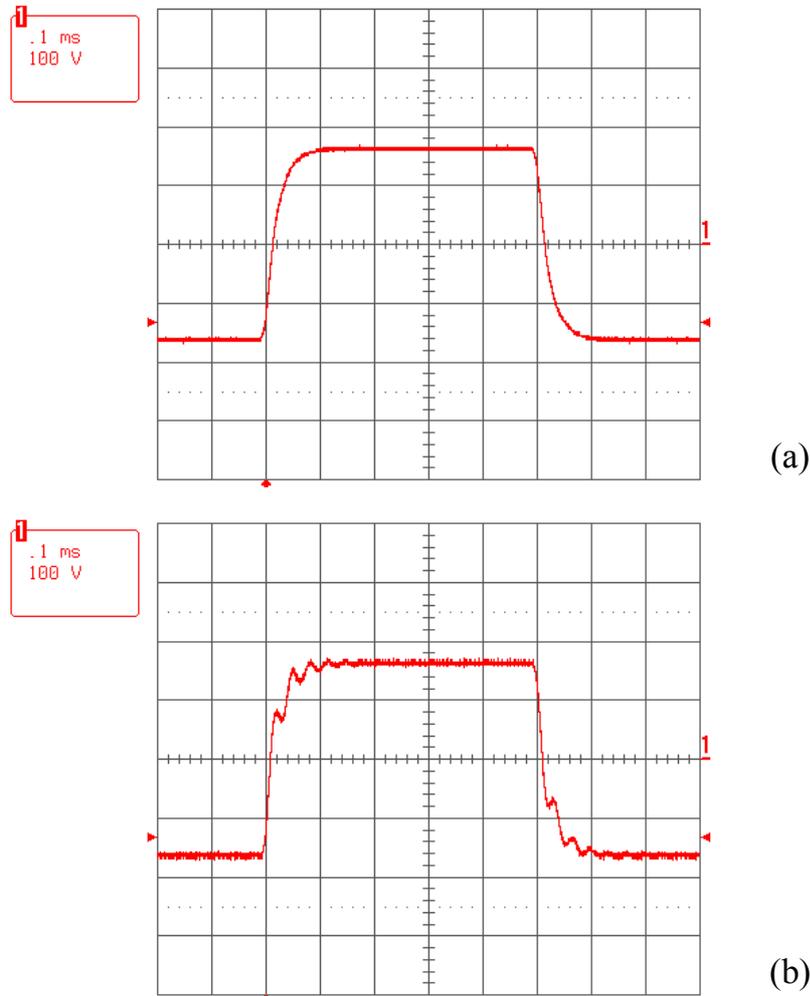


Figure 4.34: Experimental results for generating a rectangular output waveform connected with nominal load, $R_L = 35 \Omega$ (a), and no-load (b). Operation parameters: $U_{in} = 200 \text{ V}$, $U_{op} = 162 \text{ V}$, $f_{sm} = 50 \text{ kHz}$, $f_o = 1 \text{ kHz}$.

Figure 4.33 demonstrates the experimental results for generating a 1 kHz triangular output waveform, where the shape of the corners is softer compared to the output voltage of H-MCA because of the lower system dynamics. The measured rectangular output waveforms are shown in Figure 4.34. There is no voltage overshoot for nominal load, $R_L = 35 \Omega$, and no-load condition because of the sufficient phase margin of the control design.

In testing power source applications, it is usual to test with a non-linear load, e.g., for computer power supplies, etc.. The experimental result for supplying a non-linear load is shown in Figure 4.35, where the output current surges up to 9 A. However the output voltage shows some crossover distortion. These resonances are initiated by the reverse recovery of the rectifier diodes. For this test, a circuit of a full bridge rectifier followed by a 2.5 mH inductor in series with the parallel-connected 100 μF capacitor and 35 Ω resistor is used as the load.

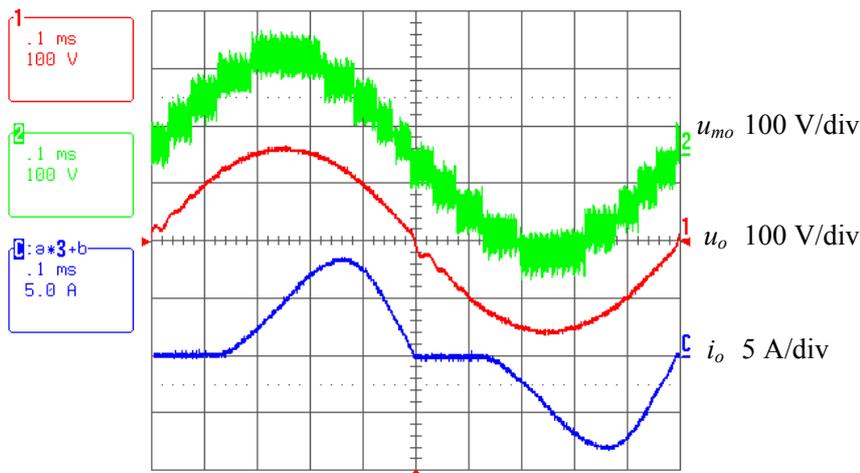


Figure 4.35: Experimental results for supplying a non-linear load. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_{sm} = 50 \text{ kHz}$, $f_o = 1 \text{ kHz}$.

The measured large-signal output voltage in dependency on the output frequency is depicted in Figure 4.36, where the input voltage is $U_{in} = 200 \text{ V}$ and the output voltage reference is fixed to $U_{o,rms,ref} = 115 \text{ V}$. At 7 kHz the output voltage drops to $U_{o,rms,ref}/\sqrt{2}$ (-3dB). Based on these measurements, the output voltage THD in dependency on the output frequency is demonstrated in Figure 4.37. The THD is less than 0.4% for output frequencies up to 1 kHz. In the THD calculation, the harmonics up to 40 times the

fundamental frequency are taken into consideration according to IEC 61000-3-2.

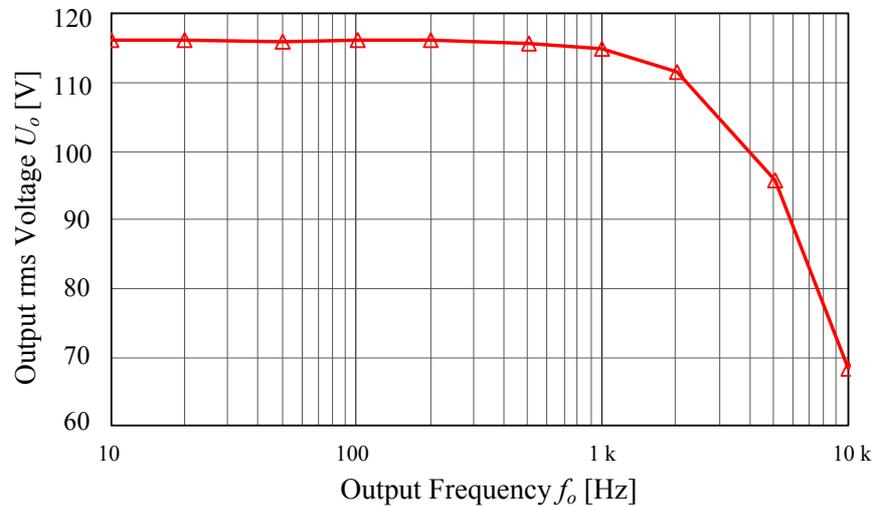


Figure 4.36: Measured large-signal output voltage in dependency on the output frequency f_o . Operation parameters: $U_{in} = 200$ V, $U_{o,rms,ref} = 115$ V, $f_{sm} = 50$ kHz, $R_L = 35$ Ω .

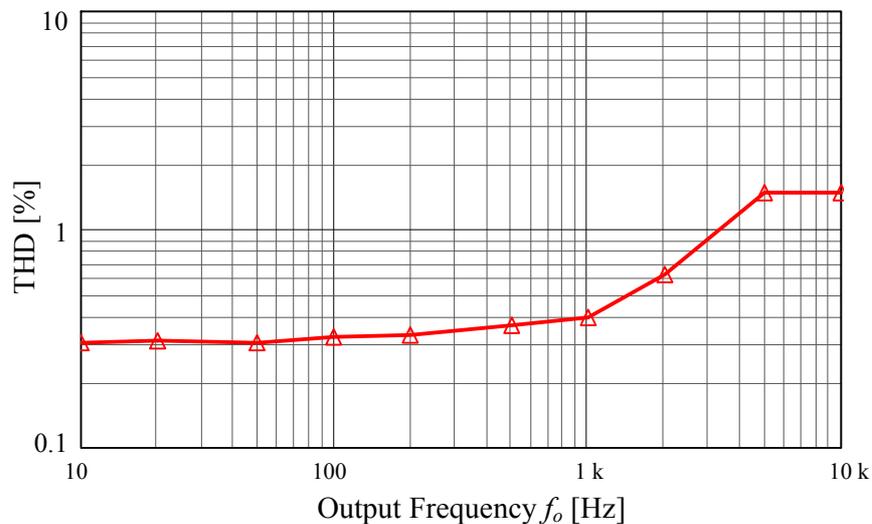


Figure 4.37: Measured output voltage THD in dependency on the output frequency f_o . Operation parameters: $U_{in} = 200$ V, $U_{o,rms} = 115$ V, $f_{sm} = 50$ kHz, $R_L = 35$ Ω .

The prototype efficiency curves are shown in Figure 4.38, where the system efficiency is similar to the AP-MCA system efficiency depicted in Figure 3.56. This is because both systems have the same effective switching frequency, i.e. 500 kHz.

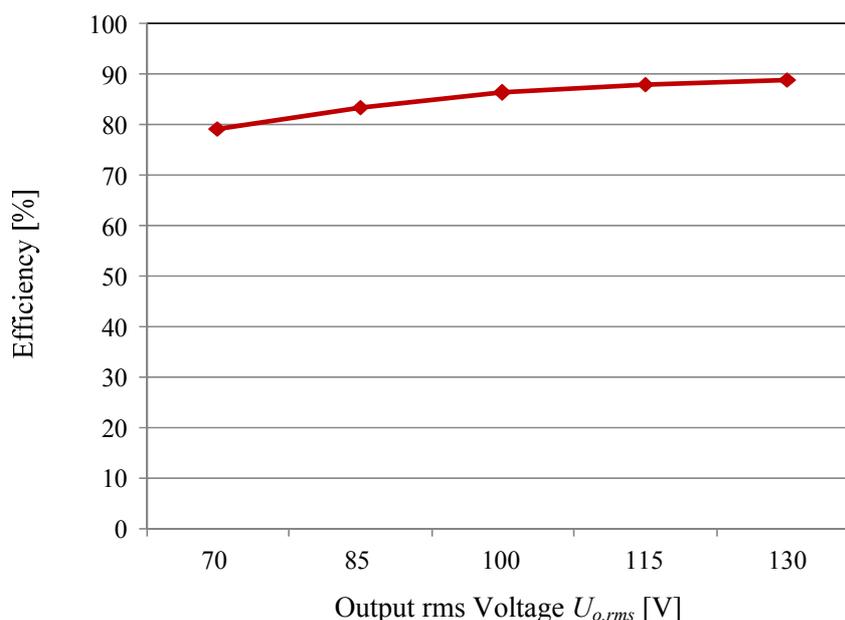


Figure 4.38: Measured system efficiency. Operation parameters: $U_{in} = 200$ V , $f_{sm} = 50$ kHz, $R_L = 35$ Ω , $f_o = 1$ kHz.

4.4 Conclusions

In this chapter, two multi-cell switch-mode power amplifiers, AP-MCA and P-MCA, are presented. The operation principles, small signal modelling and control design are described. Finally the experimental results measured from the universal laboratory prototype have verified the theoretical analysis.

For AP-MCA, AM + PWM hybrid modulation is utilized, while P-MCA only uses phase-shifted unipolar SPWM. Both systems have the equivalent switching frequency of 500 kHz.

Mixed analog and digital control is implemented for AP-MCA, where the AM modulation for the nine-cell inverter is realized by eighteen fast analog comparators and the PWM modulation of the class-D amplifier is done by DSP+FPGA. P-MCA employs a fully digital control.

A small signal model of AP-MCA that is considered as a PCT system is built and verified by frequency response measurements. Based on the small-

signal model, a simple PI-controller is designed. The experimental results show that the system is stable for the full range of load conditions, including the no-load condition. Similar modelling and control design is done for P-MCA as well. Both systems achieve a small-signal bandwidth of 4.5 kHz.

Both systems show low THD, that is less than 0.4% up to 200 Hz. However, the THD of AP-MCA deteriorates for higher output frequencies due to the internal disturbance of the nine-cell inverter output voltage.

The measured efficiencies of both systems are about 90% at 130 V output voltage supplying the nominal load of 35 Ω . The efficiency is significantly high than for the H-MCA.

Chapter 5.

Hardware and Performance Comparison

In this chapter, firstly the designed laboratory prototype for verifying the three different amplifier topologies is introduced; then the measurements from these amplifiers are compared.

5.1 Hardware Realization

In order to create a common basis for comparison, the specifications applying for all the amplifiers are given in Table 5.1. Because of different utility voltages in various countries and applications, each amplifier has two possibilities of output voltage ranges, a 135 V range and a 270 V range. The first voltage range is considered for testing equipments that are connected to lower voltage grids, e.g., U.S. utility grid, Japan utility grid and aircraft ac bus, etc.. The 270 V range is used for higher voltage grid application, e.g., European countries, most Asian countries except Japan, etc.

Table 5.1: Specifications of Laboratory Prototype

135V Range	270V Range
$U_{in} = 200 \text{ V}$	$U_{in} = 400 \text{ V}$
$U_{o,rms} = 0 \text{ V} \sim 135 \text{ V}$	$U_{o,rms} = 0 \text{ V} \sim 270 \text{ V}$
$R_{L,nom} = 35 \ \Omega$	$R_{L,nom} = 70 \ \Omega$
$P_o = 500 \text{ W @ } 135 \text{ Vac}$	$P_o = 1 \text{ kW @ } 270 \text{ Vac}$
$I_{o,max} = 4.5 \text{ A (continuous)}$	
Power bandwidth = 5 kHz	
Load phase angle = $-\pi/4 \dots +\pi/4$	

where U_{in} is the DC input voltage which could be provided by a bi-directional single phase rectifier, U_o is the rms value of the output voltage and spans the universal input voltage range, and P_o is the output power.

For both output voltage ranges, the amplifiers are able to output maximum 4.5 A continuous current. The nominal input voltage is regulated to be 200 V and 400 V respectively for the 135 VAC and 270 VAC output voltage ranges. This brings the benefit that the amplifiers can utilize all the levels for both output voltage ranges, so that the output voltage quality does not suffer when amplifiers generate low-amplitude output voltage. In the laboratory, an external DC power supply is used to produce the input voltages. An ac-dc bi-directional converter can be employed to provide the regulated dc voltage in an industrial application.

The power circuit scheme of the laboratory prototype is depicted in Figure 5.1. When designing the prototype, the following issues were considered:

- Flexible structure which allows a single hardware to perform all the three topologies.
- Compact and symmetric design.

Table 5.2: Jumper Table for Hardware Configuration of Different Topologies

Topology	J_1	J_2	J_3	J_4
H-MCA	1	1	1	1
AP-MCA (AM + PWM)	2	2	2	2
P-MCA (PWM)	2	2	2	2

Table 5.3: Components List

Name	Denotation	Type	Manufacture
Input Capacitor	C_i	2 X 100 μ F / 450 V	Nichicon
Primary MOSFETs	$T_{P11}, T_{P12}, T_{P21}, T_{P22}$	SPP20N60CFD	Infineon
Primary Resonant Capacitor	$C_{PX} (X=A...K)$	3 X 15 nF / 400 V	AVX
Transformer	$Tr_X (X=A...J)$	EFD 30/15/9, N87, 120:6	Epcos
Secondary MOSFETs	$T_{SX1}, T_{SX2} (X=A...K)$	IRF6648	IRF
Secondary Half Bridge Capacitor	$C_{SX1}, C_{SX2} (X=A...J)$	4 X 10 nF / 25 V	MuRata
Secondary DC Link Capacitor	$C_{SoX} (X=A...J)$	2 X 330 μ F / 50V	PANASONIC
Inverter MOSFETs	$T_{IX11}, T_{IX12}, T_{IX21}, T_{IX22} (X=A...K)$	IRF6648	IRF
Output Inductor	L_F	10 μ H, 10 A	RENCO
Output Damping Inductor	L_{d1}, L_{d2}	68 μ H, 6.2 A	C & D TECH.
Damping Resistor	R_d	2 X 10 Ω (parallel)	BI Technologies
Output Capacitor	C_F	220 nF / 500 VAC	EPCOS
Power Operational Amplifier		MP111FD	APEX

By the proper selection of the jumpers and different digital control coding, this prototype is able to perform three topologies: H-MCA (nine-cell AM inverter plus LPA), AP-MCA (nine-cell AM inverter plus one-cell PWM amplifier), and P-MCA (ten-cell PWM amplifier). Table 5.2 shows the jumper configurations for realizing the different topologies, where the jumpers are realized by using connectors and zero-ohm resistors. E.g., for switching the system from AP-MCA to H-MCA, one daughter board has to be plugged out and

The front and rear views of the ten-cell amplifier laboratory prototype are shown in Figure 5.2. This hardware comprises one mother board, five daughter boards, five mirrored daughter boards, one FPGA/measurement board, and one DSP board. The motherboard mainly serves as interface between FPGA/measurement board and daughter boards. Besides that, the primary MOSFETs as well as their gate drivers, the current sensors, output filter, LPA and main contactors are assembled on the mother-board as well.

The high frequency ac voltage bus generated by the primary full bridge provides the input voltage for all the daughter boards. Each daughter board, as shown in Figure 5.3, mainly consists of a resonant capacitor, isolation transformer, and the secondary side MOSFETs. The reason for designing five mirrored daughter boards is to limit the interfering high frequency ac voltage to a small area and to have a symmetric system design. Furthermore, four N-channel MOSFETs are used for each inverter cell. That requires that the corresponding four gate drivers must have three different ground potentials. There is an alternative way to form the H-bridge by using complementary P- and N-channel MOSFETs, which brings the benefits of reducing the realization effort and saving printed circuit board space.

Because of the large number of MOSFETs employed, the system requires forty nine independent gate control signals. Therefore, a 144-pin lattice FPGA chip, LCMXO2280C, with 2280 look-up tables (LUTs) and 113 I/Os is selected to fulfil the requirement in the FPGA/measurement board as demonstrated in Figure 5.4. This board also includes twenty high-speed comparators, MAX964, which are used for generating the AM inverter control signals with minimized delay time in H-MCA. The control signals measurement circuits are integrated in this board as well. The DSP board shown in Figure 5.5 is the universal DSP control board of the Power Electronic Systems (PES) Laboratory, ETH Zurich. This is equipped with the 16-bit, fixed point DSP controller from Analog Devices, ADSP-21992. This device also embeds 8-channel, 14-bit AD converters with up to 20 MSPS.

For H-MCA, the most important requirement for the linear power amplifier is that it must have a high enough slew rate to compensate for the ramp-up and ramp-down slope of the multi-cell inverter. In this design, the dv/dt of

the step voltages from the multi-cell inverter is designed as $50\text{V}/\mu\text{s}$. Therefore a commercial APEX power operational amplifier MP111FD, as shown in Figure 5.6, is used in the system. The main specifications of MP111FD are: $\text{SR} = 130 \text{ V}/\mu\text{s}$, $15\text{A} / 100\text{V}$, maximum allowed power dissipation $130\text{W}@60^\circ\text{C}$. This device is assembled in the central area of the mother board where the corresponding heat sink and fan have to be attached in addition, in order to dissipate the amplifier losses. Furthermore, the fins of the heat sink are placed horizontally so that the air blown by the fan can also flow to all the daughter boards, which helps to improve their thermal condition.

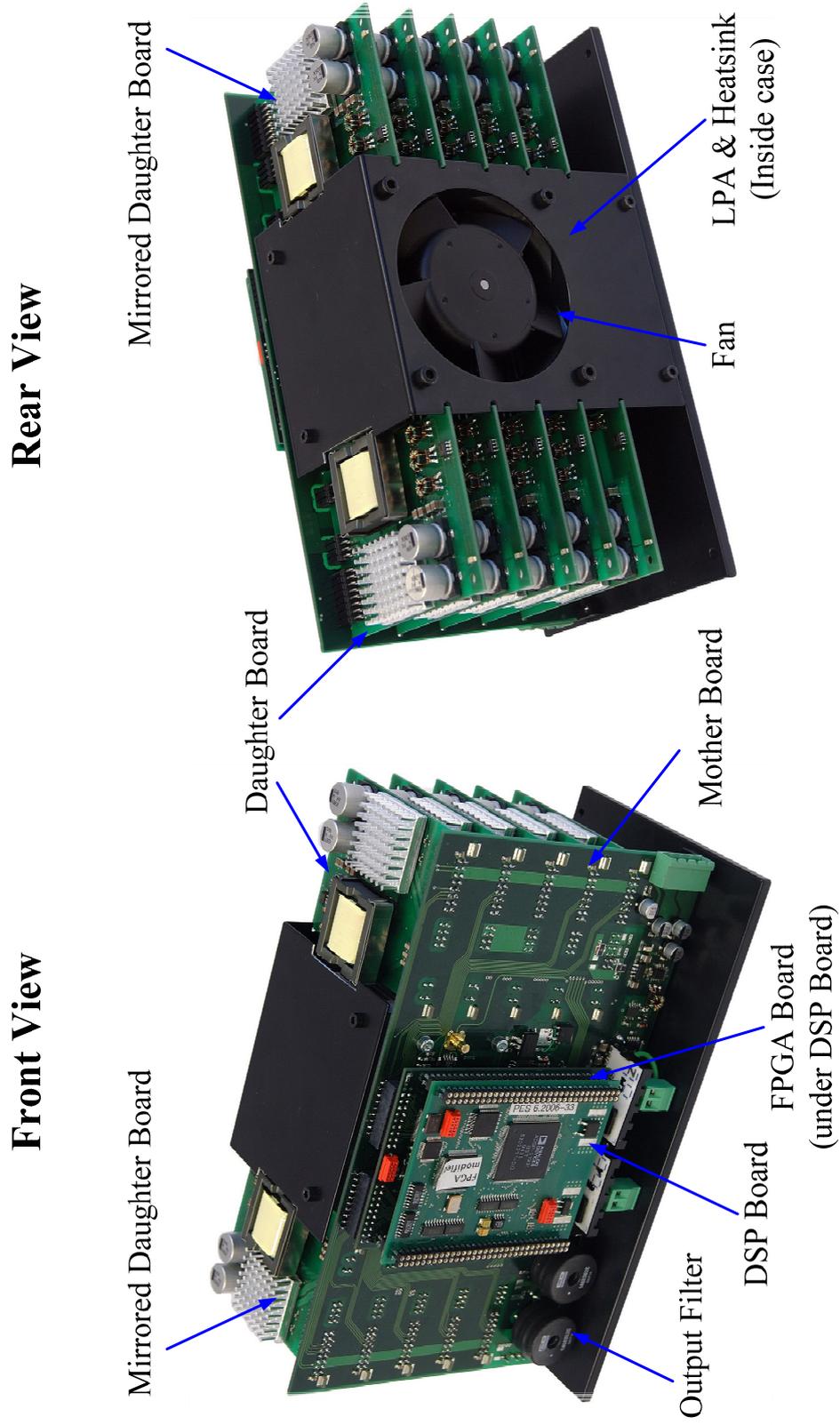


Figure 5.2: Photo of laboratory prototype with both front and rear views.

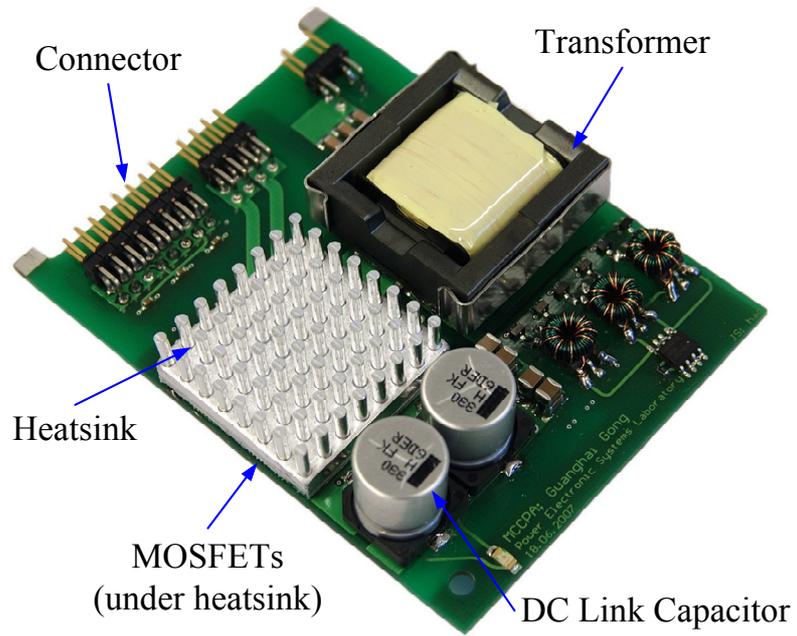


Figure 5.3: Photo of a daughter board.

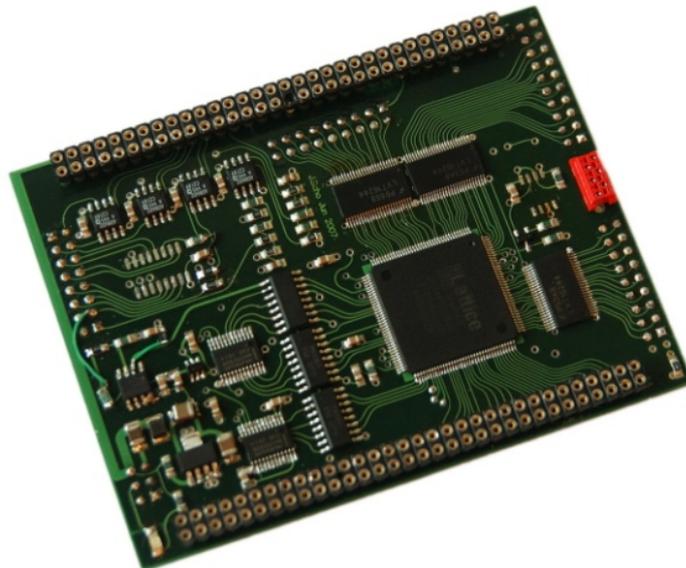


Figure 5.4: FPGA and measurement Board with 49 independent gate control signals.

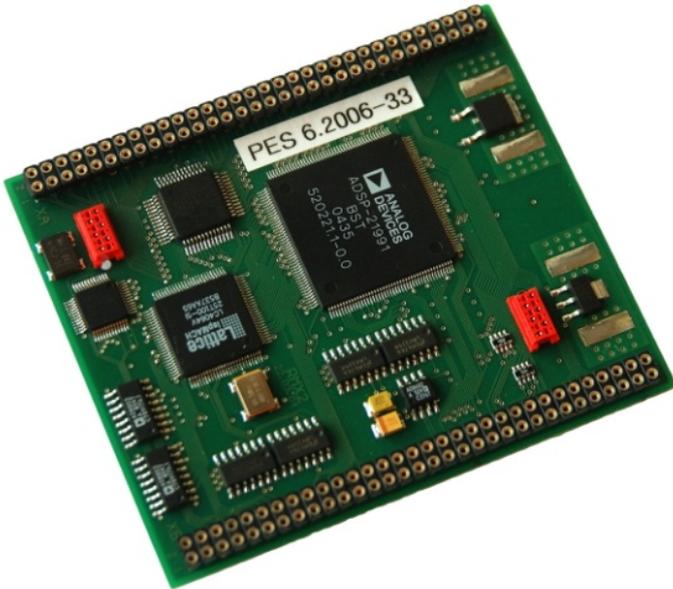


Figure 5.5: Universal DSP control board from Power Electronic Systems (PES), ETH Zurich.



Figure 5.6: APEX power operational power amplifier MP111FD. The dimensions are 41.4 mm x 63.2 mm x 11.5mm.

5.2 Performance Comparison of Multi-cell Amplifiers

Based on the universal prototype introduced in Chapter 5.1, the system performances of H-MCA, AP-MCA and P-MCA are measured and compared.

Figure 5.7 shows the key system waveforms at nominal operation. In H-MCA, the sinusoidal output voltage is achieved by using a high slew rate LPA to correct the stair-shaped voltage generated by the multi-cell inverter. For AP-MCA and P-MCA, the output voltage is attained by low-pass filtering the 500 kHz switching ripple in u_{mo} , where AM+SPWM and phase-shifted unipolar SPWM are utilized for AP-MCA and P-MCA respectively. Both H-MCA and P-MCA generate smooth 1 kHz sinusoidal output voltage waveforms, whereas there is notable distortion in the output voltage produced by AP-MCA. This distortion is due to the fact that the control system does not have sufficient attenuation for the disturbance caused by the AM modulated multi-cell output voltage, as explained in Chapter 4.2.3. In the following measurements, the nominal output frequency is reduced to 200 Hz in order to guarantee a clean output voltage shape. Furthermore, H-MCA shows much less common-mode noise in contrast with other two systems.

The measured waveforms for supplying an inductive load of 2.5 mH / 35 Ω in series are demonstrated in Figure 5.8. The experimental results presented in the previous two chapters also show that all three systems are able to feed a non-resistive load as specified in Table 5.1 without any stability problem.

Figure 5.9 illustrates the experimental results when the systems generate rectangular waveforms for nominal load. H-MCA shows the highest slew rate of 60 V/ μ s but with a voltage overshoot of 6%. There is no voltage overshoot for P-MCA but it has the slowest slew rate that is only 6.5 V/ μ s. AP-MCA is not suitable for generating rectangular output voltage because of the excessive overshoot.

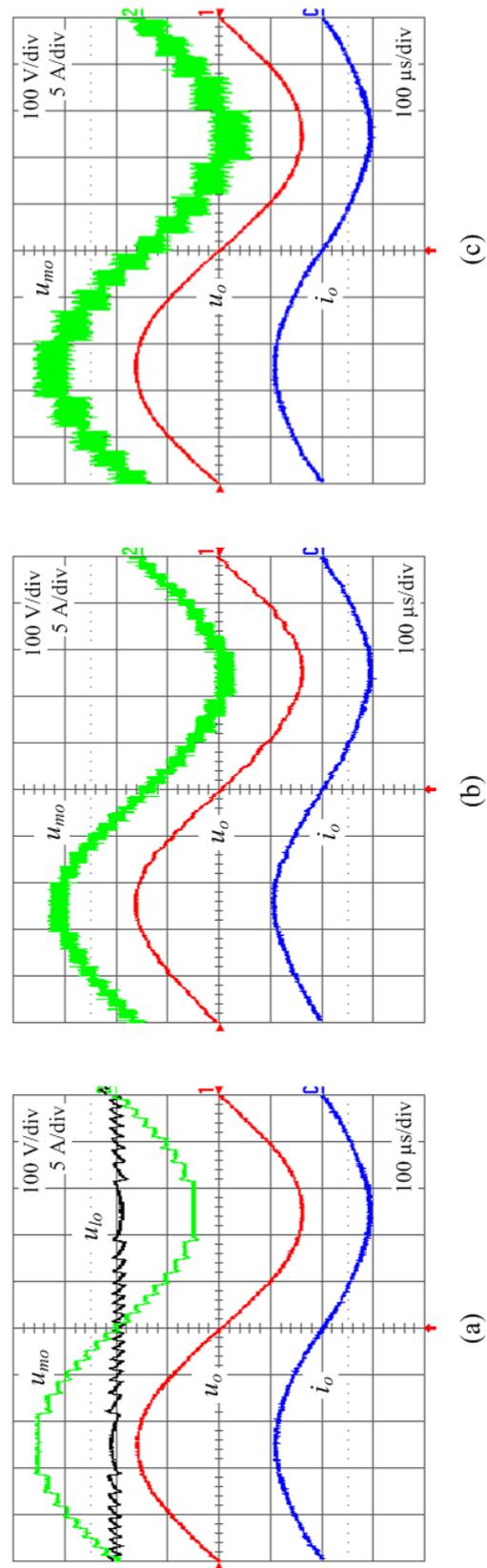


Figure 5.7: Key waveforms at nominal operation: (a) H-MCA, (b) AP-MCA, (c) P-MCA. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $R_L = 35 \Omega$, $f_o = 1 \text{ kHz}$.

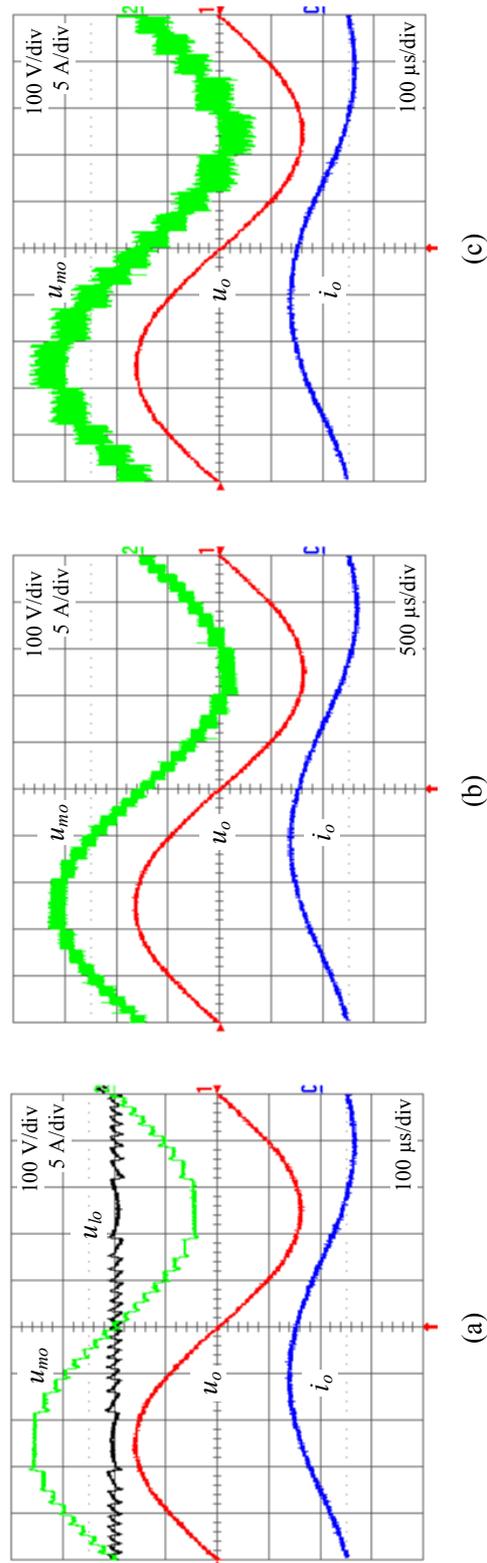


Figure 5.8: System operation for an inductive load of 2.5 mH / 35 Ω in series: (a) H-MCA, (b) AP-MCA, (c) P-MCA. Operation parameters: $U_{in} = 200$ V, $U_{o,rms} = 115$ V, $f_o = 1$ kHz (200 Hz for AP-MCA).

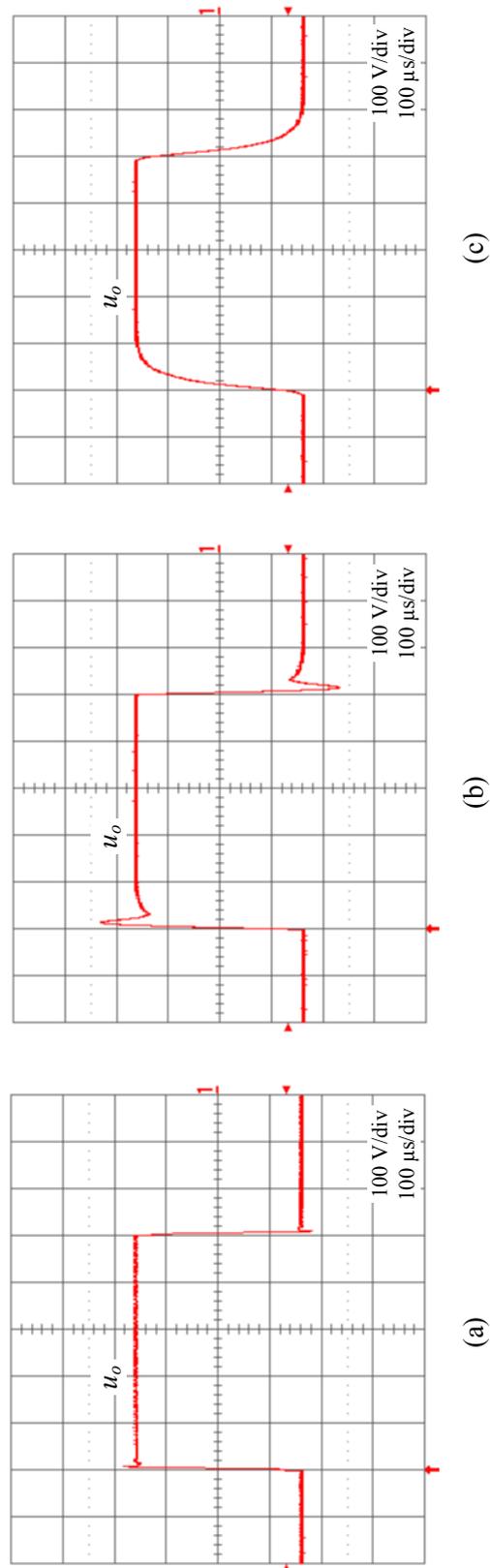


Figure 5.9: System behaviour for rectangular output waveform: (a) H-MCA, (b) AP-MCA, (c) P-MCA. Operation parameters: $U_{in} = 200$ V, $U_{op} = 162$ V, $R_L = 35$ Ω , $f_o = 1$ kHz.

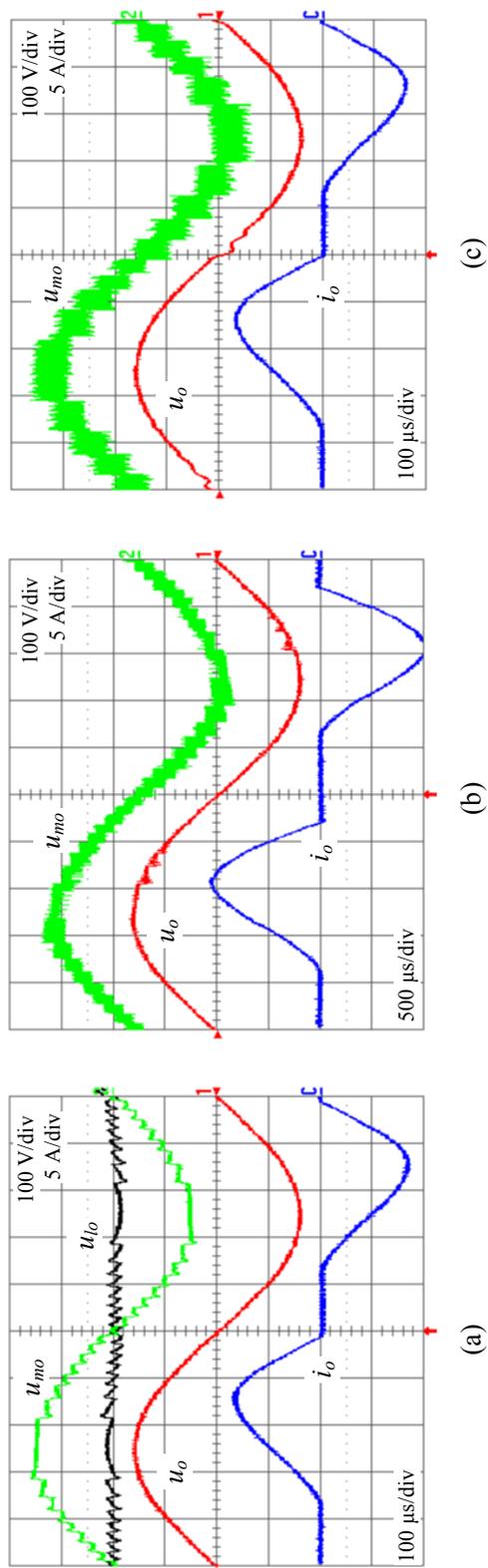


Figure 5.10: System behaviour for supplying a non-linear load whose parameters are specified in Chapter 3.7: (a) H-MCA, (b) AP-MCA, (c) P-MCA. Operation parameters: $U_{in} = 200 \text{ V}$, $U_{o,rms} = 115 \text{ V}$, $f_o = 1 \text{ kHz}$ (200 Hz for AP-MCA).

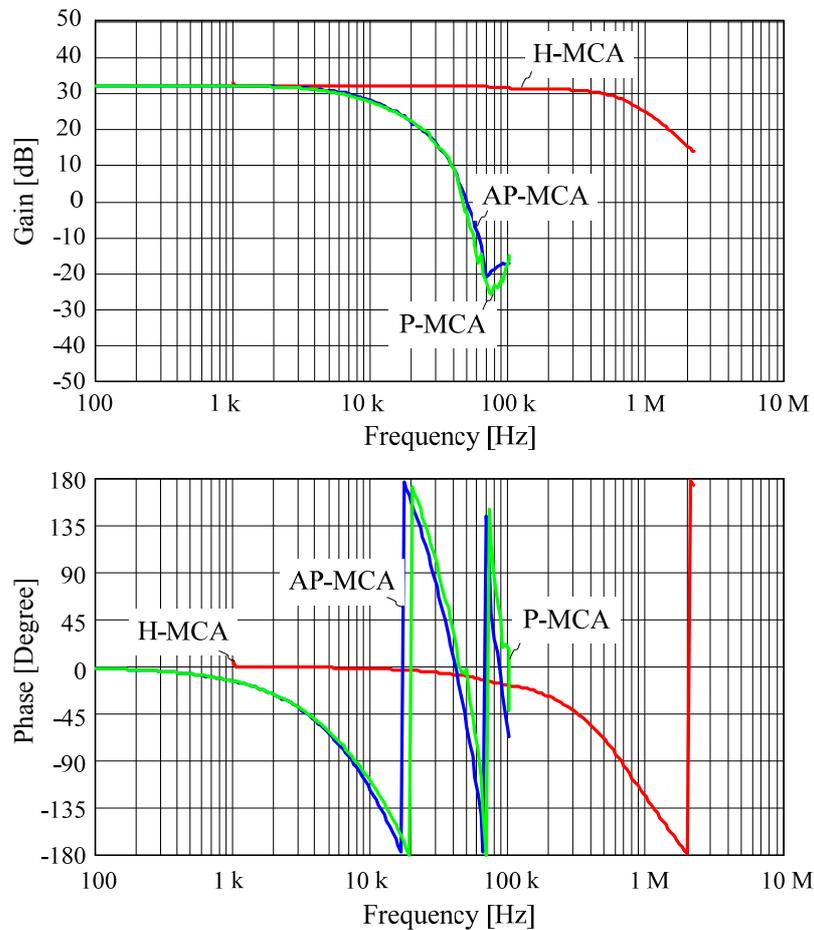


Figure 5.11: Bode plots of small-signal input-to-output transfer function. DC operation parameters: $U_o = 120 \text{ V}$, $R_L = 35 \Omega$.

The performances of the systems for supplying a non-linear load are compared in Figure 5.10. H-MCA shows the cleanest output voltage shape. There is a small crossover distortion occurring in the output voltage of P-MCA. In AP-MCA, the peak current is larger because of the lower test frequency applied. The over-current causes too much voltage drop in the dc supply voltages of the inverter cells, hence a distortion occurs in AP-MCA.

Figure 5.11 shows the measured Bode plots of the small-signal input-to-output transfer functions. H-MCA has a much higher bandwidth, 600 kHz, compared to that of AP-MCA and P-MCA, which is about 7 kHz. H-MCA also has much lower output impedance in contrast to AP-MCA and P-MCA as demonstrated in Figure 5.12. The reasons are that H-MCA has a much higher

bandwidth and the dv/dt filter has higher corner frequency and a much higher damping factor compared to the output filters of AP-MCA and P-MCA.

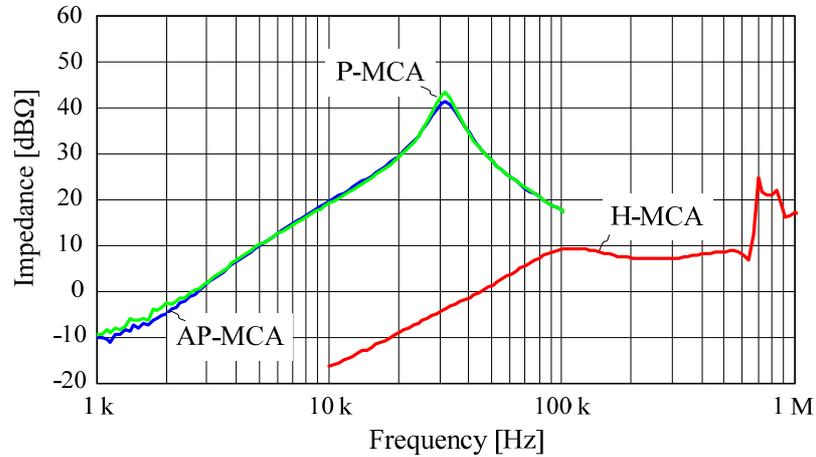


Figure 5.12: System output impedance in dependency on the output frequency. DC operation parameters: $U_o = 120 \text{ V}$, $R_L = 35 \Omega$.

The large-signal output voltage in dependence on the output frequency for a specified output voltage reference $U_{o,rms,ref} = 115 \text{ V}$ is measured and compared in Figure 5.13, where the output voltage amplitude of H-MCA is able to be kept almost constant for the frequency range from 10 Hz to 10 kHz. But the output voltage amplitude of P-MCA starts to fall after 1 kHz because of the limited bandwidth.

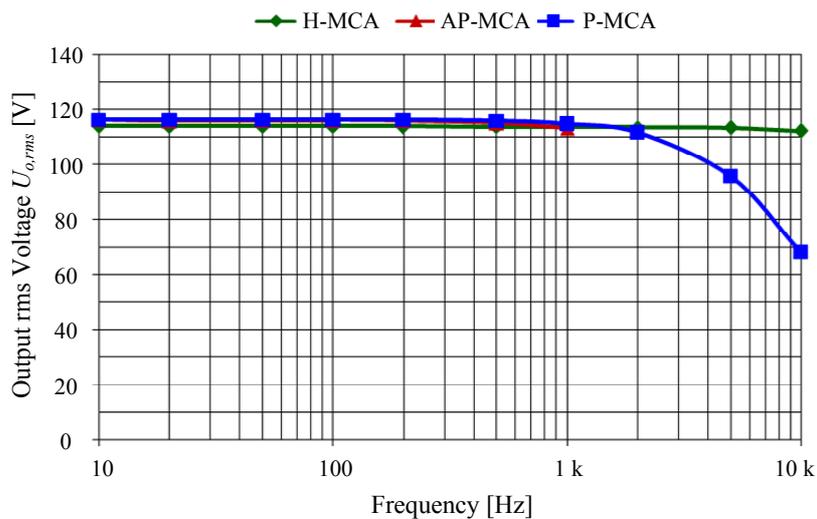


Figure 5.13: Large-signal output voltage in dependency on the output frequency for a specified output voltage reference of $U_{o,rms,ref} = 115 \text{ V}$.

Figure 5.14 shows the measured THDs of the output voltage. There H-MCA and P-MCA show similar THD values from 10 Hz to 10 kHz. However the THD of AP-MCA increases very fast after 200 Hz because of the internal disturbance, as discussed already.

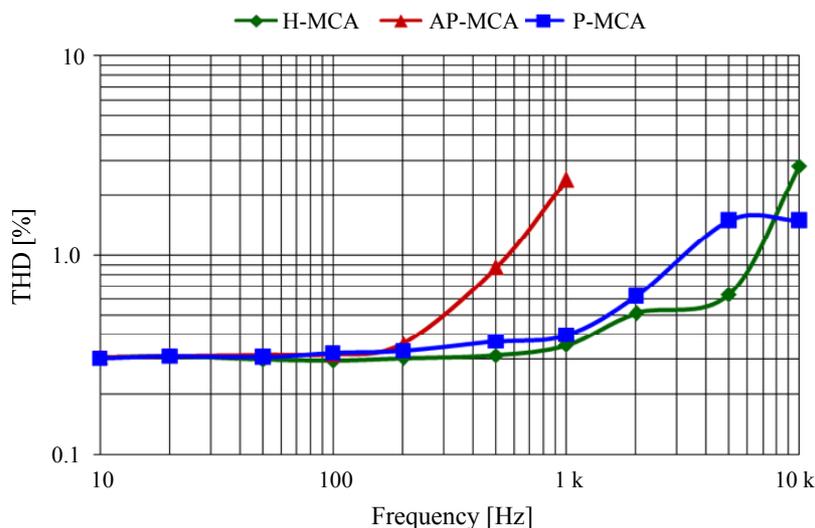


Figure 5.14: THD of the output voltage in dependency on the output frequency where $U_{o,rms,ref} = 115$ V.

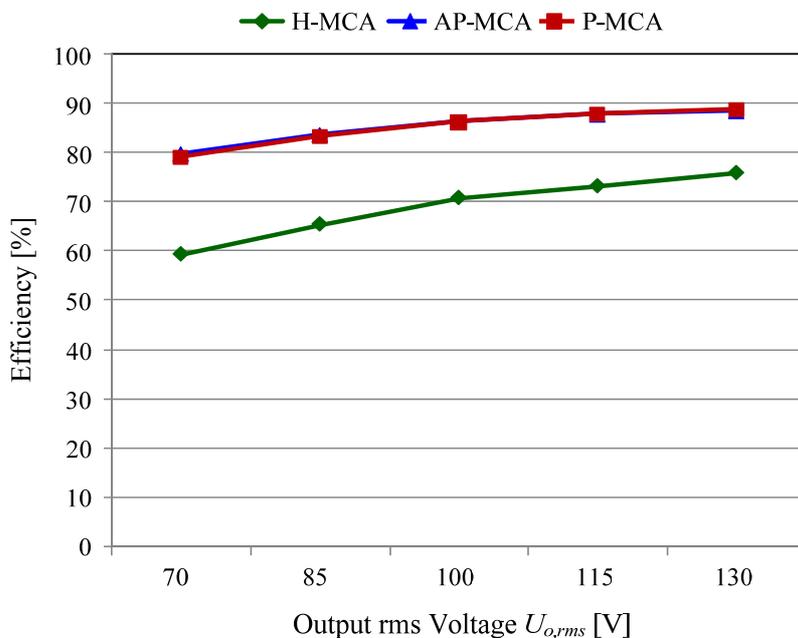


Figure 5.15: Measured system efficiency in dependency on the output voltage for nominal load.

The measured system efficiencies are depicted in Figure 5.15, where AP-MCA and P-MCA have an increased efficiency by at least 13% compared to H-MCA due to eliminating the LPA.

The main system performances that have been compared above are summarized in Table 5.4.

Table 5.4: System Performance Comparison.

Topologies	H-MCA	AP-MCA	P-MCA
Efficiency ($U_{o,rms} = 130 \text{ V}$, $R_L = 35 \Omega$)	76%	89%	89%
Slew Rate ($U_{op} = 162 \text{ V}$, $R_L = 35 \Omega$)	60 V/ μ s	32 V/ μ s	6.5 V/ μ s
THD ($U_{o,rms} = 115 \text{ V}$, $R_L = 35 \Omega$, $f_o = 1 \text{ kHz}$)	0.35%	2.4%	0.39%
Power Bandwidth	10 kHz	1 kHz	7 kHz
Small-signal Bandwidth	600 kHz	8 kHz	7 kHz
Output Impedance ($f = 10 \text{ kHz}$)	0.16 Ω	10 Ω	10 Ω

5.3 Conclusions

An universal laboratory prototype with a compact and symmetric design is presented. This prototype is able to perform three topologies: H-MCA, AP-MCA, and P-MCA, by proper selection of jumpers and different digital control coding. The performances of these three amplifiers are measured from the prototype and compared.

All three amplifiers are able to produce clean sinusoidal output voltage waveforms for both resistive and non-resistive loads. H-MCA has a power bandwidth of 10 kHz and the P-MCA power bandwidth is 8 kHz. But the power bandwidth of AP-MCA is limited to 1 kHz because of the voltage distortion caused by the internal disturbance. Here the power bandwidth is defined in a way that we not only look at the “-3dB” frequency but also at the THD value which is limited to a maximum of 2%.

P-MCA shows the advantages of simple modulation/low implementation effort, high efficiency, low THD, sufficient power bandwidth, and no overshoot voltage for step response. But it has a limited slew rate of only $6.5 \text{ V}/\mu\text{s}$. This topology can be employed for low cost ac power source applications which do not require very high dynamics, or as grid utility interface for renewable energy applications.

Concerning the system dynamics, H-MCA is obviously the best topology, possessing many merits like high slew rate, high power and small-signal bandwidth, low output impedance that make it have excellent performance in the case of non-linear load, and low THD. However the system performance is impaired by the low efficiency and this system is relatively costly compared to the pure switch-mode amplifiers.

The output voltage quality at high frequencies of AP-MCA suffers from the AM+SPWM hybrid modulation scheme. There the control signals of the AM multi-cell inverter are obtained by comparing the input reference signal and a series of threshold voltages, so that the feedback voltage has no influence on determining the output voltage of the AM multi-cell. Thus this multi-cell inverter acts as a disturbance voltage source for the control system.

Conclusions and Outlook

Conclusions

In this thesis, two novel hybrid power amplifiers have been presented. The first hybrid power amplifier connects a 3-level buck-boost converter with adjustable output voltages with a linear power amplifier in a cascaded way. The second hybrid power amplifier, H-MCA, connects a high slew rate linear power amplifier and H-bridges cells in series. These two hybrid power amplifiers belong to hybrid type I and type II respectively.

Besides these two hybrid systems, two other switch-mode amplifiers, AP-MCA and P-MCA, are analyzed and designed. The system performances of efficiency, power bandwidth, dynamic behavior, output voltage THD and output impedance measured from a universal laboratory prototype are compared with H-MCA.

TPS+LPA

A new boost-type TPS topology for conditioning the supply voltages of a LPA has been proposed which reduces the voltage drops across the linear amplifier power transistors to low values and therefore considerably lowers the amplifier power losses. This proposed boost-type TPS has some major advantages over the existing buck-type tracking power supplies, such as no requirement for dc bus voltage to be higher than the output voltage, small

output filter and high output voltage dynamics. These benefits make the boost-type TPS more suitable for high output voltage applications, e.g., testing power sources.

The theoretical calculations demonstrate that the power transistor losses in the LPA are significantly reduced when employing variable supply voltages. The current stresses on the power semiconductors of the proposed system are calculated analytically. The output filter is implemented and dimensioned according to the PSRR of the LPA to ensure a high output voltage quality of the system. Furthermore, the small signal model of the TPS is derived, and based on this model the constant current loop and feed-forward control are designed to insure the inductor current remaining constant even when the output power is varying at high frequency. An active damping strategy for the output filter which is easy to implement is designed. As an example for testing application of single-phase aircraft equipment, a 1kW laboratory prototype including TPS and LPA is built to verify the theoretical analysis. The experimental system shows a clear system efficiency improvement compared to a conventional class-AB LPA and a high output voltage dynamic of $6V/\mu s$ is achieved. As a result, the proposed system is applicable for linear amplifiers generating large amplitude output signals in the kHz range.

H-MCA

An isolated multi-cell cascaded power amplifier with high efficiency, high bandwidth, and wide load displacement range is presented. Firstly the operation principle and AM scheme are described. Due the limited bandwidth of the LPA, the slew rate of the inverter output voltage has to be limited for guaranteeing a clean output waveform. A simple method to limit the slew rate of inverter output voltage is developed, which utilizes a dv/dt filter composed of a LC filter with a LR damping network.

Loss calculations show a significant efficiency improvement compared to a conventional class-AB power amplifier, especially for non-linear load conditions. Furthermore, it also shows that the major system losses come from

the LPA part and the power losses of the multi-cell inverter can be almost neglected because it operates at the output voltage frequency.

An isolated, bidirectional dc-dc converter is developed to provide the power for the inverter cells and the linear power amplifier. The simple 50% fixed-duty cycle control is implemented and the converter achieves $\pm 5\%$ load regulation through careful circuit parameters design.

Based on the measured small signal model of APEX MP 111 and the dv/dt filter, the feedback loop is designed. A system bandwidth of 570 kHz is obtained.

For the measured data from the laboratory prototype under the test condition of 135 V output voltage range specifications, H-MCA shows the performances of 570 kHz system bandwidth, 60 V/ μ s maximum slew rate, 0.6% THD up to 5 kHz and 76% system efficiency at $U_{o,rms} = 135$ V, $R_L = 35 \Omega$, which by the way can be further improved through optimising the dc supply voltages of the LPA.

AP-MCA & P-MCA

Two multi-cell switch-mode power amplifiers, AP-MCA and P-MCA, are presented. The operation principles, small signal modelling and control design are described. The experimental results measured from the universal laboratory prototype verified the theoretical analysis.

For AP-MCA, AM + PWM hybrid modulation is utilized, while P-MCA only uses phase-shifted unipolar SPWM. Both systems have the equivalent switching frequency of 500 kHz. Mixed analog and digital control is implemented for AP-MCA, where the AM modulation of the nine-cell inverter is realized by eighteen fast analog comparators and the PWM modulation of the class-D amplifier is done by DSP+FPGA. P-MCA employs a fully digital control.

A small signal model of AP-MCA, that is considered as a PCT system, is built and verified by frequency response measurements. Based on the small-signal model, a simple PI-controller is designed. The experimental results

show that the system is stable for the full range of load conditions, including the open-load condition. A similar modelling and control design is done for P-MCA. Both systems achieve a small-signal bandwidth of 4.5 kHz.

Both systems show low THD, less than 0.4% up to 200 Hz. However, the THD of AP-MCA deteriorates for high output frequency due to the internal disturbance of the nine-cell inverter output voltage. The measured efficiencies of both systems are about 90% at 130 V output voltage supplying the nominal load of 35 Ω . The efficiency is significantly higher than for H-MCA.

Prototype & Comparison

A universal laboratory prototype with a compact and symmetric design is developed to verify the theoretical analysis. This prototype is able to perform three topologies: H-MCA, AP-MCA, and P-MCA, by proper selection of jumpers and different digital control coding. All three amplifiers are able to produce clean sinusoidal output voltage waveforms for both resistive and non-resistive loads. H-MCA has a power bandwidth of 10 kHz and P-MCA of 8 kHz. But the power bandwidth of AP-MCA is limited to 1 kHz because of the voltage distortion caused by the internal disturbance.

P-MCA has the advantages of simple modulation/low implementation effort, high efficiency, low THD, sufficient power bandwidth, and no overshoot voltage for step response. But it has a limited slew rate of only 6.5 V/ μ s. This topology can be employed for low cost ac power source applications which do not require very high dynamics, or as a grid utility interface for renewable energy applications.

Concerning the system dynamics, H-MCA is obviously the best topology, possessing many merits like high slew rate, high power and small-signal bandwidth, low output impedance, that makes it have excellent performance in the case of a non-linear load, and low THD. However the system performance is impaired by the low efficiency and this system is relatively costly compared to the pure switch-mode amplifiers.

For the AP-MCA, the output voltage quality at high frequencies suffers from the AM+SPWM hybrid modulation scheme. There the control signals of the

AM multi-cell inverter are obtained by comparing the input reference signal and a series of threshold voltages, hence the feedback voltage has no influence on determining the output voltage of the AM multi-cell inverter. Thus this multi-cell inverter acts as a disturbance voltage source for the control system.

Outlook

Based on the studies of the four hybrid and/or switch-mode amplifiers in this work, some ideas for improving the system performance in the course of further research are listed below.

TPS+LPA

- The experimental hardware could be extended to the topology shown in Figure 2.2(b), i.e. an isolated three-level buck-type dc-dc converter could be employed as the input stage.
- The output filter could be substituted by a higher order circuit in order to reduce the supply voltage phase shift when outputting high frequency signals.
- The selection of the width of the hysteresis band has a significant influence on the switching losses and the output filter size. For instance, if the band-width is reduced, the switching frequency increases. This results in high switching losses, but the filtering requirement is less due to the smaller voltage ripples. A numerical optimization could be implemented in order to optimise the band-width, with the objective of minimum volume or maximum efficiency.
- The adaptive current control scheme depicted in Figure 2.11 [31] could be implemented in order to further reduce the system losses.

H-MCA

- The fundamental assumption in the analysis of the steady-state character of the dc-dc bi-directional converter is that we consider i_p to have a sinusoidal shape. However, in the hardware i_p is not sinu-

soidal any more especially due to the sharp current step. A more accurate steady-state equivalent circuit model of the dc-dc bi-directional converter could be derived based on the analysis of the instantaneous current waveform.

- LPA design is the key to achieving better system performance. Instead of the commercial LPA used in H-MCA, a custom-designed LPA with higher power bandwidth could be employed, where the feed-forward control also could be applied as show in Figure 3.2. This would further improve the output voltage quality and dynamic behaviour.

AP-MCA & P-MCA

- For some applications where the flexibility to increase or decrease the output voltage is not necessarily required, an asymmetric multi-cell inverter would significantly reduce the number of inverter cells needed for generating the same number of output voltage levels.
- There would be several possibilities for further improvement of the system dynamics performance: reducing sampling time, using higher switching frequency / smaller output filter, or utilizing fast control methods, e.g., single-cycle control.

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Publications	<ul style="list-style-type: none">• G. Gong, H. Ertl, and J. W. Kolar, “Novel power supply for linear power amplifiers,” <i>IEEE Trans. on Industrial Electronics</i>, Vol. 55, pp. 684-698, Feb. 2008.• T. Nussbaumer, G. Gong, M. L. Heldwein, and J. W. Kolar, “Modeling and Robust Control of a Three-Phase Buck+Boost PWM Rectifier (VRX-4),” <i>IEEE Trans. on Industrial Applications</i>, Vol. 44, pp. 650-662, March-April 2008.• K. Mino, G. Gong, and J. W. Kolar, “Novel Hybrid 12-Pulse Line Interphase Transformer Boost-Type Rectifier with Controlled Output Voltage,” <i>IEEE Trans. on Aerosp. Electron. Syst.</i>, Vol. 41, pp. 1008 – 1018, July 2005.• G. Gong, M. L. Heldwein, U. Drofenik, J. Minibock, K. Mino, and J. W. Kolar, “Comparative Evaluation of Three-Phase High Power Factor AC-DC Converter Concepts for Application in Future More Electric Aircrafts,” <i>IEEE Trans. on Industrial Electronics</i>, Vol. 52, pp. 727 – 737, June 2005.• G. Gong, H. Ertl, and J. W. Kolar, “A multi-cell cascaded power amplifier,” in <i>Proc. 2006 Applied Power Electronics Conference</i>, pp. 1550-1556.

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