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Advanced Bidirectional Three-Phase Current/Voltage DC-Link Buck-Boost/Boost-Buck PFC AC/DC Converter Systems

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presented by

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致金晶。
致我的父母，艳岩和虎平。

To Jinjing.
To Yanyan and Huping, my parents.

Acknowledgments

I finally started to write this acknowledgment on a rainy Swiss national day and memory is journeying back and forth…

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Daifei Zhang
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世上本没有路，走的人多了，也便成了路。
– 鲁迅

Paths are not made in this world,
but as more people walk, they become roads.
– Lu Xun

Abstract

More efficient and compact electric vehicle (EV) chargers promote sustained transportation electrification towards a low-carbon economy. Advanced three-phase (3-Φ) bidirectional AC/DC converter systems with buck-boost functionality, e.g., with an extended output voltage range of 200 V to 1000 V, could be employed as standard building blocks in various galvanically isolated EV chargers, but could promisingly also serve as future RCD-based *non-isolated* EV chargers characterized by significantly increased efficiency and power density compared to state-of-the-art isolated EV charger solutions, and are accordingly reviewed and analyzed in this thesis comprehensively considering both the current DC-link (current source) and the voltage DC-link (voltage source) topologies.

A 3-Φ current DC-link buck-boost (bB) PFC AC/DC converter system, where a 3-Φ buck-type current source rectifier (CSR)-stage and a subsequent 3-L boost-type DC/DC-stage are combined through one advantageous shared DC-link inductor, is first selected from the category of current source converter systems. The buck functionality is achieved by operating the CSR-stage solely in 3/3-PWM without switching the DC/DC-stage such that the DC/DC-stage only creates the inevitable conduction losses but zero switching losses. In the boost-mode, the DC/DC-stage steps up the rectified voltage of the 3-Φ mains to a required large output value and, beneficially, shapes the DC-link current to follow the upper envelope of the absolute value of the 3-Φ currents to eliminate the zero switching state (shoot-through state) of the CSR-stage, i.e., the CSR-stage operates with 2/3-PWM. These loss-optimum operations, i.e., reduced number of switching instants due to clamping of one phase of the CSR-stage or the DC/DC-stage, and minimum possible DC-link current for any operating point, are guaranteed by a proposed synergetic control strategy. These favorable features are experimentally verified, including conducted EMI measurements, using a 10 kW hardware demonstrator with a power density of 6.4 kW/dm^3 (107.5 W/in^3) and a peak efficiency of 98.8%. The measured ultra-flat efficiency surface proves the expected highly efficient operation over wide output voltage and power ranges.

Furthermore, the synergetic control concept of the 3-Φ current DC-link bB PFC AC/DC converter system is extended to regulate two independent DC outputs for heavy-duty EVs. The loss-optimal operations are still retained, i.e., the reduced number of switching instants due to clamping of one phase of the CSR-stage (switching only two out of the three phases, i.e., 2/3-PWM) or individual clamping of the DC/DC-stage's two half-bridges, and minimum possible DC-link current for any operating point. Experimental confirmation

of the proposed control scheme using the built 10 kW demonstrator system is provided, and a significant measured efficiency improvement, e.g., from 97.9 % to 98.4 % (0.5 %) at 10 kW, is demonstrated, which is largely independent of output voltage asymmetries and load asymmetries.

Targeting *non-isolated* EV chargers based on the analyzed 3-Φ current DC-link bB PFC AC/DC converter system, a virtual grounding control (VGC) is proposed to operate the DC/DC-stage to compensate the low-frequency (LF) common-mode (CM) voltage resulting from the CSR-stage modulation and thus controls the LF CM voltage between the DC output and protective earth (PE) to zero. This enables further a direct connection of the DC output midpoint to PE, where an additionally proposed ground current control (GCC) prevents nuisance tripping of mandatory RCDs by regulating the measured LF CM ground current. The proposed concepts are verified on the realized 10 kW hardware demonstrator considering Terra-Terra (TT) and Terra-Neutral (TN) grounding systems. The proposed GCC successfully limits the LF CM leakage current to < 6 mA RMS, i.e., significantly below typical RCD trip levels, and, using the human-body impedance model according to UL 2202, achieves a test voltage of 110 mV that is clearly below the most stringent limit (250 mV) of the standard, which provides a viable solution for future *non-isolated* EV chargers.

Besides the aforementioned current DC-link topologies, such bidirectional AC/DC buck-boost converter systems can also be realized in the form of widely-analyzed voltage DC-link topologies. A three-level (3-L) realization of the 3-Φ voltage DC-link rectifier stage facilitates small EMI filters and hence compact converter realization so that a T-type (Vienna) voltage source rectifier (VSR)-stage is selected as front-end. To achieve buck-boost functionality, the boost-type VSR-stage must be combined with a buck-type DC/DC stage, which again advantageously is realized as a 3-L structure to reduce the magnetics volume and to enable controllability of the voltage DC-link midpoint potential. Thus, a 3-Φ voltage DC-link boost-buck (Bb) PFC AC/DC converter system is selected and studied from the category of voltage source topologies. For high output voltages, the VSR-stage continuously modulates all three phases to regulate the output voltage (3/3-PWM) while the DC/DC-stage remains clamped to avoid switching losses. For low output voltages, the DC/DC-stage advantageously controls the DC-link voltage to enable 1/3-PWM (only one of the three bridge-legs operates with PWM at any given time) of the VSR-stage with reduced switching losses. Furthermore, a novel 2/3-PWM scheme for the output voltage transition region, where output voltages are in between the buck-mode and the boost-mode operation limits,

guarantees operation with minimal losses, i.e., the minimum number of the VSR-stage bridge-legs operating with PWM, and with the minimum possible DC-link voltage, for any output voltage. These advantageous operations are ensured by a proposed synergetic control concept which achieves a seamless transition between the loss-optimum operating modes. A comprehensive experimental verification, including pre-compliance EMI measurements, using a 10 kW hardware demonstrator with a power density of 5.4 kW/dm^3 (91 W/in^3) and a peak efficiency of 98.8% confirms the theoretical analyses.

Finally, based on two realized hardware demonstrators, a comprehensive comparison of current and voltage DC-link buck-boost AC/DC converter systems is provided regarding hardware realization, synergetic control implementation, efficiency characteristics, and conducted EMI noise emissions. The thesis concludes with a summary of the main results and a discussion of future research areas.

Kurzfassung

Effizientere und kompaktere Ladegeräte für Elektrofahrzeuge unterstützen die Elektrifizierung des Transportsektors und die Transformation hin zu einer klimafreundlichen Wirtschaft. Fortschrittliche dreiphasige (3-Φ) bidirektionale AC/DC-Konverter mit Leistungsfaktorkorrektur (Power Factor Correction, PFC, d.h. Sinuseingangsstrom) und Hoch- und Tiefsetzstellerfunktion, d.h. einem weiten Ausgangsspannungsbereich von beispielsweise 200 V bis 1000 V bei Speisung aus einem 3-Φ-400 V-Netz, können einerseits in galvanisch getrennten, vielfach modular aufgebauten Fahrzeugladegeräten eingesetzt werden, bieten andererseits aber auch eine interessante Lösung für zukünftige mittels FI-Schutzschaltern überwachte nicht isolierte Ladegeräte, welche sich durch höhere Effizienz und Leistungsdichte (verglichen mit isolierten Ladegeräten) auszeichnen, und werden demgemäss in dieser Arbeit umfassend analysiert, wobei sowohl Topologien mit (Konstant)stromzwischenkreis als auch (Konstant)spannungszwischenkreis betrachtet werden.

Im ersten Schritt wird ein 3-Φ-AC/DC-Konverter mit PFC und Tief-Hochsetzfunktion und Stromzwischenkeis analysiert (3-Φ-bB-AC/DC-Konverter), d.h. die Kopplung eines 3-Φ-AC/DC-Tiefsetzstellersystems mit Stromausgang und eines Dreilevel-DC/DC-Hochsetzstellers mit Stromeingang über eine gemeinsame Zwischenkreisinduktivität betrachtet. Für Tiefsetzstellerbetrieb der Gesamtanordnung werden sämtliche Phasen der Gleichrichtereingangsstufe getaktet (3/3-PWM) und die DC/DC-Hochsetzausgangsstufe geklemmt, wodurch Schaltverluste der DC/DC-Stufe vermieden werden bzw. diese Stufe nur Leitverluste aufweist. Für Hochsetzstellerbetrieb wird die gleichgerichtete Spannung des 3-Φ-Netzes mittels der DC/DC-Stufe auf den gewünschten Spannungswert angehoben und weiters der Zwischenkreisstrom derart geformt, dass dieser der Einhüllenden der Absolutwerte der 3-Φ-Eingangsphasenstromsollwerte folgt, womit kein Freilauf- bzw. Nullschaltzustand der Eingangsstufe erforderlich ist und die Taktung unter deutlicher Einsparung an Schaltverlusten auf zwei von drei Phasen beschränkt werden kann (2/3-PWM). Diese synergetische verlustoptimierte Regelung von Gleichrichterstufe und DC/DC-Ausgangsstufe, welche die Zahl an Schalthandlungen dadurch reduziert, dass entweder der Schaltzustand von einer Phase der Gleichrichterstufe oder der Schaltzustand des Hochsetzstellers festgehalten/geklemmt und der Zwischenkreisstrom stets auf dem minimal erforderlichen Wert gehalten wird, wird durch die vorgeschlagene Regelstruktur auch für den Übergangsbereich zwischen reinem Tiefsetzsteller- und reinem Hochsetzstellerbetrieb des Gesamtsystems garantiert. Die vorteilhaften Eigenschaften des neuen Konzeptes werden experimentell, inklusive

EMV-Messungen, anhand eines Demonstratorsystems mit 10 kW Nennleistung verifiziert, welches eine Leistungsdichte von 6.4 kW/dm^3 (107.5 W/in^3) und eine Effizienz von bis zu 98.8% aufweist. Die gemessene, extrem flache Effizienzcharakteristik belegt die erwartete hocheffiziente Funktion über einen weiten Ausgangsspannungs- und Ausgangsleistungsbereich.

Darüber hinaus wird das synergetische Regelungskonzept des 3-Φ-bB-AC/DC-Konverters derart erweitert, dass zwei unabhängige Gleichspannungsausgänge für elektrische Nutzfahrzeuge zur Verfügung stehen. Der verlustoptimale Betrieb wird dabei weiterhin aufrechterhalten, d.h., es wird weiterhin die Anzahl an Schaltvorgängen entweder durch das Klemmen einer Phase der Gleichrichterstufe oder durch das Klemmen einer der beiden Halbbrücken des DC/DC-Hochsetzstellers reduziert und der Zwischenkreisstrom für jeden Arbeitspunkt minimiert. Das vorgeschlagene Regelkonzept wird mithilfe des 10 kW-Demonstratorsystems experimentell verifiziert und eine signifikante Steigerung der gemessenen Effizienz von 97.9 % auf 98.4 % (0.5 %) bei 10 kW, weitgehend unabhängig von Ausgangsspannungs- und Ausgangsleistungsasymmetrien nachgewiesen.

Mit Blick auf zukünftige nicht isolierte Fahrzeugladegeräte wird für das 3-Φ-bB-AC/DC-Konvertersystem weiters eine Pseudoerdungsregelung vorgeschlagen, welcher die DC/DC-Hochsetzstellestufe derart regelt, dass die seitens der Gleichrichterstufe generierte niederfrequente Gleichtaktspannung kompensiert und dadurch die niederfrequente Gleichtaktspannung zwischen dem Gleichspannungsausgangsmittelpunkt und Schutzerde zu Null wird. Dadurch kann der Mittelpunkt des Gleichspannungsausgangs direkt mit Schutzerde verbunden werden, wobei in diesem Fall eine Erdstromregelung mit Sollwert Null verhindert, dass die vorgeschriebenen FI-Schutzschalter unnötigerweise auslösen. Das vorgeschlagene Konzept wird mithilfe des 10 kW-Demonstratorsystems sowohl für Terra-Terra-(TT)- als auch für Terra-Neutral-(TN)-Erdungssysteme verifiziert. Die Erdstromregelung limitiert den niederfrequenten Gleichtaktleckstrom auf < 6 mA RMS, d.h. auf deutlich unter typischen Auslöseschwellen von FI-Schutzschaltern liegende Werte, zudem wird, unter Verwendung des Körper-Ersatznetzwerkes nach UL 2202, eine verbleibende Erdspannung von 110 mV verifiziert, welche deutlich unter dem strikten Limit von 250 mV der Norm liegt, und somit eine für zukünftige nicht isolierte Fahrzeugladegeräte einsetzbare Lösung präsentiert.

Nebst der vorstehend beschriebenen Topologie mit Stromzwischenkreis, können auf-/abwärts wandelnde 3-Φ-PFC-Gleichrichtersysteme auch mittels einer industriell weit verbreiteten Spannungszwischenkreisschaltungstopologie realisiert werden. Eine Dreilevelrealisierung der Gleichrichterstufe

hat hierbei den Vorteil, dass EMV Filter geringeren Bauvolumens Einsatz finden können, bzw. der Konverter eine höhere Leistungsdichte aufweist, weshalb ein T-typ-(Vienna)-Hochsetzgleichrichter als Eingangsstufe gewählt wird. Um zudem die Tiefsetzfunktion zu etablieren wird diese Konverterstufe mit einem nachgeschalteten DC/DC-Tiefsetzsteller kombiniert, und dieser ebenfalls in Dreilevelstruktur realisiert, um das Volumen der magnetischen Komponenten zu verkleinern und eine Regelung der Spannung des Mittelpunktes des beiden Konvertersystemen gemeinsamen Spannungszwischenkreises zu ermöglichen. Für hohe Ausgangsspannungen werden, um die Ausgangsspannung zu regeln alle drei Phasen der Gleichrichtereingangsstufe getaktet (3/3-PWM), wobei der DC/DC-Tiefsetzsteller geklemmt verbleibt um Schaltverluste zu vermeiden. Bei tiefen Ausgangsspannungen wird die Zwischenkreisspannung vorteilhafterweise durch den DC/DC-Tiefsetzsteller mit Rücksicht auf einen sechspulsigen, durch die Einhüllende der Absolutwerte der Netzsphasenspannungen definierten Verlauf geregelt, bzw. findet 1/3-PWM Einsatz, d.h. es wird jeweils nur eine der drei Phasen der Eingangsstufe getaktet und der Strom in den beiden verbleibenden Phasen indirekt durch den DC/DC-Tiefsetzsteller bzw. die vorstehend erwähnte Formung der Zwischenkreisspannung geregelt und so gegenüber 3/3-PMW eine massive Reduktion der Schaltverluste erreicht. Des Weiteren wird durch ein neuartiges 2/3-PWM-Modulationsschema für jene Fälle, in denen eine Ausgangsspannung des Gesamtsystems zwischen den durch reinen Hochsetz- oder reinen Tiefsetzbetrieb abgedeckten Spannungsbändern eingestellt werden muss garantiert, dass ein Betrieb mit minimalen Verlusten vorliegt, d.h. in jedem Moment nur die minimale Anzahl an Halbbrücken getaktet und die Zwischenkreisspannung auf dem tiefst möglichen Wert gehalten wird. Hervorzuheben ist, dass das vorgeschlagene synergetischen Regelkonzept einen nahtlosen Übergang zwischen den verschiedenen verlustoptimalen Betriebsarten sicherstellt. Eine umfassende experimentelle Verifikation, inklusive EMV Messungen, durchgeführt mithilfe eines Demonstratorsystems mit 10 kW Nennleistung und einer Leistungsdichte von 5.4 $\mathrm{kW/dm^3}$ (91 $\mathrm{W/in^3}$) und einer Effizienz von bis zu 98.8%, bestätigt die theoretische Analyse.

Abschliessend wird bezugnehmend auf die beiden realisierten Demonstratorsysteme ein umfassender Vergleich der Hardwarerealisierungen, der synergetischen Regelungen, der Hardwareimplementierungen, der Effizienzcharakteristiken und der leitungsgebundenen EMV Störaussendungen dreiphasiger Tief-Hochsetz-Stromzwischenkreis- und Hoch-Tiefsetz-Spannungszwischenkreis-PFC-AC/DC-Konvertersysteme gegeben. Die Arbeit

schliesst mit einer Zusammenfassung der wichtigsten Forschungsergebnisse und einer Diskussion zukünftiger Forschungsbereiche.

Abbreviations

1/3-PWM	One-Third Pulse-Width Modulation
2/3-PWM	Two-Third Pulse-Width Modulation
2-L	Two-Level
3/3-PWM	Three-Third Pulse-Width Modulation
3-L	Three-Level
3-Φ	Three-Phase
AC	Alternating Current
bB	buck-Boost
Bb	Boost-buck
BEV	Battery Electric Vehicle
CC	Constant Current
CCS	Combined Charging System
CM	Common-Mode
CSR	Current Source Rectifier
CV	Constant Voltage
DAB	Dual Active Bridge
DC	Direct Current
DM	Differential-Mode
EMI	Electromagnetic Interference
EV	Electric Vehicle
FET	Field-Effect Transistor
GaN	Gallium Nitride
GCC	Ground Current Control
GFCI	Ground Fault Circuit Interrupter
GND	Ground
HB	Half-Bridge
HF	High-Frequency
HTS	High-Temperature Superconducting
HV	High-Voltage
IEA	International Energy Agency
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
LF	Low-Frequency
M-BDS	Monolithic Bidirectional Switch
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NPC	Neutral Point Clamped
OBC	On-Board Charger

PCB	Printed Circuit Board
PE	Protective Earth
PFC	Power Factor Correction
PHEV	Plug-In Hybrid Electric Vehicle
PI	Proportional-Integral
PV	Photovoltaic
PWM	Pulse-Width Modulation
RCD	Residual Current Device
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SoC	State of Charge
STEPS	Stated Policies Scenario
SVPWM	Space Vector Pulse-Width Modulation
TN	Terra-Neutral
TT	Terra-Terra
UL	Underwriters Laboratories
VGC	Virtual Grounding Control
VSR	Voltage Source Rectifier

Contents

1 Introduction

Transportation of passengers and freight currently accounts for approximately 25% of world energy use [1] and generates 25% of all CO_2 emissions [2]. Given a more efficient conversion technology and, at the same time, enabling the use of renewable energy, electrified transportation is believed as one of the most promising measures to reduce fossil fuel consumption significantly and support the net-zero CO_2 emission target set forth in the Paris Agreement before 2050 [3]. Furthermore, electric vehicles (EVs) are the single most important technology for decarbonizing the transport sector since EVs are more and more powered by renewable energy and much more efficient at converting energy into propulsion than gasoline and diesel vehicles.

According to International Energy Agency (IEA), **Fig. 1.1** shows historical global EV data with projections to 2030 on numbers of EV sales, public charging points, and electricity demand consumed by the EV fleet. Obvious prosperities have been already observed before 2021 and exponential increases are expected until 2030, e.g., more than 270 million EVs will be sold, 13 million public EV charging points will be installed, and electricity consumption is supposed to be 430 000 GWh/year in 2030 by EVs.

EVs have been popular on the street since the 1900s. **Fig. 1.2** depicts an old-fashioned electric brougham, which was driven by two four-pole electric motors (rated at two horsepower) allowing reverse rotating capability. The battery pack, consisting of 48 cells of chloride accumulators, was placed beneath the driver's seat [6]. Interestingly, a similar drivetrain structure is being implemented on modern EVs even though more than a hundred years have passed. **Fig. 1.3** shows a drivetrain system of the Audi RS e-tron GT with a battery voltage of 800 V and an on-board charger (OBC) allowing 11 kW AC charging. If using fast DC charging, a charging power of up to 270 kW can charge the battery from 5% to 80% SoC (state of charge) within 25 minutes [7].

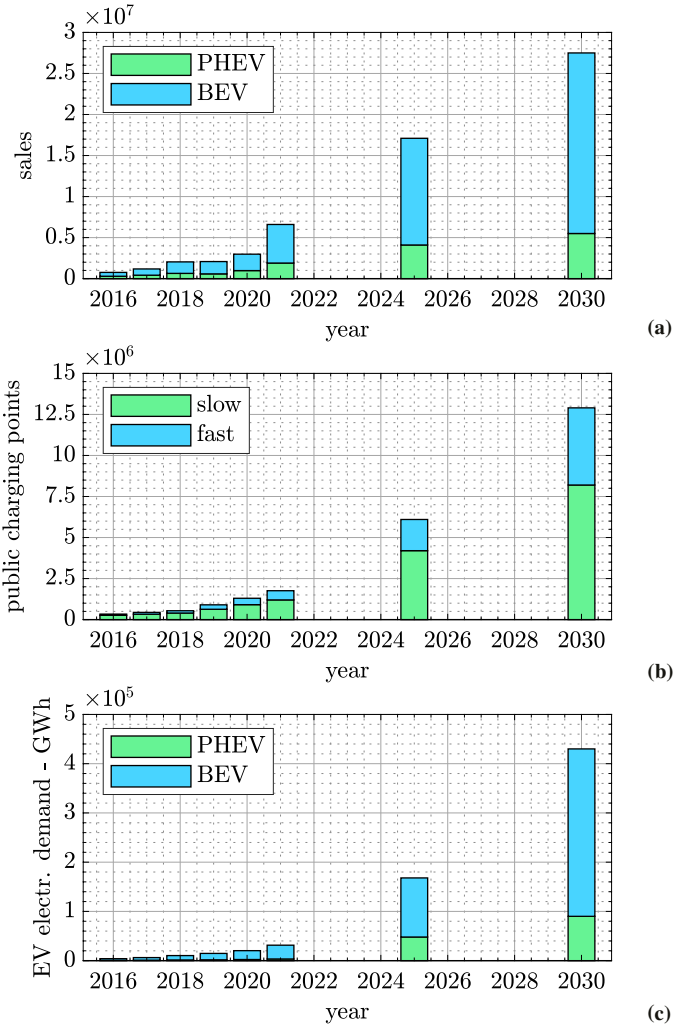

Fig. 1.1: Historical global EV data with projections to 2030 on numbers of **(a)** EV sales, **(b)** public charging points, and **(c)** electricity demand consumed by the EV fleet [4]. Note that EVs include battery electric vehicles (BEVs) and plug-in hybrid electric vehicles (PHEVs). Also, note that the Stated Policies Scenario (STEPS) projection model, proving a more conservative benchmark for the future, is applied in this analysis [5].

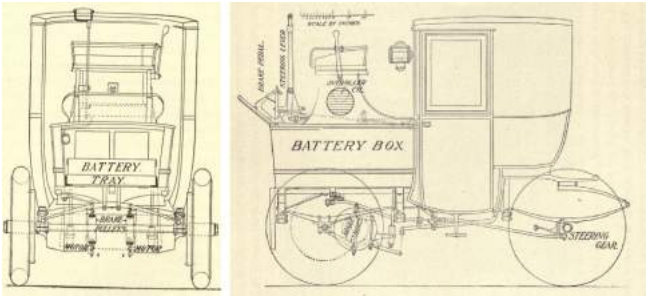

Fig. 1.2: Electric brougham, i.e., also called *horseless vehicle*, was extensively used around the 1900s [6].

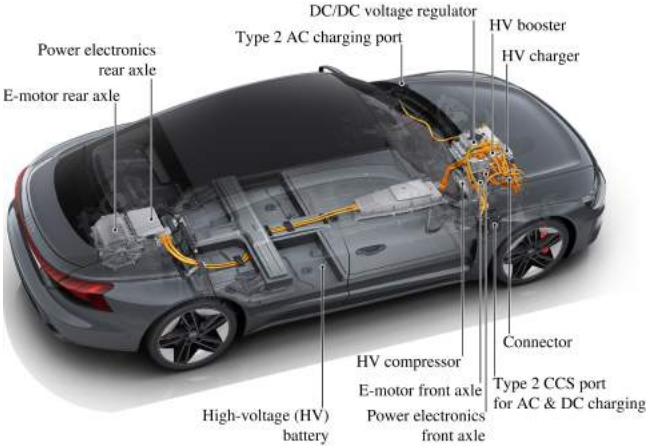

Fig. 1.3: 800 V drivetrain system of Audi RS e-tron GT [7].

To facilitate the transition from fossil-fuel-based to carbon-free road transportation by EVs, more efficient and compact EV battery chargers are key enablers to overcome range anxiety and further reduce the costs of EVs. The EV chargers are typically realized as multi-stage solutions where PFC AC/DC converter systems are always needed to convert the AC mains voltage into a DC output charging the EV batteries [8]. Furthermore, a wide charging voltage range (typically from 200 V up to 1000 V, as shown in **Fig. 1.4**) requires buck-boost functionality, which is provided by such converter systems. State-of-the-art isolated EV chargers are additionally employing a series resonant

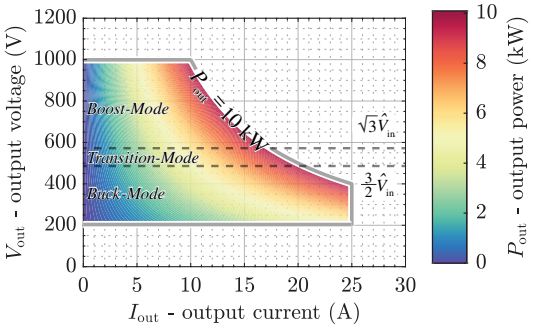

Fig. 1.4: Typical operating range of a 10 kW EV charger module [12]; note the output current limit of $I_{out} = 25$ A.

converter with limited voltage controllability but high efficiency for isolating the output voltage; in the future, the isolation stage could be omitted, i.e., the buck-boost AC/DC converter systems directly used as non-isolated EV charging systems [9]. In this regard, a synergetically-controlled 3-Φ current DC-link buck-boost (bB) PFC AC/DC converter system featuring ultra-flat efficiency characteristics over a wide operating range is first studied and analyzed in this thesis. Furthermore, the proposed synergetic control strategy is extended to regulate two independent DC outputs for future high-voltage batteries of heavy-duty electric vehicles [10], which could advantageously be split into upper and lower halves [11]. Then, new virtual grounding control (VGC) and ground current control (GCC) schemes are proposed to avoid nuisance tripping of residual current devices (RCDs) and to ensure the resilient operation of future non-isolated EV chargers. Finally, a synergetically-controlled 3-Φ voltage DC-link boost-buck (Bb) PFC AC/DC converter system, from the category of widely-analyzed voltage DC-link topologies, is investigated and comprehensively compared with the 3-Φ current DC-link bB PFC AC/DC converter system.

Section 1.1 provides a brief overview of EV charger developments, where several main structures of EV battery chargers are summarized, including isolated and non-isolated EV charging structures. **Section 1.2** introduces several buck-boost AC/DC converter topologies with voltage or current DC-links and the two most promising 3-Φ buck-boost AC/DC converter systems are selected regarding simplicity and high performance as subjects of this thesis. **Section 1.3** presents the main contributions of this thesis and all

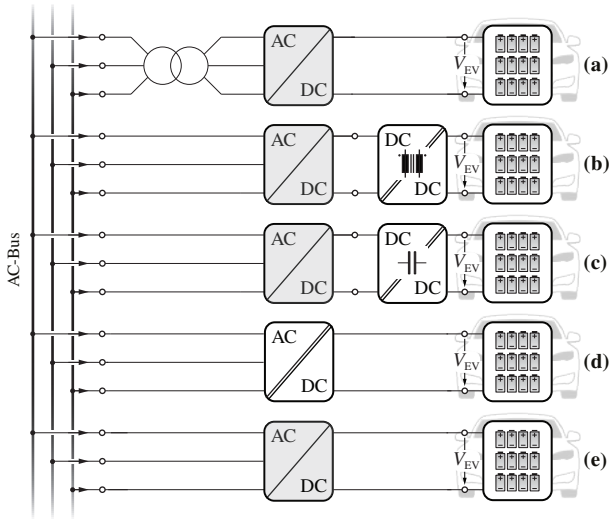

Fig. 1.5: Structures of typical isolated or future non-isolated EV battery chargers. The multi-stage structure is the dominant solution where the galvanic isolation functionality can be provided by a dedicated transformer or converter stage, i.e., **(a)** a low-frequency (LF) transformer, **(b)** a high-frequency (HF) DC/DC converter featuring inductive isolation, **(c)** an HF DC/DC converter featuring capacitive isolation. **(d)** The isolation functionality can also be integrated into the PFC rectifier stage to achieve a single-stage isolated AC/DC converter. **(e)** Non-isolated charger concepts facilitating more compact and more efficient realizations of future EV chargers are analyzed in this thesis.

related publications are listed in **Section 1.4**. **Section 1.5** outlines the content of each chapter.

1.1 Electric Vehicle (EV) Charger Development

Typical structures of isolated or future non-isolated EV chargers (see **Fig. 1.5**) are summarized in this section. The galvanically isolated solutions are presently dominant since a high common-mode (CM) impedance provided by either inductive or capacitive isolation is realized between the grid and the vehicle to ensure electrical safety passively [9, 13, 14].

The galvanic isolation can be achieved by a low-frequency (LF), i.e., mains frequency transformer (see **Fig. 1.5a**), but LF transformers are intrinsically

penalized by large volumes [15]. Thus, advantageously operating the transformer at an increased frequency can achieve high efficiency and reduce system volume, as shown in **Fig. 1.5b**, where an additional high-frequency (HF) transformer-based isolated DC/DC converter is applied. Such an isolated converter stage can be implemented as a dual active bridge (DAB) converter [16–19], an LLC resonant converter [20–22], or a series resonant DC/DC converter, i.e., DC transformer (DCX, [23, 24]). Even though, in this case, the required ultra-wide output voltage regulation capability can be provided by both the DC/DC converters and the 3-Φ PFC rectifier front-ends, loss-optimal operating modes of the whole system are very hard to be specified since collaborative operations of the two converters (DC/DC and PFC rectifier stages) with varying voltage gains are fairly complex. Thus, optimal EV charger designs of the cascaded system have to take the front-end and the isolation-stage into account at the same time instead of optimizing them separately. To avoid such complicated design and control issues, DCXs are preferably selected as standard isolated building blocks with a near-unity voltage conversion ratio [25]. Thus, the 3-Φ AC/DC converter system must cover a correspondingly wide output voltage range and/or the PFC rectifier front-end must incorporate buck-boost capability.

Even though HF transformers can successfully reduce losses and required volume compared to conventional LF transformers, such main magnetic components are still typical obstacles to future EV chargers with even higher efficiencies and power densities. Thus, research on capacitive coupling (see **Fig. 1.5c**), as a dual coupling type of inductive transformers, has been carried out where power is transferred between two isolated metal barriers [26–30]. Either series resonant [29] or switched capacitor [27] topologies can be implemented to realize the capacitive galvanic isolation with fairly small magnetic components resulting in compact isolation realizations. However, only very limited voltage regulation capabilities can be obtained by the capacitive galvanic isolation stage, therefore, the 3-Φ AC/DC converter needs, again, to provide the full buck-boost capability.

Furthermore, the buck-boost functionality and the galvanic isolation capability can also be realized by one single converter stage as shown in **Fig. 1.5d**, e.g., 3-Φ matrix-type DAB converter [31] or 3-Φ isolated phase-modular converter [32]. However, single-stage isolated PFC rectifiers need very complicated control/modulation strategies to cover the required ultra-wide output voltage range and high-efficiency operation over such a wide range can hardly be guaranteed.

Providing galvanic isolation always means placing an additional element, i.e., an LF transformer or an isolated DC/DC converter, in the power flow path and consequently leads to more bulky and more complex systems with increased power losses and costs. To roughly quantify these drawbacks, consider photovoltaic (PV) inverter systems: compared to traditional solutions that include galvanic isolation, their transformerless counterparts feature an efficiency improvement of 1 % to 2 % and about twice the power density [33,34]. Thus, non-isolated converter structures become attractive solutions for future EV chargers allowing compact, highly efficient, and low-cost realizations as shown in **Fig. 1.5e**. Without galvanic isolation, reliable protection against electrical hazards can only be provided by residual current devices (RCDs)[1] installed at the grid interface, which is mandatory according to standards (e.g., IEC 61851, UL 2202) [9]. Furthermore, to achieve compatibility with the wide range of EV battery voltages, non-isolated EV chargers, i.e., 3-Φ AC/DC converter systems, must provide buck-boost functionality.

All in all, except for the single-stage isolated EV charger solution (see **Fig. 1.5d**), 3-Φ AC/DC converter systems covering an ultra-wide output voltage range, e.g., from 200 V up to 1000 V, serve as a standard building block for various kinds of EV charging structures. Most importantly, they can be adapted as future non-isolated EV chargers and used to build chargers of even higher power levels with reduced costs and improved efficiencies.

1.2 3-Φ Buck-Boost AC/DC Converter Systems

3-Φ buck-boost AC/DC converter systems are introduced in this section. Generally speaking, 3-Φ AC/DC converter systems, either with or without the buck-boost functionality, can be categorized into two main types, widely-used voltage DC-link (voltage source) systems, and less-frequently employed current DC-link (current source) systems. Thus, two promising topologies, i.e., 3-Φ buck-boost (bB) current DC-link PFC AC/DC converter system (see **Fig. 1.6b**) and 3-Φ boost-buck (Bb) voltage DC-link PFC AC/DC converter system (see **Fig. 1.6d**), are selected from the two categories as main subjects for a detailed analysis and performance comparison between two topologies over an ultra-wide output voltage range is conducted in this thesis.

[1] Another common name is "ground fault circuit interrupter" (GFCI).

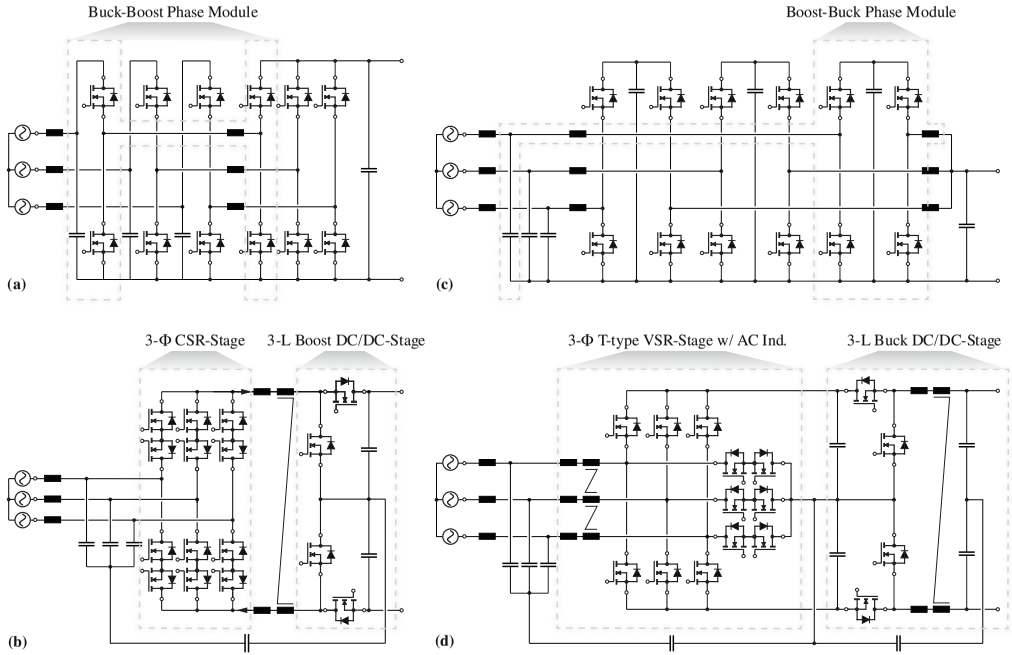

Fig. 1.6: Typical topologies of buck-boost and/or boost-buck 3-Φ PFC AC/DC converter systems, which are commonly grouped into two categories, i.e., **(a)** and **(b)** current DC-link (current source) systems, and **(c)** and **(d)** voltage DC-link (voltage source) systems. The **(b)** 3-Φ bB current DC-link PFC AC/DC converter system and **(d)** 3-Φ Bb voltage DC-link PFC AC/DC converter system are the main subjects of this thesis with integrated CM filters for full functionality, i.e., partial EMI filtering. Two benchmark topologies, i.e., **(a)** 3-Φ bB phase-modular PFC Y-rectifier and **(c)** 3-Φ Bb phase-modular PFC rectifier, are also shown.

1.2.1 3-Φ Buck-Boost (bB) Current DC-Link System

Fig. 1.6a shows a 3-Φ bB phase-modular PFC Y-rectifier composed of three identical bB DC/DC-stages [35, 36]. The converter belongs to the current DC-link category as the 3-Φ mains currents are generated by pulse-width modulation based on the currents of the phase inductors (for buck-type operation). The phase-modular structure allows an easy rearrangement of the converter structure for single-phase operation to deliver full output power. However, the 3-Φ bB phase-modular Y-rectifier is penalized by an increased number of main inductors, i.e., three inductors instead of only one inductor in a conventional 3-Φ current DC-link PFC rectifier. Furthermore, the transistors of the DC-side half-bridges (HBs) have to block and switch the full output voltage so that operating at a very high output voltage is problematic in terms of significant hard-switching losses and larger HF voltage-time areas across the three phase inductors requiring relatively large inductance values for limiting the current ripples.

Therefore, instead of the phase-modular structure, a 3-Φ bB current DC-link PFC AC/DC converter system (see **Fig. 1.6b**), formed by a 3-Φ buck-type current source rectifier (CSR)-stage and a subsequent 3-L boost-type DC/DC-stage, is selected. The 3-Φ bB current DC-link PFC AC/DC converter system shows an increased complexity in the CSR front-end since each HB of the CSR-stage requires two inverse-series connected power semiconductors to provide the bidirectional blocking capability. However, its output DC/DC boost-stage is simpler and more straightforward compared to the 3-Φ bB phase-modular Y-rectifier. Only four transistors are needed in the 3-Φ bB current DC-link PFC AC/DC converter system output stage but twelve transistors would be needed for the Y-rectifier to achieve a 3-L characteristic of the bridge-legs connected to the DC output.

1.2.2 3-Φ Boost-Buck (Bb) Voltage DC-Link System

Fig. 1.6c presents a 3-Φ Bb phase-modular PFC rectifier employing three independently regulated boost-buck converter stages (modules) [36, 37]. Each converter module generates an AC input voltage for controlling the current in the input inductor and/or related grid phase current by pulse-width modulating the corresponding phase DC-link voltage (for boost-type operation), and thus, this system is of voltage source type. Similar to the aforementioned dual current DC-link system, the phase modular topology allows a convenient converter rearrangement for single-phase supply. However, the 3-Φ Bb phase-modular PFC rectifier is impaired by an increased number of DC-side buck

inductors, i.e., three inductors instead of only one inductor in a conventional 3-Φ voltage DC-link PFC AC/DC converter system. Moreover, each transistor needs to block and switch the full related DC-link voltage, leading to increased semiconductor costs and reduced power conversion efficiency. Furthermore, extending the 2-L structure shown in **Fig. 1.6c** into a 3-L realization (input and output stage) would result in 24 required power transistors.

A 3-L realization of a 3-Φ PFC rectifier stage facilitates small EMI filters and hence compact converter realizations [38, 39]. In particular, the T-type (Vienna) voltage source PFC rectifier (VSR)-stage [40, 41] is a widely used industry-standard solution [42–44]. Thus, a 3-Φ Bb voltage DC-link PFC AC/DC converter system (see **Fig. 1.6d**) is considered to achieve boost-buck functionality, where the boost-type VSR-stage is combined with a buck-type DC/DC-stage (e.g., [45, 46]), which again advantageously is realized as a 3-L structure to reduce the magnetics volume and to enable controllability of the VSR-stage DC-link midpoint potential. Therefore, this system (see **Fig. 1.6d**) is selected in the voltage DC-link category and analyzed in detail in this thesis.

Compared to conventional Bb voltage DC-link systems (e.g., **Fig. 1.6d**), bB current DC-link systems (e.g., **Fig. 1.6b**) offer several advantages:

- Only one shared main DC-link inductor connecting the CSR-stage and the DC/DC-stage is needed in bB current DC-link systems instead of three boost AC-side inductors and, at least, one DC-side inductor, which leads to a compact converter realization with reduced manufacturing costs.

- Furthermore, since only one main DC-link inductor current has to be regulated in bB current DC-link systems, synergetic control implementation is more straightforward, and the 3-Φ mains currents and the DC output current can be generated in an open-loop manner [47]. In contrast, the 3-Φ mains currents and the DC output current in Bb voltage DC-link systems have to be measured and regulated to ensure a sufficient control bandwidth. Accordingly, a significantly more complex synergetic control structure and/or an increased number of current sensors is required.

- EMI noise emissions of current source PFC rectifiers are dependent on the DC-link current (proportional to the output power) instead of the DC-link voltage (equal to the output voltage in boost-mode) as in voltage source PFC rectifiers. Thus, less additional EMI noise filtering efforts are required when operating current source rectifiers at high DC

output voltages (in contrast to voltage source rectifiers), i.e., especially for charging of future heavy-duty EVs with the battery voltage up to 1500 V [10].

Furthermore, upcoming monolithic bidirectional switches (M-BDSs), which can overcome the factor-of-four penalty in chip area usage of a conventional discrete realization, will significantly decrease the implementation complexity of the 3-Φ current DC-link PFC rectifier front-end stages since two inverse-series connected transistors can be substituted by only one device with a single drift region for blocking both voltage polarities [48].

1.3 Main Contributions

As outlined above, 3-Φ bB PFC AC/DC converter systems are fundamental building blocks for conventional isolated and future non-isolated EV battery chargers. Thus, this thesis focuses on two advanced 3-Φ buck-boost PFC AC/DC converter systems employing either a current DC-link or a voltage DC-link, and their loss-optimal synergetic control over an ultra-wide output voltage range, i.e., from 200 V up to maximum 1000 V. Furthermore, regarding the selected 3-Φ bB current DC-link PFC AC/DC converter system (see **Fig. 1.6b**), the synergetic control strategy is extended to regulate two independent DC outputs for applications with voltage asymmetries and/or load asymmetries. Moreover, a novel virtual grounding control (VGC) and a ground current control (GCC) are proposed to enable future non-isolated EV chargers, where the ground current is measured and closed-loop controlled to avoid the nuisance tripping of RCDs and to ensure end-user safety. Finally, the proposed synergetic control strategy, operating efficiency, and EMI performance of the 3-Φ bB current DC-link and the 3-Φ Bb voltage DC-link PFC AC/DC converter systems are verified and comparatively evaluated.

1.3.1 Scientific Contributions

The following points, which so far have not been studied in the literature, are carefully analyzed in this thesis:

- ***Advanced PWM Schemes Enabling Optimal Clamping*** – Conventional space vector pulse-width modulation (SVPWM) schemes are typically utilized for generating the required 3-Φ sinusoidal quantities, either 3-Φ PWM voltages or currents, by modulating a *constant* DC-link voltage in voltage source converters or a *constant* DC-link current in

current source converters. Accordingly, the degrees of freedom associated with a time-varying DC-link voltage/current have typically been disregarded. In this thesis, advanced PWM schemes that enable time-varying DC-link voltage/current are comprehensively reviewed. These include 2/3-PWM operation for current source topologies, as well as 1/3-PWM operation and a proposed 2/3-PWM scheme for voltage source topologies. The focus is on enhancing efficiencies and reducing conducted EMI noise emissions.

- ***Synergetic Control / Loss-Optimal Buck-Boost Operation*** – The ultra-wide output voltage range from 200 V up to 1000 V, requiring buck-boost functionality, is necessary for EV charger applications. Therefore, the analyzed 3-Φ buck-boost PFC AC/DC converter systems need to operate in different modes, such as buck-mode (step-down), boost-mode (step-up), and transition-mode in between buck and boost operation. However, a comprehensive analysis and experimental verification of the loss-optimal operations of the two selected 3-Φ buck-boost current/voltage DC-link PFC AC/DC converter systems under such a wide output voltage range is still missing. This thesis derives loss-optimal operation modes that minimize semiconductor losses for any output voltage level by ensuring the minimum possible DC-link voltage/current and the minimum number of switching actions. Synergetic control strategies are then proposed to achieve democratic/automatic decisions concerning the switching action of the converter stages and a seamless transition between these loss-optimal operating modes, with thorough experimental verifications.

- ***Independent Output Voltage Control for Heavy-Duty EVs*** – To address voltage and load asymmetries occurring in specific applications, such as heavy-duty EVs and high-power heaters, an extended synergetic control strategy is proposed in this thesis. This approach utilizes the 3-Φ bB current DC-link PFC AC/DC converter system (illustrated in **Fig. 1.6b**) to fully leverage the hardware capacity and supply two independent loads. The proposed extended synergetic control strategy maintains the aforementioned loss-optimal operation, which reduces the number of switching instants by clamping a phase of the CSR-stage (employing only two out of the three phases, i.e., 2/3-PWM, for input current shaping), or by individually clamping the two half-bridges of the DC/DC-stage while minimizing the DC-link current, for any operating point.

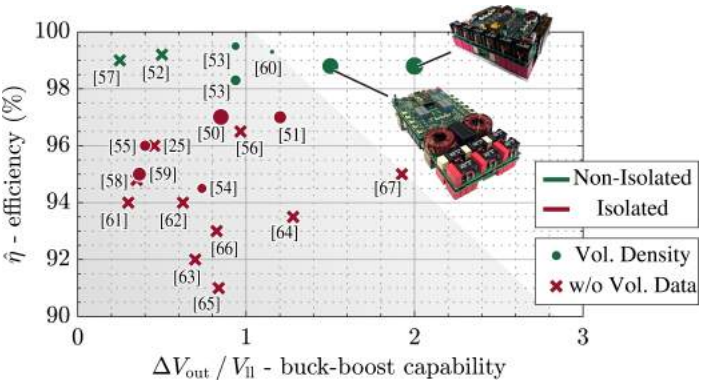

Fig. 1.7: Overview of 3-Φ EV charger prototypes and products reported in the literature in the coordinate system of peak efficiency $\hat{\eta}$ and buck-boost capability ΔV_{out} / V_{ll}, where $\Delta V_{out} = V_{out,max} - V_{out,min}$ and V_{ll} denominates the RMS value of the grid line-to-line voltage. The two EV chargers built in this thesis are highlighted. University demonstrators: [25, 50–60]. Industry products: [61–67]. The volumetric power density values are indicated by according symbol sizes.

- ***VGC and GCC for Non-Isolated EV Chargers*** – Many EV chargers on the market incorporate LF or HF galvanic isolation stages to ensure electric safety, but this comes at a cost of increased losses, system complexity, and reduced power density. As a result, non-isolated EV chargers are becoming more attractive as they rely on RCDs to protect users from electric shocks. However, the challenge with non-isolated EV chargers is the risk of RCD nuisance tripping. In this thesis, two control strategies, VGC and GCC, are proposed to address this issue. These methods involve measuring and controlling the ground current to limit the LF CM leakage current to less than 6 mA RMS, which is well below typical RCD trip levels. Using the human-body impedance model specified in UL 2202 [49], the proposed method achieves a test voltage of only 110 mV, which is significantly below the most stringent limit of 250 mV in the standard. The new concepts are successfully verified using a 10 kW hardware demonstrator.

1.3.2 Demonstrator Systems and Performance Benchmark

As shown in **Fig. 1.7**, the peak efficiencies of most isolated EV chargers described in the literature are below 97 %, while non-isolated solutions can achieve operating efficiencies above 98 %. Similar performance improvements have already been demonstrated for PV inverter systems: compared to traditional solutions that include galvanic isolation, their transformerless counterparts feature an efficiency improvement of 1 % to 2 % and about twice the power density [33, 34].

The achieved performance of both hardware demonstrators realized in the course of this thesis is significantly beyond the state-of-the-art in terms of efficiency, power density, and buck-boost capability. The built 3-Φ bB current DC-link PFC AC/DC converter system (see **Fig. 1.8a**) can cover an ultra-wide output voltage range from 200 V up to 1000 V, i.e., buck-boost capability $\Delta V_{\text{out}} \,/\, V_{\text{ll}} = (V_{\text{out,max}} - V_{\text{out,min}}) \,/\, V_{\text{ll}} = 2$, with a peak efficiency of 98.8 % and a volumetric power density of 6.4 kW/dm^3 (107.5 W/in^3). The realized 3-Φ Bb voltage DC-link PFC AC/DC converter system (see **Fig. 1.8b**) can cover a very wide output range from 200 V up to 800 V, i.e., provides a buck-boost capability of $\Delta V_{\text{out}} \,/\, V_{\text{ll}} = 1.5$, with a peak efficiency of 98.8 % and a volumetric power density of 5.4 kW/dm^3 (90.9 W/in^3).

1.4 List of Publications

Key insights presented in this thesis have already been published or will be published in international patents, international scientific journals, conference proceedings, or presented at workshops. The publications created as part of this thesis, or also in the scope of other related projects, are listed below.

1.4.1 Patents

[P.4] **D. Zhang**, J. Huber, and J. W. Kolar, "Virtual Grounding Control and Ground Current Control of Non-Isolated EV Chargers," Patent Application, 2023 (Under Review).

[P.3] **D. Zhang**, J. Huber, J. W. Kolar, and N. Nain, "Method for Operating a Current Source Converter, Control Circuit, and Current Source Converter," U.S. Patent, 179/67 588, 2023.

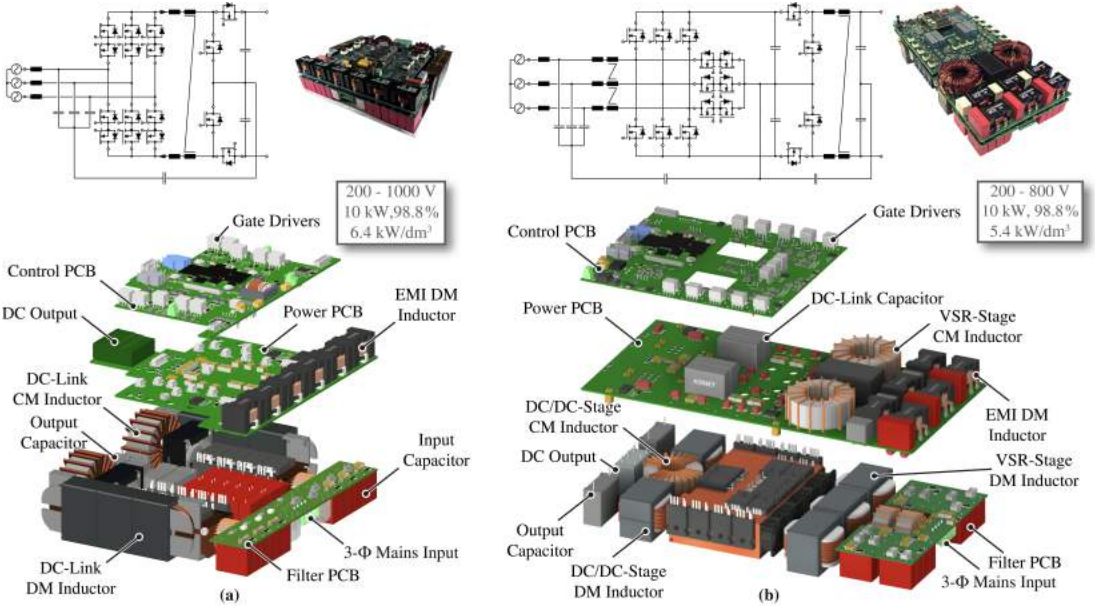

Fig. 1.8: Circuit schematics, exploded views, and photos of the realized 10 kW hardware demonstrators, i.e., **(a)** a 3-Φ bB current DC-link and **(b)** a 3-Φ Bb voltage DC-link PFC AC/DC converter system.

[P.2] **D. Zhang**, J. Huber, J. W. Kolar, and J. Everts, "Electrical Converter with Overvoltage Protection Circuit ," International Patent, WO2022243423A1, 2022.

[P.1] **D. Zhang**, M. Guacci, J. W. Kolar, and J. Everts, "Electrical Power Converter," International Patent, WO2021219761A1, 2021.

1.4.2 Journal Papers

[J.5] **D. Zhang**, J. Huber, and J. W. Kolar, "A Three-Phase Synergetically Controlled Buck-Boost Current DC-Link EV Charger," IEEE Trans. Power Electron. (Early Access).

[J.4] **D. Zhang**, C. Leontaris, J. Huber, and J. W. Kolar, "Optimal Synergetic Control of High-Efficiency Three-Phase/Level Boost-Buck Voltage DC-Link Very Wide Output Voltage Range EV Charger," IEEE J. Emerg. Sel. Topics Power Electron. (Early Access).

[J.3] **D. Zhang**, D. Cao, J. Huber, J. Everts, J. W. Kolar, "Non-Isolated Three-Phase Current DC-Link Buck-Boost EV Charger with Virtual Output Midpoint Grounding and Ground Current Control," IEEE Trans. Transp. Electrific. (Early Access).

[J.2] **D. Zhang**, D. Cittanti, P. Sun, J. Huber, R. Bojoi, and J. W. Kolar, "Detailed Modeling and In-Situ Calorimetric Verification of Three-Phase Sparse NPC Converter Power Semiconductor Losses," IEEE J. Emerg. Sel. Topics Power Electron, Vol. 11, No. 3, pp. 3409-3423, June 2023.

[J.1] **D. Zhang**, D. Cao, J. Huber, and J. W. Kolar, "Three-Phase Synergetically Controlled Current DC-Link AC/DC Buck-Boost Converter with Two Independently Regulated DC Outputs," IEEE Trans. Power Electron., Vol. 38, No. 4, pp. 4195-4202, April 2023.

Moreover, part of the research activity of the author supported, which is reflected in the co-authorship of the following publications:

[J] P. Czyz, T. Guillod, **D. Zhang**, F. Krismer, R. Färber, J. Huber, C. M. Franck, and J. W. Kolar, "Analysis of the Performance Limits of 166 kW / 7 kV Air-Core and Magnetic-Core Medium-Voltage Medium-Frequency Transformers for 1:1-DCX Applications," IEEE J. Emerg. Sel. Topics Power Electron., Vol. 10, No. 3, pp. 2989-3012, June 2022.

[J] M. Guacci, **D. Zhang**, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Three-Phase Two-Third-PWM Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," CPSS Trans. Power Electron. Appl., Vol. 4, No. 4, pp. 339-354, December 2019.

1.4.3 Conference Papers

[C.4] **D. Zhang**, D. Cao, J. Huber, and J. W. Kolar, "Advanced Synergetic Charge Control of Three-Phase PFC Buck-Boost Current DC-Link EV Chargers," Proc. IEEE Workshop Control Modeling Power Electron. (COMPEL), Tel Aviv, Israel, June 20-23, 2022.

[C.3] **D. Zhang**, M. Guacci, J. W. Kolar, and J. Everts, "Synergetic Control of a Three-Phase Buck-Boost Current DC-Link Bidirectional EV Battery Charger Considering Wide Output Range and Irregular Mains Conditions," Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia), Nanjing, China, November 29-December 2, 2020.

[C.2] **D. Zhang**, M. Guacci, J. W. Kolar, and J. Everts, "Three-Phase Bidirectional Ultra-Wide Output Voltage Range Current DC-Link AC/DC Buck-Boost Converter," Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON), Singapore, October 18-21, 2020.

[C.1] **D. Zhang**, M. Guacci, M. Haider, D. Bortis, J. W. Kolar, and J. Everts, "Three-Phase Bidirectional Buck-Boost Current DC-Link EV Battery Charger Featuring a Wide Output Voltage Range of 200 to 1000 V," Proc. IEEE Energy Conversion Congr. Expo. (ECCE USA), Detroit, MI, USA, October 11-15, 2020.

Moreover, part of the research activity of the author supported, which is reflected in the co-authorship of the following publications:

[C] D. Cao, **D. Zhang**, J. W. Kolar, J. Huber, "Conceptualization of a Cryogenic 250-A Power Supply for High-Temperature-Superconducting (HTS) Magnets of Future Particle Accelerators," Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia), Jeju, Korea, May 22-25, 2023.

[C] N. Nain, **D. Zhang**, J. Huber, J. W. Kolar, K. Leong, and B. Pandya, "Synergetic Control of Three-Phase AC-AC Current-Source Converter

Employing Monolithic Bidirectional 600 V GaN Transistors," Proc. IEEE Workshop Control Modeling Power Electron. (COMPEL), Bogotá, Colombia, November 2-5, 2021. – ***Best Paper Award***

1.4.4 Keynotes and Tutorials

[W.5] **D. Zhang**, and J. W. Kolar, "Synergetic Control of Non-Isolated Three-Phase Voltage & Current DC-Link EV Chargers," IEEE Power Electronics Society USU (Utah State University, USA) Chapter Events 2023, Online presentation, July 17, 2023.

[W.4] J. W. Kolar, J. Huber, D. Menzi, and **D. Zhang**, "Next Generation SiC GaN 3-Φ PFC Rectifier / PWM Inverter Systems," Tutorial at IEEE Southern Power Electron. Conf. (SPEC), Fiji, December 5-8, 2022.

[W.3] J. W. Kolar, J. Huber, and **D. Zhang**, "Monolithic Bi-Directional Switches - Opening New Horizons in Power Electronics," Keynote Presentation at IEEE Int. Power Electron. Appl. Conf. (PEAC), Xiamen, China, November 4-7, 2022.

[W.2] J. W. Kolar, J. Huber, and **D. Zhang**, "Monolithic Bi-Directional Switches - Opening New Horizons in Power Electronics," Plenary Talk at Int. Conf. Silicon Carbide Related Materials (ICSCRM), Davos, Switzerland, September 11-16, 2022.

[W.1] J. W. Kolar, J. Huber, **D. Zhang**, and N. Nain, "Emerging Bidirectional Switches and Their Impact on Future AC Power Converter Applications," Tutorial at IEEE Energy Conversion Congr. Expo. (ECCE USA), Vancouver, Canada, October 10-14, 2021.

1.4.5 Supervised Projects and Theses

[M.8] M. Akbas, "Design and Realization of High-Efficiency Low-Voltage and High-Current Cryogenic Power Supply Unit for HTS Magnet Systems," ETH Zurich, 2023, Master Thesis LEM2310. Supervision: **D. Zhang**.

[M.7] J. Kaufmann, "Design and Realization of Three-Phase Boost-Buck Voltage DC-Link Non-Isolated EV Charger," ETH Zurich, 2023, Master Thesis LEM2311. Supervision: **D. Zhang**.

[M.6] A. Schneider, "Realization of Cryogenic Test Setup and Components Characterization under Cryogenic Conditions," ETH Zurich, 2023, Bachelor Thesis LEM2312. Supervision: **D. Zhang**.

[M.5] D. Cao, "Modeling and Control of Three-Phase Buck-Boost Current DC-Link Converter," ETH Zurich, 2021, Master Thesis LEM2142. Supervision: **D. Zhang**.

[M.4] C. Leontaris, "Design and Realization of a 10 kW Three-Level Three-Phase Boost-Buck Rectifier for EV Charging Applications," ETH Zurich, 2021, Master Thesis LEM2124. Supervision: **D. Zhang**.

[M.3] P. Sun, "Design and Realization of a Three-Phase Sparse Neutral Point Clamped Converter," ETH Zurich, 2021, Master Thesis LEM2102. Supervision: **D. Zhang**, Davide Cittanti.

[M.2] D. Cao, "Modulation Scheme Evaluation of Three-Phase Buck-Boost Current DC-Link EV Battery Charger," ETH Zurich, 2020, Semester Project LEM2036. Supervision: **D. Zhang**.

[M.1] S. Leuch, "DM/CM Inductor Design for Three-Phase Bidirectional Buck-Boost Current DC-Link EV Battery Charger," ETH Zurich, 2020, Semester Project LEM2009. Supervision: **D. Zhang**.

1.5 Thesis Outline

According to the goals and contributions mentioned above, the content of the thesis is divided into six main chapters and conclusions. All the chapters can be read independently since the interdependencies have been reduced to a strict minimum.

- **Chapter 2** presents a comprehensive analysis of the advanced 2/3-PWM concept for current DC-link systems, comparing it with the conventional 3/3-PWM scheme. Additionally, a straightforward synergetic control concept of 3-Φ bB current DC-link PFC AC/DC converter system is introduced to cover the loss-optimal operating modes in a wide output voltage range (200 V to 1000 V). For the first time, a complete experimental verification of loss-optimal synergetic operation ensured by the proposed synergetic control is provided, quantifying the loss savings achieved by 2/3-PWM. The results show a flat efficiency characteristic, with efficiencies higher than 98 % for most operating points with output voltages above 400 V and more than 25 % of rated load.

- **Chapter 3** extends the synergetic control strategy of the 3-Φ bB current DC-link PFC AC/DC converter system introduced in **Chapter 2** to provide two independently regulated DC outputs and advantageously retain loss-optimum operation, i.e., reduced number of switching instants due to clamping of a phase of the CSR-stage (switching only two out of the three phases, i.e., 2/3-PWM) or individual clamping of the DC/DC-stage's two half-bridges, and minimum possible DC-link current, for any operating point, especially for two *different* output voltages and/or two *different* loads connected to the two outputs.

- **Chapter 4** proposes VGC and GCC techniques to effectively address the nuisance tripping problem of RCDs in future *non-isolated* EV chargers based on the analyzed 3-Φ bB current DC-link PFC AC/DC converter system, while reducing the system complexity and cost compared to traditional isolated solutions. The chapter presents experimental results showing that the proposed VGC and GCC techniques can limit the LF CM leakage current to values below typical RCD trip levels and achieve a touch voltage below the most stringent limit of the standard, thus ensuring end-user safety. The study also discusses the advantages and limitations of the proposed non-isolated converter concept.

- **Chapter 5** studies the loss-optimum operations of the 3-Φ Bb voltage DC-link AC/DC converter system, considering a wide output voltage range from 200 V to 800 V. Two new 2/3-PWM schemes for the transition-mode, i.e., the operating region between the pure buck-mode and pure boost-mode, are proposed to ensure loss-optimum converter operation. The proposed synergetic operating principle requires only three (out of five) half-bridges to operate with PWM at any given point in time and the minimum possible DC-link voltage is used to ensure minimum switching losses.

- **Chapter 6** first compares the performance of current and voltage DC-link systems, based on the previous analyses and experimental results, in terms of implementation complexity, efficiency, and conducted EMI noise emissions. Then, the most significant findings of this thesis, i.e., loss-optimal operation over an ultra-wide output voltage range and its synergetic control, ground current control enabling future non-isolated EV chargers, and independent output voltage control for heavy-duty EVs are summarized. The thesis concludes with an outlook on topics for further research.

2

A Three-Phase Synergetically Controlled Buck-Boost Current DC-Link EV Charger

Chapter Abstract

With the ever-increasing share of electric vehicles (EVs) comes a need for highly efficient and compact EV chargers. EV charger modules should provide a wide output voltage range (200 V to 1000 V) to ensure compatibility with various EV battery voltages. Thus, buck-boost functionality is needed, which can advantageously be realized by a current DC-link topology: a buck-type current-source rectifier (CSR) stage and a downstream three-level (3-L) boost-type DC/DC-stage share the main magnetic component (the DC-link inductor). Furthermore, the two stages can operate collaboratively: for low output voltages, the CSR-stage controls the output voltage and the DC/DC-stage is clamped to avoid switching losses; for high output voltages, the DC/DC-stage shapes the DC-link current such that the CSR-stage operates with 2/3-PWM (switching limited to two out of the three phases) and hence with reduced switching losses. This chapter thus introduces a simplified synergetic control concept that ensures this loss-optimum operation of the two-stage system for any output voltage. A compact 10-kW hardware demonstrator with a power density of 6.4 kW/dm^3 (107.5 W/in^3) is then used to verify the control concept and the seamless transitions between operating modes. For the first time, a system-level experimental demonstration of the loss savings achieved by 2/3-PWM is provided, and pre-compliance conducted EMI test results meet CISPR 11 / Class A. Moreover, a detailed experimental characterization of losses/efficiency over the full range of output voltage and power confirms the loss models and the design procedure presented earlier. Finally, the demonstrator shows quite a flat efficiency characteristic (higher than 98% for most operating points with output voltages above 400 V and more than 25% of rated load) with a peak efficiency of 98.8% at 520 V output voltage and 5 kW. All in all, the presented current DC-link buck-boost PFC rectifier system features a promising solution for future isolated or non-isolated EV charger modules.

2.1 Introduction

The International Energy Agency (IEA) estimates that there will be 220 million electric vehicles (EVs) on the road by 2030, with China, Europe, and North America accounting for the majority of this growth according to the "Global EV Outlook 2021" report [68]. Obviously, EV batteries must be recharged or might even serve as energy storage complementing fluctuating renewable generation in future energy systems [69]. Hence, EV charging technology is vital to the widespread adoption of EVs and to shaping the future of low-carbon-emission road transport.

A typical battery charging profile comprises two charging modes, i.e., constant current (CC) mode and constant voltage (CV) mode [70, 71]. Starting with a discharged battery, first, a high charging current is applied in the CC

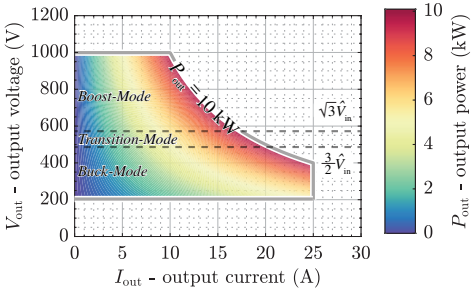

Fig. 2.1: Typical operating range of a 10 kW EV charger module covering a output voltage from 200 V to 1000 V with an output current limit of $I_{out} = 25$ A. Such a wide output voltage range is covered by three main operating modes, i.e., buck-mode, transition-mode, and boost-mode.

charging mode until the battery voltage reaches a certain threshold voltage, and then above this threshold voltage, the charger is switched to CV charging mode, completing the charging process with a decreasing current at an almost constant battery voltage to avoid thermal run-away of the battery [72]. Hence, EV chargers do not operate at full load most of the time: in the CC mode, although the charger provides rated current, the battery voltage only gradually increases starting typically from about 80% of the rated voltage for a lithium-ion battery [70]; in the CV mode, only a small charging current is allowed if the battery voltage is close to the rated value. Various nominal battery voltages such as 400 V or 800 V are in use, and hence standards such as CHAdeMO [73] define wide output voltage ranges of 150 V to 1000 V for universal EV chargers, see also **Fig. 2.1**. Thus, high-efficiency operation over wide output-power and output-voltage ranges, i.e., a flat high-efficiency characteristic, is a desirable feature of power converters used for EV charging.

EV chargers interface the AC mains to the DC terminals of EV batteries and are typically realized with two converter stages [8]: a grid-side AC/DC PFC rectifier and a subsequent, typically isolated, DC/DC-stage. Such isolated converter stages can be implemented, for example, as a dual active bridge (DAB) converter [16, 17, 19, 74] or as an LLC resonant converter [22], which both provide an adjustable voltage gain. Even though, in this case, the required ultra-wide output voltage regulation capability can be collaboratively provided by both the DC/DC converter and the 3-Φ PFC rectifier front-end, loss-optimal operating modes of the whole system depend on the specific loss characteristics of the PFC rectifier and the DC/DC-stage. In other words,

these loss-optimal operating modes are different for each specific realization of these converter stages. Thus, optimal designs of such a cascaded system have to take the front-end and the isolation-stage into account at the same time instead of optimizing them separately. To avoid such design and control issues, and to achieve high efficiency, often series-resonant DC/DC-stages with limited voltage control range, i.e., DC transformers (DCXs) [23, 24, 75], are used [25]. Then, the AC/DC PFC rectifier stage must provide buck-boost functionality to cover the wide output voltage range (typ. 200 V to 1000 V, see **Fig. 2.1**). This is especially also the case in future non-isolated EV chargers [9].

Today, most EV chargers employ topologies with a voltage DC-link [13] (i.e., a DC-link capacitor is placed between a boost-type PFC rectifier and a buck-type DC/DC converter, realizing boost-buck functionality). Alternatively, however, topologies with a current DC-link (i.e., a DC-link inductor connecting a buck-type PFC rectifier and a boost-type DC/DC converter) can also be applied.

Current DC-link topologies have first been employed in thyristor-based line-commutated medium-voltage drives in the 1970s [76]. Later, with the availability of gate-turn-off thyristors (GTOs) or gate-commutated thyristors (GCTs), PWM operation and thus motor-friendly waveforms and reliable short-circuit protection could be realized [77–81]. Applications with lower voltages and power levels have also been considered due to the advent of wide-bandgap (WBG) power semiconductors, which facilitate higher switching frequencies and thus a reduction of the otherwise potentially large DC-link inductor volume [82], such as variable speed drives [83–86], data center power supplies [87–89], solid-state transformers [90], electric springs [91], grid interfaces for renewable energy sources [92], and recently also EV chargers [11, 93–95]. Furthermore, extensive research has been conducted on the duality between and the comparative analyses of voltage DC-link and current DC-link converters [96–101].

However, current DC-link systems require switching devices with the capability to block both voltage polarities and to conduct at least one or possibly (for bidirectional AC/DC conversion and uni-polar DC voltage) both current directions. These switching devices were commonly realized by series connection of diodes with uni-polar devices, e.g., normally-on SiC JFETs [83, 102], for uni-directional operation. However, recently, the development of monolithic bidirectional power transistors has gained traction [103–105]; these devices provide the required functionality with only about one fourth of the chip area required for today's realizations based on inverse-series connections of uni-polar devices [48]; hence, in contrast to voltage DC-link

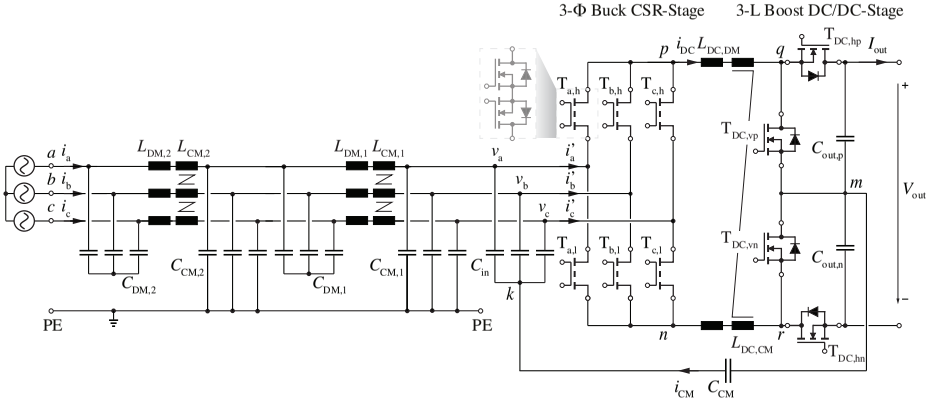

Fig. 2.2: Power circuit of the considered 10 kW three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier system including CM/DM EMI filters, which employs a 3-Φ buck-type current-source rectifier (CSR)-stage linked to a 3-L boost-type DC/DC-stage via a shared DC-link inductor. To filter the high-frequency common-mode (CM) noise at the DC output port, an integrated CM filter consisting of a shared CM inductor $L_{\mathrm{DC,CM}}$ in the DC-link and a capacitor C_{CM} that ties the DC output midpoint to the artificial mains neutral point k, formed by star-connected input capacitors, is applied. **Tab. 2.1** lists the key specifications and components.

Tab. 2.1: System specifications and key components of the demonstrator introduced in **Section 2.5**.

	Description	Value
V_{in}	RMS phase volt.	230 V
V_{out}	DC output volt. range	200 V~1000 V
P_{out}	Rated output power	10 kW
$I_{out,max}$	Output curr. limit	25 A (V_{out} < 400 V)
T_{CSR}	CSR-stage semi.	C3M0021120K, 1200 V, 21 mΩ
f_{CSR}	CSR-stage sw. freq.	100 kHz
$T_{DC/DC}$	DC/DC-stage semi.	C3M0010090K, 900 V, 10 mΩ
$f_{DC/DC}$	DC/DC-stage sw. freq.	100 kHz
$2\times L_{DC,DM}$	DC-link DM ind.	2×125 µH (3×N87 ELP 43/10/28, 14 turns)
$2\times L_{DC,CM}$	DC-link CM ind.	2×5.5 mH (VAC 500F 40/25/15, 10 turns)
C_{in}	Input filter cap.	3×6 µF
$C_{out,p} = C_{out,n}$	Output filter cap.	2×11.2 µF
C_{CM}	Integrated filter cap.	88 nF
$L_{DM,1} = L_{DM,2}$	EMI DM ind.	15 µH
$C_{DM,1} = C_{DM,2}$	EMI DM cap.	3 µF
$L_{CM,1} = L_{CM,2}$	EMI CM ind.	1.2 mH (VAC 20/12.5/8, 11 turns)
$C_{CM,1} = C_{CM,2}$	EMI CM cap.	18.8 nF

topologies, current DC-link topologies feature a significant potential for future performance improvements and/or cost reductions.

Therefore, targeting a universal[1] EV charger AC/DC module covering the wide operating range shown in **Fig. 2.1**, the 3-Φ bidirectional buck-boost (bB) current DC-link PFC rectifier system shown in **Fig. 2.2** is considered in this chapter. So far, a similar topology has been realized by a 3-Φ buck-type current-source rectifier (CSR)-stage and a subsequent two-level (2-L) boost-type DC/DC-stage [106–108]. However, in this chapter, a 3-L boost-type DC/DC-stage is employed to avoid considerable hard-switching losses occurring at high output voltages for EV battery charger applications. Compared

[1]Note that **Chapter 4** discusses a control method for the proposed topology, which regulates the low-frequency ground leakage current to zero and allows a direct connection of the DC output midpoint to protective earth, hence facilitating non-isolated charger applications.

to a conventional realization with a 3-Φ boost-buck (Bb) voltage DC-link PFC rectifier [45], advantageously only one shared main magnetic component, i.e., the DC-link inductor connecting the CSR-stage and the DC/DC-stage, is needed instead of three AC-side boost inductors plus at least one DC-side inductor of the then needed buck-type DC/DC-stage, which facilitates a compact converter realization.

The conventional loss-optimal operation and the corresponding control of such two-stage 3-Φ buck-boost current DC-link PFC rectifiers, considering 2-L DC/DC-stages, have been analyzed, e.g., in [107, 108], where a robust controller enabling operation with heavily unbalanced mains is presented in [107], and [108] derives a detailed control-oriented small-signal model. In both cases, the implemented control methods can achieve a state-of-the-art loss-optimal operation: if the output voltage is relatively low (buck-mode, see **Fig. 2.1**), the DC/DC-stage is clamped without generating switching losses but the CSR-stage solely regulates the output voltage; advantageously the DC/DC boost-stage is only activated if the output voltage is high[2] (boost-mode, see **Fig. 2.1**).

However, if the DC/DC-stage has to operate, it can advantageously be used to shape the DC-link current to follow the maximum of the absolute values of the three mains currents, which allows advanced 2/3-PWM operation of the CSR-stage [104, 107, 109, 110]. The advanced 2/3-PWM only needs to switch two instead of three phases of the CSR-stage within one switching period, resulting in a significant reduction in switching losses because there are fewer switching instants and these happen at lower voltages. Taking advantage of this, a synergetic control concept that operates the converter shown in **Fig. 2.2** in the loss-optimal mode for any output voltage (i.e., employs 2/3-PWM whenever possible, and clamps the DC/DC-stage if the output voltage is sufficiently low) has been introduced in [95]. However, the controller structure presented in [95] is quite complex regarding its implementation, and the concept has further never been experimentally verified, especially over a wide output voltage range where different modulation schemes and operating modes have to be covered.

Furthermore, [104] reports significant calculated performance improvements achieved by using advanced 2/3-PWM instead of conventional 3/3-PWM (with a constant DC-link current that is at least as high as the peak value of the phase currents), but considers only the CSR-stage. Thus, [93, 94]

[2] The boost stage needs to be (temporarily) activated if the output voltage is higher than $3/2 \cdot \hat{V}_{\mathrm{in}}$ with $\hat{V}_{\mathrm{in}}$ denoting the phase voltage amplitude, i.e., the maximum output voltage that a buck-type CSR-stage can generate.

have addressed the system-level losses (i.e., the CSR-stage and the DC/DC-stage) and provide a detailed loss modeling analysis and EMI filter design procedure for the analyzed topology shown in **Fig. 2.2**, and use Pareto optimization to select a final converter design. However, there is again a lack of a comprehensive experimental evaluation of the system-level loss reduction and of the possible impact on the EMI emission signature of using 2/3-PWM.

Therefore, this chapter addresses the research gaps mentioned earlier by introducing a simplified and intuitive implementation of the synergetic control concept retaining all the advantageous features, e.g., achieving loss-optimal operation with advanced 2/3-PWM and ensuring seamless transitions between different operating modes democratically. The proposed control strategy is then verified on a realized 10 kW hardware demonstrator to, importantly, provide extensive experimental verification of the proposed design and the synergetic control method, e.g., efficiency characteristics over a wide operating range, the efficiency improvement achievable with 2/3-PWM, and the conducted EMI noise emissions.

First, **Section 2.2** derives and explains the advanced 2/3-PWM concept for current DC-link systems with the comparison of conventional 3/3-PWM, before **Section 2.3** discusses the loss-optimal operating modes for the three regions of the wide output voltage range (200 V to 1000 V) indicated in **Fig. 2.1**. **Section 2.4** then presents the new simplified synergetic control structure that ensures operation in the respective loss-optimal mode and seamless transitions between these modes. **Section 2.5** introduces a 10 kW hardware demonstrator and provides extensive experimental results. Detailed efficiency measurements in the full operating range demonstrate a flat efficiency characteristic and a peak efficiency of 98.8%. EMI pre-compliance test results meeting CISPR 11 / Class A limits are also provided. Finally, **Section 2.6** concludes this chapter.

2.2 Current DC-Link Converter Modulation

The CSR-stage (see **Fig. 2.2**) consists of two commutation cells, each comprising three bidirectional switches (e.g., the high-side commutation cell consists of $T_{a,h}$, $T_{b,h}$, and $T_{c,h}$). At any given time, one and only one (otherwise, the line-to-line voltage would be short-circuited) switch per commutation cell is turned on and connects the DC-link current to one of the three-phase terminals. Therefore, the switching state of the CSR-stage can be described in the form [ab] (see Fig. 2.3), where this specific example indicates that the high-side commutation cell connects phase *a* to the DC-link and the low-side commu-

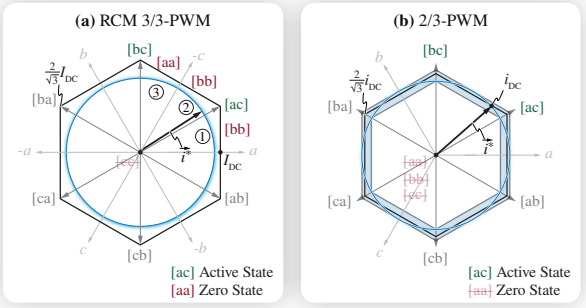

Fig. 2.3: Space vector diagrams of **(a)** Reduced CM (RCM) 3/3-PWM where the hexagon size is fixed by a constant I_{DC}, i.e., the active space vectors' magnitude is $2/\sqrt{3}\, I_{DC}$ and **(b)** 2/3-PWM where the hexagon size is pulsating (over the shaded area) according to a time-varying i_{DC}, i.e., the active space vectors' magnitude is $2/\sqrt{3}\, i_{DC}$. The switching state of the CSR-stage is expressed by the turned-on switches of the high-side and low-side commutation cells as, for example, [ac], which indicates that the DC-link current flows through $T_{a,h}$ and $T_{c,l}$.

tation cell connects phase b to the DC-link. Freewheeling states are possible, too, e.g., [bb] indicates that the DC-link current freewheels through the two commutation cells' switches connected to phase b. In each switching period, a sequence of switching states must be applied to realize sinusoidal local average values of the phase currents, i'_a, i'_b, and i'_c. Two conceptually different PWM schemes, i.e., conventional 3/3-PWM and advanced 2/3-PWM [107, 109], can be applied and are discussed in the following.

2.2.1 Conventional 3/3-PWM

Conventionally, current DC-link rectifiers operate with a constant DC-link current I_{DC} that must be at least as high as the peak value of the phase currents. A constant DC-link current and the available switching states define six active space vectors with a magnitude of $2/\sqrt{3}\, I_{DC}$ and three zero vectors (freewheeling states) as indicated in **Fig. 2.3a**. To realize a desired input current space vector $\vec{i}^*$, each switching period is composed of the two closest active states and one zero state. Therefore, all three phases are switching with PWM ("3/3-PWM", see **Fig. 2.4a**) within one switching period.

In the example shown in **Fig. 2.3a**, which considers a vector $\vec{i}^*$ in sector ②, the active states [ac] and [bc] are needed, whereas the selection of the

Fig. 2.4: Calculated hard-switching energy dissipated in the switches $T_{a,h}$ (red) and $T_{a,l}$ (green) connected to phase *a* over one mains period, and corresponding switched voltages and currents when **(a)** 3/3-PWM or **(b)** 2/3-PWM is applied. In both cases, V_{out} = 800 V and P_{out} = 10 kW. In average, 1.7 W instead of 7.5 W, i.e., a 77% reduction of switching losses, results if 2/3-PWM instead of 3/3-PWM is employed, since the switches switch less frequently and with reduced voltages and currents (details in the text). Note that soft-switching transitions and their losses are neglected.

Tab. 2.2: Modulation sequences, i.e., switching state sequences, within one switching period considering three exemplary sectors (see **Fig. 2.3**). The hard turn-on switching transitions of the two switches connected to phase a are indicated by the $\Rightarrow$ symbol, whereas the soft turn-on and all turn-off switching transitions are indicated by the $\rightarrow$ symbol.

Sector	RCM 3/3-PWM	2/3-PWM
①	[bb]⇒[ab]→[ac]→[ab]→[bb]	[ab]→[ac]→[ab]
②	[bb]→[bc]⇒[ac]→[bc]→[bb]	[bc]⇒[ac]→[bc]
③	[aa]→[ac]→[bc]→[ac]→[aa]	[ac]→[bc]→[ac]

zero state ([aa] or [bb] or [cc]) is a degree of freedom to optimize, e.g., the overall switching losses [82] or the resulting low-frequency CM voltage [111]. If the zero state corresponding to the phase with the minimum phase voltage, i.e., phase b and hence state [bb] in sector ②, is selected, a Reduced Common-Mode (RCM) 3/3-PWM[3] results without sacrificing switching losses [111], which advantageously features a continuous low-frequency CM voltage without any voltage step at the sector boundaries [94]. This facilitates the integrated CM filter composed of $L_{\mathrm{DC,CM}}$ and C_{CM} (see **Fig. 2.2**). **Tab. 2.2** lists the resulting RCM 3/3-PWM switching sequences for $\vec{i}^{\,*}$ in three exemplary sectors. Note that the sequences are symmetric with respect to the center of a switching period, which facilitates synchronous sampling of the local average (over one switching period) DC-link current and further ensures that only one commutation cell switches (instead of two commutation cells) during each transition [82, 83, 94, 99, 111].

Note that the modulation index of the CSR-stage is

$$M = \frac{\hat{I}_{\mathrm{in}}}{i_{\mathrm{DC}}} = \frac{\bar{v}_{\mathrm{pn}}}{\frac{3}{2}\hat{V}_{\mathrm{in}}} \leq 1, \tag{2.1}$$

and hence a maximum DC output voltage of $\bar{v}_{\mathrm{pn}} = V_{\mathrm{out}} \leq 3/2\hat{V}_{\mathrm{in}} = 488\,\mathrm{V}$ (the numerical value refers to a 400 V mains) can be realized without a downstream DC/DC-stage (or with a DC/DC-stage not operating as shown in **Fig. 2.2**).

[3] Unless otherwise noted, 3/3-PWM indicates RCM 3/3-PWM in the rest of chapter.

2.2.2 Advanced 2/3-PWM

Differently, if such a DC/DC-stage is present (see **Fig. 2.2**), the DC/DC-stage can be utilized to realize 2/3-PWM of the CSR-stage [104, 107, 109, 110], which requires a time-varying DC-link current i_{DC}. This time-varying DC-link current i_{DC} follows the upper envelope of the 3-Φ current absolute values (see **Fig. 2.4b**), i.e., shows the typical six-pulse shape. In the space vector diagram (see **Fig. 2.3b**), such a six-pulse-shaped DC-link current is translated into a correspondingly pulsating size of the hexagon spanned by the six active vectors (whose length, after all, is given by the instantaneous value of the DC-link current) [104]. Zero states are not needed to modify the length of the synthesized vector; actually, any point on the hexagon can be reached by only applying active vectors. Because now the hexagon's size is pulsating, it becomes possible to synthesize the circular trajectory of $\vec{i}^{*}$ without any zero states, which is clearly visible from the exemplary switching sequences given in **Tab. 2.2**. Consequently, each switching period is only composed of two active switching states but no zero state such that only two out of three phases are switching with PWM ("2/3-PWM") over one switching period. The switching sequence is implemented to minimize the voltage-time area of the DC-link inductor HF voltage, i.e., the corresponding switching-frequency DC-link current ripple, by centering the switching state with a larger v_{pn} within one switching period, e.g., in sector ②, with $v_{\mathrm{ac}} > v_{\mathrm{bc}}$ switching state [ac] is centered, and vice versa in sector ③ [94, 104].[4]

Importantly, an additional converter stage, e.g., a boost DC/DC-stage as shown in **Fig. 2.2**, is always needed to implement 2/3-PWM because **(i)** the six-pulse shape of the DC-link current has to be regulated by this additional converter stage; **(ii)** 2/3-PWM can only rectify 3-Φ mains voltages into six-pulse shape $\bar{v}_{\mathrm{pn}}$ at the output of the CSR-stage, so that this converter stage is required to regulate $\bar{v}_{\mathrm{pn}}$ into a constant DC output voltage.

2.2.3 Switching Loss Comparison

The potential switching loss savings of operating the CSR-stage with 2/3-PWM instead of 3/3-PWM are analyzed in the following. Focusing on the CSR-stage, a high output voltage ($V_{\mathrm{out}} = 800\,\mathrm{V}$) that requires operating the boost-type DC/DC-stage in both cases is considered. **Fig. 2.4** compares the hard-switching losses E_{sw} generated in the two bidirectional switches

[4] Note that the switched voltage of the 3-L boost DC/DC-stage is also aligned at the center of one switching period such that the voltage-time area of the DC-link inductor HF voltage, i.e., the time integral of the voltage difference $v_{\mathrm{pn}} - v_{\mathrm{qr}}$ (see **Fig. 2.2**), is minimized.

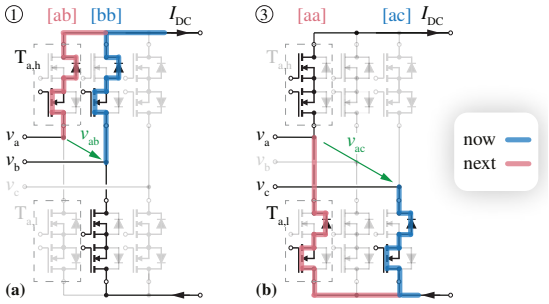

Fig. 2.5: Two exemplary switching states before and after actual commutations occurring in sectors **(a)** ① and **(b)** ③ (see **Fig. 2.3**), which directly involve $T_{a,h}$ or $T_{a,l}$, respectively. In sector ①, switching from [bb] to [ab] is a hard-switching transition since the switched voltage $v_{ab} > 0$ and the switched current flows out of the switching node (see **Fig. 2.2**). In sector ③, the switched voltage is $v_{ac} > 0$ but the switched current flows into the switching node. Thus, switching from [ac] to [aa] is a soft transition. A more detailed explanation is given in the main text.

connected to phase a (i.e., $T_{a,h}$ and $T_{a,l}$) considering the 3/3-PWM[5] and the 2/3-PWM for $V_{out} = 800\,\text{V}$ and $P_{out} = 10\,\text{kW}$.

Before further exploring these results, it is important to briefly discuss the physical realization of these switches, which is indicated in **Fig. 2.2** and shown in detail in **Fig. 2.5**, and the nature of the commutations. In general, commutations occur between two switches of one commutation cell in a current DC-link rectifier, e.g., changing the state from [bb] to [ab] implies that the DC-link current commutates from $T_{b,h}$ to $T_{a,h}$ as indicated in **Fig. 2.5**; the involved commutation voltage is the instantaneous line-to-line voltage v_{ab}. As the line-to-line voltage attains both polarities, each switch must be realized by an inverse-series connection of two MOSFETs to block these bipolar voltages. Note that, different from the voltage DC-link PFC rectifier where the commutation loop closes over the DC-side commutation capacitors (in parallel with the DC-link capacitors), the commutation loop of the current DC-link rectifier includes AC-side commutation capacitors (in parallel with the AC-side filter capacitors C_{in} in **Fig. 2.2**).

For a given polarity of a line-to-line voltage, e.g., v_{ab}, two of the four involved MOSFETs can either be turned-on or turned-off without affecting the switching state because their anti-parallel diodes are forward-biased by

[5] 3/3-PWM uses $i_{DC} = \hat{i}_{DC,2/3} = \hat{I}_{in}$, which is the minimum constant DC-link current required to generate 3-Φ sinusoidal mains currents without modulation saturation.

the line-to-line voltage. Whereas it is generally advantageous to keep these MOSFETs on (to reduce conduction losses), the current-direction-dependent four-step commutation sequences [112] that are needed in practice to ensure that (i) there is always a path for the DC-link current and (ii) the AC-side capacitors are never short-circuited, result in the (intermediate) circuit configurations just prior and after the actual current commutation as shown in **Fig. 2.5**. It is clearly recognizable that the actual commutations are identical to those known from half-bridge arrangements with a voltage DC-link; however, the assignment of turn-on and turn-off losses to the individual MOSFETs changes with the polarity of the involved line-to-line voltage. As here the focus is on system-level loss behavior, losses are assigned to the bidirectional switches, e.g., $T_{a,h}$ or $T_{a,l}$, without considering the individual MOSFETs for simplicity. Thus, considering the example occurring in ① when implementing 3/3-PWM (see **Fig. 2.5a**), the transition from [bb] to [ab] results in a hard-switching with $T_{a,h}$ subject to a hard turn-on.[6] The other exemplary transition in the low-side commutation cell from [ac] to [aa] occurs in ③ when implementing 3/3-PWM (see **Fig. 2.5b**), which results in a soft-switched transition with $T_{a,l}$. Soft-switching transitions are assumed to be lossless.

The hard-switching losses E_{sw} of a given transition can be modeled as

$$E_{sw} = (k_1 I_{sw}^2 + k_2 I_{sw} + k_3) V_{sw} + (C_{oss,Q} + C_{par}) V_{sw}^2, \tag{2.2}$$

where V_{sw} and I_{sw} indicate the switched voltage and current, respectively. The losses contain two main contributions, i.e., losses introduced by the overlap of the switched voltage and current waveforms, and capacitive losses resulting from the charging and discharging of the semiconductor (charge-equivalent) output capacitance $C_{oss,Q}$ and the parasitic (PCB, etc.) capacitance C_{par} [93].

The hard-switching losses dissipated in $T_{a,h}$ and $T_{a,l}$ are indicated **Fig. 2.4** assuming PFC operation with unity power factor over one mains period. Furthermore, the modulation sequences, i.e., the switching state sequences, of three exemplary sectors are listed in **Tab. 2.2**. In sector ①, the switching transition from [bb] to [ab] contributes to significant switching losses because of a comparably large switched line-to-line voltage v_{ab}. However, such a hard-switching transition only exists for 3/3-PMW since the zero state [bb] is not needed for 2/3-PWM; note that thus significantly longer intervals without hard-switching losses are achieved when using 2/3-PWM. In sector ②, hard-switching losses are generated when switching from [bc] to [ac] for both 3/3-PWM and 2/3-PWM. However, importantly, in sector ②, the switched line-to-line voltage v_{ab} (see **Fig. 2.4**) is lower, leading to relatively small switching

[6] All hard-switching losses are assigned to the turning-on switch for simplicity [93]

losses compared to the one generated in sector ① with 3/3-PWM. In sector ③, $T_{a,h}$ and $T_{a,l}$ are not subject to hard turn-on transitions and hence almost no switching losses are generated for both, 3/3-PWM and 2/3-PWM.

Thus, advantageously, 2/3-PWM does not need those hard-switched transitions that in 3/3-WPM result in the largest contributions to the overall switching losses because of high switched voltages. Considering, e.g., the applied SiC MOSFET *C3M0021120K* and its detailed switching loss models based on calorimetric measurements [93], averaging the hard-switching energy dissipation over one mains period results in switching losses of 1.7 W for 2/3-PWM instead of 7.5 W for 3/3-PWM, i.e., a 77% reduction of switching losses (for PFC operation with unity power factor). Note that furthermore also lower conduction losses (reduced by 8 % [104]) are expected since 2/3-PWM employs the minimum possible time-varying DC-link current.

2.3 Loss-Optimal Operation

Whereas 2/3-PWM reduces the CSR-stage switching losses, it requires the DC/DC-stage to operate; on the other hand, the CSR-stage alone can control low output voltages but then needs to operate with 3/3-PWM. It is therefore interesting to consider the loss-optimal operating modes of the 3-Φ bB current DC-link PFC rectifier system (see **Fig. 2.2**), whose key specifications and circuit parameters are listed in **Tab. 2.1**.

The wide output voltage range (200 V to 1000 V) is covered by three operating modes [94], i.e., buck-mode ($V_{out} < 3/2\hat{V}_{in} = 488\,V$), boost-mode ($V_{out} > \sqrt{3}\hat{V}_{in} = 563\,V$), and, in between, transition-mode ($3/2\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$), by collaboratively operating the CSR-stage and the DC/DC-stage; see also the simulated key waveforms in **Fig. 2.6**. The semiconductor losses, as the main contribution to the total converter losses, are minimized if the following two criteria are met:

1. The minimum possible DC-link current should be used, which results in minimum conduction losses of the whole system as the DC-link current flows through the turned-on semiconductors of the CSR-stage and the DC/DC-stage, and in the DC-link inductor. The CSR-stage forms the 3-Φ mains currents (see **Section 2.2**), and likewise the DC/DC-stage forms the output DC current, by pulse-width modulating the DC-link current. Thus,

$$i_{DC} \geq \max(|i_a|, |i_b|, |i_c|, I_{out}) \tag{2.3}$$

must be guaranteed at any moment; equality results in the (potentially time-varying) minimum possible DC-link current.

2. The number of switching instants and/or the switched voltages/currents should be minimized. Thus, 2/3-PWM of the CSR-stage should be used whenever the DC/DC-stage must operate anyhow because of a high output voltage, or alternatively, the DC/DC-stage should be clamped (i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on).

These three main operating modes are then explained in detail in the following.

2.3.1 Buck-Mode

If the output voltage is low, i.e., $V_{out} < 3/2\hat{V}_{in} = 488\,V$, the converter operates in the buck-mode (see **Fig. 2.6a**). The output voltage can be obtained by the CSR-stage directly stepping down the 3-Φ mains voltages, and no boost functionality is needed, i.e., the switching losses of the DC/DC-stage can be avoided by permanently turning on $T_{DC,hp}$ and $T_{DC,hn}$ (note that constant $v_{qr} = V_{out}$ in **Fig. 2.6a**). Furthermore, clamping the DC/DC-stage automatically results in

$$i_{DC} = I_{DC,3/3} = I_{out} > \max(|i_a^*|, |i_b^*|, |i_c^*|), \tag{2.4}$$

such that the minimum possible DC-link current is applied according to (2.3). Sinusoidal 3-Φ mains currents are realized by 3/3-PWM of the CSR-stage, i.e., v_{pn} also attains zero (corresponding to the zero switching states) in **Fig. 2.6a**.

2.3.2 Boost-Mode

If the output voltage is high, i.e., $V_{out} > \sqrt{3}\hat{V}_{in} = 563\,V$, the converter operates in the boost-mode (see **Fig. 2.6c**). The DC/DC-stage *must* operate to step-up the output voltage of the CSR-stage to higher output voltages. Thus, advantageously, the two converter stages should be operated synergetically/collaboratively: as the DC/DC-stage is needed anyway, it can control the DC-link current to the six-pulse shape defined by

$$i_{DC} = i_{DC,2/3} = \max(|i_a|, |i_b|, |i_c|) > I_{out}, \tag{2.5}$$

which allows implementing 2/3-PWM of the CSR-stage with significantly reduced switching losses (see **Section 2.2**). Note that in **Fig. 2.6c**, the input voltage of the DC/DC-stage, v_{qr}, is now a high-frequency (HF) switched

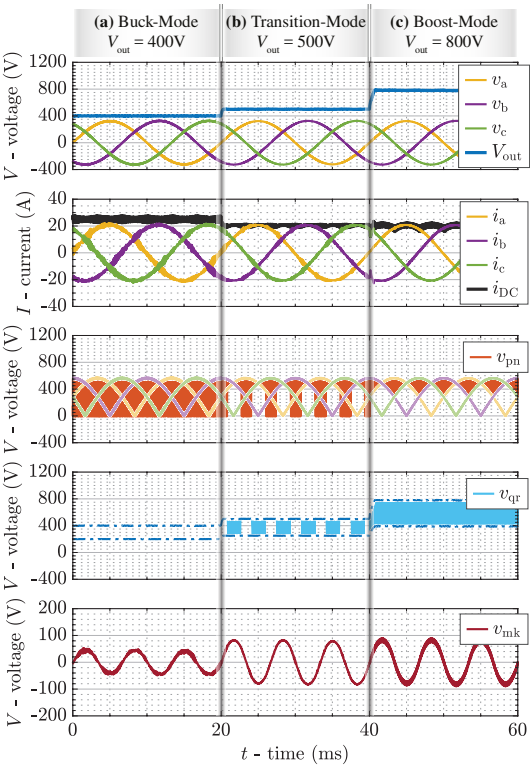

Fig. 2.6: Simulated key waveforms of the 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 2.2** when operating in **(a)** buck-mode, **(b)** transition-mode, and **(c)** boost-mode when supplying constant power at different output voltages. The switched DC-side voltage of the CSR-stage, v_{pn}, and the switched input voltage of the DC/DC-stage, v_{qr}, indicate the CSR-stage modulation method (with 2/3-PWM, v_{pn} never attains zero as no zero states are employed) and/or the clamping of the DC/DC-stage. The voltage v_{mk} across the integrated CM filter capacitor C_{CM} verifies that mainly an LF CM voltage appears at the output terminals. Note that v_{qr} is a 3-L switched voltage with the levels of 0, $V_{out}/2$, and V_{out} if the DC/DC-stage is actively switching.

voltage, and on the other hand, the DC-side voltage of the CSR-stage, v_{pn} never attains zero, corresponding to the absence of zero states in 2/3-PWM. The time-varying DC-link current $i_{DC,2/3}$ is also the minimum possible DC-link current according to (2.3) and hence minimizes the overall conduction losses.

2.3.3 Transition-Mode

If the output voltage is in the range of $^3/_2\hat{V}_{\text{in}} < V_{\text{out}} < \sqrt{3}\hat{V}_{\text{in}}$, i.e., higher than the buck-mode boundary but lower than the boost-mode boundary, the boost functionality provided by the DC/DC-stage is not needed continuously, but only during parts of the mains period. By selecting the DC-link current as in (2.3), essentially

$$i_{\text{DC}} = \max(I_{\text{DC},3/3}, i_{\text{DC},2/3}) \tag{2.6}$$

results and hence the CSR-stage operation alternates between 3/3-PWM and 2/3-PWM accordingly, and the DC/DC-stage is activated only when the boost functionality is required. This is clearly visibly in the simulated v_{pn} and v_{qr} waveforms shown in **Fig. 2.6b**.

2.4 Synergetic Control Strategy

A synergetic control strategy of the 3-Φ bB current DC-link PFC rectifier system (see **Fig. 2.2**), which ensures that two converter stages always operate collaboratively in loss-optimum modes and transition seamlessly between these modes if the output voltage changes, is presented in this section. Whereas a control method in [95] has been introduced earlier, we present here a simplified and intuitive version (without modulation indices of two stages) that, however, does not sacrifice any functionality. **Fig. 2.7** shows the corresponding block diagram and highlights the three main functional blocks, i.e., *Output Voltage Control*, *DC-Link Current Reference Generation*, and *DC-Link Current Control*, which are explained in detail in the following subsections.

2.4.1 Output Voltage Control

The outermost control loop (see **Fig. 2.7a**) tracks the output voltage reference V_{out}^* by providing the corresponding power reference P^*. From that, the CSR-stage input reference conductance G^* follows as

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{\text{in,meas}}^2}. \tag{2.7}$$

The 3-Φ sinusoidal mains current references i_{a}^*, i_{b}^*, and i_{c}^* that are then selected proportional to the corresponding measured 3-Φ input voltages v_{a}, v_{b}, and v_{c} such that purely ohmic operation of the 3-Φ mains results. The output current reference I_{out}^* is calculated by dividing P^* by V_{out}^*.

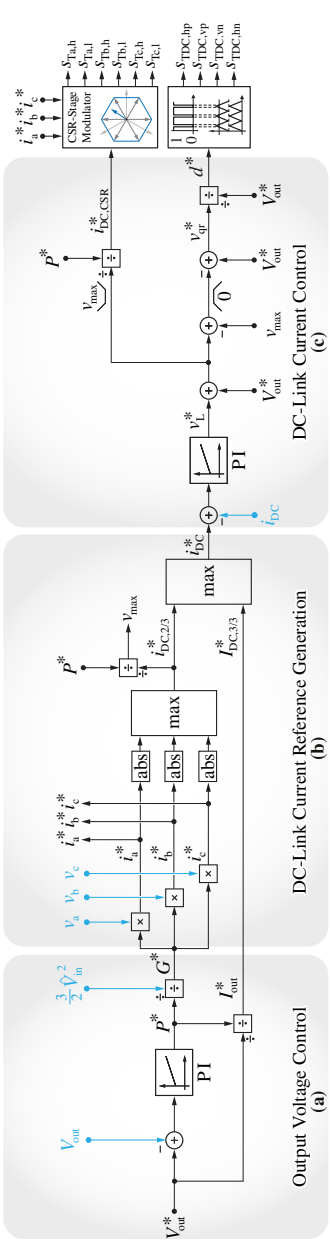

Fig. 2.7: Block diagram of the proposed synergetic control strategy of the 3-Φ buck-boost current DC-link PFC rectifier system (see **Fig. 2.2**). The three main functional blocks enable collaborative operation of the 3-Φ CSR-stage and of the boost-type DC/DC-stage, and seamless transitions between buck-mode and boost-mode needed to cover the wide output voltage range. Note that regular sampling is employed to sense only local-average (over one switching period) quantities.

2.4.2 DC-Link Current Reference Generation

The selection of the appropriate DC-link current reference (see **Fig. 2.7b**) is at the core of the proposed synergetic control structure and vital to achieving seamless and automatic transitions between the different operating modes and modulation schemes. As discussed above in **Section 2.3**, in the buck-mode, $i_{DC} = I^*_{DC,3/3} = I^*_{out}$ is used, which results in 3/3-PWM of the CSR-stage while the DC/DC-stage is clamped. In the boost-mode, $i_{DC} = i^*_{DC,2/3} = \max(|i^*_a|, |i^*_b|, |i^*_c|)$ is needed ro realize 2/3-PWM of the CSR-stage. Thus, the overall DC-link current reference is

$$i^*_{DC} = \max(I^*_{DC,3/3}, i^*_{DC,2/3}), \tag{2.8}$$

i.e., the DC-link current reference always corresponds to the minimum possible DC-link current leading to reduced switching losses and conduction losses.

2.4.3 DC-Link Current Control

Finally, the DC-link current is closed-loop-controlled (see **Fig. 2.7c**) by comparing the DC-link current reference i^*_{DC} with the measured DC-link current i_{DC}. The deviation is processed by a PI-controller that then defines the voltage v^*_L across the DC-link inductor L_{DC} needed to counteract the control error. It is important to highlight that v^*_L can be realized by either the CSR-stage *and/or* the DC/DC-stage, e.g., a positive v^*_L can be generated by either an increased output voltage v_{pn} of the CSR-stage or a decreased input voltage v_{qr} of the DC/DC-stage (see **Fig. 2.2** for the definition of these voltages). Thus, the second part of the DC-link current control structure is designed to democratically assign v^*_L to the CSR-stage or the DC/DC-stage according to the loss-optimal operating modes discussed in **Section 2.3**.

To do so, it is useful to define $v_{max} = P^*/i^*_{DC,2/3}$, i.e., v_{max} is the local average value of the CSR-stage's DC-side voltage v_{pn} that would result if $i_{DC} = i^*_{DC,2/3}$ as needed for 2/3-PWM. Note that v_{max} is thus time-varying, too, to deliver constant power.

If $V^*_{out} < v_{max}$, the CSR-stage alone can regulate the DC-link current and the DC/DC-stage should be clamped, i.e., permanently gating $T_{DC,hp}$ and $T_{DC,hn}$ on. A positive v^*_L can thus be realized by increasing the CSR-stage's DC-side voltage v_{pn}, i.e., a shortening of the zero states used in 3/3-PWM of the CSR-stage. Thus, a positive v^*_L should result in a reduced reference DC-link current $i^*_{DC,CSR}$ fed to the space-vector pulse-width modulator (SVPWM)

of the CSR-stage. Following the control diagram and assuming that v_{L}^* is comparably small, we have

$$i_{\mathrm{DC,CSR}}^* = \frac{P_{\mathrm{out}}^*}{\min(V_{\mathrm{out}}^* + v_{\mathrm{L}}^*, v_{\max})} = \frac{P_{\mathrm{out}}^*}{V_{\mathrm{out}}^* + v_{\mathrm{L}}^*}, \tag{2.9}$$

which results in the desired behavior. Likewise, a negative v_{L}^* results in an increase of $i_{\mathrm{DC,CSR}}^*$ and hence in an elongation of the zero vector dwell times. The DC/DC-stage modulation index d^* is calculated as

$$d^* = \frac{-\max(v_{\mathrm{L}}^* + V_{\mathrm{out}}^* - v_{\max}, 0) + V_{\mathrm{out}}^*}{V_{\mathrm{out}}^*} = \frac{0 + V_{\mathrm{out}}^*}{V_{\mathrm{out}}^*} = 1, \tag{2.10}$$

so that d^* is not affected by v_{L}^* and ensures that $\mathrm{T}_{\mathrm{DC,hp}}$ and $\mathrm{T}_{\mathrm{DC,hn}}$ are turned on continuously.

If, conversely, $V_{\mathrm{out}}^* > v_{\max}$, only the DC/DC-stage can regulate the DC-link current since the CSR-stage operates with 2/3-PWM, i.e., no zero switching states and, thus, no voltage regulation capability. A positive v_{L}^* can then be realized by decreasing the input voltage v_{qr} of the DC/DC-stage. Therefore, the DC/DC-stage modulation index d^* is modified by v_{L}^* (which, again, is assumed to be comparably small) as

$$d^* = \frac{-\max(v_{\mathrm{L}}^* + V_{\mathrm{out}}^* - v_{\max}, 0) + V_{\mathrm{out}}^*}{V_{\mathrm{out}}^*} = \frac{v_{\max} - v_{\mathrm{L}}^*}{V_{\mathrm{out}}^*}. \tag{2.11}$$

On the other hand,

$$i_{\mathrm{DC,CSR}}^* = \frac{P_{\mathrm{out}}^*}{\min(V_{\mathrm{out}}^* + v_{\mathrm{L}}^*, v_{\max})} = \frac{P_{\mathrm{out}}^*}{v_{\max}} = i_{\mathrm{DC},2/3}^* \tag{2.12}$$

results, which ensures 2/3-PWM operation of the CSR-stage.

Note that in the transition-mode, therefore i_{DC} is regulated alternatively by the CSR-stage or by the DC/DC-stage, i.e., v_{L}^* is realized by either (modified) 3/3-PWM of the CSR-stage as in (2.9) or by (modified) DC/DC-stage duty cycles as in (2.11). Importantly, there are no abrupt changes in v_{L}^* but only different converter stages realize the required v_{L}^* depending on the (instantaneous) relation of V_{out}^* and $v_{\max}$. Advantageously, the loop gain of the DC-link current control is not affected, and seamless transitions between different operating points are achieved.

2.5 Experimental Verification

A 10 kW hardware demonstrator (see **Fig. 2.8**) has been built to experimentally verify the proposed synergetic control structure and to comprehensively characterize the conducted EMI performance and efficiency behavior over the wide output voltage and power ranges. Detailed modeling of component losses and volumes, a corresponding Pareto optimization (considering efficiency and power density), and finally a selected design have been presented earlier in [93, 94], considering a compact two-stage EMI filter providing sufficient attenuation, i.e., the maximum required attenuation over the wide output voltage range, to meet the requirements of CISPR 11 / class A. Thus, design details are not reiterated here for the sake of brevity. **Tab. 2.1** summarizes the key components of the realized demonstrator.[7]

Fig. 2.8 shows an exploded-view 3D CAD rendering and a photo of the 10 kW hardware demonstrator with outer dimensions of $184 \times 172 \times 49\,\mathrm{mm}^3$ ($9.8 \times 5.1 \times 1.9\,\mathrm{in}^3$) and thus a power density of $6.4\,\mathrm{kW/dm}^3$ ($107.5\,\mathrm{W/in}^3$). The CSR-stage employs inverse-series connections of 1200 V SiC MOSFETs for each bidirectional switch and the 3-L DC/DC-stage uses 900 V SiC MOSFETs. The realized demonstrator is composed of three separate PCBs: the control PCB (Zynq 7000 SoC, gate drivers, measurement data acquisition, etc.), the power PCB (carrying the power transistors, AC-side and DC-side capacitors, etc.), and a dedicated EMI filter PCB.

2.5.1 Experimental Waveforms

Characteristic waveforms of the 10 kW hardware demonstrator are presented in **Fig. 2.9** for operation in **(a)** buck-mode, **(b)** transition-mode, and **(c)** boost-mode. The phase *a* voltage v_a, the phase *a* current i_a, the DC-link current i_DC, and the output voltage V_out illustrate the desired behavior at the AC input and the DC output. Furthermore, the switched voltage v_pn at the output of the CSR-stage clearly indicates the CSR-stage operation with 2/3-PWM or 3/3-PWM. Similarly, the switched voltages v_qm and v_mr indicate whether the DC/DC-stage operates or is clamped. The measured CM capacitor voltage v_mk, mainly consisting of LF components, verifies the function of the integrated CM filter, i.e., suppressing the HF CM noise at the DC output. Note the close similarity of the measured waveforms to the simulation results shown in **Fig. 2.6**.

[7] Minor differences with respect to the selected design from [93] are due to mechanical/availability considerations. The loss calculations shown in the following employ the loss models from [93] but, of course, consider the actual components' data.

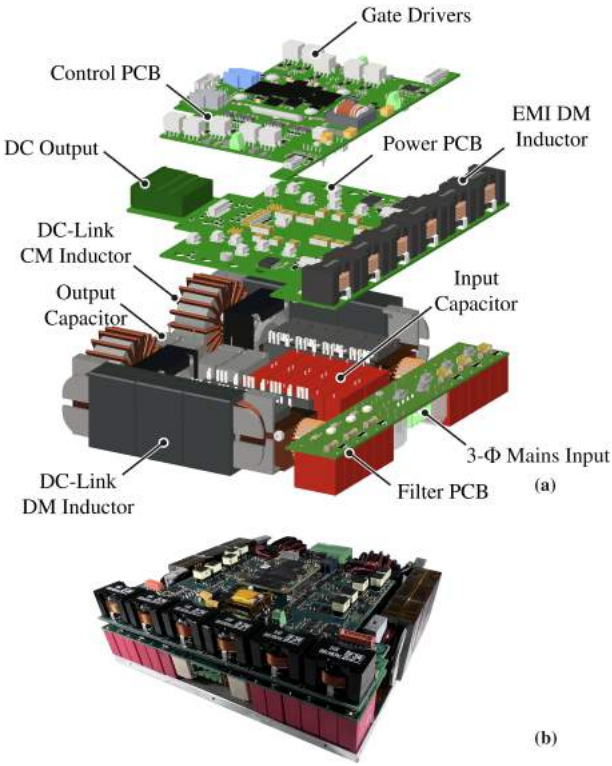

Fig. 2.8: (a) Exploded view of the 10 kW 3-Φ bB current DC-link PFC rectifier hardware demonstrator (see **Fig. 2.2** for the schematics and **Tab. 2.1** for key components) and **(b)** photo of the realized prototype. The dimensions are 184×172×49 mm^3 (9.8×5.1×1.9 in^3), resulting in a power density of 6.4 kW/dm^3 (107.5 W/in^3). Operating from the 400 V 3-Φ mains and employing 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) power MOSFETs, a wide output voltage range of 200 V to 1000 V is covered.

Specifically, **Fig. 2.9a** presents buck-mode operation with $V_{out} = 400\,V$, $P_{out} = 10\,kW$, where the CSR-stage operates with 3/3-PWM and the DC/DC-stage clamps, i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on as visible from v_{qm} and v_{mr}. **Fig. 2.9c** shows boost-mode operation with $V_{out} = 1000\,V$, $P_{out} = 10\,kW$, where the DC-link current i_{DC} is regulated into the six-pulse shape, i.e., the envelope of the phase current absolute values, needed for 2/3-PWM of the CSR-stage, i.e., v_{pn} never attains zero volt (freewheeling states are not

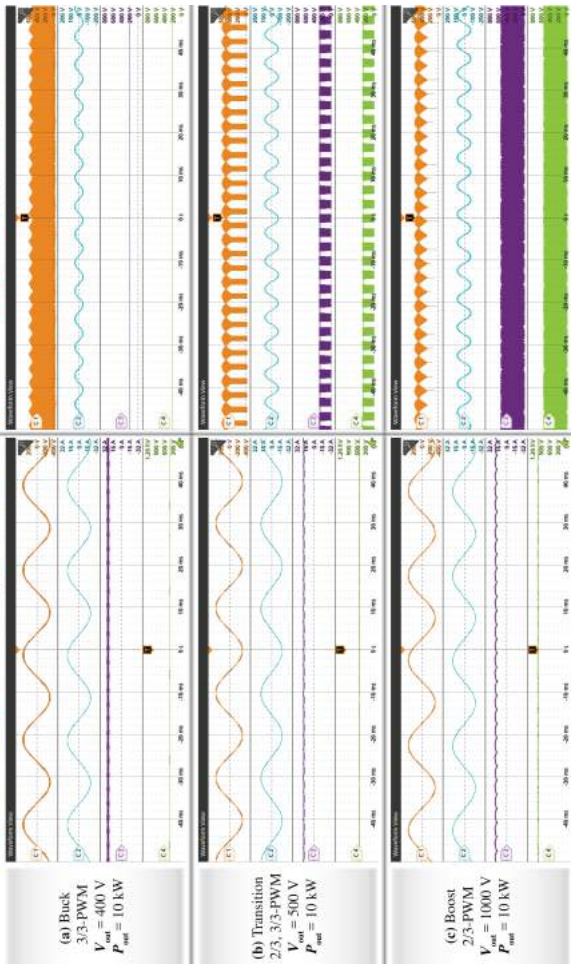

Fig. 2.9: Experimental waveforms of the converter shown in **Fig. 2.8**, operating with the proposed synergetic control strategy. **(a)** Buck-mode, where the CSR-stage uses 3/3-PWM to step down the mains voltage to the low output voltage and the DC/DC-stage is clamped (note that v_{qm} and v_{mr} are constant). **(b)** Transition-mode, where the CSR-stage changes between 3/3-PWM and 2/3-PWM, and the DC/DC-stage is democratically activated only when the boost functionality is required. **(c)** Boost-mode, where the DC/DC-stage regulates the DC-link current i_{DC} to the six-pulse shape needed for 2/3-PWM of the CSR-stage (note the absence of the zero level in v_{pn}).

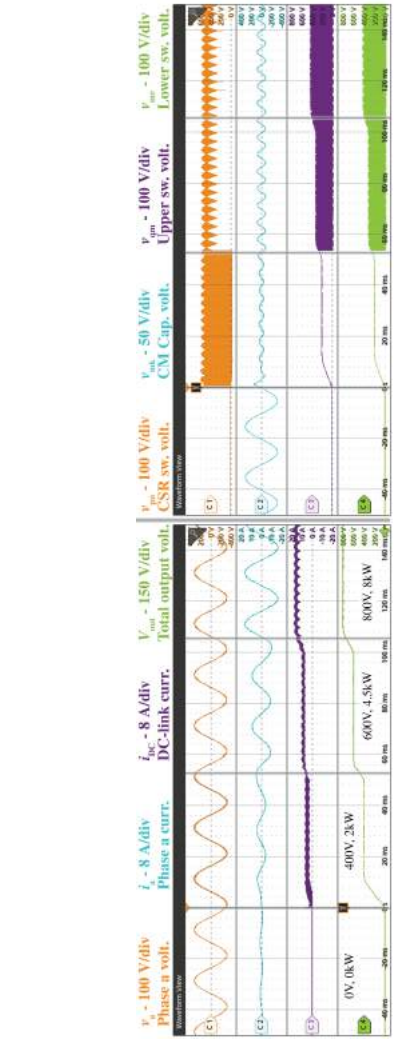

Fig. 2.10: Experimental waveforms of the converter shown in **Fig. 2.8** when supplying a resistive load of 80 Ω and the output voltage set point is changed from 0 V to 800 V, i.e., covering a wide output voltage range. Automatic and seamless transitions from buck-mode to boost-mode are achieved by the proposed synergetic control strategy (see **Fig. 2.7**). Note also the very smooth start-up.

employed), resulting in reduced switching losses of the CSR-stage. However, the DC/DC-stage has to regulate the DC-link current in the boost-mode and to control the output voltage at the same time. In the transition-mode operation, the CSR-stage alternatively operates with 2/3-PWM and 3/3-PWM and the DC/DC-stage is democratically activated to shape the DC-link current if needed; this ensures loss-optimal operation.

The proposed control strategy is thoroughly verified by the measurements shown in **Fig. 2.10**, where the output voltage steps up from 0 V to 800 V with a load resistance of 80 Ω. Automatic and smooth transitions between the different operating modes, i.e., buck-mode, transition-mode, and boost-mode, are achieved, and the loss-optimum modulation (i.e., 2/3-PWM of the CSR-stage if possible; clamped DC/DC-stage otherwise) employed. Note further the smooth start-up, which the current DC-link topology achieves without the need for pre-charging a DC-link capacitor (via pre-charge resistors) as is the case for voltage DC-link converters.

2.5.2 Efficiency Measurements

The efficiency of the 10 kW hardware demonstrator shown in **Fig. 2.8** is measured (Yokogawa WT3000) over the full wide output voltage range (from 200 to 1000 V) and the output power (from full load down to 25 % load). Thus, **Fig. 2.11a** shows the measured efficiency results in dependence of the output voltage and the load, considering the loss-optimum operating mode for each operating point; **Fig. 2.11b** shows the same information in a 2D contour plot, where in addition the operating points at which the efficiency measurements have been taken are indicated (linear interpolation is used in-between). Clearly, the converter features a relatively flat characteristic over the full operating area. High efficiencies, i.e., above 98%, are achieved for a large part of the operating range, i.e., in most of the operating range with output voltages above 400 V and more than 25% of rated load. To further illustrate this, **Fig. 2.12a** shows efficiency versus output voltage at rated power, and **Fig. 2.12b** shows efficiency versus output power for different output voltages. A peak efficiency of 98.8% at 520 V and 5 kW can be observed.

It is further worthwhile, for the first time, to experimentally quantify the system-level efficiency improvement when using 2/3-PWM instead of 3/3-PWM in the boost-mode and the transition-mode (note that the boost-type DC/DC stage sensibly *must* be clamped in the buck-mode). **Fig. 2.11c** shows the measured efficiency when operating with 3/3-PWM in those parts of the operating range where the loss-optimal operation would employ 2/3-PWM.

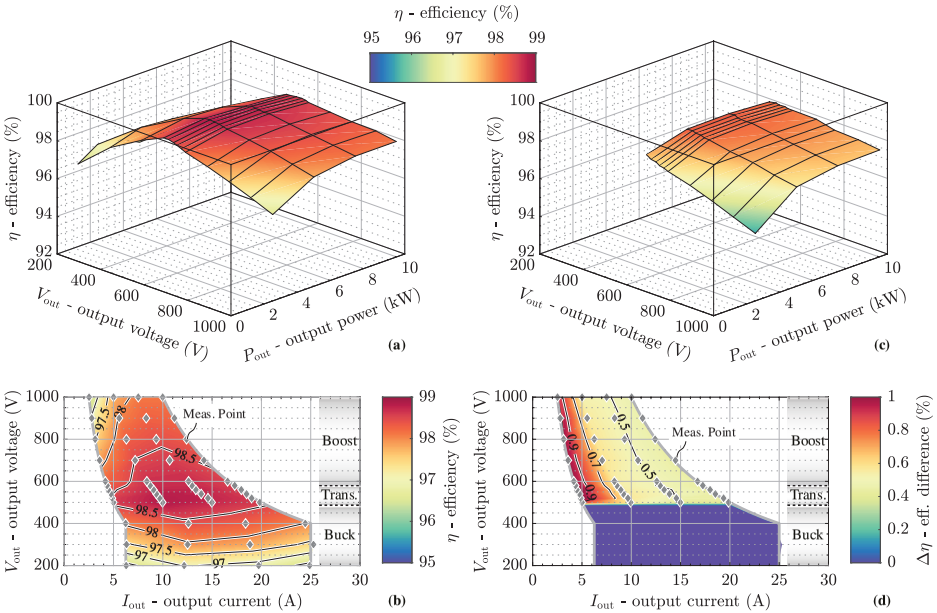

Fig. 2.11: Measured (Yokogawa WT3000) efficiencies of the realized 10 kW hardware demonstrator shown in **Fig. 2.8** when operating over a wide output voltage range (200 V to 1000 V) and output power range (from full load to 25 % load), using **(a)** the proposed loss-optimal modulation scheme with 2/3-PWM of the CSR-stage whenever possible; **(b)** shows the corresponding efficiency contours and indicates the measured operating points (linear interpolation in-between). **(c)** The measured efficiency when using 3/3-PWM instead of 2/3-PWM where applicable (i.e., in the boost-mode and the transition-mode), i.e., conventional operation. **(d)** The efficiency difference between **(a)** the proposed and **(c)** the state-of-the-art methods, highlighting up to 1% efficiency improvement in the transition-mode and the boost-mode. Note that no efficiency difference is expected in the buck-mode, where 3/3-PWM must be used in all cases. Thus, **(c)** does not show efficiencies for buck-mode operating points; the efficiency difference in this operating range is always zero (see **(d)**).

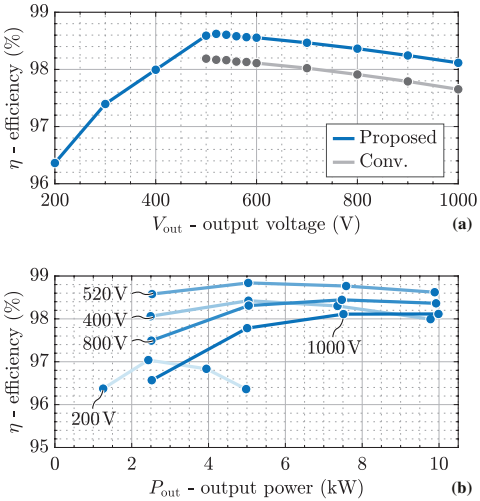

Fig. 2.12: Measured (Yokogawa WT3000) efficiency curves of the realized 10 kW hardware demonstrator shown in **Fig. 2.8**. **(a)** Efficiency versus output voltage V_{out} at rated power (or rated output current below 400 V, see **Fig. 2.1**), and **(b)** efficiency versus output power P_{out} (using the proposed loss-optimal modulation scheme). A peak efficiency of 98.8% when $V_{out} = 520$ V and $P_{out} = 5$ kW is achieved.

Fig. 2.11d then shows the efficiency improvements between the proposed loss-optimum operation (using 2/3-PWM whenever possible) and the conventional approach that does never employ 2/3-PWM, indicating improvements of up to 1% in the transition-mode and the boost-mode (again, no difference is expected in the buck-mode).

Finally, **Fig. 2.13** provides the calculated loss breakdowns versus **(a)** output voltage at rated power, **(b)** output power at 400 V (buck-mode), and **(c)** output power at 800 V (boost-mode). The loss modeling has been presented earlier [93], but the calculation results shown here have been updated to reflect the components actually used in the demonstrator (see **Tab. 2.1**). Moreover, the loss breakdowns provide the following observations:

- Conduction losses account for a significant proportion of the total losses. As these reduce with the square of the current (and accordingly with the power), a relatively flat efficiency characteristic of the converter results.

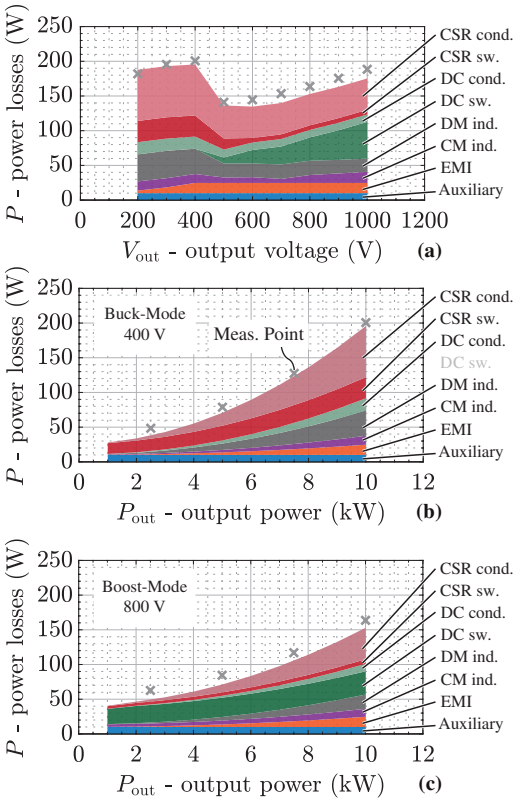

Fig. 2.13: Calculated loss breakdowns of the converter shown in **Fig. 2.8** and loss-optimal operation, in **(a)** for different output voltages V_{out} and rated power (or rated output current below 400 V), in **(b)** for buck-mode operation (V_{out} = 400 V) and varying power P_{out}, and in **(c)** for boost-mode operation (V_{out} = 800 V) and varying power. The measured (Yokogawa WT3000) total losses are in excellent agreement with the calculations.

- In buck-mode, the CSR-stage operating with 3/3-PWM contributes considerable switching losses whereas the DC/DC-stage only generates conduction losses and zero switching losses due to clamping.

- In boost-mode, 2/3-PWM is used for the CSR-stage and leads to almost negligible switching losses. On the other hand, the DC/DC-stage gen-

erates comparably high switching losses because of the high switched voltage (boost-mode).

Fig. 2.13 also indicates the measured (Yokogawa WT3000) losses, and a very close match between calculation and measurement can be observed.

2.5.3 EMI Measurements

Conducted EMI pre-compliance tests have been carried out to assess the compliance of the realized 10 kW hardware demonstrator (see **Fig. 2.8**) with the limits set forth in CISPR 11 / Class A for the frequency range of 150 kHz to 30 MHz. The test setup consists of a Rhode & Schwarz ESH2-Z5 three-phase LISN and a Rhode & Schwarz ESPI3 EMI test receiver.

First, the differences in the conducted EMI emission characteristics when operating with 2/3-PWM or, conventionally, 3/3-PWM for boost-mode operating points are compared. **Fig. 2.14a** presents EMI measurement results when operating in the boost-mode ($V_{\text{out}} = 800\,\text{V}$, $P_{\text{out}} = 10\,\text{kW}$) with the two different modulation schemes used in the CSR-stage. In general, 2/3-PWM results in lower noise levels, with a maximum reduction of 9.7 dBμV at 2.4 MHz. This can be explained by the difference between DM/CM noise sources: **Fig. 2.15** first presents the HF DM/CM noise source waveforms generated by 2/3-PWM and 3/3-PWM, i.e., the switched current $i_{\text{a'}}$ (see **Fig. 2.2**), and the CSR-stage CM voltage $v_{\text{CM,CSR}} = (v_{\text{pk}} + v_{\text{nk}})/2$ (see [93] for a detailed analysis; note that the CM noise generated by the DC/DC-stage is neglected here since the focus is on comparing the EMI performances of different CSR-stage modulation schemes). To compare the required EMI filter efforts, the DM and CM voltage spectra that would be measured by a LISN in the absence of an EMI filter are provided. The DM noise source can thus be represented by the voltage that would appear at the LISN's 50 Ω measurement resistor if $i_{\text{a'}}$ would directly flow in this resistor. On the other hand, the CM voltage defined above is directly the relevant noise source if a comparably large parasitic capacitance of the converter's output to PE is assumed as a worst case. The thus calculated noise spectra (see **Fig. 2.15**) indicate that 2/3-PWM results in a reduction of the DM noise of up to 6 dBμV (at 500 kHz). Regarding the CM noise, the maximum reduction is similar, i.e., 6 dBμV $\sim$ 8 dBμV, but observed for (almost) all frequency components. Hence, it can be assumed that mainly the lower CM noise, which is a direct consequence of the CSR-stage not using zero states with 2/3-PWM [94], contributes to the overall lower noise emissions of the converter operating with 2/3-PWM compared to 3/3-PWM. This implies

further that a converter originally designed without considering 2/3-PWM can advantageously be operated with 2/3-PWM (by, essentially, only changing the control method) without the need for a redesign of the EMI filter.

Moreover, considering the loss-optimum operation, **Fig. 2.14b** shows conducted EMI noise emission measurements of the 10 kW demonstrator over the full output voltage range at rated power (note that the output current limit restricts the power to $P_{\text{out}} = 5\,\text{kW}$ for the operating point at $V_{\text{out}} = 200\,\text{V}$). Because the designed EMI filter (see **Tab. 2.1**) achieves similar DM and CM attenuation, e.g., roughly 110 dBμV at 200 kHz according to the detailed discussion in [93], and because of the higher DM noise emission levels for the exemplary operating point discussed in the context of **Fig. 2.15**, it is likely that the DM noise dominates in the measurement results, especially when the CSR-stage operates with high modulation indices. Thus, focusing on the measured noise at 200 kHz, i.e., the first harmonic of the switching frequency that lies inside of the regulated frequency range, it is observed that:

- Higher noise results for operating points in the buck-mode, e.g., $V_{\text{out}} = 200\,\text{V}$ or 400 V, than for operating points in the boost-mode, e.g., $V_{\text{out}} = 600\,\text{V}$, 800 V, or 1000 V, since a higher DC-link current, i.e., a constant DC-link current of 25 A in the buck-mode instead of a six-pulse-shaped DC-link current with a peak value of 20.5 A in the boost-mode, must be used.
- The worst case at 400 V is expected by comparing RMS values of the HF switched current $i_{\text{a'}}$, i.e., 10.5 A at 200 V, 10.8 A at 400 V, and 6.8 A at 800 V.
- Similar EMI noise spectra are measured for the three operating points in boost-mode since the CSR-stage operates identically with 2/3-PWM and thus with the same DC-link current. These results indicate that the DC/DC-stage does not strongly affect the AC-side EMI performance.

Finally, considering the worst-case operating point at $V_{\text{out}} = 400\,\text{V}$ and $P_{\text{out}} = 10\,\text{kW}$, **Fig. 2.14c** shows a screenshot of the EMI test receiver with a quasi-peak (QP) measurement result of 64.4 dBµV at 200 kHz, which indicates compliance with CISPR 1 / Class A.

2.6 Summary

Targeting advanced AC/DC front-end converters for EV charger applications, this chapter thoroughly studies and analyzes a three-phase (3-Φ) buck-boost

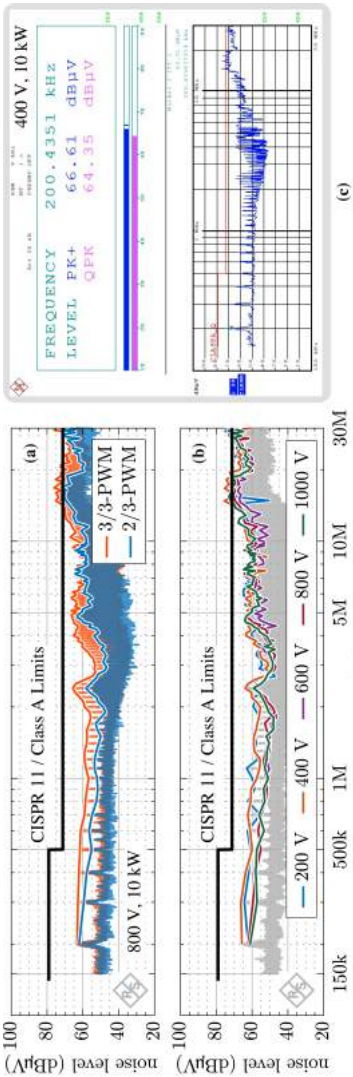

Fig. 2.14: Measured conducted EMI noise emission spectra of the realized 10 kW hardware demonstrator shown in **Fig. 2.8**. The Rhode & Schwarz ESPI$_3$ test receiver uses the CISPR 11 peak (PK) detector with resolution bandwidth of 9 kHz, 4 kHz step size, and 1 ms measurement time. The local peak values are connected by colored envelopes for easier comparisons between different operating points. **(a)** Comparison of the EMI noise emissions between 2/3-PWM and 3/3-PWM when operating in the boost-mode, i.e., at $V_{\text{out}} = 800\,\text{V}$, $P_{\text{out}} = 10\,\text{kW}$, indicating a maximum reduction of 9.7 dBμV at 2.4 MHz when using 2/3-PWM instead of 3/3-PWM. **(b)** Final conducted EMI pre-compliance test results of the demonstrator using the loss-optimum operating modes for each operating point (different output voltages, rated power); note that the minor violations of the CISPR 11 / Class A limit above 10 MHz could likely be avoided by placing the converter in a grounded housing. **(c)** Screenshot directly taken from the EMI test receiver at the worst-case operating point ($V_{\text{out}} = 400\,\text{V}$, $P_{\text{out}} = 10\,\text{kW}$), indicating a quasi-peak (QP) value of 64.4 dBμV at 200 kHz.

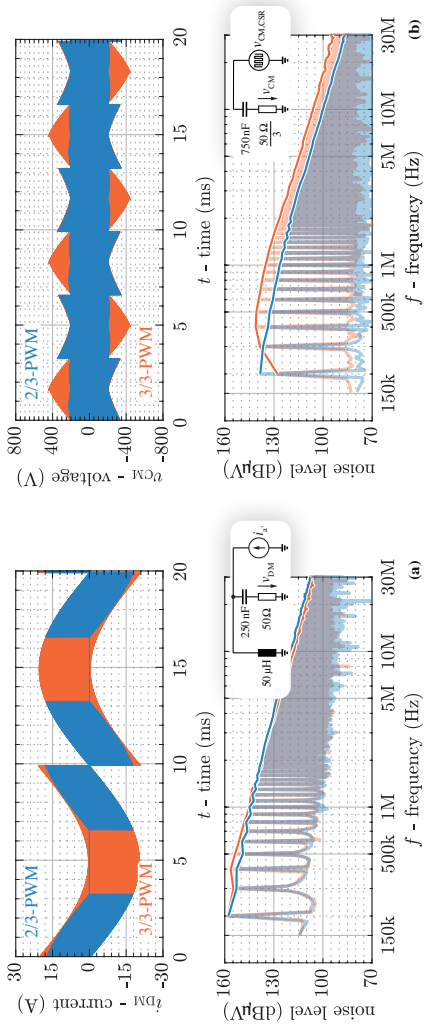

Fig. 2.15: Comparison of calculated HF **(a)** DM and **(b)** CM EMI noise waveforms and spectra (as they would appear at the LISN without an EMI filter present) for operation with 2/3-PWM **(blue)** or 3/3-PWM **(orange)** in the boost-mode at V_{out} = 800 V and P_{out} = 10 kW.

(bB) current DC-link PFC rectifier that consists of a 3-Φ buck-type current-source rectifier (CSR)-stage linked to a downstream 3-L boost-type DC/DC-stage via a shared DC-link inductor. An ultra-wide output voltage range, i.e., from 200 V to 1000 V, can be covered by three loss-optimal operating modes: in the buck-mode (for low output voltages), the CSR-stage operates with Reduced Common-Mode (RCM) 3/3-PWM and the DC/DC-stage is clamped to avoid switching losses; in the boost-mode (for high output voltages), the CSR-stage operates with 2/3-PWM, i.e., only two out of three phases switch within one switching period such that the CSR-stage bridge-legs switch less frequently, and advantageously only in those respective sectors of the main periods where the switching occurs at relatively low voltages and currents; at the same time, still sinusoidal grid currents are achieved by using the DC/DC-stage to shape the DC-link current to follow the typical six-pulse shape given by the maximum absolute values of the 3-Φ mains currents. Furthermore, a simple and intuitive synergetic control strategy is proposed to operate the CSR-stage and the DC/DC-stage collaboratively in the loss-optimum operating modes, and to achieve an automatic, seamless transition between these loss-optimal operating modes when the output voltage changes. In particular, this also ensures loss-optimum operation in the transition-mode (for output voltages between buck-mode and boost-mode), where the minimum possible DC-link current is always ensured and the system hence seamlessly and democratically transitions between 3/3-PWM and 2/3-PWM several times per mains period.

A compact 10 kW hardware demonstrator with a power density of 6.4 $\mathrm{kW/dm^3}$ (107.5 $\mathrm{W/in^3}$) is presented and used to verify, for the first time, the key functionality of the proposed synergetic control method. Then, comprehensive efficiency measurements over the full output voltage and output power range confirm a flat efficiency characteristic (higher than 98% for most operating points with output voltages above 400 V and more than 25% of rated load), and a peak efficiency of 98.8% at $V_{\mathrm{out}} = 520\,\mathrm{V}$ and $P_{\mathrm{out}} = 5\,\mathrm{kW}$ (partial load). These measurements agree closely with the calculation results. Again, for the first time, the efficiency improvement of 2/3-PWM over 3/3-PWM on the system-level, i.e., including a DC/DC-stage, is experimentally confirmed to be up to 1%. Finally, the conducted EMI pre-compliance tests reveal that, for a given operating point where both PWM schemes are applicable, 2/3-PWM results in lower noise emissions than 3/3-PWM. Using the loss-optimum operating modes, measurements taken over the full output voltage range and rated power indicate compliance with CISPR 11 / Class A limit concerning conducted emissions.

All in all, current DC-link buck-boost PFC rectifiers such as the system presented herein are promising realization options for future EV chargers that require a wide output voltage range, high efficiency, and compact size.

3

3-Φ Synergetically Controlled Current DC-Link AC/DC Buck-Boost Converter with Two Independently Regulated DC Outputs

Chapter Abstract

A three-phase current DC-link AC/DC buck-boost converter, composed of a three-phase current-source rectifier (CSR) front-end and a three-level DC/DC-stage, can provide two independently regulated DC outputs. A conventional synergetic control strategy, which coordinates the modulation of the CSR and the DC/DC converter stage to achieve minimum overall switching losses, is extended to the case of two independent DC outputs, retaining all advantageous features such as seamless transitions between operating modes and modulation schemes. The extended synergetic control strategy allows loss-optimum operation (i.e., reduced number of switching instants due to clamping of a phase of the CSR-stage (switching only two out of the three phases, i.e., 2/3-PWM) or individual clamping of the DC/DC-stage's two half-bridges, and minimum possible DC-link current) for any operating point, especially also for two *different* output voltages and/or two *different* loads. Finally, experimental confirmation of the proposed control scheme using a 10 kW demonstrator system is provided. Operating in the boost-mode at a total output voltage of 800 V, the proposed synergetic control achieves a significant measured efficiency improvement over a wide load range, e.g., from 95.7 % to 96.9 % (1.2 %) at 2 kW and from 97.9 % to 98.4 % (0.5 %) at 10 kW, which is largely independent of output voltage asymmetries and load asymmetries.

3.1 Introduction

The availability of two independently regulated DC outputs presents a considerable cost-saving potential for advanced three-phase (3-Φ) Power Factor Corrected (PFC) AC/DC converter systems that supply separate loads, e.g., high-power heaters for different process stages [113], or chargers of future high-voltage batteries for heavy-duty electric vehicles [10], which could advantageously be split into upper and lower halves [11]. Recently, research on fully controllable hybrid or monolithic bidirectional bipolar switches [84, 103] has triggered renewed interest in current DC-link systems [90, 97, 100, 101, 114]. Compared to conventional voltage DC-link boost-buck (Bb) rectifiers, 3-Φ current DC-link buck-boost (bB) rectifiers offer several advantages, i.e., most prominently a reduced number of magnetic components as the DC-link inductor employed in the front-end buck-type current-source rectifier (CSR) stage [89, 102, 115] is shared with the boost DC/DC output stage [116, 117] (see **Fig. 3.1a**, where a three-level (3-L) boost DC/DC-stage is used).

The 3-L boost DC/DC-stage inherently can provide two DC outputs. Thus, independent control of the two output voltages of a similar system has been analyzed in [113]. In general, the two partial output voltages $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$ can be controlled to equal or to different values, and at the same time the

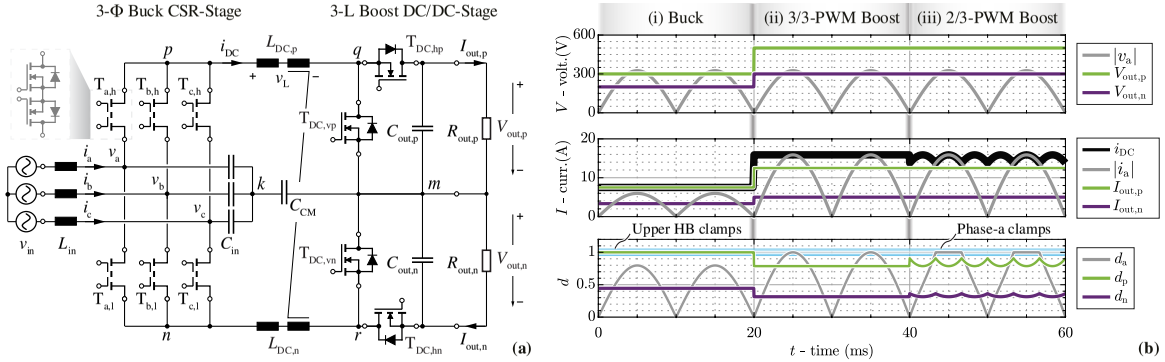

Fig. 3.1: (a) Circuit schematic of the considered 10 kW three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier system. The two DC output voltages, $V_{\text{out,p}}$ and $V_{\text{out,n}}$, are independently regulated to enable asymmetric loading capability. Circuit parameters are designed based on [93], i.e., switching frequencies $f_{\text{CSR}} = f_{\text{DC/DC}} = 100\,\text{kHz}$, DM DC-link inductor $L_{\text{DC,DM}} = 250\,\mu\text{H}$, input filter capacitor $C_{\text{in}} = 3 \times 6\,\mu\text{F}$, CM DC-link inductor $L_{\text{DC,CM}} = 11\,\text{mH}$, CM filter capacitor $C_{\text{CM}} = 88\,\text{nF}$, and output capacitor $C_{\text{out}} = 2 \times 11.2\,\mu\text{F}$. **(b)** Exemplary key waveforms for **(i)** operation in the buck-mode (identical for the conventional concept [113] and proposed concepts), **(ii)** conventional boost-mode with 3/3-PWM, and **(iii)** proposed boost-mode with 2/3-PWM where the DC/DC-stage controls the DC-link current to follow the six-pulse shape of the envelope of the phase current absolute values. Thus, at all times in boost-mode operation, only two out of the CSR-stage's three phases are operated with PWM while the third phase is clamped, which results in a considerable reduction of switching losses.

loads connected to either DC output can differ, i.e., $R_{\mathrm{out,p}} \neq R_{\mathrm{out,n}}$ is possible. However, the concept presented in [113] considers only conventional operation with a constant DC-link current i_{DC}, which must be selected at least as high as the mains phase current amplitudes such that the desired sinusoidal phase currents can be obtained by pulse-width modulated distribution of the constant DC-link current to the three phases. The CSR-stage thus operates with the so-called 3/3-PWM, i.e., all three phases of the CSR-stage are operated with PWM regardless of the operating mode (buck-mode if $V_{\mathrm{out,p}} + V_{\mathrm{out,n}} < {}^{3}/_{2}\hat{V}_{\mathrm{in}}$ or boost-mode if $V_{\mathrm{out,p}} + V_{\mathrm{out,n}} > \sqrt{3}\hat{V}_{\mathrm{in}}$, where $\hat{V}_{\mathrm{in}}$ denotes the grid phase voltage amplitude). Similarly, the two output DC currents, $I_{\mathrm{out,p}}$ and $I_{\mathrm{out,n}}$, are again obtained from the constant DC-link current by PWM operation of the two DC/DC-stage bridge-legs. Consequently, the constant DC-link current must also be at least as high as the higher of the two DC output currents and/or load currents. This is illustrated in **Fig. 3.1b.i** and **Fig. 3.1b.ii**, respectively.

In the buck-mode, the DC-link current is selected equal to the larger of the two output DC currents (i.e., $i_{\mathrm{DC}} = I_{\mathrm{out,p}}$ in the example shown in the figure) and hence the corresponding half-bridge (HB) of the DC/DC-stage can be clamped (i.e., operated with duty cycle $d_{\mathrm{p}} = 1$ and thus $\mathrm{T}_{\mathrm{DC,hp}}$ permanently turned on). On the other hand, the second HB of the DC/DC-stage operates with a duty cycle $d_{\mathrm{n}} < 1$ to reduce the DC-link current to the second, lower output current $I_{\mathrm{out,n}}$. Furthermore, as the DC-link current is larger than the peak phase current (only phase a is shown in the figure for better readability), the CSR-stage operates all three phases with PWM (i.e., with duty cycles $d_{\mathrm{a,b,c}} < 1$).

In the boost-mode, the DC-link current is still constant but the minimum required value is given by the amplitude of the phase currents and not by one of the two output currents, which are both lower than the DC-link current. Consequently, both HBs of the DC/DC-stage operate with $d_{\mathrm{p,n}} < 1$ to adapt the DC-link current to the respective output currents, $I_{\mathrm{out,p}}$ and $I_{\mathrm{out,n}}$. As the DC-link current is still constant, also all phases of the CSR-stage operate with PWM as in the buck-mode, i.e., with $d_{\mathrm{a,b,c}} < 1$ at all times, and hence with 3/3-PWM.

However, if a time-varying (i.e., not constant) DC-link current is accepted, this current only needs to be at least as high as the highest *instantaneous* value of the rectified three-phase input currents. A two-stage 3-Φ bB current DC-link PFC rectifier system can thus advantageously operate the CSR-stage with so-called 2/3-PWM [107, 109] in the boost-mode by using the DC/DC-stage to control the DC-link current into the six-pulse shape of the envelope of the

phase current absolute values. This is possible if the DC output current is lower than the minimum value of that envelope, i.e., if the converter operates in boost-mode. This then allows switching only two instead of three phases of the CSR-stage with a corresponding reduction in switching losses as illustrated in **Fig. 3.1b.iii**. Note that $d_a = 1$ for 1/3 of the grid period, i.e., the phase is clamped. Considering only a single load connected between the upper positive and the lower negative output terminals, a synergetic control concept that achieves 2/3-PWM whenever possible and ensures seamless transitions between the buck-mode (the CSR-stage operates with 3/3-PWM and regulates the DC-link current, while the switches $T_{DC,hp}$ and $T_{DC,hn}$ of the DC/DC-stage permanently conduct) and the boost-mode (the CSR-stage operates with 2/3-PWM, while the DC/DC-stage regulates the DC-link current along the above mentioned six-pulse shaped envelope) has been proposed in [95].

In this chapter, this synergetic and/or collaborative control concept is extended to the case with two fully independently controlled DC outputs. The control scheme (see **Fig. 3.2**, **Fig. 3.3** and the detailed description in **Section 3.3**) achieves loss-optimal operation of the converter system over a wide output voltage range, and still ensures seamless transitions between the different operating modes (i.e., buck- and boost-mode) and modulation schemes (i.e., 2/3-PWM and 3/3-PWM), considering especially also corner cases with zero loading of one output. Experimental results of a 10 kW demonstrator system confirm the proposed concept and reveal a considerable efficiency improvement over a wide load range, e.g., from 95.7 % to 96.9 % (1.2 %) at 2 kW and from 97.9 % to 98.4 % (0.5 %) at 10 kW with 800 V output voltage, also for boost-mode operation with unequal loads and with unequal output voltages.

3.2 Operating Modes with Independent Outputs

A 3-Φ bB current DC-link PFC rectifier system as shown in **Fig. 3.1a** with its two partial output voltages $V_{out,p}$ and $V_{out,n}$ utilized as a single output $V_{out} = V_{out,p} + V_{out,n}$ (connection of the load between the positive terminal of $V_{out,p}$ and the negative terminal of $V_{out,n}$) features only two main operating modes, i.e., buck-mode ($3/2\hat{V}_{in} > V_{out}$) and boost-mode ($\sqrt{3}\hat{V}_{in} < V_{out}$) as described in [95]. However, *four* main operating modes (see **Tab. 3.1**) must be distinguished in case of utilizing $V_{out,p}$ and $V_{out,n}$ as individual, independently regulated DC outputs.

Similar to the single-output case, operation in these modes should optimally feature reduced switching losses by using 2/3-PWM of the CSR-stage whenever possible, or, alternatively, clamping both, one or none of the 3L DC/DC-stage's HBs, depending on the load conditions. Furthermore, minimum overall conduction losses should be achieved by ensuring operation with the minimum possible DC-link current: The 3-Φ input currents and the two output DC currents are obtained by PWM-based reduction of the impressed DC-link current. Consequently, the DC-link current value has to be at least as high as the six-pulse time-varying upper envelope $i_{DC,2/3}$ of the instantaneous values of the rectified mains phase currents and at least as high as each of the two DC output currents. The minimum possible DC-link current at any given point in time is thus the maximum of these three currents, i.e., $i_{DC} = \max\{I_{out,p}, I_{out,n}, i_{DC,2/3}\}$, where $i_{DC,2/3}$ denotes the envelope of the absolute values of the 3-Φ mains currents (see also **Fig. 3.1b**) [95].

On the basis of the generic explanations given in the context of **Fig. 3.1b** and for the sake of brevity, the following description of the four operating modes (see **Tab. 3.1**) is directly illustrated by later experimental results of a 10 kW hardware demonstrator (see Fig. 3.4), which are in excellent agreement with simulation results (see Fig. 3.5 for buck-mode and Fig. 3.6 for boost-mode operation). **Section 3.3** addresses the challenge of finding a control system that operates the converter in the respective optimum mode for a given load condition and furthermore achieves seamless transitions between the modes when the operating point changes.

3.2.1 Buck-Mode

The converter operates in the buck-mode if $I_{out,max} = \max\{I_{out,p}, I_{out,n}\} > i_{DC,2/3}$ and hence the DC-link current is defined by $i_{DC} = I_{out,max}$. The CSR-

Tab. 3.1: Operating modes of the proposed synergetically controlled 3-Φ bB current DC-link PFC rectifier system with two independent DC outputs (for the definition of x_p^* and x_n^* see **Section 3.3**).

Mode	CSR-stage	DC/DC-stage	i_{DC}	x_p^*	x_n^*
Buck-I	3/3-PWM	No HB Sw.	I_{out}	0	0
Buck-II	3/3-PWM	1 HB Sw.	$I_{out,max}$	0 (1)	1 (0)
Boost-I	2/3-PWM	1 HB Sw.	$i_{DC,2/3}$	0 (1)	1 (0)
Boost-II	2/3-PWM	2 HBs Sw.	$i_{DC,2/3}$	α_p^*	α_n^*

stage then operates with conventional 3/3-PWM to step down the 3-Φ mains voltages to a lower DC output voltage (AC/DC voltage conversion of the CSR-stage and control of the DC-link current). Considering the DC/AC current conversion of the CSR-stage, 3/3-PWM sinusoidally distributes i_{DC} to the three mains phases. Because $i_{\mathrm{DC}} = I_{\mathrm{out,max}}$, advantageously at least one HB of the DC/DC-stage is clamped to reduce the switching losses.

Specifically, in the **Buck-I** mode, the output power is only delivered through one of the two outputs, e.g., the upper output (i.e., no load is present at the lower output, $I_{\mathrm{out,n}} = 0$) and the DC/DC-stage switching losses are avoided by ensuring $i_{\mathrm{DC}} = I_{\mathrm{out,p}}$ and permanently turning on $\mathrm{T}_{\mathrm{DC,hp}}$ and $\mathrm{T}_{\mathrm{DC,vn}}$, where the continuous on-state of $\mathrm{T}_{\mathrm{DC,vn}}$ prevents a current flow into $C_{\mathrm{out,n}}$.

In the **Buck-II** mode, both outputs deliver power to their respective (possibly different) loads at (in the general case) two independent voltages. If, e.g., $I_{\mathrm{out,n}} > I_{\mathrm{out,p}}$, the lower HB is clamped, i.e., $\mathrm{T}_{\mathrm{DC,hn}}$ is continuously turned on and i_{DC} is controlled to $I_{\mathrm{out,n}}$. However, switching of the upper HB is required to step down i_{DC} to $I_{\mathrm{out,p}}$ and, at the same time, this HB regulates i_{DC}. The CSR-stage modulates the thus externally impressed i_{DC} into sinusoidal 3-Φ input currents with 3/3-PWM as i_{DC} is constant. The modulation index M of the CSR-stage can then be calculated as

$$M = \frac{\hat{I}_{\mathrm{in}}}{i_{\mathrm{DC}}} = \frac{\bar{v}_{\mathrm{pn}}}{\frac{3}{2}\hat{V}_{\mathrm{in}}} = \frac{\bar{v}_{\mathrm{qr}}}{\frac{3}{2}\hat{V}_{\mathrm{in}}} = \frac{d_{\mathrm{p}} \cdot V_{\mathrm{out,p}} + V_{\mathrm{out,n}}}{\frac{3}{2}\hat{V}_{\mathrm{in}}}, \tag{3.1}$$

where $\hat{I}_{\mathrm{in}}$ denotes the grid phase current amplitude. Thus, the input power drawn from the mains through the CSR-stage is controlled indirectly by the upper HB duty cycle d_{p} which ultimately modifies the CSR-stage modulation index M.

3.2.2 Buck-Mode

The converter operates in the boost-mode if $I_{\mathrm{out,max}} < i_{\mathrm{DC},2/3}$ and $i_{\mathrm{DC}} = i_{\mathrm{DC},2/3}$, as shown in **Fig. 3.1b.iii**. The CSR-stage then operates with 2/3-PWM where no zero switching state is employed (v_{pn} never attains 0 V). To still obtain sinusoidal 3-Φ mains currents, at least one HB of the DC/DC-stage is required to regulate i_{DC} to follow the six-pulse shape $i_{\mathrm{DC},2/3}$ needed for 2/3-PWM.

Specifically, in the **Boost-I** mode, the output power is only delivered through one of the two outputs, e.g., the upper output, so that the upper HB switches to control the DC-link current.

Differently, both, the upper and the lower HBs are activated in the **Boost-II** operation and both outputs are loaded. The DC/DC-stage's two HBs are modulated such that they together control the DC-link current to the required six-pulse shape, while at the same time adapting this common DC-link current to the respective, possibly different output currents $I_{\mathrm{out,p}}$ and $I_{\mathrm{out,n}}$.

3.2.3 Hybrid-Mode

Furthermore, **hybrid** modes, i.e., combinations of the aforementioned buck- and boost-modes within one mains period, occur because of the time-varying characteristic of $i_{\mathrm{DC},2/3}$, which could be lower and higher than $I_{\mathrm{out,max}}$ over the course of one mains period; e.g., the converter operation could change between **Buck-II** mode (when $I_{\mathrm{out,max}} > i_{\mathrm{DC},2/3}$) and **Boost-II** ($I_{\mathrm{out,max}} < i_{\mathrm{DC},2/3}$) mode.

3.3 Synergetic Control Strategy

The proposed synergetic control strategy (see **Fig. 3.2**) ensures that the converter always operates in the optimum mode for a given operating point, i.e., with minimum possible losses, and transitions seamlessly between modes in case of changing operating points. As shown in **Fig. 3.2**, the control system consists of three functional blocks whose roles are explained in detail in the following subsections.

3.3.1 Independent Output Voltage Control

The two outermost control loops track the two output voltage references $V^*_{\mathrm{out,p}}$ and $V^*_{\mathrm{out,n}}$, respectively, by calculating the corresponding output power references $P^*_{\mathrm{out,p}}$ and $P^*_{\mathrm{out,n}}$. From that, the total power reference, i.e., the power that the CSR-stage must ultimately draw from the grid, $P^*_{\mathrm{out}} = P^*_{\mathrm{out,p}} + P^*_{\mathrm{out,n}}$, follows. Furthermore, it is convenient to define the corresponding power shares α^*_{p} and α^*_{n} as

$$\alpha^*_{\mathrm{p}} = \frac{P^*_{\mathrm{out,p}}}{P^*_{\mathrm{out}}} \quad \text{and} \quad \alpha^*_{\mathrm{n}} = \frac{P^*_{\mathrm{out,n}}}{P^*_{\mathrm{out}}} \tag{3.2}$$

for later use in the *DC-Link Current Control* block (see **Fig. 3.2**). Finally, the output current references, $I^*_{\mathrm{out,p}}$ and $I^*_{\mathrm{out,n}}$, are obtained and fed to the next functional block.

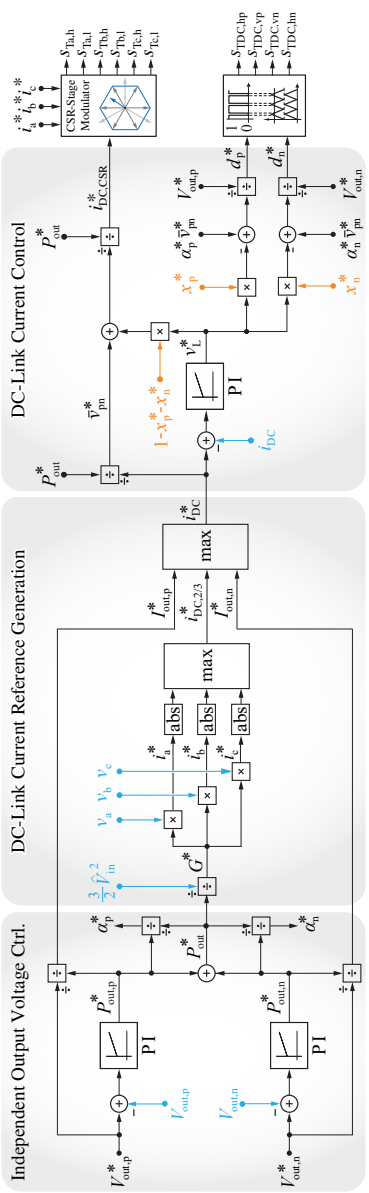

Fig. 3.2: Block diagram of the proposed synergetic control strategy for the 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 3.1**, which achieves fully independent regulation of the two DC output voltages, $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$, and optimum clamping of the CSR-stage and the two individual DC/DC-stage half-bridges (HBs).

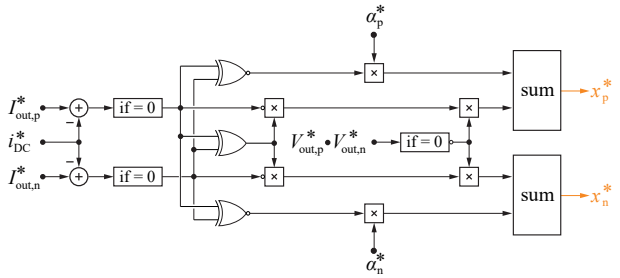

Fig. 3.3: Algorithm to calculate the distribution factors x_p^* and x_n^* (continuous values between 0 and 1) for the upper and lower DC/DC-stage HBs, respectively. Outputs are listed in **Tab. 3.1** for different operating modes.

3.3.2 DC-Link Current Reference Generation

First, a CSR-stage input reference conductance G^* is derived from the total power reference P_{out}^*. The 3-Φ sinusoidal mains current references i_a^*, i_b^*, and i_c^* that are proportional to the corresponding (measured) 3-Φ input voltages v_a, v_b, and v_c, i.e., ensure purely ohmic operation, directly follow. The envelope of the absolute 3-Φ sinusoidal mains current references defines the varying DC-link current reference $i_{DC,2/3}^*$ for 2/3-PWM operation.

As mentioned earlier, the minimal and thus optimal DC-link current value for a given operating condition is the maximum of the three possible reference values discussed so far, i.e., $i_{DC}^* = \max\{i_{DC,2/3}^*, I_{out,p}^*, I_{out,n}^*\}$. Thus, a DC-link current following the reference i_{DC}^* ensures minimized converter switching and conduction losses for any operating point, because (i) the DC-link current has the lowest possible value that is necessary to supply both outputs and to draw the total power from the grid, and (ii) because it facilitates clamping of one DC/DC-stage HB in buck-mode operation[1] and advantageous, in contrast to the state-of-the-art [113], operation of the CSR-stage with 2/3-PWM in the boost-mode[2].

[1] The HB corresponding to the output with the higher current can be clamped, as the DC-link current i_{DC} equals that output current.

[2] The DC-link current follows $i_{DC,2/3}^*$, i.e., it always equals the (absolute value of) one phase current, and thus the corresponding phase of the CSR-stage can be clamped.

3.3.3 DC-Link Current Control

The next functional block is the DC-link current controller that uses the CSR-stage and the two DC/DC-stage HBs to synergetically control the DC-link current to the aforementioned reference value i_{DC}^*. The required voltage v_{L}^* across the DC-link inductor L_{DC} is first calculated by comparing the reference i_{DC}^* and the measured DC-link current i_{DC}. The realization of this voltage is then synergetically assigned to either the CSR-stage or the DC/DC-stage, e.g., a positive v_{L}^* can be generated by either an increased output voltage v_{pn} of the CSR-stage or a decreased input voltage v_{qr} of the DC/DC-stage (see **Fig. 3.1a** for the definition of these voltages). Note that a feedforward of the local average voltage $\bar{v}_{\mathrm{pn}}^*$ at the CSR-stage's output can be obtained from the DC-link current reference i_{DC}^* and the total power (reference) P_{out}^*.

Different from the case with a single DC output [95], the synergetic generation of v_{L}^* now must consider two HBs of the DC/DC-stage individually. Thus, the two distribution factors x_{p}^* and x_{n}^* are introduced, whereby $x_{\mathrm{p}}^*, x_{\mathrm{n}}^* \in [0,1]$ and $0 \leq x_{\mathrm{p}}^* + x_{\mathrm{n}}^* \leq 1$. The distribution factors are determined from i_{DC}^*, $I_{\mathrm{out,p}}^*$ and $I_{\mathrm{out,n}}^*$ (i.e., from the operating point) as shown in **Fig. 3.3**. To better understand that flowchart and the role of the distribution factors, it is useful to consider the effect of x_{p}^* and x_{n}^* in the DC-link current controller from **Fig. 3.2** for the different operating modes:

For operating points in the **Buck-I** mode, we have $x_{\mathrm{p}}^* = x_{\mathrm{n}}^* = 0$ and consequently the entire v_{L}^* is added to $\bar{v}_{\mathrm{pn}}^*$. This modifies the reference DC-link current $i_{\mathrm{DC,CSR}}^*$ used in the space-vector pulse-width modulator (SVPWM) of the CSR-stage as

$$i_{\mathrm{DC,CSR}}^* = \frac{P_{\mathrm{out}}^*}{\bar{v}_{\mathrm{pn}}^* + (1 - x_{\mathrm{p}}^* - x_{\mathrm{n}}^*) \cdot v_{\mathrm{L}}^*}. \tag{3.3}$$

For $v_{\mathrm{L}}^* > 0$, a reduced $i_{\mathrm{DC,CSR}}^*$ leads to prolonged active switching states of the CSR-stage and thus realizes the desired increase of $\bar{v}_{\mathrm{pn}}$. Thus, only the CSR-stage regulates i_{DC} (to track, e.g., $i_{\mathrm{DC}}^* = I_{\mathrm{out,p}}^*$ if only the positive output port is activated) and the DC/DC-stage HBs can remain clamped (for the considered example, $d_{\mathrm{p}}^* = 1$ and $d_{\mathrm{n}}^* = 0$ follow from the control diagram[3]). This is clearly visible from the measured waveforms shown **Fig. 3.5.i** and

[3]For example, we find

$$d_{\mathrm{p}}^* = \frac{\alpha_{\mathrm{p}}^* \bar{v}_{\mathrm{pn}}^*}{V_{\mathrm{out,p}}^*} = \frac{P_{\mathrm{out,p}}^*}{P_{\mathrm{out}}^*} \cdot \frac{P_{\mathrm{out}}^*}{i_{\mathrm{DC}}^*} \cdot \frac{1}{V_{\mathrm{out,p}}^*} = \frac{P_{\mathrm{out,p}}^*}{I_{\mathrm{out,p}}^* V_{\mathrm{out,p}}^*} = 1$$

using the earlier definitions; $d_{\mathrm{n}}^* = 0$ follows likewise.

Fig. 3.5.iv, where 3/3-PWM operation of the CSR-stage can be recognized from v_{pn} attaining the zero voltage level, and where both DC/DC-stage HBs are not switching.

Differently, in **Buck-II** mode and assuming, as an example, $I^*_{\mathrm{out,p}} > I^*_{\mathrm{out,n}}$ and hence $i^*_{\mathrm{DC}} = I^*_{\mathrm{out,p}}$, we find $x^*_{\mathrm{p}} = 0$ and $x^*_{\mathrm{n}} = 1$. Thus, the CSR-stage has no need to participate in the generation of v^*_{L} and only the DC/DC-stage controls the DC-link current. The CSR-stage modulation index M can be calculated as in (3.1). As discussed above, the upper HB of the DC/DC-stage remains clamped as $x^*_{\mathrm{p}} = 0$ leads to $d^*_{\mathrm{p}} = 1$. In contrast, $x^*_{\mathrm{n}} = 1$ modifies the duty cycle d^*_{n} of the DC/DC-stage's lower HB such that its input voltage v_{mr} (see **Fig. 3.1a**) is decreased (again considering the example of realizing a $v^*_{\mathrm{L}} > 0$) accordingly. The distribution factors α^*_p and α^*_n adjust the ratio between v_{qm} and v_{mr} according to the two ports' output powers, and the two duty cycles are given by

$$d^*_{\mathrm{p}} = \frac{\alpha^*_{\mathrm{p}} \cdot \bar{v}^*_{\mathrm{pn}} - x^*_{\mathrm{p}} v^*_{\mathrm{L}}}{V^*_{\mathrm{out,p}}} \quad \text{and} \quad d^*_{\mathrm{n}} = \frac{\alpha^*_{\mathrm{n}} \cdot \bar{v}^*_{\mathrm{pn}} - x^*_{\mathrm{n}} v^*_{\mathrm{L}}}{V^*_{\mathrm{out,n}}}. \tag{3.4}$$

Fig. 3.5.ii illustrates that in the **Buck-II** mode the CSR-stage still operates with 3/3-PWM, and that always one of the two DC/DC-stage HBs is switching while the other is clamped.

In the boost-modes, $x^*_{\mathrm{p}} = \alpha^*_{\mathrm{p}}$ and $x^*_{\mathrm{n}} = \alpha^*_{\mathrm{n}}$ are obtained according to **Tab. 3.1**. Since, by the definition in (3.2), $\alpha^*_{\mathrm{p}} + \alpha^*_{\mathrm{n}} = 1$, only the DC/DC-stage HBs are used to control the DC-link current i_{DC} to the six-pulse shape $i^*_{\mathrm{DC,2/3}}$ that enables the CSR-stage to advantageously operate with 2/3-PWM, i.e., the proposed synergetic control concept automatically ensures that once possible (once the system operates in the boost mode) 2/3-PWM operation of the CSR-stage is achieved. In general, if both outputs are loaded, the v^*_{L} required by the DC-link current controller is distributed between the two HBs of the DC/DC-stage according to the power ratio (note that v^*_{L} is scaled with x^*_{p} and x^*_{n} in (3.4), respectively, before it is used to modify the duty cycles d^*_{p} and d^*_{n}, respectively, and $x^*_{\mathrm{p}} = \alpha^*_{\mathrm{p}}$, $x^*_{\mathrm{n}} = \alpha^*_{\mathrm{n}}$), i.e., both HBs are switching when operating in the **Boost-II** mode. **Fig. 3.6.iii** clearly proves that the CSR-stage operates with 2/3-PWM as v_{pn} does not attain the zero voltage level.

If only one output delivers power at a high-enough voltage, the converter operates in **Boost-I** mode, which can be considered a special case with, e.g., $\alpha^*_{\mathrm{p}} = 1$ and $\alpha^*_{\mathrm{n}} = 0$ if only the upper DC output delivers power.

Importantly, the inner DC-link current control loop gain is not affected by the seamless transitions between the modes, i.e., there are no abrupt changes in v^*_{L} but only different stages/HBs realize the required v^*_{L} at different

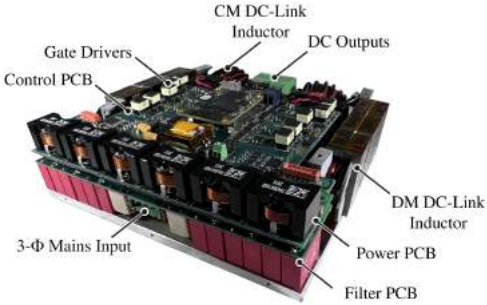

Fig. 3.4: 10 kW hardware demonstrator ($184 \times 172 \times 49\,\mathrm{mm}^3$, $6.4\,\mathrm{kW/dm}^3$, $9.8 \times 5.1 \times 1.9\,\mathrm{in}^3$, $107.5\,\mathrm{W/in}^3$) of the system shown in **Fig. 3.1** operating from the 400 V 3-Φ mains. 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs are employed. Both DC outputs can operate independently, whereby the maximum output voltages are limited to 600 V (in order not to exceed 2/3 of the 900 V rated blocking capability of the DC/DC-stage power semiconductors) and the maximum output currents are limited to 25 A (DC-link design current). Circuit parameters are specified in **Fig. 3.1**.

operating modes. This ensures a resilient and robust DC-link current tracking capability, especially in the **hybrid** operating modes, where the system may transition between buck and boost modes several times during a grid period.

3.4 Measured Efficiency Improvement

As outlined above, whereas in buck-mode the system behaves in the same way as a conventional realization [113], the proposed synergetic control concept promises significant loss reductions in boost-mode operation compared to the state-of-the-art [113], which would maintain a constant DC-link current and 3/3-PWM even though the DC/DC-stage, which needs to operate anyway to step-up the CSR-stage output voltage and/or step-down the DC-link current, could be utilized to shape the DC-link current into the six-pulse shape that would facilitate 2/3-PWM operation of the CSR-stage. **Fig. 3.7** quantifies the efficiency improvements obtained when operating the 10 kW hardware demonstrator (see **Fig. 3.4**) at different boost operating modes with either the conventional approach (i.e., 3/3-PWM) or the proposed synergetic control concept (i.e., 2/3-PWM). All efficiencies have been measured with a Yokogawa WT3000 power analyzer and for a total output voltage of $V_{\mathrm{out,p}}+V_{\mathrm{out,n}} = 800\,\mathrm{V}$.

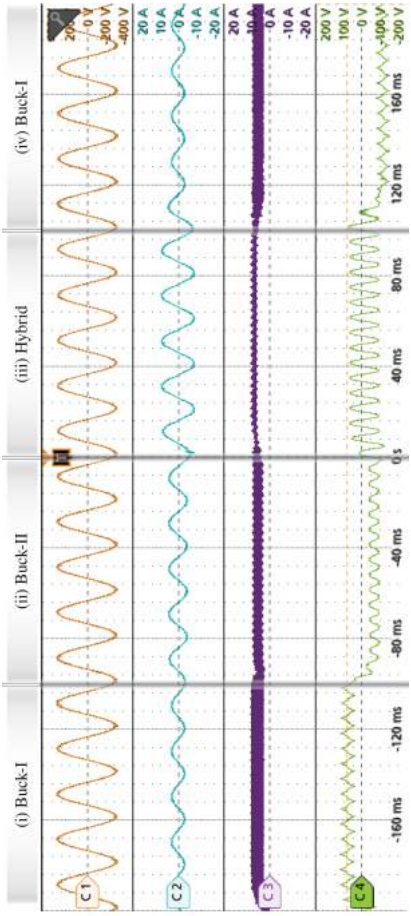

Fig. 3.5: Experimental waveforms of the converter shown in **Fig. 3.1a** with the proposed synergetic control operating in the two buck-modes with a load resistance of $R_p = 30\ \Omega$ at the upper and of $R_n = 40\ \Omega$ at the lower DC output, for different set points of the two output voltages $V_{out,p}$ and $V_{out,n}$. Note that for unequal DC output voltages a corresponding offset appears in the voltage v_{mk} across the CM filter capacitor C_{CM} in addition to the third-harmonic voltage component (due to the low capacitance $C_{CM} = 88$ nF, the resulting low-frequency current flow is negligible, however). Note further the smooth and seamless transitions between different operating modes and modulation schemes.

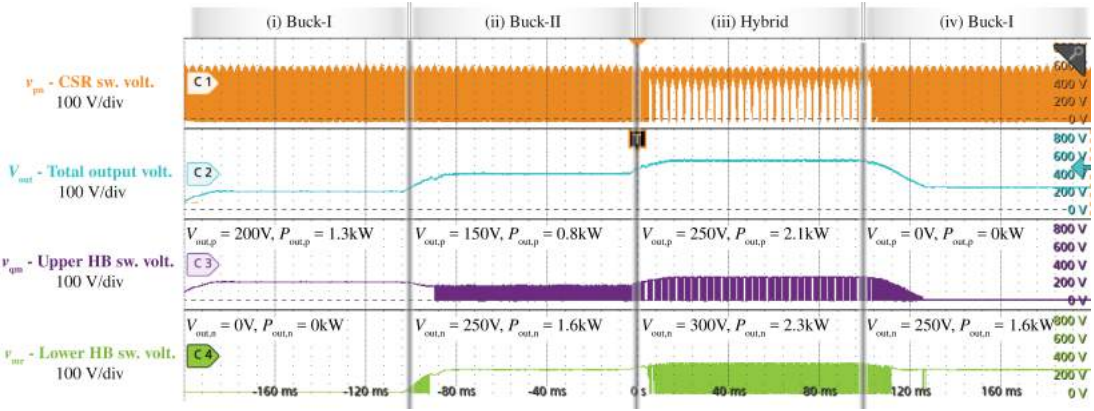

Fig. 3.5 (Continued): Experimental waveforms of the converter shown in **Fig. 3.1a** with the proposed synergetic control operating in the two buck-modes with a load resistance of $R_p = 30\,\Omega$ at the upper and of $R_n = 40\,\Omega$ at the lower DC output, for different set points of the two output voltages $V_{out,p}$ and $V_{out,n}$. Note that for unequal DC output voltages a corresponding offset appears in the voltage v_{mk} across the CM filter capacitor C_{CM} in addition to the third-harmonic voltage component (due to the low capacitance $C_{CM} = 88\,nF$, the resulting low-frequency current flow is negligible, however). Note further the smooth and seamless transitions between different operating modes and modulation schemes.

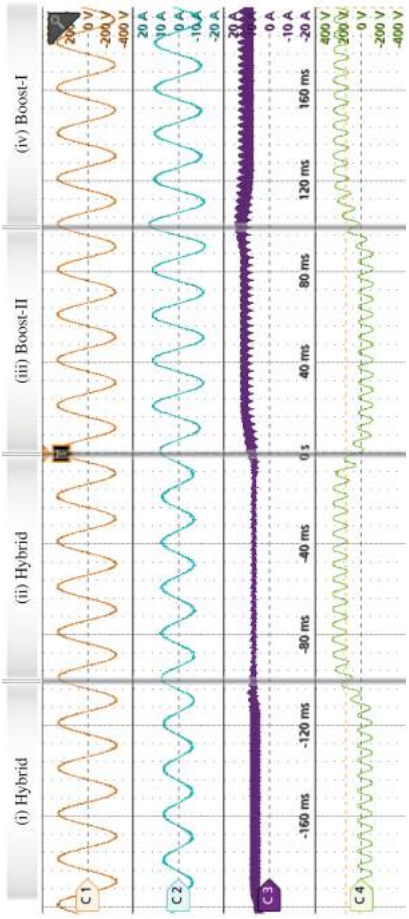

Fig. 3.6: Experimental waveforms of the converter shown in **Fig. 3.1a** with the proposed synergetic control operating in the two boost-modes with a load resistance of $R_p = 60\ \Omega$ at the upper and of $R_n = 40\ \Omega$ at the lower DC output. Note the absence of zero states in v_{pn} when the CSR-stage operates with 2/3-PWM. Note further that for unequal DC output voltages a corresponding offset appears in the voltage v_{mk} across the CM filter capacitor C_{CM} in addition to the third-harmonic voltage component (due to the low capacitance $C_{CM} = 88$ nF, the resulting low-frequency current flow is negligible, however). Note again (cf. **Fig. 3.5**) the smooth and seamless transitions between different operating modes and modulation schemes.

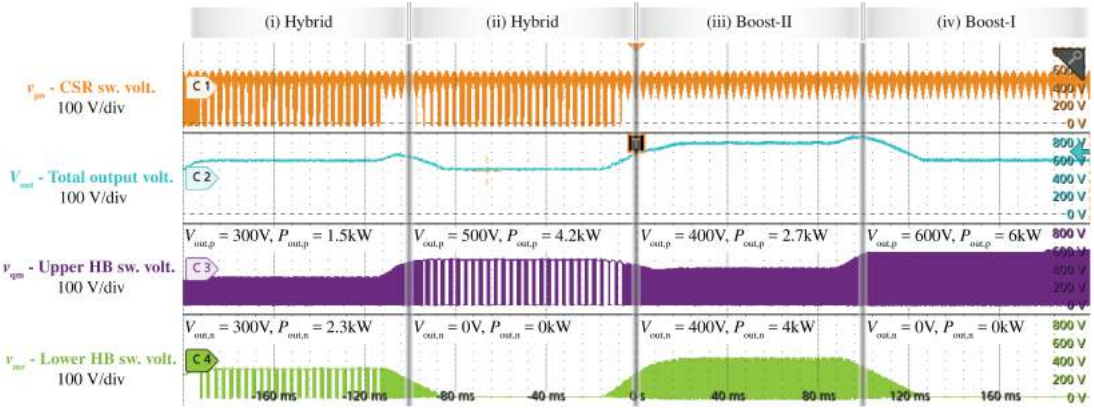

Fig. 3.6 (Continued): Experimental waveforms of the converter shown in **Fig. 3.1a** with the proposed synergetic control operating in the two boost-modes with a load resistance of $R_p = 60\ \Omega$ at the upper and of $R_n = 40\ \Omega$ at the lower DC output. Note the absence of zero states in v_{pn} when the CSR-stage operates with 2/3-PWM. Note further that for unequal DC output voltages a corresponding offset appears in the voltage v_{mk} across the CM filter capacitor C_{CM} in addition to the third-harmonic voltage component (due to the low capacitance $C_{CM} = 88$ nF, the resulting low-frequency current flow is negligible, however). Note again (cf. **Fig. 3.5**) the smooth and seamless transitions between different operating modes and modulation schemes.

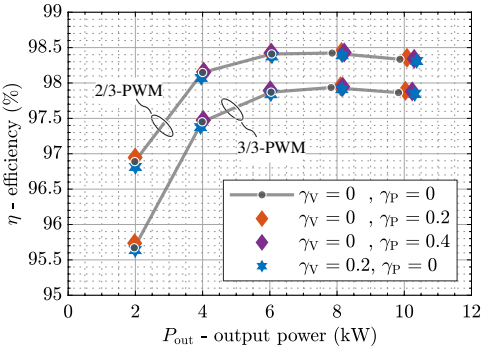

Fig. 3.7: Measured (Yokogawa WT3000) efficiencies of the 10 kW hardware demonstrator (see **Fig. 3.4**) in boost-mode operation ($V_{\text{out,p}} + V_{\text{out,n}} = 800\,\text{V}$) using the conventional approach with 3/3-PWM and the proposed synergetic control concept that facilitates 2/3-PWM of the CSR-stage. There is little impact of unequal output voltages ($\gamma_V \neq 0$) or of unequal loads ($\gamma_P \neq 0$). The total output power P_{out} is defined as $P_{\text{out}} = P_{\text{out,p}} + P_{\text{out,n}}$.

As a baseline, symmetric conditions are considered, i.e., equal output voltages $V_{\text{out,p}} = V_{\text{out,n}}$ and hence

$$\gamma_V = (V_{\text{out,p}} - V_{\text{out,n}})/(V_{\text{out,p}} + V_{\text{out,n}}) = 0; \tag{3.5}$$

as well as equal loads $P_{\text{out,p}} = P_{\text{out,n}}$ and hence

$$\gamma_P = (P_{\text{out,p}} - P_{\text{out,n}})/(P_{\text{out,p}} + P_{\text{out,n}}) = 0. \tag{3.6}$$

For this case, an efficiency improvement of more than 0.5 % is found over a wide load range (e.g., from 95.7 % to 96.9 % at 2 kW and from 97.9 % to 98.4 % at 10 kW). Then, two cases with equal voltages ($\gamma_V = 0$) but asymmetric loads ($\gamma_P = 0.2$, i.e., a 60 % : 40 % split of the total output power $P_{\text{out}} = P_{\text{out,p}} + P_{\text{out,n}}$, and $\gamma_P = 0.4$, i.e., a 70 % : 30 % split) show almost exactly the same efficiencies and especially efficiency improvements between the conventional and the proposed control methods. This is expected because the operating conditions of the CSR-stage do not change, and even though the conduction times of the DC/DC-stage's switches change, the total generated conduction and switching losses of the DC/DC-stage remain the same. Finally, a case with equal load powers ($\gamma_P = 0$) but asymmetric output voltages ($\gamma_V = 0.2$, i.e., $V_{\text{out,p}} = 480\,\text{V}$ and $V_{\text{out,p}} = 320\,\text{V}$) also shows very similar efficiency improvements; a partially slight reduction can be attributed to the higher

switched voltage of one DC/DC-stage HB. These measurements thus confirm (i) a significant efficiency improvement in the boost-mode and (ii) that this efficiency improvement is rather independent of the asymmetries of the output voltages and the two loads.

3.5 Summary

In this chapter, a synergetic control concept for a three-phase (3-Φ) buck-boost (bB) current DC-link AC/DC converter featuring two independently regulated DC outputs is proposed. The control scheme achieves a synergetic and/or collaborative operation of the 3-Φ buck-type CSR-stage and the two half-bridges (HBs) of the boost-type DC/DC-stage with minimum losses for any operating point (2/3-PWM of the CSR-stage or clamping of DC/DC converter HBs, and minimum possible DC-link current). Furthermore, seamless transitions between the different optimal operating modes and modulation schemes are ensured.

All features are experimentally verified with a 10 kW hardware demonstrator system over a wide output voltage range, i.e., a total output voltage of 200 V to 800 V and individual port voltages of up to 600 V. Efficiency measurements show a significant improvement over a wide load range, e.g., from 95.7 % to 96.9 % (1.2 %) at 2 kW and from 97.9 % to 98.4 % (0.5 %) at 10 kW, compared to the state-of-the-art methods when operating in the boost mode. This improvement is largely independent of output voltage asymmetries and/or load asymmetries.

4

Non-Isolated 3-Φ Current DC-Link Buck-Boost EV Charger with Virtual Output Midpoint Grounding and Ground Current Control

Chapter Abstract

Non-isolated three-phase AC/DC converter concepts facilitate more compact and more efficient realizations of future EV chargers. However, without the galvanic isolation and/or high common-mode (CM) impedance provided by an isolation transformer, non-isolated chargers must employ other means to suppress CM leakage currents to ground sufficiently and to prevent nuisance tripping of (mandatory) residual current devices (RCDs). Typically, the required EMI filters reduce high-frequency (HF) CM leakage currents to uncritical values. However, low-frequency CM voltages as, e.g., generated by third-harmonic injection modulation, may drive significant LF CM currents through the parasitic capacitances of the DC output (including the battery pack) to protective earth (PE). Therefore, considering a non-isolated three-phase buck-boost current DC-link PFC rectifier system that consists of a buck-type current-source rectifier (CSR) stage and a three-level boost-type DC/DC-stage, this chapter first proposes a virtual grounding control (VGC) of the DC output voltage midpoint. VGC employs the DC/DC-stage to compensate the LF (third-harmonic) CM voltage inherently generated by the CSR-stage, and thus controls the LF CM voltage between the DC output and PE to zero. This enables further a direct connection of the DC output midpoint to PE, where an additionally proposed ground current control (GCC) ensures near-zero LF CM leakage current. The proposed concepts are verified with a 10 kW hardware demonstrator (power density of 6.4 kW/dm³ or 107.5 W/in³, full-load peak efficiency of 98.5%) considering TT (Terra-Terra) and TN (Terra-Neutral) grounding systems. With a direct connection of the DC output midpoint to PE, GCC limits the LF CM leakage current to < 6 mA RMS, i.e., significantly below typical RCD trip levels, and, using the human-body impedance model according to UL 2202, achieves a test voltage of 110 mV that is clearly below the most stringent limit (250 mV) of the standard.

4.1 Introduction

Decarbonizing transportation is essential to meet climate goals and the world is moving full-force toward transportation electrification. Accordingly, the market penetration of electric vehicles (EVs) is steadily increasing: in 2021, almost 10% of all global car sales were EVs, which is a fourfold increase compared to 2019 [118]. More efficient and compact EV battery chargers are key enablers for further acceleration of this transition to electric mobility. Even though relevant standards for EV chargers, e.g., UL 2202 [49] or IEC 61851 [119], do not require galvanic isolation between the grid-connected input and the output charging ports (IEC 61851-23 [120], for example, mentions that regulations for non-isolated DC chargers are under consideration), conventional EV chargers typically include either traditional 50 Hz transformers or DC/DC

converters with high-frequency (HF) isolation to provide a large common-mode (CM) impedance between the grid and the vehicle to ensure electrical safety [9, 13, 14]. However, providing galvanic isolation means placing an additional conversion stage, i.e., a low-frequency transformer or an isolated DC/DC converter, in the power flow path and consequently leads to more bulky and more complex systems with increased power losses and costs. To roughly quantify these drawbacks, consider photovoltaic (PV) inverter systems: compared to traditional solutions that include galvanic isolation, their transformerless counterparts feature an efficiency improvement of 1 % to 2 % and about twice the power density [33, 34]. Thus, extensive research has been carried out on non-isolated EV chargers over the recent years [9, 53, 121–129].

However, without galvanic isolation, reliable protection against electrical hazards can only be provided by residual current devices (RCDs)[1] installed at the grid interface, which is thus mandatory according to standards (e.g., IEC 61851, UL 2202) [9]. In three-phase (3-Φ) systems, RCDs measure the sum of the three individual phase currents to detect any deviation from zero, which corresponds to a CM ground current (that potentially could be flowing through a human body touching a live part during a fault situation) and quickly disconnect the converter from the grid if certain trip levels (typ. 30 mA AC and 6 mA DC, see IEC 61851-1 [119]) are reached. **Fig. 4.1a** shows a conceptual block diagram of a typical 3-Φ non-isolated EV charger. Note that a connected battery pack, due to its physically large dimensions, often contributes significantly to the total parasitic CM capacitance between the DC output terminals and the vehicle chassis (and thus to protective earth (PE), as safety standards require the chassis grounded).

To achieve compatibility with the wide range of EV battery voltages (200 V to 800 V, see **Fig. 4.2**), non-isolated EV chargers must provide buck-boost functionality and are thus usually realized as two-stage systems that consist of an AC/DC boost-type voltage DC-link PFC rectifier and a buck-type DC/DC converter. As indicated in the CM equivalent circuit of **Fig. 4.1b**, both the AC/DC-stage and the DC/DC-stage generate HF CM voltages ($v_{\mathrm{AC/DC,CM}}$ and $v_{\mathrm{DC/DC,CM}}$, respectively) due to PWM operation, and the AC/DC-stage may, in addition, generate a low-frequency (LF) CM voltage $\bar{v}_{\mathrm{AC/DC,CM}}$ if third-harmonic injection modulation is employed to improve the DC-link voltage utilization. The total CM voltage could drive significant leakage currents through the parasitic capacitors into the protective earth (PE) conductor (note that C_{p} from the power converter and C_{b} from the battery pack together form the DC-side grounding impedance Z_{g}). Without countermeasures, such

[1] Another common name is "ground fault circuit interrupter" (GFCI).

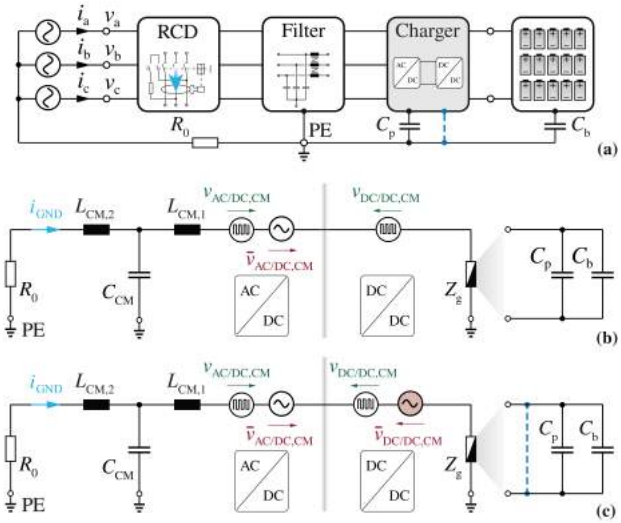

Fig. 4.1: (a) Block diagram of a typical non-isolated three-phase (3-Φ) two-stage AC/DC buck-boost EV charger, and **(b)** its common-mode (CM) equivalent circuit for conventional operation. High-frequency (HF) CM voltage components are limited by the EMI filter. Low-frequency (LF) CM components generated by the AC/DC rectifier stage (e.g., by third-harmonic injection modulation) appear at the DC output terminals, i.e., across the parasitic capacitance of the DC output to earth, potentially driving leakage currents that could lead to nuisance tripping of the mandatory RCD. Note that both, the converter (C_p) and the connected battery pack (C_b) contribute to the total parasitic capacitance. **(c)** As proposed in this chapter, the DC/DC-stage can inject a compensating LF CM voltage, which allows virtual grounding control (VGC), i.e., regulating the LF CM voltage to zero. Similarly, a proposed ground current control (GCC) can be employed to regulate the LF CM leakage current to zero and hence facilitates even a direct connection (blue dashed line) of the output midpoint to ground.

leakage ground currents can easily reach the RCD trip level and thus lead to nuisance tripping [9, 125].

However, as EV chargers are connected to the public mains, EMI standards such as CISPR 11 must be met. Thus, passive differential-mode (DM) and especially also CM filters must be employed, as also (conceptually) indicated in **Fig. 4.1b**, which attenuate the HF CM voltages to levels that do not cause

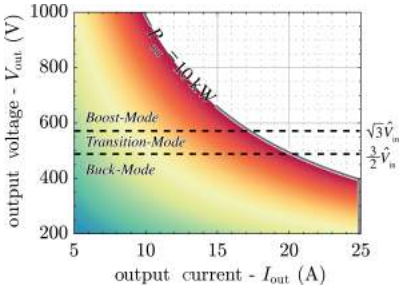

Fig. 4.2: Typical operating range of EV chargers, including a constant output current $I_{out} = 25\,A$ region when $V_{out} < 400\,V$ and a constant output power $P_{out} = 10\,kW$ when $V_{out} > 400\,V$. Three operating modes, i.e., buck-mode, boost-mode and transition-mode, are required to cover such a wide output voltage range [93].

significant HF CM leakage currents.[2] Thus, most non-isolated EV chargers discussed in the literature employ corresponding (CM) EMI filters, whereby often integrated (or so-called floating filter concepts, i.e., essentially DC-link-referenced first (innermost) CM filter stages [130–133], are used, e.g., in [9, 53, 124, 127, 129]). Other approaches target a reduction of the HF CM noise sources by special modulation techniques [128] or CM-free system configurations [126], which, however, rely on the availability of a neutral conductor (three-phase, four-wire systems).

In voltage DC-link boost-type rectifier systems, the generation of an LF CM voltage can be avoided if no third-harmonic injection modulation is used, i.e., by accepting a limitation of the modulation index of $M \leq 1$ compared to $M \leq 1.15$ otherwise, where $M = \hat{V}_{in}/(V_{DC}/2)$ considering that $\hat{V}_{in}$ is the AC phase voltage amplitude and V_{DC} is the DC-link voltage. Furthermore, to ensure a constant LF CM voltage and hence suppress any LF CM leakage currents, the rectifier stage can actively control the LF CM voltage, as, e.g., suggested for converters interfacing the AC mains and DC microgrids [134] or specifically for non-isolated EV chargers in [53, 127, 129]. Finally, a three-phase voltage DC-link rectifier/inverter can be extended by a fourth bridge-leg, which is then modulated to compensate the LF and HF CM noise emissions generated by the other three bridge-legs. This concept has been proposed

[2] With respect to **Fig. 4.1b**, the HF CM voltages appear across the CM EMI filter inductors, i.e., in this example across $L_{CM,1}$ and $L_{CM,2}$ as, at HF, their impedances are significantly larger than those of the capacitive elements in the equivalent circuit; i.e., only residual HF voltage fluctuations appear at the DC output terminals and across Z_g.

for two-level [135] and three-level (3-L) [136] voltage DC-link topologies, but without considering closed-loop control of the ground leakage current.

As demonstrated in [137] for back-to-back 3-Φ T-type rectifier and inverter systems, the rectifier stage can also control the LF CM leakage *current*, provided the system is equipped with a dedicated and highly accurate current sensor measuring the sum of the 3-Φ input currents in the same way an RCD does. Finally, considering two-stage interfaces (i.e., an AC/DC rectifier connected to a DC/DC converter) between a split-phase AC system and a DC microgrid, [138] employs the DC/DC-stage to control the LF CM voltage (see **Fig. 4.1c**), whereas [139] also relies on the DC/DC converter to reduce the LF CM voltage, but only with a feed-forward approach instead of closed-loop control.

In contrast to the aforementioned combination of a voltage DC-link boost-type PFC rectifier and buck-type DC/DC-stage, this chapter focuses on a non-isolated EV charger implemented with a 3-Φ bidirectional buck-boost (bB) *current DC-link* PFC rectifier system (see **Fig. 4.3**), which is formed by a 3-Φ buck-type current-source-rectifier (CSR) stage and a subsequent boost-type DC/DC-stage [93, 94], which has been introduced in **Chapter 2**. Compared to a conventional voltage DC-link PFC rectifier approach, the current DC-link system has several advantages, e.g., a reduced number of main magnetic components (only one DC-link inductor instead of three AC-side boost inductors; the DC-link inductor is shared between the CSR-stage and the DC/DC-stage), which facilitates low manufacturing costs and higher volumetric power density. Note that the main structural weakness of CSRs, i.e., the need for switches that feature bipolar voltage blocking capability, is being eliminated by the recent availability of monolithic bidirectional power transistors [104, 105, 141]. Advantageously, synergetic control [47, 95, 104] of the two-stage system shown in **Fig. 4.3** achieves minimum-loss operation: in the boost-mode ($V_{\text{out}} \geq \sqrt{3}\hat{V}_{\text{in}}$, where $\hat{V}_{\text{in}}$ is the AC phase voltage amplitude and V_{out} is the DC output voltage, see **Fig. 4.2**), the DC/DC-stage shapes the DC-link current such that the CSR-stage can operate with 2/3-PWM [107, 109], i.e., with cyclically changing temporary clamping of a phase (only two and not all three phases are generating switching losses), and in the buck-mode ($V_{\text{out}} \leq 3/2 \cdot \hat{V}_{\text{in}}$) the CSR-stage operates with conventional 3/3-PWM to control the output voltage but the DC/DC-stage is clamped without switching.

Transformerless operation of such a 3-Φ bB current DC-link EV charger has not been investigated and the feasibility of complying with the relevant standards such as UL 2202 [49] or IEC 61851 [119] has not been demonstrated. Different from voltage DC-link rectifier systems, typical modulation schemes

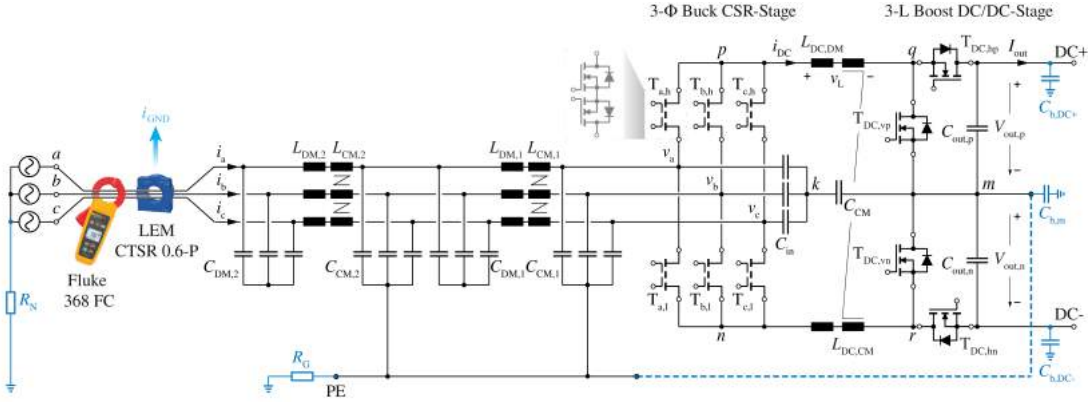

Fig. 4.3: Power circuit of the considered 10 kW three-phase (3-Φ) two-stage current DC-link PFC rectifier system (see **Fig. 4.2** for an overview on the operating range and **Tab. 4.1** for detailed specifications) including a CM/DM EMI filter, which employs an integrated first-stage CM filter [94, 131–133] to limit the DC output HF CM voltage by connecting the artificial 3-Φ neutral point k and the DC voltage midpoint m with a CM filter capacitor C_{CM}. The proposed virtual grounding control (VGC, see **Section 4.2.2**) uses the DC/DC-stage to inject a LF CM voltage and thus regulate the LF voltage across C_{CM} to zero. Alternatively, the proposed ground current control (GCC, see **Section 4.2.3**) enables a low-impedance connection of the output midpoint m to the PE conductor (dashed blue line) with the LF ground current $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ regulated to values < 30 mA, as verified with a leakage current clamp meter *Fluke 368 FC* [140] (see **Section 4.4**). Note that the experimental verification considers two different grid grounding schemes (for details see **Section 4.4.3**), i.e., TT (Terra-Terra) with $R_{\mathrm{N}} = 10\,\Omega$ and $R_{\mathrm{G}} = 100\,\Omega$ and TN (Terra-Neutral) with $R_{\mathrm{N}} = R_{\mathrm{G}} = 0\,\Omega$ [9].

for the CSR-stage always result in an LF CM voltage component $\bar{v}_{\mathrm{AC/DC,CM}}$. However, the employed three-level (3-L) DC/DC converter stage advantageously also can generate an LF CM voltage, which in principle opens the possibility of compensating the LF CM voltage of the AC/DC rectifier stage by selecting $\bar{v}_{\mathrm{DC/DC,CM}} = \bar{v}_{\mathrm{AC/DC,CM}}$, see **Fig. 4.1c**.

Therefore, this chapter provides a comprehensive analysis of a new virtual grounding control (VGC) method, i.e., a feedback control of the LF CM voltage that ensures zero voltage (i.e., a virtual connection) between the artificial neutral point k formed by the AC-side input filter capacitors and the midpoint m of the DC-side output (see **Fig. 4.3**). Thus, the proposed VGC effectively minimizes the parasitic ground current flowing through $C_{\mathrm{b,m}}$. By further selecting sufficiently large output capacitors $C_{\mathrm{out,p}}$ and $C_{\mathrm{out,n}}$, also the amplitudes of the LF CM voltages at the terminals DC+ and DC- with reference to PE are decreased, which ultimately leads to greatly reduced ground leakage currents through $C_{\mathrm{b,DC+}}$ and $C_{\mathrm{b,DC-}}$.

Furthermore, closed-loop ground current control (GCC) is proposed to allow a direct connection[3] of the output DC-bus midpoint m to the system PE connector (see also the blue dashed line in **Fig. 4.1c** and **Fig. 4.3**) by controlling the ground current $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ (i.e., the leakage current measured and limited by RCDs) of the analyzed current DC-link system to near-zero. GCC prevents nuisance tripping of mandatory RCDs and is hence considered an enabling concept for future transformerless EV chargers. Importantly, such a direct connection also removes the impact of any parasitic ground capacitance, e.g., $C_{\mathrm{b,DC+}}$ or $C_{\mathrm{b,DC-}}$, that might vary between different battery packs, since these parasitic capacitors are then directly in parallel with the relatively large output capacitors $C_{\mathrm{out,p}}$ and $C_{\mathrm{out,n}}$.

In the following, **Section 4.2** first derives the CM equivalent circuit of the analyzed 3-Φ bB current DC-link PFC rectifier system and explains the operating principle of the proposed VGC and GCC concepts. **Section 4.3** then presents the corresponding control structure that realizes the synergetic operation of the two converter stages and implements VGC or GCC. Finally, **Section 4.4** provides experimental results of a 10 kW hardware demonstrator that verify the proposed VGC. Using a direct grounding of the DC output midpoint and the proposed GCC, we further demonstrate total leakage currents of well below the typical RCD trip level of 30 mA for TT and TN grid grounding schemes (these are explained in detail in Section 4.4.3), and (for TN systems) an output voltage of the human-body impedance model according

[3]Note that such a direct connection also removes the impact of any parasitic ground capacitances that might vary between different battery packs.

Tab. 4.1: System specifications.

	Description	Value
V_{in}	Phase RMS volt.	230 V
V_{out}	DC output volt. range	300 V~1000 V
P_{out}	Rated output power	10 kW
$I_{out,max}$	Output current limit	25 A (V_{out} < 400 V)
f_{CSR}	CSR-stage sw. freq.	100 kHz
$f_{DC/DC}$	DC/DC-stage sw. freq.	100 kHz
$L_{DC,DM}$	DC-link DM inductor	250 µH
$L_{DC,CM}$	DC-link CM inductor	11 mH
C_{in}	Input filter capacitor	3×6 µF
$C_{out,p} = C_{out,n}$	Output filter capacitor	2×11.2 µF
C_{CM}	Integrated CM filter cap.	88 nF
$L_{DM,1} = L_{DM,2}$	EMI DM inductor	10 µH
$C_{DM,1} = C_{DM,2}$	EMI DM capacitor	3 µF
$L_{CM,1} = L_{CM,2}$	EMI CM inductor	1.2 mH
$C_{CM,1} = C_{CM,2}$	EMI CM capacitor	18.8 nF

to UL 2202 of clearly less than the limit of 250 mV, i.e., full compliance with applicable standards over a wide output voltage and power range.

4.2 Operating Principle

The considered bidirectional two-stage 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 4.3** connects the 3-Φ AC mains to a DC load through a buck-type CSR front-end and a cascaded boost-type 3-L DC/DC output stage, which advantageously share the main magnetic components, i.e., the DC-link inductor L_{DC} and the first-stage CM filter inductor $L_{DC,CM}$ [93, 94]. In conventional rectifier operation, the buck-type CSR-stage first steps down the 3-Φ AC mains voltages (v_a, v_b, v_c) to a lower DC voltage v_{pn} using PWM; or, considering the more illustrative reverse current conversion, the 3-Φ mains currents (i_a, i_b, i_c) are realized by pulse-width-modulated distribution of the constant DC-link current to the three phases. As long as the output voltage is below the maximum DC-side voltage that the CSR-stage can generate ($V_{out} < {}^3/_2\hat{V}_{in}$, buck-mode), the DC/DC-stage is not needed and can be clamped, i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on. If the output voltage is higher

($V_{\text{out}} > \sqrt{3}\hat{V}_{\text{in}}$, boost-mode), the boost-type DC/DC-stage must be operated to step up v_{pn} to the higher output voltage accordingly. Note that the artificial 3-Φ neutral point k formed by the CSR-stage's DM input filter capacitors C_{in} and the DC output voltage midpoint m are connected through a CM filter capacitor C_{CM}, i.e., C_{CM} and $L_{\text{DC,CM}}$ form an integrated CM filter [94, 131–133]. In this section, first, a CM equivalent circuit of the converter shown in **Fig. 4.3** is developed to then facilitate clear explanations of the proposed virtual grounding control (VGC) and ground current control (GCC) concepts, considering both, boost-mode and buck-mode operation.

4.2.1 CM Equivalent Circuit

Neglecting the grid-side EMI filter in the first step, the analyzed converter can be represented by the equivalent circuit shown in **Fig. 4.4a**, where the CSR-stage's upper and lower switching cells are replaced by the voltage sources v_{pk} and v_{kn}, respectively, and the DC/DC-stage's upper and lower half-bridges (HBs) by v_{qm} and v_{mr}. These voltage sources contain HF components (i.e., switching frequency and its harmonics) and LF components (i.e., at frequencies significantly below the switching frequency, such as DC or low-order harmonics of the grid frequency). It is then useful to separate the voltages generated by both stages into DM and CM components, which yields the equivalent circuit shown in **Fig. 4.4b**, whereby

$$v_{\text{CSR,CM}} = \frac{v_{\text{pk}} - v_{\text{kn}}}{2}, \qquad v_{\text{DC,CM}} = \frac{v_{\text{qm}} - v_{\text{mr}}}{2}, \tag{4.1}$$

$$v_{\text{CSR,DM}} = v_{\text{pk}} + v_{\text{kn}}, \qquad v_{\text{DC,DM}} = v_{\text{qm}} + v_{\text{mr}}. \tag{4.2}$$

The final CM equivalent circuit (see **Fig. 4.4c**) includes the two-stage CM EMI filter and the impedances modeling the considered grid grounding schemes (TT and TN). Note the similarity to the conceptual drawing discussed earlier (see **Fig. 4.1c**), i.e., HF CM components are suppressed by a passive multi-stage EMI filter, which in particular features an integrated CM filter formed by C_{CM} and $L_{\text{DC,CM}}$.

Therefore, focusing on the LF components, $\bar{v}_{\text{CSR,DM}} = \bar{v}_{\text{DC,DM}}$ must always be attained in steady-state operation.[4] Considering the state-of-the-art synergetic operation, the two output DC voltages are balanced ($V_{\text{out,p}} = V_{\text{out,n}}$) [95] and thus the two half-bridges of the DC/DC-stage are modulated with equal duty cycles so that $\bar{v}_{\text{qm}} = \bar{v}_{\text{mr}}$ and, hence, zero LF CM injection

[4] The minor LF voltage difference needed to shape the DC-link current into the six-pulse shape in boost-mode operation with 2/3-PWM is neglected.

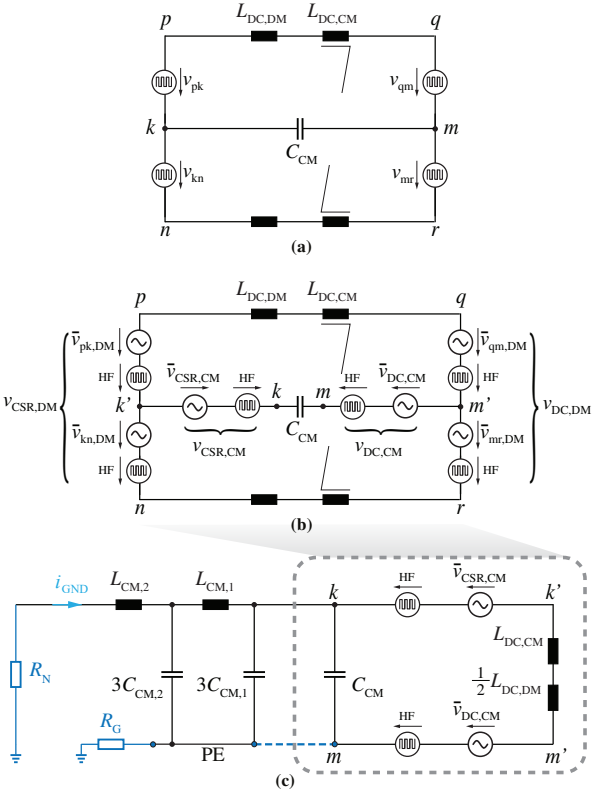

Fig. 4.4: Derivation of the CM equivalent circuit of the 3-Φ bB current DC-link PFC rectifier system from **Fig. 4.3**. Neglecting the EMI filter in a first step, **(a)** shows the main power converter consisting of the CSR-stage and the DC/DC-stage which are replaced by switched voltage sources. **(b)** These switched voltage sources are decomposed to present DM and CM as well as HF and LF components explicitly. **(c)** The final CM equivalent circuit is obtained from **(b)** by retaining only the LF and HF CM voltage sources and adding the CM EMI filter as well as the grounding scheme of the grid. Note that an LF CM voltage $\bar{v}_{DC,CM}$ generated by the DC/DC-stage can compensate the LF CM voltage $\bar{v}_{CSR,CM}$ inevitably generated by the CSR-stage. This enables the proposed VGC (where the DC output is not explicitly grounded) or the novel GCC (where the DC output is hard grounded as indicated by the dashed blue line and the ground current i_{GND} is controlled to zero in closed loop).

($\bar{v}_{\mathrm{DC,CM}} = 0$) results. In contrast, typical CSR modulation schemes do not achieve $\overline{v}_{\mathrm{pk}} = \overline{v}_{\mathrm{kn}}$ [94], and hence we have $v_{\mathrm{CSR,CM}} \neq 0$. As a result, an LF CM voltage $\bar{v}_{\mathrm{mk}} = \bar{v}_{\mathrm{CSR,CM}} - \bar{v}_{\mathrm{DC,CM}} \neq 0$ appears across the integrated CM filter capacitor C_{CM}, i.e., between the DC output midpoint, m, and the (artificial) grid star point k.

As can be seen in **Fig. 4.4c**, $\bar{v}_{\mathrm{mk}}$ is approximately equal to $\bar{v}_{\mathrm{mPE}}$ considering a symmetric 3-Φ mains. Thus, this LF CM voltage prevents a direct low-impedance connection of m and PE, as then significant LF CM leakage currents would flow, i.e., $L_{\mathrm{CM},1}$ and $L_{\mathrm{CM},2}$ can only provide limited LF impedance. In the case of TN grounding systems with nonzero R_{G}, significant touch voltages (i.e., voltages between the local PE and true earth) could appear. On the other hand, **Fig. 4.4c** also clearly shows that, in principle, the DC/DC-stage can inject an LF CM voltage $\bar{v}_{\mathrm{DC,CM}} = \bar{v}_{\mathrm{CSR,CM}}$ such that $\bar{v}_{\mathrm{mk}} = 0$, which is possible without interfering with the LF DM voltage regulation. This (virtually) ties m to PE (i.e., $\bar{v}_{\mathrm{mPE}} = 0$) and thus facilitates a direct connection of these two points, i.e., hard grounding of the DC output midpoint m. Furthermore, $\bar{v}_{\mathrm{mk}} = 0$, ideally, leads to zero LF CM current flowing through the CM inductor $L_{\mathrm{DC,CM}}$ of the integrated filter, which allows a more compact CM inductor realization because of reduced saturation margin and/or a larger CM capacitance C_{CM} and, for a given attenuation requirement, thus a lower $L_{\mathrm{DC,CM}}$ can be selected.

4.2.2 Virtual Grounding Control (VGC)

The analyzed converter operated with synergetic control provides buck-boost functionality and thus features two main operating modes, i.e., boost-mode ($V_{\mathrm{out}} > \sqrt{3}\hat{V}_{\mathrm{in}}$) and buck-mode ($V_{\mathrm{out}} < {}^{3}/_{2}\hat{V}_{\mathrm{in}}$), as described in [95]. In the following, the generic analysis from above will be explained in detail for each of these two operating modes.

Boost-Mode

In boost-mode operation (see **Fig. 4.5.i**), the CSR-stage operates with 2/3-PWM where no zero switching states are employed (v_{pn} never attains 0 V in **Fig. 4.5d**), i.e., one phase is always clamped, which advantageously reduces the switching losses. To still ensure sinusoidal 3-Φ mains currents, the DC/DC-stage is required to regulate the DC-link current to follow the six-pulse shape (defined by the envelope of the phase current absolute values) needed for 2/3-PWM (see **Fig. 4.5b**). As mentioned above, the CSR-stage inevitably generates an LF CM voltage $\bar{v}_{\mathrm{CSR,CM}}$, which is independent of the output voltage since the CSR-stage operates identically over the boost-mode operating range

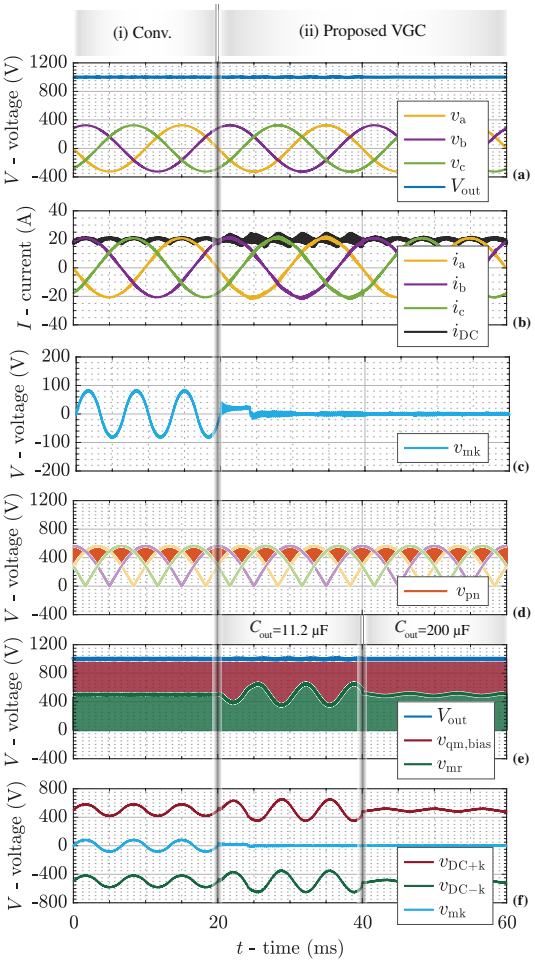

Fig. 4.5: Simulated key waveforms for operation in the boost-mode, **(i)** regulated by conventional synergetic control without VGC and **(ii)** with the proposed VGC. **(a)** 3-Φ mains voltages v_a, v_b, v_c and DC output voltage V_{out}. **(b)** 3-Φ mains currents i_a, i_b, i_c and DC-link current i_{DC}. **(c)** CM voltage v_{mk}. **(d)** Switched voltage v_{pn} at the output of the CSR-stage; note that 2/3-PWM does not employ the zero (shoot-through) switching state of the CSR-stage (v_{pn} never attains 0 V). **(e)** Switched voltages $v_{qm,bias} = v_{qm} + V_{out,n}$ and v_{mr} at the input of the DC/DC-stage's upper and lower HBs. **(f)** LF CM voltages v_{DC+k}, v_{DC-k}, v_{mk} at the DC output terminals, which could drive ground leakage currents through the parasitic capacitances $C_{b,DC+}$, $C_{b,DC-}$, and $C_{b,m}$ (see **Fig. 4.3**).

[94]. Different from the CSR-stage, only HF CM noise (no LF CM voltage) is generated by the DC/DC-stage in case of conventional synergetic control [94], since typically the two output capacitor voltages, i.e., $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$, are equal and the DC/DC-stage's upper and lower HBs operate with the same duty cycles. Thus, the LF CM capacitor voltage becomes $\bar{v}_{\mathrm{mk}} = \bar{v}_{\mathrm{CSR,CM}}$ and contains major LF components (see **Fig. 4.5c.i**). Note that therefore also the voltages between each of the three output nodes (m, DC+ and DC-) and PE (same potential as the node k) contain significant LF components (see **Fig. 4.5f.i**) that might drive comparably high LF CM currents through the corresponding parasitic ground capacitances; note that especially $C_{\mathrm{b,DC+}}$ and $C_{\mathrm{b,DC-}}$ are dominated by the connected battery pack and can be as high as several µF [45, 126].

To suppress this LF CM voltage $\bar{v}_{\mathrm{mk}}$, the virtual grounding control (VGC) is proposed, where the DC/DC-stage is modulated to actively compensate the LF CM voltage generated by the CSR-stage such that $\bar{v}_{\mathrm{mk}} \approx 0\,\mathrm{V}$, i.e., the potentials m and k are virtually connected. Only a minor (and hence here neglected) LF DM voltage component is needed to obtain the six-pulse shape of the DC-link current, resulting in the DM requirement $\bar{v}_{\mathrm{CSR,DM}} = \bar{v}_{\mathrm{DC,DM}}$. To enable the proposed VGC, the CM requirement $\bar{v}_{\mathrm{CSR,CM}} = \bar{v}_{\mathrm{DC,CM}}$ directly leads to the conditions $\bar{v}_{\mathrm{qm}} = \bar{v}_{\mathrm{pk}}$ and $\bar{v}_{\mathrm{mr}} = \bar{v}_{\mathrm{kn}}$, see also **Fig. 4.4a**. Then, the local average power balance at the input (i.e., DC-link side) and the output of the upper DC/DC-stage HB can be written as

$$\bar{v}_{\mathrm{pk}} \cdot \bar{i}_{\mathrm{DC}} = V_{\mathrm{out,p}} \cdot \left(I_{\mathrm{out}} + C_{\mathrm{out,p}} \cdot \frac{\mathrm{d}V_{\mathrm{out,p}}}{\mathrm{d}t}\right), \tag{4.3}$$

where $\bar{i}_{\mathrm{DC}}$ is the local average value of the DC-link current. Assuming a constant output current I_{out}, $V_{\mathrm{out,p}}$ must show a time-varying behavior defined by the time-varying power flowing through the CSR-stage's upper commutation cell, which mainly consists of a 150 Hz (i.e., third harmonic of the grid frequency) variation when using 2/3-PWM. Likewise, the power balance for the lower commutation cell is obtained as

$$\bar{v}_{\mathrm{kn}} \cdot \bar{i}_{\mathrm{DC}} = V_{\mathrm{out,n}} \cdot \left(I_{\mathrm{out}} + C_{\mathrm{out,n}} \cdot \frac{\mathrm{d}V_{\mathrm{out,n}}}{\mathrm{d}t}\right). \tag{4.4}$$

Neglecting the capacitive current flowing through $C_{\mathrm{out,p}}$, the sum of the two equations leads to

$$(\bar{v}_{\mathrm{pk}} + \bar{v}_{\mathrm{kn}}) \cdot \bar{i}_{\mathrm{DC}} = \bar{v}_{\mathrm{CSR,DM}} \cdot \bar{i}_{\mathrm{DC}} = (V_{\mathrm{out,p}} + V_{\mathrm{out,n}}) \cdot I_{\mathrm{out}}, \tag{4.5}$$

where the left-hand side describes the constant input power delivered by a symmetric 3-Φ system. Thus, since the load current I_{out} is constant, operation

with VGC still ensures a constant total output voltage $V_{out} = V_{out,p} + V_{out,n}$. On the other hand, as the VGC circuit simulation results from **Fig. 4.5.ii** show, the individual output capacitor voltages $V_{out,p}$ and $V_{out,n}$ vary complementarily at 150 Hz (see **Fig. 4.5e.ii**). Note further that the CM voltage becomes $\bar{v}_{mk} \approx 0\,V$ while the CSR-stage still advantageously operates with 2/3-PWM (see **Fig. 4.5c.ii** and **Fig. 4.5d.ii**).

In this context, note that the overall LF CM voltage generated by the DC/DC-stage has two contributions: A CM component added to the duty cycles of the upper and the lower HBs, and the difference between the two output capacitor voltages $V_{out,p}$ and $V_{out,n}$ contribute to the CM voltage before modulation of the two HBs. If a large voltage variation is accepted, correspondingly smaller CM duty cycle components are needed to realize a given $\bar{v}_{DC,CM}$, which will be an important consideration for buck-mode operation (see **Section 4.2.2**).

The proposed VGC regulates the output midpoint to potential k (equivalent to PE), which almost completely suppresses parasitic LF ground currents flowing through $C_{b,m}$. However, as can be seen in **Fig. 4.5f.ii**, the LF voltage fluctuations of the output capacitor voltages still result in LF CM voltages v_{DC+k} and v_{DC-k} across the parasitic capacitances $C_{b,DC+}$ and $C_{b,DC-}$ at the terminals DC+ and DC- (see **Fig. 4.3**). However, the two output capacitances $C_{out,p}$ and $C_{out,n}$ are a degree of freedom to lower the amplitudes of these LF CM voltages as needed to limit the ground leakage currents through $C_{b,DC+}$ and $C_{b,DC-}$. Note that the ground current control (GCC) proposed below mitigates these leakage currents without the need for larger output capacitances.

The output capacitor voltage variation affects (increases) the maximum blocking voltage of the DC/DC-stage's power transistors. It is therefore important to calculate the maximum voltage ripple ΔV_{pp} of each of the two output capacitors. The output capacitor voltages mainly consist of a DC component of $1/2 V_{out}$ and an LF (150 Hz) variation. Neglecting other (minor) LF harmonics, this LF voltage variation can be accurately calculated from (4.3), resulting in a closed-form expression for the peak-to-peak voltage ripple as

$$\Delta V_{pp} = \frac{2A\,\omega_1 \sin\theta_1 + 2B\cos\theta_1}{(A\omega_1)^2 + B^2} + \frac{2A\,\omega_2 \sin\theta_2 + 2B\cos\theta_2}{(A\omega_2)^2 + B^2}, \tag{4.6}$$

with

$$A = \frac{C_{out}\,V_{out}}{\hat{i}_{in}\,\hat{v}_{CSR,CM}}, B = \frac{2I_{out}}{\hat{i}_{in}\,\hat{v}_{CSR,CM}}, \theta_1 = \omega_1 t_p, \theta_2 = \omega_2 t_p, \tag{4.7}$$

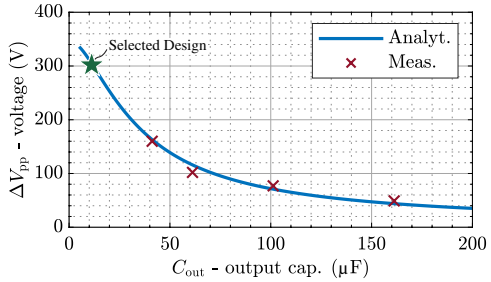

Fig. 4.6: Peak-to-peak variation ΔV_{pp} of the voltages of the two output capacitors $C_{out,p}$ and $C_{out,n}$ (see **Fig. 4.3**) under the proposed VGC as a function of the DC output capacitance C_{out} when operating at $V_{out} = 1000\,V$ and $P_{out} = 10\,kW$. The analytical calculation results are confirmed by measurements taken with the hardware demonstrator described in **Section 4.4**, whereby the DC output capacitance has been externally increased above the design value of 11.2 µF to realize the other indicated capacitances.

where $\omega_1 = 2\pi(f_{CSR,CM} + f_{in})$, $\omega_2 = 2\pi(f_{CSR,CM} - f_{in})$, and $t_p = {}^1/_{\omega_1} \cdot \operatorname{atan}({}^{A\omega_1}/_{B})$. Furthermore, f_{in} is the grid frequency and $\hat{v}_{CSR,CM}$ and $f_{CSR,CM}$ denote the amplitude and the frequency of the LF CM voltage injected by the CSR-stage, which should be compensated by the DC/DC-stage using VGC. The equation is visualized and verified in **Fig. 4.6** considering $V_{out} = 1000\,V$ (i.e., the worst-case operating point in terms of voltage stress for the DC/DC-stage transistors), $P_{out} = 10\,kW$ and different output capacitance values C_{out}. Note that an increased C_{out} leads to a reduced ΔV_{pp} as expected. Furthermore, a clear trade-off between the blocking voltage rating of the transistors in the DC/DC-stage and the system's power density is observed, i.e., a large output capacitance can be implemented to reduce the LF voltage variation but leads to a lower volumetric power density. Finally, $C_{out} = 11.2\,\mu F$ as originally designed based on a HF voltage ripple criterion and without taking into account VGC results in a peak blocking voltage stress on the DC/DC-stage HBs of 500 V + 150 V = 650 V, which is compatible with the employed 900 V SiC transistors. Therefore, no design modifications are needed for VGC operation.

Buck-Mode

In the buck-mode operation, the DC output voltage is low enough to be directly generated by the buck-type CSR-stage. Then, the DC-link current

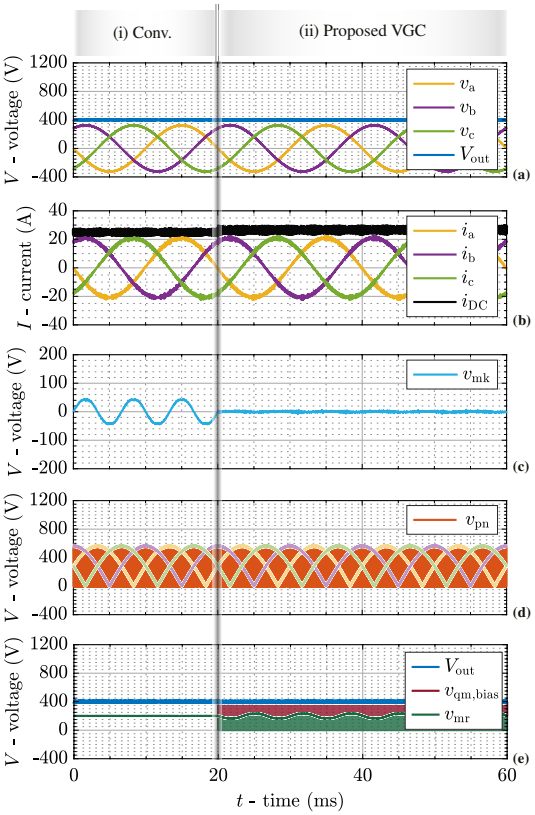

Fig. 4.7: Simulated key waveforms for operation in the buck-mode, **(i)** without and **(ii)** with VGC. **(a)** 3-Φ mains voltages v_a, v_b, v_c and DC output voltage V_{out}. **(b)** 3-Φ mains phase currents i_a, i_b, i_c and DC-link current i_{DC}. **(c)** CM voltage v_{mk}. **(d)** Switched voltage v_{pn} at the output of the CSR-stage; note that 3/3-PWM is used (i.e., the zero and/or shoot-through states are employed). **(e)** Switched voltages $v_{qm,bias} = v_{qm} + V_{out,n}$ and v_{mr} at the input of the DC/DC-stage's upper and lower HBs. Note that the DC/DC-stage must be activated to realize VGC, which requires a slight increase of the DC-link current by about 5 % from 25 A to 26.4 A, see (b), as explained in the text.

is constant and equals the output current, i.e., $i_{DC} = I_{out}$ (see **Fig. 4.7.i**), and the CSR-stage operates with 3/3-PWM. As the step-up functionality of the DC/DC-stage is not needed, an advantageous synergetic control [95] allows to automatically clamp the DC/DC-stage, i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently turned on to reduce switching losses. However, this implies that $\bar{v}_{DC,CM} = 0$ and hence the CM voltage becomes $\bar{v}_{mk} = \bar{v}_{CSR,CM} \neq 0$ as all typically employed 3/3-PWM switching sequences of the CSR-stage result in certain LF (mainly third-harmonic) CM voltage components [94].

However, it is of course possible to select a slightly higher DC-link current ($i_{DC} = k_{VGC} \cdot I_{out}$ with $k_{VGC} > 1$), such that the DC/DC-stage must be activated to step down the DC-link current to the output current. This, in principle, again opens the possibility of injecting a CM voltage $\bar{v}_{DC,CM} = \bar{v}_{CSR,CM}$ to compensate the CM voltage generated by the CSR-stage as shown in **Fig. 4.7.ii**. Thus, VGC can be achieved in the buck-mode, too, but results in switching losses of the DC/DC-stage, i.e., forgoes the advantageous clamping of the DC/DC-stage; however, relatively low additional switching losses are expected because of the low switched voltages. Furthermore, the DC-link current must be increased above the minimum necessary value, i.e., I_{out} in the buck-mode, to facilitate VGC. The required increase quantified by k_{VGC}, i.e., the sufficient margin for LF CM voltage injection by the DC/DC-stage, is thus clarified in the following.

Similar to the boost-mode operation, the value of the DC output capacitors C_{out} has a significant impact on the circuit operation. A smaller C_{out} leads to an increased output capacitor voltage variation (i.e., ΔV_{pp} increases) but this decreases the variation of the duty cycles d_p and d_n of the two DC/DC-stage HBs, which is required to generate the compensating $\bar{v}_{DC,CM}$. This means that the duty cycles remain closer to unity, which, in turn, means that the required increase of the DC-link current over the output current becomes smaller. Thus, a smaller C_{out} is preferable for buck-mode operation as shown in **Fig. 4.8**, e.g., $i_{DC} = 26.4\,A$ ($k_{VGC} = 1.05$, i.e., a 5 % increase) is needed at 400 V, 10 kW to eliminate the LF CM emission ($\bar{v}_{mk} = 0$) if $C_{out} = 11.2\,\mu F$ (realized design) but $i_{DC} = 28.1\,A$ would be necessary if a higher $C_{out} = 200\,\mu F$ would be used.

The dependencies of the needed DC-link current to enable VGC on the output voltage show distinct kinks at around 320 V (see **Fig. 4.8**). This can be explained as follows: if the CSR-stage operates with a large modulation index[5], i.e., $M > 0.65$ for $V_{out} > 320\,V$, the LF CM voltage $\bar{v}_{CSR,CM}$ generated

[5]The modulation index of a current DC-link rectifier is defined as $M = \hat{I}_{in}/I_{DC} = V_{out}/(3/2 \cdot \hat{V}_{in})$.

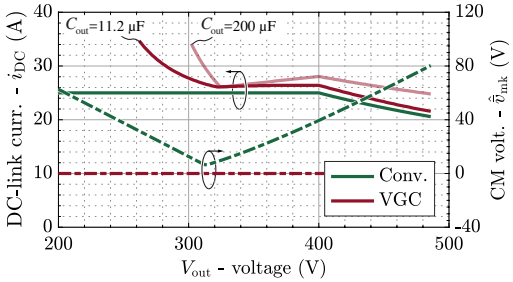

Fig. 4.8: Minimum buck-mode DC-link current i_{DC} (at rated load) and resulting peak LF CM voltage $\hat{v}_{mk}$ at the DC output when operating with conventional synergetic control (green), i.e., with the DC/DC-stage clamped so that $\bar{v}_{mk} = \bar{v}_{CSR,CM}$, or the proposed VGC (red), where the DC/DC-stage injects a compensating LF CM voltage to realize $\bar{v}_{mk} = 0$. Note that a higher output capacitance C_{out} leads to a higher required DC-link current to facilitate VGC, e.g., $i_{DC} = 26.4\,A$ is needed at 400 V, 10 kW to achieve zero LF CM emission if $C_{out} = 11.2\,\mu F$ (realized design) but 28.1 A would be necessary if $C_{out} = 200\,\mu F$. The kink observed in the capacitance curves at around $V_{out} = 320\,V$ is explained in the text.

by the CSR-stage is predominantly composed of the CM voltage contributions of the active switching states. Thus, increasing i_{DC} as required by VGC leads to a reduction of the LF CM voltage $\bar{v}_{CSR,CM}$ of the CSR-stage due to the shortened on-time of the active switching states, i.e., advantageously *reduces* the LF CM voltage to be compensated by the DC/DC-stage. However, in the low-modulation-index region, i.e., for $M < 0.65$ at $V_{out} < 320\,V$, the CSR-stage's LF CM voltage $\bar{v}_{CSR,CM}$ is mainly defined by the zero switching state. Thus, increasing i_{DC} as needed to enable VGC also *increases* the LF CM voltage of the CSR-stage, which should be compensated in the first place. As a result, an even higher DC-link current would be required to achieve sufficient modulation margin for the DC/DC-stage, etc. This effect defines the lower output voltage limit of the proposed non-isolated EV charger, for which VGC can reasonably be employed (about 300 V in the case at hand).

Thus, VGC is feasible in the buck-mode, too, but comes at the price of slightly increased switching losses (the DC/DC-stage switches comparably low voltages) and also slightly higher conduction losses (about 5 % higher DC-link current) compared to optimum synergetic operation with a clamped DC/DC-stage. The proposed VGC concept can thus achieve zero LF CM voltage ($\bar{v}_{mk} = 0\,V$) over a wide buck-boost output voltage range of 300 V to 1000 V, which is crucial for the targeted EV charging application.

4.2.3 Ground Current Control (GCC)

So far, it has been shown how the proposed VGC can achieve zero LF CM voltage, i.e., $\bar{v}_{\mathrm{mk}} = 0\,\mathrm{V}$, in principle, and **Section 4.3** discusses a closed-loop implementation that actually *controls* $\bar{v}_{\mathrm{mk}}$ to zero. However, unless relatively large output capacitors are employed, still significant LF CM components appear across the parasitic ground capacitances at the battery terminals, i.e., DC+ and DC-. Increasing the output capacitors, first, reduces the power density of the system and, second, increases the required extra DC-link current in buck-mode operation.

Therefore, it is desirable to implement a low-impedance grounding of the DC-output midpoint *m*, i.e., a direct connection of *m* to PE (see the dashed blue line in **Fig. 4.3** and **Fig. 4.4c**), which essentially removes the parasitic capacitances at the battery terminals (since they are effectively connected in parallel to the relatively large output capacitors). Then, however, direct feedback control of the LF CM ground *current*, i.e., the proposed ground current control (GCC), is the most reliable way to prevent nuisance tripping of RCDs. The ground current is thus best measured as the sum of the three-phase mains phase currents, i.e., $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ as shown in **Fig. 4.3**, as the same measurement method is implemented in RCDs. Note that the considerations made in the context of VGC (e.g., regarding the voltage stress of the DC/DC-stage's power transistors, etc.) remain valid, as in theory (and considering sufficiently large output capacitors) achieving $\bar{v}_{\mathrm{mk}} = 0$ is equivalent to realizing zero LF ground current, i.e., $i_{\mathrm{GND}} = 0$. The latter, however, can advantageously also be achieved with small output capacitors.

4.3 Control Strategy

After clarifying the ideal operation of the two converter stages to achieve the proposed VGC or GCC, this section discusses the implemented control strategy that realizes that desired behavior. The proposed control strategy (see **Fig. 4.9**) is closely based on the synergetic control concept described in [95], and therefore especially the modifications necessary to implement VGC or GCC are highlighted in the following.

4.3.1 Output Voltage and DC-Link Current Control

The outermost control loop performs the output voltage regulation (see *Output Voltage Control* block in **Fig. 4.9**). The difference between the measured V_{out}

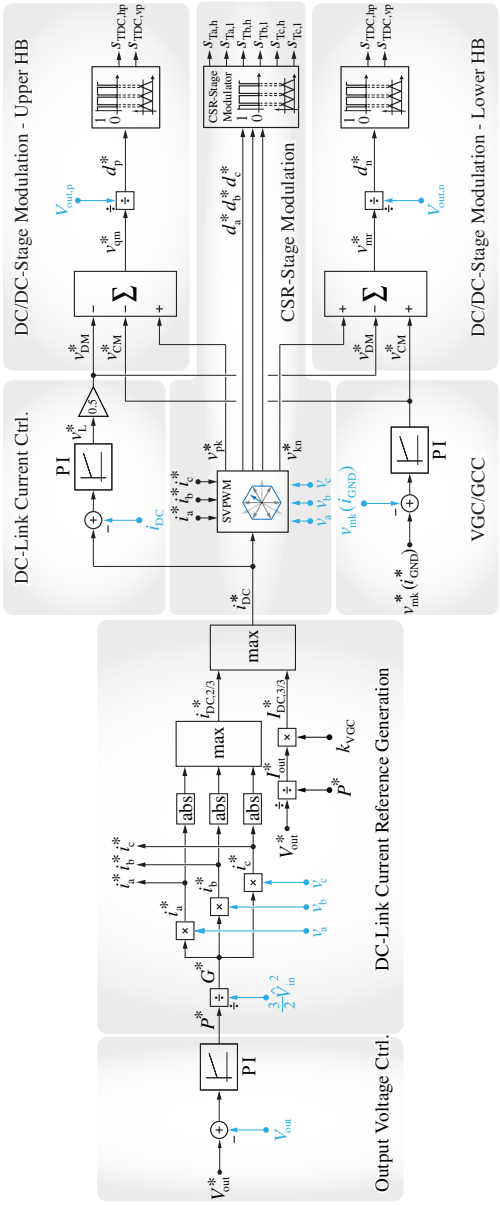

Fig. 4.9: Proposed control block diagram for the 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 4.3**. It is based on the synergetic control concept from [93] but in addition implements virtual grounding control (VGC) or ground current control (GCC). The functionality and the interaction of the individual control blocks are described in the text. Note that all quantities refer to local average values here.

and the reference output voltage V_{out}^* defines the input power reference P^* through a PI-controller. To ensure ohmic mains behavior, this power reference is then translated into an input conductance reference

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{\text{in}}^2}. \tag{4.8}$$

In the following *DC-Link Current Reference Generation* block, this ensures 3-Φ sinusoidal mains current references i_{a}^*, i_{b}^*, and i_{c}^* that are proportional to the corresponding 3-Φ input voltages v_{a}, v_{b}, and v_{c}, i.e., realizes ohmic behavior.

For operation in the boost-mode with 2/3-PWM, the envelope of the absolute 3-Φ sinusoidal mains current references defines the (time-varying) DC-link current reference $i_{\text{DC,2/3}}^*$. In contrast, for buck-mode operating points, the DC-link current must be at least as high as the output current reference. However, note that if VGC (or GCC) is employed, this minimum value must be slightly increased by a factor $k_{\text{VGC}} > 1$ (see **Section 4.2.2** above), with typical values being in the order of about $k_{\text{VGC}} = 1.05$, i.e., $I_{\text{DC,3/3}}^* = k_{\text{VGC}} \cdot I_{\text{out}}^* = k_{\text{VGC}} \cdot P^*/V_{\text{out}}^*$. Finally, selecting the DC-link current reference as $i_{\text{DC}}^* = \max\left(i_{\text{DC,2/3}}^*, I_{\text{DC,3/3}}^*\right)$ ensures automatic transitions between 2/3-PWM in the boost-mode and 3/3-PWM in the buck mode.

The inner DC-link current control loop calculates the required voltage v_{L}^* across the DC-link inductor L_{DC} by comparing the reference i_{DC}^* and the measured i_{DC} DC-link current in the *DC-Link Current Control* block. To achieve the proposed VGC or GCC, the DC/DC-stage needs to operate at all times (especially also in the buck-mode, which is different from conventional synergetic control [95] without VGC), the control voltage v_{L}^* is exclusively realized by the DC/DC-stage, e.g., a positive v_{L}^* is generated by a decreased input voltage v_{qr} of the DC/DC-stage.

4.3.2 Virtual Grounding Control & Ground Current Control

The *VGC/GCC* block, finally, implements either VGC or GCC with a PI controller to calculate the LF CM voltage injection reference v_{CM}^* for the DC/DC-stage. Specifically, for VGC v_{CM}^* is obtained by feeding the difference between the reference v_{mk}^*, i.e., in most cases $v_{\text{mk}}^* = 0\,\text{V}$, and the measured v_{mk} CM voltage through a PI controller. For GCC, the error between the reference $i_{\text{GND}}^* = 0\,\text{A}$ and the measured i_{GND} ground current serves as the controller input. The system modeling and the PI controller tuning are conducted based on [137] and not detailed here for the sake of brevity.

4.3.3 CSR-Stage and DC/DC-Stage Modulation

The CSR-stage modulation is implemented in the *CSR-Stage Modulation* block. The 3-Φ mains current references and the DC-link reference current serve as inputs to an SVPWM (Space Vector based Pulse Width Modulation) unit, which generates the 3-Φ duty cycles d_a^*, d_b^*, and d_c^*, which the PWM modulator finally translates into the switch-level gate signals that ensure correct commutation sequences for the CSR-stage's commutation cells. Furthermore, the SVPWM unit calculates the LF voltages v_{pk}^* and v_{kn}^* at the output of the CSR-stage's upper and lower commutation cell from the measured 3-Φ input voltages v_a, v_b, and v_c, which are then used as feed-forward terms for the DC/DC-stage modulation.

In the *DC/DC-Stage Modulation* block, the DC-link current controller output v_L^*, the feed-forward voltage terms v_{pk}^* and v_{kn}^* from the CSR SVPWM unit, and the VGC/GCC controller output voltage v_{CM}^* are summarized to obtain the input voltage reference of the upper DC/DC-stage HB as

$$v_{qm}^* = v_{pk}^* - v_{DM}^* - v_{CM}^*, \tag{4.9}$$

and of the lower HB as

$$v_{mr}^* = v_{kn}^* - v_{DM}^* + v_{CM}^*. \tag{4.10}$$

Selecting $v_{DM}^* = 0.5 v_L^*$ ensures that the DM control voltage v_L^* is generated by the upper and lower HBs equally to avoid CM voltage injection and thus disturbing or interfering with the CM control loop. Furthermore, the upper and lower HBs realize the CM control voltage v_{CM}^* without generating DM voltages, which is proved by v_{CM}^* appearing in v_{qm}^* and v_{mr}^* with opposite sign but identical amplitude. Thus, the DM and CM control loops are fully decoupled and independent. Finally, the DC/DC-stage duty cycles d_p^* and d_n^* are calculated, taking into account the respective measured output capacitor voltages, $V_{out,p}$ and $V_{out,n}$.

4.4 Experimental Results

To validate the proposed VGC and GCC concepts, a hardware demonstrator (see **Fig. 4.10**) of the 3-Φ bB current DC-link PFC rectifier system has been realized according to the specifications shown in **Tab. 4.1** with 1200 V SiC MOSFETs (CREE *C3M0021120K*) in the CSR-stage and 900 V SiC MOSFETs (CREE *C3M0010090K*) in the DC/DC-stage. The experiments focus on operation in the boost-mode, as this can be considered a more challenging scenario

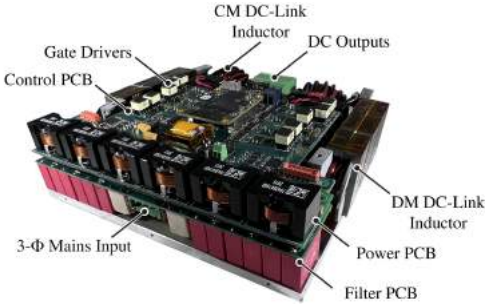

Fig. 4.10: Photo of the realized 10 kW 3-Φ current DC-link buck-boost PFC rectifier (see **Fig. 4.3**) hardware demonstrator, which interfaces a 400 V mains and a DC output voltage in the range of 300 V to 1000 V; detailed specifications are given in **Tab. 4.1**. Employing 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs, the converter achieves a power density of 6.4 kW/dm^3 ($184 \times 172 \times 49$ mm^3) or 107.5 W/in^3 ($7.2 \times 6.8 \times 1.9$ in^3).

(the DC/DC-stage shapes the DC-link current to facilitate 2/3-PWM of the CSR-stage *and* now also realizes the VGC or GCC functionality). The results demonstrate that GCC facilitates compliance with the relevant standards for EV chargers such as UL 2202 [49] and IEC 61851 [119], considering two different grid grounding systems (TT and TN [142]). The VGC and GCC functionalities are achieved without a significant efficiency penalty compared to the state-of-the-art synergetic operation, which is finally verified by measured efficiencies of the realized demonstrator.

4.4.1 Operation with VGC

Fig. 4.11 and **Fig. 4.12** show measured key waveforms when the hardware demonstrator (see **Fig. 4.10**) is operated with the conventional synergetic control [95], i.e., without VGC, or with the proposed VGC, respectively. In both cases, a resistive load of 110 Ω is used and the output voltage is varied to realize operating points between $V_{\text{out}} = 700\,\text{V}$, $P_{\text{out}} = 4.5\,\text{kW}$ and $V_{\text{out}} = 1000\,\text{V}$, $P_{\text{out}} = 9.1\,\text{kW}$. The output midpoint m is left floating, i.e., the grounding impedance is defined by the parasitic capacitances only.

The experimental results confirm the simulation results provided earlier in **Fig. 4.5**. The LF component of the CM voltage v_{mk} originally contains a significant (80 V amplitude) component at 150 Hz (see **Fig. 4.11**), which VGC reduces to almost zero (2.2 V RMS at $V_{\text{out}} = 1000\,\text{V}$, see **Fig. 4.12**). Note that

even though the two output capacitor voltages vary, the total output voltage is always a constant DC value also with the proposed VGC. This confirms that the regulation of the CM voltage does not interfere with the system's DM behavior, i.e., CM and DM quantities can be controlled independently. Finally, **Fig. 4.13** shows the spectra of v_{mk} as calculated from the recorded waveforms, which confirms the suppression of the LF CM voltage components and highlights that the proposed VGC results in the amplitudes of all harmonics below 5 kHz to be less than 1 V.

4.4.2 Operation with GCC

First, the required ground current i_{GND} measurement for GCC is realized by feeding the three input phase conductors through a high-precision *LEM CTSR-0.6P* [143] current sensor with a measurement range of up to 600 mA (see **Fig. 4.3**), which is intended for leakage current measurements in transformerless PV inverters. The bandwidth of the designed ground current controller is 1.5 kHz. The proposed GCC is then tested under the same load scenario as used with VGC above, and the measured key waveforms shown in **Fig. 4.14** are, as expected, very similar to those obtained for VGC (see **Fig. 4.12**). With GCC, however, the ground current i_{GND} is directly regulated instead of the CM voltage v_{mk}. Note that by connecting m to PE, the battery parasitic capacitances, e.g., $C_{\mathrm{b,DC+}}$, $C_{\mathrm{b,DC-}}$, and $C_{\mathrm{b,m}}$ as shown in **Fig. 4.3**, are effectively short-circuited or connected in parallel to the output capacitors, and are thus irrelevant. Therefore, GCC achieves ground current regulation capability without the need for large output capacitances (the demonstrator uses only $C_{\mathrm{out}} = 11.2\,\mu\mathrm{F}$), which facilitates compact non-isolated EV chargers.

4.4.3 TT and TN Grounding Systems

Moreover, two different grid grounding systems [9] must be distinguished when evaluating the performance of the proposed GCC.

- TN (Terra-Neutral): in a TN system, the converter's PE and the mains neutral point (i.e., the star-point of the nearest transformer's LV-side winding system) are directly connected via a dedicated PE conductor. Thus, with respect to **Fig. 4.3**, $R_{\mathrm{G}} = R_{\mathrm{N}} = 0\,\Omega$ models a TN grounding system.

- TT (Terra-Terra): in a TT system, there is no dedicated PE conductor. Instead, the mains neutral point is locally grounded via an impedance in

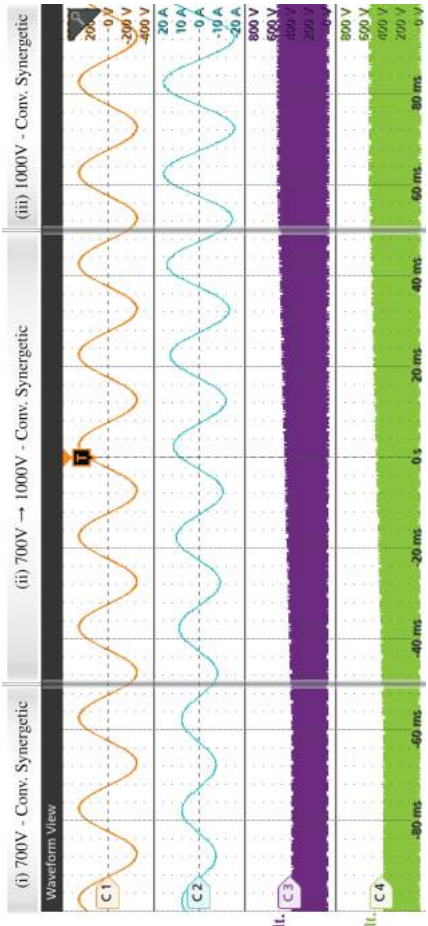

Fig. 4.11: Experimental waveforms of the converter operating with the conventional synergetic control strategy [95], i.e., without activating the proposed VGC or GCC. Using a resistive load of 110 Ω and varying the output voltage, different operating points between V_{out} = 700 V, P_{out} = 4.5 kW and V_{out} = 1000 V, P_{out} = 9.1kW are covered. Note that the CSR-stage operates with 2/3-PWM (boost-mode), and especially note that the CM voltage v_{mk} shows a pronounced 150 Hz component with an amplitude of approximately 80 V, which originates from the SVPWM of the CSR-stage [94].

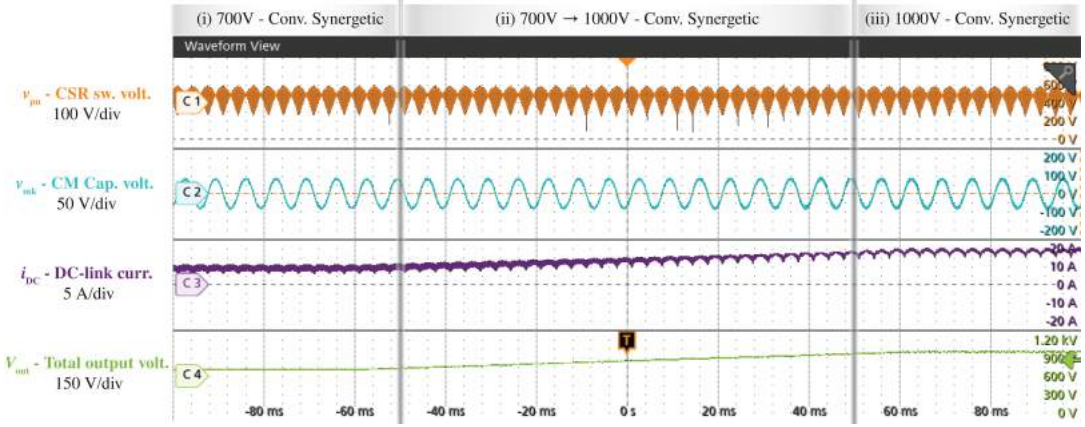

Fig. 4.11 (Continued): Experimental waveforms of the converter operating with the conventional synergetic control strategy [95], i.e., without activating the proposed VGC or GCC. Using a resistive load of 110 Ω and varying the output voltage, different operating points between $V_{\text{out}} = 700\,\text{V}$, $P_{\text{out}} = 4.5\,\text{kW}$ and $V_{\text{out}} = 1000\,\text{V}$, $P_{\text{out}} = 9.1\,\text{kW}$ are covered. Note that the CSR-stage operates with 2/3-PWM (boost-mode), and especially note that the CM voltage v_{mk} shows a pronounced 150 Hz component with an amplitude of approximately 80 V, which originates from the SVPWM of the CSR-stage [94].

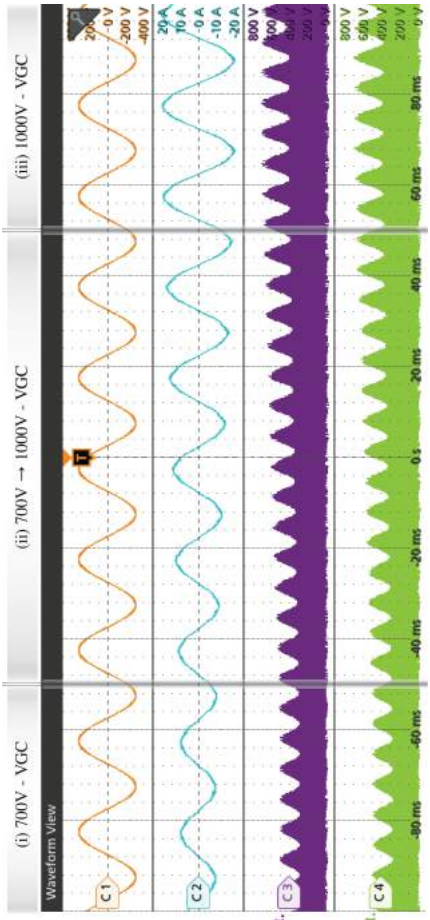

Fig. 4.12: Experimental waveforms of the converter with VGC enabled, which suppresses the LF component of the CM voltage v_{mk} almost completely (see also **Fig. 4.13**). Again (see **Fig. 4.11**), using a resistive load of 110 Ω and varying the output voltage, different operating points between V_{out} = 700 V, P_{out} = 4.5 kW and V_{out} = 1000 V, P_{out} = 9.1kW are covered. Note that the CSR-stage still operates with 2/3-PWM (boost-mode) and also note the expected opposed fluctuation of the two output capacitor voltages, which is visible in the envelopes of the DC/DC-stage HB's switched voltages, v_{qm} and v_{mr}.

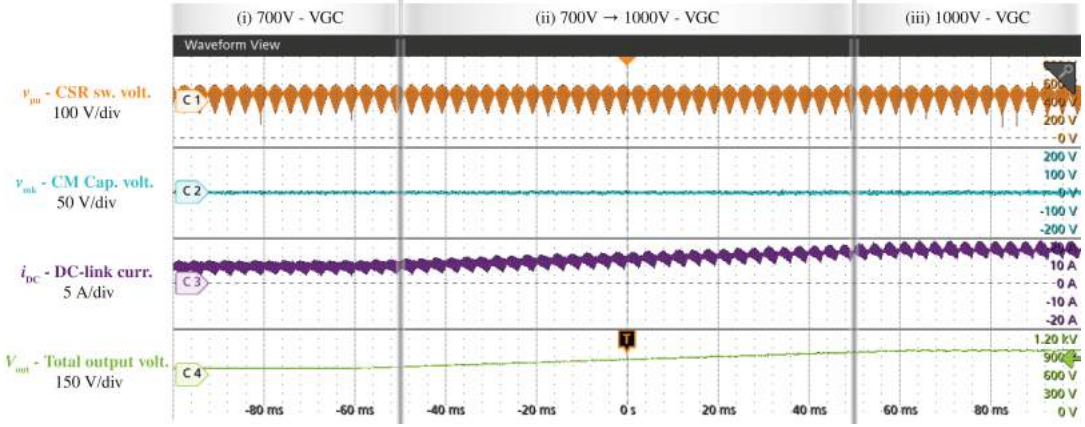

Fig. 4.12 (Continued): Experimental waveforms of the converter with VGC enabled, which suppresses the LF component of the CM voltage v_{mk} almost completely (see also **Fig. 4.13**). Again (see **Fig. 4.11**), using a resistive load of 110 Ω and varying the output voltage, different operating points between $V_{\mathrm{out}} = 700\,\mathrm{V}$, $P_{\mathrm{out}} = 4.5\,\mathrm{kW}$ and $V_{\mathrm{out}} = 1000\,\mathrm{V}$, $P_{\mathrm{out}} = 9.1\,\mathrm{kW}$ are covered. Note that the CSR-stage still operates with 2/3-PWM (boost-mode) and also note the expected opposed fluctuation of the two output capacitor voltages, which is visible in the envelopes of the DC/DC-stage HB's switched voltages, v_{qm} and v_{mr}.

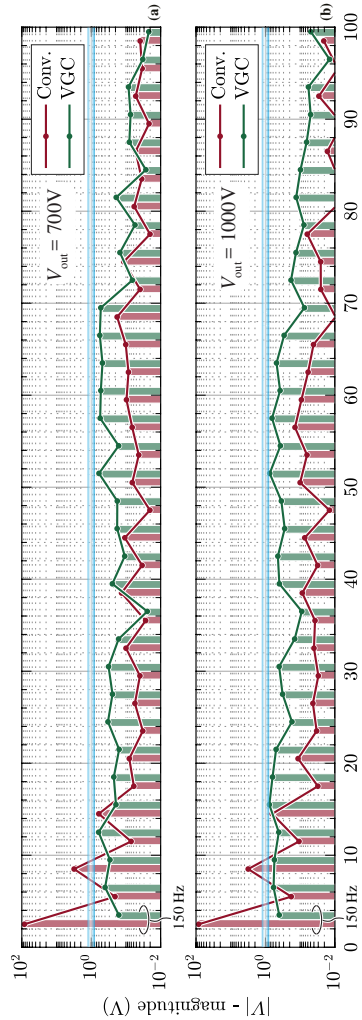

Fig. 4.13: Comparison of the harmonic spectra calculated from measured v_{mk} when operating without **(Fig. 4.11)** and with **(Fig. 4.12)** the proposed VGC at **(a)** V_{out} = 700 V, P_{out} = 4.5 kW and **(b)** V_{out} = 1000 V, P_{out} = 9.1 kW; in all cases from a 50 Hz mains. Note that VGC successfully suppresses LF CM voltage harmonics, i.e., especially the third-harmonic component is reduced from 80 V without VGC to less than 1 V with VGC.

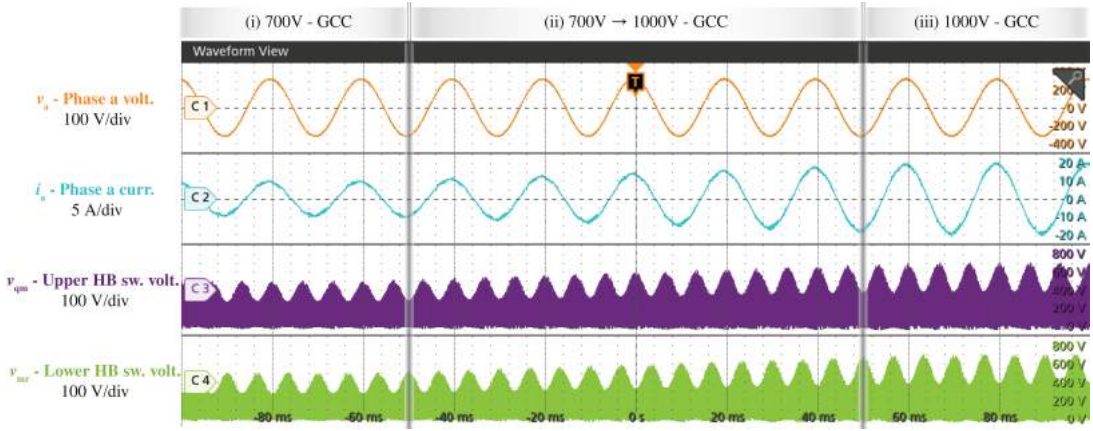

Fig. 4.14: Experimental waveforms of the converter with GCC enabled and using a TN grounding system configuration (direct low-impedance connection of the three-phase source's star-point and the converter's PE, i.e., $R_N = R_G = 0\,\Omega$ in **Fig. 4.3**). Again, using a resistive load of 110 Ω and varying the output voltage, different operating points between $V_{out} = 700\,V$, $P_{out} = 4.5\,kW$ and $V_{out} = 1000\,V$, $P_{out} = 9.1\,kW$ are covered. Note the expected similarity of all waveforms to those obtained with VGC in **Fig. 4.12**. GCC achieves an RMS ground current of less than 5 mA (40 Hz to 1 kHz) as confirmed by a *Fluke 368 FC* leakage current clamp meter.

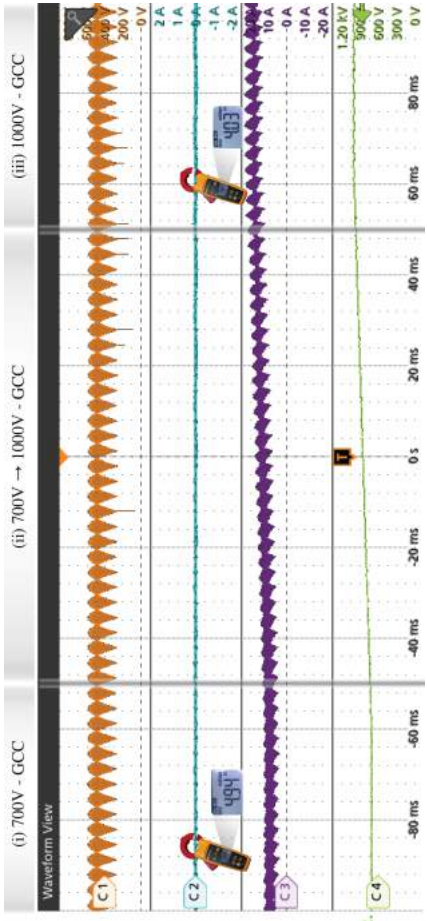

Fig. 4.14 (Continued): Experimental waveforms of the converter with GCC enabled and using a TN grounding system configuration (direct low-impedance connection of the three-phase source's star-point and the converter's PE, i.e., $R_N = R_G = 0\ \Omega$ in **Fig. 4.3**). Again, using a resistive load of 110 Ω and varying the output voltage, different operating points between $V_{out} = 700$ V, $P_{out} = 4.5$ kW and $V_{out} = 1000$ V, $P_{out} = 9.1$ kW are covered. Note the expected similarity of all waveforms to those obtained with VGC in **Fig. 4.12**. GCC achieves an RMS ground current of less than 5 mA (40 Hz to 1 kHz) as confirmed by a *Fluke 368 FC* leakage current clamp meter.

the order of $R_N = 10\,\Omega$ [9], and the converter's PE terminal is connected to ground locally, too, whereby a worst-case grounding impedance of $R_G = 100\,\Omega$ according to IEC60364-4 [142] must be assumed. Note that in contrast to a TN system, any ground current flows through R_G, which results in a corresponding voltage drop between the local PE and true earth and thus potentially endangers a person touching the vehicle chassis while standing next to it. Therefore, for example, UL 2202 and also IEC 61851 require a so-called touch current test (see **Section 4.4.5** below).

In the test setup, R_N and R_G are realized with explicit resistors to mimic the two scenarios.

4.4.4 Ground Current Measurements

Fig. 4.15 shows the measured ground current i_{GND} at different output power levels and for $V_{out} = 700\,V$ and $V_{out} = 1000\,V$. Considering that i_{GND} features an amplitude in the range of several milliamperes only, a special leakage current clamp meter *Fluke 368 FC*, specifically designed for RCD testing, is used to accurately measure i_{GND}. The device performs a true-rms measurement with 0.01 mA resolution, considering a frequency range of 40 Hz to 1 kHz [140].

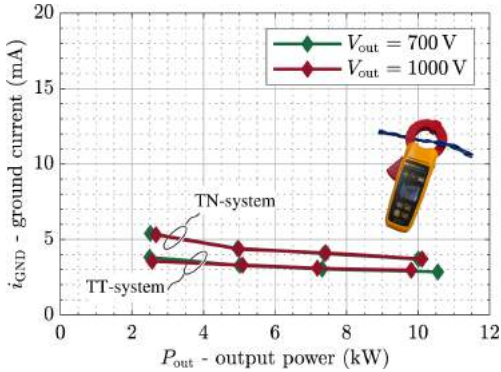

Fig. 4.15: Ground current i_{GND} measured with a leakage current clamp meter *Fluke 368 FC* [140] for operation with two different output voltages and various power levels from 25 % to 100 % of rated load. For both grounding schemes (TT and TN), the measured ground current remains far below RCD trip levels of 30 mA.

Note that i_{GND} occurring in the TN system ($R_G = R_N = 0\,\Omega$ in **Fig. 4.3**) is always larger than i_{GND} resulting in the TT system ($R_G = 100\,\Omega$, $R_N = 10\,\Omega$) due to the lower series impedance. However, all measured values are between 2.8 mA (TT system, 10 kW) and 5.4 mA (TN system, 2 kW), and thus far below the typical RCD trip levels of 30 mA [49,119]. The values are, in particular, also below the permissible PE conductor current in normal operation (7.25 mA RMS for a 10 kW system) according to IEC 61140 [144].

4.4.5 Touch Current Test

Even though the TT system's higher grounding impedances, i.e., R_G and R_N, lead to lower ground current values, the ground current flowing through R_G creates a potential difference between the local EV PE (e.g., the chassis) and true earth, which implies a risk for electric shocks to humans [9]. Thus, standards (UL 2202, IEC 61851) require a so-called touch current test, where an impedance network modeling the frequency-dependent impedance of the human body is connected between the local EV PE (note that in case of GCC, a direct connection of PE and the DC output midpoint m is used) and true earth, see **Fig. 4.16**. The figure also shows the body voltage V_{body} obtained by post-processing the voltage V_{touch} with the impedance networks' transfer

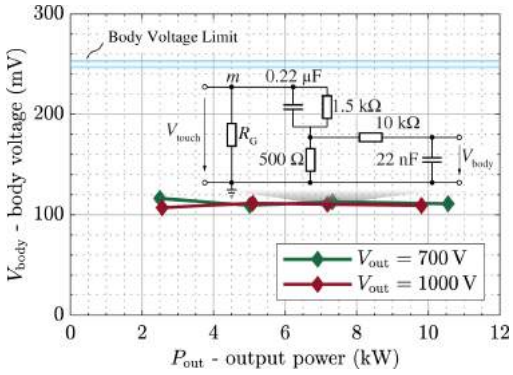

Fig. 4.16: Body voltage V_{body} obtained by processing the measured touch voltage V_{touch} with the transfer function of the human body impedance network according to UL 2202. The converter operates with the proposed GCC at $V_{out} = 700\,V$ and $V_{out} = 1000\,V$, considering different output power levels. In all cases, the measured body voltages of around 110 mV are well below the safe level of 250 mV defined in UL 2202 [49].

function; V_{touch} is measured across the explicit resistor R_{G} used to realize a TT grounding system. The resulting $V_{\text{body}} \approx 110\,\text{mV}$ is well below the most stringent limit of 250 mV defined by UL 2202 [49]. There is little dependence on the output voltage and power level, because mainly LF CM components, which are strongly suppressed by the GCC, contribute to V_{body} (the human body impedance network features a low-pass filter characteristic). Note that only the TT system is considered here since the TN system's dedicated PE conductor ($R_{\text{G}} \approx 0$) prevents any significant voltage between the chassis and true ground (i.e., $V_{\text{touch}} \approx 0$) even for non-zero ground current.

4.4.6 Efficiency

Fig. 4.17 shows the measured system efficiencies when operating the demonstrator at two different output voltages ($V_{\text{out}} = 700\,\text{V}$ and 1000 V), with or without the proposed GCC enabled. All efficiencies have been measured with a Yokogawa WT3000 power analyzer over a wide output power range. GCC has only little impact on the efficiency for the following reasons: (i) The same converter conduction losses, which are solely dependent on the DC-link current if neglecting HF ripples, are generated.[6] (ii) The CSR-stage always operates with 2/3-PWM and hence generates identical switching losses. (iii) Even though the switched voltages of the DC/DC-stage ($V_{\text{out,p}}$ and $V_{\text{out,n}}$) are varying with 150 Hz if GCC is used, the total output V_{out} stays constant. The switching losses of SiC MOSFETs can be modeled as [93]

$$E_{\text{sw}} = (k_1 I_{\text{sw}}^2 + k_2 I_{\text{sw}} + k_3) V_{\text{sw}} + (C_{\text{oss,Q}}) V_{\text{sw}}^2. \tag{4.11}$$

Therefore, considering the *sum* of the upper and lower DC/DC-stage HB's switching losses, the loss contribution resulting from voltage/current overlap (the first term in (4.11)) does not depend on the ratio $V_{\text{out,p}}/V_{\text{out,n}}$ due to the linear dependency on the switched voltage V_{sw}. In contrast, the capacitive loss term shows a quadratic dependency on the switched voltage V_{sw} and hence slightly increased losses are expected if GCC is used. The impact on the overall system efficiency, however, remains very limited as the measurement results demonstrate. All in all, the built 10 kW hardware demonstrator achieves high efficiencies over a wide operating range, reaching a peak efficiency of about 98.5 % at $V_{\text{out}} = 700\,\text{V}$ and rated load.

[6] This applies to the boost-mode operation considered here; note that in the buck-mode, a slightly higher (yet still minor) impact of VGC/GCC on the converter efficiency would be expected as the DC/DC-stage cannot be clamped and because of the necessary increase of the DC-link current by about 5 %.

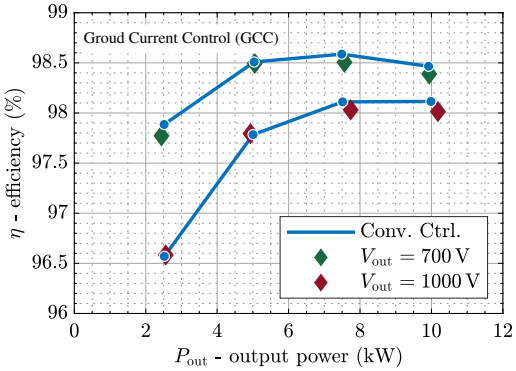

Fig. 4.17: Measured (Yokogawa WT3000) efficiencies of the 10 kW hardware demonstrator (see **Fig. 4.10**) with V_{out} = 700 V and V_{out} = 1000 V (i.e., boost-mode) and for various output power levels. Enabling GCC has almost no impact on the efficiency with or without GCC, and a high peak efficiency of about 98.5 % is achieved.

4.5 Summary

Targeting non-isolated EV chargers supporting a wide output voltage range of 300 V to 1000 V, this chapter proposes virtual grounding control (VGC) for a three-phase (3-Φ) buck-boost (bB) current DC-link AC/DC converter that consists of a buck-type current-source rectifier (CSR) stage and a boost-type three-level DC/DC-stage. Whereas HF CM conducted emissions are limited by the EMI filter, LF CM voltage components inherently resulting from the CSR-stage modulation can be compensated by the DC/DC-stage. This enables VGC to control the LF CM voltage between the DC-output midpoint and an artificial star-point of the three-phase mains (formed by the CSR-stage's DM input capacitors) to zero, i.e., establishes a virtual connection. Furthermore, the proposed ground current control (GCC) allows a direct connection of the DC output midpoint to protective earth (PE), as indicated by the dashed lines in **Fig. 4.3**, by regulating the measured LF CM ground current (i.e., the sum of the of the three mains phase currents) to near zero and hence prevents nuisance tripping of mandatory RCDs. Both, VGC and GCC are experimentally verified with a 10 kW hardware demonstrator considering TT and TN grid grounding systems. With a directly grounded DC output midpoint, the measured LF CM ground leakage current is less than 6 mA RMS for all considered cases, i.e., significantly below the typical 30 mA trip level of RCDs. Similarly, considering the human-body impedance network defined

in UL 2202 (touch current test), the resulting test voltage of 110 mV is clearly below the most stringent limit (250 mV) of the standard. GCC is found to have only a minor impact on the efficiency, with the compact (6.4 kW/dm^3 or 107.5 W/in^3) demonstrator reaching a full-load peak efficiency of 98.5 %.

5

Optimal Synergetic Control of High-Efficiency 3-Φ 3-L Boost-Buck Voltage DC-Link Very Wide Output Voltage Range EV Charger

Chapter Abstract

Universal high-power three-phase mains interfaces for electric vehicle (EV) charging must provide a wide output voltage range (e.g., 200 V to 800 V) and thus provide buck and boost capability. An advantageous realization combining a three-level (3-L) T-type (Vienna) boost-type PFC voltage-source rectifier (VSR) with a 3-L buck-type DC/DC converter stage is presented in this chapter. For high output voltages (boost-mode), the VSR-stage operates with 3/3-PWM, i.e., continuous PWM of all three phases to regulate the output voltage while the DC/DC-stage remains clamped to avoid switching losses. For low output voltages (buck-mode), the DC/DC-stage advantageously controls the DC-link voltage according to a time-varying reference value, which allows to sinusoidally shape the currents of two mains phases, such that the VSR-stage can operate with 1/3-PWM (only one of the three bridge-legs operates with PWM at any given time) with reduced switching losses. This chapter proposes a novel 2/3-PWM scheme for the output voltage transition region, where output voltages are between the buck-mode and the boost-mode. This enables loss-optimum operation (i.e., the minimum number of the VSR-stage bridge-legs operating with PWM, and with the minimum possible DC-link voltage) for any output voltage. Furthermore, this chapter introduces a new synergetic control concept that ensures seamless transitions between the loss-optimum operating modes. A comprehensive experimental verification, including pre-compliance EMI measurements, using a 10-kW hardware demonstrator with a power density of 5.4 kW/dm^3 (91 W/in^3), a peak efficiency of 98.8% at rated power and 560 V output voltage, and >98% efficiency for all operating points with >400 V output voltage and more than about 50% of rated power, confirms the theoretical analyses.

5.1 Introduction

More efficient and compact EV battery chargers are key enablers for the transition from fossil-fuel-based to carbon-free road transportation by electric vehicles (EVs). This transition is an important element for achieving the net-zero CO_2 emission target set forth in the Paris Agreement before 2050 [3]. Typical high-power EV chargers include, first, a three-phase (3-Φ) power-factor-correcting (PFC) AC/DC rectifier stage and a subsequent DC/DC converter stage with high-frequency (HF) isolation (see **Fig. 5.1a**). The isolation stage provides voltage adaption and galvanic isolation, i.e., a large common-mode (CM) impedance between the 3-Φ mains and the vehicle, which ensures electrical safety [13]. Recently, also extensive research has been carried out on non-isolated EV chargers (see **Fig. 5.1b**), where the ground leakage current is monitored by Residual Current Devices (RCDs) to guarantee end-user safety [9].

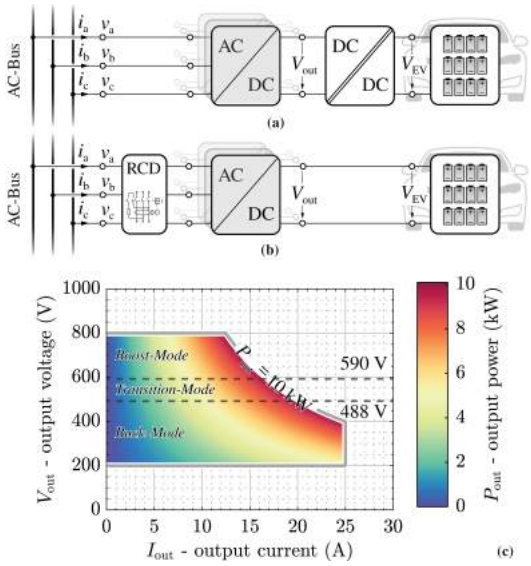

Fig. 5.1: (a) Typical two-stage EV charger architecture including a DC/DC stage with high-frequency (HF) isolation and constant voltage transfer ratio, i.e. a DC transformer (DCX, [23–25]). **(b)** Typical non-isolated EV charger architecture using residual current devices (RCDs) to ensure end-user safety. **(c)** Typical operating range of a 10 kW EV charger module [12, 145]; note the output current limit of $I_{out} = 25$ A.

Universal DC fast chargers should support today's typical EV battery voltages of 200 V to 750 V [12, 62, 64, 145]. To achieve high efficiency, often series resonant DC/DC converters with limited voltage regulation capability, i.e. DC transformers (DCX, [23, 24]) are employed [25]. Assuming a near-unity voltage conversion ratio, the AC/DC PFC rectifier front-end must cover a correspondingly wide output voltage range of 200 V to 800 V and/or the AC/DC front-end must incorporate buck-boost capability. The same is true for non-isolated chargers. **Fig. 5.1c** shows the corresponding operating range of an exemplary 10 kW universal AC/DC EV charger module. Note that several such modules could be paralleled to realize higher output power levels, and that the concepts discussed throughout the article are likewise applicable to units with higher power ratings.

A three-level (3-L) realization of the 3-Φ AC/DC PFC rectifier stage facilitates small EMI filters and hence compact converter realizations [38]. In particular, the T-type (Vienna) voltage source rectifier (VSR)-stage [40, 41] is a

widely used industry-standard solution [42–44]. To achieve boost-buck (Bb) functionality, the boost-type VSR-stage must be combined with a buck-type DC/DC stage (e.g., [45, 46]) as shown in **Fig. 5.2**, which again advantageously is realized as a 3-L structure to reduce the magnetics volume and to enable controllability of the VSR-stage DC-link midpoint potential.

The basic and/or conventional, decoupled operating regime of this two-stage system is as follows: For high output voltages (boost-mode), the VSR-stage switches all three bridge-legs with PWM (3/3-PWM) whereas the DC/DC-stage is clamped ($T_{DC,hp}$ and $T_{DC,hn}$ are always on), i.e., the VSR-stage directly controls the output voltage. Advantageously, the VSR-stage low-frequency (LF) common-mode (CM) voltage injection is selected as proposed in [146] to achieve zero local average (over a pulse period) mid-point current (ZMPC), i.e., $\bar{i}_y \approx 0$, which implies that two small DC-link capacitors are sufficient for high-frequency ripple filtering and that there is no need for large (electrolytic) capacitors as energy buffers.[1] As will be discussed later, such a decoupled operation requires a minimum DC-link voltage of $V_{pn} > 590\,V$ for a 400 V mains (if ZMPC is used), and typical DC-link voltage values would be $V_{pn} = 640\,V$ or $V_{pn} = 720\,V$, taking into account grid voltage fluctuations and some control margin. If the output voltage is lower, the DC/DC-stage must operate with PWM, too, to step-down the DC-link voltage accordingly.

However, recently extensive research has been conducted on a variable DC-link voltage modulation strategy, so-called 1/3-PWM[2]. Proposed in the early 2000 [110, 156, 157], for 2-L converters, the key idea is to utilize the DC/DC-stage for shaping the DC-link voltage such that two phases of the AC/DC rectifier can be clamped and only the remaining phase must operate with PWM; both stages together regulate the mains currents. This leads to a significant reduction of switching losses generated by the VSR-stage. 1/3-PWM has been analyzed mostly for 3-Φ two-stage systems with 2-L voltage DC-link front-ends [110, 153–155], and [158–160] have described the operation of such systems, in the context of motor drive/photovoltaic inverter and EV charger applications, covering a wide output voltage range, i.e., with buck-boost functionality, emphasizing the advantages of 1/3-PWM for low output voltages and the seamless transition to 3/3-PWM for high output voltages.

[1] Note that discontinuous PWM (DPWM) concepts [147–150] (which would allow one bridge-leg of the VSR-stage to be clamped) are not considered because these would lead to relatively high midpoint currents [146, 151, 152].

[2] Note that 1/3-PWM is sometimes also called space vector pulse-width amplitude modulation (SVPWAM) [110], 240°-CPWM [153, 154], or two-phase-clamped DPWM [155].

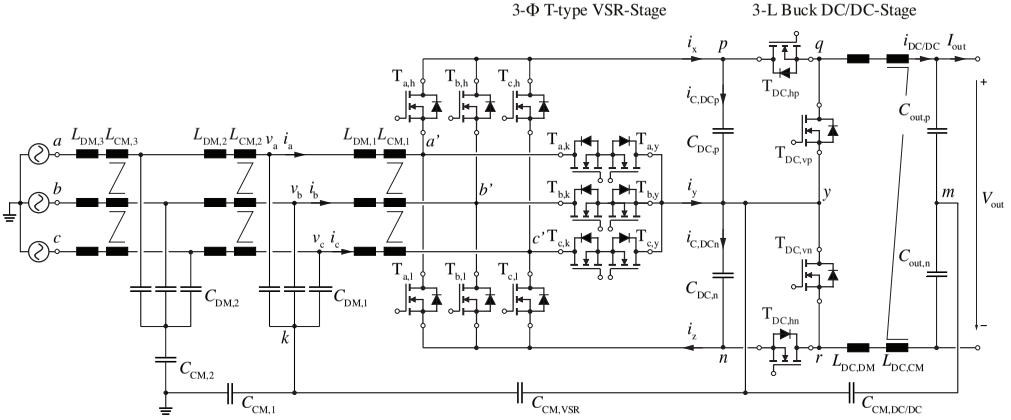

Fig. 5.2: Circuit schematic of the considered 10 kW three-phase (3-Φ) boost-buck (Bb) voltage DC-link PFC rectifier system including CM and DM EMI filter stage, which employs a 3-Φ three-level (3-L) T-type (Vienna) voltage-source rectifier (VSR)-stage cascaded by a 3-L buck-type DC/DC-stage. To filter the common-mode (CM) noise at the DC-link and the DC output port, integrated CM filter capacitors, i.e, $C_{CM,VSR}$ and $C_{CM,DC/DC}$, are applied.

For two-stage systems with 3-L AC/DC front-ends, there are even concepts that operate this front-end only as a mains-frequency commutated three-phase unfolder and use two DC/DC converters to draw according currents from the two DC-link voltages provided by the unfolder (i.e., v_{py} and v_{yn} in **Fig. 5.2**) such that ultimately sinusoidal grid currents result [161–163]. However, in this case, the two DC-link voltages vary widely and reach zero several times per mains period. Therefore, first, the two DC/DC stages are not utilized well as the power they process fluctuates correspondingly, and, second, they must provide boost and buck functionality. Therefore, this approach cannot be adapted for the considered topology with a non-isolated buck-type DC/DC stage.

Alternatively, 1/3-PWM has also been suggested for 3-L NPC AC/DC front-ends combined with isolated DC/DC converters [164], or a combination of a 3-L ANPC front-end with a non-isolated 3-L DC/DC converter [165], and finally for a 3-L VSR-stage front-end with arbitrary (i.e., featuring buck and boost functionality and thus typically isolation) DC/DC converters in [145], which also shows the transition between 1/3-PWM and 3/3-PWM. However, all these studies are based on simulations only. A detailed analysis of the wide-output-voltage-range operation of the 3-Φ 3-L Bb voltage DC-link PFC rectifier system shown in **Fig. 5.2** is thus missing, especially considering the non-isolated buck-type DC/DC-stage where the input voltage can only be stepped down to a lower value but not also be boosted as would typically be feasible with isolated DC/DC-stages [145]. Note further that if isolated DC/DC converters (with buck-boost functionality enabling unconstrained selection of the DC-link voltage) are used, the decision on the optimum operating mode (i.e., 1/3-PWM or 3/3-PWM) is solely based on an optimization, e.g., for maximum efficiency. With non-isolated DC/DC buck converters as considered here, in contrast, for each output voltage a single loss-optimum operating mode with a defined DC-link voltage exists.

This chapter therefore studies the loss-optimum operation of the converter shown in **Fig. 5.2**, considering the wide output voltage range of 200 V to 800 V. Complementing a detailed discussion of the already mentioned 3/3-PWM (for the boost-mode) and 1/3-PWM (for the buck-mode), two new 2/3-PWM modulation methods for the transition-mode (see **Fig. 5.1c**) are proposed in **Section 5.2**. Further, **Section 5.3** introduces a synergetic control concept that ensures loss-optimum converter operation and seamless transitions between the three PWM variants. The proposed synergetic operating principle requires only three (out of five) half-bridges (HBs) to operate with

PWM at any given point in time,[3] and the minimum possible DC-link voltage is used to ensure minimum switching losses. Furthermore, the DC-link capacitors are only needed for switching frequency ripple filtering but do not need to buffer low-frequency power fluctuations, which contributes to a compact realization. Thus, **Section 5.4** provides a detailed experimental verification, including efficiency and conducted EMI measurements, using a 10 kW hardware demonstrator with a peak efficiency of 98.8% at rated power and a power density of 5.4 kW/dm^3 (91 W/in^3), before **Section 5.5** concludes the chapter.

5.2 Operating Principle

The operating principle of the analyzed 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 5.2** is analyzed in this section, considering operation interfacing a 400 V mains with near-unity power factor. Advantageously, the following goals should be achieved for the full output voltage range of 200 V to 800 V:

- A total of three HBs of the VSR-stage and the DC/DC-stage are operating with HF switching while the remaining two HBs are clamped, and the minimum possible DC-link voltage is used. This guarantees loss-optimum operation, i.e., minimum possible switching losses of the whole converter.

- LF currents in the DC-link capacitors are avoided and hence the DC-link capacitors are only needed to filter HF ripples; no bulky energy-buffering DC-link capacitors are needed. Note that 1/3-PWM in the buck-mode (see **Section 5.2.2**) necessitates small DC-link capacitors to minimize the capacitive charging and discharging currents needed to control the DC-link voltage to the time-varying six-pulse shape.

Before discussing the most suitable operating modes for different output voltages, it is useful to first thoroughly explain and derive the range of the CM injection voltage v_{CM} that is available for the modulation of the VSR-stage. Considering Kirchhoff's Voltage Law and the VSR-stage front-end and $v_{\mathrm{CM}} = v_{\mathrm{ky}}$ (occurring across the CM filter capacitor $C_{\mathrm{CM,VSR}}$ as shown in

[3] Note that this corresponds to the minimum of three degrees of freedom needed to control the total constant power flow (two mains currents to ensure PFC operation) and the power sharing between the two DC/DC-stage half-bridges (i.e., the DC-link midpoint potential).

Fig. 5.2, i.e., showing a continuous waveform) all three phases, at the same time, should follow $\bar{v}_{s'k} + v_{CM}$, with

$$-\frac{1}{2}V_{DC} = V_{ny} \leq \bar{v}_{s'k} + v_{CM} \leq V_{py} = \frac{1}{2}V_{DC}, \tag{5.1}$$

where $s \in \{a, b, c\}$ and $\bar{v}_{s'k}$ is the local average DM voltage at the VSR-stage switching node; V_{DC} is the total DC-link voltage, i.e., $V_{DC} = V_{py} + V_{yn}$. Then, assuming $v_{max} = \max(\bar{v}_{s'k})$ and $v_{min} = \min(\bar{v}_{s'k})$, the boundaries of v_{CM} can be derived as

$$-\frac{1}{2}V_{DC} + |v_{min}| \leq v_{CM} \leq \frac{1}{2}V_{DC} - v_{max}, \tag{5.2}$$

which is as a general (time-varying) limitation of the injected CM voltage regardless of specific modulation schemes [150].[4]

5.2.1 Boost-Mode

If the output voltage is sufficiently (depending on the employed CM injection) higher than the peak value of the line-to-line voltages, the converter operates in the boost-mode: the VSR-stage uses 3/3-PWM, where all three HBs of the VSR-stage operate with HF PWM to ensure 3-Φ sinusoidal mains currents and step up the 3-Φ mains voltages to the higher DC output voltage such that the switches $T_{DC,hp}$ and $T_{DC,hn}$ of the DC/DC-stage are permanently on and do not contribute to switching losses. Thus, the DC-link voltage $V_{DC,3/3}$ is simply equal to the output voltage V_{out}, which is the minimum possible DC-link voltage in this case.

3/3-PWM can be simply implemented without any CM injection, i.e., $v_{CM} = 0\,V$ as shown in **Fig. 5.3a**. However, this comes with two main drawbacks: **(i)** limited linear modulation range, i.e., over-modulation for higher modulation indices and **(ii)** large LF currents $\bar{i}_{C,DCp}$ and $\bar{i}_{C,DCn}$ (up to 4 A) flowing through the DC-link capacitors, which are causing LF DC-link voltage variations (not shown in the figure). Such LF DC-link voltage variations increase the transistors' voltage stresses, lead to additional switching losses, and possibly cause LF distortions of the 3-Φ mains currents [166–171]. Importantly, such DC-link voltage variations are inversely proportional to the DC-link

[4]Note that conventional DPWM is achieved if one of the two equalities in (5.2) is attained. E.g., if $v_{CM} = -1/2 V_{DC} + |v_{min}|$, the switching node of the phase with the minimum voltage is connected to negative DC-link potential n, e.g., if $v_{min} = \bar{v}_{a'y}$, the switching node a' is connected to n by turning on $T_{a,l}$. As mentioned above, DPWM would lead to relatively high LF midpoint currents (and hence LF currents in the DC-link capacitors) and is therefore not further considered.

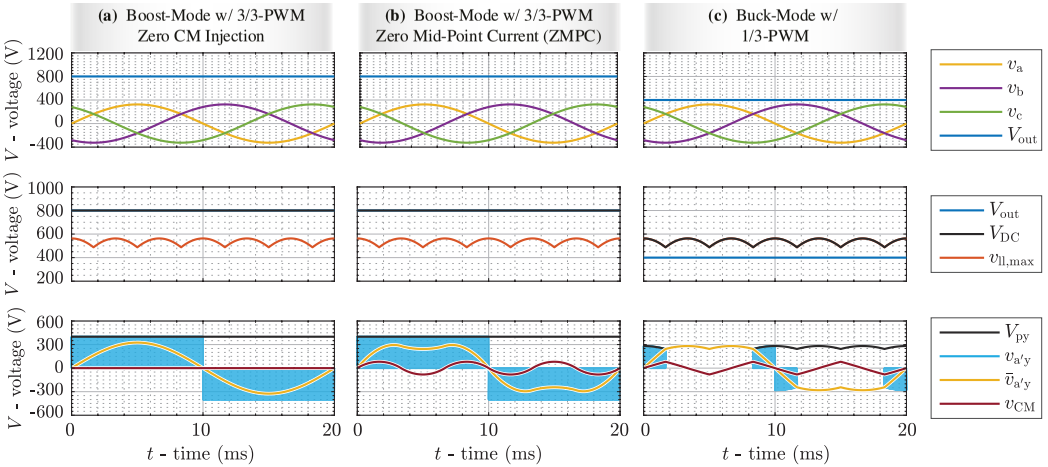

Fig. 5.3: Exemplary key waveforms for operating over a wide output voltage range, i.e., buck-boost operation, of the considered 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 5.2**. In the boost-mode, the VSR-stage operates with 3/3-PWM to ensure 3-Φ sinusoidal mains currents and regulate the output voltage. **(a)** 3/3-PWM can be implemented with zero LF CM injection, however, LF capacitive currents (up to 4 A) flow through the DC-link capacitors (note that here the DC-link capacitors are replaced with ideal voltage sources such that these LF DC-link capacitor currents do not result in LF DC-link voltage variations). Thus, **(b)** another variety of 3/3-PWM with LF CM voltage injection that ensures zero mid-point current (ZMPC) [146] and hence is finally implemented. **(c)** In the buck-mode, the VSR-stage operates with 1/3-PWM [145], where the DC/DC-stage controls the DC-link voltage to follow the six-pulse shape of the envelope of the line-to-line voltage absolute values and hence only one of the VSR-stage's three HBs operates with HF PWM at any given time.

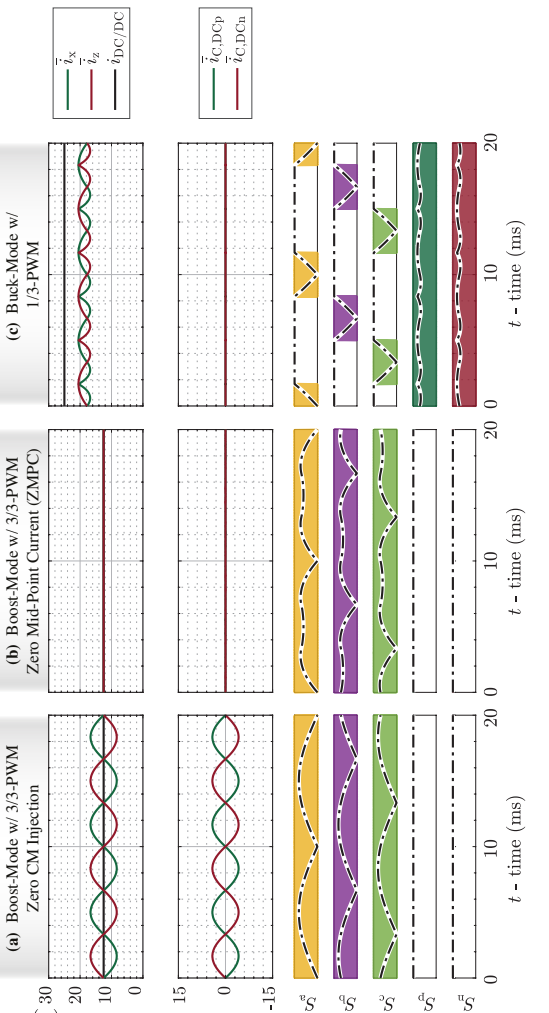

Fig. 5.3 (Continued): Exemplary key waveforms for operating over a wide output voltage range, i.e., buck-boost operation, of the considered 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 5.2**. In the boost-mode, the VSR-stage operates with 3/3-PWM to ensure 3-Φ sinusoidal mains currents and regulate the output voltage. **(a)** 3/3-PWM can be implemented with zero LF CM injection, however, LF capacitive currents (up to 4 A) flow through the DC-link capacitors (note that here the DC-link capacitors are replaced with ideal voltage sources such that these LF DC-link capacitor currents do not result in LF DC-link voltage variations). Thus, **(b)** another variety of 3/3-PWM with LF CM voltage injection that ensures zero mid-point current (ZMPC) [146] and hence is finally implemented. **(c)** In the buck-mode, the VSR-stage operates with 1/3-PWM [145], where the DC/DC-stage controls the DC-link voltage to follow the six-pulse shape of the envelope of the line-to-line voltage absolute values and hence only one of the VSR-stage's three HBs operates with HF PWM at any given time.

capacitance values, which must be small to allow 1/3-PWM in the buck-mode (see below). Therefore, 3/3-PWM with zero CM injection is discarded in this application.

Alternatively, as shown in [146], it is possible to inject a nonzero CM voltage such that the LF mid-point current $\bar{i}_y$ is zero and, as a result, zero LF currents flow through the DC-link capacitors (see **Fig. 5.3b**). The required LF CM injection voltage can be obtained by first considering the expression for the LF mid-point current $\bar{i}_y$ in dependence on the phase modulation indices and the phase currents as

$$\bar{i}_y = \sum_s (1 - \frac{|\bar{v}_{s'k} + v_{CM}|}{V_{DC}/2}) \cdot i_s, \tag{5.3}$$

where $s \in \{a, b, c\}$, and $i_s = G \cdot \bar{v}_{s'k}$ is the phase current of the 3-Φ mains assuming ohmic behavior with a conductance of G. Then, a zero mid-point current (ZMPC) is attained [146] if

$$\bar{i}_y = G \cdot \sum_s (1 - \frac{|\bar{v}_{s'k} + v_{CM}|}{V_{DC}/2}) \cdot \bar{v}_{s'k} = 0. \tag{5.4}$$

From that, the required LF CM voltage $v_{CM,3/3}$ can be calculated as

$$v_{CM,3/3} = v_{CM,ZMPC} = v_{mid} \cdot (1 - \frac{|v_{mid}|}{\max(|v_{min}|, |v_{max}|)}), \tag{5.5}$$

where v_{mid} is defined after sorting the 3-Φ mains voltages such that $v_{max} > v_{mid} > v_{min}$. Injecting $v_{CM,ZMPC}$ ensures zero midpoint current and hence removes the need for bulky DC-link capacitors as energy buffers even without operating the cascaded DC/DC-stage. Note that $v_{CM,ZMPC}$ always lies within the range defined in (5.2) without attaining either equality, i.e., without clamping any of the three phases. Note further that $v_{CM,ZMPC}$ does not depend on the DC-link voltage, so that the result from (5.2) is applicable to the 2/3-PWM-ZMPC method discussed below in **Section 5.2.3**.

Therefore, considering a 400 V mains and (5.1), the converter operates in the boost-mode with 3/3-PWM when $V_{out} > 590$ V (see **Fig. 5.3b**); unless otherwise noted, 3/3-PWM indicates using ZMPC third-harmonic injection modulation. Note that the minimum DC-link voltage allowing 3/3-PWM-ZMPC is slightly larger than the theoretical boost-mode boundary of $\sqrt{3}\hat{V}_{in} = 563$ V as stated in [93].

5.2.2 Buck-Mode

The converter operates in the buck-mode when $V_{\text{out}} < {}^{3}/_{2}\hat{V}_{\text{in}} = 488\,\text{V}$ (see **Fig. 5.3c**) [93]. For such low output voltages, the DC/DC-stage *must* operate. Advantageously, however, the VSR-stage operates with 1/3-PWM where each phase only switches with PWM during one-third of the mains period (see $v_{\text{a'y}}$ in **Fig. 5.3c**), or in other words, two out of the three phases are clamped at all times. To still obtain 3-Φ sinusoidal mains currents, the two DC/DC-stage HBs have to regulate the DC-link voltage V_{DC} following the six-pulse shape of the envelope of the 3-Φ line-to-line mains voltage absolute values; this necessitates relatively small DC-link capacitors as otherwise excessive capacitive currents would occur. Importantly, no additional switching losses are generated since the DC/DC-stage anyway has to be operated to step down the DC-link voltage to a lower output voltage value.

The required time-varying DC-link voltage $V_{\text{DC,1/3}}$ can be derived from (5.2), i.e., if two phases are required to clamp, both equalities in (5.2) must be met and we have

$$V_{\text{DC,1/3}} = v_{\text{max}} - v_{\text{min}}. \tag{5.6}$$

The injected CM voltage $v_{\text{CM,1/3}}$ is

$$\begin{aligned} v_{\text{CM,1/3}} &= \frac{1}{2}V_{\text{DC}} - v_{\text{max}} = -\frac{1}{2}V_{\text{DC}} + |v_{\text{min}}| \\ &= -\frac{1}{2}(v_{\text{max}} - |v_{\text{min}}|). \end{aligned} \tag{5.7}$$

Therefore, the LF CM voltage for 1/3-PWM is fixed and not subject to choice (as for 3/3-PWM). Adding this LF CM injection signal to the voltage references of the VSR-stage modulator automatically ensures the desired clamping of the phases with the maximum and the minimum phase voltages and appropriate PWM of the third phase.

Even though the resulting LF mid-point current of the VSR-stage, $\bar{i}_{\text{y}}$, is not zero for 1/3-PWM (notice $i_{\text{x}} \neq -i_{\text{z}}$ in **Fig. 5.3c**), it is compensated by the cascaded DC/DC-stage that controls the DC-link voltage; this again ensures essentially zero (neglecting the very small current needed to shape the DC-link voltage) LF capacitor current (see $\bar{i}_{\text{C,DCp}} = \bar{i}_{\text{C,DCn}} = 0$ in **Fig. 5.3c**).

5.2.3 Transition-Mode

Whereas for both, boost-mode and buck-mode operation the stated goals (only three HBs switching, minimum DC-link voltage, no LF currents in the

DC-link capacitors) are achieved by the described conventional methods, this is not the case in the transition-mode, i.e., when $488\,\mathrm{V} < V_{\mathrm{out}} < 590\,\mathrm{V}$ (for a 400 V mains). The state-of-the-art transition-mode operation employs a time-varying DC-link voltage $V_{\mathrm{DC}} = \max(V_{\mathrm{out}}, V_{\mathrm{DC},1/3})$ for a direct change from 3/3-PWM to 1/3-PWM, see **Fig. 5.4a**. This approach has been analyzed and implemented for 2-L voltage-source front-ends [160] or 3-L front-ends but with (two) cascaded isolated *buck-boost* DC/DC converters [145]. For these cases, this straightforward approach to handling the transition-mode is feasible since either no mid-point current can occur (2-L front-end) or isolated DC/DC-stages provide full buck-boost functionality.

However, in contrast to two-stage systems with isolated DC/DC-stages [145], here only buck, i.e., step-down, functionality can be achieved by the DC/DC-stage. Therefore, the time-varying VSR-stage DC-rail currents $\bar{i}_{\mathrm{x}}$ *and* $\bar{i}_{\mathrm{z}}$ cannot be larger than the DC/DC-stage inductor current $i_{\mathrm{DC/DC}}$ (see **Fig. 5.2**) to avoid LF current flows in the DC-link capacitors and a corresponding voltage variation (remember that the DC-link capacitors must be comparably small for 1/3-PWM operation). Considering **Fig. 5.4a**, note that the converter operates with 1/3-PWM in interval ① and with 3/3-PWM in interval ③, where in both cases the LF DC-link capacitor currents actually *are* zero. However, the state-of-the-art transition-mode operation cannot satisfy the requirement during the highlighted (pink) interval ②, where, e.g., $\bar{i}_{\mathrm{x}}$ is larger than $i_{\mathrm{DC/DC}}$, and this current difference (shaded) corresponds to $\bar{i}_{\mathrm{C,DCp}}$ flowing through the top DC-link capacitor. These DC-link capacitor currents not only contain LF components but even a DC offset, which implies that practical realizations of the considered topology with finite capacitance DC-link capacitors (note that the DC-link capacitors are replaced in **Fig. 5.4a** with ideal voltage sources for illustrative purposes) could not operate in this mode. There is thus a need to find alternative modulation schemes for the transition-mode that do not cause such LF DC-link capacitor currents; two different options are proposed in the following.

The first possible solution is an extension of 3/3-PWM-ZMPC to the 2/3-PWM-ZMPC (see **Fig. 5.4b**), where the time-varying DC-link voltage allows always to clamp one of the VSR-stage's three phases (the two others are operating with PWM, hence 2/3-PWM). The injected CM voltage is calculated as in (5.5) to ensure zero midpoint current even during 2/3-PWM operation. Then, the DC-link voltage $V_{\mathrm{DC,ZMPC}}$ for 2/3-PWM-ZMPC can be derived from (5.2) when only one equality is attained as

$$V_{\mathrm{DC,ZMPC}} = 2 \cdot \max(-v_{\mathrm{min}} - v_{\mathrm{CM,ZMPC}}, v_{\mathrm{max}} + v_{\mathrm{CM,ZMPC}}). \tag{5.8}$$

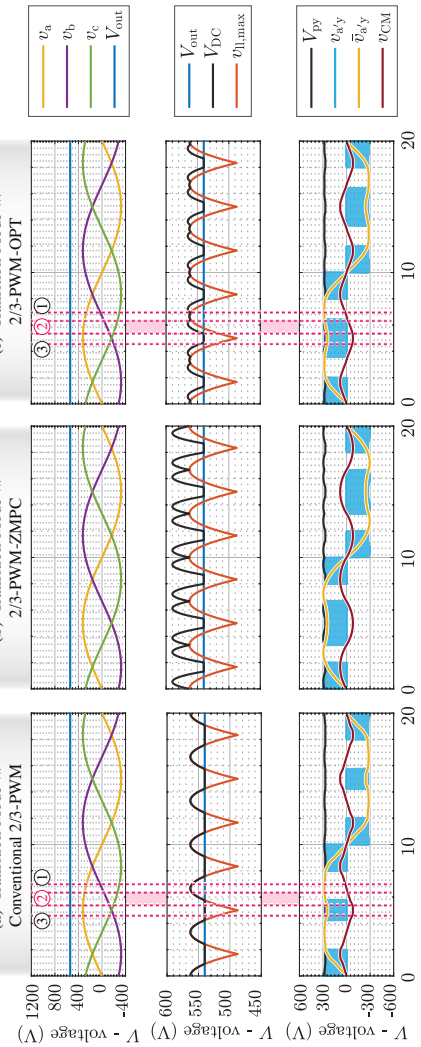

Fig. 5.4: Exemplary key waveforms for operation in the transition-mode at V_{out} = 540 V, considering different modulation schemes. **(a)** Conventional 2/3-PWM with $V_{DC} = \max(V_{out}, V_{DC,1/3})$ uses 3/3-PWM in interval ③ and 1/3-PWM in interval 3/3-PWM ①, but the resulting 2/3-PWM in interval ② generates LF currents in the DC-link capacitors (note that here again the DC-link capacitors are replaced with ideal voltage sources such that these LF DC-link capacitor currents do not result in LF DC-link voltage variations) if the DC/DC-stage does not provide buck-boost functionality as in [145]. **(b)** The proposed 2/3-PWM-ZMPC achieves zero LF current in the capacitors but requires PWM-operation of a total of four HBs and a higher-than-necessary DC-link voltage. **(c)** Proposed loss-optimum 2/3-PWM-OPT with adapted DC-link voltage shape (derivations in the text) that results again in 3/3-PWM in interval ③, 1/3-PWM in interval ①, and, advantageously, also only three HBs switching in interval ② as well as minimum possible DC-link voltage.

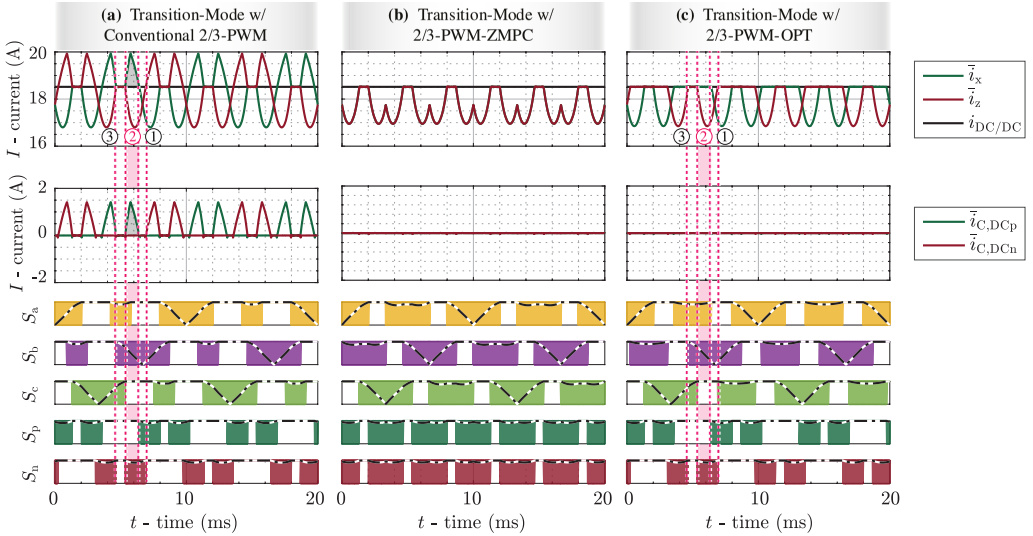

Fig. 5.4 (Continued): Exemplary key waveforms for operation in the transition-mode at $V_{out} = 540\,V$, considering different modulation schemes. **(a)** Conventional 2/3-PWM with $V_{DC} = \max(V_{out}, V_{DC,1/3})$ uses 3/3-PWM in interval ③ and 1/3-PWM in interval 3/3-PWM ①, but the resulting 2/3-PWM in interval ② generates LF currents in the DC-link capacitors (note that here again the DC-link capacitors are replaced with ideal voltage sources such that these LF DC-link capacitor currents do not result in LF DC-link voltage variations) if the DC/DC-stage does not provide buck-boost functionality as in [145]. **(b)** The proposed 2/3-PWM-ZMPC achieves zero LF current in the capacitors but requires PWM-operation of a total of four HBs and a higher-than-necessary DC-link voltage. **(c)** Proposed loss-optimum 2/3-PWM-OPT with adapted DC-link voltage shape (derivations in the text) that results again in 3/3-PWM in interval ③, 1/3-PWM in interval ①, and, advantageously, also only three HBs switching in interval ② as well as minimum possible DC-link voltage.

The DC-link voltage waveform consists of two sections, i.e., 3/3-PWM ($V_{DC} = V_{out}$) is applied while the output voltage defines the minimum DC-link voltage, and $V_{DC} = V_{DC,ZMPC}$ ensures 2/3-PWM operation of the VSR-stage but *both* DC/DC-stage HBs have to operate with PWM (and equal duty cycles) to shape the DC-link voltage accordingly. Consequently, there are time intervals where a total of four HBs operate with PWM (one more than needed), given that the three degrees of freedom that must be controlled remain the same. Hence, 2/3-PWM-ZMPC cannot yet be the loss-optimum operating mode for the transition region.

To arrive at the second proposed solution, it is useful to first reconsider that the state-of-the-art transition-mode operation (see **Fig. 5.4a**) employs 3/3-PWM during interval ③ and 1/3-PWM during interval ①, and only the highlighted interval ② (pink) is problematic due to LF currents through the DC-link capacitors. Therefore, a second modulation scheme, 2/3-PWM-OPT (see **Fig. 5.4c**), is proposed for the highlighted interval ② (pink), which ensures that also the transition-mode does never require more than three PWM-operated bridge-legs. Generally speaking, compared to **Fig. 5.4a**, in interval ② a higher DC-link voltage is necessary to reduce $\bar{i}_x$ such that it is equal or smaller than $i_{DC/DC}$. Equality is preferred in this case such that the upper HB of the DC/DC-stage doesn't have to operate to compensate the current difference between $\bar{i}_x$ and $i_{DC/DC}$.

The operating principle of 2/3-PWM-OPT is explained in detail focusing on the highlighted interval ② (pink) in **Fig. 5.4c** (note that an analogous consideration can be made for $\bar{i}_z$ and the lower DC/DC-stage HB for intervals where the conventional transition-mode operation would result in $\bar{i}_z > i_{DC/DC}$). In this exemplary interval, only the phase voltage v_a, i.e., the maximum absolute phase voltage, is positive and the switch-node potential *a'* is alternatively connected to potentials *p* and *y*. By doing so, the phase current i_a can be modulated such that $\bar{i}_x = i_{DC/DC}$ and hence the upper DC/DC-stage HB can be clamped (see S_p), i.e., $T_{DC,hp}$ is permanently on, to save switching losses generated in the DC/DC-stage. The phase with the middle voltage v_{mid}, i.e., phase *b* in this interval, always has to be operated with PWM to ensure 3-Φ sinusoidal mains currents (similar to 1/3-PWM), but the third phase (the phase with the minimum voltage v_{min}, i.e., here phase *c*) can be clamped to the negative DC-link rail. However, because then $\bar{i}_z$ equals the phase current of phase c, we have $\bar{i}_z \neq i_{DC/DC} = \bar{i}_x$ and therefore the lower HB of the DC/DC-stage must operate with PWM to adapt $\bar{i}_z$ to $i_{DC/DC}$. Thus, two out of the three VSR-stage HBs, i.e., those connected to the phase with the maximum voltage v_{max} and the phase with the middle voltage v_{mid}, and the

lower HB of the DC/DC-stage (see S_n), i.e., three HBs in total, are operating with PWM in interval ②. The VSR bridge-leg corresponding to the phase with the minimum voltage (see S_c) and the upper HB of the DC/DC-stage (see S_p) are clamped as shown in **Fig. 5.4c**. Furthermore, compared to the 2/3-PWM-ZMPC discussed above, a lower DC-link voltage is used.

To obtain an expression for the DC-link voltage needed to realize the advantageous 2/3-PWM-OPT, first consider that a CM voltage $v_{CM,OPT}$ has to be injected to ensure that the VSR modulator clamps the phase with the minimum v_{min} voltage, e.g., phase c in the considered example, to the negative DC-link rail:

$$v_{CM,OPT} = -\frac{V_{DC,OPT}}{2} + |v_{min}|. \tag{5.9}$$

The duty cycle of the phase with the maximum v_{max} voltage, e.g., phase a, considering the forward voltage conversion and the backward current conversion ($i_{DC/DC} = I_{out}$ due to negligible HF components), can be written as

$$d_{max} = \frac{v_{max} + v_{CM,OPT}}{\frac{V_{DC,OPT}}{2}} = \frac{i_{DC/DC}}{i_{max}} = \frac{I_{out}}{i_{max}}, \tag{5.10}$$

and the DC-link voltage $V_{DC,OPT}$ can be calculated by inserting (5.9) into (5.10) as

$$V_{DC,OPT} = 2 \cdot \frac{v_{max} - v_{min}}{1 + \frac{I_{out}}{i_{max}}}. \tag{5.11}$$

Until now, only the case where $|v_{max}| > |v_{min}|$ and hence the clamping of the phase with v_{min} is considered. Similarly, considering also the case $|v_{min}| > |v_{max}|$ where, by analogy, the phase with v_{max} should clamp, the general expression for the DC-link voltage $V_{DC,OPT}$ becomes

$$V_{DC,OPT} = 2 \cdot \frac{v_{max} - v_{min}}{1 + \frac{I_{out}}{\max(|i_{max}|,|i_{min}|)}}. \tag{5.12}$$

Finally, in the optimum transition-mode operation, the time-varying DC-link voltage (see **Fig. 5.4c**) consists of three sections, i.e., ③ $V_{DC} = V_{out}$ (3/3-PWM), ② $V_{DC} = V_{DC,OPT}$ (2/3-PWM-OPT), and ① $V_{DC} = V_{DC,1/3}$ (1/3-PWM), which guarantees a *true* seamless transition between the buck-mode and boost-mode.

The proposed 2/3-PWM-OPT completes thus the wide-range loss-optimal operation of the analyzed converter from **Fig. 5.2**:

- Three HBs of the VSR-stage and the DC/DC-stage are switching in total regardless of the operating mode, which is the minimum number of required active HBs.
- The minimum required DC-link voltage, i.e., the minimum switched voltage, is always employed.
- Furthermore, there are no LF currents in the DC-link capacitors.

Note that the conduction losses in a first step solely depend on the system operating points but not the modulation schemes. Thus, the proposed modulation schemes for buck-, boost-, and transition-modes ensure the minimum switching losses of the VSR-stage and the DC/DC-stage, and hence overall loss-optimum operation can be achieved for any operating point by a suitable synergetic control strategy.

5.3 Synergetic Control Strategy

The proposed synergetic control strategy (see **Fig. 5.5**, based on generic cascaded-loop control strategy from [172, 173]) ensures a collaborative operation of the VSR-stage and the DC/DC-stage such that the converter always operates in the loss-optimum mode for a given operating point and transitions seamlessly between modes, i.e., boost or buck operation in case of changing operating points. The control system is explained in detail in the following subsections.

5.3.1 Output Voltage Control & Mains Current Control

The outermost control loop tracks the output voltage reference V_{out}^* by calculating the corresponding output power reference P_{out}^*, which is used to generate the VSR-stage input reference conductance G^*. The 3-Φ sinusoidal mains current references i_{a}^*, i_{b}^*, and i_{c}^* that are proportional to the corresponding measured 3-Φ input voltages v_{a}, v_{b}, and v_{c}, i.e., ensure purely ohmic operation, directly follow. The 3-Φ mains current errors, resulting from the subtraction of the references from the measured 3-Φ mains currents (boost inductor currents), are fed into the mains current controller to calculate the needed 3-Φ input inductor voltages v_{La}^*, v_{Lb}^*, and v_{Lc}^*. Subtracting these calculated 3-Φ inductor voltage references from the measured 3-Φ input voltages (mains voltage feedforward) sets the 3-Φ VSR-stage voltage references $v_{\text{a}}^{*'}$, $v_{\text{b}}^{*'}$, and $v_{\text{c}}^{*'}$.

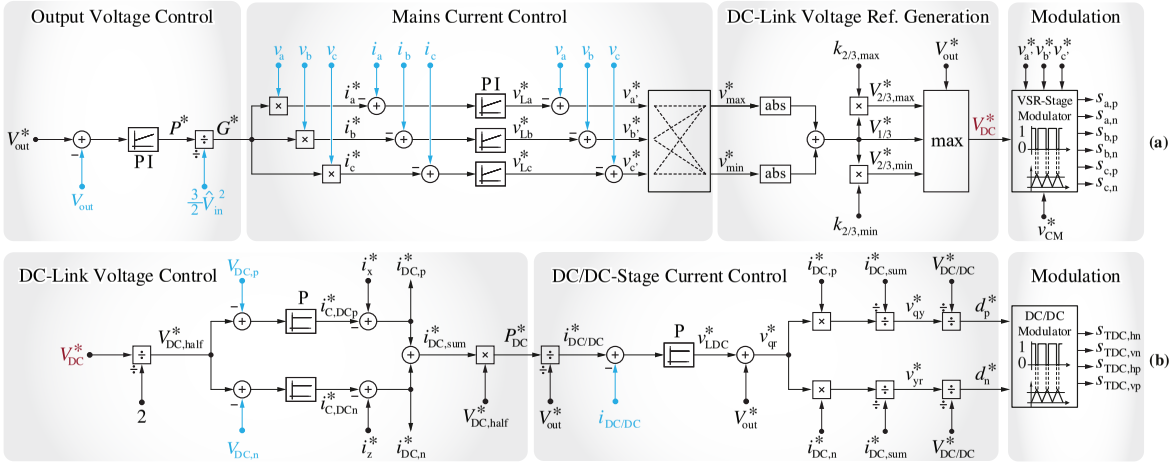

Fig. 5.5: Proposed synergetic control strategy block diagram for the 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 5.2**. **(a)** The VSR-stage controller achieves closed-loop DC output voltage control, ensures 3-Φ sinusoidal-shape mains currents, derives required DC-link voltage V_{DC}^{*} for wide-range loss-optimal operation and generates the VSR-stage gating signals. **(b)** The DC/DC-stage controller achieves closed-loop DC-link voltage V_{DC} and DC/DC-stage inductor current $i_{\mathrm{DC/DC}}$ controls, and ensures proper clamping of zero, one, or both HBs according to different operating modes and modulation schemes.

5.3.2 DC-Link Voltage Reference Generation

The DC-link voltage reference generation block first selects the maximum $v^*_{\max}$ and the minimum $v^*_{\min}$ of the 3-Φ VSR-stage voltage references, which are used to calculate the time-varying DC-link voltage reference $V^*_{1/3}$, i.e., the upper envelope of the absolute value of the 3-Φ VSR-stage voltage references (see **Fig. 5.3c**), for 1/3-PWM in buck-mode operation [145]. The DC-link voltage reference for 3/3-PWM operation simply equals the constant output voltage reference V^*_{out} due to the clamping of the DC/DC-stage (see **Fig. 5.3b**). During 3/3-PWM operation, the VSR-stage alone ensures 3-Φ sinusoidal mains currents; however, with 1/3-PWM, the 3-Φ mains currents are controlled by both, the VSR-stage (directly by the only switching bridge-leg) and the DC/DC-stage (indirectly by the impressed six-pulse-shaped DC-link voltage according to $V^*_{1/3}$).

The DC-link voltage reference $V^*_{2/3} = V_{\text{DC,OPT}}$ in (5.12) for the new 2/3-PWM-OPT can be formulated as a function of voltages instead of currents for simpler control implementation by substituting $I^*_{\text{out}} = {}^{P^*_{\text{out}}}\!/_{V^*_{\text{out}}}$ and

$$i^*_{\max} = G^* \cdot v^*_{\max} = \frac{P^*_{\text{out}}}{{}^3\!/_2 \cdot \hat{V}^2_{\text{in}}} \cdot v^*_{\max}, \tag{5.13}$$

$$i^*_{\min} = G^* \cdot v^*_{\min} = \frac{P^*_{\text{out}}}{{}^3\!/_2 \cdot \hat{V}^2_{\text{in}}} \cdot v^*_{\min} \tag{5.14}$$

to finally obtain

$$\begin{aligned} V^*_{2/3} &= \max(V^*_{2/3,\max}, V^*_{2/3,\min}) \\ &= \max(k_{2/3,\max}, k_{2/3,\min}) \cdot V^*_{1/3} \end{aligned} \tag{5.15}$$

where

$$k_{2/3,\max} = \frac{2}{1 + \frac{{}^3\!/_2 \cdot \hat{V}^2_{\text{in}}}{V^*_{\text{out}} \cdot |v^*_{\max}|}} \quad \text{and} \quad k_{2/3,\min} = \frac{2}{1 + \frac{{}^3\!/_2 \cdot \hat{V}^2_{\text{in}}}{V^*_{\text{out}} \cdot |v^*_{\min}|}}. \tag{5.16}$$

This guarantees again that only the minimum number of HBs are switching in the transition-mode.

The final DC-link voltage reference

$$V^*_{\text{DC}} = \max(V^*_{1/3}, V^*_{2/3,\max}, V^*_{2/3,\min}, V^*_{\text{out}}) \tag{5.17}$$

then guarantees seamless and smooth transitions between different operating modes and modulation schemes over a wide output voltage range. The

corresponding injected CM voltage can then be calculated based on (5.2) and (5.5) as

$$v^*_{\mathrm{CM}} = \max(\min(V^*_{\mathrm{CM},3/3}, \frac{1}{2}V^*_{\mathrm{DC}} - v_{\max}), -\frac{1}{2}V^*_{\mathrm{DC}} - v_{\min}). \tag{5.18}$$

Therefore, the duty cycles of the VSR-stage bridge-legs can be determined, e.g., considering phase *a*, as

$$d^*_{\mathrm{a}} = \frac{v^*_{\mathrm{a}'} + v^*_{\mathrm{CM}}}{\frac{1}{2}V^*_{\mathrm{DC}}}. \tag{5.19}$$

Note that $d^*_{\mathrm{a}} = 1$ is automatically attained whenever possible when operating with 1/3-PWM and 2/3-PWM-OPT as a result of selecting V^*_{DC} and v^*_{CM} as defined above, i.e., each bridge-leg is clamped whenever possible, resulting in minimum VSR-stage switching losses.

5.3.3 DC-Link Voltage Control

The DC-link voltage has to be regulated by the DC/DC-stage in the buck-mode (with 1/3-PWM) and transition-mode (with 2/3-PWM-OPT) operation, which is implemented in the *DC-Link Voltage Control* block shown in **Fig. 5.5**. The voltage error between half of the DC-link voltage $V^*_{\mathrm{DC,half}}$ and the measured upper DC-link capacitor voltage $V_{\mathrm{DC,p}}$ is fed into a P-controller [5] defining the upper DC-link capacitive current reference $i^*_{\mathrm{C,DCp}}$. The LF input current reference $i^*_{\mathrm{DC,p}}$ of the DC/DC-stage upper HB is specified by $i^*_{\mathrm{C,DCp}}$ and the LF current i^*_{x} in the VSR-stage's upper DC rail, which can be calculated with the information of the measured 3-Φ boost inductor currents and the duty cycles. The same logic is applied to the lower DC/DC-stage HB to derive $i^*_{\mathrm{DC,n}}$. Thus, the input power reference P^*_{DC}, the upper input current reference $i^*_{\mathrm{DC,p}}$ and the lower input current reference $i^*_{\mathrm{DC,n}}$ of the DC/DC-stage are forwarded to the following *DC/DC-Stage Current Control* block.

5.3.4 DC/DC-Stage Current Control

The buck-inductor current reference $i^*_{\mathrm{DC/DC}}$, set by P^*_{DC} and V^*_{out}, is compared with the measured value $i_{\mathrm{DC/DC}}$ to determine the required voltage v^*_{LDC} over the DC/DC-stage buck inductor. The sum of v^*_{LDC} and V^*_{out} (output voltage

[5] A P-controller is implemented to avoid a runaway of the voltage error integral if operating with 3/3-PWM and the clamped DC/DC-stage. A PI-controller with an anti-windup functionality is also feasible.

feedforward) leads to the output voltage reference v^*_{qr} of the DC/DC-stage, which needs to be realized by both DC/DC-stage HBs together. Thus, v^*_{qr} is distributed to the two HBs according to the power ratio between the upper and lower HBs; since $V_{DC,p} = V_{DC,n}$, the power ratio equals the ratio between $i^*_{DC,p}$ and $i^*_{DC,n}$. From that, the output voltage reference v^*_{qy} for the upper HB and v^*_{yr} for the lower HB result. Then, the duty cycles are given by

$$d^*_p = \frac{v^*_{qy}}{V^*_{DC/DC}} \quad \text{and} \quad d^*_n = \frac{v^*_{yr}}{V^*_{DC/DC}}, \tag{5.20}$$

where

$$V^*_{DC/DC} = \frac{1}{2}\max(V^*_{2/3,max}, V^*_{2/3,min}, V^*_{1/3}). \tag{5.21}$$

Note that (5.20) automatically ensures optimal clamping of both HBs in the different operating modes:

- In the buck-mode ($V^*_{out} < 488\,V$), $V^*_{DC/DC} = 1/2 V^*_{1/3}$ since $\max(k_{2/3,max}, k_{2/3,min}) < 1$ is always attained[6] and hence $V^*_{2/3,max} < V^*_{1/3}$ and $V^*_{2/3,min} < V^*_{1/3}$. Both DC/DC-stage HBs are switching to regulate the DC-link voltage into the required six-pulse shape.

- In the boost-mode, if neglecting v^*_{LDC}, $V^*_{out} > 590\,V$ leads to $v^*_{qy} = v^*_{yr} = 1/2 V^*_{out} \geq V^*_{DC/DC} = 1/2\,\max(V^*_{2/3,max}, V^*_{2/3,min})$. Thus, $T_{DC,hp}$ and $T_{DC,hn}$ of the DC/DC-stage are permanently on since d^*_p and d^*_n are always larger than unity and saturate the corresponding modulator.

- In the transition-mode ($488\,V < V^*_{out} < 590\,V$), when operating in 2/3-PWM-OPT and $|v_{max}| > |v_{min}|$, the upper DC/DC-stage HB should be clamped (see highlighted interval ② in **Fig. 5.4c**). Neglecting v^*_{LDC} and $i^*_{DC,p}$, we have $v^*_{qy} = 1/2\ V^*_{2/3,max} = V^*_{DC/DC}$ and $v^*_{yr} < V^*_{DC/DC}$, such that the upper HB is permanently conducting ($d^*_p = 1$) and the lower HB is switching ($d^*_n < 1$).[7]

[6] $\max(k_{2/3,max}, k_{2/3,min}) \leq \dfrac{2}{1 + \frac{3/2 \cdot \hat{V}^2_{in}}{V^*_{out} \cdot \hat{V}_{in}}} = \dfrac{2V^*_{out}}{V^*_{out} + 3/2\hat{V}_{in}} < 1$ during the buck-mode operation because of $V^*_{out} < 3/2\hat{V}_{in}$.

[7] $v^*_{qy} = i^*_x/(i^*_x + i^*_z)\ V^*_{out} = V^*_{DC/DC}$ considering $i^*_x = I^*_{out}$ and $i^*_z = (V^*_{out} - V^*_{DC/DC})/V^*_{DC/DC}\ I^*_{out}$ during the highlighted interval when 2/3-PWM is applied.

Tab. 5.1: Demonstrator system specifications and list of the main components; the EMI filter component values are listed in **Tab. 5.2**.

	Description	Value
V_{in}	RMS phase voltage	230 V
V_{out}	DC output voltage range	200 V ~ 800 V
P_{out}	Rated output power	10 kW
$I_{out,max}$	Output current limit	25 A (V_{out} < 400 V)
T_{VSR}	VSR-stage semicond. $T_{h\{l\}}$	C3M0016120K, 1200 V, 16 mΩ
	VSR-stage semicond. $T_{k\{y\}}$	C3M0030090K, 900 V, 30 mΩ
f_{VSR}	VSR-stage sw. freq.	100 kHz
$T_{DC/DC}$	DC/DC-stage semicond.	C3M0010090K, 900 V, 10 mΩ
$f_{DC/DC}$	DC/DC-stage sw. freq.	200 kHz
C_{DC}	DC-link cap.	2×11.2 µF
C_{out}	Output cap.	2×5 µF
$L_{DM,1}$	Main input DM ind.	3×194 µH (2×KoolMu60 E43/17, 25 turns)
$L_{CM,1}$	Main input CM ind.	4.6 mH (2×VAC 45/30/15, 12 turns)
$L_{DC,DM}$	Output DM ind.	2×34 µH (2×N87 E40/16/12, 11 turns)
$L_{DC,CM}$	Output CM ind.	2.6 mH (VAC 40/25/15, 10 turns)
$C_{CM,VSR}$	VSR-stage CM cap.	40 nF
$C_{CM,DC/DC}$	DC/DC-stage CM cap.	40 nF

5.4 Hardware and Experimental Verification

A hardware demonstrator is built to experimentally verify the proposed synergetic control structure over the wide output voltage operating range under different modulation schemes. Significant power efficiency improvements are observed by implementing 1/3-PWM in the buck-mode and the new 2/3-PWM-OPT in the transition-mode. Furthermore, conducted EMI noise emission measurements are provided.

5.4.1 Hardware Demonstrator

Fig. 5.6 shows the 10 kW hardware demonstrator of the analyzed 3-Φ Bb voltage DC-link PFC rectifier system and its exploded view. The prototype

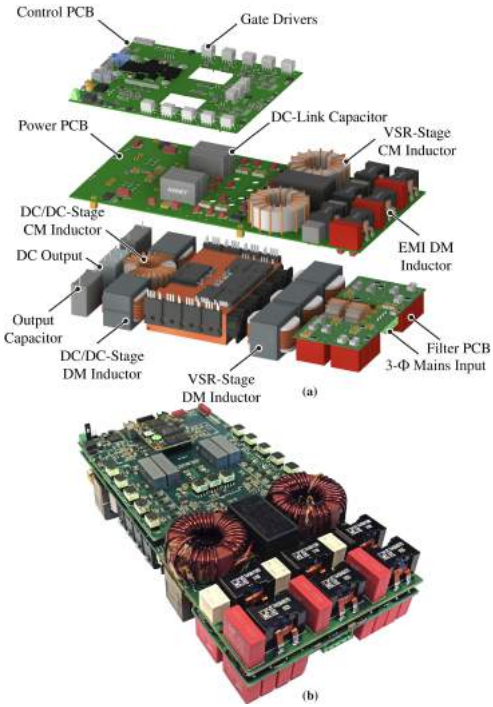

Fig. 5.6: (a) Exploded view and **(b)** photo of the realized 10 kW hardware demonstrator with a power density of 5.4 kW/dm^3 (91 W/in^3) and dimensions of $250 \times 130 \times 57$ mm^3 ($9.8 \times 5.1 \times 2.2$ in^3), featuring the power circuit shown in **Fig. 5.2**. The demonstrator operates from the 400 V 3-Φ mains and provides a wide output voltage of 200 V to 800 V. The maximum output current is limited to 25 A.

achieves a high power density of 5.4 kW/dm^3 (91 W/in^3). The realized demonstrator is composed of three separate PCBs, including a 6-layer control PCB (FPGA, gate drivers, measurement data acquisition, etc.), an 8-layer power PCB carrying the main power converter components, and a 4-layer EMI Filter PCB. The system specifications and key components are listed in **Tab. 5.1**.

5.4.2 Experimental Waveforms

Fig. 5.7 shows measured key waveforms of the 10 kW hardware demonstrator for the three different loss-optimal operating modes, i.e., phase *a* voltage

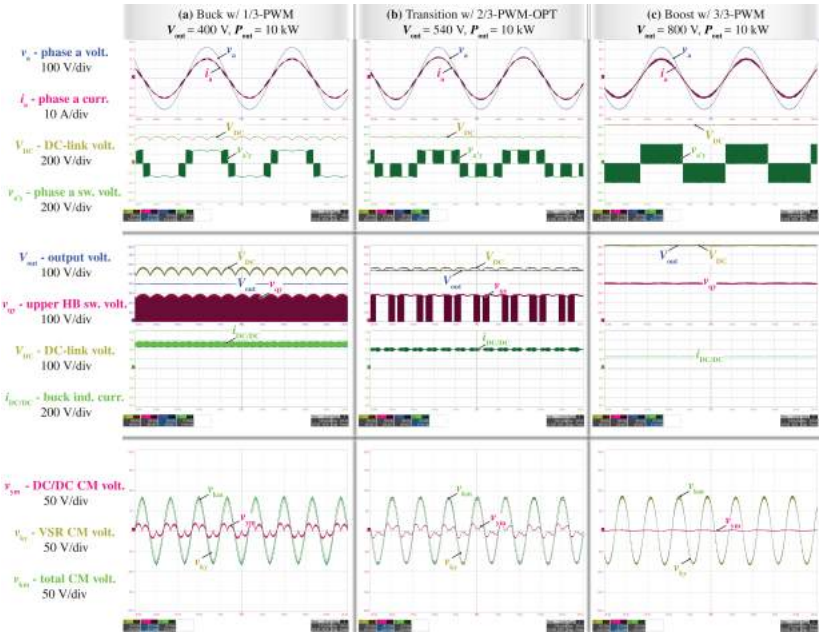

Fig. 5.7: Experimental waveforms of the converter shown in **Fig. 5.2** with the proposed synergetic control strategy when operating in **(a)** ***buck-mode***, **(b)** ***transition-mode*** and **(c)** ***boost-mode*** at 10 kW nominal output power. In the ***buck-mode*** operation, the DC/DC-stage regulates the DC-link voltage V_{DC} to the six-pulse shape to facilitate 1/3-PWM of the VSR-stage where only one phase is switching at any given time (see the switched voltage of phase a, $v_{a'y}$). In the ***transition-mode***, the proposed 2/3-PWM-OPT is applied to ensure not only the automatic and seamless transition between buck- and boost-modes, but also for guaranteeing loss-optimal operation, i.e., only three HBs are switching at any given time. Finally, 3/3-PWM is applied in the VSR-stage during the boost-mode operation while the DC/DC-stage is clamped ($T_{DC,hp}$ and $T_{DC,hn}$ are permanently on to avoid switching losses).

v_a, phase a current i_a, DC-link voltage V_{DC}, and output voltage V_{out}, and proves basic converter functionalities. Furthermore, the switched voltage of phase a, $v_{a'y}$, clearly differentiates the switching or clamping states of the corresponding VSR-stage bridge-leg. Similarly, the switched voltage of the DC/DC-stage's upper HB, v_{qy}, indicates the clamping intervals of the DC/DC-stage. Two integrated CM filters of the VSR-stage and the DC/DC-stage (i.e., capacitive connection between the artificial mains star point k and the DC-link midpoint y; and between the output midpoint m and y, respectively) are used to suppress HF CM noise at the DC-link and DC output midpoints and the measured CM capacitor voltages v_{ym} and v_{ky} thus mainly consist of LF components.

Fig. 5.7a presents the buck-mode operation with $V_{out} = 400\,V$, $P_{out} = 10\,kW$. The DC/DC-stage regulates V_{DC} into the six-pulse shape, i.e., the envelope of the line-to-line voltage absolute values to achieve 1/3-PWM operation (see $v_{a'y}$) of the VSR-stage, i.e., each phase switches only during one-third of a mains period. **Fig. 5.7b** presents the transition-mode operation with $V_{out} = 540\,V$, $P_{out} = 10\,kW$. Note that V_{DC} is in excellent agreement with the analytical reference shown in **Fig. 5.4c**, and the extended clamping interval of the DC/DC-stage can be seen in v_{qy}. **Fig. 5.7c** shows boost-mode operation with $V_{out} = 800\,V$, $P_{out} = 10\,kW$ where all three phases of the VSR-stage switch all the time and the DC/DC-stage clamps, i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on.

The proposed control strategy is verified in **Fig. 5.8**, where automatic and smooth transitions between different operating modes are achieved when the output voltage reference values increase from 460 V to 600 V. Both modulation schemes proposed for the transition-mode are compared, i.e., **(a)** 2/3-PWM-ZMPC and **(b)** the proposed loss-optimal 2/3-PWM-OPT. Note that to implement the transition mode with the (sub-optimal) 2/3-PWM-ZMPC, a slight modification of the control structure from **Fig. 5.5** is needed; specifically, $V^*_{2/3}$ has to be changed to the DC-link voltage reference $V^*_{DC,\,ZMPC}$ from (5.8).

5.4.3 Efficiency Measurements

The achievable efficiency improvement is quantified on the realized 10 kW hardware demonstrator shown in **Fig. 5.6** considering operation over a wide output voltage range (from 200 V to 800 V) and a wide output power range (from 25 % to 100 % of the rated load). The (measured) 3D efficiency surface (see **Fig. 5.9a**), featuring a fairly flat characteristic over the full operating area, is first shown for the proposed loss-optimal modulation scheme, i.e., 1/3-PWM

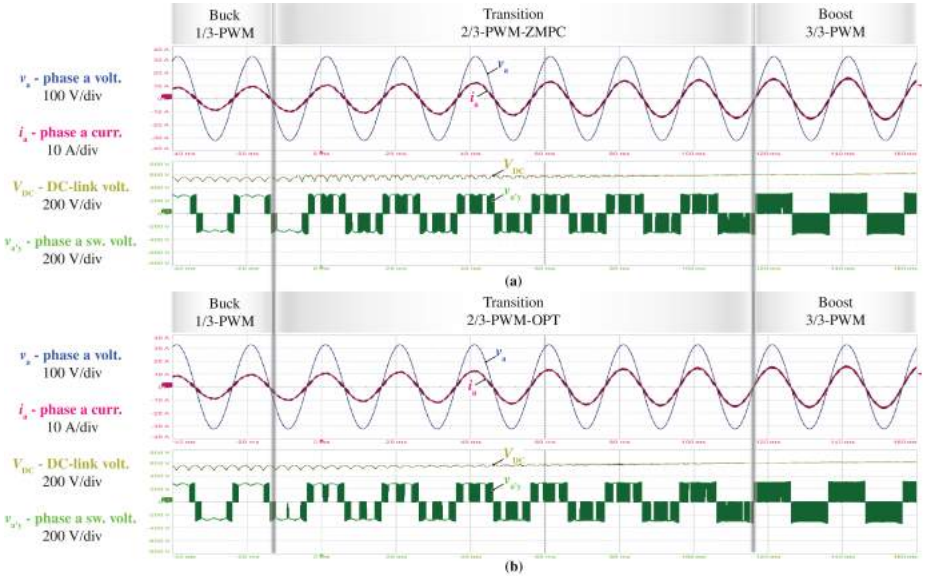

Fig. 5.8: Experimental waveforms of the converter shown in **Fig. 5.2** with the proposed synergetic control strategy operating with a constant resistive load of 50 Ω and a linearly increasing output voltage $V_{\text{out}} = 460\,\text{V} \sim 600\,\text{V}$, where different modulation schemes, i.e., **(a)** 2/3-PWM-ZMPC, and **(b)** 2/3-PWM-OPT, are applied in the transition-mode. 2/3-PWM-OPT achieves an automatic and seamless transition from the buck-mode to the boost-mode with the proposed control structure (see **Fig. 5.5**) with an extended clamping time of the VSR-stage bridge-legs (see $v_{a'y}$) and also of the DC/DC-stage bridge-legs (not shown), compared to 2/3-PWM-ZMPC. Note further the different shapes of the DC-link voltage V_{DC} between the modes (see also **Fig. 5.4**).

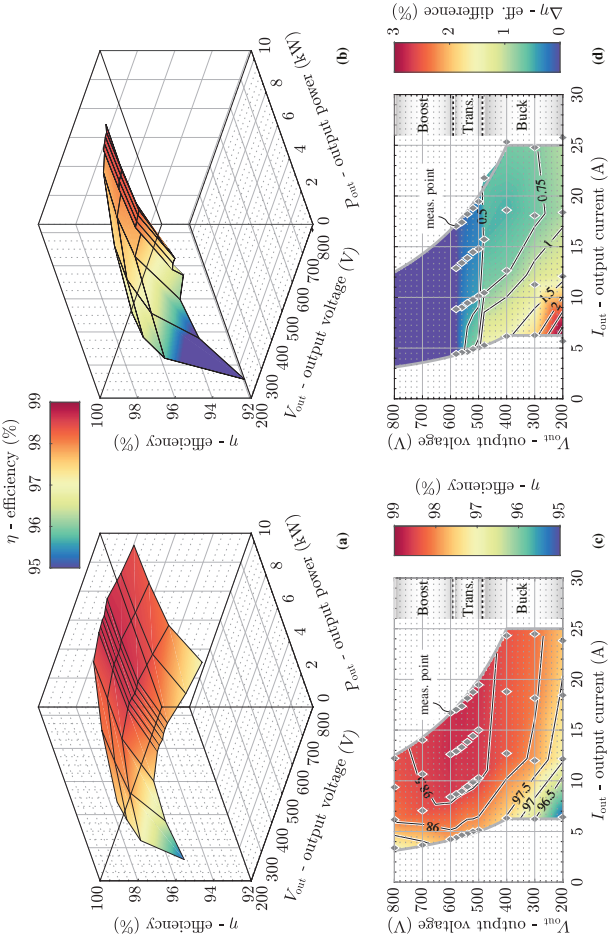

Fig. 5.9: Measured (Yokogawa WT3000) efficiencies of the realized 10 kW hardware demonstrator shown in **Fig. 5.6**, using **(a)** the proposed loss-optimal modulation scheme (1/3-PWM in the buck-mode, 2/3-PWM-OPT in the transition mode, and 3/3-PWM (with ZMPC) in the boost-mode) and **(b)** the conventional operating scheme, i.e., 3/3-PWM (without ZMPC) in the buck-mode and 2/3-PWM-ZMPC in the transition-mode. **(c)** The efficiency contours correspond to **(a)** and indicates the measured points. **(d)** Efficiency difference between the proposed **(a)** and state-of-the-art **(b)** methods, highlighting efficiency improvements of up to 3.2% and 0.8% in the buck-mode and the transition-mode, respectively. Note that efficiency surfaces and curves are linearly interpolated from measured points.

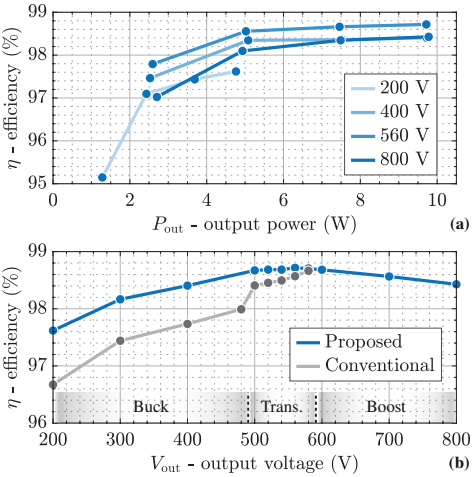

Fig. 5.10: Measured (Yokogawa WT3000) efficiency curves, i.e., **(a)** efficiency versus output power P_{out} (using the proposed loss-optimal modulation scheme) and **(b)** efficiency versus output voltage V_{out} at rated power (or rated output current below 400 V), where also the curve for conventional operation is shown as a reference. A peak efficiency of 98.8 % when $V_{out} = 560$ V and $P_{out} = 10$ kW can be achieved.

in the buck-mode, 2/3-PWM-OPT in the transition-mode, and 3/3-PWM in the boost-mode. This surface is further visualized as a 2D contour plot in **Fig. 5.9c**, where the measured operating points are indicated. It is clear that high-efficiency operation, e.g., efficiencies above 98%, are achieved over a large part of the wide output voltage and power range. **Fig. 5.10a** shows efficiency versus output power for different output voltages and **Fig. 5.10a** shows efficiency versus output voltage at rated power, where the peak efficiency of 98.8% at 10 kW can be noticed.

To highlight the efficiency advantages of using 1/3-PWM over 3/3-PWM in the buck-mode, efficiencies when operating with 3/3-PWM[8] in the buck-mode and the (sub-optimal) 2/3-PWM-ZMPC in the transition-mode are also measured (see **Fig. 5.9b**). The efficiency improvements are quantified in the contour plot shown in **Fig. 5.9d**. Clearly, using 1/3-PWM in the buck-

[8]Using $V_{DC} = \sqrt{3}\hat{V}_{in}$, i.e., the minimum possible value for 3/3-PWM, and triangular third harmonic injection, i.e., $v_{CM} = -1/2(v_{max} + v_{min})$ (i.e., the same LF CM injection as results for 1/3-PWM), is used for a fair comparison in the buck-mode. In the boost-mode, however, 3/3-PWM-ZMPC is used as before. The same approach is also used in the later EMI comparison of 1/3-PWM and 3/3-PWM in the buck-mode.

Tab. 5.2: EMI Filter Specifications.

	Description	Value
$C_{DM,1}$	1st EMI DM film capacitor	3×3 µF
$C_{CM,1}$	1st EMI CM ceramic capacitor	18 nF
$L_{DM,2}$	2nd EMI DM inductor	3×15 µH, *WE 7443641500*
$C_{DM,2}$	2nd EMI DM film capacitor	3×6 µF
$L_{CM,2}$	2nd EMI CM inductor	870 µH, VAC 25/16/10, 8 turns
$C_{CM,2}$	2nd EMI CM ceramic capacitor	18 nF
$L_{DM,3}$	3rd EMI DM inductor	3×4.7 µH, *WE 7443640470*
$L_{CM,3}$	3rd EMI DM inductor	870 µH, VAC 25/16/10, 8 turns

mode realizes a significant improvement of up to 3.2%, and the proposed 2/3-PWM-OPT gives still a notable improvement of 0.8% over 2/3-PWM-ZMPC. **Fig. 5.10b** visualizes the efficiency gains at rated power for the different output voltages. Note that no efficiency difference is expected in the boost-mode, where 3/3-PWM (with ZMPC) is used in all cases.

5.4.4 EMI Measurements

Finally, conducted EMI tests have been carried out to assess the compliance of the realized 10 kW hardware demonstrator (see **Fig. 5.6**) with the limits according to CISPR 11 / Class A for the frequency range of 150 kHz to 30 MHz. The designed EMI filter parameters are listed in **Tab. 5.2**. The test setup consists of a Rhode & Schwarz ESPI3 EMI test receiver and a Rhode & Schwarz ESH2-Z5 three-phase LISN.

First, **Fig. 5.11** presents EMI measurement results when operating in the buck-mode (V_{out} = 400 V, P_{out} = 5 kW) with different modulation schemes, i.e., 3/3-PWM and 1/3-PWM. 8.5 dBµV more noise emission is measured if 3/3-PWM is applied instead of 1/3-PWM, which can be explained by the following two reasons:

- The EMI noise sources of the VSR-stage, in a first step, can be simply represented by the RMS value of all HF components [174], i.e., the HF components of $v_{CM} = 1/3 \cdot (v_{a'y} + v_{b'y} + v_{c'y})$ and of $v_{DM} = v_{a'y} - v_{CM}$ (phase *a* as an example). Thus, 1/3-PWM achieves 2 dBµV less DM noise emission and 4 dBµV less CM noise emission compared with the conventional 3/3-PWM as shown in **Fig. 5.12**.

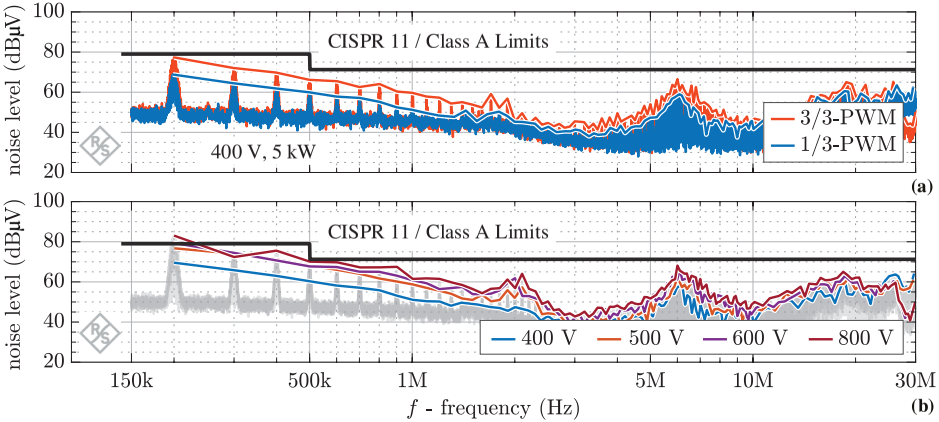

Fig. 5.11: Conducted EMI noise emission measurements. **(a)** Comparison between 1/3-PWM and 3/3-PWM operating at $V_{\text{out}} = 400\,\text{V}$ and $P_{\text{out}} = 5\,\text{kW}$, i.e., in the buck-mode. **(b)** Pre-qualification measurements at rated power and for four typical output voltages which are measured on the realized 10 kW hardware demonstrator shown in **Fig. 5.6**. The CISPR 11 peak (PK) detector has been used with a 4 kHz step size, 9 kHz resolution bandwidth (RBW), and 1 ms measurement time. The local peak values are connected as an envelope for easier comparisons between different operating points.

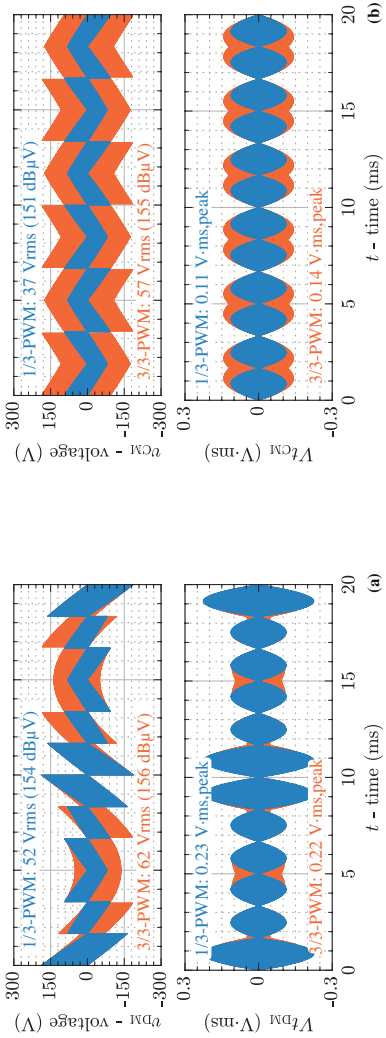

Fig. 5.12: Comparison of analytically calculated HF **(a)** DM and **(b)** CM noise source characteristics of the VSR-stage using 1/3-PWM (blue) and 3/3-PWM (orange) for operation in the buck-mode at V_{out} = 400 V. Note that the operating conditions for the DC/DC-stage are similar in both cases and hence neglected.

- The voltage-time area (peak value) stresses applied to the EMI DM/CM inductors are also compared between 1/3-PWM and conventional 3/3-PWM in **Fig. 5.12**. Similar DM stresses but significantly increased CM stress, i.e., a 33% larger applied voltage-time area compared to 1/3-PWM, are observed when using 3/3-PWM.

Note that the DC/DC-stage operates similarly for both 1/3-PWM and 3/3-PWM employed in the buck-mode, i.e., both HBs are always switching but only at slightly different DC-link voltages, so the impact from the DC/DC-stage can be neglected. Furthermore, this analysis also validates that the EMI filter designed for 3/3-PWM can be directly used in 1/3-PWM operation without any additional EMI redesign or filter modifications.

Finally, **Fig. 5.11b** summarized conducted EMI pre-compliance measurements of the hardware demonstrator for four typical output voltage operating points and rated output power, where always the loss-optimal modulation method is used (i.e., 1/3-PWM in the buck-mode for $V_{\text{out}} = 400\,\text{V}$, 2/3-PWM-OPT in the transition mode for $V_{\text{out}} = 500\,\text{V}$, and 3/3-PWM (with ZMPC) in the boost-mode for $V_{\text{out}} = 600\,\text{V}$ and $V_{\text{out}} = 800\,\text{V}$). Except for some minor violations at the maximum output voltage, which are likely due to partial saturation of CM chokes and could be addressed by minor redesigns, the demonstrator meets the CISPR 11 / Class A limits.

5.5 Summary

Aiming for a standard building block for isolated and non-isolated EV chargers, this paper comprehensively studies and analyzes a three-phase (3-Φ) boost-buck (Bb) voltage DC-link AC/DC converter that consists of a 3-Φ three-level (3-L) T-type (Vienna) voltage-source rectifier (VSR)-stage and a 3-L buck-type DC/DC-stage. Whereas loss-optimum modulation schemes for the buck-mode (1/3-PWM) and for the boost-mode (3/3-PWM) are known, this paper proposes a new modulation scheme for the transition-mode (i.e., for output voltages between buck-mode and boost-mode): the new 2/3-PWM-OPT enables loss-optimal operation for the full wide output voltage range of 200 V to 800 V. This loss-optimal operation mode ensures that only three (of the converter's five) half-bridges (HBs) are actively switching (i.e., operate with PWM) at any given point in time and do so with the minimum possible DC-link voltage, which results in the minimum possible switching losses. Furthermore, a synergetic control strategy is proposed to operate the VSR-stage and the DC/DC-stage collaboratively to achieve automatic and seamless transitions

between the different loss-optimum operating modes and modulation schemes when the output voltage changes.

The operating modes and the control strategy are implemented and verified with a compact 10 kW hardware demonstrator (5.4 kW/dm^3 or 91 W/in^3) with a peak efficiency of 98.8% at rated load and 560 V output voltage. Comprehensive efficiency measurements confirm the expected improvement achieved by the loss-optimal operation over the basic decoupled operation of the two converter stages, i.e., up to 3.2% in the buck-mode with 1/3-PWM and up to 0.8% in the boost-mode with 2/3-PWM-OPT. Finally, the conducted EMI compliance with CISPR 11 / Class A is tested and the regulations are largely met. Importantly, an EMI filter designed for 3/3-PWM can be directly used for 1/3-PWM operation.

All in all, the modulation and control concept presented in this paper can be considered the optimum way of operating a three-level boost-buck voltage DC-link AC/DC grid interface with a wide output voltage range.

6

Conclusion and Outlook

The primary aim of this thesis is to contribute to the promotion of sustainable transportation electrification towards a low-carbon economy by enhancing the efficiency and compactness of EV chargers. To attain this objective, advanced 3-Φ bidirectional AC/DC converter systems with buck-boost and boost-buck functionality are analyzed, which serve as crucial building blocks of both galvanically isolated and non-isolated EV chargers. Additionally, the thesis reviews and studies a future RCD-based non-isolated EV charger, which is anticipated to bring about significant advancements in efficiency and power density. Two advanced 3-Φ AC/DC converter systems, i.e., a current DC-link buck-boost converter and a voltage DC-link boost-buck converter (see **Fig. 6.1**), are constructed. The advantageous sharing of the main magnetic components between the front-end buck-type CSR-stage and the series-connected DC/DC boost-stage allows the 3-Φ bB current DC-link PFC AC/DC converter system (see **Fig. 6.1a**) to achieve similar efficiencies in a more compact design and simpler synergetic control strategy compared to the conventional 3-Φ Bb voltage DC-link PFC AC/DC converter system (see **Fig. 6.1b**).

In this chapter, the advanced 3-Φ buck-boost AC/DC converter systems are first compared in **Section 6.1** regarding hardware realization, synergetic controller implementation, efficiency characteristics, and conducted EMI noise emissions. The main findings of the thesis are then summarized in **Section 6.2**. Finally, possible future research areas are discussed in **Section 6.3**.

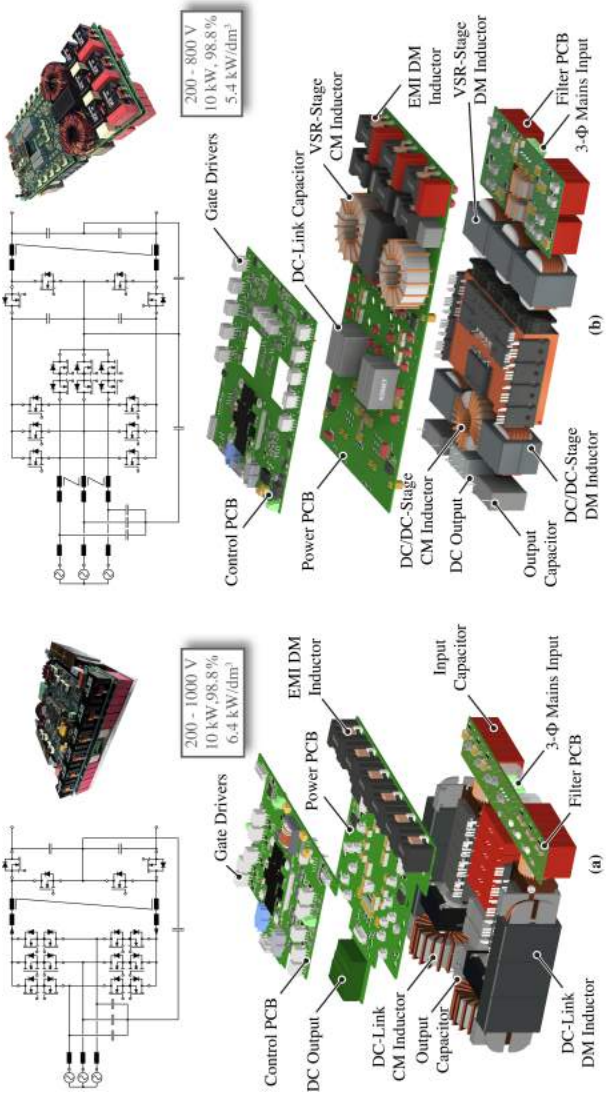

Fig. 6.1: Circuit schematics, exploded views, and photos of the realized 10 kW hardware demonstrators, i.e., **(a)** a 3-Φ bB current DC-link and **(b)** a 3-Φ Bb voltage DC-link PFC AC/DC converter system.

6.1 Comparison of Current and Voltage DC-Link AC/DC Converter Systems

In the following, the two advanced 3-Φ buck-boost AC/DC converter systems, i.e., the 3-Φ bB current DC-link (see **Fig. 6.1a**) and the 3-Φ Bb voltage DC-link (see **Fig. 6.1b**) PFC AC/DC converter systems are compared based on built hardware demonstrators.

- ***Hardware Realization***

  The two built hardware demonstrators and their exploded structure views are presented in **Fig. 6.1**, where **(a)** shows the 3-Φ bB current DC-link PFC AC/DC converter system and **(b)** shows the 3-Φ Bb voltage DC-link PFC AC/DC converter system. A first obvious advantage of the 3-Φ bB current DC-link system is that only a single DM and a single CM inductors are employed in the shared current DC-link whereas at least four DM and two CM inductors are needed in the 3-Φ Bb voltage DC-link system. The reduced inductor count decreases beneficially the manufacturing cost and simplifies labor-related manufacturing procedures.

  Furthermore, in the 3-Φ Bb voltage DC-link system, commutation loops of the VSR-stage and the DC/DC-stage both include the DC-link capacitor so that two converter stages have to be placed as close as possible to the DC-link to minimize the commutation loop inductances. Thus, the PCB layouts and physical positions for two stages are actually coupled and need to be optimized together. In contrast, advantageously, the current (inductive) DC-link allows to optimize the realization of the two converter stages, i.e., the arrangement of the CSR-stage and the DC/DC-stage. This simplifies the design complexity and helps to increase the system form factor since no physical restriction is imposed between the two converter stages.

- ***Synergetic Control Implementation***

  Synergetic control of the 3-Φ bB current DC-link PFC AC/DC converter system is more intuitive than for the 3-Φ Bb voltage DC-link system because of the possible indirect AC mains current control where only the DC-link current is closed-loop controlled but the 3-Φ mains currents and the DC output current are generated in an open-loop manner. Thus, only two cascaded PI controllers are needed for the output voltage and the DC-link current regulation. In contrast, the implementation of

the synergetic control strategy for the 3-Φ Bb voltage DC-link system includes four cascaded PI controllers, especially when 1/3-PWM is needed. Currents flowing through the 3-Φ boost inductors and the DC/DC-stage output inductor have to be measured and regulated to ensure a sufficient current controller bandwidth. Furthermore, an output voltage control loop is required to track the output voltage (power) reference and a DC-link voltage control loop has to ensure the six-pulse shape for 1/3-PWM. Therefore, a more straightforward synergetic controller design and implementation of the 3-Φ bB current DC-link system can be expected.

- ***Efficiency Characteristics***

  Measured efficiencies of two built hardware demonstrators are presented in **Fig. 6.2a** for the 3-Φ bB current DC-link system and in **Fig. 6.2b** for the 3-Φ Bb voltage DC-link system. Both systems can cover wide operating areas with high efficiencies (> 98 %) and achieve a peak efficiency of 98.8 %, even though different efficiency characteristics are observed.

  The 3-Φ bB current DC-link system presents ultra-flat efficiency characteristics since conduction losses are dominant in the realized converter (see **Fig. 6.3a**), which is beneficial for EV charger applications which need to operate in partial-power. However, full-load efficiencies are limited because **(i)** in buck-mode, large DC-link currents generate large conduction losses of the entire system, and **(ii)** in boost-mode, two HBs of DC/DC-stage hard switch a high voltage and current, i.e., half of the output voltage and the full DC-link current, leading to significant hard-switching losses.

  In contrast, the 3-Φ Bb voltage DC-link system generates relatively low losses due to the employed 3-L T-type VSR-stage front-end (see **Fig. 6.3b**). Furthermore, even though switching transitions of the DC/DC-stage are hard as for the current DC-link converter, the DC/DC-stage only needs to be actively switched at reduced switching voltages and current in buck-mode operation. Thus, high efficiencies are observed in the 3-Φ Bb voltage DC-link system during full-load operation.

- ***Conducted EMI Noise Emission***

  Measured conducted EMI noise emissions of the two built hardware demonstrators are presented in **Fig. 6.4a** for the 3-Φ bB current DC-link system, and in **Fig. 6.4b** for the 3-Φ Bb voltage DC-link system. It is

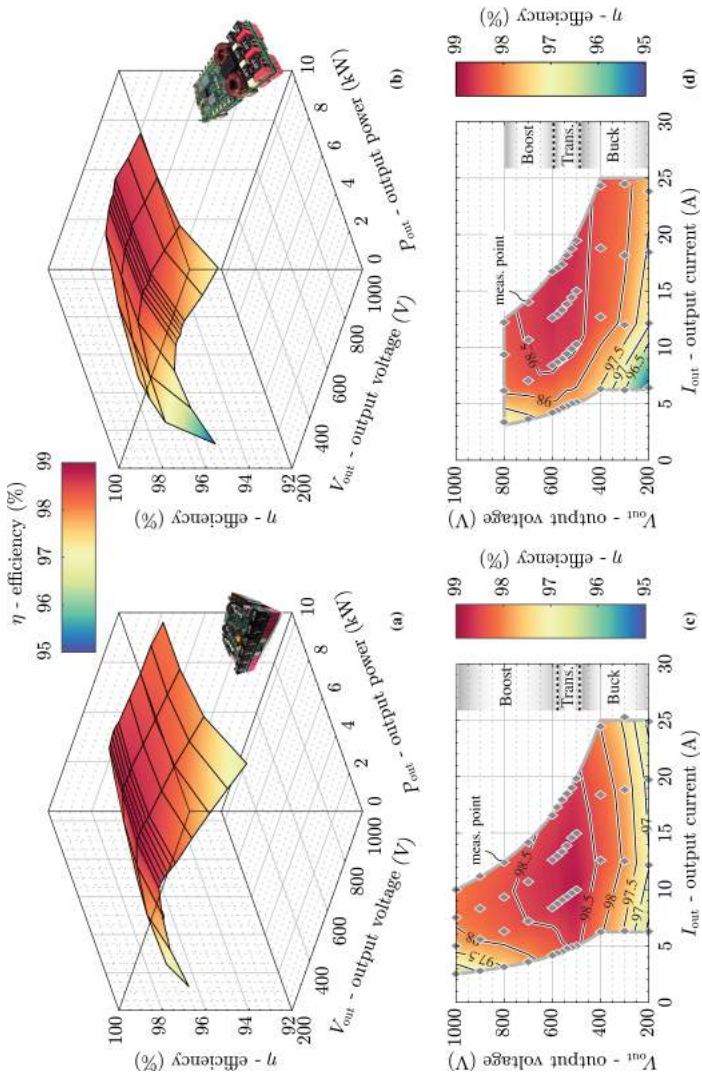

Fig. 6.2: Measured (Yokogawa WT3000) efficiencies of the realized 10 kW hardware demonstrators, i.e., of **(a)** 3-Φ bB current DC-link and **(b)** 3-Φ Bb voltage DC-link PFC AC/DC converter system. In **(b)** and **(d)**, the corresponding efficiency contours indicating the measured points are presented.

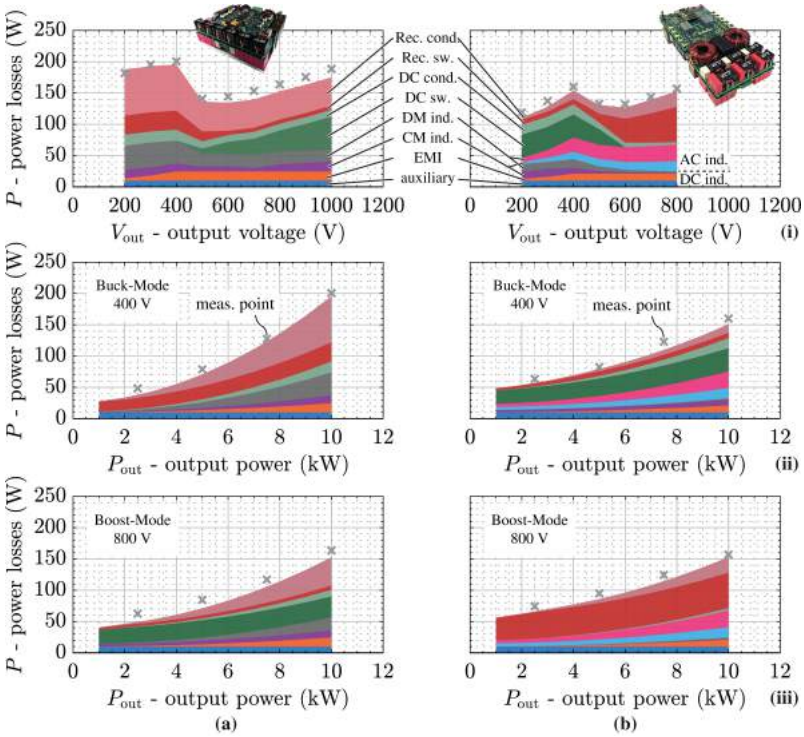

Fig. 6.3: Loss Breakdown of the 3-Φ EV charger prototypes, i.e., of **(a)** 3-Φ bB current DC-link and **(b)** 3-Φ Bb voltage DC-link PFC AC/DC converter system, during **(i)** full-load operation at different output voltages, and for **(ii)** buck-mode (400 V) and **(iii)** boost-mode (800 V) operation at different output powers.

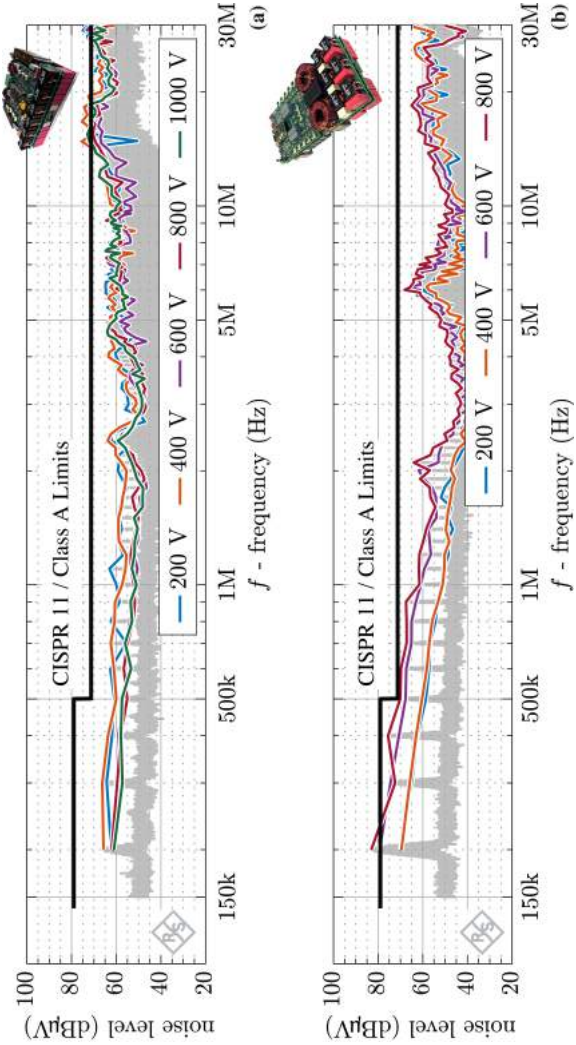

Fig. 6.4: Conducted EMI noise emission pre-qualification analyses at rated power and typical output voltages which are measured on the realized 10 kW hardware demonstrator of **(a)** 3-Φ bB current DC-link and **(b)** 3-Φ Bb voltage DC-link PFC AC/DC converter system. The CISPR 11 peak (PK) detector has been used with a 4 kHz step size, 9 kHz resolution bandwidth (RBW), and 1 ms measurement time. The local peak values are connected as an envelope for easier comparisons between different operating points.

clearly observed that the conducted EMI noise emissions for the current DC-link system are output voltage independent, but more related to the DC-link current (the output power) since the DM noise source can be replaced with a switched current source representing the DC-link current. In comparison, the voltage DC-link system creates increased conducted EMI noise emissions when operating with higher DC-link voltages, i.e., equal to the high output voltages in boost-mode.

6.2 Summary

The descriptions in this section are limited to the main achievements of the thesis since a summary of important results is also given at the end of each chapter.

- ***3-Φ bB Current DC-Link PFC AC/DC Converter System***

  A 3-Φ bB current DC-link PFC AC/DC converter system is introduced, which is composed of a buck-type CSR-stage and a downstream 3-L boost-type DC/DC-stage connected via a single main magnetic component, the DC-link inductor. The two stages operate collaboratively to achieve loss-optimal operation over an ultra-wide output range (200 V to 1000 V): for low output voltages, the CSR-stage controls the output voltage and the DC/DC-stage is clamped to avoid switching losses; for high output voltages, the DC/DC-stage shapes the DC-link current such that the CSR-stage operates with 2/3-PWM (switching limited to two of the three phases) and hence with reduced switching losses.

  Furthermore, a compact 10 kW hardware demonstrator with a power density of 6.4 $\mathrm{kW/dm^3}$ (107.5 $\mathrm{W/in^3}$) is presented and used to verify, for the first time, the key functionality of a proposed synergetic control method. Then, comprehensive efficiency measurements over the full output voltage and output power range confirm a flat efficiency characteristic (higher than 98 % for most operating points with output voltages above 400 V and more than 25 % of rated load). Importantly, the efficiency improvement of 2/3-PWM over 3/3-PWM on the system-level, i.e., including the DC/DC-stage, is experimentally confirmed to be up to 1 %.

- ***Independent Output Voltage Synergetic Control***

  A synergetic control concept for a 3-Φ bB current DC-link PFC AC/DC converter system featuring two independently regulated DC outputs

is proposed, ensuring minimum losses for any operating point (2/3-PWM of the CSR-stage or clamping of the DC/DC converter HBs, and minimum possible DC-link current).

Experimental confirmation of the proposed control scheme using a 10 kW demonstrator system is provided. Operating in the boost-mode at a total output voltage of 800 V, the proposed synergetic control achieves a significant measured efficiency improvement compared to conventional operation over a wide load range, e.g., from 95.7 % to 96.9 % (1.2 %) at 2 kW and from 97.9 % to 98.4 % (0.5 %) at 10 kW, which is largely independent of output voltage asymmetries and load asymmetries.

- ***VGC and GCC for Non-Isolated EV Chargers***

  The proposed VGC and the GCC schemes allow a direct connection of the DC output midpoint to PE by regulating the sum of the three mains phase currents, i.e., the ground current, to near zero and hence prevents nuisance tripping of mandatory RCDs.

  The proposed concepts are verified with a 10 kW hardware demonstrator considering TT and TN grounding systems. With a direct connection of the DC output midpoint to PE, GCC limits the LF CM leakage current to 6 mA RMS, i.e., to a value significantly below typical RCD trip levels, and, using the human-body impedance model according to UL 2202, achieves a test voltage of 110 mV that is clearly below the most stringent limit (250 mV) of the standard.

- ***3-Φ Bb Voltage DC-Link PFC AC/DC Converter System***

  A 3-Φ Bb voltage DC-link PFC AC/DC converter system consisting of a 3-Φ three-level T-type (Vienna) VSR-stage and a downstream 3-L buck-type DC/DC-stage is studied, focusing on a new modulation scheme for the transition-mode (i.e., for output voltages between buck-mode and boost-mode): the proposed new 2/3-PWM-OPT scheme enables loss-optimal operation for the full wide output voltage range, i.e., only three half-bridges are actively switching at any given point in time and the DC-link voltage is controlled to the minimum possible value.

  Furthermore, a synergetic control strategy is proposed to achieve automatic and seamless transitions between the different loss-optimum operating modes and modulation schemes when the output voltage changes. This is experimentally verified using a 10 kW hardware demonstrator with a peak efficiency of 98.8% at rated power and a power

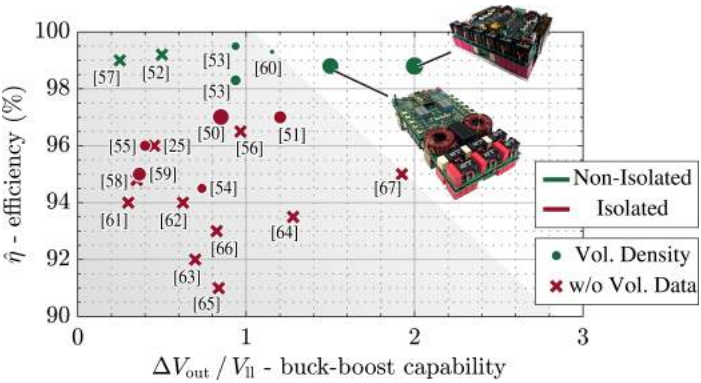

Fig. 6.5: Overview of 3-Φ EV charger prototypes and products reported in the literature in the coordinate system of peak efficiency $\hat{\eta}$ and buck-boost capability $\Delta V_{out} / V_{ll}$, where $\Delta V_{out} = V_{out,max} - V_{out,min}$. The two EV chargers built in this thesis are highlighted. University demonstrators: [25, 50–60]. Industry products: [61–67]. The volumetric power density values are indicated by according symbol sizes.

density of 5.4 kW/dm^3 (91 W/in^3) including efficiency and conducted EMI measurements.

6.3 Outlook and Future Research Areas

- ***Non-Isolated EV Chargers***

  Even though relevant standards for EV chargers, e.g., UL 2202 [49] or IEC 61851 [119], do not require galvanic isolation between the grid-connected AC input and the output DC charging port (IEC 61851-23 [120], for example, mentions that regulations for non-isolated DC chargers are under consideration), conventional EV chargers typically include either traditional 50 Hz transformers or DC/DC converters with high-frequency isolation to provide a large common-mode (CM) impedance between the grid and the vehicle to ensure electrical safety.

  However, providing galvanic isolation means placing an additional conversion stage, i.e., a low-frequency transformer or an isolated DC/DC converter, in the power flow path and consequently leads to more bulky and more complex systems with increased power losses and costs. **Fig. 6.5** summarizes the performance of 3-Φ EV charger proto-

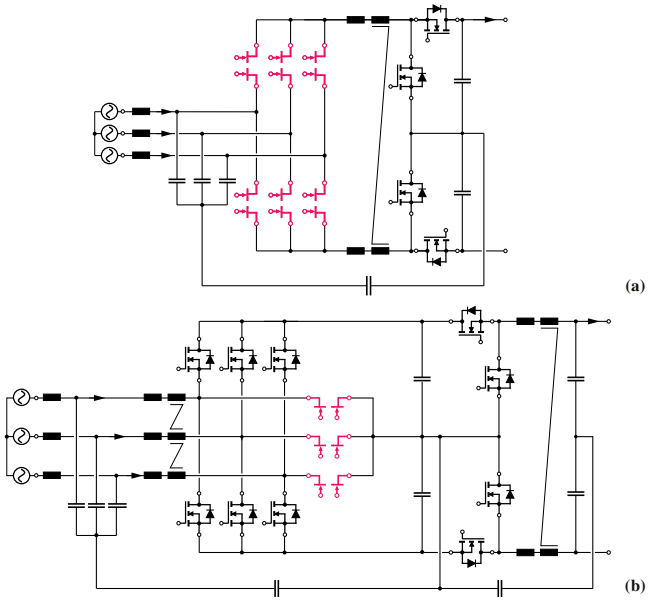

Fig. 6.6: Circuit schematics of **(a)** 3-Φ bB current DC-link and **(b)** 3-Φ Bb voltage DC-link PFC AC/DC converter system, where monolithic bidirectional switches (M-BDSs) are implemented to provide bipolar voltage blocking and bidirectional current conduction capability instead of inverse-series connected unipolar devices, e.g., MOSFETs.

types and products reported in the literature. It is observed that the required wide output voltage range can be covered by both isolated and non-isolated systems, but the non-isolated EV chargers feature an efficiency improvement of 1 % to 2 % and about twice the power density.

- ***Monolithic Bidirectional Switches***

  Both of the studied topologies, i.e., 3-Φ bB current DC-link PFC AC/DC converter system and 3-Φ Bb voltage DC-link PFC AC/DC converter system, need inverse-series connected power transistors to achieve the required bipolar voltage blocking capability, resulting in increased transistor counts and construction complexity. This structural weakness, i.e., the factor-of-four penalty in chip area usage for conventional discrete realization, is being eliminated by the recent availability of monolithic bidirectional switches (M-BDSs) where a single drift region can block either voltage polarity resulting in reduced on-state resistance

and/or chip area. 900 V or 1200 V M-BDSs are needed in the current source PFC rectifier front-end (see **Fig. 6.6a**) to interface 400 V mains, whereas 600 V M-BDSs are necessary for the 3-L T-type (Vienna) PFC rectifier front-end (see **Fig. 6.6b**).

Using future M-BDSs, the 3-Φ bB current DC-link PFC AC/DC converter system can be built with only ten power transistors (see **Fig. 6.6a**) and low conduction losses, which is a main requirement for achieving high power conversion efficiency. Accordingly, M-BDS-based current DC-link 3-Φ buck-boost PFC AC/DC mains interfaces can be considered a top choice for the realization of next-generation low complexity, highly compact/efficient EV chargers.

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