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Novel Medium-Voltage Solid-State Transformer Technologies

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to Adrianna & Hubert,

to Anna and Zbigniew, my parents.

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The future is already here – it's just not evenly distributed.
William Gibson

Mądrość musisz sam z siebie własną dobyć pracą.
Wisdom with your own work must be gained.
Adam Mickiewicz

Abstract

With a strong global push towards a sustainable energy future and decarbonization, it is expected that in the following decades the electrification of transportation will play a major role in reducing the global greenhouse gas emissions. The research on and development of technologies for the electrification of all transport modes, i.e., road, rail, maritime, and air, drive continuous advancements towards increasing power density of power converters in general and, due to the typically high-power demand of these applications, detailed investigations of power electronic interfaces connected directly to medium-voltage (MV) grids in particular. One of the key technologies that enables such advancements are solid-state transformers (SSTs), which represent a class of power electronic converters providing galvanic isolation between a MV and a low-voltage (LV) system using medium-frequency (MF) transformers (MFTs). Additional properties such as high achievable gravimetric and/or volumetric power density and efficiency render SSTs a key component for a wide range of applications for more electric transport, such as high-power electric vehicle (EV) charging stations, power electronic traction transformers (PETTs), or future ships and future aircraft with distributed propulsion and on-board MVDC distribution grids.

Regardless of whether an SST interfaces AC and/or DC systems, its core conversion stage is an isolated MV DC-DC converter (i.e., MVDC-LVDC or MVDC-MVDC) that, in the light of the aforementioned requirements of future electric transportation applications, should be realized with low weight and high efficiency. State-of-the-art high-efficiency MV DC-DC converters with galvanic isolation typically feature limited gravimetric power densities of not more than 5 kW/kg. Achieving higher power densities in MV converters is possible with the use of 10 kV SiC MOSFETs, which can operate at high switching frequencies thanks to their very low soft-switching losses. Whereas in theory this enables a reduction of the weight of the magnetic components (i.e., the MFT), however, in conventional magnetic-core transformers (MCTs), a substantial part of the core window is required for the electric insulation. Due to the resulting low fill factor of the core window and also because of thermal limitations of the core materials, only limited gains in gravimetric power density can be realized by selecting high switching frequencies.

Addressing these key challenges, the first main goal of this thesis is to explore and identify suitable technologies for the realization of lightweight and highly efficient MV MFTs. The literature on inductive power transfer systems reveals that high efficiency operation of transformers can be achieved at high frequencies also with loosely coupled coils, i.e., without a closed mag-

netic core. This indicates a potential for realizing ultra-lightweight isolated MV DC-DC converters by employing air-core transformers (ACTs). Thus, the first part of the thesis focuses on the derivation of performance limits (gravimetric and volumetric power densities, efficiency) of ACTs and MCTs for a lightweight 166 kW / 7 kV MV DC-DC converter with a DC-DC efficiency of $\geq$ 99 %.

In a first step, to take into account multiple design objectives simultaneously, a multi-objective optimization process is proposed for the design of a lightweight 166 kW / 7 kV MV DC-DC converter realized as a series-resonant converter operated at the resonant frequency (i.e., a DC transformer, DCX) with equal input and output voltages (1:1-DCX), where two realization options for the MFT are considered and compared: ACT and MCT. A combination of analytical models with electromagnetic finite element method (FEM) simulations is employed for the ACT-based DCX (ACT-DCX), whereas for the MCT-DCX a semi-analytical optimization routine is used. Next, the proposed optimization process is theoretically and experimentally validated by the design of two 166 kW / 7 kV transformer prototypes (i.e., one ACT and one MCT prototype). The design process includes detailed considerations of insulation, cooling, and shielding of the magnetic stray flux. A thorough experimental validation of the two prototypes, including a variety of measurements, e.g., small-signal impedance measurements, large-signal tests, loss measurements, transient thermal responses, magnetic stray flux densities (without and with shielding), insulation tests, and dielectric losses, demonstrates their full functionality and facilitates an experimentally-backed comparison of the two concepts. The ACT prototype (16.5 kW/kg, 2.2 kW/dm^3) achieves a measured full-load efficiency of 99.5 % at an operating frequency of 77.4 kHz. The MCT prototype (6.7 kW/kg, 5.4 kW/dm^3), operated at 40.0 kHz due to the selected core material, reaches a measured full-load efficiency of 99.7 %. Furthermore, the use of 10 kV SiC MOSFETs enables calculated system-level DC-DC efficiencies for the ACT-DCX and the MCT-DCX of 99.0 % and 99.2 %, respectively, whereas the resulting system-level gravimetric power density is 9.7 kW/kg for the ACT-DCX and 5.6 kW/kg for the MCT-DCX, which confirms the suitability of the ACT concept for the realization of lightweight converter systems.

In addition to the challenges related to the realization of MV MFTs, further challenges in SSTs appear with respect to the employed converter topology and semiconductors, since the blocking voltages required for the realization of MV DC-DC converters in many applications exceed the capabilities of today's cutting-edge 10 kV and 15 kV SiC power semiconductors. Recent research

has focused on quasi-2-level (Q2L) operation of various types of multi-level bridge-legs as an interesting option for realizing single-cell power conversion. Compared to conventional realizations, Q2L-operated multi-level bridge-legs feature minimized capacitive energy storage requirements. Compared to 2-level high-voltage SiC realizations (as far as possible due to the system voltage level), lower average voltage slew rates of the Q2L transitions facilitate EMI filter design and reduce insulation stress. In particular, Q2L-operated flying capacitor converters (Q2L-FCCs) are of interest due to the snubberless design and low number of components.

Therefore, the second part of this thesis investigates Q2L operation of a 5-level FCC (5L-FCC) half-bridge to realize a versatile, compact and integrated power semiconductor stage for zero-voltage-switched (ZVS) and hard-switched (HS) applications, where the system voltages exceed the voltage ratings of available power semiconductors.

First, the state-of-the-art methods to realize such a MV power semiconductor stage are reviewed, in particular, direct series connection of semiconductors, super-cascode configurations, or multi-level converter structures, i.e., the modular multi-level converter (MMC) and the FCC. The considerations confirm that the Q2L-operated FCC is the most promising realization option. However, a key challenge is to ensure balanced voltages of the low-capacitance flying capacitors (FCs). Therefore, a fundamental analysis of Q2L operation of the 5L-FCC half-bridge for ZVS and HS Q2L transitions with non-zero output current is performed. Next, Q2L transitions at zero output current (i.e., no-load operation) are analyzed, too, and a generic description of the charge and voltage increments of the FCs during a transition, which result from the charge that needs to be delivered to the output capacitances of the power semiconductors during hard-switching, is derived. Based on those findings, a comprehensive concept for load-independent balancing of the FC voltages in Q2L-FCCs with arbitrary numbers of levels is proposed and applied to the considered 5L-FCC. For non-zero load current, a model predictive control (MPC) approach is used to identify the commutation sequence of the individual switches within a Q2L transition that minimizes the errors of the FC voltages or of the cell voltages, the latter being defined as the differences between the voltages of the two FCs adjacent to the two switches forming a given cell (i.e., the cell voltage corresponds to the semiconductor blocking voltage). In case of zero load current, a novel MPC-based approach using cell multiple switching (CMS) is presented. The CMS method inserts additional zero-current (lossy) commutations within a Q2L transition, which leads to additional charging of the output capacitances of switches and to correspond-

ing charge exchanges between the FCs. Hence, CMS increases the degrees of freedom available for controlling the FC voltages or the cell voltages. The proposed methods are thoroughly examined and then comprehensively verified using a 5L-FCC LV half-bridge demonstrator. The experiments confirm the validity of the employed models and the results confirm good FC voltage tracking and symmetric blocking voltage stress of the transistors. To complete the Q2L-FCC considerations, an integration concept for a complete MV bridge-leg, including gate drivers, isolated cooling interfaces, measurements, and Q2L control into a 300 kVA / 40 kV SiC Super-Switch Intelligent Power Module (SiC-SS-IPM) is presented.

Finally, the thesis concludes with a summary and a discussion of the obtained insights and gives an outlook on future research vectors.

Kurzfassung

Im Zuge der grossen globalen Anstrengungen zur Realisierung einer nachhaltigen Energiezukunft wird erwartet, dass in den kommenden Jahrzehnten die Elektrifizierung des Transportwesens einen wichtigen Beitrag zur Reduktion der globalen Treibhausgasemissionen leisten wird. Die Forschung an und die Entwicklung von Technologien zur Elektrifizierung aller Transportmodi, d.h. Strasse, Schiene, See- und Luftfahrt, treiben kontinuierliche Fortschritte in Richtung höherer Leistungsdichte von leistungselektronischen Konvertern im Allgemeinen und aufgrund der typischerweise hohen Leistungen derartiger Applikationen insbesondere auch die detaillierte Untersuchung von leistungselektronischen Interfaces, die direkt an Mittelspannung (medium voltage, MV) angebunden sind. Eine der Schlüsseltechnologien, die solche Fortschritte ermöglichen, sind Solid-State-Transformatoren (SSTs), d.h., eine Klasse von leistungselektronischen Konvertern, die eine galvanische Trennung zwischen einem MV-System und einem Niederspannungssystem (low voltage, LV) mittels Mittelfrequenztransformatoren (MFTs) realisieren. Weitere Eigenschaften wie hohe erreichbare gravimetrische und/oder volumetrische Leistungsdichte und hoher Wirkungsgrad machen SSTs zu einer Schlüsselkomponente für eine breite Palette von Anwendungen im Bereich des elektrifizierten Transportwesens, wie beispielsweise Hochleistungsladestationen für Elektrofahrzeuge, leistungselektronische Traktionstransformatoren in Schienenfahrzeugen, und zukünftige Schiffe oder Flugzeuge mit einem bordeigenen Mittelspannungsgleichstromverteilnetz (MVDC-Verteilnetz).

Unabhängig davon, ob ein SST an Wechselspannungs- und/oder Gleichspannungssysteme angebunden ist, wird die Kernfunktionalität durch einen MV DC-DC-Konverter (d.h. MVDC-LVDC-Konverter oder MVDC-MVDC-Konverter) realisiert, der im Lichte der oben erwähnten Anforderungen an zukünftige elektrische Transportapplikationen mit möglichst tiefem Gewicht und hohem Wirkungsgrad realisiert werden soll. Dem heutigen Stand der Technik entsprechende hocheffiziente MV DC-DC-Konverter mit galvanischer Trennung erreichen typischerweise beschränkte gravimetrische Leistungsdichten von nicht mehr als 5 kW/kg. Die Verwendung von 10 kV SiC-MOSFETs, die aufgrund der sehr tiefen Verluste bei weichem Schalten auch bei hohen Schaltfrequenzen betrieben werden können, ermöglicht es, auch höhere Leistungsdichten zu erreichen: hohe Schaltfrequenzen führen zumindest theoretisch zu einer Reduktion des Gewichts der magnetischen Komponenten (d.h. des MFTs in einem MV DC-DC-Konverter). In der Praxis muss jedoch bei konventionellen MFTs mit Magnetkern (magnetic-core transformer, MCT) ein substanzieller Anteil des Wicklungsfensters für die elektrische Isolati-

on aufgewendet werden. Aufgrund des so resultierenden tiefen Füllfaktors der Wicklungen und zusätzlich auch wegen thermischer Limitierungen der verfügbaren Kernmaterialien, können letztlich auch mit einer Erhöhung der Schaltfrequenz nur begrenzte Verbesserungen der gravimetrischen Leistungsdichte erzielt werden.

Das erste Hauptziel dieser Arbeit ist es daher, diese Schlüsselherausforderung zu adressieren und passende Technologien für die Realisierung von leichten und hocheffizienten Mittelspannungs-MFTs zu identifizieren und zu untersuchen. Der Literatur zu drahtlosen induktiven Energieübertragungssystemen ist zu entnehmen, dass hocheffizienter Betrieb von MFTs bei hohen Frequenzen auch bei nur loser Kopplung der primär- und sekundärseitigen Spulen möglich ist, d.h. ohne einen geschlossenen magnetischen Kern. Dies weist auf hohes Potential zur Realisierung von ultraleichten isolierten MV DC-DC-Konvertern durch die Verwendung von kernlosen Transformatoren (air-core transformers, ACTs) hin. Der erste Teil der Arbeit fokussiert deshalb auf die Herleitung und den Vergleich der maximal erreichbaren gravimetrischen und volumetrischen Leistungsdichten sowie der Wirkungsgrade von ACTs und MCTs für einen leichten 166 kW / 7 kV MV DC-DC-Konverter mit einem DC-DC-Wirkungsgrad von $\geq$ 99 %.

Um mehrere Designziele gleichzeitig berücksichtigen zu können, wird in einem ersten Schritt ein Mehrkriterienoptimierungsverfahren für das Design eines leichten 166 kW / 7 kV MV DC-DC-Konverters, der als im Resonanzpunkt betriebener Serienresonanzkonverter (d.h. als DC-Transformator, DCX) mit gleichen Eingangs- und Ausgangsgleichspannungen (1:1-DCX) realisiert werden soll, vorgeschlagen. Dabei werden zwei verschiedene Realisierungsoptionen für die Kernkomponente MFT betrachtet und verglichen: ACT und MCT. Der ACT wird unter Verwendung einer Kombination von analytischen Modellen und elektromagnetischen Simulationen mittels der Finite-Elemente-Methode (FEM) beschrieben und optimiert, während für den MCT eine teilanalytische Optimierungsroutine zur Anwendung kommt. Der vorgeschlagene Modellierungs- und Optimierungsprozess wird anschliessend durch das Design von zwei 166 kW / 7 kV Transformatorprototypen (d.h. eines ACT und eines MCT) theoretisch und experimentell verifiziert. Der Designprozess umfasst detaillierte Betrachtungen bezüglich elektrischer Isolation, Kühlung und Abschirmung von magnetischen Streuflüssen in der Umgebung der MFTs. Eine gründliche experimentelle Validierung der beiden Prototypen, die eine Vielzahl von Messungen beinhaltet wie zum Beispiel Kleinsignalimpedanzmessungen, Grosssignaltests, Verlustmessungen, Messung der thermischen Zeitkonstanten, der magnetischen Streuflussdichten

in der Umgebung mit und ohne Abschirmung, Isolationstests, sowie eine detaillierte Charakterisierung der dielektrischen Verluste in den Isolationsmedien, zeigt die volle Funktionsfähigkeit beider Prototypen und ermöglicht schliesslich einen experimentell breit abgestützten Vergleich der beiden Konzepte. Der ACT-Prototyp (16.5 kW/kg, 2.2 kW/dm^3) erreicht einen gemessenen Volllastwirkungsgrad von 99.5 % bei der Betriebsfrequenz von 77.4 kHz. Der MCT-Prototyp (6.7 kW/kg, 5.4 kW/dm^3) wird aufgrund des verwendeten Kernmaterials bei 40.0 kHz betrieben und erreicht eine gemessene Volllasteffizienz von 99.7 %. Bei Verwendung von 10 kV SiC-MOSFETs zur Realisierung der Schaltstufen des DC-Transformators können auf der Systemebene so DC-DC-Wirkungsgrade von 99.0 % für den ACT-DXC und von 99.2 % für den MCT-DXC errechnet werden. Die gravimetrischen Leistungsdichten der Gesamtsysteme betragen 9.7 kW/kg für den ACT-DCX und 5.6 kW/kg für den MCT-DCX, womit die gute Eignung des ACT-Konzepts für die Realisierung von leichten Konvertersystemen bestätigt wird.

Zusätzlich zu den oben umrissenen Herausforderungen stellen sich bei der Realisierung von Mittelspannungs-MFTs Fragen hinsichtlich der eingesetzten Konvertertopologien und der Leistungshalbleiter, da in vielen Anwendungen die von MV DC-DC-Konvertern benötigten Halbleitersperrspannungen die Spezifikationen selbst modernster heute verfügbarer Siliziumkarbidleistungshalbleiter, d.h. 10 kV oder 15 kV SiC MOSFETs oder IGBTs, überschreiten. Kürzlich veröffentlichte Forschungsarbeiten haben daher den sogenannten Quasi-2-Levelbetrieb (Q2L) von verschiedenen Multilevelbrückenzweigstrukturen untersucht und als interessante Option zur Realisierung von nichtmodularen MV DC-DC-Konvertern (und anderer direkt an MV angebundener leistungselektronischer Konvertersysteme) identifiziert. Im Vergleich zu konventionellen Realisierungen von Multilevelbrückenzweigen zeichnen sich Q2L-Multilevelbrückenzweige durch minimierte kapazitive Energiespeicher aus. Auch gegenüber 2-Level-Brückenzweigen, die mit hochsperrenden Siliziumkarbidhalbleitern mittleren realisiert werden könnten (soweit aufgrund der Systemspannung möglich), sind die tieferen Spannungssteilheiten der Q2L-Schaltflanken als vorteilhaft hinsichtlich EMV-Filterung und reduzierter Beanspruchung von Isolationsystemen, beispielsweise von MFTs, zu bewerten. Von besonderem Interesse sind im Q2L-Betrieb ausgeführte Flying-Capacitor-Konverter (flying capacitor converters, FCCs) aufgrund der tiefen Komponentenzahl und des Fehlens von zusätzlichen Beschaltungsnetzwerken, z.B., zur Überspannungsbegrenzung oder Sicherstellung von symmetrischer Beanspruchung von Komponenten.

Deshalb wird im zweiten Teil der vorliegenden Arbeit der Q2L-Betrieb einer 5-Level FCC-Halbbrücke (5L-FCC) untersucht mit dem Ziel, eine vielseitig einsetzbare, kompakte und integrierte Halbleiterschaltstufe für hart- und weichgeschaltete Anwendungen zu schaffen, in der die Systemspannung die Sperrspannungen verfügbarer Leistungshalbleiter überschreitet.

Zunächst wird ein Überblick über den Stand der Technik zur Realisierung einer derartigen Halbleiterschaltstufe für Mittelspannung gegeben, d.h. die direkte Serienschaltung von Leistungshalbleitern, Kaskodenschaltungen, oder Multilevelstrukturen wie den modularen Multilevelkonverter (modular multilevel converter, MMC) und den FCC. Der Vergleich dieser Ansätze bestätigt, dass der mit Q2L-Modulation betriebene FCC eine sehr vielversprechende Option ist. Ein Schlüsselaspekt ist dabei jedoch die Sicherstellung von balancierten Spannungen der vorteilhaft mit nur kleiner Kapazität ausgeführten Kondensatoren (flying capacitors, FCs). Daher wird eine grundlegende Analyse des Q2L-Betriebes einer 5L-FCC-Halbbrücke sowohl für weiches als auch für hartes Schalten bei einem Ausgangsstrom ungleich null durchgeführt. Anschliessend werden auch Q2L-Transitionen für den Fall von verschwindendem Ausgangsstrom (d.h., lastfreien Betrieb) analysiert, und eine allgemeine Beschreibung der Ladungs- und Spannungsinkremente der FCs während der Q2L-Transition hergeleitet, die auf den Ladungsaustausch zwischen den FCs zufolge der bei hartem Schalten auftretenden Ladeströme in den Ausgangskapazitäten der Halbleiterschalter zurückzuführen sind. Basierend auf diesen Resultaten wird schliesslich ein umfassendes Konzept für das lastunabhängige Balancieren der FC-Spannungen in Q2L-FCCs mit beliebiger Anzahl von Levels vorgeschlagen und auf das Beispiel des vorgängig erwähnten 5L-FCCs angewendet. Das Verfahren nutzt bei vorhandenem Laststrom einen modellbasierten prädiktiven Regler (model predictive control, MPC), um die Kommutierungssequenz der einzelnen Halbleiterschalter des FCC-Brückenzweigs während einer Q2L-Transition derart auszuwählen, dass die durch den Laststrom resultierenden Spannungsänderungen der FCs die Abweichungen der FC-Spannungen von den Sollwerten minimieren. Alternativ können auch die Zellenspannungen, d.h. die Spannungsdifferenzen zwischen zwei aufeinanderfolgenden FCs, die direkt die Sperrspannungsbeanspruchung der dazwischenliegenden Halbleiter definieren, geregelt werden. Für den Fall von verschwindendem Laststrom wird ein neuartiger, ebenfalls auf MPC basierender Ansatz vorgeschlagen, der mehrfaches Schalten einzelner Zellen (cell multiple switching, CMS) während einer Q2L-Transition nutzt. Die CMS-Methode fügt zusätzliche stromfreie (aber verlustbehaftete) Kommutierungen innerhalb einer Q2L-Transition ein, die zu zusätzlichen Ladevorgängen von

Ausgangskapazitäten von Schaltern führen und damit wie oben beschrieben auch einen entsprechenden Ladungsaustausch zwischen den FCs nach sich ziehen. So werden zusätzliche Freiheitsgrade für die Regelung der FC- oder Zellenspannungen geschaffen. Die vorgeschlagenen Methoden werden auf der theoretischen Ebene gründlich untersucht und dann umfassend mittels einer 5L-FCC GaN-Niederspannungshalbbrücke experimentell verifiziert. Die Experimente validieren die Gültigkeit der entwickelten Modelle und bestätigen das gute Tracking der FC-Spannungen sowie die symmetrische Sperrspannungsaufteilung zwischen den Transistoren. Die Betrachtungen zum Q2L-FCC werden schliesslich mit der Entwicklung eines Integrationskonzepts für einen kompletten Mittelspannungs-Q2L-FCC-Brückenzweig abgeschlossen, der neben dem Leistungsteil auch Gatetreiber, isolierte Kühlinterfaces, Messchaltungen, sowie die beschriebene Q2L-Regelung in einem 300 kVA / 40 kV SiC Super-Switch Intelligent Power Module (SiC-SS-IPM) integriert.

Die Arbeit schliesst mit einer Zusammenfassung sowie einer Diskussion der erarbeiteten Resultate und einem Ausblick auf Stossrichtungen für die zukünftige Forschung.

Abbreviations

2-D	Two-Dimensional
3-D	Three-Dimensional
1-Φ	Single-Phase
3-Φ	Three-Phase
AC	Alternating Current
ACT	Air-Core Transformer
CM	Common-Mode
CMS	Cell Multiple Switching
DC	Direct Current
DCX	DC Transformer
DAB	Dual Active Bridge
DM	Differential-Mode
EMI	Electromagnetic Interference
EV	Electric Vehicle
FC	Flying Capacitor
FCC	Flying Capacitor Converter
FEM	Finite Element Method
FET	Field-Effect Transistor
FPGA	Field Programmable Gate Arrays
GaN	Gallium Nitride
GSE	Generalized Steinmetz Equation
HF	High-Frequency
HS	Hard-Switching
HV	High-Voltage
IGBT	Insulated Gate Bipolar Transistor
iGSE	Improved Generalized Steinmetz Equation
ISOP	Input-Series Output-Parallel
ISOS	Input-Series Output-Series
LF	Low-Frequency
LV	Low-Voltage
MCT	Magnetic-Core Transformer
MF	Medium-Frequency
MFT	Medium-Frequency Transformer
MMC	Modular Multi-Level Converter
MOSFET	Metal-Oxide-Semiconductor FET
MPC	Model Predictive Control
MS	Mixed Sequences

MV	Medium-Voltage
PCB	Printed Circuit Board
PD	Partial Discharge
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse-Width Modulation
RMS	Root-Mean-Square
Si	Silicon
SiC	Silicon Carbide
SRC	Series Resonant Converter
SST	Solid-State Transformer
Q2L	Quasi-2-Level
WBG	Wide-Bandgap
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

With the worldwide goal to limit the global warming to 1.5℃ above pre-industrial levels, the carbon emissions must be reduced significantly. According to International Panel on Climate Change (IPCC), the transport sector is responsible for a 14% contribution to global emissions [1], whereas in Europe it accounts up to 25% of all emissions [2], and in the US it is even a 29% share [3]. In this context, the goal of transport decarbonization can be met by electrification which combines an energy efficient power train systems with the opportunity to use non-fossil fuels, especially electric energy from renewable sources.

As can be seen from annual electricity consumption projections presented in **Fig. 1.1**, currently the electricity demand for transport is marginal, however it is projected to increase up to 6× in the EU and up to 32× in the US by 2050 [2, 4]. Furthermore, it is estimated that in 2050 in Europe the electricity will account for up to 9% of total energy consumption in the transport sector, a nine-fold increase compared to 2020 [5]. This development is attributed to electric vehicles (EVs) penetration in the road transport and partly driven by the substitution of diesel-powered locomotives with electric traction vehicles in rail transport. Those projections seem to be in line with more than 20 countries announcing plans to end the sale of diesel and gasoline cars between 2030 and 2040 [6] and many automakers pledging to become carbon neutral or "fully electric" manufacturers by 2040 [7].

In the latest study on electrification of the transport system in the European Union prepared by the European Commission (EC) [2], the future research needs in the process of electrifying transport are presented. Moreover, EC sets a strategic implementation plan with the specific milestones for each of the four modes of transport, i.e., road, rail, maritime, and air. From

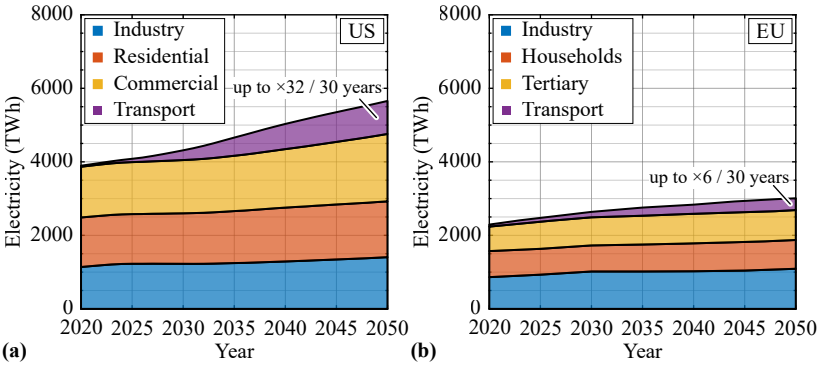


Fig. 1.1: Annual electricity consumption by economic sector: **(a)** US (medium scenario), figure is reproduced from [4]; **(b)** EU, figure is reproduced from [2].

the point of power electronic systems view, the key technologies to accelerate the electrification of transport are:

- *Road* (e.g., passenger cars, buses, heavy-duty vehicles) - high-power charging; small and light passenger EVs.
- *Rail* - commercialization of $\geq$ 1.2 kV Silicon Carbide (SiC) based medium-frequency traction converters (operated with switching frequencies in the range of kHz); light trains in small and medium cities.
- *Maritime* - shore-based infrastructure to enable fast charging; expansion of electric storage systems.
- *Air* (commercial aviation, 50-70 seats) - electrification of auxiliary power units (APUs) and non-propulsive systems with gravimetric power density targets of: 5 kW/kg in 2025, 10 kW/kg in 2035 and 20 kW/kg (with high temperature super conducting power distribution etc.) in 2055+.

Furthermore, it is highlighted that lightweight power electronics and batteries are desirable for all modes of transport. All of the above indicate the need of continued advancements towards increasing power density of converters and due to the high-power demand, investigations of medium-voltage (MV) connected power electronic interfaces. One of the key technologies that facilitates achieving those requirements are solid-state transformers (SSTs) which represent a class of power electronic converters with medium-frequency (MF)

galvanic isolation usually operating between a MV and a low-voltage (LV) system. In this regard, in the following the characteristics, applications and challenges of MV SSTs are presented.

1.1 MV Solid-State Transformer Characteristics and Applications

An SST is commonly realized with three power converters being connected in series: an AC-DC converter that is connected to the MV mains, a DC-DC converter for voltage step-down, and a DC-AC converter connecting to the LV mains. Besides voltage step-down, the DC-DC converter also features a medium-frequency transformer (MFT) and accordingly enables galvanic isolation of separated DC systems. The benefits of SSTs are mainly the controllability, i.e., reactive power compensation, active filtering, fault handling, grid monitoring, and energy routing, as well as a potential increase in power density compared to low-frequency transformer (LFT) solutions. However, typically SSTs underperform in terms of cost, efficiency and complexity compared to realizations with LFTs in smart grid applications [8].

SSTs can not only interface two AC systems, but can also directly interconnect DC systems, or a combination of both. In such cases AC-DC SSTs outperform the LFT-based equivalents with regard to power density and efficiency [9]. Therefore, SSTs are of special interest in:

- high-power EV charging stations [10, 11], see **Fig. 1.2(a)**,
- future traction applications [12–14], see **Fig. 1.2(b)**,
- hyperscale data centers [15, 16],
- hybrid smart grid systems with AC and DC sections [13, 17],

Finally, the DC-DC converter stage of the SST, realized as a series resonant converter (SRC) operated at the resonance frequency, which therefore acts as a DC transformer (DCX) [16, 18–20], is commonly used to tightly couple the DC input and output voltages without the need for closed-loop control. Furthermore, it can be utilized for ensuring a 1:1 voltage-transfer-ratio, i.e., equal primary-side and secondary-side DC port voltages (1:1-DCX), which is suitable for several applications:

- contactless and spark-free high-power plugs for fast charging in future ships [21–23], see **Fig. 1.3(a)**,

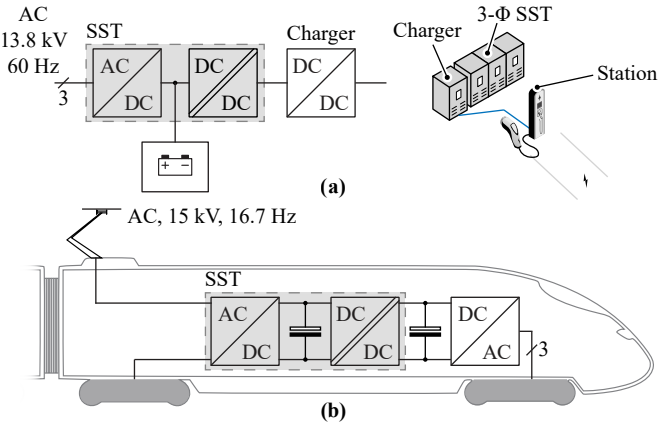


Fig. 1.2: AC-DC SST applications: **(a)** MV high-power electric vehicle charging stations with buffer storage; **(b)** power electronic traction transformer (PETT) for a future single-phase 15 kV / 16.7 Hz system.

- DC bus-tie applications in on-board MVDC grids of future aircraft with distributed propulsion systems [23–25], see **Fig. 1.3(b)**,
- grid interfaces for renewable power sources in which it enables a flexible grounding [26, 27], see **Fig. 1.4(a)** for MVDC PV collector grids and **Fig. 1.4(b)** for a cascaded converter arrangement that connects utility-scale PV fields to the HV grid.

1.2 MV SST Key Challenges

Due to the requirements of low weight and compactness and/or high operating voltage of SSTs for the aforementioned electric transport applications, the challenges arise especially in the realization of a DC-DC converter stage. State-of-the-art high efficiency DC-DC converters with galvanic isolation typically feature gravimetric power densities up to 5 kW/kg, however, as mentioned above, aircraft applications require gravimetric power densities greater than 10 kW/kg at an efficiency of $\eta = 99\%$. This can be achieved using MV converters operated at high switching frequency, which enables a reduction of the weight of magnetic components, provided suitable MV power switches are available. With 10 kV SiC MOSFETs very low switching losses

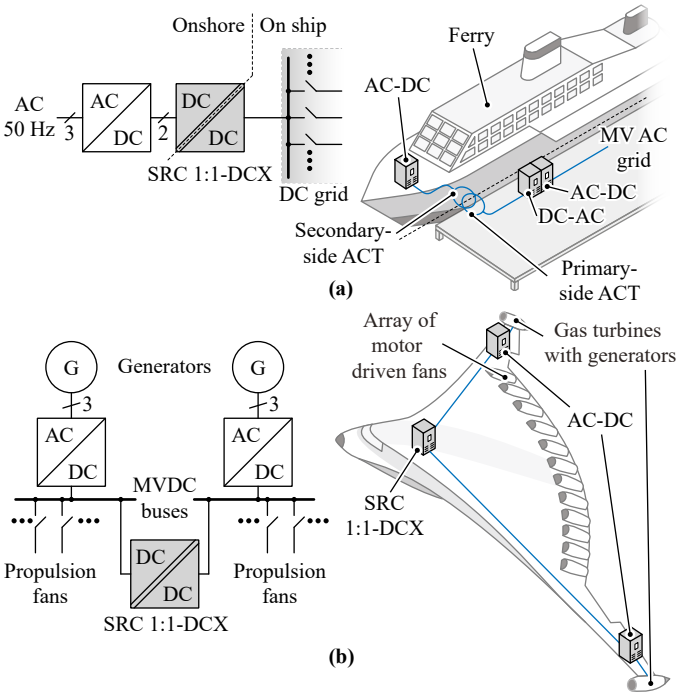


Fig. 1.3: (a) A primary DC power system on-board of a vessel for DC-based electric propulsion [22]. The connection to the shore is realized through a DCX and energy transfer occurs when the vessel is docked, i.e., the secondary coil of the DCX is placed in the vessel and the primary coil is placed onshore. **(b)** Concept of TeDP aircraft, based on [28], where the 1:1-DCX could be used as a DC bus-tie.

can be achieved for soft-switching operation, which, in principle, enables MV converters to be operated with very high switching frequencies exceeding 100 kHz. However, in conventional DC-DC converters with MV/MF magnetic-core transformers (MCTs), a substantial part of the core window is required for insulation (between the coils and between coils and core). Due to the associated low fill factor of the core window and further limitations imposed by the core material, limited benefits are resulting at high switching frequencies. However, literature on inductive power transfer systems [29] reveals that high efficiency operation of transformers can be achieved at high frequencies also with loosely coupled coils, which potentially allows

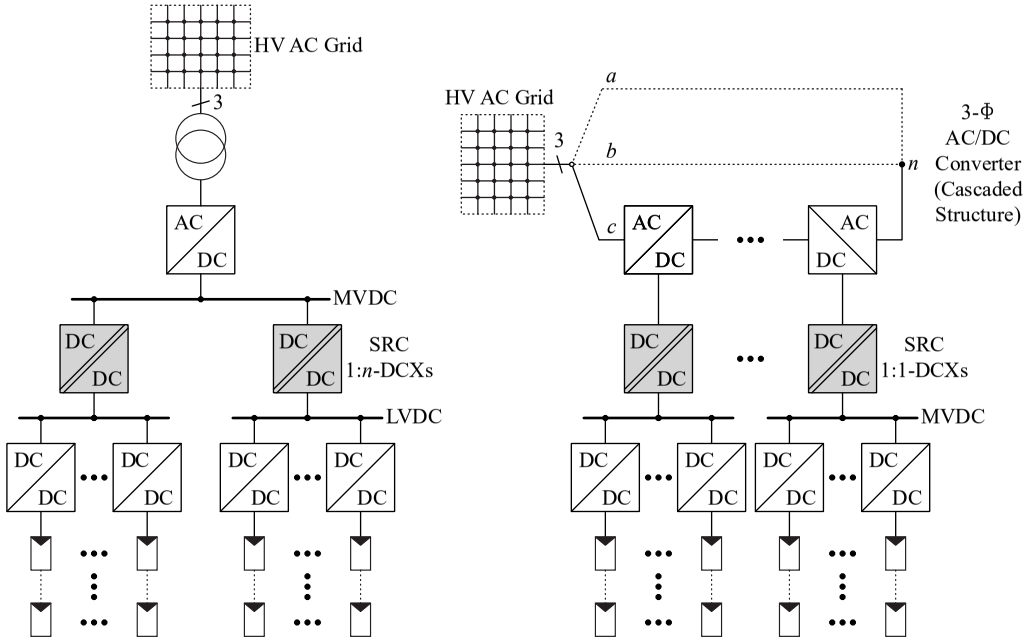


Fig. 1.4: (a) MVDC collector grids of large PV plants with 1:*n*-DCX or 1:1-DCX as isolated DC-DC interface. **(b)** 1:1-DCX as part of a cascaded converter cells arrangement that connects utility-scale PV fields to the HV grid.

for ultra-light weight systems with air-core transformers (ACTs). Therefore, it is not yet clear how ACTs perform, compared to conventional MCTs, in high-power MV/MF applications.

In addition to the challenges related to MV/MF transformers, further challenges appear with regard to the employed power converter topology and power semiconductors, since the blocking voltages required for the realization of DC-DC converter topologies typically exceed the capabilities of today's cutting-edge 10 kV and 15 kV SiC power semiconductors. This renders multi-level converters or multi-cell structures necessary, which, besides a high number of power semiconductors, leads to high efforts concerning the required capacitors. Alternatively, a series connection of switches, e.g., in super-cascode structure could be employed. However, this arrangement does not provide active means to stabilize the blocking voltages of the individual switches and in general is not a versatile solution due to the high complexity already on the switch level, which limits the scalability concerning blocking voltage.

Recent developments increasingly aim for circuit and control concepts that utilize multi-cell structures only to achieve defined blocking voltages across series connected switches while, by means of quasi-2-level (Q2L) operation capacitive energy storage requirements are minimized. Q2L operation of modular multi-level converter (MMC) structures has been proposed in the literature, which considers staggered switching to achieve reduced average voltage slew rates besides low module capacitor volumes, however the circuits still demand for high numbers of power semiconductors. But, Q2L operation of a flying capacitor converter (FCC) based half-bridge was found to be an interesting alternative approach. However, this concept has not yet been considered for the realization of a MV versatile power semiconductor stage. Such analysis could reveal the best candidate to overcome unfavorable scaling properties of high voltage capacitors which would allow to simplify the converter realization by means of integration of the capacitors into a SiC Super-Switch Intelligent Power Module (SS-IPM).

It is in this context, therefore, that this thesis aims to tackle those two main challenges related to realization of lightweight MV/MF transformers and MV power semiconductor stages, and hence to develop novel technologies for SSTs.

1.3 Aims and Contributions

PART 1 - **Medium-Voltage Medium-Frequency Transformers**

The objective of Part I of this thesis is to explore the suitability of air-core transformers for a lightweight and ≥ 99 % efficient 166 kW / 7 kV DC-DC SST and benchmark them against magnetic-core counterparts. In this regard, two fully-rated MFT prototypes are designed and constructed. Furthermore, the proposed models and optimization results are validated through comprehensive testing. Additional focus is on insulation, cooling, shielding of the magnetic stray fields and dielectric losses.

The contributions of this part of thesis to the field of MV/MF transformers are listed below:

- *Overview of MFTs* - The design of MFTs involves various trade-offs between competing goals, e.g., power density, efficiency, insulation voltage, and a large number of degrees of freedom, e.g., winding and core geometry, insulation material, operating frequency, cooling method. It is hence a challenging process resulting in vastly diversified MFT prototypes. To provide the background for investigations, the overview of state-of-the-art MFTs is prepared with classification of insulation voltage, operating frequency, efficiency and gravimetric power density.

- *Ultra lightweight air-core transformer* - There are several promising arrangements for the realization of ACTs, e.g., planar coils, coaxially wound cable or cylindrical solenoids. To identify the applicability of ACTs for MV high-power SSTs those arrangements need to be evaluated considering the desired performance indices (efficiency, power density) and ease of construction. In this context, the most favourable arrangement is selected, i.e., cylindrical solenoids, and through the means of Pareto optimization an ultra lightweight 166 kW / 7 kV ACT prototype is designed and built. Furthermore, the comparison of optimization and experimental results reveals that the employed relatively straightforward models capture the key performance characteristics quite accurately, especially regarding the expected ACT efficiency and the mass of its active part.

- *Weight-optimized magnetic-core transformer* - Given the aforementioned large number of degrees of freedom and various objectives in the design of MFTs, the constructed ACT cannot be fairly compared to existing prototypes. Therefore, a weight-optimized dry-type 166 kW / 7 kV MCT is designed and constructed for a fair benchmarking. In order to increase the achievable gravimetric power density, advanced forced air cooling concepts need to be explored, e.g., by gapping of the stacked cores to obtain air channels and increased core cooling surfaces. Both prototypes

are experimentally verified and a comparison of their performance is presented.

- *Magnetic shielding of MFTs* - Magnetic flux density in the proximity of MFTs, especially in ACTs or close to the air gap in the MCTs, can reach several mT, causing eddy-current losses in metallic elements and disturbances in nearby circuitry. It is therefore interesting to analyze the stray magnetic fields and compare them against the ICNIRP 2010 guidelines. The stray magnetic fields are simulated using FEM and it is found that the ACT requires shielding. To realize the shielding two methods can be used, i.e., conductive and magnetic shielding. Targeting a lightweight shielding, a conductive (aluminum) shielding is realized for the ACT. Furthermore, a setup for the measurement of magnetic fields is built and used to verify the simulations and efficacy of the proposed shielding.
- *MV insulation in MFTs* - High insulation voltage requirement necessitates special care in the design of insulation in order to limit the electric fields inside transformers and ensure reliable and partial-discharge-free operation. To obtain compact MCTs a dry-type insulation is preferred, e.g., by potting the windings in silicone or epoxy. However, potting comes with several drawbacks of dry-type insulation, e.g., the need for a void-free process, handling of increased thermal resistances, or higher parasitic capacitances. To circumvent those disadvantages, air can be used as an insulation medium in ACTs. Furthermore, the required clearance and creepage distances can be tailored, even for a finished design, by inserting appropriate barrier elements between the coils, facilitating scalability of the insulation system.
- *Dielectric losses in MFTs* - Dielectric losses can contribute a non-negligible share of total MFT losses in case of dry-type insulation. To clarify that the losses can be computed with the use of FEM electric field simulations and validated with the measurements of the dielectric responses of the entire transformer assemblies. It is found that initial environmental conditioning of silicone insulation, in particular the initial moisture content, has a high impact on the dielectric losses. In order to explicate this impact, first silicone specimen and then the MCT are stored in different environments at different humidity and temperature, and afterwards thorough measurements of the dissipation factor are conducted. Contrarily, it is found that in the ACT due to the air insulation, the dielectric losses can be neglected.

- *DCX-level application oriented evaluation* - The considered MFTs are the core part of a 166 kW / 7 kV 1:1-DCX and their distinct properties and trade-offs are reflected in the performance on the system level. To clarify which concept is the most suitable for a specific application, a qualitative discussion of the key features is conducted to aid the design of SSTs. The special emphasis is on: partial-load and nominal efficiency, power density, linearity, operating temperature, overload capabilities, stray magnetic fields, insulation coordination, mechanical construction, resonant capacitor banks and semiconductor stages.

PART 2 - **MV Power Semiconductor Stage**

The objective of Part II of this thesis is to analyze quasi-2-level (Q2L) operation of a 5-level flying capacitor half-bridge with regard to the realization of a versatile MV power semiconductor stage. Furthermore, the goal is to provide a load-independent balancing method of FC voltages. In this context, a demonstrator prototype is built and used to experimentally verify the Q2L operation and proposed open-loop and closed-loop balancing methods. Further focus is on the module integration of the investigated FCC half-bridge, i.e., all power semiconductors, capacitors, gate drivers, the voltage balancing control, the isolated gate drive power supplies, the isolated cooling surfaces, and a common-mode emission shield would be integrated into a power module stage.

The contributions of this part of thesis to the field of MV power semiconductor stage realizations are recognized as follows:

- *Q2L operation of the FCC-based half-bridge* - Q2L modulation of multilevel converters, which uses intermediate voltage levels only during the switching transitions, is known to be an advantageous type of a power semiconductor stage realization due to the minimized capacitive requirements and reduced $\mathrm{d}v/\mathrm{d}t$. However, it is not clear for the Q2L-operated FCC, what are the charges delivered to the FCs for soft- and hard-switching, and switching transitions at zero load current. In this regard, simulations with non-linear models of switches are developed and comprehensive analyses of transitions are performed.

- *Cell multiple switching without output current* - The charges delivered to the FCs and hence the balancing of FC voltages relies on the output current of the FCC. The balancing is therefore, no longer possible, when no output current is present (no-load operation). Due to non-idealities in the switches and circuit, over time the FC voltages could diverge

from the well-defined voltage levels and pose a threat of switch voltage breakdown. To tackle the problem of balancing without an output current, a method called *cell multiple switching* (CMS) is developed. In switching transitions with CMS, additional hard-switching commutations of MOSFETs are inserted and the flow of current required to charge switches' output capacitances leads to exchange of energy between the FCs, hence enabling balancing of their voltages.

- *Closed-loop method of load-independent voltage balancing* - The aforementioned in-depth understanding of charges delivered to the FCs in all types of transitions enables the development of a closed-loop (active) method of FC voltages balancing. Within this framework, a concept of load-independent voltage balancing is proposed and it comprises of a model predictive controller with FC voltage or cell voltage reference tracking and CMS for balancing at zero output current. Finally, a hardware demonstrator of a 5L-FCC is built and used to experimentally validate the proposed concepts.

- *Concept of a MV SiC "Super-Switch" Intelligent Power Module (SiC-SS-IPM)* - The realization of a DC-DC step-down converter for a single-phase 15 kV / 16.7 Hz traction system leads to an input-side DC-link voltage of 28 kV. Hence, the DC-DC's MV side, realized as a half-bridge, requires power electronic switches which withstand blocking voltages that exceed the rating of today's cutting-edge 10 kV SiC MOSFETs. On this basis, a 300 kVA / 40 kV Q2L-5L-FCC half-bridge is evaluated for the realization of a power semiconductor stage with focus on the semiconductor and capacitor volumes. In addition, the integration of the Q2L-FCC half-bridge into the SiC-SS-IPM which includes all circuits for gate drivers, measurements, and control is considered. This concept is also studied to evaluate the impact of Q2L operation on the electrical insulation ($\mathrm{d}v/\mathrm{d}t$ and dielectric losses) in comparison to a 2-level bridge-leg realized with a direct series connection of MOSFETs.

1.4 Outline of the Thesis

The core part of this thesis is structured in two parts and nine chapters, whose content is summarized herein. In particular:

Part 1 - **Medium-Voltage Medium-Frequency Transformers**

- **Chapter 2** introduces a unity-voltage-transfer-ratio 166 kW / 7 kV DC transformer (1:1-DCX) based on a series resonant converter (SRC) topology which is considered for the isolated DC-DC SST converter stage. First, the specifications, operation principle and emerging applications for the 1:1-DCX are briefly explained. Next, the modeling of the non-magnetic converter's components, i.e., semiconductors, DC-link and resonant capacitors is shown. Finally, the optimization routines for the ACT- and MCT-based DCXs are presented in detail. The considered 1:1-DCX is a converter framework for the investigated two types of MFTs, i.e., an ACT, see **Chapter 3**, and an MCT, see **Chapter 4**.

- **Chapter 3** explores the design and performance space of air-core transformers for the realization of a lightweight and highly efficient 166 kW / 7 kV 1:1-DCX. Thus, first possible transformer coil arrangements and their geometries, e.g., coaxial cable, half-filled flat disc, double-D or coaxial cylindrical solenoids are briefly investigated. Next, the coaxial cylindrical solenoids geometry is selected and its coil interconnections and shielding configurations are analyzed. Furthermore, 2–D and/or 3–D FEM simulations are employed for the modeling of an ACT and used in multi-objective optimization with focus on high achievable gravimetric power density to select the optimum design of an ACT. Afterwards, a fully-rated 166 kW / 7 kV prototype is designed and built. Finally, simulation and optimization results are validated by extensive experimental testing.

- **Chapter 4** exhibits a weight-optimized conventional 166 kW / 7 kV magnetic-core MFT as a benchmark for the ACT presented in **Chapter 3**. For the realization of the MCT, a dry-type (silicone) transformer with forced air cooling is selected. Similarly as for the ACT, a multi-objective optimization is used to reveal the most suitable type of the MCT regarding the core material (ferrite) and configuration (E-core with shell-type winding), and to select the design for construction. Next, the detailed design procedure is provided and critical aspects are compared with the ACT. In the final step, a fully-rated prototype is constructed and experimentally tested.

- **Chapter 5** presents a comparative evaluation on component- and system-level of the investigated ACT-DCX and MCT-DCX. First, the results of multi-objective optimizations are discussed in detail. Afterwards, the constructed resonant capacitor banks are shown and the

realization of required switching stages with DC-link capacitors is discussed. This is followed by an experimental comparison of selected aspects of the ACT and MCT prototypes, i.e., examination of dielectric losses, especially the influence of initial environmental conditioning on the dissipation factor of the silicone, long-term overload capability and partial discharge measurement. Finally, the system-level performance of the ACT-DCX and MCT-DCX is discussed. In particular, the focus is on breakdowns of masses, volumes, and losses, partial-load efficiency, and a qualitative application-oriented evaluation.

Part 2 - **MV Power Semiconductor Stage**

- **Chapter 6** discusses state-of-the-art methods to realize a MV power semiconductor stage, in particular, the direct series connection of semiconductors, super-cascode configurations, or multi-level converter structures, i.e., the modular multi-level converter (MMC) and flying capacitor converter (FCC). The considerations reveal that the Q2L-operated FCC is the most promising realization owing to not only minimized capacitive energy storage requirements and lower average voltage slew rates but also due to the snubberless design and low number of components. Moreover, based on typical voltage requirements and industrial practices a 5-level FCC (5L-FCC) is selected for analysis as a good trade-off between the number of levels (complexity) and voltage scalability for available semiconductor ratings. Next, the fundamental principles of Q2L operation of a 5L-FCC half-bridge for zero voltage switching (ZVS) and hard-switching (HS) transitions with non-zero output current are identified. Moreover, Q2L transitions with zero load current are analyzed, too, and a generic description of resulting charge and voltage increments is derived. With this, a robust voltage balancing controller for a versatile half-bridge can be developed, i.e., suitable for symmetric (typical, e.g., for an isolated DC-DC converter) or asymmetric (typical, e.g., for a PFC rectifier or a motor inverter) output currents.

- **Chapter 7** proposes a comprehensive concept for load-independent balancing of the voltages of Q2L-FCCs. For non-zero load current a model predictive controller (MPC) is employed to identify the commutation sequence of the individual switches within a Q2L transition (1-step horizon) from all possible permutations by minimizing the predicted deviation from the reference values. In case of zero load current, a

novel MPC-based approach with flying capacitor (FC) voltage reference tracking (6-step horizon) using cell multiple switching (CMS) is presented. It relies on the insertion of additional zero-current commutations within a Q2L transition which creates the flow of current in the cells required to charge switches' output capacitances. This in turn, leads to exchange of energy between the capacitors, i.e., DC-link capacitors or FCs, adjacent to the commutated switches. Thus, by adding additional switching actions, the FC voltages can be adjusted. A 5L-FCC LV half-bridge demonstrator is realized and used to thoroughly examine the Q2L transitions and proposed balancing methods. The experiments of HS and ZVS output voltage transitions, load transients, as well as of start-up and shut-down operation modes show good agreement with the proposed description and simulations. Furthermore, the presented closed-loop cell voltage control concept demonstrates an excellent average FC voltage tracking as well as symmetric cell voltages.

- **Chapter 8** discusses an integration of a complete 5L-FCC bridge-leg, including power semiconductors (10 kV SiC MOSFETs), flying and commutation DC-link capacitors, gate drivers, isolated cooling interfaces, measurements, and Q2L control into a 300 kVA / 40 kV SiC Super-Switch Intelligent Power Module (SiC-SS-IPM). In this context, the dimensioning of semiconductors and capacitors is presented and in particular their volumes are evaluated. The realization of a SiC-SS-IPM is modeled and visualized including the placement of the components. Furthermore, the impact of a Q2L operation on the electrical insulation is studied by analyzing the output voltage spectrum and dielectric losses, and it is compared to waveforms of a 2-level bridge-leg with series connection of MOSFETs.

- **Chapter 9** concludes the thesis and summarizes the main contributions and key insights. Additionally, an outlook on possible future research topics is provided.

1.5 Publications

The main results of the research activity created as part of this thesis have been published in international scientific journals and conference proceedings, or presented at workshops. The most significant contributions are listed in the following in reverse-chronological order.

1.5.1 Journal Papers

④ **P. Czyz**, P. Papamanolis, F. Bruguera, T. Guillod, F. Krismer, V. Lazarevic, J. Huber, and J. W. Kolar, "Load-Independent Voltage Balancing of Multi-Level Flying Capacitor Converter in Quasi-2-Level Operation," *Electronics*, vol. 10, no. 19, pp. 1-31, 2021.

③ **P. Czyz**, T. Guillod, D. Zhang, F. Krismer, J. Huber, R. Färber, C. M. Franck and J. W. Kolar, "Analysis of the Performance Limits of 166 kW / 7 kV Air-Core and Magnetic-Core Medium-Voltage Medium-Frequency Transformers for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.

② T. Guillod, **P. Czyz**, and J. W. Kolar, "Geometrical Optimization of Medium-Frequency Air-Core Transformers for DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2022.

① **P. Czyz**, T. Guillod, F. Krismer, J. Huber, and J. W. Kolar, "Design and Experimental Analysis of 166 kW Medium-Voltage Medium-Frequency Air-Core Transformer for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.

1.5.2 Conference Papers

③ P. Favre-Perrod, J. Biela, M. Carpita, A. Christe, **P. Czyz**, D. Dujic, C. M. Franck, T. Guillod, F. Krismer, J. W. Kolar, S. Milovanovic, M. Paolone, F. Rachidi, R. Razzaghi, T. Schultz, G. Tsolaridis, M. Utvic, and Z. Wang, "Swiss Competence Center on Energy Research FURIES - Overview and Contributions in the Area of Power Electronics and SmartGrids," in *Proc. of the IEEE European Conf. on Power Electron. and Appl. (EPE)*, 2019.

② **P. Czyz**, P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "New 40 kV / 300 kVA Quasi-2-Level Operated 5-Level Flying Capacitor SiC "Super-Switch" IPM," in *Proc. of the IEEE Int. Power Electron. Conf. (ECCE Asia)*, 2019.

① **P. Czyz**, T. Guillod, F. Krismer, and J. W. Kolar, "Exploration of the Design and Performance Space of a High Frequency 166 kW / 10 kV SiC Solid-State Air-Core Transformer," in *Proc. of the IEEE Int. Power Electron. Conf. (ECCE Asia)*, 2018. Awarded a *Best Paper Award*.

1.5.3 Patents

① **P. Czyz**, P. Papamanolis, V. Lazarevic, T. Guillod, F. Krismer, and J. W. Kolar, "Voltage Source Converter Configured to Transition Between at Least Two Voltage Levels," SE Patent 2051394-1, 2020.

1.5.4 Workshops, Tutorials, Keynotes, etc.

③ **P. Czyz**, T. Guillod, F. Krismer, and J. W. Kolar, "Experimental Analysis of a 166 kW Medium Voltage/Frequency Air-Core Transformer for 1:1-DCX Applications," *Presentation at the IEEE Energy Conversion Congress and Exposition (ECCE USA), Special Session on Sustainable Energy Systems and Opportunities for Power Electronics"*, Detroit, USA, 2020.

② J. W. Kolar, F. Krismer, **P. Czyz**, T. Guillod, and P. Papamanolis, "Emerging MV Applications - Data Centers & Superfast EV Charging," *Presentation at the ECPE Workshop on Power Semiconductors in Medium Voltage Applications – SiC vs. Silicon"*, Freiburg i. Br., Germany, 2019.

① **P. Czyz**, T. Guillod, F. Krismer, and J. W. Kolar, "Do We Need Magnetic Cores? Exploration of the Design and Performance Spaces of High Frequency SiC Solid-State Air-Core Transformers," *Presentation at the Technical Workshop on Special Transformers for SSTs and Pulsed Power Applications"*, Rapperswil, Switzerland, 2018.

Part 1

Medium-Voltage Medium-Frequency Transformers

2
1:1-DC Transformer

This chapter summarizes major research findings also published in:

- **P. Czyz**, T. Guillod, D. Zhang, F. Krismer, J. Huber, R. Färber, C. M. Franck and J. W. Kolar, "Analysis of the Performance Limits of 166 kW / 7 kV Air-Core and Magnetic-Core Medium-Voltage Medium-Frequency Transformers for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.
- **P. Czyz**, T. Guillod, F. Krismer, J. Huber, and J. W. Kolar, "Design and Experimental Analysis of 166 kW Medium-Voltage Medium-Frequency Air-Core Transformer for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.

Executive Summary

For the realization of a lightweight and high-efficiency isolated MV DC-DC converter a series resonant DC-DC converter operated at the resonance frequency is selected, which therefore acts as a DC transformer (DCX). Advantageously, the DCX tightly couples the DC input and output voltages without the need for closed-loop control and features zero-voltage switching (ZVS) over the full load range. A 166 kW / 7 kV 1:1-DCX converter system with two types of MV/MF transformers is considered, i.e., an air-core transformer (ACT) and a magnetic-core transformer (MCT). Furthermore, in this chapter, the modeling of 166 kW / 7 kV 1:1-DCX systems and the employed multi-objective optimization routines are presented. The two types of MFTs are subsequently investigated in **Chapter 3** (ACT) and in **Chapter 4** (MCT).

Tab. 2.1: Specifications of the 1:1-DCX.

P_N	166 kW	output power
V_{dc}	7 kV(±3.5 kV)	input and output DC voltage
V_i	10 kV DC	pri.-sec. insulation voltage

This chapter first introduces the selected type of an isolated MV DC-DC converter realization, i.e., a DC transformer (DCX) which could be built using the two types of MV MFTs investigated in **Chapter 3** (air-core transformer, ACT) and in **Chapter 4** (magnetic-core transformer, MCT). Next, the employed multi-objective optimization and the modeling of DCX components are presented in detail. For the sake of clarity, the results of a multi-objective optimization with focus on η-γ-ρ-performance space (efficiency, gravimetric power density, and volumetric power density) and thus the performance limits, are presented in **Chapter 5**, i.e., after the MV/MF ACT and the MCT are discussed in detail. Furthermore, **Chapter 5** includes a comparative evaluation on a component- and system-level of the resulting ACT-DCX and MCT-DCX, and provides an application oriented evaluation.

2.1 1:1-DCX Characteristics and Applications

Regardless of whether solid-state transformers (SSTs) interface AC and/or DC systems, their core conversion stage is an isolated MV DC-DC converter, i.e., a MVDC-LVDC or MVDC-MVDC converter. In the light of the requirements of future electric transportation applications (see **Chapter 1**, e.g., high-power EV charging stations, future traction vehicles, fast charging in future ships, and future aircraft with distributed propulsion systems), the DC-DC SST should be realized with low weight and high efficiency. Therefore, in Part I of this thesis we exemplify the considerations on a 166 kW DCX system, i.e., a series resonant DC-DC converter operated at the resonance frequency, which therefore acts as a DC transformer (DCX) [16, 18–20]. The DCX tightly couples the DC input and output voltages without the need for closed-loop control. **Tab. 2.1** lists the system's key specifications. Furthermore, targeting a lightweight and high-efficiency realization, we focus on realization of a MF transformer (MFT), which is a core element of the DCX, and we explore the performance limits of two types of 166 kW DCX systems, i.e., air-core transformer (ACT) based and magnetic-core transformer (MCT) based.

We consider a unity ratio of primary-side to secondary-side DC port voltages (1:1-DCX), which is suitable for several applications: in DC bus-tie applications [23] (see **Fig. 2.1(a)**), the galvanic isolation of the 1:1-DCX enables a more flexible grounding of subsystems than conventional switches or connectors do. In open-loop operation it ensures equal bus voltages and free bidirectional exchange of power. Furthermore, the 1:1-DCX can provide power flow control or output current limitation, e. g., by employing the quantum operating mode introduced in [30]. To facilitate the coupling of two AC grids [31], the 1:1-DCX can be complemented by AC-DC and DC-AC converters, which then take over the power flow control, see **Fig. 2.1(b)**. Furthermore, the ACT-based DCX (ACT-DCX), due to the absence of a magnetic core, lends itself to the realization of contactless (and hence spark-free) plugs (see **Fig. 2.1(c)**) which could find use in subsea applications or in other harsh or explosion-prone environments such as in mining [32–35]. Finally, a 1:1-DCX facilitates straightforward high-power back-to-back testing, i.e., the secondary-side DC port can be directly connected back to the primary-side DC port. In this configuration, the system can be tested at high rated power levels with the supply only covering the comparably low losses of the system [29]. Moreover, as shown in **Fig. 2.1(d)** and **(e)**, several 1:1-DCX converters can be combined to scale the overall voltage or power rating, depending on the application. Note that the input-series, output-parallel (ISOP) configuration would require a higher insulation voltage rating between the transformer's primary and secondary windings. Using an input-parallel, output-parallel (IPOP) configuration of six 166 kW-1:1-DCX converters, a 1 MW system could be realized. **Fig. 2.2(a)** shows the SRC topology of the 1:1-DCX converter and exemplary key waveforms are presented for the ACT-DCX in **Fig. 2.2(b)** and for the MCT-DCX in **Fig. 2.2(c)**. The series resonant capacitor, C_r, is chosen such that it compensates the corresponding stray inductance, L_σ, at the operating frequency, which thus equals the resonant frequency, i.e., $f_\mathrm{s} = f_0 = 1/(2\pi\sqrt{C_\mathrm{r} L_\sigma})$. Considering the selected DC bus voltage of 7 kV, available 10 kV SiC MOSFETs can be employed with sufficient margin regarding the blocking voltage utilization. The realization with one half-bridge and one capacitive voltage divider per bridge requires only half the number of switches compared to a full-bridge [12]. Advantageously, the SRC converter features zero-voltage switching (ZVS) over the full load range, which is supported by the magnetizing current that appears in the primary- and secondary-side half-bridges [18], and well-defined voltages across the switches.

In the following, the modeling of 166 kW / 7 kV 1:1-DCX systems and employed multi-objective optimization routines are presented.

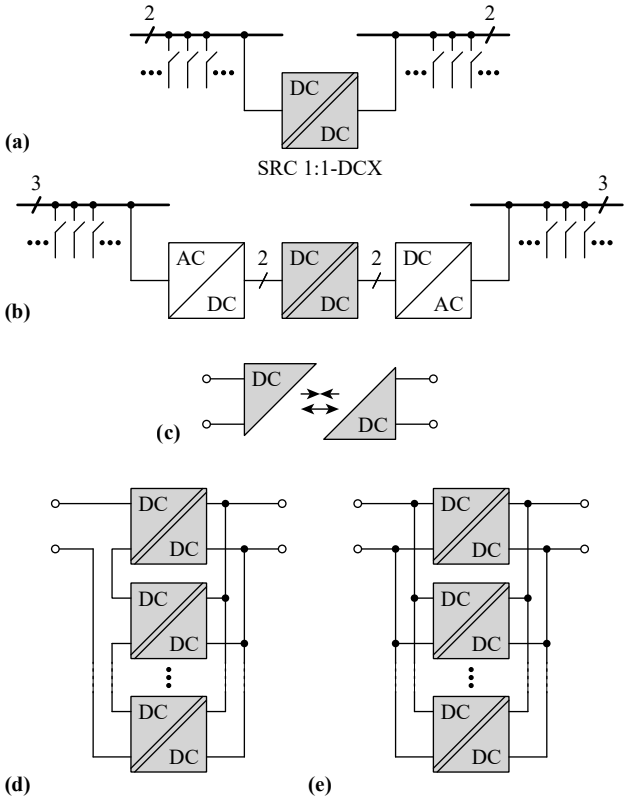


Fig. 2.1: 1:1-DCX applications and options for scaling voltage and power ratings. **(a)** 1:1-DCX as a power electronic link between two MVDC buses, acting as a flexible bus-tie switch. **(b)** Coupling of two AC grids [31], where the 1:1-DCX provides isolation and dedicated AC-DC converters control the power flows (active power, input- and output-side reactive power). **(c)** An air-core transformer facilitates the realization of contactless and spark-free plugs, e.g., for subsea applications. Combinations of several 1:1-DCX in either **(d)** input-series, output-parallel (ISOP) or **(e)** input-parallel, output-parallel (IPOP) configuration facilitate a scaling to higher overall voltage or power ratings.

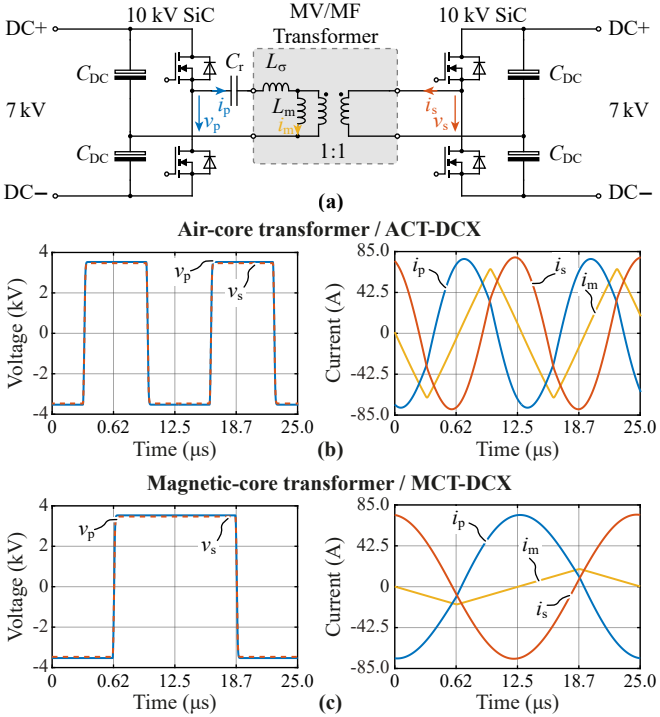


Fig. 2.2: (a) Converter topology of the considered 166 kW / 7 kV 1:1-DCX. Simulated current and voltage waveforms at rated power and with an operating frequency resulting for optimal designs (see **Chapter 5**). **(b)** f_s = 77.4 kHz for the ACT. **(c)** f_s = 40.0 kHz for the MCT.

2.2 Multi-Objective Optimization

To derive the performance limits (efficiency, gravimetric power density, and volumetric power density) of MCT- and ACT-based 166 kW / 7 kV 1:1-DCX converter systems, we employ the multi-objective optimization approach illustrated by **Fig. 2.3**, which calculates the performance indices for a wide range of different designs. In general, two separate strategies are employed depending on the transformer type. For the ACT (cf. **Fig. 2.3(a)**), a 2-D-FEM-based optimization is used, which first calculates the electromagnetic fields in the frequency domain, which are then used to calculate the performance indices. For the MCT (cf. **Fig. 2.3(b)**), we employ a semi-analytical (analytical equations but solved numerically) optimization routine. With the properties of a given transformer design, the system-level performance can be obtained by appropriately dimensioning and modeling the DCX's remaining components (switching stage, resonant capacitors, cooling system).

2.2.1 1:1-DCX Converter Modeling

As mentioned in the introduction and shown in **Fig. 2.2**, a 1:1-DCX is a series resonant converter. To realize the desired DCX behavior, the resonant tank formed by the transformer's leakage inductance, L_σ, and a series resonant capacitor, C_r, must be tuned such that C_r compensates the leakage inductance at the desired operating (switching) frequency, i.e., $f_\mathrm{s} = f_0 = 1/(2\pi\sqrt{C_\mathrm{r} L_\sigma})$.

The detailed considerations of MV/MF transformers including configurations and modeling are presented in **Chapter 3** for the ACT realization and in **Chapter 4** for the MCT realization.

With regard to the DC bus voltage of 7 kV and a certain margin regarding the blocking voltage utilization, we consider 10 kV SiC MOSFETs from CREE/Wolfspeed [36, 37]. Note, that the primary and secondary switching stages are built as half-bridges with a split DC-link capacitor to halve the number of switches used (as compared to full-bridge circuits, [12]). We model conduction losses with the on-state resistance at a junction temperature of 125 °C, i.e., 275 mΩ per device (note that a device/package contains two paralleled dies). Making use of the magnetizing current that appears in both, the primary-side and the secondary-side half-bridges, the DCX achieves zero-voltage switching (ZVS) for all operating points [18]. The corresponding residual soft-switching losses, which are non-negligible for the considered switching frequencies, are modeled with experimental data from [38, 39]. **Tab. 2.2** summarizes the key data of the selected semiconductors.

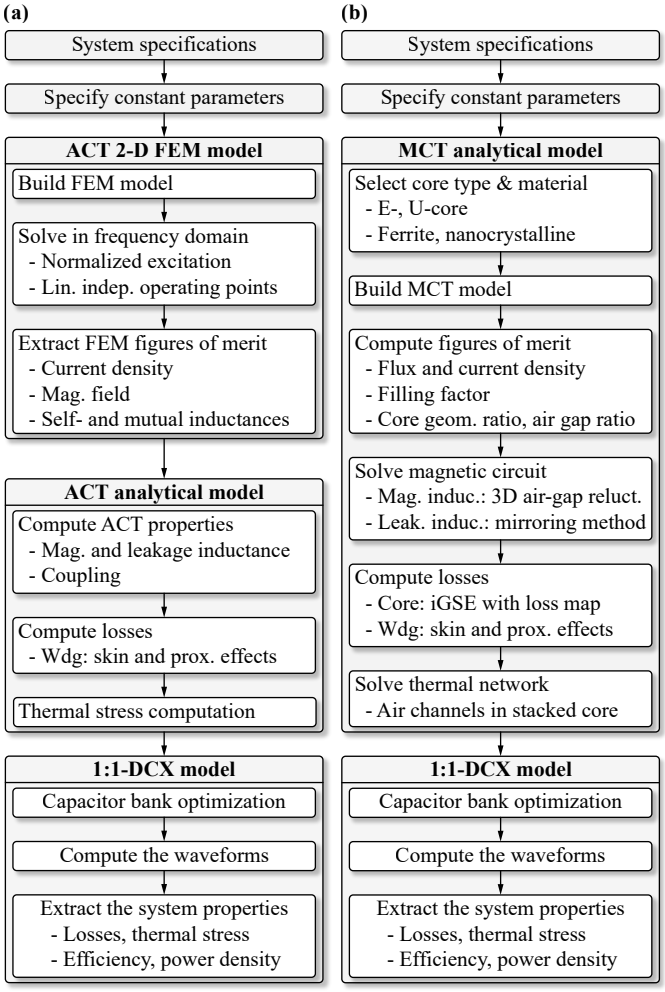


Fig. 2.3: Optimization flowcharts for **(a)** ACT- and **(b)** MCT-based 1:1-DCX systems.

Tab. 2.2: Parameters used for modeling of the 1:1-DCX components.

SiC MOSFET package with 2 parallel dies		
$V_{\mathrm{ds,max}}$	10 kV	max. blocking voltage
$I_{\mathrm{ds,max}}$	2x18 A	max. drain current
$R_{\mathrm{ds,on}}$	550/2 mΩ	on-state res. @ 125°C
P_{max}	100 W	max. package dissipation
$n_{\mathrm{pack,max}}$	3	max. parallel packages
Resonant capacitors		
$U_{\mathrm{r,max}}$	10 kV	max. peak voltage
$\tan\delta_{\mathrm{r}}$	0.05 %	dissipation factor
$e_{\mathrm{r,m}}$	1 J/kg	gravim. energy density
$e_{\mathrm{r,v}}$	2 J/dm^3	vol. energy density
DC-link capacitors		
$u_{\%}$	4 %	peak-peak voltage ripple
$\tan\delta_{\mathrm{link}}$	0.1 %	dissipation factor
$e_{\mathrm{link,m}}$	30 J/kg	gravim. energy density
$e_{\mathrm{link,v}}$	40 J/dm^3	vol. energy density

We consider high-power polypropylene capacitors (CELEM CSP120/200 [40]) for the resonant capacitor bank and high-voltage polypropylene capacitors for the DC-link (FTCAP FSP [41]). The losses are calculated via the corresponding dissipation factors. Volume and mass are modeled using the volumetric and gravimetric energy densities of existing prototypes based on these capacitors (see [42] for the resonant capacitors and [16] for the DC-link capacitors). **Tab. 2.2** provides the corresponding data.

Finally, we model volume and mass of the overall converter's forced-air cooling system (i.e., for switching stages, resonant capacitors, and MFT) based on experimental data from [38] and assume a total fan power consumption of 80 W.

3
MV/MF Air-Core Transformer Prototype

This chapter summarizes the major research findings also published in:

- **P. Czyz**, T. Guillod, F. Krismer, J. Huber, and J. W. Kolar, "Design and Experimental Analysis of 166 kW Medium-Voltage Medium-Frequency Air-Core Transformer for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.

Executive Summary

The galvanic isolation of solid-state transformers (SSTs) is typically realized with a medium-frequency (MF) magnetic-core transformer (MCT). Previous demonstrations indicate that achieving highly power dense and lightweight MCTs imposes several challenges on the design because of stringent requirements related to insulation and cooling. This work investigates the achievable efficiency of an optimized 166 kW / 7 kV air-core transformer (ACT), which is a core element of a DC Transformer (DCX), i.e., an unregulated DC-DC SST with a voltage scaling defined by the transformer turns ratio. The ACT features relatively low complexity of the construction, comparably high coupling values, and high efficiency. Modeling, optimization, and construction of the realized ACT are explained and guidelines regarding insulation, cooling, and shielding of the magnetic stray flux are discussed in detail. Furthermore, the prototype is experimentally validated to demonstrate its full functionality. In the investigated DCX, which is based on a series resonant converter (SRC) topology, the realized ACT is found to achieve a full-load efficiency of 99.5 % and an unprecedented gravimetric power density of 16.5 kW/kg. With the use of 10 kV SiC MOSFETs, the complete DCX is estimated to reach an efficiency of 99 % at 166 kW output power.

3.1 Introduction

Solid-state transformers (SSTs) provide galvanic isolation between two or more ports by means of medium-frequency (MF) transformers, whereby at least one port operates at medium-voltage (MV) levels (i.e., at voltages higher than 1 kV). Typical power levels range from 50 kW to several megawatts. These characteristic properties render SSTs a key component for a wide range of emerging applications, such as future hybrid smart grid systems with AC and DC sections [13, 17], grid interfaces for renewable power sources [26, 27], hyperscale data centers [15,16], high-power EV charging stations [10,11], future ships [21–23], and future aircraft with distributed propulsion and on-board MVDC grids [24, 25, 28].

The SST's key component, i.e., the medium-frequency transformer (MFT), is typically realized as a magnetic-core transformer (MCT), preferably as a dry-type MCT. However, the design of the MCT is challenging, mainly because of stringent requirements related to insulation and cooling, e.g., the need for void-free potting of the windings, handling of increased thermal resistances, and higher parasitic capacitances [43]. Furthermore, the mass of the magnetic cores and of the dry-type insulation limits the achievable gravimetric power density [16, 44, 45], which is clearly a drawback for the airborne applications mentioned above, but may also complicate handling during production and assembly in general.

Air-core transformers (ACTs) represent an interesting alternative as, by definition, they lack a magnetic core and hence the windings must still be isolated from each other but not from a magnetic core. This, in turn, facilitates the use of air as insulation medium and, simultaneously, for direct cooling of the windings. Hence, ACTs feature comparably straightforward construction and can achieve high gravimetric power densities; however, a lower volumetric power density must be expected. Recent publications reveal that high-power inductively coupled wireless power transfer (WPT) systems can reach high efficiencies close to 99 % and allow for overall DC-DC converter efficiencies up to about 96 % [29], even though these systems typically employ planar coils with relatively low coupling factors. The achievable efficiency of such inductive power transfer (IPT) systems increases with the product of quality factor and coupling coefficient [42]. Since for stationary applications alternative coil geometries with potentially higher coupling factors than planar coils (at similar quality factors) can be explored, ACT designs for SST applications should be able to achieve efficiencies considerably higher than 99 %. Furthermore, by taking advantage of available SiC power semi-

conductors that feature a high blocking voltage capability and a low on-state resistance, the realization of an ACT-based isolated DC-DC converter with an efficiency of close to 99 %, which is a typical target efficiency for SSTs, seems to be feasible, even considering that relatively high operating frequencies are necessary due to the low magnetizing inductance of an ACT (e.g., 85 kHz is a typical value for high-power IPT systems [29, 46]).

This chapter analyzes an ACT that is the key component of a series resonant converter (SRC) operated at the resonance frequency, which therefore acts as a DC transformer (DCX) [16, 18–20], i.e., tightly couples the DC input and output voltages without the need for closed-loop control. **Tab. 2.1** lists the system's key specifications. As presented in **Section 2.1**, we consider a unity ratio of primary-side to secondary-side DC port voltages (1:1-DCX) which facilitates straightforward high-power back-to-back testing, i.e., the secondary-side DC port can be directly connected back to the primary-side DC port. In this configuration, the system can be tested at high rated power levels with the supply only covering the comparably low losses of the system [29].

Figs. 2.2(a)-(b) show the SRC topology of the 1:1-DCX converter and exemplary key waveforms, respectively. The series resonant capacitor C_r is split into two capacitors, C_r1 and C_r2 (see **Section 3.2.2**), which are chosen such that they compensate the corresponding ACT stray inductances, $L_{\sigma1}$ and $L_{\sigma2}$, at the operating frequency, which thus equals the resonant frequency, i.e., $f_\mathrm{s} = f_0 = 1/(2\pi\sqrt{C_\mathrm{r1}L_{\sigma1}} = 1/(2\pi\sqrt{C_\mathrm{r2}L_{\sigma2}})$.

In this context, this chapter first covers generic realization options and coil arrangements for ACTs in **Section 3.2**. **Section 3.3** then provides an in-depth discussion of the modeling and the multi-objective optimization of the 166 kW / 7 kV ACT. **Section 3.4** covers the actual hardware design of the optimized ACT, including details related to the insulation system and the conductive shielding that limits magnetic stray fields in the ACT's surroundings. Furthermore, we conduct a thorough experimental analysis of the full-scale ACT prototype in **Section 3.5**. This includes small-signal measurements, large-signal waveforms, calorimetric loss measurements, and measurements of magnetic flux densities in the vicinity of the ACT to assess the efficacy of the shielding. **Section 3.6**, finally, discusses the efficiency characteristics of the ACT and the complete 1:1-DCX. The realized ACT prototype achieves a measured efficiency of 99.5 % for output power levels between 25 kW and 166 kW, and a gravimetric power density of 16.5 kW/kg. With the use of 10 kV SiC MOSFETs, the complete 1:1-DCX can attain an efficiency of 99 % at rated output power.

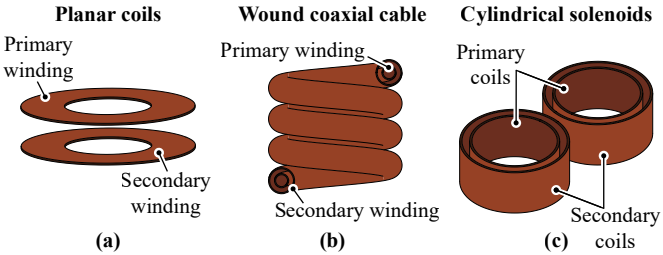


Fig. 3.1: Considered coil arrangements for the ACT realization: **(a)** (spiral) planar coils; **(b)** wound coaxial cable in a solenoid arrangement; **(c)** cylindrical solenoids.

3.2 Basic Air-Core Transformer Configurations

An ACT consists of at least one primary-side and one secondary-side coil, which can be arranged in various configurations. This section provides a brief survey and an initial, qualitative comparison of such realization options to identify the most suitable one for further optimization and design considerations. In addition, we introduce the two basic options (i.e., employing magnetic or conductive materials) to provide shielding against excessive magnetic stray fields.

3.2.1 Coil Arrangements

A first promising arrangement for the realization of an ACT uses planar coils, as typical for IPT/WPT systems [47], cf. **Fig. 3.1(a)**. Various lateral coil shapes have been employed, e.g., spiral [42], rectangular [42, 48] or double-D [29, 49, 50]. Planar coils are advantageous because they facilitate straightforward solutions for thermal management and insulation. High-power IPT systems typically achieve high efficiencies by adding magnetic cores to guide the magnetic fields (mainly on the non-mating sides of the coils), which increases the coupling and simultaneously contributes to the shielding of the magnetic stray flux [29, 47, 50]. However, the mass of the magnetic cores limits the achievable gravimetric power density, which is an important aspect regarding airborne applications and, more generally, handling considerations. Literature on high-power air-core IPT systems, i.e., planar coil arrangements without any magnetic material, is very scarce; a corresponding 40 kW system recently reported in [48] is characterized by

a relatively low overall DC-DC efficiency of around 90 %. Even though for stationary applications such arrangements of planar coils can be expected to achieve higher coupling than typical mobility-oriented IPT/WPT systems (e.g., because a shorter air gap between the coils may be feasible) and hence higher efficiency, the absence of magnetic cores would require other means for shielding of the magnetic stray flux. Most important, however, the bounding-box geometry of planar IPT coil arrangements has essentially only two degrees of freedom as they are necessarily flat, i.e., the lateral dimensions become larger with increasing power transfer capability. The possible aspect ratios are thus constrained and may not be suitable for some of the various potential ACT applications discussed in the previous section. To clarify those aspects, an in-depth theoretical analysis of the planar (spiral) arrangement for the realization of an ACT is investigated, however, it is not in the main scope of this thesis, therefore it is included in **Appendix A**.

Regarding MCTs with unity turns ratio and high insulation voltage requirements, windings made of a MV coaxial cable wound onto a magnetic core have been proposed [51–53]. Advantageously, this arrangement contains the leakage flux within the inter-winding space, i.e., between the core (primary-side winding) and the metallic shield (secondary-side winding) of the coaxial cable, which inherently provides galvanic isolation, too. The cooling of the inner winding, on the other hand, is not straightforward, and requires a comparably complex liquid- or forced-air cooling system. Furthermore, an ACT in this configuration (cf. **Fig. 3.1(b)**) would require long multi-turn coils [54] to achieve a sufficiently high magnetizing inductance. This complicates the manufacturing and cooling of the windings and a relatively low coupling must be expected even for a multi-turn coaxial-cable ACT; therefore we do not pursue this option further.

In [28] we proposed an ACT configuration consisting of a pair of coaxial solenoids, cf. **Fig. 3.1(c)**, i.e., essentially a winding configuration similar to that of a core-type MCT, but without a magnetic core (and adapted dimensions). This coil arrangement achieves relatively high coupling for the considered insulation voltages, features low-complexity construction and insulation (air), as well as simplified thermal management, as large surfaces are available for direct (forced) air cooling. Because of these favorable characteristics, we consider this coil arrangement for the subsequent optimization and design of a high-power MV/MF ACT. Note that the magnetic stray flux in the proximity of the ACT must be limited, which requires some sort of shielding (see **Section 3.2.3** below). First however different possibilities for interconnecting the arrangement's four coils shown in **Fig. 3.1(c)** to form

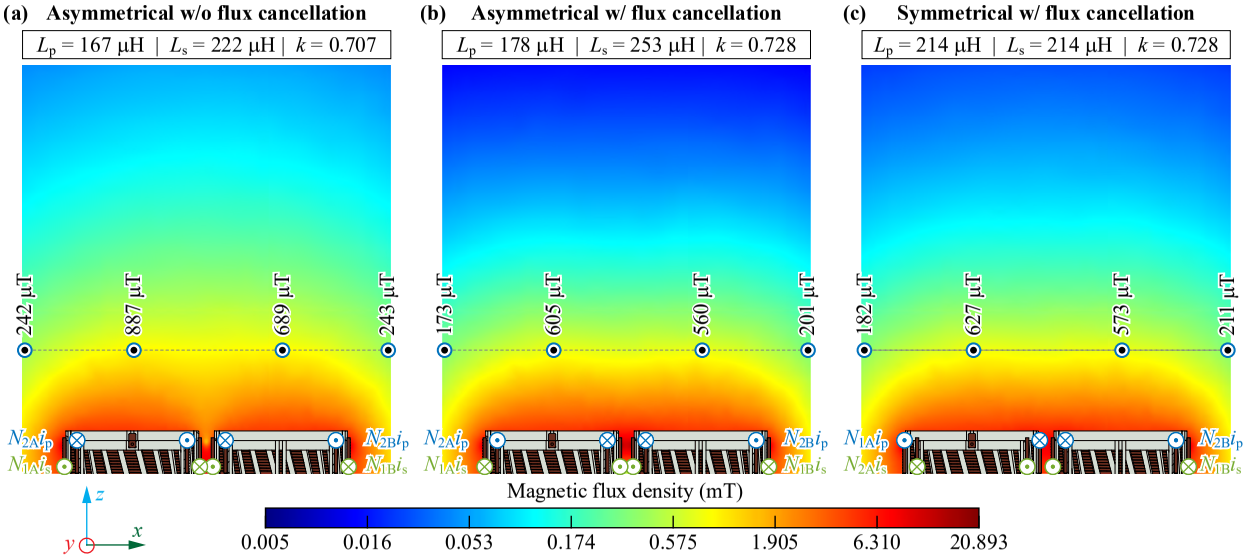


Fig. 3.2: FEM-simulated flux densities within the cut plane defined in **Fig. 3.3**: **(a)** coil interconnections with asymmetrical L_p (coils 2A with 2B) and L_s (coils 1A with 1B) without magnetic stray flux cancellation; **(b)** asymmetrical connections of the two sets of coils with partial cancellation of magnetic stray flux (note the inverted sense of winding of the coils on the left); **(c)** proposed coil interconnections with partial cancellation of magnetic stray flux and symmetrical self inductances L_p and L_s (note that the primary-side and the secondary-side winding each comprise one outer and one inner coil). In the simulations, nominal primary- and secondary-side currents, i_p and i_s respectively, are used.

a four-terminal (i.e., two primary-side and two secondary-side terminals) transformer are discussed.

3.2.2 Coil Interconnections

Considering the interconnections of the four coils, the straightforward approach would be to use two identical sets of two coaxially arranged coils, e.g., with the inner coils being connected in series to form the primary winding and the two outer coils connected likewise to form the secondary winding. **Fig. 3.2(a)** shows a 2-D finite-element method (FEM) simulation of the magnetic field for this case as well as extracted self inductances of the primary-side winding, L_p, and of the secondary-side winding, L_s, which are *asymmetric* (essentially because the diameters of both primary-side coils are larger than those of the two secondary-side coils).

Inverting the winding direction of the coils in one set achieves partial cancellation of the magnetic stray flux, as shown in **Fig. 3.2(b)**. However, whereas the coupling increases slightly, L_p and L_s remain similarly asymmetric as before.

Thus, **Fig. 3.2(c)** shows a *symmetric* interconnection of the coils, where the primary- and the secondary-side windings consist of one outer and one inner coil each, i.e., the series connection of coil 1A and coil 2B forms the primary-side winding, and the series connection of coil 1B and coil 2A forms the secondary-side winding (see **Fig. 3.3** for the definitions of the coil identifiers). Furthermore, the winding directions are such that again partial stray flux cancellation is achieved, i.e., the magnetic flux density averaged over the points indicated in the figure is about 25 % lower for the symmetrical case when compared to the asymmetrical interconnection without flux cancellation from **Fig. 3.2(a)**, however, 5 % higher than for the asymmetrical configuration with flux cancellation from **Fig. 3.2(b)**. Nonetheless, the benefits of symmetrical self inductances on the system level are significant: as the 1:1-DCX is then symmetric, too, it can operate with identical series resonant capacitance values on both sides of the transformer, which facilitates construction using standardized building blocks, e.g., resonant capacitor banks.

Thus, we consider two coaxially-arranged, cylindrical primary- and secondary-side windings and the symmetrical coil interconnection approach for the further analysis of the MV/MF ACT, see **Fig. 3.3**, which also shows the corresponding lossless linear equivalent circuit. Since the primary- and secondary-side self inductances are symmetric, i.e., $L_\mathrm{p} \approx L_\mathrm{s}$, so are the two leakage inductances, i.e., $L_{\sigma 1} \approx L_{\sigma 2}$.

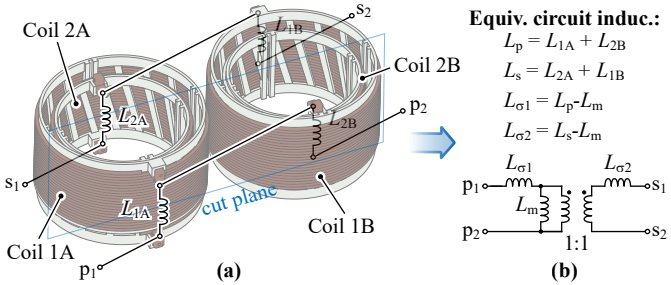


Fig. 3.3: (a) CAD rendering showing the selected coil arrangement with coil interconnections according to **Fig. 3.2(c)**: the series connection of L_{1A} and L_{2B} forms the primary-side self inductance, L_p, and the same applies for the secondary side. **(b)** Lossless linear equivalent circuit of the ACT. Overall, the primary- and secondary-side windings are symmetrical, thanks to the implemented interconnections between the coil sets A & B.

Note that a turns ratio of $n = 2:1$ could be realized by simply connecting the two coils of the secondary winding in parallel, i.e., employing an ISOP configuration of the transformer windings. To ensure equal current sharing among the two parallel-connected secondary-side coils, they must be geometrically identical, i.e., a configuration according to **Fig. 3.2(b)** must be used. A further evaluation of such configuration is beyond the scope of this thesis.

3.2.3 Shielding Configurations

As mentioned above, shielding must be provided to limit the values of the magnetic stray flux densities in the proximity of the ACT, whereby magnetic or conductive shielding materials can be considered. Shielding concepts that employ flux-guiding magnetic materials such as ferrite increase the weight of the system significantly [28], see more details in **Appendix B**, which is a consequence of the high density of the material and of the required material thickness to avoid saturation.

Alternatively, conductive shielding materials, e.g., copper or aluminum, can be considered [29]. The shielding effect is then achieved through a compensating field produced by eddy currents that are induced in the conductive material. As quite thin (e.g., 0.5 mm) aluminum sheet metal provides sufficiently low resistances for these eddy currents to circulate without generating excessive losses, we only consider this approach to realize a lightweight and cost-effective shielding.

3.3 Modeling and Optimization

The selected arrangement and interconnection scheme of the coils define the general geometry of the ACT, see **Fig. 3.3**. However, the actual dimensions (e.g., coil diameters, width and length of the windings), the number of turns, and the operating frequency are free parameters. In the following, we introduce detailed 2-D and 3-D FEM models of the ACT that enable a multi-objective Pareto optimization. The optimal set of parameters can then be selected by taking into account the performance of the overall 1:1-DCX as well.

3.3.1 2-D and 3-D FEM Modeling of the ACT

For a given geometry, 2-D and 3-D FEM simulations of the electromagnetic fields are used to parametrize the ACT equivalent circuit from **Fig. 3.3(b)**, without considering the conductive shielding. Three different levels of detail have been considered in the course of this analysis and **Fig. 3.4** illustrates the corresponding models. The *first model*, depicted in **Fig. 3.4(a)**, is based on 2-D FEM simulations of one of the two coil sets A or B. The component values needed for the equivalent model of the entire ACT, see **Fig. 3.3(b)**, are then determined from the individual values computed for the two coils in the considered set. The *second model* (3-D simple, **Fig. 3.4(b)**) uses 3-D FEM and approximates each coil with a solid hollow cylinder. Finally, the *third model* (3-D detailed, **Fig. 3.4(c)**) considers each turn of the coils individually

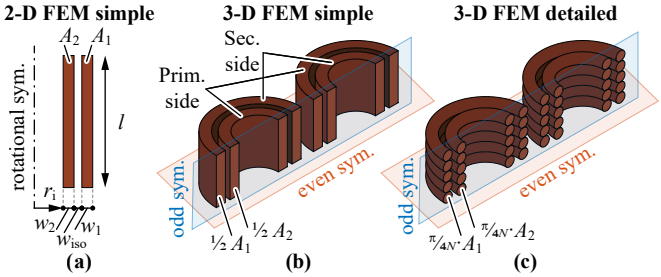


Fig. 3.4: (a) 2-D FEM model for one set of the coils and a simplified winding geometry (rectangular winding cross section). **(b)** 3-D FEM model with a simplified winding geometry and two sets of coils, **(c)** 3-D FEM model with a detailed winding geometry (individual turns with circular cross sections). The shown symmetry planes reduce the complexities of the models.

Tab. 3.1: Comparison of selected results obtained with different modeling methods: 2-D FEM, 3-D FEM simple and 3-D FEM detailed. Self inductances, coupling factors, and winding losses are normalized to that obtained with 3-D FEM detailed.

Param.	Sim. 2-D	Sim. 3-D simple	Sim. 3-D detailed
$L_{p,s}$ (%)	94.9	98.7	100.0
k (%)	98.6	101.4	100.0
Losses (%)	103.4	97.1	100.0
Comp. time (s)	3	34	776

with a circular cross section and thus achieves highest accuracy. The FEM simulations utilize all available symmetry planes to reduce the computational effort, however, in case of 3-D FEM, only quarter symmetries exist, due to the coil sets' interconnections described above and shown in **Fig. 3.3(c)**.

Tab. 3.1 shows a comparison of the accuracies (with respect to the 3-D FEM detailed simulation) and the required computing demands of the presented methods. For the benchmarking, we use a mid-range laptop (Intel Core i7-7600U with 20 GB RAM). The approach with 2-D FEM is best suited for the optimization runs, since it features lowest computational demands and sufficient accuracy (the deviations are in the range of 5 %, since the approach slightly underestimates the coupling factor due to the independent consideration of the two coil sets). Moreover, the simple 3-D FEM simulation provides a very good matching (deviation below 3 %) and is thus used to verify the finally selected design of the ACT.

3.3.2 3-D FEM Modeling of the Conductive Shielding

The losses in the conductive shielding are computed with 3-D FEM simulations. The model considers aluminum sheets forming a fully closed box around the ACT. The 3-D model takes a third symmetry plane between the coil sets into account to reduce the computational effort. This implies that the model considers the series connections of the coils 2A and 2B on the primary side and of coils 1A and 1B on the secondary side, i.e., there is no cancellation effect of magnetic stray fluxes (see **Fig. 3.2(a)**). Accordingly, this is a conservative approach that computes increased losses in the shielding (compared to the real setup).

Adding the considered conductive shielding enclosure has minimal effect on the losses in the windings and on the coupling between the primary-

and the secondary-side winding (deviation below 1.5 %), i.e., the design of the conductive shielding can be decoupled from the design of the ACT's active part. Therefore, we do not include the modeling of the shielding in the multi-objective optimization; instead, the conductive shielding can be designed afterwards, which opens the possibility for advanced designs that do not require a full enclosure, thus reducing material usage and improving accessibility. **Section 3.4.3** describes these considerations in detail.

3.3.3 Multi-Objective Optimization of the ACT

The multi-objective optimization of the ACT maps the design space given in **Tab. 3.2** to a η-γ-ρ-performance space (efficiency, gravimetric power density, and volumetric power density). Note that the minimum distance between the primary- and the secondary-side windings is fixed to $w_{\mathrm{iso}} = 16.5\,\mathrm{mm}$, which follows from the rated insulation voltage of $V_{\mathrm{i}} = 10\,\mathrm{kV}$ and a (conservative, to account for inhomogeneous field distributions, humidity, etc.) maximum permissible electric field of 0.6 kV/mm in air. Note that **Section 3.4.1** discusses the realization of extended clearance and creepage distances in the actual prototype according to standards by means of added insulation barriers. This, again, can be decoupled from the optimization of the ACT's active part.

During the optimization, which follows [28], a sweep over the following geometrical parameters is carried out, cf. **Fig. 3.4(a)**:

- internal diameter of the inner coil (r_{i}),
- widths of outer and inner coils ($w_{1,2}$),
- length of coil (l).

For each geometry (60750 in total), the inductances and the coupling are extracted using the 2-D FEM model. Then, considering each geometry, the number of turns (N) and the operating frequency (f_{s}) are varied, and for each of these designs, a model of the entire 1:1-DCX is evaluated to obtain the winding currents, whereby appropriate resonant capacitor values to compensate the calculated leakage inductances must be considered, i.e.,

$$C_{\mathrm{r1}} = \frac{1}{(2\pi f_{\mathrm{s}})^2 L_{\sigma 1}}, \qquad C_{\mathrm{r2}} = \frac{1}{(2\pi f_{\mathrm{s}})^2 L_{\sigma 2}}, \tag{3.1}$$

which is in contrast to typical IPT systems, where the respective self inductances are compensated because of the variation of the coupling in case of

Tab. 3.2: Design space and constant parameters for the 2-D FEM-based optimization.

Var.	Min.	Max.	# Pts.	Description
f_s	20 kHz	200 kHz	15	operating frequency
N	1	200	200	number of turns
r_i	35 mm	105 mm	15	internal radius
w_1	5 mm	60 mm	15	width of outer coil
w_2	5 mm	60 mm	15	width of inner coil
l	60 mm	700 mm	18	length of coil
Constant parameters				
w_{iso}	16.5 mm			insulation distance
d_{litz}	71 µm			litz strand diameter
k_{litz}	39.5 %			total fill factor of the windings
k_{loss}	30 %			loss penalty due to imperfect twisting

misalignment [55]. With the winding current waveforms known, the calculation of the ACT losses takes high-frequency effects in the litz wire according to [56, 57] into account, whereby the dimensions of the litz wire for a given design follow from the width of the windings, the number of turns, and the (fixed) strand diameter (d_{litz} = 71 µm and fill factor, k_{litz} = 39.5 %). Moreover, the calculated losses are increased by 30 % (loss penalty factor k_{loss}) to account for additional losses due to imperfect twisting of litz wires, based on [57, 58]. Transformer designs that exceed a current density of $J_{max} = 20\,A/mm^2$ or a surface-related loss density of $p_{v,max} = 0.25\,W/cm^2$ are discarded in order to exclude thermally unfeasible designs. The optimization does not consider the weights and volumes of fans, cable terminations, and, as discussed above, the shielding.

Figs. 3.5(a), **(b)** show the results of the multi-objective optimization of the ACT. The maximum achievable values of the ACT's efficiency (η), the gravimetric power density (γ), and the volumetric power density (ρ) increase if the operating frequency increases. However, a separately conducted overall optimization of the 1:1-DCX, which includes the losses of the SiC MOSFETs, cf. [28], reveals a strong impact of the semiconductor switching losses at high operating frequencies (as experimentally shown in [39], the considered 10 kV SiC MOSFETS show clearly non-negligible soft-switching losses). According to the obtained results, the operating frequency must remain below 100 kHz

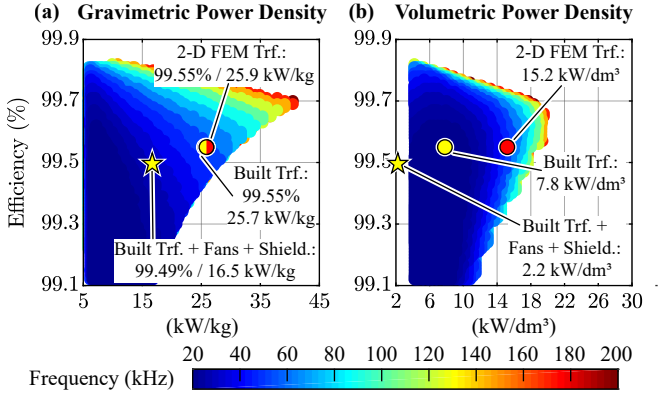


Fig. 3.5: Results of the multi-objective optimization of the 166 kW / 7 kV ACT, revealing the characteristic dependencies of the η-γ- and η-ρ-Pareto fronts on the operating frequency. The markers highlight the results obtained for the selected design (f_s = 77.4 kHz): ● refers to the result obtained with 2-D FEM; ☆ and ○ represent measured characteristics of the realized prototype with and without the weights and volumes of fans and aluminum conductive shielding, respectively. **(a)** Results for gravimetric power density, γ, versus efficiency; **(b)** results for volumetric power density, ρ, versus efficiency. Note that **Section 3.5.8** provides a detailed comparison of the highlighted design and prototype results.

to achieve a system-level efficiency higher than 99.0 %. This constraint together with the availability of only discrete capacitance values of high-power resonant capacitors led us to the selection of a design with an operating frequency of f_s = 77.4 kHz, which is highlighted with ● in **Fig. 3.5**.

In addition to the operating frequency, the selected design defines the geometry of the ACT's active part as well as the number of turns and the dimensions of the litz wire. These values are summarized in the first two sections of **Tab. 3.4**. The following **Section 3.4** discusses the actual hardware realization of this ACT design in detail.

Note that **Fig. 3.5** already shows the actually built prototype's characteristic in the performance space for comparison purposes. However, please refer to **Section 3.5.8** for a detailed comparison between model-based optimization results and measured characteristics of the hardware prototype.

3.4 Design and Construction

With the geometry of the ACT's active part identified from the Pareto optimization described in the previous section, certain additional considerations impact the actual mechanical design of the protoype, i.e., the insulation coordination, cooling and airflow, and the practical realization of a suitable conductive shielding. Regarding the overall mechanical arrangement, **Fig. 3.6(a)** shows how the single-layer winding of each coil is placed on an individual 3-D-printed polycarbonate coil former to facilitate the manufacturing.

3.4.1 Insulation Coordination

For the optimization, a fixed insulation distance ($w_{\mathrm{iso}} = 16.5\,\mathrm{mm}$) between the primary- and the secondary-side windings has been considered, which ensures safe electrical fields in the air gap between the coils. However, by blocking this direct air gap by placing a cylindrical barrier of insulation material (see **Fig. 3.6)**, the effective clearance and creepage distances can be tailored to meet requirements defined in corresponding standards.

We consider a rated DC insulation voltage of $V_{\mathrm{i}} = 10\,\mathrm{kV}$, i.e., with some reserves over the strict functional requirement of the 7 kV DC bus voltage, and design clearance and creepage distances according to IEC 62477 [59, 60]. The minimum required clearance distance for overvoltage category III (OV-III), which demands an impulse withstand voltage of 37 kV, thus becomes 55 mm. Similarly, the minimum required creepage distance, considering pollution degree 2 (PD2) and insulation material group II, is 71 mm.

In order to realize these clearance and creepage distances, cylindrical barrier elements made of NOMEX pressboards with a thickness of 1.5 mm are placed between the primary- and secondary-side coils and a rectangular NOMEX plate (thickness of 1.5 mm) is used between the two sets of coils, cf. **Fig. 3.6(c)**. Both, clearance (66 mm, i.e., corresponding to an impulse withstand voltage of about 43 kV) and creepage (79 mm) distances could be made larger than the minimum values without compromising other aspects of the mechanical design.

Note that for high-altitude applications (higher than 2 km above sea level), larger clearance distances are requested by the standard because of the lower air pressure. E.g., the A1 category for airborne equipment according to the DO160 G standard [61] requires operation in environmentally protected (pressurized) zones up to an altitude of 4.6 km (15, 000 fts), which would require an increase of the clearance distances by a factor of 1.4 according to IEC 62477. In contrast to typical MCTs, the clearance (and creepage) distances of the pro-

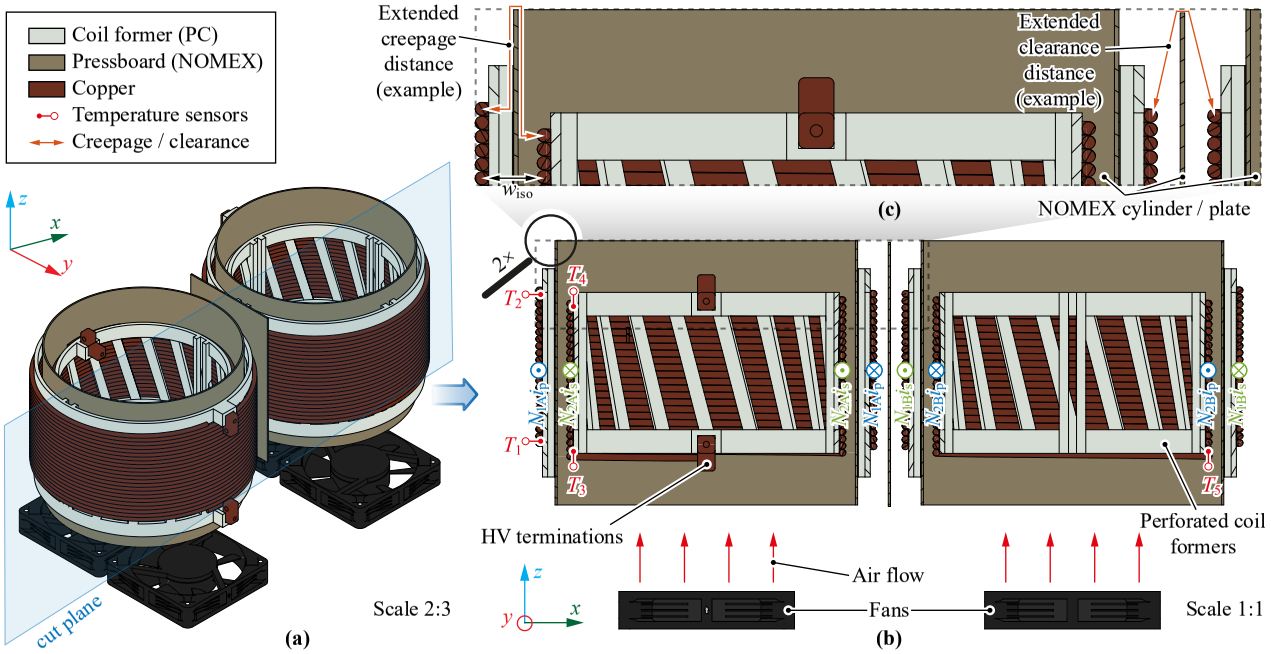


Fig. 3.6: (a) Simplified view of the transformer 3-D model showing windings, terminations, coil formers, insulation barriers, and fans. **(b)** Cut view of the transformer including the flow directions of the currents in the windings, the locations of the temperature sensors, and the direction of the airflow. **(c)** Magnified partial view of the outline of the cross section of the employed insulation concept: required clearance and creepage distances are obtained by placing NOMEX cylinders between coaxial coils and a plate between two sets of coils.

posed ACT can be easily extended to meet such requirements by increasing the length of the NOMEX barrier elements. This is supported by the conservative dimensioning of the maximum electric field between the primary-side and secondary-side coils (see **Section 3.3.3**).

For the peak voltage applied to a winding of the transformer, which is the difference of the voltage applied by a half-bridge ($v_{p,s}$) and the voltage of the corresponding resonant capacitor ($v_{Cr1,Cr2}$), the maximum voltage between two adjacent turns of a coil is only about $5.4\,\mathrm{kV}/44 \approx 123\,\mathrm{V}$, which is well below the capability of the litz wire's insulation, i.e., a double layer of polyamide. The ends of the coils are soldered to copper block terminations which are edgeless (i.e., feature rounded edges) to prevent excessive local electric fields in the surrounding air.

3.4.2 Cooling and Airflow

To improve the thermal design of the windings, the walls of the coil formers are perforated (similar to a squirrel cage rotor), in order to increase the winding's surface that is directly exposed to the airflow (see **Fig. 3.6(b)**). The fans are placed below the transformer. Thus, the airflows due to forced cooling and natural convection have the same direction, which opens the possibility of passive cooling at light load.

3.4.3 Optimized Conductive Shielding

As discussed earlier, the presence of a conductive shielding enclosure does not affect the ACT's coupling or winding losses. Therefore, the shielding can be designed in a second step, whereby the mass (and hence the volume) of the enclosure is minimzed conditional on sufficient distance from the coils and the required interconnections, considering clearance/creepage distances, and low losses ($< 10\,\%$ of the total losses). This is an iterative process aided by the 3-D FEM simulations described in **Section 3.3.2**.

However, whereas the FEM-based design considers a fully closed box, this would limit the accessibility of the coils. Thus, to facilitate access to the windings and simplify experimental testing, we realize a partial shielding, which is composed of a bottom part and a top part only (i.e., the walls on the sides are omitted), instead of a full enclosure. **Fig. 3.7** shows one part of the designed shielding and **Tab. 3.3** lists the corresponding dimensions. FEM simulations shown in **Fig. 3.8** reveal that the top and bottom of the ACT are critical regarding external stray fields (see **Fig. 3.8(a)**), and that the selected

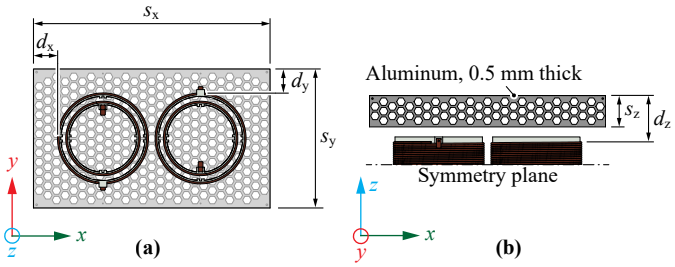


Fig. 3.7: Simplified 3-D CAD model of the transformer, showing windings, coil formers, terminations, and conductive aluminum shielding featuring a honeycomb pattern of holes: **(a)** top view, **(b)** side view. Projections are in scale and main mechanical dimensions are shown.

Tab. 3.3: Specifications of the conductive aluminum shielding.

Dimensions of shielding		
d_x	60.5 mm	distance from coils in x-axis
d_y	60.5 mm	distance from coils in y-axis
d_z	126.0 mm	distance from coils in z-axis
s_x	601 mm	width of shielding
s_y	353 mm	depth of shielding
s_z	80 mm	height of shielding
t_{sh}	0.5 mm	thickness of shielding

partial shielding provides the required shielding efficacy in these locations (see **Fig. 3.8(b)**). In addition, **Fig. 3.8(c)** indicates that a full enclosure further improves the shielding effect. Therefore, measuring the external stray fields of a prototype with partial shielding (see **Section 3.5.7**) is a conservative approach, which further confirms its suitability for testing purposes. Also, the partial shielding configuration is conservative with regard to losses, since it overestimates the total losses in the shielding by a factor of 1.8 compared to a complete enclosure. The increased losses in the partial shielding can be explained by a crowding of the eddy currents close to the edges (i.e., especially on the sides where the partial shielding ends, and where a full enclosure would provide additional area for the eddy currents to flow), thus leading to areas with a high local current density and hence losses.

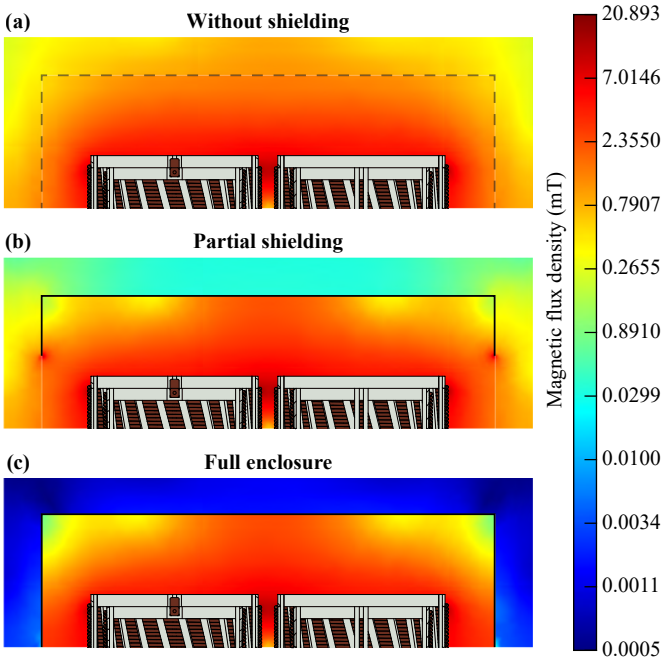


Fig. 3.8: FEM-simulated flux densities with nominal primary- and secondary-side currents (cf. cut plane defined in **Fig. 3.3**): **(a)** ACT without shielding; **(b)** partial shielding as employed in the prototype to facilitate access to the windings; **(c)** full enclosure. The shielding is modeled without honeycomb pattern. Note the logarithmic color scale.

Furthermore, a full enclosure made of solid sheet-metal would complicate forced-air cooling. Thus, we perforate the shield in a honeycomb pattern (cf. **Fig. 3.7**), achieving also a reduction of the weight of the shielding by 30 %. With this, the shielding efficacy remains sufficiently high, however, the losses in the shielding increase by 29 % (compared to non-perforated shielding); essentially because similar shielding efficacy implies similar circulating eddy currents, which generate higher losses because of the reduced cross-sectional area.

3.4.4 Resulting Prototype

Fig. 3.9 depicts the realized MV/MF ACT of the 1:1-DCX and **Tab. 3.4** summarizes its dimensions and key design parameters. Acrylic glass plates with slots are inserted from the top and the bottom of the coils (along the z-axis, cf. **Fig. 3.9(a)**), to fix the positions of all components, including the fans and the partial top- and bottom-side shielding. In the following section we describe the experimental methodology and provide detailed measurement results to characterize the prototype's performance.

3.5 Experimental Setup and Results

This section summarizes the experimental characterization of the ACT prototype shown in **Fig. 3.9**, including a variety of measurements, e.g., small-signal impedance measurements, large-signal tests, loss measurements, transient thermal responses, magnetic stray flux densities (without and with shielding), and insulation tests. The results provide further validation of the employed models described in **Section 3.3**.

As a preliminary remark, note that several measurement approaches make use of an important property of an ACT: its linearity. As there is no core material, there are no saturation phenomena, i.e., the ACT's key properties such as coupling, inductances, and AC resistances do not directly depend on current and voltages (not considering thermal effects).

Note that the ACT is placed on a wooden table (i.e., without metal legs) and the used measurement equipment (i.e., its active parts) is placed at sufficient distance ($> 1\,\mathrm{m}$) to prevent interactions of the ACT's fields with nearby metal parts.

3.5.1 Impedance Measurements

To validate the computed values of $L_{\sigma 1,2}$ and L_m from the equivalent circuit of **Fig. 3.3,** the short-circuit and open-circuit impedances are measured with an Agilent 4924A precision impedance analyzer from the primary and from the secondary side (without the shielding present). Moreover, the common-mode (CM) impedance across the galvanic insulation is measured between the shorted primary-side winding and the shorted secondary-side winding. **Fig. 3.10** shows the obtained results and **Tab. 3.5** compares the simulated and the measured values of the equivalent circuit parameters (at a frequency of 77.4 kHz). All deviations between measurements and simulations are below 16 %. The CM capacitance is relatively low and equal to 102 pF. Furthermore,

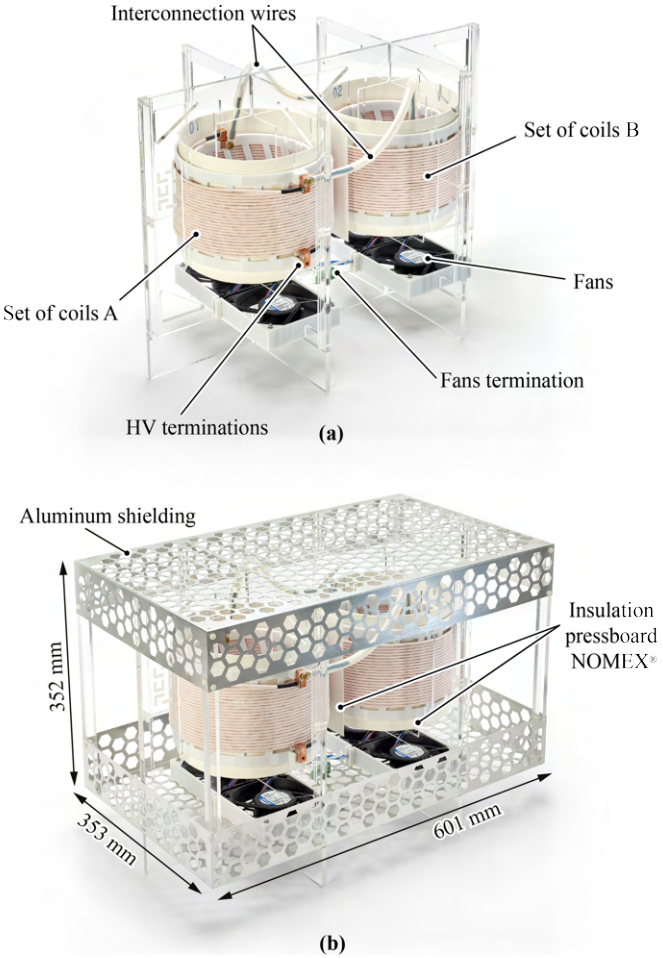


Fig. 3.9: Photo of the realized 166 kW / 7 kV air-core transformer (ACT): **(a)** without shielding, **(b)** with aluminum conductive shielding.

Tab. 3.4: Key characteristics of the realized 166 kW / 7 kV air-core transformer (ACT) prototype and the resonant capacitor bank.

Air-Core Transformer		
r_i	90 mm	internal radius, cf. Fig. 3.4(a)
w_1	4.5 mm	width of outer winding
w_2	4.5 mm	width of inner winding
l	98.6 mm	length of coil
Winding		
N	2×22	number of turns (single layer)
Litz wire	$5 \times 10 \times 40$	strands in 3 bundle levels (total of 2000 strands)
Litz wire	double layer polyamide	outer insulation of litz wire
d_litz	71 µm	single strand diameter
n_litz	2000	number of strands
J_litz	7.2 A/mm^2	current density
Equivalent circuit parameters		
$L_{\sigma 1,2}$	51.8 µH	primary / secondary leakage inductance
L_m	162.6 µH	magnetizing inductance
n	1 : 1	transformer turns ratio
k	0.76	coupling factor
$I_\mathrm{p,s}$	56.6 A	primary / secondary transformer rms current
I_m	40.0 A	magnetizing rms current
Insulation		
V_i	10 kV	DC insulation voltage
d_clear	66 mm	clearance distance
d_creep	79 mm	creepage distance
Resonant capacitor bank		
f_s	77.4 kHz	operating frequency
$C_{\mathrm{r}1,2}$	81.6 nF	input / output side resonance capacitance

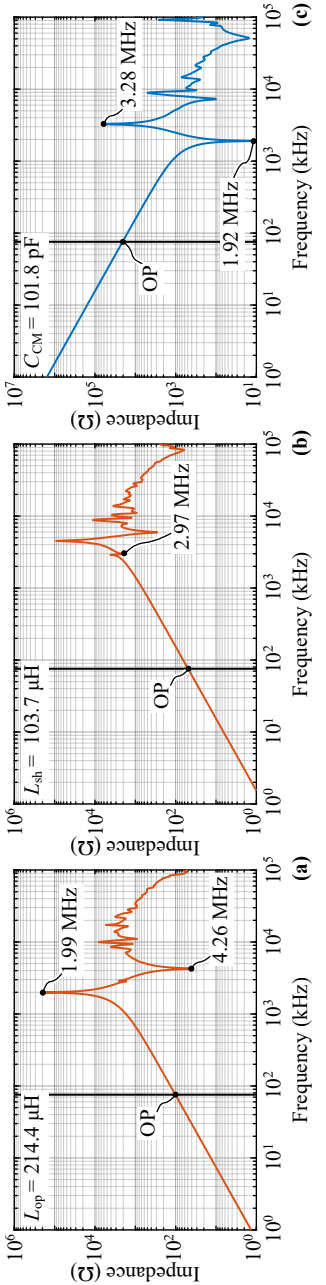


Fig. 3.10: Measured frequency characteristics of selected impedances of the transformer (without shielding): **(a)** primary-side impedance for open secondary-side winding; **(b)** primary-side impedance in case of a secondary-side short-circuit; **(c)** CM impedance between shorted primary-side and shorted secondary-side windings. The impedance values corresponding to the operating frequency (77.4 kHz) are marked with a black dot (operating point, OP). Additionally, different resonance frequencies are labeled.

Tab. 3.5: Small-signal parameters of the ACT (without shielding, determined at $f = 77.4\,\mathrm{kHz}$).

Param.	Sim. 2-D	Sim. 3-D	Meas.	Dev. 2–D \ 3-D
$L_{1,2}$	204.5 µH	214.2 µH	214.4 µH	4.6 % \ 0.1 %
L_m	144.4 µH	155.9 µH	162.6 µH	11.2 % \ 4.2 %
$L_{\sigma 1,2}$	60.1 µH	58.4 µH	51.8 µH	16.0 % \ 12.6 %
k	0.706	0.728	0.758	7.4 % \ 3.8 %

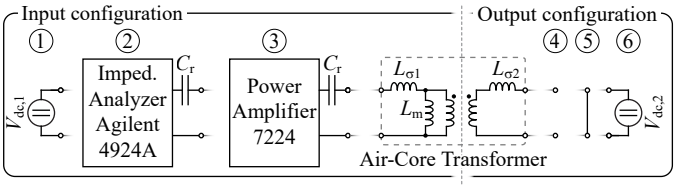


Fig. 3.11: Input devices and output configurations of the different measurement circuits. ① DC source for thermal calibration, ② impedance analyzer with series resonant capacitor for small-signal measurements of AC resistances, ③ power amplifier with series resonant capacitor for large-signal measurements. Depending on the measurement, either an open-circuit ④ or a short-circuit ⑤ is realized at the secondary side. The last configuration, with a secondary-side DC source ⑥, is used for the thermal calibration only.

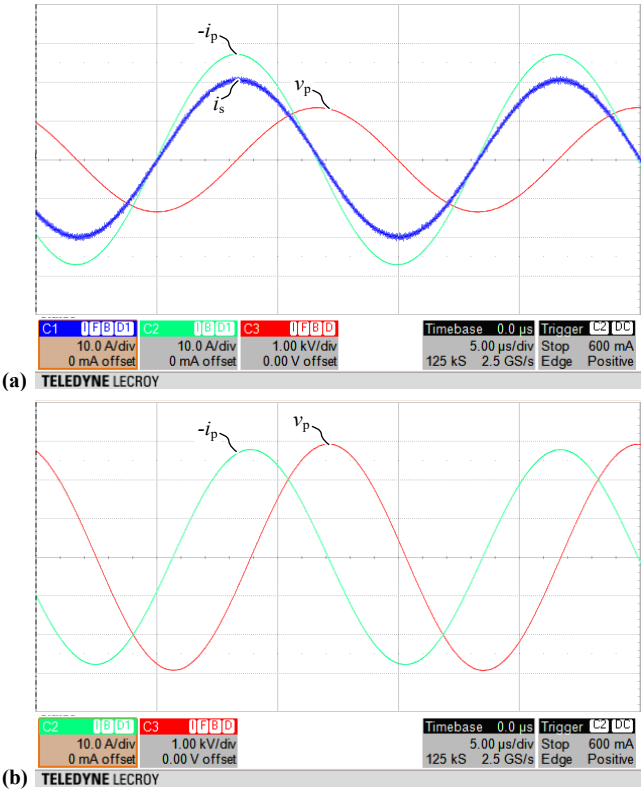


Fig. 3.12: Voltage and current waveforms measured in the course of the large-signal tests that utilize series resonant operation. **(a)** Secondary-side short-circuit (rms values): primary-side current is 19.6 A, primary-side voltage is 0.93 kV, secondary-side current is 14.6 A, and resonance frequency is 75.3 kHz. **(b)** Secondary-side open-circuit (rms values): primary-side current is 19.9 A, primary-side voltage is 2.04 kV, and resonance frequency is 78.0 kHz.

all resonance frequencies are much higher than the operating frequency and are found to be uncritical with regard to the operation of the 1:1-DCX [62].

3.5.2 Large-Signal Tests

Large-signal tests of the ACT could be conducted in the course of an experimental test of the entire 1:1-DCX, cf. **Fig. 2.2(a)**, which, however, requires two

fully operational MV/MF half-bridges. Each of the half-bridges needs to process the rated power of 166 kW and allow for operation with $f_s = 77.4$ kHz. To circumvent the costs and uncertainties related to the realization and operation of such 10 kV half-bridge converters, an alternative approach is pursued in this thesis. Since the currents in the ACT of the 1:1-DCX are quasi-sinusoidal (cf. **Fig. 2.2b**), the ACT can be operated in a series resonant circuit that is supplied by a power amplifier, instead. This effectively emulates power operation. Note that since the ACT is not subject to core losses and is a linear device, large-signal validation can be done with scaled voltages/currents, i.e., operation at rated current is not necessary. **Fig. 3.11** gives an overview of the different input and output configurations used to assess the ACT. With regard to the large-signal test at scaled current, the input configuration ③ is used, i.e., an AE Techron 7224 power amplifier with a capacitor connected in series. This resonant capacitor C_r is realized as a high-power polypropylene capacitor bank (CELEM CSP120/200) and the series resonance frequency is set to approx. f_s. The transformer currents are measured with a Pearson 110A current probe and a LeCroy HDO4054A 12-bit oscilloscope. The current measurement is subject to a total uncertainty of +2 % / −1 %.

Fig. 3.12(a) shows the result of the test with a secondary-side short-circuit (output configuration ⑤), which reveals a secondary-side rms current of 14.6 A for a primary-side rms current of 19.6 A. This result agrees well with the expected secondary-side current of 14.8 A (for $k = 0.76$ as obtained from the impedance analyzer measurements described above, cf. **Tab. 3.5**).

The same setup can be used to assess the self inductance of the ACT; in this case, the secondary-side winding is left open (output configuration ④). **Fig. 3.12(b)** presents the measurement results, with a primary-side rms voltage of 2.04 kV, a primary-side rms current of 19.9 A, and a phase shift of 90°. This corresponds to a self inductance of 209 µH, which corroborates the impedance analyzer measurement, see **Tab. 3.5**.

The close agreement of the coupling and inductances values measured with an impedance analyzer (i.e., small-signal) and with a power-amplifier-based setup (i.e., large-signal) confirms that the ACT is a linear system.

3.5.3 AC Resistances of the Windings

The measurement of the coils' AC resistances is a challenging task, due to their high quality factors ($Q \geq 1000$), which complicates electrical measurements, and because of the large volume of the ACT (75 dm^3) that renders steady-state calorimetric approaches impractical.

Tab. 3.6: Comparison of FEM-simulated AC resistances with measurement results obtained with an impedance analyzer with a series resonant compensation, cf. input configuration ② in **Fig. 3.11**. In the short-circuit case, R_{AC} is the sum of *both* winding's AC resistances, referred to the primary side. Note that the operating frequencies do not exactly match the nominal value because only discrete capacitance values are available to realize the series compensation capacitor.

Param.	Sim. 3-D	Measurement	
		w/o Shield.	w/ Shield.
Open-circuit		**@ 79.0 kHz**	**@ 80.5 kHz**
R_{AC}	72.4 mΩ	116.3 mΩ (dev. 60.6 %)	182.9 mΩ
Short-circuit		**@ 79.0 kHz**	**@ 79.8 kHz**
R_{AC}	114.3 mΩ	172.0 mΩ (dev. 50.5 %)	192.9 mΩ

Impedance analyzer

However, as the ACT is a linear system, a direct measurement of the AC resistances with an impedance analyzer is possible, at least in theory. Unfortunately, the high reactive component of the coil's impedance leads to a very inaccurate measurement of the resistive component, which renders the result of the direct measurement unusable. In order to avoid its unwanted impact, the reactance of the tested coil can be compensated at the measurement frequency. For this purpose, a high quality capacitor with very low losses is connected in series (input configuration ② in **Fig. 3.11**; MLCC COG *Knowles High Q* capacitors have been used for C_r). Still, the measured primary-side AC resistances for secondary-side open- and short-circuits are 60.6 % and 50.5 % higher than the resistances computed with the corresponding 3-D FEM simulations, respectively, cf. **Tab. 3.6** (without considering a loss-correction factor k_{loss}, cf. **Tab. 3.2**, to account for imperfect twisting observed in practical litz wires, see **Sec. 3.5.4** below). This indicates a significant impact of the capacitor's equivalent series resistance on the total resistance and limits the measurement method to applications where a *change* of the resistance is assessed, e.g., when evaluating the AC resistances without and with the shielding present to determine the losses in the shielding, see **Section 3.5.7**.

Transient calorimetric

Alternatively, a transient calorimetric method can be used to measure the AC resistance, which is a two-step procedure that relies on measuring the winding temperatures over time. To do so, two types of sensors are placed between the

first two turns and the last two turns of the coils at the five positions marked with $T_{\{1,2,3,4,5\}}$ in **Fig. 3.6(b)**. NTC sensors (PS104J2 thermistor) are used during thermal tests with DC currents; however, due to the lack of isolation, only one NTC sensor, T_1, can be used during AC tests because of the significantly higher voltage levels. Thus, fiber optic sensors (FOTEMPMK-19 Modular) are used to measure $T_{\{1,2,3,4,5\}}$ during AC tests.

Firstly, DC currents are injected into the windings in order to determine the step responses of all measured temperatures for given losses in the windings (in the range of 10 W to 40 W). In this context, one DC source is used if a secondary-side open-circuit is assessed (input configuration ① in **Fig. 3.11**) and two DC sources if a secondary-side short-circuit is evaluated (input and output configurations ① and ⑥ in **Fig. 3.11**, respectively). **Fig. 3.13(a)** presents example step responses of the temperature sensor T_1 (cf. **Fig. 3.6(b)**) for four different values of power being dissipated in the primary-side coils. In this measurement, the secondary side of the ACT has been left open. The obtained step responses enable the compilation of a loss-vs.-temperature characteristic for each temperature sensor, which relates the losses to a measured temperature increase after a defined time, Δt. **Fig. 3.13(b)** depicts the loss curve that results for the transient temperature waveforms of **Fig. 3.13(a)**, i.e., for temperature sensor T_1 and a secondary-side open-circuit, and $\Delta t = 600$ s.

Subsequently to this initial calibration, the ACT is operated in AC resonance (using a power amplifier and series compensation capacitor, see **Section 3.5.2**) with a defined primary-side current, I_{meas}. After the time interval Δt has elapsed (cf. **Fig. 3.13(c)**), the temperature increase measured by each temperature sensor together with the corresponding calibration data for that sensor allows to determine the winding losses (cf. **Fig. 3.13(b)**). Finally, the AC resistance is calculated as $R_{\mathrm{AC}} = P_{\mathrm{meas}}/I_{\mathrm{meas}}^2$. The uncertainties of the temperature measurements with the high-precision NTC sensors and the fiber optic sensors are $\pm 0.1\,^{\circ}\mathrm{C}$ and $\pm 0.2\,^{\circ}\mathrm{C}$, respectively, which corresponds to loss deviations of ± 0.4 W and ± 0.8 W and resistance deviations of $\pm 2\,\mathrm{m\Omega}$ and $\pm 4\,\mathrm{m\Omega}$, respectively (for a measurement current of 14 A). The maximum uncertainty of the current measurement is $+2\,\%/-1\,\%$, cf. **Section 3.5.2**, which corresponds to an additional uncertainty of the measured R_{AC} of $+2\,\%/-4\,\%$, e.g., $+2\,\mathrm{m\Omega}/-4\,\mathrm{m\Omega}$ for a typical $P_{\mathrm{meas}} = 20$ W and a measurement current of 14 A (corresponding to an R_{AC} of about $100\,\mathrm{m\Omega}$).

Tab. 3.7 lists the results of the conducted measurements. The final AC resistances are calculated by averaging the values obtained from different temperature sensors and are listed in **Tab. 3.8** together with the results of corresponding FEM simulations. Note that the transient calorimetric method enables individual measurements of the AC resistances of the primary and

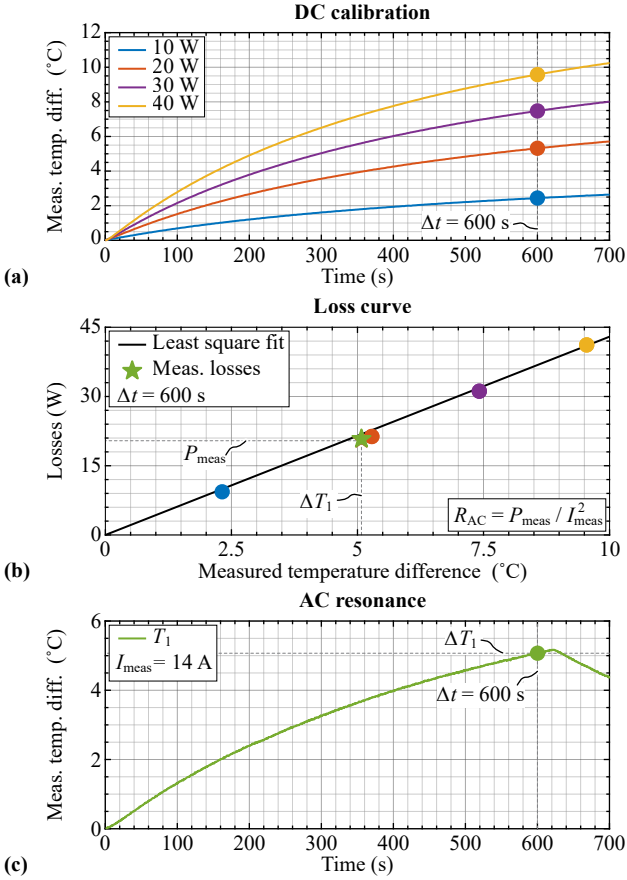


Fig. 3.13: Transient calorimetric measurement of the AC resistance—exemplary illustration of the processing of the measured step responses of temperature sensor T_1 for a secondary-side open-circuit of the ACT: **(a)** initial measurements of the temperature step responses for defined losses on the primary side, ranging from 10 W to 40 W; **(b)** linear approximation of the dependency of the temperature increase, $\Delta T_1(\Delta t = 600\,\mathrm{s}) = T_1(\Delta t) - T_1(0)$, on the losses; the slope of this function is computed with a least squares optimization; **(c)** final measurement of the step response of T_1 for a primary-side AC rms current of 14 A.

of the secondary-side winding also for a shorted secondary-side winding (in contrast to the small-signal approach discussed earlier). It can be seen

that the transient calorimetric method allows to measure the AC resistance more accurately than the small-signal method (cf. **Tab. 3.6**), however the deviations to the simulated values (25 % to 40 %, without applying the loss-correction factor k_{loss} to the FEM results) are still high. A likely reason for this is imperfect twisting of the litz wire, which is known to cause increased winding losses [57, 58] and is thus investigated in the next section.

Tab. 3.7: Results of the transient calorimetric method for the measured AC resistances.

Sensor	ΔT (°C)	P (W)	I_p (A)	I_s (A)	$R_{AC,1}$ (mΩ)	$R_{AC,2}$ (mΩ)
Open-circuit						
T1 (NTC)	5.0	20.5			104.4	-
T1 (OPT)	5.3	19.5	14.0	-	99.5	-
T2 (OPT)	4.9	20.0			101.9	-
Short-circuit						
T1 (NTC)	4.0	17.2			95.4	-
T1 (OPT)	4.3	17.3			95.9	-
T2 (OPT)	4.0	17.2	13.4	10.2	95.0	-
T3 (OPT)	3.5	16.8			93.2	-
T5 (OPT)	2.9	10.2			-	97.5

NTC - PS104J2 thermistor

OPT - fiber optic thermometer FOTEMPMK-19 Modular

Tab. 3.8: Comparison of FEM-simulated AC resistance values against the results obtained through transient calorimetric measurements. Note that the operating frequencies do not exactly match the nominal value because only discrete capacitance values are available to realize the series compensation capacitor, cf. input configuration ③ in **Fig. 3.11**.

Param.	Sim. 3-D	Meas.	Deviation
Open-circuit @ 80 kHz / 14.0 A			
$R_{AC,1}$	72.4 mΩ	101.9 mΩ	40.8 %
Short-circuit @ 75.3 kHz / 13.4 A			
$R_{AC,1}$	69.5 mΩ	95.4 mΩ	37.3 %
$R_{AC,2}$	77.9 mΩ	97.5 mΩ	25.1 %

3.5.4 Litz Wire Current Sharing

The current sharing in the bundles of the used litz wire is analyzed in order to determine whether the measured increase of the AC resistance above the values expected from simulations may be caused by imperfect twisting. The litz wire used in the transformer consists of 2000 strands with a single-strand diameter of 71 µm. It is twisted in 3 levels: top-level (5 bundles), mid-level (10 subbundles) and strand-level (40 strands), see **Fig. 3.14(a)**. To examine the current sharing, a test coil with an inner diameter of 160 mm and 31 turns (single layer, total length of 51 cm) is wound, i.e., the test coil has similar dimensions as one of the ACT's coils. Its litz wire has been partially untwisted to have access to all bundles and, in addition, one of the subbundles (No. 5) has been untwisted to have access to all of its strand-level bundles. **Figs. 3.14(b), (c)** depict the measured currents flowing in the individual bundles and subbundles, respectively, for a total rms current of 0.6 A at a frequency of 80 kHz. The amplitudes of the currents flowing in the top-level bundles deviate on average by 23.2 % from the ideal values in case of symmetric current sharing, and the phase-shifts are rather small (between -2 ° and 5 °). In bundle No. 5, i.e., on the middle level, the amplitudes deviate on average by 18.4 %, and the phase-shifts are larger, i.e., between -18 ° and 55 °. Thus, the current sharing among bundles, and within a bundle among the subbundles is clearly not symmetric, confirming a non-ideal twisting scheme of the litz wire [58].

To quantitatively assess the impact of this imperfect twisting on the coil's AC resistance, the losses in the investigated test litz wire are compared with losses in a hypothetical, perfectly twisted one. The analysis is based on the assumption that the current sharing in the subbundles of all bundles is the same as measured in bundle No. 5; this is a valid assumption because all top-level bundles are of identical internal structure. The corresponding computation reveals an increase of the AC resistance by 24 %, which explains the largest part of the deviations between the AC resistances obtained from (transient-calorimetric) measurements and FEM simulations (not yet considering the loss penalty factor k_{loss}), cf. **Tab. 3.8**. The remaining deviation may be related to uncertainties of the computed fields, further imperfections of the litz wires, or resistances of terminations. Furthermore, this result justifies the value of the loss penalty factor used in the optimization, $k_{loss} = 30$ %, which had been selected *a priori* based on literature and experience [57, 58].

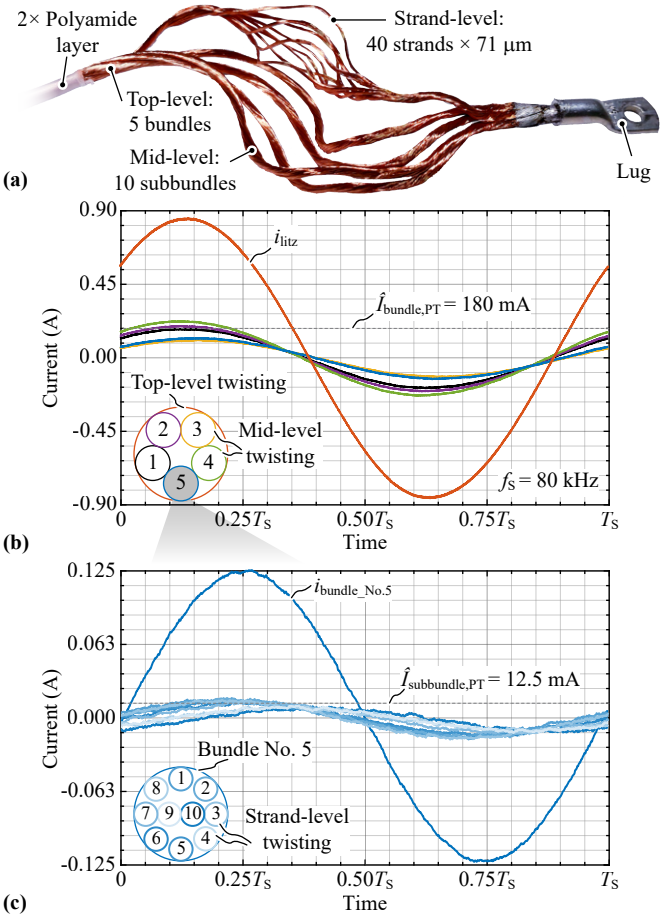


Fig. 3.14: (a) Photo of the litz wire ($5 \times 10 \times 40$ strands with single-strand diameter of 71 µm) being prepared for current sharing measurements. **(b)** Current sharing in the five top-level bundles; **(c)** current sharing in the ten mid-level subbundles of bundle No. 5. The total current in the litz wire, I_{litz}, is 600 mA. For reference, the peak values of the currents in the bundles of a hypothetical, perfectly twisted litz wire are shown on top level ($\hat{I}_{bundle,PT}$) and middle level ($\hat{I}_{subbundle,PT}$).

3.5.5 Thermal Tests

To verify the thermal feasibility of the transformer, heat runs are carried out considering two different operating conditions, i.e., nominal operation with active cooling (4×12 W, 4414FNH fans) and maximum allowable transformer power without overheating in case of passive cooling. We emulate these operating conditions using high DC currents, i.e., we employ a DC source that injects a current into the series connection of the primary- and secondary-side windings of the ACT. The current is selected based on the ratio of AC to DC resistances ($R_{AC}/R_{DC} = 1.48$ @ 30 °C) such that the losses expected for operation with AC currents are generated.

Fig. 3.15 shows the thermal images of the prototype and the evolution of measured temperature waveforms during the heat runs. Note that even though the litz wire features temperature class V155, the maximum allowable temperature is $T_{max} = 130$ °C due to the thermal stability of the outer polyamide insulation [63]. During rated operation, the hotspot reaches 103 °C at an ambient temperature of 25 °C, cf. **Fig. 3.15(a)** and ① in **Fig. 3.15(b)**, which leaves a margin of $\Delta T = 27$ °C to T_{max}, or, alternatively, would allow operation at ambient temperatures of up to about 50 °C.

Furthermore, the transformer can operate with passive cooling (e.g., in case the fans would fail) up to approximately 420 W of losses, cf. **Fig. 3.15(c)** and ② in **Fig. 3.15(b)**. This corresponds to operation at an output power of 117 kW (70 % rated output power).

Finally, the thermal time constants of the ACT with and without fans can be extracted from **Fig. 3.15** as 3.2 min and 5.2 min, respectively, which are several times shorter than for high-power MF MCTs [44, 62].

3.5.6 Insulation and Voltage Withstand Tests

To test the insulation of the transformer, first, the DC insulation resistance between primary and secondary side, i.e., common-mode insulation, is measured with an insulation tester (Megger MIT410, DC test voltage of 1 kV). The measured insulation resistance is greater than 100 GΩ, which corresponds to a leakage current of less than 70 nA for a voltage of 7 kV. This insulation resistance is more than a hundred times higher than the specified values [64, 65]. Additionally, the same insulation has been successfully tested at higher voltages, with a Schleich GLP2 voltage tester (for 1 min each): +9.6 kV (DC), −9.6 kV (DC), and 6.36 kV (rms) at $f = 50$ Hz. In summary, those tests indicate that the realized prototype withstands the rated insulation voltage.

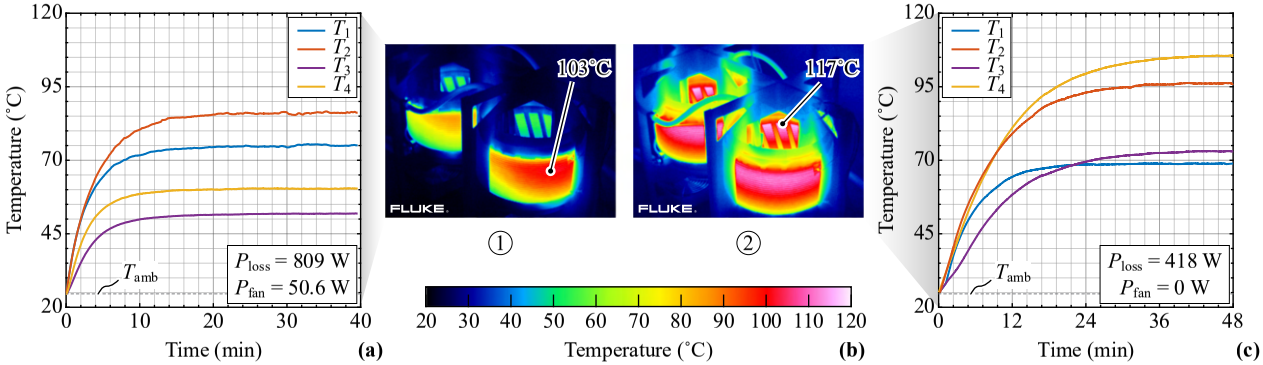


Fig. 3.15: Temperatures measured with four PS104J2 NTC thermistors, $T_{1...4}$, placed in the windings (cf. **Fig. 3.6(b)**), for **(a)** a nominal load step with nominal cooling and for **(c)** a maximum allowable load step ($P_{passive} \cong 0.7 \cdot P_N$) with passive cooling (derating in case of fan failure). **(b)** Corresponding thermal images with labeled hotspots of the ACT during two load step tests: ① nominal operation, ② allowable load with passive cooling.

3.5.7 Magnetic Fields and Shielding

Shielding losses

The losses in the conductive shielding are directly related to the difference of the AC resistances that are measured with and without shielding. Accordingly, the small-signal setup described in **Section 3.5.1** can be used for this purpose. **Tab. 3.6** lists the measurement results and reveals an increase of the AC resistance by 12 % (short-circuit test, i.e., all coils carry current). This corresponds to 92 W of losses in the tested conductive shielding, which covers only the top and bottom parts. Using FEM results to scale this measurement to a full enclosure (made of aluminum sheet metal with a honeycomb pattern of openings) results in 50 W of expected losses, cf. **Section 3.4.3** for an explanation for these lower losses in case of a full enclosure.

Considering the large surface area of the shield A_s and a conservative heat transfer coefficient for natural convection of $h_c = 5\,\mathrm{W/m^2K}$, the shield's temperature rise follows from a simplified calculation as approximately $T_s = 50\,\mathrm{W}/(h_c \cdot A_s) = 13\,\mathrm{K}$. In practice, the heat transfer coefficient would be significantly higher because of the fans (forced convection). Therefore, it can be concluded that the heating of the shielding due to the induced eddy currents is negligible.

Note that the change of the AC resistance for open-circuit tests (60 %) is larger, because there is no current in the secondary-side winding that would have a cancelling effect on the magnetic stray flux outside of the ACT, see **Section 3.2.2**.

Stray fields without shielding

The FEM-based predictions of the magnetic stray flux densities in the vicinity of the ACT and the efficacy of the shielding are experimentally verified using a custom-made magnetic field probe. The implemented field probe measures the induced voltage at the design frequency of 80 kHz and is constructed similarly to the probe presented in [66]. For the measurement of three spatial components of the magnetic flux density vector, three sensor windings are arranged perpendicularly on a 3-D printed spherical support made from polycarbonate, as shown in **Fig. 3.16(a)**; **Fig. 3.16(b)** depicts the dimensions of the spherical support. Each winding consists of 50 turns to achieve a sensitivity of approx. $0.75\,\mathrm{mV/\mu T}$. The output signal of the built field probe has been compared to that of a commercial field probe (MC162 by *Magnetic*

Sciences Inc.), confirming deviations of less than 3 %.[1] The custom-made positioning setup depicted in **Fig. 3.16(c)** enables a precise positioning of the field probe in x-, y-, and z-coordinates. The setup consists of non-conductive materials and uses profiles for changing the probe's position in x-, y-directions. A threaded fiberglass rod holds the probe and allows for a change of the position in z-direction.

In a first step, the magnetic flux densities in the proximity of the ACT (without the shielding) are measured and compared to the results of the 3-D FEM simulations. The ACT is operated in a series resonant circuit (input configuration ③ from **Fig. 3.11**), with a primary-side rms current of $I_{\mathrm{meas}} = 10\,\mathrm{A}$ at a frequency of 80 kHz. The magnetic fields are measured in the following observation planes:

- xy-planes at $d_{\mathrm{z},\{\mathrm{a,b,c}\}} = \{30\,\mathrm{mm},\ 200\,\mathrm{mm},\ 500\,\mathrm{mm}\}$, cf. **Fig. 3.16(c)**;
- xz-planes at cuts A, B, and C, cf. **Fig. 3.16(d)**.

Within cuts A, B, and C, the 11 points marked in **Fig. 3.16(d)** are selected for the measurements. Except for the points 8 to 11, which are not measured for $d_{\mathrm{z}} = d_{\mathrm{z,c}}$ (due to the low fields, there), all points are measured for $d_{\mathrm{z},\{\mathrm{a,b,c}\}}$, which yields a total of $33 - 4 = 29$ measurement points.

Figs. 3.17(a)–(c) present a comparison of simulated (3-D FEM) and measured results, considering an open secondary-side winding. The FEM simulation uses a primary-side rms current of 1 A at a frequency of 80 kHz and thus the measured flux densities, $B_{\mathrm{meas,n}}$, are normalized to 1 A,

$$B_{\mathrm{meas,n}} = B_{\mathrm{meas}} \frac{1\,\mathrm{A}}{I_{\mathrm{meas}}}. \tag{3.2}$$

The average of the absolute value of the relative deviation between the simulated and the measured results is 15.2 % for an open secondary-side winding. As expected, the deviation increases to 26.8 % when considering a short-circuited secondary-side winding (not shown in the figure), which is a consequence of the deviation between the simulated and measured magnetic coupling and hence lower-than-expected secondary-side current for the short-circuit case. However, the open-circuit measurement, which enables a clearly defined current in the primary winding, confirms the high accuracy of the employed 3-D FEM simulation.

[1] The MC162 is a single-axis sensor, has a length of 13 cm, and measures the average of the flux densities along its length. For these reasons, it could not be used for measuring the ACT's stray fields.

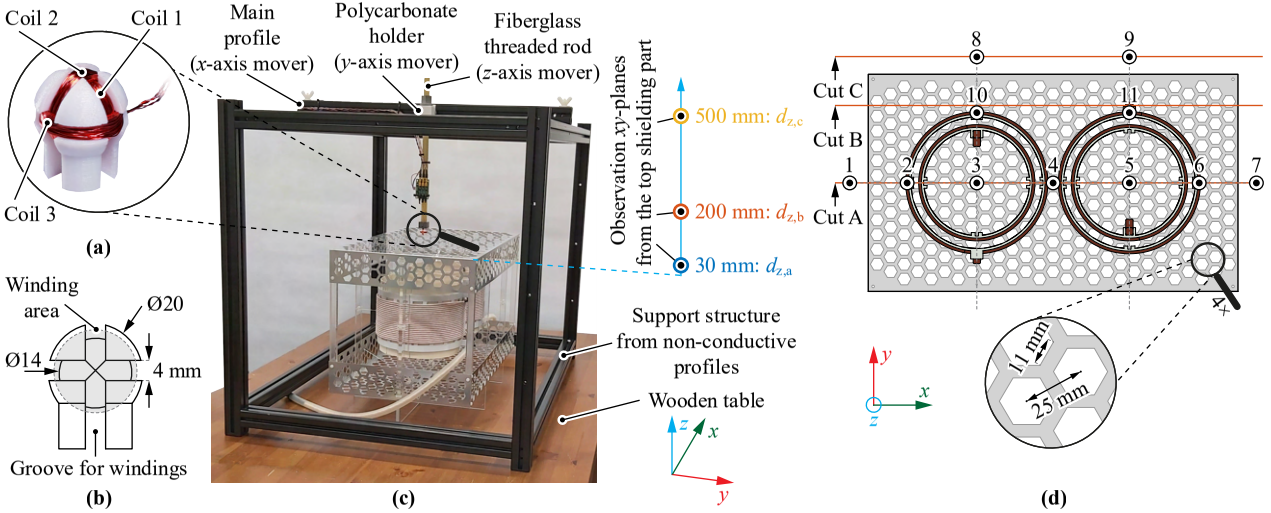


Fig. 3.16: **(a)** Picture and **(b)** CAD drawing of the field probe that is used to measure the magnetic flux density. A 3-D-printed polycarbonate sphere is used to support three coils with 50 turns each. **(c)** Picture of the measurement setup used to achieve a precise positioning (± 1 mm) of the field probe in x-, y-, z-directions. Additionally, the distances in z-direction, $d_z = d_{z,\{a,b,c\}}$, between the top surface of the shielding and the plane containing the observation points for the measurements are shown. **(d)** Top view of the transformer; the points 1 to 11 mark the locations of the observation points in the xy-plane.

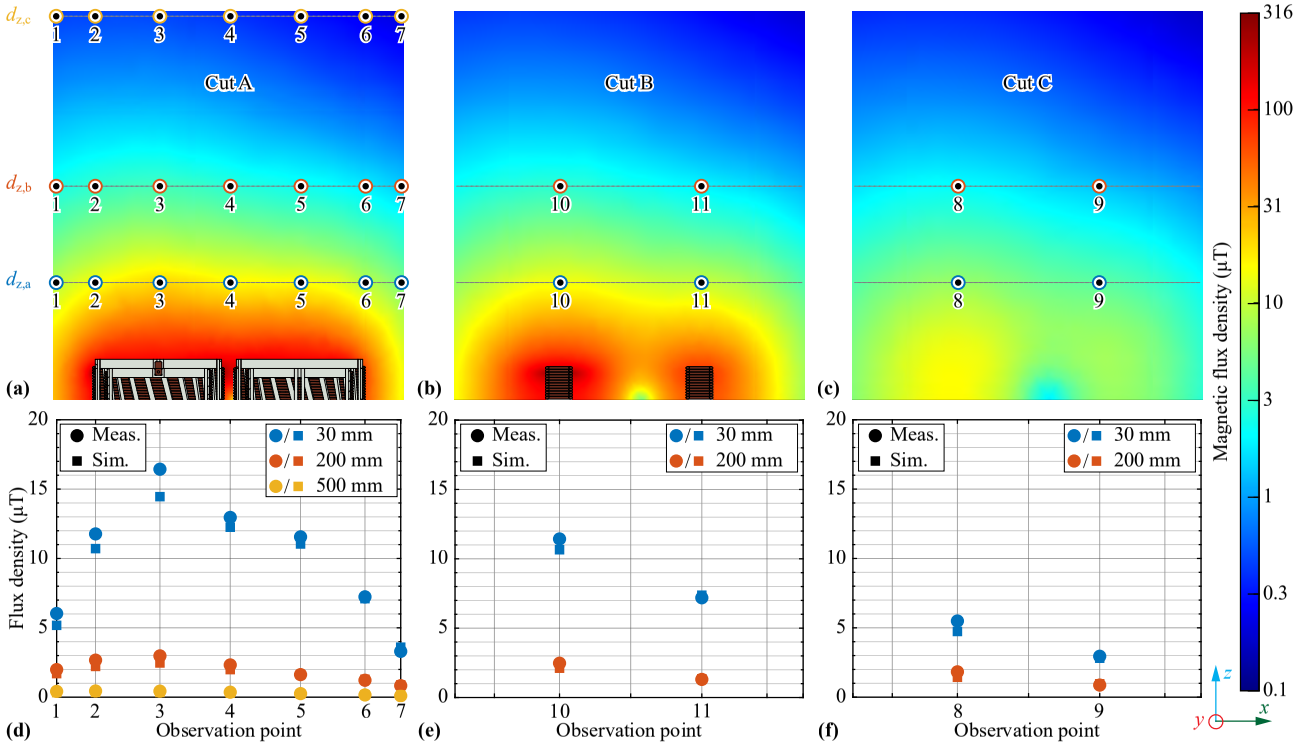


Fig. 3.17: (a)–(c) FEM-simulated flux densities within the cut planes A, B, C (see **Fig. 3.16(d)**): ACT without shielding, open-circuit at a secondary-side, primary-side current of 1 A. **(d)–(f)** Measured and simulated rms values of the magnetic flux densities at the observation points defined in **Fig. 3.16(d)**. The measured results are normalized to a primary-side current of 1 A to allow a comparison with the FEM results.

Shielding efficacy

In a second step, the measurement setup is used to determine the efficacy of the shielding for two different secondary-side configurations, i.e., open- and short-circuit. The open-circuit case is representative for no- or low-load operation, where the ACT's comparably high magnetizing current dominates (I_m = 40 A rms, cf. **Tab. 3.4**, due to the ACT's limited magnetizing inductance). The short-circuit case corresponds to operation at higher current, close to rated load where the load current becomes dominant. **Figs. 3.18(a)–(f)** depict the results that are measured for an rms current of I_meas = 10 A and scaled to the nominal current of $I_\mathrm{p,rms}$ = 74.6 A (for $I_\mathrm{s,rms}$ = 56.6 A) in case of a secondary-side short-circuit and $I_\mathrm{p,rms}$ = 30.0 A for open-circuit (considering a first harmonic component of the nominal primary voltage of $V_\mathrm{p,rms} = 4V_\mathrm{1,DC}/(2\sqrt{2}\pi)$ = 3.2 kV),

$$B_\mathrm{meas,s} = B_\mathrm{meas}\frac{I_\mathrm{p,rms}}{I_\mathrm{meas}}. \tag{3.3}$$

According to **Figs. 3.18(a)** and **(d)**, the designed ACT with shielding fulfills ICNIRP 2010 guidelines [67] for occupational exposure at a distance of 30 mm from the shielding, if the spatial average[2] of the flux density is considered. Furthermore, **Figs. 3.18(b)** and **(e)** reveal that the ACT with shielding fulfills the guidelines for both occupational and public exposure at a distance of 200 mm from the shielding when considering the spatial average (even though the local values at points 8 and 10 exceed the reference level for the short-circuit case). Lastly, the measurements in a distance of 500 mm, depicted in **Figs. 3.18(c), (f)**, show that the guidelines for occupational exposure are met even without the shielding (spatial average). Lastly, as in practice the shielding would be realized as a full enclosure, the flux density in the proximity of the ACT would be even lower (cf. **Fig. 3.8(c)**), and hence the exposure limits would already be met closer to the shielding. In summary, the shielding provides an adequate efficacy, especially considering that an ACT would typically be located in an area with limited public access, as opposed to IPT systems.

[2] The spatial average is calculated / measured by scanning a planar area equivalent to the area occupied by a standing adult human (projected area). In most instances, a simple vertical, linear scan of the fields over a height of 2 meters is sufficient [68].

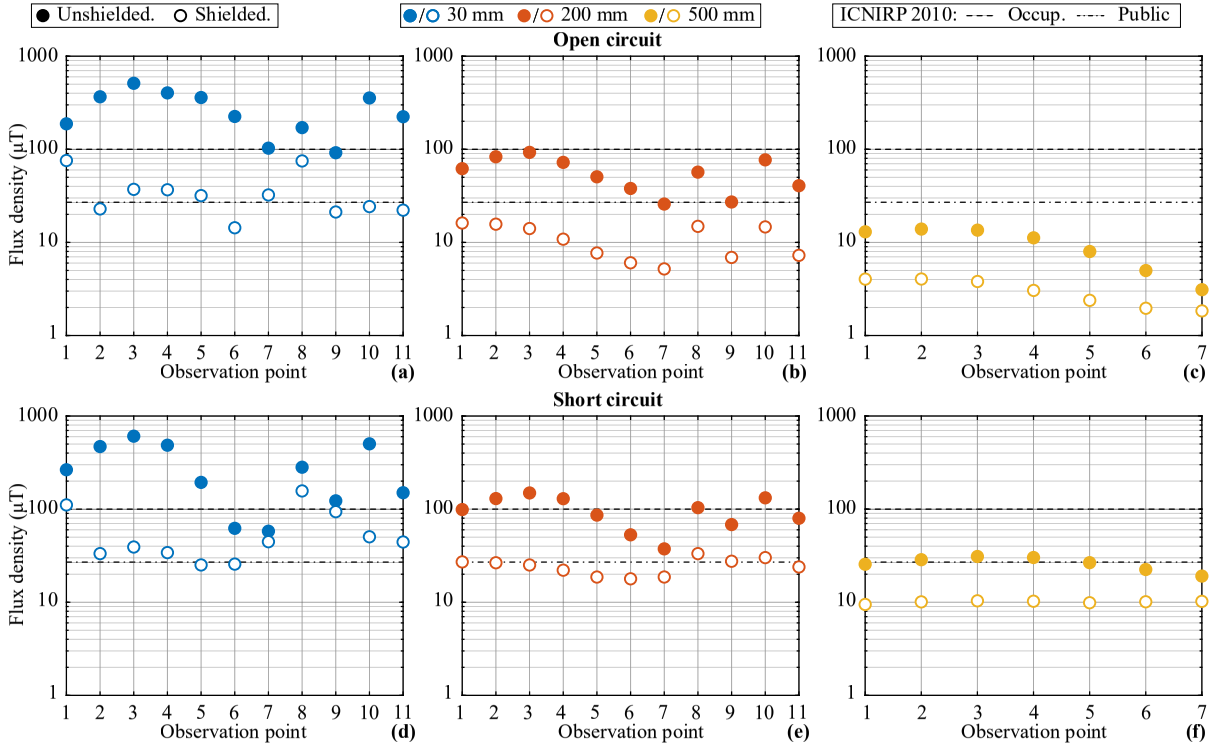


Fig. 3.18: Measured rms values of the mag. flux densities at the points defined in **Fig. 3.16(d)**, w/ and w/o shielding: **(a)–(c)** secondary-side open-circuit. **(d)–(f)** secondary-side short-circuit. Results are scaled to the nom. current, cf. (3.3). The levels for the allowable field exposure of the general public (27 µT) and of personnel in occupational settings (100 µT) are shown [67].

3.5.8 Comparison of Optimization and Experimental Results

In addition to the specific validation of individual models discussed throughout the experimental section, e.g., regarding the shielding, the experimental results also enable an overall comparison of the ACT prototype's measured characteristics (e.g., losses, power density) with those obtained from the initial model-based multi-objective optimization described in **Section 3.3.3**.

To do so, we highlight the prototype's location in the performance space shown in **Fig. 3.5**: the marking ● corresponds to the built prototype when considering the active part only, i.e., the two sets of coils, corresponding terminal blocks, and insulation barriers. In contrast, the symbol ★ represents the full ACT prototype, i.e., including the conductive shielding (full enclosure with honeycomb holes), the fans, and mechanical supports etc. The marking ● indicates the performance of the selected design according to the optimization results, as discussed earlier. Furthermore, **Fig. 3.19** presents mass, volume and loss breakdowns for the three cases.

Regarding the gravimetric power density, **Fig. 3.19(a)** reveals that the mass of the realized active part matches the optimization results closely ($\gamma = 25.7\,\mathrm{kW/kg}$, including a certain offset to account for fans, insulation etc.). However, the complete prototype's overall gravimetric power density is lower ($\gamma = 16.5\,\mathrm{kW/kg}$), mainly because of the weight of the structural parts required for the mechanical assembly. The mass breakdown reveals the great importance of low-weight realizations of coil formers, supports, fixtures, and insulation components, as they account for more than 55 % of the prototype's total mass. This relatively high share partly results from prototyping constraints and could be improved with industrial processes. Note that this is usually not the case for conventional MCTs where the weight of the core dominates [62]. Consequently, the gravimetric power density of MCTs is limited to approx. $10\,\mathrm{kW/kg}$ [28].

As shown in **Fig. 3.19(b)**, the volume of the realized prototype's active part is approximately 50 % higher compared to the optimization result, which is a consequence of the implemented clearance and creepage distances (see **Section 3.4**) that demand longer coil formers and insulation barriers. The overall volumetric power density of the complete prototype of $\rho = 2.2\,\mathrm{kW/dm^3}$ is determined by the box-shaped shielding enclosure, which has been designed a posteriori. Note that smaller enclosures would be possible if higher losses in the shielding would be accepted. It is important to point out that the initial analysis presented in [28] clearly shows that a conventional MCT is

the better choice for achieving high compactness, as an up to 50 % higher volumetric power density can be achieved. However, compactness together with stringent requirements related to insulation and cooling (potting of the windings, handling of increased thermal resistances) render the design of the MCT challenging. In contrast, the clearance (and creepage) distances of the

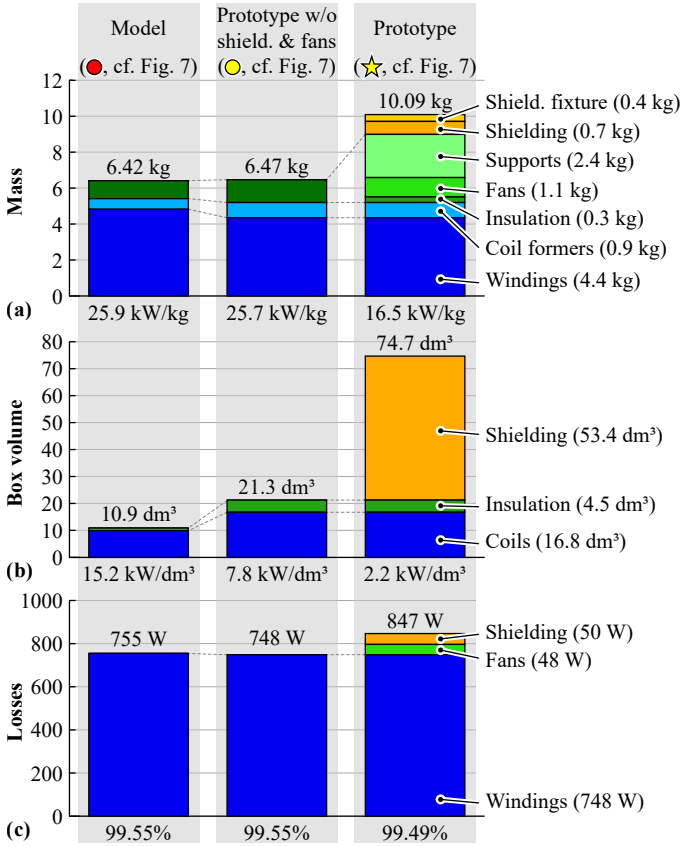


Fig. 3.19: Comparison of ACT modeling with experimentally validated results (see also **Fig. 3.5**). Breakdowns of: **(a)** masses; **(b)** boxed volumes, **(c)** losses. The left column represents results of the model-based optimization; the middle column considers measured results of the prototype's active part only; the right column finally considers the full ACT prototype.

proposed ACT can be easily extended to meet various insulation requirements by changing the NOMEX barrier elements (see **Section 3.4.1**).

Finally, the loss model used during the optimization (based on 2-D FEM simulations) proves highly accurate (see **Fig. 3.19(c)**). The loss contributions of the shielding (6 % of the total losses) and of the fans (6 %, whereby one should remember that passive cooling is feasible up to about 70 % of rated power) reduce the prototype's full-load efficiency ($\eta = 99.49\,\%$) only slightly.

All in all, the relatively straightforward models employed for the Pareto optimization capture the key performance characteristics quite accurately, especially regarding the expected ACT efficiency and the mass of its active part. The now established know-how regarding the mechanical assembly and the dimensions of a suitable conductive shielding could be included in future versions of the optimization procedure. However, as there are various degrees of freedom regarding both, the mechanical assembly and the design of an optimized shielding, which may further depend on specific application scenarios, a decoupled approach as used here might still be attractive to retain full design flexibility.

3.6 Transformer Operation in 1:1-DCX

The final section of this chapter discusses the overall performance of the ACT-based 1:1-DCX, with a special focus on the ACT's partial-load efficiency.

Since the ACT is a linear system, the previously validated loss models can be evaluated at reduced power levels to calculate the losses of the ACT for partial-load operation. This holds for the losses in the windings and in the conductive shielding (FEM-based calculations). Furthermore, passive cooling is sufficient up to about 70 % of the rated power. Hence, the power consumption of the fans must be considered only for higher power levels. **Fig. 3.20** shows measured (stars) and simulated (circles) distributions of the ACT losses and the corresponding efficiency curve. The partial-load efficiency of the transformer is very high, i.e. $\eta > 99.4\,\%$ applies for a very wide range of the output power, i.e., $P_\mathrm{o} \in [15\%, 100\%]P_\mathrm{N}$. The ACT achieves this high partial-load efficiency despite the high magnetizing current (compared to a conventional MCT) and increased winding losses, which is possible thanks to the absence of core losses. Finally, on the system-level, the relatively high magnetizing current advantageously facilitates ZVS for the 1:1-DCX power semiconductors.

With regard to the overall 1:1-DCX system, the losses of the semiconductors (conduction and switching losses) and the capacitors (resonant and

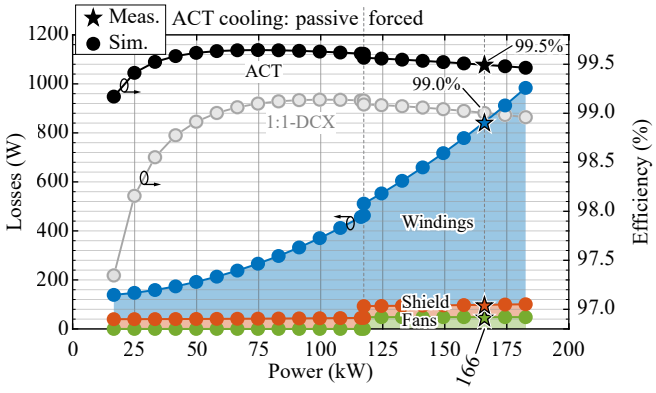


Fig. 3.20: Measured (★) and simulated (●) distributions of the transformer losses; efficiencies of transformer and 1:1-DCX. At the rated power of 166 kW, the transformer efficiency is 99.5 %, whereas the converter efficiency reaches 99.0 %.

DC-link) as well as the power demand of the fans are considered in a simulation as presented in **Chapter 2**. **Fig. 3.20** shows the calculated overall system-level efficiency of the ACT-based 1:1-DCX. At the rated power of $P_N = 166$ kW, the transformer efficiency is 99.5 %, and the converter efficiency reaches 99.0 %, which it even exceeds down to about 35 % of the rated power. For the detailed analysis and discussion of the ACT-based 1:1-DCX see **Chapter 5**.

3.7 Conclusion

In this chapter the design, realization, and the experimental evaluation of a 166 kW / 7 kV air-core transformer (ACT) as part of a DC transformer (DCX), i.e., the DC-DC converter stage of a solid-state transformer (SST) is presented. The realized full-scale prototype of the MV/MF ACT consists of two sets of coaxially arranged solenoids, achieving a relatively high coupling factor of 0.76. Thanks to this construction, a symmetrical design of primary- and secondary-side windings results and partial cancellation of magnetic stray flux is achieved.

The realization of the ACT is of relatively low complexity, as air can be used as an insulation and cooling medium, i.e., the ACT does not require potting material for insulation and thus the corresponding challenges known for conventional magnetic-core transformers (MCTs) are avoided, e.g., dielectric

losses, partial discharges, and the need for void-free potting of the windings. Furthermore, the thermal design is simplified as large areas of the transformer coils are available for direct (forced) air cooling. Thus, the ACT can be operated with a winding current density of more than 7 A/mm^2. Also, operation at up to 70 % of the rated power is feasible with passive cooling (i.e., natural convection) only, e.g., in case of defective fans. These aspects translate into comparably simple and hence cost-effective manufacturing, which is complemented by simplified handling because of the relatively low mass.

The ACT prototype features a nominal insulation voltage of 10 kV. Clearance and creepage distances according to IEC 62477 are realized by adding barrier elements made of NOMEX into the air gaps between primary- and secondary-side windings. In contrast to MCTs, the clearance and creepage distances can be increased by simply extending the length of the barrier elements, i.e., they can be tailored to meet more stringent requirements, e.g., for airborne applications, where larger clearance distances must be used to account for lower air pressure.

To reduce the magnetic stray flux in the proximity of the transformer, a conductive (aluminum) shielding enclosure is designed, built, and tested. With the proposed shielding, the ACT fulfills the ICNIRP 2010 guidelines regarding the magnetic stray flux levels for public exposure at a distance of 200 mm from the shielding. Adding the shielding enclosure increases the weight by around 10 %, the overall losses by 6 %, and determines the boxed volume of the transformer, yielding a volumetric power density of 2.2 kW/dm^3 (compared to 7.8 kW/dm^3 without the shielding).

The ACT prototype achieves a measured full-load efficiency of 99.5 % at an operating frequency of 77.4 kHz, and an unprecedented gravimetric power density of 16.5 kW/kg. Moreover, considering the use of 10 kV SiC MOSFETs, a system-level efficiency of 99 % is estimated for the complete 1:1-DCX at an output power of 166 kW. In addition, the ACT-based 1:1-DCX is characterized by an extremely flat efficiency curve because of the ACT's low no-load losses. Overall, these properties render the ACT a serious competitor of the MCT. The ACT concept is thus particularly well suited for emerging applications in which robustness, weight, serviceability and cost-effective manufacturing of the transformer are of high importance.

4

MV/MF Magnetic-Core Transformer Prototype

This chapter summarizes the major research findings also published in:

- **P. Czyz**, T. Guillod, D. Zhang, F. Krismer, J. Huber, R. Färber, C. M. Franck and J. W. Kolar, "Analysis of the Performance Limits of 166 kW / 7 kV Air-Core and Magnetic-Core Medium-Voltage Medium-Frequency Transformers for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.

Executive Summary

Solid-state transformers (SSTs) are employing compact high-power medium-voltage (MV) medium-frequency transformers (MFTs) and enable the power transfer between galvanically isolated DC systems. Considering a typical SST isolation stage, i.e., a 166 kW unregulated series-resonant DC-DC converter acting as DC transformer (DCX) with equal input and output MV DC voltages of 7 kV (1:1-DCX), a component-level performance limit of a magnetic-core transformer (MCT) is derived. The design of a fully rated MCT prototype is described in detail and selected construction aspects are compared to equally rated air-core transformer (ACT). Furthermore, a comprehensive experimental characterization to validate the derived performance limits is provided, including also the analysis of stray magnetic fields. The realized MCT prototype achieves a measured efficiency of 99.7 % at a gravimetric power density of 6.7 kW/kg.

4.1 Introduction

Fuelled by the availability of wide-bandgap (WBG) SiC power semiconductors with blocking voltage ratings of up to 10 kV and beyond, solid-state transformers (SSTs) have been proposed as flexible isolation and voltage-scaling interfaces between medium-voltage (MV) and low-voltage (LV) DC or AC buses. Typical applications include, e.g., hybrid smart grid systems with AC and DC sections [13, 17], grid interfaces for renewable power sources [26, 27], hyperscale data centers [15, 16], high-power electric vehicle (EV) charging stations [10, 11], future ships [21–23], and future aircraft with distributed propulsion systems and on-board MVDC grids [24, 25, 28].

SSTs are comprising compact high-power MV medium-frequency transformers (MFTs) and accordingly enable voltage scaling and power conversion between galvanically separated DC systems. The design of MFTs involves various trade-offs between competing goals (e.g., power density, efficiency, insulation voltage, cost) and a large number of degrees of freedom (e.g., winding and core geometry, insulation material, operating frequency, cooling method) to balance these trade-offs. It is hence a non-trivial process resulting in vastly diversified MFT prototypes as reported in [12, 16, 44, 45, 51–53, 69–98]. **Fig. 4.1** provides an overview and classification of these MFTs.

Considering certain SST applications (e.g., airborne, marine) and, in general, handling aspects and resource usage, the MFT's gravimetric power density $\gamma = P_N/m$ (with P_N as the rated power) is an important characteristic. **Fig. 4.1(b)** indicates $\gamma < \approx 12\,\mathrm{kW/kg}$ for air-cooled (natural or forced convection) MFTs. A first approach to cross this barrier is the use of liquid cooling ($\gamma < \approx 25\,\mathrm{kW/kg}$). However, on the system level also the mass of the cooling system (heat exchanger, piping, pumps) would need to be accounted for. Furthermore, the relatively high complexity of a liquid cooling system may not be desirable in all applications.

Typically, air-cooled MFTs are realized with magnetic cores (magnetic core transformer, MCT) and a dry-type (potting) insulation system, whose combined mass ultimately limits the achievable gravimetric power density [16, 44, 45]. Thus, a second approach to increase the gravimetric power density beyond this limit requires that neither a magnetic core nor a dry-type insulation system is used. Accordingly, inspired by inductive power transfer (IPT) systems, we have proposed a MV air-core transformer (ACT) [28, 96, 99], see **Chapter 3**, which utilizes air as insulation medium and for direct cooling of the exposed windings. In addition to high gravimetric power density of up to $\gamma \approx 40\,\mathrm{kW/kg}$, ACTs feature comparably straightforward insulation design

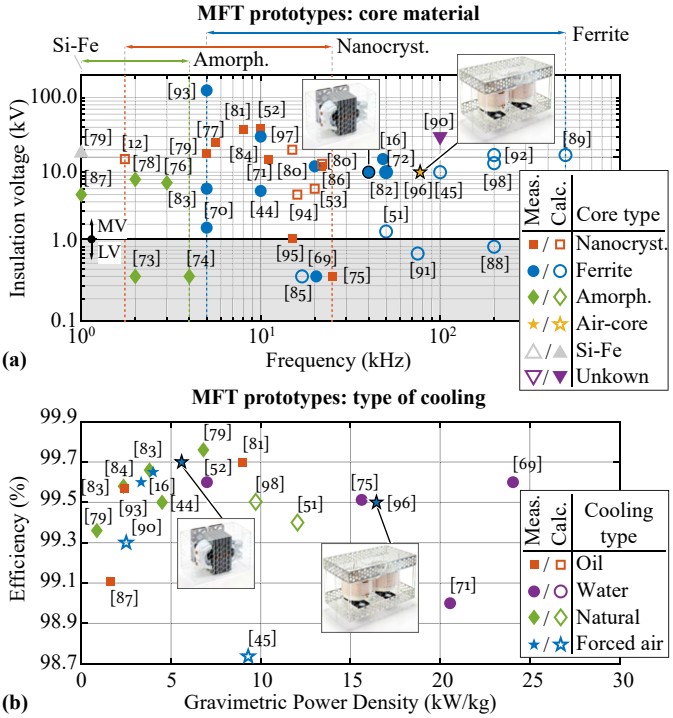


Fig. 4.1: Overview on MFT prototypes reported in the literature; the two MFTs discussed in this thesis are highlighted. **(a)** Rated insulation voltage[a] and operating frequency. Note the frequency-dependence of core material selection. **(b)** Efficiency and gravimetric power density of those prototypes where data on mass was available[b]. Note that the mass of external parts of liquid cooling systems is not considered.

[a] In cases where no explicit insulation voltage rating has been reported, the voltage rating of the high-voltage winding is shown.
[b] Note that information about the masses of prototypes [83, 87, 93, 98] was obtained directly from the authors.

and mechanical construction, which, together with the absence of magnetic cores, creates a potential for resource and cost savings. On the other hand, the volumetric power density $\rho = P/V$ of an ACT will be relatively low due to the lack of guidance for the magnetic flux.

Whereas the theoretical limits for the volumetric power density of MCTs have been derived in [100–102] and a weight-optimized low-power MCT has been presented in [45], to the knowledge of the author literature does not yet cover a comprehensive and experimentally supported analysis of the gravimetric power density limits of dry-type MCTs and a comparative evaluation against ACTs. Extending and improving the preliminary theoretical analysis from [28], and building on the detailed experimental characterization of an ACT prototype from [96], this chapter aims to fill that gap and clarify the comparative evaluation of MCT and ACT concepts. A special focus is placed on the insulation design and the analysis of magnetic stray fields.

We exemplify the considerations on a 166 kW 1:1-DCX system presented in **Chapter 2**, i.e., a series resonant DC-DC converter operated at the resonance frequency, which therefore acts as a DC transformer (DCX) [16, 18–20]. **Tab. 2.1** summarizes the considered specifications and **Figs. 2.2(a),(c)** show the topology and key waveforms.

The chapter is organized as follows: **Section 4.2** describes the detailed modeling and multi-objective optimization of a 166 kW / 7 kV MCT for a 1:1-DCX converter system, resulting in the theoretical performance limits. **Section 4.3** then discusses realization aspects for both MFTs, i.e., ACT and MCT, and constructed prototypes, whereas **Section 4.4** covers the experimental characterization of a full-scale MCT prototype (for the corresponding characterization of the ACT prototype, see **Chapter 3**). Finally, **Section 4.5** provides concluding remarks about the realized MCT prototype which at the rated power of 166 kW achieves an efficiency (calculated based on experimentally measured loss components) of 99.7 % at a gravimetric power density of 6.7 kW/kg and a volumetric power density of 5.4 kW/dm^3.

Note that this chapter characterizes experimentally only the MCT. For more comparative results and a discussion of two DCXs (MCT-DCX and ACT-DCX) please refer to **Chapter 5**.

4.2 Modeling and Optimization

To derive the performance limits (efficiency, gravimetric power density, and volumetric power density) of a MCT-based 166 kW / 7 kV 1:1-DCX converter system, we employ the multi-objective optimization approach illustrated

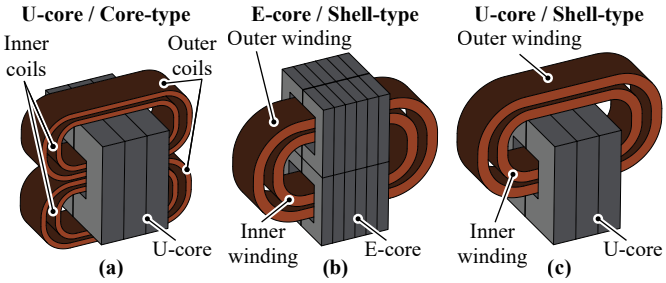


Fig. 4.2: Considered MCT configurations: **(a)** core-type transformer consisting of an U-core with one set of concentric windings per limb; **(b)** shell-type transformer consisting of an E-core with concentric windings; **(c)** shell-type transformer consisting of an U-core with concentric windings.

by **Fig. 2.3(b)**, which calculates the performance indices for a wide range of different designs. For the MCT, we employ a semi-analytical (analytical equations but solved numerically) optimization routine. With the properties of a given transformer design, the system-level performance can be obtained by appropriately dimensioning and modeling the DCX's remaining components (switching stage, resonant capacitors, cooling system).

The following subsections first describe the considered transformer configurations and the modeling approach before then presenting the optimization results and the selection of the design for the actually realized prototype.

4.2.1 Multi-Objective Optimization

As discussed earlier, we consider an air-cooled MCT with a dry-type insulation system. **Fig. 4.2** shows the three basic arrangements of cores and windings: core-type with U-core, shell-type with E-core, and shell-type with U-core. However, the core-type transformer (cf. **Fig. 4.2(a)**) uses two sets of windings, which increases the number of cable terminations and leads to a higher complexity of the insulation system, especially in the winding window of the core. Therefore, we consider only the shell-type configurations with E- or U-core for the optimization. We do not consider interleaving of the primary and secondary windings due to the insulation requirements. To avoid problems with current sharing [103], windings are realized without paralleling of litz wires.

Considering the target operating frequency range of several 10 kHz, the magnetic core can be realized from either ferrite or nanocrystalline mate-

rial (amorphous cores would yield unacceptable hysteresis and eddy-current losses) [102]. By introducing an air gap between the core halves (all limbs), the magnetizing inductance, L_m, and hence the magnetizing current available for realizing ZVS of the two converter bridges can be adjusted. The transformer windings are made of litz wires where we consider two different strand diameters (71 µm and 100 µm, 47 % fill factor) to account for the potentially lower operating frequencies compared to the ACT. The minimum insulation distance considered for the MCT is $w_\mathrm{iso} = 4\,\mathrm{mm}$, as the windings are encapsulated with silicone elastomer insulation (Dow Corning TC4605 HLV, [104]). Considering that in practical designs part of the inter-winding space is taken by the perforated coil former, the effective distance becomes 2.5 mm (1.5 mm thick coil former) which results in an electric field of 4 kV/mm, well below the silicone's breakdown electric field of 24 kV/mm. Details of the actually realized insulation design and capabilities of the MCT are discussed in **Section 4.3.1**.

We characterize the MCT's performance with analytical models and based on the routine presented in [62, 105]. The magnetic field in the winding window and the leakage inductance L_σ are computed with the mirroring method [106]. Based on the fields, the HF winding losses are analytically computed [105, 106]. Again, the winding loss calculation accounts for imperfect twisting of the litz wire strands with a loss penalty factor $k_\mathrm{loss,w} = 30\,\%$, see [57, 58]. The magnetizing inductance L_m and the flux inside the core are obtained with a reluctance model, which considers the air gap fringing field [106, 107]. Furthermore, the core losses are computed with the improved generalized Steinmetz equation (iGSE) [108] using a loss map of the respective core material [109] (function of flux density, frequency, temperature and DC bias). The calculated core losses are increased by 20 % (safety factor $k_\mathrm{loss,c}$) to include potential deviations of the employed datasheet-based core loss map from the actual loss density of the cores based on experience from previous prototypes [80], see **Section 4.4.3** for experimental validation. Finally, the total dielectric losses of the dry-type insulation system are assumed to be 40 W, which is based on experience from [43]. The thermal management of the transformer is based on heat conduction (from the windings through the dry-type insulation) and forced-air cooling. Thus, the thermal behavior of the MCT can be modeled with a lumped thermal equivalent circuit [109, 110] and it considers thermal and loss coupling between the windings, insulation and core.

Whereas **Tab. 4.1** summarizes fixed parameters of the MCT model (and of the ACT for reference), **Tab. 4.2** provides an overview on the design space, i.e., the parameters varied to generate different transformer designs:

Tab. 4.1: Fixed parameters for ACT and MCT models.

Var.	Value		Description
	ACT	MCT	
Constant parameters			
w_{iso}	16.5 mm	4 mm	insulation distance
d_{litz}	71 µm	71/100 µm	litz strand diam.
k_{litz}	39.5 %	47 %	total litz fill factor
$k_{\mathrm{loss,w}}$	30 %		imperfect twisting loss penalty
$k_{\mathrm{loss,c}}$	–	20 %	core loss map penalty
P_{diel}	0 W	40 W	dielectric losses
$I_{\mathrm{m,peak}}$	N/A	20 A	peak mag. current

- operating frequency (f_{s}),
- core shape, material (3C94 or VITROPERM 500F), dimensions (including the number of stacked cores), and peak flux density (r_{A}, $\hat{B}_{\mathrm{s}}$),
- number of turns and layers in windings (N, N_{layer}),
- current density (J_{litz}),
- air speed (v_{air}) as well as air channel width (d_{air}, for discrete design space only, cf. **Fig. 4.4(a)**).

Note that for the MCT two design spaces can be distinguished: first, a continuous variation of the core geometry is assumed, i.e., the geometry follows from a variable ratio of core depth to core limb width, r_{A}, the selected winding configuration with insulation that defines the core window height and width, and the necessary total area of the core given by the desired peak flux density. However, in practice only discrete core geometries and litz wire configurations are available off-the-shelf. Therefore, a second optimization run considers only such realizable geometries, whereby several off-the-shelf cores can be stacked to obtain the required total core cross section. Note that, in order to minimize the weight of the core, the length of the individual U-core (along y-axis, cf. **Fig. 4.4(b)**) is still variable to adapt the winding window optimally to the height of a given winding. Shortening of the limbs can easily be done by the manufacturer and significantly expands the available performance space. Furthermore, introducing air channels between the

Tab. 4.2: Analytical design space and constant parameters for the MCT optimization.

Var.	Value		Description
	E-core / U-core		core type
	Ferrite	Nanocrystalline	core material
f_s	[20, 70] kHz	[10, 40] kHz	op. frequency
r_A	[0.3, 2]	[0.3, 1]	core geometry
$\hat{B}_s$	[70, 250] mT	[100, 800] mT	peak flux density
	Shell-type		winding type
J_{litz}	[0.5, 10] A/mm^2		current density
N	[4, 120]		num. of turns
N_{layer}	[1, 3]		num. of layers
v_{air}	[1, 10] m/s		air speed
d_{air}	[0, 4] mm		air channel width

r_A – ratio of the U-core thickness to width of limb

stacked cores (gapped core, see e.g., **Fig. 4.4**) improves the heat extraction from the cores [111, 112].

4.2.2 Optimization Results

The multi-objective optimization procedure outlined in **Chapter 2** generates a high number of valid designs of MCT-based 166 kW / 7 kV 1:1-DCX systems. These can be compared regarding their efficiency, gravimetric power density and volumetric power density on the component level.

Fig. 4.3 compares the different MCT configuration options in the η-γ-performance space (thus emphasizing the aim for a lightweight design). Considering designs using ferrite cores without cooling channels in between (ungapped core), and a conservative airflow velocity of 1 m/s, **Figs. 4.3(a)–(b)** show that designs based on E-cores and U-cores achieve similar gravimetric power densities that cannot exceed $\gamma < \approx 9$ kW/kg, however with a slight advantage of E-core designs in terms of efficiency. **Fig. 4.3(c)** indicates that replacing the ferrite cores by nanocrystalline cores (while keeping cooling conditions identical) still allows to reach similar yet not significantly better performance. However, the presence of air gaps in nanocrystalline cores is critical regarding losses [113]. Furthermore, owing to the presence of high

capacitively coupled voltages in the core, short-circuits can occur between the laminations [114]. Therefore, and because of the scarce availability and high cost of nanocrystalline cores, we do not consider this core material further.

Aiming for an actual realization of an MCT prototype, we consider a discrete design space comprising actually obtainable cores and litz wires. With the same boundary conditions as used for the idealized results (continuous design space) shown in **Figs. 4.3(a)**, **(b)**, the maximum gravimetric power density of designs obtained from the discrete design space is limited to $\gamma < \approx 5\,\mathrm{kW/kg}$. To prevent this significant reduction, we insert air channels between the stacked cores [111], which improves the heat extraction. Increasing in addition the airflow velocity to still moderate 5 m/s facilitates the performance shown in **Fig. 4.3(d)**, which is similar to the earlier results. Further increasing the airflow velocity results in diminishing improvements only but clearly requires higher effort (larger and more powerful fans), which is why we consider 5 m/s suitable for practical realizations. Thus, the maximum gravimetric power density of practical MCT designs can reach $\gamma = 10\,\mathrm{kW/kg}$. We consider the results of this discrete design space based on ferrite E-cores for the comparison with the ACT below.

Note that the above considerations highlight the importance of considering real dimensions of available components, mainly of the magnetic cores, during the optimization of MCTs. No such restrictions exist for the design of ACTs (except regarding available litz wires).

As mentioned in **Chapter 3** we select the MFTs (ACT and MCT) designs to be realized as prototypes by demanding a system-level DC-DC efficiency of $\geq 99.0\,\%$ (for the DCXs evaluation see **Chapter 5**) and then choosing the MFT design with highest calculated (component-level) gravimetric power density. Therefore, the selected MCT is indicated in **Fig. 4.3(d)** and as it can be seen from the results, there is no significant benefit of increasing the MCT operating frequency above 40 kHz (e.g., to 70 kHz), which is thus selected. Note that various practical aspects and mainly mechanical constraints (see **Section 4.3**) typically decrease the power density of prototypes compared to idealized calculation results. This explains why the realized prototypes do not lie on the η-γ-Pareto front, see **Section 5.1** for details.

Further evaluation on component- and system-level including gravimetric and volumetric power density as well as efficiency is presented in **Chapter 5**.

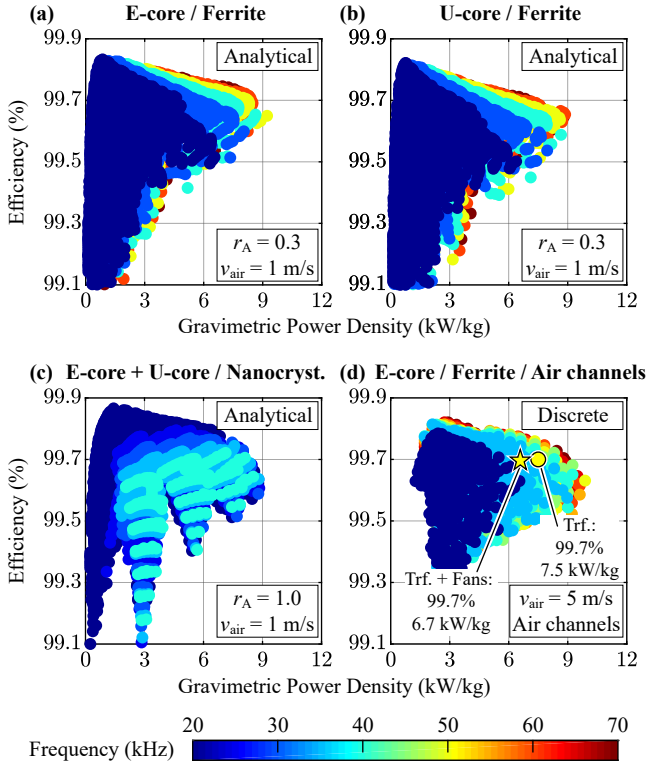


Fig. 4.3: Results of the multi-objective optimization for different types of the 166 kW / 7 kV MCT, revealing the characteristic dependencies of the η-γ-Pareto fronts on the operating frequency. Results based on the continuous design space showing theoretical limits of realization with ungapped cores and conservative cooling (1 m/s airflow): **(a)** ferrite E-core type; **(b)** ferrite U-core type; **(c)** nanocrystalline E- and U-core types. **(d)** Results based on off-the-shelf components (discrete design space) for the selected concept of ferrite E-core type with air channels between the stacked cores (gapped) to improve the cooling capabilities (5 m/s airflow). The marker ○ represents the selected design and the marker ☆ indicates measured result of the actually realized MCT prototype (f_s = 40.0 kHz). Note the performance deviation from the optimization results which are due to additional construction constraints and because the idealized models do not include weight and volume of the cooling system (fans).

4.3 Design and Construction

As mentioned above, the ultimately achievable mass and volume of the selected ACT and MCT designs strongly depend on practical realization aspects and are mainly determining the performance of the corresponding DCX systems. Therefore, this section presents the design and construction of the two transformer prototypes, focusing on the key aspects of insulation design, shielding of electromagnetic stray fields and cooling.

4.3.1 MFT Insulation Design

For both transformers, the rated CM DC insulation voltage is $V_\mathrm{i} = 10\,\mathrm{kV}$. According to IEC 62477 [59, 60], the minimum required clearance distance for overvoltage category III (OV-III), which demands an impulse withstand voltage of 37 kV, becomes 55 mm. Similarly, the minimum required creepage distance, considering pollution degree 2 (PD2) and insulation material group II, is 71 mm.

Regarding the overall mechanical arrangement of the ACT, **Fig. 3.6** shows how the single-layer winding of each coil is placed on an individual 3-D-printed polycarbonate coil former. A fixed insulation distance ($w_\mathrm{iso} = 16.5\,\mathrm{mm}$) between the primary- and the secondary-side windings has been considered already during the optimization, limiting the field strength in the air between the windings to safe values ($< 0.6\,\mathrm{kV/mm}$ considering homogeneous field). In order to realize the required clearance and creepage distances, cylindrical barrier elements made of 1.5 mm type 993 Nomex pressboards are placed between the primary- and secondary-side coils. Similarly, a rectangular Nomex plate (thickness of 1.5 mm) ensures sufficient clearance between the two coil sets; a creepage distance of 79 mm was realized. The implemented clearance distance of 66 mm corresponds to an impulse withstand voltage of about 43 kV. Note that this relatively simple insulation system allows to tailor clearance and creepage distances as required by standards and environmental conditions a posteriori (i.e., after the optimization) by adapting the dimensions of the Nomex elements, with little impact on the overall mechanical design.

Fig. 4.4 shows a 3-D CAD rendering of the MCT prototype which consists of a ferrite E-core (assembled from 24 ferrite U126/72/20 U-cores), and a winding package. The winding package contains two (primary and secondary) two-layer coils that are wound on corresponding coil formers, encapsulated in a dry-type (silicone) insulation and enclosed by a 3-D-printed polycarbonate cover. The realized minimum distance between the primary and the

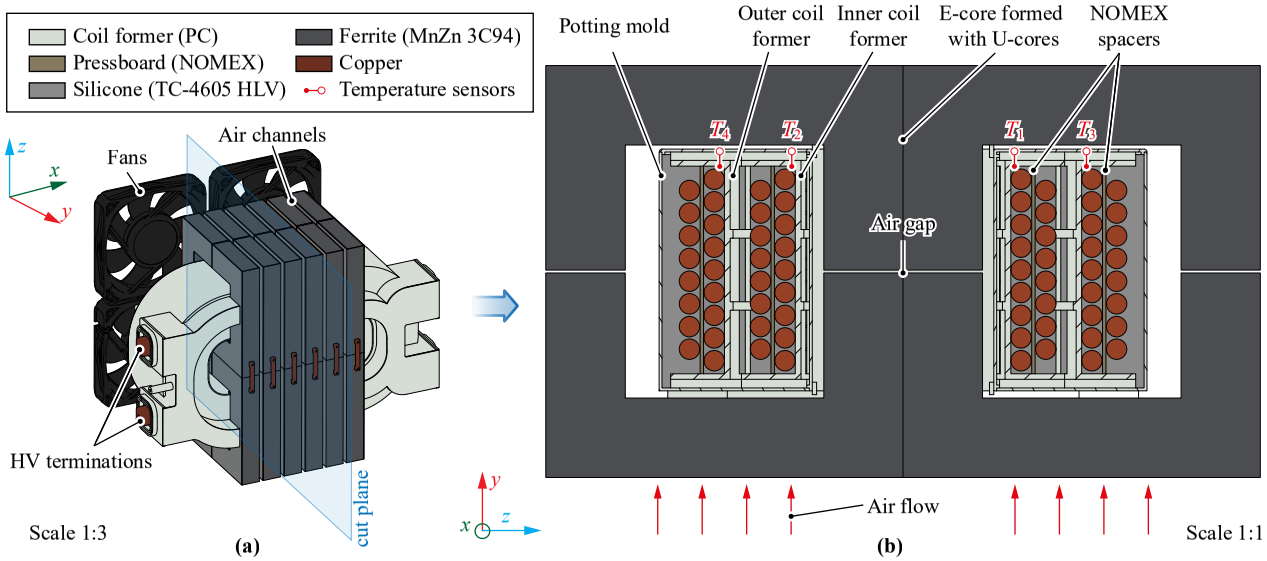


Fig. 4.4: (a) 3-D CAD rendering of the MCT prototype showing winding package (terminations, polycarbonate cover), cores with air channels, and cooling fans. **(b)** Cut view of the transformer. The direction of the airflow as well as the positions of temperature sensors used during characterization are indicated. Note the Nomex spacers that are used to maintain a distance of at least 1.5 mm between the layers of the windings.

secondary sides is $w_{iso} = 6\,mm$, which is higher than the value used during the optimization ($w_{iso} = 4\,mm$, see **Section 4.2.1**). This is necessary because of the increased dimensions of the coil formers needed to provide sufficient rigidity to facilitate the manufacturing of the windings using relatively thick litz wire. The windings are encapsulated (potted) with a two-component silicone compound (TC4605 HLV, [104]) that is characterized by a relatively low dissipation factor and a high thermal conductivity. With the insulation distance $w_{iso} = 6\,mm$ and the considered insulation voltage of 10 kV, the electric field in the insulation becomes 1.7 kV/mm, which is significantly below the breakdown electric field of the silicone (24 kV/mm). The realized clearance distance is the same as for the ACT (66 mm, impulse withstand voltage of about 43 kV). The creepage distance is much longer, i.e., about 200 mm, owing to the realized creepage distance extenders surrounding the terminations, which are integrated into the polycarbonate cover of the winding package, see **Fig. 4.4(a)**.

From the peak voltage applied to a winding of the transformer, which is the difference of the voltage applied by a half-bridge ($v_{p,s}$) and the voltage of the corresponding resonant capacitor (v_{Cr} in case of the MCT or $v_{Cr1,Cr2}$ in case of the ACT), the maximum voltage between two adjacent turns of a coil can be obtained. This voltage is about $5.4\,kV/44 \approx 123\,V$ for the ACT and about $4.0\,kV/17 \approx 235\,V$ for the MCT. Both values are well below the capability of the litz wire's insulation, i.e., a double layer of polyamide. As the MCT uses a two-layer winding, the worst-case voltage between the two layers is 2.0 kV, resulting in an electric field of 1.3 kV/mm. Thus, the insulation between the two layers is ensured by 1.5 mm Nomex spacers (electric strength of 34 kV/mm).

The winding terminations of both prototypes are copper blocks that are edgeless (i.e., feature rounded edges) to prevent excessive local electric fields in the surrounding air.

We employ 3-D FEM simulations of the electric fields inside the transformers for a final verification of the insulation design for the CM voltage of +5 kV/−5 kV. The structural and insulation materials are modeled using the dielectric parameters given in **Section 5.3.1**. The results for the MCT shown in **Fig. 4.5(a)** indicate a maximum peak value of the electric field in the inter-winding space of $E_{peak,max} = 17.0\,kV/cm$, which is more than 14× lower than the breakdown field strength of silicone (240 kV/cm). **Figs. 4.5(b), (c)** show the results for the ACT, where a maximum peak value of the electric field of $E_{peak,max} = 21.3\,kV/cm$ is found around the wires. This value is lower than the critical field strength of dry air (24.4 kV/cm bar).

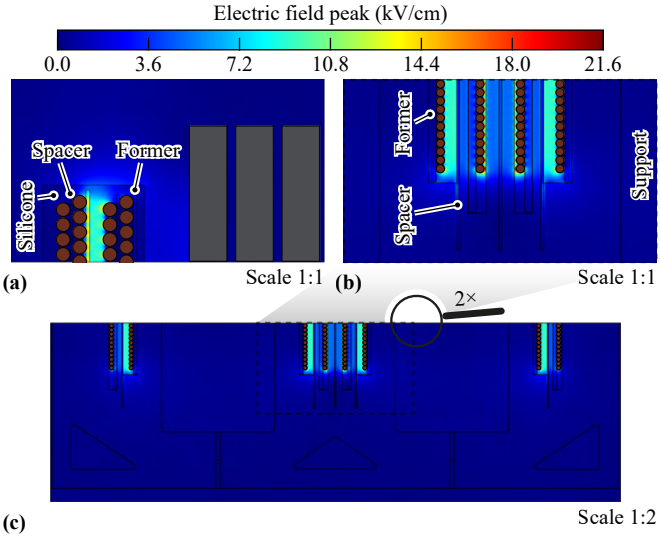


Fig. 4.5: Cross sectional views of 3-D-FEM simulations of the electric field distribution (peak values) in the transformers for the worst-case operating point with +5 kV/−5 kV CM excitation: **(a)** MCT, **(b)** ACT (magnified partial view of the middle of the transformer), and **(c)** ACT (complete cross section view).

4.3.2 MFT Shielding

In **Chapter 3**, we have described the design of a lightweight, low-loss conductive shielding to limit the magnetic stray fields in the vicinity of the ACT to safe levels according to the ICNIRP 2010 guidelines [67]. A conductive shielding (cf. **Fig. 3.7** and **Tab. 3.3** for dimensions) allows for eddy currents to flow such that they, according to Lenz's law, (partially) compensate the stray magnetic field. Of course, these eddy currents generate losses; however, a quite thin (e.g., 0.5 mm) aluminum sheet provides sufficiently low resistance to limit these to reasonable values of about 50 W (estimated with 3-D FEM simulations). Using a honeycomb perforation of the shielding facilitates forced-air cooling and decreases the weight without compromising the shielding efficacy. Note that for the prototype, we realize only a partial shielding covering the worst-case regions with respect to magnetic stray fields (see **Fig. 4.8(b)**). This simplifies experimental testing as the access to the windings remains free.

Even though magnetic-core MFTs commonly are not shielded [12, 16, 44, 45, 51–53, 69–95, 97, 98], it has been shown that the magnetic flux density in the proximity of MCTs, especially close to the air gap, can reach up to several mT [115], causing eddy-current losses in metallic elements and disturbances in nearby electronic circuitry [116, 117]. It is therefore interesting to analyze the magnetic stray fields of the MCT prototype and to compare them against the ICNIRP guidelines [67] and the results for the ACT, thereby clarifying whether additional shielding is necessary.

Figs. 4.6(a)–(b) show the simulated (3-D-FEM) rms flux densities in the proximity of the MCT and of the ACT, respectively, for their nominal currents and without shielding, and **Figs. 4.6(c)–(d)** present respective values of the magnetic flux densities at the observation points 1…8 along the x- and z-axis. Close to the MCT, the stray flux density in the plane of the air gap is similarly high as that of the ACT, however, decays faster with increasing distance. Thus, the ICNIRP [67] limit for occupational exposure is met at a distance of about 130 mm from the MCT, in both, x- and z-directions (cf. points 4). The stray field decays below the limit for the exposure of the general public at a distance of about 250 mm. Note that the respective threshold distances for the (unshielded) ACT are 210 mm and 370 mm (beyond the range shown in **Fig. 4.6(b)**), i.e., are significantly higher, which makes explicit shielding necessary.

We thus conclude that in contrast to the ACT, the MCT does not require additional shielding of magnetic stray fields, as 250 mm seems a reasonable minimum distance between persons and an MV system also for reasons of

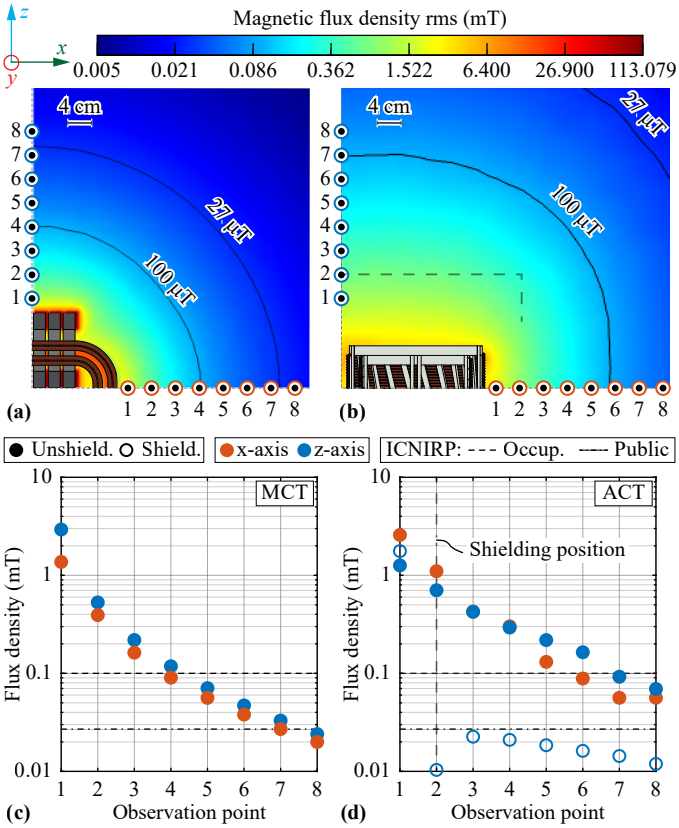


Fig. 4.6: Magnetic flux densities (rms) for nominal winding currents obtained from 3-D-FEM simulations: **(a)** MCT (plane of an air gap), **(b)** ACT (without shielding, plane through middle of coils). **(c)–(d)** Respective values of the magnetic flux densities at the indicated observation points 1...8. Additionally, the shielding efficacy along the z-axis for the ACT is visualized for comparison (non-filled circles). The ICNIRP 2010 [67] exposure limits for the general public (27 µT) and personnel in occupational settings (100 µT) are indicated, too.

electrical safety. However, two relatively simple methods to shield magnetic stray fields of an MCT exist, i.e., to use an air gap in the center leg (of an E-core) only or to wrap a thin copper foil around the core. The latter is known as *flux band* or *bellyband* and is common in audio or safety isolation transformers. Furthermore, such a copper band can also serve a second purpose and be used to define the electrical potential of the magnetic cores, e.g., by connecting the band to safety ground.

4.3.3 MFT Cooling

Both transformers employ forced-air cooling with identical sets of four fans (4×12 W, 4414FNH).

To improve heat extraction from the ACT's windings, the coil formers are perforated (see **Fig. 3.6**), which increases the winding surface that is directly exposed to the airflow generated by the fans placed below the transformer. For further details, please refer to [96].

In contrast, the extraction of losses from the MCT windings is hindered by the dry-type insulation, despite the relatively high thermal conductivity of the chosen silicone material. Therefore, a design with low winding losses is preferred as the heat can be much easier extracted from the cores. Placing 4 mm wide air channels between the stacked core sets significantly increases the core and winding package surface areas available for cooling. Furthermore, the transformer is oriented with the largest core surface (xz-plane, cf. **Fig. 4.4**) facing the airflow (along y-axis), ensuring also symmetric cooling conditions of the winding package.

4.3.4 Realized MFT Prototypes

Fig. 4.7 presents photos of the MCT's windings before potting and of the assembled MCT without the cooling system. It can be seen that the windings are placed on 3-D printed coil formers which are perforated (cf. **Fig. 4.7(a)**) to facilitate the silicone's flow during the vacuum pressure potting [16]. Furthermore, 2 NTC temperature sensors (PS104J2) are placed close to the endings of both, inner and outer, windings. **Fig. 4.7(b)** presents the assembled MCT and the remaining features such as potting pipes, creepage extenders and grounding bars.

The complete MCT and ACT prototypes including the cooling systems are shown in **Fig. 4.8**. **Tab. 4.3** gives an overview on the key characteristics of the realized prototypes.

Tab. 4.3: Key characteristics of the realized 166 kW / 7 kV magnetic-core (MCT) and air-core (ACT) transformer prototypes and their resonant capacitor banks.

	MCT	ACT	
Equivalent circuit parameters			
L_σ	52.4 µH	2×51.8 µH	pri. / sec. leak. induc.
L_m	1.18 mH	162.6 µH	magnet. inductance
n	1 : 1		turns ratio
k	0.98	0.76	coupling factor
$I_{p,s}$	52.4 A	56.6 A	pri. / sec. rms current
I_m	10.3 A	40.0 A	magnet. rms current
Winding			
N	17	2×22	number of turns
Litz wire	$5 \times 6 \times 5 \times 36$	$5 \times 10 \times 40$	bundles / strands
	double layer polyamide		insulation of litz wire
d_{litz}	71 µm		single strand diameter
n_{litz}	5400	2000	number of strands
J_{litz}	2.5 A/mm^2	7.2 A/mm^2	current density
Core			
N	24× U126/72/20	–	ferrite material 3C94
d_{gap}	2×1.1 mm	–	air gap
Insulation			
	dry-type	air	type
V_i	10 kV	10 kV	DC insulation voltage
w_{iso}	6 mm	16.5 mm	insulation distance
Power density			
γ	6.7 kW/kg	16.5 kW/kg	gravimetric
ρ	5.4 kW/dm^3	2.2 kW/dm^3	volumetric
Resonant capacitor bank			
f_s	40 kHz	77.4 kHz	operating frequency
C_r	300 nF	2×81.6 nF	resonance cap.

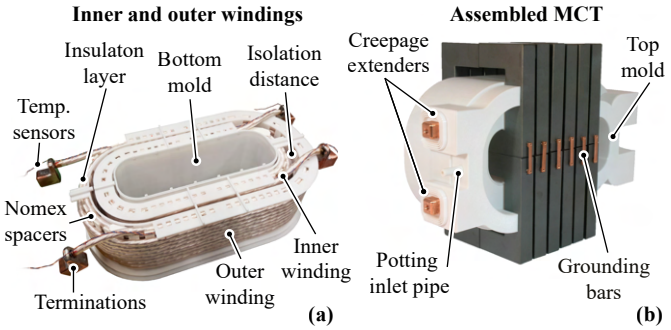


Fig. 4.7: (a) Photos of the realized windings of the MCT (before potting) and **(b)** final assembly without the cooling system.

Tab. 4.4: Small-signal parameters of the MCT (determined at $f = 40\,\mathrm{kHz}$).

Param.	Analyt.	Sim. 3-D	Meas.	Dev. Analyt. \ 3-D
L_σ	47.7 µH	50.0 µH	52.5 µH	9.0 % \ 4.8 %
L_m	1.13 mH	1.23 mH	1.18 mH	4.3 % \ 4.0 %
k	0.96	0.98	0.98	1.9 % \ 0.2 %

4.4 Experimental Characterization of the MCT

Whereas the characterization of the ACT prototype (cf. **Fig. 4.8(b)**) has been reported in detail in **Chapter 3**, this section summarizes the corresponding experimental characterization of the MCT prototype shown in **Fig. 4.8(a)**, i.e., experiments covering small-signal impedance measurements, insulation tests, large-signal tests, winding and core loss measurements, transient thermal response characterization, and magnetic stray flux density measurements. These results together with those for the ACT (see **Chapter 3**), as well as further comparative experimental analyses of specialized aspects such as the dielectric losses, given in **Section 5.3**, provide a comprehensive verification of the system-level comparison of ACT-DCX and MCT-DCX concepts given in **Chapter 5**.

4.4.1 Impedance Measurements and Resonances

We measure the MCT's short-circuit and open-circuit impedances from the primary and from the secondary side with a precision impedance analyzer

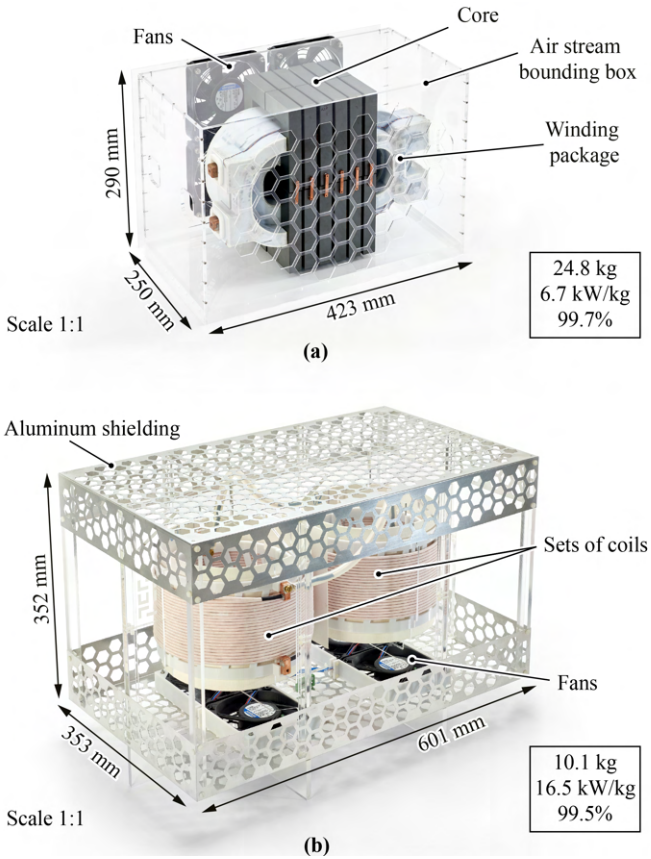


Fig. 4.8: Photo of the realized 166 kW / 7 kV **(a)** magnetic-core transformer (MCT), **(b)** air-core transformer (ACT).

(Agilent 4924A) to validate the computed values of L_σ and L_m from the equivalent circuit of **Fig. 2.2(a)**. **Tab. 4.4** compares the simulated and the measured values at the operating frequency of 40 kHz. All deviations between measurements and simulations are below 9 %, confirming good accuracy of the models employed for the optimization.

Fig. 4.9 shows the frequency characteristics of the open- and short-circuit impedances of the MCT as well as the common-mode (CM) impedance across the galvanic insulation (measured between the shorted primary-side winding

and the shorted secondary-side winding). The CM capacitance of 190 pF is relatively low, yet higher than that of the ACT (102 pF).

To check for any undesired impact of the resonances observed from **Fig. 4.9**, we compare the first series resonance frequency with the spectral envelope of the PWM voltage applied to the transformer, as suggested in [118]. The spectral envelope of a symmetric PWM voltage with a fundamental period of $T_s = 1/f_s$ and equal rise time (t_r) and fall time (t_f), see **Fig. 2.2**, can be described by the two corner frequencies $f_{c,1} = 1/\pi T_s$ and the higher $f_{c,2} = 1/\pi t_r$. For $f > f_{c,2}$, the envelope decays with −40 dB/dec. Even for very short rise/fall times of $t_r = t_f = 200$ ns, we find $f_{c,2} = 1.6$ MHz, which is lower than the MCT's first series resonance frequency of 1.73 MHz (as short-circuit resonances have even higher values, see **Fig. 4.9**). Therefore, the resonances are uncritical with regard to the operation of the 1:1-DCX.

4.4.2 Large-Signal Tests

As outlined in **Chapter 2**, since the currents in the MFT of the 1:1-DCX are quasi-sinusoidal (also see **Fig. 2.2**), the MCT can be operated in a series resonant circuit that is supplied by a power amplifier to effectively emulate power operation. Furthermore, the large-signal validation is done with similar open-circuit primary voltage and short-circuit secondary current as for the ACT, cf. **Section 3.5**. Due to test setup limitations, these are below nominal yet high enough to give sufficient confirmation of operation. Therefore, we use an AE Techron 7224 power amplifier and a series resonant capacitor to supply the MCT. The resonant capacitor C_r is realized as a high-frequency polypropylene capacitor bank (MMKP B32643B) and the series resonance frequency is set to $f_s = 39.6$ kHz for short-circuit and $f_s = 41.5$ kHz for open-circuit tests. The transformer currents are measured with Pearson 110A current probes and a LeCroy HDO4054A 12-bit oscilloscope. The current measurement is subject to a total uncertainty of +2 % / −1 %.

Fig. 4.10(a) shows the result of the test with a secondary-side short-circuit, which reveals a secondary-side rms current of 19.1 A for a primary-side rms current of 19.7 A. This result agrees well with the expected secondary-side current of 19.3 A (for $k = 0.98$ as obtained from the impedance analyzer measurements described above, cf. **Tab. 4.4**).

A second test with open secondary-side winding characterizes the self inductance of the MCT. **Fig. 4.10(b)** presents the measurement results, with a primary-side rms voltage of 2.01 kV, a primary-side rms current of 7.2 A, and a phase shift of 90°. This corresponds to a magnetizing inductance of 1.08 mH, again corroborating the impedance analyzer measurement, see **Tab. 4.4**.

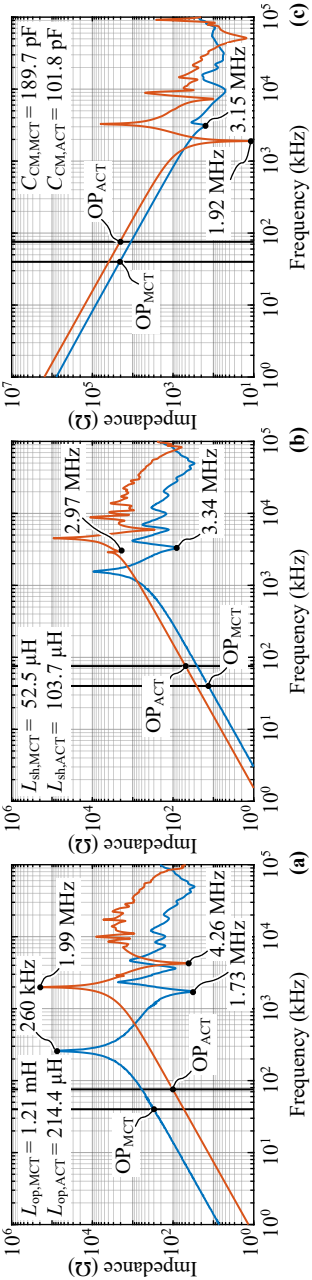
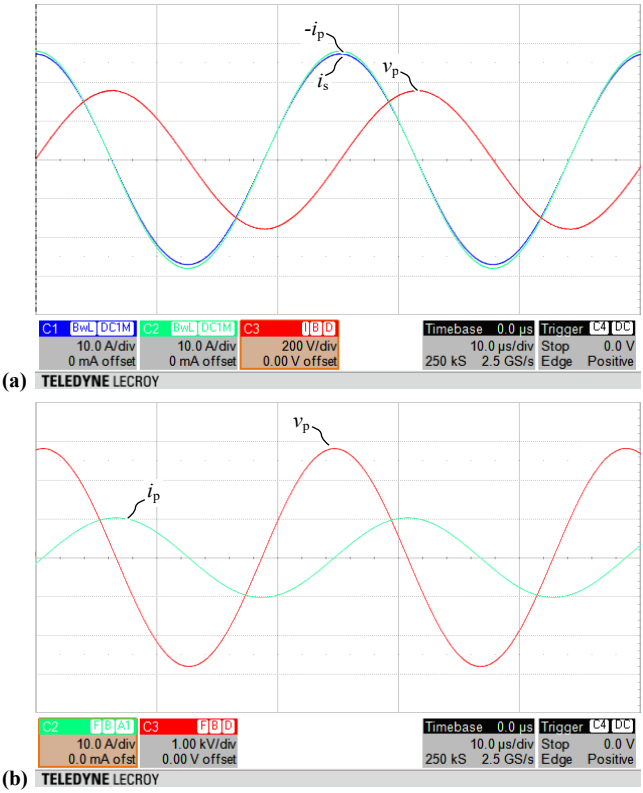


Fig. 4.9: Measured frequency characteristics of selected impedances of the transformers (MCT in blue; for reference, corresponding data for the ACT (w/o shielding) from **Chapter 3** and [96] is shown in red): **(a)** primary-side impedance for open secondary-side winding; **(b)** primary-side impedance for shorted secondary-side winding; **(c)** CM impedance between shorted primary-side and shorted secondary-side windings. The impedance values corresponding to the operating frequencies (40.0 kHz for the MCT, 77.4 kHz for the ACT) are marked (OP).



(a)

(b)

Fig. 4.10: Large-signal voltage and current waveforms of the MCT measured in series resonant operation. **(a)** Secondary-side short-circuit (rms values): primary-side current is 19.7 A, primary-side voltage is 0.25 kV, secondary-side current is 19.1 A, and resonance frequency is 39.6 kHz. **(b)** Secondary-side open-circuit (rms values): primary-side current is 7.2 A, primary-side voltage is 2.01 kV, and resonance frequency is 41.5 kHz.

Tab. 4.5: AC short-circuit resistance of the MCT windings obtained from transient calorimetric measurements at 39.6 kHz and comparison with value obtained from a 3-D-FEM simulation.

Sensor	ΔT (°C)	P (W)	I_p (A)	I_s (A)	R_{AC} (mΩ)	$R_{AC,FEM}$ (mΩ)
Short-circuit						
T1	2.8	15.8			33.4	26.8 (18%)
T2	2.4	14.6	21.8	21.1	30.8	
T3	2.4	14.4			30.5	

4.4.3 Loss Measurements

Winding Losses

We validate the winding loss calculations by measuring the coils' AC resistances. Due to the low expected total AC resistance of the windings (approx. 30 mΩ), we employ the transient calorimetric method presented in [96]: the winding temperatures are measured with several NTC sensors (PS104J2 thermistors) placed in the winding package at the three positions marked with $T_{\{1,2,3\}}$ in **Fig. 4.4(b)**. In a first calibration step, the sensors' temperature responses to accurately measurable DC losses injected into the windings are measured. In a second step, the transformer is operated in AC series resonance (see **Section 4.4.2**) and the corresponding temperature measurements are recorded and translated into losses using the calibration data. Due to the high coupling of the MCT ($k = 0.98$) and as it corresponds to the relevant operation mode of the DCX, the experiments are done for the case of a short-circuited secondary-side winding only. The total AC resistance seen from the primary-side is finally extracted from the measured losses and the measured AC current.

Tab. 4.5 lists the results. Averaging the values obtained based on the three different temperature sensors ($R_{AC,avg} = 31.6$ mΩ), the measured AC resistance is about 18 % higher than the result obtained from 3-D-FEM simulations, i.e., in good agreement. Based on the measured AC resistance the nominal losses in the windings are computed as 105 W (at 130 °C).

Tab. 4.6: Comparison of core losses obtained from experiments (measured Steinmetz parameters and magnetic flux from 3-D-FEM simulation) against the analytical results from the optimization obtained from analytical calculations using datasheet-based Steinmetz parameters of the considered ferrite material (3C94, [119]). Both methods use the iGSE equation.

Param.	Analyt.	Meas.	Deviation
P_{core}	363.5 W	328.4 W	9.6 %

Core Losses

During the optimization, core losses were calculated with the iGSE using manufacturer data (Steinmetz parameters for sinusoidal excitation) and analytically calculated flux densities. The accuracy of this approach mainly depends on the accuracy of the Steinmetz parameters. Therefore, the core loss characteristics of the material considered for the prototype (Ferroxcube 3C94, [119]) has been measured with sinusoidal excitation in a series resonance setup (open-circuit). A sample of two U126/72/20 core halves (without air gap) is placed in a temperature-controlled chamber and equipped with an excitation winding with a series capacitor (to compensate the reactive power) and a sense winding to measure to flux in the core (see **Fig. 4.11(a)**).

Figs. 4.11(b)-(c) present the measured loss density characteristics and **Tab. 4.6** compares the core losses calculated with the measured loss map and 3-D-FEM simulations of the actual flux density in the core of the prototype against the approach used in the optimization (based on analytical calculation of the flux density and datasheet-based Steinmetz parameters). The minor deviation of less than 10 % justifies using the datasheet-based loss map.

4.4.4 Thermal Tests

To verify the thermal feasibility of the MCT, a heat run at the nominal operating point with active cooling (4×12 W) is carried out. We emulate these operating conditions using two independent DC circuits, cf. **Fig. 4.12(a)**. A DC current source is used to impress the nominal winding losses in the series connected windings, whereby the experimentally obtained ratio of AC to DC resistances ($R_{\text{AC}}/R_{\text{DC}} = 1.68$ @ 30 °C) is considered to achieve accurate results. To emulate the core losses, we utilize the electrical conductivity of the bulk ferrite, i.e., we treat the cores as electrical conductors [120, 121]. A closed circuit is formed by appropriately connecting the cores in series and in parallel with conductive silver glue (MG Chemicals 8331) and thin

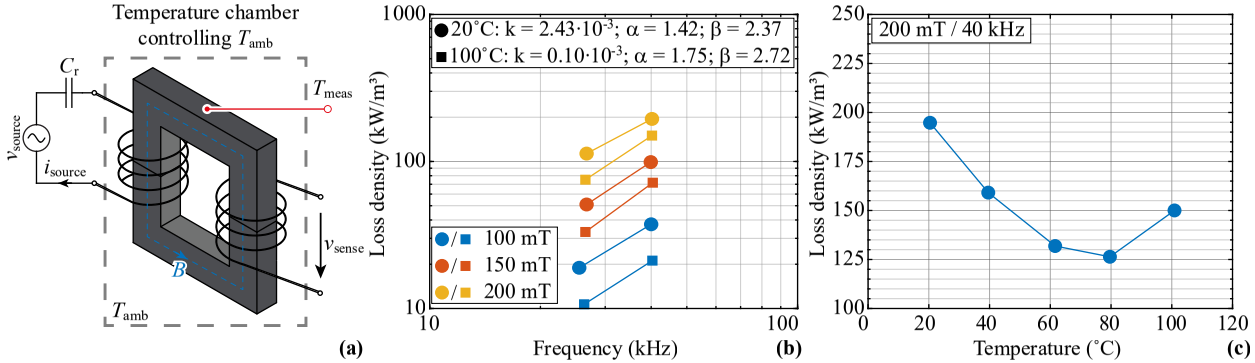


Fig. 4.11: (a) Schematic of the employed setup to extract the loss map of the MnZn ferrite material Ferroxcube 3C94. Loss density: **(b)** vs. frequency for various peak flux densities; **(c)** vs. temperature for the operating parameters of 200 mT / 40 kHz.

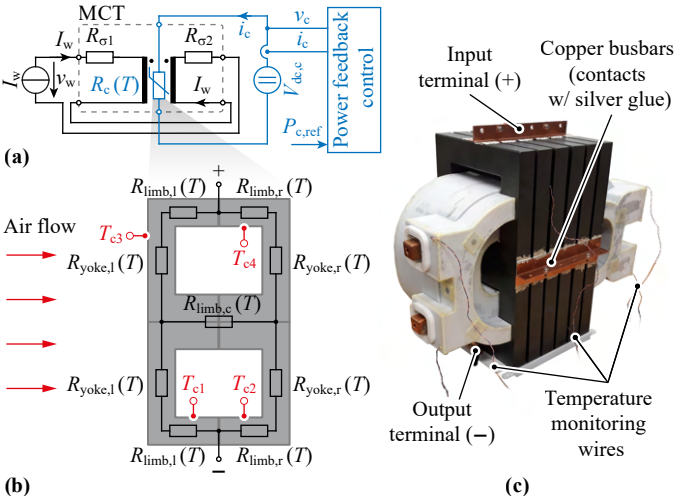


Fig. 4.12: DC-source based injection of winding and core losses for thermal verification. **(a)** Schematic showing the DC current source that impresses a DC current in the windings and the closed-loop controlled DC voltage source that impresses constant core losses. **(b)** Representative electrical network of stacked cores using a simplified model; note that the DC resistance of the ferrite is strongly temperature-dependent. For reference, the placement of PS104J2 NTC thermistors, $T_{c1...c4}$, in the core is shown. **(c)** Photo of the realized electrical connections of all the cores with the use of a conductive silver glue and copper busbars.

copper sheets as shown in **Figs. 4.12(b)–(c)**. Note that the equivalent center limb resistance ($R_{limb,c}$, cf. **Figs. 4.12(b)**) will not see the current flow and effectively can be modeled as an open-circuit. This leads to inhomogeneous distribution of losses within the core volume, and therefore represents the thermal worst-case for the core. Because of the strong inverse dependency of the ferrite electrical resistivity on temperature, the second DC source injecting the core losses operates in a controlled constant-power mode. This is a straightforward approach to test the thermal behavior of the transformer, because only DC power sources and relatively low voltages in the range of hundreds of volts are required.

Fig. 4.13 shows the evolution of measured temperatures during the heat run and thermal images of the prototype taken after reaching the thermal steady-state under nominal operating conditions. Note that the losses injected into the windings are increased by 15 W to account for the dielectric losses

(note that whereas during the optimization a value of 40 W has been used based on [16] (approx. 10% of total losses), we measure much lower dielectric losses in the realized prototype, see **Section 5.3.1**. At an ambient temperature of 25 ℃, the maximum temperature measured with NTC sensors is 54 ℃ for the core and 56 ℃ for the windings, see **Fig. 4.13(a)**, whereas the surface hotspot registered with a FLIR camera reaches 70 ℃ on the core, cf. ① in **Fig. 4.13(b)**. The second image ② in **Fig. 4.13(b)** shows that the surface of the core which is directly exposed to the airflow has a lower surface hotspot temperature of less than 40 ℃. **Fig. 4.13(c)** shows the change of the electrical resistances of the windings and of the ferrite cores during the test. The change of winding resistance allows to estimate the average temperature of the winding based on the copper properties as 63 ℃. This leaves a margin of over 60 ℃ to $T_{\mathrm{max,w}} = 130$℃ (polyamide insulation). Similarly, the core has a temperature rise reserve of $\Delta T = 30$ ℃, as the maximum temperature of the core is defined as $T_{\mathrm{max,c}} = 100$℃ due to the increased losses beyond that value. These margins would allow operation at ambient temperatures of up to 55 ℃ and the low thermal stress can be explained by the targeted high efficiency ($\geq$ 99 %) of the DCX.

Furthermore, the thermal coupling between the winding package and the core is found to be very low. We inject nominal losses in one of the two and measure the temperature rise of the second. The experiments reveal that when the core is under load the average temperature rise of the winding package is only about 6 ℃. Similarly, fully loaded windings yield a rise of the core temperature of only about 1 ℃. This indicates that the MCT may have a very good overload capability, as thus increased winding losses will not give rise to a significant additional temperature increase of the core (which is closer to the temperature limit under nominal conditions). For that reason the overloading capabilities of both MCT and ACT are investigated in **Section 5.3**.

Note that despite the overload capability, passive cooling of the MCT would not be feasible even for partial load due to relatively high losses in the core. In contrast, the ACT can operate with natural convection cooling up to 70 % of the rated power [96].

4.4.5 Insulation and Voltage Withstand Tests

To test the insulation of the transformer, first, the DC insulation resistance between primary and secondary sides, i.e., the common-mode insulation, is measured with an insulation tester (Megger MIT410, DC test voltage of 1.1 kV). The measured insulation resistance is greater than 30 GΩ, which corresponds to a leakage current of less than 235 nA for a voltage of 7 kV.

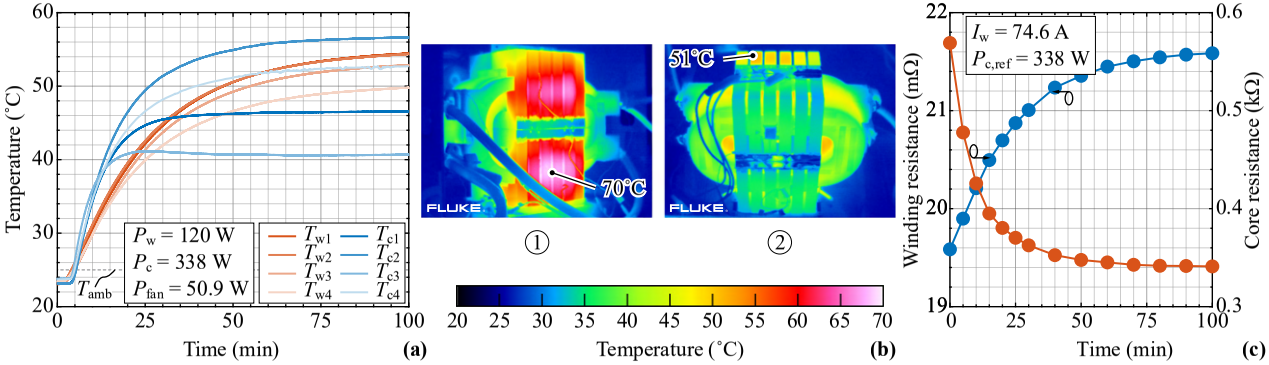


Fig. 4.13: (a) Temperatures measured with eight PS104J2 NTC thermistors ($T_{w1...w4}$ placed in the winding package and $T_{c1...c4}$ in the core) for a nominal load step with nominal cooling. **(b)** Corresponding thermal images with labeled hotspots of the MCT: ① front-side in the steady-state, ② back-side shortly after switching off the sources and cooling, and after removal of the enclosure with fans. **(c)** Measured change of winding and ferrite core DC resistance due to the temperature change; note the negative temperature coefficient of the ferrite DC resistance.

This insulation resistance is more than a hundred times higher than the specified minimum values [64, 65]. Additionally, the same insulation has been successfully tested at higher voltages, with a Schleich GLP2 voltage tester (for 1 min each): +9.6 kV (DC), −9.6 kV (DC), and 6.36 kV (rms) at $f = 50$ Hz. In summary, those tests indicate that the realized prototype withstands the rated insulation voltage.

4.4.6 Magnetic Stray Fields

In order to verify the levels of the magnetic field computed for the nominal operating point and presented in **Section 4.3.2**, the magnetic stray flux densities are measured in the vicinity of the MCT using the field probe and setup presented in [96]. In a first step, the magnetic flux densities are computed with 3-D FEM simulations and results (normalized to 1 A rms) for open-circuit and short-circuit operation are presented in **Figs. 4.14(a)–(b)**, respectively. The simulations confirm that the highest values of magnetic field are in the plane of the air gap. Therefore, the magnetic stray flux densities are measured in this plane and along the symmetry plane given by the x- and z-axis (see **Figs. 4.14(a)–(b)**). Furthermore, in each axis 9 points are selected for the validation.

During the tests, the MCT is operated in a series resonant circuit with a primary-side rms current of 1 A for open-circuit and 4 A for short-circuit at a frequency of 40 kHz. **Figs. 4.14(c)–(d)** present a comparison of normalized (to a current of 1 A) simulated and measured results. The average of the absolute value of the relative deviation between the simulated and the measured results is 10.6 % for an open secondary-side winding. The deviation increases to 32.8 % for the x-axis and to 55 % for the z-axis in case of shorted secondary side as the expected flux densities are low and close to the lower end of the field probe's measurement range. Moreover, it was found that measurements in the range of several µT are challenging due to the residual magnetic fields generated by passive components of the circuits such as the cabling. In order to measure the fields for the case of secondary-side short-circuit with better accuracy, a higher measurement current could be used or alternatively a probe with a higher sensitivity be built. Nevertheless, the obtained results provide sufficient validation of the 3-D-FEM simulations for nominal operation of the MCT presented in **Section 4.3.2**.

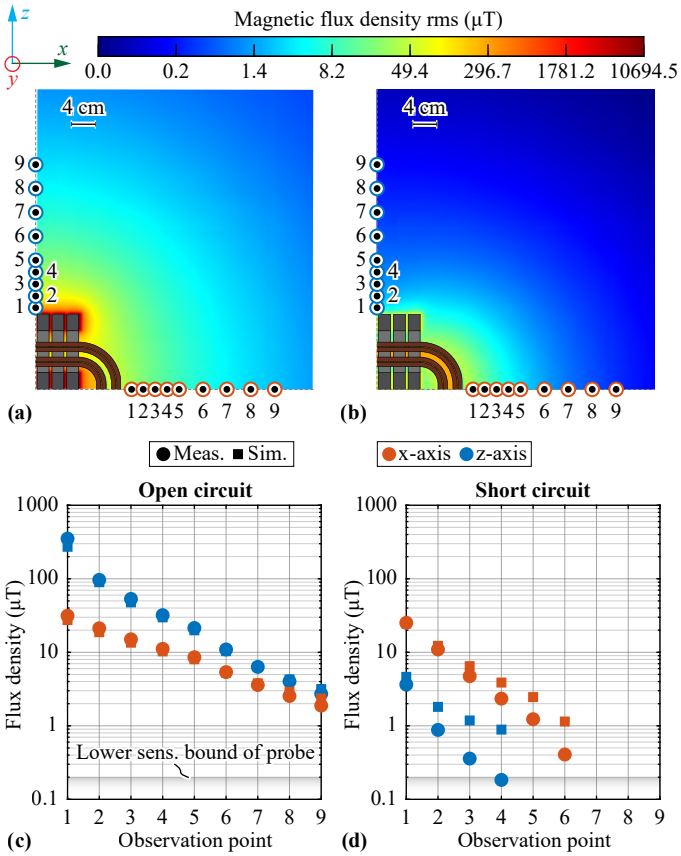


Fig. 4.14: Simulated rms values of the magnetic flux densities in the plane of the air gap for secondary-side **(a)** open-circuit and **(b)** short-circuit. **(c)–(d)** Respective measured and simulated rms values of the magnetic flux densities at the observation points (normalized to a primary-side current of 1 A).

4.5 Conclusion

This chapter quantifies the theoretical performance limits of 166 kW / 7 kV magnetic-core transformers (MCTs) for unity voltage conversion ratio (1:1-DC transformer, 1:1-DCX) application. To derive the performance limits (efficiency, gravimetric power density, and volumetric power density) we

employ a multi-objective optimization and consider air-cooled MCTs with a dry-type (silicone) insulation system. Furthermore, we consider the shell-type winding arrangements with E-core and U-core, and targeting a MF operating range of several 10 kHz we investigate ferrite and nanocrystalline core materials.

With emphasis on a lightweight design, the results of an analytical multi-objective optimization, i.e., η-γ-performance space, show that ferrite E-cores and U-cores achieve similar gravimetric power densities that cannot exceed $\gamma < \approx 9\,\mathrm{kW/kg}$ (cores without cooling channels in between with a conservative airflow velocity of 1 m/s), however with a slight advantage of E-core designs in terms of efficiency. Furthermore, replacing the ferrite cores by nanocrystalline cores (while keeping cooling conditions identical) still allows to reach similar yet not significantly better performance. In this context, for final considerations ferrite E-core MCTs are selected due to ferrite's superior properties (low cost, better availability etc.) and aiming for an actual realization of an MCT prototype, we consider a discrete design space comprising actually obtainable cores and litz wires. With the same boundary conditions as used for the idealized results (analytical design space), the maximum gravimetric power density of designs is limited to $\gamma < \approx 5\,\mathrm{kW/kg}$. To prevent this significant reduction, we insert air channels between the stacked cores, which improves the heat extraction. In order to achieve similar performance as the one resulting from analytical optimization, i.e., $\gamma \approx 10\,\mathrm{kW/kg}$, the airflow has to be increased to still moderate 5 m/s.

To validate the employed models and theoretical analysis, one design of a shell-type MCT consisting of an E-core with concentric windings encapsulated in silicone insulation is selected for realization. A full-scale MCT prototype which features a nominal insulation voltage of 10 kV with clearance and creepage distances realized according to IEC 62477 is experimentally characterized in detail. The MCT prototype (6.7 kW/kg, 5.4 kW/dm^3), operated at 40.0 kHz, reaches a measured efficiency of 99.7 %. Furthermore, the measurements of the magnetic stray flux in the proximity of the MCT reveal that the MCT prototype does not require additional shielding, as stray fields decay below the limits already geometrically relatively close to the MFT (250 mm), a distance which is a reasonable clearance to maintain in MV systems.

5

Component-Level and System-Level (ACT- and MCT-DCX) Performance Evaluation

This chapter summarizes the major research findings also published in:

- **P. Czyz**, T. Guillod, D. Zhang, F. Krismer, J. Huber, R. Färber, C. M. Franck and J. W. Kolar, "Analysis of the Performance Limits of 166 kW / 7 kV Air-Core and Magnetic-Core Medium-Voltage Medium-Frequency Transformers for 1:1-DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2021.

Executive Summary

It has been shown that air-core transformers (ACTs) are serious competitors of the conventional magnetic-core transformers (MCTs) and are well suited for a series-resonant DC-DC converter acting as a DC transformer (DCX) with equal input and output MV DC voltages of (1:1-DCX), particularly in emerging applications for which robustness, weight, serviceability and cost-effective manufacturing of the transformer are of high importance. However, a direct comparative evaluation of the ACTs and MCTs, and the corresponding DCXs (i.e., ACT-DCX and MCT-DCX) remains unclear. Therefore, in this chapter component-level and system-level performance limits of realizations with either an ACT or with an MCT for a 166 kW / 7 kV 1:1-DCX are presented. For the selected designs of DCXs, **Chapter 3** and **Chapter 4** present the transformers and their experimental validation, therefore in this chapter, the realization of the remaining DCX components is described, i.e., resonant capacitor bank and switching stages with DC-link capacitors. Additionally, an extension of the experimental characterization of MFTs is provided focusing on the dielectric losses, long-term overload capability and partial discharge (PD) measurements. Finally, considering 10 kV SiC MOSFETs, calculated system-level efficiencies of the ACT-DCX and MCT-DCX result in 99.0 % and 99.2 % at the nominal operating point, with similar part-load efficiency characteristics. The achieved power densities are 9.7 kW/kg and/or 2.0 kW/dm^3 for the ACT-DCX and 5.6 kW/kg and/or 4.5 kW/dm^3 for the MCT-DCX. The chapter concludes with an application-oriented qualitative evaluation of the two concepts.

In **Chapter 3** and **Chapter 4** the details of modeling and optimization of the ACT and MCT are discussed which are the core part of the 166 kW / 7 kV 1:1-DCX. Furthermore, the design, construction and basic experimental characterization of two fully rated MFT prototypes, i.e., ACT and MCT, are presented. However, a direct comparative evaluation of the MFTs and the corresponding DCXs remains unanswered. Hence, this chapter presents a comparative evaluation of the investigated ACT-DCX and MCT-DCX on a component- and system-level. First, the results of multi-objective optimizations are compared and discussed in detail. Next, the remaining parts of the DCXs are addressed, i.e., the constructed resonant capacitor banks are shown and the realization of the switching stages with DC-link capacitors is discussed. This is followed by an experimental comparison of selected aspects of the ACT and MCT prototypes, i.e., examination of dielectric losses, especially the influence of initial environmental conditioning on the dissipation factor of the silicone insulation, long-term overload capability and partial discharges (PDs) measurement. Finally, the system-level performance of the ACT-DCX and MCT-DCX is shown. In particular, the focus is on the breakdowns of masses, volumes, and losses, partial-load efficiency, and a qualitative application-oriented evaluation.

5.1 Multi-Objective Optimization Results

Fig. 5.1 and **Fig. 5.2** show the η-γ-ρ-performance spaces and thus unveil the performance limits of the optimized ACT and MCT and of the overall ACT- and MCT-1:1-DCXs. On the system level, the η-γ-performance planes from **Fig. 5.1** show that the MCT-DCX cannot achieve a power density of more than 7.5 kW/kg due to thermal limitation of the MCT. In contrast, the ACT-DCX can achieve twice the gravimetric power density, i.e., up to 16 kW/kg, while maintaining a lower but still comparably high DC-DC efficiency of 98.9 %. It is worth to point out that even though there are highly efficient ACT designs (99.7 %, cf. **Fig. 5.1(a)**), a high operating frequency up to 200 kHz is required. As this leads to high switching losses of the SiC MOSFETs, those designs have poor system-level performance (cf. **Fig. 5.1(b)**). Similarly, the higher maximum system-level efficiency of the MCT-DCX follows from the lower operating frequencies and lower magnetizing current of typical MCTs.

The picture reverses when considering the volumetric power density: **Fig. 5.2(a)** reveals that on the component level, the ACT is limited to $\rho < \approx 19.5\,\mathrm{kW/dm^3}$, and more compact realizations (up to $26\,\mathrm{kW/dm^3}$) can be achieved with the MCT. This trend is even more pronounced on the system-

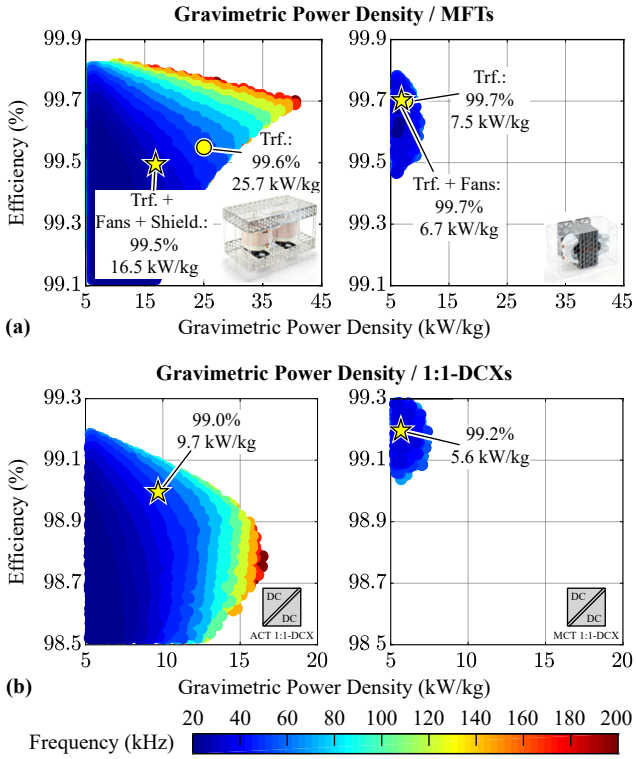


Fig. 5.1: Results of the multi-objective optimization of the ACT- and MCT-based 166 kW / 7 kV 1:1-DCX. Efficiency vs. gravimetric power density on: **(a)** the component-level (ACT and MCT) and **(b)** the system-level (ACT-DCX and MCT-DCX). The markers ○ represent the selected designs and the markers ☆ indicate measured results of the actually realized MFT prototypes (f_s = 77.4 kHz for the ACT; f_s = 40.0 kHz for the MCT). Note that the performance deviations from the optimization results exist because of additional constructive constraints and because the idealized models did not yet include weight and volume of the cooling system (fans) and of the aluminum conductive shielding of the ACT.

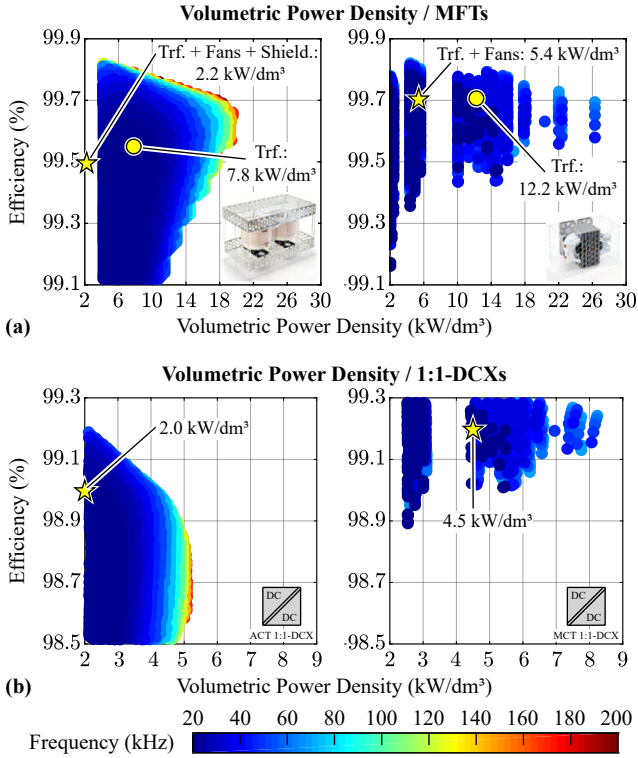


Fig. 5.2: Results of the multi-objective optimization of the ACT- and MCT-based 166 kW / 7 kV 1:1-DCX. Efficiency vs. volumetric power density on: **(a)** the component-level (ACT and MCT) and **(b)** the system-level (ACT-DCX and MCT-DCX). The markers ○ represent the selected designs and the markers ☆ indicate measured results of the actually realized MFT prototypes (f_s = 77.4 kHz for the ACT; f_s = 40.0 kHz for the MCT). Note that the performance deviations from the optimization results exist because of additional constructive constraints and because the idealized models did not yet include weight and volume of the cooling system (fans) and of the aluminum conductive shielding of the ACT.

level, for which **Fig. 5.2(b)** indicates maximum volumetric power densities of 8.2 kW/dm^3 for the MCT-DCX compared to 5.2 kW/dm^3 for the ACT-DCX. In addition, note that these results do not yet include a shielding enclosure of the ACT (see **Section 4.3.2**), which would significantly increase the overall boxed volume. This can also be seen from the two markers that indicate the predicted performance of the selected designs and the actually measured values of the realized MFT prototypes.

Finally, **Fig. 5.1(b)** and **Fig. 5.2(b)** show the selected 1:1-DCXs designs (indicated with a ☆), i.e., an ACT-DCX (99.0 %, 9.7 kW/kg, 2.0 kW/dm^3) and MCT-DCX (99.2 %, 5.6 kW/kg, 4.5 kW/dm^3). For a detailed evaluation of those systems see **Section 5.4**.

5.2 DCX Components

As mentioned before, the realization of MFTs is shown in detail in **Chapter 3** and **Chapter 4**. In this section, the realization of remaining parts of the selected 1:1-DCXs, indicated with a ☆ in the performance spaces obtained from the optimizations in **Fig. 5.1** and **Fig. 5.2**, is presented. First, the constructed resonant capacitor banks are shown and next the realization of required switching stages with DC-link capacitors is discussed.

5.2.1 Resonant Capacitor Banks

As discussed earlier, the required series resonant capacitance must compensate the transformer's leakage inductance at the target operating frequency, i.e., $C_\mathrm{r} = 1/((2\pi f_\mathrm{s})^2 L_\sigma)$. Thus, we obtain $C_\mathrm{r} = 41\,\mathrm{nF}$ for the ACT and $C_\mathrm{r} = 300\,\mathrm{nF}$ for the MCT.

In case of the MCT, the resulting peak resonant capacitor voltage of 1.0 kV facilitates a compact realization on one side of the transformer, using ceramic COG capacitors (4 series × 12 parallel CGA9 100 nF), see **Fig. 5.3(a)**. The designed PCB offers the flexibility to configure a large number of individual capacitors in a series-parallel arrangement. It is therefore not optimum in terms of size, yet its volume and mass are still negligible compared to the MCT.

In contrast, the peak capacitor voltage in case of the ACT would reach 4.0 kV if a single component were used. Therefore, to reduce the component stress and facilitate meeting the necessary clearance and creepage distances, we split C_r into two capacitor banks $C_{\mathrm{r}1} = C_{\mathrm{r}2} = 82\,\mathrm{nF}$ that are placed on either side of the transformer (cf. **Section 3.3**). Still, the capacitors process high

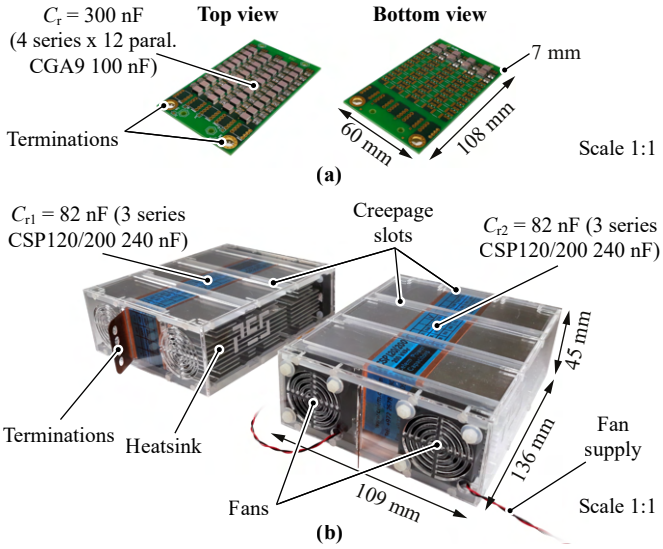


Fig. 5.3: Photos of the realized resonant capacitor banks: **(a)** C_r for the MCT; **(b)** C_{r1} and C_{r2} for the ACT. Note that due to lower reactive power and hence losses, the ceramic capacitors (C_r for the MCT) do not require active cooling.

reactive power and high currents. Therefore, we realize them with polypropylene capacitors (each with 3 series-connected 240 nF CELEM CSP120/200). Since the expected losses are substantial (see **Section 5.4.1** for the discussion of losses), they require a cooling system consisting of heatsinks and fans as shown in **Fig. 5.3(b)**. The cooling system is optimized to minimize the mass according to [122], whereas the thermal modeling of capacitors is based on [55]. The contribution to the overall volume and mass is clearly higher compared to the capacitor bank required for the MCT-based system.

5.2.2 Switching Stages and DC-link Capacitors

Each switching stage consists of a MOSFET half-bridge and two DC-link capacitors (C_{DC}). Note that these switching stages actually were not built due to the associated high cost and limited availability of the 10 kV switches, and because of the limited additional insights with respect to the MFTs that could be gained. Nevertheless, the volume, mass and losses of their components can be reliably estimated based on the models discussed above and earlier prototype systems [16].

The required capacitance C_{DC} is 1.3 µF and 2.3 µF for the ACT- and MCT-DCX, respectively, and it is obtained based on the specified maximum peak-peak voltage ripple, see **Tab. 2.2**. The difference follows from the two different switching frequencies of 77.4 kHz and 40 kHz, respectively.

Note that because of the higher operating frequency and also because of the higher rms current in case of the ACT-DCX, the switching stages require a higher total chip area (more dies in parallel per switch). Consequently, 6 parallel dies (3 packages) are needed for the ACT-DCX, whereas 4 parallel dies (2 packages) are sufficient for the MCT-DCX.

5.3 Experimental Comparison of ACT & MCT

The basic experimental characterizations of the MV/MF ACT and MCT prototypes shown in **Fig. 4.8** have been presented in **Chapter 3** and **Chapter 4**, respectively, and **Tab. 4.3** summarizes the key characteristics. This section extends the provided experimental analysis of the realized transformers by a detailed comparative experimental evaluation of dielectric losses, the overload capability and partial discharges measurements.

5.3.1 Dielectric Losses

Dielectric losses can contribute a non-negligible share of total MFT losses in case of dry-type insulation systems [43]. Therefore, we provide an experimental verification of the corresponding assumptions made during the optimization. The dielectric response of the employed insulation materials is linear with the electric field in the range of practically relevant field strengths (at most some kV/mm). Therefore, the dielectric losses of the constituting materials can be measured with small-signal excitations [43], and 3-D FEM electric field simulations can be employed to compute the dielectric losses of the transformer assembly. For validation, we then provide also measurements of the dielectric responses of the entire transformer assemblies and compare them to the results obtained by the FEM-based calculation. For all dielectric response measurements, a setup consisting of a Novocontrol Broadband Dielectric Spectrometer with an Alpha-A High Performance Frequency Analyzer [123] is used.

First, we measure the frequency-dependent dielectric responses of the insulation/construction materials employed in the ACT and MCT prototypes: silicone TC4605 HLV (dry-type insulation), polycarbonate (coil formers), aramid polymer Nomex (spacers and barriers), and PMMA (mechanical supports). **Fig. 5.4(a)** shows the measurement cell with an exemplary sample and **Fig. 5.4(b)** gives the results. Note that the samples have been stored under room conditions (22℃ and 45 % relative humidity (RH)) before the measurements. **Tab. 5.1** summarizes the dissipation factors and the dielectric constants extracted for the considered frequency range ($40 - 80$ kHz). Using these parameters in a 3-D-FEM simulation of the electric fields in the dielectric materials of the MCT and of the ACT yields the dielectric losses, CM capacitances and total dissipation factors given in **Tab. 5.2(a)**. Note that we consider two values for the dissipation factor of silicone (minimum and maximum) to account for environmental and temperature effects, which will be discussed shortly. The high-field region in the MCT (inter-winding space, cf. **Fig. 4.5(a)**) is mainly filled with dry-type insulation, thus the silicone accounts for up to 95 % of the MCT's total dielectric losses, leading to a worst-case total dissipation factor $\tan\delta_{\mathrm{MCT}} \approx 1.0\%$. On the other hand, as expected, the dielectric losses of the ACT can be neglected as $\tan\delta_{\mathrm{ACT}} \approx 0.1\%$. Lastly, the computation of the CM capacitances shows very good agreement with the small-signal impedance measurements presented earlier (< 9 %, cf. **Fig. 4.9(c)**).

As the dielectric losses of the ACT can be neglected, only the dielectric response of the entire MCT is measured. **Fig. 5.4(c)** shows the measured dissipation factor of the MCT, which was stored at room conditions (22℃,

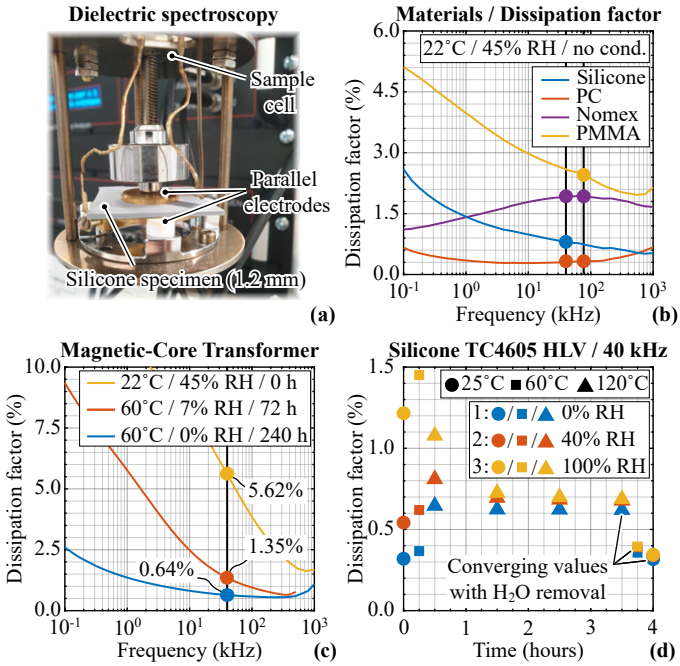


Fig. 5.4: (a) Photo of the dielectric spectrometry setup with an exemplary material specimen (silicone, thickness of 1.2 mm) placed in the sample cell. **(b)** Frequency characteristic of the dissipation factors of the construction/dielectric materials used for the realization of transformers (at 22℃, 45% RH, w/o conditioning). **(c)** Measured dissipation factor of the entire MCT stored in different conditions prior to the measurement: 22℃, 45% RH (w/o conditioning); 60℃, 7% ambient RH (cond. 72 hours); 60℃, 0% RH (cond. 240 hours). **(d)** Time evolution of the measured dissipation factors of three silicone specimens stored in different environments before the test under the indicated heating protocol (25℃ → 60℃ → 120℃ (3 hours) → 60℃ → 25℃).

Tab. 5.1: Measured dielectric properties of the materials employed in the MFT prototypes (valid for operating frequencies in the range of 40 – 80 kHz, at 25℃ and 45% relative humidity).

Material	**Diel. constant** ε_r	**Diss. factor** tanδ
Silicone	4.1	0.8 %
PC	2.7	0.3 %
Aramid polymer (Nomex 993)	3.2	1.9 %
PMMA	3.0	2.4 %

45 % RH) prior to the test. At 40 kHz we measure $\tan\delta_{MCT} = 5.6\%$, which is surprisingly high compared to the value computed by the 3-D-FEM simulation ($\tan\delta_{MCT} \approx 1.0\%$) using the dissipation factors measured for the individual material samples. Since the behavior of the silicone dominates $\tan\delta_{MCT}$, we further investigate the influence of the initial environmental conditioning (namely the impact of water ingress into the polymer during storage) on the dissipation factor of the silicone.

Therefore, three silicone specimens of 1.2 mm thickness are prepared and conditioned in environments with different relative humidity after first exposing them for 4 hours to a temperature of 120℃ in an atmosphere of dry air, which ensures equal initial conditions by erasing the effects of previous tests. Afterwards, the following conditioning procedures were applied:

- Sample 1: stored for 20 hours at 120℃ and 0% RH (in N_2 atmosphere).
- Sample 2: stored for 2 weeks at 25℃ and 40% RH.
- Sample 3: stored for 2 weeks at 25℃ and 100% RH (non-condensing).

Then, the dissipation factors of all samples are measured in the same chamber during a heating cycle consisting of a temperature ramp from 25℃ to 120℃, 3 hours conditioning at 120℃, and a ramp down back to 25℃. The results are presented in **Fig. 5.4(d)**. It can be seen that the initial dissipation factor depends strongly on the initial relative humidity of the sample and ranges from 0.3 % (sample 1) to 1.2 % (sample 3). During the first part of the heating sequence, two opposing effects are active simultaneously: the increased sample temperature causes an increase of the dissipation factor for a given water content [124], while the initiated removal of moisture decreases it. The

measurements confirm that in all cases the exposure to a higher temperature over some hours removes moisture from the samples by thermal diffusion. Indeed, towards the end of the heating sequence, the dissipation factors of all samples converge to approximately 0.3 %. This equals the initial value for sample 1, which suggests almost complete removal of any residual moisture.

In light of these results, the MCT was conditioned by placing it in an oven (natural convection) for a total of 72 hours. The temperature was regulated to 60°C at RH of 7 % (which corresponds to RH of 45 % at room temperature). **Fig. 5.4(c)** shows that the dissipation factor of the MCT is still relatively high compared to the computed value (1.4 % vs. 1.0 %). To further reduce the moisture content of the insulation, the MCT was placed in the oven at 60°C with a dry purge airflow (absolute and relative humidity close to 0%) for a total of 240 hours. As expected, the measured value of $\tan\delta_{\mathrm{MCT}} = 0.64\%$ (cf. **Tab. 5.2(b)**) matches the result obtained above for the silicone samples at 60°C towards the end of the heating sequence[1] ($\tan\delta_{\mathrm{silicone}} \approx 0.4\%$, cf. **Fig. 5.4(d)**).

These results highlight the important impact of the initial environmental conditioning on the dissipation factor of dry-type MFTs with silicone insulation, and hence on the dielectric losses. Depending on the initial moisture content of the silicone, the dielectric losses can initially be several times higher than what would be expected from values obtained from a "dry" transformer (e.g., after operating for several hours in thermal steady state). This worst-case scenario should be considered during the design, e.g., by taking into account a range (min./max.) for the dissipation factor instead of a single value (see **Tab. 5.2(a)**).

5.3.2 Long-Term Overload Capability

The heat runs with losses corresponding to the nominal output power (cf. **Section 3.5.5** and **Section 4.4.4**) reveal that the steady-state temperatures of the MCT and the ACT leave significant margins with respect to the maximum allowable values. In case of the MCT, this can be explained by the fact that the loss penalty factors included in the design (for winding and core losses) were too conservative. Therefore, the realized cooling system enables operation of the transformer at lower temperatures than designed for. Furthermore, the airflow at the air inlet of the MCT enclosure was measured with an airflow meter. Due to very turbulent nature of the airflow in the enclosure, locally

[1] Considering that 95 % of the total dielectric losses in the MCT occur in the silicone.

Tab. 5.2: FEM-simulated dielectric losses, CM capacitances and dissipation factors of MFTs. Comparison with measurement results obtained with dielectric spectrometer.

(a) Sim. param.	**MCT**		**ACT**
	Min.	Max.	
Silicone tanδ	0.4 %	1.2 %	
Losses			
Silicone	3.61 W	10.83 W	–
Coil formers (PC)	0.40 W	0.40 W	0.44 W
Spacers / barriers (Nomex)	0.02 W	0.02 W	0.77 W
Supports (PMMA)	–	–	0.69 W
Total	4.0 W	11.2 W	1.9 W
CM capacitance	187.6 pF		111.2 pF
Dissipation factor	0.35 %	0.97 %	0.14 %
(b) Meas. param.			
CM capacitance	161.1 pF		106.8 pF
Dissipation factor	0.64 %	5.62 %	–

the airflow speed reaches up to 9 m/s, which is almost twice the assumed value of 5 m/s, further improving the performance of the cooling system.

Similarly, the simplified thermal model of the ACT is based on a surface related-loss density of $p_{v,max} = 0.25$ W/cm^2), an assumption which has been found to be too conservative, too, because [96] demonstrates that $p_{v,max} = 0.30$ W/cm^2 is achievable. Additionally, the analysis of the temperature gradient along the circumference of the coils shows that due to the mismatch of the fan and coil diameters (with fans being smaller, cf. **Fig. 3.6(b)**), the outer parts of the windings are not situated in the direct airflow, leading to local hot-spots. For this reason, we place air ducts to guide the airflow along the whole circumference of the coils, thus potentially unlocking operation with even higher surface-related loss densities.

To evaluate the overload capability, we carry out heat runs with losses that correspond to operation at higher-than-nominal power. The maximum temperatures that must not be exceeded once steady-state is attained are defined as $T_{hs,c} = 100$℃ (hotspot in the core), $T_{hs,w} = 105$℃ (hotspot in the winding), $T_{avg,w} = 95$℃ (maximum average winding temp.) for the ambi-

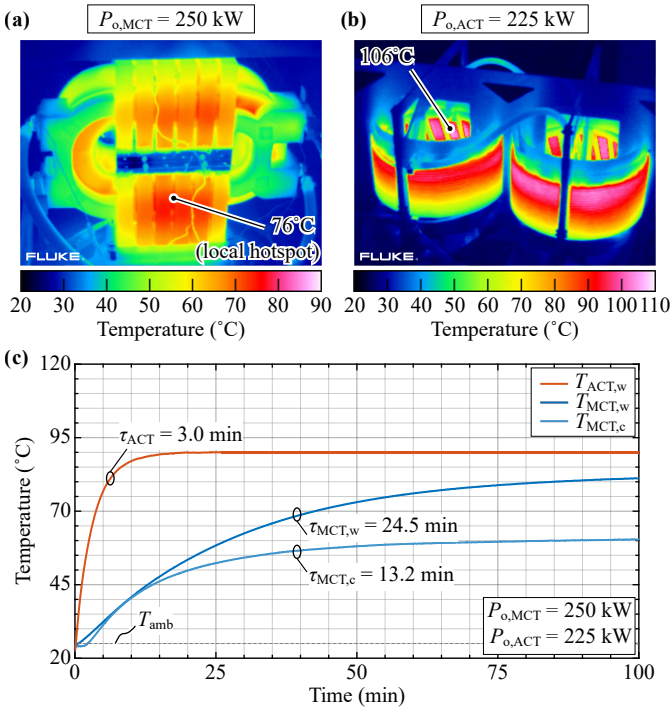


Fig. 5.5: Thermal images of the transformers in the thermal steady-state at maximum overload with (surface) hotspot temperatures indicated: **(a)** MCT with losses corresponding to operation at 250 kW, **(a)** ACT with losses corresponding to operation at 225 kW. **(c)** Maximum temperatures measured with NTC thermistors ($T_{ACT,w}$: windings of the ACT; $T_{MCT,w}$ and $T_{MCT,c}$: windings and core of the MCT, respectively) during the corresponding overload heat runs.

ent temperature of 25℃. **Figs. 5.5(a)–(b)** show the thermal images of the transformers operated with losses that correspond to the maximum possible overload power and **Fig. 5.5(c)** presents the evolution of maximum measured temperature waveforms during the corresponding heat runs. The results show that the MCT can be operated with a power transfer of up to 250 kW (P_w = 249W, P_c = 340W, P_{fan} = 48W), whereas the ACT can reach 225 kW (P_w = 1281W, P_{fan} = 48W). The average winding temperatures are 94.2℃ and 90.3℃ for the MCT and ACT, respectively (at 25℃ ambient). Furthermore, in the overload test the ACT achieves a surface-related winding loss density of $p_{v,max}$ = 0.47 W/cm^2. Note that for long-term overload operation in industrial environments, it would be preferable to use litz wires of higher temperature class than the ones used in the prototypes (V155).

Finally, the thermal time constants can be extracted from **Fig. 5.5(c)** as 13.2 min for the core and 24.5 min for the MCT's winding package, in contrast to 3.0 min for the ACT. With this, it can be concluded that the MCT's short-term overload capability (< 10 min) is significantly higher than that of the ACT because of the approximately 8 × longer thermal time constant of the windings. Note that the thermal coupling from windings to the core is relatively weak, therefore the time constant of the core is unimportant for this consideration.

5.3.3 Partial Discharges Measurement

During the nominal conditions, MFTs should be free of partial discharges to prevent accelerated insulation ageing and reduced breakdown voltages. The critical impact of MF PWM voltages on partial discharges has been highlighted in many publications [64, 124–126], however, the measurement of partial discharges is a complex process and the interpretation of the partial discharge patterns requires empirical knowledge, which is not yet available for MFTs. In this regard, we measure only partial discharge activity with LF AC voltages.

Fig. 5.6(a) shows the schematic of the partial discharge (PD) measurement setup. It consists of a low-frequency (50 Hz) step-up transformer (LFT), capacitive voltage divider, low-pass filter and device under test, i.e., the MV/MF transformer. The partial discharges are measured with the optically isolated high-end measurement and analysis system MDP600 from Omicron which is connected to a low-voltage (LV) partial discharge impedance (PDZ). The setup is controlled through the PC and programmable LV source. **Fig. 5.6(b)** presents the photo of the physical setup and the ACT prototype prepared for testing. The PDs are measured according to the standard IEC 62477 [59, 60] and an exemplary measured voltage ramp is presented in **Fig. 5.6(c)**. Accord-

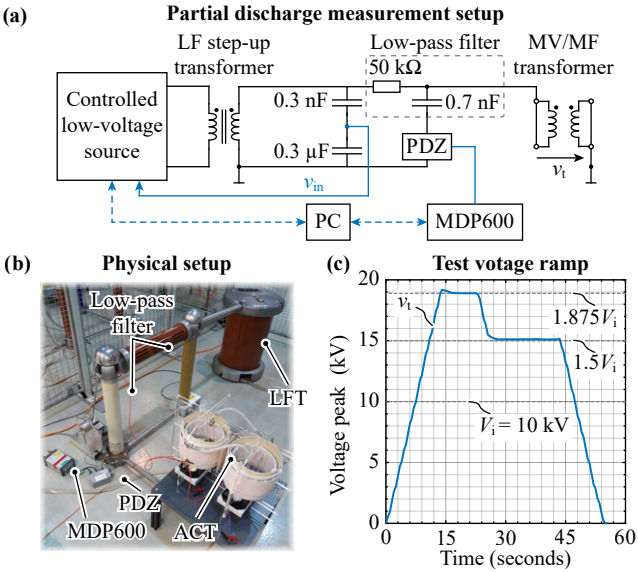


Fig. 5.6: Partial discharges measurement setup: **(a)** schematic, **(b)** photo with the ACT connected for the test. **(c)** Example of a measured waveform of the test voltage ramp applied to the ACT (scaled by the voltage divider's ratio, front 19.0 kV peak, back 15.1 kV peak).

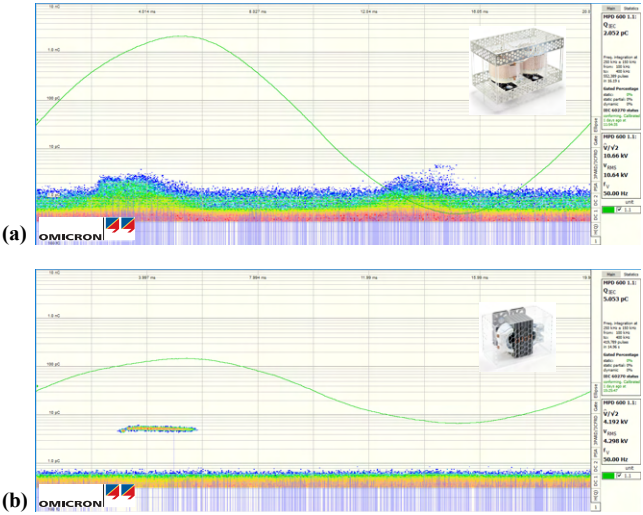


Fig. 5.7: Results of partial discharge measurements using the MDP600: **(a)** ACT (front 19.0 kV peak, back 15.1 kV peak), **(b)** MCT (front 7.9 kV peak, back 6.3 kV peak).

ing to the standard, during the test, the peak voltage v_t reaches $1.875V_{iso}$ for 5 s, and afterwards is reduced to $1.5V_{iso}$ for 15 s. The voltage rate of change is set to 1 kV/s (rms).

Results of the PD measurements are presented in **Fig. 5.7**. According to the standard IEC 62477, the partial discharges shall remain below the 10 pF level, hence for the evaluation of critical PD levels, a stringent criterium that amplitudes of all discharge events shall remain below the 10 pF value is used. This is in contrast to the commonly used average value of capacitance as calculated, e.g., by default by the MDP600 based on IEC 60270. The ACT passes the PD test at 10.7 kV rms (15.1 kV peak) for the rated insulation voltage of V_{iso} = 10 kVDC, whereas the MCT can reach PD-free operation only up to 4.2 kVDC which results from the test at 6.3 kV peak.

Further measurements indicate that the PDs in the MCT occur in the winding package (test without the core), however, due to its closed structure, i.e., winding and silicone are enclosed in a plastic mold, it is impossible to locate the source of the PDs, e.g., with an ultrasonic imaging camera. In order, to identify the source of PDs, further basic studies of PDs development in windings potted with the same technology and materials are required.

5.4 System-Level 1:1-DCX Performance Evaluation

The initial Pareto optimizations and the extensive experimental analyses of full-scale ACT and MCT prototypes provide a solid basis for a concluding quantitative system-level performance comparison of the ACT- and MCT-based 1:1-DCX, and finally a qualitative application-oriented evaluation.

5.4.1 System-Level Performance of ACT- and MCT-DCX

The actually realized transformer prototypes and the corresponding 1:1-DCXs are indicated with a ☆ in the performance spaces obtained from the optimization in **Fig. 5.1** and **Fig. 5.2**. **Fig. 5.8** shows the breakdowns of masses, volumes, and losses of the components employed in the two 1:1-DCX designs. The values for the two transformers and for the resonant capacitor banks are measured as described above, whereas the remaining data follows from the modeling used for the Pareto optimization (see **Chapter 2**); note that the calculation of the MOSFET masses, volumes and losses relies on experimental data from [38, 39]. Therefore, all important contributions to mass, volume, and losses of the two systems are backed by experimental results, which enables a realistic comparison.

The mass breakdown (see **Fig. 5.8(a)**) shows that the mass of the MCT accounts for about 84 % of the total converter's mass with the core alone contributing 45 %. In addition, also the dry-type insulation increases the overall weight considerably. Interestingly, the weights of windings and coil formers are very similar for both transformers. Due to the low copper mass of the ACT, the realization of mechanical parts such as coil formers, supports, and fixtures becomes important, as they account for more than 55 % of the ACT's total mass. On the other hand, the capacitor bank for the MCT-DCX can be realized as a PCB with COG ceramic capacitors of almost negligible mass, which represents a clear advantage over the ACT-DCX that requires high-power capacitors with a dedicated cooling system consisting of heatsinks and fans, which ultimately contributes more than 14 % of the converter's total mass. Overall, the ACT-DCX features a gravimetric power density of $\gamma = 9.7\,\mathrm{kW/kg}$, whereas the MCT-DCX achieves $\gamma = 5.6\,\mathrm{kW/kg}$.

Not considering the ACT's shielding, its boxed volume is still 56 % larger than the MCT's, see **Fig. 5.8(b)**. Nevertheless, the ACT itself achieves a rather high volumetric power density of $7.8\,\mathrm{kW/dm^3}$. However, the overall converter volume is dominated by the volume of the shielding enclosure

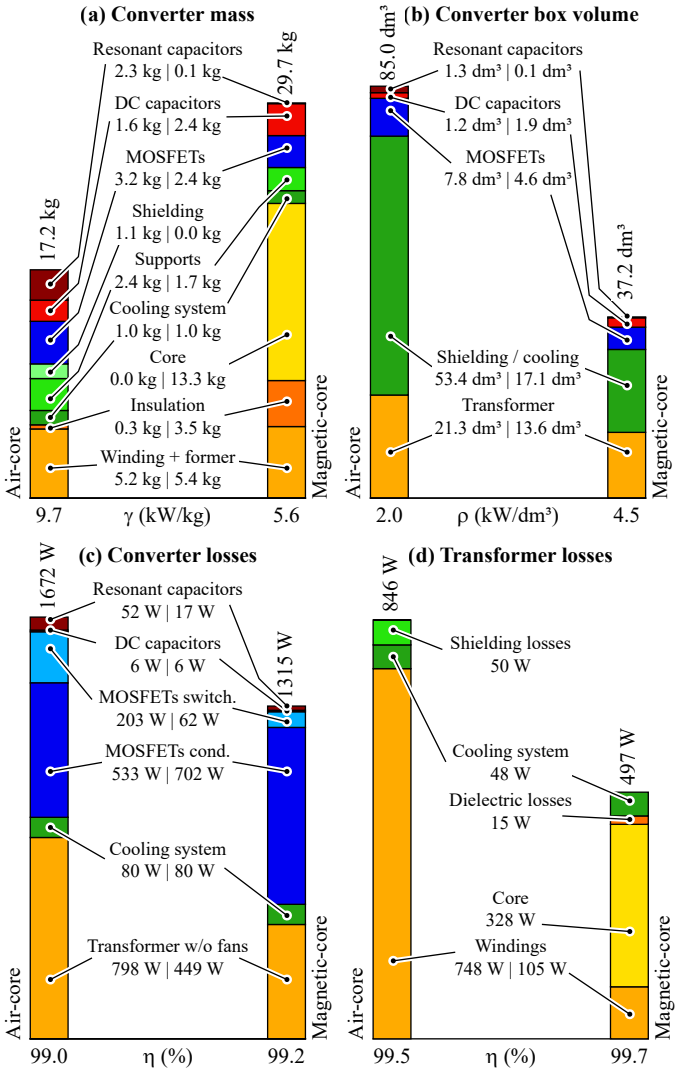


Fig. 5.8: Breakdown of the **(a)** masses, **(b)** volumes, **(c)** losses of the components employed in the ACT-based and MCT-based 166 kW / 7 kV 1:1-DCX designs. **(d)** Measured transformers losses including losses for the cooling system.

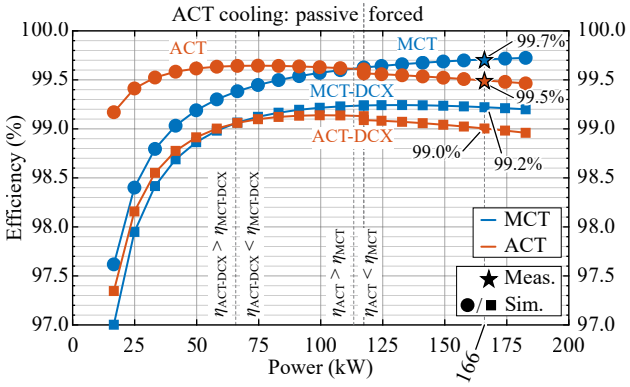


Fig. 5.9: Measured (★) and simulated (● / ■) efficiencies of the transformers and the complete 1:1-DCXs (MCT-based in blue, ACT-based in red).

around the ACT. Therefore, the MCT-DCX is significantly more compact and features a 2.2 × higher volumetric power density. Note that the shielding enclosure of the ACT could be much more compact, however, with a trade-off of increased losses (in the built prototype the objective was to obtain marginal losses in the shielding)[2].

The breakdown of the converters' losses at nominal power (see. **Fig. 5.8(c)**) shows that the total semiconductor losses are almost equal for both solutions (764 W for the MCT-DCX vs. 736 W for the ACT-DCX) even though the switched/conducted currents and the switching frequencies are higher in the ACT-DCX. It is important to highlight that this is achieved by employing more chip area in the ACT-DCX, i.e., a total of 6 paralleled dies (3 packages) are used compared to only 4 parallel dies (2 packages) in case of the MCT-DCX. Therefore, the realization of the half-bridges of the ACT-DCX switching stages is more complex (gate driving circuitry) and especially significantly more expensive, in addition to requiring a bulkier cooling system that is reflected in the increased mass and volume, cf. **Fig. 5.8(a)–(b)**. On the system level, with 99.2 % efficiency the MCT-DCX achieves a slightly higher DC-DC efficiency at nominal load than the ACT-DCX (99.0 %); the quite different efficiency characteristics at partial-load operation will be discussed below.

Fig. 5.8(d) provides detailed insight into the transformer loss components. The majority of MCT's losses are core losses (about 73 %). This is a characteristic of the weight-optimized design, as it is much easier to extract the heat

[2]Furthermore, no shielding is considered for the MCT.

from the stacked cores with air channels in between compared to extracting losses from the potted winding. Furthermore, relatively high core losses are a consequence of selecting a design with rather high magnetic flux densities, which reduces the necessary core cross section and thus reduces its mass. The ACT incurs a 0.2 % efficiency penalty compared to the MCT, which is mainly attributed to the higher-than-necessary winding losses: due to imperfect twisting, the litz wire used in the prototype has been measured to cause up to 30 % higher losses [96]. With a correctly manufactured litz wire, the efficiency is expected to increase by 0.1 %, bringing it close to that of the MCT.

For a comprehensive evaluation of the efficiency, **Fig. 5.9** shows measured (stars) and simulated (circles for MFTs and squares for 1:1-DCXs) efficiency curves for the ACT and the MCT as well as the corresponding DCX systems. Note that the ACT can operate with passive cooling (fans not activated and corresponding losses not considered) up to about 70 % of the rated power. The ACT's efficiency curve is rather flat and shows a very high partial-load efficiency, i.e. $\eta > 99.4\,\%$ applies for a very wide range of the output power of $P_\mathrm{o} \in [15\%, 100\%]P_\mathrm{N}$. In contrast, the MCT features comparatively low partial-load efficiency due to relatively high load-independent core losses. Thus, for the realized prototypes, the ACT outperforms the MCT in terms of efficiency for output power levels of up to $P_\mathrm{o} \approx 70\%P_\mathrm{N}$.

With regard to the overall 1:1-DCX systems, both efficiency curves are relatively flat for loads between 35 % and 100 % of the nominal power. The MCT-DCX attains a very high efficiency (close to 99.2 %) even up to $110\%P_\mathrm{N}$. Conversely, the ACT-DCX achieves slightly higher part-load efficiency for loads $< 40\%P_\mathrm{N}$ due to the aforementioned exceptional partial-load characteristic of the ACT and in spite of high magnetizing current which causes load-independent switching losses in MOSFETs. From the similarity of the system-level efficiency curves at low loads, we conclude that the impact of the magnetizing current losses in the ACT-DCX is comparable to the transformer's core losses in the MCT-DCX. Finally, at the rated power of $P_\mathrm{N} = 166\,\mathrm{kW}$, the transformer efficiencies are 99.7 % and 99.5 % for the MCT and ACT, respectively, whereas the DC-DC efficiencies reach 99.2 % for the MCT-DCX and 99.0 % for the ACT-DCX.

5.4.2 Application-Oriented Evaluation

From the quantitative results presented above, we conclude that ACTs represent a promising alternative to dry-type MCTs for isolated DC-DC converters, in particular for 1:1-DCX applications, where similar efficiency characteristics can be achieved. However, both concepts show distinct strengths and

weaknesses. To aid in selecting the concept most suitable for a specific application, we provide a qualitative discussion of the key distinctive features in the following:

- *Lightweight* - ACTs can achieve several times higher gravimetric power density compared to MCTs. However, on the system level this advantage reduces to about 2× higher gravimetric power density of the ACT-DCX compared to the MCT-DCX.
- *Compactness* - Due to lack of guidance for the magnetic flux and the resulting shielding requirements, the volume of an ACT is relatively high. ACTs thus achieve significantly lower volumetric power density. Consequently, MCT-based systems are more favorable for compact solutions.
- *Linearity* - ACTs are perfectly linear and, therefore, can withstand significant temporary overcurrents or overvoltages without changing their properties. Because of the nonlinear behavior (e.g., saturation) of the magnetic cores, this is not the case for MCTs.
- *Temperature* - The operating temperature of ACTs is not limited by the Curie temperature of a magnetic core material. Therefore, ACTs are well suited for high-temperature environments. Furthermore, due to simple construction, thermal management is straightforward compared to MCTs with dry-type insulation systems.
- *Overload capabilities* - Due to the linearity and high-temperature capability of an ACT, and owing to the large thermal time constant of the MCT, both solutions offer good long-term overload capabilities.
- *Stray field / shielding* - The medium-frequency magnetic stray field emitted by MFTs is not negligible and should be shielded in order to avoid eddy-current losses in nearby metallic conductors and/or electromagnetic interference issues. However, the magnetic stray fields in the vicinity of an MCT are typically lower and decay faster with distance. Hence, ensuring a relatively small distance to other equipment or persons is usually sufficient. In contrast, ACTs typically require explicit shielding. If this is not anyway provided from the application's assembly situation (e.g., cabinet), a low-loss and lightweight conductive shielding can be implemented.
- *Insulation coordination* - ACTs employ air as insulation medium. The required clearance and creepage distances can be tailored, even for

a finished design, by inserting appropriate barrier elements between the coils. This is advantageous, e.g., for input-series output-parallel (ISOP) arrangements of DCX cells as the transformers are experiencing different CM voltages in such converter structures, or for airborne applications, where the insulation strength of air depends on altitude. In contrast, once the insulation system of an MCT has been defined, the insulation voltage rating cannot be changed anymore.

- *Dielectric losses* - Thanks to the employed air insulation, the dielectric losses of the ACT can be neglected. Conversely, the dielectric losses of dry-type MCTs with silicone insulation must be taken into account, and in particular the impact of initial environmental conditioning (relative humidity).
- *Construction* - Clearly, the construction of ACTs is relatively simple, as mainly structural elements to support the windings are needed. In contrast, dry-type MCTs require a controlled pressurized vacuum potting process to achieve a void-free insulation system.
- *Resonant capacitor bank* - Due to relatively high leakage inductances, an ACT requires low resonant capacitance values for a given operating frequency, which results in high resonant capacitor voltages. Therefore, high-power capacitor bank assemblies are necessary, which are bulky and generate significant losses (possibly requiring active cooling). On the other hand, for the MCTs, the capacitor bank for the considered 1:1-DCX could be realized with ceramic capacitors of negligible losses, mass and volume.
- *Semiconductors* - Owing to the higher operating frequency and rms currents (due to higher magnetizing current), an ACT-DCX requires more power semiconductor chip area per switch than an MCT-DCX, which results in higher converter cost and increased realization complexity. Nevertheless, the high magnetizing currents of ACTs are advantageous for soft-switching applications.

5.5 Conclusion

This chapter compares the theoretical performance limits of a 166 kW / 7 kV air-core transformer (ACT) and magnetic-core transformer (MCT) for unity voltage conversion ratio (1:1-DC transformer, 1:1-DCX) application on both, the component (transformer) and on the system (DCX) level. The results

of multi-objective optimizations show that ACTs can achieve several times higher gravimetric power densities compared to MCTs. Furthermore, on the system level, ACT-based DCXs reach about two times higher gravimetric power density compared to MCT-based DCXs. However, ACTs typically require a shielding enclosure to limit magnetic stray fields, which increases the volume. Thus, only about half of an MCT's volumetric power density is achievable.

An extension of experimental characterization of full-scale ACT and MCT prototypes is presented with focus on the dielectric losses, long-term overload capability and partial discharges (PDs) measurement, facilitating a practical comparative evaluation. It has been shown that initial environmental conditioning of the MCT's dry-type silicone insulation has a significant influence on the dielectric losses. Depending on the state of the silicone (moist or dry), the dielectric losses can vary by more than a factor of three. Hence, in some dry-type MFTs the dielectric losses can account for up to 15 % of the total losses and must be considered in the design calculations. In contrast, there are no noteworthy dielectric losses in an ACT, thanks to the air insulation.

Conservative assumptions during the optimization and design phase enable significant overload capability of both prototypes, as winding and core temperatures in thermal steady-state with injected core and winding losses that correspond to the nominal operating point remain clearly below limiting values. Therefore, heat runs with losses that correspond to maximum thermally feasible power transfer were carried out. At room temperature, the MCT prototype can be operated with power transfer of up to 250 kW, whereas the ACT prototype can reach 225 kW.

Partial discharges measurements realized according to IEC 62477 show that the ACT passes the PD test, i.e., amplitudes of all discharge events are below the 10 pF limit, at 10.7 kV rms (15.1 kV peak) for the rated insulation voltage of $V_{\mathrm{iso}} = 10$ kVDC, whereas the MCT can reach PD-free operation only up to 4.2 kVDC which results from the test at 6.3 kV peak. Further investigations and basic studies of PDs development in windings potted in the same technology and materials are required as the measurements indicate that the PDs occur in the winding package of the MCT.

The ACT prototype (16.5 kW/kg, 2.2 kW/dm^3) achieves a measured full-load efficiency of 99.5 % at an operating frequency of 77.4 kHz. The MCT prototype (6.7 kW/kg, 5.4 kW/dm^3), operated at 40.0 kHz, reaches a measured efficiency of 99.7 %. Furthermore, the use of 10 kV SiC MOSFETs enables system-level efficiencies (calculated) for the ACT-DCX and the MCT-DCX of 99.0 % and 99.2 %, respectively. Moreover, both DCXs are characterized by a flat efficiency curve, with the ACT-DCX's efficiency being slightly higher

for loads < 40% of rated power, thanks to the ACT's low no-load losses. In contrast, for higher power levels, the MCT's relatively low winding losses enable higher efficiencies. For the overall systems, the achieved power density indices are 9.7 kW/kg, 2.0 kW/dm^3 for the ACT-DCX and 5.6 kW/kg, 4.5 kW/dm^3 for the MCT-DCX.

Finally, the presented application-oriented qualitative evaluation clarifies the strengths and weaknesses of the ACT- and MCT-based systems, and can aid in the selection of the most suitable concept for a given application.

Part 2

Medium-Voltage Power Semiconductor Stage

6

MV Power Semiconductor Stage: Quasi-2-Level Flying Capacitor Converter

This chapter summarizes the major research findings also published in:

- **P. Czyz**, P. Papamanolis, F. Bruguera, T. Guillod, F. Krismer, V. Lazarevic, J. Huber, and J. W. Kolar, "Load-Independent Voltage Balancing of Multi-Level Flying Capacitor Converter in Quasi-2-Level Operation," *Electronics*, vol. 10, no. 19, pp. 1-31, 2021.

Executive Summary

Quasi-2-level (Q2L) operation of multi-level bridge-legs, especially of flying-capacitor converters (FCC), is an interesting option for realizing single-cell power conversion in applications whose system voltages exceed the ratings of available power semiconductors. To ensure equal voltage sharing among a Q2L-FCC's switches, the voltages of a Q2L-FCC's minimized flying capacitors (FCs) must always be balanced. Thus, in this chapter a concept for load-independent FC voltage balancing is proposed: for non-zero load current, a model predictive control (MPC) approach is used to identify the commutation sequence of the individual switches within a Q2L switching transition that minimizes the FC or cell voltage errors. In case of zero load current, a novel MPC-based approach using cell multiple switching (CMS) is employed, i.e., the insertion of additional zero-current commutations within a Q2L transition, to exchange charge between the FCs via the charging currents of the switches' parasitic capacitances. Experiments with a 5-level FCC half-bridge demonstrator confirm the validity of the derived models and verify the performance of the proposed load-independent balancing concept.

6.1 Introduction

Stringent efficiency requirements for the supply of high-power DC applications such as hyperscale data centers [15, 16, 92, 98] and high-power electric vehicle (EV) charging stations [10, 11, 90, 127] drive the interest in direct power electronic interfaces between a medium-voltage (MV) AC grid and a low-voltage (LV) DC bus. Such flexible isolation and voltage-scaling MVAC-LVDC interfaces are commonly referred to as solid-state transformers (SSTs) [13, 16, 89, 92]. Given the typical MV grid voltage levels of 6.6 kV rms line-to-line (3.8 kV line-to-neutral) in Europe [16] and 4.16 kV rms line-to-line (2.4 kV line-to-neutral) in the USA [89, 92], clearly either latest technology wide-bandgap (WBG) power semiconductors with extreme blocking voltage ratings of up to 15 kV [128–131] or, alternatively, multi-cell topologies employing production-grade LV power semiconductors (e.g., 1.2 kV – 3.3 kV SiC MOSFETs or Si IGBTs) are necessary.

Even though multi-cell SSTs can achieve a high conversion performance by configuring the cells in an input-series/output-parallel (ISOP) fashion, they are highly complex due to the typically high number of sub-units, the required communication system, and ultimately, the high component count. Therefore, recently the research focus has shifted to single-cell SST realizations, i.e., 2- or 3-level topologies enabled by new 6.5 kV – 15 kV SiC MOSFETs or IGBTs [16, 132]. However, the availability of these HV transistors is limited (mainly engineering samples), and prices remain high despite strong activity towards commercialization and manufacturing [133].

Alternatively, bridge-legs for single-cell SSTs can be realized with a series connection of semiconductors [134, 135], see **Fig. 6.1(a)**, super-cascode configurations [136, 137], see **Fig. 6.1(b)**, or multi-level converter structures, i.e., modular multi-level converter (MMC, cf. **Fig. 6.1(c)**) [138–142] and flying capacitor converter (FCC, cf. **Fig. 6.1(d)**) structures [135, 143–145]. However, due to unavoidable differences (manufacturing tolerances etc.) of the semiconductor and gate driver properties, direct series connections of semiconductors require additional circuitry, i.e., (lossy) snubbers, to ensure equal transient and stationary blocking voltage sharing. The super-cascode approach [136, 137] employs a series connection of several HV SiC (normally-on) JFETs and a LV Si (normally-off) MOSFET for initiating turn-on and turn-off. Similarly, it requires a passive network that is adapted to the parasitic capacitances of the SiC JFETs to ensure proper operation with balanced blocking voltages. Furthermore, only a few suppliers of MV SiC JFETs exist. The main drawbacks of an MMC topology are the high total chip area usage, the high number of gate

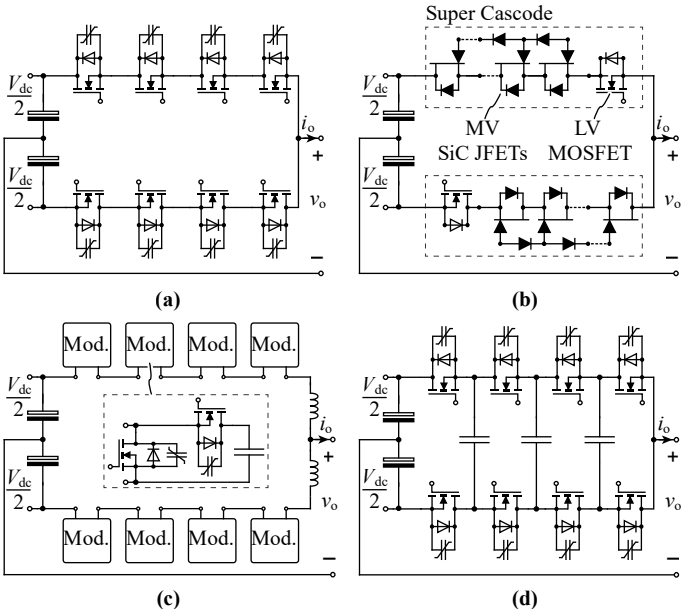


Fig. 6.1: Realization of a MV half-bridge using different semiconductor arrangements: **(a)** direct series connection of MV SiC MOSFETs, **(b)** super-cascode (series connection of MV SiC JFETs with a low-voltage MOSFET), **(c)** 5-level MMC, and **(d)** 5-level FCC.

drivers, and the presence of branch inductors. Finally, a FCC half-bridge (HB) features several advantages such as reduced switching losses (snubberless, on the contrary to direct series connection) and robust voltage balancing without additional chip area and gate drivers (compared to a MMC HB). However, conventional multi-level operation of MMC and FCC bridge-legs, while resulting in low harmonic content of the generated output voltage, requires a relatively large total volume of the flying capacitors (FCs).

The large capacitor volumes required for the MMC and FCC can be reduced by employing a quasi-2-level modulation scheme (Q2L-MMC, Q2L-FCC). With Q2L modulation, the intermediate voltage levels are only used during the switching transitions. The bridge-leg's output voltage thus transitions between the two DC voltage levels (positive and negative) in a staggered fashion [139–141, 145–151]. Note that these staggered transitions of the Q2L-MMC and Q2L-FCC topologies feature lower average $\mathrm{d}v/\mathrm{d}t$ compared to the (MV) 2-level converters, which is beneficial for the design of EMI filters and

magnetics such as medium-frequency transformers, and lowers the stress of the electric insulation [43, 125, 126, 146, 152].

However, whereas in conventional multi-level operation of a FCC bridge-leg, balancing of the FC voltages occurs naturally [153], balancing is not automatically ensured in Q2L operation. In this regard, in-depth investigations of the switching operations in a Q2L-FCC and resulting charges delivered to the FCs are conducted. Aiming for generic results, two exemplary DC-link/load configurations resulting in symmetric (typical, e.g., for an isolated DC-DC converter) or asymmetric (typical, e.g., for a PFC rectifier or a motor inverter) output currents are considered. **Figs. 6.2(b)–(c)** show corresponding exemplary waveforms and the characteristic staggered Q2L transitions of the bridge-leg's output voltage in case of zero-voltage switching (ZVS) and hard-switching (HS).

This chapter is organized as follows: **Section 6.2.1** describes the Q2L operating principle of the 5L-FCC half-bridge for ZVS and HS transitions with non-zero output current. In addition, Q2L transitions with zero output current are analyzed in **Section 6.2.2** and a generic description of resulting charge and voltage increments is derived. Furthermore, the novel cell multiple switching (CMS) concept is introduced to facilitate FC voltage balancing with zero output current. **Section 6.2.4** investigates the behavior of the CMS for semiconductors of different voltage classes and **Section 6.2.5** complements the analysis of load-independent balancing in Q2L-FCC by discussing the behavior under overload and short-circuit conditions. Finally, **Section 6.3** provides a concluding discussion.

6.2 Q2L Operation of the 5L-FCC

This section recaps the processes in the Q2L-operated 5L-FCC for ZVS and HS transitions employing consecutive switching sequences described in [146]. Next, the analysis is extended by first considering also non-consecutive switching sequences and second including operation of the Q2L-FCC with zero output current. The in-depth analysis of the switching transitions given here is required to determine the total net charge exchange of the flying capacitors during Q2L transitions and ultimately to enable the development of a robust FC voltage balancing concept for Q2L-FCCs. Note that the obtained results are generic and also apply to N-level Q2L-FCCs. However, we exemplify the considerations using a 5L-FCC (see **Fig. 6.2)** for clarity. The corresponding circuit simulations employ an exemplary MOSFET equivalent circuit that consist of a voltage-controlled current source, the non-linear parasitic MOSFET

capacitances, the antiparallel body diode, the diode reverse recovery, and the package inductances.

6.2.1 Operating Principle with Non-Zero Output Current

As it can be seen in **Fig. 6.2**, a 5L-FCC consists of 4 cells (in general, an N-level FCC consists of $n = N-1$ cells), each comprising two complementary switches ($S_{x\mathrm{p}}$ and $S_{x\mathrm{n}}$) and a flying capacitor ($C_{\mathrm{FC}x}$), whereas the cell which is the closest to the DC-link includes the DC-link capacitor. A Q2L (switching) transition

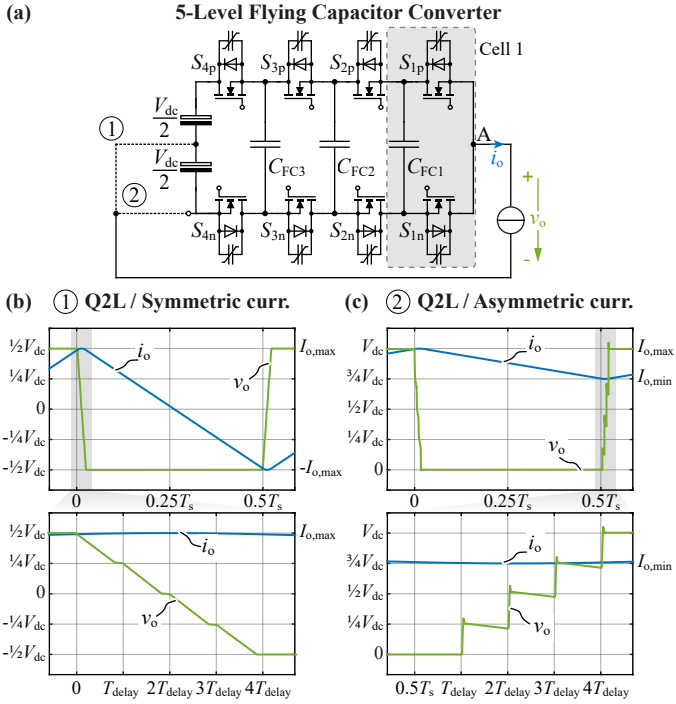


Fig. 6.2: **(a)** Considered 5-level flying capacitor converter (5L-FCC) HB with two alternative load/DC-link connections (① and ②). Corresponding exemplary output waveforms and characteristic staggered Q2L transitions of the output voltage v_{o} for: **(b)** symmetric output current i_{o} (ZVS transitions), **(c)** asymmetric output current i_{o} (ZVS & HS transitions).

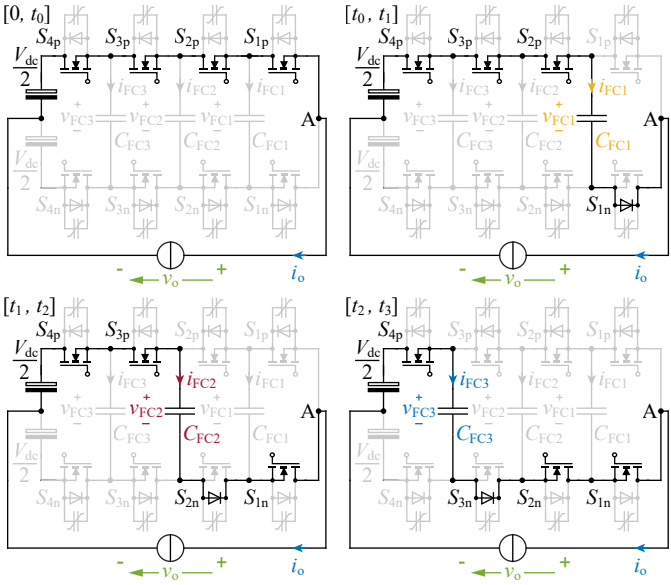


Fig. 6.3: Switching states of a Q2L-operated 5L-FCC HB with constant positive output current ($I_{o,max}$) during a Q2L switching transition with negative slope of v_o, resulting in ZVS.

is a commutation of the load current from all upper switches (S_{1p}-S_{4p}) in state *on* to all bottom switches (S_{1n}-S_{4n}) in state *on*, cf. **Fig. 6.2(a)**, or vice versa. The bride-leg output voltage v_o thus attains two distinct voltage levels ($V_{dc}/2$ and $-V_{dc}/2$) for most of the time and the several intermediate voltage levels appear only shortly during the Q2L transitions. A Q2L transition is characterized by a switching sequence (*SEQ*) that defines the order in which the individual cells are commutated. For example, in a 5L-FCC SEQ_{1234} means that the cells are commutated consecutively starting from cell 1 and ending with cell 4, see **Fig. 6.3**.

Fig. 6.3 illustrates such a Q2L transition and defines selected time intervals for the example of a falling slope of v_o, positive output current i_o and SEQ_{1234} which results in ZVS transitions for all switches. **Fig. 6.4** shows the simulated key waveforms of this transition. Similarly, **Fig. 6.5** shows key waveforms for a HS transition, i.e., constant positive output current ($I_{o,max}$) during the switching transition with positive slope of v_o and SEQ_{4321}. For a more in-depth

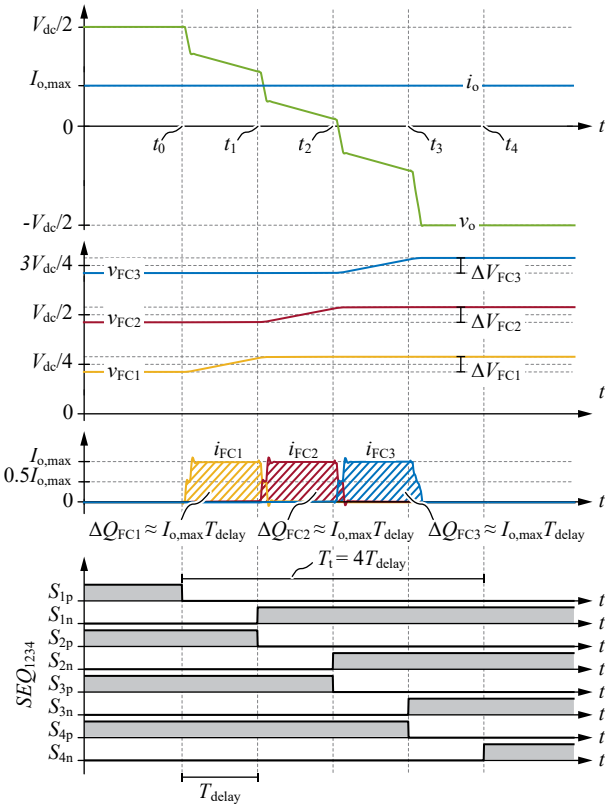


Fig. 6.4: Simulation results for the ZVS case of Q2L-operated 5L-FCC: time intervals and simulated waveforms of output current (i_o) and output voltage (v_o), FC voltages ($v_{FC\{1,2,3\}}$) and currents ($i_{FC\{1,2,3\}}$), and MOSFET gating signals.

description of processes in the sub-intervals of ZVS and HS commutations see [146].

Note that consecutive sequences, i.e., SEQ_{1234} or SEQ_{4321}, lead to FC charge increments given by

$$|\Delta Q_{FC\{j\}}| \approx T_{delay\{j\}} |I_{o,max}|, \tag{6.1}$$

where j is the number of the FC and T_{delay} is the time allocated for the transition of an individual cell. Note that the selection of T_{delay} is discussed in detail in **Section 6.2.3**. To facilitate the modeling and balancing of FC

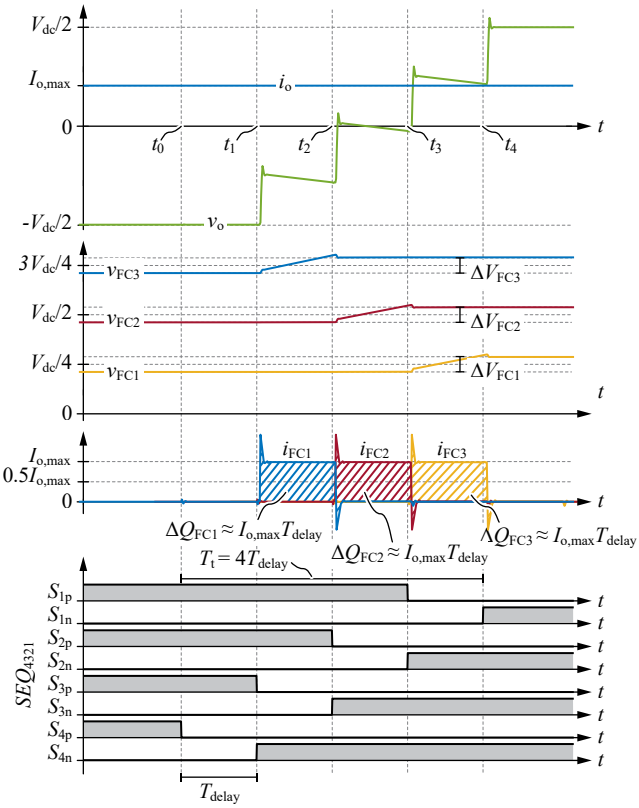


Fig. 6.5: Simulation results for the HS case of Q2L-operated 5L-FCC: time intervals and simulated waveforms of output current (i_o) and output voltage (v_o), FC voltages ($v_{FC\{1,2,3\}}$) and currents ($i_{FC\{1,2,3\}}$), and MOSFET gating signals.

voltages, we assume equal delay times T_{delay} for all cells and thus identical base charge increments result:

$$\Delta Q_{FCo} = \Delta Q_{FC1} = \Delta Q_{FC2} = \Delta Q_{FC3} \approx T_{delay} I_{o,max}. \tag{6.2}$$

It is worth noting that for the assumed equivalent circuit (i.e., neglect of parasitic ground capacitances) the transferred charges are independent of the switching frequency and the number of levels. However, the sign of the net charge exchange of an FC during a Q2L transition for a given sequence depends on the sign of the load current and the direction of the voltage slope.

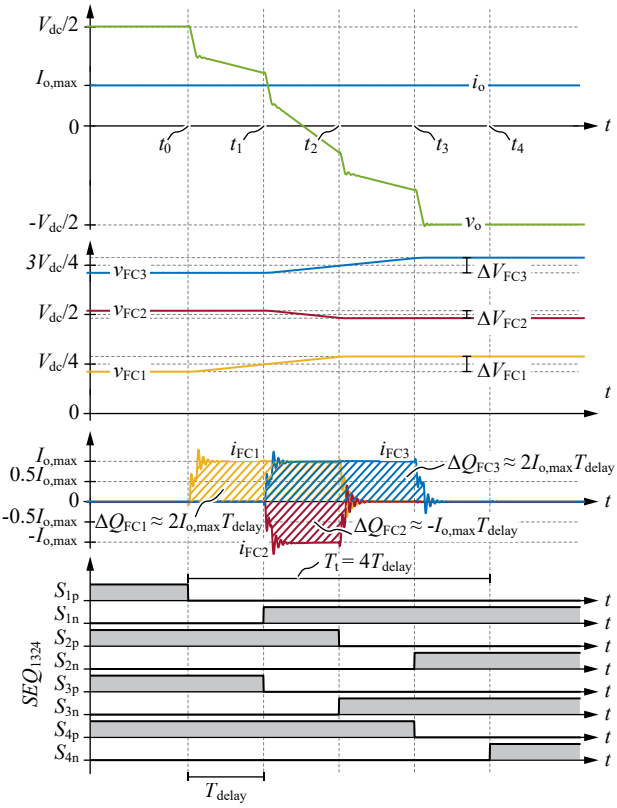


Fig. 6.6: Simulation results for Q2L operation of the 5L-FCC with constant positive output current (I_o) during the switching transition with negative slope of v_o, exemplifying the effect of a non-consecutive sequence SEQ_{1324}: charging of FC_1 and FC_3, discharging of FC_2.

For FCC realizations with more than two cells, i.e., $n > 2$ ($N > 3$), the cells can also be switched in a non-consecutive manner and thus a total of $(n!)$ different consecutive and non-consecutive sequences exists. The subset of non-consecutive sequences contains $(n! - 2)$ sequences. **Fig. 6.6** presents an example of a Q2L transition with the non-consecutive sequence SEQ_{1324}: FC_1 and FC_3 are charged with $2\Delta Q_{FCo}$, whereas the FC_2 is discharged with ΔQ_{FCo}. Therefore, in contrast to consecutive sequences, non-consecutive sequences lead to non-equal charge exchanges of the individual FCs (for the

Tab. 6.1: Effect of all sequences available ($\mathcal{S}_{\mathrm{CL}}$) for a Q2L-5L-FCC on FC charge increments in function of delay times for Q2L ZVS transition (for HS transition, the same value but opposite signs apply): (+1) charge, (-1) discharge, (0) no effect. Scaling the values with the respective $T_{\mathrm{delay}\{n\}}$ and $I_{\mathrm{o,max}}$ gives the charge increment values. Note that the table is simplified and values for $SEQ_{3\mathrm{xxx}}$ and $SEQ_{4\mathrm{xxx}}$ are obtained by considering symmetry and multiplying the respective values by (-1).

⇵	FC_1				FC_2				FC_3				
Sequence	$T_{\mathrm{delay}1}$	$T_{\mathrm{delay}2}$	$T_{\mathrm{delay}3}$	$T_{\mathrm{delay}4}$	$T_{\mathrm{delay}1}$	$T_{\mathrm{delay}2}$	$T_{\mathrm{delay}3}$	$T_{\mathrm{delay}4}$	$T_{\mathrm{delay}1}$	$T_{\mathrm{delay}2}$	$T_{\mathrm{delay}3}$	$T_{\mathrm{delay}4}$	
SEQ_{1234}	+1	0	0	0	0	+1	0	0	0	0	+1	0	$-SEQ_{4321}$
SEQ_{1243}	+1	0	0	0	0	+1	0	+1	0	0	0	-1	$-SEQ_{4312}$
SEQ_{1324}	+1	0	+1	0	0	0	-1	0	0	+1	+1	0	$-SEQ_{4231}$
SEQ_{1342}	+1	0	+1	+1	0	0	-1	-1	0	0	+1	0	$-SEQ_{4213}$
SEQ_{1423}	+1	0	0	+1	0	+1	0	0	0	-1	0	-1	$-SEQ_{4132}$
SEQ_{1432}	+1	0	+1	+1	0	0	-1	0	0	0	0	-1	$-SEQ_{4123}$
SEQ_{2134}	0	-1	0	0	+1	+1	0	0	0	0	+1	0	$-SEQ_{3421}$
SEQ_{2143}	0	-1	0	0	+1	+1	0	+1	0	0	0	-1	$-SEQ_{3412}$
SEQ_{2314}	0	-1	-1	0	0	+1	0	0	+1	0	+1	0	$-SEQ_{3241}$
SEQ_{2341}	0	-1	-1	-1	0	+1	0	0	0	0	+1	0	$-SEQ_{3214}$
SEQ_{2413}	0	-1	0	-1	+1	+1	0	+1	-1	0	0	-1	$-SEQ_{3142}$
SEQ_{2431}	0	-1	-1	-1	0	+1	0	+1	0	0	0	-1	$-SEQ_{3124}$
	$T_{\mathrm{delay}4}$	$T_{\mathrm{delay}3}$	$T_{\mathrm{delay}2}$	$T_{\mathrm{delay}1}$	$T_{\mathrm{delay}4}$	$T_{\mathrm{delay}3}$	$T_{\mathrm{delay}2}$	$T_{\mathrm{delay}1}$	$T_{\mathrm{delay}4}$	$T_{\mathrm{delay}3}$	$T_{\mathrm{delay}2}$	$T_{\mathrm{delay}1}$	Sequence
	FC_3				FC_2				FC_1				⇵

same T_{delay} and $I_{\text{o,max}}$). Therefore, even charging of some FCs and discharging of others during the same Q2L transition can be achieved. Note, however, that all FCs experience a charge exchange, and hence are coupled through a sequence in the sense that it is not possible to influence only a selected subset of the FCs. Considering the exemplary 5L-FCC, **Tab. 6.1** summarizes all sequences, denoted henceforth as set $\mathcal{S}_{\text{CL}}$, and their effects on the FCs' charge for the case of ZVS transitions. It is found that for the HS transition, the sequences have opposite effect. Therefore, the values from **Tab. 6.1** need to be multiplied by (-1) to obtain the charge increments for HS transitions. Furthermore, **Tab. 6.1** is simplified by symmetry considerations, i.e., the fact that sequences $SEQ_{3\text{xxx}}$ and $SEQ_{4\text{xxx}}$ result in the same absolute values of total charge exchanges as $SEQ_{2\text{xxx}}$ and $SEQ_{1\text{xxx}}$, respectively. However the order of FCs and delay times is reversed, and the values from the table must be multiplied with (-1) to obtain the actual FC charge exchanges, which is denoted by the $-$ sign preceding the sequence's name (see right & bottom labels in **Tab. 6.1**).

Based on this analysis, we formulate the total change of charge provided to the FCs as

$$\Delta \boldsymbol{Q}_{\text{FC}} = \begin{bmatrix} \Delta Q_{\text{FC}1} \\ \dots \\ \Delta Q_{\text{FC}\{j\}} \end{bmatrix} = I_{\text{o,max}} (\boldsymbol{S} \times \boldsymbol{T}_{\text{delay}}), \tag{6.3}$$

where

$$\boldsymbol{T}_{\text{delay}} = \begin{bmatrix} T_{\text{delay}1} & \dots & T_{\text{delay}\{n\}} \end{bmatrix}^T \tag{6.4}$$

is a delay time vector and $\boldsymbol{S}$ is a matrix which specifies how the particular delay times influence the change of charge of the FCs and is equivalent to the rows in **Tab. 6.1**. The matrix $\boldsymbol{S}$ is constructed by stacking the effects of the sequences have on each FC, hence it has dimensions of $j \times n$. From **Tab. 6.1** it is apparent that the charge increments can be equal to values from the following set: $\pm \Delta Q_{\text{FCo}} \cdot \{1, 2, ..., j\}$. In order to ensure well defined voltage levels across the switches and ease of balancing, equal values C_{FC} of all FCs are selected, which consequently leads to the voltage increments

$$\Delta \boldsymbol{V}_{\text{FC}} = \begin{bmatrix} \Delta V_{\text{FC}1} \\ \dots \\ \Delta V_{\text{FC}\{j\}} \end{bmatrix} = \frac{\Delta \boldsymbol{Q}_{\text{FC}}}{C_{\text{FC}}}. \tag{6.5}$$

Henceforth, for the sake of simplicity, equal delay times T_{delay} are considered for all cells, and the implications of that assumption are discussed further in

Section 7.2. Taking as an example the sequence SEQ_{1324} (cf. **Fig. 6.6**) and equal delay times T_{delay} results in:

$$\Delta \boldsymbol{V}_{1324} = \frac{I_{\text{o,max}}}{C_{\text{FC}}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 1 & 1 & 0 \end{bmatrix} \times \begin{bmatrix} T_{\text{delay}} \\ T_{\text{delay}} \\ T_{\text{delay}} \\ T_{\text{delay}} \end{bmatrix}, \tag{6.6}$$

$$\Delta \boldsymbol{V}_{1324} = \frac{\Delta Q_{\text{FCo}}}{C_{\text{FC}}} \begin{bmatrix} 2 \\ -1 \\ 2 \end{bmatrix}. \tag{6.7}$$

which corresponds to the FC voltage waveforms depicted in **Fig. 6.6**.

6.2.2 Operating Principle with Zero Output Current: Cell Multiple Switching

From (6.3) it is obvious that in case of zero output current, the charge increments of the FCs are expected to be zero. **Fig. 6.7** presents the simulation results for Q2L operation with $i_o = 0$ during the switching transition with negative slope of v_o. It can be seen that during each commutation, due to the hard-switching and charging of the switches' output capacitances, the commutation loop current leads to an exchange of charges, i.e., subtraction of charge from a cell's input-side capacitor and addition of charge to the output-side capacitor of the respective converter cell. This can be seen, e.g., in **Fig. 6.7** between $t_2 < t < t_3$ where the exchange of charges between FC_1 and FC_2 occurs. Note that in case of zero-current switching of cell 1, the charge is delivered to the load, whereas in case of cell 3, the charge delivered to FC_3 is subtracted from the DC-link. For an in-depth analysis see [154]. However, the net charge exchange of each FC over the entire transition is approximately zero. Nevertheless, the exchange of charge between the FCs during no-current Q2L transitions can be utilized in a novel method for balancing the FC voltages in case of zero output current.

To do so, additional commutations are inserted in one or more cells during a Q2L transition. This leads to additional hard-switching events of one or several of the MOSFETs. This concept which is denoted as *cell multiple switching* (CMS) thus allows to obtain non-zero net charge exchange of certain FCs over a Q2L transition, therefore offering a means of balancing the FC voltages even in case of zero output current.

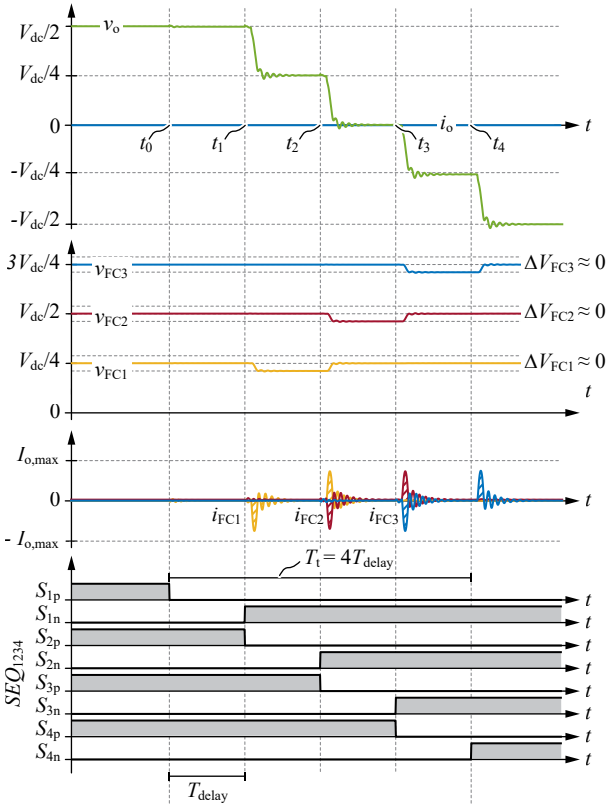


Fig. 6.7: Simulation results for the 5L-FCC in configuration ① with zero output current during the Q2L transition with negative slope of v_o: zero net charge increments of the FCs result.

Fig. 6.8 shows the exemplary simulation results for a 5L-FCC in split DC-link configuration with zero output current during the Q2L transition with negative slope of v_o and a CMS event inserted in cell 3. It can be noticed that until $t < t_3$ the processes in the transition occur as for a sequence SEQ_{1234} (see **Fig. 6.7**). However, at $t = t_4$, S_{3n} turns off and the circuit remains in steady-state during $[t_4, t_5]$ and $v_o = -V_{dc}/4$ applies. The time interval between t_3 and t_4, in which S_{3n} is *on*, has a duration of one pulse time T_p. Two additional switching operations are inserted between $t_5 < t < t_8$: first, v_o is switched back to 0 during $t_5 < t < t_7$, and, subsequently, v_o is switched to $-V_{dc}/4$

during $t_7 < t < t_8$. During $t_3 < t < t_4$, the charge of FC_2 is increased by ΔQ_{S3p} and FC_3 is discharged by the same value, where

$$\Delta Q_{S3p} = Q_{oss,3p} + Q_{rr,3p}, \tag{6.8}$$

with $Q_{oss,3p}$ and $Q_{rr,3p}$ being the charges stored in the output capacitance C_{oss} of the MOSFET and the reverse-recovery charge of the anti-parallel diode, respectively. During $t_5 < t < t_6$, FC_2 is again charged, whereas FC_3 is discharged by ΔQ_{S3n}. Finally, at $t = t_8$, S_{4n} turns on and the last commutation is completed. It can be seen that the presented sequence introduces 2 additional switching pulses in cell 3, therefore it is denoted as $SEQ_{123(33)4}$, where subscript (33) denotes the CMS event in cell 3.

Assuming that the charge increment from each switch is approximately the same and equal to ΔQ_S, a CMS event results in a total net charge increment of the affected FCs equal to:

$$\Delta Q_{FC} \approx 2\Delta Q_S. \tag{6.9}$$

The corresponding voltage increment per CMS event is thus:

$$\Delta V_{CMS} \approx \frac{\Delta Q_{FC}}{C_{FC}} \approx \frac{2\Delta Q_S}{C_{FC}}. \tag{6.10}$$

Using the linear charge-equivalent output capacitance $C_{Q,eq}$ and assuming that $Q_{rr} \approx 0$, (6.10) can be further simplified to:

$$\Delta Q_S = \int_0^{V_{ds}} C_{oss}(v) \cdot \mathrm{d}v = C_{Q,eq} \cdot V_{ds}, \tag{6.11}$$

$$\Delta V_{CMS} \approx \frac{2C_{Q,eq} \cdot V_{ds}}{C_{FC}}. \tag{6.12}$$

Therefore, the CMS balancing controllability depends on the capacitance ratio $k_c = 2C_{Q,eq}/C_{FC}$ and is discussed in detail for semiconductors of different voltage classes in **Section 6.2.4**.

6.2.3 Duty Cycle Limitation / Selection of Delay Time

For a certain output current $I_{o,max}$ the charge increments of the FCs during a Q2L transition are proportional to the delay times, see (6.3). Hence this parameter is a degree of freedom in the design of Q2L-FCCs and its constraints

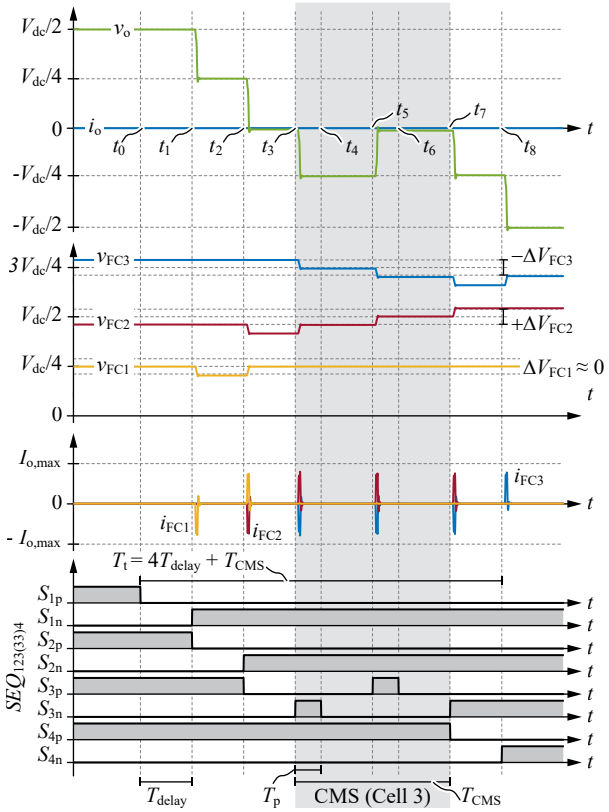


Fig. 6.8: Simulation results for the 5L-FCC in configuration ① with zero output current during the Q2L transition with negative slope of v_o: Note the single cell multiple switching event of cell 3. A delay T_{delay} and a pulse time $T_p = 0.5T_{delay}$ are used. Note that the same T_{delay}, but a different time base are used compared to **Fig. 6.7**.

are discussed in the following. The duration T_t of a complete Q2L transition, cf. **Fig. 6.4**, in the NL-FCC is given by

$$T_t \approx (N-1)T_{delay}, \tag{6.13}$$

$$\approx 4T_{delay}, \text{ for } N = 5. \tag{6.14}$$

Thus, the Q2L transitions limit the maximum duty cycle to

$$d_{\max} = 1 - \frac{2T_t}{T_s}, \tag{6.15}$$

$$= 1 - \frac{8T_{delay}}{T_s}, \text{ for } N = 5. \tag{6.16}$$

Therefore, the delay time can be selected only within certain boundaries

$$T_{delay} \in [T_{min}, T_{max}]. \tag{6.17}$$

The maximum boundary T_{max} follows from the allowable duration of the switching transition, i.e., from the application-specific d_{max}, given that increased commutation times decrease the available output voltage-time product. The minimum boundary T_{min} follows from the system's physical limitations, i.e., the required interlock delay time to prevent shoot-through events. In practical applications additional constraints can be considered, e.g., in soft-switching Q2L-FCCs the time required to achieve ZVS in partial-load operation increases T_{min} above the minimum required to prevent shoot-through.

Note that if CMS is activated in the Q2L-FCC, the duration of the transition increases due to the inserted additional pulses. In case of inserting n_{CMS} events of duration T_{CMS} (cf. **Fig. 6.8**), the transition time is:

$$T_{CMS} \approx 2n_{CMS}(T_p + T_{delay}), \tag{6.18}$$

$$T_t \approx (N-1)T_{delay} + T_{CMS}, \tag{6.19}$$

$$\approx 6T_{delay} + 2T_p, \text{ for } N = 5, n_{CMS} = 1. \tag{6.20}$$

Therefore, based on the application specific d_{max}, the allowable number of CMS events, the number of involved cells, and T_p must be defined together with T_{delay}.

6.2.4 CMS for Semiconductors of Various Voltage Classes

The proposed method for balancing the FC voltages without load current, i.e., cell multiple switching (CMS), relies on the charge stored in the output capacitances of the switches, cf. (6.12). **Section 7.4.3** shows experimental validation for 150 V GaN eFETs (EPC2033) operated at a reduced (for safety reasons) $V_s = 25$ V, cf. ① in **Tab. 6.2.** However, the question arises whether this result is representative also for higher voltages, and then for power semiconductors of different voltage classes.

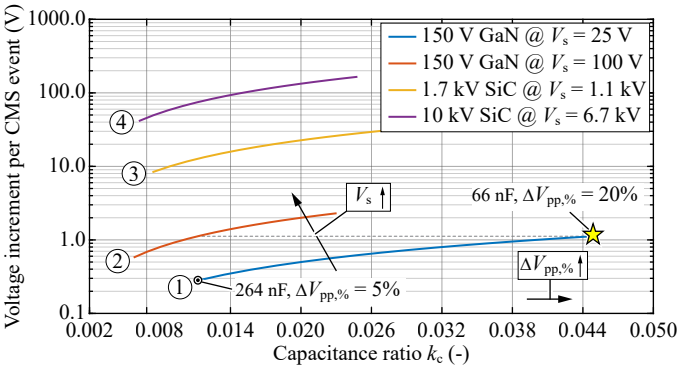


Fig. 6.9: Absolute voltage increment per CMS event (ΔV_{CMS}) for semiconductors of various voltage classes as functions of the capacitance ratio $k_c = 2C_{\mathrm{Q,eq}}/C_{\mathrm{FC}}$ for the considered relative peak-to-peak FC voltage ripple range $\Delta V_{\mathrm{pp},\%} = \Delta V_{\mathrm{pp}}/\ V_s \in [5\%, 20\%]$.

Therefore, we consider the following semiconductors in Q2L-5L-FCC designs with typical ratings for the given device: 150 V GaN eFET (EPC2033), 1.7 kV SiC MOSFET (C2M0045170P) and 10 kV SiC MOSFET (QPM3-10000-0300), cf. **Tab. 6.2. Fig. 6.9** shows the absolute voltage increment per CMS event, cf. (6.12) as a function of the capacitance ratio $k_c = 2C_{\mathrm{Q,eq}}/C_{\mathrm{FC}}$. For a fixed delay time and a maximum output current, a higher allowed FC voltage ripple results in a lower FC capacitance requirement, and therefore, for a given switch voltage, in a better controllability (i.e., larger voltage increment per CMS event). Moreover, it can can be noticed that for the GaN eFETs operated at 25 V (for $\Delta V_{\mathrm{pp},\%} = 20\%$, see ☆), the value of $\Delta V_{\mathrm{CMS}} = 1.1\,\mathrm{V}$ corresponds to approx. half of the maximum increment when operated at 100 V (2.3 V). This can be explained by the 4× higher switch voltage but approx. factor of 2 lower $C_{\mathrm{Q,eq}}$ in case of ② which indicates that the controllability at 100 V would be better for the same absolute value of voltage ripple which is discussed in detail in the following.

To assess CMS controllability, a relative voltage increment k_V defined as ratio of $\Delta V_{\mathrm{CMS}}/\Delta V_{\mathrm{pp}}$ is introduced. Since the value of the FCs is designed for a desired voltage ripple, the relative voltage increment is constant for the considered semiconductor and operating parameters, and the respective values are shown in **Tab. 6.2.** We use the same absolute voltage ripple in the experiments with the demonstrator at 25 V as for operation at 100 V, hence reducing the controllability (5.6% vs. 11.5%), therefore the measurements

represent the worst-case scenario. Finally, it can be seen that CMS events in case of 1.7 kV and 10 kV SiC MOSFETs provide even more controllability than Q2L-FCC with 150 V GaN eFETs.

6.2.5 Discussion of Overload and Short-Circuit Operation

In case of excessive currents, i.e., overload or short-circuit currents (e.g., 10× higher than nominal) at the output of a Q2L-operated half-bridge, there is a risk of overcharging the FCs. Also, unequal voltage sharing among the switches could ultimately lead to their destruction. However, from the Q2L operation description in **Section 6.2.1** we know that a fault needs to be present during the switching transition, therefore in a relatively short interval compared to the dynamics of the system ($\mathrm{d}i/\mathrm{d}t$), to create hazardous conditions for the capacitors and their voltages. To mitigate the eventual overvoltage conditions, we propose to set an ultra-short delay time $T_{\mathrm{delay}} = T_{\mathrm{sh}}$ (with T_{sh} in the range of rise/fall switching times of the semiconductors, as hard-switching is expected), which is applied in the Q2L switching transitions following an overcurrent detection. If the gate drivers are equipped with (ultra)-fast overcurrent detection, the fault can be cleared within ≈100 ns for LV GaN switches [155] and within ≈200 ns for MV SiC MOSFETs [156]. Thus, in the worst-case scenario, only a single Q2L transition will be impacted by excessive currents. In this regard, a correctly dimensioned T_{sh} should be sufficient to avoid harmful voltage deviations.

Furthermore, in case of some MOSFETs, e.g., 10 kV SiC MOSFETS, due to the excessively high drain current in the conducting switches the so-called *self turn-off* occurs, caused by the voltage drop across the source inductance [156]. This phenomenon effectively leads to the simultaneous switching of series connected MOSFETs as in a 2L bridge-leg. As a result, the commutations of the individual cells overlap, leading to a continuous output voltage change instead of a staggered transition. Hence, the charge increments of the FCs are negligible and it can be concluded that under such conditions the operation of the Q2L-FCC is not critical. Further investigations are out of the scope of this thesis, but should be performed in the course of further analyses of the proposed FC voltage balancing concept.

Tab. 6.2: Parameters for CMS controllability analysis for semiconductors of various voltage classes for the considered relative peak-to-peak FC voltage ripple range $\Delta V_{pp,\%} = \Delta V_{pp} / V_s \in [5\%, 20\%]$.

Param.	**150 V GaN** (EPC2033)		**1.7 kV SiC** (C2M0045170P)	**10 kV SiC** (QPM3-10000-0300)	
	①	②	③	④	
V_{dc}	100 V	400 V	4.4 kV	26.8 kV	DC-link voltage
V_s	25 V	100 V	1.1 kV	6.7 kV	switch voltage
$C_{oss,eq}$	1480 pF	760 pF	727 pF	200 pF	charge eq. capacitance
$I_{o,max}$	6.6 A	6.6 A	28 A	10.75 A	max. output current
$I_{o,ZVS}$	2.5 A	2.5 A	8 A	6 A	min. output current w/ ZVS
T_{delay}	100 ns	100 ns	200 ns	1000 ns	max. delay time
Relative controllability					
$k_V = \Delta V_{CMS}/\Delta V_{pp}$	5.6%	11.5%	14.7%	12.4%	relative CMS controllability
ΔV_{pp}	$5 - 20$ V[1]	$5 - 20$ V	$57 - 227$ V	$0.33 - 1.33$ kV	peak-to-peak volt. ripple

[1] Note that in case ① in experiments a relative peak-to-peak FC voltage ripple of 80% is used.

6.3 Conclusion

This chapter presents the detailed simulation results of quasi-2-level (Q2L) operation of a flying capacitor converter (FCC) half-bridge. Based on the analysis of zero voltage switching (ZVS) and hard-switching (HS) transitions with non-zero output current as well as transitions without an output current (zero-current HS), a generic description of resulting charge and voltage increments is derived.

In principle, the charge of a flying capacitor (FC) is proportional to the product of the delay time and the local maximum of the output current of the FCC-based half-bridge, where the delay time is the time allocated for the transition of an individual cell. Furthermore, all available switching sequences, i.e., the order in which the individual FC cells are commutated, are analysed for the 5L-FCC and it is concluded that there are two consecutive sequences resulting in the same value and sign of charge change in all FCs, whereas $((N-1)!-2)$ non-consecutive sequences enable to provide charges of different values and various effects (charging and/or discharging), however all FCs are coupled and it is not possible to influence only a selected set of FCs.

Conversely, when the output current is zero, the net charge exchange of each FC over the entire transition is approximately zero. Therefore, a novel method to balance the FC voltages by means of cell multiple switching (CMS) is proposed. CMS utilizes the fact that during zero-current hard-switching of a switch, the commutation loop current leads to an exchange of charge (subtraction of charge in cell's input-side capacitor and addition of that charge to the output-side capacitor) which is equal to the charge finally stored in the switch's parasitic capacitance. By adding additional switching actions during a Q2L transition, the FC voltages can be adjusted which can be utilized in active balancing methods.

7

Balancing of Flying Capacitors in Q2L Operation

This chapter summarizes the major research findings also published in:

- **P. Czyz**, P. Papamanolis, F. Bruguera, T. Guillod, F. Krismer, V. Lazarevic, J. Huber, and J. W. Kolar, "Load-Independent Voltage Balancing of Multi-Level Flying Capacitor Converter in Quasi-2-Level Operation," *Electronics*, vol. 10, no. 19, pp. 1-31, 2021.

Executive Summary

To ensure equal voltage sharing among the switches in a quasi-2-level (Q2L) operated multi-level flying capacitor converter (FCC), the flying capacitor (FC) voltages must be balanced at all times. Using the description of resulting charge and voltage increments in FCs during Q2L switching transitions, derived in **Chapter 6**, a concept for load-independent balancing of FC voltages of Q2L-FCCs is proposed: for non-zero load current a model of the FC voltages for a predictive control (MPC) approach is used to identify the commutation sequence of the individual switches within a Q2L transition that minimizes the FC or cell voltage errors. In case of zero load current, a novel MPC-based approach using cell multiple switching (CMS) is employed, i.e., the insertion of additional zero-current commutations within a Q2L transition to exchange charge between the FCs via the charging of the switches' parasitic capacitances. The proposed methods are thoroughly analyzed and then comprehensively verified using a 5-level FCC half-bridge demonstrator. The experiments confirm the validity of the employed models and good FC voltage tracking performance and symmetrized switch blocking voltages.

In the quasi-2-level (Q2L) operated flying capacitor converter (FCC), the charge of a flying capacitor (FC) is proportional to the product of the delay time, i.e., time allocated for the transition of an individual cell, and the local maximum of the output current of the FCC-based half-bridge. Furthermore, the available switching sequences, i.e., the order in which the individual FC cells are commutated, enable either the same value and sign of charge change in all FCs, or provide charges of different values and various effects (charging and/or discharging). However, all FCs are coupled and it is not possible to influence only a selected set of FCs.

On the other hand, when the output current is zero, the net charge exchange of each FC over the entire transition is approximately zero. To tackle the balancing during zero output current operation, in **Chapter 6** a novel method to balance the FC voltages by means of *cell multiple switching* (CMS) has been proposed. CMS utilizes the fact that during zero-current hard-switching of a switch, the commutation loop current leads to an exchange of charge which is equal to the charge stored in the switch's parasitic capacitance. By adding additional switching actions during a Q2L transition, i.e., CMS events, the FC voltages can be adjusted which can be utilized in active balancing methods.

Recently, the evaluation of Q2L modulation, including the selection of the number of levels, dimensioning of FCs, switching frequency and modulation index have been considered in [150]. In [148], methods of FC voltage balancing through adaptation of delay times without using redundant switching sequences are presented for a Q2L-operated 5-level FCC (Q2L-5L-FCC). In this context, *switching sequence* refers to the order in which the individual FC cells are commutated during a single Q2L transition. The authors of [149] present a balancing algorithm incorporating all switching sequences based on FC voltage errors by prioritizing the FC with the largest voltage error. As shown in [149] due to the opposite voltage ripple on FCs, the switches can by unbalanced by a maximum peak-to-peak voltage ripple that leads to a strong asymmetry of the switches' blocking voltages. To mitigate this asymmetry, further investigations of active balancing methods are required, and experimental verification of such methods, which, to the knowledge of the author, is so far missing in literature, is needed. In addition, so far no method to ensure voltage balancing in no-load operation, i.e., with zero output current, has been presented.

In this context, in [146] a Q2L-5L-FCC half-bridge has been proposed and the fundamental description of Q2L operation as well as the passive and active balancing of the FC voltages for a Q2L-3L-FCC has been provided. Addressing

the need discussed above, this chapter generalizes these analyses and proposes a new, comprehensive concept for load-independent FC voltage balancing of Q2L-FCC bridge-legs, which so far is lacking in the literature. Similarly, literature so far does not report experimentally validated Q2L operation of FCC bridge-legs with non-sinusoidal (i.e., DC) or even zero output currents. This chapter addresses this need by providing a comprehensive experimental validation of the proposed concept for load-independent FC voltage balancing. This concept comprises an original method of active cell voltage balancing using all switching sequences and it includes a novel method to balance the FC voltages even without a load current flowing (e.g., during start-up). **Figs. 6.2(a)** presents the considered 5L-FCC.

In this regard, **Section 7.1** briefly recapitulates the open-loop (passive) balancing method of FCs proposed in [146], before then **Section 7.2** presents the novel concept of load-independent closed-loop FC voltage balancing using a model predictive controller (MPC) with FC voltage or cell voltage reference tracking. **Section 7.3** covers the 5L-FCC hardware demonstrator used to experimentally validate the proposed concepts. The experimental results are presented and discussed in **Section 7.4**.

7.1 Open-Loop FC Balancing

As described earlier in [146], the balancing of the FC voltages can be achieved with a passive modulation that employs consecutive sequences, hence either by charging or discharging all FCs with the same charge increment during a Q2L transition, see **Tab. 6.1**. For a versatile HB realization, i.e., designed for operation with asymmetrical or symmetrical output currents, the following modulation scheme has been proposed:

$$\mathcal{S}_{\mathrm{OL}} = \{SEQ_{1234}, SEQ_{1234}, SEQ_{4321}, SEQ_{4321}, \ldots\}. \tag{7.1}$$

The scheme results in open-loop balancing over two switching periods (4 Q2L transitions). However, the maximum peak-to-peak voltage ripple is

$$\Delta V_{\mathrm{pp}} \approx 2\frac{T_{\mathrm{delay}} \cdot I_{\mathrm{o,max}}}{C_{\mathrm{FC}}}, \tag{7.2}$$

due to the charging characteristic with asymmetric currents. Please refer to [146] for an in-depth discussion.

Whereas in principle this modulation scheme is sufficient to achieve balanced FC voltages, the controllability is limited and results in a non-optimal

FC voltage ripple. Advantageously, this approach does not require FC voltage measurements. On the other hand, balancing resistors connected in parallel to the switches are necessary to ensure balanced FC voltages in case of zero output current. This approach is hereinafter referred to as open-loop (OL) balancing and experimental evaluation is provided in **Section 7.4.2**.

7.2 Load-Independent Closed-Loop Balancing

In this section a concept for load-independent closed-loop (CL) balancing is proposed. The most straightforward approach is to implement a controller which uses measurements of the FC voltages and of the output current to achieve close tracking of the FC voltage references. However, as indicated in [149] due to the opposite voltage ripple on FCs, the switches can be operated with a strong asymmetry of the blocking voltages. To address this issue, alternatively the controller can be built to equalize the cell voltages, derived as differences between the voltages of capacitors adjacent to the switches, and hence ensuring equal voltage sharing among the series-connected switches. The two aforementioned approaches are presented in detail in **Section 7.2.1**. Furthermore, the proposed balancing concept is eventually implemented and tested, see **Section 7.4**.

Fig. 7.1(a) shows the block diagram of a FCC HB with Q2L voltage balancing controller. The measured HB output current i_o is fed to the output quantity controller which specifies the reference output voltage V_o^* for the modulator and the Q2L voltage balancing controller. The design and realization of the output quantity controller is decoupled from Q2L operation and not within the scope of this thesis. For that reason, the considered Q2L-FCC is operated with a fixed duty cycle of $d = 50\%$ in the following.

As mentioned before, a given switching sequence affects several FC voltages, i.e., they are coupled through the selection of the sequences. Therefore, controlling all FC voltages is a multiple-input multiple-output (MIMO) control problem. MIMO systems can be easily addressed by model predictive control (MPC) which is formulated in the time domain [157, 158]. Therefore, MPC with reference tracking is used to realize a Q2L voltage balancing controller.

Essentially, based on the slope of reference output voltage V_o^*, the measured FC voltages $v_{\mathrm{FC1}}, \ldots, v_{\mathrm{FCj}}$, the measured output current i_o, and the DC-link voltage v_dc, the Q2L voltage balancing controller selects a switching sequence SEQ and respective times T_delay, T_p, which are the input to the actual Q2L modulator. **Fig. 7.1(b)** presents the detailed block diagram of the controller which contains two distinct parallel paths (sub-controllers), i.e., one for

control without load current using CMS ($i_o = 0$, based on FC voltage tracking, see **Section 7.2.1**) and one for operation with non-zero load current ($|i_o| > 0$, based on cell voltage tracking, see **Section 7.2.1**). The implementation of these sub-controllers is explained in the following subsections. In the last part of the Q2L controller, based on the value of i_o, the multiplexer decides which of the two sub-controllers is activated.

Ultimately, both controllers define a certain commutation sequence (SEQ) for a given Q2L transition (e.g., $SEQ = 123(33)4$ for the example shown in **Fig. 6.7**) and also the values for T_{delay} and T_p to be used. During the Q2L transition, the modulator translates this information into gate signals for the individual switches according to the state machine shown in **Fig. 7.2**.

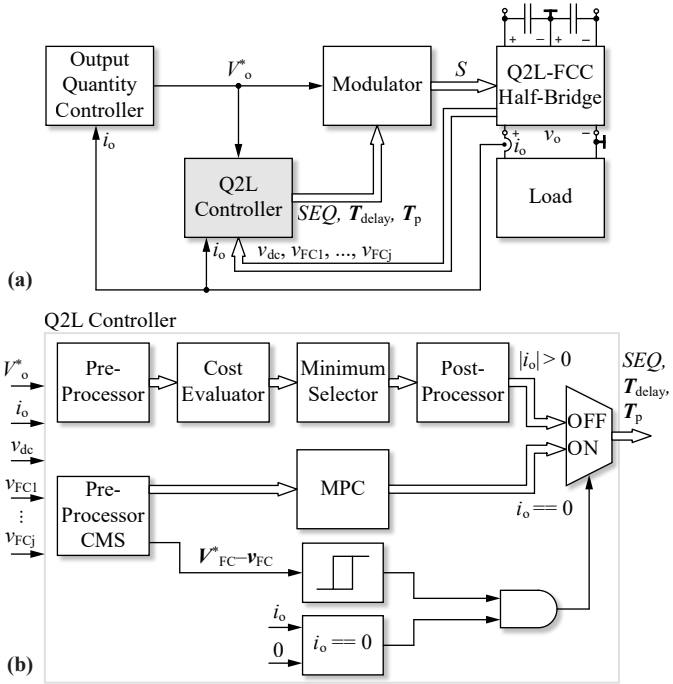


Fig. 7.1: (a) Block diagram of a FCC HB with Q2L voltage balancing controller and modulator. Note that the output quantity (e.g., load current) controller is not in this thesis' scope and hence we consider an exemplary fixed duty cycle of $d = 50\%$. **(b)** Control block diagram of the proposed load-independent Q2L voltage balancing controller.

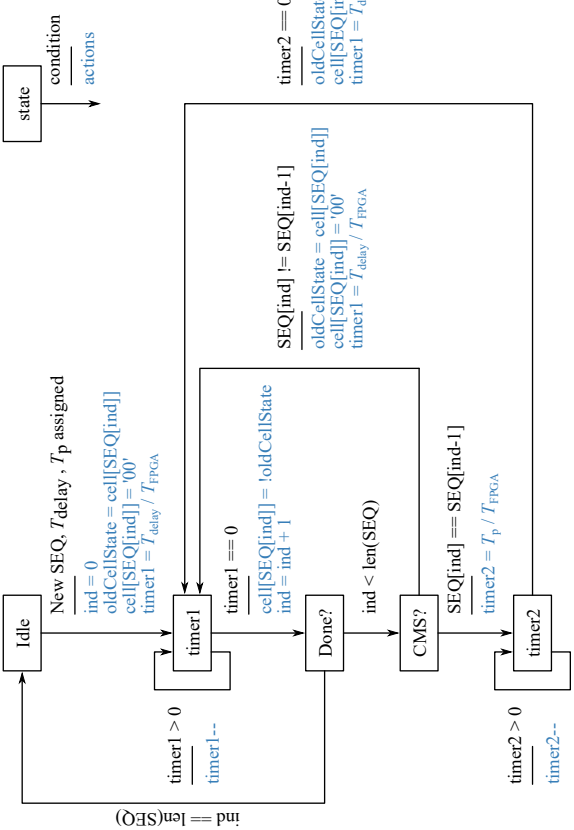


Fig. 7.2: Detailed state machine of the modulator shown in **Fig. 7.1(a)**. `Cell[i]` stores the two gate signals of the two switches of cell i; T_{FPGA} denotes the FPGA clock period. Note that T_{delay} and T_p are shown as scalars for simplicity (i.e., all commutations within one Q2L transition use the same values), but it would be possible to specify vectors indexed by `ind` such that individual values for each commutation could be used.

7.2.1 Closed-Loop Control with Non-Zero Output Current

In [146] we have proposed an active method for FC voltage balancing in a Q2L-3L-FCC. This method relies on the determination of an optimal ripple of v_{FC} and then the computation of individual delay times that eliminate any voltage ripple error in the next transition, similarly to a deadbeat controller. This method is however complex and computationally expensive for FCC realizations with $N > 3$: for each of the $(N-1)!$ available sequences, $(N-1)$ different delay times for $(N-2)$ FCs need to be considered. For that reason, in this work we propose a different approach that still utilizes all available sequences. However, to limit the degrees of freedom, we make the following simplifications:

- All delay times in a given switching transition are equal, i.e., $T_{\text{delay1}} = T_{\text{delay2}} = T_{\text{delay3}} = T_{\text{delay4}} = T_{\text{delay}}$.
- Two discrete delay time values are used: $T_{\text{delay}} \in \{T_{\min}, T_{\max}\}$, where $T_{\min}$ is intended to be selected by the controller in the steady-state in order to keep the voltage ripple small. On the other hand, $T_{\max}$ is selected in cases of significant unbalance to reduce the error more aggressively.

For the exemplary 5L-FCC, there are thus only 48 different possible actions that the controller needs to consider (24 unique sequences × 2 unique delay times). Note that with a higher number of levels, the number of possible actions increases substantially, as does the computation effort. However, to reduce the computation effort, the solution to the optimization problem can be solved offline and stored in a look-up table (LUT), see more details of implementation presented in **Section 7.2.2**.

As presented in **Section 6.2.1** the charge increments in the FCs occur during the switching transition only, whose duration is relatively short compared to the switching period. Therefore, a discrete time domain with constant sampling interval $k(0.5T_s)$ is defined, where $k \in \mathbb{N}$ denotes the time steps, cf. **Fig. 7.3a**. Note that this simplified expression is valid for a fixed duty cycle of 50 % only. For realizations with variable duty cycle, the sampling intervals would need to be changed such that the sampling instants coincide with the Q2L transitions. **Fig. 7.3b** shows the timing of the measurement data acquisition and the control routine execution in the FPGA within the highlighted Q2L transition. It can be noticed that the measured value of the

output current is delayed by a measurement delay T_{ADC} due to analog-to-digital conversion (ADC). Furthermore, T_{comp} denotes the delay resulting from performing the required computations in the FPGA. For the experimental system considered in this thesis (cf. **Section 7.3** for details) the total delay amounts to approx. 600 ns and the deviation between the measured current used for the controller execution and the current value present during the

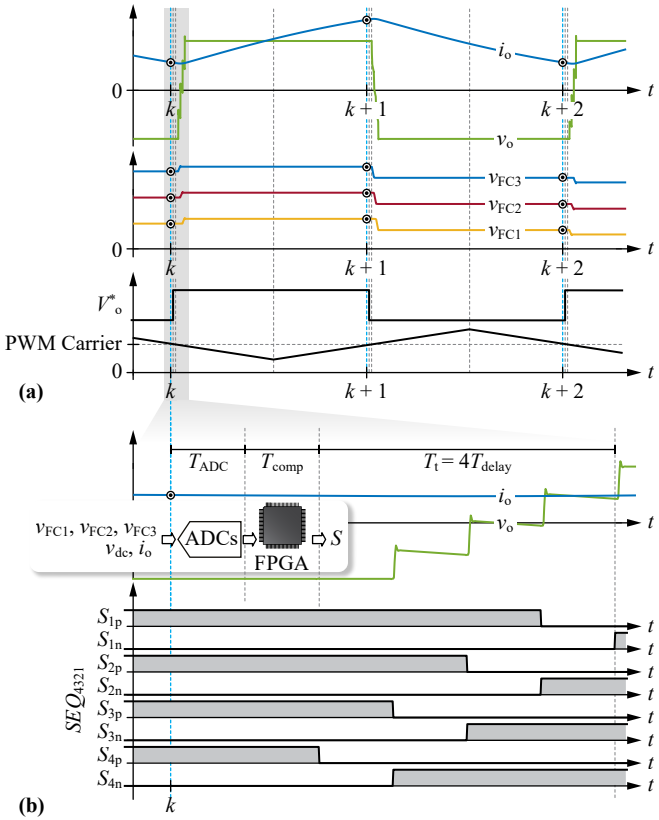


Fig. 7.3: (a) Simulation results illustrating the PWM carrier, output voltage switching transition reference V_{o}^{*} and main waveforms. Note that the ADCs are triggered shortly before the switching transition. **(b)** Gate signals, output voltage and current waveforms at discrete time step k including the delay times introduced by the ADC conversion and FPGA computation.

actual switching transition is found to be less than 2.6 %; therefore no delay compensation is employed.

FC voltage tracking

In this approach the proposed MPC relies on the model of the voltage increment (cf. (6.5)) to predict the future FC voltages,

$$\boldsymbol{V}_{\mathrm{FC}}(k+1) = \boldsymbol{V}_{\mathrm{FC}}(k) + \Delta\boldsymbol{V}_{\mathrm{FC}}(k), \tag{7.3}$$

where

$$\boldsymbol{V}_{\mathrm{FC}} = \begin{bmatrix} v_{\mathrm{FC}1} & \dots & v_{\mathrm{FC}\{j\}} \end{bmatrix}^T \tag{7.4}$$

and it depends on the available control actions and input variables:

$$\Delta\boldsymbol{V}_{\mathrm{FC}}(k) = f_1(V_{\mathrm{o}}^*, \mathcal{S}_{\mathrm{CL}}, \boldsymbol{T}_{\mathrm{delay}}, i_{\mathrm{o}})(k). \tag{7.5}$$

In order to keep the computation effort low and eliminate the need to predict the future output current, a one-step prediction horizon is used, i.e., $N_{\mathrm{p}} = 1$, which is found to provide sufficient performance. The control problem at time step k of tracking the FC voltage reference can be mapped into the cost function:

$$J_1 = \sum [(\boldsymbol{V}_{\mathrm{FC}}^* - \boldsymbol{V}_{\mathrm{FC}}(k+1))^2], \tag{7.6}$$

using the squared 2-norm, where

$$\boldsymbol{V}_{\mathrm{FC}}^* = \frac{V_{\mathrm{dc}}}{N-1} \begin{bmatrix} 1 & 2 & \dots & j \end{bmatrix}^T \tag{7.7}$$

$$= V_{\mathrm{dc}} \begin{bmatrix} 1/4 & 1/2 & 3/4 \end{bmatrix}^T, \text{ for } N = 5. \tag{7.8}$$

Using the squared 2-norm, possible control actions that would lead to large voltage deviations and hence poor reference tracking are heavily penalized, which ultimately ensures good tracking performance. The optimization problem can be stated as

$$[SEQ_{\mathrm{opt}}(k), \boldsymbol{T}_{\mathrm{opt}}(k)] = \text{arg minimize } J_1 \tag{7.9a}$$

$$\text{subject to } \boldsymbol{T}_{\mathrm{delay}} \in \mathbf{1}_{1,\mathrm{n}} \times \{T_{\min}, T_{\max}\} \tag{7.9b}$$

$$SEQ(k) \in \mathcal{S}_{\mathrm{CL}} \tag{7.9c}$$

Cell voltage tracking

In the second approach, to ensure well defined voltage levels across the switches, the controller is built to equalize the cell voltages,

$$\boldsymbol{V}_{\text{cell}} = \begin{bmatrix} v_{\text{FC}_1} \\ v_{\text{FC}_2} - v_{\text{FC}_1} \\ \cdots \\ v_{\text{dc}} - v_{\text{FC}\{j\}} \end{bmatrix}, \tag{7.10}$$

instead of the FC voltages. Note that unlike the FC voltages, all cell voltages are ideally equal. Using the cell voltage increments defined as

$$\Delta\boldsymbol{V}_{\text{cell}} = \begin{bmatrix} \Delta V_{\text{cell}_1} \\ \Delta V_{\text{cell}_2} \\ \cdots \\ \Delta V_{\text{cell}\{n\}} \end{bmatrix} = \begin{bmatrix} \Delta V_{\text{FC}_1} \\ \Delta V_{\text{FC}_2} - \Delta V_{\text{FC}_1} \\ \cdots \\ -\Delta V_{\text{FC}\{j\}} \end{bmatrix}, \tag{7.11}$$

the MPC can predict the cell voltages at the next time step as

$$\boldsymbol{V}_{\text{cell}}(k+1) = \boldsymbol{V}_{\text{cell}}(k) + \Delta\boldsymbol{V}_{\text{cell}}(k), \tag{7.12}$$

which, similar to (7.5), depends on the available control actions and input variables

$$\Delta\boldsymbol{V}_{\text{cell}}(k) = f_2(V_{\text{o}}^*, \mathcal{S}_{\text{CL}}, \boldsymbol{T}_{\text{delay}}, i_{\text{o}})(k). \tag{7.13}$$

The function f_2 maps the sequences to effects on the cell voltage increments in dependence of the delay times based on **Tab. 6.1**. Consequently, the following cost function describes the control problem of tracking the cell voltage references at time step k:

$$J_2 = \sum [(\boldsymbol{V}_{\text{cell}}^* - \boldsymbol{V}_{\text{cell}}(k+1))^2], \tag{7.14}$$

where

$$\boldsymbol{V}_{\text{cell}}^* = \frac{V_{\text{dc}}}{n} \times \mathbf{1}_{1,\text{n}}. \tag{7.15}$$

Finally, the optimization problem is stated as (7.9), however in this case minimizes the cost function J_2. Both proposed control targets, i.e., tracking of FC voltages or cell voltages, result in good FC voltage balancing performance. However, the cell voltages controller ensures more balanced and symmetrized switch voltages and is used in experiments presented in **Section 7.4**.

Regarding implementation (cf. **Fig. 7.1(b)**), first a pre-processor computes (7.12)-(7.13), i.e., based on the required v_o slope, the sign of i_o, the expected cell voltage increments $\Delta \boldsymbol{V}_{cell}$ for all combinations of sequences (cf. **Tab. 6.1**) and $\{T_{min}, T_{max}\}$ are computed and the cell voltages at time step $k+1$ are predicted. Next, the cost function (7.14) is evaluated and the optimization problem (7.9) for J_2 solved, resulting in the selection of the control action (i.e., one sequence and either T_{min} or T_{max}) with the minimum cost, i.e., leading to cell voltages at time step $k+1$ that are as close as possible to the reference values. Note that **Tab. 6.1** shows the effect on charge increments for the ZVS-type of transitions, therefore, in the last step, the post-processor by using symmetry properties, adapts the signs if the next transition is of HS-type instead (note that the transition type follows from the desired output voltage change and the output current direction). In the prototype system described below in **Section 7.3**, this control algorithm has been implemented in a high-performance Xilinx Zynq Z-7020 SoC.

7.2.2 Closed-Loop Control with Zero Output Current

As discussed in **Section 6.2.2**, CMS can be utilized to charge/discharge FCs even in case of zero output current. The following assumptions are considered for the realization of the corresponding CMS-based controller, i.e., the second path shown in **Fig. 7.1(b)**:

- The delay times T_{delay} are set to the minimum value T_{min} as their duration does not impact the balancing when $i_o = 0$.
- Similarly, the sequence of the switching actions within a Q2L transition does not influence the total voltage increments when $i_o = 0$. Therefore only the sequence SEQ_{1234} is used for simplicity when CMS is active.
- The pulse time T_p of a CMS event must be sufficiently long for a zero-current HS transition to complete. Therefore, we set $T_p = T_{min}$.

Note that using short delay and pulse times is preferable to minimize the overall transition times T_t.

The analysis presented above in **Section 6.2.2** indicates that theoretically there is an infinite number of ways to insert CMS events if the number of events inserted per Q2L transition is not limited. However, practically, it is desirable to keep the number of CMS events per transition low (duty cycle limitation) and it is found that for the considered exemplary 5L-FCC a selection of only 6 CMS sequences (given in **Tab. 7.1**) is sufficient to achieve robust

Tab. 7.1: Effect on charge increments of the FCs in dependence of different CMS events/sequences: (+1) charge, (-1) discharge, (0) no effect. Scaling the values by $2\Delta Q_S$ gives the charge increment values.

CMS events	CMS seq.	ΔQ_{FC1}	ΔQ_{FC2}	ΔQ_{FC3}
0001	$SEQ_{1234(44)}$	0	0	+1
0010	$SEQ_{123(33)4}$	0	+1	-1
0100	$SEQ_{12(22)34}$	+1	-1	0
1000	$SEQ_{1(11)234}$	-1	0	0
0011	$SEQ_{123(33)4(44)}$	0	+1	0
1100	$SEQ_{1(11)2(22)34}$	0	-1	0

controllability. The reasoning behind the selection of these CMS sequences is explained in the following.

Interestingly, it can be seen from **Tab. 7.1** that inserting a CMS event in the m^{th} cell leads to a discharge of FC_m (in case of $m = n$, the energy is exchanged with the DC-link capacitor), and charges FC_{m-1} (for $m = 1$ there is no FC to charge). Furthermore, the CMS events can be superimposed to achieve desired charge increments, e.g., events '0001' and '0010' inserted over two subsequent Q2L switching transitions yield the same effect as the same two events '0011' within one Q2L transition. However, the latter results in a longer Q2L transition time and hence a reduction of the available duty cycle. This characteristic can be used to obtain individual balancing of FCs (charge/discharge) over two Q2L transitions. Note that in the following design of the controller, for flexibility reasons, all CMS events shown in **Tab. 7.1** are used.

Similar to the approach used in case of non-zero output current, again a MPC with reference tracking over a finite prediction horizon is employed, but in this case of length $N_p = 6$, to accommodate the aforementioned superposition of CMS events in the controller. Moreover, FC voltage tracking (not cell voltage tracking) is used, because for zero output current operation, no large voltage ripples occur. Based on **Tab. 7.1** the set of available CMS sequences is defined as

$$\mathcal{U} = \{0001, 0010, 0100, 1000, 0011, 1100\}. \tag{7.16}$$

A vector of CMS sequences for the considered prediction horizon is introduced as:

$$\boldsymbol{U}(k) = \begin{bmatrix} u(k) & u(k+1) & \dots & u(k+N_p-1) \end{bmatrix}. \tag{7.17}$$

The prediction model of FC voltages is

$$\boldsymbol{V}_{\mathrm{FC,CMS}}(k+1) = \boldsymbol{V}_{\mathrm{FC}}(k) + \Delta\boldsymbol{V}_{\mathrm{CMS}}(k), \tag{7.18}$$

$$\Delta\boldsymbol{V}_{\mathrm{CMS}}(k) = f_3(\boldsymbol{\mathcal{U}})(k). \tag{7.19}$$

The control problem can be described by the cost function

$$J_3 = \sum_{l=k}^{k+N_\mathrm{p}-1} [\sum [(\boldsymbol{V}_{\mathrm{FC}}^{*} - \boldsymbol{V}_{\mathrm{FC,CMS}}(l+1))^2]], \tag{7.20}$$

and the solution to the optimization problem is the choice of $\boldsymbol{U}(k)$ that minimizes this cost function J_3:

$$\boldsymbol{U}_{\mathrm{opt}}(k) = \text{arg minimize } J_3 \tag{7.21a}$$

$$\text{subject to } \forall l = k, \ldots, k + N_\mathrm{p} - 1 \tag{7.21b}$$

$$\boldsymbol{U}(k) \in \mathbb{U}, \tag{7.21c}$$

where $\mathbb{U}$ is the $N_\mathrm{p}-$times Cartesian product of the set of CMS sequences $\boldsymbol{\mathcal{U}}$, cf. (7.16). Following the principle of receding horizon policy, only the first element of the optimal CMS sequence $\boldsymbol{U}_{\mathrm{opt}}(k)$ is applied at time step k, and another optimization is performed at the next time step.

The CMS controller (cf. **Fig. 7.1(b)**) relies on the solution to the optimization problem (7.21) which is solved offline: the FC voltage errors $(\boldsymbol{V}_{\mathrm{FC}}^{*} - \boldsymbol{V}_{\mathrm{FC}})$ as well as the expected voltage increments $\Delta\boldsymbol{V}_{\mathrm{CMS}}$ are normalized by the capacitance ratio k_c (cf. **Section 6.2.2**) and then stored in a look-up table (LUT) for the considered voltage error range. In the online implementation, the CMS pre-processor computes the voltage errors $(\boldsymbol{V}_{\mathrm{FC}}^{*} - \boldsymbol{V}_{\mathrm{FC}}(k))$ and normalizes them. This information is fed to the MPC block which retrieves the optimum solution from the precomputed LUT in the FPGA's memory. To avoid unnecessary CMS activation, especially when the FC voltages are close to the references (small errors), a voltage hysteresis is considered. Again, the online part of the algorithm has been implemented in a high-performance Xilinx Zynq Z-7020 SoC.

7.3 Hardware Implementation

In order to validate the proposed concepts, a LV proof-of-concept hardware demonstrator of a 5L-FCC HB has been designed according to the schematic

presented in **Fig. 7.4**. Depending on the connection of the load, two types of operation can be achieved (see also **Fig. 6.2)**: ① symmetrical output current with ZVS transitions, and ② asymmetrical output current ZVS and HS transitions. In order to test OL balancing, resistors R_b can be placed in parallel to the switches.

Fig. 7.5 shows the photos of the realized 5L-FCC bridge-leg demonstrator and **Tab. 7.2** summarizes the main specifications and the selected control parameters. Even though 150 V GaN e-FETs are used (EPC2033) and hence a DC-link voltage of up to 400 V would be possible, all experiments have been carried out with a reduced DC-link voltage of 100 V for safety reasons. Note that the DC voltage level does not impact the validity of the experimental verification (see also **Section 6.2.4**). The converter is operated with 50 kHz switching frequency and a fixed 50 % duty cycle. For demonstration purposes, a relatively large maximum peak-to-peak FC voltage ripple of 20 V is selected. With a maximum output current of 6.6 A and a maximum delay time of 100 ns, the required capacitance value of the FCs is 66 nF, see (7.2). The FCs are realized with COG ceramic capacitors due to their linearity (1 kV CAA572C0G3A663J640LH).

The FC voltage measurement circuitry is placed on a separate PCB that is mounted on top of the main power board (cf. **Fig. 7.5(a)**) and it can be disconnected for the tests with OL balancing. The power board, cf. **Fig. 7.5(b)** contains the switching-cell daughter boards (carrying the GaN eFETs) on top and the FCs on the bottom. Furthermore, it contains the DC-link voltage and

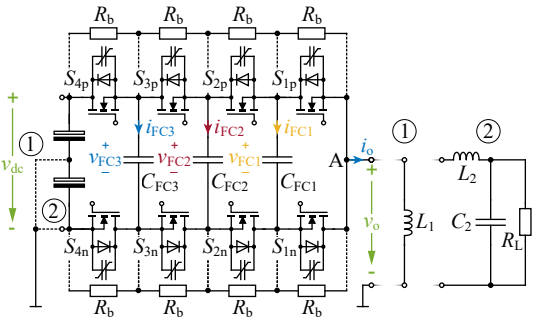


Fig. 7.4: Schematic (cf. also **Fig. 6.2)** of the 5L-FCC used in experiments with two configurations: ① split DC-link at the input and inductive load connected to the DC-link mid-point to obtain symmetrical currents; ② full DC-link at the input and LC filter with resistive load at the output to achieve asymmetrical currents.

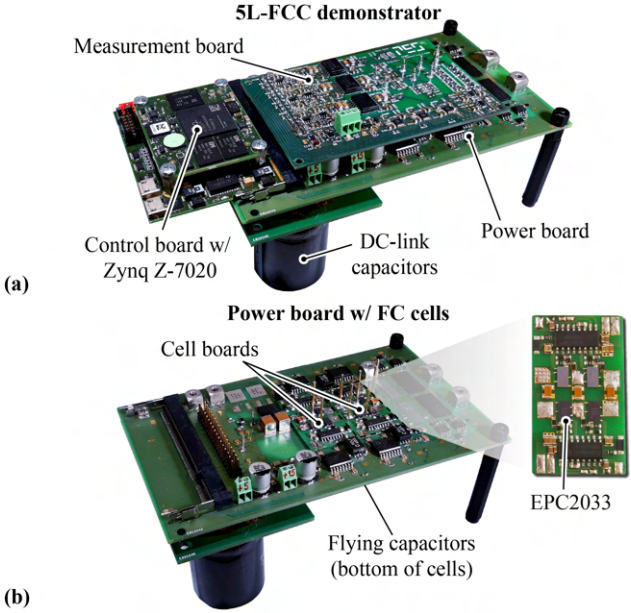


Fig. 7.5: Photos of the realized 5L-FCC HB demonstrator: **(a)** general assembly, **(b)** power board and detailed view of a switching cell PCB.

output current measurements circuitry. The Q2L controller and modulator are implemented in a high-performance Xilinx Zynq Z-7020 SoC.

7.4 Measurement Results

This section presents experimental results obtained with the 5L-FCC hardware demonstrator introduced in **Section 7.3**. In order to demonstrate the Q2L operation and the proposed concepts for FC voltage balancing, two synchronized LeCroy HDO4054A 12-bit oscilloscopes are used to measure waveforms of the DC-link voltage (v_{dc}), all FC voltages ($v_{\mathrm{FC}\{1,2,3\}}$), and the half-bridge output voltage (v_{o}) as well as the output current (i_{o}), see **Fig. 7.4**. Consequently, for each experiment two (temporally aligned) oscillograms are presented. Unless stated otherwise, resistive balancers $R_{\mathrm{b}} = 30\,\mathrm{k\Omega}$ are connected in parallel to the switches.

Tab. 7.2: Specifications and control parameters of the Q2L-5L-FCC proof-of-concept demonstrator.

V_{dc}	100 V	DC-link voltage
$I_{o,max}$	6.6 A	output current maximum
f_s	50 kHz	switching frequency
d	50 %	duty cycle
Flying capacitors		
C_{FC}	66 nF	CAA572C0G3A663J640LH
$\Delta V_{pp,max}$	20 V	max. peak-to-peak volt. ripple
Semiconductors		
S	150 V / 7 mΩ	GaN eFET EPC2033
$C_{oss,eq}$	760 pF	charge eq. capacitance
Control parameters		
$T_{t,max}$	400 ns	max. transition time
T_{min}	50 ns	min. delay time
T_{max}	100 ns	max. delay time
T_p	50 ns	pulse time

7.4.1 Q2L Transitions

First, Q2L output voltage transitions are analyzed to confirm the Q2L operation and the description of charge and voltage increments presented in **Section 6.2**. **Fig. 7.6** shows measured waveforms during the switching transition with a positive slope of v_o and negative output current ($i_o \approx I_o = -5.9$ A), which results in a ZVS transition. **Fig. 7.7** shows waveforms of the switching transition with a positive slope of v_o and positive output current ($i_o \approx I_o = 2.9$ A), which results in a HS transition. Based on the employed delay times and FC capacitance values, the voltage increments are calculated according to (6.5) and compared with the measured voltage changes (see oscillograms). The average absolute relative deviation of the estimated from the measured voltage changes is 3.7 % for ZVS (cf. **Fig. 7.6**) and 13.3 % for HS (cf. **Fig. 7.7**), thus confirming good accuracy of the estimation.

Fig. 7.8 shows an exemplary CMS sequence $SEQ_{1(11)234}$ (events in cells '1000') during a switching transition with negative slope of v_o and zero output current. It can be seen that the voltage change of FC_1 is about −0.7 V, whereas the expected voltage change calculated with (6.12) is −0.8 V, again

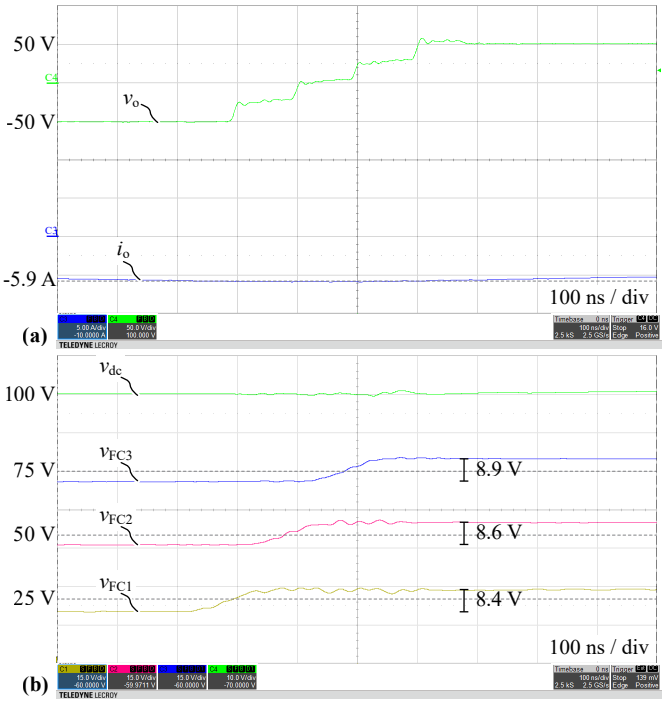


Fig. 7.6: Measured waveforms for Q2L-5L-FCC in configuration ① with negative output current ($I_o = -5.9$ A) during the switching transition with positive slope of v_o, which results in a ZVS transition: **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time of $T_{delay} = 100$ ns is used.

showing good agreement with a deviation of 13 % between calculation and measurement. Moreover, it can be noticed that also the voltages of FC_2 and FC_3 change slightly, i.e., by -0.11 V and -0.19 V, respectively, which is due to the non-idealities of the circuit.

7.4.2 Open-Loop Balancing

Next, measurement results confirming the OL balancing concept proposed in [146] and briefly described in **Section 7.1** are presented. The modulation scheme from (7.1) is implemented with $T_{delay} = 100$ ns for all cells. Consequently, all of the capacitors are charged/discharged with the same charge

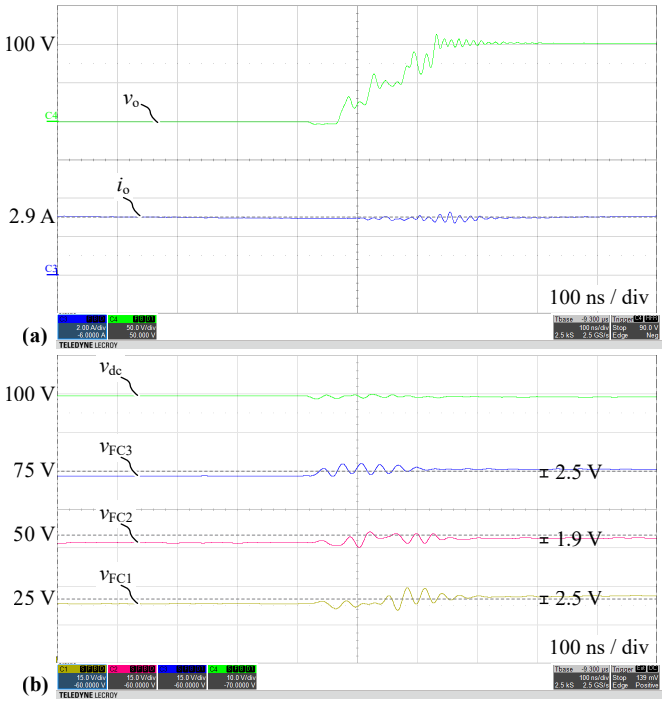


Fig. 7.7: Measured waveforms for Q2L-5L-FCC in configuration ② with positive output current ($i_o = 2.9\,\text{A}$) during the switching transition with positive slope of v_o, which results in a HS transition: **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time of $T_{delay} = 50\,\text{ns}$ is used.

value in each transition, and open-loop balancing over two fundamental switching periods is achieved.

Fig. 7.9 shows measured waveforms for split DC-link configuration with OL balancing and triangular current ($I_{o,max} = 7.0\,\text{A}$, $I_{o,min} = -5.8\,\text{A}$). The average absolute relative deviation of the estimated peak-to-peak voltage ripple (19.4 V, cf. (7.2)) from the measured value is 3 %, which corroborates the proposed model. However, note that in steady-state the mean values of the FC voltages deviate from the reference values (cf. (7.7)), on average by 4.9 V (15 %). This is a consequence of the circuit's equivalent impedances formed by the switches and the resistive balancers.

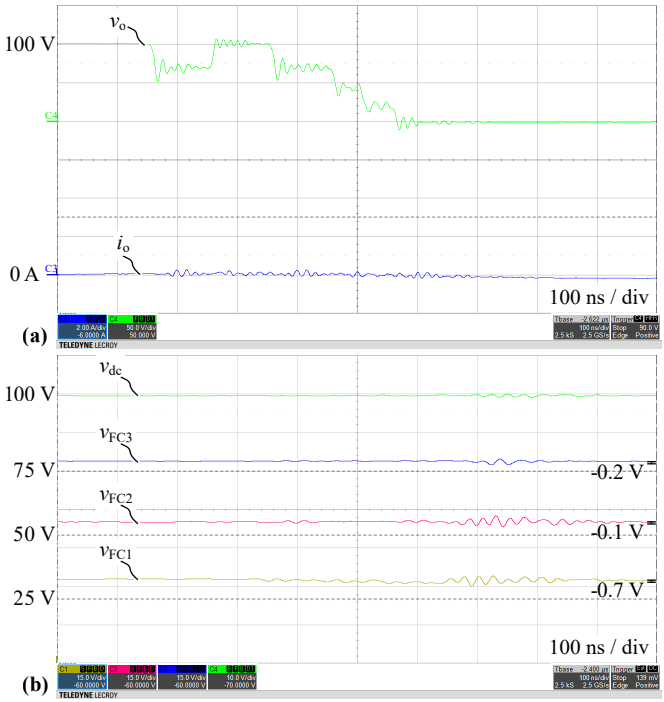


Fig. 7.8: Measured waveforms for Q2L-5L-FCC in configuration ② with zero output current ($I_o = 0\,A$) during the switching transition with negative slope of v_o and CMS sequence $SEQ_{1(11)234}$ (events in cells '1000'): **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. Delay times and pulse time $T_{delay} = T_p = 50\,ns$ are used.

Fig. 7.10 presents measured waveforms for full DC-link configuration with OL balancing during a negative load step from 100% to 67% of nominal load ($I_o = 4.6\,A \rightarrow 3.0\,A$, $\Delta I_{pp} = 4\,A$). Note that balancing is maintained despite the transient at the FCC bridge-leg's output. It can be concluded that even without closed-loop voltage balancing, load steps within the nominal load range are not critical regarding FC voltage balancing thanks to correctly dimensioned FCs.

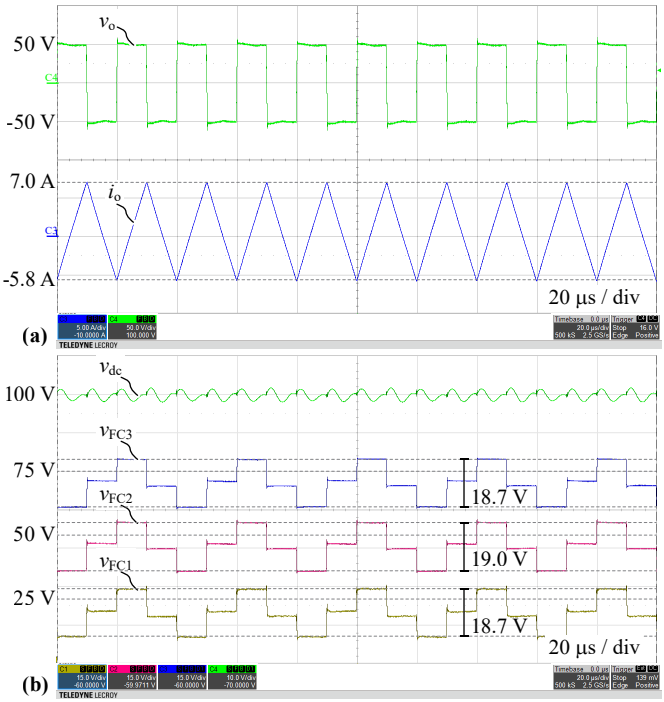


Fig. 7.9: Measured waveforms for Q2L-5L-FCC in configuration ① with OL balancing and triangular current ($I_{o,max} = 7.0\,A$, $I_{o,min} = -5.8\,A$): **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time $T_{delay} = 100\,ns$ is used.

7.4.3 Closed-Loop Balancing

This section presents experimental verification of the CL balancing concept proposed in **Section 7.2**. First, operation with non-zero load currents is demonstrated, cf. **Section 7.2.1**, where the cell voltage tracking MPC with horizon one, see (7.11)-(7.15), is employed and $T_{delay} = \{50, 100\}$ ns for all cells is used. Next, for the operation with zero load current, the FC voltage tracking MPC with a horizon of six steps ($N_p = 6$) is employed, see (7.16)-(7.21), and $T_{delay} = T_p = 50\,ns$ are used, cf. **Section 7.2.2**.

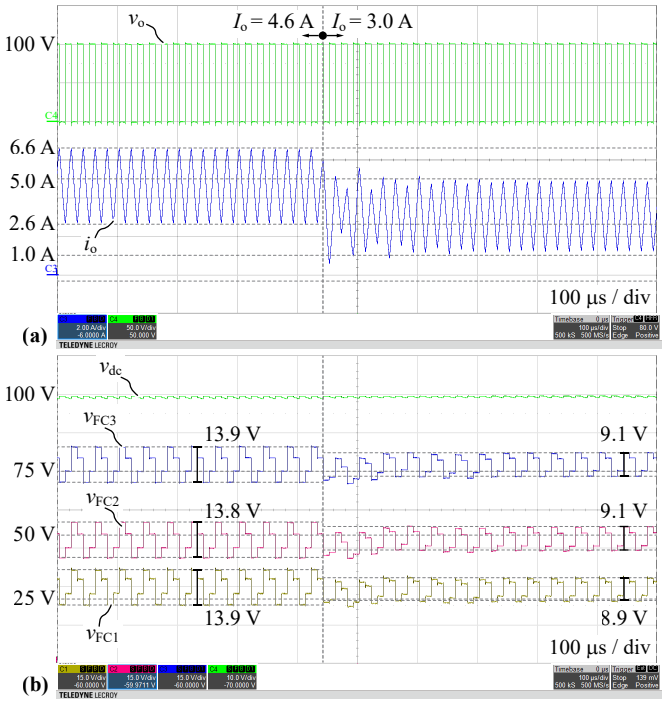


Fig. 7.10: Measured waveforms for Q2L-5L-FCC in configuration ② with OL balancing during a negative load step from 100% to 67% of nominal load ($I_o = 4.6\,\text{A} \rightarrow 3.0\,\text{A}$, $\Delta I_{pp} = 4\,\text{A}$): **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage (v_{dc}) and FC voltages $v_{FC\{1,2,3\}}$. A delay time $T_{delay} = 100\,\text{ns}$ is used.

Balancing with non-zero output current

Fig. 7.11 shows measured waveforms for split DC-link configuration with CL balancing and triangular current ($I_{o,max} = 5.9\,\text{A}$, $I_{o,min} = -5.8\,\text{A}$). The average absolute relative deviation of the estimated peak-to-peak voltage ripple (4.5 V) from the measured value is 11 %, which again corroborates the proposed model. Note that compared to OL balancing, an approx. 4× smaller peak-to-peak voltage ripple is achieved for the following two reasons. First, with CL balancing in steady-state a minimum delay time ($T_{delay} = 50\,\text{ns}$) is selected by the optimization, whereas with OL balancing the FCs operate with voltage ripples that are characteristic for the maximum delay time ($T_{delay} = 100\,\text{ns}$), which is a consequence of the need to account for the the worst-case output

current type (cf. **Section 7.1**). Second, in OL operation balancing occurs over 4 output voltage transitions, cf. (7.1), whereas in CL balancing, the optimization is carried out in every transition, ensuring minimum FC voltage ripple. Furthermore, under CL voltage balancing, the mean values of the FC voltages deviate in steady-state from the ideal reference values (cf. (7.7)) on average only by 1.9 V (3 %), which results in more symmetric voltage sharing among the switches compared to OL balancing (cf. **Fig. 7.9**).

Fig. 7.12 presents measured waveforms for the full DC-link configuration with CL balancing during a negative load step from 100% to 67% of nominal load (similar to **Fig. 7.10**, $I_\mathrm{o} = 4.6\,\mathrm{A} \rightarrow 3.0\,\mathrm{A}$, $\Delta I_\mathrm{pp} = 4\,\mathrm{A}$). It can be seen that CL with MPC does not feature a symmetric balancing cycle of fixed length like OL, which explains why the voltage ripple shows a stochastic pattern. At a first glance, it seems as if the FC voltages in case of CL are not as well balanced as in the OL case, i.e., during nominal load operation, the maximum voltage ripples in CL are {11.4 V, 15.0 V, 8.5 V} compared to {13.9 V, 13.9 V, 13.9 V} in OL. This is, however, an intended result of the employed MPC that regulates the cell voltages (and not directly the FC voltages) and is addressed in more detail in the following.

Subsequently, **Fig. 7.13** demonstrates measured waveforms during the switch-over from OL balancing ($T_\mathrm{delay} = 100\,\mathrm{ns}$) to the CL balancing ($T_\mathrm{delay} = \{50, 100\}$ ns) in a full DC-link configuration with nominal output current $I_\mathrm{o} = 4.6\,\mathrm{A}$. It is clear that the CL balancing enables better FC voltage reference tracking. Furthermore, based on the stored waveforms, the corresponding cell voltages $\boldsymbol{V}_\mathrm{cell}$ are computed and **Fig. 7.14** presents the results. It can be observed for the OL balancing that even though the FC voltages are well balanced, the outermost cells, i.e., cell 1 and cell 4, operate with the maximum voltage ripple across their switches, whereas the middle cells (2 and 3) see an almost constant voltage. As can be seen from the example of voltage sharing on the lower arm of the HB (①, cf. **Fig. 7.14**) this leads to a large asymmetry of blocking voltages (e.g., $V_\mathrm{S1n} = 36.6\,\mathrm{V}$ and $V_\mathrm{S4n} = 15.0\,\mathrm{V}$).

On the other hand, with CL balancing (worst-case example, cf. ② in **Fig. 7.14**) the voltage sharing among the cells is symmetrical, which ensures well-defined voltage levels across the switches. To quantify those differences, the cell voltage error ($\boldsymbol{V}^*_\mathrm{FC} - \boldsymbol{V}_\mathrm{cell}$) for OL and CL intervals is analyzed and averaged for each cell over the number of considered half-periods. Considering all cells, the mean voltage deviation with CL balancing is approximately half that observed with OL balancing, i.e., 10.8 % instead of 21.8 %, respectively.

The proposed CL balancing concept compared to methods proposed in the literature, e.g., [148,149], avoids the operation with opposite voltage ripple on FCs, therefore, the switch voltages are not unbalanced by a maximum

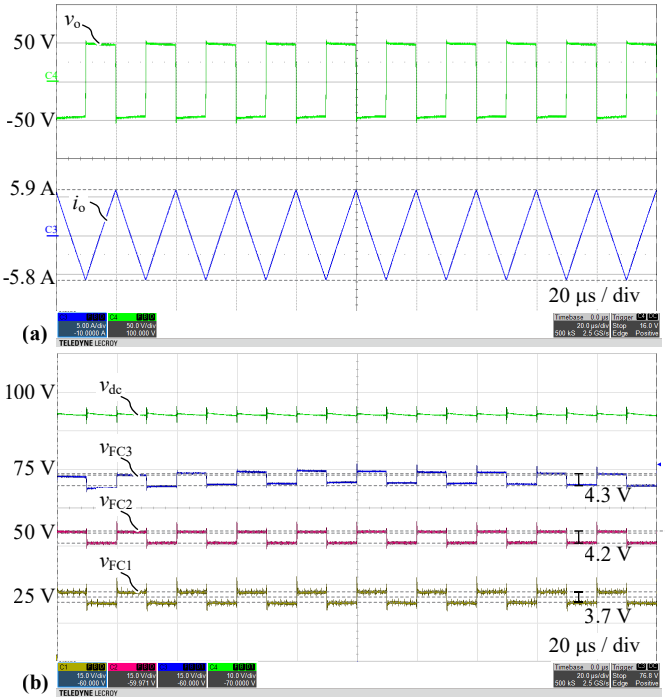


Fig. 7.11: Measured waveforms for Q2L-5L-FCC in configuration ① with CL balancing and triangular current ($I_{o,max} = 5.9\,A$, $I_{o,min} = -5.8\,A$): **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time $T_{delay} = 50\,ns$ is used.

peak-to-peak voltage ripple of the FCs, which significantly improves the symmetry of the switches' blocking voltages as shown above. This highlights the superiority of the proposed CL balancing concept.

Balancing with zero output current

Fig. 7.15 compares no-load FC voltage balancing for OL and CL balancing during full load shedding ($I_o = 5\,A \rightarrow 0\,A$) in a full DC-link configuration. **Fig. 7.15(a)** shows the operation with resistive balancers and OL balancing, whereas **Fig. 7.15(b)** illustrates the proposed CL controller concept employing CMS, cf. **Section 7.2.2**. Note the delay before CMS activation which is a consequence of the implemented hysteresis. Nevertheless, the CL controller

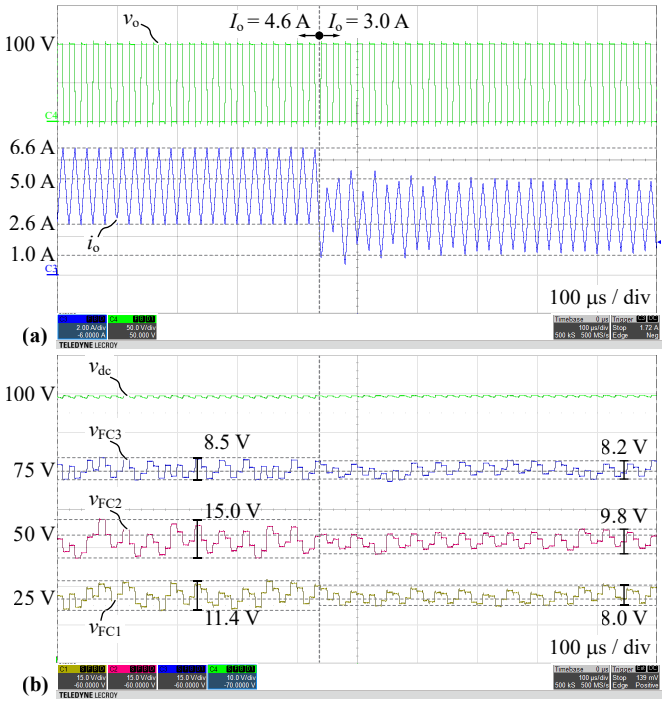


Fig. 7.12: Measured waveforms for Q2L-5L-FCC in configuration ② with CL balancing during a negative load step from 100% to 67% of nominal load ($I_o = 4.6\,\text{A} \rightarrow 3.0\,\text{A}$, $\Delta I_{pp} = 4\,\text{A}$): **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. Delay times $T_{delay} = \{50, 100\}$ ns are used.

achieves better dynamics as the steady-state is achieved after approx. 130 µs compared to appox. 540 µs settling time in case of resistive/OL balancing. It is noteworthy that the resistive balancers need to be selected considering the leakage currents of the switches and capacitors, therefore the time constant of the resistive balancing is determined by the circuitry and there are only limited tuning possibilities, especially if the losses in the balancing resistors must be limited. Furthermore, the resistive balancers are generating continuous losses, whereas in case of balancing with CMS, the zero-current hard-switching losses occur only during activation of CMS, i.e., several events at most over tens of switching transitions which leads to negligible average losses.

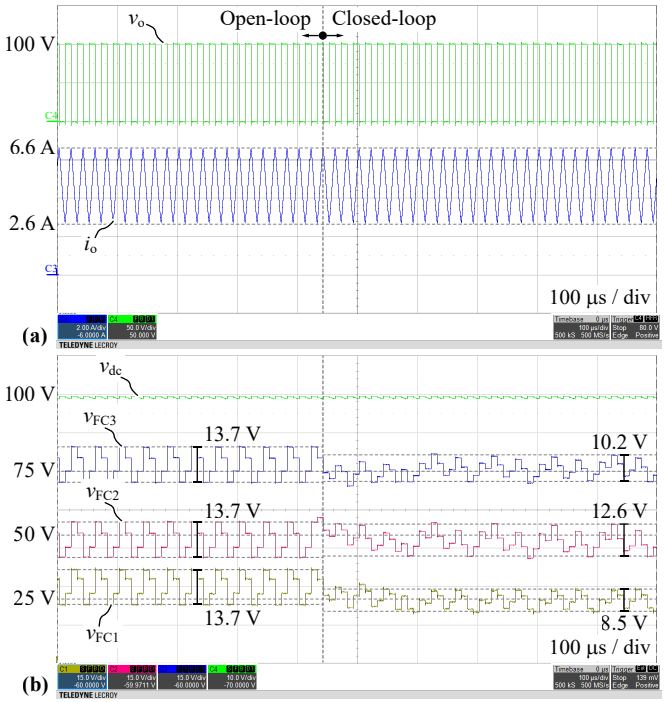


Fig. 7.13: Measured waveforms for Q2L-5L-FCC in configuration ② with transition from OL ($T_{\text{delay}} = 100$ ns) to CL ($T_{\text{delay}} = \{50, 100\}$ ns) balancing with nominal output current ($I_o = 4.6$ A): **(a)** output voltage v_o and current i_o, **(b)** DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$.

7.4.4 Start-Up and Shut-Down

In the last part of experimental validation voltage balancing during start-up and shut-down of the Q2L-5L-FCC is demonstrated. Note that in both experiments CL balancing is used.

Fig. 7.16(a)) presents measured waveforms in a full DC-link configuration with resistive balancers. The operation profile consists of the following intervals: a DC-link precharge via a resistor (disconnected load) → idle operation of Q2L-FCC after bridging the precharge resistor → connection of the load (nominal FC voltage ripple) → disconnection of the input supply and dissipation of the DC-link energy in the load. It can be noticed that the FC voltages are brought smoothly to and remain close to their reference average

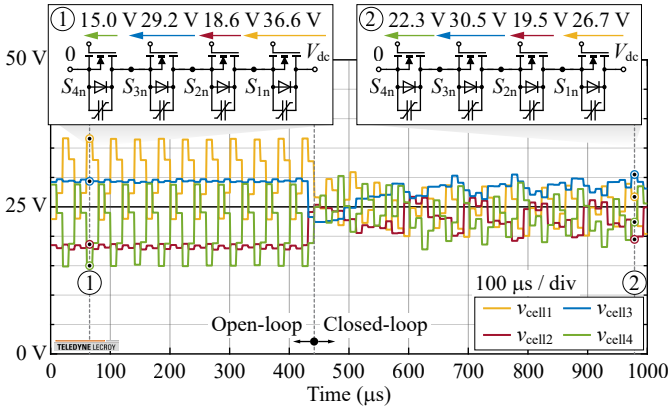


Fig. 7.14: Cell voltages $\boldsymbol{V}_{\text{cell}}$, cf. (7.11), corresponding to the experiment from **Fig. 7.13** (transition from OL to CL balancing with nominal current). Data computed and filtered from oscilloscope waveforms. Note that the ideal cell voltages should be equal to $100\,\text{V}/4 = 25\,\text{V}$.

values in the steady-state. Note that the jump in the capacitor's voltage at the transition from *precharge* to *idle* interval is caused by the bridging of the precharge resistor. Furthermore, from the start of the *idle* interval the CL controller is active.

Fig. 7.16(b) shows measured waveforms of a similar operation profile but in a split DC-link configuration without resistive balancers, however, in this case, the load is connected at all times. Again, it can be stated that the proposed CL balancing concept ensures balanced FC voltages and thus defined blocking voltage stresses on the switches in all operating modes of the Q2L-FCC.

7.5 Conclusion

This chapter presents a new, comprehensive control concept for load-independent voltage balancing of flying capacitor converters (FCCs) operated in quasi-2-level mode (Q2L-FCC). This new and fully experimentally-verified concept ensures well-defined FC voltages and equal blocking voltages across the series-connected switches with and without load current flowing in the bridge-leg's output terminal.

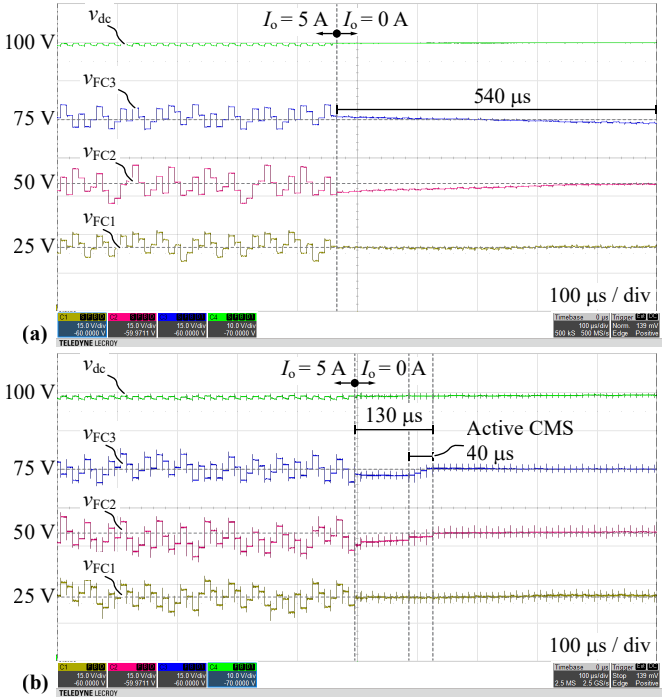


Fig. 7.15: Comparison of measured waveforms (DC-link capacitor voltage v_{dc}, FC voltages $v_{FC\{1,2,3\}}$) for Q2L-5L-FCC in a full DC-link configuration during load disconnection ($I_o = 5\,A \rightarrow 0\,A$): **(a)** OL with resistive balancers; **(b)** CL balancing with CMS. Delay times $T_{delay} = T_p = 50$ ns are used.

The proposed closed-loop voltage balancing control concept comprises two methods which are activated depending on the output current of the bridge-leg. In case of a non-zero output current, a first method of active cell voltage balancing involves a model predictive controller (MPC) that selects the most suitable sequence of FC cell commutations within a Q2L transition (1-step horizon) from all possible permutations by minimizing the predicted deviation from the reference values. On the other hand, when the output current is zero, a novel method to balance the FC voltages by means of cell multiple switching (CMS) is used. CMS utilizes the fact that during zero-current hard-switching of a switch, the commutation loop current leads to an exchange of charge (subtraction of charge in a cell's input-side capacitor

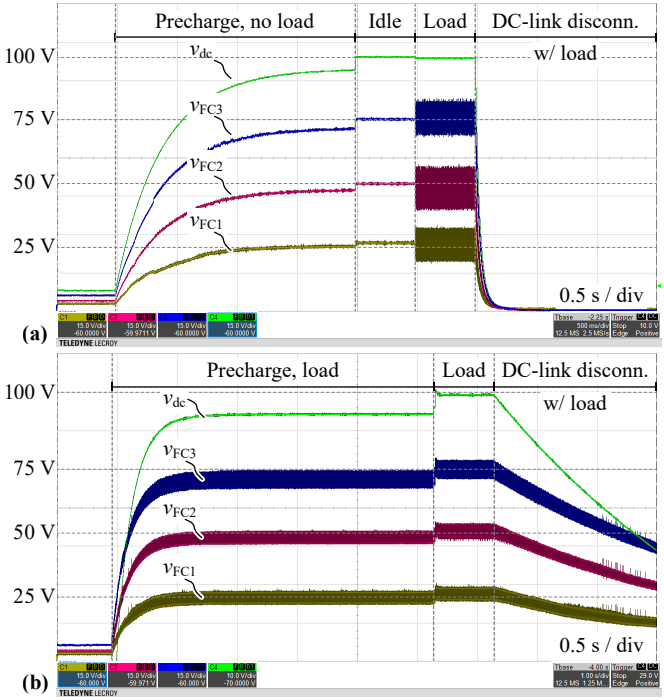


Fig. 7.16: Measured waveforms (DC-link capacitor voltage v_{dc}, FC voltages $v_{FC\{1,2,3\}}$) for start-up (precharging) and shut-down of Q2L-5L-FCC: **(a)** full DC-link configuration with resistive balancers (precharge → idle → nominal load → DC-link voltage disconnection under load). **(b)** Split DC-link configuration without resistive balancers (precharge under load → nominal load → DC-link voltage disconnection under load). Note the different time bases due to the different DC-link capacitance values used in the setups.

and addition of that charge to the output-side capacitor) which is equal to the charge stored in the switch's parasitic capacitance. By adding additional switching actions during a Q2L transition, the FC voltages can be adjusted. Again, a MPC approach is utilized to select the optimum CMS sequence, however, using FC voltage reference tracking over a 6-step horizon.

The proposed voltage balancing control concept is thoroughly validated with a 5-level FCC half-bridge demonstrator for hard-switching and soft-switching output voltage transitions, during load transients, as well as for start-up and shut-down operation modes. The hardware experiments demon-

strate an excellent average FC voltage tracking as well as symmetric cell voltages. More importantly, the results prove the validity of the proposed description of charge and voltage increments in FCs. The presented closed-loop cell voltage control concept, compared to open-loop (passive) balancing or active balancing directly controlling FC voltages, results in voltages across the switches that are close to the ideal values and optimum FC voltage ripples. The versatility of the proposed solution comes at the price of the required measurement circuitry to sense the FC voltages. In return, however, the proposed controller is computationally efficient and can be easily implemented in an FPGA, partially using offline-generated look-up tables.

The proposed closed-loop voltage balancing turns the Q2L-FCC into a robust versatile half-bridge power semiconductor stage for various hard-switched and soft-switched applications such as AC-DC rectifiers and isolated DC-DC converters, where the system voltages exceed the voltage ratings of available power semiconductors.

8

Concept of a 40 kV / 300 kVA SiC 'Super-Switch' IPM

This chapter summarizes the major research findings also published in:

- **P. Czyz**, P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "New 40 kV / 300 kVA Quasi-2-Level Operated 5-Level Flying Capacitor SiC "Super-Switch" IPM," in *Proc. of the IEEE Int. Power Electron. Conf. (ECCE Asia)*, 2019.

Executive Summary

Emerging applications, e.g., traction systems and utility scale renewable energy systems, demand for medium-voltage (MV) power electronic switches with blocking capabilities above 20 kV, which cannot be provided with today's 10 kV or 15 kV SiC power semiconductors. Therefore, this chapter investigates a flying capacitor converter (FCC) topology for the realization of a MV half-bridge. The FCC topology features several advantages such as reduced switching losses, typically, the total chip area is significantly lower, lower average $\mathrm{d}v/\mathrm{d}t$ of the switching transitions, and robust voltage balancing. Moreover, the volume of the flying capacitors can be reduced with quasi-2-level (Q2L) operation of the half-bridge, where the intermediate voltage levels are only used during very short time intervals, i.e., during the switching transitions. This chapter analyzes the design and integration of a complete bridge-leg, including gate drivers, isolated cooling interfaces, measurements, and Q2L control into a 300 kVA / 40 kV SiC Super-Switch Intelligent Power Module (SiC-SS-IPM). Furthermore, the impact of a Q2L operation on electrical insulation is studied and compared to waveforms of a 2-level bridge-leg with series connection of MOSFETs.

8.1 Introduction

At present, solid-state transformers (SSTs) for traction and smart-grid applications are intensively discussed [12–14]. However, despite the recent availability of 10 kV or 15 kV SiC MOSFET technology, the corresponding high AC input voltages, e.g., 15 kV or 25 kV for traction applications and 13.8 kV in case of a typical medium-voltage (MV) mains in the USA [159], still represent a key challenge for converter realization. In this chapter, a 250 kW DC-DC step-down dual active bridge (DAB) converter (cf. **Fig. 8.1(a)**) is considered, which is part of the SST of a future single-phase 15 kV / 16.7 Hz traction system, where two such DAB converters could deliver the power necessary to supply axle motors in a distributed traction chain.

According to the standard [160], the SST is subject to non-permanent maximum AC grid rms voltages of 18 kV for up to 5 minutes (peak voltage of 25.5 kV), which leads to a selected input-side DC-link voltage of $V_{\mathrm{dc}} = 28\,\mathrm{kV}$. Hence, the DAB converter's MV half-bridge requires power electronic switches which withstand blocking voltages that clearly exceed the rating of today's cutting-edge 10 kV or 15 kV SiC power semiconductors. Furthermore, the peak currents in the switches are 21.5 A and the apparent switching power is 300 kVA.

As it is shown in **Chapters 6–7** quasi-2-level (Q2L) operation of multilevel bridge-legs is an interesting option for realizing single-cell power conversion as they feature minimized capacitive energy storage requirements. Moreover, compared to 2-level half-bridges employing power semiconductors with high blocking voltage ratings, lower average voltage slew rates facilitate EMI filter design and reduced isolation stress. Q2L-operated flying capacitor converters (Q2L-FCCs) are of particular interest due to the snubberless design and low number of components. Furthermore, the proposed closed-loop voltage balancing (see **Chapter 7**) turns the Q2L-FCC into a robust versatile half-bridge power semiconductor stage for both hard-switched and soft-switched applications. Therefore, with the focus of this chapter on the module integration of a complete half-bridge of the DAB converter, i.e., all power semiconductors, commutation capacitors, gate drivers, control and measurements, isolated gate driver power supplies, and isolated cooling surfaces, are accommodated in a *SiC Super-Switch Intelligent Power Module* (SiC-SS-IPM), a Q2L-FCC topology is selected for the realization.

Thus, the dimensioning of semiconductors and capacitors for the considered Q2L-FCC based SiC-SS-IPM is presented and in particular their volumes are evaluated in **Section 8.2**. Moreover, **Section 8.3** evaluates the impact of

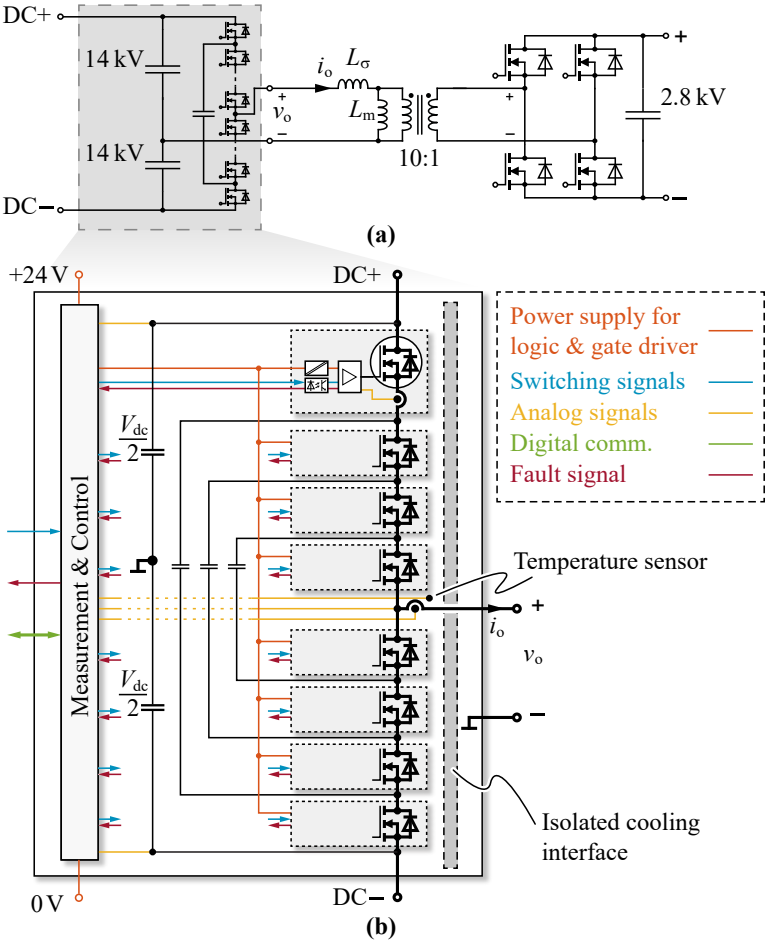


Fig. 8.1: (a) Considered 28 kV / 2.8 kV step-down 250 kW DAB converter and **(b)** block diagram of the proposed SiC Super-Switch Intelligent Power Module (SiC-SS-IPM) used to realize the MV half-bridge of a DAB converter. The half-bridge module is realized with a 5-level Flying Capacitor Converter (FCC) operated with quasi-2-level (Q2L) modulation; power switches, gate drivers, flying capacitors, commutation capacitors, measurements, and control are integrated in the module such that the Q2L commutations can be triggered by a single optical signal.

Q2L operation on the electrical insulation in comparison to a 2-level bridge-leg realized with direct series connection of MOSFETs.

8.2 Design of the 5-Level Q2L-FCC based SiC-SS-IPM

This section provides an evaluation of the Q2L-FCC bridge-leg considering the semiconductors and the capacitor volumes. In addition, the integration of the Q2L-FCC half-bridge into the SiC-SS-IPM is shown. The proposed Q2L-FCC is part of a DAB converter as depicted in **Fig. 8.1**, with specifications as listed in **Tabs. 8.1**.

8.2.1 Power Semiconductors

Each die of the used SiC MOSFETs [36] features a blocking voltage of 10 kV, an on-state resistance of $R_{\mathrm{ds,on}} \approx 550\,\mathrm{m\Omega}$ (at $T_{\mathrm{j}} = 150^{\circ}\mathrm{C}$,) and a linearized charge equivalent capacitance of $C_{\mathrm{oss,eq}} = 200\,\mathrm{pF}$ [39]. Two parallel dies per switch are considered in order to reduce the conduction losses. With this, $280\,\mathrm{ns} < T_{\mathrm{ZVS}} < 1\,\mu\mathrm{s}$ applies for $21.5\,\mathrm{A} > i_{\mathrm{o}} > 6\,\mathrm{A}$. Thus, with $T_{\mathrm{delay}} = 1\,\mu\mathrm{s}$, ZVS is achieved in a wide load range and the total output voltage transition time remains reasonable: $T_{\mathrm{t}} = nT_{\mathrm{delay}} = 4\ \mu\mathrm{s}$.

The 5-level Q2L-FCC requires 8 MOSFETs and/or 16 dies. In this regard, a Q2L-operated modular multi-level converter (Q2L-MMC) based approach, the

Tab. 8.1: Specifications of the considered Q2L-5L-FCC based 40 kV / 300 kVA SiC-SS-IPM.

(a) SiC MOSFET package with 2 parallel dies		
$V_{\mathrm{ds,max}}$	10 kV	max. blocking voltage
$I_{\mathrm{ds,max}}$	2×18 A	max. drain current
$R_{\mathrm{ds,on}}$	550 mΩ / 2	on-state res. @ 125℃
$C_{\mathrm{oss,eq}}$	2×200 pF	charge eq. capacitance
(b) 5-level Q2L-FCC specifications (40 kV / 300 kVA**)**		
n	4	devices in series
N	5	voltage levels
C_{FC}	21.5 nF	flying capacitors
V_{dc}	28 kV	DC-link voltage
$I_{\mathrm{o,max}}$	21.5 A	nominal output current

closest competitive design, would require 16 MOSFETs and a total of 16 + 8 = 24 dies, since the switches connected in series to the DC-link capacitors, cf. **Fig. 6.1(c)**, are subject to low currents in case of Q2L operation and could be realized with only one die. The higher number of MOSFETs employed in the MMC would be linked to a higher number of gate drivers and additional isolation requirements. In this regard, the redundancy featured by a Q2L-MMC-based half-bridge would come at the cost of a more expensive and complex system compared to the Q2L-FCC.

8.2.2 Capacitors

Based on (7.2), for $T_{\text{delay}} = 1\,\mu\text{s}$, a maximum instantaneous current during switching of $I_{\text{o,max}} = 21.5\,\text{A}$, and a specified peak-to-peak capacitor voltage ripple of $\Delta V_{\text{FC}} = 2\,\text{kV}$, the value of the flying capacitors are

$$C_{\text{FC}} = 2\frac{T_{\text{delay}} I_{\text{o,max}}}{\Delta V_{\text{FC}}} = 21.5\,\text{nF}. \tag{8.1}$$

With $\Delta V_{\text{FC}} = 2\,\text{kV}$, the maximum voltage applied to a MOSFET is 8 kV ($V_{\text{dc}}/n + \Delta V_{\text{FC}}/2$). However, this voltage ripple only appears for passive balancing with asymmetric currents, cf. **Section 7.1**. For passive balancing with symmetrical currents, the maximum voltage is 7.5 kV, cf. [146].

Of particular interest is the investigation of the implications of the capacitor volumes on the converter's volume. For this analysis, high voltage film capacitors are found to be most suitable, due to their high voltage ratings, low losses, and highest volumetric capacitance density, in comparison to high voltage ceramic capacitors. An algorithm analyzing combinations of different capacitors, connected in series and / or parallel, has been implemented and used for selecting the combination which yields minimum total volume. According to the results of this optimization, *HA*-type capacitors manufactured by FTCAP GmbH [161], arranged as stated in **Tab. 8.2**, are found to be optimal. However, the considered film capacitors are subject to capacitance reductions at elevated case temperatures, which is accounted for by over-dimensioning the nominal capacitance by 10%. It is found that the total boxed volume for all flying capacitors of the Q2L-FCC is only $0.30\,\text{dm}^3$. In comparison, a Q2L-MMC with similar rating would lead to a capacitor volume of $0.70\,\text{dm}^3$.

In addition to flying capacitors, also DC-link commutation capacitors are considered. For the discussed realization of a half-bridge-based Q2L-FCC, a configuration with a split DC-link is preferred. It enables the use of the mid-point as reference ground for voltage measurements to reduce the voltage stresses on the measurement circuits. Since the main, high energy DC-link

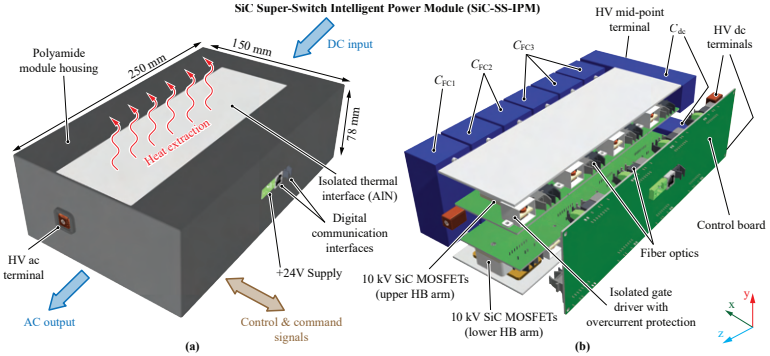


Fig. 8.2: 3–D rendering of the 300 kVA / 40 kV half-bridge SiC-SS-IPM: **(a)** external appearance and **(b)** internal layout.

has to be designed for a specific application and is located outside of the SiC-SS-IPM module, a reduced total capacitance of 12 nF is installed inside the module.

8.2.3 Realization of the SiC-SS-IPM

A 3–D model of the SiC-SS-IPM is presented in **Fig. 8.2**. The designed SiC-SS-IPM is enclosed in a polyamide housing, which is integrated with Aluminum Nitride (AlN) baseplates on top and bottom of the module to provide isolated thermal interfaces between the MOSFETs' baseplates and the external cooling system. The high voltage terminals are located on the sides of the module (labelled with "DC input" and "AC output"). The MOSFETs of the upper half-bridge arm are located on the top side and those of the lower half-bridge arm on the bottom side. This layout allows for the realization of low-inductance commutation loops that are arranged in the xy-plane. The control board implements isolated communication and isolated power supply of the module. The presented layout features a very compact design and consequently a low boxed volume of 2.9 dm^3, i.e., the presented 300 kVA / 40 kV SiC-SS-IPM features a power density of 102 kVA/dm^3. Furthermore, the SiC-SS-IPM enables scalability, e.g., a full-bridge topology could be built by stacking modules in y-axis direction, and interleaving them with a required cooling system (cold plates with heat pipes of water cooling or heat sinks).

Tab. 8.2: Flying capacitors and commutation DC-link capacitors of the 5-level Q2L-FCC.

Capacitor (nF)		Operating voltage (kV)	Rated voltage (kV)	Capacitor realization	Volume (dm^3)	Total volume (dm^3)
C_{FC1}		7	8 (surge 12)	24 nF	0.03	
C_{FC2}	$1.1 \cdot 21.5 \approx 24$	14	15 (surge 22.5)	2 parallel 12 nF	0.06	0.30
C_{FC3}		21	24 (surge 36)	3 series 72 nF	0.20	
C_{dc}	12	28	30 (surge 45)	2 series 24 nF	0.13	0.13

8.3 Impact of Q2L on the Electrical Insulation

From the design of the Q2L-FCC, presented in the previous section, it is clear that it offers a less complex, more compact, and cheaper realization than the MMC-based counterpart. In the following, it is proven that the Q2L staggered switching also offers reduced average dv/dt of the switching transitions compared to 2-level topologies (cf. **Figs. 6.1(a), (b)**) and, thus, reduces the stress on the electrical insulation and the emitted EMI disturbances.

The fast voltage transients (up to 100 kV/µs [39]) with high repetition rates (up to 100 kHz [9]), generated by MV SiC switches, have negative effects on the electrical insulation, as shown for MF transformers, HVDC converters, and inverter-fed electrical machines [126, 162–164]. Such degradations are mainly explained by the following effects:

- *Partial Discharges* - The damages inflicted to insulation materials by partial discharges are proportional to the operating frequency. Moreover, fast switching transitions increase the amplitudes of the discharges. This leads to reduced breakdown voltages and accelerated ageing [125, 126, 163].

- *Resonances* - Fast switching transitions can excite resonances inside passive components (e.g., transformers, inductors, and electrical machines) or between passive components and cables (e.g., electrical machines connected through long cables). Such oscillations create an uneven voltage sharing inside the components and/or overvoltages between the terminals [162, 165].

- *Dielectric Losses* - The dielectric losses, which are proportional to the operating frequency, cannot be neglected for MV systems operated at MF. Additionally, the associated dielectric heating can lead to thermal breakdowns or thermal runaways [126, 164].

These problems become particularly critical for the JFET super-cascode and the series connection of MOSFETs with snubbers. For these arrangements, all series connected devices are switched synchronously in order to guarantee equal voltage sharing. This implies that the switching speed at the output node of a bridge with n series connected semiconductors, each with a given dv/dt (for a defined load current), is equal to $n\,(dv/dt)$. This means that, for increasing n, the switching speed becomes problematic for the electrical insulation but also from an EMI point of view [166–168]. The limitation of

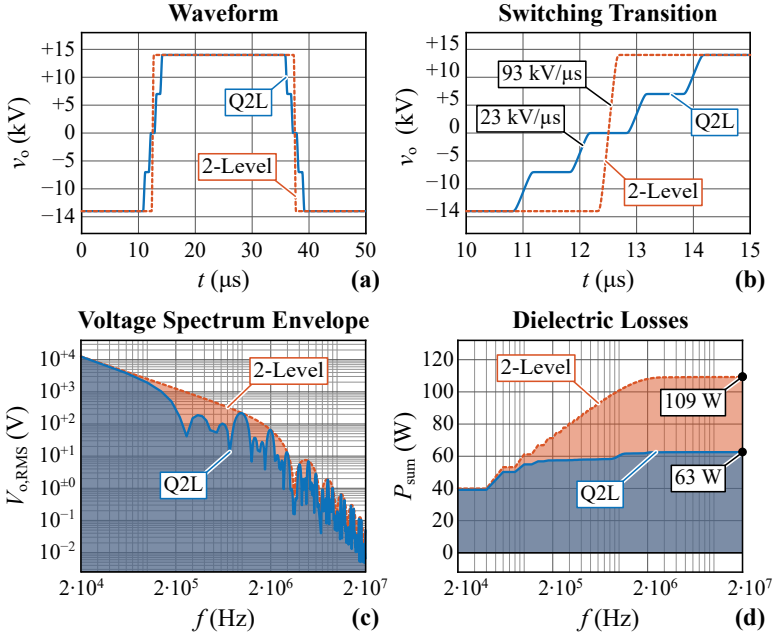


Fig. 8.3: A classical 2-level bridge-leg is compared with the proposed Q2L-FCC: **(a)** voltage waveforms, **(b)** switching transitions, **(c)** voltage spectrum envelope, and **(d)** cumulative sum of the dielectric losses. The ratings shown in **Tabs. 8.1(a),(b)** are considered and the system is operated at 20 kHz. ZVS is considered with a switched current of $I_{o,max}$. The dielectric losses are computed for a typical capacitance of 200 pF and a dissipation factor of 1 % [164].

the switching speed (by the gate drivers or with a snubber) is possible but creates substantial additional losses.

This disadvantage does not appear in the presented Q2L-FCC since the series connected devices are switched sequentially. Hence, the local dv/dt during the staggered switching transition is independent of n [166–168]. Therefore, the Q2L-FCC reduces the partial discharge amplitudes, mitigates the impacts of resonances, and reduces the dielectric losses.

Figs. 8.3(a),(b) show the obtained waveforms for a 2-level bridge-leg realized with a series connection of MOSFETs and for the 5-level-based Q2L-FCC according to the specifications in **Tabs. 8.1(a),(b)**. The obtained switching speeds are 28 kV/300 ns = 93 kV/µs for the 2-level bridge-leg and 7 kV/300 ns = 23 kV/µs for the Q2L-FCC. **Figs. 8.3(c),(d)** depict the voltage

spectrum and the associated dielectric losses, determined according to [164]. As expected, the Q2L-FCC features reduced high-frequency harmonics and, therefore, reduced dielectric losses (63 W instead of 109 W).

8.4 Conclusion

This chapter presents a new 300 kVA / 40 kV quasi-2-level (Q2L) half-bridge SiC Super-Switch Intelligent Power Module (SiC-SS-IPM), which includes all circuits for gate drivers, measurements, and control. The module implements a 5-level Flying Capacitor Converter (FCC) structure for defining the blocking voltages across the power semiconductors and the Q2L operation reduces the average voltage slew rate during switching and minimizes capacitive energy storage requirements.

Compared to the Q2L-MMC counterpart, the Q2L-FCC features a lower component count (8 devices and associated gate drivers instead of 16) and substantially lower capacitor volume. Furthermore, the Q2L-FCC achieves a lower $\mathrm{d}v/\mathrm{d}t$ of the switching transitions (23 kV/µs) than a direct series connection of MOSFETs or a JFET super-cascode (93 kV/µs) without increasing switching losses. In this regard a respective analysis is conducted and reveals that Q2L operation reduces the stress applied to the electrical insulation. Thus, the Q2L-FCC provides a balanced trade-off between complexity and practicability.

With the very compact design presented in this chapter, a low boxed volume of the overall Q2L-FCC SiC-SS-IPM concept of 2.9 dm^3 is achieved, which results in a module-specific power density of 102 $\mathrm{kVA/dm}^3$.

9 Conclusion and Outlook

With a global focus on decarbonisation of transportation, the research and development of technologies for transport electrification requires continued advancements towards increasing power density of converters and due to the high-power demand, investigations of medium-voltage (MV) connected power electronic interfaces. In this context, fuelled by the availability of wide-bandgap (WBG) SiC power semiconductors with blocking voltage ratings of up to 10 kV and beyond, solid-state transformers (SSTs) have been proposed as flexible isolation and voltage-scaling interfaces between medium-voltage (MV) and low-voltage (LV) DC or AC buses. Typical applications include high-power electric vehicle (EV) charging stations, power electronic traction transformers (PETTs), and emerging applications which comprise future ships and future aircraft with distributed propulsion and on-board MVDC grids.

Due to the aforementioned requirements of low weight or high operating voltage of SSTs, the challenges arise especially in the realization of an SST's DC-DC converter stage. In the light of these challenges, this thesis explored and identified suitable technologies for the core functional parts of the MV DC-DC SST, i.e., for a MF transformer (MFT) and a power semiconductor stage.

In the first part of the thesis, the performance limits of air-core transformers (ACTs) and magnetic-core transformers (MCTs) for a lightweight and high-efficiency 166 kW / 7 kV DC transformer (DCX) are explored. The derived models and results have been used to design, construct and test two full-rated MV/MF transformer prototypes: ACT and MCT realizations. The second part of the thesis investigates the quasi-2-level (Q2L) operation of a 5-level flying capacitor converter (5L-FCC) based half-bridge with respect to the realization of a versatile, compact and integrated power semiconductor stage for soft- and hard-switched applications, where the system voltages

exceed the voltage ratings of available power semiconductors. Based on the generic description of Q2L operation, a robust control method to balance the voltages is developed and validated in a LV 5L-FCC prototype demonstrator.

The main findings of this thesis are summarized hereafter in **Section 9.1**, while possible future research areas are discussed in **Section 9.2**.

9.1 Results of the Thesis

The main achievements of this thesis are summarized in the following:

PART 1 - **Medium-Voltage Medium-Frequency Transformers**

- *Design and performance space of MV MFTs and 1:1-DCXs* - The performance limits (gravimetric and volumetric power densities, efficiency) are found for the 166 kW / 7 kV unity-voltage-transfer-ratio DC transformer (1:1-DCX) with two MFT realization options: ACT and MCT. The results of multi-objective optimizations show that on a component-level there are highly efficient and lightweight ACT designs (99.7 %, up to 40 kW/kg), however high operating frequencies up to 200 kHz are required. As this leads to high switching losses of SiC MOSFETs, those designs have poor system-level performance (below 99.0 %). On the system-level, the η-γ-performance planes exhibit that the MCT-DCX cannot achieve a power density of more than 7.5 kW/kg due to thermal limitation of the MCT ($\gamma < \approx 9$ kW/kg). In contrast, the ACT-DCX can achieve twice the gravimetric power density, i.e., up to 16 kW/kg, while maintaining a lower but still comparably high DC-DC efficiency of 98.9 %. The picture reverses when considering the volumetric power density (excluding the shielding) and on a component-level, the ACT is limited to $\rho < \approx 19.5\,\mathrm{kW/dm^3}$, and more compact realizations (up to $26\,\mathrm{kW/dm^3}$) can be achieved with the MCT. This trend is even more pronounced on the system-level, for which maximum volumetric power densities of $8.2\,\mathrm{kW/dm^3}$ for the MCT-DCX compared to $5.2\,\mathrm{kW/dm^3}$ for the ACT-DCX result.

- *Ultra lightweight MV/MF air-core transformer* - A fully-rated prototype of a 166 kW / 7 kV ACT in a configuration with a pair of coaxial solenoids is designed, constructed and experimentally tested. The realization of the ACT is of relatively low complexity, as air can be used as an insulation and cooling medium. Furthermore, the thermal design is simplified as large areas of the transformer coils are available for direct (forced) air

cooling. Also, operation at up to 70 % of the rated power is feasible with passive cooling (i.e., natural convection) only. These aspects translate into comparably simple and hence cost-effective manufacturing, which is complemented by simplified handling because of the relatively low mass. However, for the same reason, special attention must be paid to the realization of mechanical/support parts as they contribute up to 50 % of total mass. Moreover, the construction (twisting) of litz wire used for the windings is critical, as even slight imperfections might have unfavorable effects on the overall efficiency. The ACT prototype achieves a measured full-load efficiency of 99.5 % at an operating frequency of 77.4 kHz, volumetric power density of 2.2 kW/dm^3 and an unprecedented gravimetric power density of 16.5 kW/kg. The ACT concept is thus particularly well suited for emerging applications in which robustness, weight, serviceability and cost-effective manufacturing of the transformer are of high importance.

- *Weight-optimized MV/MF magnetic-core transformer* - For benchmark purposes a weight-optimized, conventional 166 kW / 7 kV MCT in a shell-type configuration consisting of an E-core (ferrite, 3C94) with concentric windings encapsulated in silicone insulation (dry-type, TC4605 HLV) is designed, built and validated. Conservative assumptions during the optimization and design phase enable significant overload capability of the MCT and the heat run with losses that correspond to maximum thermally feasible power transfer, show that at room temperature, the MCT prototype can be operated with power transfer of up to 250 kW. The MCT prototype (6.7 kW/kg, 5.4 kW/dm^3), operated at 40.0 kHz, reaches a measured efficiency of 99.7 %. The MCT concept is hence particularly well suited for emerging applications in which high compactness, efficiency and thermal overload capability of the transformer are required.

- *Magnetic shielding of MFTs* - The magnetic flux density in the proximity of MFTs, especially ACTs or close to the air gap of MCTs, can reach up to several mT, causing eddy-current losses in metallic elements and disturbances in nearby electronic circuitry. The measurements of the magnetic stray flux in the proximity of the MFTs confirm that shielding is required for the ACT prototype to conform with the ICNIRP 2010 exposure limits. To reduce the magnetic stray flux in the proximity of the transformer, a conductive (aluminum) shielding enclosure is designed, built, and tested. With the proposed shielding, the ACT fulfills the ICNIRP guidelines regarding the magnetic stray flux levels for public

exposure at a distance of 200 mm from the shielding. Adding the shielding enclosure increases the weight by around 10 %, the overall losses by 6 %, and determines the boxed volume of the transformer, yielding a volumetric power density of 2.2 kW/dm^3 (compared to 7.8 kW/dm^3 without the shielding). On the other hand, the MCT prototype does not require additional shielding, as stray fields decay below the limits already geometrically relatively close to the MFT (250 mm), a distance which is a reasonable clearance to maintain in MV systems.

- *MV insulation in MFTs* - The realized prototypes feature a nominal insulation voltage of 10 kV. The ACT employs air as insulation medium and the required clearance and creepage distances can be tailored, even for a finished design, by inserting appropriate barrier elements between the coils. This is advantageous, e.g., for input-series output-parallel (ISOP) arrangements of DCX cells as the transformers are experiencing different CM voltages in such converter structures, or for airborne applications, where the insulation strength of air depends on altitude. In contrast, once the insulation system of a dry-type MCT has been defined, the insulation voltage rating cannot be changed anymore.

- *Dielectric losses in MFTs* - Thanks to the employed air insulation, the dielectric losses of the ACT can be neglected. Conversely, in some dry-type MFTs with silicone insulation the dielectric losses can account for up to 15% of the total losses. It has been shown that initial environmental conditioning of the MCT's dry-type silicone insulation has a significant influence on the dielectric. Depending on the state of the silicone (moist or dry), the dielectric losses can vary by more than a factor of three. Hence, the dielectric losses must be considered in the design calculations including this phenomenon.

- *Resonant capacitor bank* - Due to relatively high leakage inductances, an ACT requires low resonant capacitance values for the considered operating frequency, which results in high resonant capacitor voltages. Therefore, high-power polypropylene capacitor bank assemblies are necessary, which are bulky and generate significant losses hence active cooling is required. On the other hand, for the MCT, the capacitor bank for the considered 1:1-DCX is realized with ceramic capacitors of negligible losses, mass and volume.

- *DCX-level performance evaluation* - With regard to the overall 1:1-DCX systems, both efficiency curves are relatively flat for loads between

35 % and 100 % of the nominal power P_N. The MCT-DCX attains a very high efficiency (close to 99.2 %) even up to 110%P_N. Conversely, the ACT-DCX achieves slightly higher part-load efficiency for loads $< 40\%P_N$ due to the exceptional partial-load characteristic of the ACT and in spite of high magnetizing current which causes load-independent switching losses in MOSFETs but facilitates ZVS. From the similarity of the system-level efficiency curves at low load, it is concluded that the impact of the magnetizing current losses in the ACT-DCX is comparable to the transformer's core losses in the MCT-DCX. At the rated power of $P_N = 166$ kW the efficiencies (calculated) for the ACT-DCX and the MCT-DCX are 99.0 % and 99.2 %, respectively.

PART 2 - **MV Power Semiconductor Stage**

- *Quasi-2-level operation of the FCC-based half-bridge* - With the use of detailed simulations including non-linear models of the switches, the fundamental principles of Q2L operation of the FCC half-bridge are identified. Based on the analysis of zero voltage switching (ZVS) and hard-switching (HS) transitions with non-zero output current as well as transitions without output current (no load, zero-current HS), a generic description of resulting charge and voltage increments is derived. In principle, the charge increment of a flying capacitor (FC) is proportional to the product of the delay time and the local maximum of the output current of the FCC-based half-bridge, where the delay time is the time allocated for the transition of an individual cell. Noteworthy, the transferred charges are independent of the switching frequency and the number of levels N. Furthermore, all available switching sequences, i.e., the order in which the individual FC cells are commutated, are analysed for a 5L-FCC and it is concluded that there are two consecutive sequences resulting in the same value and sign of charge change in all FCs, whereas $((N-1)!-2)$ non-consecutive sequences enable to provide charges of different values and various effects (charging and/or discharging), however all FCs are coupled and it is not possible to influence only a selected set of FCs.

- *Cell multiple switching* - In case of zero output current, the charge increments of the FCs are expected to be zero. An in-depth analysis of Q2L operation during zero-current HS transition reveals that there are charges delivered to FCs originating from the current flow required to charge output capacitances of the switches, however, the net charge

exchange of each FC over the entire transition is approximately zero. To provide means for balancing the FC voltages in case of zero output current a novel method called *cell multiple switching* (CMS) is proposed. It relies on the insertion of additional zero-current (lossy) commutations within a Q2L transition which leads to additional charging of the output capacitances of switches and to corresponding charge exchanges between the FCs (or DC-link capacitor and FCs). Thus, by adding additional switching actions, the FC voltages can be adjusted.

- *Closed-loop method of load-independent voltage balancing* - Based on the derived generic description of charge and voltage increments in Q2L-FCCs and the proposed CMS method, a comprehensive concept for load-independent balancing of voltages is proposed. For non-zero load current a model predictive controller (MPC) is employed to identify the commutation sequence of the individual switches within a Q2L transition (1-step horizon) from all possible permutations by minimizing the predicted deviation from the reference values. In case of zero load current, also an MPC-based approach with FC voltage reference tracking (6-step horizon) using the CMS is used. In order to examine the Q2L transitions and the proposed balancing methods a 5L-FCC LV half-bridge demonstrator is realized. The experiments of hard-switching and soft-switching output voltage transitions, load transients, as well as of start-up and shut-down operation modes show good agreement with the proposed description and simulations. Furthermore, the presented closed-loop cell voltage control concept demonstrates an excellent average FC voltage tracking as well as symmetric cell voltages.
- *Concept of a MV SiC "Super-Switch" Intelligent Power Module (SiC-SS-IPM)* - Aiming for high integration and compactness of the considered Q2L-FCC-based power semiconductor stage, a concept of a MV SiC "Super-Switch" Intelligent Power Module (SiC-SS-IPM) is introduced. SiC-SS-IPM envisages the integration of a complete 5L-FCC bridge-leg, including power semiconductors (10 kV SiC MOSFETs), flying and commutation DC-link capacitors, gate drivers, isolated cooling interfaces, measurements, and Q2L control into a 300 kVA / 40 kV power module. In this context, dimensioning of semiconductors and capacitors is shown and in particular their volumes are evaluated. The realization of a SiC-SS-IPM is modeled including the layout of components. The SiC-SS-IPM features a low boxed volume of 2.9 dm^3 which results in a module-specific power density of 102 kVA/dm^3. Additionally, the impact of a Q2L operation on electrical insulation is studied by analyzing

harmonics contained in the output voltage and compared to waveforms of a 2L bridge-leg with series connection of MOSFETs. It is found that $\mathrm{d}v/\mathrm{d}t$ during the staggered switching transition is independent of the number of series-connected switches and, therefore, the Q2L operation reduces the partial discharge amplitudes, mitigates the impacts of resonances, and reduces high frequency harmonics compared to a conventional 2L bridge-leg. Thus, for a considered equivalent common-mode capacitance of insulation system, of a typical value of 200 pF and a dissipation factor of 1 %, thanks to the Q2L operation, the dielectric losses are computed to be reduced by approximately 40 %.

9.2 Outlook and Future Research Areas

Although this thesis already explored several novel medium-voltage SST technologies and provided solutions how to realize them, a number of potential research areas emerged in the course of the analysis, and could be investigated in the future to accelerate the advancements in SST technologies. In particular:

PART 1 - **Medium-Voltage Medium-Frequency Transformers**

- *MFT operation in a complete DCX system* - The realized prototypes of an air-core and a magnetic-core transformer have been validated only on a component-level. For a complete experimental analysis and fully-rated verification, MV power semiconductor stages should be build and operated with the constructed MFTs and resonant capacitor banks as a 1:1-DCX. Moreover, efficiency measurements of DCXs could be taken and compared with the results of calculations.

- *Partial discharges in dry-type MFTs* - The realized MCT prototype reaches a PD-free operation only up to 4.2 kVDC, however the insulation system was designed for 10 kVDC. Furthermore, the conducted measurements indicate that the PDs occur in the winding package, however, due its closed structure, i.e., winding and silicone are enclosed in a plastic mold, it is impossible to locate the source of the PDs, e.g., with an ultrasonic imaging camera. In order, to identify the source of PDs, basic studies of PD development in potted winding samples are required with focus on the silicone material and potting process quality, e.g., void-free potting and the contact layer of silicone with insulation of litz wires.

- *Lightning surges* - The insulation of MV/MF transformers should be tested with respect to lightning surges, i.e., undergo a basic lightning impulse (BLI) test. This test is required to guarantee the integrity of galvanic isolation during fault conditions.
- *Numerical solution of ACT coils models* - The proposed modeling and optimization of an ACT realized as a pair of cylindrical solenoids involves 2-D FEM simulations. In order to accelerate this process, an analytical or semi-numerical model of the self-inductances and mutual inductance of coils could be researched and derived. This could potentially allow for rapid design space exploration and/or partial elimination of FEM simulations.
- *Alternative air-core transformer configurations* - The presented theoretical investigations (see **Appendix A**) indicate that ACTs in a flat-disc configuration are characterized by a very similar performance space (gravimetric and volumetric power densities, efficiency) compared to the cylindrical solenoids configuration. To validate those findings and identify all properties, a high-power MV/MF flat-disc ACT still has to be demonstrated in hardware.

Part 2 - **MV Power Semiconductor Stage**

- *Q2L operation in short-circuits* - The operation of a Q2L-operated FCC has been analyzed with the use of simulations in conditions of a short-circuit current in the output of a half-bridge. The proposed approach to reduce the charge change in the flying capacitors relies on the availability of a fast overcurrent protection in the gate driver and shortening of the delay times to the minimum limited by the potential shoot-through of switches. This approach, however has not been tested so far and could be the subject of further research and experimental validation.
- *Balancing method without FC voltage measurements* - A method of load-independent voltage balancing in the Q2L-FCC proposed in this thesis relies on the measurements of FC voltages. This is, however, challenging with regard to the realization effort of measurement circuitry, especially in MV systems. In order to eliminate the necessity of FC voltage measurements, a method using only the half-bridge's output voltage and DC-link measurements could be used. This, however requires multiple sampling of the output voltage during the Q2L transition in order to reconstruct all FC voltages based on the difference with the

DC-link voltage. The method is challenging due to requirement of low noise measurement of the switched output-node and high-bandwidth or parallel sampling.

- *Realization of a MV SiC-SS-IPM* - Integration of a MV FCC-based half-bridge power semiconductor stage with all circuits for gate drivers, measurements, and control into an intelligent power module, i.e., a SiC Super-Switch IPM is a challenging task. In particular, due to the numerous measurement circuits and large creepage and clearance distances depending on the required insulation voltage, the compactness could be determined by the insulation system and not by the volume of the flying capacitors. Such detailed investigations could be a topic of further research.

Appendices

A

Geometrical Optimization of Medium-Frequency Air-Core Transformers

This Appendix summarizes the most relevant research findings published in:

- T. Guillod, **P. Czyz**, and J. W. Kolar, "Geometrical Optimization of Medium-Frequency Air-Core Transformers for DCX Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2022.

Executive Summary

This Appendix analyzes the potential of air-core transformers (ACTs) for realizing medium-voltage high-power isolated DC-DC converters. ACTs, i.e., transformers without magnetic cores, are particularly interesting for their simple construction and reduced weight. However, the reduced magnetizing inductance, the reduced magnetic coupling, and the stray fields are challenging aspects for the design of ACTs. A complete model of the ACT (e.g., magnetic field patterns, skin and proximity losses, shield's eddy currents, harmonics, insulation constraints, and thermal limit) is proposed and verified with measurements obtained with a prototype. Afterwards, a complete multi-objective optimization of a series resonant converter (SRC) operating as DC transformer (DCX) between two 7 kV buses with a rated power of 166 kW is conducted. Two different geometries are considered for the ACT: concentric cylindrical coils and planar spiral coils. As a result, the optimal ACT, (operated at 162 kHz) features extreme power densities of 7.5 kW/dm^3 and 31 kW/kg, which confirms the superiority of ACTs regarding the gravimetric power density. The calculated efficiencies are 99.5 % and 98.7 % for the ACT and the complete DC-DC converter, respectively. Finally, the different trade-offs are highlighted and analyzed, e.g., considering mass, volume, efficiency, switching frequency, part-load behavior, and insulation distance.

A.1 Introduction

Isolated DC-DC converters are essential building blocks of modern high-power energy conversion systems, such as fast electric vehicle chargers, converters for renewable energy, datacenter power supplies, drive systems, or more electric aircraft [169–172]. The usage of medium-frequency transformers and wide-bandgap power semiconductors allows the construction of more compact and efficient DC-DC converters [18, 20, 89]. Nevertheless, due to their limited gravimetric power density (i.e., 2 kW/kg to 12 kW/kg), the magnetic-core transformers (MCTs) are typically the heaviest components of power electronic systems. This is particularly problematic for airborne or battery-powered applications [28, 44, 45, 96, 170].

In order to drastically reduce the weight of medium-frequency transformers, air-core transformers (ACTs), which consist of two coils that are magnetically coupled without the help of a magnetic circuit, have been proposed [28, 96, 173]. Even if air-core magnetic components are typically found in high-frequency low-power systems [174, 175], they are also interesting for high-power systems [96]. It has been shown that ACTs can exhibit gravimetric power densities above 25 kW/kg with efficiencies above 99.5 % [96]. Therefore, ACTs represent a promising alternative for weight-optimized converters with the following advantages:

- *Mass* - The magnetic core is typically the heaviest component of MCTs. Therefore, ACTs are significantly lighter than MCTs.
- *Linearity* - ACTs are perfectly linear and, therefore, can withstand significant temporary overcurrents or overvoltages without changing their properties.
- *Temperature* - The operating temperature of ACTs is not limited by the Curie temperature of the magnetic core. Therefore, ACTs are well suited for high-temperature environments.
- *Construction* - Due to their simple structure, ACTs facilitate the design of the mechanical parts and the cooling systems. Additionally, high-voltage electrical insulation can be easily integrated.
- *Electrical circuit* - The high leakage and low-magnetizing inductances of ACTs can be advantageous for some applications (e.g., LLC converters, resonant tank). Due to the possibility to integrate large insulation distances, ACTs also feature reduced parasitic capacitances.

However, removing the magnetic core has a critical impact on the magnetic field pattern of a transformer. This creates several challenges for the design and operation of ACTs:

- *Volume* - Without a magnetic core, the magnetic flux is not confined in the transformer. For this reason, ACTs are less compact than MCTs.
- *Electrical circuit* - The lower self-inductance and magnetic coupling of ACTs have to be considered for the converter design (i.e., increased magnetizing current, voltage drop under load).
- *Stray field* - The medium-frequency magnetic stray field emitted by ACTs is not negligible and should be shielded in order to avoid eddy-current losses and/or electromagnetic interferences.
- *Modeling* - The magnetic field patterns of ACTs are difficult to approximate with accurate analytical equations. Moreover, the different parameters (e.g., voltage transfer ratio, leakage, and magnetizing inductance) are difficult to determine. This implies that numerical simulations and numerical optimization are typically required for ACTs.

In many aspects, ACTs are similar to inductive power transfer (IPT) coils [29, 48, 50, 176]. However, for ACTs, the air gap, which is only determined by the electric insulation distance, is much smaller and, therefore, the magnetic coupling is higher (i.e., 50 % to 80 %). Additionally, a misalignment between the coils can be excluded. These properties allow for the selection of a converter topology with a load-independent voltage gain, which is often desired for DC-DC converters. Several non-resonant (e.g., dual-active bridge converter) and resonant converter topologies (e.g., series-series and series-parallel) can be selected for systems with ACTs [172, 176].

In this Appendix, a series-series compensated system is selected for its simplicity, flexibility, quasi-sinusoidal currents, and ability to achieve zero voltage switching (ZVS) over the full load range. **Fig. A.1** shows the converter topology which corresponds to the well-known series-resonant converter (SRC) operated at the resonance frequency as a DC transformer (DCX) [18, 177, 178]. For the analysis, a 1 : 1 medium-voltage DC-DC converter operating between two 7 kV buses with a rated power of 166 kW is selected. Such systems are employed for flexible bus-tie interconnection (current limit, power flow control, and fault handling) or in input-series output-parallel converter structures [48, 172]. However, the obtained results are also applicable to systems with arbitrary voltage transfer ratios.

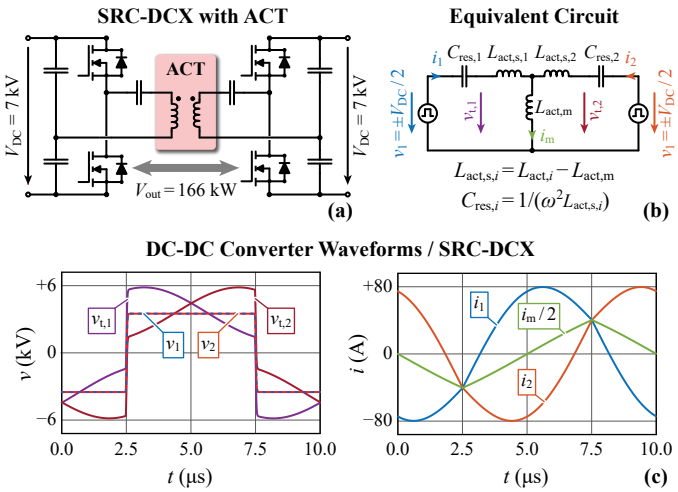


Fig. A.1: (a) SRC-DCX DC-DC converter with an ACT. **(b)** SRC-DCX equivalent circuit using a T-type transformer equivalent circuit. **(c)** Voltage and current waveforms obtained with an active magnetizing current splitting SRC-DCX modulation (P_{out} = 166 kW, V_{DC} = 7 kV, f = 100 kHz, $L_{act,i}$ = 150 µH, and $L_{act,m}$ = 105 µH).

The goal of this Appendix is to find and analyze the optimal coil geometry for ACTs [50, 96, 173]. **Figs. A.2(a)-(b)** depict the selected geometries: concentric cylindrical coils (C-ACT) as used in [28, 96] and planar spiral coils (S-ACT), which are typically used for IPT systems [29, 50]. In order to shield the ACT (magnetically and electrically), a conductive enclosure is placed around the coils [67]. All the parameters (e.g., wire size, coil size, insulation distance, placement of the shield, operating frequency, and semiconductor chip area) are optimized for both geometries with an algorithm combining brute force grid search and genetic optimization [179, 180]. This represents the first comprehensive modeling and analysis of ACTs with high magnetic coupling factors (i.e., magnetic field patterns, skin and proximity losses, shield's eddy currents, harmonics, insulation constraints, and thermal limit) and allows for a detailed characterization of the Pareto fronts and the underlying design trade-offs. Additionally, simple and general scaling laws, which describe the performance of ACTs, are proposed.

The Appendix is organized as follows. **Section A.2** introduces the ACT and SRC-DCX models. **Section A.3** provides experimental validation of the ACT model with the ACT prototype presented in [96]. **Section A.4** describes the considered ACT and SRC-DCX design spaces and optimization strategies. The obtained Pareto fronts and optimal designs are discussed in **Section A.5**. **Section A.6** presents ACT scaling laws that allow the extrapolation of the presented results to different specifications.

A.2 ACT and SRC-DCX Models

In this Section, the working principle of the SRC-DCX with an ACT is explained and the models of the different components (ACT, resonant capacitors, and semiconductor bridges) are detailed.

A.2.1 SRC-DCX Model

The SRC-DCX, cf. **Fig. A.1(a)** is a LLC converter featuring a load-independent voltage transfer ratio without requiring closed-loop control [177, 178]. The selected SRC-DCX features two MOSFET half-bridges with split DC-links as it reduces the number of switches and the voltage stress applied to the transformer [18]. Furthermore, the converter is bidirectional since both semiconductor bridges are constructed with active switches [18, 181].

In order to achieve a load-independent voltage transfer ratio, the transformer is operated at the resonance frequency, where the leakage impedance

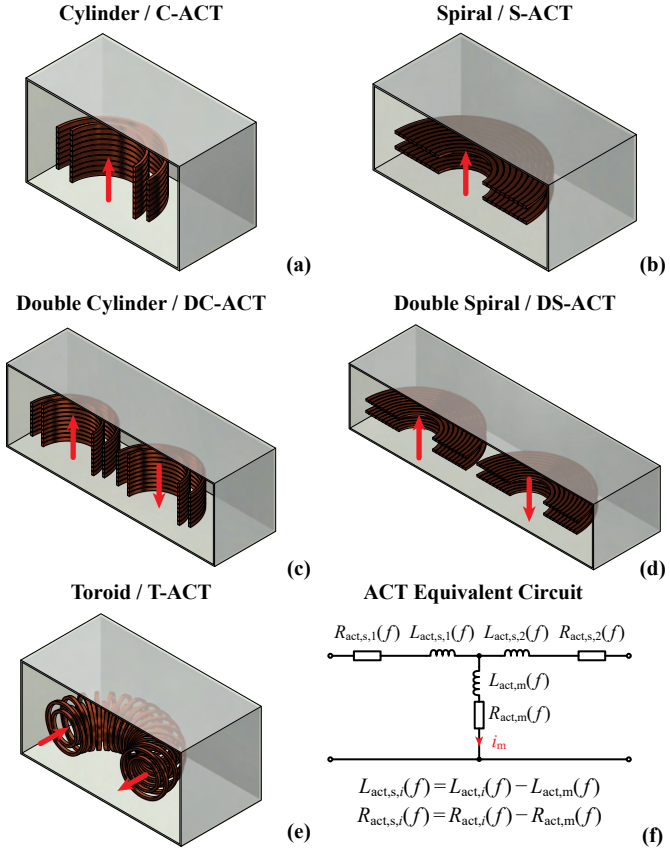


Fig. A.2: (a) Cylindrical ACT (C-ACT). **(b)** Spiral ACT (S-ACT). **(c)** Double cylinder ACT (DC-ACT). **(d)** Double spiral ACT (DS-ACT). **(e)** Toroidal ACT (T-ACT). **(f)** Full ACT equivalent circuit (T-type). The ACT geometries are cut along a symmetry plane and half of the components are shown. The following color coding is used: sienna for the coils and gray for the conductive shield. The direction of the magnetic field produced by the magnetizing current (i_m) is highlighted in red.

is compensated by the resonant capacitor impedance (cf. **Fig. A.1(b)**). For the considered 1 : 1 voltage transfer ratio, the simple T-type equivalent circuit can be used and the resonant capacitors can be selected as

$$C_{\mathrm{res},i} = \frac{1}{(2\pi f)^2 L_{\mathrm{act,s},i}}, \tag{A.1}$$

where f is the operating frequency. Due to the resonant tank, a quasi-sinusoidal load current is flowing in the ACT (cf. **Fig. A.1(c)**). It should be noted that the resonant tank can be located on the primary side, secondary side, or split between both sides [18, 176]. However, splitting the resonant capacitors between both sides is advantageous as it reduces the voltage stress applied to the ACT. Furthermore, for SRC-DCXs with arbitrary voltage transfer ratios, it is usually better to use a transformer equivalent circuit featuring an ideal transformer, as shown in [18, 182].

Besides the load current, a triangular magnetizing current is also flowing in the transformer and allows for ZVS of the MOSFETs. With the traditional SRC-DCX modulation scheme, the transmitter bridge is actively operated and the receiver bridge is operated as a passive or synchronous diode rectifier. Then, the magnetizing current is exclusively flowing in the transmitter coil and not in the receiver coil [178]. However, as shown in [18], the magnetizing current can be split between the coils if both bridges are actively switched with a small phase shift, cf. **Fig. A.1(c)**. Splitting the magnetizing current equalizes the switching speed of the MOSFETs and reduces the RMS currents. This is particularly important for ACTs, which feature low magnetizing inductances and high magnetizing currents.

The considered circuit model is fully coupled, i.e., all circuit equations are solved together without approximations. The complete magnetizing current splitting modulation scheme of SRC-DCX is considered with the following nonidealities: harmonic distortion, losses (ACT, resonant capacitors, and MOSFETs), frequency-dependency of the component values, and finite slew rate of the semiconductors (ZVS model).

A.2.2 Semiconductor and Resonant Capacitor Models

The semiconductor half-bridges are using SiC MOSFETs. The conduction resistance (R_{ds}) and the soft switching losses (E_{sw}) are scaled with the chip area (A_{die}):

$$\begin{aligned} R_{\mathrm{ds}} &= r_{\mathrm{ds}}/A_{\mathrm{die}}, \\ E_{\mathrm{sw}} &= e_{\mathrm{sw}} A_{\mathrm{die}} + k_{\mathrm{sw}} I_{\mathrm{sw}}, \end{aligned} \tag{A.2}$$

where r_{ds} is the conduction resistance per chip area, e_{sw} the current-independent switching losses per chip area, k_{sw} the current dependency of the switching losses, and I_{sw} the switched current. The losses per chip area (h_{die}) are limited in order to ensure the thermal feasibility of the semiconductor half-bridges.

The resonant capacitors are realized with polypropylene film technology and the losses are modeled with a frequency-dependent dissipation factor ($\tan\delta$):

$$\tan\delta = \tan\delta_0 + k_\delta f, \tag{A.3}$$

where $\tan\delta_0$ is the frequency-independent dissipation factor, k_δ the frequency-dependency of the dissipation factor, and f the operating frequency.

The different coefficients representing the semiconductor (r_{ds}, e_{sw}, k_{sw}, and h_{die}) and resonant capacitor models ($\tan\delta_0$ and k_δ) can be approximated from the datasheets. However, for obtaining an accurate model, dedicated measurements are often preferable.

A.2.3 ACT Coil Geometries

Several geometries are suitable for the realization of ACTs, cf. **Figs. A.2(a)-(e)**. Due to the linearity of the ACT, all geometries feature the same, current-independent, equivalent circuit, cf. **Fig. A.2(f)**. Furthermore, these geometries can be classified into two categories:

- *Non-compensated field* - For the geometries shown in **Figs. A.2(a)-(b)**, the magnetic field generated by the magnetizing current is creating a stray field in the axis of the coils [28, 176].
- *Compensated field* - For the geometries shown in **Figs. A.2(c)-(e)**, the magnetic field generated by the magnetizing current is partially compensated, either with a double-D structure (two sets of coils) or with a toroidal structure [28, 49, 50, 96, 173]. This implies that the magnetic field is mostly confined inside the ACT.

The magnetic performance (coupling and stray field) of these configurations can be improved with the addition of magnetic cores, as often seen for IPT systems [29, 49, 50]. However, with magnetic cores, ACTs are losing their competitive advantage with respect to the gravimetric power density. Therefore, in this Appendix, no magnetic materials are used to guide the magnetic flux.

A.2.4 ACT Model

The ACT is composed of litz wire windings surrounded by a conductive shield, which blocks the magnetic and electric stray fields (cf. **Figs. A.2(a)-(e)**). In the windings, the skin depth should be larger than the strand diameter in order to mitigate the skin and proximity effects [183]. For the shield, the skin depth should be smaller than the wall thickness such that the magnetic field is blocked [183]. Due to the lack of accurate analytical models for such configurations, the magnetic field patterns are simulated with a finite element method (FEM) in the frequency domain (2-D or 3-D models) [184]. In the FEM model, the discrete winding turns and the shield are modeled. The discrete strands of the litz wire are, however, not considered for the FEM model in order to reduce the computational cost. This assumption can be done as the stranding of a perfectly twisted litz wire does not impact the magnetic field pattern. The effect of the stranding of the litz wire on the losses can be computed in the post-processing without degrading the accuracy of the results [58, 183].

Due to the frequency dependency of the eddy currents in the shield, static simulations cannot be used. Since the component is linear, the inductance and resistance matrices fully describe the ACT (cf. **Fig. A.2(f)**). These matrices can be extracted from three linearly independent operating points:

$$\begin{aligned} &\text{OP1: } \hat{i}_1 = 1 \ \wedge \ \hat{i}_2 = 0, \\ &\text{OP2: } \hat{i}_1 = 0 \ \wedge \ \hat{i}_2 = 1, \\ &\text{OP3: } \hat{i}_1 = +1 \ \wedge \ \hat{i}_2 = -1. \end{aligned} \tag{A.4}$$

The inductance matrix is directly related to the energy stored in the magnetic field. The peak energy is extracted with the following integral:

$$\hat{W} = \iiint_{\text{all}} \frac{1}{2} \hat{B}\hat{H} \mathrm{d}V, \tag{A.5}$$

Where $\hat{B}$ is the magnetic flux density and $\hat{H}$ denotes the magnetic field. From the peak energy obtained for the three linearly independent operating points, the inductance matrix can be easily computed as

$$\begin{aligned} L_{\text{act,1}} &= 2\hat{W}_{\text{OP1}}, \\ L_{\text{act,2}} &= 2\hat{W}_{\text{OP2}}, \\ L_{\text{act,m}} &= \frac{1}{2}\left(L_{\text{act,1}} + L_{\text{act,2}}\right) - \hat{W}_{\text{OP3}}, \end{aligned} \tag{A.6}$$

where $\hat{W}_{\mathrm{OP}i}$ represents the peak extracted energy (cf. (A.5)) for the operating point OPi (cf. (A.4)). It should be noted that, the inductance matrix can also be extracted from the flux linkage between the coils or the induced voltages.

The extraction of the resistance matrix is more complex as it requires loss models for the litz wire and the shield. From the FEM simulations, the following integrals are extracted:

$$\begin{aligned} \hat{K}_{J,\mathrm{shield}} &= \iiint_{\mathrm{shield}} \hat{J}^2 \mathrm{d}V, \\ \hat{K}_{J,\mathrm{winding},i} &= \iiint_{\mathrm{winding},i} \hat{J}^2 \mathrm{d}V, \\ \hat{K}_{H,\mathrm{winding},i} &= \iiint_{\mathrm{winding},i} \hat{H}^2 \mathrm{d}V, \end{aligned} \tag{A.7}$$

where $\hat{J}$ is the current density. The shield losses are generated by the eddy currents and can be expressed with the spatial integral of the current density, which leads to

$$P_{\mathrm{shield}} = \frac{1}{2\sigma_{\mathrm{shield}}} \hat{K}_{J,\mathrm{shield}}, \tag{A.8}$$

where σ_{shield} is the electrical conductivity of the shield. For the litz wire losses, the skin and proximity effects in the strands can be calculated as

$$\begin{aligned} P_{\mathrm{winding,skin},i} &= \frac{F_{\mathrm{r}}}{\sigma_{\mathrm{winding}} k_{\mathrm{winding}}} \hat{K}_{J,\mathrm{winding},i}, \\ P_{\mathrm{winding,prox},i} &= \frac{G_{\mathrm{r}} k_{\mathrm{winding}}}{\sigma_{\mathrm{winding}} A_{\mathrm{strand}}^2} \hat{K}_{H,\mathrm{winding},i}, \end{aligned} \tag{A.9}$$

where $\sigma_{\mathrm{winding}}$ is the electrical conductivity of the strands, k_{winding} the litz wire fill factor, and A_{strand} the cross section of a single strand. The factors F_{r} and G_{r} describe the skin and proximity effects in a single strand and are computed with Bessel functions, as shown in [57,183,185]. This model assumes a perfect twisting of the litz wire, i.e., the current is equally shared between the strands [58]. From the computed losses (shield, skin effect, and proximity

effect), the resistance matrix can be extracted as

$$\begin{aligned} R_{\text{act},1} &= 2P_{\text{OP}1}, \\ R_{\text{act},2} &= 2P_{\text{OP}2}, \\ R_{\text{act,m}} &= \frac{1}{2}\left(R_{\text{act},1} + R_{\text{act},2}\right) - P_{\text{OP}3}, \end{aligned} \tag{A.10}$$

where $P_{\text{OP}i}$ represents the extracted losses (cf. (A.9)) for the operating point OPi (cf. (A.4)). It should be noted that the resistance matrix can be computed for the complete ACT (total losses) or just for a sub-component (e.g., shield, primary winding, or secondary winding).

The electric field stress between the coils has two components: a common-mode voltage across the galvanic insulation and the differential-mode voltage across the coils. Under the assumption of a quasi-homogeneous field between the coils, the peak value of the electric field can be expressed as

$$\hat{E}_{\text{act}} = \frac{\hat{v}_{\text{t},1} + \hat{v}_{\text{t},2} + \hat{v}_{\text{CM}}}{d_{\text{iso}}}, \tag{A.11}$$

where $\hat{v}_{\text{t},i}$ is the differential-mode voltage (cf. **Fig. A.1**), $\hat{v}_{\text{CM}}$ the common-mode voltage, and d_{iso} the insulation distance between the coils. For the electric field computation, the most critical case is considered, i.e., both differential-mode voltages ($\hat{v}_{\text{t},1}$ and $\hat{v}_{\text{t},2}$) are added.

Due to the open structure of ACTs, an efficient forced air cooling of the coils is easily achievable [96]. More specifically, each coil can be cooled down from both sides. The thermal feasibility of the ACT is ensured by comparing the losses of the different components (primary coil, secondary coil, and shield) and the exposed area available for forced convection [29, 96].

A.2.5 Model Implementation

The aforementioned models allow for a fully coupled multi-objective optimization of the SRC-DCX [179, 186]. As shown in **Fig. A.3**, the models are divided into two blocks, which are fully vectorized (parallel computing):

- *ACT FEM model* - The ACT FEM magnetic model is computed in the frequency domain for three linearly independent operating points (cf. (A.4)). The figures of merit (cf. (A.5) and (A.7)) are extracted for a limited number of frequencies in the range of interest. It has to be noted that all the properties computed in this step are independent of the operation condition (e.g., operating frequency, voltages, currents) of the ACT.

- *SRC-DCX model* - First, the FEM results are interpolated at the desired operating frequencies. The interpolation limits the number of required FEM simulations and is accurate since the extracted properties are only slightly frequency-dependent (cf. (A.5) and (A.7)). Afterwards, the frequency-dependent impedance matrices (cf. (A.6) and (A.10)), which include the high-frequency winding (skin and proximity effects) and shield (eddy-current) losses, are extracted. Finally, the SRC-DCX waveforms and the system properties (e.g., losses, efficiency, power density, and thermal limit) are computed.

The separation of the model into these two blocks allows for the isolation of the computationally intensive FEM task from the computationally cheap SRC-DCX model. Therefore, for each computed ACT geometry, many designs (e.g., operating frequency, litz wire stranding, and chip area) can be extracted.

A.3 Experimental Validation

The ACT model presented in **Section A.2.4** is compared with measurements obtained with the prototype presented in **Chapter 3**. This ACT is part of a $P_{\text{out}} = 166\,\text{kW}$ SRC-DCX operating between two $V_{\text{DC}} = 7\,\text{kV}$ buses. The key parameters are summarized in **Tab. A.1**. The prototype consists of two sets of coils connected in series (DC-ACT, cf. **Fig. A.2(c)**) and is depicted in **Fig. 3.3** and **Fig. 3.9**. Due to the magnetizing field compensation between the coil sets and the shield geometry (perforated shield above and below the coils), the prototype features a complex magnetic field pattern. Hence, this design is particularly interesting for validating the models. Extensive experimental validation of this prototype is presented in **Chapter 3**, including small-signal measurements, large-signal tests, resonance frequency analysis, thermal tests, and stray field measurements.

The comparison between small and large-signal measurements indicates that the ACT is perfectly linear. Therefore, the ACT terminal behavior is fully characterized by the impedance matrix. The impedance matrix, in turn, is fully identified from the open-circuit and short-circuit behaviors. **Tab. A.2** compares the measured and simulated values:

- *Inductances* - The ACT inductances are measured with a high precision impedance analyzer. The comparison between the measurements and the simulations indicates that the field pattern is correctly captured.

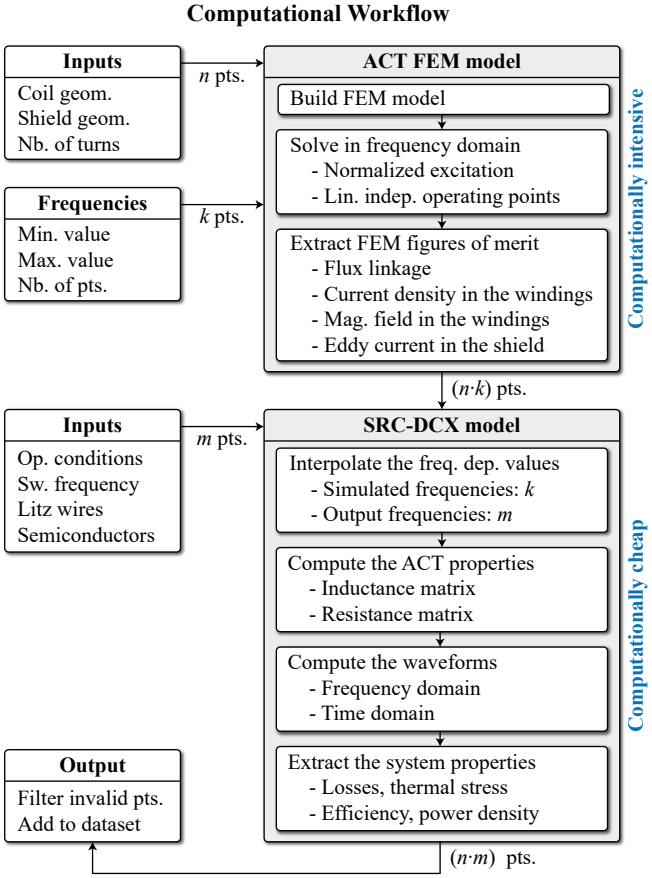


Fig. A.3: Modeling workflow separating the computationally intensive ACT FEM models and the computationally cheap SRC-DCX model.

Tab. A.1: DC-ACT Prototype [96].

Specifications	
Topology	SRC-DCX with half-bridges
Power	166 kW
DC bus	7 kV / 7 kV
ACT design	
Geometry	DC-ACT (cf. **Fig. A.2(c)**)
Frequency	77.4 kHz
Coils	2×22 turns in series
Litz wire	$2000 \times 71\,\mu$m
Shield	0.5 mm perforated aluminum
Fans	4×12 W
ACT performance	
Volume	74.7 dm^3 / 2.2 kW/dm^3
Mass	10.1 kg / 16.5 kW/kg
Losses	0.85 kW / 99.49 %

- *Resistances* - Due to the high quality factor of the ACT ($Q \approx 1000$ in open-circuit), electrical measurements of the winding resistance feature a limited accuracy. Therefore, highly accurate transient calorimetric measurements of the winding losses are performed **Section 3.5.3**. The slightly increased resistances of the prototype are mainly explained by the imperfect twisting of the litz wire, as shown in [58, 96].

- *Shield* - The impact of the shield on the inductances and resistances is assessed with a high precision impedance analyzer. The comparison between the measurements and the simulations demonstrates that the impact of the shield on the flux linkages and losses is correctly predicted.

Additionally, the measurements show that the self-resonance frequencies (open-circuit, short-circuit, and common-mode) are all located above 2 MHz. This implies that the impact of the resonances and parasitic capacitances is negligible during nominal operation. Finally, the thermal capabilities of the ACT are inspected (for a maximum temperature elevation of 80 °C). With the selected fans, 0.81 kW of losses in the coils are achievable, leading to a

Tab. A.2: Measured and Simulated Parameters.

Var.	Meas.	Sim.	Err.
ACT inductances (without shield)			
Open circuit	214.4 µH	203.9 µH	4.9 %
Short circuit	51.8 µH	53.7 µH	3.6 %
ACT resistances (without shield)			
Open circuit	101.9 mΩ	89.6 mΩ	12.1 %
Short circuit	151.9 mΩ	118.6 mΩ	21.9 %
Shield impact on the inductances			
Open circuit	−3.7 %	−3.4 %	0.3 %
Short circuit	−2.0 %	−1.6 %	0.4 %
Shield impact on the resistances			
Open circuit	+57.3 %	+52.6 %	4.6 %
Short circuit	+12.2 %	+9.9 %	2.2 %

dissipation per exposed area of $0.30\,\mathrm{W/cm^2}$. With the addition of air ducts, which improve the airflow around the coils, these numbers are increased to 1.28 kW and $0.47\,\mathrm{W/cm^2}$.

A.4 Optimization Boundary Conditions

The considered SRC-DCX operates between two $V_{\mathrm{DC}} = 7\,\mathrm{kV}$ buses at a rated power of $P_{\mathrm{out}} = 166\,\mathrm{kW}$ (cf. **Fig. A.1**), which are the same specifications as in [28, 96]. The maximum common-mode peak isolation voltage applied between the primary and secondary sides is $\hat{v}_{\mathrm{CM}} = 14\,\mathrm{kV}$. This Section describes the different parameters used in the optimization. Additionally, the multi-objective cost function and the optimization algorithm are described.

Even if the optimization is conducted with fixed specifications (166 kW and 7 kV), the obtained results are, to a large extend, useful for other converter systems. In order to extrapolate the results, scaling laws are presented in **Section ??**.

Tab. A.3: Semiconductor and Resonant Capacitors / Parameters.

Semiconductors	
$r_{ds} = 24.5\,\Omega mm^2$	Conduction resistance (at 125 °C)
$e_{sw} = 2.04\,\mu J/mm^2$	Switching losses (current-indep.)
$k_{sw} = 3.03\,\mu J/A$	Switching losses (current-dep.)
$h_{die} = 2.00\,W/mm^2$	Maximum thermal dissipation
Resonant capacitors	
$\tan\delta_0 = 150\,ppm$	Dissipation factor (frequency-indep.)
$k_\delta = 2.5\,ppm/kHz$	Dissipation factor (frequency-dep.)

A.4.1 Semiconductor and Resonant Capacitor Model

Both half-bridges are realized with "Cree/Wolfspeed QPM3-10000-0300" 10 kV SiC MOSFETs [36, 37]. The properties per chip area are considered (cf. (A.2)) and are depicted in **Tab. A.3**. The data are directly extracted from the calorimetric loss measurements shown in [39].

For the resonant capacitors, the properties of a high-performance heavy-duty film capacitor "CELEM CSP 120/200" are taken [40]. The corresponding parameters are shown in **Tab. A.3**. The dissipation factor is measured with the calorimetric setup described in [187].

A.4.2 ACT Coil Geometries

The ACT geometries (non-compensated field, double-D, and toroidal structures) introduced in **Section A.2.3** feature distinct advantages and drawbacks, which can be summarized as follows:

- The non-compensated field structures (C-ACT and S-ACT, **Figs. A.2(a)-(b)**) are magnetically advantageous (i.e., magnetic coupling, inductance, and quality factor). Due to the limited number of coils and structural elements, these geometries not only facilitate the cooling and the insulation design but also reduce the weight of the component [96]. However, these ACTs produce a significant magnetic stray field and, therefore, are potentially challenging to shield.

- Double-D structures (DC-ACT and DS-ACT, cf. **Figs. A.2(c)-(d)**) allow for a reduction of the magnetic stray field. This leads to a reduction

of the losses in the shield or, alternatively, the distance between the shield and the coils can be decreased [96]. However, splitting a large coil into two smaller coils is intrinsically not advantageous for the magnetic properties (i.e., magnetic coupling, inductance, and quality factor). This has a negative impact on the losses, volume, and mass of the component [49, 50].

- The toroidal structures (T-ACT, cf. **Fig. A.2(e)**) are magnetically advantageous but suffer from practical issues concerning the thermal management, electrical insulation, coil former design, and winding realization. These drawbacks are particularly critical for a high-power medium-voltage system; hence the toroidal geometries are ruled out.

For the selected specifications, a preliminary Pareto analysis has shown that the double-D structures (DC-ACT and DS-ACT) are slightly inferior to the non-compensated field structures (C-ACT, and S-ACT). For a given power density (gravimetric or volumetric), the efficiencies of double-D designs are found to be 0.03 % to 0.18 % lower than the non-compensated field designs. It appears that, due to the high magnetic coupling factors achieved by ACTs (compared to IPT systems), the stray field produced by the non-compensated field structures can be shielded with moderate losses. Therefore, the reduction of the lower stray field achieved with double-D structures does not provide a sufficient advantage to compensate for their handicap with respect to the winding losses, mass, and volume. For these reasons, the non-compensated field geometries (C-ACT, and S-ACT, **Figs. A.2(a)-(b)**) are selected for a detailed analysis.

A.4.3 ACT Model

Besides the selection of the ACT coil geometry, several other design choices are required for the ACT. The selected parameters are shown in **Tab. A.4** and explained as follows:

- *Winding* - Single-layer windings are used for the coils. Such windings are easier to construct, feature reduced stray capacitances, and do not require layer insulation.

- *Litz wire* - The coils are realized with profiled copper litz wires. Aluminum litz wires, which would be advantageous for the gravimetric power density, are not considered due to a lack of commercial availability. The size and aspect ratio of the litz wire is limited in order to ensure

manufacturability. A safety margin (10 % for the skin effect losses and 30 % for the proximity effect losses) is accepted for the winding losses, taking into account the impact of potential twisting imperfections. These safety margins are selected according to the measurements conducted in [57, 96] and the analysis presented in [58].

- *Shield* - The shield is made of non-perforated copper plates, which feature better performance than the perforated aluminum plates used in [96]. The thickness of the shield is selected with respect to the skin depth, ensuring the effectiveness of the shielding [96]. Openings in the shield are required for the cooling and the cable terminations and are causing eddy-current crowding in the shield. The impact of the openings has been assessed with FEM simulations and is found to increase shield losses by 20 % to 30 %. However, the optimization model does not consider the openings. Accordingly, a safety margin of 30 % is added for the eddy-current losses.
- *Insulation* - An air insulation concept, which is compatible with medium-frequency electric fields with fast slew rates, is considered. As shown in [96], a dielectric barrier is placed between the coils in order to avoid a direct air clearance. The peak electric field between the coils is limited to a maximum value of 15 kV/cm, which is below the ionization electric field of air (ca. 25 kV/cm) [188, 189]. Therefore, partial discharges, surface discharges, and problematic dielectric losses, which are particularly critical for converters with medium-voltage SiC devices, are not expected during rated conditions [43, 60, 190]. Besides being simple and robust, an air insulation concept also has the advantage to reduce the stray capacitances of the ACT.
- *Thermal management* - The ACT is cooled down with forced air cooling where the airflow is primarily directed towards the coils. The selected air insulation concept allows for a direct double-sided cooling of the coils and a conservative thermal limit of $0.28\,\mathrm{W/cm^2}$ is selected [29, 96]. The shield is cooled down by the residual airflow and a thermal limit of $0.15\,\mathrm{W/cm^2}$ is considered.
- *Construction* - The structural elements are constructed with glass-reinforced plastic, which brings high mechanical stability with reduced weight. The boxed volume of the ACT considers the coils, the shield, and the fans. The mass of the ACT consists of the coils, the shield, the coil formers, the electrical insulation, the structural elements, and the fans.

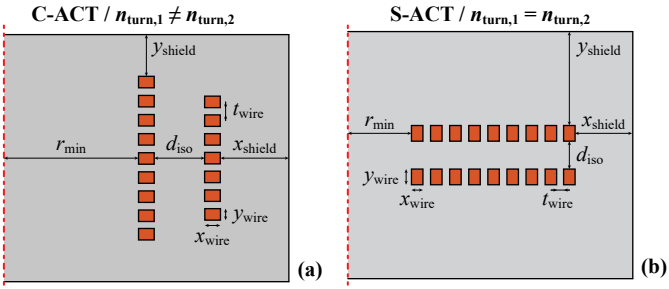


Fig. A.4: (a) Geometry of the C-ACT. **(b)** Geometry of the S-ACT. The symmetry plane (3-D model) or rotation axis (2-D axisymmetric model) is indicated with a dotted red line.

In order to reduce the computational effort, and due to the strong rotational symmetry of the selected geometries (C-ACT, and S-ACT), 2-D axisymmetric FEM models are used for the optimization. The coils are fully rotational symmetric and can be modeled in 2-D without any approximation. The rectangular cuboid shield is approximated by a cylinder with the same minimal distance between the shield and the coils. This approximation represents a conservative choice, which slightly overestimates the ACT losses (1 % to 10 %). At the end of the optimization process, the obtained designs are verified with 3-D FEM models.

A.4.4 Optimized Input Variables

Fig. A.4 shows the dimensions of the ACT, whereby all the parameters are optimized. The same litz wire (dimension and number of strands) is used for both windings. It should be noted that, for ACTs, the voltage transfer ratio is not only proportional to the physical turns ratio but also depends on the geometry and position of the coils. For the C-ACT geometry, the inductance per turn differs for the primary and secondary windings, which feature different radii. Therefore, even for the selected 1 : 1 voltage transfer ratio, the C-ACT geometry requires a different number of turns for the primary and secondary windings. For the S-ACT, the same number of turns is used for both windings as both coils have the same dimension.

Furthermore, the litz wire fill factor (k_{winding}) is optimized in order to find the optimal trade-offs between the weight, conduction losses, and proximity effect losses. The chip area per switch (A_{die}) is also swept as it represents a

trade-off between conduction losses, switching losses, and cost. Finally, the operating frequency (f) is swept. All the optimized parameters are listed in **Tab. A.5**.

A.4.5 Computed Output Variables

Tab. A.6 considers the figures of the merit of the ACT and SRC-DCX. Most of the listed parameters are typical for power electronic systems (e.g., power density, losses, and efficiency). However, three parameters are more specific to ACTs and are defined as (cf. **Fig. A.1**)

$$\begin{aligned} k_{\mathrm{act}} &= \frac{L_{\mathrm{act,m}}}{\sqrt{L_{\mathrm{act},1} L_{\mathrm{act},2}}}, \\ \xi_{\mathrm{src}} &= \max\left(\frac{\hat{v}_{\mathrm{t},1}}{V_{\mathrm{DC}}/2}, \frac{\hat{v}_{\mathrm{t},2}}{V_{\mathrm{DC}}/2} \right), \\ \lambda_{\mathrm{src}} &= \frac{P_{\mathrm{out}}}{\frac{1}{2}\left(\frac{V_{\mathrm{DC}}}{2} I_1 + \frac{V_{\mathrm{DC}}}{2} I_2 \right)}, \end{aligned} \tag{A.12}$$

where k_{act} is the magnetic coupling of the ACT, ξ_{src} the ratio between the ACT peak voltage and the DC-link voltage, and λ_{src} the power factor between the transferred active power and the apparent power delivered by the semiconductor bridges. The following values would describe a SRC-DCX with an ideal transformer [18]: $k_{\mathrm{act}} = 1$, $\xi_{\mathrm{src}} = 100\,\%$, and $\lambda_{\mathrm{src}} = \sqrt{8}/\pi \approx 90\,\%$.

A.4.6 Design Space Exploration

The goal of the Appendix is to present a comprehensive view of the design space of ACTs. Therefore, the complete design space (cf. **Tab. A.5**) of the SRC-DCX has been systematically explored with a brute force strategy (using grid refinement for the Pareto optimal designs). In total, 2.0 million valid C-ACT geometries and 1.7 million valid S-ACT geometries have been simulated (ACT 2-D FEM model, cf. **Fig. A.3**). From the ACT FEM results, 127.4 million valid SRC-DCX designs are obtained (SRC-DCX model, cf. **Fig. A.3**).

This dataset provides extremely interesting insight on the properties of ACTs with respect to the different performance metrics (e.g., volume, mass, chip area, efficiency, and magnetic coupling). However, the required computational effort (6 days using two "AMD EPYC 7742" CPUs [191]) is unreasonable from a component design perspective.

A.4.7 Optimization Strategy

Fig. A.5 depicts the optimization workflow used to design ACTs with a reasonable computation cost. More precisely, the optimal design is selected with respect to a multi-objective scalar cost function. The variables required for the ACT FEM model (cf. **Tab. A.5**) are optimized by a multi-objective genetic algorithm in order to efficiently explore the design space [179, 180]. In order to initialize the genetic algorithm, random points are selected for the first iteration. For the SRC-DCX model (cf. **Tab. A.5**), a brute force grid search approach can be used due to the reduced number of variables and the small computational cost. This hybrid optimization workflow, combining a genetic and a brute force approach has two advantages: the number of FEM simulations is reduced (genetic algorithm) and the performed FEM simulations are fully exploited (brute force).

For the brute force grid search (SRC-DCX model), a regular grid with 3′500 points is considered. For the genetic algorithm (ACT FEM model), the following parameters are used [192, 193]:

- For the initialization step, 25′000 random combinations are considered. Using a large number of combinations ensures that designs with reasonable performance are present in the initialization pool.
- From the initialization pool, the 800 designs with the lowest cost function value are selected as the initial population of the genetic algorithm.
- After each iteration of the genetic algorithm, crossover and mutation are applied to the population with the following split: 50 elite children, 350 crossover children, 250 mutation children, and 150 random new combinations.
- The convergence of the genetic algorithm is evaluated over 10 generations with the following metrics: the relative change of the cost function (0.5 % tolerance) and the relative change of the input (cf. **Tab. A.5**) and output (cf. **Tab. A.6**) variables (3 % tolerance).
- Convergence is typically reached after 120 generations, which implies that approximately 120′000 ACT geometries are simulated (including the initialization step). Given the number of optimized input variables (cf. **Tab. A.5**), this represents a massive improvement over brute force grid search. With two "AMD EPYC 7742" CPUs [191], the optimization is performed in 6 hours.

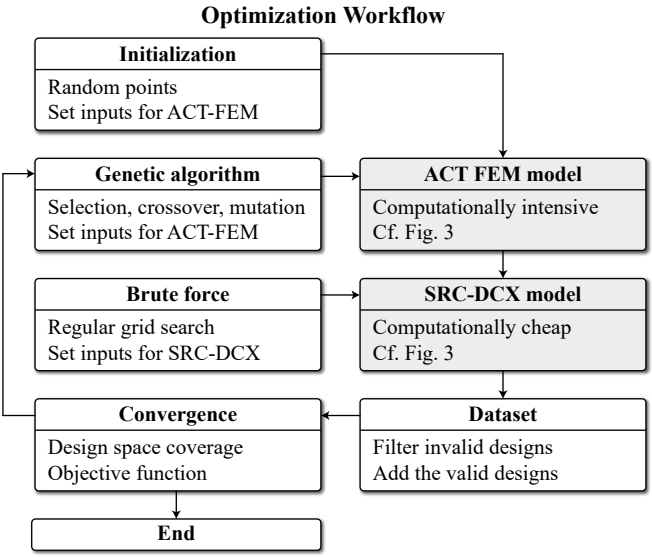


Fig. A.5: Optimization workflow using a genetic algorithm for the ACT FEM model and brute force grid search for the SRC-DCX model.

A.4.8 Multi-Objective Cost Function

The multi-objective cost function should be selected with respect to the constraints (e.g., target efficiency, target power density, production cost, and total cost of ownership) of the considered application (e.g., automotive, airborne, and stationary). As the ACT optimization presented in this work is not tied to a specific application, the cost function is selected to highlight the unique potential of ACTs to design power converters with extreme gravimetric power densities. A quadratic cost function is used and the weights (scaling factors) determine the desired trade-off between the objectives.

The selection of the weights typically requires several iterations. The initial weights are selected with respect to the desired performance. However, since the position and steepness of the Pareto optimal surface is, a priori, not known, the targeted performance might be exceeded or impossible to reach. In such cases, an adaptation of the weights is often required, using the dataset (initialization pool, population across the iterations, and optimal design) produced by the genetic algorithm with the previously selected weights.

In this Appendix, the cost function is decomposed into two parts. First, the ACT gravimetric power density, the ACT volumetric power density, and the SRC-DCX chip area power density (transferred power divided by the total installed semiconductor chip area) are considered. These three values are combined into a single power density cost function:

$$d = \sqrt{\frac{\left(\frac{8\,\mathrm{kW/dm^3}}{\rho_{\mathrm{act}}}\right)^2 + \left(\frac{30\,\mathrm{kW/kg}}{\gamma_{\mathrm{act}}}\right)^2 + \left(\frac{170\,\mathrm{W/mm^2}}{\kappa_{\mathrm{src}}}\right)^2}{3}}, \tag{A.13}$$

where the weights quantify the selected power density objectives. In order to highlight the potential of ACTs for realizing lightweight systems, the main weight (30 kW/kg) is set for the gravimetric power density. The remaining weights (8 kW/dm^3 and 170 W/mm^2) are ensuring the competitiveness of ACTs with respect to typical values obtained with MCTs [28, 96].

In a second step, the obtained power density cost function (cf. (A.13)) is combined with the SRC-DCX losses (more precisely the loss fraction, $1 - \eta_{\mathrm{src}}$) in order to obtain the global multi-objective cost function:

$$c = \sqrt{\frac{d^2 + \left(\frac{1-\eta_{\mathrm{src}}}{1.09\,\%}\right)^2}{2}}. \tag{A.14}$$

The weight on the loss fraction (1.09 %) is iteratively selected such that, for the optimal design, the power density cost function approaches $d \approx 1$, i.e.,

the optimal design will meet the criteria defined in (A.13) with the highest possible efficiency.

A.5 Optimization Results

In this Section, the results obtained in **Section A.4** are analyzed in detail. First, the Pareto fronts describing the performance space of the ACT and SRC-DCX are presented. Afterwards, the properties of the optimal design are discussed. Finally, the impact of the insulation requirement on the ACT is examined.

A.5.1 Pareto Fronts

The dataset described in **Section A.4.6** is considered and **Fig. A.6** depicts the obtained Pareto fronts between the achieved efficiency (ACT and SRC-DCX) and power density (volumetric and gravimetric). The analysis of the Pareto fronts reveals the following characteristics:

- *Efficiency* - Despite the increased magnetizing current, high efficiency can be achieved for both the ACT (up to 99.65 %) and the SRC-DCX (up to 99.05 %).

- *Volume* - As already highlighted in [96], the $\eta_{\text{act}} - \rho_{\text{act}}$ Pareto front of ACTs is below what is achievable with MCTs. However, the optimization of the shield geometry presented in this work allows the achievement of volumetric power densities above 10 kW/dm^3, which is significantly higher than the results presented in [96].

- *Mass* - The main advantages of ACTs are their exceptional gravimetric power densities (up to 41 kW/kg, including the coil formers, the fans, the coils, and the shield), which is significantly higher than for MCTs (typically below 12 kW/kg) [28, 45, 96]. This confirms that ACTs are particularly interesting for weight-constrained applications [45, 170].

- *Frequency* - The SRC-DCX can be operated in a large frequency range. Operation at high-frequency (above 100 kHz) is still offering better performance, especially, for the gravimetric power density. Due to the low magnetizing inductance, ACTs are operated at higher frequencies than MCTs in order to limit the magnetizing current.

Tab. A.4: ACT / Parameters.

ACT type	
Coils	C-ACT or S-ACT
Shield	Conductive shield
Litz wire	
Type	Profiled litz wire (rectangular)
Stranding	71 µm, less than 7′500 strands
Aspect ratio	Between 1 : 3 and 3 : 1
Skin effect losses	10 % safety margin
Proximity effect losses	30 % safety margin
Thermal limit	0.28 W/cm^2 for the exposed area
Op. temperature	130 °C
Shield	
Type	Copper shield
Thickness	200 % of the skin depth
Proximity effect losses	30 % safety margin
Thermal limit	0.15 W/cm^2 for the exposed area
Op. temperature	70 °C
Coil former and fans	
Peak electric field	Less than 15 kV/cm
Coil former	Glass-reinforced plastic
Dielectric barrier	Nomex aramid polymer
Fan weight	1.0 kg
Fan volume	2.0 dm^3
Fan losses	70 W

Tab. A.5: Optimized Input Parameters.

ACT FEM model	
$n_{\text{turn},1} \in [5, 120]$	Primary number of turns (int.)
$n_{\text{turn},2} \in [5, 120]$	Secondary number of turns (int.)
$r_{\text{min}} \in [20, 180]$ mm	Minimum coil radius
$x_{\text{shield}} \in [20, 180]$ mm	Shield distance (x direction)
$y_{\text{shield}} \in [20, 180]$ mm	Shield distance (y direction)
$d_{\text{iso}} \in [5, 25]$ mm	Distance between the coils
$t_{\text{wire}} \in [0.5, 5.0]$ mm	Distance between the turns
$x_{\text{wire}}\, y_{\text{wire}} \in [6, 60]$ mm^2	Litz wire cross section
$x_{\text{wire}} / y_{\text{wire}} \in [1/3, 3]$	Litz wire aspect ratio
SRC-DCX model	
$k_{\text{winding}} \in [40, 48]$ %	Litz wire fill factor
$A_{\text{die}} \in [150, 300]$ mm^2	Chip area per switch
$f \in [25, 200]$ kHz	Operating frequency

Tab. A.6: Computed Figures of Merit.

ACT output variables		
V_{act}	dm^3	ACT boxed volume
m_{act}	kg	ACT mass
r_{act}	%	Ratio between the ACT height and width
$L_{\text{act,1}}$	µH	ACT primary inductance
$L_{\text{act,2}}$	µH	ACT secondary inductance
k_{act}	%	ACT magnetic coupling factor
C_{act}	pF	ACT interwinding capacitance
P_{act}	kW	ACT losses
$\hat{E}_{\text{act}}$	kV/cm	ACT peak electric field
h_{act}	W/cm^2	ACT thermal dissipation per area
ρ_{act}	kW/dm^3	ACT volumetric power density
γ_{act}	kW/kg	ACT gravimetric power density
η_{act}	%	ACT efficiency
SRC-DCX output variables		
A_{src}	mm^2	SRC-DCX total chip area
P_{src}	kW	SRC-DCX losses
κ_{src}	W/mm^2	SRC-DCX chip area power density
λ_{src}	%	SRC-DCX power factor
ξ_{src}	%	SRC-DCX peak voltage ratio
η_{src}	%	SRC-DCX efficiency

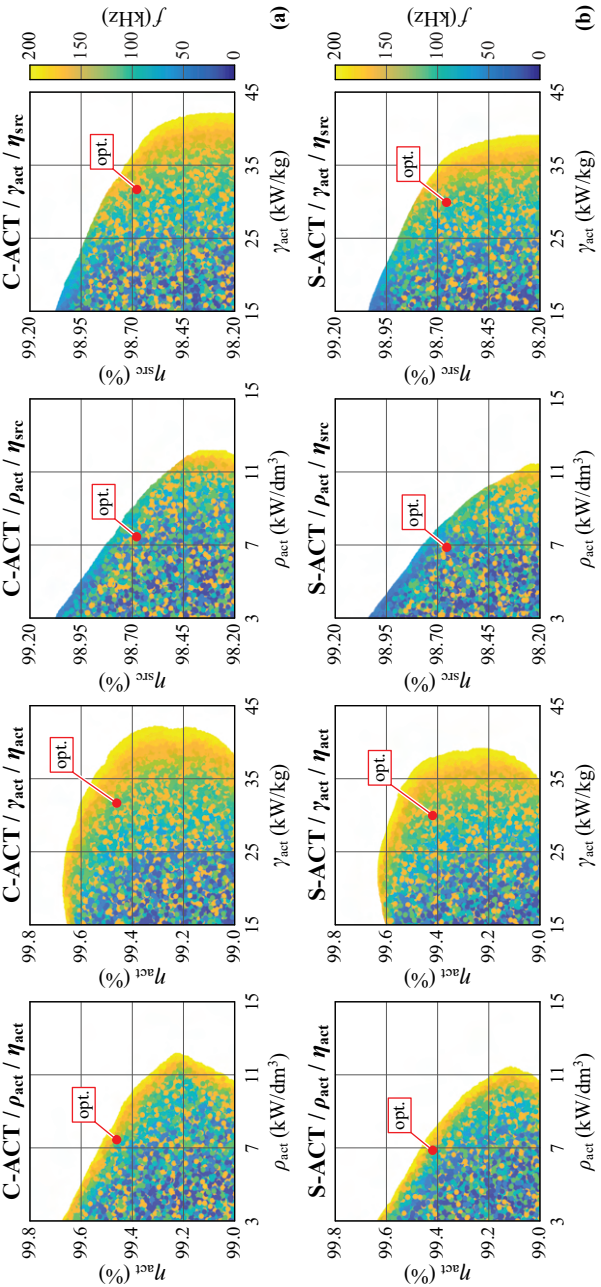


Fig. A.6: Pareto fronts for **(a)** C-ACT and **(b)** S-ACT. The efficiency of the ACT and complete SRC-DCX are considered for both the gravimetric and volumetric densities. The frequencies (color map) are randomly sorted in order to show the design space diversity. The optimal designs (cf. (A.14)) are highlighted in red.

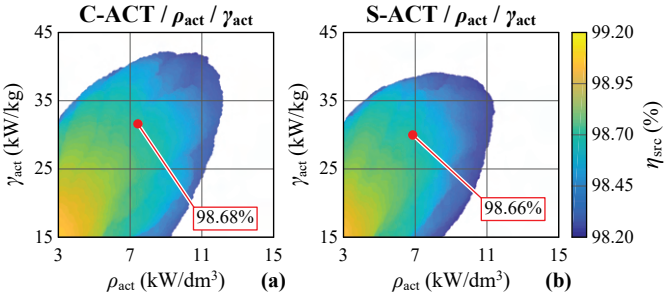


Fig. A.7: Correlation between the gravimetric and volumetric densities for **(a)** C-ACT and **(b)** S-ACT. For each combination ($\rho_{act} - \gamma_{act}$), only the designs with the highest SRC-DCX efficiencies (color map) are shown. The optimal designs (cf. (A.14)) are highlighted in red.

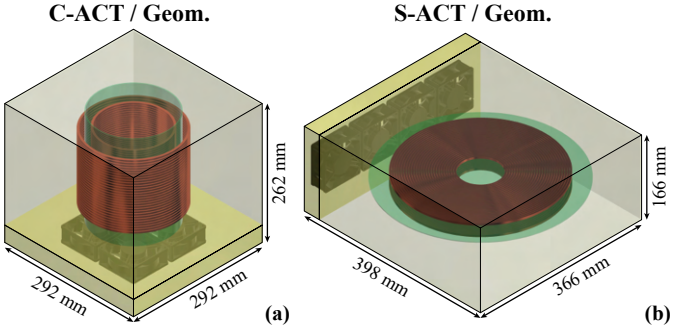


Fig. A.8: (a) Optimal C-ACT geometry. **(b)** Optimal S-ACT geometry. The coils (sienna), the fans (yellow), the dielectric barrier (green), and the shield (gray) are depicted.

Fig. A.7 shows the correlation between the SRC-DCX efficiency and the ACT gravimetric and volumetric densities. It can be seen that, for a given efficiency, interesting trade-offs exist between the gravimetric and volumetric densities.

A.5.2 Optimal Designs

The optimal designs (C-ACT and S-ACT) obtained with the aforementioned optimization workflow (cf. **Section A.4.7**) and cost function (cf. **Section A.4.8**) are depicted in **Fig. A.8**. These optimal designs are computed with 3-D FEM models and the deviation with respect to the 2-D axisymmetric models is below 5 % for all the considered variables (cf. **Tab. A.6**).

Tab. A.7 and **Tab. A.8** describe the optimized input variables and the obtained figures of merit. Both ACT optimal designs feature extreme gravimetric power densities (above 25 kW/kg) while maintaining good efficiencies (above 99.4 %) and volumetric power densities (above 6.5 kW/dm^3). The efficiencies of the complete optimal SRC-DCX systems are also above 98.6 %.

Fig. A.9 shows the magnetic field pattern without the shield. The magnetic field is mostly confined between the coils but a non-negligible stray field (above 5 mT) is also created by the magnetizing current. This issue is resolved by the conductive shield, as shown in **Fig. A.10**. The eddy currents in the shield are, as expected, completely blocking the magnetic field. It should be noted that, for the optimal designs, the shield is placed in the direct vicinity of the coil in order to limit the volume and the mass. This implies that the

Tab. A.7: Optimal Designs / Parameters.

Var.	C-ACT	S-ACT
P_{out}	166 kW	166 kW
V_{DC}	7 kV	7 kV
$\hat{v}_{\text{CM}}$	14 kV	14 kV
$n_{\text{turn,1}}$	36	27
$n_{\text{turn,2}}$	29	27
r_{min}	64.0 mm	39.0 mm
x_{shield}	55.4 mm	35.9 mm
y_{shield}	44.5 mm	69.8 mm
d_{iso}	17.8 mm	18.0 mm
t_{wire}	1.3 mm	0.6 mm
x_{wire}	4.3 mm	3.4 mm
y_{wire}	3.3 mm	4.3 mm
k_{winding}	48.0 %	48.0 %
A_{die}	225.0 mm^2	225.0 mm^2
f	161.8 kHz	148.6 kHz

losses in the shield and the impact of the shield on the inductance matrix cannot be neglected. More specifically, the losses in the shield amount to 18 % and 20 % of the total C-ACT and S-ACT losses, respectively. However, these numbers could be reduced to 9 % and 10 % if the shield would be placed 20 mm further away from the coils, indicating a clear trade-off between the shield losses and the power density.

A.5.3 Geometry Comparison

Fig. A.6 reveals that the C-ACT and S-ACT feature extremely similar Pareto fronts. Nevertheless, the maximum volumetric and gravimetric power densities of the C-ACT designs are slightly superior: 7 % and 6 %, respectively. **Fig. A.7** shows that, for a given power density (gravimetric and volumetric), SRC-DCXs featuring C-ACTs are slightly more efficient (0.02 % to 0.15 %) than SRC-DCX with S-ACT.

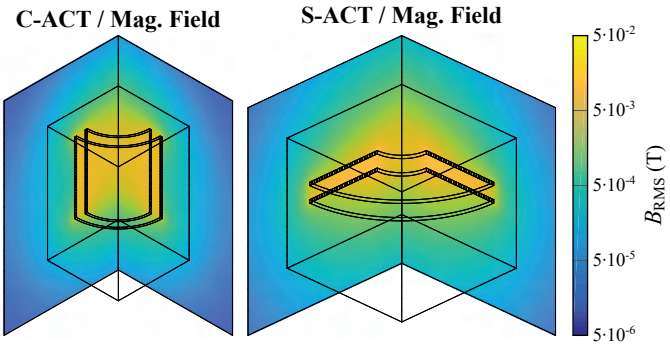


Fig. A.9: RMS magnetic field produced by the ACT coils without shielding. As the ACT features symmetry planes, only one quarter of the geometry is shown. The position of the shield is indicated to allow for a direct comparison with **Fig. A.10**.

A comparison between the optimal C-ACT and S-ACT designs (cf. **Section A.5.2**) also indicates a slight advantage for the C-ACT geometry with a 3 % lower cost function value (cf. **Section A.4.8**). However, all the parameters (e.g., frequency, inductance, volume, mass, and losses) are similar for both designs, indicating that the trade-offs are the same for C-ACT and S-ACT geometries.

It should be noted that, despite the lower performance, the S-ACT geometry has several advantages over the C-ACT. First, the S-ACT designs typically feature a flat geometrical aspect ratio, making them easier to integrate into converter systems. Additionally, the flat structure of S-ACT facilitates the coil former design, the cooling, and the common-mode insulation. Therefore, in many cases, the practical advantages of S-ACT compensate for the slightly increased losses.

Due to the similarities between the C-ACT and S-ACT geometries, the remaining analyses (loss sharing, part-load efficiency, frequency trade-off, design space diversity, and insulation distances) are conducted with C-ACT geometries. However, all the conclusions are also valid for S-ACT.

A.5.4 Volume, Mass, and Loss Sharing

Fig. A.11 depicts the volume, mass, and loss sharing for the optimal C-ACT design (cf. **Section A.5.2**). It can be seen that the copper volume is almost negligible (less than 1 %), explaining the reduced weight of the ACT. Most of the volume is the boxed volume around the coil and the boxed volume

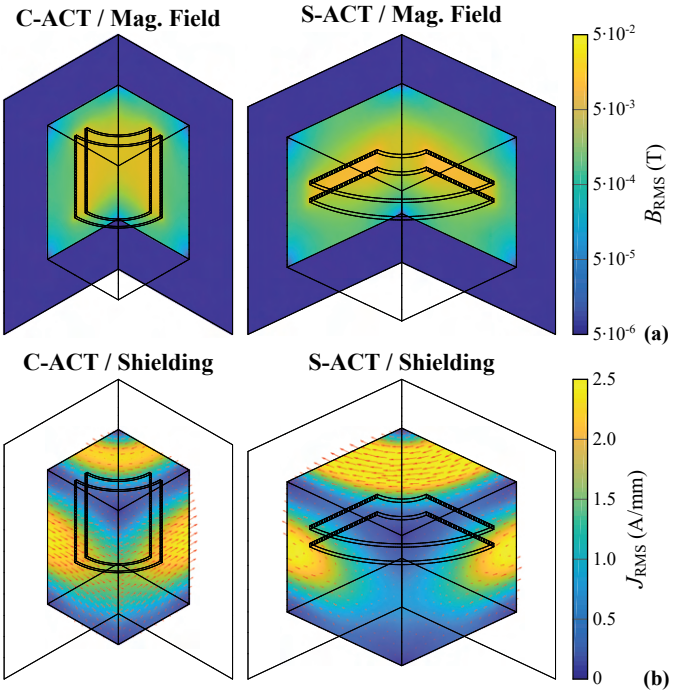


Fig. A.10: (a) RMS magnetic field inside and outside the shield. **(b)** RMS eddy current density in the shield. As the ACT features symmetry planes, only one quarter of the geometry is shown.

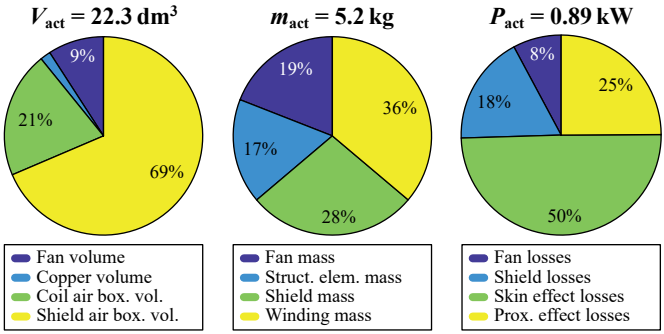


Fig. A.11: Volume, mass, and loss sharing for the ACT. The optimal C-ACT design (cf. **Section A.5.2**) is considered.

required for the shield. Therefore, it can be concluded that the volume of the ACT is only fully defined with a shield or a detailed stray field analysis. Due to the limited mass of the copper (coils and shield), the mass of the fans and structural elements is not negligible. Finally, even if the majority of the losses originates from the coils, the shield's eddy-current losses cannot be neglected either.

A.5.5 Part-Load Efficiency

The part-load behavior of a SRC-DCX using an ACT is of high interest. More particularly, the impact of large magnetizing currents and high operating frequencies (compared to systems using MCTs) should be examined. **Fig. A.12** shows the part-load behavior of the optimal C-ACT design (cf. **Section A.5.2**). It can be seen that the SRC-DCX still features an efficiency of 98 % at 33 % load.

The part-load performance can be analyzed as follows. The MOSFET switching losses are load-independent. The winding losses, resonant capacitor losses, and the MOSFET conduction losses have two components: a quadratic term (proportional to the load current) and a constant term (due to the magnetizing current). Finally, the shielding losses are mostly load-independent, indicating that they are mainly linked the magnetizing current. It can be concluded that the part-load behavior of a SRC-DCX with an ACT is very similar to the case with a MCT. The impact of the magnetizing current losses in an ACT is comparable to the core losses in a MCT.

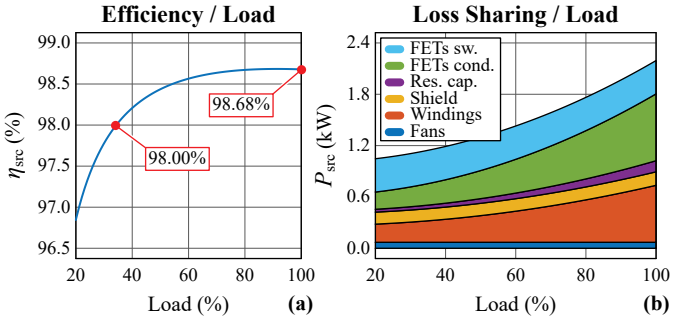


Fig. A.12: (a) SRC-DCX efficiency. **(b)** Loss sharing. The optimal C-ACT design is selected and operated at different loads (cf. **Section A.5.2**).

A.5.6 Optimal Operating Frequency

The choice of the operating frequency is one of the critical parameters for ACTs. In order to analyze the trade-offs, the optimal C-ACT design (cf. **Section A.5.2**) is selected and operated at different frequencies. All the other parameters (e.g., voltage, power level, and geometry) are kept constant, only the value of the resonant capacitors is adapted to the operating frequency. **Fig. A.13** shows the obtained results, which are interpreted as follows:

- *Power factor* - The impedance of the ACT is proportional to the frequency. This implies that the magnetizing current is inversely proportional to the frequency. Therefore, the power factor of the SRC-DCX (cf. (A.12)) increases with increasing frequency (towards the theoretical maximum of the SRC-DCX, $\sqrt{8}/\pi \approx 90\,\%$).
- *MOSFET switching losses* - As expected, the switching losses are increasing with the frequency. However, this effect is slightly mitigated by a reduction of the ZVS current, which is proportional to the magnetizing current (current-dependency of the ZVS losses, cf. (A.2)).
- *MOSFET conduction losses* - The conduction losses are quadratic with respect to the RMS current. Therefore, the conduction losses are reduced with increasing frequency (due to the increased power factor).
- *Resonant capacitor losses* - Two reasons explain the increase of the capacitor losses with the frequency: the frequency-dependency of the dissipation factor (cf. (A.3)) and the increased reactive power in the resonant capacitors.

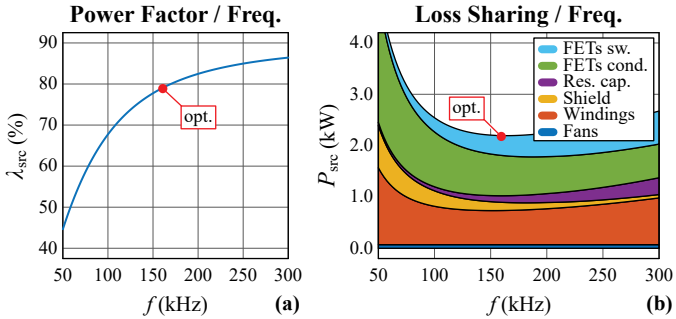


Fig. A.13: (a) SRC-DCX power factor. **(b)** Loss sharing. The optimal C-ACT design is selected and operated at different frequencies (cf. **Section A.5.2**). The optimal frequency is highlighted in red.

- *Shield losses* - The fact that the shielding losses are decreasing with the frequency is especially interesting. The resistances describing the shield losses slightly increases with the frequency (approximately with the square root of the frequency). However, the eddy currents in the shield are mostly produced by the magnetizing current, which is inversely proportional to the frequency. As a result, the shield losses decrease with increasing frequency.
- *Winding losses* - The winding losses are quadratic with respect to the RMS current. The RMS current decreases with increasing frequency (due to the increased power factor). However, the resistance matrix describing the winding losses increases with the frequency (due to the skin and proximity effects). Therefore, with these two counteracting effects, the winding losses are optimal for a given frequency.

As shown in **Fig. A.13**, the sum of all the loss components features a minimum at the optimal frequency. It should be noted that the optimal frequency of the ACT is, in the general case, different from the optimal frequency of the complete SRC-DCX. Furthermore, the optimum is flat with respect to the frequency, indicating that quasi-optimal losses are obtained for a wide range of frequencies.

A.5.7 Design Space Diversity

The aforementioned operating frequency trade-off indicates that the mapping between the design space (cf. **Tab. A.5**) and the performance space (cf.

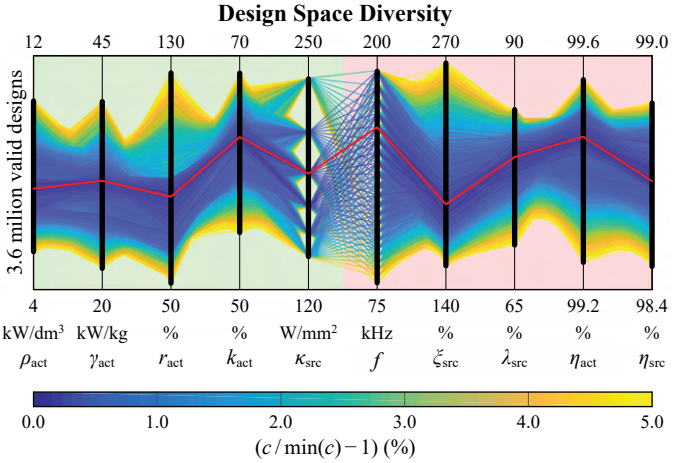


Fig. A.14: Parallel coordinate plot of the quasi-optimal C-ACT designs. Each line represents a design with a cost function value close to the minima (within a 5 % tolerance). In total 3.6 million quasi-optimal designs are plotted. The optimal C-ACT (cf. **Section A.5.2**) is highlighted in red.

Tab. A.6) is complex and very different designs will feature similar performance (i.e., design space diversity). Therefore, the design space diversity around the optimal C-ACT design (cf. **Section A.5.2**) is examined. All the designs with a cost function value (cf. **Section A.4.8**) less than 5 % above the minima are considered. **Fig. A.14** depicts all the obtained quasi-optimal designs in a parallel coordinate plot.

Many different designs are mapped to quasi-optimal cost function values. This implies that the optimum is flat and that many trade-offs exist. The design space diversity is particularly significant for the switching frequency considering that many effects compensate each other (cf. **Fig. A.13**). It can also be seen that designs with the highest magnetic coupling and power factors are not automatically optimal since other factors are also important for the ACT (e.g., coil impedance, coil quality factor, and power density trade-offs).

Finally, the parallel coordinate plot is useful to select the proper cost function and to ensure that all the degrees of freedom in the design space have been leveraged. The parallel coordinate plot shows that multi-objective optimization (e.g., mass, volume, and efficiency) is required in order to extract the full potential of SRC-DCXs with ACTs. Due to the size of the design space

and the complexity of the mapping between the design and performance spaces, a Pareto optimization with two variables (mass vs. losses or volume vs. losses) is not sufficient to capture the design trade-offs in a satisfactory manner.

A.5.8 Insulation Distance

As shown in **Section A.5.1** and **Section A.5.2**, high performance can be achieved with large insulation distances between the coils, allowing for an air insulation concept. However, a large insulation distance is diminishing the magnetic coupling of the ACT, leading to a reduced power factor (λ) and an increased peak voltage in the resonant capacitors (ξ). Therefore, examining the impact of the insulation distance on the system performance is interesting.

Fig. A.15 depicts the obtained Pareto fronts (ACT and SRC-DCX) for different insulation distances (cf. (A.11)). The red curves show the Pareto fronts respecting the constraint $\hat{E}_{\text{act}} < 15\,\text{kV/cm}$, which corresponds to the Pareto fronts shown in **Fig. A.6(a)**. As expected, designs with low insulation distances feature better performance, especially for the volumetric power density (i.e., 40 % increase). However, the designs with low insulation distances would require dry-type or liquid insulation concepts which are significantly more complex (e.g., thermal management, partial discharges, dielectric losses, and manufacturing) [18, 43, 190]. These results also highlight that ACTs are an interesting concept for high-power low-voltage systems with reduced insulation requirements [173].

A.6 ACT Scaling Laws

The goal is to derive ACT scaling laws similar to the results obtained in [102] for MCTs. Scaling laws are not meant to provide accurate quantitative results but general qualitative statements about the performance achievable with ACTs for different power levels, power densities, and voltages. Hence, several assumptions are required in order to obtain closed-form solutions:

- *Circuit model* - The SRC-DCX depicted in **Fig. A.1**, which features half-bridges with split DC-links and a 1 : 1 voltage transfer ratio, is considered. However, the extracted scaling laws are valid for any SRC-DCX configuration.

Tab. A.8: Optimal Designs / Figures of Merit.

Var.	C-ACT	S-ACT
V_{act}	22.3 dm^3	24.2 dm^3
m_{act}	5.2 kg	5.5 kg
r_{act}	81.8 %	45.5 %
$L_{\text{act},1}$	89.6 µH	96.8 µH
$L_{\text{act},2}$	83.7 µH	96.8 µH
k_{act}	63.1 %	61.7 %
C_{act}	49.6 pF	47.0 pF
P_{act}	0.89 kW	0.96 kW
$\hat{E}_{\text{act}}$	15.0 kV/cm	14.9 kV/cm
h_{act}	0.28 W/cm^2	0.28 W/cm^2
ρ_{act}	7.5 kW/dm^3	6.9 kW/dm^3
γ_{act}	31.6 kW/kg	29.9 kW/kg
η_{act}	99.46 %	99.42 %
A_{src}	900.0 mm^2	900.0 mm^2
P_{src}	2.19 kW	2.23 kW
κ_{src}	184.4 W/mm^2	184.4 W/mm^2
λ_{src}	79.2 %	79.3 %
ξ_{src}	187.4 %	184.8 %
η_{src}	98.68 %	98.66 %
c	1.11	1.14

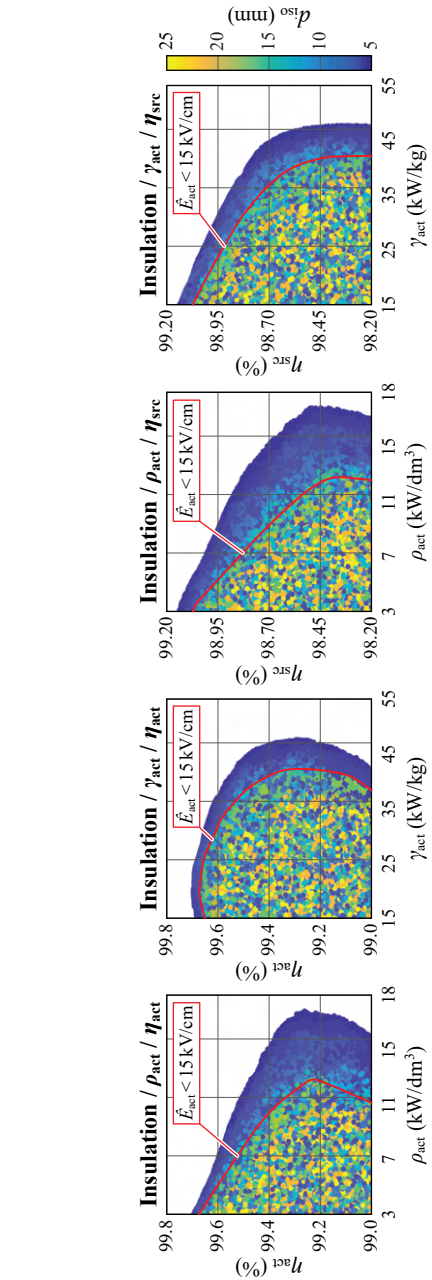


Fig. A.15: Pareto fronts for different insulation distances (C-ACT geometries). The efficiency of the ACT and complete SRC-DCX are considered for both the gravimetric and volumetric densities. The insulation distances (color map) are randomly sorted in order to show the design space diversity. The red curves show the Pareto fronts respecting the constraint $\hat{E}_{act} < 15$ kV/cm, which corresponds to the Pareto fronts shown in **Fig. A.6(a)**.

- *Waveform model* - A fundamental frequency approximation of the SRC-DCX waveforms, which include the load and magnetizing currents, is made.
- *Loss model* - The ACT winding losses, including the high-frequency effects, are considered. The losses produced by the semiconductors, the resonant capacitors, and the shield are neglected.
- *Winding model* - The windings are modeled as blocks, i.e., the discrete turns are not considered. The stranding (strand diameter and fill factor) is accepted to be constant. The number of turns is assumed to be a continuous (non-discrete) variable and the same number of turns is used for both coils.
- *Scaling* - The volume of the ACT is scaled with a homothetic transformation, i.e., all the dimensions (e.g., litz wire dimension, coil dimension, insulation distance, and shield geometry) are scaled together.

With these assumptions, the inductance and resistance matrices can be expressed as functions of the ACT boxed volume (V_{act}), the number of turns (n), and the operating frequency (f). The inductance matrix is frequency-independent and can be scaled as

$$L_{\text{act}}\left(V_{\text{act}}, n\right) = \begin{bmatrix} L_{\text{act},1} & L_{\text{act,m}} \\ L_{\text{act,m}} & L_{\text{act},2} \end{bmatrix} = V_{\text{act}}^{+\frac{1}{3}} n^2 L'_{\text{act}}, \tag{A.15}$$

where L'_{act} represents a scaled (per turn and per volume) inductance matrix. The frequency-independent resistance matrix (R_{lf}) is a diagonal matrix, which represents the low-frequency losses of the ACT windings [102]:

$$R_{\text{lf}}\left(V_{\text{act}}, n\right) = \begin{bmatrix} R_{\text{lf},1} & 0 \\ 0 & R_{\text{lf},2} \end{bmatrix} = V_{\text{act}}^{-\frac{1}{3}} n^2 R'_{\text{lf}}, \tag{A.16}$$

where R'_{lf} represents a scaled (per turn and per volume) low-frequency resistance matrix. The frequency-dependent resistance matrix (R_{hf}) contains off-diagonal elements and models the proximity effect losses of the ACT windings, which are quadratic with respect to the frequency [102]:

$$R_{\text{hf}}\left(V_{\text{act}}, f, n\right) = \begin{bmatrix} R_{\text{hf},1} & R_{\text{hf,m}} \\ R_{\text{hf,m}} & R_{\text{hf},2} \end{bmatrix} = V_{\text{act}}^{+\frac{1}{3}} f^2 n^2 R'_{\text{hf}}, \tag{A.17}$$

where R'_{hf} represents a scaled (per turn, per frequency, and per volume) high-frequency resistance matrix. Finally, the area available for the cooling of the coils can be expressed as a function of the boxed volume:

$$A_{\mathrm{act}}\left(V_{\mathrm{act}}\right) = V_{\mathrm{act}}^{+\frac{2}{3}} A'_{\mathrm{act}}. \tag{A.18}$$

The load and magnetizing current peak values can be computed with a fundamental frequency approximation, as shown in [18]. The following results are obtained:

$$\begin{aligned} \hat{i}_{\mathrm{load}} &= \sqrt{2}\frac{\pi}{\sqrt{8}}\frac{P_{\mathrm{out}}}{V_{\mathrm{DC}}/2}, \\ \hat{i}_{\mathrm{mag}} &= \frac{4}{\pi}\frac{V_{\mathrm{DC}}/2}{2\pi f L_{\mathrm{act,m}}}, \end{aligned} \tag{A.19}$$

where P_{out} and V_{DC} represent the power flow and the DC-link voltage, cf. **Fig. A.1**. It should be noted that the leakage impedances ($L_{\mathrm{act},1} - L_{\mathrm{act,m}}$ and $L_{\mathrm{act},2} - L_{\mathrm{act,m}}$) are canceled by the resonant capacitors and, therefore, have no impact on the load and magnetizing currents. The magnetizing current is equally split between the primary and secondary sides, leading to the following current phasors [18]:

$$\hat{i} = \begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \end{bmatrix} = \begin{bmatrix} +\hat{i}_{\mathrm{load}} - \mathrm{j}\frac{\hat{i}_{\mathrm{mag}}}{2} \\ -\hat{i}_{\mathrm{load}} - \mathrm{j}\frac{\hat{i}_{\mathrm{mag}}}{2} \end{bmatrix}. \tag{A.20}$$

With the defined resistance matrices (cf. (A.16) and (A.17)) and the current vector (cf. (A.20)), the main figures of merit of the ACT can be computed. More specifically, the ACT losses, the loss fraction, the thermal stress, and the power density are extracted:

$$\begin{aligned} P_{\mathrm{act}} &= \frac{1}{2}\hat{i}^{*}\left(R_{\mathrm{lf}} + R_{\mathrm{hf}}\right)\hat{i}, \\ \epsilon_{\mathrm{act}} &= \frac{P_{\mathrm{act}}}{P_{\mathrm{out}}}, \\ h_{\mathrm{act}} &= \frac{P_{\mathrm{act}}}{A_{\mathrm{act}}}, \\ \rho_{\mathrm{act}} &= \frac{P_{\mathrm{out}}}{V_{\mathrm{act}}}. \end{aligned} \tag{A.21}$$

Additionally, the power factor of the SRC-DCX, which is a figure of merit for the reactive power delivered by the semiconductor bridges, is defined as

$$\lambda_{\mathrm{src}} = \frac{P_{\mathrm{out}}}{\frac{1}{2}\left(\frac{V_{\mathrm{DC}}}{2}\frac{|\hat{i}_1|}{\sqrt{2}} + \frac{V_{\mathrm{DC}}}{2}\frac{|\hat{i}_2|}{\sqrt{2}}\right)}. \tag{A.22}$$

The ACT losses are subject to the following trade-offs. Low operating frequencies and/or low numbers of turns are leading to large magnetizing currents (cf. (A.15) and (A.19)) and, therefore, large losses. On the other hand, high-frequencies and/or high numbers of turns are linked to large winding resistance matrices (cf. (A.16) and (A.17)). Therefore, the frequency and the number of turns feature an optimum:

$$\left(f_{\mathrm{opt}}, n_{\mathrm{opt}}\right) = \underset{f,n}{\operatorname{argmin}} P_{\mathrm{act}}\left(f, n\right). \tag{A.23}$$

Analytical expressions for f_{opt} and n_{opt} exist and can be easily extracted with a symbolic calculus tool. However, the obtained results cannot be written compactly and therefore are not presented in this work.

For the scaling laws, different boundary conditions are considered: constant volume, constant voltage, constant power, and constant power density. Additional, only optimal designs (cf. (A.23)) are used. The resulting scaling coefficients are depicted in **Tab. A.9** and can be interpreted as follows:

- Changing the voltage level can be achieved by adapting the number of turns. All the other metrics (frequency, efficiency, thermal stress, and power factor) are not affected.
- A variation of the power level with a constant volume does not impact the operating frequency, the power factor, and the achieved efficiency. However, it should be noted that the maximum power level is limited by the thermal limit.
- Changing the ACT volume (homothetic transformation) with a constant power level does not impact the power factor. Large ACTs are more efficient and operated at lower frequencies. Compact designs will, under a certain volume, run over the thermal limit.
- The scaling of the power level with a constant power density indicates that high-power ACTs are more efficient and operated at lower frequencies. Nevertheless, the power factor and the thermal stress remain constant, indicating that ACTs are applicable for a wide range of power levels.

A comparison between **Tab. A.9** and the MCT scaling laws presented in [102] reveals their similarities. Therefore, it can be concluded that ACTs represent an interesting alternative to MCTs for a large range of power levels, power densities, and voltages.

Tab. A.9: ACT Scaling Laws ($f = f_{\mathrm{opt}} \ \wedge \ n = n_{\mathrm{opt}}$).

$\boldsymbol{V_{\mathrm{DC}}}$**=var.** $\wedge$ $\boldsymbol{P_{\mathrm{out}}}$**=const.** $\wedge$ $\boldsymbol{V_{\mathrm{act}}}$**=const.**		
f_{opt}	$\propto$	const.
n_{opt}	$\propto$	$(V_{\mathrm{DC}})^{+1}$
ϵ_{act}	$\propto$	const.
h_{act}	$\propto$	const.
λ_{src}	$\propto$	const.
$\boldsymbol{P_{\mathrm{out}}}$**=var.** $\wedge$ $\boldsymbol{V_{\mathrm{act}}}$**=const.** $\wedge$ $\boldsymbol{V_{\mathrm{DC}}}$**=const.**		
f_{opt}	$\propto$	const.
n_{opt}	$\propto$	$(P_{\mathrm{out}})^{-1/2}$
ϵ_{act}	$\propto$	const.
h_{act}	$\propto$	$(P_{\mathrm{out}})^{+1}$
λ_{src}	$\propto$	const.
$\boldsymbol{V_{\mathrm{act}}}$**=var.** $\wedge$ $\boldsymbol{P_{\mathrm{out}}}$**=const.** $\wedge$ $\boldsymbol{V_{\mathrm{DC}}}$**=const.**		
f_{opt}	$\propto$	$(V_{\mathrm{act}})^{-1/3}$
n_{opt}	$\propto$	const.
ϵ_{act}	$\propto$	$(V_{\mathrm{act}})^{-1/3}$
h_{act}	$\propto$	$(V_{\mathrm{act}})^{-1}$
λ_{src}	$\propto$	const.
$\boldsymbol{P_{\mathrm{out}}}$**=var.** $\wedge$ $\boldsymbol{\rho_{\mathrm{act}}}$**=const.** $\wedge$ $\boldsymbol{V_{\mathrm{DC}}}$**=const.**		
f_{opt}	$\propto$	$(P_{\mathrm{out}})^{-1/3}$
n_{opt}	$\propto$	$(P_{\mathrm{out}})^{-1/2}$
ϵ_{act}	$\propto$	$(P_{\mathrm{out}})^{-1/3}$
h_{act}	$\propto$	const.
λ_{src}	$\propto$	const.

A.7 Conclusion

This Appendix describes the modeling and optimization of an air-core transformer (ACT) for a medium-voltage DC-DC series resonant converter (SRC) operating as DC transformer (DCX) between two 7 kV buses at a rated power of 166 kW. Two different geometries are considered for the ACT, a structure with concentric cylindrical coils (C-ACT) and a flat structure with spiral coils (S-ACT). The ACT coils are realized with litz wires and surrounded by a metallic shield that blocks the magnetic and electric stray fields.

A complete model of the SRC-DCX is presented with a special focus on the ACT. The ACT is modeled with FEM, taking into account the eddy currents in the shield, the skin and proximity losses of the windings, the impact of the harmonics, the thermal limit, and the insulation distances. The ACT model has been successfully validated with measurements. Due to the large number of variables, an optimization strategy that combines a genetic algorithm (for the ACT) and brute force grid search (for the SRC-DCX) has been implemented. This allows for the extraction of the multi-objective (volume, mass, chip area, and losses) optimal mapping between the design and performance spaces.

It has been shown that both geometries (C-ACT and S-ACT) are suitable for realizing ACTs and feature similar performance. The main advantage of ACTs is their gravimetric power density (up to 41 kW/kg), which is three to eight times higher than classical medium-frequency transformers. With the presented fully coupled model (co-optimization of the coils and the shield geometry), significant improvements of the volumetric power density of ACTs (up to 12 kW/dm^3) are obtained. Moreover, despite the limited magnetizing inductance and magnetic coupling of ACTs, very good efficiencies are achievable for the complete SRC-DCX, i.e., up to 99.05 %. Hence, it appears that ACTs are a competitive solution for DC-DC converters with weight constraints, high-temperature specifications, air insulation constraints, or strong linearity requirements.

Finally, the properties of the optimal systems are examined with respect to the loss sharing, the part-load behavior, the switching frequency, and the insulation distances. The ACTs are characterized by a very flat efficiency curve as well as flat loss optimum with respect to the operating frequency. However, it is found that the mapping between the design and performance space is complex, i.e., very different designs feature similar performances. This implies that numerical models and multi-objective optimizations are required to fully exploit the great potential of ACTs.

B

Investigations of Dry-Type Insulation & Magnetic Shielding in the ACT

This Appendix summarizes the most relevant research findings also published in:

- **P. Czyz**, T. Guillod, F. Krismer, and J. W. Kolar, "Exploration of the Design and Performance Space of a High Frequency 166 kW / 10 kV SiC Solid-State Air-Core Transformer," in *Proc. of the IEEE Int. Power Electron. Conf. (ECCE Asia)*, 2018.

The goal of this Appendix is to investigate the influence of dry-type insulation (silicone) and magnetic shielding on the gravimetric power density of coaxial solenoid ACTs. The modeling and data used in this Appendix has a preliminary character and differ from the optimization presented in **Chapter 3**, however it is sufficient to demonstrate the influence of adding dry-type insulation or using magnetic shielding in ACTs. In this regard, in the following, first the differences in methodology compared to **Chapter 3** are explained and next the results of considerations are shown.

For the analysis of dry-type insulation and magnetic shielding in the ACT, a 1:1-DCX according to the specifications (cf. **Tab. 2.2**) and models presented in **Section 2.2.1** are considered. However, instead of half-bridge-based primary and secondary power semiconductor stages, full-bridge realizations are used. The ACT is implemented with two coaxially arranged primary and secondary windings connected in an *asymmetric* fashion, see **Fig. 3.2(a)**, i.e., inner coils

being connected in series to form the primary winding and the two outer coils connected likewise to form the secondary winding.

In the following, first 2–D FEM-based modelling for multi-objective Pareto optimization is presented. From the optimization results we select an ACT design for investigations of dry-type insulation. Afterwards, the analysis is extended with 3–D FEM-based modelling of plates for magnetic shielding which are optimized for several selected designs. Finally, the results of subsequent optimizations are evaluated.

B.1 MV/MF ACT Modeling and Optimization

B.1.1 2–D FEM-Based Design and Optimization

Different approximations of the transformer configuration depicted in **Fig. 3.1(c)** can be considered. One approximation is to run separate 2–D FEM simulations for the two sets of coils, and determine the final values for inductances and couplings from the electric series connection of both sets of coils. This method is used in **Section 3.3.1**. Another 2–D approximation considers the placement of two sets of coils, coils I and II (see **Fig. B.1**), coaxially in series such that a single set of coils with a length of $2l$ results. The first approach fully decouples coils I and II and underestimates the coupling, whereas the second approach overestimates the coupling. In this Appendix, the second approach is selected with the corresponding axisymmetric 2–D FEM model shown in **Fig. B.1**. The employed 2–D model considers no shielding plates. Furthermore, the primary coil (inner solenoid) is separated from the secondary coil (outer solenoid) by an isolation distance of width w_{iso}.

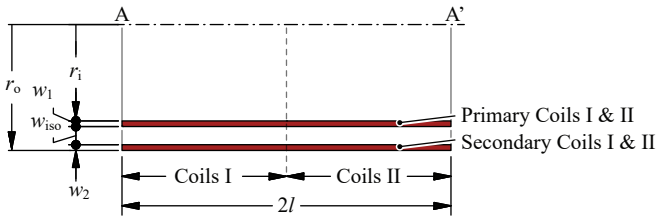


Fig. B.1: Schematic representation of the 2–D axisymmetric model (in r–, z–spatial coordinates, cylindrical axis A-A') of one set of the coils as used for the FEM simulation.

Tab. B.1: Design space and constant parameters for the FEM-based optimization.

Var.	Min.	Max.	# Pts.	Description
2–D FEM sweep				
f_s	20 kHz	200 kHz	15	operating frequency
N	30	200	170	number of turns
r_i	35 mm	105 mm	15	internal radius
w_1	5 mm	60 mm	15	width of outer coil
w_2	5 mm	60 mm	15	width of inner coil
l	60 mm	350 mm	15	length of coil
3–D FEM sweep				
s_d	50 mm	80 mm	4	shielding plate distance from end of transf. coils
s_w	4 mm	9 mm	15	thickness of shielding plate
d	1.05	1.20	4	shielding plate to transformer cross section ratio[1]
Constant parameters				
w_{iso}	16 mm			insulation distance
d_{litz}	71 µm			litz strand diameter
k_{litz}	28 %			total fill factor of the windings
k_{loss}	30 %			loss penalty due to imperfect twisting

[1] $s_a = d \cdot 4r_o$, $s_b = d \cdot 2r_o$, cf. **Fig. B.2**

For the investigated winding arrangement, the design space with geometry dimensions shown in **Table B.1** is fed to an optimization routine presented in **Fig. 2.3(a)**.

B.1.2 3–D FEM-Based Design and Optimization with Shielding Plates

The 3–D FEM simulations of the ACT are conducted for the actual physical configuration with splitted primary- and secondary-side coils, i.e., two sets of coils, such that the external magnetic fields cancel, see **Fig. 3.2(b)**. The simulations are conducted with and without shielding plates (back iron), for closing the flux path and/or for limiting the magnetic stray field, for three

selected, optimal 2–D designs. The results are presented and discussed in **Section B.2.3**.

Rectangular ferrite shielding plates (material N97) are assumed to be placed at both ends of the splitted coils according to **Fig. B.2**. For the 3–D models parameter sweeps for different geometries of plates are conducted, similarly to the procedure in **Fig. 2.3(a)**. However, only one optimization loop is realized since for one design the operating frequency and the number of turns are constant. Therefore, instead of the windings geometry sweep, the distances between coils and the plates, thicknesses, widths, and lengths of the plates are varied (cf. **Table B.1**). For each configuration, the model is solved and all performance indexes are calculated and stored. The modeled transformer has three planes of symmetry, thus, to reduce the computational effort, mirroring is used in all planes to simplify the model.

B.2 Evaluation

B.2.1 η-γ-ρ-Pareto Fronts Without Shielding (2–D FEM)

The η-γ-ρ-performance spaces (planes) and the η-γ-ρ-Pareto fronts that result from the 2–D FEM simulations for the ACT and ACT-DCX are shown in **Figs. B.3(a)–(d)**. From the η-γ-performance planes shown in **Figs. B.3(a),(c)** it becomes apparent that the ACT-DCX can achieve densities higher than 21 kW/kg, while still maintaining a comparably high efficiency of 99.0%. It is worth to point out that, even though there are high-efficient (99.7%) ACT designs (cf. **Fig. B.3(a)**) with relatively high switching frequencies up to 200 kHz, due to high switching losses of the transistors those designs have poor overall system performance (cf. **Fig. B.3(c)**). From the η-ρ-performance plane shown in **Figs. B.3(b)** and **(d)** it can be seen that the maximum achievable volumetric power density for an ACT is 17 kW/dm^3. The large volume of the ACT can be explained by the fact that either a higher number of turns (long transformer) or a larger diameter of the solenoid windings is needed to obtain effectively the same inductances in comparison to the MCTs.

For investigations of dry-type insulation, one ACT-DCX design is selected for analysis, as indicated by yellow stars in **Fig. B.3**, and it has the following characteristic: $\gamma = 16.1\,\mathrm{kW/kg}$, $\rho = 7.5\,\mathrm{kW/dm^3}$, $\eta = 99.0\,\%$, $f_\mathrm{s} = 103.6\,\mathrm{kHz}$, whereas the dimensions of the ACT are presented in **Fig. B.2**. The design is selected by introducing the following DCX performance criteria: efficiency >99.0% and the highest achievable gravimetric power density. The selected design is not located on the front of the Pareto plane because such design is

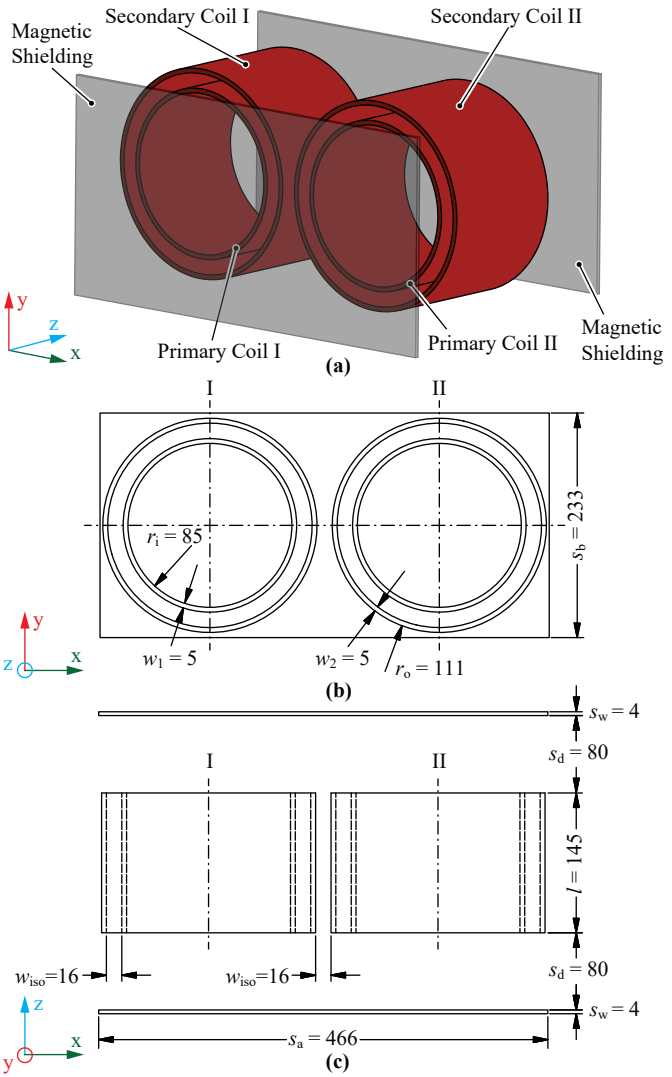


Fig. B.2: (a) Schematic representation of a MV/MF ACT with primary and secondary coils divided into two equal parts to provide guidance of the magnetic flux along the whole geometric path. Magnetic shielding plates provide the functions of back irons for stray fields at the ends of the transformer. **(b)** Projection from front. **(c)** Projection from top. Projections are in scale, dimensions are in mm.

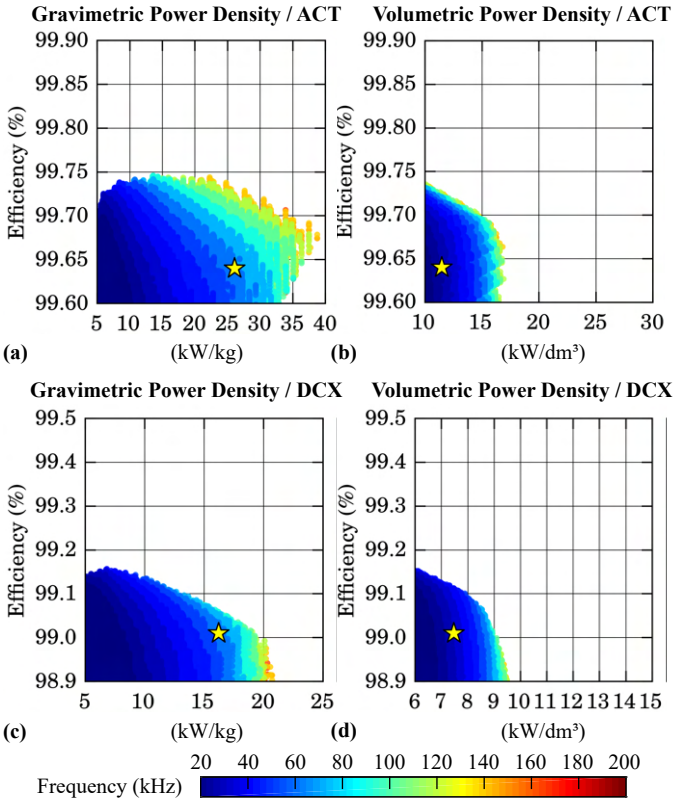


Fig. B.3: Results of the 166 kW / 7 kV multi-objective optimization (2–D FEM-based). η-γ-ρ-performance planes for the ACT: **(a)** gravimetric power density γ and **(b)** volumetric power density ρ; for the ACT-DCX: **(c)** gravimetric power density γ and **(d)** volumetric power density ρ.

not optimal after adding shielding plates, which is explained in more detail in **Section B.2.3**.

B.2.2 Investigations of Isolation Distances and Insulation in ACT

Further exploration of the design space of the ACT focuses on the inter-winding isolation distance and insulation material. In the analyzed system for the operating voltage of 7 kV the required withstand voltage for the transformer is chosen to be 10 kV. It can be achieved either with dry-type insulation for small distances or air insulation provided that the distance is at least equal to the air clearance distance for the required withstand voltage and given that no creepage path exists.

For the selected ACT design ({99.0%, 103.6 kHz}) additional 2–D FEM simulations are carried out for different isolation distances between the windings $w_{\text{iso}} \in \{1, 2, ..., 30\}$ mm and both insulation types: dry-type (silicone) and air. In case of dry-type insulation, the additional mass of the insulation material is accounted for in the gravimetric power density. In **Fig. B.4(a)** the volumetric power density for ACTs without shielding plates is presented along with the information about the coupling factor which varies from 0.67 to theoretically 0.94 for small isolation distances. **Figs. B.4(b),(c)** clearly show that feasible designs start from the dry-type insulation breakdown boundary (2.25 mm), which is the only possibility up to the air breakdown boundary (13.33 mm). As expected it is more beneficial to use air insulation as significantly higher gravimetric densities can be achieved, since air insulation designs have higher gravimetric power density than dry-type insulation designs with same isolation distance. Furthermore, the selected design ($w_{\text{iso}} = 16$ mm) with air insulation allows to avoid using additional insulation materials and associated challenges such as dielectric losses, and partial discharges [43].

B.2.3 η-γ-Pareto Fronts With Shielding Plates (3–D FEM)

Fig. B.5 shows the η-γ-performance space for an ACT-DCX, achieved from 2–D FEM simulations (without shielding plates, cf. **Fig. B.3(c)**). The designs are colored according to the lengths of the transformers. Additionally, three selected designs are shown for reference, for three different transformer lengths $2l \in \{17.5, 22.5, 29.0\}$ cm and equal efficiencies of 99.0%. Finally, for those three designs the corresponding Pareto optimal results with optimized shielding plates from 3–D FEM simulations are presented considering the

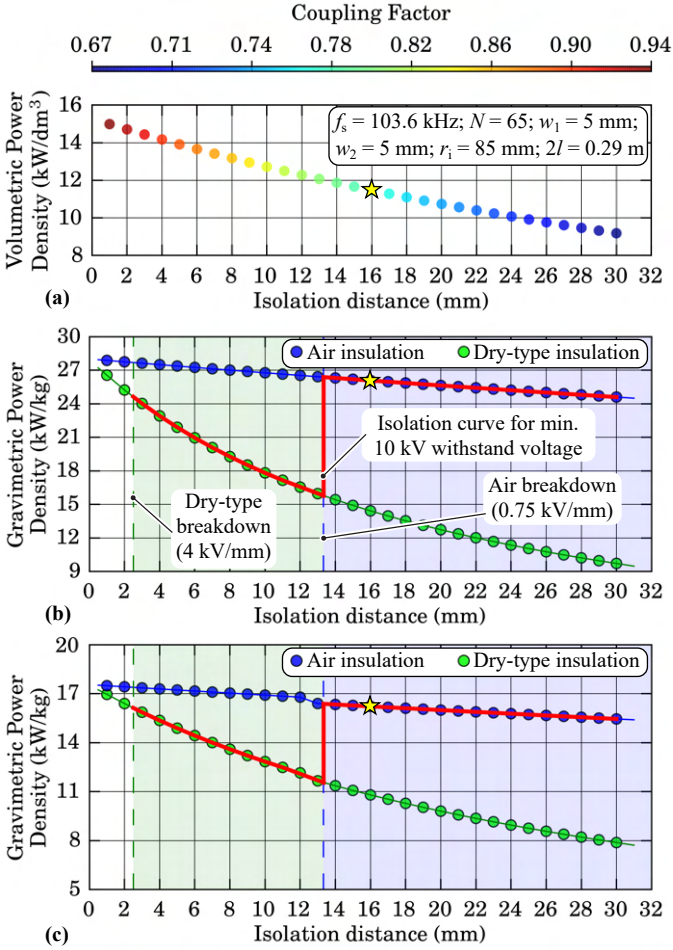


Fig. B.4: Volumetric and gravimetric power density for the selected ACT-DCX for different isolation distance w_{iso} between the windings and different insulation materials, i.e., air and silicone (from 2–D FEM simulations without shielding plates). **(a)** Volumetric power density of the ACT. **(b)** and **(c)** gravimetric power density of the ACT and ACT-DCX, respectively. For the chosen 10 kV withstand voltage, the breakdown boundaries and the resulting functional isolation curve for the system are plotted.

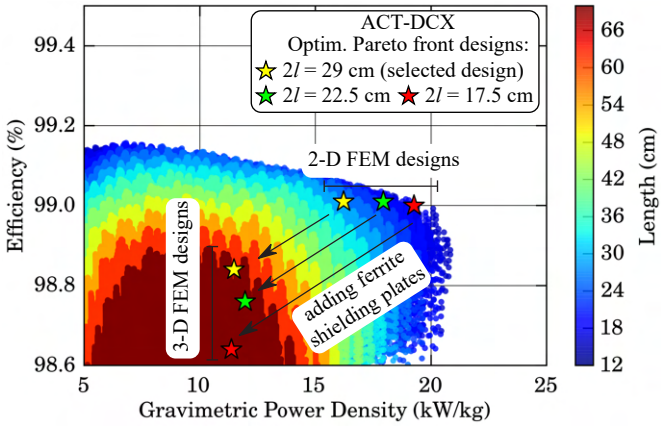


Fig. B.5: Results of the multi-objective optimization for the 166 kW / 7 kV ACT-DCX without shielding plates (2–D FEM) and with shielding plates (3–D FEM) for three designs of different transformer lengths. The mapping of 99% efficient 2–D designs calculated without considering shielding plates (**Fig. B.3(c)**) into corresponding optimal 3–D designs with plates is indicated with arrows.

shielding plates. The 3–D FEM optimal results are selected with respect to gravimetric power density and from the subset of designs, in which the shielding plates are not in saturation, i.e., the maximum magnetic flux density in the plates is below 300 mT.

From **Fig. B.5** it can be seen that choosing the optimal design without shielding plates ($2l$ = 17.5 cm) does not lead to the best design after adding the shielding plates. In fact, the best performance with shielding plates is achieved for the longest transformer that features the lowest gravimetric density without shielding plates. This relation can be explained by the fact that long transformers are also characterized by smaller outer diameters, which determine the sizes of the shielding plates. More detailed performance indexes of the selected optimal design ($2l$ = 29 cm) for all models, i.e., 2–D, 3–D without shielding plates, and 3–D with shielding plates, are shown in **Table B.2**. Adding the ferrite shielding plates generates additional losses, which causes a reduction of the efficiency of approx. 0.1% and a drop of the gravimetric density from 16.2 kW/kg to 11.5 kW/kg. On the other hand, the shielding plates realize the function of back iron for stray fields, which otherwise could cause eddy-current losses in surrounding conductive elements or generate EMI perturbations. In the presented case the shielding plates are

Tab. B.2: Performance indexes of the selected optimal design ($2l$ = 29 mm) of the ACT converter: 2–D, 3–D without shielding plates and 3–D with shielding plates.

Solution	Gravim. density (kW/kg)	Volum. density (kW/dm^3)	System efficiency (%)	Stray magnetic flux density (mT)
2–D	16.2	7.47	99.01	-
3–D without shielding plates	16.2	7.47	98.94	3.0
3–D with shielding plates	11.5	3.97	98.84	0.5

reducing the value of the magnetic flux density in axial distance of 94 mm from the end of the coils (1 cm from shielding plates) from 3.0 mT to 0.5 mT (cf. **Fig. B.6**), which is below typical values specific for MV magnetic core transformers [115].

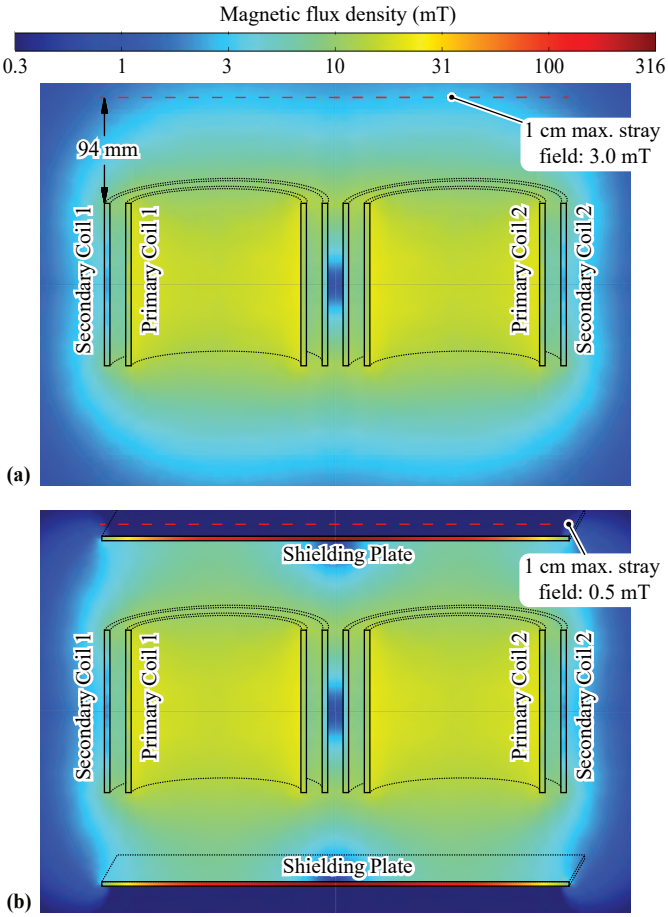


Fig. B.6: Results of the 3–D FEM simulation for the selected design: magnetic flux density in the xz–plane. Air-core transformer **(a)** without shielding plates and **(b)** with shielding plates. The maximum values of the magnetic flux density in 1 cm distance from shielding plates are provided.

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