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Advanced Modeling and Multi-Objective Optimization of Power Electronic Converter Systems

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Für meine Eltern
Rosa und Joe

"I suppose it is tempting, if the only tool you have is a hammer,
to treat everything as if it were a nail."

Abraham Maslow

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Contents

Kurzfassung

Dank der anhaltenden Fortschritte im Bereich der Leistungselektronik erfährt eine Vielzahl von Anwendungen elektrischer Energie eine stetig wachsende Durchdringung mit leistungselektronischen Konvertersystemen. Prominente Beispiele sind die Umwälzungen im Bereich der Energieerzeugung und –übertragung (Solar- und Windenergie, „Smart-Grid“) und die voranschreitende Elektrifizierung der Mobilität, welche beide durch erhöhtes Umweltbewusstsein und gesteigerte Funktionalitätsansprüche der modernen Gesellschaft getrieben sind. Für die Zukunft kann erwartet werden, dass der Bedarf nach noch leistungsfähigeren Konvertersystemen mit erhöhter Effizienz, Zuverlässigkeit und Funktionalität bei gleichzeitiger Reduktion von Kosten, Gewicht, Bauvolumen und Entwicklungszeit weiter steigen wird.

Das Studium der Fachliteratur zeigt, dass die Auslegungen und Optimierungen von Konvertersystemen oft nur punktuell und unter dem Gesichtspunkt von nur einem Zielkriterium oder wenigen Zielkriterien durchgeführt werden. Dies ist oft bedingt durch das Fehlen eines systematischen Ansatzes, der den typisch auftretenden Zielkonflikten zwischen den Performancegrössen (z.B. Bauvolumen gegen Effizienz) hinreichend Rechnung trägt. Darüber hinaus fehlen oft auch die geeigneten Modelle für die Quantifizierung von zusätzlichen Kenngrössen. Dies trifft in besonderem Masse für die Kostenbewertung von typischen Konverterkomponenten zu. Insgesamt können diese Umstände dazu führen, dass die optimale Lösung (Topologie, Modulationsverfahren und Auslegung) nicht gefunden wird, da die betrachteten Konvertersysteme und Technologien zu wenig umfassend bewertet und miteinander verglichen werden können.

Der Schwerpunkt dieser Dissertation liegt daher in der Entwicklung von Methoden welche systematische Mehrkriterien-Optimierungen sowie umfassende Vergleiche von leistungselektronischen Konvertersystemen hinsichtlich Effizienz, Volumen, Gewicht und Kosten ermöglichen. Hierzu werden auf Basis von analytischen Rechnungen, Simulationen und Messungen neue Modelle entwickelt, die typische Komponenten von Konvertersystemen wie Leistungshalbleiter, Induktivitäten, Kondensatoren, Kühler und Leiterplatten hinsichtlich dieser Kenngrössen bewerten können. Des Weiteren werden Modelle zur Beschreibung des Konverterverhaltens und der sich einstellenden Strom- und Spannungsverläufe abhängig vom Modulationsverfahren und Betriebspunkt hinzugefügt, wobei der Modellierung der Netzrückwirkungen und der elektro-

magnetischen Verträglichkeit (EMV) besondere Beachtung geschenkt wird. Das Ziel der Methodik besteht in der möglichst präzisen Voraussage der Eigenschaften eines Konvertersystems. Dies erlaubt eine effektive Systemoptimierung bei gleichzeitiger Reduktion der Anzahl gebauter Hardware Prototypen und insgesamt kürzerer Entwicklungszeit.

Die vorgeschlagenen Methoden werden für die Mehrkriterien-Optimierung und den Vergleich verschiedener DC/DC- und DC/AC-Anwendungen im Bereich der erneuerbaren Energien und unter Miteinbezug von SiC Leistungshalbleiter der neuesten Generation verwendet. Die Anwendungsbeispiele verdeutlichen einerseits die Fähigkeit der Methoden, hochkomplexe Optimierungsprobleme mit vergleichsweise kleinem Rechen- und Zeitaufwand lösen zu können. Andererseits beweisen Messungen anhand eines implementierten DC/DC Laborprototyps die hohe Modellgenauigkeit der Methoden. Die Ergebnisse der beiden Mehrkriterien-Optimierungen zeigen auf, dass der Einsatz von SiC Leistungshalbleiter in den betrachteten Anwendungen trotz höherer Bauteilkosten gegenüber herkömmlichen Si Leistungshalbleiter sinnvoll ist. In beiden Beispielen ermöglichen die überlegenen Eigenschaften von SiC Leistungshalbleiter erhebliche Verbesserungen der Effizienz, Leistungsdichte und Funktionalität der Konvertersysteme bei vergleichbaren Kosten des Gesamtsystems.

Abstract

As a result of the ongoing improvements in the area of power electronics, the penetration of power electronic converter systems into numerous traditional and modern applications has continuously been increasing. A prominent example is the developments in today's electric power systems towards smart grids featuring high shares of new renewable energy sources such as solar and wind. Another example is the growing utilization of electric propulsion in automobiles and aircraft. Both examples are driven by the increased environmental awareness and the demand for higher functionality of the modern society. Based on the observed trends in state-of-the-art applications, it can be expected that the need for enhanced power electronic converter systems with a higher efficiency, reliability and functionality at concurrently lower costs, weight, volume and development time will further increase in the near future.

The analysis of the relevant literature shows that the dimensioning and optimization of converter systems is often carried out with a limited scope and focusing on only one or a few performance criteria. This is often a consequence of a missing systematic approach which enables a comprehensive consideration of the inherent trade-offs between different performance measures (e.g. converter volume vs. losses). Furthermore, the employment of such an approach is often prohibited due to incomplete modeling frameworks to quantitatively assess the respective performance measures. Notably, suitable cost models to assess the costs of the typical components in converter systems are rare to find in literature. As a result of these deficits, it is unlikely that the optimal solution (topology, modulation scheme and component dimensioning) for a given application can be found by such limited approaches.

The main focus of this thesis is thus set on the derivation of a suitable methodology which enables a systematic multi-objective optimization and comprehensive comparison of power electronic converter systems regarding achievable efficiency, volume, weight and costs. Thereby, a modeling framework is established which allows for the assessment of typical converter components such as semiconductors, inductors, capacitors, cooling systems and printed circuit boards regarding the selected performance measures. In addition to the component models, further models are developed which describe the converter behavior and the resulting current and voltage waveforms in the system depending on the employed modulation scheme and operating point. The models and their parameters are derived based on analytical calculations, simula-

tions, measurements and empirical research. The primary aim of the proposed design method is the precise prediction of the converter characteristics which enables an effective and efficient system optimization with fewer hardware prototype iterations and a shorter time to market.

The proposed methodology is applied to the multi-objective optimization and comparison of various DC/DC and DC/AC converter systems under consideration of the latest available SiC semiconductors. The case studies on the one hand highlight the capability of the employed methodology to handle complex optimization problems and to find the corresponding solutions with a comparably low computational effort and time need. Experimental measurements on an implemented DC/DC hardware prototype on the other hand verify the high accuracy of the employed models. The results of the two case studies reveal that the employment of SiC semiconductors in the considered applications is attractive despite the higher costs of SiC semiconductors in contrast to conventional Si components. In both examples, the superior performance of SiC enables considerable improvements regarding efficiency, power density and functionality of the converter systems at comparable overall system costs.

1 Introduction

THE start of the Industrial Revolution in the late 18. century marked the beginning of an ongoing period in which technological advancements and innovations have become the main driver of increased wealth and economical growth. In this context, the utilization of electrical power by means of power electronic converter systems has made major contributions towards a higher productivity and prosperity. Power electronics was a prerequisite for the automation in industry, for modern wireless communication, the world wide web and the enabler of electromobility. At present time, power electronics represents the key technology to overcome some of the most urgent challenges of modern society, i.e. the rapidly growing energy demand, the scarcity of fossil fuels and the global warming associated with the predominant utilization of fossil fuels in the energy supply. One of the most promising options to combat these challenges is the replacement of conventional fossil-fueled technologies with renewable energy sources such as photovoltaics (PV), wind power and wave power. Here, power electronics is the enabling technology which allows the large-scale integration into the grid and the efficient distribution to the loads.

The increasing utilization of electrical equipment and appliances in most areas of modern society has been accompanied by significant improvements of the corresponding power electronic converter systems. In fact, further and steady improvements, i.e. a higher performance of the power electronic converter systems are mandatory to guarantee a continuous growth of the productivity and wealth, to open up new fields of application and to overcome the challenge of clean energy generation.

In this chapter, different performance measures of power electronic converter systems are defined and shown to be continuously improving

in commercial systems. Furthermore, it is discussed by what means performance can be improved. Eventually, system optimization and in particular multi-objective optimization-based virtual prototyping considering the power conversion efficiency, the volume and the costs is proposed as a powerful means to boost the performance of today's power electronic converter systems.

1.1 Performance Trends in Power Electronics

The performance of a power electronic converter system can be defined using a range of converter performance measures. Typical technical quantitative measures are the losses of the power conversion, the converter weight, the volume, the component costs and the failure rate as depicted in **Fig. 1.1(a)**. These measures are largely determined by the implementation of the converter system, i.e. the selection of the topology, modulation scheme, components and the converter layout according to a set of given specifications (e.g. required output power, operating conditions, etc.). For the remainder of this thesis, these measures are referred to as *primary performance measures*. In contrast, a more generalized definition of the performance of a power electronic converter system may, in addition to the primary converter performance, also include further measures which can also be of non-technical and/or qualitative nature and furthermore not only be determined by the converter's implementation. Examples of such *general converter measures* are given in **Fig. 1.1(b)**. Measures such as the converter functionality or the compatibility (with other systems) are rather qualitative measures and are determined by features such as galvanic isolation, bidirectional power flow or the offered grid services. Factors other than the converter's implementation which have an impact on the general converter performance measure are the labor costs (having an impact on the development, manufacturing and maintenance costs) or the manufacturing processes in the factory (influencing the environmental impact and again the manufacturing costs). The analysis of the historical evolution of commercial power electronic converter systems shows a general trend towards a higher converter performance, i.e. a continuous improvement of both the primary and general performance measures.

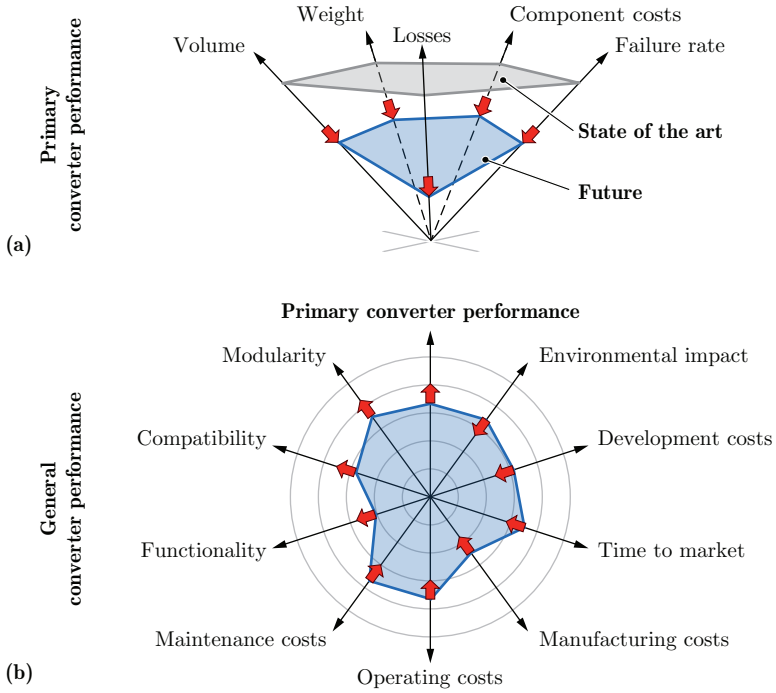

Fig. 1.1: Performance measures and future trends of power electronic converter systems. **(a)** Primary converter performance defined by technical quantitative measures which are largely determined by the implementation of the converter, i.e. the selection of the topology, modulation scheme, components and the converter layout. **(b)** General converter performance which in addition to the primary converter performance also includes non-technical, qualitative performance measures which are not only determined by the implementation of the converter but also other factors (e.g. labor costs as part of the manufacturing costs). A general trend towards a higher performance, i.e. a continuous improvement of all performance measures as indicated by red arrows can be observed in commercial systems (cf. **Fig. 1.2**). This thesis mainly deals with the improvement of the primary performance of power electronic converter systems.

1.1.1 Examples

The following examples depict performance trends for commercial telecom AC/DC power supply modules, PV inverters and converters in automotive applications based on market surveys and conference contributions of the respective industries.

- In **Fig. 1.2(a)**, the continuous reduction of the relative volume, i.e. the increase of the power density is shown for 2-stage telecom AC/DC power supply modules comprising a power factor correction (PFC) rectifier and a DC/DC converter stage [1–4]. The trend line based on the shown real commercial systems indicates an increase of the power density by a factor of 10 every 20 year. The reduction in volume has mainly been achieved by changing from natural convection to forced air cooling and by increasing the switching frequency [8]. Assuming forced air cooling, the theoretical power density barrier [3] can only be overcome with new semiconductor technologies allowing for higher junction temperatures and/or lower losses.
- **Fig. 1.2(b)** shows the historical loss reduction, i.e. the increase of the efficiency of PV inverter systems with a rated power of 1-10 kW. Such systems are predominantly used in residential applications. The data representing commercial systems proves a loss reduction by a factor of 2 every 10 years. A market survey on the losses of state-of-the-art systems reveals that the projection of the studies in 2006 [5, 6] were accurate.
- The reduction of the relative price of PV inverter systems with a rated power of 1-10 kW can be seen in **Fig. 1.2(c)**. In addition, the underlaying study [5] emphasizes the importance of economy of scale to reduce the costs which eventually translates into lower system prices. A factor of 2 in price reduction every 10 years is projected by the study. A market survey on commercial systems in 2015 proof the study to be accurate, i.e. system costs of approximately 0.2 €/W in contrast to 0.4 €/W in 2005 were found.
- In **Fig. 1.2(d)**, The projected evolution of the costs of electrical drivetrain systems in automotive applications [7] shows that the cost reduction is driven by different factors. On the one hand, economy of scale allows for continuously decreasing production costs at a rate of approximately 3 % per year. On the other hand,

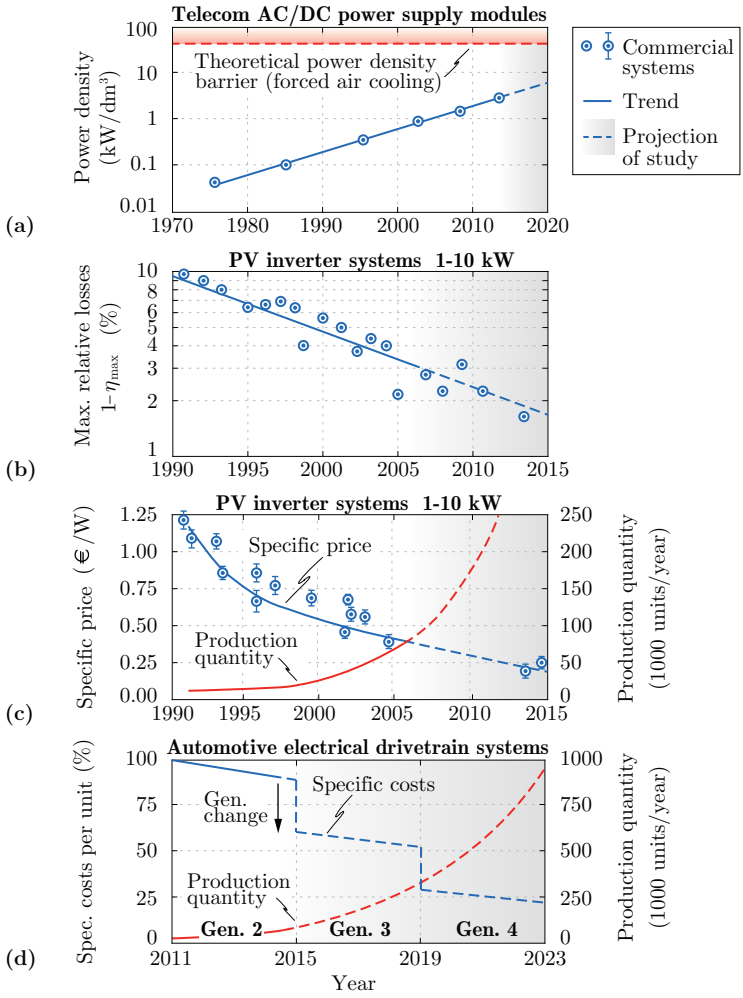

Fig. 1.2: Performance trends of commercial power electronic converter systems. **(a)** Increase of the power density of 2-stage telecom AC/DC PFC rectifier modules [1–4] and theoretical barrier as calculated in [3]. **(b)**, **(c)** Loss and price reduction of PV inverter systems as shown in [5, 6]. The systems for the projected years were added based on a market survey. **(d)** Cost reduction enabled by economy of scale and generation changes (modularization and standardization of the converters) for automotive systems as projected in [7].

major optimizations of the system (here modularization and integration) lead to generation changes. A generation change is typically accompanied by a significant and stepwise reduction of the costs within a short time. On overall, a cost reduction of 10 % per year is expected.

- The evolution of PV inverter systems serves as an example for the continuously increasing functionality (general performance measure) of power electronic converter systems. Due to the fast growing penetration of distributed renewable energy sources on all levels of the distribution grid, PV inverters are required to offer more and more grid services. Modern PV inverters must feature low-voltage ride-through (LVRT) capabilities, must support the grid voltage control with reactive power provision and facilitate the frequency stability by means of dynamic output power control [9–11].

The above examples emphasize the reality of the trend towards higher system performances in power electronics. Whereas the *driver* of these performance improvements is the obvious urge towards a higher productivity and economical growth, it remains to be discussed what the *enablers* of the performance trends are.

1.1.2 Enablers of Performance Trends

Consider the simplified conceptual view on the research and development activities in power electronics depicted in **Fig. 1.3**. The shown activities can be grouped and summarized into two distinct vectors

Innovation Vector

The innovation vector summarizes the activities aiming at the search and introduction of *new* building blocks for the converter design. In this thesis, building blocks denote the converter topologies, the control schemes and the converter components. Examples of innovations are:

- *Novel power components*, i.e. semiconductors, magnetics, capacitors, cooling systems and printed circuit boards (PCB). Possible novelties include:
  - Novel types, e.g. the insulated-gate bipolar transistor (IGBT) in 1979 [12],

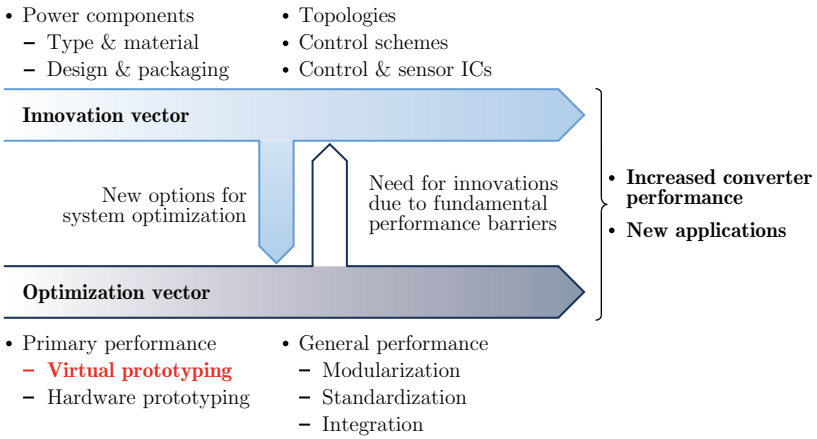

Fig. 1.3: Main vectors of research and development activities in power electronics aiming at higher converter performances and new applications. On the one hand, innovation deals with the search for *novel* building blocks for the converter design. On the other hand, optimization attempts to optimize the converter performance based on *given* building blocks. The main topic of this thesis is the research and application of advanced concepts in the field of virtual prototyping.

  - Novel materials, e.g. wide bandgap (WBG) materials for semiconductors or new core materials,
  - Novel designs and shapes, e.g. flexible PCBs or core shapes, or
  - Novel packaging, e.g. discrete semiconductor packages with Kelvin source [13];

- *Novel topologies*, e.g. the H5 topology for PV inverters [14] or the modular multi-level converter (MMC) [15];
- *Novel control schemes*, e.g. minimum rms current control for dual active bridge (DAB) topologies [16, 17]; or
- *Novel control and sensor ICs*, e.g. the introduction of microcontrollers enabling digital control in the 1970s.

Optimization Vector

Contrary to the innovation vector, activities summarized by the optimization vector are restricted to the *given* building blocks and attempt to optimize the primary and general converter performance (cf. **Fig. 1.1**) solely based on the available topologies, control schemes and components. Some of the possible strategies which can be pursued are:

- *Virtual prototyping*: the employment of mathematical models and/or multi-physics simulations to digitally synthesize converter systems can be summarized as virtual prototyping [8,18,19]. Virtual prototyping tools can be used to investigate and optimize the converter performance as a function of the available building blocks.
- *Hardware prototyping*: the investigation and optimization of the performance of a particular converter system can also be carried out by means of experimental measurements and (iterative) hardware prototyping [8,19].
- *Modularization* focuses on increasing the reusability of subsystems based on defined interfaces. This strategy increases the flexibility in the system design process, reduces the time to market and may lower the maintenance effort [20].
- *Standardization* is an important enabler of system modularization by means of providing standardized interfaces between the subsystems [20]. Furthermore, standardization may also include the aim of employing the same components, topologies and control schemes in as many systems or subsystems as possible [21]. This strategy can help to reduce the development costs, the complexity of the manufacturing as well as the involved logistics.
- *Integration* is the replacement of a number of building blocks with a single building block offering the same functionality. Advantages may include higher compactness, reduced development costs and a lower manufacturing complexity [22,23]. Examples are the use of ICs rather than discrete logics or the employment of power semiconductor modules replacing discrete semiconductors and their interconnecting wiring.

Virtual and hardware prototyping is typically employed to study and optimize the primary performance measures (i.e. the losses, the weight

or the component costs) of the converter system. Contrarily, the common feature of modularization, standardization and integration is the predominant focus on improving general performance measures such as increased flexibility, lower complexity and a shorter time to market. The common approach to achieve this is by restricting the available building blocks, i.e. by narrowing down the choice of the components, topologies and control schemes.

Interaction between Innovation and Optimization

The above discussed research and development activities have in common that they eventually aim at increasing the performance of a power electronic converter system and at enabling new fields of application. Both innovation and optimization interact and stimulate each other: on the one hand, innovation, i.e. novel topologies, control schemes and components always offers new options and opportunities for optimization. On the other hand, systematic optimization can be used to identify the absolute performance trade-offs and performance barriers (cf. **Fig. 1.2**) of the available technologies and thus indicates where innovation is mandatory and the most remunerative.

1.2 Multi-Objective Optimization

This thesis deals with the investigation and application of new concepts and methods in the field of virtual prototyping for power electronic converter systems. An advanced multi-objective optimization (MOO) approach based on detailed mathematical multi-physics models of the system and underlaying converter components is proposed. The optimization objectives are the power conversion efficiency, the converter volume and the component costs. The ultimate goal of the approach is the determination of the Pareto fronts, i.e. the absolute performance trade-off limits for a given set of converter building blocks (topologies, control schemes and components).

This section first revises the fundamental principles of MOO. In a subsequent step, it is discussed how MOO can be incorporated into virtual prototyping of power electronic converter systems. A historical review of the topic as well as a discussion of state-of-the-art contributions which can be found in the relevant literature are presented in the

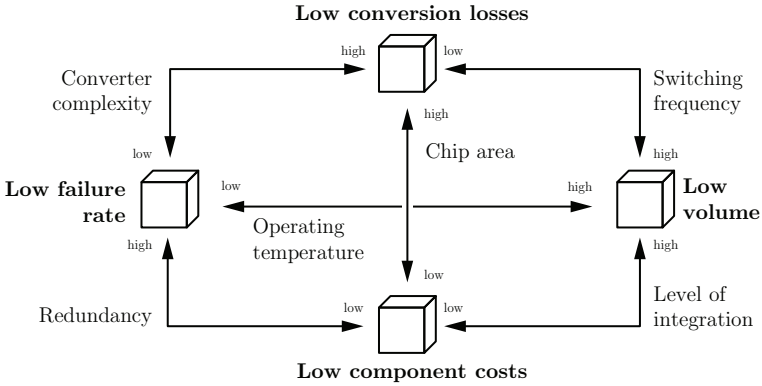

Fig. 1.4: Fundamental performance trade-offs in power electronic converter systems. The effects of the manipulating variables are shown in a simplified form. Exemplary, increasing the power semiconductor switching frequency may not only increase the conversion losses (here the switching losses) while decreasing the volumes of the passive components but also reduce the corresponding costs of the passives.

third section. Finally, the requirement for quantitative cost considerations is derived.

1.2.1 Fundamentals

The basic concept of optimization is the search for optimal solutions amongst a set of alternatives with respect to defined performance measures. Regarding the optimization of power electronic converter systems, a fundamental observation is the fact that typical primary performance measures (but also general performance measures) are coupled, i.e. inherent trade-offs complicate the concurrent improvement of multiple or all performance measures. Examples are given in **Fig. 1.4**. Consequently, single-objective optimizations should be avoided as the aggressive improvement of a particular performance measure will usually result in poor performance regarding other performance measures (e.g. [24]).

Mathematically, a constrained m-objective MOO problem can be stated as

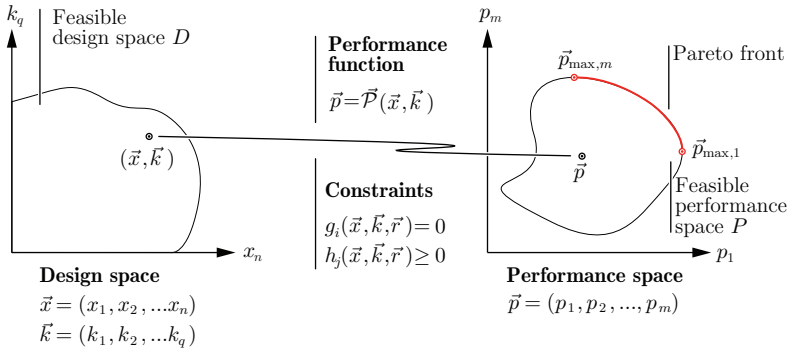

Fig. 1.5: Fundamentals of constrained MOO. The vector-valued performance function $\vec{\mathcal{P}}$ maps the constrained set D of design vectors $(\vec{x},\vec{k})$ into the set P of feasible performance vectors $\vec{p}$ in the multi-dimensional performance space. MOO aims at identifying the Pareto front, i.e. the set of vectors $\vec{p}$ representing the best possible compromise regarding the performance measures p_i. In contrast, single-objective optimization based on a scalar performance function would only identify a single vector to be optimal (here either $\vec{p}_{\max,1}$ or $\vec{p}_{\max,m}$).

$$\begin{aligned} \max\ \vec{\mathcal{P}}(\vec{x},\vec{k}) = \ \max\ & \left(\mathcal{P}_1(\vec{x},\vec{k}),\mathcal{P}_2(\vec{x},\vec{k}),...\mathcal{P}_m(\vec{x},\vec{k})\right), \\ \text{such that}\quad & g_i(\vec{x},\vec{k},\vec{r})=0, \quad i=1,...s\ , \\ & h_j(\vec{x},\vec{k},\vec{r})\geq 0, \quad j=1,...t\ . \end{aligned} \tag{1.1}$$

Following the relevant literature (e.g. [25]), $(\vec{x},\vec{k})$ with $\vec{x}=(x_1,x_2,...x_n)$ and $\vec{k}=(k_1,k_2,...k_q)$ denotes a vector of design variables and constants in the $n\times q$-dimensional design space $\mathbb{R}^n\times\mathbb{R}^q$. The vector-valued performance function (alternatively called objective function) $\vec{\mathcal{P}}:\mathbb{R}^n\times\mathbb{R}^q\mapsto\mathbb{R}^m$ assigns each vector $(\vec{x},\vec{k})$ a performance vector $\vec{p}=(p_1,p_2,...p_m)$ in the m-dimensional performance space. The constraints g_i and h_j in conjunction with the set of parameters $\vec{r}=(r_1,r_2,...r_l)$ define the set of feasible design vectors,

$$\begin{aligned} D=\{(\vec{x},\vec{k})|(\vec{x},\vec{k})\in\mathbb{R}^n\times\mathbb{R}^q \\ \wedge\ g_i(\vec{x},\vec{k},\vec{r})=0, \quad i=1,...s \\ \wedge\ h_j(\vec{x},\vec{k},\vec{r})\geq 0, \quad j=1,...t\}\ , \end{aligned} \tag{1.2}$$

which is referred to as the feasible design space D . Thus, the problem (1.1) can be reformulated as

$$\max \ \vec{\mathcal{P}}(\vec{x},\vec{k})\Big|_{(\vec{x},\vec{k})\in D} \ . \tag{1.3}$$

Mapping D into the performance space using the performance function $\vec{\mathcal{P}}$ yields the set of feasible performance vectors,

$$P = \vec{\mathcal{P}}(D) \ , \tag{1.4}$$

which is referred to as the feasible performance space P or image of D. See **Fig. 1.5** for an illustration of the introduced sets and mappings.

The fundamental aim of MOO is the identification of the optimal design vectors $(\vec{x},\vec{k})$ in D and corresponding optimal performance vectors $\vec{p}$ in P. For this purpose, criteria for optimality must be defined. In a non-trivial MOO problem no single vector exists which concurrently maximizes each performance measure, i.e. the performance functions $\mathcal{P}_i$ are conflicting. Therefore, the concept of Pareto optimality is usually employed [25]. A particular design $(\vec{x}^*,\vec{k}^*)$ is said to be Pareto-optimal if there is no other design for which all performance measures can simultaneously be improved with respect to $(\vec{x}^*,\vec{k}^*)$. Alternatively, $(\vec{x}^*,\vec{k}^*)$ is Pareto-optimal if the improvement of one or more of the performance measures can only be achieved if a degradation in at least one of the remaining measures is accepted. Mathematically, this can be stated as

$$\begin{aligned}
&(\vec{x}^*,\vec{k}^*) \in D \quad \text{Pareto-optimal} \quad \Longleftrightarrow \\
&\quad \nexists \ (\vec{x},\vec{k}) \in D \ \text{ such that} \\
&\quad p_i = \mathcal{P}_i(\vec{x},\vec{k}) > \mathcal{P}_i(\vec{x}^*,\vec{k}^*) = p_i^* \quad \forall \quad i = 1...m \ .
\end{aligned} \tag{1.5}$$

Searching for the Pareto-optimal performance vectors yields the Pareto front which consists of the vectors $\vec{p}$ representing the best possible compromise with respect to the selected m performance measures p_i. For $m = 2$, the Pareto front has the shape of a boundary curve in the performance space (cf. **Fig. 1.5**). For $m = 3$, the Pareto front can be described by a boundary surface (cf. **Fig. 1.6**) and for $m > 3$ a hypersurface will result. For simplicity reasons, however, for the remainder of this thesis the term Pareto front will be used independent from the number of involved dimensions.

1.2.2 Application to Converter Optimizations

The theoretical concept of optimization and in particular MOO can be applied to the field of virtual prototyping of power electronic converter systems [8, 18]. With reference to the fundamentals of MOO discussed in the previous section, the most general form of MOO-based virtual prototyping is explained in detail below. An illustration of the concept can be found in **Fig. 1.6**.

Design Space

In converter optimization, the range of available building blocks, i.e. the range of different topologies, control schemes (including the switching frequency) and components account for the design variables x_i. Analogously, the design constants k_i represent the material and component characteristics such as the permeability of the core materials, switching loss energies and on-state resistances of semiconductors or fixed parameters of the control schemes. Consequently, each possible combination of building blocks and associated characteristics forming an individual converter design are allocated to a point $(\vec{x}, \vec{k})$ in the design space.

Constraints

Usually, a large number of both implicit and explicit constraints apply to the selection of the design variables. On the one hand, every topology consists of a fixed number of components of specified kinds (inductors, power semiconductors, etc.) which translates into implicit constraints on the permissible design variable combinations. On the other hand, in most cases the consideration of the entire set of permissible combinations of building blocks is not desirable and is thus explicitly constrained. E.g., the combination of litz wire with laminated grain-oriented electrical steel (GOES) is usually not practically meaningful in the inductor design as expensive litz wire can only be justified for high-frequency operation where GOES performs poorly. Further constraints arise e.g. from (user-defined) maximum permissible junction temperatures of the semiconductors or maximum permissible flux densities in the magnetics. Many constraints depend on the converter specifications such as the operating points (e.g. voltages, power level, ambient temperature). These converter specifications can be described with the parameters $\vec{r}$. Finally, the range of applicable constraints can be cap-

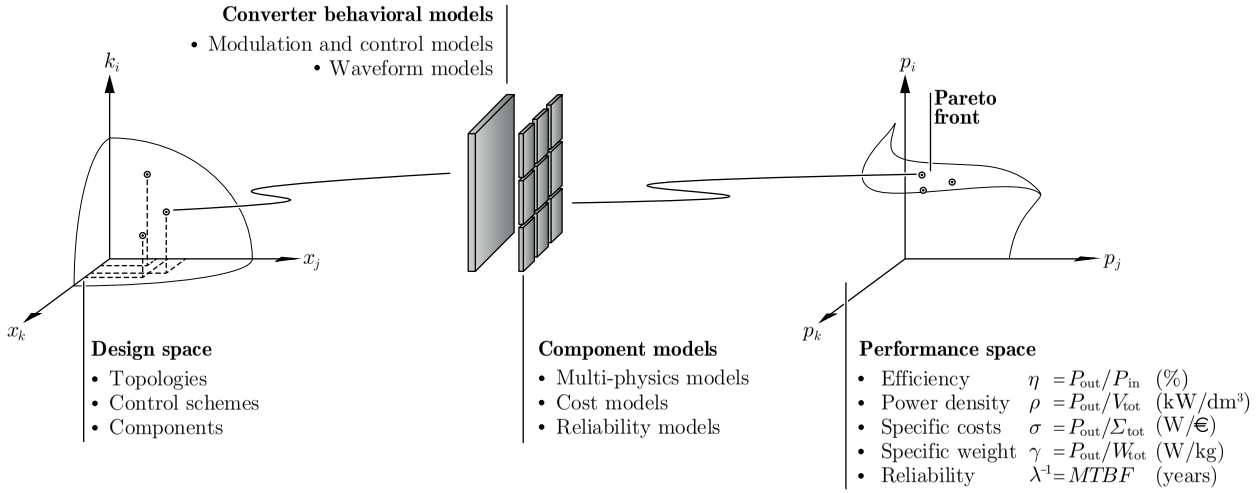

Fig. 1.6: Conceptual visualization of virtual prototyping of power electronic converter systems based on MOO. In a first step, the design space representing the possible combinations of converter building blocks is defined. In a second step, the multi-dimensional design space is mapped into the multi-dimensional performance space, i.e. using mathematical models of the converter behavior and the components, the performance of each of the converter designs in the design space is calculated. Considering only the Pareto-optimal systems in the performance space yields the Pareto front. The designs making up the Pareto front may then serve as candidate systems for a hardware prototype.

tured by means of formulating constraint equalities $g_i(\vec{x}, \vec{k}, \vec{r}) = 0$ and inequalities $h_j(\vec{x}, \vec{k}, \vec{r}) \geq 0$. The remaining combinations of building blocks that are both of interest to the designer and meet all requirements form the feasible design space D.

Performance Function

In MOO-based converter design, the performance space is spanned by performance measures p_i such as the power conversion efficiency η, the power density ρ, the (specific) component costs σ, the (specific) weight γ and the reliability λ^{-1}. In order to determine the performance of each of the feasible system designs in D, mathematical models must be employed which describe the system behavior and waveforms as a function of the modulation scheme and operating point and determine the performance of each component, i.e. the losses, volume, weight, costs and failure probability. This procedure can be interpreted as the mapping of the designs in the feasible design space D into the feasible performance space P. Thus, in analogy to the fundamentals of MOO, the employed system and component models correspond to the performance function $\vec{\mathcal{P}}$.

Pareto Front

As mentioned above, MOO in virtual prototyping aims at finding the Pareto-optimal converter designs for which the best possible compromise between the selected performance measures can be attained. The identification of the Pareto front enables the study of the converter properties and the performance trade-offs solely focused on the set of optimal designs rather than considering all converter designs. Furthermore, the designs making up the Pareto front obviously represent the most attractive choices to serve as candidate systems for a hardware prototype. Further benefits of the presented MOO-based virtual prototyping approach are discussed in Section 1.3.1.

1.2.3 History and State of the Art

This section presents a short overview of past and state-of-the-art contributions to virtual prototyping. Note that in this work the methodology of virtual prototyping is defined as the computation and optimization of the primary performance (i.e. the efficiency, weight or the

volume) of power electronic converter systems based on computer-aided design (CAD) tools such as mathematical models and/or multi-physics simulations. The CAD tools are mainly used to design and optimize the converter components. Algorithms which draw and optimize the 3D layout of the converter may be included but are not considered as a necessary part.

Early References

First references to systematic virtual prototyping of power electronic converter systems can be dated back to the mid 1970s. The formulation of a power electronics design task as a mathematical optimization problem is first shown in [26] and subsequently applied to the weight optimization of a buck converter [18, 27, 28]. In [29], the same approach was employed to weight-optimize an isolated half-bridge DC/DC converter. In addition to [18, 27, 28], the analysis in [29] was repeated for several switching frequencies revealing the fundamental trade-off between weight and efficiency. These early pioneering publications discovered and stated the potential of a systematic mathematical treatment and optimization of the converter design procedure in contrast to approaches which are solely based on the designer's experience and subjective judgment. Not only does virtual prototyping result in designs closer to the real optimum but also does it allow to reduce the development costs and the number of hardware prototyping iterations. The major challenge at that time was found to be the high number of design variables, the strong non-linearities of the model functions and the number of constraints which are inherent to any converter optimization problem. Closed-form solutions as presented in [26] can thus only be found for simple cases and numerical means were usually employed instead. As a consequence, high emphasis was put on the investigation of suitable search strategies which minimize the – at that time – expensive computational effort. [18, 27–29] employ non-linear programming techniques. Three main limitations of the proposed virtual prototyping framework were identified in [18, 30]: i) the convergence of the search algorithm and the final solution strongly depend on the provided initial values and the scaling of the variables; ii) only continuous design variables can be processed which frequently results in unfeasible solutions (e.g. unavailable core size); iii) the lack of accurate models (e.g. models that take into account the HF effects in the magnetics) as well as the lack of comprehensive sets of model constants (e.g. operating

point-dependent switching loss energies) may yield optimization results of dubious value.

1990s and 2000s

In later years, i.e. during the 1990s, the major work published in literature focused on the optimization of specific components and subsystems rather than entire topologies and systems. This reorientation was partly triggered by the emerging and increasingly powerful commercial simulation tools for fluid dynamics, thermodynamics and magnetics problems as well as for the simulation of electrical circuits. [31] describes a simulation-based optimization of heat sinks. [32] and [33] both present a CAD tool based on finite element methods (FEM) for automated design of magnetic components. Further simulation-based optimization tools are proposed in [34] and [35] for the optimization of a gate driver circuit for lowest switching losses and for the power semiconductor package design. Contrary to the aforementioned contributions, purely analytical problem descriptions were used in [36] and [37] for the minimization of the loop inductances in electrical circuits and the minimization of the instantaneous value of the active filter rating of hybrid filter systems, respectively.

In the early 2000s, virtual prototyping of entire converter systems regained attention in literature. Purely mathematical problem descriptions and optimizations rather than simulations were again employed in [38–40]. The mathematical problem formulation was supported by the growing available computational power which allowed for the analysis of more complex systems. A combined PFC and associated EMI filter design was presented in [39]. The introduction of genetic search algorithms (GA) in the optimization procedure by [41] marked a major improvement. In contrast to previously used continuous search algorithms, GAs could fully capture the discrete nature of converter design and perform optimizations taking into account databases of feasible and commercially available components. In [41], a buck converter in conjunction with an analog control circuit is optimized using GAs and mathematical formulations whereas [42,43] optimize the PFC converter of [39] regarding component costs using this new method. Optimization approaches based on a direct search method, i.e. a systematic variation of the design variables instead of heuristic search methods are proposed in [44] and [45]. There, partly simulation-supported tools are used to optimize converter systems with respect to efficiency [44] or power den-

sity [45].

State of the Art

Until the beginning of the 2010s, publications on virtual prototyping in power electronics such as [18, 26–45] were exclusively dealing with single-objective design and optimization problems. The major research effort was spent on the search for efficient optimization algorithms due to the limited available computational power and the high complexity of the involved problems.

Whereas the concurrent optimization of multiple objectives (or performance measures) using MOO-based approaches had already been demonstrated in other areas such as the design of liquid-cooled semiconductor modules [46], aeronautics and space applications [47, 48] and analog circuit design [49], [8, 19, 50] were the first to propose MOO for virtual prototyping of power electronic converter systems. [8] discusses the fundamental limitations of single-objective optimization and proposes a virtual prototyping scheme based on systematic mathematical modeling and MOO as similarly presented in Section 1.2.2. The converter losses, volume and costs are declared to be the most important performance measures which should concurrently be considered in future research. Furthermore, the proposed approach is considered to be a valuable tool to support roadmapping initiatives. It allows to determine the best attainable design trade-offs for the available technology base and to identify the need for disruptive technologies at an early stage to overcome fundamental performance barriers. Although [50] and other publications such as [51–53] present Pareto fronts showing the trade-offs between efficiency and power density (η-ρ Pareto front) of PFC and PV inverters, no real MOO is employed as the Pareto fronts are obtained by means of efficiency- or power density-maximizations at varying switching frequencies. A wide range of virtual prototyping examples employing true MOO can be found in recent literature. In [54–57], η-ρ MOO is employed. The use of η-γ MOO (with γ being the specific weight) proves to be beneficial mainly in airborne and space applications [58–61]. [62–65] perform η-σ (with σ being the specific costs) for PV, solid state transformer (SST) and inductive power transfer (IPT) applications. Finally, [66] demonstrates an η-ρ-σ MOO, [67] shows an η-σ-λ^{-1} MOO with λ^{-1} representing the mean time between failures and [68] performs an η-ρ-λ^{-1} MOO.

The state of the art of MOO-based virtual prototyping of power

electronic converter systems can be summarized by the following observations:

- *Performance measures:* the large majority of contributions which employ MOO consider two performance measures. [66–68] represent the only exceptions found in the literature considering three objectives. The most popular performance measure was found to be the converter efficiency which is considered in all analyzed contributions [54–68]. The second performance measure is usually either the power density [54–57] or the specific weight [58–61]. Cost considerations are becoming more prominent recently. Examples are shown in [62–67] where [63,65] employ the cost models presented in this thesis.
- *Search methods:* apart from [54,60,64,66–68] using GAs or [58] using particle swarm optimization, an increasing number of state-of-the-art contributions employ direct search methods, i.e. methods which do not rely on metaheuristics but systematically enumerate all possible design variables for the search of the Pareto front.
- *Modeling detail:* although the detail and complexity of the underlaying models has generally greatly improved since the beginnings of virtual prototyping in the mid 1970s, significant differences in the modeling detail can be observed among state-of-the-art contributions. Whereas the temperature-dependence of the semiconductor losses are only neglected in [55, 59, 61, 67], the use of (often incomplete) data sheet values for the switching loss energies which may largely differ depending on the application and layout can frequently be found (e.g. [54, 58, 60, 64, 66–68]). A major modeling challenge represent the magnetic components and especially the core losses which are mostly calculated based on data sheet values neglecting important dependencies like the core temperature or DC flux biases ([54, 58–62, 64, 66–68]). Furthermore, details on the thermal models for the magnetics or the cooling system are often missing (e.g. [55, 58, 62–65, 67, 68]) or simple models without experimental verification are employed [54,60,66]. Finally, the publications that employ cost models often miss to state the numerical values of the model parameters and their origin [62, 64, 66, 67].
- *Sensitivity analysis:* most contributions mainly focus on the presentation of the Pareto front, i.e. the optimal solutions. On the

other hand, sensitivity analysis, i.e. the analysis of the impact of modeling errors on the Pareto front or the systematic study of the impact of parameter variations (e.g. the converter specifications or the statistics of the operating points/mission profile) are rarely performed yet. Some of the few exceptions are [50, 69, 70].

1.2.4 Necessity of Cost Considerations

As seen in the previous section, the majority of literature dealing with virtual prototyping of converter systems does not implement cost models in the optimization. However, numerous practical reasons render inevitable the consideration of costs. The most compelling reason seems the fact that cost is by far the most important performance objective and thus the main driver of innovation and optimization in most applications of power electronics. Prominent industries facing a high cost pressure are PV, IT and telecom, automotive and consumer electronics [2, 5–7, 10, 63, 71–74]. Consequently, the exclusive consideration of the converter losses, the volume and weight in MOO is thus mostly insufficient. This limited approach is likely to result in impractical systems as many of the fundamental design trade-offs of **Fig. 1.4** become ineffective. The following examples demonstrate that the concurrent reduction of the losses, volume and weight is technically often feasible, however, usually only at higher costs.

Consider the fictitious design example depicted in **Fig. 1.7**. In **Fig. 1.7(a)**, a state-of-the-art 2-level 6-switch AC/DC inverter based on Si IGBT technology for low-voltage drive applications [75] is shown. **Fig. 1.7(b)** shows the same system employing advanced SiC MOSFETs. The significantly lower switching losses of SiC allow to concurrently reduce the converter losses and the volume of the passives and the cooling system by means of a moderate increase of the switching frequency (cf. **Fig. 1.7(c)**). A MOO with respect to the losses and volumes only would hence suggest using SiC for obvious reasons. However, in reality such a system has low chances to be built due to the higher overall system costs in this example (3-4 times higher costs of SiC). Whether a more pronounced increase of the switching frequency could compensate the higher semiconductor costs can only be assessed with quantitative component cost models. Further examples demonstrating the need of cost considerations in MOO are given below.

- The losses, volume and weight of DC or 50 Hz magnetic compo-

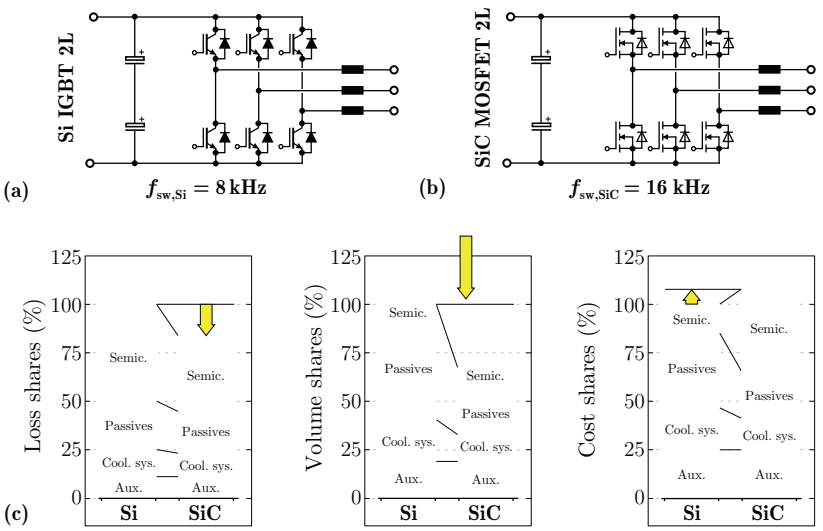

Fig. 1.7: Fictitious example illustrating the necessity of cost considerations in MOO. **(a)** State-of-the-art Si IGBT AC/DC inverter system for low-voltage drive applications [75]. **(b)** Same system based on advanced SiC MOSFETs. **(c)** The low switching losses of SiC allow to concurrently reduce the converter losses and volume by means of a higher switching frequency. Despite obvious advantages regarding losses and volume in this example, the shift from Si to SiC would have only low chances in reality due to the higher overall system costs (3-4 times higher costs of SiC). Such effects can only be evaluated with quantitative cost models of the components.

nents can often concurrently be reduced using high-performance nanocrystalline core materials. Analogously, the volume and losses of HF inductors can be reduced employing litz wires with a lower strand diameter. However, both options are expensive and thus likely to increase the component costs.

- Multi-layer PCBs facilitate more compact auxiliaries and short power traces resulting in lower conduction losses. Multi-layer PCBs are, however, considerably more expensive than two-sided PCBs.
- Other optimization strategies rather than virtual prototyping, e.g. integration and modularization (cf. **Fig. 1.3**), usually aim at

improving the general converter performance measures such as lowering the development and manufacturing costs. Here, virtual prototyping using cost models is imperative to assess the possibly adverse impact on the converter component costs (e.g. the use of power modules instead of discretes may lower the development and manufacturing costs but typically increases the component costs).

Finally, it is obvious that the consideration of the reliability – apart from the efficiency, volume and the costs – would further boost the significance and usefulness of the results of MOO-based virtual prototyping. A prerequisite of such analysis is the availability of comprehensive and resilient reliability data for the considered components. Obtaining such data, however, is deemed impractical for academia as i) such data often does not exist, ii) conducting large-scale reliability tests is beyond the means of most research groups and iii) the access to such data compiled by manufacturers is largely restricted to buying customers. Furthermore, relying on the reliability prediction models published in the Military Handbook 217F Notice 2 (MIL-HDBK-217F) [76] as frequently proposed (e.g. [67]) is not recommended. On the one hand, important components such as MOSFETs are not described and the generalized models based on reliability data of components from the 1980s might not apply to modern and more specialized components. On the other hand, the application-specific stresses on the components (which have a crucial impact on the reliability) cannot directly be considered.

1.3 Scientific Contributions

This thesis proposes a novel advanced η-ρ-σ virtual prototyping routine for power electronic converter systems which is considerably more comprehensive, detailed and accurate than previous contributions in this field. The usefulness of the virtual prototyping routine is furthermore demonstrated by means of two case studies employing the routine. A more detailed discussion of the main contributions of this thesis are given below.

- This thesis proposes an advanced virtual prototyping routine for MOO of power electronic converter systems regarding the efficiency, volume and the costs. An intelligent direct search method

in conjunction with an efficient software implementation is employed to identify the η-ρ-σ Pareto surface.

- The original MOO approach of **Fig. 1.6** is extended by an additional optimization step as illustrated in **Fig. 1.8**. The resulting Pareto front usually comprises a large number of system designs which all represent a compromise between the chosen performance measures. In order to facilitate a systematic selection of a single candidate system, it is proposed to assign each system of the Pareto front a single (i.e. 1D) key figure as a function of its performance, $\mathcal{C} : (\eta, \rho, \sigma) \mapsto \mathbb{R}$. The corresponding mission cost function $\mathcal{C}$ may represent the (arbitrary) preferences of the design engineer. The candidate design is then found in a systematic and straightforward manner by selecting the system which achieves the best key figure value as shown in **Fig. 1.8**. The advantage of this multi-objective two-step optimization approach with an *a posteriori* selection of the candidate system in contrast to a conventional single-objective approach (which directly results in a single candidate system) is twofold: on the one hand, the Pareto-front is obtained which provides valuable insight of the design trade-offs. On the other hand, the design engineer's preferences of how to select the candidate system, i.e. the mission cost function $\mathcal{C}$ can easily be modified without re-executing the time-consuming optimization step. In this thesis, a mission cost function estimating the life cycle costs (LCC) depending on the efficiency, volume and costs is proposed.
- Detailed and comprehensive system models and multi-physics component models are employed. Accurate experimentally verified model parameters are systematically derived and incorporated into the models. Model simplifications based on the abstraction of components (e.g. cooling system design based on a cooling system performance index [50, 53] or volumes of passives as a function of the stored energy [75]) was avoided in the component modeling.
- The modeling framework is complimented with novel cost models for power semiconductors, cooling systems, magnetic components, capacitors, PCBs and a selection of auxiliary circuits such as gate drivers.
- The proposed virtual prototyping routine is utilized to optimize a bidirectional galvanically isolated 5 kW universal power con-

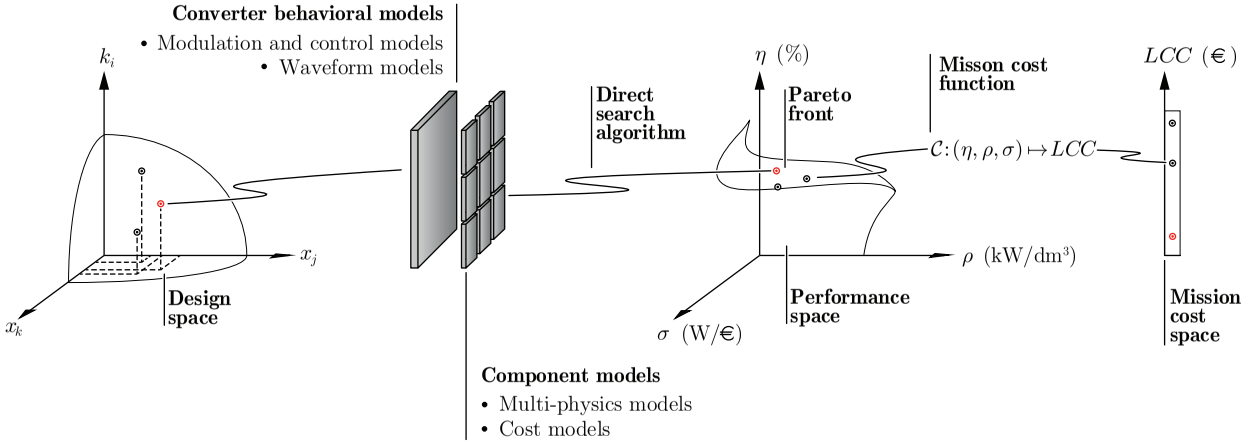

Fig. 1.8: Proposed approach for advanced virtual prototyping of power electronic converter systems based on MOO regarding the efficiency, power density and the specific component costs. A direct search algorithm based on computationally-efficient design routines is employed to identify the η-ρ-σ Pareto front. The system and component modeling framework comprises detailed and experimentally verified multi-physics and cost models. In contrast to existing MOO routines, the proposed routine is extended by an additional optimization step in which an arbitrary mission cost function $\mathcal{C} : (\eta, \rho, \sigma) \mapsto \mathbb{R}$ is used to map the Pareto surface into a 1D mission cost space. This step facilitates the identification of the optimal system based on a single user-defined key figure. In this work, the optimal system on the Pareto surface is determined using life cycle cost evaluations based on the converter efficiency, volume and costs.

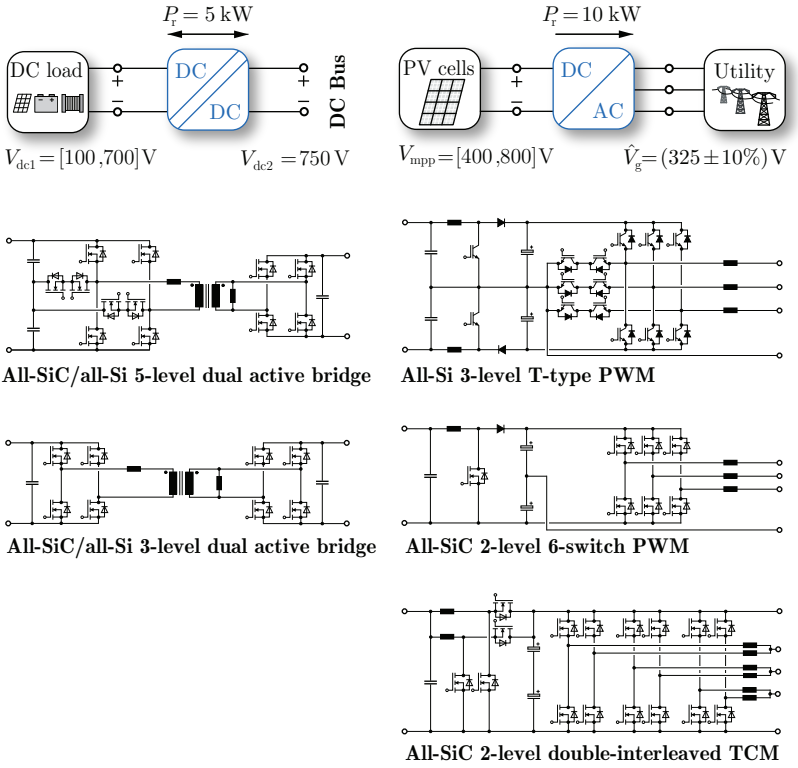

Fig. 1.9: Considered case studies for which the proposed advanced MOO-based virtual prototyping routine is employed. **(a)** Bidirectional galvanically isolated 5 kW universal power conditioner with ultra-wide input voltage range for residential DC-microgrid applications. A conventional 3L dual active bridge (DAB) converter system is compared to a 5L DAB which features a higher control degree of freedom. The analysis includes the investigation of the employment of either SiC MOSFETs or Si IGBTs. **(b)** 10 kW PV inverter system consisting of a DC/DC boost converter input stage, DC/AC inverter stage and EMI filter output stage. A state-of-the-art hard-switched PWM-modulated all-Si 3L T-type converter system is compared to a hard-switched PWM-modulated all-SiC 2-level 6-switch system and a to a soft-switched TCM-modulated all-SiC 2-level double-interleaved system.

ditioner with ultra-wide input voltage range for residential DC-microgrid applications (cf. **Fig. 1.9(a)**). The purpose of this case study is to check whether the use of SiC allows the implementation of a highly functional converter system while still achieving a high efficiency and low volume at competitive costs. Two different topologies are optimized and comprehensively compared. A hardware prototype is built to verify the employed MOO routine.

- The proposed virtual prototyping routine is further utilized to investigate the potential of SiC in PV applications. For this purpose, a state-of-the-art Si IGBT-based system and two SiC MOSFET-based concepts are optimized regarding the efficiency, volume and component costs and compared with respect to the achievable minimum LCC.

Different parts of the presented research in this thesis have already been published in international scientific journals, conference proceedings, tutorials and workshops. The respective list of publications can be found at the end of this chapter.

1.3.1 Opportunities

The opportunities offered by the MOO-based virtual prototyping routine proposed in this thesis are discussed below.

- *Systematically optimized designs*: the proposed MOO-based virtual prototyping routine facilitates the systematic design and the concurrent optimization with respect to the efficiency, volume and the component costs of power electronic converter systems in arbitrary applications. Although not shown in this thesis, the consideration of the converter weight can be added with ease to the existing routine. As a result of the employed direct search method, the global solution to the optimization problem can be identified in a guaranteed and deterministic manner without convergence problems.
- *Performance barriers and novel technologies*: on the one hand, the virtual prototyping routine facilitates the detection of fundamental performance barriers of available technologies. On the other hand, innovative concepts and disruptive technologies such

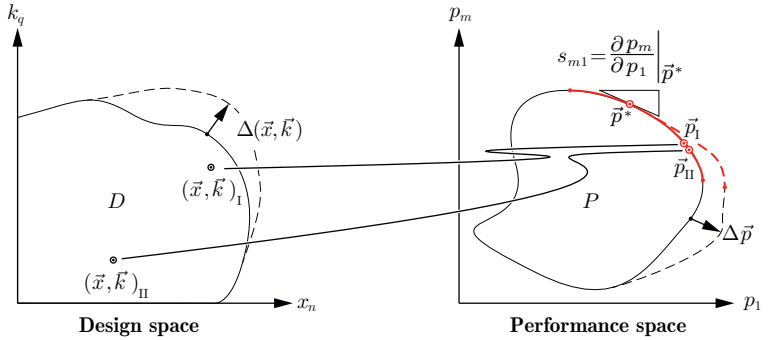

Fig. 1.10: Opportunities of the proposed MOO-based virtual prototyping routine. For clarity reasons, a generalized 2D illustration of the Pareto front is shown. On the one hand, the routine allows to study the impact $\Delta\vec{p}$ on the feasible performance space P caused by an extension (e.g. novel core materials) or restriction (e.g. due to standardization) $\Delta(\vec{x},\vec{k})$ of the feasible design space D. Another option is the investigation of the sensitivity of the Pareto front with respect to modifications in the converter specifications or the operating points. On the other hand, investigations going the opposite direction include the detailed analysis why the designs $(\vec{x},\vec{k})_{\mathrm{I}}$, $(\vec{x},\vec{k})_{\mathrm{II}}$ achieve optimal performances $\vec{p}_{\mathrm{I}}$, $\vec{p}_{\mathrm{II}}$. This step also provides insight into the design space diversity. Finally, the performance trade-offs at different points $\vec{p}^*$ on the Pareto front, i.e. the sensitivities between different performance measures p_i, can be studied.

as novel semiconductor technologies can be comprehensively assessed and on the converter system level and compared to state-of-the-art technologies (cf. **Fig. 1.10**).

- *General performance measures*: apart from the optimization of the selected primary performance measures (efficiency, volume, costs), the proposed virtual prototyping routine may also contribute to an improvement of general measures such as development costs and time to market. Similarly, other system optimization strategies such as modularization, standardization and integration (cf. Section 1.1) mostly also aim at optimizing general performance measures (development costs, time to market, manufacturing costs, maintenance) by means of allowing the use of only a limited number of specified building blocks in the converter design. This is equivalent to a restriction of the design space. The

entailed impact on the primary converter performance measures can be studied by means of the proposed virtual prototyping routine (cf. **Fig. 1.10**).

- *Hardware implementation*: the consideration of abstract component models is largely avoided in the design routines. Therefore, most of the designs in the performance space can be implemented with only little additional design effort.
- *Sensitivity analysis*: from an academic point of view, the routine can provide valuable insight into the trade-offs and sensitivities of converter design. On the one hand, the sensitivity of the Pareto front with respect to parameter variations (e.g. converter specifications, operating points) or model uncertainties can be studied. On the other hand, a systematic analysis of the design variables which are mapped onto the Pareto front provides insight into the design of optimized converters which at best allows to derive simple generalized design rules (cf. **Fig. 1.10**).

1.3.2 Challenges

The design and implementation of a virtual prototyping routine employing MOO represents a challenging interdisciplinary task. The main challenges are listed below.

- *Modeling accuracy*: the significance of the generated data of the proposed routine strongly depends on the level of detail and accuracy of the underlying models. The precise calculation of the waveforms is essential. The waveforms largely determine the component stress and are thus crucial for the dimensioning and performance evaluation of the components. The waveform synthesis becomes more complex if a high number of operating points or a mission profile is taken into account. On the component level, different thermodynamic, fluid dynamic and electromagnetic effects must be considered. Parasitic effects such as thermal coupling or stray capacitances and inductances further complicate the modeling.
- *Parameter accuracy*: the implementation of an accurate modeling framework does not only include the reproduction of all relevant physical aspects and couplings in the models but also the determination of realistic and accurate model parameters. For multi-

physics models (e.g. modeling the core losses or the switching losses) this usually requires extensive measurements and subsequent verification efforts. For the cost models, empirical investigations must be conducted.

- *Complexity of optimization problem*: from a conceptual point of view, the sheer complexity of the problem poses a big challenge regarding the search for the Pareto-optimal solutions. Depending on the number of involved topologies, control schemes and components, the number of independent design variables in the optimization of typical power electronic converter systems can reach the amount of 100. The case studies presented in this thesis feature a complexity of $\mathcal{O}(n^{24})$ and $\mathcal{O}(n^{46})$. As a consequence, finding suitable strategies which divide the overall optimization problem into independent sub-problems is highly important.
- *Software implementation*: due to the complexity of the problem, the software implementation of the routine must be able to cope with the handling and processing of large amounts of data. Therefore, a careful selection of the software architecture and the utilization of computationally-efficient code and suitable concepts for data organization and storage are mandatory. In addition, rigorous debugging and testing of the code is of primary importance in order to avoid unrealistic or flawed optimization results.
- *Analysis of results*: the large amount of data further poses a challenge regarding the analysis and post-processing of the generated data and results. For this reason, powerful analysis and visualization tools are required in order to provide insight and to gain an understanding of the design trade-offs.

1.4 Outline of the Thesis

The main goal of this thesis is the presentation of an advanced virtual prototyping routine based on MOO for the concurrent optimization of the efficiency, power density and the component costs of power electronic converter systems. The thesis is organized as described below.

In Chapter 2, the proposed virtual prototyping routine is presented. The different sub-routines dealing with the dimensioning and optimization both on the system level and the component level are discussed in

detail. This is complemented with information on the practical software implementation.

The multi-physics models involved in the design and optimization routines are presented in Chapter 3. The considered modeling aspects are discussed for all typical component types in power electronic converters, namely the power semiconductors, cooling systems, magnetics, capacitors and the PCB. Furthermore, the sources of the different model parameters are discussed whereby results of various core and switching loss measurement are shown.

Due to the empiric nature and the special importance for this work, the cost modeling is presented separately in Chapter 4. The chapter discusses the challenges of cost modeling and presents a comprehensive set of collected cost data based on which suitable models are derived.

The proposed virtual prototyping routine and the derived models are subsequently applied to a DC/DC converter design example (cf. **Fig. 1.9(a)**) which is presented in Chapter 5. In a first step, the suitable topologies and control schemes are identified which is followed by the selection of the components and materials. The calculated optimization results are discussed in detail and in a last step experimentally verified by means of a hardware prototype.

The second case study is presented in Chapter 6 where the DC/AC PV inverter system of **Fig. 1.9(b)** is analyzed. Different topologies either employing Si or SiC semiconductors are selected and suitable control schemes are identified. By means of the proposed virtual prototyping routine the potential of SiC in PV is investigated in detail.

The thesis concludes with Chapter 7 in which the main contributions and findings of this work are summarized and an outlook on the possibilities regarding future work is given.

1.5 List of Publications

Different parts of the research findings presented in this dissertation and of other research projects carried out in parallel have already been published or will be published in international scientific journals, conference proceedings, tutorials, and workshops. The publications developed in the course of this Ph.D. thesis are listed below.

Journal Papers

- R. M. Burkart, and J. W. Kolar, "Comparative Life Cycle Cost Analysis of Si and SiC PV Converter Systems Based on Advanced η-ρ-σ Multi-Objective Optimization Techniques," *IEEE Trans. PE, accepted for publication.*
- R. M. Burkart, and J. W. Kolar, "Comparative η-ρ-σ Pareto Optimization of Si and SiC Multi-Level Dual Active Bridge Topologies with Wide Input Voltage Range," *IEEE Trans. PE, submitted for review.*
- M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS Condition and ZVS Switching Losses Revisited," *IEEE Trans. PE*, , vol. 31, no. 12, pp. 8063-8067, Dec. 2014.
  DOI: 10.1109/TPEL.2016.2574998
- T. Baumgartner, R. M. Burkart, and J. W. Kolar, "Analysis and Design of a 300-W 500 000-r/min Slotless Self-Bearing Permanent-Magnet Motor," in *IEEE Trans. IE*, vol. 61, no. 8, pp. 4326-4336, Aug. 2014.
  DOI: 10.1109/TIE.2013.2284159

Conference Papers

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2

Virtual Prototyping Routine

This chapter details the implementation of the proposed advanced MOO-based virtual prototyping routine. The fundamental task of the virtual prototyping routine is the mapping of the design space into the performance space and ultimately the identification of the Pareto front, i.e. the Pareto-optimal combinations of the building blocks, i.e. the topologies, control schemes and components, which are available in the design space. Thereby, different constraints and system specifications must be taken into account.

The main challenge of the implementation of the virtual prototyping routine is the minimization of the computation time. Since typical converter optimization problems may feature up to 100 and more design variables, solving the optimization problem can be complex. Therefore, suitable strategies which render the optimization problem tractable must be found and incorporated into the employed optimization scheme which, in this thesis, employs a direct search method. Such strategies include the identification and definition of independent groups of design variables which allow to break the optimization into smaller sub-problems, the intelligent exploitation of physical relationships and the realization of computationally efficient software code.

The outline of this chapter can be summarized as follows: in Section 2.1, the main virtual prototyping routine is derived and discussed in detail. The subordinate design routines for the semiconductors, magnetics and capacitors are presented in Section 2.2. Complementary comments on the practical software implementation are given in Section 2.3. Note that this chapter focuses on the design and optimization routines whereas the required component models are discussed in Chapter 3.

2.1 Main Design Routine

In this section, a suitable main design routine is derived which implements the specifications of the virtual prototyping methodology as stated in Chapter 1. For this purpose, the challenges of solving the general multi-objective converter optimization problem are analyzed first. In a next step, suitable strategies to manage and simplify the problem are introduced. Finally, the main design routine is presented and discussed in detail.

2.1.1 Problem Analysis

The design space includes a varying number of converter building blocks, i.e. topologies, modulation schemes and components. This usually translates into a vast number of design variables such as the switching frequency, the layout and component geometries and different component values and types. A main task of the design routine is the calculation of the resulting system performance of each of the permissible combinations of these design variables, i.e. the mapping of the design space into the performance space. In the real world, the large majority of the design variables have a coupled impact on the performance of the entire system including all of its components. The main coupling effects which are causing this system-wide impact are discussed below.

- *Parasitic electromagnetic coupling*: parasitic electromagnetic coupling effects are a result of undesired electromagnetic stray fields within the converter system. This can equivalently be interpreted as stray capacitances and coupling inductances between the converter components whose values largely depend on the geometry of the converter layout. Ultimately, electromagnetic coupling effects modify the system waveforms and influence the component losses and thus their optimal dimensioning. Note that the electromagnetic fields in a transformer are largely (apart from stray fields, e.g. in IPT applications) a desired and not a parasitic effect as they are required for the power transfer.
- *Parasitic thermal coupling*: thermal coupling between the converter components arises from radiated heat and conducted heat in the interconnecting wiring. Thermal coupling has on the one hand the effect that the mostly temperature-dependent component losses mutually influence each other. On the other hand, the

dimensioning of components can be affected as the temperature is often a critical criterion. The extent of parasitic thermal coupling effects is again mainly a function of the geometry of the converter layout.

- *Direct conducted waveform coupling*: parasitic thermal and electromagnetic coupling effects are mainly a function of the geometry of the converter layout and have a parasitic and mostly *undesired* nature. However, the performance of the components is not only mutually coupled by electromagnetic and thermal effects but also by the conducted waveforms in the interconnecting wiring. The latter have, in contrast, almost exclusively an intended and *desired* nature as the conducted waveforms enable the power transfer. As a consequence, any design variable which modifies the conducted current and voltage waveforms has a system-wide impact.

The following examples illustrate the impact of typical design variables on the conducted waveforms:

- Design variables which are related to the modulation scheme such as the switching frequency have an obvious and intended impact on the conducted waveforms. Clearly, the switching frequency therefore influences the performance of most components in the system.
- Most design variables modify the losses of one or more components. As a consequence, the conducted waveforms in the system are altered as well due to the changed loss-related voltage drop of the component(s). A particularly evident example is the forward voltage drop depending on the diode (being the design variable, e.g. different types of Schottky or PiN diodes) in LV rectifier applications.
- Parasitic stray inductances and capacitances do not only occur between components as a function of the geometry of the converter layout, but also within components as a function of the component geometry. Therefore, a real inductor with specified inductance does not act as an ideal inductor because of the parasitic and geometry-dependent inter-winding capacitance. Such effects also alter the conducted waveforms between the components. Therefore, the corresponding design variables which deter-

mine the component geometry also have a coupled impact on the system performance.

As a consequence of the above analysis, since each design variable has a coupled impact on the performance of the entire or at least a large fraction of the system, the mapping of the design space into the performance space would mean the complete computation and analysis of

$$N_{\text{sys}} = \prod_{j=1}^{N_{\Pi}} N_{\Pi_j} \ , \tag{2.1}$$

different system designs where N_{Π} is the number of design variables and N_{Π_j} the number of discrete options which are analyzed per design variable. In other words, due to the system-wide impact of the design variables Π_j, the mapping of the entire system including all components and regarding all performance measures (efficiency, volume and costs) would have to be repeated for all N_{sys} combinations of variables. Clearly, if the mapping, i.e. the involved models describing the system behavior and components, is not trivial and/or highly computationally efficient, such an optimization approach with an order of complexity of $\mathcal{O}(n^{N_{\Pi}})$ becomes unfeasible with standard means if the number of design variables N_{Π} is high. Therefore, suitable strategies must be found which significantly reduce the complexity and the computational time of the optimization problem.

2.1.2 Approach

Various strategies can be pursued to reduce the complexity and computational time of the optimization problem at hand:

(i) Utilization of efficient software code performing the optimization,

(ii) Employment of intelligent optimization schemes which minimize the mapping of non-Pareto-optimal designs, and

(iii) Simplification of selected coupling effects and division of the optimization problem into independent sub-problems.

Software Implementation

The first strategy of utilizing efficient software code is obvious and thus pursued in all software implementations of the virtual prototyping routine in this thesis. Besides a generally efficient handling of the data and the use of computationally inexpensive code, a specific and powerful example is the strategic exploitation of termination conditions. Here, it is attempted to check the satisfaction of constraints as early as possible in the course of the mapping of a design into the performance space. This allows to prematurely discard a design if a constraint is not met and thus to save computational time. With reference to Chapter 1, this can be interpreted as checking as early as possible whether a specific design belongs to the feasible design space D or not. Additional details and examples will be given in Section 2.2.

Intelligent Direct Search Method

The second strategy aims at reducing the number of calculations of designs which are feasible, i.e. belong to the feasible design space D and can be mapped into P, but are not Pareto-optimal and thus not part of the solution to the optimization problem. In other words, it is ideally attempted to map only the Pareto-optimal subset of the design space into the performance space. The potential of this strategy in converter optimization problems is typically tremendous as only a diminishing fraction of the design space achieves a Pareto-optimal performance.

This type of strategy is predominantly employed by metaheuristic search methods such as gradient-based optimization schemes [39], genetic algorithms (GA) [54, 60, 64, 66–68] and particle swarm optimization [58]. In such approaches, the optimization problem is stated as a set of abstract equations and is solved without exploiting any physical insight. The approaches have in common that it is attempted to a priori estimate whether a specific design $(\vec{x}^*, \vec{k}^*)$ is promising, i.e. is likely to achieve a higher performance than previously (and often nearby in the design space) analyzed designs. Depending on the optimization scheme, different metaheuristics are utilized to asses the potential of $(\vec{x}^*, \vec{k}^*)$. If based on the employed metaheuristic it is found that it is likely that a better performance can be achieved $(\vec{x}^*, \vec{k}^*)$ will be analyzed, i.e. mapped into the performance space. If the chances are estimated to be low a further analysis of $(\vec{x}^*, \vec{k}^*)$ will be avoided. A number of serious drawbacks complicates these metaheuristic approaches: on the one

hand, the mapping from the design space is usually highly non-linear and discontinuous which renders a reliable a priori estimation of the performance of $(\vec{x}^*, \vec{k}^*)$ solely based on the performance of other designs challenging. On the other hand, most of the discussed approaches suffer from non-deterministic results due to the employed statistical means in the search algorithm and metaheuristics.

For the above stated reasons, an intelligent direct search method to identify the Pareto front is proposed instead. The proposed method is based on a systematic enumeration of the design space for the Pareto-optimal solutions. Thereby, it is guaranteed that the solution to the optimization problem is found in a deterministic manner. In contrast to a mere brute-force search method, the proposed intelligent direct search method incorporates additional problem-specific heuristics which enable a reduction of the number of designs to be analyzed. These heuristics mostly exploit physical relationships and insight of the employed models in order to prematurely detect designs which, due to physical reasons, cannot be Pareto-optimal. Examples are:

- When designing an inductor for a given inductance value and (outer) core and winding dimensions, a higher number of turns will concurrently decrease the core losses and increase the winding losses. Therefore, the number of turns should not be further increased as soon as the total core and winding losses start increasing.
- For a given fan, no further reduction of the thermal resistance $R_{\text{th,hs-amb}}$ can be achieved beyond a certain length of the heat sink. The physical reason here is the pressure drop of the heat sink which increases with the length (at otherwise unchanged dimensions of the fins and channels) and causes the volume flow of the air through the heat sink to decrease.

Note that this approach to reduce the size of the searched feasible design space is not based on abstract and possibly stochastic metaheuristics as employed in GAs or particle swarm optimizations. In fact, the proposed direct search method systematically enumerates the designs in the design space. It employs problem-specific heuristics as discussed above which only discards designs which, based on physical insight, cannot be optimal. Thereby, finding the globally optimal solutions can be guaranteed which is contrary to GAs and particle swarm optimizations.

Problem Simplifications

Simplification poses a third powerful strategy and aims at reducing the complexity of the optimization problem. As implicitly done in numerous contributions (e.g. [52]) and explicitly proposed in [8], a natural strategy is to break the converter optimization problem into sub-problems where the converter components can individually be optimized. This can predominantly be achieved by means of neglecting a range of coupling effects in the mapping from the design space into the performance space. With respect to the proposed virtual prototyping routine in this thesis, the following coupling effects are neglected:

(i) Most parasitic electromagnetic and thermal coupling effects between individual components are neglected.

(ii) With respect to the waveform synthesis, lossless components and interconnecting wires are assumed.

(iii) Parasitic capacitances and inductances of the components are to a wide extent neglected.

The following paragraphs discuss how the above neglected effects will affect the complexity but also the loss of accuracy of the virtual prototyping.

Comments to (i): parasitic, i.e. unwanted electromagnetic coupling effects play a major role in the EMI filter design due to a likely degradation of the EMI filter attenuation [77]. Apart from that, however, this type of coupling normally only has a minor impact on the remaining components regarding the selected performance measures, i.e. efficiency, volume and costs. Note that with respect to the semiconductor switching losses, the parasitic effects can to a wide extent be taken into account if measured switching losses are considered where the commutation-specific part of the (PCB) layout of the final converter is assumed to be similar as for the switching loss measurement test bench (cf. Section 3.1). The problem of unwanted electromagnetic coupling can further be relaxed if the magnetics either employ ungapped cores or gapped cores with air gaps that are limited in length and shielded by the windings (as applicable for the magnetics of this thesis). Apart from the lower complexity of the optimization problem, a second major motivation to neglect most electromagnetic coupling effects is the tremendous required modeling effort: on the one hand, the converter layout must be known in advance and taken into account. On the other

hand, the accurate modeling of electromagnetic coupling can usually only be attained with complex and time-consuming simulation tools (e.g. [77, 78]) which are not suitable for systematic optimizations. The only exception regarding the explicit consideration of parasitic electromagnetic coupling effects in this thesis are the parasitic capacitances of the semiconductor packages to the heat sink (which for given semiconductors are a priori known). These capacitances have a significant impact on the soft-switching operation of MOSFETs (Chapter 5) and the common mode (CM) EMI filter design of grid-tied DC/AC inverter systems (Chapter 6).

Comments to (ii): not only the electromagnetic but also the thermal coupling can only be accurately modeled if the system layout is a priori known. Note that in this thesis, the passive components are not mounted on a common heat sink (as sometimes done to enhance the cooling) which would simplify the calculation of the thermal coupling. Therefore, thermal coupling between different system components might be an issue in some cases. However, its implications can often be relaxed with a careful converter layout and/or conservative assumptions in the thermal models as the thermal models presented in this thesis (cf. Chapter 3). Therefore, due the challenging and time-consuming modeling effort on the one hand and the manageable impact on the system performance on the other hand, thermal coupling effects are neglected in this work.

Comments to (iii): parasitic capacitances and inductances of components usually have a minor impact on the considered performance measures, i.e. efficiency, volume and costs and can therefore mostly safely be neglected without substantially loosing accuracy. Non-negligible exceptions in this thesis are i) the parasitic MOSFET output capacitances and ii) the parasitic PCB capacitance which are, together with the parasitic capacitances of the semiconductor packages to the heat sink (cf. above), both decisive for attaining soft-switching (Chapter 5). Although not explicitly implemented in this thesis, a viable strategy to further relax the problem of parasitic capacitances and inductances could be the introduction of termination conditions in the component design stages which check for maximum tolerable values. This could, e.g., be a strategy to discard designs of a HF transformer with adverse resonant frequencies which cause excessive oscillations during the switching transitions [79].

2.1.3 Design Routine

The flow chart of the MOO-based main virtual prototyping routine is depicted in **Fig. 2.1**. The steps of the flow chart represent the practical implementation of the abstract performance function $\vec{\mathcal{P}}$ introduced in Chapter 1 which maps the design space into the performance space. From a conceptual point of view, the different steps of the routine shown in **Fig. 2.1** can be divided into the steps which are iterated on a global system level and the steps which are locally iterated on the component level. A step-by-step discussion of the individual design and optimization tasks of the routine is given below.

Input Data

The required inputs to the proposed implementation of the virtual prototyping routine includes the design variables ($\widehat{=}\ \vec{x}$, cf. Chapter 1), the component and material databases ($\widehat{=}\ \vec{k}$), the parameters of the employed design constraints as well as the system specifications (both $\widehat{=}\ \vec{r}$). The design variables are composed of the corresponding ranges, i.e. the N_{Π_j} discrete options which are analyzed for the corresponding variables Π_j. The material and component databases contain the information and constants, such as switching loss energies or core losses which describe the materials and components associated with the design variables. The constraints are relevant to control the permissible designs (feasible design space D) and typically includes parameters such as the maximum permissible semiconductor junction temperature or the maximum stacking factor of inductor cores. Note that these parameters are user-defined but should not violate any physical constraints or data sheet recommendations. Finally, the system specifications include all necessary information on how the converter system is operated. This mainly includes the input and output voltage ranges, power levels and ambient temperature ranges, i.e. the permissible operating conditions.

Global System-Level Loop

A fundamental feature of the proposed virtual prototyping routine is the omission of most unwanted parasitic coupling effects as discussed in the previous section. Certainly, the conducted waveforms do not belong to this category of coupling effects as they are the desired primary means of power transfer. Consequently, the conducted waveforms

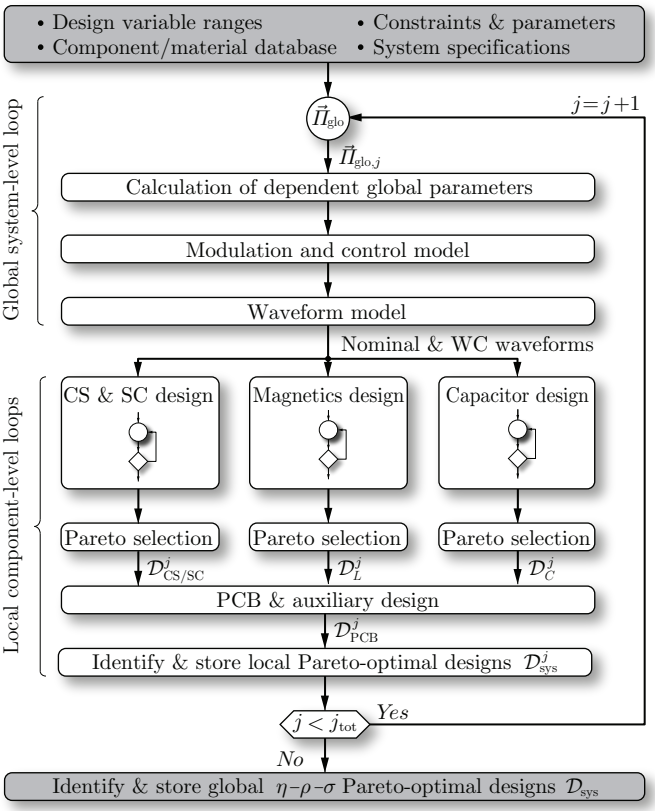


Fig. 2.1: Proposed main virtual prototyping design routine. The routine performs the mapping of the design space into the performance space under the consideration of user-defined constraints and system specifications. The routine incorporates a MOO scheme which identifies the η-ρ-σ Pareto front. The simplification of selected coupling effects enables the separation of the optimization problem into a global problem on the system level and various local component-related sub-problems. Thereby, all design variables $\Pi_{\mathrm{glo},j}$ which have an impact on the conducted waveforms must be assigned to the system level whereas the remaining variables can be split into independent groups of which each is associated with a particular component. For each global iteration, i.e. for each calculated set of nominal and worst case waveforms, this approach allows to individually dimension and optimize the components and to determine the optimal system designs $\mathcal{D}^j_{\mathrm{glo}}$ as combinations of the found optimal component designs $\mathcal{D}^j_{\mathrm{CS/SC}}$, $\mathcal{D}^j_L$, $\mathcal{D}^j_C$, $\mathcal{D}^j_{\mathrm{PCB}}$.

have a coupled and system-wide impact on the converter performance. Therefore, all design variables $\Pi_{\mathrm{glo},j}$ which have an effect on the waveforms must be globally iterated. This means that the calculation and design of the entire system including all components must be repeated for each iteration of the these global variables. It thus becomes evident that global variables are computationally expensive. If none of the coupling effects discussed in the previous section were neglected, the large majority of design variables would have to be assigned to this global system-level loop. However, in the proposed case where the conducted waveforms are the only maintained coupling effect (apart from a few exceptions as discussed above), typical global variables are:

- The topology,
- Any modulation scheme-related variables such as the switching frequency, and
- All primary, i.e. non-parasitic component values such as inductances, capacitances and turns ratios.

At the beginning of each global iteration, in a first step, additional global parameters are defined. These parameters are not part of the global design variables $\Pi_{\mathrm{glo},j}$ but are chosen as a function of them. These parameters which often represent component values (inductances, capacitances) have in common that they are relevant for the subsequent behavioral models, i.e. the converter modulation and control model and the waveform model.

In a next step, the modulation and control model is executed. This model mainly determines how the converter operates as a function of the operating points, component values and the chosen modulation scheme. Questions like how many of the branches in parallel interleaved converters are active or which operating mode of the modulation scheme is employed must be answered here. This consequently allows to calculate the waveforms in the next step. Note that the waveform calculation not only involves the calculation of the nominal waveforms but also the identification of the worst case waveforms. The former are typically used to calculate the (averaged) nominal efficiency whereas the latter are required for the proper and realistic system dimensioning. Depending on the component type, one or more worst cases are relevant:

- *Semiconductors and cooling system:* thermal worst case;

- *Magnetics:* winding thermal, core thermal and linked flux worst cases;
- *Capacitors:* rms current and voltage ripple, i.e. charge worst cases; and
- *EMI filter:* DM and CM emission level worst cases.

If the operating point is not only defined by the active power level but also includes further parameters such as the reactive power level as well as the input and output voltages, finding the respective worst case operating points is usually not obvious. In many cases a substantial subset of the entire operating range must be screened which can thus imply a considerable computational effort. The search of the thermal worst case operating points for semiconductors and magnetics is further complicated as more than one loss source contributes to the thermal heating of these components. E.g. for semiconductors with both current-sensitive conduction and current-/voltage-sensitive switching losses it is a priori not clear whether an operating point with high currents/low blocking voltages or an operating point with low currents/high blocking voltages results in the maximum device temperature. As a consequence, mostly more than one set of candidate thermal worst case waveforms must be calculated and stored for the semiconductors and magnetics.

Further details on the behavioral models cannot be given here as the involved modulation and control and waveform models are application- and converter system-specific. More information is given in the respective case studies in Chapter 5 and Chapter 6 for a DC/DC and DC/AC system, respectively.

Local Component-Level Loops

The nominal and worst case waveforms of the global behavioral model represent a main input to the component design routines. At this stage of a global iteration, each component is individually optimized based on the specified component-related design variables, material and component constants and constraints. Details on the involved sub-routines for the different component types, such as the semiconductors and the cooling system, the magnetics and the capacitors are given in Section 2.2. Note that the PCB can either be modeled as an independent component or as a component whose area depends on the size of the other converter components as indicated in **Fig. 2.1**.

The local component level-iterations are concluded by the identification and storage of the Pareto-optimal system designs $\mathcal{D}_{\text{sys}}^{j}$ which are composed of valid combinations of the found optimal component designs $\mathcal{D}_{\text{CS/SC}}^{j}$, $\mathcal{D}_{L}^{j}$, $\mathcal{D}_{C}^{j}$, $\mathcal{D}_{\text{PCB}}^{j}$.

Output Data

The completion of the iteration over all available combinations of the global variables $\vec{\Pi}_{\text{glo},j}$ also marks the completion of the mapping of the design space into the performance space. Consequently, the final step to be accomplished is the identification of the global Pareto front, i.e. the globally Pareto-optimal designs $\mathcal{D}_{\text{sys}}$ amongst the calculated locally Pareto-optimal designs $\mathcal{D}_{\text{sys}}^{j}$.

One of the opportunities after the identification of the Pareto front is the employment of analysis tools which investigate the characteristics of the underlying designs and components. Furthermore, post-processing tools to determine a candidate system amongst the Pareto-optimal designs can be employed. As proposed in Chapter 1, this can be facilitated by an additional mapping of the Pareto front into a 1D mission cost space according to an arbitrary user-defined mission cost function which allows to compare the Pareto-optimal designs based on a single key figure. This task is again application-specific and more information is thus given in the respective case studies in Chapter 5 and Chapter 6 for a DC/DC and DC/AC system, respectively.

2.2 Component Design Routines

This section details the proposed component design and optimization sub-routines which are part of the main virtual prototyping routine shown in **Fig. 2.1**. Note that in this thesis the component routines are, in contrast to the converter behavioral models, largely invariant from the specific application and converter system.

2.2.1 Semiconductors and Cooling System

This section discusses the proposed design and optimization routine of the semiconductors and the associated cooling system. The respective flow chart for the semiconductor design is depicted in **Fig. 2.2**.

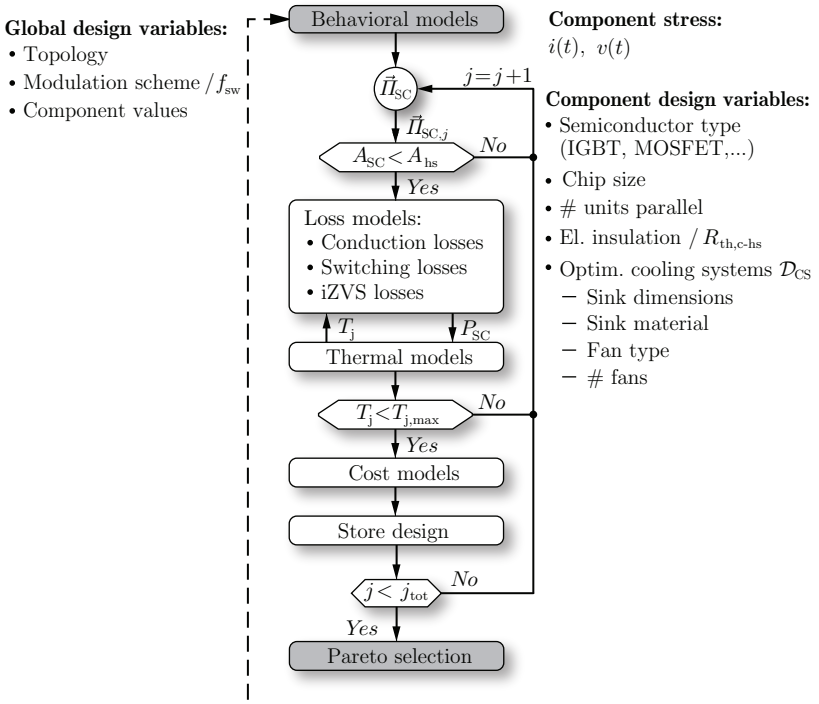


Fig. 2.2: Simplified design and optimization flow chart for the semiconductors as employed in the main virtual prototyping routine depicted in **Fig. 2.1**. Based on the waveforms provided by the superordinate behavioral models, the temperature-dependent semiconductor losses are calculated. The main termination conditions include the total area A_{SC} occupied by the semiconductor packages (plus margin) which must not be larger than the area of the selected heat sink A_{hs} and the compliance with the (user-defined) maximum permissible junction temperatures $T_{j,max}$. After the iteration over all permissible design options $\vec{\Pi}_{SC,j}$, only the Pareto-optimal designs are kept. The set of optimized cooling system designs $\mathcal{D}_{CS}$ which represents a design variable in this routine is obtained from the off-line routine depicted in **Fig. 2.3**.

Input Data

As in all of the presented component design routines, the operating point-dependent waveforms (including the worst case waveforms) obtained from the superordinate behavioral models represent the dynamic

input. On the other hand, the static inputs to the component routine are composed of the user-defined constraints and the selected component design variables and associated material and component database. Prominent design variables for the semiconductor design are:

- The type of each semiconductor,
- The chip size of each semiconductor,
- The number of parallelized packages per switch,
- The thermal resistance $R_{\mathrm{th,c\text{-}hs}}$ of the insulation between the packages and the heat sink, and
- The cooling system.

The cooling system in turn can be implemented taking into account various design variables such as the heat sink dimensions and fan types. In this thesis, the cooling system are designed off-line, i.e. in advance and separately from the main virtual prototyping design routine shown in **Fig. 2.1**. Only the set of optimized cooling system designs is then considered as input to the main routine, i.e. as design variable in the semiconductor design routine. Further details on the cooling system optimization are given below.

Design Procedure

For each of the above mentioned design variables it is first checked whether the semiconductors fit onto the heat sink. The semiconductor losses P_{SC} are then calculated in a next step. The semiconductor loss models in this thesis are temperature dependent. As the derivation of a general closed-form solution is difficult, the losses P_{SC} and corresponding junction temperatures T_{j} must be iteratively determined by means of a repeated execution of the loss and thermal models until sufficient convergence of the junction temperatures is reached. In this work, a relative temperature change of less than 1 % with respect to the calculated absolute junction temperature (in °C) is considered to be sufficient. Note that this step must be carried out for the waveforms of all nominal and worst case operating points. In a subsequent step it is checked whether the obtained junction temperatures violate the maximum permissible values. If all constraints are met and the design must not prematurely be discarded, the cost model can be employed to calculate the component costs and the design can be stored. After looping

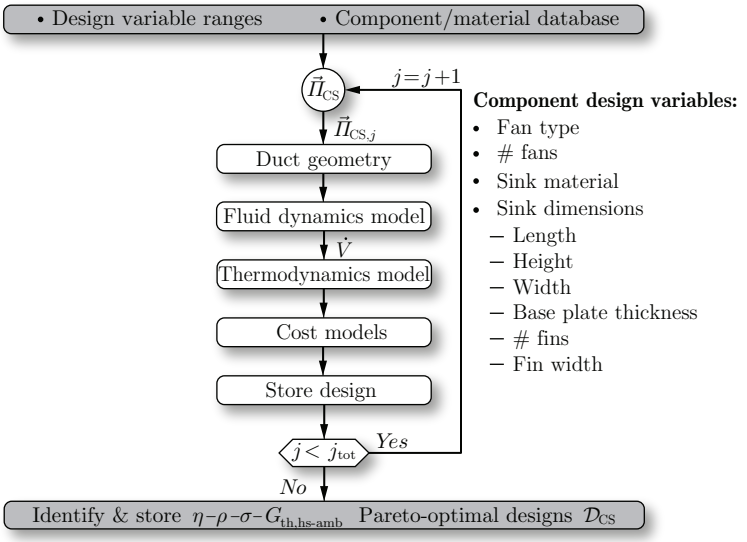


Fig. 2.3: Cooling system design and optimization routine. This routine identifies cooling system designs $\mathcal{D}_{\mathrm{CS}}$ which are optimized regarding the losses, volume, costs and the thermal resistance. The routine is executed off-line, i.e. separately from the main virtual prototyping routine. Only the stored outputs $\mathcal{D}_{\mathrm{CS}}$ are then used in the semiconductor design routine in **Fig. 2.2** which is part of the main routine. For details regarding the geometric variables of the heat sink refer to Section 3.2.

over all available design variable combinations $\vec{\Pi}_{\mathrm{SC},j}$, the design procedure terminates with the identification of the Pareto-optimal designs. Only the Pareto-optimal designs are kept and used in the subsequent analysis.

Note that for clarity reasons, **Fig. 2.2** only shows the conceptual design procedure which is partly simplified when compared to the actual implementation. In the actual implementation the design procedure is optimized with respect to the minimization of the computational time and of the number of designs which must be checked to identify the Pareto-optimal designs. E.g. a design can already be discarded if only one semiconductor in a single operating point does not meet the junction temperature constraint. This can strategically be exploited by always calculating the worst case operating points first. Moreover,

all cooling systems which feature a higher thermal resistance $R_{\text{th,hs-amb}}$ than the current cooling system which lead to the violation of the temperature constraint do not have to be analyzed anymore (for the semiconductor configuration at hand).

Design of the Cooling System

The off-line design and optimization routine for the cooling system is depicted in **Fig. 2.3**. All possible design variables are related to the fans and the heat sink geometry. At the beginning of each iteration, the required duct geometry linking the fans with the heat sink is calculated. Fluid dynamics and thermodynamics models enable the calculation of the thermal conductance $G_{\text{th,hs-amb}} = R_{\text{th,hs-amb}}^{-1}$ of the design. Finally, all Pareto-optimal designs $\mathcal{D}_{\text{CS}}$ with respect to the (fan) losses, the volume, the costs and the thermal conductance are stored and subsequently employed in the semiconductor design routine of **Fig. 2.2**.

2.2.2 Magnetics

Fig. 2.4 depicts the proposed sub-routine for the design and optimization of the magnetic components. In this thesis, this includes DC and AC chokes, transformers and common mode (CM) inductors.

Input Data

The required input data is composed of the component-specific design variable ranges, the associated material and component database entries and the constraints. The design variables for magnetics may include the following main positions:

- Core options (e.g. type, dimensions, number of air gaps, number of stacked cores, material),
- Winding options (e.g. type, dimensions, number of turns, material, insulation), and
- Coil former options (e.g. dimensions, material).

The additionally required dynamic inputs are provided by the preceding behavioral models and consist of the current and voltage waveforms in time domain as well as the corresponding spectrum of the current in the frequency domain. Note that the required inductance L^* for DC

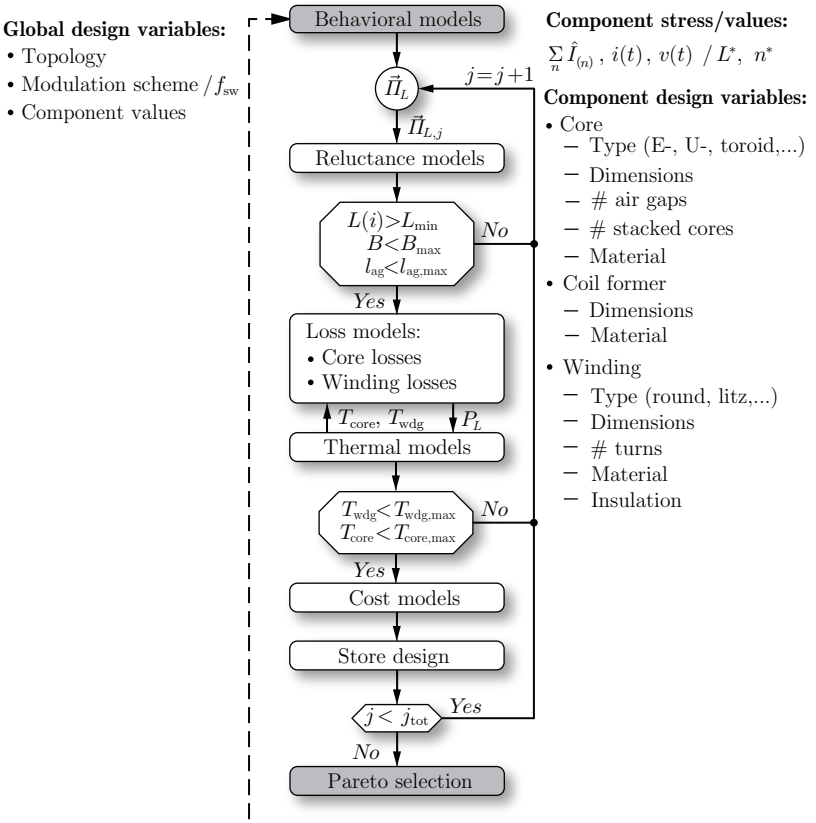


Fig. 2.4: Simplified design and optimization flow chart for the magnetic components as employed in the main virtual prototyping routine depicted in **Fig. 2.1**. The required inductance value L^* or transformer turns ratio n^* and the waveforms are provided by the superordinate global system-level loop. Based on the reluctance model the magnetic characteristics such as the current-dependent inductance $L(i)$, the flux densities B and the required air gap length l_{ag} are calculated and checked for the respective constraints. In a next step, the temperature-dependent core and winding losses are computed and again checked. If all constraints are met, the costs can be calculated and the design stored. Only Pareto-optimal designs are kept.

or AC chokes or the turns ratio n^* for transformers is normally also determined in the superordinate iteration of the global system-level loop and is either given by an independent design variable or calculated as part of the dependent system parameters (cf. **Fig. 2.1**).

Design Procedure

Each iteration of the design procedure commences with the execution of the reluctance model which calculates, based on the core geometry, core material and the number of winding turns, the required air gap length l_{ag} to achieve the required inductance L^*, the operating point-dependent flux densities B and the varying (non-linear) inductance $L(i)$ as a function of the current. If the constraints corresponding to these quantities are met, the temperature-dependent core losses P_{core} and winding losses P_{wdg} in conjunction with the respective temperatures T_{core} and T_{wdg} are iteratively calculated until a sufficient level of convergence is achieved. If the temperature constraints are not violated, the costs are calculated and the design stored. After iterating over all possible combinations of design variables $\vec{\Pi}_{L,j}$, the design procedure terminates with the identification of the Pareto-optimal designs. Only the Pareto-optimal designs are kept and used in the subsequent analysis.

Note again that for clarity reasons, **Fig. 2.4** only shows a simplified version of the implemented design routine for the magnetics. The calculation of magnetic components belongs to the most time-consuming tasks of the overall routine due to the large number of available design variables and the complexity of the involved models. Therefore, various schemes are incorporated to either avoid the investigation of inefficient designs or at least to detect and discard inefficient designs as early as possible during the design procedure.

2.2.3 Capacitors

Fig. 2.5 depicts the proposed sub-routine for the design and optimization of capacitors. In this thesis, the capacitor includes DC capacitors as well as differential and common mode filter AC filter capacitors. The same routine could also be used for resonant capacitors.

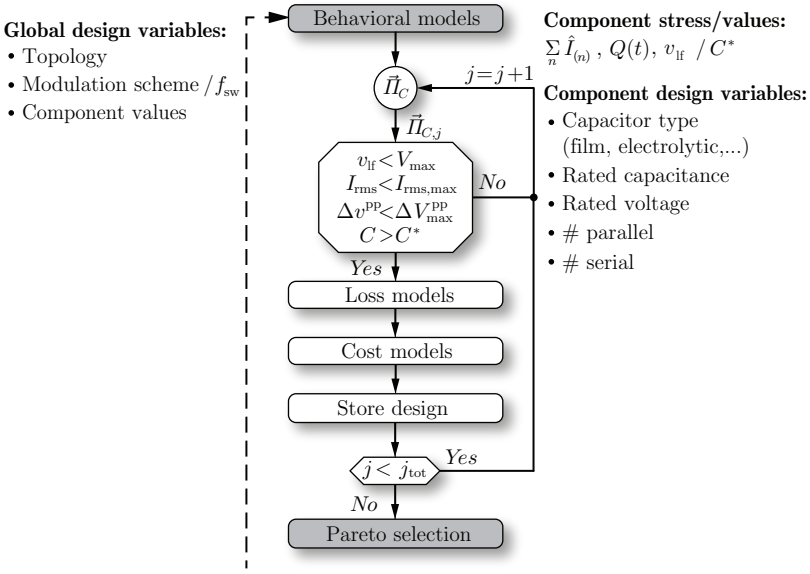


Fig. 2.5: Simplified design and optimization flow chart for the capacitors as employed in the main virtual prototyping routine depicted in **Fig. 2.1**. A selected design must be able to handle the LF (DC or 50 Hz AC) voltage stress v_{lf} and the current stress. Furthermore, the minimum specified capacitance C^* and in some cases a (HF) voltage-ripple criterion must be met. If all requirements are fulfilled, the losses and costs of the capacitor design is calculated and stored. Only Pareto-optimal designs are kept.

Input Data

On the one hand, the input data comprises the static information which is given by the design variable ranges, the material and component information and the constraints. Typical design variables are:

- The capacitor type,
- The number of capacitors in parallel,
- The number of capacitors in series,
- The rated capacitance of each capacitor, and
- The rated voltage of each capacitor.

On the other hand, the capacitor routine additionally requires the dynamic input data from the current iteration of the global system-level loop which provides the current spectrum $\sum \hat{I}_{(n)}$, the time-dependent capacitor charge balance $Q(t)$ and the LF voltage waveforms v_{lf} (DC or 50 Hz – without superimposed HF ripple due to the charge variation $Q(t)$). The target (minimum) capacitance value C^*, if specified, is also provided.

Design Procedure

Each configuration of capacitors, i.e. each combination of design variables $\vec{\Pi}_{C,j}$ is first checked for sufficient voltage and current handling capabilities. Furthermore, the capacitor must feature or exceed the minimum specified capacitance C^* (e.g. to attain sufficient control stability) and meet the maximum voltage-ripple criterion. The latter predominantly applies to DC capacitors. In case that all requirements are fulfilled, the costs and losses are calculated and the design is stored. After iterating over all possible combinations of design variables $\vec{\Pi}_{C,j}$, the design procedure terminates with the identification of the Pareto-optimal designs. Only the Pareto-optimal designs are kept and used in the subsequent analysis.

The actual implemented design routine for capacitors again slightly differs from the simplified procedure depicted in **Fig. 2.5** for reasons of achieving a higher computational efficiency.

2.3 Software Implementation

This section discusses some of the practical aspects and challenges of the software implementation of the proposed design routines and models in this thesis.

The large majority of models and routines are implemented as MATLAB scripts and functions. The main benefit of using MATLAB is its extremely powerful and broad diversity of in-built numerical methods. Particularly useful methods include the efficient methods for the fast Fourier transform (FFT) and handling of dynamic systems and transfer functions. Other advantages are the simple syntax, the powerful options of organizing and handling complex data structures and the comprehensive graphics functions for the analysis of intermediate and final results. The main drawback poses the comparatively slow execu-

tion times as MATLAB code is directly interpreted rather than first compiled into native binary code before the execution. This drawback, however, is partly compensated by the possibility of parallel computing and the embedding of more computationally efficient compiled C code. The implemented MATLAB code encompasses approximately 10 000 lines of code for the component-related routines and models. Another 7 000 lines were written for the application-specific system-related models and routines needed in the DC/DC and DC/AC case studies of this thesis. About 60 % of the component-related code is dedicated to the magnetics.

2.3.1 Execution of the Virtual Prototyping Routine

The MATLAB implementation of the proposed virtual prototyping routines is executed on workstations equipped with 2×2.4 GHz Intel XEON quad-core CPUs and 64 GB of RAM. Depending on the model complexity, the full execution of the routine for a single converter concept (cf. Chapter 5 and Chapter 6) using one workstation takes between 5 and 20 hours of which roughly 40 % of the time is spent for waveform and EMI filter calculations as part of the global system-level loop, 50 % for the magnetics design as part of the local component-level loop and 10 % for the rest. Parallel computing is employed whenever applicable. It is advisable to store the full set of operating point-dependent waveforms once calculated. If adjustments in the code or modifications to the input parameters are only made on the component level, the time-consuming execution of the global system-level loop can then be skipped. Further information on execution speeds and the complexity of the optimization problems are given in the case studies in Chapter 5 and Chapter 6.

2.3.2 Identification of the Pareto front

The identification of the Pareto-optimal designs in the performance space represents both a fundamental task but also a big challenge. The main reason for this non-trivial task is the high number of up to 100 design variables which can be involved in the optimization of power electronic converter systems. Despite many constraints this high number of variables still results in an enormous amount (trillions) of designs in the feasible performance space. The complexity of identifying the Pareto-optimal designs amongst n designs with p associated performance measures (here $p = 3$) is $\mathcal{O}(n^2 \cdot p)$. It thus becomes evident

that the implementation of specific strategies in the virtual prototyping routine is mandatory to render this task tractable within a reasonable time and with the given memory:

- *Discard non-optimal designs*: non-optimal intermediate results (such as designed components) are detected and discarded as early as possible as on principle they cannot result in optimal designs at a later stage of the design routine. Therefore, on the component level, for each component only the Pareto-optimal designs, i.e. $\mathcal{D}^j_{\mathrm{CS/SC}}$, $\mathcal{D}^j_L$, $\mathcal{D}^j_C$, $\mathcal{D}^j_{\mathrm{PCB}}$ in **Fig. 2.1**, are kept. Furthermore, at the end of a global iteration, the optimal overall converter system designs $\mathcal{D}^j_{\mathrm{sys}}$ based on the possible combinations of the Pareto-optimal component designs of the current jth iteration are determined. All other non-optimal combinations are not considered anymore and components which are not part of any optimal overall design $\mathcal{D}^j_{\mathrm{sys}}$ are discarded at this stage. This approach enables to identify the globally optimal system designs $\mathcal{D}_{\mathrm{sys}}$ amongst as few as possible designs, namely the union of all locally optimal designs $\bigcup_j \mathcal{D}^j_{\mathrm{sys}}$.
- *Multi-stage Pareto analysis*: despite the forgoing omission of non-optimal component designs the complexity of finding the overall optimal component combinations $\mathcal{D}^j_{\mathrm{sys}}$ (cf. **Fig. 2.1**) remains very high. Consider a converter system which can feature up to 20 components. If only 10 Pareto-optimal designs per component have been found, 10^{20} (!) possible combinations result. Clearly, this tremendous number of combinations cannot be treated at once with the given memory and computation power ($n^2 \cdot p = 10^{20} \cdot 10^{20} \cdot 3$ comparisons would be needed). Therefore, the problem must be split into sub-problems. The key here is to analyze the possible combinations of only 3-5 components at the time and to keep again only the (few) Pareto-optimal combinations. In a second and third step, the analyzed groups are merged and analyzed again. Certainly, this approach can only succeed provided that only a diminishing number of combinations is Pareto-optimal and thus only very few combinations are left after each stage of the procedure.
- *Utilization of embedded C code*: for the specific task of identifying the Pareto front, compiled C code was embedded instead of employing MATLAB code. Due to the simple but repetitive

steps which are involved in the Pareto front identification, C code performs particularly well here and allows to reduce the computational time by more than a factor 1 000 (!) when compared to the MATLAB equivalent.

The combined use of the above strategies render a virtually intractable problem into a task which takes less than 5 % of the total execution time of the main virtual prototyping routine.

3

Multi-Physics Component Modeling

The multi-physics component models represent an essential part of every powerful virtual prototyping routine. The main task of these models is to provide estimations on the component performance measures (losses, volume and costs) as a function of the design variables. This information enables the superordinate design and optimization routine presented in the previous chapter to search and identify the optimal selection of the design variables. Thereby, it becomes evident that the significance and relevance of the identified Pareto-optimal solutions dramatically depend on the accuracy of the employed models.

This chapter comprehensively discusses the models which are required in the routine presented in the previous Chapter 2. Detailed models for the typical power components of state-of-the-art switched-mode power electronic converters are presented. This includes the semiconductors, the cooling system, the magnetics and the capacitors. As the overall achievable accuracy not only depends on the range of the modeled dependencies (e.g. the dependency from the temperature) but also strongly on the accurate model parametrization, strong emphasis is put on model parameter determinations which are based on experimental measurements and subsequent verifications. The corresponding measurement methods and results are discussed in detail in this chapter. Some application-specific models, e.g. for the PCB and auxiliary supply losses, are treated in the respective case studies of this thesis.

Selected parts of this chapter are based on the work presented in [80–83].

3.1 Semiconductors

This section proposes detailed models for the calculation of the conduction and switching losses of power semiconductors. Furthermore, soft-switching operation based on zero voltage switching (ZVS) of MOSFETs is revisited and the occurring switching losses are modeled and analyzed in detail.

3.1.1 Conduction Losses

The conduction losses of a particular power semiconductor is a function of its output characteristic. For devices with an built-in pn-junction such as IGBTs the average losses within a time interval T can be computed with

$$P_{\mathrm{c}}^{\mathrm{pn}}\big(i_{\mathrm{ce}}(t), T_{\mathrm{j}}, V_{\mathrm{gate}}\big) = \frac{1}{T}\int_0^T V_{\mathrm{ce}}\big(i_{\mathrm{ce}}(t), T_{\mathrm{j}}, V_{\mathrm{gate}}\big) \cdot i_{\mathrm{ce}}(t)\,\mathrm{d}t\ . \tag{3.1}$$

In (3.1), V_{ce} denotes the collector-to-emitter voltage which depends on the current i_{ce} through the device, the device junction temperature T_{j} and the voltage applied to the gate V_{gate}. In the case of a PiN or Schottky diode the same model can be employed where the dependency from V_{gate} does not apply and V_{ce} is substituted with the anode-to-cathode forward voltage $V_{\mathrm{f}}\big(i_{\mathrm{ac}}(t), T_{\mathrm{j}}\big)$. For field effect transistors (FET) such as MOSFETs or JFETs, the model (3.1) can analogously be used. However, due to the ohmic properties of the linear region of the output characteristic, (3.1) is usually modified to

$$P_{\mathrm{c}}^{\mathrm{fet}}\big(i_{\mathrm{ds}}(t), T_{\mathrm{j}}, V_{\mathrm{gate}}\big) = \frac{1}{T}\int_0^T R_{\mathrm{ds,on}}\big(i_{\mathrm{ds}}(t), T_{\mathrm{j}}, V_{\mathrm{gate}}\big) \cdot i_{\mathrm{ds}}^2(t)\,\mathrm{d}t\ , \tag{3.2}$$

with

$$R_{\mathrm{ds,on}}\big(i_{\mathrm{ds}}, T_{\mathrm{j}}, V_{\mathrm{gate}}\big) = \frac{\partial\, V_{\mathrm{ds}}(i_{\mathrm{ds}}, T_{\mathrm{j}}, V_{\mathrm{gate}})}{\partial\, i_{\mathrm{ds}}}\ . \tag{3.3}$$

In (3.2), $R_{\mathrm{ds,on}}$ denotes the equivalent on-state resistance of the device which depends on the drain-to-source current i_{ds}, the junction temperature T_{j} and the gate voltage V_{gate}. Care must be taken if the FETs are operated in the third quadrant, i.e. with negative i_{ds}. If the negative current in the FET channel is high enough to forward bias the parasitic

anti-parallel body diode, the current splits between the ohmic channel and the diode. This type of operation can then usually be better described with the model (3.1).

Input Variables

The proposed conduction loss models take into account the dependencies from the time-varying current, the average junction temperature and the gate voltage. The implications regarding the calculation of the input variables are discussed below.

- The model requires the synthesis and availability of the entire current waveform in time-domain. These currents are provided by the waveform model which is part of the superordinate behavioral models. The chosen modeling approach enables the detailed consideration of the strongly non-linear output characteristics which are typical for pn-junction-based devices and to some extent also for FETs (cf. **Fig. 3.1**). In contrast to the frequently used (e.g. [17, 52, 84]) linearized conduction loss models,

$$P_{\mathrm{c}}^{\mathrm{pn,lin}}\big(I_{\mathrm{ce,avg}}, I_{\mathrm{ce,rms}}\big) = V_{\mathrm{fw}} \cdot I_{\mathrm{ce,avg}} + R_{\mathrm{fw}} \cdot I_{\mathrm{ce,rms}}^2 \ , \tag{3.4}$$

$$P_{\mathrm{c}}^{\mathrm{fet,lin}}\big(I_{\mathrm{ds,rms}}\big) = R_{\mathrm{ds,on}} \cdot I_{\mathrm{ds,rms}}^2 \ , \tag{3.5}$$

  (dependence from T_{j} and V_{gate} omitted for clarity reasons), an improved accuracy can be gained which comes at the cost of a higher computational effort during the optimization due to the (numerically performed) integration in (3.1) and (3.2).

- The proposed models consider the dependence from the average junction temperature T_{j}. This implies the need of calculating the average junction temperature as a function of the (operating point-dependent) average semiconductor losses by means of a static thermal model as presented below in this section. The consideration of a time-varying rather than average junction temperature $T_{\mathrm{j}}(t)$ in the model would considerably increase the computational effort. Furthermore, such an approach would require a dynamic rather than a static thermal model. The smallest time constants of the junction-to-case thermal impedances $Z_{\mathrm{th,jc}}$ of semiconductors are typically in the range of 10-100 µs (e.g. [85])

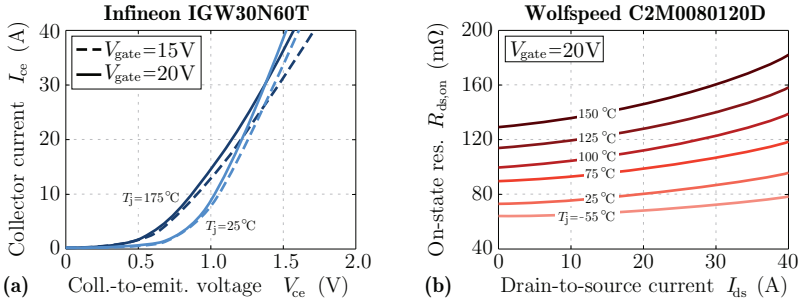


Fig. 3.1: Example of typical data sheet information for the parametrization of the proposed conduction loss models. **(a)** Output characteristics of a 600 V Si IGBT [85] for different gate voltages V_{gate} and junction temperatures T_j for the model (3.1). **(b)** On-state resistance $R_{ds,on}$ of a 1200 V SiC MOSFET [87] for different junction temperatures T_j for the model (3.2). In both cases, continuous parameterizations can be achieved by means of interpolation.

but can be significantly higher in case of larger chip areas. Therefore, in DC/DC converters switching at several tens of kHz the resulting thermal cycling is usually not an issue which renders the consideration of a time-varying junction temperature obsolete. Similarly in 50 Hz grid applications where the thermal cycling of $T_j(t)$ is somewhat more pronounced and might be in the range of $\pm[3, 10]$ °C (e.g. [75]), no significant improvement in accuracy can be expected. Within such a narrow window, the temperature-dependence is usually weak and almost linear and can thus be accurately captured with the proposed approach based on the average operating point-dependent junction temperature T_j.

- The gate voltage in this work is assumed to be user-defined and time- and operating point-invariant. The dynamic control of the switching transitions by means of the gate voltage (as e.g. shown in [86]) is not considered. Hence, no calculations or further models are required.

Parametrization

The parameters of the proposed conduction loss models, i.e. V_{ce}, V_f and $R_{ds,on}$ can mostly be extracted from the device data sheets which

usually provide sufficiently accurate and detailed data. Examples from a data sheet of a commercial Si IGBT and SiC MOSFET are shown in **Fig. 3.1**. Parameterizations which are continuous in all variables can be obtained by means of interpolation of the provided data sheet information.

3.1.2 Switching Losses

The switching losses P_{sw} in this thesis are calculated using

$$P_{\mathrm{sw}}\big(I_{\mathrm{on}}, I_{\mathrm{off}}, V_{\mathrm{on}}, V_{\mathrm{off}}, T_{\mathrm{j}}, V_{\mathrm{gate,on}}, V_{\mathrm{gate,off}}, R_{\mathrm{gate,on}}, R_{\mathrm{gate,off}}\big) = \frac{1}{T} \cdot \Bigg[\sum_{i=1}^{N_{\mathrm{sw,on}}} E_{\mathrm{on}}\big(I_{\mathrm{on},i}, V_{\mathrm{on},i}, T_{\mathrm{j}}, V_{\mathrm{gate,on}}, R_{\mathrm{gate,on}}\big) + \sum_{i=1}^{N_{\mathrm{sw,off}}} E_{\mathrm{off}}\big(I_{\mathrm{off},i}, V_{\mathrm{off},i}, T_{\mathrm{j}}, V_{\mathrm{gate,off}}, R_{\mathrm{gate,off}}\big) \Bigg], \quad (3.6)$$

with $N_{\mathrm{sw,on}}$, $N_{\mathrm{sw,off}}$ being the number of turn-on and turn-off switching transitions within the time interval T. $E_{\mathrm{on/off}}$ denote the turn-on and turn-off switching loss energies which are here a function of the switched currents $I_{\mathrm{on/off},i}$ and corresponding blocking voltages $V_{\mathrm{on/off},i}$, the average semiconductor junction temperature T_{j} as well as the gate voltages $V_{\mathrm{gate,on/off}}$ and the respective gate resistances $R_{\mathrm{gate,on/off}}$.

Input Variables

The proposed model (3.6) requires the calculation and definition of the following input variables:

- All pairs of switched current and switched (blocking) voltage $(I_{\mathrm{on/off},i}, V_{\mathrm{on/off},i})$ within T. The switched currents $I_{\mathrm{on/off},i}$ can be extracted from the synthesized current waveforms in time domain which are required for the calculation of the conduction losses. The switched voltages , $V_{\mathrm{on/off},i}$ can analogously be extracted from the voltage waveform $v(t)$ across the semiconductor and are often constant within T;
- The calculation of the average junction temperature T_{j} based on the thermal model which is presented further below in this section; and

- The definition of the gate voltages and gate resistances $V_{\text{gate,on/off}}$ and $R_{\text{gate,on/off}}$, respectively. Contrary to dynamic gate drivers (e.g. [86]), in this thesis these user-defined values are constant, i.e. time- and operating point-invariant.

Parametrization

The required parameters for the proposed model are the switching loss energies $E_{\text{on/off}}$. For several reasons relying on the respective information in data sheets is not recommended: on the one hand, the data sheet information is often incomplete where the desired ranges of the input variables are not covered or the dependency from one variable is only shown at fixed values of the remaining input variables. On the other hand, the switching loss energies strongly depend on the layout/parasitics of the gate driver, the gate driver components and the layout/parasitics of the power circuit including the parasitics resulting from the mounting of the semiconductor.

Due to the decisive impact on the system performance it is therefore recommended to determine the switching loss energies individually for each combination of semiconductor, gate driver unit and power circuit layout. The measurements usually require the implementation of a hardware measurement test bench as shown in **Fig. 3.2**. Several methods have been reported to accomplish this task:

- *Direct waveform measurement*: the concurrent measurement of the current and voltage waveforms in the semiconductor under test enables the calculation of the switching loss energies. The measurements obtained by performing short double pulse waveforms can be repeated for varying input variables of the model (3.6) at a reasonable effort. Hereby, due to the non-continuous double-pulse waveforms, the semiconductor junction temperatures can be assumed to be equal to the temperature of the heat plate on which they are mounted to (cf. **Fig. 3.2**). A high accuracy of the measurement can be expected provided that suitable measurement equipment with sufficient bandwidth is available. The employment of this method is mainly limited in case of i) very fast switching dynamics causing a high sensitivity towards the deskew of the voltage and current measurement, and ii) very small packages and commutation loops where the probes are difficult to

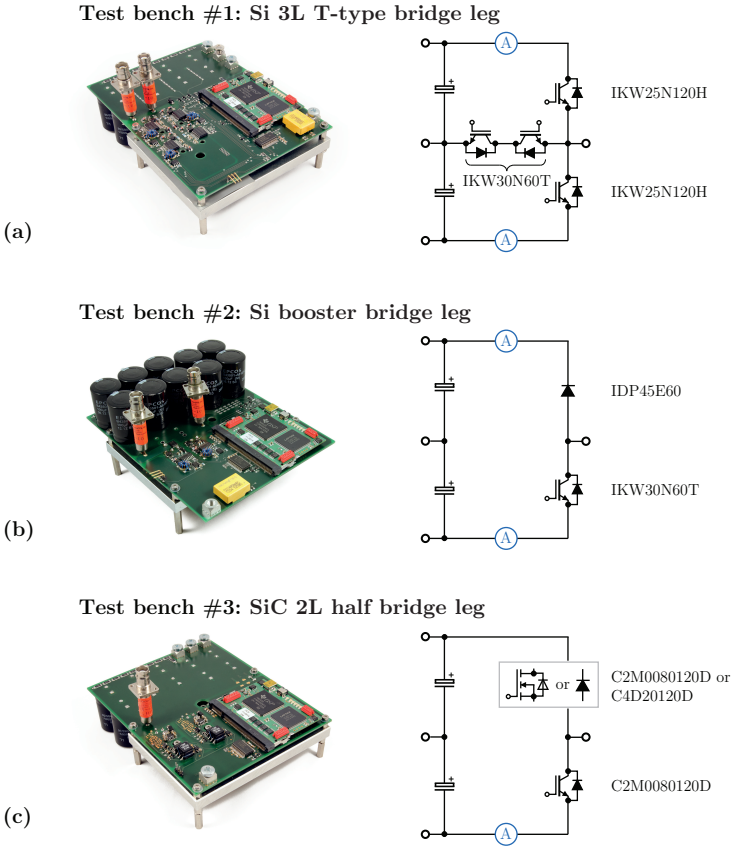


Fig. 3.2: Implemented test benches used to determine the switching loss energies depicted in **Fig. 3.3**, **Fig. 3.4** and **Fig. 3.6** (with a connected external inductive load). **(a)** 3-level test bench implementing a T-type bridge leg with 600 and 1200 V Si IGBTs. **(b)** Test bench implementing a booster bridge leg with a 600 V Si IGBT and a 600 V Si PiN diode. **(c)** Test bench implementing a 2-level half bridge leg where a 1200 V SiC MOSFET commutates either with another 1200 V SiC MOSFET or a 1200 V SiC Schottky diode (interchangeable semiconductors). All test benches employ a digital controller to generate suitable gate signals for double pulse tests. High-bandwidth 1 GHz current shunts are used to measure the currents by means of a coaxial cable whereas the voltages are measured with high-voltage passive probes. The semiconductors are mounted on heating plates which allow for measurements at different junction temperatures.

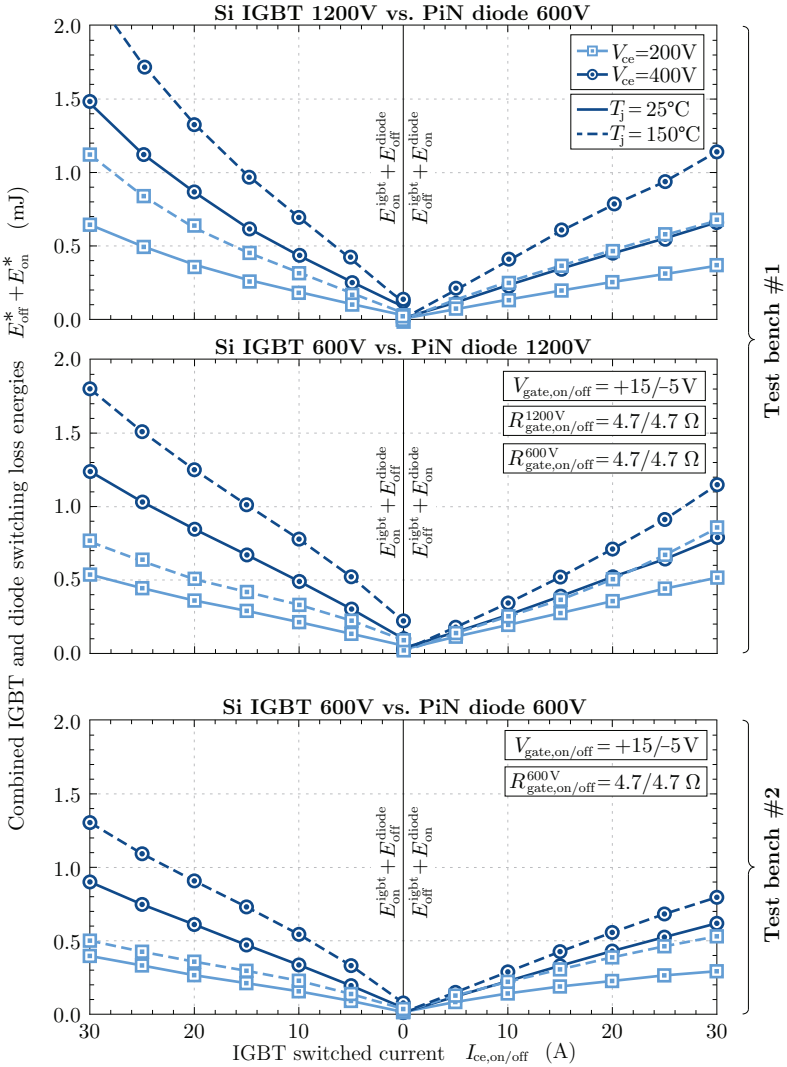


Fig. 3.3: Selection of the experimentally determined Si IGBT and Si PiN diode switching loss energies measured with the hardware setups depicted in **Fig. 3.2(a)** and **Fig. 3.2(b)** and inductive loads. The left-hand side of the figures shows the sum of IGBT turn-on and diode turn-off losses whereas the right-hand side shows the sum of IGBT turn-off and diode turn-on losses. The latter are mainly turn-off losses due to the tail current of the IGBTs. Further measurements were carried out at intermediate temperatures and voltages.

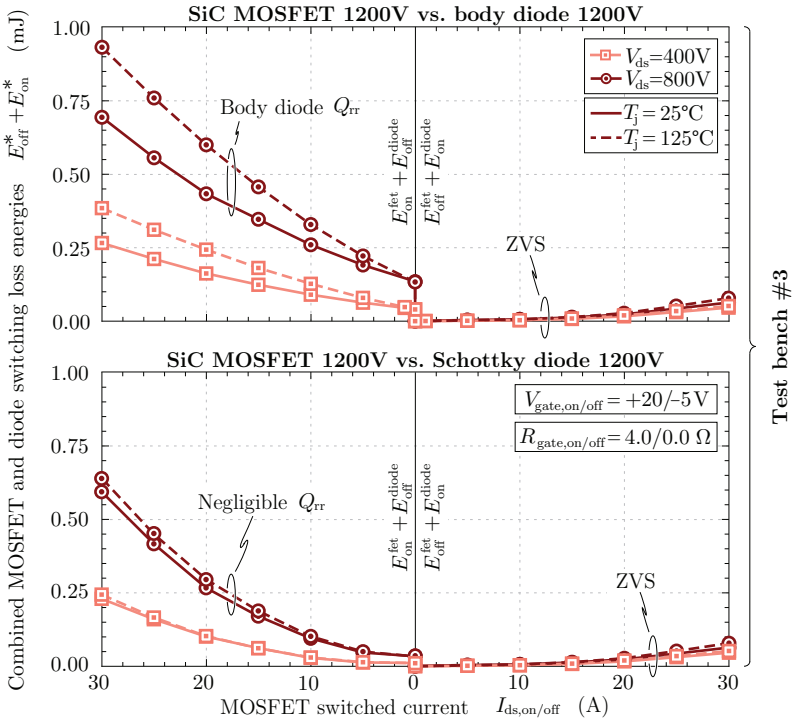


Fig. 3.4: SiC MOSFET and Schottky diode switching loss energies obtained with the test bench of **Fig. 3.2(c)** connected to an inductive load. The left-hand side of the figures shows the sum of MOSFET turn-on and diode turn-off losses whereas the right-hand side shows the sum of MOSFET turn-off and diode turn-on losses. Notable reverse recovery effects of the pn-junction body diode can be observed in hard turn-on switching transitions of the MOSFET where the current commutates from the body diode of the complementary switch (upper figure, left-hand side). For this type of commutation, the total losses show a similarly pronounced temperature-dependence as observed for the Si devices in **Fig. 3.3**. When replacing the complementary switch with a SiC Schottky diode, the reverse recovery-related losses and the temperature-dependence become insignificant (lower figure, left-hand side). The employed MOSFETs feature superior ZVS capabilities with very low turn-off losses and almost ideal, i.e. lossless charging/discharging of the parasitic output capacitors C_{oss} (right-hand side of the figures) Further measurements were carried out at intermediate temperatures and voltages.

mount and their impact on the switching transients becomes non-negligible.

- *Simulation*: it has been proposed to extract $E_{\mathrm{on/off}}$ from simulations (e.g. [88]). A prerequisite of this method to be accurate is the exact knowledge and modeling of all parasitics and gate driver and semiconductor characteristics. This information can often only be obtained by measurements. Mainly the temperature-dependent characteristics of the semiconductors are often difficult to model. Furthermore, it is desirable that the simulated $E_{\mathrm{on/off}}$ are experimentally verified using one of the other listed methods. The advantages of this simulative approach are that the simulations take only little time, that the sensitivities regarding the parasitics or other parameters can be investigated with ease and that highly dynamic switching transients can be accurately visualized and investigated.
- *Calorimetric measurement*: the loss energies $E_{\mathrm{on/off}}$ can be determined based on calorimetric measurements where the test bench is in continuous operation at a desired operating point as shown in [89]. The main benefits of this method are that the switching transitions are not influenced by the measurement and that high switching dynamics become irrelevant from the measurement point of view. The main challenges are the long time constants of this measurement method and the post-processing where other origins of the measured losses (mainly conduction losses) must be accurately known and deducted from the measurements. Furthermore, in contrast to the direct waveform measurement method, the junction temperatures are unknown due to the continuous operation and must therefore be estimated based on a thermal model.
- *Loss balance method*: if the hardware test bench implements a suitable topology, e.g. a DC/DC buck converter, the switching losses can also be determined by means of measuring the difference between input and output power, i.e. the total losses, for continuous operation in a desired operating point [89]. Provided that the losses of the remaining converter components are known, the switching losses can be determined.

In this thesis, mainly because of the manageable switching dynamics of the investigated semiconductors and thus because of the high attain-

able accuracy, all switching loss energies were measured utilizing the direct waveform measurement method. For this purpose, the hardware test benches of **Fig. 3.2** were implemented and used together with external inductive loads. The test benches feature single bridge legs of different combinations of semiconductors and topologies which are investigated in the case studies in Chapter 5 and Chapter 6. The selected layouts could be similarly implemented in complete converter systems. The layout and gate driver components of the SiC MOSFET test bench in **Fig. 3.2(c)** is largely identical to the layout and gate drivers of the prototype shown in Chapter 5.

A selection of the measured loss energies is depicted in **Fig. 3.3** and **Fig. 3.4**. The obtained Si IGBT and diode switching losses in **Fig. 3.3** are all in a similar range and mainly differ due to different combinations of 600 and 1200 V technologies. The commutations within the combinations 1200 V IGBT/600 V diode and 600 V IGBT/1200 V diode in the 3-level T-type bridge leg result in comparable losses whereas the commutations within the combination 600 V IGBT/600 V diode in the boost bridge leg feature moderately lower losses. Generally, a pronounced temperature-dependence of the switching loss energies can be observed which can be explained with the temperature-dependence of the stored charge. The SiC MOSFET and Schottky diode switching losses shown in **Fig. 3.4** are significantly smaller when compared to the Si counterparts for same currents and voltages. Whereas the turn-on losses (including reverse recovery effect in the commutating diode) are between 4 and 6 times lower, the turn-off losses are reduced by up to a factor 10. The latter emphasizes the superior zero voltage switching (ZVS) capabilities of these devices.

3.1.3 Incomplete ZVS Losses

The losses associated with incomplete zero voltage switching (iZVS) transitions are investigated in this section. In this work, iZVS refers to a switching transition with incomplete charging/discharging of the involved semiconductor output capacitances. In a first step, the requirements and fundamentals of complete ZVS are revisited. In a second step, the characteristics of incomplete ZVS are explained in more detailed and the associated losses are described by a suitable model. Finally, experimental verifications are presented which demonstrate the validity of the model. Note that the analysis in this section assumes

MOSFET devices as this type of semiconductors is typically employed when ZVS is exploited. The principles of ZVS can also be applied to bipolar IGBTs where, however, the reduction of the switching losses is far less significant than with unipolar MOSFETs [90].

Fundamentals of Complete ZVS

In hard turn-on switching transitions, the current commutates from the conducting (body) diode to the complementary MOSFET channel. Mainly because of the reverse recovery effect of the body diode high switching losses result in both devices which are involved in the switching transition. In order to avoid these losses, ZVS is commonly utilized where the current always commutates from the MOSFET channel to the (body) diode. Typical waveforms for ZVS are depicted in **Fig. 3.5**. ZVS requires the presence of an impressed current of an inductive component which charges/discharges the output capacitances of the MOSFETs within a bridge leg during the dead time of the associated gate signals, as visualized in **Fig. 3.5** for a transition where switch S_2 turns off and S_1 turns on. The required energy of the inductance for a complete soft-switching transition can be found by considering the energy balance of

$$E_{\text{initial}} + E_{\text{delivered}} = E_{\text{final}} + E_{\text{dissipated}} \,, \tag{3.7}$$

where E_{initial} denotes the energy within the system for $t < t_1$, and E_{final} denotes the energy after the ZVS transition. $E_{\text{delivered}}$ is the energy which is delivered by the source and $E_{\text{dissipated}}$ is the energy which is dissipated during the ZVS transition which is assumed to be $E_{\text{dissipated}} = 0$ for complete ZVS. Furthermore, it is assumed that the switches S_1 and S_2 in the half bridge are equal, which means that they exhibit the same non-linear characteristic of $C_{\text{oss}}(V_{\text{ds}})$. This is also typically the case in half bridge configurations with bidirectional power flow capability.

At the beginning of the transition ($t < t_1$), the current $i_L(t) \equiv I_1$ of the inductor is free-wheeling through S_2 and the output capacitance C_{oss1} of switch S_1 is charged to the source voltage V_{dc}. Assuming a linear inductance, the energy within the system for $t < t_1$ is therefore equal to

$$E_{\text{initial}} = E_{\text{oss}}(V_{\text{dc}}) + \frac{1}{2} L_\sigma I_1^2 \,. \tag{3.8}$$

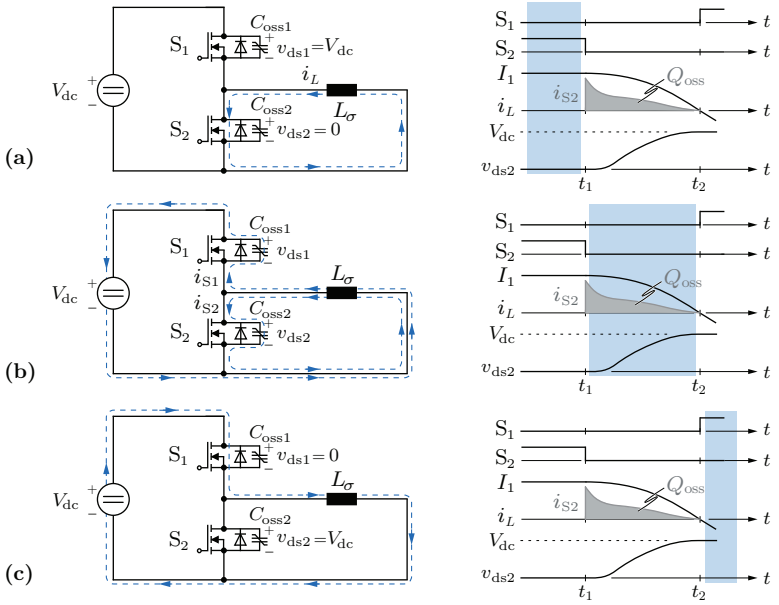


Fig. 3.5: Complete soft-switching transition of a MOSFET half bridge leg and an inductor L_σ. **(a)** Free-wheeling interval with inductor current $i_L = I_1$. **(b)** Switch S_2 turns off and a resonant transition starts with an additional current path through the DC source. **(c)** End of the transition when the drain-to-source voltage of S_2 has reached the source voltage, i.e. $v_{ds2} = V_{dc}$, and switch S_1 turns on at zero voltage.

During the switching transition ($t_1 < t < t_2$), the inductor and the capacitances of the switches form a resonant circuit. The current i_L is split between both capacitances and charges C_{oss2} and discharges C_{oss1}. If the charging/discharging is completed by the time t_2 at which S_1 is turned on, complete ZVS is achieved and the channel of S_1 turns on at zero voltage without causing losses. In the case of a complete ZVS transition at the boundary to loosing ZVS, the charging/discharging process is finished at the same time t_2 at which the inductor current reaches $i_L = 0\,\mathrm{A}$. The energy in the system after the ZVS transition equals

$$E_{\mathrm{final}} = E_{\mathrm{oss}}(V_{\mathrm{dc}})\,, \tag{3.9}$$

and the energy received by the source during the transition equals

$$E_{\text{delivered}} = -Q_{\text{oss}}(V_{\text{dc}}) \cdot V_{\text{dc}} \ , \tag{3.10}$$

since the charge of switch S_1 was moved by i_{S1} to the source with voltage V_{dc}. As a result, the energy balance of (3.7) reveals that the requirement for a complete ZVS transition is given by

$$\frac{1}{2} L_\sigma I_1^2 \geq Q_{\text{oss}}(V_{\text{dc}}) \cdot V_{\text{dc}} \ . \tag{3.11}$$

Please note that additional parasitic capacitances of the switch node (e.g. PCB capacitances and the parasitic capacitance of the inductor) also influence the required energy of the inductor for soft-switching. The parasitic capacitances are assumed to be linear with respect to their capacitance value in dependence of the applied voltage, which allows us to lump them into a total parasitic capacitance $C_{\text{par,tot}}$. Accordingly, considering **Fig. 3.5** the energy term $\frac{1}{2} C_{\text{par,tot}} V_{\text{dc}}^2$ has to be added to the right-hand side of (3.11).

Based on the above analysis, ideal ZVS can be defined as a switching transition where the condition (3.11) for a complete zero voltage transition is fulfilled and no energy is dissipated during the transition. In practice, however, even if the condition of complete ZVS (3.11) is fulfilled, switching losses still occur due to the two following non-ideal effects:

- At large inductor currents the snubber effect of the output capacitance C_{oss} of the turning off MOSFET may become too weak and non-negligible losses occur. From another viewpoint, this can also be described as the gate driver circuitry being too slow to turn off the MOSFET channel before the drain-to-source voltage v_{ds} rises. In either way, the resulting overlap of the current to be switched off and the rising v_{ds} cause turn-off switching losses in the semiconductor.
- The process of charging/discharging the output capacitances creates additional losses [91, 92]. For low-voltage Si MOSFETs, SiC MOSFETs and GaN HEMTs this effect is mainly of resistive nature and typically causes a dissipation of up to 10 % of the stored energy E_{oss} in the output capacitance. Note that the charging of the Miller capacitance as part of the output capacitance by the switched bridge leg current i_L occurs via the gate driver path.

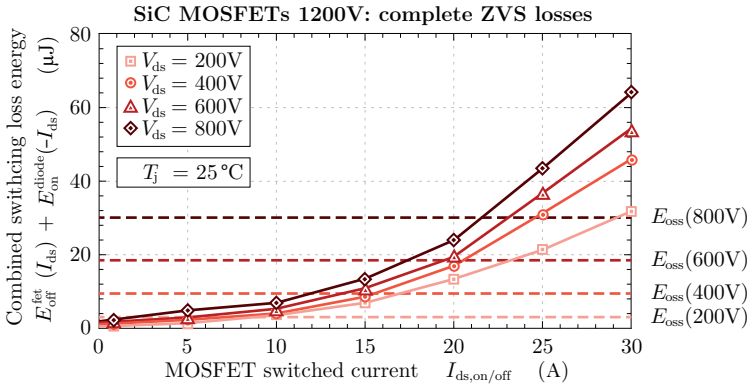


Fig. 3.6: Measured combined complete ZVS MOSFET turn-off and body diode turn-on switching loss energies using the SiC MOSFET C2M0080120D 2-level half bridge leg test bench shown in **Fig. 3.2(c)**. The data of this figure is also depicted in **Fig. 3.4**. It can be seen that at low currents most of the measured turn-off losses correspond to the stored energy in the parasitic output capacitor C_{oss}. This energy is fully released at turn-on (measured as negative energy) yielding nearly zero total losses ($< 10\,\%$ of E_{oss}). With increasing currents, non-zero total losses occur. This is mainly due to the finite turn-off speed of the gate driver which results in a rising drain-to-source voltage while the current through the MOSFET channel has not yet decayed to zero.

> Consequently, the gate resistor also contributes to the resistive losses. For super-junction (SJ) Si MOSFETs, the loss mechanism is a combination of a resistive and additionally a diode-like component and might dissipate more than 50 % of E_{oss} and thus contributes to significant switching losses despite complete ZVS.

The above listed non-idealities are exemplified in **Fig. 3.6** which shows measured switching losses for complete ZVS operation using the 2-level SiC MOSFET test bench of **Fig. 3.2(c)**.

Incomplete ZVS Loss Model

Apart from the losses due to the MOSFET non-idealities, additional losses result if the condition for complete ZVS (3.11) is not fulfilled. In this thesis, such a switching transition is referred to as *incomplete*

ZVS (iZVS). iZVS is characterized by a residual voltage ΔV across the turning on switch. A residual voltage can either occur if the energy in L_σ is too low to fulfill (3.11) or if the dead time T_d is too short to accomplish the complete charging/discharging during the dead time T_d of the gate signals as depicted in **Fig. 3.7**. These resulting iZVS losses can be directly measured and incorporated into the switching loss energies employing one of the above listed switching loss measurement methods. However, this straightforward approach implies a considerably higher effort as the measurements must not only be repeated for different currents, voltages and temperatures but also for different values of ΔV. Therefore, a theoretical modeling approach is presented here which does not require more measured data than already shown in **Fig. 3.6**.

In order to calculate the remaining voltage ΔV at the end of the dead time interval T_d (cf. **Fig. 3.7**) , the energy expression E_final has to be revised to

$$E_\mathrm{final} = E_\mathrm{oss}(V_\mathrm{dc} - \Delta V) + E_\mathrm{oss}(\Delta V) \,, \tag{3.12}$$

and the energy delivered by the source has to be changed to

$$E_\mathrm{delivered} = -Q_\mathrm{oss}(V_\mathrm{dc} - \Delta V) \cdot V_\mathrm{dc} \,. \tag{3.13}$$

The value of ΔV can then be found by solving the energy balance of (3.7) (again for $E_\mathrm{dissipated} = 0$). Please note that additional parasitic capacitances are not included in this equation. In the iZVS transition, switch S_1 turns on while C_oss1 is still charged to ΔV. This dissipates a certain amount of energy during T_iZVS as depicted in **Fig. 3.7** that can be derived by solving the energy balance of

$$E_\mathrm{diss,iZVS} = E_\mathrm{initial,iZVS} - E_\mathrm{final,iZVS} + E_\mathrm{delivered,iZVS} \,. \tag{3.14}$$

Before S_1 turns on, the energy within the system is equal to

$$E_\mathrm{initial,iZVS} = E_\mathrm{oss}(V_\mathrm{dc} - \Delta V) + E_\mathrm{oss}(\Delta V) \,. \tag{3.15}$$

After S_1 has turned on, C_oss2 of switch S_2 is charged to V_dc, therefore

$$E_\mathrm{final,iZVS} = E_\mathrm{oss}(V_\mathrm{dc}) \,. \tag{3.16}$$

In order to charge the output capacitance of S_2 to V_dc, the remaining charge

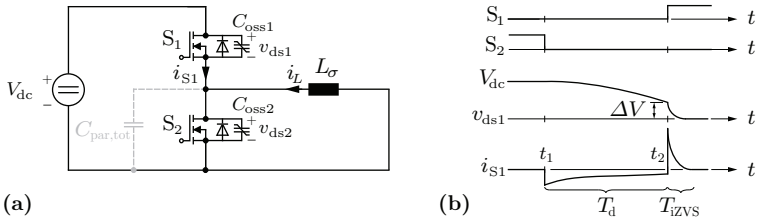


Fig. 3.7: Incomplete ZVS transition of a MOSFET half bridge leg and an inductor L_σ. **(a)** Considered circuit including the non-linear output capacitances C_{oss} and a lumped layout-specific parasitic capacitance $C_{par,tot}$ to study the energy balance for a switching transition where S_1 turns on at a non-zero residual drain-to-source voltage $v_{ds1} = \Delta V$. **(b)** The evolution of the schematic waveforms can be split into the dead time interval (T_d) where energy is recovered from S_1 and a dissipative phase (T_{iZVS}) which occurs when switch S_1 is turned on at non-zero $v_{ds1} = \Delta V$.

$$\Delta Q_{S2} = Q_{oss}(V_{dc}) - Q_{oss}(V_{dc} - \Delta V)\ , \tag{3.17}$$

has to be taken from the source; accordingly the source delivers the energy

$$E_{\text{delivered, iZVS}} = \Delta Q_{S2} \cdot V_{dc}\ . \tag{3.18}$$

As a result, the dissipated energy of the iZVS transition in switch S_1 during T_{iZVS} can be derived and interpreted as

$$\begin{aligned} E_{diss,iZVS} = & \underbrace{E_{oss}(\Delta V)}_{\text{(i) Dissipation of residual energy in } C_{oss1}} \\ & + \underbrace{\Delta Q_{S2} \cdot V_{dc}}_{\text{(ii) Energy provided by source during } T_{iZVS}} \\ & - \underbrace{\big(E_{oss}(V_{dc}) - E_{oss}(V_{dc} - \Delta V)\big)}_{\text{Share of energy of (ii) which is stored in } C_{oss2}}\ . \end{aligned} \tag{3.19}$$

For the case of a complete ZVS transition (i.e. $\Delta V \to 0\,\text{V}$) the above equation yields $E_{diss,iZVS} \to 0\,\text{J}$ whereas the result for no resonant transition (i.e. $\Delta V \to V_{dc}$) is $E_{diss,iZVS} \to Q_{oss}(V_{dc}) \cdot V_{dc}$. Note again that

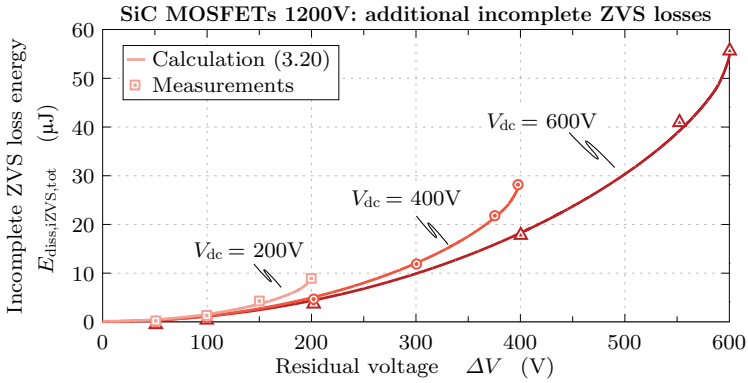


Fig. 3.8: Experimental verification of the switching energies for incomplete ZVS conditions. The measurement setup of **Fig. 3.2(c)** was used of which the equivalent circuit and schematic waveforms are shown in **Fig. 3.7**. The circuit includes two SiC MOSFETs in a 2-level half bridge leg configuration switching an inductive load and a lumped layout-specific parasitic capacitance $C_{\mathrm{par,tot}}$. The figure shows the measured dissipated energy $E_{\mathrm{diss,iZVS,tot}}$ due to incomplete ZVS for different DC-link voltages V_{dc} and different residual voltages ΔV in comparison to the calculated values according to (3.20). The observed agreement between measurement and calculation is very good with a maximum error of $< 5\,\%$.

non-idealities (turn-off losses, charging/discharging losses of C_{oss}) resulting in additional losses are not included in the equations and must hence be separately calculated as regular switching losses based on the data of **Fig. 3.6**.

Experimental Verification

In order to verify the derived formula for iZVS loss energies, measurements were conducted using the test bench of **Fig. 3.2(c)**. The experimental setup includes two SiC MOSFETs in a 2-level half bridge leg configuration which have an almost ideal soft-switching behavior if the switched currents are low (cf. **Fig. 3.6**). Accordingly the losses of the charging and discharging process of C_{oss} can be neglected. The experimental setup contains a specific layout-dependent parasitic capacitances (e.g., probes, PCB) that are included in the calculation by means of a lumped capacitance. It was measured to amount to $C_{\mathrm{par,tot}} = 123\,\mathrm{pF}$.

The residual energy stored in the parasitic capacitances is also dissipated in switch S_1 and has to be included in the calculations, which yields

$$E_{\text{diss,iZVS,tot}} = E_{\text{diss,iZVS}} + \frac{1}{2} C_{\text{par,tot}} \Delta V^2 \ . \tag{3.20}$$

It can be shown that due to the linearity of the parasitic capacitance, the additional losses due to $C_{\text{par,tot}}$ are independent from whether $C_{\text{par,tot}}$ is lumped in parallel to S_1 or in parallel to S_2 in **Fig. 3.7**.

The measurements of the iZVS losses were conducted for different levels of the DC-link voltage V_{dc} and different levels of residual voltages ΔV. The results are depicted in **Fig. 3.8**. The theory is confirmed by the measurements which show a high accuracy where the maximum observed error is $< 5\,\%$.

3.1.4 Thermal Modeling

The thermal model for semiconductors in this thesis is depicted in **Fig. 3.9**. The heat flow from the semiconductors to the ambient is modeled with static equivalent thermal resistances. The junction temperature $T_{\text{j},x}$ of a semiconductor chip can be calculated with,

$$\begin{aligned} T_{\text{j},x} =& R_{\text{th,j-c},x} \cdot P_{\text{SC},x} \\ &+ R_{\text{th,c-hs},x} \cdot \sum_{i=1}^{N_{\text{co}}} P_{\text{SC},i} + R_{\text{th,hs-amb}} \cdot \sum_{i=1}^{N_{\text{cs}}} P_{\text{SC},i} + T_{\text{amb}} \ , \end{aligned} \tag{3.21}$$

where N_{co} is the number of chips in the same package and N_{cs} the number of semiconductor chips on the same cooling system. $R_{\text{th,j-c},x}$, $R_{\text{th,c-hs},x}$ and $R_{\text{th,hs-amb}}$ denote the junction-to-case, case-to-heat sink and heat sink-to-ambient thermal resistances. Note that the model assumes homogeneous package and heat sink temperatures due to the high heat conductivity of the employed copper lead frame of the packages [93] and the typical base materials (e.g. aluminum) of the heat sink. Contrarily, no thermal interaction between the packages via the insulation pad is assumed due to its comparably high specific thermal resistance and thin geometry which results in a weak heat spreading. The losses $P_{\text{SC},x}$ represent the sum of conduction, switching and iZVS (if applicable) losses of the respective semiconductor chip.

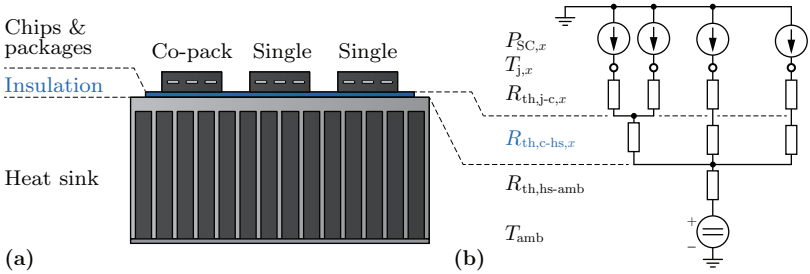


Fig. 3.9: Proposed thermal model to compute the semiconductor junction temperature $T_{\mathrm{j},x}$. **(a)** Co-pack and single semiconductor chips in discrete packages on a common heat sink and insulating pad. **(b)** Assumed equivalent thermal resistance circuit. The circuit is composed of the loss power sources $P_{\mathrm{SC},x}$ of the individual semiconductor chips, the junction-to-chase, case-to-heat sink and heat sink-to-ambient thermal resistances $R_{\mathrm{th,j\text{-}c},x}$, $R_{\mathrm{th,c\text{-}cs},x}$ and $R_{\mathrm{th,hs\text{-}amb}}$, respectively. IGBTs and anti-parallel diodes usually come in co-packs. Note that modules can be similarly treated as co-packs.

Parametrization

The junction-to-case parameters $R_{\mathrm{th,j\text{-}c},x}$ of the proposed thermal model (3.21) can be found in the respective data sheets of the semiconductors. The thermal resistance of the insulation pad is a function of the thermal conductivity $\lambda_{\mathrm{th,iso}}$ and thickness d_{iso} of the insulation pad, the area of the metal back of the semiconductor package A_{pack} and the quality of the contacts from the pad to the package and the heat sink. Mainly due to the latter [94], the simplified formula

$$R_{\mathrm{th,c\text{-}cs}} = \frac{d_{\mathrm{iso}}}{\lambda_{\mathrm{th,iso}} \cdot A_{\mathrm{pack}}} \,, \tag{3.22}$$

usually results in too optimistic estimations. In this thesis, the phase change insulation material Hi-Flow 300P from Bergquist is considered [95]. Based on measurements, a total thermal resistance of

$$R_{\mathrm{th,c\text{-}hs}}^{\text{TO-220}} = 0.94\,\mathrm{K/W} \,, \tag{3.23}$$

is stated in the data sheet. It is thus proposed to scale the thermal resistance of the pad for other packages with the area of the metal backs, i.e.

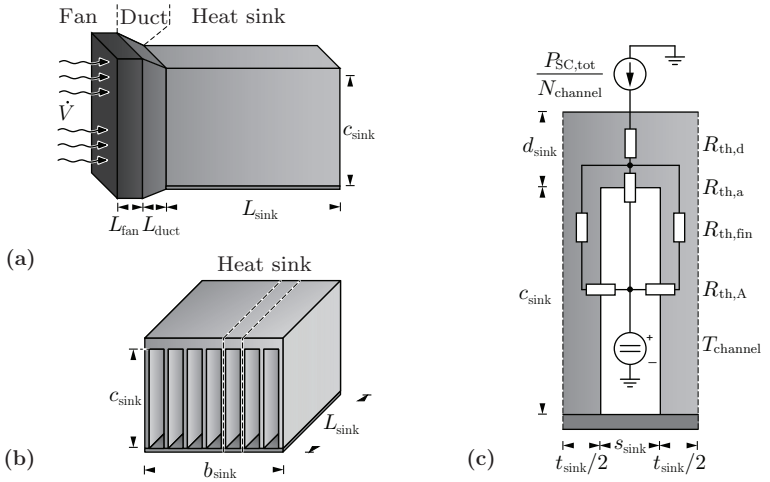


Fig. 3.10: Geometry of the considered cooling systems. **(a)** Fan and air duct attached to a heat sink with bottom plate to prevent airflow bypass. **(b)** Outer dimensions of the heat sink and marked symmetry axes for the thermal model. **(c)** Heat sink thermal model. Due to symmetry properties, only two half-fins with thicknesses $t_{\text{sink}}/2$ and one channel with height c_{sink} and width s_{sink} need to be analyzed. $P_{\text{SC,tot}}$ is the total losses of all semiconductor chips on the heat sink.

$$R^{\text{y}}_{\text{th,c-hs}} = R^{\text{TO-220}}_{\text{th,c-hs}} \cdot \frac{A^{\text{TO-220}}_{\text{pack}}}{A^{\text{y}}_{\text{pack}}} = 0.94\,\text{K/W} \cdot \frac{115\,\text{mm}^2}{A^{\text{y}}_{\text{pack}}} \,. \tag{3.24}$$

Using (3.24), the thermal resistance for a TO-247 package can be estimated to

$$R^{\text{TO-247}}_{\text{th,c-hs}} = 0.57\,\text{K/W} \,. \tag{3.25}$$

Finally, the calculation of the thermal resistance of the heat sink to the ambient $R_{\text{hs-amb}}$ is detailed in the next section.

3.2 Cooling Systems

The modeling framework for the cooling system design which is used in this thesis is derived and presented in [96]. The models of the framework

enable the calculation of the equivalent thermal resistance from the heat sink to the ambient $R_{\text{th,hs-amb}}$ as required in the thermal model (3.21) of the semiconductors. The modeling of a cooling system as depicted in **Fig. 3.10** involves two steps:

(i) *Fluid dynamics problem*: for a given fan and a defined heat sink geometry as shown in **Fig. 3.10(a)** and **Fig. 3.10(b)**, the resulting volume flow $\dot{V}$ must be determined first.

(ii) *Thermodynamics problem*: the thermal resistance characteristic of the heat sink is a function of the volume flow $\dot{V}$ of the cooling fluid flowing through the system shown in **Fig. 3.10(c)**. Consequently, knowing $\dot{V}$ permits the calculation of the equivalent thermal resistance $R_{\text{th,hs-amb}}$ of the heat sink.

Both steps and involved models are summarized in short below and illustrated in **Fig. 3.11** whereas a more detailed description can be found in [96].

3.2.1 Fluid Dynamics Model

The purpose of the fluid dynamics model is the determination of the volume flow $\dot{V}$ which represents the essential input variable to the thermodynamics model. The modeling effort mainly concerns the calculation of the fluid dynamic system impedance characteristic $\Delta p_{\text{tot}}(\dot{V})$ of the heat sink. Δp_{tot} correlates the static pressure difference between the fluid inlet and outlet of the heat sink to the volume flow $\dot{V}$. The function Δp_{tot} depends on the duct and heat sink geometry (cf. **Fig. 3.10(a)** and **Fig. 3.10(b)**) and a range of empirically found parameters and factors. After calculating $\Delta p_{\text{tot}}(\dot{V})$ for a given duct and heat sink geometry, the volume flow $\dot{V}$ can be determined by solving

$$\Delta p_{\text{tot}}(\dot{V}) - \Delta p_{\text{fan}}(\dot{V}) = 0 \,. \tag{3.26}$$

The static pressure drop versus volume flow characteristic $\Delta p_{\text{fan}}(\dot{V})$ of the selected fan is usually given in the respective data sheet.

3.2.2 Thermodynamics Model

The thermodynamics model is utilized to estimate the thermal resistance $R_{\text{th,hs-amb}}$ from the heat sink base plate to the ambient. The 3D

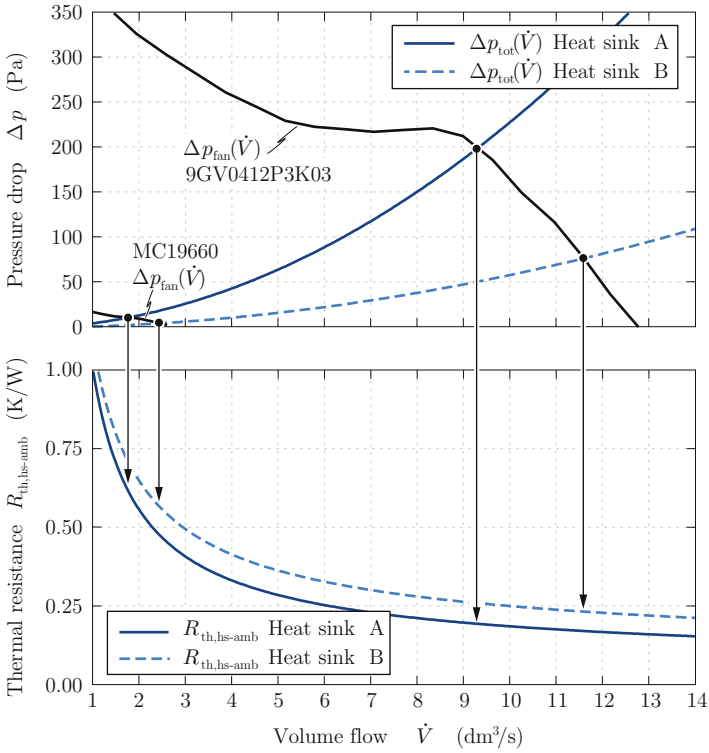


Fig. 3.11: Basic cooling system design process: the intersections of the heat sink impedances $\Delta p_{\mathrm{tot}}(\dot{V})$ of the heat sinks A and B with the characteristic of the selected fan determine the operating points, i.e. the volume flows $\dot{V}$ and the equivalent thermal resistances $R_{\mathrm{th,hs\text{-}amb}}$. The heat sink geometries {A, B} are: $N_{\mathrm{channel}} = \{13, 9\}$, $c_{\mathrm{sink}} = \{25, 36\}$ mm, $L_{\mathrm{sink}} = 100$ mm, $b_{\mathrm{sink}} = 40$ mm, $d_{\mathrm{sink}} = 4$ mm and $t_{\mathrm{sink}} = 1$ mm (cf. **Fig. 3.10**).

heat conduction problem is modeled with the thermal resistance network depicted in **Fig. 3.10(c)** where the symmetry of the heat sink channels and fins is exploited. It is assumed that the total semiconductor power loss $P_{\mathrm{SC,tot}}$ is uniformly distributed across the heat sink base plate area $A_{\mathrm{hs}} = b_{\mathrm{sink}} \cdot L_{\mathrm{sink}}$. The desired value $R_{\mathrm{th,hs\text{-}amb}}$ can be calculated with

$$R_{\mathrm{th,hs\text{-}amb}} = R_{\mathrm{th,d}} + R_{\mathrm{th,conv}} \ , \tag{3.27}$$

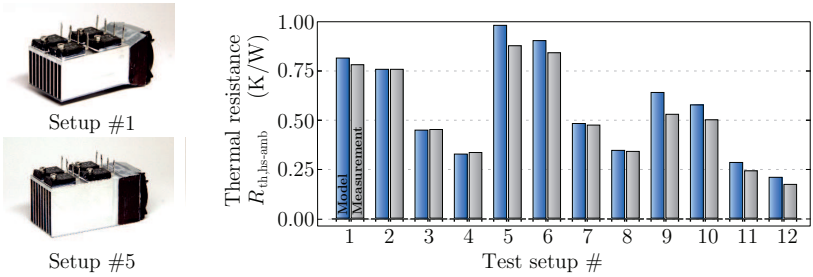


Fig. 3.12: Experimental verification presented in [96] of the employed fluid dynamics and thermodynamics models to design the cooling systems. The measurements of different setups showed a mean deviation of 8 % between the experiments and the model predictions.

where $R_{\mathrm{th,d}}$ is the thermal resistance of the heat sink base plate as depicted in **Fig. 3.10**,

$$R_{\mathrm{th,d}} = \frac{d_{\mathrm{sink}}}{A_{\mathrm{hs}} \cdot \lambda_{\mathrm{hs}}} \,, \tag{3.28}$$

with λ_{hs} being the thermal conductivity of the assumed heat sink's base material (in this work: aluminum). In (3.27), $R_{\mathrm{th,conv}}$ models the thermal resistances $R_{\mathrm{th,fin}}$, $R_{\mathrm{th,A}}$ and $R_{\mathrm{th,a}}$ and the channel temperature T_{channel} along the longitudinal axis of the channel by means of the single fluid heat exchanger model,

$$R_{\mathrm{th,conv}}(\dot{V}) = \left[\rho_{\mathrm{air}}\, c_{\mathrm{air}}\, \dot{V} \cdot \left(1 - \mathrm{e}^{-\frac{h \cdot A_{\mathrm{eff}}}{\rho_{\mathrm{air}}\, c_{\mathrm{air}}\, \dot{V}}}\right) \right]^{-1} . \tag{3.29}$$

The model input is the volume flow $\dot{V}$ from the fluid dynamics model. The parameters ρ_{air} and c_{air} denote the density and thermal capacitance of air. A_{eff} is the effective convective surface area which depends on the heat sink geometry and λ_{hs}. The heat transfer coefficient h can be estimated based on empirically obtained parameters and factors including the Nusselt, Prandtl and Reynolds number.

3.2.3 Experimental Verification

The presented fluid dynamics and thermodynamics models have been verified in [96] by means of a set of different cooling systems. The

thermal resistances $R_{\text{th,hs-amb}}$ of the implemented cooling systems were experimentally determined and then compared to the predictions of the models. The measurement results of [96] are depicted in **Fig. 3.12**. The observed mean error between measurement and model prediction is 8 %. Due to this very good agreement, the modeling framework proposed in [96] was incorporated into the cooling system design routine presented in Section 2.2.

3.3 Magnetics

The accurate modeling of magnetic components is a challenging task which involves reluctance models, loss models and thermal models. This section identifies suitable and experimentally verified reluctance and winding models from literature and derives new models for the core losses and the thermal modeling. Since magnetics are often critical components in a converter regarding size and costs, special effort was undertaken to perform own experimental verifications of the selected models and the proposed design routine presented in Section 2.2.

The following descriptions refer to the modeling of an inductor with a single winding and an E-core geometry as shown in **Fig. 3.13** but can equivalently be applied to other geometries and magnetic components such as transformers.

3.3.1 Reluctance Model

The core reluctance in conjunction with an impressed flux Φ_L due to an inductor current i_L is described with the model,

$$N_{\text{wdg}} \cdot i_L = \Phi_L \cdot \left[R_{\text{mag,core}} \left(\frac{\Phi_L}{k_{\text{fill}} A_{\text{core}}} \right) + R_{\text{mag,ag}} \right] , \tag{3.30}$$

where N_{wdg} is the number of winding turns. The above model is non-linear due to the non-linear dependency of the core reluctance $R_{\text{mag,core}}$ from the flux density $B = \frac{\Phi_L}{k_{\text{fill}} A_{\text{core}}}$,

$$R_{\text{mag,core}}(B) = \frac{l_{\text{mag,core}}}{\mu_0 \, \mu_{\text{r}}(B) \, k_{\text{fill}} A_{\text{core}}} . \tag{3.31}$$

The product $k_{\text{fill}} \, A_{\text{core}}$ denotes the effective core cross section taking into account the core filling factor (mainly relevant for laminated cores). μ_{r}

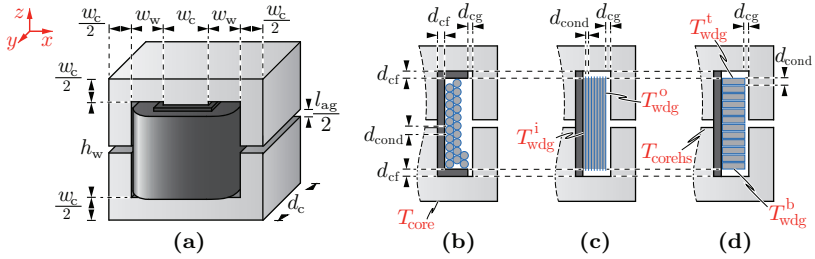


Fig. 3.13: Example inductor geometry. **(a)** Symmetric E-core geometry with equal air gap lengths for all legs, center leg width w_c, core depth d_c, total air gap length l_{ag}, window width w_w and window height h_w. **(b)** Round and litz wire winding geometry with conductor diameter (copper and insulation) d_{cond}, coil former with constant thickness d_{cf} and gap between core and winding d_{cg}. **(c)** Foil and **(d)** flat wire winding geometry with equal gaps to the core as for round/litz wire. The figure furthermore depicts the location of the modeled temperatures of the thermal network model in **Fig. 3.18**.

represents the non-linear relative core permeability expressed as a function of the flux density B. Details on the employed approach on how to accurately calculate the magnetic path length $l_{mag,core}$ including the treatment of the core corner sections can be found in [97]. The reluctance of the air gaps $R_{mag,ag}$ is calculated based on a 3D application of the Schwartz-Christoffel-transformation which takes into account the 3D core geometry and gives accurate results also for large relative air gap lengths. Formulas and experimental verifications can be found in [98, 99].

The non-linear permeability $\mu_r(B)$ can usually be extracted from the B-H curves of the core material data sheets. μ_r is often not only dependent from the flux density but also the core temperature or the frequency. These effects are, however, not modeled in this thesis. Especially the frequency-dependency is often only relevant at very high frequencies at which the material is not intended to be operated.

3.3.2 Winding Losses

Using Maxwell's equations, it can be shown that the general solution for the area losses (per length) of a single conductor x within an inductor winding bundle with arbitrary shapes and conducting a sinusoidal current with frequency f and amplitude $\hat{I}_{L(f)}$ is always of the form

$$P^{x}_{\mathrm{wdg}}(T_{\mathrm{wdg}}, f) = R^{*}_{\mathrm{dc}}(T_{\mathrm{wdg}}) \cdot X^{*}\left(\xi^{*}(T_{\mathrm{wdg}}, f)\right) \cdot \hat{I}^{2}_{L(f)} \,, \tag{3.32}$$

where R^{*}_{dc} is the conductor's DC resistance per length depending on the winding temperature T_{wdg}. X^{*} denotes a function which depends on the geometries of the conductor x and the winding bundle. For the different winding types, different approaches were chosen to determine the unknown geometry-dependent function X^{*} in (3.32).

Solid Round and Litz Wire

For solid round and litz wire conductors, well-known and tractable analytical solutions for X^{*} exist based on 1D field approximations (e.g. [97, 98]). The solutions distinguish between skin and proximity effect losses. The solution for X^{*} for round wires is

$$X^{\mathrm{ro}}(\xi^{\mathrm{ro}}) = F^{\mathrm{ro}}_{\mathrm{skin}}(\xi^{\mathrm{ro}}) + G^{\mathrm{ro}}_{\mathrm{prox}}(\xi^{\mathrm{ro}}) \cdot \overline{H}^{2}_{\mathrm{ext}(f)} \,, \tag{3.33}$$

with

$$F^{\mathrm{ro}}_{\mathrm{skin}}(\xi^{\mathrm{ro}}) = \frac{\xi^{\mathrm{ro}}}{4\sqrt{2}} \left[\frac{\mathrm{Ber}_0(\xi^{\mathrm{ro}})\mathrm{Bei}_1(\xi^{\mathrm{ro}}) - \mathrm{Ber}_0(\xi^{\mathrm{ro}})\mathrm{Ber}_1(\xi^{\mathrm{ro}})}{\mathrm{Ber}_1(\xi^{\mathrm{ro}})^2 + \mathrm{Bei}_1(\xi^{\mathrm{ro}})^2} - \frac{\mathrm{Bei}_0(\xi^{\mathrm{ro}})\mathrm{Ber}_1(\xi^{\mathrm{ro}}) - \mathrm{Bei}_0(\xi^{\mathrm{ro}})\mathrm{Bei}_1(\xi^{\mathrm{ro}})}{\mathrm{Ber}_1(\xi^{\mathrm{ro}})^2 + \mathrm{Bei}_1(\xi^{\mathrm{ro}})^2} \right] , \tag{3.34}$$

and

$$G^{\mathrm{ro}}_{\mathrm{prox}} = - \frac{\xi^{\mathrm{ro}} \pi^2 d^2_{\mathrm{cond,cop}}}{2\sqrt{2}} \left[\frac{\mathrm{Ber}_2(\xi^{\mathrm{ro}})\mathrm{Bei}_1(\xi) - \mathrm{Bei}_2(\xi^{\mathrm{ro}})\mathrm{Ber}_1(\xi^{\mathrm{ro}})}{\mathrm{Ber}_0(\xi^{\mathrm{ro}})^2 + \mathrm{Bei}_0(\xi^{\mathrm{ro}})^2} - \frac{\mathrm{Bei}_2(\xi^{\mathrm{ro}})\mathrm{Bei}_1(\xi^{\mathrm{ro}}) - \mathrm{Bei}_2(\xi^{\mathrm{ro}})\mathrm{Ber}_1(\xi^{\mathrm{ro}})}{\mathrm{Ber}_0(\xi^{\mathrm{ro}})^2 + \mathrm{Bei}_0(\xi^{\mathrm{ro}})^2} \right] , \tag{3.35}$$

where

$$\xi^{\mathrm{ro}}(T_{\mathrm{wdg}}, f) = \frac{d_{\mathrm{cond,cop}}}{\sqrt{2}\,\delta_{\mathrm{cop}}(T_{\mathrm{wdg}}, f)} = d_{\mathrm{cond,cop}} \cdot \sqrt{\frac{\pi f \mu_0\, \sigma_{\mathrm{cop}}(T_{\mathrm{wdg}})}{2}} \,. \tag{3.36}$$

$\sigma_{\mathrm{cop}}(T_{\mathrm{wdg}})$ is the temperature-dependent electrical conductivity of copper and $d_{\mathrm{cond,cop}}$ is the conductor copper diameter. The n^{th} order

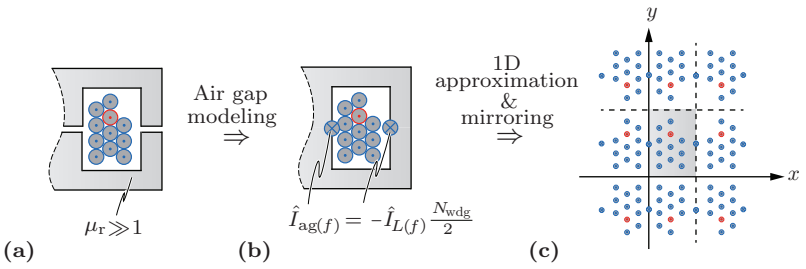


Fig. 3.14: Method of images (mirroring) used for the calculation of the normalized external fields $\overline{H}_{ext(f)}$ in round and litz wire windings. **(a)** Round wire winding inside the winding window. **(b)** The fringing field of the air gaps can be modeled with equivalent currents generating a similar field distribution. **(c)** The impact of the core material ($\mu_r \gg 1$, e.g. $\mu_r > 20$) is imitated by mirrored conductors. The individual conductors are modeled as point-currents (1D approximation) and the external field $\overline{H}_{ext(f)}$ in the center of a conductor of interest can be calculated with (3.38). The mirroring can be repeated in order to improve the accuracy. In this work, three mirroring steps are performed. The mirroring approach must separately be employed for the part of the winding which is outside the winding window where different magnetic fields will result than inside window.

Kelvin functions $\mathrm{Ber}_n(\xi)$ and $\mathrm{Bei}_n(\xi)$ are obtained from the n^{th} order Bessel function $\mathrm{J}_n(\xi)$: $\mathrm{Ber}_n(\xi) = \mathrm{Re}[\mathrm{J}_n(\xi e^{\mathrm{j}\cdot 3\pi/4})]$ and $\mathrm{Bei}_n(\xi) = \mathrm{Im}[\mathrm{J}_n(\xi e^{\mathrm{j}\cdot 3\pi/4})]$. The DC resistance per length of round conductors can be calculated with

$$R'^{\mathrm{ro}}_{\mathrm{DC}}(T_{\mathrm{wdg}}) = \frac{4}{\pi\, \sigma_{\mathrm{cop}}(T_{\mathrm{wdg}})\, d^2_{\mathrm{cond,cop}}} \,. \tag{3.37}$$

The required normalized external field amplitude $\overline{H}_{ext(f)}$ in (3.33) at the position $\vec{r}$ of conductor x can be approximated by means of a superposition of all occurring fields at this position,

$$\overline{H}_{ext(f)}(\vec{r}) = \frac{1}{\hat{I}_{L(f)}} \cdot \left| \sum_{i=1}^{N^*} \vec{H}_{i(f)}(\vec{r}) \right| . \tag{3.38}$$

The N^* field sources result from the $(N_{\mathrm{wdg}} - 1)$ currents in the neighboring winding turns and the fringing fields of the air gaps as shown in **Fig. 3.14(b)**. In order to accurately predict the resulting fields, the

method of images (mirroring, [97]) is employed. It accurately takes into account the impact of the air gap fringing fields and the core material as shown in **Fig. 3.14(c)** on $\overline{H}_{\mathrm{ext}(f)}$. A 2D finite element method (FEM) analysis has revealed that the main assumption of the method of images, namely the assumption of a core material with infinite permeability is in practice sufficiently met if $\mu_{\mathrm{r}} > 20$.

The solution for X^* for litz wires is

$$X^{\mathrm{li}}(\xi) = F^{\mathrm{li}}_{\mathrm{skin}}(\xi) + G^{\mathrm{li}}_{\mathrm{prox}}(\xi) \cdot (\overline{H}^2_{\mathrm{int}(f)} + \overline{H}^2_{\mathrm{ext}(f)}) \,, \tag{3.39}$$

with

$$F^{\mathrm{li}}_{\mathrm{skin}}(\xi^{\mathrm{li}}) = F^{\mathrm{ro}}_{\mathrm{skin}}(\xi^{\mathrm{li}}) \,, \tag{3.40}$$

$$G^{\mathrm{li}}_{\mathrm{prox}}(\xi^{\mathrm{li}}) = N^2_{\mathrm{strand}} \cdot G^{\mathrm{ro}}_{\mathrm{prox}}(\xi^{\mathrm{li}}) \,, \tag{3.41}$$

with N_{strand} being the number of strands and

$$\xi^{\mathrm{li}}(T_{\mathrm{wdg}}, f) = \frac{d_{\mathrm{strand,cop}}}{d_{\mathrm{cond,cop}}} \cdot \xi^{\mathrm{ro}}(T_{\mathrm{wdg}}, f) \,, \tag{3.42}$$

where $d_{\mathrm{strand,cop}}$ is the copper diameter of a single strand. The DC resistance per length of litz wires calculates as

$$R^{\mathrm{li}}_{\mathrm{DC}}(T_{\mathrm{wdg}}) = \frac{1}{N_{\mathrm{strand}}} \cdot \frac{4}{\pi \, \sigma_{\mathrm{cop}}(T_{\mathrm{wdg}}) \, d^2_{\mathrm{strand,cop}}} \,. \tag{3.43}$$

In a single strand of a litz wire proximity losses are not only caused by the surrounding conductors but also the surrounding strands. The corresponding normalized inner magnetic field causing the inner proximity losses can be calculated with

$$\overline{H}_{\mathrm{int}(f)} = \frac{1}{2\pi^2 d^2_{\mathrm{cond,cop}}} \,. \tag{3.44}$$

The external field $\overline{H}_{\mathrm{ext}(f)}$ can again be estimated with (3.38) and the mirroring approach shown in **Fig. 3.14**.

Flat and Foil Windings

Investigations (e.g. found in [97, 98]) show that an accurate analytical determination of X^* is highly challenging for foil and flat wire geometries. This is mainly due to the fact that the magnetic fields on spatially

extended foil and flat windings cannot accurately be described with 1D approximations. As a consequence, a pragmatic and more accurate approach based on FEM simulations was pursued where X^* is modeled by means of interpolated FEM results. Note that the FEM simulations must only sweep over a few *relative* geometric parameters and a sufficiently wide range of frequencies, as the relationship between f, T_{wdg} and $d_{\mathrm{cond,cop}}$ is known with (3.36). This reduces the computational effort by $\mathcal{O}(n^2)$. The statistical mean error introduced by the interpolation approach for foil and flat wire conductors is below 3 % with maximum errors of 20 % in special cases. Note that no extrapolation was necessary for all results shown in this work.

An alternative approach for the calculation of the winidng losses in foil and flat wire windings was presented in [100]. In contrast to the method described above which relies on off-line, i.e. previously carried out FEM simulations and subsequent interpolation, the method in [100] calculates each problem/geometry on-line based on the partial element equivalent circuit (PEEC) method. Although a high accuracy can be achieved with this method, the computational effort was considered too high for the type of optimizations carried out in this work.

Calculation of the Winding Losses

The winding losses must be calculated for each winding turn x separately due to varying external magnetic fields. Furthermore, for the individual turns x it must be distinguished between the part of the turn inside the core window and the part outside the window as again different magnetic fields apply. Due to the frequency-dependency of (3.32), the overall losses are the sum of the losses caused by each harmonic of the spectrum of the inductor current $\sum \hat{I}_{L(n)}$. The spectrum is provided by the behavioral models. The formula for the losses of an entire inductor winding yields to

$$P_{\mathrm{wdg}}(T_{\mathrm{wdg}}) = \sum_{n} \sum_{x=1}^{N_{\mathrm{wdg}}} P_{\mathrm{wdg}}^{x,\mathrm{i}}(T_{\mathrm{wdg}}, f_n) \cdot l_{\mathrm{wdg}}^{x,\mathrm{i}} + P_{\mathrm{wdg}}^{x,\mathrm{o}}(T_{\mathrm{wdg}}, f_n) \cdot l_{\mathrm{wdg}}^{x,\mathrm{o}} \,, \tag{3.45}$$

where $P_{\mathrm{wdg}}^{x,\mathrm{i}}$ denotes the area losses per length of turn x inside the winding window and $P_{\mathrm{wdg}}^{x,\mathrm{o}}$ the losses outside the window. $l_{\mathrm{wdg}}^{x,\mathrm{i}}$ and $l_{\mathrm{wdg}}^{x,\mathrm{o}}$ are the corresponding lengths of turn x inside and outside the winding win-

dow. The winding model assumes a homogeneous winding temperature T_{wdg} which must be obtained by means of a suitable thermal model.

3.3.3 Core Losses

The core losses are calculated distinguishing between LF and HF excitations. In this thesis, the LF excitations are represented by the LF voltages which drive 50 Hz sinusoidal load currents in grid applications. HF excitations are the superimposed HF voltages which in switched-mode converters can usually be approximated with ideal square-wave voltage trains. Due to the low frequency of 50 Hz, the LF losses are negligible in this work. For the calculation of the HF losses, the improved-improved generalized Steinmetz equation (i^{2}GSE) for square-wave excitations is employed [97],

$$P_{\mathrm{core}} = k_{\mathrm{fill}}\, V_{\mathrm{core}} \cdot \frac{1}{T} \sum_{i=1}^{N_{\Delta B}} \overline{k}_i \, |\Delta T_i|^{1-\alpha_i} |\Delta B_i|^{\beta_i} \ , \tag{3.46}$$

with

$$\overline{k}_i = \frac{k_i}{(2\pi)^{\alpha_i - 1} \int_0^{2\pi} |\cos\theta|_i^{\alpha} \, 2^{\beta_i - \alpha_i} \mathrm{d}\theta} \ . \tag{3.47}$$

ΔB_i denotes the $N_{\Delta B}$ peak-to-peak flux density swings of the piecewise linear HF flux waveform and T_i the corresponding time intervals where $\sum T_i = T$. Operating point-dependent Steinmetz parameters (k_i, α_i, β_i) are determined for each interval. The two improvements of the i^{2}GSE with respect to the conventional generalized Steinmetz equation (GSE) are:

(i) The capability of considering arbitrary flux waveforms rather than only sinusoidal waveforms, and

(ii) The employment of operating point-dependent Steinmetz parameters rather than fixed Steinmetz parameters.

The proposed procedure of the core loss calculation is illustrated in **Fig. 3.15** whereas further remarks are listed below:

- A prerequisite of the proposed core loss model is the knowledge of the LF and HF core excitations, i.e. the LF load current $i_{L,\mathrm{lf}}(t)$

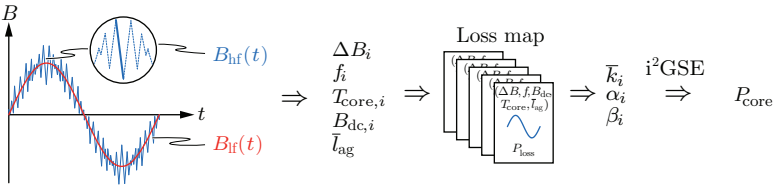


Fig. 3.15: Core loss modeling approach. Based on the LF and HF core flux densities $B_{\mathrm{lf}}(t)$ and $B_{\mathrm{hf}}(t)$, the core geometry and temperature, the operating point parameters $(\Delta B_i, f_i, T_{\mathrm{core},i}, B_{\mathrm{dc},i}, \bar{l}_{\mathrm{ag}})$ of each linear HF flux density segment can be determined. The operating point-dependent local Steinmetz parameters $(\bar{k}_i, \alpha_i, \beta_i)$ are extracted from a loss map which enables the calculation of the core losses P_{core} by means of the i²GSE (3.46).

(either DC, 50 Hz or none for pure AC operation) and the HF square-wave voltage trains. This information is provided by the waveform model.

- Knowing the LF load current $i_{L,\mathrm{lf}}(t)$ enables the calculation of the LF flux $B_{\mathrm{lf}}(t)$ density by means of the reluctance model (3.30). Based on the HF square-wave voltage trains $v_{L,\mathrm{hf}}(t)$ the HF excitations, i.e. the linear HF flux density swings ΔB_i can be calculated with

$$\Delta B_i = \frac{\int_{t_{i-1}}^{t_i} v_{L,\mathrm{hf}}(t)\,\mathrm{d}t}{N_{\mathrm{wdg}}\,k_{\mathrm{fill}}\,A_{\mathrm{core}}} = \frac{V_{L,\mathrm{hf},i}\,\Delta T_i}{N_{\mathrm{wdg}}\,k_{\mathrm{fill}}\,A_{\mathrm{core}}}\,. \tag{3.48}$$

- In this thesis, a loss map approach is employed as similarly shown in [97]. The loss map contains loss data of the respective core material as a function of the operating point defined by the linear flux density swing ΔB, the frequency of the swing f, the core temperature T_{core}, the DC offset B_{dc} of the swing and the air gap length of the core $\bar{l}_{\mathrm{ag}}$. For any operating point of interest, i.e. for each of the calculated linear HF flux segments, the closest data in the loss map are used to extract local Steinmetz parameters $(\bar{k}_i, \alpha_i, \beta_i)$ which can then be used for a loss interpolation by means of the i²GSE (3.46). Note that the losses in the loss map could also be interpolated in a linear manner rather than via the local Steinmetz parameters and the i²GSE. However, the latter interpolation approach does more accurately capture the

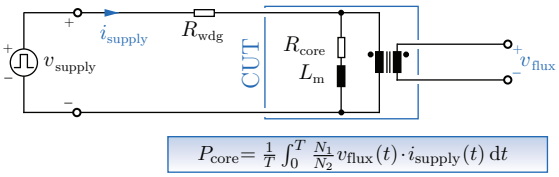
empirically found core loss dependencies (i.e. the GSE) and thus facilitates an improved accuracy.

- The core model assumes a homogeneous core temperature T_{core} which must be obtained by a suitable thermal model.

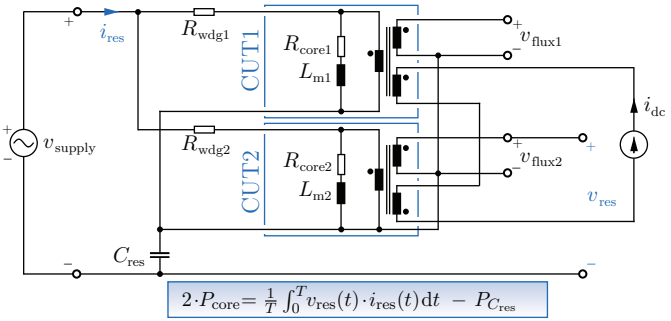
Parametrization

In strong contrast to the winding loss model, the core loss model is strongly parameter-sensitive where the parameters are represented by the core loss data. Moreover, the core losses are usually dependent from a multitude of variables such as the AC flux density swings ΔB, the frequency f, the core temperature T_{core}, the DC offset B_{dc} and the air gap length of the core $\bar{l}_{\mathrm{ag}}$. The latter is mainly important in tape-wound cores where the components of the air gap fringing fields which are perpendicular to the lamination cause increased eddy current losses. The information found in data sheets is usually insufficient and incomplete to compile a comprehensive loss map. Therefore, due to the high impact on the system performance, the core losses are experimentally determined in this thesis. For this purpose, the advanced measurement circuit depicted in **Fig. 3.16(b)** was employed which is a modified version of the circuit proposed in [102]. The modification In contrast to the widely used standard circuit/method (e.g. [97]) as depicted in **Fig. 3.16(a)**, the cores under test (CUT) in the shown circuit are operated near the resonance frequency. On the one hand, this renders the measurement insensitive towards phase discrepancies between voltage and current measurements which the standard method is prone to. On the other hand, ideally, only the core losses must be provided by the supply whereas the standard circuit must additionally provide (usually much larger) reactive power to the CUT. This enables considerably wider frequency and flux excitation ranges. Furthermore, gapped cores with a high Q-factor can be analyzed with high accuracy whereas the standard approach is practically limited to ungapped cores [103]. The disadvantages of the advanced circuit of **Fig. 3.16(b)** are the requirement of a low-loss resonant capacitor C_{res} with variable capacitance depending on the desired resonant frequency, the type of excitation which is constrained to sinusoidal waveforms and the considerably higher effort required to measure the core losses with DC flux offsets.

For this thesis, two core materials were extensively studied: the



(a)



(b)

Fig. 3.16: Core loss measurement setups. **(a)** Conventional two-winding setup enabling arbitrary excitations of the core including measurements with DC flux offsets. **(b)** Advanced core loss measurement setup used in this thesis. The cores under test (CUT) are always operated in or close to resonance, where the resonance frequency can be tuned with the low-loss series capacitor C_{res} (Vishay MKP385 series). The voltage v_{res} thus mainly comprises the resistive voltage drop across the equivalent core loss resistance R_{core} where, as a matter of principle, the winding resistance R_{wdg} is not included. As a result, the core losses can be accurately calculated based on the time-integral of $i_{\text{res}}(t) \cdot v_{\text{res}}(t)$ ($N_1 = N_2 = N_3$). Due to the largely ohmic relationship, the loss integral is insensitive to phase discrepancies in the current and voltage measurement caused by the probes and parasitics. The second key advantage of this circuit over the standard non-resonant circuit in **(a)** is the low power requirement for the AC supply since due to the resonant operation only negligible reactive power must be provided. A DC magnetization offset can be established by means of a series-connected third winding on the 2 CUTs. The opposite polarities of the third winding allows to cancel the transformed primary voltage and thus to prevent power transmitted to the DC source which would distort the measurement.

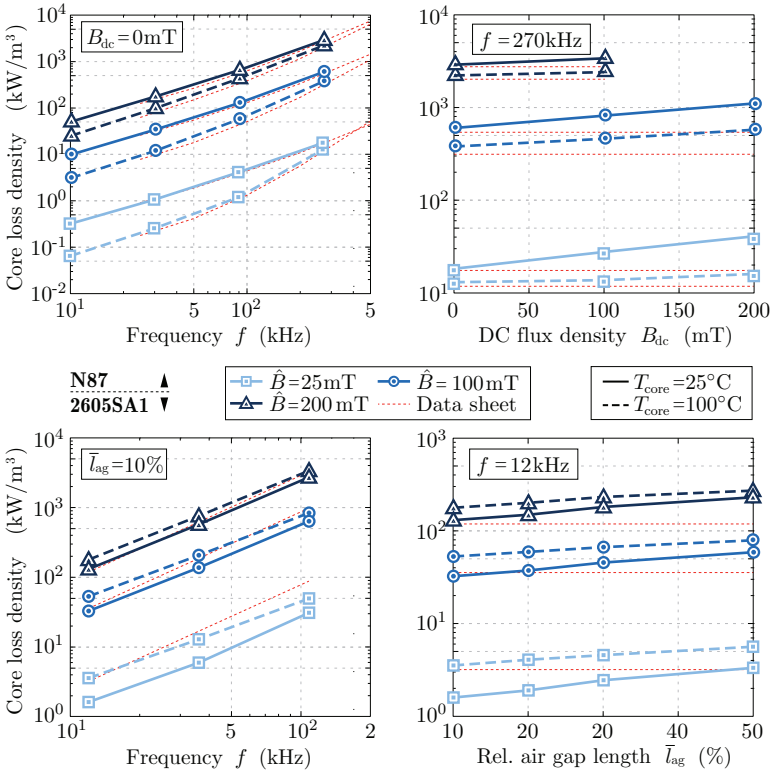


Fig. 3.17: Selection core loss measurement results for ferrite N87 and tape-wound amorphous iron 2605SA1 utilizing the circuit depicted in **Fig. 3.16**. Besides the impact of the frequency f, (sinusoidal) flux density $\hat{B}$ and the core temperature T_{core}, additionally, the impact of the DC magnetization B_{dc} on N87 and the the impact of the air gap length $\bar{l}_{ag}$ (relative to the core leg width) on 2605SA1 was studied. Whereas $\bar{l}_{ag}$ has no effect on the bulk material N87, B_{dc} was found to only moderately increase the 2605SA1 core losses (0-10 % up to 1.2 T; this supports the findings in [101]). The measured data reveals that B_{dc} increases the N87 losses by up to a factor of 2.5 which is not reported by the data sheet. Likewise for 2605SA1, T_{core} and $\bar{l}_{ag}$ have a similarly adverse effect. In sum, the conducted measurements allow for a significantly increased level of detail and accuracy in the inductor design routine which is not possible when only relying on data sheet information. Further measurements have been carried out for intermediate values of the loss variables f, $\hat{B}$, T_{core}, B_{dc} and $\bar{l}_{ag}$.

ferrite material N87 from Epcos and the tape-wound amorphous iron 2605SA1 from Metglas. Both are widely used (academic literature and industry) representatives of the respective core material types. Regarding the core loss measurements, a high priority was put on the investigation of the effects of DC magnetization, temperature and air gap length. In particular, the adverse effect of large air gaps on tape-wound cores (such as 2605SA1) has widely been discussed and confirmed in literature (e.g. in [57, 101, 103, 104]). However, to the author's knowledge, systematic and quantitative results have not been published so far. A selection of the measured core losses is depicted in **Fig. 3.17**. Inspection of the data reveals partially tremendous deviations (factor of 2 to 3) with respect to the data sheet values. This emphasizes the importance and value of the conducted measurements which enable a greatly increased level of detail and accuracy in the inductor design routine.

3.3.4 Thermal Modeling

A thermal model for inductors has been derived which takes into account the 3D geometry and the anisotropic, direction-dependent thermal properties of the underlying materials. The thermal resistance network is shown in **Fig. 3.18**. The modeled inductor geometry is depicted in **Fig. 3.13**. The winding hot spot temperature is, based on measurements, assumed to be on the outer surface of the winding, whereas the core hot spot location is assumed to be in the center of the core. Different winding surface temperatures (inner, outer, top, bottom) are modeled, whereas a uniform core surface temperature is assumed due to the high thermal conductivity of common core materials.

Heat Transfer Mechanisms

Three different types of heat transfer mechanisms are considered for the resistances shown in **Fig. 3.18**. For the thermal constants and parameters used in the below equations refer to **Tab. 3.2**.

- *Heat conduction:* the thermal resistance which models conducted heat transfer is given by

$$R_{\mathrm{th,cond}} = \frac{l_*}{\lambda_{\mathrm{th},*} \cdot A_*} \,, \tag{3.49}$$

Tab. 3.1: Modeled heat transfer mechanisms in the thermal network depicted in **Fig. 3.18**. Due to tolerances, the coil former does usually not firmly contact the core. This is modeled with a thin layer of air between coil former and core.

Resistances:	**Conduction**	**Radiation**	**Convection**
$\boldsymbol{R}_{\mathbf{th,wdghs\text{-}wdg}}^{\mathbf{\{i,t,b\}}}$	✓		
$\boldsymbol{R}_{\mathbf{th,corehs\text{-}core}}^{\mathbf{\{xy,z\}}}$	✓		
$\boldsymbol{R}_{\mathbf{th,wdg\text{-}core}}^{\mathbf{\{i,o,t,b\}}}$	✓	✓	
$\boldsymbol{R}_{\mathbf{th,wdg\text{-}amb}}^{\mathbf{\{o,t,b\}}}$		✓	✓
$\boldsymbol{R}_{\mathbf{th,core\text{-}amb}}^{\mathbf{xyz}}$		✓	✓

Tab. 3.2: Thermal parameters and material characteristics employed in the thermal inductor models. The data is taken from [105, 106], from the respective material data sheets or based on own measurements.

Emissivity of enameled copper	ϵ_{wdg}	0.8
Emissivity of the core materials	ϵ_{wdg}	0.9
Stephan-Boltzmann constant	σ	$5.67 \cdot 10^{-8}\,\mathrm{W/m^2\,K^4}$
Vertical-positioning coefficient	C_{v}	1.58
Reference pressure (sea level)	p_{ref}	101.32 kPa
Reference ambient temperature	$T_{\mathrm{amb,ref}}$	$(25 + 273.15)\,\mathrm{K}$
Conductivity of round wire [1,2)]	$\lambda_{\mathrm{th,wdg}}^{\mathrm{ro}}$	$1.0\,\mathrm{W/m\,K}$
Conductivity of litz wire [1,2)]	$\lambda_{\mathrm{th,wdg}}^{\mathrm{li}}$	$0.3\,\mathrm{W/m\,K}$
Conductivity of flat wire [3)]	$\lambda_{\mathrm{th,wdg}}^{\mathrm{fl}}$	$401/0.15\,\mathrm{W/m\,K}$
Conductivity of foil wire [4)]	$\lambda_{\mathrm{th,wdg}}^{\mathrm{fo}}$	$401/0.03\,\mathrm{W/m\,K}$
Conductivity of Epcos N87	$\lambda_{\mathrm{th,core}}^{\mathrm{N87}}$	$4.18\,\mathrm{W/m\,K}$
Conductivity of Metglas 2605SA1 [5)]	$\lambda_{\mathrm{th,core}}^{\mathrm{2605SA1}}$	$9/5\,\mathrm{W/m\,K}$
Conductivity of Magnetics Koolmu	$\lambda_{\mathrm{th,core}}^{\mathrm{KoolMu}}$	$8\,\mathrm{W/m\,K}$

[1)] For a hexagonal winding arrangement including air (cf. **Fig. 3.13**)

[2)] Based on measurements and simulations

[3)] IACS copper / Kapton foil and air insulation between conductors

[4)] IACS copper / air insulation between conductors

[5)] Along / perpendicular to lamination

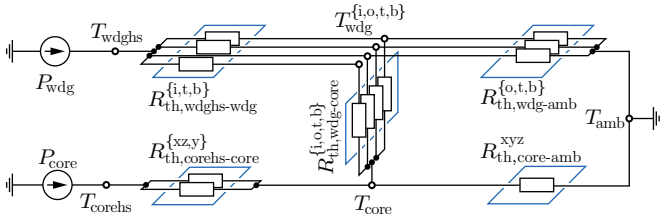


Fig. 3.18: Anisotropic 3D thermal model for inductors. P_{wdg} and P_{core} denote the total winding and total core losses, respectively. $R_{\text{th,wdghs-wdg}}^{\{\text{i,t,b}\}}$ are the thermal resistances from the winding hot spot, which is assumed to be on the outer winding surface, to the respective inner, top and bottom winding surface. $R_{\text{th,wdg-core}}^{\{\text{i,o,t,b}\}}$ and $R_{\text{th,wdg-amb}}^{\{\text{o,t,b}\}}$ are the resistances from the winding surfaces to the core surface and to the ambient, respectively. For the corresponding E-core geometry (cf. **Fig. 3.13**) of this network but also for U-cores, the inner winding surface is not exposed to the ambient. $R_{\text{th,corehs-core}}^{\{\text{xy,z}\}}$ and $R_{\text{th,core-amb}}^{\text{xyz}}$ are the resistances from the core hot spot to the core surface with uniform temperature T_{core} and from the surface to the ambient.

where $\lambda_{\text{th},*}$ is the material's thermal conductivity and l_* and A_* the (direction-dependent) length and cross section of the heat conductor to be modeled.

- *Heat radiation:* radiated heat from an object 1 to an object 2 can be modeled with the thermal resistance,

$$R_{\text{th,rad}} = \frac{1}{h_{\text{rad},*} \cdot A_*} = \frac{T_{1,*} - T_{2,*}}{\epsilon_{1,*} \cdot \sigma \left(T_{1,*}^4 - T_{2,*}^4 \right)} \cdot \frac{1}{A_*} \,, \tag{3.50}$$

where $h_{\text{rad},*}$ represents the heat transfer coefficient, A_* is the overlapping area of the two objects and $T_{1,*} > T_{2,*}$ are the respective temperatures.

- *Natural convection:* for natural convection the transfer coefficient $h_{\text{rad},*}$ in (3.50) changes to [105]

$$h_{\text{conv},*} = C_{\text{v}} \left(\frac{p}{p_{\text{ref}}} \right)^{0.477} \left(\frac{T_{\text{amb}}}{T_{\text{amb,ref}}} \right)^{-0.218} \frac{(T_* - T_{\text{amb}})^{0.225}}{L_{\text{ch},*}^{0.285}} \,. \tag{3.51}$$

In the above equation (3.51), $L_{\mathrm{ch},*}$ is the characteristic length [105] which for the given inductor geometry was calculated with

$$L_{\mathrm{ch},xz} = 2 \cdot (w_\mathrm{w} + w_\mathrm{c}) + (w_\mathrm{c} + h_\mathrm{w}) \,, \tag{3.52}$$

$$L_{\mathrm{ch},yz} = d_\mathrm{c} + (h_\mathrm{w} - 2d_\mathrm{cf}) + 2 \cdot \sqrt{w_\mathrm{w}^2 + (\frac{w_\mathrm{c}}{2} + d_\mathrm{cf})^2} \,, \tag{3.53}$$

for the airflow in the xz and yz plane, respectively.

Most of the thermal resistances depicted in the thermal network model in **Fig. 3.18** combine more than one of the above mechanisms. The total resistances shown in **Fig. 3.18** can be calculated by the parallel connection of the individual type-specific resistances,

$$\frac{1}{R_\mathrm{th,tot}} = \frac{1}{R_\mathrm{th,cond}} + \frac{1}{R_\mathrm{th,rad}} + \frac{1}{R_\mathrm{th,conv}} \,. \tag{3.54}$$

The applicable types of heat transfer of each of the thermal resistances depend on the specific geometry and/or winding type. For the considered E-core inductor geometry this information is listed in **Tab. 3.1**. Note that generally all of the heat transfer mechanisms should be considered as typically all mechanisms have a non-negligible impact on the thermal properties.

3.3.5 Experimental Verifications

In order to validate the core loss measurements and the proposed loss models, 2605SA1-based inductors were tested under different operating conditions using the calorimeter setup depicted in **Fig. 3.19**. The model-predicted losses show a very good agreement with the measured losses when considering the complexity of the underlaying physics. A mean error of $< 10\,\%$ was achieved. The accuracy and error variance is improved by more than a factor of 2 when compared with data sheet-based loss predictions. In particular, the calorimetric measurements largely confirm the operating point-dependent relative differences between the experimentally obtained core losses and the data sheet values: the data sheet-based loss calculations tend to overestimate the losses for small flux excitations and low temperatures whereas for large air gaps and higher flux excitations the losses are clearly underestimated. Experimental verifications of the N87 core loss measurements are shown

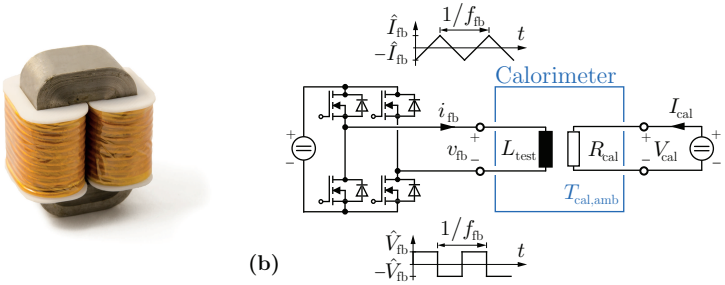


Fig. 3.19: Experimental verification of the core loss measurements and the employed inductor loss models. **(a)** Sample test inductor with litz winding. **(b)** Employed calorimetric measurement setup. A full bridge converter is used to excite the inductor under test L_{test} with a triangular current. The ambient temperature inside the calorimeter $T_{\mathrm{cal,amb}}$ increases due to the power loss of the test inductor reaches a steady-state value $T^{ss}_{\mathrm{cal,amb}}$. $T_{\mathrm{cal,amb}}$ is homogeneous inside the calorimeter due to the employment of a fan. The full bridge is then turned off while the DC calibration network is turned on. $\Delta P_{\mathrm{cal}} = {}^{\Delta V^2_{\mathrm{cal}}}/_{R_{\mathrm{cal}}}$ is adjusted so as to keep the calorimeter ambient temperature $T_{\mathrm{cal,amb}}$ constant at $T^{ss}_{\mathrm{cal,amb}}$. This approach yields a good measure of the total inductor losses, i.e. $P_{L_{\mathrm{test}}} \approx \Delta P_{\mathrm{cal}}$.

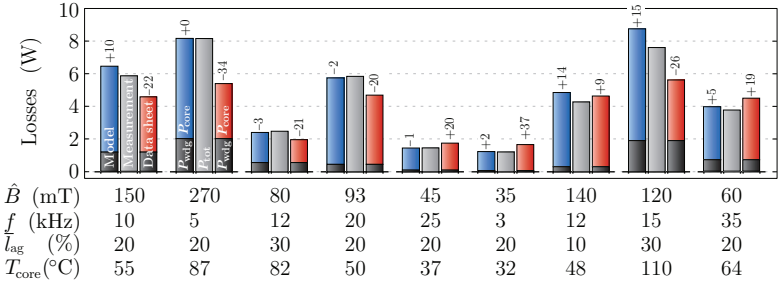


Fig. 3.20: Representative selection of the conducted core loss and inductor modeling verification measurements using the setup of **Fig. 3.19**. Depicted are the measured losses versus the calculated winding and core losses either based on the data sheet values or the measured core loss data as depicted in **Fig. 3.17**. The calorimetric measurements largely confirm the operating point-dependent relative differences between the experimentally obtained core losses and the data sheet values. The proposed inductor models achieve a mean absolute deviation of 8.6 % at a standard deviation of 5.0 % ($N_{\mathrm{pop}} = 25$). The data sheet-based approach achieves a mean error of 19.5 % at a standard deviation of 9.8 %.

Tab. 3.3: Test inductor design parameters for the experimental verification of the thermal and loss models shown in **Fig. 3.21**. The high DC resistance of the DCL inductor winding results from the large number of winding turns ($N_{\mathrm{wdg}} > 300$) which was used to obtain an experimentally estimated thermal conductivity $\lambda^{\mathrm{ro}}_{\mathrm{th,wdg}}$ for hexagonal round wires (cf. **Tab. 3.2**).

Inductor name:	**DCL**	**ACL**
Core material	N87	2605SA1
Core type	E80/38/20 (1 set × 3 stacked)	AMCC06R3 (2 sets × 2 stacked)
Air gap length l_{ag}	None	1.0 mm
Winding type	Round	Round
$R_{\mathrm{dc}}(T_{\mathrm{wdg}} = 25\,°\mathrm{C})$	21.2 Ω	7.8 mΩ
LF current	0 Hz (DC)	50 Hz
HF current	None	16 kHz / 9.5 A

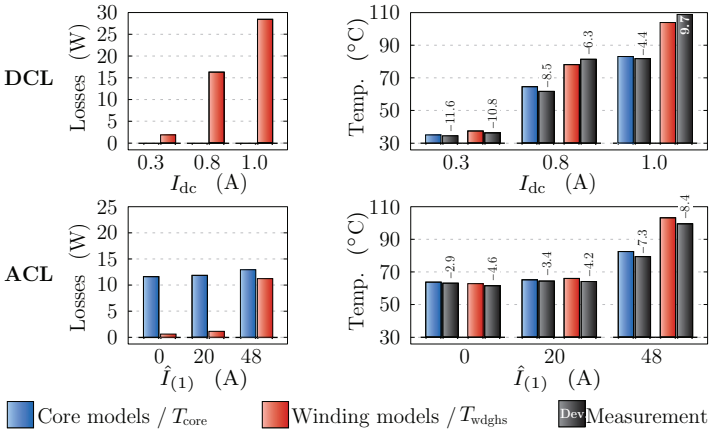


Fig. 3.21: Results of the experimental verification of the proposed thermal and loss models based on the inductor designs of **Tab. 3.3**. **(a)** Separate verification of the thermal model only using different DC currents I_{dc} in conjunction with a known DC winding resistance $R_{\mathrm{dc}}(T_{\mathrm{wdg}})$. **(b)** Combined verification of the thermal and loss models using different 50 Hz LF AC currents $\hat{I}_{(1)}$ superimposed by a 9.5 A/16 kHz peak-to-peak HF current. Deviations of usually less than 10 % between actual and calculated temperatures/losses were observed.

in Chapter 5 where various N87-based inductors and transformers are employed in a dual active bridge (DAB) converter.

In order to verify the accuracy of the proposed thermal model, measurements have been performed on two test inductors with parameters as listed in **Tab. 3.3**. The inductors were placed on small columns and far apart from other objects in order to implement the assumed conditions in the model as accurately as possible. In a first experiment (DCL), only DC currents without superimposed HF currents were employed **Fig. 3.21(a)**. This allows to evaluate the performance of the thermal model with only negligible uncertainty regarding the excitations of the thermal model, i.e. the losses. In a second experiment (ACL), LF AC currents with a superimposed HF current component were employed to verify the performance of the combined loss and thermal models **Fig. 3.21(b)**. In all analyzed operating points deviations of less than 10 % between measurement and calculation were observed. Furthermore, it was found that the model usually overestimates the temperatures, i.e. is conservative. This can mainly be reasoned with the neglected heat flow via the connecting wires and via the columns to the ground.

3.4 Capacitors

The capacitors as used in this thesis are comparably simple to model. Apart from the cost models presented in the next chapter, the only physical models which are required are the loss models.

3.4.1 Loss Models

The losses in an aluminum electrolytic capacitor can be calculated with

$$P_C^{\text{Al-e}} = \sum_n R_{\text{esr}}\big(f_{(n)}, T_{\text{amb}}\big) \cdot \frac{1}{2}\hat{I}_{C(n)}^2 \quad + I_{\text{leak}}(V_{C,\text{op}}, T_{\text{amb}}) \cdot V_{C,\text{op}} \ , \tag{3.55}$$

where T_{amb} is the ambient temperature, $\hat{I}_{C(n)}$ the harmonics of the spectrum of the current flowing into the capacitor and $V_{C,\text{op}}$ the DC operating voltage of the capacitor. R_{esr} is the frequency- and temperature-dependent equivalent series resistor (ESR) which summarizes the resistances of the electrolyte, the electrodes and the terminals. The

temperature- and operating voltage-dependent residual leakage current arises from the non-ideal dielectric. Note that in some cases external balancing resistors must be employed to ensure symmetric voltage stress on electrolytic capacitors connected in series. The current through these resistors may then be added to the capacitor losses.

The losses in metalized plastic polypropylene film capacitors for DC or filter applications can be calculated with

$$P_C^{\text{film}} = \sum_n R_{\text{esr}}\big(f_{(n)}\big) \cdot \frac{1}{2}\hat{I}^2_{C(n)} \; . \tag{3.56}$$

The leakage currents of film capacitor as well as the temperature-dependence of the ESR can usually be neglected.

3.4.2 Parametrization

If resonant converter applications with typically high HF AC capacitor currents are neglected, the losses in the capacitors are usually low when compared to other components. This observation legitimates the utilization of simple data sheet parameters for the capacitor losses. The numerical values for the parameters R_{esr} for electrolytic and film capacitors and I_{leak} for electrolytic capacitors as required in this thesis can be found in [107, 108] and the individual data sheets of the capacitor series. Note that the information regarding achievable lifetime and maximum permissible current stress which are typically required for the dimensioning of the capacitors can also be found in [107, 108].

4 Cost Modeling

Costs are a main driver of research and development in industrial companies and represent a key parameter for market success and a sustainable competitive advantage [2, 5–7, 10, 63, 71–73]. A general screening of the academic literature in the field of power electronics, however, shows that the majority of contributions mainly focus on physical performance measures such as the efficiency, volume and the weight whereas a deeper analysis and consideration of costs is only rarely addressed. In order to make a first step towards closing this gap between academia and industry, in this chapter, systematic cost models for power electronic converter systems are proposed.

From the viewpoint of academia, the availability of quantitative cost

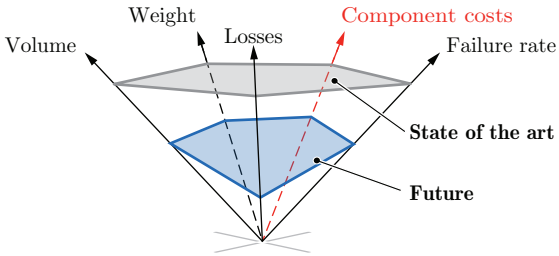


Fig. 4.1: Cost reduction is a main enabler for market success and a sustainable competitive advantage of industrial companies. In strong contrast, the predominant topic in research publications is the improvement of converter efficiency, weight and volume, whereas (component) cost aspects are rarely considered.

models and a better understanding of the cost shares in power electronic converter systems could enable several advantages and opportunities:

- Cost considerations strongly enhance the significance of the outcome of (multi-objective) optimizations and virtual prototyping (cf. Section 1.2.4).
- Cost data and models allow to assess novel technologies and concepts proposed by academia also from the cost point of view. Thereby, a more realistic and practice-oriented picture of the potential of the innovation can be obtained. The more comprehensive cost-aware assessment in turn may serve as a guideline for further (technical) refinements.
- Analogously, a better understanding of the costs and/or the cost structure of *existing* applications facilitates the identification of the aspects and areas which are the most remunerative and promising for future research activities.

This chapter presents the derivation of component cost models based on empirically obtained cost data. This data and the derived cost models represent the key to making the cost dimension available to the MOO-based virtual prototyping routine proposed in this thesis. In a first step, the literature survey in Section 4.1 confirms the poor availability of cost models and cost data in academia. Section 4.2 analyzes the difficulties which are faced in cost modeling and suggests an approach to overcome the challenges. Finally, Section 4.3 discusses the empirically collected cost data and derives cost models for the power semiconductors, cooling systems, passive components, PCBs and auxiliary electronics. A range of concluding remarks on cost modeling is given in Section 4.4.

This chapter is based on the work published in [109]. In comparison to [109], the cost models of this chapter have partially been refined and parts of the cost database has been updated.

4.1 Literature Review

This section provides a short overview on how cost aspects are incorporated in research and summarizes the cost data and models which are available in literature.

On the component level, cost considerations for single components can be found in [110–112] for semiconductors, inductive components and

heat sinks. Here, the component costs are only indirectly estimated by means of representing and substituting the costs by physical quantities such as the total chip area or the stored energy and volume of the passive components. The significance and possibilities of this approach are, however, strongly limited if the estimated "costs" must be compared to other components and materials. This is typically the case when designing entire converter systems. Further examples for cost consideration for single types of components can be found in [51, 113–115]. In contrast to the previous contributions, direct and quantitative cost models are employed rather than substituting physical quantities. The models are employed for the optimization of transformers, litz wires, inductors and semiconductors. Partly for reasons of confidentiality, however, no details on the cost models [113], only normalized values [114] or simple distributor prices [51, 115] for unknown order quantities are provided for the parameters of the cost models.

More detailed cost models enabling the description and comparison of several types of components and manufacturing processes are presented in [116–118] for the projection of levelized wind energy costs, the manufacturing costs of integrated circuits (IC) or for the optimization of photovoltaic (PV) power plant configurations at system level.

With respect to comprehensive cost analysis for modern switched-mode power converters including all relevant components (such as semiconductors, cooling systems and passives), some of the few examples which can be found in literature are [62–67, 119, 120]. Here, a mix of discrete cost data as well as continuous cost models are employed for converter optimizations. Alas, except for [63,65] which employ the cost models presented in [109] and this thesis, the cost modeling in all contributions suffer from one or more severe drawbacks. [62,67,120] neither show cost data nor detailed cost models and restrict the information on costs to the presentation of the final, normalized converter costs. [119] presents normalized cost data for unknown components. The optimizations in [64] are based on a limited set of real cost data for discrete components. However, the components and order quantities are not specified. Finally, [66] presents some useful models giving insight into the cost structure of inductors. However, only a normalized and an incomplete set of cost parameters is provided.

From an academic point of view, it can be concluded that the found publications on cost modeling pose only a minimal gain as the presented models and data are rather limited regarding their application. More-

over, the presented results are largely non-reproducible from the cost point of view.

4.2 Challenges and Approach

Developing cost models for power electronics components poses several challenges:

- *Confidentiality of cost data:* costs do not represent a physical quantity and can thus not be explained with physical laws nor obtained by means of experimental measurements. The knowledge of cost data for components, materials and manufacturing processes is thus a fundamental requirement for cost modeling and can only be gained by empirical means. However, collecting cost data is often severely impeded by the non-disclosure of such data by sellers and manufacturers.
- *Complexity of the cost structure of components:* the manufacturing of power electronic components usually involves a broad mix of different base materials, a multitude of manufacturing processes and labor. Modeling these cost factors is challenging and requires an extensive set of cost data.
- *Influence of non-physical, non-product-related cost factors:* apart from direct cost factors (base materials, processes and labor) there is a wide range of additional cost factors. These cost factors are not directly related to the product itself but typically influence the final price of the components significantly. Such factors are the minimum order quantity (MOQ), the location of manufacturing and delivery, currency effects and price negotiations between seller and buyer.
- *Time-dependence of costs:* due to varying raw material costs, economy-of-scale, learning effects and changing pricing strategies of the manufacturers, component costs vary with time and must hence be checked and updated regularly.

A range of strategies is proposed to facilitate cost modeling and to overcome most of the above stated challenges. In order to enhance the significance and comparability, the acquiring of the cost data was conducted according to standardized rules:

- Quote requests were only made to the component manufacturers directly or – where not possible – to the direct and exclusive distributors. This approach largely eliminates unnecessary overhead costs due to distribution and results in less distorted data. Furthermore, this approach does more closely model the situation of large power electronic manufacturers for whom such overhead costs normally do not apply.
- Generally, MOQs larger than 10 000 units were requested to give more realistic figures for the industrial mass production and to further cut the influence of overhead costs.
- Prices were exclusively inquired in Euros or – if not possible – in U.S. Dollars. An exchange rate of 1.2 € per $ was assumed throughout this work.

The complexity of the cost structure and the multitude of different cost factors determining the price of the components is obviously most accurately captured if the final price is known. Therefore, it is proposed to directly use the acquired component cost data rather than models for the calculation of the total converter costs. This is mainly possible where fixed, non-scalable components are employed such as specific discrete semiconductors, capacitors or fans.

In many practical situations, however, using cost models proofs to be a valuable tool for cost estimations:

- Manufacturers would frequently refuse to provide the cost data of all components of a specific series (e.g. a series of capacitors of a specific type) and/or the analysis and post-processing of a large set of data can be time-consuming. Here, cost models offer the advantage of inter- and extrapolation based on well-known sampling points.
- The manufacturing of a number of components is usually customized. Basic features of such components are thus inherently scalable such as the volume of heat sinks or the weight of the winding of magnetic components. In converter optimization, such quantities normally represent continuous design variables rather than fixed constants. As a result, estimating the costs of such components can only be accomplished by means of cost models rather than a discrete set of cost data.

- Cost models provide interesting insight into the cost structure and cost factors of components.

Due to the already mentioned complexity of the cost structure of power electronic components, it is proposed to employ reduced-order modeling techniques. The presented models in the following section largely depend on variables which are related to commonly used physical component properties, e.g. the chip area, the weight of the inductor winding and core and the heat sink volume. This approach is especially useful for optimizations as the models can be incorporated into the converter dimensioning process in a straightforward manner and linked to already available parameters and variables.

For the remainder of this chapter, *cost* designates the component manufacturing cost, whereas *price* refers to the final component selling price which corresponds to the buying cost of the converter manufacturers.

4.3 Derivation of Component Cost Models

In this section, cost models for power semiconductors, magnetic components, capacitors, cooling systems, PCBs and auxiliary ICs and electronics are derived. The models are applicable to typical components of a broad variety of switched-mode power electronic converters with an approximate power rating of 1-50 kW. The models are designed taking the viewpoint of the converter manufacturers. The underlying cost data are derived based on empirical research and represent a snapshot of the market between beginning of 2013 and 2015.

4.3.1 Power Semiconductors

Generally, the cost structure of semiconductors derives from a complex mix of sophisticated manufacturing processing steps and high R&D efforts, whereas the (unprocessed) raw materials take only a negligible share of the total costs [121]. From an engineering point of view, the two most important features of a semiconductor are its chip size and the package. Together they largely define the electrical and thermal behavior of the device [122]. Therefore, these two quantities are selected to summarize and model the range of factors contributing to the overall costs,

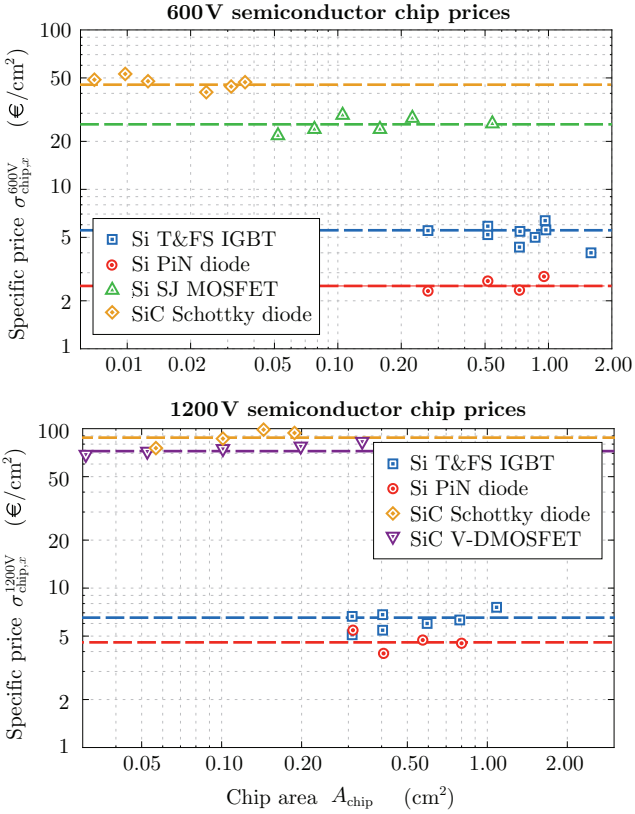


Fig. 4.2: Specific prices for common semiconductor chip technologies based on data from two major semiconductor manufacturers. The packaging costs $\Sigma_{\mathrm{pack},x}$ according to **Tab. 4.1** were deduced from the obtained price samples based on which the depicted data in the figures was calculated. The dashed lines represent the numerical values of the fitted cost model parameters $\sigma_{\mathrm{chip},x}$. The current rating of the considered semiconductors is approximately in the range of 5-100 A. It should be noted that SiC semiconductors generally employ smaller chip areas for the same current ratings as a result of the significantly lower specific on-state resistance when compared to Si.

Tab. 4.1: Derived numerical values for the specific semiconductor chip prices $\sigma_{\text{chip},x}$ and package prices $\Sigma_{\text{pack},x}$ of the semiconductor cost model (4.1). MOQs for modules are MOQ = 10 000 and for discretes MOQ = 50 000.

Chip technology:	**Si T&FS IGBT**	**Si PiN diode**	**Si SJ MOSFET**	**SiC Schottky diode**	**SiC V-DMOSFET**
$\boldsymbol{\sigma^{600\,\text{V}}_{\text{chip},x}}$ **(€/cm²)**	5.52 [1)]	2.46 [2)]	27.34 [3)]	46.24 [4)]	
$\boldsymbol{\sigma^{1200\,\text{V}}_{\text{chip},x}}$ **(€/cm²)**	6.57 [1)]	4.46 [2)]		86.47 [5)]	72.01 [6)]
Package type:	**TO-247**	**SOT-227**	**SP1**	**SP3**	**SP4**
$\boldsymbol{\Sigma_{\text{pack},x}}$ **(€/unit)**	0.55	8.10	7.62 [7)]	10.01 [7)]	15.06 [7)]

[1)] Infineon IGBT 4 [2)] Infineon EmCon [3)] Infineon CoolMos C7
[4)] Wolfspeed Z-REC Gen 3 [5)] Wolfspeed Z-REC Gen 4
[6)] Wolfspeed Z-FET Gen 2 [7)] Microsemi

SOT−227 $38 \times 25 \times 12$ mm³ | **SP1** $52 \times 41 \times 18$ mm³ | **SP3** $73 \times 41 \times 18$ mm³ | **SP4** $93 \times 41 \times 21$ mm³

Fig. 4.3: Photographs and dimensions of the modules listed in **Tab. 4.1**.

$$\Sigma_{\text{SC}} = \Sigma_{\text{chip},x} + \Sigma_{\text{pack},x} = \left(\sum_n \sigma_{\text{chip},x(n)} A_{\text{chip}(n)} \right) + \Sigma_{\text{pack},x} \,. \quad (4.1)$$

In (4.1), $\sigma_{\text{chip},x}$ is the specific price per chip area A_{chip} depending on the chip technology and $\Sigma_{\text{pack},x}$ summarizes the package price including the chip integration, bonding and the testing. Eq. (4.1) is motivated by [51,122] where it is observed that the semiconductor prices scale approximately linearly with the chip size. The parameter $\sigma_{\text{chip},x}$ can hence be interpreted as the aggregate sum of all processing and R&D costs for a given chip technology. The validity of the model is underpinned by the acquired database of over 50 discretes and power modules with associated prices and chip areas from two major semiconductor manufacturers. The visualization of a large fraction of this data in **Fig. 4.2** shows relatively constant specific chip prices for all considered technolo-

gies. **Tab. 4.1** lists the numerical values for $\sigma_{\mathrm{chip},x}$ which have been identified based on a multi-parametric least square fitting (mean error 6.7 %, standard deviation 4.9 %) of the database samples.

4.3.2 Magnetics

In contrast to most other power electronic components, inductors for converters in the considered power range are often material and labor intense, i.e. a considerable fraction of the total price can be reasoned with the material and labor costs. This motivates the use of the following inductor cost model of which a simplified version can also be found in [66],

$$\Sigma_L^{\mathrm{dc}} = \Sigma_{\mathrm{core}} + \Sigma_{\mathrm{wdg}} + \Sigma_{\mathrm{lab}} \ , \tag{4.2}$$

where

$$\Sigma_{\mathrm{core}} = N_{\mathrm{stack}} \cdot \Sigma_{\mathrm{core},x}^{\mathrm{fc}} + \sigma_{\mathrm{core},x}\, W_{\mathrm{core}} \ , \tag{4.3}$$

$$\Sigma_{\mathrm{wdg}} = \Sigma_{\mathrm{wdg},x}^{\mathrm{fc}} + \sigma_{\mathrm{wdg},x}\, W_{\mathrm{wdg}} \ , \tag{4.4}$$

$$\Sigma_{\mathrm{lab}} = \Sigma_{\mathrm{lab}}^{\mathrm{fc}} + \sigma_{\mathrm{lab},x}\, W_{\mathrm{wdg}} \ . \tag{4.5}$$

$\Sigma_{\mathrm{core},x}^{\mathrm{fc}}$, $\Sigma_{\mathrm{wdg},x}^{\mathrm{fc}}$ and $\Sigma_{\mathrm{lab}}^{\mathrm{fc}}$ represent fixed costs for the cores (N_{stack} being the stacking factor), for the connectors and coil formers as well as for labor. $\sigma_{\mathrm{core},x}$, $\sigma_{\mathrm{wdg},x}$ and $\sigma_{\mathrm{lab},x}$ are specific costs per weight depending on the employed core and winding type. **Tab. 4.2** lists numerical values for the parameters of the proposed inductor cost model. The data is on the one hand obtained from core and winding manufacturers for large MOQs. Additionally, the expertise of several inductor manufacturers could be sourced for further information on core and winding costs as well as the labor costs. According to these manufacturers of magnetic components, a large MOQ $> 15\,000$ usually implies Asian manufacturing due to lower labor costs. Moreover, the cost for manufacturing tools for custom core sizes (typically around 5 000-15 000 €) can be neglected in a first approximation considering the high MOQs. As converter manufacturers often purchase the assembled magnetic components from such external suppliers, a cost premium must be added. The sum Σ_L^{dc} in (4.2) represents the direct costs of the supplier, i.e. all costs which can directly be attributed to the product. Hence, the figure does not yet include any overhead costs and profit. The final

Tab. 4.2: Derived numerical values for the inductor cost model (4.7) based on data from several winding, core and inductor manufacturers (cores: MOQ = 50 000 sets; windings: MOQ = 1 metric ton). In the case of the ferrite and powder E-cores and the amorphous C-cores one unit refers to a set of two core halves. The indicated costs for grain-oriented electrical steel (GOES) follows world market prices and is valid with good accuracy for the grades M2 to M4 (0.18-0.27 mm sheet thickness). The GOES price applies to the unprocessed base material only.

Core material:	**Ferrite** [1)]	**Amorphous** [2)]	**Nanocrystalline** [3)]	**Powder** [4)]	**GOES**
$\Sigma^{\mathrm{fc}}_{\mathrm{core},x}$ (€/unit)	0.08	5.10	1.05	0.60	0.00
$\sigma_{\mathrm{core},x}$ (€/kg)	7.50	14.10	48.90	10.20	2.00
Core type:	**E/ELP**	**U/C**	**Toroid** [5)]		
$\Sigma^{\mathrm{fc}}_{\mathrm{wdg},x}$ (€/unit)	0.25	1.00	0.05		
Winding type:	**Round**	**Flat**	**Foil**	**Litz**	
$\sigma_{\mathrm{wdg},x}$ (€/kg)	10.00	10.00	20.00	variable [6)]	
$\sigma_{\mathrm{lab},x}$ (€/kg)	7.00	14.00	14.00	7.00	
$\Sigma^{\mathrm{fc}}_{\mathrm{lab},x}$ (€/unit)	0.75	1.25	1.50	0.75	
GM (%)			25.0		

[1)] Epcos N87 E-cores [2)] Metglas Powerlite 2605SA1 AMCC C-cores

[3)] Vitroperm 250F/500F coated toroids [4)] KoolMu 40µ/60µ E-cores

[5)] Coated core; causes 33 % higher labor costs $\Sigma^{\mathrm{fc}}_{\mathrm{lab},x}$, $\sigma_{\mathrm{lab},x}$ due to closed shape

[6)] Pack Feindrähte Rupalit Classic, AWG{48,46,44,41,38,32,27}
$\hat{=}$ {30,40,50,71,100,200,355} µm → {111.5, 58.5, 32.5, 23.5, 21.5, 18.5, 16.5} €/kg

component price can be approximated by means of the supplier's gross margin GM [123],

$$GM = \frac{\textit{Gross profit}}{\textit{Revenue}} = \frac{\textit{Revenue-COGS}}{\textit{Revenue}} \,, \tag{4.6}$$

where $COGS$ is the costs of all goods sold excluding any overhead costs and profit, or equivalently the sum of direct costs of all sold products (and/or services). Hence, assuming a similar gross margin for all individual products of the supplier, the final selling price Σ_L can be estimated with

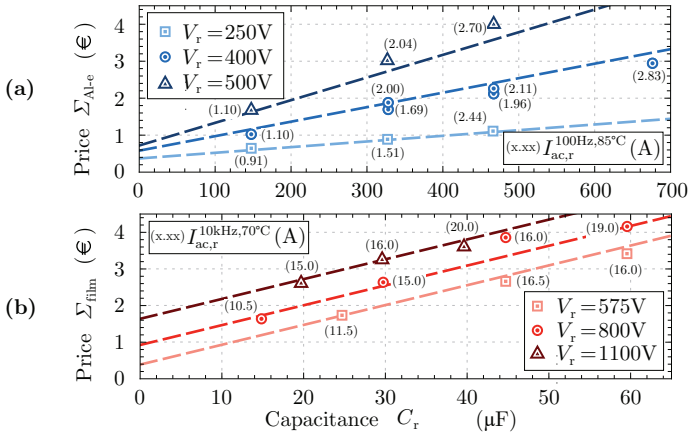


Fig. 4.4: Unit prices for **(a)** different standard type aluminum electrolytic (Al-e) and **(b)** metalized polypropylene (PP) thin film power capacitors based on prices from a major capacitor manufacturer (MOQ = 10 000, PVC insulation). $I_{ac,r}$ is the capacitor rated rms current. The figures further depict the corresponding curves of the cost models (4.8), (4.9) based on the fitted parameters presented in **Tab. 4.3**.

$$\Sigma_L = \frac{1}{1 - GM} \cdot \Sigma_L^{dc} \ . \tag{4.7}$$

Typical values of the gross margin of industrial companies are in the range of 20-30 %. Hence, a gross margin of $GM = 25\,\%$ was assumed throughout this work.

4.3.3 Capacitors

Power Capacitors

The predominant types of power capacitors in the field of power electronics are aluminum electrolytic and thin film capacitors. **Fig. 4.4** shows the unit prices of a selection of standard aluminum electrolytic capacitors (Al-e) and metalized polypropylene (PP) thin film capacitors from a major manufacturer. The data reveals the different price dependencies of the two considered capacitor types: whereas the prices of the electrolytic capacitors scale with the rated stored energy, i.e.

Tab. 4.3: Proposed numerical values for the capacitor cost models (4.8),(4.9),(4.10),(4.11) for electrolytic and PP film capacitors based on data provided by a major capacitor manufacturer (MOQ = 10 000).

	a_x	b_x	c_x
Al-electrolytic [1)]		$1.437 \cdot 10^{-3}$ €/V	$24.757 \cdot 10^{-9}$ €/µF V^2
DC PP film [2)]	-1.022 €	$2.426 \cdot 10^{-3}$ €/V	$54.956 \cdot 10^{-3}$ €/µF
AC X2 film [3)]	0.065 €		0.155 €/µF
AC Y2 film [4)]	0.073 €		2.604 €/µF

[1)] Epcos B3277x [2)] Epcos B43501x
[3)] Epcos B3292x [4)] Epcos B3202x

$\Sigma_{\text{Al-e}} \propto C_\text{r} V_\text{r}^2$, the film capacitor unit prices scale only linearly with the rated capacitance C_r and voltage V_r, i.e. $\Sigma_{\text{film}} \propto c_1 \cdot C_\text{r} + c_2 \cdot V_\text{r}$. For the latter, this implies that the stored energy becomes cheaper for higher rated voltages. According to manufacturers, this characteristic is due to the lower manufacturing cost of thicker films which are used for higher rated voltages (holds true up to 2-3 kV).

Based on the preceding observations, the following (unit) cost models are proposed for electrolytic and film capacitors,

$$\Sigma_{\text{Al-e}} = b_{\text{Al-e}} V_\text{r} + c_{\text{Al-e}} C_\text{r} V_\text{r}^2 \ , \tag{4.8}$$

$$\Sigma_{\text{film}} = a_{\text{film}} + b_{\text{film}} V_\text{r} + c_{\text{film}} C_\text{r} \ . \tag{4.9}$$

Numerical values for electrolytic and PP film capacitors were obtained by means of a multi-parametric least square fitting of the data shown in **Fig. 4.4** (mean error 7.7 %, standard deviation 3.9 %) and are listed in **Tab. 4.3**.

EMI Capacitors

EMI suppression capacitors on the mains supply side of a power converter must comply with the applicable EMC directives and standards, such as IEC 60384-14 [124]. Depending on the safety class (X1-X3 for line-to-line and Y1-Y4 for line-to-ground capacitors), different degrees of safety requirements concerning overvoltages, (mains) transients and inflammability must be met [124]. Although this implies higher capacitor costs and a potentially more complex cost structure, the simple (unit) cost models

$$\Sigma_{\mathrm{X2}} = a_{\mathrm{X2}} + c_{\mathrm{X2}} C_{\mathrm{r}} \ , \tag{4.10}$$

$$\Sigma_{\mathrm{Y2}} = a_{\mathrm{Y2}} + c_{\mathrm{Y2}} C_{\mathrm{r}} \ , \tag{4.11}$$

are proposed, which imply that the variable costs scale with the capacitance C_{r}. The models do not take into account varying safety classes or rated voltages since X2/Y2-ratings are usually sufficient for a wide range of applications and the availability of different voltage ratings is often strongly limited. **Tab. 4.3** suggests numerical values for the model parameters based on fitted manufacturer data (set of $N_{\mathrm{pop}} = 10$ data samples, mean error 7.1 %, standard deviation 4.6 %). The higher specific price per capacitance when compared to the power capacitors can clearly be seen.

4.3.4 Cooling Systems

Heat Sinks

The costs of heat sinks generally depends on the base material, volume and weight as well as the manufacturing and engineering costs. **Fig. 4.5(a)** shows manufacturer prices of different types of off-the-shelf aluminum heat sinks. Comparing the weight of the heat sinks and taking into account the approximate world market price for aluminum ($\approx$1.4 €/kg, as of Nov. 2015), it can be deduced that (for Al heat sinks) the costs only poorly scale with the weight (e.g. hollow-fin is light in weight but the most expensive) and that the total costs must hence largely be a result of the manufacturing processes. However, the analysis of the data in **Fig. 4.5(a)** as well as additional distributor prices show a strong linear dependence between price and volume for each type of heat sink. Consequently, the following cost model is proposed,

$$\Sigma_{\mathrm{sink}} = \Sigma^{\mathrm{fc}}_{\mathrm{sink},x} + \sigma_{\mathrm{sink},x} V_{\mathrm{sink}} \ , \tag{4.12}$$

where $\sigma_{\mathrm{sink},x}$ is the specific costs per volume depending on the heat sink type. $\Sigma^{\mathrm{fc}}_{\mathrm{sink},x}$ are fixed costs which can result from additional engineering work and processing steps which are independent from the heat sink volume (e.g. drilling holes for fan mounting). For the considered heat sink data, no significant fixed costs have been identified. The corresponding values for $\sigma_{\mathrm{sink},x}$ are listed in **Tab. 4.4** (mean error 0.4 %; standard deviation 0.2 %).

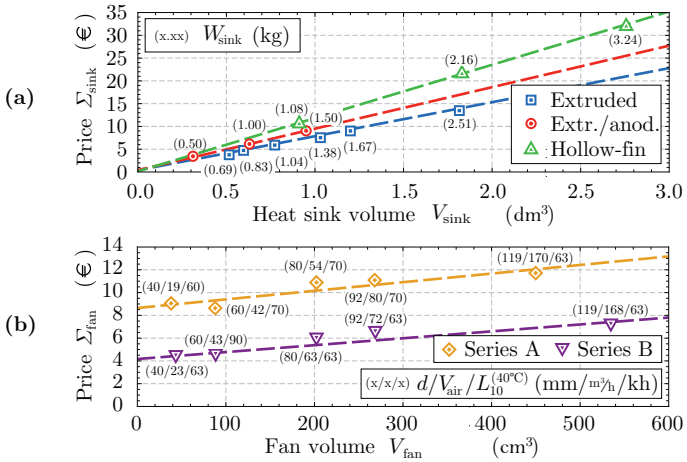


Fig. 4.5: **(a)** Unit prices of off-the-shelf extruded, extruded/anodized and hollow-fin aluminum heat sinks (MOQ = 10 000). W_{sink} denotes the heat sink weight. **(b)** Unit prices of two standard 12 V axial DC fan series without additional features from two leading manufacturers (MOQ = 10 000). d is the fan diameter, V_{air} the maximum air flow and $L_{10}^{(40\,^\circ\text{C})}$ denotes the life expectancy (90 % survival rate at continuous operation and 40 °C ambient). The figures further depict the corresponding curves of the cost models (4.12), (4.13) based on the fitted parameters in **Tab. 4.4**.

Tab. 4.4: Proposed numerical values for the heat sink and fan cost model (4.12),(4.13), based on data provided by three manufacturers (MOQ = 10 000).

Heat sink type:	**Extruded** [1]	**Extruded/ anodized** [1]	**Hollow-fin** [2]
$\Sigma^{\text{fc}}_{\text{sink},x}$ (€/unit)	0.23	0.25	0.17
$\sigma_{\text{sink},x}$ (€/dm³)	7.69	9.30	11.94
Fan series:	**A** [3]	**B** [4]	
$\Sigma^{\text{fc}}_{\text{fan},x}$ (€/unit)	8.78	4.19	
$\sigma_{\text{fan},x}$ (€/cm³)	$7.69 \cdot 10^{-3}$	$6.18 \cdot 10^{-3}$	

[1] Fischer Elektronik SK85x [2] Fischer Elektronik LA7x

[3] EBM Papst {412J, 612NN, 8312, 3312, 4312}

[4] Sanyo {109P0412B3, 109R0612D4, 109P0812H2, 9G0912M2, 9G1212H1}

Fans

Empirical analysis of distributor prices for standard axial DC compact fans generally shows large price offsets and only weak dependencies from the fan power (maximum airflow) and size. This finding is also confirmed by the obtained manufacturer data shown in **Fig. 4.5(b)**. According to manufacturers, the dominant cost factors of DC compact fans are the bearings and their lubricants, whose costs increase only slowly with growing fan size. Furthermore, the engineering and assembly costs (fully automated) are similar for all fans and thus additionally contribute to the high fixed costs. Finally, also the costs for the motor electronics is relatively constant as often the same or very similar designs and components are used for wide ranges of the fan power. With reference to the fan series considered in the case studies (see Chapter 5 and Chapter 6), it was found that the fan price is often constant for a given fan size independent from the fan power. The price differences between the two manufacturers depicted in **Fig. 4.5(b)** can partly be explained by the higher input voltage and temperature (more expensive lubricant) range of manufacturer B, while also different plant locations and price policies can have an impact.

Based on the above analysis, a simple linear cost model is proposed,

$$\Sigma_{\text{fan}} = \Sigma_{\text{fan},x}^{\text{fc}} + \sigma_{\text{fan},x} V_{\text{fan}} \ , \tag{4.13}$$

with $\Sigma_{\text{fan},x}^{\text{fc}}$ modeling the fixed costs and $\sigma_{\text{fan},x}$ the volume dependence. Numerical values based on least square fits (mean error 4.9 %, standard deviation 3.0 %) can be found in **Tab. 4.4**. The main purpose of the model is to show that physical factors, such as the volume or fan power have only a moderate impact on the fan price. With respect to a converter optimization it is, however, recommended to use the specific discrete price data from the manufacturers for each of the considered fans rather than relying on the model (4.13).

4.3.5 PCBs and Auxiliary Electronics

PCBs

The prices for PCBs generally depend on a multitude of physical variables. In order to reduce the model complexity and to focus on the most important criteria which are the PCB area, the number of layers

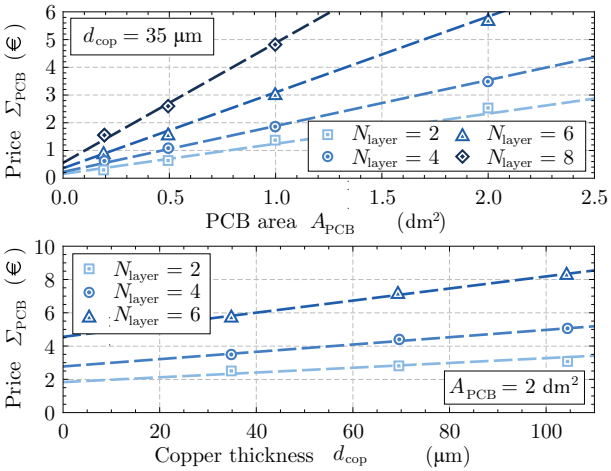


Fig. 4.6: Manufacturer price data (MOQ = 10 000) of standard PCBs (FR4 TG 130 °C 1.55 mm, drills > 0.3 mm, no blind/buried vias and controlled impedances, track width/spacing/annular ring > 0.15 mm, E-test, IPC-A-600G class 2). The figures further depict the corresponding curves of the cost model (4.14) based on the fitted parameters listed in **Tab. 4.5**.

and the copper thickness, standard PCBs with fixed and typical values for the remainder of the variables are considered:

- FR4 TG 130 °C 1.55 mm base material;
- No blind/buried vias and controlled impedances;
- Drills > 0.3 mm, track width/spacing/annular ring > 0.15 mm;
- HAL lead-free surface finish, white marking print and green solder mask on both sides;
- E-test, IPC-A-600G class 2 quality standard.

Based on these assumptions, the price data depicted in **Fig. 4.6** was requested from a PCB manufacturer. The linear dependence of the unit price from the PCB area and the copper thickness is clearly visible, whereas the number of layers has a quadratic impact. The latter can be explained with additional required processing steps and the generally higher complexity of multilayer PCBs [125]. Samples of the acquired

Tab. 4.5: Identified numerical values for the PCB cost model (4.14) based on manufacturer data [1)] for MOQ = 10 000.

	a_x	b_x	c_x
A_{PCB}	$0.407\,€^{1/3}$	$3.240\,€^{1/3}/\mathrm{dm}^2$	
d_{cop}	$8.489\,€^{1/3}$	$67.947 \cdot 10^{-3}\,€^{1/3}/\mu\mathrm{m}$	
N_{layer}	$29.409 \cdot 10^{-3}\,€^{1/3}$	$-2.779 \cdot 10^{-3}\,€^{1/3}$	$1.829 \cdot 10^{-3}\,€^{1/3}$

[1)] All data from MultiCB

price data were compared to prices offered by other manufacturers and found to be in a similar range with maximum deviations of ±15 %.

Based on the preceding analysis, the following cost model for standard PCBs is proposed,

$$\Sigma_{\mathrm{PCB}} = (a_{A_{\mathrm{PCB}}} + b_{A_{\mathrm{PCB}}} A_{\mathrm{PCB}}) \cdot (a_{d_{\mathrm{cop}}} + b_{d_{\mathrm{cop}}} d_{\mathrm{cop}}) \cdot (a_{N_{\mathrm{layer}}} + b_{N_{\mathrm{layer}}} N_{\mathrm{layer}} + c_{N_{\mathrm{layer}}} N_{\mathrm{layer}}^2)\,, \tag{4.14}$$

where A_{PCB} denotes the PCB area, d_{cop} the copper thickness (all layers) and N_{layer} the number of layers. The corresponding fitted numerical parameter values are listed in **Tab. 4.5** (mean error 4.1 %; standard deviation 3.9 %).

Auxiliary Electronics

Power electronic converters usually rely on a multitude of different electronic components such as sensors, gate drivers and embedded microcontrollers which enable the proper functioning of the device. Due to the vast variety of such (mostly) ICs, developing detailed cost models would pose an involved and time-consuming task. It is hence suggested to estimate the approximate costs based on distributor data, which is for ICs often provided for high MOQs. For many investigations and optimization tasks the amounts and types of ICs and other electronic components do not change, i.e. do not represent any design variables and are thus fixed costs. Therefore, the proposed approach is pragmatic yet meaningful as it provides a rough idea of the fixed costs but does not modify the relative results of the optimization. The approach is exemplified in the case studies of this thesis (Chapter 5 and Chapter 6).

4.4 Conclusion and Outlook

Permanent cost reduction is a key strategy for industries to maintain a sustainable advantage in competitive markets. The main objective of this chapter is to make the cost dimension available to the MOO-based virtual prototyping routine proposed in this thesis. Thereby, more comprehensive and industry-relevant results become attainable. A further intention of this chapter is to provide an analysis tool which helps broaden the sensitivity and awareness regarding costs in academic research.

A first step of a systematic approach towards cost considerations is presented by proposing component cost models for power semiconductors, inductors, capacitors, cooling systems and PCBs for switched-mode power converters with an approximate rated power of 1-50 kW. Numerical reference values for the model parameters are presented based on empirically collected manufacturing data for high order quantities. It was found that most of the data can be fitted with sufficient accuracy based on simple cost models where intuitive physical quantities are the model variables.

Future work could include the development of additional models for further relevant components such as the converter housings. The major challenge for additional and more detailed cost models is, however, imposed by the data acquisition. Furthermore, due to the nature of costs and prices, the presented data must be updated on a regular basis. The frequent publication of standardized cost parameters by an industry consortium, such as ECPE, would be of great assistance here.

As a final remark, the author would like to emphasize that the intention of this chapter is to provide an additional analysis tool to enhance the understanding of the trade-offs in converter design and power electronics in general. However, it is not proposed that future academic research activities should be driven by costs only. It is undisputed that one of the core competencies and opportunities of academia is the freedom to conduct research in areas whose short-term practical relevancy is low but might enable unforeseen technological revolution and progress in the long-term.

5

Case Study I: DC/DC Converter System

THIS chapter presents the first case study of this thesis in which the proposed virtual prototyping routine is employed. In this study, isolated bidirectional Si and SiC DAB concepts for a 5 kW 100-700 V input voltage range DC microgrid application are investigated. Two different DAB topologies are analyzed: a conventional 3-level DAB topology (3LDAB) is compared to a more complex 5-level DAB (5LDAB) where the latter allows for lower rms currents within the given voltage range. Both topologies either employ Si IGBTs or SiC MOSFETs. A systematic η-ρ-σ Pareto optimization is carried out evaluating the efficiency, power density and the costs in order to identify the most attractive concept. A hardware prototype is presented in order to verify the accuracy of the employed models as well as the usefulness of the virtual prototyping routine. The case study presented in this chapter is based on the work in [82].

This paper is organized as follows: the background and motivation of the case study are presented in Section 5.1. Section 5.2 reasons the selection of the topologies, modulation schemes and components. Section 5.3 presents the employed models whose accuracy is proven in Section 5.4 using a hardware prototype. The modeling framework is subsequently incorporated into the design and optimization routine presented in Section 5.5. Finally, the resulting optimized converter concepts are comprehensively analyzed and compared in Section 5.6.

5.1 Motivation

Due to the consequences of climate change and the scarcity of resources ongoing efforts have been made to increase the share of renewable energies in the mix of electricity generation. As a result, the number of installed (distributed) renewable energy sources has rapidly increased during the past decade. Against this background, the implementation of DC microgrids as depicted in **Fig. 5.1** has been proposed for both residential and commercial applications [126–132]. Such DC microgrids are (partly) powered by PV and fuel cell energy sources where the corresponding DC power can be used to directly supply the local loads via a DC bus. Typical DC loads are a wide range of household appliances, battery storage systems, electric vehicles (EV) and IT equipment in telecom and data center applications. Expected advantages in contrast to a conventional AC energy system are an increased reliability, stability and efficiency at system level. The DC microgrid architecture can be implemented in residential and commercial sites as well as ships and future aircraft. If equipped with smart meters and an intelligent load management algorithm the DC microgrids may form a key element in future smart grid systems [133, 134].

As highlighted in **Fig. 5.1**, a DC microgrid is comprised of numerous DC/DC converters which must meet various requirements, such as:

- *Galvanic isolation* for safety reasons and the suppression of circulating currents,
- *Bidirectional power flow*, e.g. for a battery interfacing application,
- *A wide input voltage range* due to the *I-V* characteristics of batteries, PV panels and fuel cells, and
- *Exceptional performance*, i.e. a high efficiency and power density at low costs.

This work proposes a highly functional DC/DC converter which meets all of the above requirements in a single system. Such a universal converter can be employed in a wide range of different applications within the DC microgrid. Suitable converter topologies to deal with a wide combined input-output voltage range, i.e. $\frac{V_{\mathrm{dc1,max}}}{V_{\mathrm{dc1,min}}} \cdot \frac{V_{\mathrm{dc2,max}}}{V_{\mathrm{dc2,min}}} \geq 2$, have extensively been discussed in literature. Whereas for *uni*directional isolated converters a multitude of converter topologies has been proposed, e.g. [135–138], most *bi*directional applications in literature are based

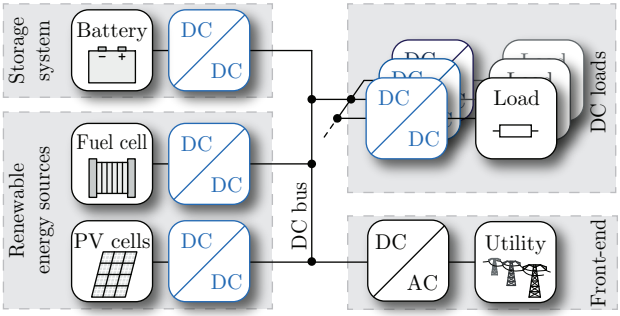


Fig. 5.1: DC microgrid architecture for residential or commercial applications as part of a future smart grid. This case study focuses on the DC/DC converters which are required to connect the renewable energy sources, the storage system and the DC loads to the common DC bus. A highly functional single converter type featuring galvanic isolation, bidirectional power flow and a wide input voltage range is proposed. It can universally be applied whereby increasing the system reliability, stability and efficiency.

on the (non-resonant) DAB topology as shown in **Fig. 5.2(a)**. In order to deal with the wide voltage range, most contributions propose the employment of a variable switching frequency [139, 140] and/or of advanced modulation schemes [16, 141] and/or of modified DAB circuits [142–144] instead of the originally proposed DAB with two full bridges (cf. **Fig. 5.2(a)**) and the conventional phase shift (CPM) modulation scheme [145].

Based on the observation that a DAB can generally be most efficiently operated if the input-output voltage ratio is close to the transformer turns ratio, i.e. $\frac{V_{\mathrm{dc1}}}{V_{\mathrm{dc2}}} \approx n$, a 5-level DAB (5LDAB) topology as shown in **Fig. 5.2(b)** was proposed in [17]. This topology extends the standard set of possible voltages which can be applied to the primary side of the transformer, $v_{\mathrm{ac1}} \in \{-V_{\mathrm{dc1}}, 0, +V_{\mathrm{dc1}}\}$, by $v_{\mathrm{ac1}} \in \{-\frac{V_{\mathrm{dc1}}}{2}, +\frac{V_{\mathrm{dc1}}}{2}\}$ when compared to the conventional 3-level DAB (3LDAB). This modification is expected to extend the primary voltage range where the converter can be operated with high efficiency.

The selection of a suitable converter concept and its dimensioning and adaption for a given application are key issues in industry. Based on a project in collaboration with an industrial partner, this case study aims at identifying a suitable converter concept and dimensioning for

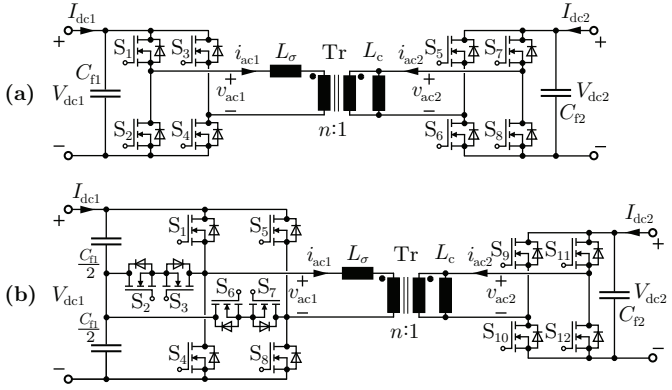


Fig. 5.2: Dual active bridge topologies for wide input voltage range applications. **(a)** 3-level DAB (3LDAB) with 2-level bridge legs consisting of 1200 V rated semiconductors on both the primary and secondary side of the transformer. **(b)** 5-level DAB (5LDAB) with 3-level T-type bridge legs on the primary variable-voltage side. The switches S_x with $x \in \{2, 3, 6, 7\}$ are 600 V rated whereas the remaining switches are 1200 V rated. Additional (small) filter inductors (not part of the considerations in this work) must be employed on the DC input and output side to block the AC ripple currents and to facilitate the control of the converter [146].

Tab. 5.1: Specifications of the universal DC/DC converter.

Rated power	P_r	5 kW
Input voltage range	$[V_{dc1,min}, V_{dc1,max}]$	$[100, 700]$ V
Output voltage	V_{dc2}	750 V
Maximum input current	$I_{dc1,max}$	22 A

a 5 kW 100-700 V input voltage range DC microgrid application (cf. **Tab. 5.1**) as discussed above. In particular, the conventional 3LDAB of **Fig. 5.2(a)** is compared to the 5LDAB of **Fig. 5.2(b)**. The 3LDAB is analyzed due to its relative simplicity and proven practical applicability which are preferred features in industry. The comparison to the 5LDAB is carried out in order to investigate whether the higher 5LDAB complexity (topology and modulation scheme) can be justified by a better achievable performance. Finally, the two concepts are analyzed for both Si IGBTs and SiC MOSFETs in order to compare the potential of advanced semiconductor technology against state-of-the-art low-cost

Tab. 5.2: Selection of the main components and materials.

Component	**3LDAB**	**5LDAB**
Si IGBTs	IKW25N120T2 [1)]	IKW30N60T / IKW25N120T2 [2)]
SiC MOSFETs	C2M0080120D [1)]	Scaled 600/1200 V C2M0080120D [3)]
Heat sink	Custom optimized Al heat sink	
Fans	NMB DC fan series 1x04KL-01W-By0	
Magnetics	Pack Feindrähte litz wire [30,355] µm 1-10 × stacked Epcos ferrite N87 E-/ELP-cores	
Capacitors	Epcos MKP film capacitors B3277x, $V_\mathrm{r} \in \{575, 1200\}$ V	

[1)] 2 / 1 units in parallel for primary / secondary side switches

[2)] 1 unit in parallel for all switches

[3)] scaled chip areas according to Section 5.5

technology in this application.

The comparison of the Si and SiC 3LDAB and 5LDAB concepts in this case study is based on a prior multi-objective optimization of the converter concepts including all relevant components. Three performance criteria are considered, i.e. the efficiency, power density and the costs. For this purpose, the virtual prototyping routine of this thesis is employed. On the one hand, the exclusive consideration of thoroughly optimized systems (instead of random non-optimized system designs) strongly increases the significance of the comparison. On the other hand, the concurrent consideration of multiple performance criteria instead of only a single criterion increases the comprehensiveness and enables a more complete picture of the concepts. Finally, the consideration of costs strongly increases the relevance of the investigations as costs are typically a key criterion in industry. The comparison of this approach to similar multi-objective optimizations found in literature [54–62, 64–68] reveals that only [66, 67] feature the same combination of incorporating three optimization criteria (others: two) and considering costs (see also Section 1.2 and Section 1.3). In [66,67], however, the numerical values and origin of the cost model parameters are not stated which considerably reduces the value for practicing engineers or researchers. This is in contrast to this case study which employs the cost modeling framework of Chapter 4 which provides explicit models and detailed numerical values for the parameters for each component type. Another main difference of the approach in this work to the above

cited contributions is the employment of advanced and experimentally verified loss and thermal models for all considered components. For this purpose the component modeling framework of Chapter 3 is used. Furthermore, a novel behavioral model which accurately predicts the non-linear switching transitions is proposed in this case study which enables the accurate calculation of the incomplete zero voltage switching (iZVS) losses.

5.2 Selection of Topologies, Modulation Schemes and Components

This section reasons the selection of the topologies and modulation schemes and details the employed components as listed in **Tab. 5.2** and their costs. In most cases, the cost models and data from Chapter 4 were utilized. Where other cost data were required, the same empirical methods were employed as discussed in Chapter 4 (list prices from manufacturers, large minimum order quantities MOQ $> 10\,\text{kpcs.}$).

5.2.1 Topologies and Modulation Schemes

This work investigates the 3LDAB and the 5LDAB depicted in **Fig. 5.2**. T-type instead of neutral-point-clamped (NPC) 3-level bridge legs are considered in the 5LDAB due to the two reasons below:

(i) A T-type bridge leg can be operated as a 2-level bridge leg. This means that switching directly between the negative and positive rail voltage without freewheeling in the intermediate state is possible provided that both 600 V switches are turned off, cf. **Fig. 5.2(b)**. This allows for higher duty cycles and a reduced control complexity.

(ii) In NPC bridge legs, residual charges in the semiconductor output capacitors occur on principle of the topology and despite complete ZVS operation [147]. As a result of these residual charges increased switching losses occur in NPC bridge legs which can be avoided when using T-type bridge legs.

The main motivation of considering the 5LDAB topology derives from the observation that a DAB can generally be most efficiently operated if the input-output voltage ratio is close to the transformer turns ratio,

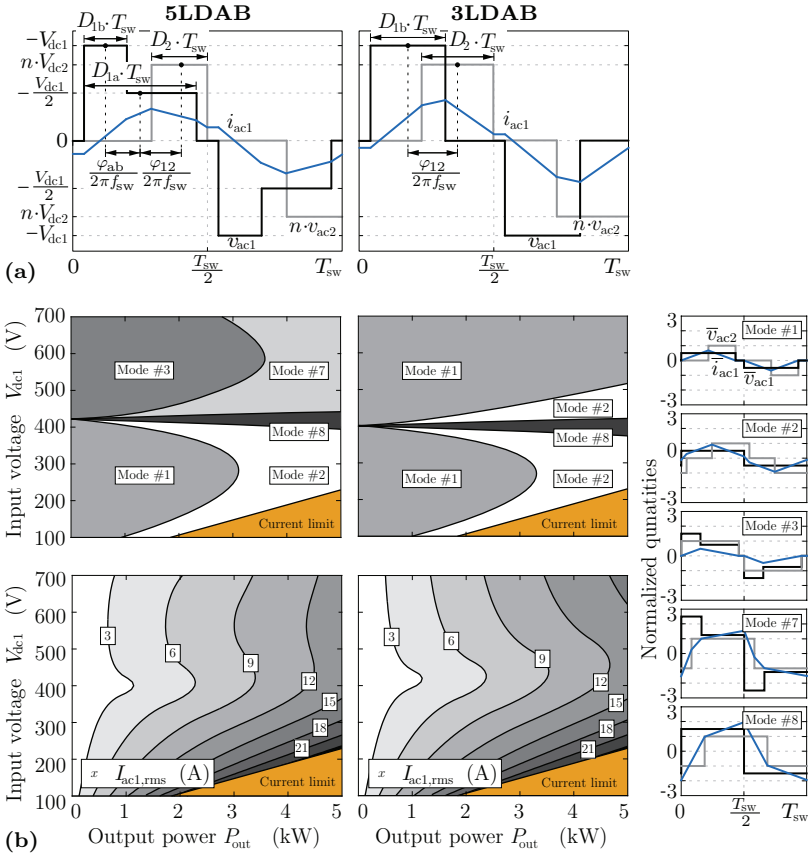


Fig. 5.3: DAB modulation schemes. **(a)** Generalized waveforms with ideal, i.e. instantaneous, switching transitions and definition of the respective control variables $D_{1a}, D_{1b}, D_2, \varphi_{ab}$, and φ_{12}. The simpler 3LDAB topology entails a lower number of available control variables, i.e. $D_{1a} = D_{1b}$ and $\phi_{ab} = 0$. **(b)** Minimized transformer rms currents $I_{ac1,rms}$ obtained by solving (5.1) (values for n and L_σ from **Tab. 5.7**; currents in L_c neglected). Depending on the operating point, different control modes/waveform patterns are optimal where in the lower voltage regime, both converters are similarly operated employing the same control modes. Due to the higher control degree of freedom, the 5LDAB achieves a lower current stress in the higher voltage regime when compared to the 3LDAB.

i.e. $\frac{V_{\mathrm{dc1}}}{V_{\mathrm{dc2}}} \approx n$ [17]. The 5LDAB extends the standard 3LDAB set of possible voltages applied to the primary side of the transformer $v_{\mathrm{ac1}} \in \{-V_{\mathrm{dc1}}, 0, +V_{\mathrm{dc1}}\}$, by $v_{\mathrm{ac1}} \in \{-\frac{V_{\mathrm{dc1}}}{2}, +\frac{V_{\mathrm{dc1}}}{2}\}$. In case of a fixed output voltage V_{dc2}, this enables two instead of one input voltage regimes where the above condition can be met: consider a given turns ratio and a fixed output voltage, e.g. $n \cdot V_{\mathrm{dc2}} = 0.5 \cdot 750\,\mathrm{V} = 375\,\mathrm{V}$. In case of high input voltages $V_{\mathrm{dc1}} \approx 750\,\mathrm{V}$ the converter can apply $|v_{\mathrm{ac1}}| = \frac{V_{\mathrm{dc1}}}{2} \approx 375\,\mathrm{V}$ to the primary side of the transformer while at low input voltages $V_{\mathrm{dc1}} \approx 375\,\mathrm{V}$ the converter uses $|v_{\mathrm{ac1}}| = V_{\mathrm{dc1}} \approx 375\,\mathrm{V}$ in order to meet $\frac{V_{\mathrm{dc1}}}{V_{\mathrm{dc2}}} \approx n$.

The differing number of possible voltage levels of the 3LDAB and 5LDAB is reflected by three and five available control variables $\vec{\Xi}^*$, respectively as depicted in **Fig. 5.3(a)**. This work employs the optimized 3LDAB modulation scheme proposed in [16] and the extended 5LDAB scheme proposed in [17]. The modulation schemes choose the control parameters $\vec{\Xi}^*$ so as to minimize the transformer rms current,

$$\vec{\Xi}^* = \arg\min_{\vec{\Xi}} \; I_{\mathrm{ac1,rms}}(n, L_\sigma, \vec{\Lambda}, \vec{\Xi}) \;, \tag{5.1}$$

$$\begin{aligned} &0 \le D_{1\mathrm{a}} \le 0.5 \;, \quad && D_{1\mathrm{b}} - D_{1\mathrm{a}} \le \varphi_{\mathrm{ab}}/\pi \le D_{1\mathrm{a}} - D_{1\mathrm{b}} \;, \\ &0 \le D_{1\mathrm{b}} \le D_{1\mathrm{a}} \;, && -1 \le \varphi_{12}/\pi \le 1 \;, \\ &0 \le \; D_2 \; \le 0.5 \;, \end{aligned}$$

for a given transformer turns ratio n, series inductance L_σ and any given operating point vector $\vec{\Lambda} = (V_{\mathrm{dc1}}, V_{\mathrm{dc2}}, P_{\mathrm{out}})^\top$. Both modulation schemes allow for ZVS in the entire operating range. **Fig. 5.3(b)** shows the resulting operating point-dependent minimized transformer rms currents assuming similar values of n and L_σ. Inspection reveals that in the lower voltage regime ($V_{\mathrm{dc1}} < n \cdot V_{\mathrm{dc2}}$), the modulation schemes of the 3LDAB and 5LDAB are identical. For the reasons stated above, the 5LDAB scheme does not exploit the additional voltage levels. Consequently, nearly equal rms currents result for both concepts. Contrary, in the higher voltage regime ($V_{\mathrm{dc1}} > n \cdot V_{\mathrm{dc2}}$), the 5LDAB achieves significantly lower rms currents which is a direct benefit of the application of the additional voltage levels.

The above analysis provides the main motivation for the comparison of the 3LDAB and 5LDAB. On the one hand, the 5LDAB seems to be better suited for the wide voltage range application considered in this work due to lower achievable rms currents. On the other hand, the proposed virtual prototyping routine is employed to clarify whether

the lower achievable rms currents of the 5LDAB translate into a better converter performance (efficiency, power density and component costs) when compared to the 3LDAB. If a significantly better performance results, the higher complexity (component count and modulation scheme) of the 5LDAB concept may be justified.

5.2.2 Semiconductors

The main focus of this work is set on the investigation of the achievable converter performance based on vertical SiC V-DMOSFETs. The reference switch was chosen to be the discrete 80 mΩ 1200 V TO-247-3-packaged SiC MOSFETs from Wolfspeed (C2M0080120D, 8 €/unit, total/active chip areas of $A_{\text{chip}} = 0.1042\,\text{cm}^2 / A_{\text{chip,a}} = 0.0819\,\text{cm}^2$) In order to obtain a benchmark for the still expensive commercial SiC MOSFETs, both converter concepts are additionally analyzed considering 600 V / 1200 V IGBTs from Infineon (IKW30N60T / IKW25N120T2, 1.6 / 2.4 €/unit). Note that Si super-junction (SJ) MOSFETs are not considered as a further alternative. In fact, inspection of the component characteristics of the chosen SiC MOSFETs and state-of-the-art Si SJ MOSFETs reveals a clear inferiority of SJ MOSFETs which renders the incorporation of such devices in the optimization obsolete:

- *ZVS capabilities*: achieving both a high converter efficiency and power density usually requires soft-switching techniques such as ZVS. In this regard, SiC V-DMOSFETs offer a twofold advantage over Si SJ MOSFETs:

  (i) On the one hand, for SiC V-DMOSFETs the charging / discharging process of the parasitic output capacitors is almost lossless whereas for SJ MOSFETs up to 50 % of the stored energy can be lost despite ZVS ([91, 92], cf. Section 3.1).

  (ii) On the other hand, the relative output capacitance $C_{\text{oss,rel}}$ per chip area is much lower for SiC (cf. **Tab. 5.3**). This is especially important when dealing with a wide power and input voltage range (as for the application at hand) where the available charge during the dead time T_{d} to achieve (complete) ZVS strongly varies [139].

- *Breakdown voltages*: contrary to Si MOSFETs, high-performance SiC MOSFETs are widely available up to a breakdown voltage

of 1200 V. For the given voltage specifications (cf. **Tab. 5.1**), this enables the employment of standard 2-level bridge legs and T-type 3-level bridge legs instead of NPC 3-level bridge legs in the investigated 3LDAB and 5LDAB.

- *Robustness*: although the modulation schemes proposed in this work enable ZVS in all operating points, hard-switching transitions can still occur, e.g. during transients. In such an event, SiC MOSFETs are much more robust than most Si counterparts. This is mainly due to the superior SiC body diodes whose reverse recovery effect is negligible whereas the large occurring reverse recovery currents of typical SJ MOSFETs can lead to high switching losses and eventually to the destruction of the device.
- *Costs*: a solution based on 600 V Si SJ MOSFETs featuring the same on-state resistance as a solution based on 1200 V SiC MOSFETs requires approximately three times the chip area: a factor of 1.5 higher areas because of the higher specific resistance and a factor of 2 to achieve the same breakdown voltage. As evident from the specific costs per chip area σ_{chip} shown in **Tab. 4.1**, this renders the Si solution more expensive, i.e.

$$\frac{\sigma_{\text{chip}}^{\text{SiC MO}}}{\sigma_{\text{chip}}^{\text{Si}}} = \frac{72.01\,€/\text{cm}^2}{27.34\,€/\text{cm}^2} \approx 2.63 < 3\,. \tag{5.2}$$

Approach

For the 3LDAB topology, two of the considered C2M0080120D SiC MOSFET units are employed in parallel for all primary side switches and one unit in parallel for all secondary side switches (this selection corresponds to the configuration of the implemented hardware prototype introduced in Section 5.4). With the intention of performing a comparison which is as fair as possible, the 5LDAB total chip area is chosen so as to yield equal semiconductor costs. As a consequence of this approach, a continuous scaling scheme of the main semiconductor properties as a function of the chip size must be established since only a few other chip sizes within the considered SiC MOSFET series are available. Furthermore, the 5LDAB also employs 600 V switches (cf. **Fig. 5.2(b)**) and therefore an additional scaling of the semiconductor properties with the breakdown voltage must be accomplished. The selected 3LDAB 80 mΩ 1200 V SiC MOSFET serves as the reference

Tab. 5.3: Figures of merits of different semiconductors. Some of the cost data are are taken from **Tab. 4.1**.

Semiconductor	Type / $V_{\mathrm{ds,max}}$ (V)	$R_{\mathrm{ds,on}} \cdot A_{\mathrm{chip,a}}$ ($\mathrm{m\Omega \cdot cm^2}$)	$R_{\mathrm{ds,on}} \cdot Q_{\mathrm{oss}}$ [3] ($\mathrm{m\Omega \cdot nC}$)	σ_{chip} ($\mathrm{€ \cdot cm^{-2}}$)
C2M0080120D	SiC / 1200	6.55	5408	72.01
Scaled C2M [1]	SiC / 600	4.93	6462	64.81
CoolMOS SJ C7 [2]	Si / 650	10.00	34190	27.34
GS66508T	GaN / 650	6.78	3135	52.55

[1] based on (5.4)-(5.8) [2] average values of series [3] @ $V_{\mathrm{ds}} = 400\,\mathrm{V}$

switch for both tasks and is denoted by $(^*)$ in the following equations. A summary of the calculated switch properties and costs along with a comparison to a state-of-the-art SJ MOSFET series and a preproduction GaN HEMT is depicted in **Tab. 5.3**.

Whereas the scaling laws of the physical properties are derived in the sections below, the scaling of the costs can be determined with the presented cost model of Section 4.3,

$$\Sigma_{\mathrm{SC}} = 0.55\,€ + \sigma_{\mathrm{chip}}^{x} \cdot A_{\mathrm{chip}} \,. \tag{5.3}$$

The package costs and specific costs per chip area of the C2M0080120D are taken from **Tab. 4.1**. The specific costs per chip area of the scaled 600 V switches are assumed to be 10 % lower than for the original 1200 V switch due to similar findings for 600 / 1200 V IGBTs in Section 4.3.

Scaling with A_{chip}

The study of fundamental semiconductor physics [148,149] suggests the use of an inverse scaling law for the on-state resistance $R_{\mathrm{ds,on}}$ and the thermal junction-to-case resistance $R_{\mathrm{th,j\text{-}c}}$ as a function of the total and active chip area A_{chip} and $A_{\mathrm{chip,a}}$, respectively,

$$R_{\mathrm{ds,on}}(A_{\mathrm{chip,a}}) = R^*_{\mathrm{ds,on}} \cdot \frac{A^*_{\mathrm{chip,a}}}{A_{\mathrm{chip,a}}} \,, \tag{5.4}$$

$$R_{\mathrm{th,j\text{-}c}}(A_{\mathrm{chip}}) = R^*_{\mathrm{th,j\text{-}c}} \cdot \frac{A^*_{\mathrm{chip}}}{A_{\mathrm{chip}}} \,. \tag{5.5}$$

On the other hand, the parasitic capacitances C_{gs}, C_{gd} and C_{ds} scale linearly,

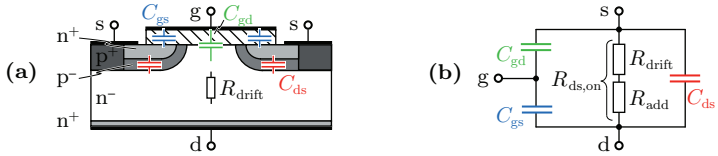


Fig. 5.4: Schematic structure of a vertical DMOSFET unit cell depicting the parasitic capacitances **(a)** and the equivalent circuit model of the switch in the ohmic region **(b)**. The on-state resistance $R_{\mathrm{ds,on}}$ is the sum of the resistance R_{drift} of the n^- drift layer and an additional resistance R_{add} mainly originating from the modulated channel and the terminals. The relevant output capacitance for soft-switching calculates as $C_{\mathrm{oss}} = C_{\mathrm{gd}} + C_{\mathrm{ds}}$.

$$C_x(A_{\mathrm{chip,a}}) = C_x^* \cdot \frac{A_{\mathrm{chip,a}}}{A^*_{\mathrm{chip,a}}} \quad \text{with } x \in \{\mathrm{gs},\, \mathrm{gd},\, \mathrm{ds}\}\ . \tag{5.6}$$

The underlying assumptions of (5.4)-(5.6) are a fixed MOSFET unit cell geometry as depicted in **Fig. 5.4** and a constant cell density per area.

Scaling with $V_{\mathrm{ds,max}}$

For the following analysis, the active chip area is held constant, i.e. $A_{\mathrm{chip,a}} = A^*_{\mathrm{chip,a}}$. If the MOSFET is scaled to a lower breakdown voltage $V_{\mathrm{ds,max}}$, the drift layer thickness can be reduced while increasing its doping concentration $N_{\mathrm{d,drift}}$ [148,149]. This results in a significantly reduced contribution of the drift layer resistance according to

$$R_{\mathrm{drift}}(V_{\mathrm{ds,max}}) = R^*_{\mathrm{drift}} \cdot \left(\frac{V_{\mathrm{ds,max}}}{V^*_{\mathrm{ds,max}}} \right)^{\frac{5}{2}}\ , \tag{5.7}$$

to the total on-state resistance $R_{\mathrm{ds,on}}$ (cf. **Fig. 5.4**). Here, a contribution of $\frac{R^*_{\mathrm{drift}}}{R^*_{\mathrm{ds,on}}} = 30\,\%$ was assumed for the original switch based on information provided by Wolfspeed. The change of $N_{\mathrm{d,drift}}$ also affects the capacitances C_{gd} and C_{ds},

$$C_x(V_{\mathrm{ds,max}}) \approx C_x^* \cdot \left(\frac{V_{\mathrm{ds,max}}}{V^*_{\mathrm{ds,max}}} \right)^{-\frac{2}{3}} \quad \text{with } x \in \{\mathrm{gd},\, \mathrm{ds}\}\ , \tag{5.8}$$

where the influence of the gate oxide on C_{gd} was neglected. Note that these capacitances form the output capacitance $C_{\mathrm{oss}} = C_{\mathrm{gd}} + C_{\mathrm{ds}}$ which is a key figure for ZVS considerations.

5.2.3 Cooling System

Custom aluminum heat sinks in combination with a range of standard axial DC compact fans from NMB (series 1x04KL-01W-By0, $x \in \{0, 2, 4, 6\}$, $y \in \{3, 4, 5\}$) are considered. Assuming extrusion for the manufacturing of the heat sinks, the cooling system costs Σ_{CS} can be calculated using the model of Section 4.3,

$$\Sigma_{\mathrm{CS}} = 7.69\,\text{€}/\mathrm{dm}^3 \cdot V_{\mathrm{sink}} + \Sigma_{\mathrm{fan}}\ , \tag{5.9}$$

with V_{sink} being the heat sink volume. The fan unit costs of the individual fans were requested from the manufacturer for MOQ = 10 000 units. The costs remain in a relatively narrow range $\Sigma_{\mathrm{fan}} \in [5.23, 6.63]$ € despite the widely varying fan power. This characteristic is typical and is further discussed in Section 4.3. Note that the entire range of considered cooling systems is optimized utilizing the procedure described in Section 2.2.1.

5.2.4 Magnetics

The magnetic components of the investigated topologies are purely AC excited. Therefore, the selection of core and winding materials which are suitable for HF operation is mandatory. The complete range of N87 ferrite E- and ELP-cores from Epcos and litz wires from Pack Feindrähte with strand diameters d_{strand} between 30 and 355 µm are considered. The costs Σ_L can be estimated with the data in Section 4.3,

$$\Sigma_L = \frac{1}{0.75} \cdot \Big\{ N_{\mathrm{stack}} \cdot 0.08\,\text{€} + 7.50\,\text{€}/\mathrm{kg} \cdot W_{\mathrm{core}} + \big(\sigma_{\mathrm{wdg,litz}}(d_{\mathrm{strand}}) + 7.00\,\text{€}\big) \cdot W_{\mathrm{wdg}} + 1.00\,\text{€} \Big\}\ , \tag{5.10}$$

where $\sigma_{\mathrm{wdg,litz}}$ are the specific winding costs for litz wire depending on the strand diameter d_{strand} as listed in **Tab. 4.2**.

Tab. 5.4: Cost data and number of employed gate drivers.

Circuit:	**GD**	$\mathbf{GD}_{\mathbf{iso}}^{\mathbf{single}}$	$\mathbf{GD}_{\mathbf{iso}}^{\mathbf{shared}}$
$\boldsymbol{\Sigma_x}$ **(€)**	1.7	3.4	2.2
# 3LDAB	4	4	0
# 5LDAB	4	4	4[1)]

[1)] 600 V switches S_x with $x \in \{2, 3, 6, 7\}$

5.2.5 Capacitors

Polypropylene MKP film capacitors from Epcos (series B3277x) with a rated voltage of $V_\mathrm{r} \in \{575, 1200\}$ V are used. Using the cost model of Section 4.3, the unit costs Σ_C can be estimated with

$$\Sigma_C = -1.02\,€ + 2.43 \cdot 10^{-3}\,€/\mathrm{V} \cdot V_\mathrm{r} + 54.96 \cdot 10^{-3}\,€/\mu\mathrm{F} \cdot C_\mathrm{r}\ , \quad (5.11)$$

where C_r denotes the rated unit capacitance.

5.2.6 PCB

A 4-layer control and a 6-layer power PCB with estimated total costs of $\Sigma_\mathrm{PCB} = 7\,€$ are included into the analysis. The respective dimensions are assumed to be same as for the implemented prototype which is shown in Section 5.4.

5.2.7 Auxiliary Electronics

The costs of the control, gate driver and sensor electronics Σ_AUX were estimated based on the implemented prototype and distributor prices for large order quantities, i.e. usually MOQ > 10 000 units,

$$\Sigma_\mathrm{AUX} = 40\,€ + \Sigma_\mathrm{GD}^x\ , \quad (5.12)$$

with $\Sigma_\mathrm{GD}^{\{\mathrm{3LDAB,\ 5LDAB}\}} = \{20.4, 29.2\}\,€$ being the total gate driver costs based on **Tab. 5.4**. Note that only the minimally required electronics were considered in (5.12) whereas the implemented prototype employs additional circuitry for research purposes.

5.3 Modeling

This chapter details the models which are employed in this case study. The discussion mainly focuses on the behavioral model whereas the majority of component models are derived from the general models presented in Chapter 3.

5.3.1 Behavioral Model

A behavioral model as depicted in **Fig. 5.5(a)** is proposed to synthesize the operating point-dependent waveforms. In a first step, the modulator executes the closed-form expressions derived in [16, 17] which yield the optimal control parameters $\vec{\Xi}^*(V_{\mathrm{dc1}}, V_{\mathrm{dc2}}, P_{\mathrm{mod}})$ solving (5.1). In a next step, the waveforms are synthesized in time domain where the strongly non-linear finite-speed switching transitions are modeled in detail (cf. **Fig. 5.5(b)**). The dynamics of the transitions are mainly governed by the charging/discharging of the parasitic layout and semiconductor output capacitances and the feedback of the resulting non-linear voltage on the currents in the magnetics. The corresponding differential equations are solved using the Euler forward integration method and a sufficiently small step size. Note that the modulator assumes ideal waveforms (cf. **Fig. 5.3(a)**) and thus neglects the switching transition time intervals which do not contribute to the active power transfer of the DAB. Therefore the modulator and waveform synthesis must be iterated using adjusted modulator power levels P_{mod} until the actual transferred power P_{out} of the synthesized waveform matches the reference P^*_{out}.

This case study distinguishes complete and incomplete ZVS (iZVS) transitions as shown in **Fig. 5.5(b)**. The analysis conducted in Section 3.1 shows that the latter occurs if the switched bridge leg current does not deliver sufficient charge within the adaptive dead time interval $T_{\mathrm{d}} \in [0, T_{\mathrm{d,max}}]$ to fully charge/discharge the involved output and layout capacitances. In this case, additional and non-negligible losses depending on the residual voltage ΔV occur. The proposed detailed modeling of the switching transition waveforms is therefore indispensable to accurately determine the amount of available charge and to identify complete/incomplete ZVS transitions. Note that many publications solely consider the sign of the switched current for this analysis (e.g. [142–144]). Such an approach may thus result in significantly underestimated losses. Publications which also employ charge-based ap-

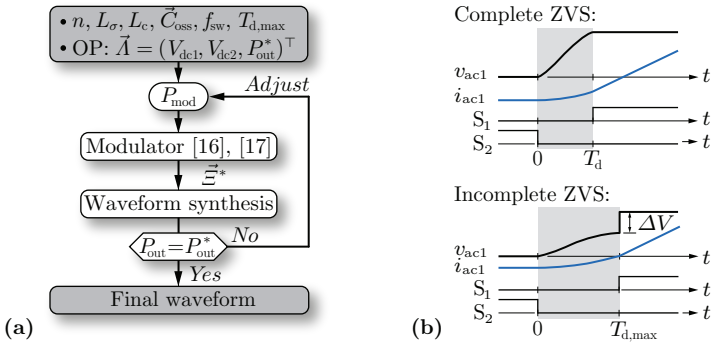


Fig. 5.5: Behavioral model. **(a)** Routine to synthesize the waveforms for a given operating point $\vec{\Lambda}$. **(b)** Examples of complete and incomplete ZVS transition waveforms in the primary side of the 3LDAB ($S_3 = 0$, $S_4 = 1$, $n \cdot v_{ac2} = 0$). The intervals highlighted in gray do not contribute to the active power transfer of the DAB.

proaches are found to be [139,150–152]. These approaches, however, are simplified when compared to the proposed behavioral model in this work and are thus likely to yield a reduced accuracy: the additional charge requirement for the parasitic layout capacitance $C_{par,tot}$ is neglected in all cited publications. Furthermore, only linear current and voltage waveforms are assumed during the switching transition in [139, 150, 151]. Finally, the approach in [152] is limited to stating the conditions for complete ZVS whereas the residual voltage ΔV cannot be predicted.

5.3.2 Semiconductors

Conduction Losses

The conduction losses P_c are computed considering the current- and junction temperature-dependent output characteristics $V_{ce}\big(i_{ce}(t), T_j\big)$ and $R_{ds,on}\big(i_{ds}(t), T_j\big)$, respectively, of the considered IGBT and MOSFET devices. Interpolated data sheet parameters are employed which in case of the SiC MOSFETs are scaled with the active chip area $A_{chip,a}$ according to (5.4). A gate voltage of $V_{gate} = 15\,\mathrm{V}$ was considered for all Si IGBTs and a gate voltage of $V_{gate} = 20\,\mathrm{V}$ for the SiC MOSFETs. Since the DABs are assumed to be operated with adaptive dead times $T_d \in [0, T_{d,max}]$, the off-state conduction losses in the MOSFET body

diodes are neglected.

Switching Losses

The occurring (regular) switching losses P_{sw} in case of complete ZVS are calculated using current-, voltage- and temperature-dependent switching loss energies. For the SiC MOSFET-based converters, the experimentally determined switching losses of the employed reference switch C2M0080120D of **Fig. 3.6** are used to calculate the MOSFET switching losses according to

$$\begin{aligned} P_{\mathrm{sw}}(I_{\mathrm{on/off}}, V_{\mathrm{on/off}}, T_{\mathrm{j}}) = f_{\mathrm{sw}} \cdot \frac{A_{\mathrm{chip,a}}}{A^*_{\mathrm{chip,a}}} \cdot \\ \sum_{i=1}^{N_{\mathrm{sw}}} \left[E^*_{\mathrm{sw,on}}\Big(- I_{\mathrm{on/off},i} \cdot \frac{A^*_{\mathrm{chip,a}}}{A_{\mathrm{chip,a}}}, V_{\mathrm{on/off}}, T_{\mathrm{j}}\Big) + \right. \\ \left. E^*_{\mathrm{sw,off}}\Big(I_{\mathrm{on/off},i} \cdot \frac{A^*_{\mathrm{chip,a}}}{A_{\mathrm{chip,a}}}, V_{\mathrm{on/off}}, T_{\mathrm{j}}\Big) \right] , \end{aligned} \tag{5.13}$$

with f_{sw} being the switching frequency and N_{sw} the number of full switching cycles (pairs of turn-on and turn-off transitions) of the considered switch during a switching period. Note that due to the symmetric operation of the DAB, pairs of turn-on and turn-off transitions with the same absolute values of the current $I_{\mathrm{on/off},i}$ occur. Furthermore, steady-state operation is assumed where the switched voltage $V_{\mathrm{on/off}}$ remains the same during a switching period. The switching loss model (5.13) includes a scaling scheme for the chip area based on the switched current density. Note that the voltage-dependent energies $E_{\mathrm{oss}}(V_{\mathrm{on/off}})$ in the output capacitances C_{oss} are part of the switching losses $E^*_{\mathrm{sw,on}}$ and $E^*_{\mathrm{sw,off}}$. However, it is not required to separately scale these energies as they are compensated by the sum of turn-on and turn-off losses in (5.13) (cf. **Fig. 3.6**). The scaling of the energies $E_{\mathrm{oss}}(V_{\mathrm{on/off}})$ is, on the other hand, required for the calculation of the iZVS losses described below.

Interpolated data sheet switching losses are employed for the IGBT-based converters.

Incomplete ZVS Losses

In addition to the regular switching losses P_{sw}, additional losses P_{iZVS} occur in case of iZVS as depicted in **Fig. 5.5(b)**. These additional losses

occur in the turning on switch and are partly due to the residual energy in the associated output capacitance $E_{\mathrm{oss}}(\Delta V)$ which is dissipated in the switch. In this case study, the additional iZVS losses are analytically calculated using the modeling framework for iZVS of Section 3.1 which also takes into account the parasitic layout capacitance $C_{\mathrm{par,tot}}$. Note that the involved semiconductor output capacitances C_{oss} are scaled with the chip area and maximum breakdown voltage based on (5.6), (5.8).

5.3.3 Cooling System

All cooling systems are optimized utilizing the cooling system design routine proposed in Section 2.2. The heat sink dimensioning takes into account the set of possible semiconductor arrangements which means that the minimum top surface is defined by the number and dimensions of the semiconductor packages.

5.3.4 Passives

The design of the magnetics is based on the loss models, thermal models and reluctance models presented in Section 3.3 and relies on the experimentally determined N87 core losses. The current-dependent losses P_C in the capacitors are calculated based on data sheet loss parameters of the considered capacitors.

5.3.5 PCB

The PCB losses P_{PCB} comprise the copper conduction losses and the FR4 dielectric losses. The former are calculated using the resistances measured for the PCB of the implemented prototype. The latter are estimated with

$$P_{\mathrm{FR4}} = \frac{\tan\delta_{\mathrm{FR4}}}{2\pi\, C_{\mathrm{PCB}}} \cdot \sum_n \frac{I^2_{\mathrm{FR4},(n)}}{n \cdot f_{\mathrm{sw}}} \ , \tag{5.14}$$

and are mainly significant at low power levels. In (5.14), $\delta_{\mathrm{FR4}} = 1.5\,\%$ is the loss tangent provided by the PCB manufacturer, C_{PCB} the effective PCB capacitance during a switching transition and $I_{\mathrm{FR4},(n)}$ the harmonics of the current which charges/discharges C_{PCB}. For simplicity reasons, constant currents during the charging/discharging intervals

(the dead time intervals) are assumed which deliver the required charge. Again, C_{PCB} is chosen based on the PCB of the implemented prototype.

5.3.6 Auxiliary Electronics

The losses of the auxiliary circuit P_{AUX} include the gate driver losses P_{GD}, the cooling system fan losses P_{CS} and the measured power consumption of the control and measurement electronics of the implemented prototype $P_{\mathrm{control}} = 3\,\mathrm{W}$,

$$P_{\mathrm{AUX}} = \frac{1}{\eta_{\mathrm{sup}}} \cdot \left(P_{\mathrm{GD}} + P_{\mathrm{CS}} + P_{\mathrm{control}}\right) , \tag{5.15}$$

where a relatively low auxiliary power supply efficiency of $\eta_{\mathrm{sup}} = 75\,\%$ is assumed. The gate driver losses P_{GD} are estimated with

$$P_{\mathrm{GD}} = \frac{A_{\mathrm{chip,a}}}{A^{*}_{\mathrm{chip,a}}} \cdot Q^{*}_{\mathrm{gate}} \cdot V_{\mathrm{gate}} \cdot f_{\mathrm{sw}} , \tag{5.16}$$

where $V_{\mathrm{gate}} = 20\,\mathrm{V}$ is the gate voltage and Q^{*}_{gate} the corresponding gate charge which is scaled with the chip area according to (5.6). The value for Q^{*}_{gate} can be found in the respective data sheets. Note that the formula (5.16) is most accurate for the switching of the Si IGBTs and hard-switching of the SiC MOSFETs. For soft-switching of the SiC MOSFETs, the switching mechanisms are slightly different since the Miller capacitance C_{gd} which is part of the output capacitance C_{oss} (cf. **Fig. 5.4**) is largely charged by the switched bridge leg current and not by the gate driver. This reduces the required gate charge in (5.16). However, the reduction of Q^{*}_{gate} strongly depends on the operating point and the switching dynamics and is thus difficult to estimate. Therefore, for simplicity, the model in (5.16) is also considered for soft-switching transitions of the SiC MOSFETs. Thereby, an overestimation of the gate driver losses by 25-40 % must be taken accepted which, however, is reasonable as the gate driver losses are generally low.

5.4 Experimental Verification

In the framework of this case study, a hardware prototype of a SiC MOSFET-based 3LDAB was implemented. The target volume and efficiency of the prototype were defined by an industrial partner. A maximum volume of $3\,\mathrm{dm}^3$ and an efficiency of $\eta > 98\,\%$ was demanded.

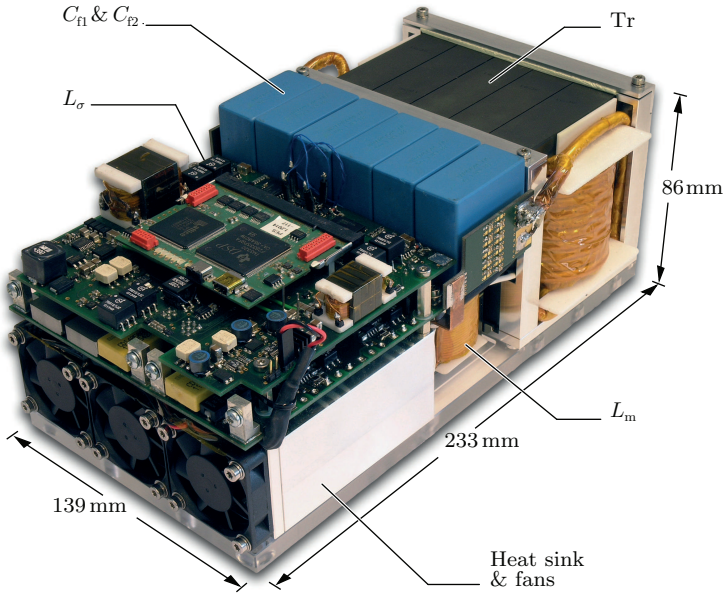


Fig. 5.6: Photograph of the implemented 3LDAB hardware prototype. The converter operates at a switching frequency of $f_{sw} = 48\,\text{kHz}$ and achieves a maximum efficiency of 98.5 % (including 9.57 W auxiliary power consumption). The total boxed converter volume is $2.79\,\text{dm}^3$ ($\widehat{=}\ 1.8\,^{\text{kW}}/_{\text{dm}^3}$) whereas the total boxed component volume is $V_{box} = 1.95\,\text{dm}^3$ ($\widehat{=}\ \rho_{box} = 2.56\,^{\text{kW}}/_{\text{dm}^3}$).

Tab. 5.5: BOM of the implemented SiC 3LDAB hardware prototype shown in **Fig. 5.6**.

Component	**Specifications**
$S_{\{1,2,3,4\}}$	2 × TO-247-3 80 mΩ 1200 V SiC MOSFET C2M0080120D
$S_{\{5,6,7,8\}}$	1 × TO-247-3 80 mΩ 1200 V SiC MOSFET C2M0080120D
$C_{f\{1,2\}}$	3 × 12 µF 1100 V MKP film capacitor B32776G0126
Tr	5 × E80/38/20 core sets N87 & 9.2 m 2205×71 µm litz wire
L_σ	3 × E42/21/15 core sets N87 & 1.2 m 2205×71 µm litz wire
L_m	1 × E42/21/20 core set N87 & 5.9 m 120×71 µm litz wire
Cooling system	(122×80×40) mm^3 custom Al sink with 39 fins of 1 mm width & 3 × (40×40×10) mm^3 12 V 1.08 W fans MC35162

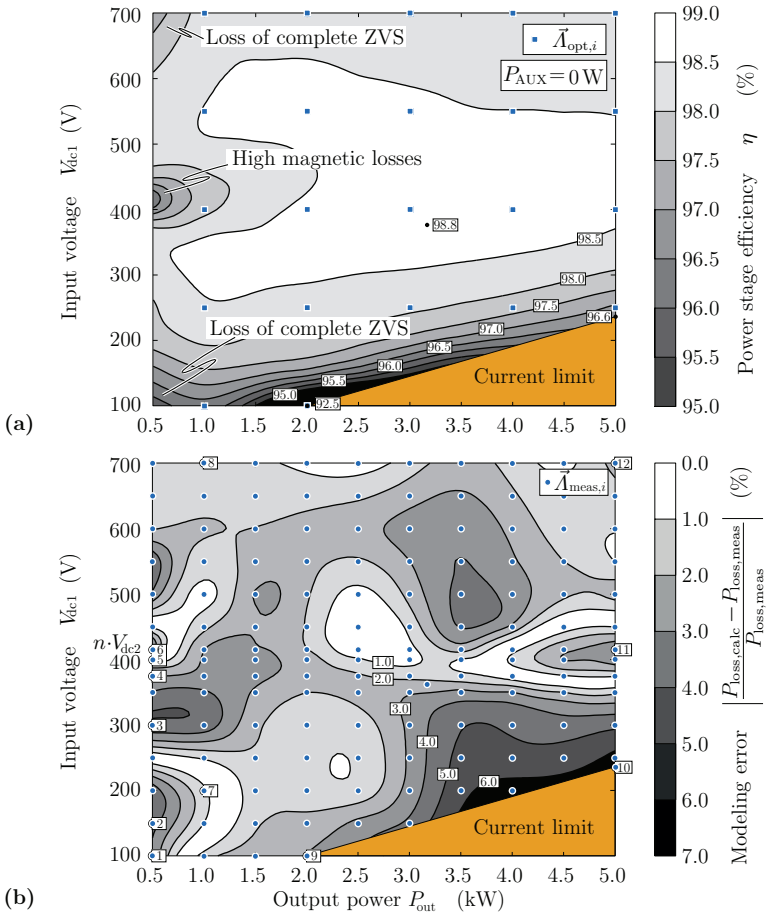


Fig. 5.7: **(a)** Measured efficiency of the power stage of the implemented SiC 3LDAB hardware prototype. Not included is the power consumption of the auxiliaries $P_{\mathrm{AUX}} = 9.57\,\mathrm{W}$ (gate drivers, fans and control ICs) in order to highlight the achieved modeling accuracy of the strongly varying loss shares of the power stage (cf. **Fig. 5.8**). The achieved average efficiency excluding/including P_{AUX} is 98.0/97.5 %. The figure furthermore depicts the considered nominal operating points $\vec{\Lambda}_{\mathrm{opt},i}$. **(b)** Relative deviation between the calculated converter losses $P_{\mathrm{loss,calc}}$ based on the models of Section 5.3 and the measured losses $P_{\mathrm{loss,meas}}$ in **(a)**. The mean modeling error across all measured operating points $\vec{\Lambda}_{\mathrm{meas},i}$ is 2.5 %.

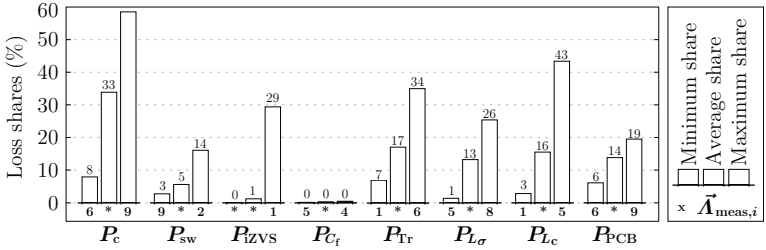


Fig. 5.8: Calculated loss shares in the prototype: average loss shares across all operating points and minimum and maximum shares with the corresponding operating point number (cf. labels in **Fig. 5.7(b)**). The widely varying shares of each loss source in conjunction with the low observed modeling error in the entire operating area **Fig. 5.7(b)** suggest a high modeling accuracy of each individual loss model.

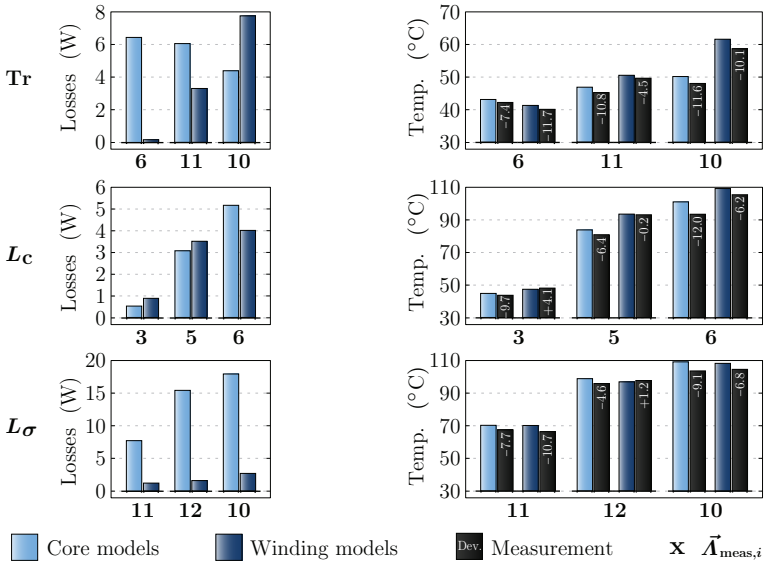


Fig. 5.9: Verification of the employed magnetics thermal models at $T_{amb} = 30\,°C$. The shown operating points (cf. labels in **Fig. 5.7(b)**) include the component-specific worst cases. The deviations of the measurements lie within -15/+5 %. The generally overestimated temperature rise can mainly be explained by the heat flow leaving the component through the connecting wires which is neglected in the model.

These specifications were met and even exceeded by the implemented hardware prototype. A photograph of the converter can be seen in **Fig. 5.6** whereas the bill of material (BOM) is listed in **Tab. 5.5**. The converter operates at $f_{\mathrm{sw}} = 48\,\mathrm{kHz}$ and achieves a maximum efficiency of $\eta_{\mathrm{max}} = 98.5\,\%$ including 9.57 W auxiliary power consumption. The measured efficiency of the power stage excluding the auxiliary supply over the specified operating area is depicted in **Fig. 5.7(a)**. The converter power stage achieves a very high efficiency of $\eta > 98\,\%$ in a wide operating range including low-load operating points. This is mainly due to complete ZVS operation (no iZVS losses) which is achieved in all nominal operating points $\vec{\Lambda}_{\mathrm{opt},i}$. The converter is able to operate in stand-alone mode and features start-up mechanisms which source the required auxiliary power from either the primary or the secondary DC voltage. The converter achieves an overall power density of $1.8\,\mathrm{kW/dm^3}$. This is reasonably compact when considering the high functionality and efficiency (>98 %) in conjunction with the wide input voltage range which means both high current *and* high voltage stress. The converter control architecture closely follows the concepts presented in [146].

The prototype was used to verify the modeling framework of the virtual prototyping routine. For this purpose, consider **Fig. 5.7(b)** which depicts the modeling error of the efficiency calculation of the prototype based on the models in Section 5.3. An excellent modeling accuracy can be observed where the mean absolute error is 2.5 % and the maximum error below 7 %. **Fig. 5.8** shows the model-based estimated minimum, average and maximum relative loss shares for each of the considered loss types. It can be found that the minimum and maximum shares of all loss types vary dramatically within the investigated operating area. It can thus be assumed with high certainty that all individual loss models must feature a high accuracy to achieve the overall excellent accuracy found in **Fig. 5.7(b)**. Moreover, an accidental compensation of different modeling errors seems to be unlikely. Further support for this conclusion can be found in **Fig. 5.9** which illustrates the accuracy of the employed thermal models for the magnetics. The measured temperatures deviate from the calculations within the range of [-15,+5] %. An essential key to the obtained close match between loss models and measurements proved to be the behavioral model which generates precise predictions of the current and voltage waveforms as demonstrated in **Fig. 5.10**.

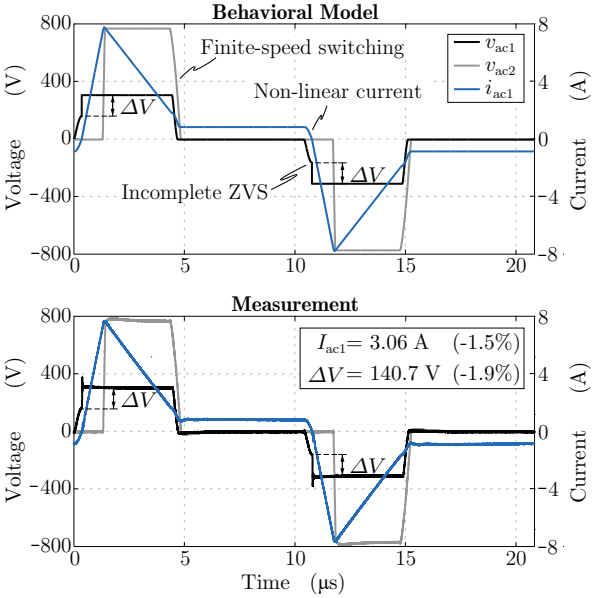


Fig. 5.10: Example of the calculated waveforms of the developed behavioral model and comparison to the measured waveforms of the prototype ($\vec{\Lambda} = \vec{\Lambda}_{\mathrm{meas},3} = (300\,\mathrm{V}, 750\,\mathrm{V}, 500\,\mathrm{W})$). The behavioral model accurately predicts the dynamics of the finite-speed switching transitions and the effects on the current which becomes non-linear during these intervals. The precise modeling of the switching transitions not only enhances the calculation of the switching and conduction losses but is indispensable for the accurate prediction of the iZVS losses.

5.5 Design and Optimization Routines

In this section, the derivation of the employed DAB virtual prototyping routine is discussed in detail. Whereas the employed component-level optimization routines have largely been discussed in Chapter 2, this section mostly deals with the application-specific routines which constitute the global iteration loop on the system level. The optimality criteria employed in this case study are the averaged efficiency η_{avg} over the operating points $\vec{\Lambda}_{\mathrm{opt},i}$ shown in **Fig. 5.7**, the power density $\rho_{\mathrm{box}} = {}^{P_{\mathrm{r}}}/_{V_{\mathrm{box,tot}}}$ based on the total boxed volume $V_{\mathrm{box,tot}}$ of the converter components and the specific costs $\sigma_P = {}^{P_{\mathrm{r}}}/_{\Sigma_{\mathrm{tot}}}$ with Σ_{tot} being

the total component costs. The employed parameters and constraints are listed in **Tab. 5.6**.

5.5.1 Virtual Prototyping Routine

If parasitic electromagnetic and thermal coupling effects are neglected, the DAB components as shown in **Fig. 5.2** are solely coupled by means of their impact on the current and voltage waveforms in the circuit. As proposed in Chapter 2, from a conceptual point of view, this observation suggests to divide the available design variables of the DAB optimization into two distinct categories as follows:

(i) Global variables which affect the waveforms: f_{sw}, T_{dead}, n, L_{σ}, L_{c}, C_{f1}, C_{f2}, $A_{\mathrm{chip}}^{600\mathrm{p}}$, $A_{\mathrm{chip}}^{1200\mathrm{p}}$, $A_{\mathrm{chip}}^{1200\mathrm{s}}$; and

(ii) Independent groups of local component-level variables with a small or negligible impact on the waveforms:

- 5 variables per inductor (type and # of stacked cores, # of turns, turn and strand diameter) and 6 variables for the transformer (additional: secondary turn diameter),
- 4 cooling system design variables (heat sink length and # of fins, # and type of fans), and
- 1 variable for each capacitor (type).

In this case study, the impact of the parasitic semiconductor output capacitances C_{oss} is not neglected as these capacitances greatly determine the waveforms during the switching transitions and eventually determine whether (complete) ZVS can be achieved. As a consequence, the chip areas which define C_{oss}, i.e. $\vec{A}_{\mathrm{chip}} = (A_{\mathrm{chip}}^{600\mathrm{p}}, A_{\mathrm{chip}}^{1200\mathrm{p}} A_{\mathrm{chip}}^{1200\mathrm{s}})^{\top}$ denoting the primary side 600 V and 1200 V as well as the secondary side 1200 V chip areas per switch (cf. **Fig. 5.2**), belong to the global category (i) design variables. On the other hand, all category (ii) component variables have a negligible impact on the current and voltage waveforms if high individual component efficiencies are assumed. This assumption and the above proposed distinction of the design variables enables the DAB virtual prototyping routine as shown in **Fig. 5.11**.

The DAB-specific routine of **Fig. 5.11** closely corresponds to the generic routine proposed in Chapter 2: the global system-level loop iterates over the switching frequency where for each iteration the remaining

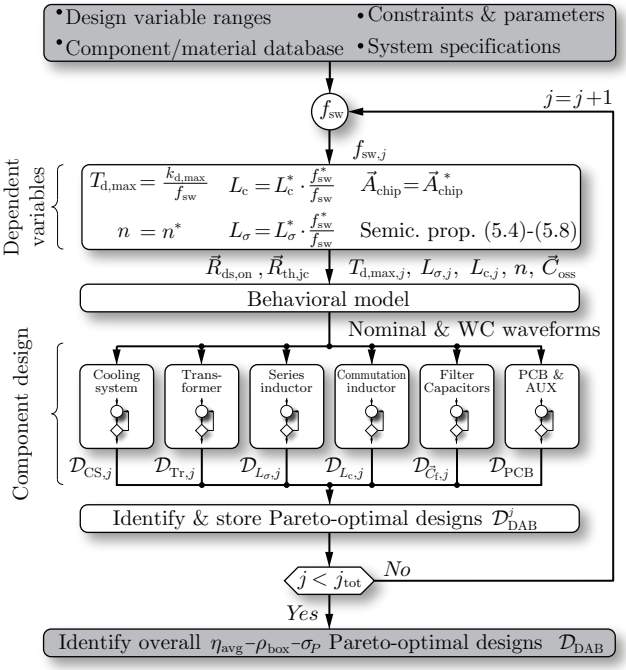


Fig. 5.11: Flow chart of the DAB virtual prototyping routine. The routine calculates and identifies the Pareto-optimal converter designs $\mathcal{D}_{\mathrm{DAB}}$ as a combination of the individually optimized components for a set of given switching frequencies. The optimality criteria are the averaged efficiency η_{avg} over the given operating points $\vec{\Lambda}_{\mathrm{opt},i}$, the power density ρ_{box} based on the total boxed volume of the components and the specific costs σ_P. The nominal waveforms correspond to the efficiency-relevant operating points $\vec{\Lambda}_{\mathrm{opt},i}$ whereas the worst case (WC) waveforms influence the component dimensioning.

global category (i) variables are determined first. The waveforms can then be calculated using the converter behavioral models. Note that this step does not only include the calculation of the nominal waveforms for the operating points $\vec{\Lambda}_{\mathrm{opt},i}$ which are required to determine the average efficiency, but also the identification of the worst case waveforms which influence the component dimensioning. This is followed by the component design loops where each component is individually optimized by means of iterating over the component-specific category (ii)

Tab. 5.6: Parameters and constraints used in the optimization routines depicted in **Fig. 5.11** and **Fig. 5.12**.

SiC MOSFET switch. frequency range	f_{sw}	$\{50{,}75{,}...{,}325\}$ kHz
Si IGBT switch. frequency range	f_{sw}	$\{5{,}6{,}...{,}20\}$ kHz
Design switching frequency	f_{sw}^{*}	50 kHz
Total SiC MOSFET semicond. costs	$\Sigma_{\mathrm{SC,tot}}$	96 €
Max. rel. dead time per switch. trans.	$k_{\mathrm{d,max}}$	2.5 %
Permissible transformer turns ratios	n	$\{\frac{1}{4},\ \frac{1}{3},\ \frac{2}{5},\ \frac{1}{2},\ \frac{3}{5},\frac{2}{3},\frac{3}{4}\}$
Max. peak-to-peak voltage ripple [1]	ΔV_{max}	2 V
Max. junction temperature	$T_{\mathrm{j,max}}$	125 °C
Ambient temperature	T_{amb}	25 °C
Total parasitic capacitance [2]	$C_{\mathrm{par,tot}}$	300 pF
Max. core stacking factor (magnetics)	$N_{\mathrm{stack,max}}$	10
Max. N87 core hot spot temperature	$T^{\mathrm{N87}}_{\mathrm{corehs,max}}$	100 °C
Max. winding temperature	$T_{\mathrm{wdghs,max}}$	125 °C
Max. permissible N87 flux density	$B^{\mathrm{N87}}_{\mathrm{max}}$	0.31 T
Max. total relative air gap length [3]	$\bar{l}_{\mathrm{ag,max}}$	0.3

[1] also applicable to the 5LDAB C_{f1} capacitor midpoint

[2] value based on prototype in Section 5.4

[3] with respect to the E-core center leg width

design variables and under consideration of the given constraints (e.g. the maximum junction temperature $T_{\mathrm{j,max}}$). At this stage, only Pareto-optimal component designs are further considered. In a next step, the Pareto-optimal converter designs $\mathcal{D}^{j}_{\mathrm{DAB}}$ as a combination of the calculated component designs are identified and stored. After the execution of the global loop, the overall Pareto-optimal converter designs are identified amongst $\bigcup_j \mathcal{D}^{j}_{\mathrm{DAB}}$.

It is evident from **Fig. 5.11** that the independent iteration of global design variables is computationally expensive as the waveform synthesis and component design must be repeated for each iteration of these variables. Due to the large number of category (i) variables in this case study, such an optimization approach would exceed the capabilities of the available standard computational means. Moreover, it can be estimated that most of the combinations of values of the global design variables would result in DAB designs with a low performance which are thus not of interest. As an example, the transformer turns ratio n greatly determines the current stress on the primary and secondary side switches. Therefore, the chip area distribution $\vec{A}_{\mathrm{chip}}$ should be chosen accordingly (and not independently from n) in order to yield a high

semiconductor and thus DAB efficiency. Therefore, the approach of **Fig. 5.11** is proposed where the complexity of the optimization problem is greatly reduced: a lower complexity is achieved by keeping only the most influential global design variable, i.e. the switching frequency f_{sw}, as an independent unconstrained design variable. Contrarily, the remaining variables are converted into dependent variables which are either held constant or chosen as a function of f_{sw}. As a consequence, a suitable approach must be found to predetermine these variables in a way which allows for high-performance DAB designs in the main optimization routine whereas inefficient designs are ruled out.

5.5.2 Dependent Global Design Variables

This section describes how the dependent system parameters, i.e. $T_{\mathrm{d,max}}$, n, L_σ, L_{c}, C_{f1}, C_{f2}, and $\vec{A}_{\mathrm{chip}}$ are predetermined in order to reduce the complexity of the subsequent main virtual prototyping routine. The determination of the parameters should be carried out in a way that potentially interesting designs which result in a high performance in the subsequent main optimization are not ruled out in the first place.

Dead Time

Long relative dead times and switching transition durations impair the minimum duty cycle capabilities of the converter, increase the circulating reactive power and decrease the maximum possible power transfer (cf. **Fig. 5.5(b)**). Therefore, a reasonable value of the maximum permissible relative dead time per switching transition is found to be $k_{\mathrm{d,max}} = 2.5\,\%$ of the switching period T_{sw} (e.g. $T_{\mathrm{d,max}} = 500\,\mathrm{ns}$ at $f_{\mathrm{sw}} = 50\,\mathrm{kHz}$).

Filter Capacitances

The employed modulation schemes (cf. Section 5.2.1) rely on close-to-ideal DC voltages V_{dc1} and V_{dc2} in order to work properly. Therefore, the maximum permissible peak-to-peak voltage ripple is limited to $\Delta V_{\mathrm{max}}^{\mathrm{PP}} = 2\,\mathrm{V}$. This constraint implies large capacitor values $\vec{C}_{\mathrm{f}} = (C_{\mathrm{f1}}, C_{\mathrm{f2}})^{\top}$ with a negligible impact on the waveforms.

Inductances, Turns Ratio and Chip Areas

The impact of the remaining design variables $\vec{\Pi} = (n, L_\sigma, L_\mathrm{c}, \vec{A}_\mathrm{chip})^\top$ with $\vec{A}_\mathrm{chip} = (A_\mathrm{chip}^\mathrm{600p}, A_\mathrm{chip}^\mathrm{1200p}, A_\mathrm{chip}^\mathrm{1200s})^\top$ on the system performance is strongly coupled. n and L_σ largely determine the current waveforms on the primary and secondary side. The selection of $\vec{A}_\mathrm{chip}$ does not only influence the conduction losses but also, based on the current waveforms and resulting C_oss, whether ZVS can achieved. Finally, the external commutation inductor L_c (cf. **Fig. 5.2**) facilitates ZVS but in turn increases the rms currents and hence the conduction losses. Due to the mutual coupling, $\vec{\Pi}$ must be determined in a combined manner. For this purpose, consider the optimization routine depicted in **Fig. 5.12**. The routine is based on a reduced and simplified set of the models discussed in Section 5.3 to enhance speed:

- The non-linear switching transitions are not calculated in detail, i.e. ideal waveforms are considered (cf. **Fig. 5.5** and **Fig. 5.3(a)**).
- Only the semiconductor losses and the cooling requirements are assessed.
- The semiconductor losses are evaluated for a fixed on-state resistance $R_\mathrm{ds,on}(I_\mathrm{ds} = 20\,\mathrm{A},\ T_\mathrm{j} = 125\,^\circ\mathrm{C})$.

In a first step, the semiconductor properties are calculated as a function of the chip areas and breakdown voltage using (5.4)-(5.8). In a next step, based on n_j, $L_{\sigma,j}$ and the proposed modulation scheme the ideal current and voltage waveforms are calculated. The magnetizing inductance L_c (which only introduces reactive power and does not contribute to the power transfer) is then added and adjusted such that complete ZVS can be achieved within $T_\mathrm{d,max}$ for each switching transition and operating point $\vec{\Lambda}_{\mathrm{opt},i}$. The considered operating points are depicted in **Fig. 5.7**. In a final step, the resulting weighted relative total semiconductor conduction and switching losses,

$$\overline{P}_\mathrm{SC} = \sum_{i=1}^{M} \frac{P_{\mathrm{c,tot},i} + P_{\mathrm{sw,tot},i}}{P_{\mathrm{out},i}}\ , \tag{5.17}$$

are calculated across the $M = 23$ given operating points $\vec{\Lambda}_{\mathrm{opt},i}$ together with the required thermal resistance of the cooling system $R_\mathrm{th,hs\text{-}amb}$ to stay below the chosen maximum semiconductor junction temperature

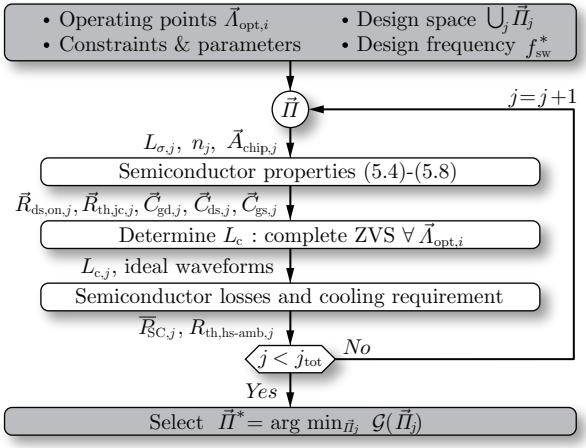


Fig. 5.12: Flow chart of the off-line optimization routine used to determine the reference values $\vec{\Pi}^* = (n^*, L_\sigma^*, L_{\mathrm{c}}^*, \vec{A}_{\mathrm{chip}}^*)$ of the dependent global design variables shown in **Fig. 5.11**.

$T_{\mathrm{j,max}} = 125\,^{\circ}\mathrm{C}$. After completion of the iterations over all variables, the cost function

$$\mathcal{G} : \vec{\Pi} \rightarrow \frac{2}{3} \cdot \frac{\overline{P}_{\mathrm{SC}}}{\overline{P}_{\mathrm{SC,min}}} + \frac{1}{3} \cdot \frac{R_{\mathrm{th,hs\text{-}amb,max}}}{R_{\mathrm{th,hs\text{-}amb}}}\,, \tag{5.18}$$

is used to determine the optimal choice of design variables $\vec{\Pi}^*$. The cost function (5.18) is designed so as to find a compromise between weighted total semiconductor losses $\overline{P}_{\mathrm{SC}}$ and required cooling effort with respect to the optimal achievable values $\overline{P}_{\mathrm{SC,min}}$ and $R_{\mathrm{th,hs\text{-}amb,max}}$ within the chosen design space of $\vec{\Pi}$.

The above outlined optimization is carried out for a design switching frequency of $f_{\mathrm{sw}}^* = 50\,\mathrm{kHz}$ for which low switching and zero incomplete ZVS losses, i.e. complete ZVS, can be achieved with a reasonably low amount of additional reactive current in L_{c}. As the switching losses P_{sw} at 50 kHz are small, low total losses $\overline{P}_{\mathrm{SC}}$ are consequently achieved at close-to-minimal rms currents. Therefore, although not explicitly considered, achieving low losses in the passives can be expected as well with the chosen approach. It can thus be estimated, that the proposed off-line optimization routine enables high-performance designs in the main

Tab. 5.7: Calculated reference values $\vec{\Pi}^*$ for the dependent global variables at $f_{\mathrm{sw}}^* = 50\,\mathrm{kHz}$ for the SiC MOSFET-based 3LDAB and 5LDAB concepts using the routine depicted in **Fig. 5.12**.

Concept	n^*	L_{σ}^* **(µH)**	L_{c}^* **(µH)**	$\vec{A}_{\mathbf{chip}}^*$ **(cm²)** [1)]
SiC 3LDAB	0.5	38.0	624	$(-, 0.2084, 0.1042)^{\top}$ [2,3)]
SiC 5LDAB	0.5	37.8	753	$(0.0521, 0.1656, 0.1003)^{\top}$ [4)]

[1)] $= (A_{\mathrm{chip}}^{600\mathrm{p}}, A_{\mathrm{chip}}^{1200\mathrm{p}} A_{\mathrm{chip}}^{1200\mathrm{s}})$ [2)] $\widehat{=} (-, 2 \times \mathrm{C2M0080120D}, 1 \times \mathrm{C2M0080120D})^{\top}$
{ [3)] $\widehat{=} (-, 40, 80)^{\top}\,\mathrm{m\Omega}$, [4)] $\widehat{=} (110.4, 47.7, 83.6)^{\top}\,\mathrm{m\Omega}$ } @ 20 A, 25 °C

virtual prototyping routine whereas the analysis of inefficient designs can largely be avoided. **Tab. 5.7** lists the reference values $\vec{\Pi}^*$ of the dependent global variables found by the off-line optimization routine depicted in **Fig. 5.12** for the SiC MOSFET-based 3LDAB and 5LDAB concepts. It can be seen that similar values result for the transformer turns ratio n^* and the series inductance L_{σ}^* whereas the SiC 5LDAB requires less reactive current provided by L_{c}^* to achieve complete ZVS in all considered operating points. The latter is a result of the more uniform current waveforms enabled by the 5LDAB modulation scheme. As already mentioned in Section 5.2, the chip area distribution $\vec{A}_{\mathrm{chip}}$ of the SiC 3LDAB equals two paralleled C2M0080120D units per switch on the primary side and one unit per switch on the secondary side. This intentional choice is motivated by several considerations:

- A system with such a chip area distribution can be realized in practice.
- The chip area distribution corresponds to the semiconductor configuration of the prototype in Section 5.4 and thus facilitates the performance comparison shown in Section 5.6.
- Investigations show that the intentionally selected chip area distribution of **Tab. 5.7** is close to the optimum distribution which is shown in **Tab. 5.10**. The intentional choice therefore impairs the achievable SiC 3LDAB performance only negligibly.

In contrast, the SiC 5LDAB chip area distribution of **Tab. 5.7** exactly corresponds to the calculated optima. The total costs of the resulting 12 C2M0080120D units in the SiC 3LDAB $\Sigma_{\mathrm{SC,tot}} = 96\,€$ is used as a constraint for the optimization of the SiC 5LDAB chip area distribution

in order to facilitate a meaningful and fair comparison between the two SiC-based topologies. Note that equal effective parasitic capacitances of $C_{\mathrm{par,tot}} = 300\,\mathrm{pF}$ are assumed for each bridge leg. The value is chosen based on the average measured values of the implemented hardware prototype and mainly originates from the PCB tracks, the capacitances between the semiconductor packages and the heat sink and the parasitic capacitances of the magnetics. Equal $C_{\mathrm{par,tot}}$ for both the 3LDAB and 5LDAB can be justified by the same number of semiconductor packages and hence similar dimensions of the PCB. The optimal reference values for the Si IGBT-based concepts were analogously determined with the routine depicted in **Fig. 5.12** where the fixed semiconductor configurations of **Tab. 5.2** were considered (no variable chip areas).

As discussed, the switching frequency remains an independent global design variable and can arbitrarily be iterated in the proposed virtual prototyping routine depicted in **Fig. 5.11**. Thus, for switching frequencies differing from the design frequency, i.e. $f_{\mathrm{sw}} \neq f_{\mathrm{sw}}^{*}$, it is proposed to scale the calculated reference inductance values according to

$$L_{\sigma} = L_{\sigma}^{*} \cdot \frac{f_{\mathrm{sw}}^{*}}{f_{\mathrm{sw}}} \;, \quad L_{\mathrm{c}} = L_{\mathrm{c}}^{*} \cdot \frac{f_{\mathrm{sw}}^{*}}{f_{\mathrm{sw}}} \;. \tag{5.19}$$

This approach will largely preserve the current and voltage waveforms guaranteeing similarly low conduction losses in the components irrespective of f_{sw}. The major difference for $f_{\mathrm{sw}} \neq f_{\mathrm{sw}}^{*}$ is the ZVS properties of the converter: since the current waveforms do not significantly change, less charge can be provided within $T_{\mathrm{d,max}} = \frac{k_{\mathrm{d,max}}}{f_{\mathrm{sw}}}$ at elevated switching frequencies. As a consequence, incomplete ZVS losses must be expected which start to occur at low-load operating points first where less reactive power for ZVS is available. A possible countermeasure could be to decrease L_{c} more than as it is proposed in (5.19), e.g. with $L_{\mathrm{c}} \propto \frac{1}{f_{\mathrm{sw}}^{2}}$. However, in such a case the increased reactive current would result in rapidly increasing additional conduction losses. These additional losses occur in all components and in the entire operating range, but most at full load. Since these operating points typically represent the thermal worst case operating points and thus have a decisive impact on the component volumes, lowering L_{c} more than as it is proposed in (5.19) would not only lead to a similar reduction of the efficiency, but also to a significant volume increase of the cooling system and magnetics.

5.6 Performance Space Analysis

This section presents the results of the η_{avg}-ρ_{box}-σ_{P} multi-objective optimization of the considered SiC and Si 3LDAB and 5LDAB concepts. Approximately 25'000 Pareto-optimal designs were found for each concept based on the virtual prototyping routine in **Fig. 5.11**. The optimization problem involves a total of 24 design variables: 22 component variables as listed in Section 5.5, the switching frequency and the selection of the concept. Standard computational means (workstation with 2×2.4 GHz Intel XEON quad-core CPUs, 64 GB RAM) were sufficient to handle the problem and find the solution in less than 5 hours. The results of the optimizations are shown in **Fig. 5.13**, **Fig. 5.14**, **Fig. 5.15** and **Fig. 5.16**.

5.6.1 Comparison of the Topologies

Fig. 5.13 and **Fig. 5.14** show the Pareto fronts of the Si and SiC 3LDAB and 5LDAB concepts. The first main finding is the dramatically lower overall system performance of the IGBT-based concepts when compared to the SiC-based counterparts. Much lower efficiencies and power densities result and, despite the employment of low-cost IGBTs, only marginally higher specific costs can be achieved (at very low efficiencies below 95 %). The main reasons for the clear superiority of SiC MOSFETs in this application are their ohmic output characteristics and the absence of stored charge in the conducting device. The former allows for considerably lower conduction losses in part-load operation than the built-in forward voltage drop of the bipolar IGBTs. The latter enables very low ZVS losses whereas the tail current effect due to the internally stored charge prohibits low-loss ZVS with Si IGBTs [90]. The higher semiconductor losses and thus lower permissible switching frequencies entail a larger and more expensive cooling system and passives which largely compensate the cost advantage of the Si IGBTs. Note that the significantly lower achievable power density of the Si IGBT-based concepts would additionally entail higher housing costs.

The second main finding of **Fig. 5.13** and **Fig. 5.14** is derived from the comparison of the SiC MOSFET-based concepts. The corresponding Pareto fronts reveal that the SiC 3LDAB is fundamentally superior and dominates the SiC 5LDAB regarding all considered performance criteria: the merging of the SiC 3LDAB and SiC 5LDAB Pareto fronts $\bigcup \mathcal{D}_{\text{DAB}}^{\text{SiC-3L}}$ and $\bigcup \mathcal{D}_{\text{DAB}}^{\text{SiC-5L}}$, respectively, and a subsequent η_{avg}-ρ_{box}-σ_{P}

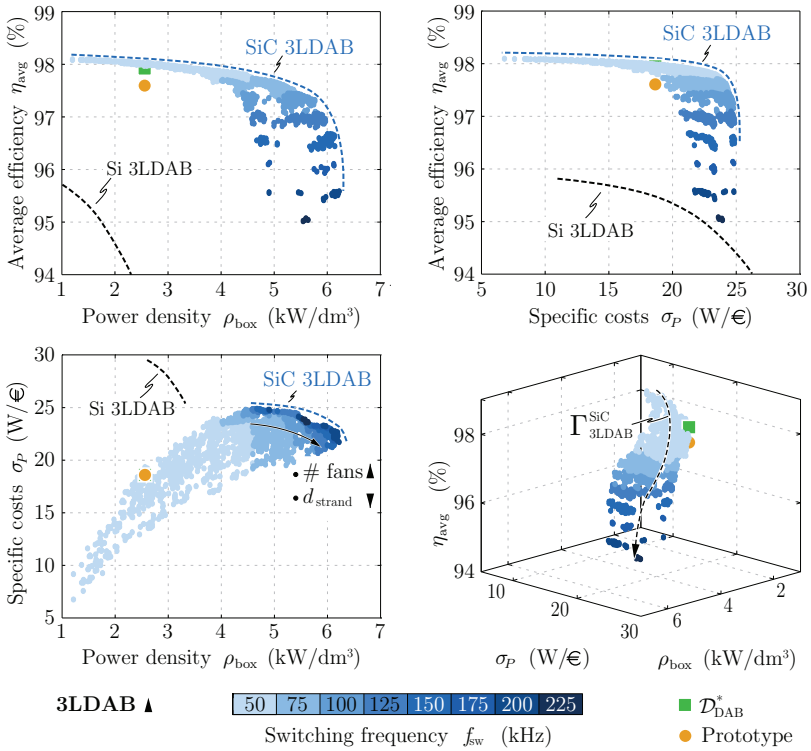


Fig. 5.13: η_{avg}-ρ_{box}-σ_P-Pareto-optimal designs $\bigcup \mathcal{D}^{SiC\text{-}3L}_{DAB}$ of the SiC 3LDAB found by the virtual prototyping routine depicted in **Fig. 5.11**. The projected 2D Pareto fronts reveal distinct trade-offs between η_{avg} and ρ_{box}/σ_P. Contrarily, the trade-off range between ρ_{box} and σ_P is rather limited and is mainly a function of the number of employed fans in the cooling system and the strand diameter d_{strand} of the magnetics. This characteristic translates into a relatively high correlation between the power density and the costs. A relaxed correlation and thus a wider 3D Pareto front can be achieved if a higher number of different materials and component types are considered (cf. **Fig. 5.18**). The figures further show the projected Pareto fronts resulting from a Si IGBT-based 3LDAB solution (switching frequency range of [5,20] kHz). The Si 3LDAB Pareto front shows a dramatically lower achievable system performance which supports the selection of SiC MOSFETs in this work.

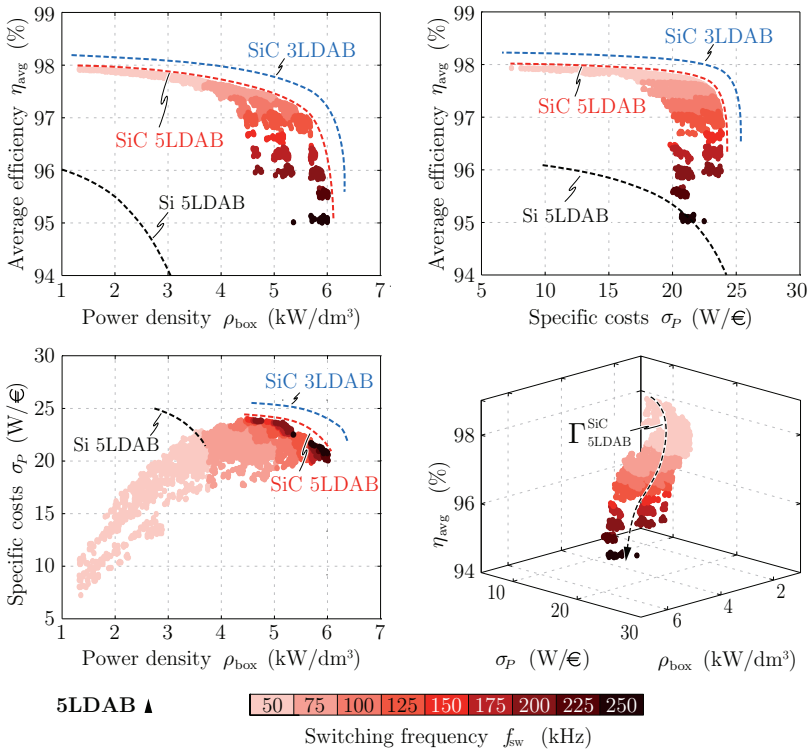


Fig. 5.14: η_{avg}-ρ_{box}-σ_P-Pareto-optimal designs $\bigcup \mathcal{D}_{DAB}^{SiC\text{-}5L}$ of the SiC MOSFET-based 5LDAB found by the virtual prototyping routine depicted in **Fig. 5.11**. By inspection of the calculated data it can be found that the SiC 3LDAB clearly outperforms the 5LDAB, i.e. there is no SiC 5LDAB design which is Pareto-optimal amongst the SiC 3LDAB designs. This also supported by the comparison of the projected 2D η_{avg}-ρ_{box}, η_{avg}-σ_P and ρ_{box}-σ_P Pareto fronts of the two topologies. The figures further show the projected Pareto fronts resulting from a Si IGBT-based 5LDAB solution (switching frequency range of [5,20] kHz). The calculated Si 5LDAB Pareto fronts show a dramatically lower achievable system performance which supports the selection of SiC MOSFETs in this work.

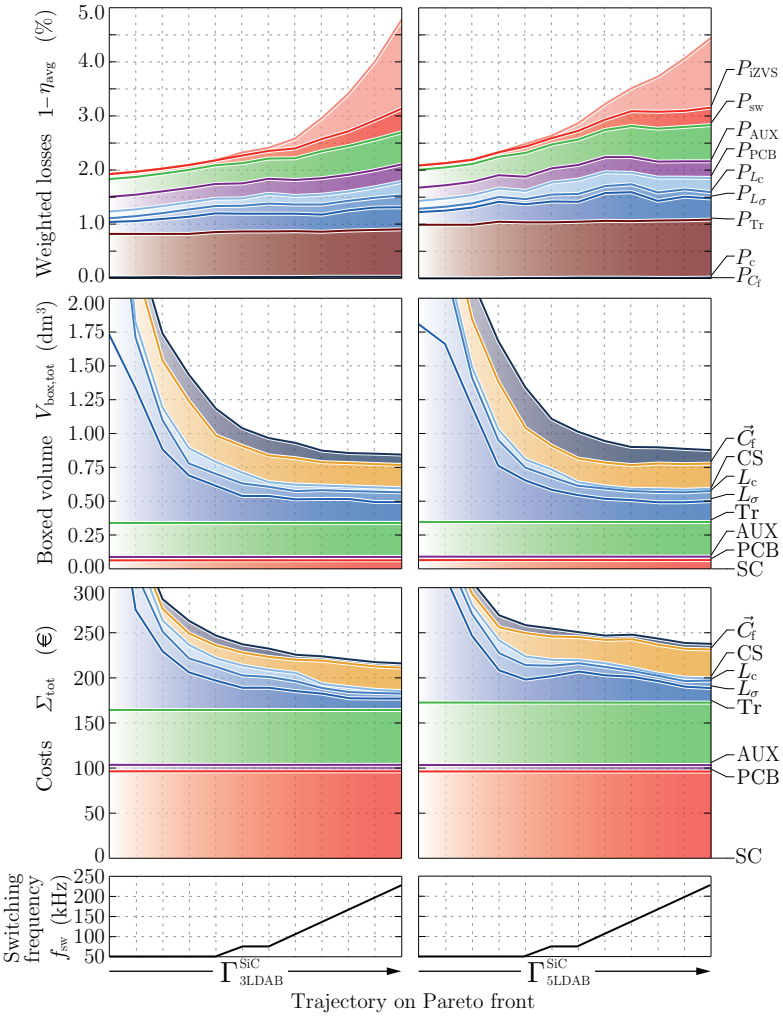


Fig. 5.15: Component loss, volume and cost breakdown of the designs forming the trajectories $\Gamma^{\mathrm{SiC}}_{\mathrm{3LDAB}}$ and $\Gamma^{\mathrm{SiC}}_{\mathrm{5LDAB}}$ on the SiC 3LDAB and SiC 5LDAB Pareto fronts shown in **Fig. 5.13** and **Fig. 5.14**. The trajectories are defined so as to attain an identical evolution of the global design variable f_{sw}.

Pareto analysis trivially results in the SiC 3LDAB Pareto front again, i.e.

$$\bigcup \mathcal{D}_{\mathrm{DAB}}^{\text{SiC-3L}} \equiv \bigcup \mathcal{D}_{\mathrm{DAB}}^{\text{SiC-3L+SiC-5L}} \tag{5.20}$$

$$\iff \bigcup \mathcal{D}_{\mathrm{DAB}}^{\text{SiC-5L}} \cap \bigcup \mathcal{D}_{\mathrm{DAB}}^{\text{SiC-3L+SiC-5L}} \equiv \varnothing \, . \tag{5.21}$$

The identification of the underlying reasons is demanding as it requires a comparative analysis of the very large number of SiC 3LDAB and SiC 5LDAB designs which form the Pareto fronts. In order to facilitate the discussion of this analysis which is presented below, the component loss, volume and cost shares of selected 3LDAB and 5LDAB designs are shown in **Fig. 5.15**. The connection of these designs form the trajectories $\Gamma_{\mathrm{3LDAB}}^{\mathrm{SiC}}$ and $\Gamma_{\mathrm{5LDAB}}^{\mathrm{SiC}}$ on the respective Pareto fronts depicted in **Fig. 5.13** and **Fig. 5.14**. The 3LDAB and 5LDAB designs are chosen so that the associated global design variable f_{sw} (i.e. the most influential design variable) evolve identically along the formed trajectories (cf. **Fig. 5.15**), thereby significantly enhancing the comparability.

Losses

Inspection of the Pareto fronts and in particular the selected designs in **Fig. 5.15** identifies the nearly 0.2 % higher average conduction losses to be the main reason for the lower SiC 5LDAB efficiency. Most remarkably, higher conduction losses result despite the advantage of lower rms currents in the power transfer (cf. **Fig. 5.3(b)**) and lower required reactive currents (cf. **Tab. 5.7**) featured by the 5LDAB. This finding can mainly be explained by the higher number of switches in the primary side bridge legs of the 5LDAB which yields a lower chip area utilization. This inherent disadvantage is pronounced enough to overcompensate the advantage of enabling lower rms currents. In fact, a closer inspection of the results reveals that with the selected chip areas of **Tab. 5.7** the total conduction losses of the 5LDAB are higher even in operating points where the rms currents are clearly lower (mainly at high power levels and high input voltages, cf. **Fig. 5.3**). Not only the lower chip area utilization per se contributes to this result but also the fact that due to the lower utilization the semiconductors operate at higher current densities and higher temperatures which both contributes to increased on-state resistances (cf. **Fig. 3.1**).

The situation changes for very high switching frequencies $f_{\mathrm{sw}} \gtrapprox 250\,\mathrm{kHz}$. There, the 3LDAB generates considerably higher iZVS losses

than the 5LDAB as a result of the less uniform current waveforms across the operating range. This shows that the 5LDAB is more suitable for high-frequency operation due to the generally more uniform current distribution within the wide operating range. However, these designs at $f_{\mathrm{sw}} \gtrapprox 250\,\mathrm{kHz}$ are irrelevant since they are not Pareto-optimal anymore and consequently not part of the Pareto fronts depicted in **Fig. 5.13** and **Fig. 5.14**. These designs are not Pareto-optimal since the corresponding converter volumes and costs do not further decrease at such switching frequencies.

Volume

Fig. 5.15 shows that the SiC 5LDAB designs generally feature a lower power density which is mainly due to the larger capacitor volume. The larger capacitor is caused by the requirement of balancing the midpoint potential of the primary filter capacitor C_{f1} which is not necessary in the 3LDAB. The evolution of the total volume of the magnetics is similar for both topologies which is mostly because of very similar worst case operating point conditions in both topologies. For switching frequencies $f_{\mathrm{sw}} \gtrapprox 200\,\mathrm{kHz}$, no further volume reductions are attainable due to the increasing share of the heat sink and approximately constant or growing shares of the magnetics.

Costs

The semiconductor costs are equal for both topologies by reason of the approach of this comparison. The SiC 5LDAB exhibits higher costs of the capacitors and the auxiliary electronics due to the higher number of gate driver units and the larger primary filter capacitor C_{f1}.

5.6.2 Best Converter Concept

The analysis in this section identifies the SiC MOSFET-based 3LDAB to be the overall most suitable concept for the given DC/DC microgrid application. It concurrently achieves a higher efficiency, power density and lower or similar costs than the other concepts. The superiority of the SiC 3LDAB concept is further emphasized by the fact that the underlying 3LDAB modulation scheme is considerably simpler than the 5LDAB scheme. In addition, the 3LDAB is likely to offer a higher reliability due to the lower component count. Note that the superiority

of the SiC 3LDAB over the SiC 5LDAB is invariant with respect to the constraints in **Tab. 5.7** as these constraints only have an impact on the *absolute* achievable performance but do not fundamentally alter the *relative* differences between the achievable SiC 3LDAB and SiC 5LDAB performance (this is verified in Section 5.7 for variable chip areas/costs). Finally, the analysis proves that a high converter performance is achievable despite the high required functionality. Most notably, the proposed combination of a 3LDAB topology, SiC MOSFETs and an optimized modulation scheme which facilitates minimized rms currents and complete ZVS in a wide operating range achieves considerably higher efficiencies than previously seen in literature. Whereas a large fraction of the SiC 3LDAB designs in **Fig. 5.13** and the hardware prototype presented in Section 5.4 achieve peak efficiencies between 98.5 and 99 %, peak efficiencies between 90 and 97.1 % are reported for the uni- and bidirectional wide voltage range systems in [16, 135–144].

5.6.3 Impact of Parasitic Capacitances

Inspection of the component loss shares in **Fig. 5.15** reveals the severe impact of the parasitic capacitances in HF operation. Whereas complete ZVS is achieved for $f_{\mathrm{sw}} = f_{\mathrm{sw}}^{*} = 50\,\mathrm{kHz}$ as targeted by the design approach, the iZVS losses P_{iZVS} grow rapidly for increasing switching frequencies. The main reasons are the frequency-invariant reactive currents and the shortening of the maximum permissible dead times which amount to less available charge for the charging/discharging of the parasitic capacitances. Note that increasing the reactive currents proportional to the switching frequency results in rapidly increasing additional conduction losses and does thus not represent an attractive countermeasure. Longer dead times in turn impair the minimum duty cycle capabilities of the converter, increase the circulating reactive power and decrease the maximum possible power transfer (cf. **Fig. 5.5(b)**). It can therefore be concluded that low parasitic capacitances are a key requirement for efficient HF operation. On the one hand, low specific output capacitances as applicable for SiC MOSFETs are desirable (cf. **Tab. 5.3**). On the other hand, a careful design of the converter layout is essential to reduce the additional parasitic layout capacitance $C_{\mathrm{par,tot}}$ which may easily be in the range of the output capacitances of SiC MOSFETs. In this context, the investigations of this work reveal the deficits of the standard packages (such as the employed TO-247-

3) in which many commercial SiC semiconductors are provided: these packages form significant undesired parasitic capacitances to the heat sink (tens of picofarads, depending on the insulation layer). In case of the prototype in this work, the packages contribute between 25 and 50 % to $C_{\mathrm{par,tot}} \approx 300\,\mathrm{pF}$ (depending on the bridge leg) and hence pose a limiting factor for ZVS.

5.6.4 Increasing Inductor Volumes

An interesting observation in **Fig. 5.15** is the fact that the maximum power density of either SiC MOSFET-based concept is not only limited by the growing volume of the heat sink but also by the increasing volume of L_σ. The scaling of the SiC 3LDAB and SiC 5LDAB series inductor designs $\mathcal{D}_{L_\sigma,j}$ with the lowest achievable volume as a function of the switching frequency is shown in **Fig. 5.16**. It can be seen that the respective designs employ large air gap lengths which are close to the maximum permissible air gap length (relative to the core size). This constraint was introduced to avoid excessive magnetic stray fields which in turn contribute to radiated EMI and induce losses in nearby conductive materials. The reason why large air gaps are employed is a combination of the low required inductance values, the low saturation flux density of the core material and high core losses in certain operating points. In the situation at hand, this combination yielding large air gaps results in the effect that increasing the switching frequency does not necessarily lead to lower inductor volumes. For the purpose of a better illustration, consider the scaling of an arbitrary inductor L_σ which employs the maximum permissible relative air gap length $\bar{l}_{\mathrm{ag,max}}$:

(i) According to Section 5.5, the required inductance scales with

$$L_\sigma \propto f_{\mathrm{sw}}^{-1} \ . \tag{5.22}$$

(ii) The number of turns must therefore scale with

$$L_\sigma \propto N_{\mathrm{wdg}}^2 \overset{(5.22)}{\Longleftrightarrow} N_{\mathrm{wdg}} \propto f_{\mathrm{sw}}^{-\frac{1}{2}} \ , \tag{5.23}$$

if the same core geometry is assumed where the air gap must not be increased any further. The number of turns must hence be reduced in case of an increased switching frequency in order to achieve the lower inductance.

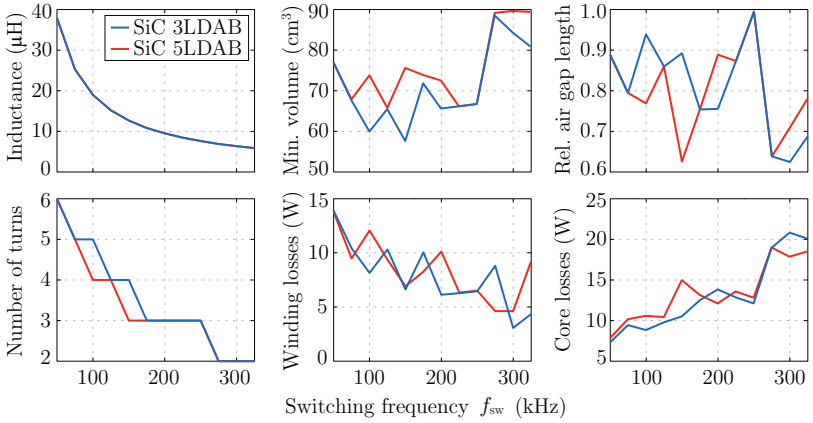


Fig. 5.16: Scaling of the SiC 3LDAB and SiC 5LDAB series inductor designs $\mathcal{D}_{L_\sigma,j}$ with the lowest achievable volume as a function of the switching frequency. Despite the drop of the required inductance with $L_\sigma \propto f_{\mathrm{sw}}^{-1}$, the minimum achievable volumes remain largely constant or even increase. The main reason for this behavior is the maximum permissible air gap length (relative to the core size) which is limited here to a value of 1.0 in order to avoid excessive stray fields. The discontinuities in most of the curves is due to the discrete nature of the number of turns and the available core sizes. The winding and core losses are given for the respective worst case operating points which determine the inductor volume due to thermal constraints.

(iii) Using (5.23), the the core and winding losses scale according to

$$P_{\mathrm{core}} \propto f_{\mathrm{sw}}^{\alpha} \cdot |\Delta B|^{\beta} \propto f_{\mathrm{sw}}^{\alpha} \cdot N_{\mathrm{wdg}}^{\beta} \propto f_{\mathrm{sw}}^{\alpha-\frac{\beta}{2}} \,, \tag{5.24}$$

$$P_{\mathrm{wdg}} \propto N_{\mathrm{wdg}}^{2} \propto f_{\mathrm{sw}}^{-1} \,, \tag{5.25}$$

if the proximity and skin effects are neglected for the scaling of the winding losses.

Based on the core loss measurements of the N87 core material shown in Section 3.3, $\alpha \approx 1.8$ and $\beta \approx 2.5$ for $f_{\mathrm{sw}} \gtrapprox 100\,\mathrm{kHz}$. It becomes clear that a continuous reduction of the inductor volume with increasing switching frequency is not possible as the core losses tend to increase whereas the further reduction of the (lower) winding losses becomes negligible. The discussed scaling with the switching frequency is confirmed

by the details in **Fig. 5.16** and is further supported by the analysis shown in [80]. Note that similar effects can also be observed for the transformer and commutation inductors.

This finding represents a fundamental limitation for the design of HF AC chokes with small inductance values and implies the need for novel technologies and/or novel/other core materials. In order to enable more balanced core and winding losses also at elevated frequencies, the maximum number of turns must not be limited by the permissible air gap length. This could either be achieved by (low-loss) core materials featuring low permeabilities and/or by means of employing cores with multiple distributed air gaps whose total length can be large without excessive stray fields.

5.6.5 Comparison to Prototype

The existing prototype introduced in Section 5.4 employs the same modulation scheme as considered in this work and was designed for similar constraints as shown in **Tab. 5.6**. Therefore, the existing prototype can directly be compared to the calculated Pareto-optimal SiC 3LDAB designs depicted in **Fig. 5.13**. Inspection of **Fig. 5.13** leads to the conclusion that the calculated Pareto fronts can be trusted with high confidence as they are in close vicinity of the prototype and rely on the same modeling framework that accurately predicts the prototype losses (cf. Section 5.4). The design of the implemented hardware prototype was accomplished prior to the investigations of this case study when the virtual prototyping routine of this thesis was not yet available. In a second step, it is therefore analyzed how the prototype could be improved in order to be located on the Pareto front. For this purpose, the prototype is compared to the marked Pareto-optimal design $\mathcal{D}^{*}_{\mathrm{DAB}}$ in **Fig. 5.13** which features an equal total component volume and equal costs. A difference in the average efficiency of more than 0.3 % can be observed. The analysis summarized in **Tab. 5.8**, **Tab. 5.9** and **Fig. 5.17** shows the differences between the prototype and the Pareto-optimal design $\mathcal{D}^{*}_{\mathrm{DAB}}$. It reveals a selection of too powerful fans for the prototype which significantly decreases the low-load efficiency due to higher constant fan losses (included in P_{AUX}). On the other hand, lower semiconductor losses result in the prototype due to lower junction temperatures at high-load conditions. However, this cannot compensate the higher fan losses. Finally, the analysis also finds a non-optimal

Tab. 5.8: Selected design variables and component implementations of the SiC 3LDAB hardware prototype shown in **Fig. 5.6** employing a switching frequency of $f_{\mathrm{sw}} = 48\,\mathrm{kHz}$.

Component	**Design variables and implementation**
$S_{\{1,2,3,4\}}$ $S_{\{5,6,7,8\}}$	2 × TO-247-3 80 mΩ 1200 V SiC MOSFET C2M0080120D 1 × TO-247-3 80 mΩ 1200 V SiC MOSFET C2M0080120D
$C_{\mathrm{f}\{1,2\}}$	3 × 12 µF 1100 V MKP film capacitor B32776G0126
Tr	$n = 0.5$, 5 × E80/38/20 core sets N87 & 2.7 m 2205×71 µm litz wire (10 turns) & 6.5 m 2205×71 µm litz wire (20 turns)
L_σ	38 µH, 3 × E42/21/15 core sets N87 & 1.2 m 2205×71 µm litz wire (8 turns)
L_{m}	630 µH, 1 × E42/21/20 core set N87 & 5.9 m 120×71 µm litz wire (73 turns)
Cooling system	$R_{\mathrm{th,hs\text{-}amb}} = 0.15\,\mathrm{K/W}$, (122×80×40) mm³ Al sink with 39×1 mm fins & 3 × (40×40×10) mm³ 12 V 1.08 W fans MC35162

Tab. 5.9: Design variables and component implementations of the Pareto-optimal SiC 3LDAB design $\mathcal{D}^*_{\mathrm{DAB}}$ shown in **Fig. 5.13** employing a switching frequency of $f_{\mathrm{sw}} = 50\,\mathrm{kHz}$. $\mathcal{D}^*_{\mathrm{DAB}}$ employs the same semiconductors and PCB as the hardware prototype of **Fig. 5.6**.

Component	**Design variables and implementation**
$S_{\{1,2,3,4\}}$ $S_{\{5,6,7,8\}}$	2 × TO-247-3 80 mΩ 1200 V SiC MOSFET C2M0080120D 1 × TO-247-3 80 mΩ 1200 V SiC MOSFET C2M0080120D
$C_{\mathrm{f}\{1,2\}}$	1 × 40 µF 1100 V MKP film capacitor B32778G0406
Tr	$n = 0.5$, 3 × E70/33/32 core sets N87 & 3.0 m 2201×71 µm litz wire (12 turns) & 6.9 m 1809×71 µm litz wire (24 turns)
L_σ	38 µH, 6 × E56/24/19 core sets N87 & 2.0 m 3899×50 µm litz wire (7 turns)
L_{m}	624 µH, 5 × E40/16/12 core set N87 & 6.8 m 765×50 µm litz wire (39 turns)
Cooling system	$R_{\mathrm{th,hs\text{-}amb}} = 0.30\,\mathrm{K/W}$, (82×110×40) mm³ Al sink with 26×1 mm fins & 2 × (40×40×10) mm³ 5 V 0.6 W fans 1604KL-01W-B40

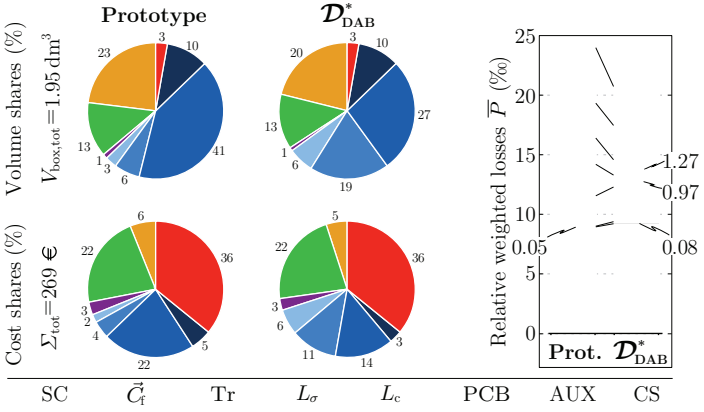


Fig. 5.17: Comparison of the implemented hardware prototype to the theoretical Pareto-optimal converter $\mathcal{D}^*_{\mathrm{DAB}}$ (cf. **Fig. 5.13**) for equal total component volumes and costs. It can be seen that the optimization routine suggests a converter design with a slightly smaller cooling system combined with less powerful fans. This will compromise the relative weighted semiconductor losses only negligibly and is overcompensated by the reduction of the fan power consumption (included in P_{AUX}). The second major difference of $\mathcal{D}^*_{\mathrm{DAB}}$ is the smaller transformer volume in favor of an approximately twofold and threefold volume increase of the series inductance and commutation inductance, respectively, which leads to lower overall losses in the magnetics. In sum, the proposed optimization routine promises an increase of the weighted efficiency by more than 0.3 % for the same total volume and costs.

volume distribution between the magnetics leading to increased losses in these components when compared to $\mathcal{D}^*_{\mathrm{DAB}}$. Besides a substantial efficiency improvement of 0.3 % for the given volume and costs, the prototype could also be significantly reduced in volume and costs. For the same efficiency, the power density could be doubled while reducing the costs by approximately 25 % as evident from **Fig. 5.13**.

The findings of the above analysis support the usefulness and potential of the proposed models and virtual prototyping framework: not only does it generate a systematic and accurate prediction of the performance trade-offs, but also does it enable a target-oriented performance improvement of the (already efficient and reasonably compact) realized prototype. Eventually, the presented analysis reveals potentials for further design improvements:

- *PCB losses:* due to high currents in some operating points, the PCB conduction losses are relatively high as evident from **Fig. 5.8** and **Fig. 5.15**. Therefore, an increase of the PCB copper thickness from currently 35 µm to 70 µm could prove to be a cost-effective ($\approx +2$ €) means to increase the overall efficiency.
- *Constant losses:* the average efficiency also considers low-power operating point (down to 20 % of rated power) efficiencies which are highly sensitive to constant losses. Therefore, the power consumption of the auxiliaries (gate driver units, fans, measurement and control ICs) and its power supply efficiency could be optimized. In particular, a fan control scheme could be implemented which varies the fan speed or turns the fans off depending on the measurement of the heat sink temperature (which is a good measure for the semiconductor losses).
- *Auxiliary costs:* **Fig. 5.15** shows that the share of the auxiliary circuits towards the total converter costs is relatively high. This is on the one hand due to the included gate driver costs and on the other hand partly due to the fact that an isolated system requires more expensive and a higher number of auxiliary components than non-isolated converters. Nevertheless, in view of a redesign of the prototype towards a commercial product, the auxiliaries would clearly offer a substantial potential for cost improvements.

5.7 Summary

This chapter presents a comprehensive cost-aware comparison of isolated bidirectional DAB concepts in a 5 kW 100-700 V ultra-wide input voltage range DC microgrid application. A conventional 3LDAB is compared to an advanced 5LDAB topology considering either Si IGBTs or SiC MOSFETs. The 5LDAB achieves lower rms currents when compared to the 3LDAB as a result of the higher degree of freedom in the modulation scheme. Based on a detailed behavioral model and the advanced multi-physics and cost models from Chapter 3 and Chapter 4, the topologies are optimized with respect to the efficiency, volume and the costs. The modeling framework was experimentally verified using a hardware prototype. The observed very good loss (mean deviation: 2.5 %) thermal and waveform modeling accuracies imply that the optimizations can be trusted with high confidence. The calculated Pareto

fronts reveal the superiority of SiC MOSFETs in the considered application: SiC enables higher efficiencies and power densities and at the same time achieves similar costs on the system level as Si IGBTs. The comparison of the optimized SiC MOSFET-based 3LDAB and 5LDAB concepts under the assumption of equal semiconductor costs shows a fundamental superiority of the conventional 3LDAB regarding all considered performance criteria: the SiC 3LDAB achieves a higher efficiency (better chip area utilization), lower volumes (smaller capacitors as no capacitor midpoint balancing required) and lower costs (fewer gate drivers) and at the same time features a lower component count and a simpler modulation scheme. The fact that the 5LDAB concept which at first glance seemed to be more promising (due to lower achievable rms currents) than the conventional 3LDAB is found to be fundamentally inferior emphasizes the value of the proposed comprehensive benchmarking approach. Finally, the calculations and the presented SiC 3LDAB hardware prototype prove that despite the galvanic isolation and wide voltage range efficiencies above 98 % in a wide operating range are possible which was previously not seen in literature.

5.7.1 Findings

Superiority of the SiC 3LDAB

It can be concluded that a multi-level approach in the given DC/DC application mainly increases the volume/costs of the gate drivers and capacitors whereas the volume/costs of the magnetics cannot substantially be reduced. The latter is mainly due to the fact that the worst case operating conditions of the magnetics predominantly occur at low input voltages (implying high currents) where the 5LDAB topology has no advantage, i.e. is operated as a 3LDAB topology (cf. **Fig. 5.3**). When employing SiC MOSFETs, the advantage of achieving lower rms currents in operating points in the higher voltage regime is overcompensated by the lower chip area utilization of the 5LDAB and thus higher resulting conduction losses. Furthermore, due to the soft-switching techniques which can be exploited with SiC MOSFETs, the switching losses are generally very low which largely neutralizes another potential advantage of the multi-level approach. These observations are in strong contrast to multi-level approaches in hard-switched DC/AC inverter/rectifier applications where a 3-level solution usually allows for lower overall semiconductor losses and lower inductor volumes when

Tab. 5.10: Calculated reference values $\vec{\Pi}^*$ for the dependent global variables at $f_{\mathrm{sw}}^* = 50\,\mathrm{kHz}$ from [82] for the SiC MOSFET-based 3LDAB and 5LDAB concepts using the same routine as depicted in **Fig. 5.12**.

	$\Sigma_{\mathrm{SC,tot}}$ (€)	n^*	L_σ^* (µH)	L_c^* (µH)	$\vec{A}_{\mathrm{chip}}^*$ (cm²)
3LDAB	74	0.5	37.9	727	$(-, 0.1549, 0.0871)^\top$
	96	0.5	37.9	614	$(-, 0.2067, 0.1134)^\top$
	141	0.5	37.9	468	$(-, 0.3117, 0.1647)^\top$
5LDAB	74	0.5	37.8	885	$(0.0391, 0.1242, 0.0750)^\top$
	96	0.5	37.8	753	$(0.0521, 0.1656, 0.1003)^\top$
	141	0.5	37.8	581	$(0.0833, 0.2484, 0.1453)^\top$

compared to 2-level solutions (e.g. [153]).

Note that the superiority of the SiC 3LDAB over the SiC 5LDAB is invariant with respect to the constraints in **Tab. 5.7** as these constraints do have an impact on the *absolute* achievable performance but do not fundamentally alter the *relative* differences between the achievable SiC 3LDAB and SiC 5LDAB performance. This was verified in [82] for variable total semiconductor costs and variable chip areas for both the SiC 3LDAB and SiC 5LDAB (in this case study a fixed semiconductor configuration of the 3LDAB was considered). In [82], the routine of **Fig. 5.12** was carried out for variable total semiconductor costs $\Sigma_{\mathrm{SC,tot}} = \{74, 96, 141\}$€ (in this case study, fixed total costs of $\Sigma_{\mathrm{SC,tot}} = 96$€ were assumed). The corresponding calculated reference values $\vec{\Pi}^*$ are shown in **Tab. 5.10**. It can be seen that the transformer turns ratio , the series inductor value and the relative chip area distribution are invariant from the total semiconductor costs $\Sigma_{\mathrm{SC,tot}}$. Investigations show that these values are only a function of the selection and weighting of the operating points. Due to varying values of the parasitic output capacitances as a function of the absolute chip areas, the commutation inductor value must be adjusted to guarantee complete ZVS at $f_{\mathrm{sw}}^* = 50\,\mathrm{kHz}$, i.e. larger chip areas require more reactive current and thus lower values of L_c. The obtained Pareto fronts of [82] are depicted in **Fig. 5.18**. It can be seen that allowing for variable chip areas/semiconductor costs does not significantly alter the *relative* differences between the achievable SiC 3LDAB and SiC 5LDAB performance. In particular, the SiC 3LDAB is still clearly superior over the SiC 5LDAB due to the same reasons as stated above.

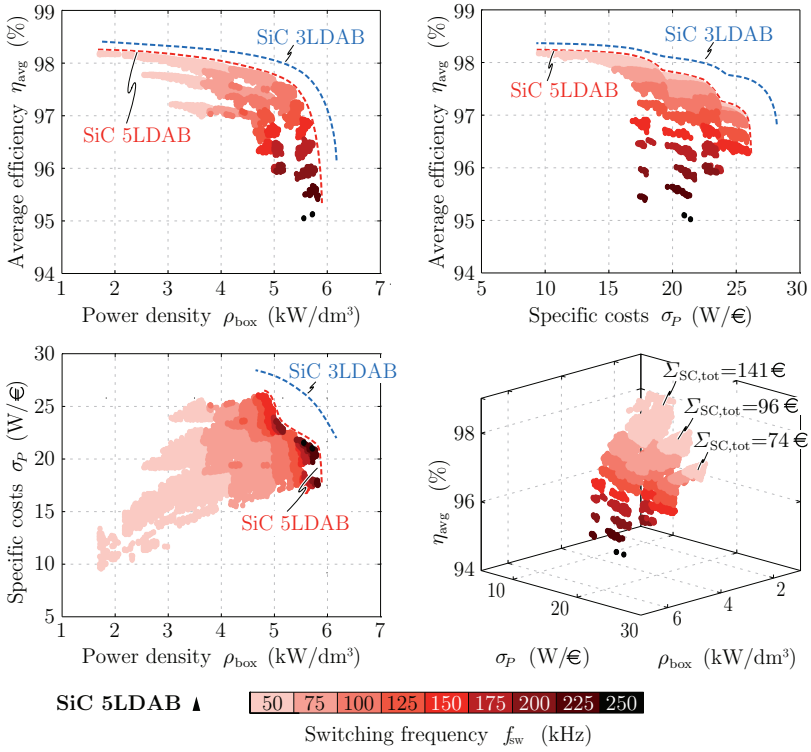


Fig. 5.18: Calculated Pareto fronts from [82] for the SiC MOSFET-based 5LDAB and projected Pareto fronts of the SiC 3LDAB. The variable chip areas from **Tab. 5.10** are employed with total semiconductor costs of $\Sigma_{SC,tot} = \{74, 96, 141\}$ €. The comparison to **Fig. 5.13** and **Fig. 5.14** shows that variable chip areas/costs do not modify the main finding of this case study, i.e. the fundamental superiority of the SiC 3LDAB.

Potential of the 5LDAB

The analysis shows that the higher complexity of the 5LDAB cannot be justified for the given application in this work. However, the 5LDAB may still have a potential in other applications. These may include applications with an even wider voltage range and/or applications with a high efficiency weighting of operating points in the high voltage regime and/or medium voltage applications. For the latter, similar 5LDAB

topologies were proposed in literature [154–156] to eliminate the device dynamic and static voltage sharing problem of otherwise cascaded semiconductors. With regard to alternative applications it is again proposed to employ the virtual prototyping routine of this thesis in order to obtain a comprehensive and quantitative decision base regarding the selection of the 3LDAB or the 5LDAB.

Potential of SiC

SiC is an enabling technology for the given application where the demonstrated performance with respect to efficiency, volume and costs cannot be achieved with Si IGBT or Si MOSFET-based solutions. The main disadvantage of Si IGBTs is found to be the loss of soft-switching whereas the drawbacks of Si MOSFETs are the lack of viable 1200 V components, the high specific C_{oss} (which complicates ZVS operation) and the comparably high costs.

ZVS

The presented analysis shows that complete ZVS is difficult to achieve at elevated frequencies mainly due to limited relative dead times and reactive currents. The analysis finds that parasitic layout capacitances arising from the PCB, the passive components and in particular from the semiconductor packages (capacitance to the heat sink) pose a limiting factor for ZVS.

Magnetics

Another fundamental limitation is found with respect to the design of HF chokes with pure AC excitation and low inductance values. The maximum permissible air gap length prevents designs with balanced core and winding losses as the maximum number of turns is limited by the required inductance value. This can cause situations where the inductor volume increases despite increasing frequencies. Here, low-loss core materials featuring a low permeability and/or core geometries allowing for multiple distributed air gaps can possibly help to overcome this limitation.

5.7.2 Conclusion

Several main conclusions can be drawn from the presented work:

- The extensive waveform, loss and thermal measurements presented in this chapter show that the proposed modeling framework can accurately describe a complex converter system. Therefore, the results of the virtual prototyping routine proposed in this work which employs this modeling framework can be trusted with high confidence.
- The results of the proposed MOO-based virtual prototyping routine prove to be both insightful and useful. In particular, the calculations show in detail how the implemented hardware prototype should be altered in order to achieve substantially improved losses, volumes and costs.
- The systematic analysis of the results generated by the virtual prototyping routine reveal several fundamental performance limitations of the employed magnetics and semiconductor packages. This may serve as a motivation and trigger for novel and innovative approaches and solutions in these fields.

6

Case Study II: DC/AC Converter System

This chapter presents the second case study of this thesis in which the proposed virtual prototyping routine is employed. The case study investigates a 10 kW DC/AC PV converter system in a residential application. The focus of the investigations is set on the analysis of the potential of SiC in PV and the comprehensive comparison to state-of-the-art Si-based systems. For this purpose, the MOO-based virtual prototyping routine and models presented in this thesis are employed to carry out a systematic η-ρ-σ Pareto optimization of three different Si- and SiC-based concepts: a state-of-the-art hard switched 3-level Si IGBT system is compared to a less complex hard-switched 2-level SiC MOSFET system and to a soft-switched interleaved 2-level SiC MOSFET system featuring a similar complexity as the benchmark Si system. A subsequent life cycle cost (LCC) analysis is used to determine the best concept and the best particular design. The case study presented in this chapter is based on the work in [53, 83].

This chapter is organized as follows: the background and motivation of the case study is presented in Section 6.1. Section 6.2 describes the features of the selected topologies and modulation schemes. Section 6.3 details the characteristics and costs of the employed components and materials whereas Section 6.4 focuses on the associated multi-physics models. Section 6.5 presents the employed design and optimization routines, followed by Section 6.6 and Section 6.7 which summarize the results of the conducted Pareto optimization and LCC analysis.

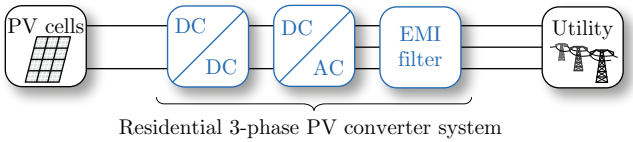


Fig. 6.1: Typical architecture of a residential PV converter system in a grid-tied application. The system consists of a DC/DC boost converter stage, a DC/AC inverter stage and an EMI filter. The main specifications are listed in **Tab. 6.1**.

Tab. 6.1: Main specifications of the 3-Phase PV converter system of **Fig. 6.1** as considered in this study.

Rated power	P_r	10 kW
Input voltage range	$[V_\mathrm{mpp,min}, V_\mathrm{mpp,max}]$	$[400, 800]$ V
Maximum input current	$I_\mathrm{mpp,max}$	22.5 A
Peak grid phase voltage @ f_g=50 Hz	$\hat{V}_\mathrm{g}$	$(325 \pm 10\,\%)$ V

6.1 Motivation

In the course of a rapidly emerging market during the 1990s and 2000s, PV converter systems saw an unprecedented increase of the conversion efficiency from below 90 % to above 98 % [6, 73, 157, 158]. After several downturns of the global economy and a slower growth of the market in recent years, cost reduction has now become the dominant driver for PV converter systems [6,10,72,73]. Against this background, there has been an ongoing discussion in literature on whether and how the commercial introduction of SiC transistors can contribute to further improvements of PV converters and most notably towards lower costs. Although the advantages of SiC- over standard Si-based devices have unanimously been found to be the superior blocking voltage capabilities and the significantly decreased switching and conduction losses (e.g. [159]), a literature review shows that divergent opinions exist on how to exploit these best.

For typical residential grid-tied 3-phase applications as depicted in **Fig. 6.1**, [112,158] propose to substitute the Si transistors of given converter systems by SiC without modifying the switching frequency and power density. [112] argues that the accumulated operational revenue as a result of the increased grid feed-in will always be higher than the

savings on smaller components. In contrast, [72, 160, 161] mainly strive for increased power densities by means of higher switching frequencies facilitated by SiC. This strategy mainly aims at lowering the overall component and system deployment costs. A mixed strategy of simultaneously increasing the power density and efficiency was pursued for the converter systems in [73, 162]. Finally, [53, 72, 161, 163, 164] point out that contrary to Si, the availability of SiC renders alternative topologies and modulation schemes attractive which offers further opportunities to lower the system costs in PV. [161] suggests the employment of efficient 1700 V SiC switches in a 3-level single-stage inverter operating at elevated system voltages of up to 1300 V. This allows to omit the DC/DC boost converter stage which is usually required in systems with a maximum system voltage of 1000 V and employing 600/1200 V semiconductors. [53, 72, 163] propose a standard 2-level topology which reduces the system complexity and limits the number of expensive SiC switches. Finally, in [164], triangular-current-mode (TCM) ZVS techniques are proposed for an interleaved 3-level topology.

The case study in this chapter makes three main contributions to the discussion outlined above:

- *Detailed quantitative cost analysis:* the large majority [53, 72, 73, 112, 158, 160–162, 164] of the above cited papers discusses the cost-saving potential of SiC with qualitative considerations and/or relative cost data. Only [163] provides selected absolute component cost data whereas [165] (analyzing single-phase systems) restricts itself to stating the overall system costs. In contrast, a main objective of this case study is the presentation of a detailed quantitative rather than qualitative cost analysis. Both the component hardware costs and the system life cycle costs (LCC) are calculated in a comprehensive way. Cost models for each component are proposed where numerical values for the parameters, i.e. the cost data are provided in detail.

- *Systematic multi-objective optimization:* the consideration of mere costs results in an incomplete picture as other performance measures such as the efficiency or the power density are usually important as well. Moreover, a less significant comparison of Si vs. SiC is attained if non-optimized and incomplete systems (e.g. no EMI filter) are considered. The study in this chapter is based on the Si and SiC converter concepts of **Fig. 6.2** which include the

EMI filters of **Fig. 6.3**. The performance comparison between the concepts is exclusively based on designs which are obtained from a systematic and comprehensive multi-objective optimization regarding the efficiency, power density and the component costs. This approach is in strong contrast to the previously cited literature where largely systems without obvious optimization are compared. Exceptions are [164,165] where, however, only a single performance measure is optimized. Eventually, [112, 160, 161] do not mention the consideration of an EMI filter.

- *Practical considerations:* the analysis attempts to incorporate important practical aspects which influence the system design, such as low-voltage ride-through (LVRT) schemes, balancing of the DC-link midpoint of the 3-level topology and the compliance with the applicable standards and regulations related to the EMI filtering.

In order to conduct the above described cost-aware comparative analysis of the potential of Si and SiC in PV, the novel virtual prototyping routine of this thesis is employed.

6.2 Topologies and Modulation Schemes

The achievable performance of Si and SiC is compared based on the three converter concepts in **Fig. 6.2**. In this chapter, a converter concept is equivalent to a combination of a converter topology, modulation scheme and a semiconductor technology:

(i) *3LPWM:* a widespread and state-of-the-art system in industry is the Si IGBT hard-switched PWM-modulated 3-level T-type inverter topology (3LPWM) of **Fig. 6.2(a)** [72, 158, 166]. This topology in combination with a symmetric boost converter will therefore serve as the Si benchmark system in this work. This all-Si benchmark system is compared to two all-SiC concepts.

(ii) *2LPWM:* following the argumentation of [53, 72, 163], the availability of efficient 1200 V SiC MOSFETs offers an opportunity to revert from a 3-level to a 2-level topology. The simpler 2-level approach is generally preferred due to the lower part count which potentially translates into a higher reliability and lower manufacturing and development costs. Furthermore, a 2-level approach re-

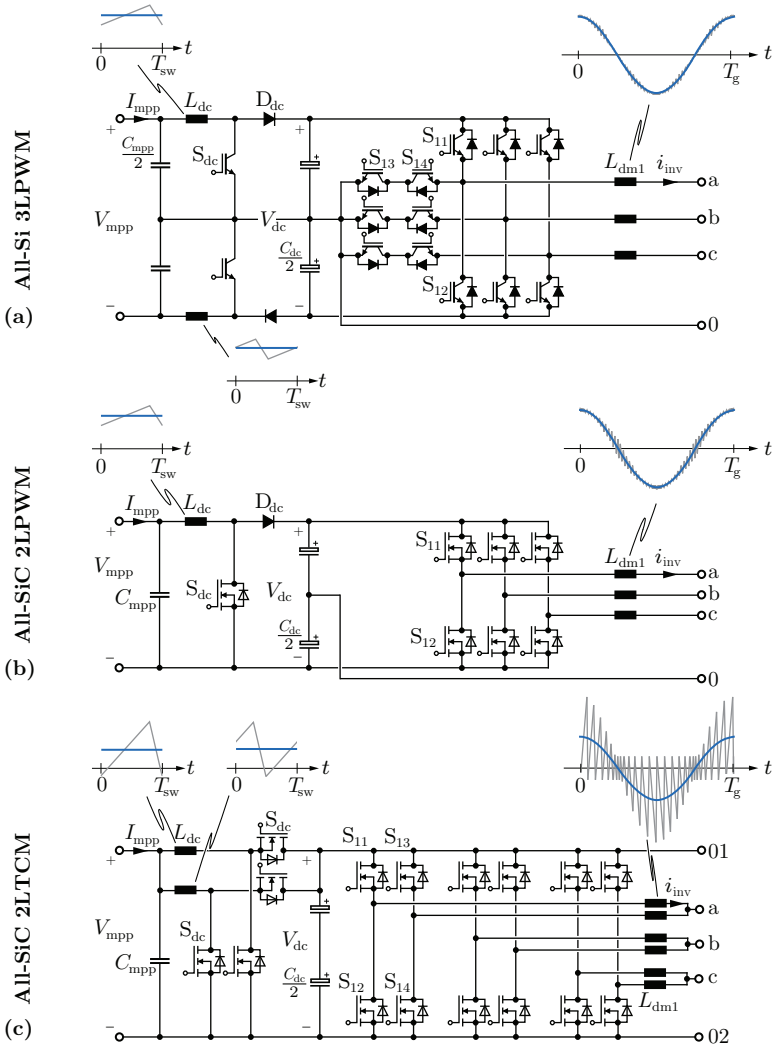


Fig. 6.2: Investigated converter concepts for the grid-tied PV converter system in **Fig. 6.1**. **(a)** All-Si hard-switched PWM-modulated 3-level T-type topology with a symmetric boost converter stage (3LPWM). **(b)** All-SiC hard-switched PWM-modulated 2-level topology with a standard boost converter stage (2LPWM). **(c)** All-SiC soft-switched TCM-modulated double-interleaved 2-level topology with a double-interleaved TCM boost converter stage (2LTCM).

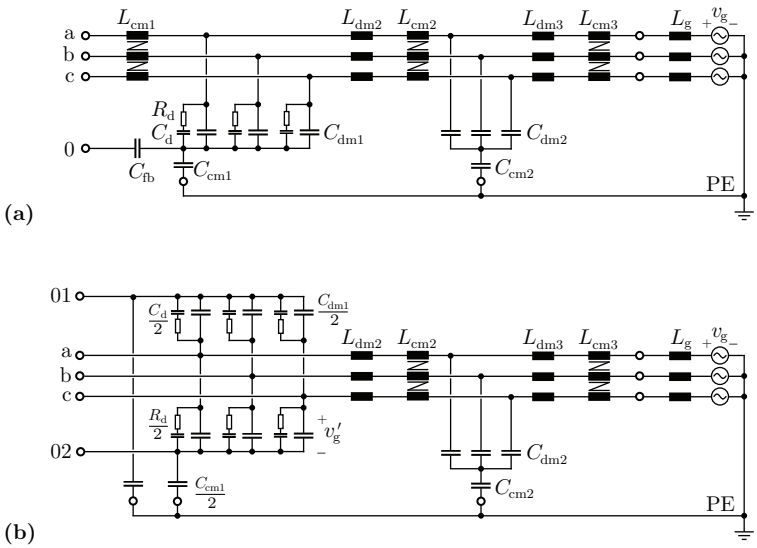


Fig. 6.3: 2-stage EMI filter topologies with connection to the grounded public 50 Hz mains grid. **(a)** EMI filter stage of the 2LPWM and 3LPWM topologies (cf. **Fig. 6.2(a)** and **(b)**). The employed common mode (CM) inductor L_{cm1} in conjunction with the feedback capacitor C_{fb} largely suppress the CM currents. **(b)** EMI filter stage of the 2LTCM (cf. **Fig. 6.2(c)**). The differential mode (DM) filter capacitors C_{dm1} are directly connected to the converter rails and no CM inductor is employed. This allows for a largely decoupled TCM modulation of each phase.

quires only a minimum number of expensive SiC switches. The potential of this SiC approach is thus investigated based on the SiC MOSFET hard-switched PWM-modulated 2-level inverter topology with a standard boost converter (2LPWM) as depicted in **Fig. 6.2(b)**.

(iii) *2LTCM:* a unique advantage of SiC MOSFETs when compared to Si IGBTs are the soft-switching capabilities. This advantage can be deliberately exploited when employing suitable modulation schemes. Therefore, the SiC MOSFET 2LTCM concept as shown in **Fig. 6.2(c)** is investigated where a TCM modulation scheme in a double-interleaved 2-level topology is employed.

A more detailed reasoning and further technical details on the selected topologies and the employed modulation schemes are given below.

6.2.1 Boost Converter Stages

Following the specifications of typical commercial systems [166], a converter input voltage range of $[V_{\mathrm{mpp,min}}, V_{\mathrm{mpp,max}}] = [400, 800]\,\mathrm{V}$ in combination with a maximum input current of $I_{\mathrm{mpp,max}} = 22.5\,\mathrm{A}$ are chosen. This selection allows to track the mainly temperature-dependent solar generator maximum power point (MPP) voltage V_{mpp} which may vary up to a factor of 2 [53, 161]. The boost converter stages are employed to generate a DC-link voltage according to

$$V_{\mathrm{dc}} = \begin{cases} \max\left\{V_{\mathrm{dc,min}}, V_{\mathrm{mpp}} + \Delta V_{\mathrm{dc}}\right\} & V_{\mathrm{mpp}} < V_{\mathrm{dc,min}} \\ V_{\mathrm{mpp}} & V_{\mathrm{mpp}} \geq V_{\mathrm{dc,min}} \end{cases}, \qquad (6.1)$$

$$\begin{aligned} &\text{where for PWM: } V_{\mathrm{dc,min}} = 650\,\mathrm{V}, \;\; \Delta V_{\mathrm{dc}} = 0\,\mathrm{V}\,, \\ &\text{and for TCM: } \quad V_{\mathrm{dc,min}} = 700\,\mathrm{V}, \;\; \Delta V_{\mathrm{dc}} = 50\,\mathrm{V}\,, \end{aligned}$$

which enables grid feed-in independent from V_{mpp}. The boost converters are deactivated in case that $V_{\mathrm{mpp}} \geq V_{\mathrm{dc,min}}$. The switching frequency of the TCM-modulated DC/DC boost converter stage of the 2LTCM concept is strongly dependent on the voltage difference $(V_{\mathrm{dc}} - V_{\mathrm{mpp}})$ (cf. (6.2) below). Therefore, a minimum voltage difference of $\Delta V_{\mathrm{dc}} = 50\,\mathrm{V}$ between V_{mpp} and V_{dc} is required in order to operate the activated boost converter stage, i.e. if $V_{\mathrm{mpp}} < V_{\mathrm{dc,min}}$. At the same time, the switching frequency of the TCM-modulated DC/AC 2LTCM inverter stage is dependent on the voltage difference $\left(V_{\mathrm{dc}}^2 - 4\,v_{\mathrm{g}}'(t)^2\right)$ (cf. (6.4) and **Fig. 6.3**). Therefore, a higher minimum DC-link voltage $V_{\mathrm{dc,min}}$ is required than for the PWM-modulated concepts.

3LPWM

A symmetric hard-switched boost converter topology with interleaved operation is employed in the 3LPWM DC/DC stage as depicted in **Fig. 6.2(a)**. Its main advantage over the conventional boost converter topology of **Fig. 6.2(b)** is its ability to contribute to the DC-link midpoint balancing [167] and thus to reduce the size of the DC-link capacitor C_{dc} (discussed in more detail below). The interleaved operation further helps to reduce the size of the input capacitor C_{mpp}. The higher

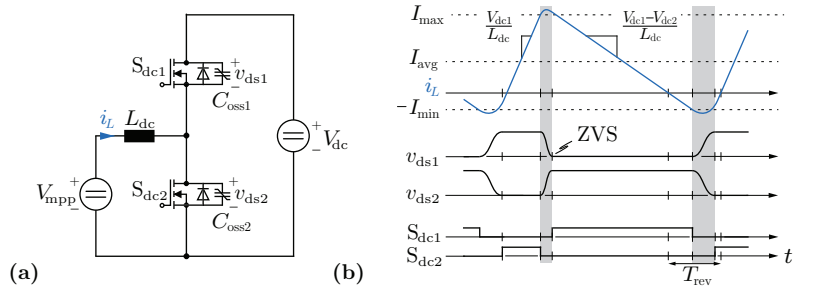


Fig. 6.4: Operating principle of TCM modulation. **(a)** Single branch of the double-interleaved bidirectional boost converter topology employed in the 2LTCM DC/DC stage shown in **Fig. 6.2(c)**. **(b)** Schematic waveforms within a switching period. During the dead time intervals (shaded gray), resonant charging/discharging of the semiconductor parasitic output capacitances $C_{oss1}||C_{oss2}$ can be exploited to achieve ZVS. The switching frequency is variable and largely dependent on the voltages V_{mpp} and V_{dc}, the average load current I_{avg} and the reverse current I_{min} according to (6.2). Note that for clarity reasons, a very long relative duration of the non-linear dead time intervals was chosen in this figure.

total conduction losses (when compared to the conventional boost topology) can be assumed to be compensated by lower total switching losses. This topology can be implemented with low-cost 600 V semiconductors which, together with the savings on the DC capacitors potentially compensates the higher gate driver and sensor costs.

2LPWM

Due to the poor availability of 600 V rated SiC transistors and since no midpoint balancing of the DC-link capacitor C_{dc} is required, a standard hard-switched boost converter topology is employed in the 2LTCM DC/DC stage as shown in **Fig. 6.2(b)**.

2LTCM

For the 2LTCM DC/DC stage, a double-interleaved bidirectional boost converter topology is employed as shown in **Fig. 6.2(c)**. This booster is operated with a soft-switched ZVS TCM modulation scheme. The basic principle of TCM modulation is illustrated in **Fig. 6.4** and briefly

discussed below. More detailed information can be found in [168, 169] along with hardware implementations and experimental results. Note that general information on ZVS of MOSFETs can be found in Section 3.1.

The TCM modulation scheme relies on a variable switching frequency $f_{\mathrm{sw,tcm}}^{\mathrm{dc}}$ which depends on the desired average inductor current I_{avg}, the reverse current I_{min} and the input and output voltages V_{mpp} and V_{dc}, respectively. It can be approximated with

$$f_{\mathrm{sw,tcm}}^{\mathrm{dc}} \approx \frac{V_{\mathrm{mpp}}(V_{\mathrm{dc}} - V_{\mathrm{mpp}})}{2(I_{\mathrm{avg}} + I_{\mathrm{min}})L_{\mathrm{dc}}\, V_{\mathrm{dc}}} = \frac{V_{\mathrm{mpp}}(V_{\mathrm{dc}} - V_{\mathrm{mpp}})}{(I_{\mathrm{max}} + I_{\mathrm{min}})L_{\mathrm{dc}}\, V_{\mathrm{dc}}}\,, \tag{6.2}$$

if the duration of the dead time intervals are neglected. Whereas I_{avg} is determined by the power which has to be transferred, the reverse current I_{min} is given through

$$I_{\mathrm{min}} = \max\left\{I_{\mathrm{min}}^{\mathrm{d}},\, I_{\mathrm{min}}^{Q_{\mathrm{oss}}}(V_{\mathrm{mpp}}, V_{\mathrm{dc}}),\, I_{\mathrm{min}}^{f_{\mathrm{sw,max}}}\right\}. \tag{6.3}$$

In (6.3), $I_{\mathrm{min}}^{\mathrm{d}}$ denotes the minimum achievable reverse current due to the delay of the zero-crossing detection circuitry which detects the beginning of the reverse current interval T_{rev} as shown in **Fig. 6.4**. Generally, the zero-crossing detection is required to measure/detect the sign/change of the sign of the current i_L in the inductor L_{dc} to operate and control the respective TCM branch. $I_{\mathrm{min}}^{Q_{\mathrm{oss}}}$ is the required current to accomplish the complete resonant charging/discharging of the parasitic semiconductor output capacitances $C_{\mathrm{oss1}}||C_{\mathrm{oss2}}$ during the (reverse) dead time interval T_{d} which enables (complete) ZVS. Finally, increased reverse currents yielding longer reverse intervals T_{rev} can also be utilized to limit the maximum switching frequency in case of low average currents/low-load operation and/or adverse voltages V_{mpp} and V_{dc}. Whereas $I_{\mathrm{min}}^{f_{\mathrm{sw,max}}}$ can be calculated using (6.2), the formula for $I_{\mathrm{min}}^{Q_{\mathrm{oss}}}$ can be derived with the analysis on complete ZVS presented in Section 3.1. Note that in low-load operation the reverse current I_{min} can be larger than the average current I_{avg}. In such a situation one out of the two interleaved boost converter TCM branches in **Fig. 6.2(c)** is turned off to achieve lower overall conduction and switching losses. At full load, the interleaving of the two branches allows to reduce the turn-off losses in the semiconductors and the current stress of the capacitors.

6.2.2 Inverter Stages

The DC/AC inverter stages of the three considered concepts employ a one-sixth third harmonic common mode (CM) injection [170] in the modulation scheme to extend the linear range of modulation to $\frac{2}{\sqrt{3}} \approx 1.15$. As a consequence, the potential of the solar generator with respect to earth oscillates at a frequency of $3 \cdot f_{\mathrm{g}} = 150\,\mathrm{Hz}$. The corresponding LF 150 Hz peak leakage current to ground can be estimated with [171] and stays below the required value of $\sqrt{2}{\cdot}50\,\mathrm{mA}$ stated in [172, 173].

3LPWM

During regular operation, the 3-level T-type topology of the 3LPWM DC/AC inverter stage is operated with a standard 3-level PWM modulation scheme based on 3-phase sinusoidal references and a superimposed third harmonic is employed. The resulting LF current into the DC-link midpoint [174] can partially be compensated by means of a corresponding modulation of the load currents in the symmetric boost converter [167]. Thereby, part of the LF midpoint variation of C_{dc} is transferred to the input capacitor C_{mpp} where a variation of the midpoint is less critical.

During LVRT where pure reactive power support of the grid is required [175], the inverter-side LF current into the DC-link midpoint becomes excessive. However, no compensating current can be provided by the unidirectional booster (as it is possible during regular operation). As the extended linear range of modulation enabled by the third harmonic injection scheme is not required during LVRT, the zero-sequence scheme proposed in [176] is employed instead which facilitates the control of the DC-link midpoint voltage.

2LPWM

As mentioned above, the 2-level topology of the 2LPWM DC/AC inverter stage is operated with a standard 2-level PWM modulation scheme based on 3-phase sinusoidal references and a superimposed third harmonic.

2LTCM

The double-interleaved 2-level topology of the 2LTCM DC/AC inverter stage is operated with a soft-switched TCM modulation scheme similar

to the associated DC/DC stage. The same operating principles apply as depicted in **Fig. 6.4** where the constant parameters V_{dc}, I_{avg} and I_{min} vary over the course of the mains period T_{g} and thus become time-dependent. Accordingly, the switching frequency of one phase varies over a mains period according to

$$f_{\mathrm{sw,tcm}}^{\mathrm{ac}}(t) \approx \frac{\left(V_{\mathrm{dc}}^2 - 4\, v_{\mathrm{g}}'(t)^2\right)}{8\big(|i_{\mathrm{avg}}(t)| + i_{\mathrm{min}}(t)\big) L_{\mathrm{dm1}}\, V_{\mathrm{dc}}}\,, \tag{6.4}$$

where $v_{\mathrm{g}}'(t)$ is the voltage across the first stage filter capacitor C_{dm1} as shown in **Fig. 6.3(a)**. The voltage $v_{\mathrm{g}}'(t)$ contains the one-sixth third harmonic CM voltage which is driven by a corresponding third harmonic current as part of $i_{\mathrm{avg}}(t)$. The reverse current $i_{\mathrm{min}}(t)$ is analogously chosen as for the DC case (6.3). For low-load operation, one of the two interleaved branches per phase is turned off.

6.2.3 EMI Filter Stages

A 2-stage output EMI filter topology is chosen as depicted in **Fig. 6.3**. Whereas for the PWM-controlled concepts 2LPWM and 3LPWM the first filter stage largely suppresses any undesired HF CM currents, these currents are an integral part of the TCM operating principle and are thus not suppressed in the first filter stage of the 2LTCM. Therefore, the CM inductor L_{cm1} is omitted and a hard connection of the capacitors C_{dm1} with the inverter rails is established. This allows for a largely decoupled TCM operation of the 2LTCM inverter branches where the full HF content of the individual branch output voltages contribute to the generation of the current ripple.

6.3 Components and Materials

This section discusses the selection of the components and materials which are employed in the different PV converter systems. An overview of all selected components and materials is listed in **Tab. 6.2**. The cost data presented in this section are largely taken from Chapter 4 or empirically collected using the same methods.

Tab. 6.2: Selection of the main components and materials.

Component	3LPWM (all-Si)	2LPWM (all-SiC)	2LTCM (all-SiC)
S_{dc} [1)]	IGW30N60T	C2M0080120D	C2M0080120D
D_{dc} [1)]	IDP45E60	C4D20120D	-
S_{x1}, S_{x2} [1)]	IKW25N120H3	C2M0080120D	C2M0080120D
S_{x3}, S_{x4} [1)]	IKW30N60T	-	C2M0080120D
Heat sink	Custom Al heat sink		
Fans	San Ace adjustable speed low power fans 9GA0412xxx01		
L_{dc}, L_{dm1}	Litz wire [30,355] µm 1-4 × stacked E-cores Epcos ferrite N87	OR	Solid round wire 1-2 × stacked U-cores Metglas amorphous 2605SA1
C_{mpp}	Epcos MKP film capacitors B3277x, $V_r \in \{575, 1200\}$ V		
C_{dc}	Epcos long life electrolytic capacitors B43501x, $V_r = 500$ V		
$L_{dm\{2,3\}}$	Solid round wire & 1-3 × stacked E-cores Magnetics powder KoolMu {40,60} µ		
$L_{cm\{1,2,3\}}$	Solid round wire & 1-5 × stacked toroidal cores Vacuumschmelze nanocrystalline Vitroperm 250F/500F		
$C_{dm\{1,2\}}$, $C_{\{d,fb\}}$	Epcos X2 film capacitors B3292x, $V_r = 305$ V		
$C_{cm\{1,2\}}$	Epcos Y2 film capacitors B3202x, $V_r = 300$ V		

[1)] one device per switch position (no paralleling of devices/variable chip areas)

6.3.1 Semiconductors

The benchmark 3LPWM system employs a combination of discrete 600 V and 1200 V 175 °C rated trench- & fieldstop Si IGBTs and PiN diodes from Infineon. The all-SiC systems 2LPWM and 2LTCM are implemented with discrete 1200 V 150 °C rated 80 mΩ SiC MOSFETs from Wolfspeed. Note, that each converter concept is investigated assuming fixed semiconductor configurations, i.e. paralleling of devices/variable chip areas are not considered. For further details and cost information refer to **Tab. 6.3**.

6.3.2 Cooling System

Custom aluminum heat sinks with forced air cooling are considered. The cooling systems are optimized according to the design and optimization routine described in Chapter 2. Due to the importance of a high part-load efficiency and a high reliability in PV applications, the

low-power fan series 9GA0412xxx01 from Sanyo is selected. This fan series features an expected lifetime of 40 kh at $T_{\mathrm{amb}} = 60\,^{\circ}\mathrm{C}$ and controllable fan speeds for part-load operating points. The cooling system costs Σ_{CS} are calculated using

$$\Sigma_{\mathrm{CS}} = 7.69\,€/\mathrm{dm}^3 \cdot V_{\mathrm{sink}} + \Sigma_{\mathrm{fan}} \,, \tag{6.5}$$

with V_{sink} being the heat sink volume and assuming an extrusion-based heat sink manufacturing process. The fan unit costs of the individual fans were requested from the manufacturer for MOQ = 10 000 units. Again, the unit costs remain in a relatively narrow range $[6.32, 6.78]$ € despite the widely varying fan power. This characteristic is typical as discussed in Section 4.3.

6.3.3 Inductors

The cost model for the inductors,

$$\Sigma_L = \frac{1}{GM}\left(\Sigma_{\mathrm{core}} + \Sigma_{\mathrm{wdg}} + \Sigma_{\mathrm{lab}}\right) , \tag{6.6}$$

where

$$\Sigma_{\mathrm{core}} = N_{\mathrm{stack}} \cdot \Sigma^{\mathrm{fc}}_{\mathrm{core},x} + \sigma_{\mathrm{core},x} W_{\mathrm{core}} \,, \tag{6.7}$$

$$\Sigma_{\mathrm{wdg}} = \Sigma^{\mathrm{fc}}_{\mathrm{wdg},x} + \sigma_{\mathrm{wdg},x} W_{\mathrm{wdg}} \,, \tag{6.8}$$

$$\Sigma_{\mathrm{lab}} = \Sigma^{\mathrm{fc}}_{\mathrm{lab}} + \sigma_{\mathrm{lab},x} W_{\mathrm{wdg}} \,, \tag{6.9}$$

and the underlying numerical parameters as summarized in **Tab. 6.4** are taken from Section 4.3. Details on the selected materials, core and winding types for the different inductors are discussed below.

Main Inductors: L_{dc}, L_{dm1}

Two core/winding material options for the boost DC inductors L_{dc} and the first filter stage AC inductors L_{dm1} are investigated. On the one hand, U-cores made of Metglas 2605SA1 tape-wound amorphous iron are considered. Solid round wires are selected due to the low costs and the high flexibility regarding the geometries when compared to foil or flat winding wires. Preliminary analysis in [57, 80] finds that this material combination shows good trade-offs between the volume, losses and the costs for PWM DC/AC applications. This is mainly due to the high

Tab. 6.3: Data of the selected semiconductors.

Component	Type	Ratings	Σ_{SC} (€) [1)]
IDP45E60	Si PiN diode	600 V / 175 °C	0.85
IGW30N60T	Si IGBT	600 V / 175 °C	1.24
IKW30N60T	Si IGBT / PiN diode	600 V / 175 °C	1.61
IKW25N120H3	Si IGBT / PiN diode	1200 V / 175 °C	2.41
C4D20120D	SiC Schottky diode	1200 V / 175 °C	8.11
C2M0080120D	SiC MOSFET	1200 V / 150 °C	8.05

[1)] based on manufacturer data for a minimum order quantity of MOQ=50 k

Tab. 6.4: Cost data for the inductor cost model (6.6).

Core [1)]:	2605SA1 U-cores	N87 E-cores	KoolMu E-cores	Vitroperm Coated toroids
Winding [2)]:	Round	Litz	Round	Round
$\Sigma^{fc}_{core,x}$ (€)	5.10	0.08	0.60	1.05
$\sigma_{core,x}$ (€/kg)	14.10	7.50	10.20	48.90
$\Sigma^{fc}_{wdg,x}$ (€)	1.00	0.25	0.25	0.05
$\sigma_{wdg,x}$ (€/kg)	10.00	variable [3)]	10.00	10.00
$\Sigma^{fc}_{lab,x}$ (€)	0.75	0.75	0.75	1.00
$\sigma_{lab,x}$ (€/kg)	7.00	7.00	7.00	9.31

[1)] MOQ = 50 k core sets [2)] MOQ = 1 metric ton [3)] AWG{48,46,44,41,38,32,27} $\triangleq$ {30,40,50,71,100,200,355} µm → {111.5, 58.5, 32.5, 23.5, 21.5, 18.5, 16.5} €/kg

Tab. 6.5: Cost data and number of employed gate driver and measurement circuits in the converter topologies to calculate the total auxiliary circuitry costs Σ_{AUX} in (6.11).

Circuit:	GD	GD^{single}_{iso}	GD^{shared}_{iso}	M_v	M_i
Σ_x (€)	1.7	3.4	2.2	1.0	2.0
# 2LPWM	4	3	0	5	4
# 3LPWM	4	1	9	7	5
# 2LTCM	8	8	0	5	4+2 [1)]

[1)] the costs of the 8 zero crossing detection circuits is equivalent to $2 \cdot \Sigma_{M_i} = 4$€

useful maximum flux density of $B_{\max} \approx 1.2\,\mathrm{T}$ paired with comparably low losses. On the other hand, the operating principle of TCM modulation with dominant HF excitations asks for excellent HF winding properties and very low core losses in L_{dc} and L_{dm1}. As a consequence, Epcos N87 ferrite in combination with litz wire with strand diameters between 30 and 355 µm were additionally selected. The considered ferrite cores feature an E-shape with a single air gap on the center leg to minimize radiated EMI. Both core/winding material options are investigated in combination with all three converter concepts.

DM Filter Inductors: L_{dm2}, L_{dm3}

For the remaining DM filter inductors, achieving low magnetic stray fields and compactness to minimize the parasitics is crucial. Therefore, gapless core materials with a high maximum flux density are desirable. KoolMu powder cores from Magnetics in combination with solid round wire windings were found to meet these requirements best.

CM Filter Inductors: L_{cm1}, L_{cm2}, L_{cm3}

The CM inductors are implemented with round wire and toroids made of nanocrystalline Vitroperm 250F/500F from Vacuumschmelze.

6.3.4 Capacitors

The capacitor cost models and parameters are taken from Section 4.3.

DC Capacitors: C_{mpp}, C_{dc}

Whereas the input capacitor C_{mpp} is implemented with MKP film technology from Epcos (series B3277x) with a rated voltage of $V_{\mathrm{r}} \in \{575, 1200\}\,\mathrm{V}$, the DC-link capacitor C_{dc} is realized with Epcos long-life aluminum electrolytic capacitors (series B43501x, $V_{\mathrm{r}} = 500\,\mathrm{V}$). The high capacitance of electrolytic capacitors in the DC-link is mainly required for a sufficient control stability.

AC Filter Capacitors: $C_{\mathrm{dm\{1,2\}}}$, C_{d}, C_{fb}, $C_{\mathrm{cm\{1,2\}}}$

The filter capacitors are implemented with Epcos X2 and Y2 capacitors (series B3292x and B3202x).

6.3.5 PCB and Auxiliary Electronics

Standard 4-layer 35 µm copper PCBs with estimated costs of

$$\Sigma_{\mathrm{PCB}} = 0.18\,€ + 1.5\,€/\mathrm{dm}^2 \cdot A_{\mathrm{PCB}}\ , \tag{6.10}$$

are assumed. The total costs of the auxiliary circuitry Σ_{AUX} is the sum of the costs for the voltage and current measurement circuits Σ_{M}, the gate driver circuits Σ_{GD} and the additional costs $\Sigma_{\mathrm{AUX+}}$ for control ICs, auxiliary power supplies, connectors, line circuit breakers etc.,

$$\Sigma_{\mathrm{AUX}} = \Sigma_{\mathrm{GD}} + \Sigma_{\mathrm{M}} + \Sigma_{\mathrm{AUX+}}\ . \tag{6.11}$$

The additional offset costs $\Sigma_{\mathrm{AUX+}} = 77\,€$ are assumed to be the same for all topologies and are thus only roughly estimated. Note that housing costs depend on the converter volume and can thus not be included as constant costs in $\Sigma_{\mathrm{AUX+}}$. More effort is put on the estimation of the gate driver and measurement circuit costs as the number of employed circuits varies for the three topologies (cf. **Tab. 6.5**). The gate driver costs were calculated based on the proven circuits employed in the switching loss test benches presented in Section 3.1. It is distinguished between non-isolated, single isolated and isolated gate drivers with a shared power supply (e.g. for the switches $\mathrm{S}_{x1}/\mathrm{S}_{x4}$ in the 3LPWM). All circuits employ the same gate driver (IXYS) and optocoupler (where required; Avago). The assumed voltage (resistive voltage dividers) and current (Allegro current sensors) measurement circuits are used by the prototypes in [153, 177]. Finally, the zero-crossing detection circuits of the 2LTCM can be implemented with low-cost toroid current transformers, a voltage clamping circuit and a comparator. The respective costs based on large MOQ = 50 000 units are depicted in **Tab. 6.5**. The discussion with industry confirmed the proposed costs to be realistic for the assumed MOQs.

6.4 Modeling

This section details the modeling of the converter behavior and the selected components. From a component point of view, the main difference between the analyzed concepts resides in the different employed semiconductor technologies and how the main inductors are utilized / excited. Since these components are responsible for the majority of the

losses, volumes and the costs, a high effort has been devoted to the detailed switching and core loss modeling to improve the relative accuracy of the results. The majority of the required models and model parameters for this case study can be derived from the modeling framework presented in Chapter 3.

6.4.1 Behavioral Models

The behavioral models are used to determine the operating-point dependent control and modulation schemes and to accordingly synthesize the current and voltage waveforms in all components of the system. The waveforms are synthesized in time and frequency domain and were rigorously checked by means of circuit simulations. For the waveform synthesis, the following simplifications are made:

(i) Lossless components are assumed;

(ii) Parasitic effects, such as stray capacitances and inductances, electromagnetic and thermal couplings are, apart from a few exceptions in the filter design (cf. Section 6.5), neglected;

(iii) The ratio between the switching frequency and the fundamental frequency f_{sw}/f_g is assumed to tend towards infinity. This simplifies the AC waveform calculations as a constant grid voltage can be assumed for the duration of a switching period (cf. [170]); and

(iv) Infinite switching speeds are assumed and the non-linear dead time intervals are neglected yielding ideal rectangular voltage patterns.

Note that the simplifications (i) and (ii) are essential to enable the separation of the virtual prototyping routine into a global system-level loop and subordinate component-level optimization loops as further discussed in Section 6.5. The loss of accuracy due to the assumption in (iii) is negligible as the switching frequencies considered in this study are high. The implication of (iv) is also moderate but mainly benefits the 2LTCM concept: during the soft-switching transitions, no active power can be transferred (cf. **Fig. 6.4(b)**). Therefore, slightly higher currents causing higher conduction losses would occur if the dead times were taken into account. Note, however, that the dead times at $I_{\max}$ (DC/DC stage) and $i_{\max}(t)$ (DC/AC stage) are typically very short due to the high amplitudes of the switched currents. Furthermore, complete

ZVS is always guaranteed as the reverse currents I_{rev} and $i_{\mathrm{rev}}(t)$ are controlled accordingly (cf. (6.3)).

6.4.2 Semiconductor Models

Conduction Losses

The conduction losses P_{c} are computed considering the current- and junction temperature-dependent output characteristics $V_{\mathrm{ce}}\big(i_{\mathrm{ce}}(t), T_{\mathrm{j}}\big)$, $R_{\mathrm{ds,on}}\big(i_{\mathrm{ds}}(t), T_{\mathrm{j}}\big)$ and $V_{\mathrm{f}}\big(i_{\mathrm{ac}}(t), T_{\mathrm{j}}\big)$ respectively, of the considered IGBT, MOSFET and diode devices. The respective values for V_{ce}, $R_{\mathrm{ds,on}}$ and V_{f} are taken from the data sheets and subsequently interpolated. A gate voltage of $V_{\mathrm{gate}} = 15\,\mathrm{V}$ was considered for all Si IGBTs and a gate voltage of $V_{\mathrm{gate}} = 20\,\mathrm{V}$ for the SiC MOSFETs.

Switching Losses

The switching losses P_{sw} of a single device are calculated using

$$P_{\mathrm{sw}}\big(I_{\mathrm{sw,on}}, I_{\mathrm{sw,off}}, V_{\mathrm{sw,on}}, V_{\mathrm{sw,off}}, T_{\mathrm{j}}\big) = \frac{1}{T_{\mathrm{g}}} \cdot \sum_{i=1}^{N_{\mathrm{sw}}} \Big[E_{\mathrm{on}}\big(I_{\mathrm{on},i}, V_{\mathrm{on},i}, T_{\mathrm{j}}\big) + E_{\mathrm{off}}\big(I_{\mathrm{off},i}, V_{\mathrm{off},i}, T_{\mathrm{j}}\big) \Big], \tag{6.12}$$

with N_{sw} being the number of full switching cycles (i.e. pairs of turn-on and turn-off switching instants) during the fundamental mains period T_{g} and $I_{\mathrm{on/off},i}$ and $V_{\mathrm{on/off},i}$ the respective switched currents and voltages. The parametrization, i.e. the switching loss energies of all combinations of topologies and semiconductors must experimentally be determined to enable accurate and significant results. The utilized switching loss measurements are presented in Section 3.1.

Gate Driver Losses

The gate driver losses P_{GD} are estimated with

$$P_{\mathrm{GD}} = \frac{1}{T_{\mathrm{g}}} \cdot Q_{\mathrm{gate}} \cdot V_{\mathrm{gate}} \cdot N_{\mathrm{sw}}\ , \tag{6.13}$$

where V_{gate} denotes the gate voltage and Q_{gate} the gate charge. Again, $V_{\mathrm{gate}} = 15\,\mathrm{V}$ and $V_{\mathrm{gate}} = 20\,\mathrm{V}$ is assumed for the Si IGBTs and SiC

MOSFETs, respectively. The corresponding gate charges can be found in the data sheets where the (weak) dependency of the gate charge from the blocking voltage and switched current is not modeled. Note that the model in (6.13) slightly overestimates the gate driver losses in case of soft switching-of the SiC MOSFETs as already discussed in Section 5.3.

6.4.3 Cooling System

The cooling system design and optimization routine is based on the models presented in Section 3.2. The heat sink dimensioning takes into account the possible semiconductor arrangements which means that the minimum top surface is defined by the number and dimensions of the semiconductor packages. The fan losses are calculated with

$$P_{\mathrm{CS}} = \frac{1}{\eta_{\mathrm{sup}}} \cdot P_{\mathrm{CS}} \ , \tag{6.14}$$

where a power supply efficiency of $\eta_{\mathrm{sup}} = 75\,\%$ is assumed.

6.4.4 Inductors

The inductor design routine is largely based on the loss models, thermal models and reluctance models presented in Section 3.3. In addition to the effects discussed in Section 3.3, the reluctance model employed in this case study also considers the distinct dependency of the permeability of the CM inductor core materials (Vitroperm 250F/500F) on the frequency. The core losses P_{core} are computed using data sheet loss parameters for the KoolMu materials (negligible HF excitations of the respective inductors L_{dm1} and L_{dm2}) and Vitroperm 250F/500F (very low losses). Contrarily, due to the high impact on the system performance, systematic and extensive core loss measurements were conducted for the materials N87 and 2605SA1 as the respective available data sheet information was found to be insufficient/incomplete. Besides the systematic measurement of the frequency-, temperature- and AC flux-dependencies, special effort has been put on investigating the adverse effects of DC flux offsets in N87 and the air gap length in 2605SA1. All measurements and a broader discussion of the topic can be found in Section 3.3.

6.4.5 Capacitors

The current-dependent losses P_C in the capacitors are calculated based on data sheet loss parameters. In order to account for the reduced cooling surface of the capacitors when arranged in bulk and to increase the lifetime, the data sheet-based permissible maximum rms currents were lowered by a factor of $\sqrt{2}$ (reduction of the losses by a factor of 2).

6.4.6 PCB and Auxiliary Electronics

For simplicity reasons, the PCB losses (such as dielectric and conduction losses) are neglected. The losses of the auxiliary circuits P_{AUX} include the gate driver losses P_{GD} and the power consumption of the control and measurement electronics P_{control},

$$P_{\mathrm{AUX}} = \frac{1}{\eta_{\mathrm{sup}}} \cdot (P_{\mathrm{GD}} + P_{\mathrm{control}}) \,, \tag{6.15}$$

where again a supply efficiency of $\eta_{\mathrm{sup}} = 75\,\%$ is assumed. In spite of slightly differing measurement circuit counts (cf. **Tab. 6.5**), constant control losses of $P_{\mathrm{control}} = 5\,\mathrm{W}$ are assumed for all topologies.

6.5 Design and Optimization Routines

This section discusses the details of the application-specific MOO-based virtual prototyping routine and the employed performance indices and optimization constraints. Whereas the component-level design routines have largely been discussed in Chapter 2, this section mostly deals with the application-specific models and routines in the global system-level loop.

6.5.1 Virtual Prototyping Routine

If parasitic electromagnetic and thermal coupling effects are neglected, the converter components are solely coupled by means of their impact on the current and voltage waveforms in the circuit. As proposed in Chapter 2, from a conceptual point of view, this observation suggests to divide the available design variables of the optimization into two distinct categories as follows:

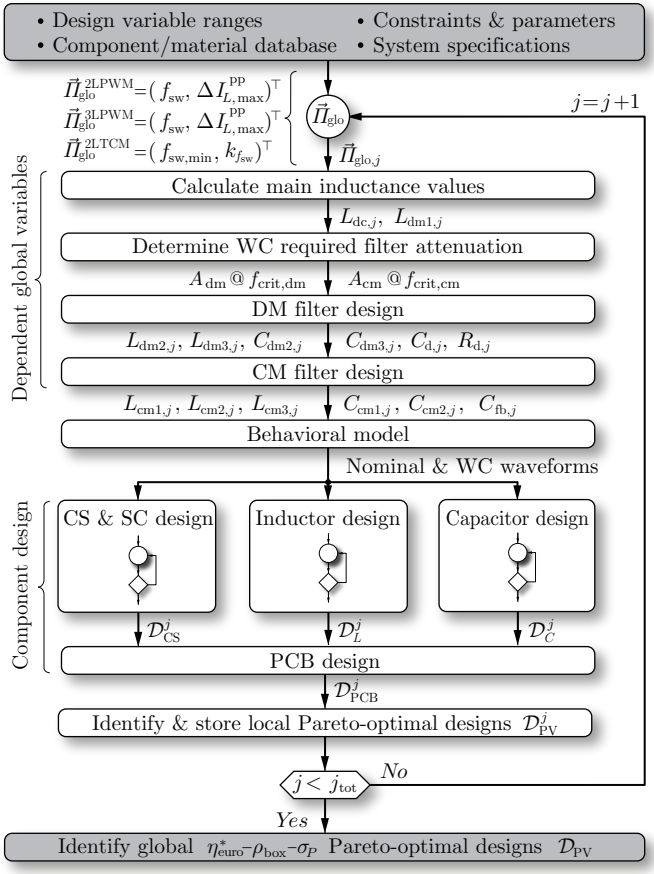


Fig. 6.5: Simplified flow chart of the employed MOO-based virtual prototyping routine for the DC/AC PV converter concepts in this study. The set of the independent global design variables $\vec{\Pi}_{\text{glo}}$ is iterated in the global system-level loop. After the calculation of remaining and dependent global variables and the necessary waveforms, the individual components are optimized within independent subordinate routines. The PCB is designed after the main components due to the dependent PCB area. Non-optimal component designs or components which are not part of an optimal system design $\mathcal{D}_{\text{PV}}^{j}$ are discarded as early as possible to avoid excessive numbers of designs and combinations in the final global Pareto-analysis.

Tab. 6.6: Employed optimization parameters and constraints.

Nom. ambient temperature	$T_{\mathrm{amb,nom}}$	30 °C
Nom. displacement factor	$\cos(\phi_{\mathrm{nom}})$	1.0
Nom. grid phase voltage	$\hat{V}_{\mathrm{g,nom}}$	325 V
Max. ambient temperature	$T_{\mathrm{amb,max}}$	60 °C
Max. MPP voltage ripple	$\Delta V^{\mathrm{pp}}_{C_{\mathrm{mpp}},\mathrm{max}}$	2 V
Max. DC-link voltage ripple [1)]	$\Delta V^{\mathrm{pp}}_{C_{\mathrm{dc}},\mathrm{max}}$	6.5 V
Max. junction temperature [2)]	$T_{\mathrm{j,max}}$	$T_{\mathrm{j,r}} - 25$ °C
Max. winding hot spot temperature	$T_{\mathrm{wdg,max}}$	125 °C
Max. 2605SA1 core temperature	$T^{\mathrm{2605SA1}}_{\mathrm{core,max}}$	125 °C
Max. N87 core temperature	$T^{\mathrm{N87}}_{\mathrm{core,max}}$	100 °C
Max. 2605SA1 flux density	$B^{\mathrm{2605SA1}}_{\mathrm{max}}$	1.2 T
Max. N87 flux density	$B^{\mathrm{N87}}_{\mathrm{max}}$	0.31 T
Max. inductance drop	$L(I_{L,\mathrm{max}})/L_0$	0.75
Max. total relative air gap length [3)]	$\bar{l}_{\mathrm{ag,max}}$	0.5

[1)] also applicable to the 3LPWM midpoint potential of C_{dc}

[2)] for rated semiconductor junction temperatures $T_{\mathrm{j,r}}$ see **Tab. 6.3**

[3)] with respect to the leg width (U-cores) or center leg width (E-cores)

(i) Global design variables with a possibly significant impact on the waveforms. That is, apart from the converter concepts, the switching frequency f_{sw} as well as all inductance and capacitance values.

(ii) Groups of component-related variables with a small or negligible impact on the waveforms. These are:

- 6 variables for the main inductors, i.e. L_{dc} and L_{dm1} (core material, core type and # of stacked cores, # of turns, turn and strand diameter) and 4 variables for the remaining inductors (core type and # of stacked cores, # of turns and turn diameter)
- 4 cooling system design variables (heat sink length and # of fins, # and type of fans), and
- 1 variable for each capacitor (type).

The second category of variables does not influence the waveforms if its impact on the component losses and on the (geometry-dependent)

parasitic stray capacitances and inductances of the components are neglected. Both assumptions are usually sufficiently accurate approximations. As a consequence, the virtual prototyping routine of **Fig. 6.5** can be employed. As in Chapter 5, the PV-specific routine of **Fig. 6.5** closely corresponds to the generic routine proposed in Chapter 2: the global system-level loop iterates over the independent global design variables where for each iteration the remaining and dependent global design variables of category (i) are determined first. The nominal and worst case waveforms can then be calculated using the converter behavioral model. Note that the converter components are dimensioned for the worst case operating conditions whereas the efficiencies are calculated for nominal conditions (cf. **Tab. 6.6**). With respect to the identification of the worst case operating points of each component, varying grid and input voltages, a displacement factor range of $\cos(\phi) = [0.95_{\text{lagging}}, 0.95_{\text{leading}}]$ [178] and pure reactive current supply to the grid up to the nominal current amplitude during LVRT [175] are taken into account. The calculation of the waveforms is followed by the component design loops where each component is individually optimized by means of iterating over the component-specific category (ii) design variables. At this stage, only Pareto-optimal component designs are further considered. In a next step, the Pareto-optimal converter designs $\mathcal{D}_{\text{PV}}^{j}$ as a combination of the calculated component designs are identified and stored. After the execution of the global loop, the overall Pareto-optimal converter designs are identified amongst $\bigcup_j \mathcal{D}_{\text{PV}}^{j}$. The performance of an aggregated PV converter design is assessed by means of the three following performance measures:

(i) The weighted efficiency,

$$\eta_{\text{euro}}^{*} = \frac{\eta_{\text{euro}}^{525\,\text{V}} + \eta_{\text{euro}}^{575\,\text{V}} + \eta_{\text{euro}}^{625\,\text{V}}}{3} \,, \tag{6.16}$$

where the European efficiency

$$\begin{aligned} \eta_{\text{euro}} =& 0.05 \cdot \eta_{0.03 \cdot P_{\text{r}}} + 0.1 \cdot \eta_{0.1 \cdot P_{\text{r}}} + 0.2 \cdot \eta_{0.2 \cdot P_{\text{r}}} + \\ & 0.3 \cdot \eta_{0.3 \cdot P_{\text{r}}} + 0.5 \cdot \eta_{0.5 \cdot P_{\text{r}}} + 1 \cdot \eta_{1.0 \cdot P_{\text{r}}} \,, \end{aligned} \tag{6.17}$$

is calculated and subsequently averaged for three different MPP voltages, i.e. $V_{\text{mpp}} = \{525, 575, 625\}\,\text{V}$. Field studies show that

at the selected MPP voltages the majority of the energy is harvested [179]. Note that the selected voltage levels do not permit to disable the boost converter stage in any of the considered topologies;

(ii) The power density $\rho_{\text{box}} = {}^{P_\text{r}}/_{V_{\text{box,tot}}}$ based on the total boxed volume $V_{\text{box,tot}}$ of the converter components; and

(iii) The specific costs $\sigma_P = {}^{P_\text{r}}/_{\Sigma_{\text{tot}}}$ with Σ_{tot} being the total component costs.

The employed parameters and constraints in the virtual prototyping routine of **Fig. 6.5** are listed in **Tab. 6.6**.

6.5.2 Separation of Global Design Variables

From the employed virtual prototyping routine in **Fig. 6.5** it becomes evident that global variables are computationally expensive as the waveform synthesis and component design must be repeated for each global iteration. Therefore, in order to reduce the optimization problem complexity, only a carefully selected subset of the category (i) variables are independently iterated whereas the remaining category (i) variables are transformed into dependent variables which are chosen as a function of the independent variables. Note that this approach has already been applied in Section 5.5.

Independent Variables

The switching frequency f_{sw} and the current ripple $\Delta I^{\text{pp}}_{L,\text{max}}$ in main inductances, i.e. L_{dc} and L_{dm1} have by far the most significant impact on the waveforms and thus on the overall system performance amongst the above listed category (i) global design variables. Therefore, these quantities are selected to be the independent global system design variables $\vec{\Pi}_{\text{glo}}$ with,

$$\vec{\Pi}^{\text{2LPWM}}_{\text{glo}} = \vec{\Pi}^{\text{3LPWM}}_{\text{glo}} = (f_{\text{sw}}, \Delta I^{\text{pp}}_{L,\text{max}})^\top \,, \tag{6.18}$$

$$\vec{\Pi}^{\text{2LTCM}}_{\text{glo}} = (f_{\text{sw,min}}, k_{f_{\text{sw}}})^\top \,. \tag{6.19}$$

For the PWM topologies, L_{dc} and L_{dm1} are thus chosen as a function of f_{sw} and the maximum peak-to-peak current ripple $\Delta I^{\text{pp}}_{L,\text{max}}$,

$$L_{\mathrm{dc}}^{\mathrm{2LPWM}} = \frac{1}{f_{\mathrm{sw}}} \cdot \left(1 - \frac{V_{\mathrm{mpp,min}}}{V_{\mathrm{dc,min}}}\right) \cdot \frac{V_{\mathrm{mpp,min}}}{\Delta I_{L,\mathrm{max}}^{\mathrm{pp}}} \,, \tag{6.20}$$

$$L_{\mathrm{dc}}^{\mathrm{3LPWM}} = \frac{1}{2f_{\mathrm{sw}}} \cdot \left(1 - \frac{V_{\mathrm{mpp,min}}}{V_{\mathrm{dc,min}}}\right) \cdot \frac{V_{\mathrm{mpp,min}}}{\Delta I_{L,\mathrm{max}}^{\mathrm{pp}}} \,, \tag{6.21}$$

$$L_{\mathrm{dm1}}^{\mathrm{2LPWM}} = \frac{1}{2\sqrt{3}f_{\mathrm{sw}}} \cdot \frac{\hat{V}_{\mathrm{g,nom}}}{\Delta I_{L,\mathrm{max}}^{\mathrm{pp}}} \,, \tag{6.22}$$

$$L_{\mathrm{dm1}}^{\mathrm{3LPWM}} = \frac{4\sqrt{3} - \frac{V_{\mathrm{mpp,max}}}{\hat{V}_{\mathrm{g,nom}}} - 9\frac{\hat{V}_{\mathrm{g,nom}}}{V_{\mathrm{mpp,max}}}}{6f_{\mathrm{sw}}} \cdot \frac{\hat{V}_{\mathrm{g,nom}}}{\Delta I_{L,\mathrm{max}}^{\mathrm{pp}}} \,. \tag{6.23}$$

For the 2LTCM, the switching frequency is variable. Hence, L_{dc} and L_{dm1} are chosen as a function of the permissible switching frequency range $f_{\mathrm{sw}} \in f_{\mathrm{sw,min}} \cdot [1, k_{f_{\mathrm{sw}}}]$. The values of L_{dc} and L_{dm1} can be found using (6.2) and (6.4) and searching for the worst case conditions of the involved voltages, the power level and the displacement factor.

The virtual prototyping routine is carried out for the following intervals of the global design variables,

$$\vec{\Pi}_{\mathrm{glo}}^{\mathrm{2LPWM}} : f_{\mathrm{sw}} \in [12, 72]\,\mathrm{kHz}, \qquad \Delta I_{L,\mathrm{max}}^{\mathrm{pp}} \in [5, 60]\,\% \,, \tag{6.24}$$

$$\vec{\Pi}_{\mathrm{glo}}^{\mathrm{3LPWM}} : f_{\mathrm{sw}} \in [6, 36]\,\mathrm{kHz}, \qquad \Delta I_{L,\mathrm{max}}^{\mathrm{pp}} \in [5, 60]\,\% \,, \tag{6.25}$$

$$\vec{\Pi}_{\mathrm{glo}}^{\mathrm{2LTCM}} : f_{\mathrm{sw,min}} \in [12, 84]\,\mathrm{kHz}, \qquad k_{f_{\mathrm{sw}}} \in [4, 12] \,, \tag{6.26}$$

where the intervals are sampled at 10 to 16 equally distributed discrete values.

Dependent Variables

The remaining category (i) global design variables apart from the switching frequency and the current ripple in the main inductors are the DC capacitor values and the EMI filter values.

Stable DC voltages V_{mpp} and V_{dc} with low voltage ripples in C_{mpp} and C_{dc} guarantee non-distorted current waveforms in the DC/DC and DC/AC converter stages, low measurement noise and thus sufficient control stability and robustness. Furthermore, low voltage ripples in C_{dc} improve the tracker efficiency of the solar generator MPP. Therefore, low values for the peak-to-peak voltage ripples $\Delta V_{C,\mathrm{max}}^{\mathrm{pp}}$ are defined as a design constraint (cf. **Tab. 6.6**) which define the minimum capacitance values. Consequently, a negligible impact of C_{mpp} and C_{dc} on

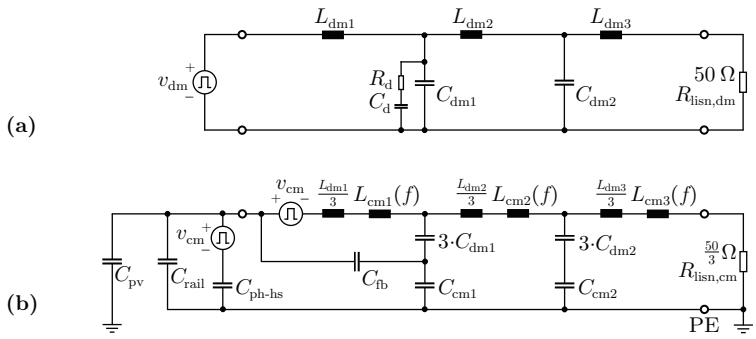


Fig. 6.6: Equivalent circuits for the EMI filter design. **(a)** Equivalent DM filter circuit with connected line impedance stabilization network (LISN) between filter and mains. According to the inner structure of the LISN, the connection to the mains can be neglected for EMI-relevant frequencies greater than 150 kHz. **(b)** Equivalent CM filter circuit. An additional CM noise path exists through the parasitic ground capacitance C_{pv} of the solar generator. Note that the Vitroperm-based CM inductance values are non-linear with frequency. The equivalent CM core loss resistances (not shown) usually provide enough damping to prevent oscillations whereas the DM filter needs additional damping (R_d and C_d).

Tab. 6.7: Employed constants and constraints for the filter design.

Considered EMI emission limits		CISPR B
DM & CM attenuation margin	A_{margin}	6 dB(µV)
Max. filter resonance frequency	$f_{res,max}$ / f_{fsw} [1)]	0.8
Max. react. power consumption	Q_{filt} / P_r	8.75 %
Max. voltage ripple in C_{dm1}	$\Delta V^{pp}_{C_{dm1},max}$	13 V
Mains grid impedance range	$[L_{g,min}, L_{g,max}]$	[0,50] µH
Min. 1st stage CM inductance	$L_{cm1}(f_{sw})$ / L_{dm1}	3
Max. HF current in C_{pv} (rms)	I_{pv} [2)]	100 mA
CM capacitor values	$C_{cm\{1,2\}}$	44 nF
Capacitance range of C_{pv}	$[C_{pv,min}, C_{pv,max}]$	[0,1.6] µF
2LPWM parasitic capacitances	$\{C^{2LPWM}_{rail}, C^{2LPWM}_{ph\text{-}hs}\}$	{288,173} pF
3LPWM parasitic capacitances	$\{C^{3LPWM}_{rail}, C^{3LPWM}_{ph\text{-}hs}\}$	{533,345} pF
2LTCM parasitic capacitances	$\{C^{2LTCM}_{rail}, C^{2LTCM}_{ph\text{-}hs}\}$	{575,345} pF

[1)] $f_{res,max}$ / $f_{sw,min}$ for the 2LTCM [2)] evaluated without LISN

the waveforms can be assumed. Thereby, the DC capacitances C_{mpp} and C_{dc} are converted into dependent global design variables.

The remaining global design variables define the EMI filter characteristics. As a complete and independent iteration would translate into a very high computational effort, these design variables are as well converted into dependent variables and thus chosen as a function of the selected global design variables $\vec{\Pi}_{\mathrm{glo}}$. Since no systematic sweep is performed, the challenge here resides in the identification of those values which lead to optimal or at least close-to-optimal filter component designs. The design procedure to determine the EMI filter values is largely based on the methods and considerations presented in [170, 180–183]. As shown in **Fig. 6.5**, the first step of the filter design is the identification of the worst case required filter attenuations A_{dm} and A_{cm}, respectively to comply with the CISPR B EMI limits [184]. In a next step, the DM filter values are determined according to the following procedure:

(i) Choose i^{th} vector of design variables, i.e. $L_{\mathrm{dm2},i} = L_{\mathrm{dm3},i}$, $C_{\mathrm{dm1},i}$ and $C_{\mathrm{dm2},i}$,

(ii) Calculate $C_{\mathrm{d},i}$ and $R_{\mathrm{d},i}$ to prevent oscillations in the filter using the methods presented in [185],

(iii) Check for compliance with the CISPR B EMI limits and all filter resonance frequencies below f_{sw},

(iv) In case of compliance, calculate the filter performance by means of the cost function $\mathcal{G}_{\mathrm{dm}}$, and

(v) Sweep all permissible combinations of design variables.

The underlying equivalent circuit for the DM filter design is shown in **Fig. 6.6(a)**. The cost function $\mathcal{G}_{\mathrm{dm}}$ is designed so as to minimize the total energy in the inductors whereas the maximum reactive power consumption of the filter is limited to 8.75 % of the rated power at nominal operation. The subsequent CM filter design follows a similar procedure:

(i) Choose i^{th} vector of design variables, i.e. $L_{\mathrm{cm1},i}$, $L_{\mathrm{cm2},i} = L_{\mathrm{cm3},i}$ and $C_{\mathrm{fb},i}$,

(ii) Check for compliance with the CISPR B EMI limits, all filter resonance frequencies below f_{sw} and HF rms current through the parasitic capacitor C_{pv} of the solar generator $< 100\,\mathrm{mA}$ [173],

(iii) In case of compliance calculate the filter performance by means of the cost function $\mathcal{G}_{\mathrm{cm}}$, and

(iv) Sweep all permissible combinations of design variables.

The underlying equivalent circuit for the CM filter design is shown in **Fig. 6.6(b)** which was derived based on the considerations in [181]. The cost function $\mathcal{G}_{\mathrm{cm}}$ selects the design with the lowest total flux in the CM inductors. Apart from the employed cost functions $\mathcal{G}_{\mathrm{dm}}$ and $\mathcal{G}_{\mathrm{cm}}$, further metaheuristics are utilized in the CM filter design: the minimum first stage CM inductance value is set to $L_{\mathrm{cm1}} \geq 3 \cdot L_{\mathrm{dm1}}$ as found to be optimal in [182]. This choice implies a high attenuation of the unwanted HF CM currents in the first filter stage and a minimal CM filtering by means of the DM inductors L_{dm1}. The capacitors C_{cm1} and C_{cm2} are always set to the maximum permissible value of 44 nF stated in [186]. The parasitic solar generator capacitance to earth is assumed to be in the range of $C_{\mathrm{pv}} \in [0, 1.6]$ µF [171]. The stray capacitances C_{rail} and $C_{\mathrm{ph\text{-}hs}}$ are largely determined by the number and capacitances of the semiconductor packages to the heat sink [181] and are in the range of a few hundred picofarads. **Tab. 6.7** summarizes the constants and constraints employed in the filter design routines.

6.6 Performance Space Analysis

After the selection of the components (Section 6.3), the derivation of suitable models (Section 6.4) and the design of a tractable optimization routine (Section 6.5), the η^{*}_{euro}-ρ_{box}-σ_{P} Pareto-optimal designs $\mathcal{D}_{\mathrm{PV}}$ were calculated for each of the considered converter concepts separately. The complexity of the optimization problem at hand is $\mathcal{O}(n^{46})$: 43 component variables and the 2 global design variables $\vec{\Pi}_{\mathrm{glo}}$ as listed in Section 6.5 and the selection of the concept. The execution of the virtual prototyping routine yields approximately 150 000 Pareto-optimal designs for each topology. These numbers are significantly higher than in the previous case study on the DC/DC converter optimization. This is mainly a result of the higher number of components which exponentially increases the complexity of the problem. Despite the large numbers, standard computational means are sufficient. The solution to the optimization problem was found by means of a workstation equipped with 2×2.4 GHz Intel XEON quad-core CPUs and 64 GB of RAM within 15

to 20 hours. The results of the optimization are shown in **Fig. 6.7**, **Fig. 6.8**, **Fig. 6.9** and **Fig. 6.10**.

6.6.1 Core Materials

Fig. 6.7 and **Fig. 6.8** show the calculated Pareto fronts of the 2LTCM, 2LPWM and 3LPWM converter concepts. The most remarkable feature of **Fig. 6.7** is the division of the 3LPWM Pareto-optimal designs into two distinct clusters which cannot be observed in the other Pareto fronts. A deeper analysis reveals that the two 3LPWM Pareto clusters are formed by either amorphous iron- or ferrite-based designs whereas the other Pareto fronts exclusively contain ferrite-based designs. A more detailed illustration of the core material distribution in the Pareto fronts is depicted in **Fig. 6.8**.

When focusing on the 3LPWM Pareto fronts, it is found that the amorphous iron designs are predominantly obtained for low current ripples $\Delta I_{L,\mathrm{max}}^{\mathrm{pp}} \approx 10 - 15\,\%$ where the core excitations and thus the core losses are low. In contrast, the ferrite-based designs are only competitive at high current ripples for which lower inductance values must be employed. There, lower costs can be achieved with ferrite despite still larger volumes when compared to amorphous iron. This can be reasoned as follows:

- The considered ferrite N87 cores are significantly cheaper than the considered amorphous iron 2605SA1 cores as evident from **Tab. 6.4**.
- The offset costs for coil formers, connectors and corresponding labor are lower for the ferrite E-cores.
- The impact of the more expensive litz wire in the ferrite designs is partially offset by the use of E-cores. The volume distribution between core and winding of typical E-core geometries is clearly dominated by the core volume. This saves expensive litz wire and, moreover, relaxes the problem of the low maximum permissible flux density of ferrite.

The situation is different with the 2LTCM and 2LPWM. Here, the ferrite-based designs do not only achieve lower costs and losses, but also lower volumes than amorphous iron-based designs. Therefore, ferrite is in any case dominant over amorphous iron.

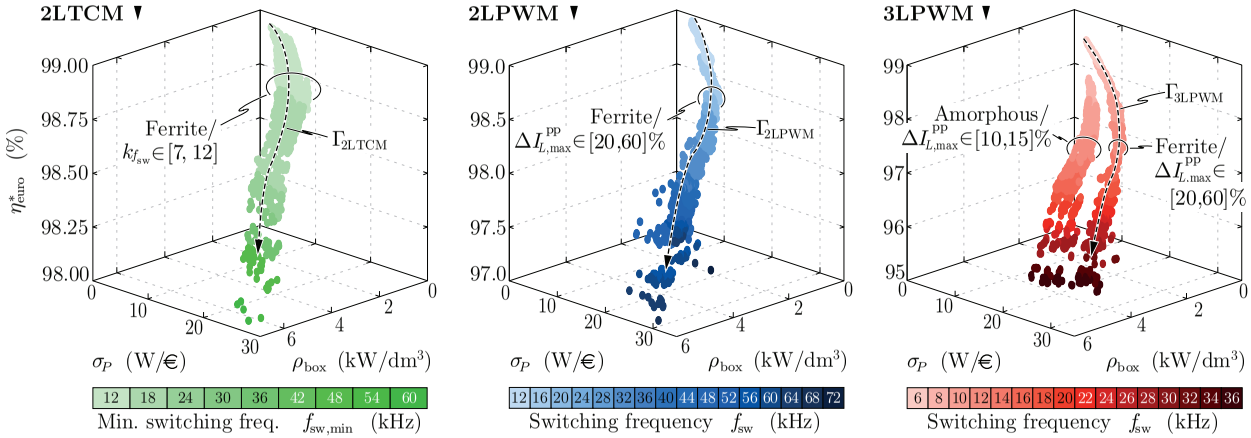


Fig. 6.7: η^*_{euro}-ρ_{box}-σ_P Pareto fronts of the investigated 2LTCM, 2LPWM and 3LPWM concepts. For the 2LTCM, no Pareto-optimal designs could be found above $f_{\text{fsw,min}} > 60\,\text{kHz}$. In contrast, Pareto-optimal designs could be found within the entire 2LPWM and 3LPWM frequency ranges (cf. (6.24), (6.25) and (6.26)). The extended Pareto front of the 3LPWM when compared to the 2LTCM and 2LPWM is due to the fact that Pareto-optimal designs result for both considered core materials. The two distinct clusters consisting of either ferrite or amorphous iron designs are clearly visible. The component loss, volume and cost breakdown of **Fig. 6.9** is done for the designs along the depicted trajectories Γ_x shown in this figure.

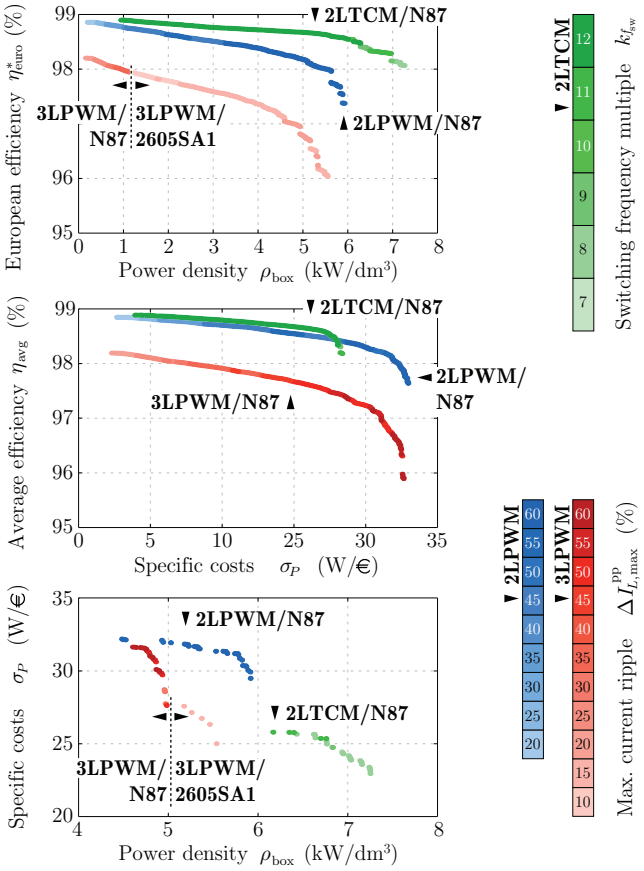


Fig. 6.8: 2D projections of the Pareto fronts shown in **Fig. 6.7**. The 2LTCM and 2LPWM Pareto fronts are exclusively composed of ferrite-based designs, whereas for the 3LPWM both ferrite and amorphous iron result in dominant designs. The amorphous iron designs are predominantly obtained for low current ripples $\Delta I^{\text{pp}}_{L,\text{max}} \approx 10 - 15\,\%$ where the core excitations and thus the core losses are low. In contrast, ferrite is only competitive at high current ripples where lower inductance values are required. The 3LPWM amorphous iron designs are generally more compact but more expensive and lossier than their ferrite counterparts. The trade-off possibilities depicted by the ρ_{box}-σ_P Pareto front mainly result from the selection of different core materials (only 3LPWM), more expensive litz wires with lower strand diameters allowing for smaller magnetics, and heat sinks with reduced volume but a higher number of more expensive fans.

For the 2LTCM it could be expected that the amorphous iron-based main inductors would not generate any dominant designs due to the extreme HF core excitation as a result of the operating principle. On the other hand, the dominance of ferrite solutions in the 2LPWM concept could not be anticipated. Inspection of the calculations shows that due to the inherently larger HF excitation of the 2LPWM when compared to the 3LPWM, core losses are already significant at low ripples. Therefore, low core losses become more important than high flux densities. Consequently, ferrite does not only offer a higher efficiency and lower costs, but also smaller volumes in the 2LPWM irrespective of the current ripple.

6.6.2 Comparison of Topologies

The achievable performance of the three considered systems with respect to efficiency, power density and specific costs is analyzed and compared in this section. The Pareto analysis of the three obtained Pareto fronts, i.e. the identification of the overall Pareto-optimal designs amongst the 2LTCM, 2LPWM and 3LPWM Pareto-optimal designs $\mathcal{D}_{\mathrm{PV}}^{\mathrm{2LTCM}}$, $\mathcal{D}_{\mathrm{PV}}^{\mathrm{2LPWM}}$ and $\mathcal{D}_{\mathrm{PV}}^{\mathrm{3LPWM}}$ shown in **Fig. 6.7**, reveals that the SiC-based concepts 2LTCM and 2LPWM dominate the Si-based 3LPWM concept. This means that in the overall Pareto front, no 3LPWM designs can be found, i.e.

$$\begin{aligned} & \bigcup \mathcal{D}_{\mathrm{PV}}^{\mathrm{3LPWM}} \cap \bigcup \mathcal{D}_{\mathrm{PV}}^{\mathrm{2LTCM+2LPWM+3LPWM}} \equiv \varnothing \\ \Longleftrightarrow \qquad & \bigcup \mathcal{D}_{\mathrm{PV}}^{\mathrm{Si}} \cap \bigcup \mathcal{D}_{\mathrm{PV}}^{\mathrm{Si+SiC}} \equiv \varnothing \,, \end{aligned} \tag{6.27}$$

and thus that SiC allows for more efficient, smaller and lower cost designs. This is also confirmed by the 2D projections of the individual Pareto fronts depicted in **Fig. 6.8**. The identification of the underlying reasons is demanding as it requires the comparison of a very large number of Pareto-optimal designs of each concept with each other. In order to facilitate the discussion of this analysis which is presented below, the component loss, volume and cost shares of selected 2LTCM, 2LPWM and 3LPWM designs are shown in **Fig. 6.9**. The connection of these designs form the trajectories Γ_{2LTCM}, Γ_{2LPMW} and Γ_{3LPWM} on the respective Pareto fronts depicted in **Fig. 6.7**. Each trajectory starts at highly efficient designs at low switching frequencies and stop at high frequencies where designs with low costs and volumes can be found.

In order to enhance the comparability, for the 3LPWM, a trajectory has been chosen which is exclusively comprised of ferrite-based designs. Note that the exact paths of the trajectories are not chosen systematically. In fact, they are made up of representative designs which give a general impression of the characteristics of each concept.

Losses

Inspection of the Pareto fronts and in particular the selected designs in **Fig. 6.9** with respect to the losses, it can be found that, although to a different degree, the semiconductor losses are dominating in all systems. The 2LTCM features the lowest semiconductor losses which increase only marginally with the switching frequency. This is a direct consequence of the modulation scheme which enables complete ZVS in all operating points. On the other hand, however, the magnetics and especially the DC capacitor losses are higher than for the 2LPWM and 3LPWM as a result of the HF high-ripple-current operation. For the DC capacitors this is despite the interleaving of two TCM branches. Due to the high weighting of part-load operation in the European efficiency (6.17), constant losses have a non-negligible impact on the system efficiency. The 2LTCM is clearly most affected by this type of losses as the HF operation of a comparably high number of switches causes high gate driver losses.

Fig. 6.10 shows an in-depth analysis of the weighted (according to (6.17)) relative semiconductor conduction and switching losses. In order to improve the comparability, the depicted losses were calculated for a cooling system which occurs in the Pareto-optimal designs of all three concepts. Whereas increasing switching frequencies (2LTCM: minimum switching frequency) have the same qualitative effect in all systems, namely the increase of the total losses, the influence of the second global design variable is clearly more complex. A wider permissible switching frequency range $f_{\mathrm{sw,min}} \cdot [1, k_{f_{\mathrm{sw}}}]$ in the 2LTCM concept by means of a higher multiple $k_{f_{\mathrm{sw}}}$ considerably reduces the conduction losses $\overline{P}_{\mathrm{c,tot}}$ at low to medium minimum switching frequencies $f_{\mathrm{sw,min}}$. This can be reasoned with the lower required reverse currents I_{min} and $i_{\mathrm{min}}(t)$ in the case of higher permissible switching frequency ranges. These currents are utilized to limit the upper bound of the switching frequency range but represent purely reactive currents which do not contribute to the power transfer (cf. Section 6.2). Contrarily, at high $f_{\mathrm{sw,min}}$ a high multiple $k_{f_{\mathrm{sw}}}$ has the opposite effect and leads to higher $\overline{P}_{\mathrm{c,tot}}$. This is due

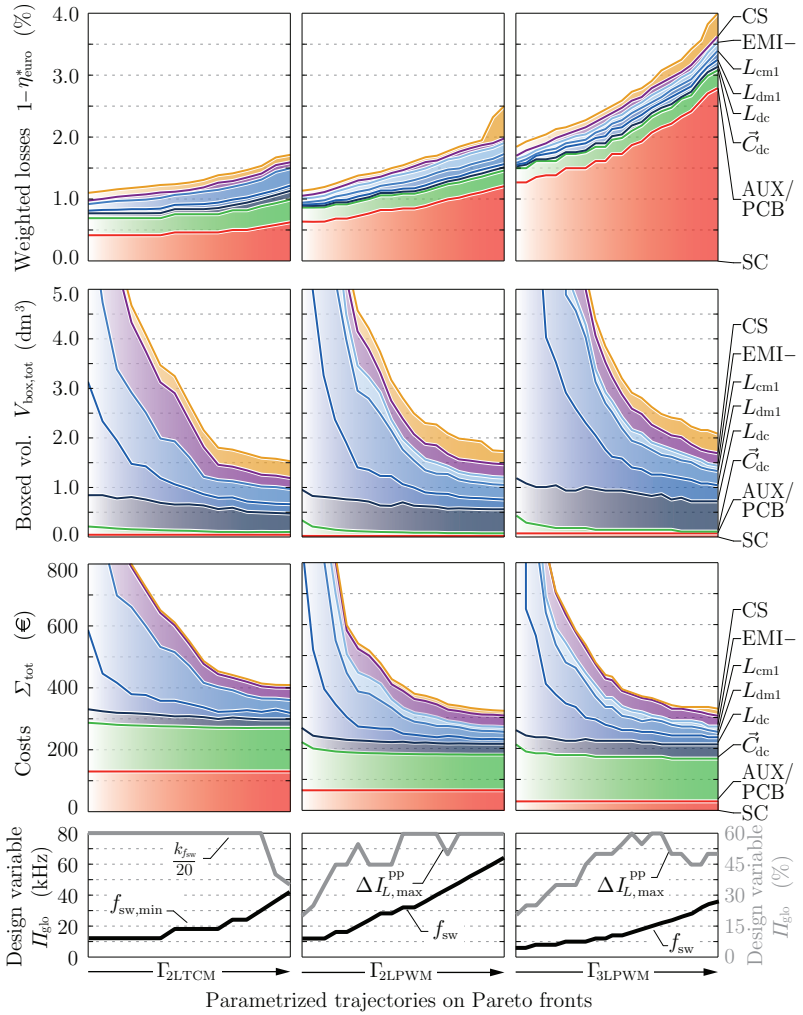


Fig. 6.9: Component loss, volume and cost breakdown of the designs along the parametrized trajectories on the Pareto fronts depicted in **Fig. 6.7**. $\vec{C}_{\text{dc}}$ summarizes C_{mpp} and C_{dc} whereas $EMI-$ denotes the filter components without L_{dm1} and L_{cm1}. It is furthermore shown how the global design variables $\vec{\Pi}_{\text{glo}}$ evolve along the chosen trajectories. For the purpose of presentation, the switching frequency multiple $k_{f_{\text{sw}}}$ has been scaled (e.g. $k_{f_{\text{sw}}}/20 = 60\,\% \Leftrightarrow k_{f_{\text{sw}}} = 12$).

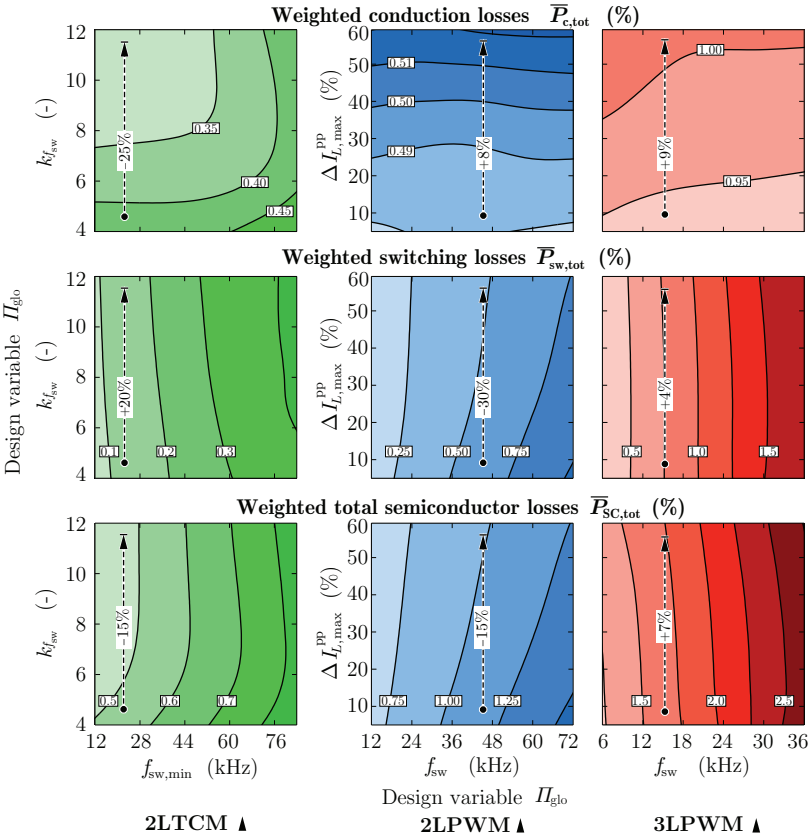


Fig. 6.10: Weighted power semiconductor losses as a function of the global design variables $\vec{\Pi}_{glo}$. The weighting was performed according to (6.17). In order to improve the comparability, the depicted losses were calculated for a cooling system which occurs in the Pareto-optimal designs of all three concepts. For both the 2LPWM and 3LPWM, elevated current ripples entail higher rms currents and thus higher conduction losses. The main difference between the SiC MOSFET-based 2LPWM and the Si IGBT-based 3LPWM can be observed with respect to the switching losses. Whereas higher current ripples facilitate more frequent ZVS transitions (predominantly at part-load operation) in the 2LPWM, the 3LPWM IGBT switching losses are almost invariant to the current ripple. The latter is mainly due to the fact that the IGBT turn-off tail currents prohibit effective soft-switching.

to the employed load-shedding scheme: at high switching frequencies and thus high corresponding switching losses, one out of the two TCM branches is also disabled at medium power levels instead of only at low power levels. This control scheme helps to reduce the switching and gate driver losses but comes at the cost of higher conduction losses as only one parallel branch remains.

Considering the 2LPWM and 3LPWM concepts, increasing the ripple currents $\Delta I_{L,\max}^{\mathrm{pp}}$ leads to higher conduction losses. The reason for this effect is twofold:

(i) On the one hand, the rms values of the boost and inverter stage currents increase, and

(ii) On the other hand, high current ripples imply low inductances L_{dm1} in the first filter stage. As a result, a higher capacitance must be employed to meet the filter design criteria (EMI and resonance). Due to the higher reactive power consumption of the filter, higher conduction losses occur which is particularly noticeable at part load.

Contrary to the similar effect regarding the conduction losses, elevated current ripples $\Delta I_{L,\max}^{\mathrm{pp}}$ have an opposite effect on the switching losses $\overline{P}_{\mathrm{sw,tot}}$ when comparing the 2LPWM and 3LPWM. Considering the 2LPWM, the SiC MOSFETs partly operate with ZVS despite the employed PWM control scheme. ZVS may occur at low load and/or in the vicinity of the zero-crossings of the fundamental currents in the DC/AC inverter output phases. In such situations, the low fundamental and comparably high superimposed ripple currents resemble the current waveforms which are intentionally generated with TCM modulation (cf. Section 6.2). It becomes evident that elevated $\Delta I_{L,\max}^{\mathrm{pp}}$ allow for more frequent ZVS transitions also at higher loads and at further distances from the zero-crossings of the fundamental current. Therefore, the operation of the 2LPWM at high $\Delta I_{L,\max}^{\mathrm{pp}}$ is desirable as it allows for considerably reduced switching losses which overcompensate the increased conduction losses. Obviously, the gain is higher at higher f_{sw}. The identified benefit is in strong contrast to the situation of the 3LPWM. **Fig. 6.10** shows switching losses which are largely invariant from $\Delta I_{L,\max}^{\mathrm{pp}}$. This can mainly be reasoned with the fundamental difference between IGBTs and MOSFETs: whereas MOSFETs benefit from waveforms that allow for ZVS by means of greatly reduced switching losses (up to a factor of 10, cf. **Fig. 3.4**), IGBTs suffer from

the turn-off tail currents which prohibit effective soft-switching, i.e. the IGBT switching loss reduction under ZVS operation is much lower (less than a factor of 2, cf. **Fig. 3.3** and [90]). Another reason lies in the different ripple distribution over the fundamental period in the DC/AC inverter stages of the 2LPWM and 3LPWM: for nominal operation, i.e. largely active power feed-in with a displacement factor of $\cos(\phi) \approx 1$, the largest current ripples occur in the vicinity of the zero-crossings of the fundamental current in case of the 2LPWM. Contrarily, in case of the 3LPWM, the current ripples are very small at these phase angles of the fundamental current and occur further apart from the zero-crossings (cf. **Fig. 6.2**). Therefore, the 2LPWM benefits considerably more from increased current ripples as they occur at the advantageous phase angles of the fundamental current (i.e. in the vicinity of the zero-crossings) where they immediately allow for more frequent ZVS transitions.

Finally, after the analysis of the semiconductor loss data of **Fig. 6.10** with respect to the different global design variables, also the absolute numbers shall be discussed here. The lower switching losses of the SiC-based 2LTCM and 2LPWM when compared to the Si-based 3LPWM can be explained with the systematic ZVS operation (2LTCM) and the much lower switching loss energies (2LPWM) of SiC MOSFETs which are a factor 5 to 10 lower when compared to the employed Si IGBTs (cf. Section 3.1). The considered SiC systems not only achieve lower switching but also considerably lower conduction losses. The 2LPWM achieves $\approx 0.5\,\%$ lower weighted conduction losses mainly due to the weighting of part-load operation where the ohmic MOSFET behavior is clearly superior over the IGBT output characteristic with its inherent constant forward voltage drop. At full load, the 2LPWM and 3LPWM achieve a similar conduction loss efficiency. Although the 2LTCM features twice the chip area, the weighted conduction losses are not half when compared to the 2LPWM. This is partly because of the employed load-shedding scheme which disables one out of the two TCM branches at low loads and already at medium loads in case of high f_{sw}, as discussed above. The main reason for increased conduction losses, however, resides in the principle of TCM operation which relies on triangular current waveforms. At the same power level, such triangular currents increase the rms current by approximately $15\,\%$ ($\approx 30\,\%$ higher $\overline{P}_{\mathrm{c,tot}}$) when compared to (low-ripple) PWM current waveforms.

Volume

The analysis of the volumes of the designs in **Fig. 6.9** and of the Pareto-optimal designs of **Fig. 6.7** in general shows that achieving very high efficiencies entails the drawback of very large volumes of the passives. When comparing the three considered concepts it can be found that the 2LTCM generally achieves the lowest volumes of the passives. Remarkably, this also includes the DC-link capacitor C_{dc}: although the 2LTCM modulation scheme causes the highest losses in the DC-link capacitor at nominal operation, an in-depth analysis shows that due to the interleaving the smallest worst case rms current (which defines the capacitor volume) of all topologies can be attained. In contrast to the 2LTCM and 2LPWM, the DC-link capacitor of the 3LPWM is capacitance-constrained rather than current-constrained. The unavoidable presence of LF currents flowing into the DC-link midpoint asks for a large capacitance in order to limit the midpoint voltage variation. Despite the advantageous DC/DC converter topology and the carefully chosen strategies in the modulation scheme (cf. Section 6.2) which relax this problem, the largest DC-link of all topologies results.

An inherent feature of TCM modulation is the low inductance value requirement. As a result, the total volume of the DC/DC boost inductors L_{dc} is generally the smallest of all systems. Likewise, the total volume of the 2LTCM main AC inductors L_{dm1} is smaller than the combined volume of the first stage DM and CM inductors L_{dm1} and L_{cm1}, respectively, of the 2LPWM and 3LPWM. However, the minimum achievable 2LTCM inductor volume decreases only slowly with increasing frequency and even tends to increase at very high switching frequencies. Therefore, the optimal switching frequency range becomes narrower towards the end, i.e. for increasing switching frequencies, of the investigated 2LTCM trajectory in **Fig. 6.9**. Furthermore, beyond $f_{\mathrm{sw,min}} = 60\,\mathrm{kHz}$, no Pareto-optimal designs can be found anymore as the inductors do not shrink any further. This observation has already been made in the first case study (see Section 5.6) and also in [80]. There it is found that high HF core and winding losses, which are predominant in the 2LTCM inductors, complicate the volume reduction by increasing the frequency. Other core materials and/or multi-gap inductors might allow to overcome this limitation. In contrast, the HF core and winding losses are rather small in the 2LPWM and 3LPWM inductors when compared to the LF winding losses. This enables continuously decreasing inductor volumes up to much higher frequencies

than investigated. As a consequence, more Pareto-optimal designs, i.e. designs with smaller total boxed volumes, can be expected for these topologies beyond the investigated frequency range, provided that the smaller magnetics are not compensated by the growing cooling system volume.

Costs

Finally, again with reference to **Fig. 6.9**, the systems are analyzed and compared regarding the component costs. The highest component costs generally result for the 2LTCM. This is mainly due to the high number of expensive SiC switches and gate drivers which dominate the total costs and which cannot be compensated by the lower costs of the passives. Despite twice the number of semiconductors, the 3LPWM Si IGBT and diode costs are only half when compared to the SiC costs of the 2LPWM. However, the savings on the semiconductors are almost compensated by the increased costs for gate driver units. Consequently, it can be concluded that with today's SiC costs using Si technology in a 3-level topology does not offer a real cost advantage. Apart from the semiconductor gate drivers, the cost structures of the 2LPWM and 3LPWM are similar: employing a two- to threefold higher switching frequency enables similar costs of the passives in the 2LPWM as in the 3LPWM.

In **Fig. 6.9**, the components summarized by $EMI-$ include all EMI filter-related components except for the main first-stage inductors L_{dm1} and L_{cm1}. When neglecting very low switching frequencies where the depicted designs on the investigated trajectory are Pareto-optimal mainly due to the exceptional efficiency rather than because of low costs, it can be found that the EMI filter components cause similar costs irrespective of the concept. This can be reasoned as follows:

- The 2LPWM generally requires more attenuation for EMI compliance than the 3LPWM due to the 2-level operation combined with higher switching frequencies. On the other hand, however, the selection of the filter components for the 3LPWM is governed by the filter resonance criterion which requires all resonance frequencies to be sufficiently lower than the switching frequency in order to avoid resonances (cf. Section 6.5). Due to the low switching frequencies of the 3LPWM, relatively large filter components result which entail similar costs as the 2LTCM and 2LPWM.

- The filter design of the 2LTCM is dictated by the EMI compliance criterion. Due to the interleaved operation in conjunction with a variable switching frequency which yields a blurred spectrum with a multitude of low amplitude harmonics, only marginally higher filter attenuations are required. Furthermore, as the critical frequencies $f_{\mathrm{crit,dm}}$ and $f_{\mathrm{crit,dm}}$ at which the highest attenuation is required are usually high, the filter effort and resulting costs are in the same range as for the 2LPWM and 3LPWM.

- The EMI filter design routines aim at minimizing the stored energy or flux in the inductors (cf. Section 6.5). As a consequence of this approach, the filter designs tend to employ more capacitance rather than inductance. As capacitance is inexpensive and causes only low losses, existing differences in the EMI filters of the three concepts can predominantly be observed in the volume whereas the differences with respect to the costs and efficiency are rather low.

6.7 LCC Mission Cost Space Analysis

The analysis of the Pareto fronts in the last section revealed the differences between the three considered concepts with respect to the efficiency, power density and the specific costs. Since all concepts exhibit certain strengths and weaknesses regarding the three performance measures (e.g. 2LTCM: efficient but expensive), determining the best concept and/or particular design solely based on the Pareto fronts is not possible. As proposed in the introduction of this thesis (cf. Chapter 1), it is therefore advised to perform a post-processing in which the identified Pareto surfaces in the performance space are mapped into a 1D mission cost space as depicted in **Fig. 6.11**. The employed mapping function $\mathcal{C} : (\eta, \rho, \sigma) \mapsto \mathbb{R}$ can be interpreted as a weighting, linking and merging of the performance measures in the performance space into a single key figure. The best design can then easily be determined in a straightforward manner by evaluating and comparing this single key figure rather than three different performance measures. The mission cost function can arbitrarily be chosen and may only reflect the (subjective) preferences of the design engineer.

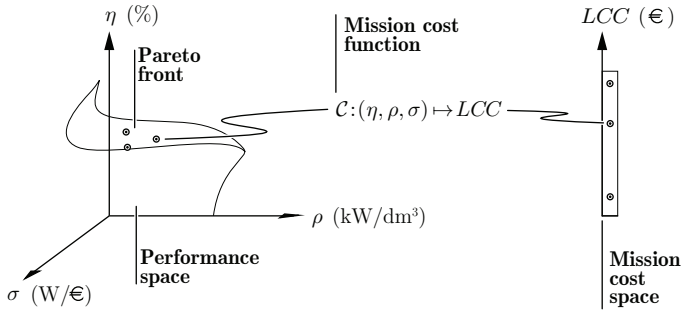


Fig. 6.11: Detail of the proposed MOO-based virtual prototyping routine as presented in Chapter 1. In order to facilitate the selection of a candidate system from the Pareto front, a mapping of the Pareto front in the performance space into the 1D mission cost space is proposed. There, the designs can be efficiently compared based on a single key figure rather than various performance measures. In this work, the utilized mission cost function $\mathcal{C}$ evaluates the life cycle costs LCC of the PV system designs based on a net present value (NPV) analysis.

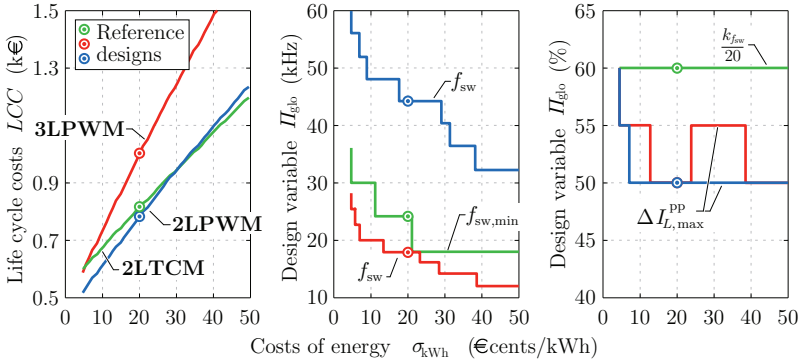


Fig. 6.12: Mission cost space analysis of the Pareto-optimal PV system designs based on life cycle mission cost considerations. The figures depict the maximum achievable LCC evaluated with (6.28) for varying costs of energy. Furthermore, the global design variables of the corresponding optimal designs are shown. For the selected reference costs of energy of $\sigma_{\mathrm{kWh}} = 0.2\,{}^{€}/_{\mathrm{kWh}}$, the 2LPWM attains the lowest LCC at $\vec{\Pi}_{\mathrm{glo}} = (44\,\mathrm{kHz}, 50\,\%)$. Whereas the 3LPWM is not competitive irrespective of σ_{kWh}, the 2LTCM achieves lower LCC in case of very high costs of energy as a result of the unsurpassed efficiency.

6.7.1 Mission Cost Function

In this case study, the identified Pareto-optimal PV systems are evaluated and assessed based on an approximation of the life cycle costs (LCC). A simple approach which incorporates a net present value analysis (NPV) is proposed,

$$LCC = \Sigma_{\text{tot}} + \sum_{n=1}^{N_{\text{life}}} \left\{ \Sigma_{\text{cap}}(q) + \Sigma_{\text{rev}}(\eta^*_{\text{euro}}) \right\} \cdot \frac{1}{(1+q)^n} \,. \tag{6.28}$$

In (6.28), q denotes the interest rate and N_{life} the number of years, i.e. the considered lifetime. The LCC is composed of the following cost contributions:

- *Initial costs*: the initial costs of all converter components Σ_{tot},
- *Capital costs*: the interests on the initially invested capital, i.e.

$$\Sigma_{\text{cap}}(q) = q \cdot \Sigma_{\text{tot}} \,, \tag{6.29}$$

  and
- *Lost operating revenue costs*: the missed operating revenue, i.e. the value of the energy which is lost in the energy conversion of the PV system and which can thus not be fed into the grid,

$$\Sigma_{\text{rev}}(\eta^*_{\text{euro}}) = \sigma_{\text{kWh}} \cdot E_{\text{loss}} \cdot (1 - \eta^*_{\text{euro}}) \tag{6.30}$$

$$= \sigma_{\text{kWh}} \cdot P_{\text{r}} \cdot CF \cdot \frac{8760\,\text{h/year}}{1000} \cdot (1 - \eta^*_{\text{euro}}) \,, \tag{6.31}$$

  with σ_{kWh} being the costs of energy per kWh and CF the capacity factor. The capacity factor is the ratio of the actual generated energy over a period of time to the potential energy generation if it were possible to operate the solar generator at rated power continuously over the same period of time.

Clearly, a more comprehensive estimation of the LCC could also take into account manufacturing or housing costs. Furthermore, the effect of the inverter reliability on the LCC may be modeled by means of repair and downtime costs. However, the calculation of these costs would require the derivation of a large set of additional models and assumptions which is beyond the scope of this work.

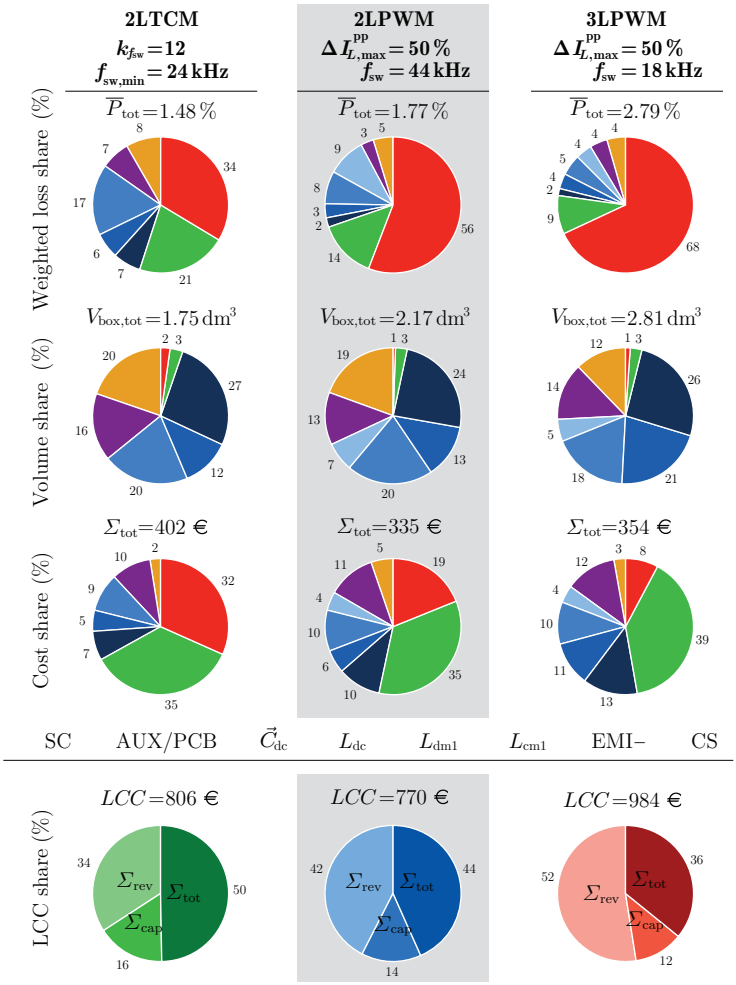


Fig. 6.13: Analysis of the power loss, volume, cost and LCC shares of the selected candidate designs depicted in **Fig. 6.12**. The typical characteristics of the three considered concepts are reflected by the different types of cost shares which make up the LCC: the 2LTCM features a low contribution of the lost operating revenue costs towards the LCC which is a direct result of the high efficiency of this concept. The LCC of the 3LPWM is dominated by the lost operating revenue costs due to the lowest efficiency. Finally, the 2LPWM features balanced LCC shares and the lowest total LCC which renders this solution the most attractive for the investigated residential PV application.

6.7.2 Comparison

Amongst the available parameters in (6.28), the cost of energy σ_{kWh} is clearly the most influential and therefore kept variable for the moment. Reasonable assumptions for the remaining parameters are,

$$CF = 0.13\,, \qquad q = 5\,\%/_{\mathrm{year}}\,, \qquad N_{\mathrm{life}} = 10\,\mathrm{years}\,. \tag{6.32}$$

The above values for the capacity factor and the interest rate are typical for private residential PV systems in Central Europe. The considered lifetime was chosen based on standard warranties of large PV converter manufacturers (usually 5 to 10 years) and the mean time between failure (MTBF) rates of PV inverters in the field as reported in [187]. Lastly, it was found that moderate variations of up to $\approx \pm 50\,\%$ of the parameters in (6.32) do not change the general findings of this study.

Fig. 6.12 shows the calculated LCC of the Pareto-optimal 2LTCM, 2LPWM and 3LPWM designs. It can be seen that based on the selected cost function (6.28) and parameters (6.32), the 2LPWM represents the most attractive concept achieving the lowest LCC over a wide range of energy costs. Only at high energy costs of $\sigma_{\mathrm{kWh}} \gtrapprox 0.32\,€/_{\mathrm{kWh}}$ the 2LTCM becomes superior over the 2LPWM as a result of its unsurpassed efficiency which helps to minimize the costs of lost operating revenue Σ_{rev}. If very low energy costs of $\sigma_{\mathrm{kWh}} \approx 0.05\,€/_{\mathrm{kWh}}$ apply, the high initial costs of the 2LTCM render the concept the least attractive. Such energy costs typically apply to industry. There, usually higher interest/discount rates of $q \approx 12\,\%/_{\mathrm{year}}$ are employed in the NPV calculation to adjust for risk, opportunity cost and or other factors. Such higher rates q even more pronounce the importance of low initial costs. As the 2LPWM features the lowest attainable initial costs, this concept appears to be the best solution in either a residential or industrial application.

In a final step, the candidate designs for each concept are chosen assuming $\sigma_{\mathrm{kWh}} = 0.20\,€/_{\mathrm{kWh}}$. This number roughly averages the feed-in tariffs ($\sigma_{\mathrm{kWh}} = 0.13\,€/_{\mathrm{kWh}}$) and the remuneration for own consumption of the generated electricity ($\sigma_{\mathrm{kWh}} = 0.30\,€/_{\mathrm{kWh}}$) as applicable for residential PV system in Germany at the beginning of 2016. The details of the selected candidate systems are shown in **Fig. 6.13**. The proposed 2LTCM candidate design operates within a switching frequency range of $f_{\mathrm{sw}} \in [24, 288]\,\mathrm{kHz}$, the 2LPWM candidate system operates at $44\,\mathrm{kHz}/50\,\%$ current ripple and the 3LPWM candidate system at $18\,\mathrm{kHz}/50\,\%$ current ripple. It is found that the 2LPWM achieves 22 %

lower LCC than the benchmark 3LPWM system and 5 % lower LCC than the 2LTCM system.

6.7.3 Proposed Candidate Design

Based on the above analysis, it can be concluded that the 2LPWM design with $f_{\mathrm{sw}} = 44\,\mathrm{kHz} \,/\, \Delta I_{L,\mathrm{max}}^{\mathrm{pp}} = 50\,\%$ as shown in **Fig. 6.13** represents the most attractive solution for the investigated PV converter application of **Fig. 6.1**. Besides featuring a 22 % / 5 % lower LCC than the competitor systems, a range of other facts underline the attractiveness of the proposed solution: the selected 2LPWM candidate design offers the lowest initial costs (i.e. the component costs, cf. **Fig. 6.13**) and hence features the lowest costs already at the beginning of the considered lifetime. From an investment perspective, this is favorable as (in theory) it involves no uncertainty. Furthermore, the 2LPWM candidate system features by far the lowest complexity in terms of component count (semiconductors, gate drivers, passive components) and control effort (standard modulation scheme, no DC-link midpoint balancing, no current zero-crossing detection). This does not only facilitate a presumably higher reliability but also allows for better general performance measures such as low development and manufacturing costs and a short time to market.

6.8 Summary

This chapter presents a systematic optimization and comparison of three different converter systems for a residential 10 kW DC/AC PV application. The set of considered systems includes i) a state-of-the-art hard-switched PWM-modulated all-Si IGBT concept employing a 3-level T-type topology (3LPWM) ii) a hard-switched PWM-modulated all-SiC MOSFET concept employing a conventional 2-level topology (2LPWM) and iii) a soft-switched TCM-modulated all-SiC MOSFET concept employing a double-interleaved 2-level topology (2LTCM). The analysis includes the EMI filter and takes into account the relevant regulations which apply to PV converter systems, e.g. concerning LVRT and permissible ground leakage currents. Based on the detailed and experimentally verified multi-physics and cost models of Chapter 3 and Chapter 4, the concepts are optimized with respect to the efficiency, volume and the component costs. The obtained η_{avg}-ρ_{box}-σ_{P} Pareto fronts show

a clear superiority of the SiC-based concepts regarding the power density and the efficiency which is mainly a result of the higher semiconductor performance. The achievable total component costs of the 2LPWM lie in a similar range as the 3LPWM whereas the 2LTCM component costs are significantly higher due to the same number of gate drivers and switches as the 3LPWM. A subsequent combined LCC/NPV analysis of the obtained Pareto-optimal PV converter designs assuming a lifetime of 10 years and energy costs of $\sigma_{\mathrm{kWh}} = 0.2\,€/\mathrm{kWh}$ underlines the attractiveness of the 2LPWM solution. Under the made assumptions, the 2LPWM operated at 44 kHz switching frequency and 50 % current ripple achieves 22 % lower LCC than the benchmark 3LPWM system and 5 % lower LCC than the 2LTCM system.

6.8.1 Findings

Superiority of SiC 2LPWM

The presented analysis identifies the found SiC 2LPWM design to be the most attractive solution for the considered residential PV application. The main technical reasons for the superiority of the found solution are summarized and discussed below:

- The chip utilization and the symmetry of the semiconductor stresses in the 2-level topology is unsurpassed, i.e. this topology attains a maximum performance benefit with a minimum number of expensive SiC MOSFET switches.
- The ohmic output characteristic of MOSFETs allows for much lower conduction losses in part-load operation than bipolar IGBTs. Therefore, SiC MOSFETs prove to be a very good match for PV applications where part-load efficiency is highly important.
- The virtual prototyping routine identified the operation at high current ripples to be optimal. The underlying reason is twofold: not only do high current ripples enable more frequent ZVS transitions and thus considerably increased part-load efficiencies of the 2LPWM, but also do high ripples allow for the use of inexpensive and highly efficient ferrite inductors instead of costly and lossier amorphous iron cores.

It can be concluded that the combination of the 2LPWM topology, operation at high ripple currents and the stressed part load-operation

of the PV application at hand allow to concurrently exploit the unique benefits of SiC, i.e. the low part- load conduction losses, the excellent soft-switching capabilities and the very competitive and robust hard-switching performance.

Potential of the 2LTCM System

The 2LTCM remains an interesting concept if unsurpassed efficiency and power density are required which are beyond the fundamental limits of the other investigated concepts. In addition, the 2LTCM offers a high potential for further improvements:

- *Innovative HF magnetics*: a main limitation of the 2LTCM is found to be the HF losses in the magnetics. The reasons are similar as already found in the first case study (cf. Chapter 5): the combination of low required inductance values, limited maximum permissible air gap lengths and a dominant share of the HF core and winding losses (with respect to the LF winding losses) complicate the reduction of the inductor volume by means of increased frequencies. Here, the consideration of lower loss core materials which possibly feature a low permeability and/or the utilization of multiple-air-gap core geometries may help to overcome these limitations and further improve the 2LTCM performance.
- *Chip area distribution*: the switch and the diode worst case losses in the DC/DC converter stage of the 2LPWM and 3LPWM are similar. The worst case operating point is at the lowest MPP voltage where the highest currents result. There, the switch usually shows lower conduction losses (duty cycle $D = 1 - \frac{450\,\mathrm{V}}{650\,\mathrm{V}} \approx 0.7$) but higher switching losses than the commutating diode. These worst case losses, however, are imbalanced in case of the 2LTCM as the switching losses are small because of ZVS (cf. **Fig. 6.4**). Therefore, the losses and corresponding cooling effort of the 2LTCM DC/DC converter stage could be lowered if an adjusted chip area distribution were employed.
- *Load-shedding scheme*: the load-shedding scheme could be further enhanced with respect to the DC/AC converter stage: similarly to low-load operation, one out of the two TCM branches could also be turned off at medium and full load in the vicinity of the zero-crossings of the fundamental current [188]. This means that

the decision on whether to operate one or two TCM branches could be taken dynamically during the entire fundamental period and not only depending on the operating point.

Finally, a rough estimation based on **Fig. 6.10** and **Fig. 6.13** suggests that the higher number of SiC MOSFETs is probably better spent on realizing the 2LTCM concept rather than on increasing the chip area of the 2LPWM switches by means of paralleling. The additional semiconductor costs of $8 \cdot 8 = 64$ € virtually equalize the total component costs (399 € vs. 402 €, cf. **Fig. 6.13**). As evident from **Fig. 6.10**, the conduction losses could be decreased by approximately 0.25 % of rated power whereas the switching losses are expected to increase due to a higher amounts of stored energy which are lost during hard-switched transitions. In sum, the 2LPWM employing the same number of switches as the 2LTCM could not achieve the same efficiency whereas the achievable volume would remain 24 % higher. Finally, it must be noted, that in any case the 2LPWM would still keep the advantage of a lower complexity and a presumably higher reliability.

Switching Frequencies

The corresponding switching frequencies of the proposed SiC candidate systems are $f_{\mathrm{sw}} \in [24, 288]$ kHz for the soft-switched 2LTCM concept and $f_{\mathrm{sw}} = 44$ kHz for the hard-switched 2LPWM. At first glance and with reference to literature on the application of WBG semiconductors, these switching frequencies might seem to be rather low. However, the 44 kHz of the 2LPWM are equivalent to a fivefold increase of the switching frequency when compared to the 3LPWM (a factor of 2.5 higher switching frequency and a factor of 2 because of 2-level instead 3-level operation). Furthermore, publications stating high switching frequencies often exclusively maximize the power density which naturally results in high switching frequencies (at the cost of low efficiencies, e.g. [72, 160]). Regarding the 2LTCM, the variable switching frequency is strongly dependent on the operating conditions. Whereas the minimum frequency of 24 kHz only applies in case of adverse voltages and full load, the switching frequency at nominal operation typically varies between 100 and 250 kHz which is another increase of a factor of 3 to 5 with respect to the 2LPWM system. Even higher switching frequencies are unattractive mainly because of the poor scaling of the magnetics.

6.8.2 Conclusions

Several main conclusions can be drawn from the presented study:

- The proposed advanced MOO-based virtual prototyping routine facilitates a highly comprehensive investigation and clarification of the potential of SiC in PV. It can be shown that SiC can concurrently improve the efficiency and power density at similar or lower costs than state-of-the-art Si-based systems. The demonstrated detail of the virtual prototyping-based investigations is to the author's knowledge unprecedented in literature and is clearly not feasible by means of hardware prototyping.
- The calculated system costs, efficiency and switching frequency of the benchmark 3LPWM system seem reasonable and realistic when compared to commercial systems. E.g. the 10 kW 3-level system in [166] features a European efficiency of 97.6 % employing SiC diodes and a switching frequency of 16 kHz (candidate all-Si 3LPWM system: 97.2 % at 18 kHz). Retailer prices are about 2000 € of which typically 20 % is component costs, i.e. ≈400 € (3LPWM: 353 € without housing). These findings and the fact that only experimentally verified models are employed support confidence level regarding the calculations in this study.
- It could be demonstrated that the proposed virtual prototyping routine and the corresponding software can handle a highly complex optimization problem involving 46 design variables with standard computational means and within reasonable time.

7 Conclusion and Outlook

DURING the past century, power electronics has been an enabling technology contributing to unprecedented productivity and wealth. Further and steady improvements of the performance of power electronic converter systems represent a key requirement to open up new fields of application, to overcome the challenge of clean energy generation and to guarantee a continuous growth of economy. Besides innovation and the employment of disruptive technologies, system optimization is a main enabler of improved performance. In this context, the methodology of virtual prototyping was identified to be a powerful tool for systematic optimizations of the converter systems' primary performance measures, i.e. the efficiency, volume, weight, component costs and the reliability. Concurrently, virtual prototyping enables the improvement of general performance measures such as lowering the development costs or the time to market. The trade-offs between the performance measures which are an inherent attribute of power electronic converter systems ask for a multi-objective optimization approach rather than a single-valued optimization in the virtual prototyping routine. In particular, it was found that a concurrent improvement of the efficiency and power density is often feasible by means of more expensive materials and components. Consequently, the consideration of the component costs apart from the losses, weight and the volume was found to be imperative in order to substantially increase the significance of the results of the virtual prototyping routine.

Motivated by the previous discussion, this thesis proposed an advanced virtual prototyping routine allowing for comprehensive and systematic multi-objective optimizations and comparisons of almost arbitrary power electronic converter systems regarding the efficiency, vol-

ume, weight and the costs. This was achieved by means of mapping the set of possible system designs, i.e. the design space, into the performance space where the Pareto-optimal designs could be identified and analyzed in detail. A subsequent mapping of the Pareto-front into a 1D mission cost space utilizing a user-defined mission cost function was proposed which facilitated the identification of a candidate system based on a single key figure. The virtual prototyping routine implemented an intelligent direct search method utilizing termination conditions and optimized software code for the guaranteed and deterministic identification of the globally optimal designs. Furthermore, suitable simplifications of the optimization problem based on the negligence of weak coupling effects were proposed to considerably reduce the problem complexity. A detailed and comprehensive multi-physics and cost modeling framework was established which allowed to compute and assess the losses, volume, weight and the costs of the converter components. The modeling framework was complemented with models allowing for the description of the operating point-dependent converter behavior and waveforms in the system. The emphasis in the model derivation was put on accuracy. As a consequence, a wide range of crucial model parameters such as the switching loss energies and the losses of magnetic core materials were determined by means of extensive multi-parametric measurements. Furthermore, the majority of models was experimentally verified.

The virtual prototyping routine was employed in the framework of two case studies. In a first example, four different Si and SiC concepts of a bidirectional galvanically isolated universal power conditioner with ultra-wide input voltage range were analyzed and compared for a 5 kW residential DC microgrid application. The main purpose of the investigations was the identification of the optimal concept and to check the potential of SiC semiconductors regarding the implementation of a highly functional converter system while achieving a high efficiency and low volume at competitive costs. The second example was dealing with the investigation of the potential of SiC in a residential 10 kW DC/AC PV application. For this purpose, a state-of-the-art Si IGBT-based concept and two SiC MOSFET-based concepts were optimized with respect to the efficiency, volume and the component costs and subsequently compared based on the achievable minimum life cycle costs.

7.1 Concluding Remarks: Virtual Prototyping Routine

The conclusions regarding the proposed and implemented advanced multi-objective optimization-based virtual prototyping routine are listed below.

- *Handling of complex problems*: the presented work demonstrates that the software implementation of the proposed virtual prototyping routine and its intelligent direct search method can handle complex multi-objective optimization problems. It requires only standard computational means and finds the solutions within reasonable time. Examples featuring nearly 50 independent design variables resulting in a very large number of design options are demonstrated to be tractable.
- *High accuracy*: the majority of the employed reluctance models, loss models and thermal models is experimentally verified where the measurements show high accuracies with mean deviations of typically less than 10 % at small standard deviations. The high achieved modeling accuracy is further confirmed by the implemented DC/DC DAB prototype ($\eta_{\max} = 98.5\,\%$, $\rho_{\mathrm{sys,tot}} = 1.8\,\mathrm{kW/dm^3}$, $\sigma_P = 18.5\,\mathrm{W/€}$, $f_{\mathrm{sw}} = 48\,\mathrm{kHz}$) where the loss modeling features a mean deviation of 2.5 % and a maximum deviation below 7 %. These findings suggest that the results of the proposed virtual prototyping routine and the underlying modeling framework can be trusted with high confidence.
- *Unprecedented detail*: the vast amount of detailed data and results generated by the employed virtual prototyping routine enables unprecedented insight into the optimization problems. The data facilitate a highly comprehensive investigation of the optimal/non-optimal solutions as well as the identification of fundamental performance limitations.
- *Practicability*: the usefulness and practical relevance of the proposed approach is underlined by the fact that to a wide extent only available components (semiconductors, cooling systems, passives) rather than abstract components have been considered. This facilitates a straightforward implementation of an arbitrary candidate system without the need for extensive additional design considerations.

7.2 Concluding Remarks: Case Studies

The conclusions regarding the case studies dealing with the multi-objective optimization of DC/DC and DC/AC converter systems are listed below.

- *Necessity of comprehensive approach*: the case studies demonstrate that the potential of SiC can only be assessed if the analysis concurrently considers the losses, volume and the component costs and if the analysis is performed on the system level rather than on the component level. Additional mission cost considerations such as life cycle cost considerations further facilitate a comprehensive analysis and a fair comparison to Si. Single-valued optimizations or 1:1 replacements of Si semiconductors are insufficient and prohibit the revealing of the full potential of SiC.
- *Superiority of simple topology with SiC (I)*: the case study on bidirectional galvanically isolated DC/DC converters with ultra-wide input voltage range identifies the conventional 3LDAB concept with SiC MOSFETs to be superior over the SiC MOSFET-based 5LDAB concept. The 3LDAB does not only feature lower losses, volume and costs but also represents the simpler system with a presumably higher reliability. The analysis further shows that the high functionality in combination with the achieved efficiency, power density and costs cannot be achieved by conventional Si IGBTs or Si MOSFETs. Hence, this application represents a so-called *killer application* for SiC.
- *Superiority of simple topology with SiC (II)*: the case study on DC/AC PV converter systems identifies the conventional hard-switched PWM-modulated SiC 2LPWM concept to be the most attractive concept. The comprehensive comparison between the selected SiC 2LPWM candidate system ($\eta^*_{\text{euro}} = 98.2\,\%$, $\rho_{\text{box}} = 4.6\,\text{kW/dm}^3$, $\sigma_P = 29.9\,\text{W/€}$, $f_{\text{sw}} = 44\,\text{kHz}$) and the state-of-the art Si 3LPWM candidate system ($\eta^*_{\text{euro}} = 97.2\,\%$, $\rho_{\text{box}} = 3.6\,\text{kW/dm}^3$, $\sigma_P = 28.2\,\text{W/€}$, $f_{\text{sw}} = 18\,\text{kHz}$) reveals a 22 % decrease of the life cycle costs (lifetime of 10 years) achieved by the SiC 2LPWM concept. As in the DC/DC case study, the simplest and thus presumably most reliable system is superior.
- *Identified performance barriers*: both studies revealed the necessity of intensified research towards low-loss HF magnetic com-

ponents and towards improved semiconductor packaging/cooling concepts to reduce the parasitic capacitances between the packages and the heat sink. Both technologies are a prerequisite for unconstrained HF ZVS-operated converter systems enabling high power densities at high efficiencies.

7.3 Outlook

7.3.1 SiC Transistors

In the framework of this thesis it could be shown that with today's available SiC transistors it is possible to implement more efficient, more compact and simpler power electronic converter systems at the same or even lower costs than with Si transistors. The lower costs result from system-level considerations where the higher SiC costs can be compensated by lower costs for passives and electronics (mainly gate drivers; due to simpler topologies). When extending the analysis to life cycle costs, the cost advantage is further emphasized due to lower energy costs as a result of the higher achievable efficiencies.

Despite the promising findings in this work, yet a number of challenges remain which impede the short-term and widespread use of SiC in commercial products. As exemplified in the two case studies, the performance of SiC can only be fully exploited if different topologies and switching frequencies are employed than with Si. For a company with an established Si-based system, this entails a complete redesign. Such a redesign does not only imply additional development costs but also the adaption of the manufacturing lines and the negotiation of new contracts with suppliers due to the altered converter BOM. The sum of required efforts to switch from Si to SiC might therefore not be justified by the performance advantages and particularly only moderate cost advantages offered by SiC. It is therefore estimated that in order to replace Si in existing designs and applications, a clearer cost advantage, i.e. mainly lower costs of SiC are required. A further cost reduction can, however, be expected owing to economy of scale effects and larger wafers in the manufacturing process [189, 190]. Other often stated issues regarding SiC transistors are the reliability and the availability of a second (supplier) source. Whereas the number of manufacturers of market-ready SiC switches and in particular SiC MOSFETs is gradually increasing (2016: Wolfspeed, Rohm, General Electric, ST, Microsemi,

Mitsubishi and others) the manufacturers at the same time claim that the reliability issues have largely been solved. Based on field data and accelerated stress tests, [189–191] have determined similar or better FIT rates than for state-of-the-art Si counterparts. At lower voltages around 600-1200 V it is estimated that in the long term, SiC will be challenged by GaN-based semiconductors [192]. GaN features even better material properties than SiC (higher critical electrical field strength, higher electron mobility and lower specific capacitances) and is therefore inherently better suited for power semiconductors than SiC. However, as of beginning of 2016, only engineering samples of GaN HEMTs are available whereas SiC MOSFETs are much more mature and widely commercialized.

In contrast to the above discussed challenges, SiC also features large potentials for future performance improvements. The development of trench gate UMOSFETs is expected to cut the specific on-state resistances by half [193] when compared to the vertical SiC DMOSFET technology as considered in this thesis. This can be achieved by the increased gate width of the trench gate structure which counteracts the low channel electron mobility of SiC. The lower contribution of the channel towards the overall on-state resistance renders SiC MOSFETs attractive already at lower voltages, i.e. in 600 V applications where nowadays traditional Si SJ MOSFETs and IGBTs are predominantly employed. The SiC material properties further allow for higher junction temperatures than Si which is already partly exploited by the 200 °C rated MOSFETs presented in [194]. Finally, the commercialization of more advanced packages which allow for lower parasitics and thus lower switching losses as well as the introduction of higher voltage rated transistors can be expected in the near future [195].

7.3.2 Further Potentials of MOO

So far, the proposed MOO-based virtual prototyping routine has mainly been used for the purpose of identifying and investigating the optimal designs for a given application with predefined specifications. More analysis could be performed regarding the sensitivity of the obtained results regarding various aspects and quantities. A sensitivity analysis with respect to varying system specifications could generate more insight into how an optimized system must be designed. Thereby, simple general design rules might be derived. Furthermore, a sensitivity

analysis towards the modeling uncertainty could be carried out. This could help to gain a deeper understanding of which modeling aspects are essential to obtain accurate results and which models have only a weak influence. Based on this information, the employed models can specifically be refined.

The presented methodology of virtual prototyping could be further expanded. Clearly, the multi-objective optimization could be carried out regarding additional performance measures. An obvious choice is the converter/component reliability. The reliability data is, however, extremely involved to obtain by means of own measurements and the chances of obtaining the required data from the respective manufacturers are very limited. Therefore, this particular expansion of the methodology seems to be challenging in the near future. A more promising potential which can be implemented more easily resides in the post-processing of the Pareto front data. Whereas in this thesis an LCC evaluation of the Pareto front was proposed to select the most attractive candidate system, more sophisticated post-processing steps are possible. For example, since the Pareto front in this thesis is identified regarding the sum of boxed component volumes rather than the overall resulting converter volume, a layout mapping could be introduced which identifies those Pareto-optimal designs whose components match well and allow for a low overall system volume.

Another substantial and immediate opportunity for improvement resides in the software implementation of the routine itself. Although intelligent search algorithms are already in place, the computational efficiency of the underlying code could be greatly enhanced. Standardized sub-routines which are executed thousandfold may be translated from MATLAB code into MATLAB-embedded C code. Depending on the type of task, 10 to 1000 times lower computational times are estimated to be achievable. The big advantage of speeding up the sub-routines is the fact that more complex optimization problems can be handled. Especially the increase of the number of computationally expensive global design variables (in contrast to the component-related design variables) could open up a new dimension of enhanced detail.

The main limitation of the presented virtual prototyping routine is given by the comparably small database of materials and components. In order to allow for more general, more comprehensive studies or even a commercialization of the implemented tool, the database is required to be significantly extended. Such an effort would mainly entail more

switching loss and core loss measurements as well as intensified empirical research to collect more cost data and to keep the present cost database up to date.

Finally, the case study on DC/DC converters revealed a significant potential for improvements regarding the implemented 3LDAB hardware prototype. In fact, a concurrent reduction of the volume by 50 % and of the component costs by 25 % at the same efficiency was predicted. It is thus both desirable and of high interest to implement such an improved system in order to verify the predicted performance of the virtual prototyping routine.

Nomenclature

Abbreviations

2D	Two Dimensional
3D	Three Dimensional
AC	Alternating Current
Al	Aluminum
AUX	Auxiliary
CAD	Computer-Aided Design
CM	Common Mode
CS	Cooling System
DC	Direct Current
DM	Differential Mode
DOI	Digital Object Identifier
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FEM	Finite Element Method
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GD	Gate Driver
HB	Half Bridge
HEMT	High-Electron-Mobility Transistor
HF	High Frequency
HV	High Voltage
IGBT	Insulated-Gate Bipolar Transistor
IPT	Inductive Power Transfer
IT	Information Technology
LCC	Life Cycle Costs
LF	Low Frequency
LISN	Line Impedance Stabilization Network
LV	Low Voltage
LVRT	Low-Voltage Ride-Through
MOO	Multi-Objective Optimization
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor

MOQ	Minimum Order Quantity
MPP	Maximum Power Point
MTBF	Mean Time Between Failure
NPV	Net Present Value
PCB	Printed Circuit Board
PFC	Power Factor Correction
PP	Polypropylene
PWM	Pulse-Width Modulation
SC	Semiconductor
Si	Silicon
SiC	Silicon Carbide
ZCS	Zero Current Switching
iZVS	Incomplete Zero Voltage Switching
ZVS	Zero Voltage Switching

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