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Modular High Bandwidth Switch-Mode Three-Phase AC Voltage Source

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Pour ma famille tant aimée

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Contents

Kurzfassung

Die Entwicklung von vielseitig einsetzbaren, geregelten AC Spannungsquellen (ACS) mit einer hohen Bandbreite wurde in den letzten Jahren von der Industrie vorangetrieben, um kostengünstiger und effizienter leistungselektronische Geräte auszulegen und zu testen. Der mögliche Anwendungsbereich einer derartigen ACS ist überaus breit und es wird daher ein Gerät verlangt, das eine hohe Flexibilität in der Anbindung möglicher Lasten oder Generatoren bietet und das hohe Anforderungen an die Qualität sowie die dynamischen Eigenschaften der Ausgangsspannung erfüllt. Die Auslegung der ACS unterscheidet sich gerade durch die erhöhte Flexibilität und die einschränkenden Vorgaben von der Anwendung diverser Methoden, die in unterschiedlichen wissenschaftlichen Veröffentlichungen vorgeschlagen werden. Obgleich bis heute schon verschiedene ACS als Produkte auf dem Markt erhältlich sind, wurde die Auslegung wie auch die Optimierung der Regelung eines solchen leistungselektronischen Konvertersytems nur teilweise oder gar nicht in der Literatur behandelt.

In dieser Arbeit wird eine dreiphasige, geschaltete ACS mit einer Leistung von 100 kW untersucht, die einen Vierquadrantenbetrieb ermöglicht und gleichzeitig eine hohe Effizienz, ein kleines Bauvolumen, eine sehr hohe Bandbreite der Ausgangsspannung als auch einen sehr kleinen Ausgangsspannungsrippel erzielt. Um eine Leistung von 100 kW zu erreichen, werden zehn Module mit je einer Leistung von 10 kW parallel zueinander geschaltet. Jedes Modul weist eine AC–DC–AC Konverterstruktur auf, die aus einer dreiphasigen AC–DC Gleichrichter-Eingangsstufe, einem DC Spannungszwischenkreis mit geteilten Kondensatoren und einer vierphasigen Wechselrichter-Ausgangsstufe besteht.

In einem ersten Schritt werden zielübergreifende Konzepte zur Auslegung, Optimierung und Regelung der Eingangs- sowie Ausgangsstufe einer 10 kW-Einheit entworfen und auf das betrachtete System angewandt. Besonders im Mittelpunkt stehen dabei die Begründung, dass jede Ausgangsphase individuell betrieben wird, die daraus folgende Auslegung des zweistufigen, für jede Phase getrennt vorgesehenen Ausgangsfilters und der Ausgangsspannungsregelstruktur wie auch die Auslegung des dreiphasigen EMV Eingangsfilters. Allen Auslegungsroutinen liegt dabei eine Mehrkriterien-Optimierung zugrunde. Messungen, welche auf einem dreiphasigen, dreistufigen T-Typ Konverter-Prototypen mit SiC MOSFETs der neusten Generation durchgeführt wurden, unterstützen

vollumfänglich die detaillierten theoretischen Untersuchungen. In einem zweiten Schritt werden die Eingangs- und die Ausgangsstufe elektrisch miteinander verbunden. Diesbezüglich werden umfassende Lösungen erarbeitet, die eine gleiche Spannungsaufteilung über den beiden Zwischenkreiskondensatoren erzwingen und die einen Erdstrom, im Falle der Erdung von Netz- und Laststernpunkt, verhindern. Ein Master-Slave Regelungskonzept, das den Betrieb mehrerer parallel-geschalteter ACS Modulen erlaubt, wird zum Schluss hergeleitet. Das Konzept wird anhand von zwei parallelen Einheiten und mit Hilfe exakter Schaltungssimulation untersucht.

Die wesentlichen neuen wissenschaftlichen Beiträge dieser Doktorarbeit sind:

- Individueller Betrieb jeder Phase der vierphasigen Ausgangsstufe mit einem zweistufigen Ausgangsfilter, das durch minimale Interaktion der Phasen gekennzeichnet ist (vgl. Abschnitt 3.1);
- Erarbeitung eines Mehrkriterien-Auslegungsalgorithmus für das individuell für jede Ausgangsphase vorgesehene zweistufige *LC* Ausgangsfilter, der auf das Design Space Konzept zurückgreift, mit Hilfe dessen mehrere Kriterien gleichzeitig berücksichtigt werden können (vgl. Abschnitt 3.2);
- Entwicklung einer Mehrkriterien-Optimierungsroutine für die Auslegung der Regelstruktur der Ausgangsspannung, mit der eine Ausgangsspannungs-Kleinsignalbandbreit von 7.1 kHz–15.5 kHz in Abhängigkeit der Last erreicht wird (vgl. Abschnitt 3.3);
- Bestimmung des optimalen Verhältnisses zwischen CM und DM Induktivität der Haupt DM / CM *LC* Stufe des EMV Eingangsfilters um das geringste Filtervolumen dieser Stufe zu erhalten (vgl. Abschnitt 3.5);
- Detaillierte Analyse ob der Kühlkörper an Erde oder den DC Mittelpunkt angebunden werde sollte, um die CM Störaussendung zufolge parasitärer Koppelkapazitäten der Leistungshalbleiter zu verringern (vgl. Abschnitt 3.5.1);
- Beweis, dass eine gleiche Spannungsaufteilung über den geteilten Zwischenkreiskondensatoren mit der vierten Phase nicht für alle

betrachteten Lastfälle und Betriebsbedingungen, unter Berücksichtigung der ACS's Spezifikationen, erreicht werden kann (vgl. Abschnitt 4.1.2);

- Regelungstechnische Unterdrückung eines Erdstromes für einen Netzsternpunkt und eine Last, welche beide mit Erde verbunden sind (vgl. Abschnitt 4.2);
- Einbindung der galvanischen Trennung und der Fähigkeit, eine gleiche Spannungsaufteilung über den geteilten Zwischenkreiskondensatoren zu erreichen, in einen einzelnen DC–DC Konverter (vgl. Abschnitt 4.3); und
- Entwicklung eines Master-Slave Konzeptes für die Regelung parallel geschalteter Module mit individuellen einphasigen Ausgangsspannungsregelstrukturen, die nicht auf den Brückenzweigausgangsstrom oder den Ausgangsstrom zurückgreifen (vgl. Abschnitt 5.1).

Abstract

In recent years, the development of general purpose, high bandwidth controllable AC voltage sources (CVSes) is pushed by industry to accelerate the design and / or testing processes of power electronics equipment in order to save costs and efforts. As the term "general purpose" suggests, the potential application area of such a CVS is vast and hence demands for a device which is highly flexible regarding the connection of possible loads or generators and features stringent specifications related to quality and dynamic properties of the output voltage. It is precisely the great flexibility and the increased requirements which make the design of the CVS to be different from standard approaches found in diverse scientific publications. To this day, even though CVS products are already available in the market, the design of such a converter system as well as the optimization of its control have not or only partially been covered in literature.

In this Ph.D. thesis, a 100 kW four-quadrant, three-phase, switch-mode CVS is researched and designed to achieve a high efficiency, a low construction volume, a very high output voltage control bandwidth, and a very low output voltage ripple. The CVS is realized by connecting ten 10 kW modules in parallel, each of the modules being implemented as an AC–DC–AC converter, consisting of a three-phase AC–DC rectifier input stage, a split DC link with an intermediate voltage circuit, and a three-phase four-leg DC–AC inverter output stage.

First, key multi-objective concepts to design, optimize, and control the output and input stages of one 10 kW unit are developed and applied to the system at hand. This especially comprises the motivation to operate each output phase individually, and subsequently the design of the output filter provided individually for each phase and of the output voltage control structure, and in a next step the three-phase EMI input filter design. All design routines are thereby based on multi-objective optimizations. The detailed analyses are fully supported by experimental results carried out on a three-phase three-level T-type converter prototype employing the newest generation of SiC MOSFETs. Second, the input and output stages are electrically interconnected and comprehensive solutions to balance the voltages of the split DC link and to eliminate a ground current for simultaneously grounded mains star-point and load are elaborated. Finally, a Master-Slave control concept is derived to operate multiple parallel connected CVS modules. The concept is investigated by accurate circuit simulations on the basis of

two paralleled units.

The major new scientific contributions of this Ph.D. thesis are:

- individual operation of each leg for the three-phase four-leg output stage with a four-line filter with minimum interaction between the lines (cf. Section 3.1);
- elaboration of a multi-objective design algorithm for a per-phase, multi-stage *LC* output filter based on the design space concept, which simultaneously considers multiple criteria (cf. Section 3.2);
- development of a multi-objective optimization routine to lay out the output voltage control structure, helping to achieve an output voltage small-signal control bandwidth of 7.1 kHz–15.5 kHz, depending on the type of load (cf. Section 3.3);
- determination of the optimal ratio between CM and DM inductances of the main DM / CM *LC* stage of the EMI input filter to obtain the smallest volume of this filter stage (cf. Section 3.5);
- detailed discussion weather the heat sink should be connected to ground or to the DC midpoint in order to achieve a higher CM attenuation of the EMI input filter (cf. Section 3.5.1);
- demonstration that the balancing of the split DC link voltages by the fourth output leg is not possible for all considered load types and operating conditions, with regard to the given CVS' specifications (cf. Section 4.1.2);
- elimination of a ground current for a mains star-point and load connected to earth by means of control (cf. Section 4.2);
- integration of the DC link voltage balancing capability and galvanic isolation into a single DC–DC converter (cf. Section 4.3); and
- development of a Master-Slave concept for the control of parallel connected modules with individual single-phase output voltage control structures that do not involve the bridge-leg output current or the load current (cf. Section 5.1).

1 Introduction

GENERAL purpose high bandwidth Controllable AC Voltage Sources (CVSes), which have the capability to emulate certain electrical characteristics, are in recent years emerging in the area of Power-Hardware-In-the-Loop (PHIL) simulations

- to emulate mains connected loads / generators to analyze power grid dynamics and control strategies [1, 2];
- to simulate grid faults to test power electronic equipment [3–5];
- to emulate motor / generator characteristics to verify the correct operation of novel drive systems [6, 7]; and
- to develop and conduct type tests on power electronic converters [8–11], e.g. harmonic tests according to IEC 61000-3-11 and flicker tests according to IEC 61000-3-2 [12].

Such CVSes accelerate the development and / or testing processes for the mentioned application areas and hence allow saving costs and efforts [6, 13–21]. This leads to an increased interest in high bandwidth CVSes and to a higher demand of such systems in the market.

In this thesis, a four-quadrant three-phase CVS rated at 100 kW needs to be designed, which is realized by ten parallel connected 10 kW three-phase CVS modules as shown in **Fig. 1.1**. Compared to a single 100 kW converter unit, this has the advantages of

- redundancy and thus higher reliability for part load operation [22–29];

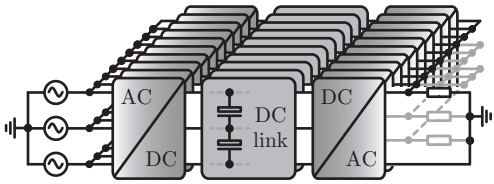


Figure 1.1: Realization of a general purpose 100 kW four-quadrant, three-phase, high bandwidth controllable AC voltage source (CVS) by ten 10 kW CVS modules. Each unit consists of an AC–DC rectifier input stage, an intermediate DC voltage link, and a DC–AC inverter output stage. As motivated in Section 2.1, three-level T-type bridge-legs are employed for the input and output stages and hence a split DC link results.

- reconfigurability leading to a higher flexibility in the usage of the modules [28, 29];
- higher efficiency in part load operation [23, 24, 26, 29];
- reduced ripple of the output voltages for synchronization and phase-shifting of the Pulse Width Modulator (PWM) carriers of the diverse modules [26]; and
- tighter control and / or faster dynamics of the output voltages [24, 26].

Due to the vast potential application areas of the CVS and because it is typically avoided to have a specific device for each task, the CVS should handle a large number of different applications and hence it needs to be highly flexible regarding the connection of possible loads or generators. Documented loads for the CVS include linear, e.g. DC, single-phase AC, and three-phase AC (balanced and unbalanced) resistive and / or inductive loads [3, 8, 11, 30, 31], and non-linear loads. Possible non-linear loads are constant power loads, e.g. DC for investigating a DC microgrid [32] and AC for emulating a low voltage supply system [33]), diode rectifiers (single-phase [6, 30] and three-phase [3]), and single-phase triac loads [8]. Due to the high flexibility of the CVS the outputs of multiple CVSes can be connected together by means of a common DC or AC bus, with some of the CVSes acting as energy sources and other as energy sinks. This, for example, enables the emulation of an island network [1, 2, 34].

Table 1.1: Electrical specifications of a 10 kW three-phase module of the 100 kW four-quadrant controllable AC voltage source (CVS). The quantities for the output and input stages are indicated for one phase, i.e. phase A for the output stage and phase a for the input stage.
[1)] line-to-neutral; [2)] line-to-line

Entire CVS	
Nominal power, P_n	10 kW
Nominal efficiency, $\eta_\mathrm{tot,n}$	$\geq$ 95%
Output stage	
Nominal rms output voltage, $V_\mathrm{A,out,n}$ [1)]	230 V
Nominal peak output voltage, $V_\mathrm{A,out,n,pk}$ [1)]	325 V
Max. peak output voltage, $V_\mathrm{A,out,max,pk}$ [1)]	350 V
Nominal rms output current, $I_\mathrm{A,out,n}$	14.5 A
Nominal peak output current, $I_\mathrm{A,out,n,pk}$	20.5 A
Full power output frequency, f_out	0 – min. 1 kHz
Output voltage small-signal bandwidth	$\geq$ 4 kHz
Conducted EMI	CISPR 11, Class A [36]
Input stage	
Rms mains voltage, V_mains [2)]	400 V_ll (+10%, -14% [37])
Nominal rms input current, $I_\mathrm{a,in,n}$	14.5 A
Nominal peak input current, $I_\mathrm{a,in,n,pk}$	20.5 A
Mains frequency, f_mains	50 Hz
Conducted EMI	CISPR 11, Class A [36]

The required high flexibility of the CVS's scope of applications leads to stringent specifications of one CVS module as summarized in **Tab. 1.1**, where the mains connected and load connected parts are referred to as input stage and output stage, respectively. Furthermore, the system needs to comply with requirements regarding quality and transient responses of the output voltage given in **Tab. 1.2**, which are motivated in Section 3.2. Additionally, a small-volume realization of the CVS is aimed for because in many applications, especially for on-site testing of power electronic circuits, e.g. avionics and telecommunication

Table 1.2: Required output properties of one CVS module, motivated in Section 3.2. The quantities are indicated for one phase, i.e. phase A.
[1)] THD: Total Harmonic Distortion

Output voltage quality	$\mathrm{THD_v}^{1)} < 2.5\%$ (cf. IEEE 1547 [53])
Output voltage slew rate	$SR \geq 209\ \mathrm{V/ms}$
Max. transient output voltage dip $\Delta v_{\mathrm{A,out}}$ due to a stepwise output current change $\Delta i_{\mathrm{A,out}}$	$\left\lvert \frac{\Delta v_{\mathrm{A,out}}}{\Delta i_{\mathrm{A,out}}} \right\rvert \leq \frac{30\ \mathrm{V}}{5\ \mathrm{A}} = 6\ \Omega$

systems, space is rather limited [35]. Even though each CVS module allows a bidirectional power flow, this work almost exclusively focuses on the case where the converter system supplies a load.

Nowadays, CVSes are already commercially available, are covering power ratings from 1 kW up to 30 MW, and are employing linear [35, 38–40], switch-mode [41–47], or hybrid, i.e. a combination of linear and switch-mode [48–51], power amplifiers. The realization of the CVSes with linear power amplifiers leads to heavy, bulky, and very expensive systems which typically have a low efficiency of only 50%–70% [35, 52] and hence cannot fulfill the efficiency requirement, i.e. $\eta_{\mathrm{tot,n}} \geq 95\%$ given in Tab. 1.1. To increase the efficiency drastically and to decrease the weight and the volume of the CVS, switch-mode amplifiers are employed. It is noted that it remains unclear to which extend hybrid concepts could be competitive alternatives to the switch-mode amplifiers. However, combinations of switch-mode and linear amplifiers definitely add a significant amount of complexity to the CVS and are for this reason not further investigated in this thesis.

On the one hand, the switch-mode CVS can be realized as a forced commutated AC–AC converter without explicit intermediate energy storage, i.e. as a matrix converter [54]. On the other hand, an intermediate energy storage element can be employed leading to an AC–DC–AC converter structure typically consisting of three parts: an AC–DC rectifier input stage, a DC link, and a DC–AC inverter output stage. The bottleneck of the matrix converters is that they do not have any voltage boosting capabilities, i.e. their maximum output voltage is limited to $\sqrt{3}/2 = 86.6\%$ of the maximum input voltage (for sinusoidal modulation) [55]. This leads, in the best case, to a maxi-

mum line-to-neutral output voltage of $110\% \times \sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3} \cdot \sqrt{3}/2 = 110\% \times V_{\mathrm{mains}}/\sqrt{2} = 311$ V, considering an increase of the mains voltage by 10% (cf. Tab. 1.1), which, however, is still smaller than the maximum required output voltage $V_{\mathrm{A,out,max,pk}} = 350$ V. Accordingly, an AC–DC–AC converter structure, as given in Fig. 1.1, is selected for the implementation of the CVS.

To store the energy in the DC link, an intermediate voltage or current circuit can be utilized, resulting in a Voltage Source Converter (VSC) or a Current Source Converter (CSC) topology.[1] Typically, for the targeted power of 10 kW per module, the VSC is the preferred solution to realize the converter system for reasons of lower costs and higher efficiency compared to the CSC [56–59].

The derived structure of one CVS module is depicted in Fig. 1.1, where each unit consists of an AC–DC rectifier input stage, an intermediate DC voltage link, and a DC–AC inverter output stage. To handle three-phase unbalanced loads and, because of further considerations explained in Section 3.1, a three-phase four-leg output stage is employed.

As it will be explained throughout this thesis, the miscellaneous application areas of the CVS mentioned at the beginning of the Introduction (see page 2) imposes advanced requirements for all three parts of the AC source and their operational interactions, but especially on the output stage as can immediately be seen from Tabs. 1.1 and 1.2. Even though CVS products are already available in the market, the design of the system as well as the optimization of its control and the consideration of a higher number of units operating in parallel have not or only partially been covered in literature. Thus, the focus of this dissertation is on the scientific investigation and design of a low-volume and efficient CVS, which achieves a very high output voltage control bandwidth and a very low output voltage ripple. This thesis is structured as follows.

In **Chapter 2**, it is first explained that a bidirectional active front end is required that regulates the DC link voltage to 700 V–800 V, followed by the motivation for the employment of a three-level T-type bridge-leg topology, which leads to a split DC link, and a switching frequency of 48 kHz for the input and output stages of one CVS module. To increase the current rating of the unit and thus to enhance the output frequency f_{out} at which full power can be delivered and / or to enlarge the over-current-carrying capacities for a limited time, bridge-

[1] Converters with a voltage-current DC link, such as the Z-source or T-source topology [55] are disregarded in this thesis.

legs can be paralleled by employing a Coupling Inductor (CI). This is analyzed in detail in the second part of the chapter. Suitable converter topologies of the CVS's output and input stage are identified in **Chapter 3** and a strong motivation for an individual operation of the output phases is given. The design of the two stages, especially of the per-phase output and the three-phase Electro-Magnetic Interference (EMI) input filters and of the per-phase output voltage control structure, are then thoroughly elaborated based on multi-objective optimizations. Furthermore, extensive measurement results are provided to verify the theoretical considerations. **Chapter 4** electrically links the input and output stages of one module and analyzes solutions to achieve in average balanced split DC link voltages for all different load scenarios mentioned on page 2 and operating conditions of each phase within the specifications given in Tab. 1.1. Moreover, the problem of a ground current i_{gnd} for earthed mains star-point and load is discussed and two options to prohibit this current are presented: suppressing i_{gnd} by means of control or by inserting a galvanic isolation in the DC link. The explanation of the module operation for grounded and floating loads concludes the chapter. Finally, a Master-Slave control concept to parallel 10 kW CVS modules is elaborated and motivated in **Chapter 5**, where simulation results for two systems in parallel support the theoretical analysis. **Chapter 6** draws the conclusion and gives an outlook on further investigations.

2 Evaluation of Key Technology

The considered 100 kW CVS is a switch-mode system and is realized by paralleling ten 10 kW modules, as motivated in the Introduction. In this chapter the topology of one such module is justified in Section 2.1, which comprises the selection of the input stage converter topology, the assignment of the DC link voltage, the determination of the bridge-leg topology, and the definition of the switching frequency for the input and output stages.

To enhance the current-carrying capacity of the CVS module, which also elevates the large-signal bandwidth of the output voltage, i.e. the output frequency up to which full power can be delivered, bridge-legs can be paralleled. An interesting option is to magnetically couple the output of the bridge-legs by a Coupling Inductor (CI), which is constituted and analyzed in detail in Section 2.2 for two bridge-legs operated in parallel, focusing on the output stage.

2.1 Topology Evaluation

A three-phase line-commutated passive diode rectifier would be the simplest realization of the input stage. Among other disadvantages, such an interface does however not permit a bidirectional power flow and accordingly is not an option. Unidirectional switch-mode mains interfaces [60, 61], such as the Vienna rectifier [62], the Swiss rectifier [63], or simple three-phase buck / boost rectifiers [64], suffer from the same latter mentioned drawback.

To allow for a bidirectional power flow, the three-phase PWM rectifier shown in **Fig. 2.1**, which has power factor correction and DC link

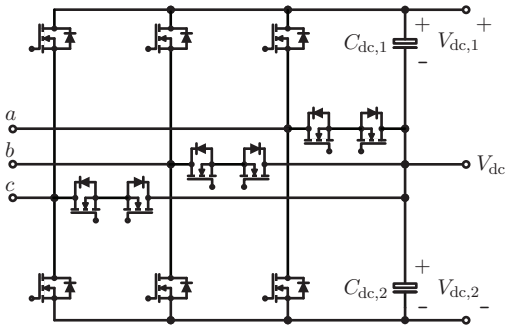


Figure 2.1: Bidirectional three-phase PWM rectifier building the input stage of the CVS. In anticipation of the results presented hereafter, a three-level T-type bridge-leg topology with SiC MOSFETs is depicted.

voltage, V_{dc}, control capabilities, must be employed. The maximum DC link voltage is set to $V_{\mathrm{dc,max}} = 800$ V, to facilitate the generation of an output stage phase voltage (e.g. $v_{\mathrm{A,out}}$ for phase A, cf. **Fig. 2.2**), with high dynamics in the range of [±350 V][1] for the different kind of loads specified on page 2.[2] In this case, the minimum absolute difference between $V_{\mathrm{dc,max}}$ and $v_{\mathrm{A,out}}$ is 50 V, which is regarded to be enough to achieve the targeted dynamic requirements given in Tab. 1.2 (cf. Section 3.2). For the nominal conditions given in Tab. 1.1, the DC link voltage is reduced to $V_{\mathrm{dc,n}} = 700$ V to enhance the efficiency of the CVS.

In a first attempt, the bidirectional output stage is realized with the same three-phase PWM converter as employed for the input stage (cf. Fig. 2.2). A refinement of the output stage inverter topology is carried out in Section 3.1. Because the reasoning for the bridge-leg topology selection is identical for the input and output stages, it is hence only explained for the output stage in the following.

The bridge-legs of the three-phase converter given in Fig. 2.2 can in the simplest form be realized with a two-level topology, as shown in **Fig. 2.3(a)**, with power semiconductors rated at a blocking voltage of 1200 V for the determined DC link voltage of 700 V–800 V. Because it

[1] The maximum output phase voltage is $V_{\mathrm{A,out,max,pk}} = 350$ V (cf. Tab. 1.1).

[2] It is noted that for three-phase output voltage systems, overmodulation is not always possible (cf. Section 4.2).

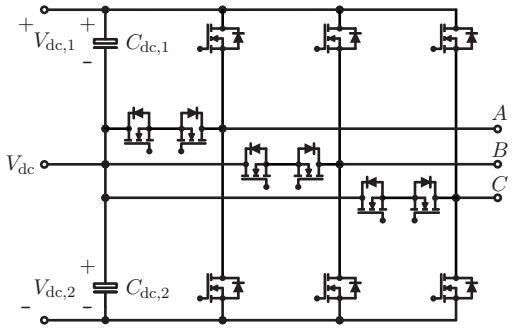


Figure 2.2: Bidirectional three-phase PWM inverter building the output stage of the CVS. In anticipation of the results presented hereafter, a three-level T-type bridge-leg topology with SiC MOSFETs is depicted.

is preferred to select a switching frequency f_s which is not located in the audible range, i.e. $f_{s,out} \geq 20$ kHz, a three-level bridge-leg topology [cf. **Figs. 2.3(b)**, **2.3(c)**, **2.3(d)**, and **2.3(e)**] leads to a significantly higher efficiency of the converter than a two-level structure [65–67]. Moreover, such a three-level topology requires for the same switching frequency less filtering to achieve the quality of the output voltage specified in Tabs. 1.1 and 1.2 [65,66]. Accordingly, the volume of the output filter can be reduced, increasing the power density of the CVS, because passive components typically take the major part of the entire converter system's volume. In addition, lower component values are also a direct consequence of the reduced filtering requirement and hence it is expected that the compliance to the dynamic requirements summarized in Tab. 1.2 can be achieved with less effort for a three-level than for a two-level topology.

The required filtering can even be further reduced by increasing the number of voltage levels at the bridge-leg output. However, such topologies drastically increase the circuit and modulation complexity of the converter and are for this reasons not regarded any further. A thorough classification, review, and comparison of multi-level converters can be found in [68–71], including modular multi-level converters with cascaded half-bridges and hybrid topologies [e.g. a combination of NPC / flying capacitor topologies with cascaded H-bridges (cf. **Fig. 2.3**)].

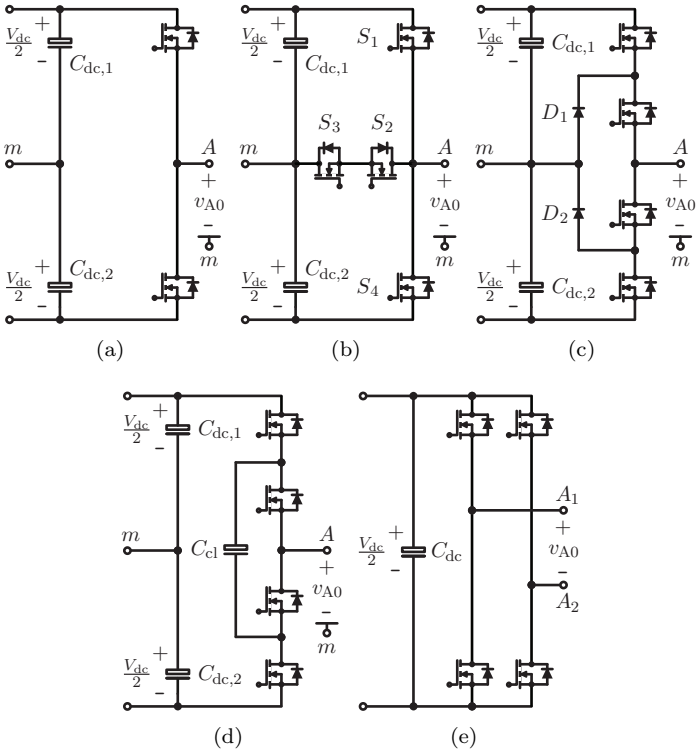


Figure 2.3: Bridge-leg topologies considered for the realization of the input and output stage converters: **(a)** two-level, **(b)** three-level T-type, **(c)** three-level neutral point clamped (NPC), **(d)** three-level flying capacitor (FC), and **(e)** H-bridge topologies. Only one phase, i.e. phase A, is depicted and, in anticipation of the results elaborated in the following, SiC MOSFETs are employed. Because it is required that the bridge-leg output voltage, v_{A0}, takes positive as well as negative values, a split DC link is considered and / or a DC link voltage midpoint m is defined also for the two-level and the three-level FC topology.

Possible basic bridge-leg topologies which generate three voltage levels at their output are [66, 68, 69]:

- the three-level transistor clamped, i.e. T-type, topology with

600 V / 650 V and 1200 V power semiconductors [cf. Fig. 2.3(b)];

- the three-level diode clamped, i.e. Neutral Point Clamped (NPC), topology with 600 V / 650 V power semiconductors [cf. Fig. 2.3(c)];
- the three-level capacitor clamped, i.e. Flying Capacitor (FC), topology with 600 V / 650 V power semiconductors [cf. Fig. 2.3(d)]; and
- the H-bridge converter with 600 V / 650 V power semiconductors [cf. Fig. 2.3(e)].

These hard-switching topologies are considered to be the most competitive ones for the realization of the output stage. Nevertheless, it is remarked that there exists other, however more complex, three-level topologies such as the split-inductor converter [72], the active NPC topology [73], or soft-switched bridge-leg topologies [74–76].

Considering Fig. 2.3, it is observed that the T-type topology embodies a two-level structure. Accordingly, this topology links the positive features of a two-level bridge-leg, such as low conduction losses, a small part count, and a simple operation principle, with the benefits of a three-level topology, which are low switching losses and superior output voltage quality [66,67]. On the one hand, the T-type structure does not require the two additional clamping diodes D_1 and D_2 compared to the NPC topology nor an additional, possibly bulky, clamping capacitor C_{cl} [77] as it is the case for the FC bridge-leg (cf. Fig. 2.3). Furthermore, with the T-type topology direct bridge-leg output voltage transitions from the positive voltage $V_{\mathrm{dc}}/2$ to the negative voltage $-V_{\mathrm{dc}}/2$ or vice versa are possible. For the NPC structure such transitions might lead to an uneven blocking voltage share in the transient stage when both power semiconductors in series turn-off at the same time [66]. On the other hand, the H-bridge converter given in Fig. 2.3(e) is built with the same number of power semiconductors than the T-type topology but requires a separate DC source for each output phase [68, 70, 77]. For a three-phase output stage converter, an additional massive DC link capacitor is hence needed, considering the power pulsation with twice the output frequency. Accordingly, the just given reasons clearly favor to realize the input and output stages with a T-type bridge-leg topology.

The operation of the T-type converter is explained to its full extent in [71]. The converter is actuated by a digital microprocessor, as further

explain in Chapter 3, and is run employing the carrier-based modulation scheme shown in **Fig. 2.4** for a positive and negative set-point bridge-leg output voltage, e.g. $v_{\mathrm{A0,set}}$ for phase A. Two in-phase triangular carriers with period $T_{\mathrm{s,out}} = 1/f_{\mathrm{s,out}}$, where $f_{\mathrm{s,out}}$ is the switching frequency, are used to generate positive and negative bridge-leg output voltages v_{A0} as shown in the figure. The process is asymmetrical, regular sampled [78], i.e. $v_{\mathrm{A0,set}}$ and required measurements for the control of the converter are updated twice in one switching period, thus when the carriers are at their minimum and maximum.[3]

To achieve the requested small-signal bandwidth $\geq 4\,\mathrm{kHz}$ of the output voltage (cf. Tab. 1.1), an output stage switching frequency $f_{\mathrm{s,out}}$ which is roughly one order of magnitude higher than 4 kHz, is necessary, i.e. $f_{\mathrm{s,out}} \overset{>}{\approx} 40\,\mathrm{kHz}$. In addition, the compliance to the conducted EMI limits given in CISPR 11, Class A [36] imposes further constraints on $f_{\mathrm{s,out}}$ as explained in the following.

The harmonic spectrum of the output voltage of a switch-mode converter shows harmonics at multiples of the switching frequency. Depending on the modulation, more or less wide sidebands around these harmonics are generated [78–80]. The CISRP 11 standard limits the conducted electromagnetic emissions of a converter (measured in dBµV) in the frequency range of [150 kHz, 30 MHz] and thus directly restricts the amplitudes of the output voltage harmonics in the indicated frequency range. Typically, to design the output filter in compliance to CISPR 11, the first harmonic with ordinal number n located in [150 kHz, 30 MHz] is decisive. Therefore, $f_{\mathrm{s,out}}$ is selected such that this particular harmonic component is pushed as much as possible to higher frequencies to maximally exploit the attenuation provided by the filter. This implies that the frequency of the $(n-1)^{\mathrm{th}}$ harmonic is located just below 150 kHz. Often, this harmonic is placed at $144\,\mathrm{kHz} < 150\,\mathrm{kHz} - 4.5\,\mathrm{kHz} = 145.5\,\mathrm{kHz}$, because the conducted EMI measurement procedure [81] employs a test receiver bandwidth of ±4.5 kHz around the center frequency. Further explanations concerning EMI measurements are given throughout Chapter 3.

Based on the above elaboration, 144 kHz needs to be an integral multiple of the switching frequency $f_{\mathrm{s,out}}$, and thus considering $f_{\mathrm{s,out}} \overset{>}{\approx} 40\,\mathrm{kHz}$, possible values of $f_{\mathrm{s,out}}$ are 36 kHz, 48 kHz, and 72 kHz. On the one hand, the higher the switching frequency the higher the switching

[3] For such a sampled process the term "double-update-mode" is sometimes used.

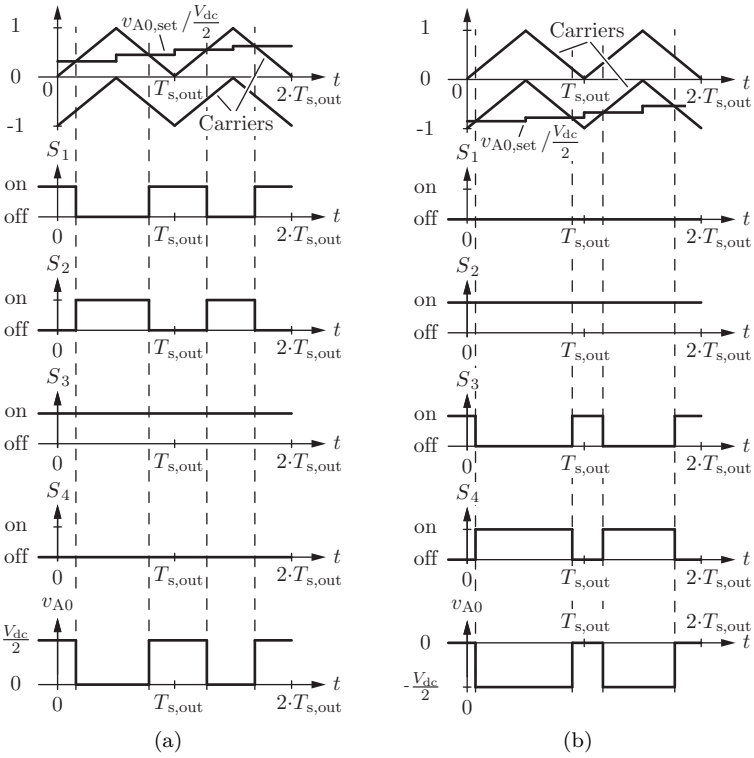


Figure 2.4: Illustrative drawing of the employed asymmetrical regular sampled carrier-based modulation scheme to actuate each T-type bridge-leg of the input and output stage converters **(a)** for a positive and **(b)** for a negative bridge-leg output set-point voltage $v_{A0,set}$ (exemplary shown for phase A of the output stage).

losses and typically also the lower the efficiency of the converter.[4] On the other hand, a higher $f_{s,out}$ potentially leads to a smaller filter volume and also allows for a faster dynamic response of the output voltage.

[4]For the designed converter system (cf. Chapter 3), the total nominal losses are composed of roughly 2/3 semiconductor (including the gate driving) and 1/3 filter losses. The semiconductor losses are further separated into approximately 4/5 of switching (and gate driving) and 1/5 of conduction losses.

Thus, as a compromise between a high efficiency, a small filter volume, and fast dynamic response, a switching frequency of $f_{\mathrm{s,out}} = 48$ kHz is selected for the output stage. For the input stage the same switching frequency of $f_{\mathrm{s,in}} = f_{\mathrm{s,out}} = 48$ kHz is utilized, although the input stage has by far lower input voltage dynamic specifications. With this choice of $f_{\mathrm{s,in}}$, a low-volume realization of the input filter is targeted.

Due to the rapid development of Silicon Carbide (SiC) power semiconductors in the last years, which feature continuously increasing power capacities and present lower losses and higher temperature operation compared to Silicon (Si), SiC MOSFETs [82] have been chosen to realize the switching devices for the selected T-type bridge-leg topology and the switching frequency of 48 kHz. In a first step, Cree's 1200 V C2M0080120D MOSFETs (with a channel resistance of 80 mΩ) are employed (cf. Section 3.2) and in a second step, because of the development occurred in the meantime, Cree's 1200 V C2M0025120D MOSFETs (with a channel resistance of 25 mΩ) are utilized. All four switching devices of the T-type topology are realized with the same type of 1200 V MOSFET (C2M0080120D or C2M0025120D), even though the two middle switches S_2 and S_3 could be realized with 600 V / 650 V devices [cf. Fig. 2.3(b)]. However, no 600 V / 650 V SiC MOSFET with comparable performance regarding switching and conduction losses than the two selected devices have been available up to this moment.

2.2 Coupling Inductor Approach

To increase the current-carrying capacity and to enhance the large-signal bandwidth of one 10 kW module of the high bandwidth controllable AC voltage source (CVS) given in Fig. 1.1, i.e. to increase the frequency $f_{\text{out,max}}$ up to which the CVS delivers full power, the current rating of each phase leg can be doubled by using two paralleled bridge-legs per phase (cf. **Tab. 2.1**).[5] For the filter designed in Section 3.2, a large-signal bandwidth of 2 kHz is from there expected, which complies to the specification indicated in Tab. 1.1. For output frequencies $f_{\text{out}} < f_{\text{out,max}}$, the CVS hence reveals over-current capabilities, i.e. it is able to provide an output current which is higher than the nominal one. At $f_{\text{out}} = 50\,\text{Hz}$ twice the nominal current of $I_{\text{out,n}} = 14.5\,\text{A}$ (rms), i.e. $I_{\text{out,max}} = 29\,\text{A}$ (rms), can be delivered for instance.

In [83,84], it is revealed that the total volume of the converter stage and filter is reduced if a Coupling Inductor (CI) [cf. **Fig. 2.5**] is employed for the two bridge-legs of each phase instead of two single inductors. Since, to the knowledge of the author, a comprehensive discussion of CIs for a coupling factor $k \approx 1$ is missing in literature (cf. **Appendix A**), the section at hand focuses on the main aspects of CI design and application for $k \approx 1$, including the basic modeling and the control as well as the experimental verification of a CI as employed in the considered CVS, and thus partly extends the knowledge base for CIs. As motivated in Section 3.1, each output phase is operated individually and hence the analysis presented below is based on single-phase considerations. The single-phase circuit for phase A in which the CI is utilized is depicted in Fig. 2.5; Tab. 2.1 summarizes the specifications of the CVS which are relevant for this section.

The outline of this part is as follows: definitions and different equivalent circuits of a CI are derived in Section 2.2.1. Section 2.2.2 introduces a splitting of the CI currents into a transverse (DM) and a longitudinal (CM) component and analyzes their influence on the magnetic flux density in the core. Stationary and dynamic conditions to guarantee a

[5] It is remarked that theoretically the large-signal bandwidth $f_{\text{out,max}}$ of the output voltage can be extended up to the value of the small-signal bandwidth $f_{\text{bw,ss}}$. However, practically, $f_{\text{out,max}}$ is often smaller than $f_{\text{bw,ss}}$ due to the limited current-carrying capability of the converter's bridge-legs and filter to conducted the elevated capacitive filter current. Accordingly, augmenting the current rating of the CVS by placing bridge-legs in parallel is an appropriate means to boost the large-signal bandwidth.

Table 2.1: For Section 2.2 relevant electrical specifications of the CVS (cf. Fig. 1.1).
[1)] line-to-neutral; [2)] $V_{dc} = V_{dc,1} + V_{dc,2}$; [3)] Current-derating: $I_{out,max}$ @ $f_{out} = 50$ Hz and $I_{out,n}$ for $f_{out,max} = 2$ kHz.

Nominal output power, $P_{out,n}$	10 kW
Nominal output voltage, $V_{out,n}$ [1)] (rms)	230 V
Nominal DC link voltage, $V_{dc,n}$ [2)]	700 V
Maximum DC link voltage, $V_{dc,max}$ [2)]	800 V
Nominal output current, $I_{out,n}$ (rms)	14.5 A
Maximum output current, $I_{out,max}$ (rms)	29 A
Output frequency, f_{out}	$0 - 2$ kHz[3]
Converter switching frequency, f_s	48 kHz
Nominal efficiency, η_n	$\geq 95\%$

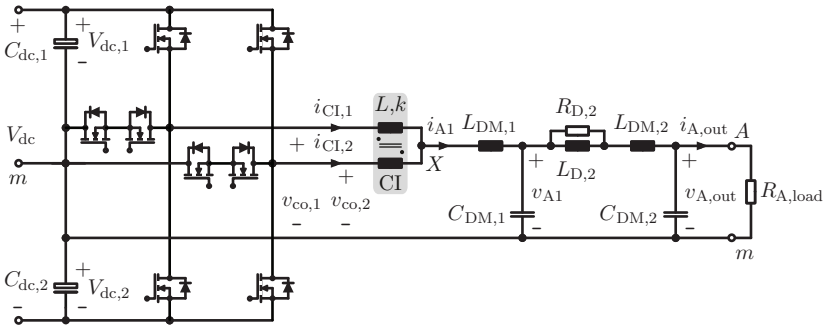


Figure 2.5: Equivalent circuit of one output phase, e.g. phase A, of the CVS realized with two bridge-legs coupled by a coupling inductor. In anticipation of the results obtained in Section 3.2 a two-stage LC output filter with a passive series RL damping branch is employed.

symmetrical CI core magnetization are elaborated in Section 2.2.3 and Section 2.2.4, respectively. To verify the theoretical analysis and the simulations, experimental results are finally presented in Section 2.2.5. Furthermore, a selection and summary of relevant literature of CIs is presented in Appendix A to support the discussion of the CI concept in the following.

2.2.1 CI: Definitions and Equivalent Circuits

The definitions of the currents, voltages, and fluxes as well as of the winding directions for the CI are shown in **Fig. 2.6(a)**. L_1 and L_2 are the self-inductances, M is the mutual inductance given by $M = k \cdot \sqrt{L_1 \cdot L_2} \geq 0$ and k is the coupling factor defined as $k = \sqrt{1-\sigma} \wedge k \in [0,1]$, where $\sigma \in [0,1]$ is the total leakage-factor.

Assuming perfect symmetry, both windings of the CI are identical, and hence they have the same number of turns ($N = N_1 = N_2$) and the same self-inductances $L = L_1 = L_2$. Consequently, the voltage across the CI windings are given by

$$\begin{aligned} v_{\mathrm{CI},1} &= L \cdot \tfrac{\mathrm{d}i_{\mathrm{CI},1}}{\mathrm{d}t} - M \cdot \tfrac{\mathrm{d}i_{\mathrm{CI},2}}{\mathrm{d}t}, \\ v_{\mathrm{CI},2} &= -M \cdot \tfrac{\mathrm{d}i_{\mathrm{CI},1}}{\mathrm{d}t} + L \cdot \tfrac{\mathrm{d}i_{\mathrm{CI},2}}{\mathrm{d}t}, \end{aligned} \tag{2.1}$$

which directly leads to the equivalent circuit model depicted in **Fig. 2.6(b)** [85–87] - which does not contain an ideal transformer for galvanic isolation as both windings are connected at node X. It is especially pointed out that M and k are defined to be positive quantities, which differs from the definition in other publications.

It can be deduced from Fig. 2.6(a) that the low-frequency components of the fluxes $\phi_{\mathrm{CI},1}$ and $\phi_{\mathrm{CI},2}$ in the core, resulting from equal low-frequency components of the bridge-leg currents $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$, have the same value for $N = N_1 = N_2$. For a high coupling factor $k \approx 1$, the fluxes almost completely cancel each other and only the leakage flux components remain. This allows employing a smaller core cross-section compared to two single inductors. However, a series inductor $L_{\mathrm{DM},1}$ then has to be provided for the DM filtering [cf. **Fig. 2.8(a)**]. It has to be noted that a low coupling factor could be realized by a proper selection of the core geometry, i.e. by reducing the length of the leakage path [87–94].

The time derivatives of both CI winding currents for Fig. 2.5 are given by

$$\begin{aligned} \tfrac{\mathrm{d}i_{\mathrm{CI},1}}{\mathrm{d}t} &= \tfrac{1}{L_{\mathrm{CI,f}}} \cdot \left[v_1 \cdot (L_{\mathrm{DM},1} + L) + v_2 \cdot (k \cdot L - L_{\mathrm{DM},1}) \right] \\ &\overset{k=1, L \gg L_{\mathrm{DM},1}}{\approx} \tfrac{1}{4 \cdot L_{\mathrm{DM},1}} \cdot (v_1 + v_2)\,, \\ \tfrac{\mathrm{d}i_{\mathrm{CI},2}}{\mathrm{d}t} &= \tfrac{1}{L_{\mathrm{CI,f}}} \cdot \left[v_2 \cdot (L_{\mathrm{DM},1} + L) + v_1 \cdot (k \cdot L - L_{\mathrm{DM},1}) \right] \\ &\overset{k=1, L \gg L_{\mathrm{DM},1}}{\approx} \tfrac{1}{4 \cdot L_{\mathrm{DM},1}} \cdot (v_1 + v_2)\,, \end{aligned} \tag{2.2}$$

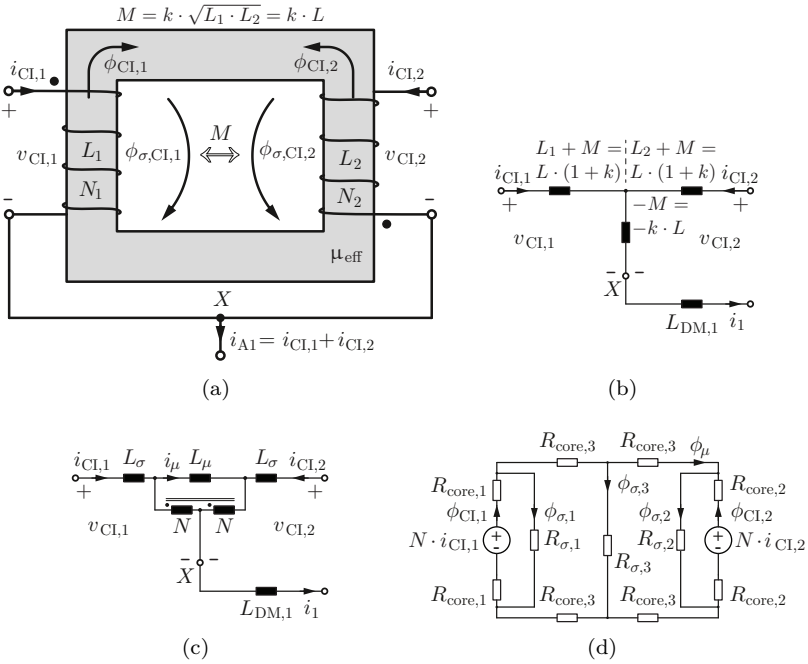


Figure 2.6: **(a)** Definitions of the CI currents, voltages, and fluxes, **(b)** equivalent circuit of the (symmetric, $N = N_1 = N_2$) CI based on the self-inductances and the mutual inductance, **(c)** equivalent circuit based on the leakage inductance and the magnetizing inductance, and **(d)** simplified reluctance model.

where $L_{\mathrm{CI,f}} = L^2 \cdot \left(1 - k^2\right) + 2 \cdot L_{\mathrm{DM},1} \cdot (1 + k) \cdot L$. $v_1 = v_{\mathrm{co},1} - v_{\mathrm{A1}}$ and $v_2 = v_{\mathrm{co},2} - v_{\mathrm{A1}}$ are the differences between the bridge-leg output voltages $v_{\mathrm{co},1}$, $v_{\mathrm{co},2}$ and the voltage across the first DM filter capacitor $C_{\mathrm{DM},1}$. From the above equations, it can be directly derived that, if the parallel bridge-legs are operated in an interleaved manner, both CI winding currents show a ripple with twice the switching frequency f_{s} of a bridge-leg. Furthermore, both winding currents are equal if $k = 1$ and $L \gg L_{\mathrm{DM},1}$. In this case, the DM filtering is only achieved by $L_{\mathrm{DM},1}$ without contribution of the CI. This is not immediately obvious from Fig. 2.6(b) (series inductance $-k \cdot L$), but can be seen directly from

Fig. 2.6(c) considering (2.3).

Remark: To achieve the interleaving, the two carriers for the PWM of the bridge-legs are phase-shifted by 180 °. An interleaved operation of the two bridge-legs is assumed for the rest of this section.

It is noted, that for $k = 1$ and $L \gg L_{\mathrm{DM},1}$, the voltage at node X (cf. **Fig. 2.6**) with reference to the DC input voltage midpoint m is approximately $(v_{\mathrm{co},1} + v_{\mathrm{co},2})/2$ and shows five levels. Therefore, the number of voltage levels is increased from three (for each bridge-leg) to five as also mentioned in Appendix A.

Since the CI is assumed to be electrically and magnetically symmetrical, the leakage inductances L_σ and the magnetizing inductance L_μ can be distributed equally to the primary and secondary side of a transformer equivalent circuit. This results in the circuit depicted in **Fig. 2.6(c)**, because both windings are connected to the same node X. The derivation of this circuit is step-by-step shown in **Fig. 2.7**. A similar CI equivalent circuit is presented in [89, 95–97]. A parameter identification of the electrical properties to Fig. 2.6(b) results in

$$\begin{aligned} L_\sigma &= L \cdot (1 - k), \\ L_\mu &= 4 \cdot k \cdot L. \end{aligned} \tag{2.3}$$

Consequently, the magnetizing inductance is roughly 4 times the self-inductance (for $k \approx 1$). The transformer shown in Fig. 2.6(c) is ideal, and clearly points out the coupling of $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$ which are, however, only identical if $L_\mu \gg L_{\mathrm{DM},1}$ and thus $L \gg L_{\mathrm{DM},1}$. For completeness a simplified reluctance model is shown in **Fig. 2.6(d)**. Especially for multi-phase systems with more than two phases, this model is a preferred approach to analyze the CI [98–105].

Before analyzing the coupling inductor in more details, the two single-stage LC filter structures shown in **Fig. 2.8** (one with a CI and one without) are compared with respect to the required filter inductances and capacitances for two difference cases:

- *Same maximum peak-to-peak bridge-leg current ripples*: In industrial converters, the maximum peak-to-peak bridge-leg output current ripples $\Delta i_{\mathrm{CI},1,\mathrm{pp,max}}$ and $\Delta i_{\mathrm{CI},2,\mathrm{pp,max}}$ are typically limited to 20%-60% of the nominal output current peak value in order to restrict current sampling errors, the peak current stress and / or the switching losses of the power semiconductors as well as the high-frequency losses in the inductive components. Thus, on one hand, compared to a standard interleaved parallel operation of

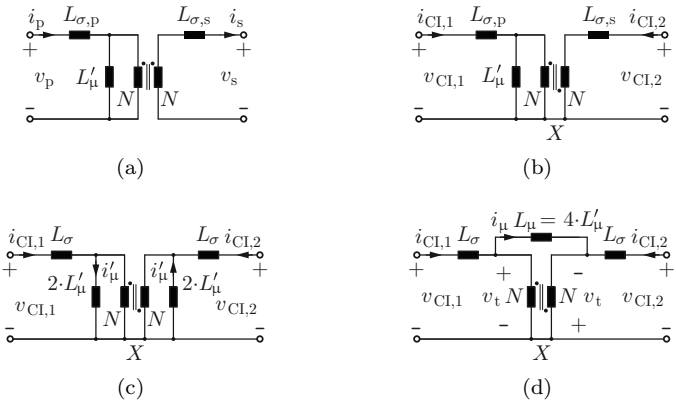


Figure 2.7: Derivation of the equivalent circuit depicted in Fig. 2.6(c) for a symmetrical CI ($N = N_1 = N_2$): **(a)** transformer equivalent circuit with primary and secondary leakage inductances $L_{\sigma,\mathrm{p}}$ and $L_{\sigma,\mathrm{s}}$ as well as magnetizing inductance L'_μ; **(b)** equivalent circuit for a CI, as employed in Fig. 2.5; **(c)** equal distribution of the leakage ($L_\sigma = L_{\sigma,\mathrm{p}} = L_{\sigma,\mathrm{s}}$) and magnetizing inductances to the primary and secondary side for a symmetric CI; and **(d)** combining the two inductances $2 \cdot L'_\mu$ to a single magnetizing inductance $L_\mu = 4 \cdot L'_\mu$, since both windings are connected at X, resulting in the circuit of Fig. 2.6(c).
The equivalence of (c) and (d) can also be shown by calculating the voltages across the CI windings: for (c) the voltages $v_{\mathrm{CI},1} = L_\sigma \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t + 2 \cdot L'_\mu \cdot \mathrm{d}i'_\mu / \mathrm{d}t$ and $v_{\mathrm{CI},2} = L_\sigma \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t - 2 \cdot L'_\mu \cdot \mathrm{d}i'_\mu / \mathrm{d}t$ result. The ideal transformer forces a magnetizing current $i'_\mu = (i_{\mathrm{CI},1} - i_{\mathrm{CI},2}) / 2$ as shown in (c) [equal voltages across $2 \cdot L'_\mu$ on both sides of the ideal transformer] which leads to $v_{\mathrm{CI},1} = (L_\sigma + L'_\mu) \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t - L'_\mu \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t$ and $v_{\mathrm{CI},2} = -L'_\mu \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t + (L_\sigma + L'_\mu) \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t$. For (d) the voltage v_t across the ideal transformer is $v_\mathrm{t} = L_\mu / 2 \cdot \mathrm{d}i_\mu / \mathrm{d}t$ with a magnetizing current of $i_\mu = (i_{\mathrm{CI},1} - i_{\mathrm{CI},2}) / 2 = i'_\mu$. Thus, the winding voltages yield $v_{\mathrm{CI},1} = L_\sigma \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t + v_\mathrm{t} = L_\sigma \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t + L_\mu / 2 \cdot \mathrm{d}i_\mu / \mathrm{d}t = (L_\sigma + L_\mu / 4) \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t - L_\mu / 4 \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t$ and $v_{\mathrm{CI},2} = L_\sigma \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t - v_\mathrm{t} = L_\sigma \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t - L_\mu / 2 \cdot \mathrm{d}i_\mu / \mathrm{d}t = -L_\mu / 4 \cdot \mathrm{d}i_{\mathrm{CI},1} / \mathrm{d}t + (L_\sigma + L_\mu / 4) \cdot \mathrm{d}i_{\mathrm{CI},2} / \mathrm{d}t$. A factor comparison then identifies $L_\mu = 4 \cdot L'_\mu$ as derived for (d).

two bridge-legs with individual inductors L_f [cf. **Fig. 2.8(b)**], the inductance value of $L_{\mathrm{DM},1}$ [cf. Fig. 2.8(a)], to obtain the same

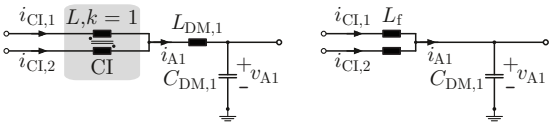


Figure 2.8: Single-stage LC filter structures: **(a)** parallel connection of two bridge-legs with a coupling inductor (CI - without DM filter influence for $k = 1$) and a filter stage formed by $L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},1}$; and **(b)** parallel connection of two bridge-legs with individual inductors L_{f}, where the LC filter stage is then effectively formed by $\frac{L_{\mathrm{f}}}{2}$ (parallel connection of both inductors L_{f}) and $C_{\mathrm{DM},1}$.

maximum peak-to-peak current ripples $\Delta i_{\mathrm{CI},1,\mathrm{pp,max}} = \Delta i_{\mathrm{CI},2,\mathrm{pp,max}}$ in both bridge-legs is

$$L_{\mathrm{DM},1} = \frac{L}{2 \cdot \left(4 \cdot \frac{L}{L_{\mathrm{f}}} - 1\right)} \underset{L \gg L_{\mathrm{f}}}{\approx} \frac{L_{\mathrm{f}}}{8}, \tag{2.4}$$

for $k \approx 1$, i.e. for a bifilar arrangement of the CI windings. However, $L_{\mathrm{DM},1}$ has to conduct a low-frequency current as well as a maximum peak-to-peak current ripple $\Delta i_{\mathrm{A1,pp,max}}$ which is twice the one through L_{f}.
On the other hand, regarding EMI noise suppression, the capacitance $C_{\mathrm{DM},1}$ in this case needs to be 4 times greater for the filter structure with a CI [cf. Fig. 2.8(a)] than for the filter without a CI [cf. Fig. 2.8(b)] to reach the same LC filter cut-off frequency. Or, for $L_{\mathrm{DM},1} = L_{\mathrm{f}}/8$ and equal capacitance values $C_{\mathrm{DM},1}$ for both filter structures, the high-frequency roll-off of the filter in Fig. 2.8(a) is reduced by 12 dB compared to the filter in Fig. 2.8(b).

- *Same maximum peak-to-peak current ripple of i_{A1}*: In this case, $L_{\mathrm{DM},1}$ is given by

$$L_{\mathrm{DM},1} \overset{k=1, L \gg L_{\mathrm{f}}}{\approx} \frac{L_{\mathrm{f}}}{2}, \tag{2.5}$$

resulting in the same filter cut-off frequency for equal capacitance values of $C_{\mathrm{DM},1}$ for both filter structures depicted in Fig. 2.8.

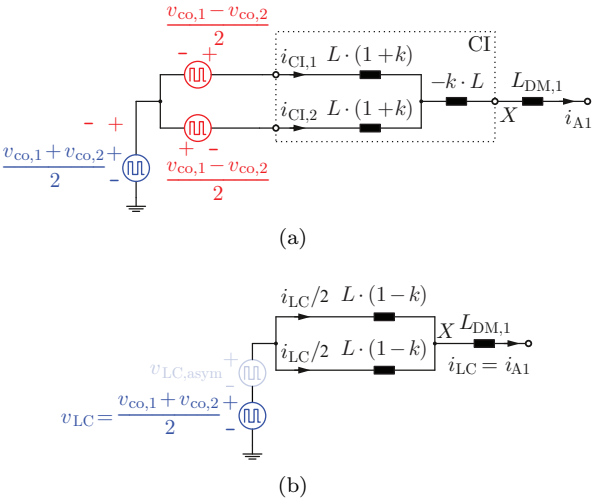
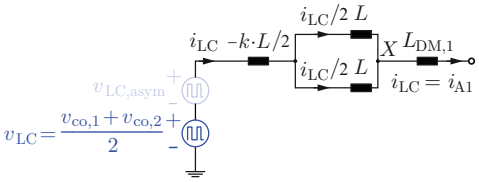


Figure 2.9: **(a)** Division of the bridge-leg voltages into a longitudinal current i_{LC} (in the direction of the power flow) forming voltage v_{LC} and a transverse current i_{TC} forming voltage v_{TC}, **(b)**, **(c)** equivalent circuits for longitudinal voltages and currents, and **(d)** equivalent circuit for transverse voltages and currents. In (c), compared to (b), the negative inductance part $-k\cdot L$ of both branches is concentrated into a single negative inductance $-k\cdot L/2$.

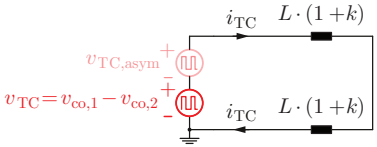
2.2.2 Transverse and Longitudinal Current Separation and Corresponding Magnetic Flux Densities

An illustrative method to analyze the CI is to distinguish between an equivalent circuit for the Longitudinal Current [LC - **Fig. 2.9(b)**] and for the Transverse Current [TC - **Fig. 2.9(d)**]. In [83,92,96,98,102,104, 106–120], the LC is denominated as a Common Mode (CM) current and the TC as a Differential Mode (DM) current. However, these denominations are associated to EMI investigations and hence to avoid confusion with the EMI nomenclature, the terms *Longitudinal Current* (in the direction of the power flow) and *Transverse Current* (and / or cross current between the converter bridge-legs) are preferred (cf. **Fig. 2.9**).

The voltages v_{LC} and v_{TC} which drive the longitudinal and the



(c)



(d)

Fig. 2.9: Continued.

transverse current, respectively, are given by

$$\begin{aligned} v_{LC} &= \tfrac{v_{co,1}+v_{co,2}}{2}, \\ v_{TC} &= v_{co,1} - v_{co,2} \end{aligned} \tag{2.6}$$

and are depicted in **Fig. 2.10(a)** and **Fig. 2.10(b)** for interleaved voltages $v_{co,1}$ and $v_{co,2}$. The associated effective longitudinal inductance L_{LC} and transverse inductance L_{TC} are

$$\begin{aligned} L_{LC} &= L\cdot(1-k) = L_\sigma, \\ L_{TC} &= L\cdot(1+k). \end{aligned} \tag{2.7}$$

Comparing Fig. 2.9(d) to Fig. 2.6(c), it is clear that the transverse current i_{TC} is equal to the magnetizing current i_μ [106,114]. Using a CI and a separate filter inductor $L_{DM,1}$ allows suppressing the transverse current by an inductance which is four times the self-inductance L of the CI [for $k \approx 1$, cf. Eq. (2.3)]. This explains why (for the same maximum peak-to-peak bridge-leg current) considerable higher inductance values [cf. Eq. (2.4)] are required for two single inductors L_f in each bridge-leg than for employing a CI and just one filter inductance $L_{DM,1}$ as depicted in Fig. 2.9(a).

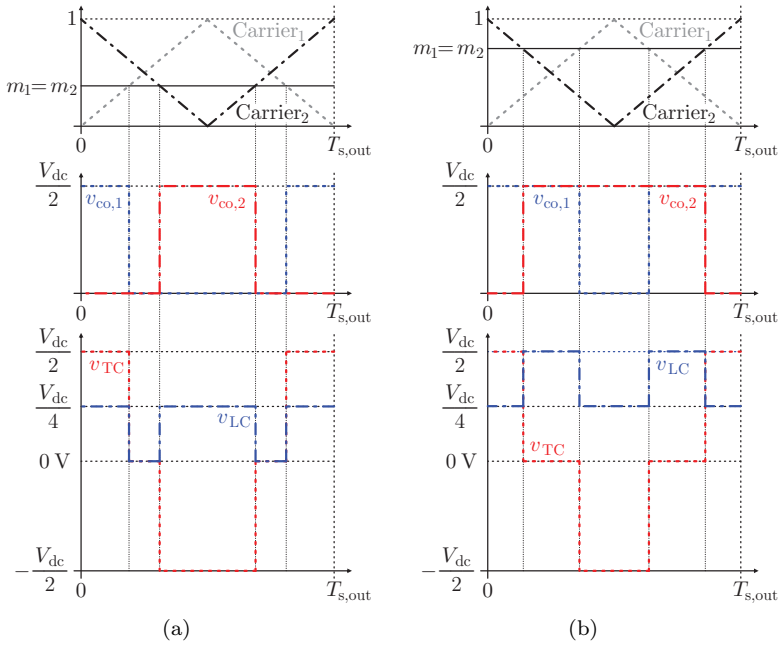


Figure 2.10: **(a)** v_{LC} and v_{TC} for a modulation index of $m_{\mathrm{i}} \leq 0.5$ and **(b)** v_{LC} and v_{TC} for a modulation index of $m_{\mathrm{i}} \geq 0.5$. The resulting longitudinal current $i_{\mathrm{LC}} = i_{\mathrm{LC,lf}} + \Delta i_{\mathrm{LC}}$ (consisting of a low-frequency and a ripple component) as well as the transverse current i_{TC} for (a) and (b) are shown qualitatively in **(c)** and **(d)**, respectively. A second set of triangular carriers is employed for modulation indices $0 > m_{\mathrm{i}} \geq -1$ (not shown; cf. Fig. 2.4).

For an ideal coupling of both CI windings ($k = 1$), L_{LC} becomes zero (as the leakage inductance) and $L_{\mathrm{TC}} = 2 \cdot L = L_{\mu}/2$ is equal to half of the magnetizing inductance L_{μ} [$L_{\mu,k=1} = 4 \cdot L$, cf. (2.3)]. Thus, the longitudinal current i_{LC} is filtered by $L_{\mathrm{DM},1}$ and the transverse current i_{TC} is filtered by $2 \cdot L_{\mathrm{TC}}$, which is also described in [96, 116, 121]. This means on the other hand that the CI, for $k = 1$, is "transparent" to the longitudinal current i_{LC} and affects only the transverse current i_{TC} [122]. Illustratively, this can be seen from Fig. 2.9(a), where the inductances $L \cdot (1+k)$ become $2 \cdot L$ for $k = 1$. For the longitudinal current i_{A1} the mentioned inductances with the value $2 \cdot L$ are in parallel, re-

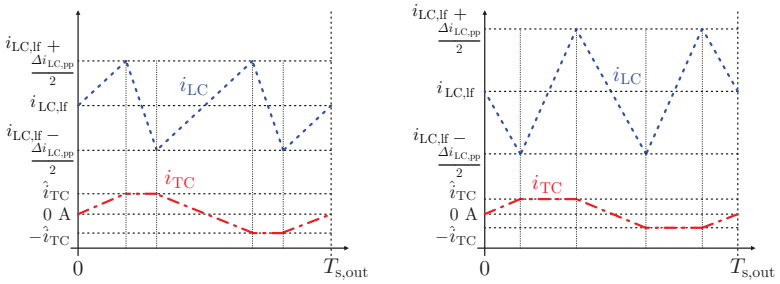


Fig. 2.10: Continued.

sulting in $2 \cdot L \| 2 \cdot L = L$. This, together with $-k \cdot L = -L$, leads to zero inductance for the longitudinal components [$k = 1$, cf. **Fig. 2.9(c)**].

The ripples of both current components are depicted in **Fig. 2.10(c)** and **Fig. 2.10(d)**. They reveal the following characteristics:

- *Longitudinal current* $i_{LC} = i_{A1}$: The current ripple shows twice the switching frequency of the bridge-legs. The low-frequency value of the longitudinal current $i_{\mathrm{LC,lf}}$ is given by the sum of the load current $i_{\mathrm{A,out}}$ and the reactive capacitor currents of the output filter. The peak-to-peak current ripple is maximal for a modulation index of $m_{\mathrm{i}} = 0.25$ and can be calculated as follows:

$$\begin{aligned} \Delta i_{\mathrm{LC,pp}} &= \frac{V_{\mathrm{dc}}}{\left(L_{\mathrm{DM},1} + \frac{L \cdot (1-k)}{2}\right) \cdot f_{\mathrm{s,out}}} \cdot \left(\frac{m_{\mathrm{i}}}{4} - \frac{m_{\mathrm{i}}^2}{2}\right) \\ &\underset{m_{\mathrm{i}}=0.25}{\leq} \frac{V_{\mathrm{dc}}}{32 \cdot \left(L_{\mathrm{DM},1} + \frac{L \cdot (1-k)}{2}\right) \cdot f_{\mathrm{s,out}}}. \end{aligned} \tag{2.8}$$

- *Transverse current* i_{TC}: The current ripple shows the switching frequency $f_{\mathrm{s,out}}$ of the bridge-legs. If both bridge-legs and the CI are completely symmetrical, the mean (low-frequency) value of i_{TC} is zero. If asymmetries are present (as given in practice), a proper current control scheme needs to guarantee that a low-frequency value of $i_{\mathrm{TC,lf}} \cong 0$ A is achieved as discussed in Section 2.2.3. The peak-to-peak ripple of i_{TC} is maximal at a mod-

ulation index of $m_\mathrm{i} = 0.5$ and is given by

$$\begin{aligned} \Delta i_{\mathrm{TC,pp}} &= \frac{m_\mathrm{i} \cdot V_\mathrm{dc}}{4 \cdot L \cdot (1+k) \cdot f_{\mathrm{s,out}}} \\ &\underset{m_\mathrm{i}=0.5}{\leq} \frac{V_\mathrm{dc}}{8 \cdot L \cdot (1+k) \cdot f_{\mathrm{s,out}}}. \end{aligned} \tag{2.9}$$

As already pointed out earlier, both CI winding currents are only equal if $L \gg L_{\mathrm{DM},1}$ - mathematically strictly only for $L \to \infty$. Since the winding currents can be formed by superposition of $i_\mathrm{LC}/2$ and i_TC for a symmetrical CI

$$\begin{aligned} i_{\mathrm{CI},1} &= \tfrac{i_\mathrm{LC}}{2} + i_\mathrm{TC} = \tfrac{i_\mathrm{A1}}{2} + i_\mathrm{TC}, \\ i_{\mathrm{CI},2} &= \tfrac{i_\mathrm{LC}}{2} - i_\mathrm{TC} = \tfrac{i_\mathrm{A1}}{2} - i_\mathrm{TC}, \end{aligned} \tag{2.10}$$

the only difference between both winding currents is the transverse current i_TC (equal winding currents can only be reached if $i_\mathrm{TC} = 0$ A, i.e. theoretically for an infinite magnetizing inductance and therefore for $L \to \infty$).

The CI shown in Fig. 2.6(a) is in some publications [87, 123, 124] called "inversely coupled inductors" (inverse coupling inductor), because a positive current change in one winding results in a negative voltage drop at the other winding [represented by the negative inductance $-M$ in Fig. 2.6(b)]. If the winding direction of one winding is reversed, "directly coupled inductors" (direct coupling inductor) are obtained. In this case, the longitudinal and transverse inductances are given by

$$\begin{aligned} L'_\mathrm{LC} &= L \cdot (1+k) = L_\mathrm{TC}, \\ L'_\mathrm{TC} &= L \cdot (1-k) = L_\mathrm{LC} \end{aligned} \tag{2.11}$$

and for $k = 1$ the CI is "transparent" to the transverse current and only filters the longitudinal current (thus, not applicable for interleaved operation of the bridge-legs).

Remark: Some publications make the difference between "transient" and "steady-state" inductances of a CI [123–126], which are synonyms for the longitudinal and transverse inductances, respectively.

The magnetic fluxes through both windings ($N = N_1 = N_2$) associated with the longitudinal and transverse currents are given by

$$\begin{aligned} \phi_{1,\mathrm{LC}} = \phi_{2,\mathrm{LC}} &= \tfrac{L_\mathrm{LC} \cdot i_\mathrm{LC}}{2 \cdot N} = \tfrac{L \cdot (1-k) \cdot i_\mathrm{LC}}{2 \cdot N}, \\ \phi_{1,\mathrm{TC}} &= \tfrac{L_\mathrm{TC} \cdot i_\mathrm{TC}}{N} = \tfrac{L \cdot (1+k) \cdot i_\mathrm{TC}}{N}, \\ \phi_{2,\mathrm{TC}} &= -\tfrac{L_\mathrm{TC} \cdot i_\mathrm{TC}}{N} = -\tfrac{L \cdot (1+k) \cdot i_\mathrm{TC}}{N}, \end{aligned} \tag{2.12}$$

and

$$\begin{aligned} \phi_{\mathrm{CI},1} &= \phi_{1,\mathrm{TC}} + \phi_{1,\mathrm{LC}}, \\ \phi_{\mathrm{CI},2} &= \phi_{2,\mathrm{TC}} + \phi_{2,\mathrm{LC}}. \end{aligned} \tag{2.13}$$

Referring to the given converter system (cf. Tab. 2.1) and the built filter with a CI (cf. **Tab. 2.3**), the maximum longitudinal and transverse current ripples (Δi_{LC} and Δi_{TC}) as well as the maximal low-frequency longitudinal current $i_{\mathrm{LC,lf,max}}$ ($i_{\mathrm{LC}} = i_{\mathrm{LC,lf}} + \Delta i_{\mathrm{LC}}$) were calculated for the maximum DC link voltage of $V_{\mathrm{dc,max}} = 800$ V and for a switching frequency of $f_{\mathrm{s,out}} = 48$ kHz per bridge-leg:

$$\begin{aligned} \Delta i_{\mathrm{TC,pp,max}} &= 1.06 \text{ A}, \\ \Delta i_{\mathrm{LC,pp,max}} &= 5.94 \text{ A}, \\ i_{\mathrm{LC,lf,max}} &= \sqrt{2} \cdot 29 \text{ A} = 41.0 \text{ A}. \end{aligned} \tag{2.14}$$

For the employed ETD 59/31/22 core (N87) from EPCOS with an equivalent magnetic cross-section area $A_{\mathrm{e}} = 368$ mm^2, the related values of the CI magnetic flux densities result for a symmetric magnetization in

$$\begin{aligned} B_{1,\mathrm{TC,pk}} = \tfrac{\phi_{1,\mathrm{TC,pk}}}{A_{\mathrm{e}}} = B_{2,\mathrm{TC,pk}} = \tfrac{\phi_{2,\mathrm{TC,pk}}}{A_{\mathrm{e}}} &= 0.11 \text{ T}, \\ \Delta B_{1,\mathrm{LC,pk}} = \tfrac{\Delta\phi_{1,\mathrm{LC,pk}}}{A_{\mathrm{e}}} = \Delta B_{2,\mathrm{LC,pk}} = \tfrac{\Delta\phi_{2,\mathrm{LC,pk}}}{A_{\mathrm{e}}} &= 0.21 \text{ mT}, \\ B_{1,\mathrm{LC,lf,max}} = \tfrac{\phi_{1,\mathrm{LC,lf,max}}}{A_{\mathrm{e}}} = B_{2,\mathrm{LC,lf,max}} = \tfrac{\phi_{2,\mathrm{LC,lf,max}}}{A_{\mathrm{e}}} &= 2.9 \text{ mT}, \end{aligned} \tag{2.15}$$

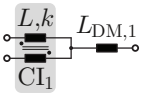
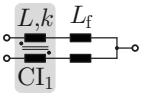
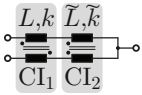
where exemplary (alike for winding 2)

$$\begin{aligned} \phi_{1,\mathrm{TC,pk}} &= \tfrac{L_{\mathrm{TC}} \cdot i_{\mathrm{TC,pk}}}{N} = \tfrac{L_{\mathrm{TC}} \cdot \Delta i_{\mathrm{TC,pp,max}}}{2 \cdot N}, \\ \Delta\phi_{1,\mathrm{LC,pk}} &= \tfrac{L_{\mathrm{LC}} \cdot \Delta i_{\mathrm{LC,pk}}}{2 \cdot N} = \tfrac{L_{\mathrm{LC}} \cdot \Delta i_{\mathrm{LC,pp,max}}}{4 \cdot N}, \\ \phi_{1,\mathrm{LC,lf,max}} &= \tfrac{L_{\mathrm{LC}} \cdot i_{\mathrm{LC,lf,max}}}{2 \cdot N}. \end{aligned} \tag{2.16}$$

For the flux density due to i_{LC}, the part resulting from the current ripple $\Delta i_{\mathrm{LC,pp,max}}$ and the one coming from the low-frequency component $i_{\mathrm{LC,lf,max}}$ are considered separately. From (2.15), it follows that $B_{1,\mathrm{TC,pk}} = B_{2,\mathrm{TC,pk}} \gg \Delta B_{1,\mathrm{LC,pk}} = \Delta B_{2,\mathrm{LC,pk}} \wedge B_{1,\mathrm{LC,lf,max}} = B_{2,\mathrm{LC,lf,max}}$ and accordingly $B_{\mathrm{CI},1,\mathrm{pk}} = \frac{\phi_{\mathrm{CI},1,\mathrm{pk}}}{A_{\mathrm{e}}} = B_{\mathrm{CI},2,\mathrm{pk}} = \frac{\phi_{\mathrm{CI},2,\mathrm{pk}}}{A_{\mathrm{e}}} \approx B_{1,\mathrm{TC,pk}} = B_{2,\mathrm{TC,pk}}$. Thus, for coupling factors k close to 1, the magnetizing flux determines the maximum flux density in the entire core and can be directly computed to

$$B_{\mu,\mathrm{pk}} = \frac{4 \cdot k \cdot L}{2 \cdot N \cdot A_{\mathrm{e}}} \cdot i_{\mathrm{TC,pk}} \approx B_{1,\mathrm{TC,pk}} = B_{2,\mathrm{TC,pk}} = 0.11 \text{ T}. \tag{2.17}$$

Table 2.2: Comparison between different placements of the first filter stage inductance for the same peak-to-peak current ripple in both bridge-legs [cf. Fig. 2.5] with respect to the required inductance value, volume and losses [referred to configuration (a)]. The comparison is based on simplified similarity relations, as could be derived by a more detailed analysis. The volume and losses of the coupling inductor CI_1 are not considered.
[1)] The direct coupling inductor CI_2 in configuration (c) can only be used to filter the longitudinal current and / or is "transparent" to the transverse current (for $\tilde{k} \approx 1$); accordingly, an inverse coupling inductor CI_1 (or individual inductors) must be employed to limit the transverse current.

			
Filter structure	$k = 1$ (a)	$k = 1$ (b)	$k,\ \tilde{k} = 1$ (c)[1)]
Inductance	$L_{\mathrm{DM},1}$	$L_{\mathrm{f}} = 2 \cdot L_{\mathrm{DM},1}$	$\tilde{L} = L_{\mathrm{DM},1}$
Volume	$V_{\mathrm{L,(a)}}$	$V_{\mathrm{L,(b)}} \sim 1.1 \cdot V_{\mathrm{L,(a)}}$	$V_{\mathrm{L,(c)}} \sim V_{\mathrm{L,(a)}}$
Losses	$P_{\mathrm{L,(a)}}$	$P_{\mathrm{L,(b)}} \sim 1.3 \cdot P_{\mathrm{L,(a)}}$	$P_{\mathrm{L,(c)}} \sim P_{\mathrm{L,(a)}}$

From these considerations, it can be seen that an unbalance between the two winding currents of only a few ampères can directly lead to large fluxes in the core, because of the large inductance seen by this current, which may result in core saturation (cf. Section 2.2.3) [119].

Remark: Since errors in the current measurement can lead to an additional transverse current (cf. Section 2.2.3), a large margin of $B_{\mu,\mathrm{pk}} \approx 0.11$ T to the N87 material's saturation flux density of $B_{\mathrm{s}} = 0.39$ T $-$ 0.49 T [127] is provided.

Compared to a CI which filters the longitudinal and the transverse currents, the filter volume can be reduced in case of employing a strong coupling ($k \approx 1$) of the two windings (almost no filtering effect on the longitudinal current) and an additional longitudinal current filtering inductance $L_{\mathrm{DM},1}$. The inductance value, the inductor volume as well as its losses for the same current ripples are compared in **Tab. 2.2** for different arrangements of the first filter stage inductors with respect to

the CI. It can be concluded that filtering option (b) is with respect to volume and losses worse than options (a) and (c). For the reason of simpler manufacturing, (a) was selected in the case at hand.

As can be deduced from Fig. 2.6(c) and as already mentioned, the transverse current is the magnetizing current $i_\mu = i_{\mathrm{TC}}$, which for $k \approx 1$ determines the maximum flux density in the CI core (assuming that the flux density is evenly distributed over the core cross-section). The CI is designed to achieve a high core material utilization and thus the magnetization should be symmetrical in all operating conditions. This is analyzed in the next two sections for stationary and dynamic conditions.

2.2.3 Symmetric Core Magnetization: Stationary Considerations

Different resistive or semiconductor on-state voltage drops (e.g. for IGBTs) in the two bridge-legs [cf. Fig. 2.5] or possible imprecisions in the conversion of the modulation indices to the bridge-leg output voltages $v_{\mathrm{co},1}$ and $v_{\mathrm{co},2}$ (e.g. imprecise switching or gate driver tolerances [119]) can lead to a difference of the average values of the voltages $v_{\mathrm{co},1}$ and $v_{\mathrm{co},2}$. Such effects will be called asymmetries between the two bridge-legs for the rest of the section and can lead to a difference in the average current of both bridge-legs $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$, as also discussed in [90, 128–130]. The effect can be modeled by an additional voltage source v_{asym} due to the asymmetries. For the analysis of the asymmetries' impact on the currents and hence on the fluxes in the core [cf. Fig. 2.9(b) and Fig. 2.9(d)], the voltage v_{asym} can further be split into a longitudinal current forming component $v_{\mathrm{LC,asym}}$ and a transverse current forming component $v_{\mathrm{TC,asym}}$ according to (2.6). A constant value of $v_{\mathrm{TC,asym}}$ results in an offset of the transverse current i_{TC} and accordingly of the magnetizing flux, as illustratively shown in **Fig. 2.11(a)**.

The mentioned asymmetries are observed in any real power electronic circuit, which means that for preventing the magnetizing flux to saturate the core, a proper control of both bridge-leg currents is required [96,103,104,112,115,118,120,128–135]. A possible control scheme of the converter stage (single-phase) is depicted in **Fig. 2.12**, where two PI-controllers assure that in "steady-state" both winding currents show equal local average values. With such a control scheme, an almost sym-

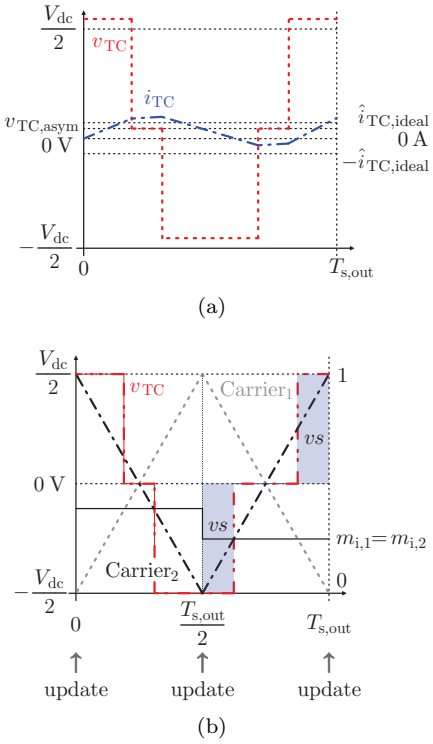


Figure 2.11: (a) Illustrative increase of the transverse current i_{TC} (offset) due to a constant voltage offset $v_{TC,\,asym}$ in v_{TC} resulting from asymmetries of both bridge-legs and **(b)** instances at which the references for the PW-modulator (triangular carriers, regular sampling) must be updated to keep a symmetrical magnetization and / or balanced volt-seconds vs.

metrical core magnetization and hence a maximal magnetic material utilization is guaranteed. It is important to note that two current controllers are necessary to avoid an offset of the transverse current i_{TC}. Alternatively, the output current $i_{A,out}$ and the difference between the two winding currents could be controlled [119]. If no current controllers or only a single controller for the sum of both bridge-leg currents is employed, the relation between the steady-state average (low-frequency)

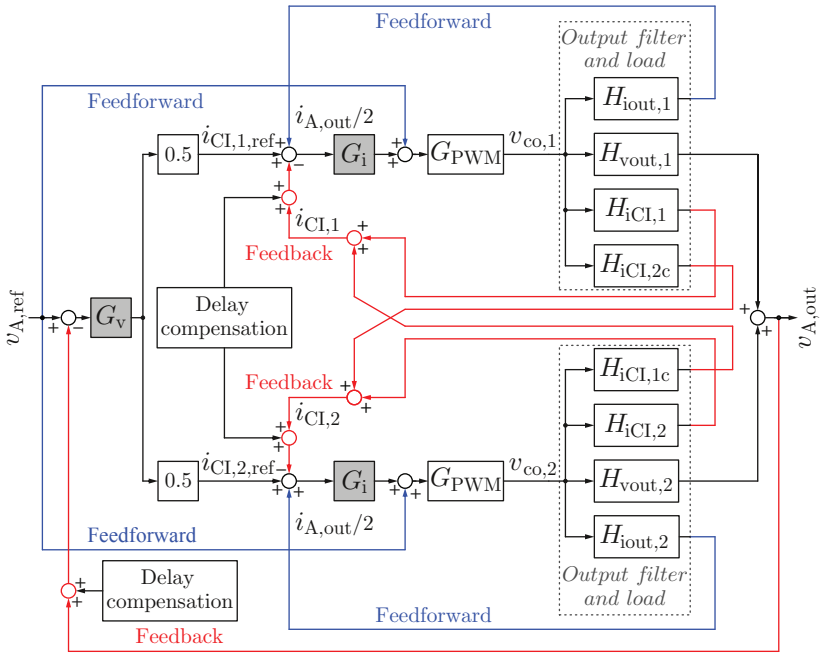


Figure 2.12: Control scheme for the circuit in Fig. 2.5 to guarantee symmetry of $i_{CI,1}$ and $i_{CI,2}$. The control structure shows delay compensations, a feedforward of the CVS output current $i_{A,out}$ and of the output voltage reference $v_{A,ref}$. The two-stage LC output filter and the load are modeled with transfer functions.

values of the two CI winding currents would be given by

$$\frac{i_{CI,1,lf}}{i_{CI,2,lf}} = \frac{R_{ws,2}}{R_{ws,1}}, \tag{2.18}$$

where $R_{ws,i}$ is the sum of the winding resistance, parasitic wiring resistances and differential on-state resistances of the power semiconductors of a bridge-leg i ($i = 1, 2$). For this consideration, it is assumed that no other asymmetries are present and that the bridge-leg output voltages $v_{co,1}$ and $v_{co,2}$ are below the modulation limit.

Remark: Dependent on the frequency f_{out} of the output voltage, a P-type controller may give satisfactory performance. The lower f_{out},

the more an employment of a PI-controller (higher loop-gain) is beneficial.

However, also the non-ideal characteristics of the current measurement has to be taken into account for the current control, as recognized in [119]. Both bridge-leg currents in the present hardware are measured with the sensor SENSITEC CDS4025. According to its data sheet, the maximal error in the current measurement is 1.3%, which is 0.53 A for twice the nominal current flowing to the output [$i_{\mathrm{A1,lf,max}} = I_{\mathrm{A,out,max}} = 29$ A (rms)], which in the worst case leads to an additional transverse current of 0.27 A. This small current error of 0.27 A increases the flux density in the core by ≈ 56 mT, which is about half (!) of the ideal magnetizing flux amplitude generated by the nominal operation transverse current and therefore needs to be considered in the course of the CI design. Supplementary errors in the current measurement setup, such as measurement value processing errors with analog amplifiers or discretization errors in the Digital Signal Processor (DSP), can further increase the magnetic flux in the core. Accordingly, a certain safety margin has to be provided and / or the core cannot be fully utilized magnetically.

2.2.4 Symmetric Core Magnetization: Dynamic Considerations

To ensure symmetry of the (average) winding currents also for transient operation, a large enough bandwidth of the current controllers [cf. Fig. 2.12] is required. Moreover, as discussed in [120], to balance the volt-seconds applied to the magnetizing inductance L_{μ}, the updates of the reference for the PW-modulators cannot occur arbitrarily. Considering an interleaved operation of both bridge-legs with a regular sampling, triangular carriers and a double-update-mode (the reference is updated and measurements are evaluated twice in a switching period $T_{\mathrm{s,out}}$), the updates must be performed when one of the carrier reaches 1 and / or the other carrier reaches 0. This reference update and sampling scheme is also referred as regular sampling and is depicted in **Fig 2.11(b)**, from where it can be seen that balanced volt-seconds *vs* result.

It has to be pointed out that for a certain limitation of the peak-to-peak current ripple in the two bridge-legs and a certain minimum bandwidth of the output voltage control of the CVS, there is a trade-

off between the inductance values of L and $L_{\mathrm{DM},1}$. For perfect coupling ($k = 1$), the self-inductance L of the CI should be as high as possible to result in the same peak-to-peak bridge-leg current ripple with a lower $L_{\mathrm{DM},1}$ [cf. (2.4)]. A large L can be obtained with a high effective permeability μ_{eff}, a large magnetic cross-section area A_{e} or a high number of turns N. The last two options lead to an increased size of the CI and increase the winding losses. Increasing μ_{eff} is promising, however, mismatches between the winding currents $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$ would more easily saturate the core. Thus, the realization of the CI with an air-gap can be advantageous or necessary. In conclusion, either the volume and / or winding losses of the CI, the current measurement accuracy or both are limiting the maximum meaningful self-inductance L of the CI. Additionally, even though coupling factors $k \approx 1$ can be reached in practice, the higher the self-inductance L the higher also the leakage inductance $L_\sigma = L \cdot (1 - k)$. This means that the CI's self-inductance L cannot be increased arbitrary without having a negative impact on the dynamics of the CVS output voltage $v_{\mathrm{A,out}}$ (cf. Fig. 2.5).

2.2.5 Experimental Verification

Because of the afore mentioned trade-off between the value of the CI's self-inductance L and the first filter stage inductance $L_{\mathrm{DM},1}$, L was chosen to be approximately 10 times larger than $L_{\mathrm{DM},1}$. The parameters of the two-stage LC filter with a passive series RL damping of the second filter stage (cf. Fig. 2.5) are given in Tab. 2.3. The measured output impedance of the filter is shown in **Fig. 2.13**. In the frequency range [200 Hz, 100 kHz] a good match between the calculation, based on the values in Tab. 2.3, and the measurement is obtained (parasitic resistances, inductances and capacitances are not considered in the calculation).

To verify the theoretical analysis conducted in this section, two phase legs of a three-phase three-level T-type voltage source converter topology [136] are employed. The performed measurements for a modulation index of $m_{\mathrm{i}} = 0.25$ and $m_{\mathrm{i}} = 0.5$ are summarized in **Fig. 2.14** and **Fig. 2.17**. These two modulation indices are selected since at $m_{\mathrm{i}} = 0.25$ the longitudinal and at $m_{\mathrm{i}} = 0.5$ the transverse current peak-to-peak ripple is at its maximum, respectively. The regular sampling (two triangular carriers per bridge-leg) is implemented in a double-update-mode, thus the Analog to Digital Converters (ADCs) are trig-

Table 2.3: Two-stage *LC* output filter component values (cf. Fig. 2.5); the measurements were conducted with an Agilent 4294A 40 Hz-110 MHz Precision Impedance Analyzer at 48 kHz (except for R_D) without a premagnetization or a voltage offset. All inductive components are wound with a litz wire (2000 × 0.05 mm - 4×Mylar) from Rotima Inc. and have an air-gap. N87 from EPCOS is used as a core material.
[1)] Nominal values for $I_{dc} = I_{A,out,n} = 14.5$ A; percentage of the nominal inductance values for twice the nominal current $I_{dc} = I_{A,out,max} = 29$ A: 55% for $L_{DM,1}$, 74% for L_D and 100% for $L_{DM,2}$ (at 100 °C). (For $L_{DM,1}$ and L_D the core is partially saturated.)

Component	*Measured values*	*Remark*
Coupling inductor CI	$L = L_1 = L_2 = 987$ µH $k = 0.9987$	2×ETD 59/31/22; bifilar winding; $N = N_1 = N_2 = 26$
$L_{DM,1}$	87.9 µH[1)]	2×ETD 49/25/16; $N = 24$
$L_{DM,2}$	4.87 µH[1)]	2×ETD 29/16/10; $N = 8$
L_D	9.32 µH[1)]	2×ETD 29/16/10; $N = 10$
R_D	$1.3\ \Omega \| 2\ \Omega = 0.79\ \Omega$	Vishay MMB 0207
$C_{DM,1}$	6.1 µF (rated value: 6.8 µF)	X2 MKP 305 V AC/max. continuous 500 V DC
$C_{DM,2}$	4.1 µF (rated value: 4.7 µF)	X2 MKP 305 V AC/max. continuous 500 V DC

gered twice in one switching period $T_{s,out} = 1/f_{s,out} = 20.83$ µs of the bridge-legs. The conversion is started when the carriers are reaching 0 and 1 [cf. Fig. 2.11(b)] and no over-sampling scheme is implemented. A TI TMS320F2808 fixed-point DSP and a Lattice Field Programmable Gate Array (FPGA) are used to implement the converter's control.

The simulations, to which the measured quantities are compared, were performed in GeckoCIRCUITS (a circuit simulator based on Java and developed at the PES laboratory [137]) with the filter parameters given in Tab. 2.3. The same sampling and DSP code as for the hardware setup have been implemented in the simulator. Because of the ADCs and PWM units, a delay of 1.5 sample intervals ($= 3/4 \cdot T_{s,out}$) occurs in the hardware (cf. Section 3.3.2).

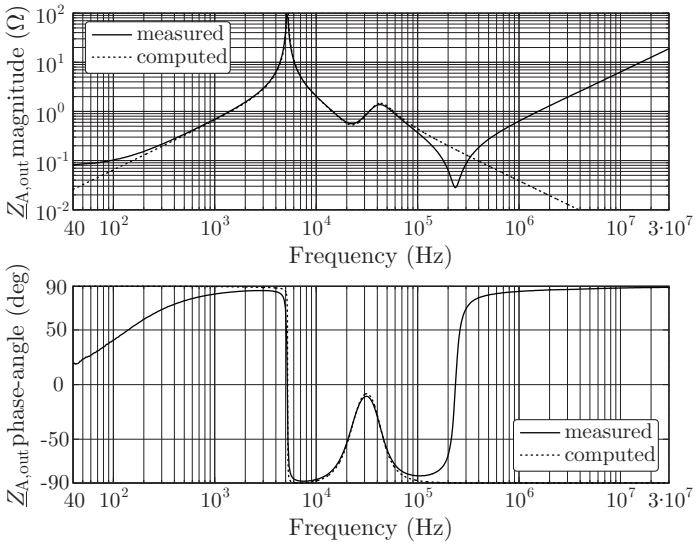
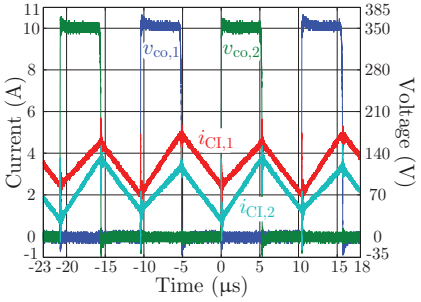
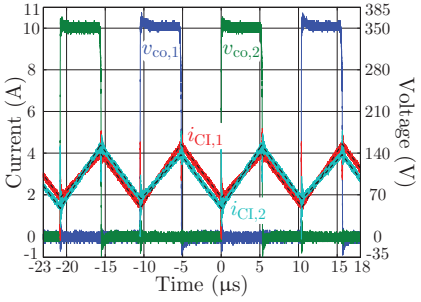


Figure 2.13: Measured (Agilent 4294A 40 Hz–110 MHz Precision Impedance Analyzer) and computed (with the measured component values as given in Tab. 2.3) output impedance of the two-stage output filter with a CI when both bridge-leg outputs are shorted (cf. Fig. 2.5). The two curves deviate at low frequencies because the parasitic resistances of the components are not included in the computation. At high frequencies the parasitic inductance of the output capacitor $C_{\mathrm{DM},2}$ and of the connecting wires lead to an inductive output impedance.

In **Fig. 2.14(a)** and **Fig. 2.14(b)**, the measured bridge-leg output voltages $v_{\mathrm{co},1}$, $v_{\mathrm{co},2}$ and currents $i_{\mathrm{CI},1}$, $i_{\mathrm{CI},2}$ are depicted for a modulation index of $m_{\mathrm{i}} = 0.25$ and for the converter running in open-loop and closed-loop, respectively. It can clearly be seen that, due to the asymmetries in the hardware setup, the average values of the two bridge-leg voltages $v_{\mathrm{co},1}$ and $v_{\mathrm{co},1}$ are not equal. This results in an additional transverse current i_{TC} between the bridge-legs and hence in different average values of $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$, if the currents are not properly controlled [cf. Fig. 2.14(a)]. With the closed-loop control as shown in Fig. 2.12, the additional transverse current is eliminated. The measured and simulated bridge-leg currents $i_{\mathrm{CI},1}$, $i_{\mathrm{CI},2}$ are in a good agreement. Even though the coupling factor $k = 0.9987 \approx 1$ is high, the two bridge-



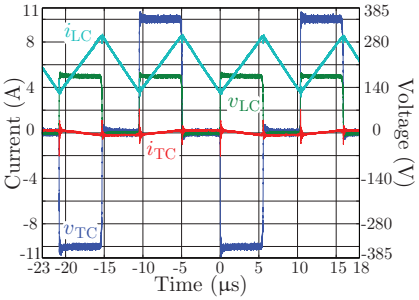
(a)



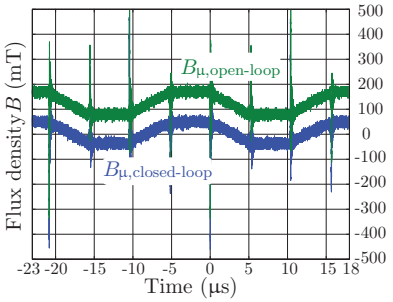
(b)

Figure 2.14: Measurements for $V_{dc,n} = 700$ V with a nominal resistive load of $R_{A,load} = 15.9\,\Omega$ for a modulation index of $m_i = 0.25$: **(a)** bridge-leg output voltages $v_{co,1}$, $v_{co,2}$ and currents $i_{CI,1}$, $i_{CI,2}$ in open-loop; **(b)** $v_{co,1}$, $v_{co,2}$, $i_{CI,1}$, and $i_{CI,2}$ in closed-loop employing the control scheme depicted in Fig. 2.12 [the dashed-lines are the simulated bridge-leg currents which coincide with the measured waveforms]; **(c)** separations into the longitudinal and transverse voltages v_{LC}, v_{TC} and currents i_{LC}, i_{TC}; and **(d)** comparison between the magnetizing flux density in closed-loop $B_{\mu,\text{closed-loop}}$ and open-loop $B_{\mu,\text{open-loop}}$, computed with (2.17) based on $i_\mu = i_{TC} = (i_{CI,1} - i_{CI,2})/2$ [see following remark]. *Remark*: The spikes shown in (d) are due to C_w [cf. Fig. 2.16(a)] and result from calculating B_μ based on $i_\mu = (i_{CI,1} - i_{CI,2})/2$. Therefore, these spikes are not present in the actual (and not reconstructed) magnetizing current and / or flux density waveform.

leg currents are not completely identical because the ratio between the CI's self-inductance L and $L_{DM,1}$ is $L/L_{DM,1} \approx 11 \neq \to \infty$. This is in



(c)



(d)

Fig. 2.14: Continued. *Controller settings*: PI-controllers $k_\mathrm{p} \cdot (1 + T_\mathrm{i} \cdot s)\,/T_\mathrm{i} \cdot s$ (trapezoidal integration): $k_\mathrm{p} = 75\,\mathrm{mA/V}$ and $T_\mathrm{i} = 500\,\mu\mathrm{s}$ for the voltage controller; $k_\mathrm{p} = 4\,\mathrm{V/A}$ and $T_\mathrm{i} = 100\,\mu\mathrm{s}$ for the current controllers.

accordance with the theoretical considerations mentioned earlier.

Remark: In a control scheme with only one current controller, the same modulation index m_i is utilized to generate the two bridge-leg output voltages. In steady-state, the modulation index m_i to generate a certain output voltage remains constant. It follows that, for the same output voltage, the unbalance in the currents $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$ is equal for running the converter in open-loop as in closed-loop with just one current controller.

In Fig. 2.14(a), the local average (low-frequency) values of the currents through the windings of the coupling inductor are $i_{\mathrm{CI},1,\mathrm{lf}} \approx 3.5\,\mathrm{A}$

and $i_{\mathrm{CI,2,lf}} \approx 2.3$ A; thus the current offset is $2 \cdot i_{\mathrm{TC,lf}} \approx 1.2$ A ($i_{\mathrm{TC,lf}}$ denotes the deviation of the CI winding currents from the ideal symmetric case). This unbalance in the currents is due to two different kinds of asymmetries, which are occurring simultaneously (cf. Fig. 2.15):

- Different effective duty-cycles δ_1, δ_2, i.e. $\delta_1 = \delta + \Delta\delta$ and $\delta_2 = \delta$ (error in the duty-cycle of $\Delta\delta$), because of an unequal switching of the bridge-legs.
- Different parasitic ohmic resistances $R_{\mathrm{w,1}}$, $R_{\mathrm{w,2}}$ and power semiconductor on-state voltage drops (v_{F}, R_{diff}) of the bridge-legs.

Remark: For the experimental results carried out below the three-level T-type converter presented in [66] has been employed as such and hence the switching elements are realized with IGBTs.

The presence of these asymmetries causes an offset in the bridge-leg currents such that the volt-seconds applied to the inductive part of the CI are balanced in steady-state. Hence, it follows

$$v_{\mathrm{TC,lf}} = v_{\mathrm{co,1,lf}} - v_{\mathrm{co,2,lf}} \stackrel{!}{=} 0 \text{ V}. \tag{2.19}$$

Considering **Fig. 2.15** and assuming in a first step that all power semiconductor on-state characteristics are identical (even if 600 V and 1200 V IGBTs are employed) and approximated by constant voltage sources v_{F} and differential resistances R_{diff} (at 75 °C)

$$v_{\mathrm{IGBT/Diode}} = v_{\mathrm{F}} + R_{\mathrm{diff}} \cdot i_{\mathrm{IGBT/Diode}} = 0.7 \text{ V} + 92 \text{ m}\Omega \cdot i_{\mathrm{IGBT/Diode}}, \tag{2.20}$$

Eq. (2.19) can be solved for $i_{\mathrm{TC,lf}} = (i_{\mathrm{CI,1,lf}} - i_{\mathrm{CI,2,lf}})/2$. This leads to

$$i_{\mathrm{TC,lf}} = \frac{1}{2} \cdot \frac{\Delta\delta \cdot (V_{\mathrm{dc}} + 2 \cdot v_{\mathrm{F}} + R_{\mathrm{diff}} \cdot i_{\mathrm{LC,lf}}) + R_{\mathrm{w,d}} \cdot i_{\mathrm{LC,lf}}}{4 \cdot R_{\mathrm{diff}} + R_{\mathrm{w,s}} - (2 \cdot \delta + \Delta\delta) \cdot R_{\mathrm{diff}}}, \tag{2.21}$$

where $R_{\mathrm{w,s}} = R_{\mathrm{w,1}} + R_{\mathrm{w,2}}$ and $R_{\mathrm{w,d}} = R_{\mathrm{w,2}} - R_{\mathrm{w,1}}$. It is noted that the resistances $R_{\mathrm{w,1}}$ and $R_{\mathrm{w,2}}$ comprise all ohmic parts from the output of the power semiconductors to node X in Fig. 2.5. Assuming $R_{\mathrm{w,1}} = R_{\mathrm{w,2}} = R_{\mathrm{w}}$, (2.21) can be simplified to

$$i_{\mathrm{TC,lf}} = \frac{1}{2} \cdot \frac{\Delta\delta \cdot (V_{\mathrm{dc}} + 2 \cdot v_{\mathrm{F}} + R_{\mathrm{diff}} \cdot i_{\mathrm{LC,lf}})}{4 \cdot R_{\mathrm{diff}} + 2 \cdot R_{\mathrm{w}} - (2 \cdot \delta + \Delta\delta) \cdot R_{\mathrm{diff}}}. \tag{2.22}$$

Therefore, the low-frequency transverse current $i_{\mathrm{TC,lf}}$ in steady-state is a function, not only of the circuit parameters v_{F}, R_{diff}, $R_{\mathrm{w,1}}$ and

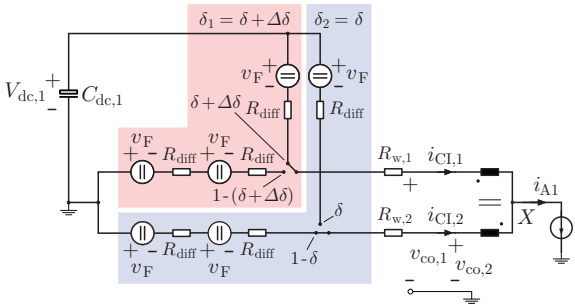


Figure 2.15: Equivalent circuit for calculating the bridge-leg current offset in Fig. 2.14(a) for the T-type converter (for a positive output voltage and current) in dependency on a duty-cycle error $\Delta\delta$ and a difference in the CI winding and PCB resistances $R_{\mathrm{w},1}$ and $R_{\mathrm{w},2}$. Equal on-state characteristics for all power semiconductors are assumed. Always only one branch of each bridge-leg is conducting current and the bridge-legs are operated in an interleaved manner.

$R_{\mathrm{w},2}$, but also of the duty-cycle δ, the duty-cycle error $\Delta\delta$, the DC link voltage V_{dc} and the low-frequency longitudinal current $i_{\mathrm{LC,lf}}$; hence

$$i_{\mathrm{TC,lf}} = f\left(\Delta\delta, \delta, V_{\mathrm{dc}}, i_{\mathrm{LC,lf}}, v_{\mathrm{F}}, R_{\mathrm{diff}}, R_{\mathrm{w},1}, R_{\mathrm{w},2}\right). \tag{2.23}$$

Assuming $\delta \gg \Delta\delta$, $V_{\mathrm{dc}} \gg 2 \cdot v_{\mathrm{F}} + R_{\mathrm{diff}} \cdot i_{\mathrm{LC,lf}}$ and $R_{\mathrm{diff}} \gg R_{\mathrm{w}}$, (2.22) can be further simplified to

$$i_{\mathrm{TC,lf}} \cong \frac{\Delta\delta}{2-\delta} \cdot \frac{V_{\mathrm{dc}}}{4 \cdot R_{\mathrm{diff}}}. \tag{2.24}$$

Thus, in a first approximation, the low-frequency transverse current $i_{\mathrm{TC,lf}}$ is directly proportional to the difference in the bridge-leg duty-cycles $\Delta\delta$ and depending on the operating point via δ.

The sensitivity of $i_{\mathrm{TC,lf}}$ to duty-cycle errors $\Delta\delta$ is assessed in the following for the considered hardware and for a duty-cycle of 0.25: If the voltage pulse in $v_{\mathrm{co},1}$ is only 10 ns longer than the one in $v_{\mathrm{co},2}$, the error in the duty-cycle δ between the bridge-legs is $\Delta\delta \approx 0.05\%$, resulting in an additional averaged (over one switching period T_{s}) voltage of 175 mV in bridge-leg 1 [cf. Fig. 2.5].

Additionally, from the Printed Circuit Board (PCB) of the three-level T-type converter, the resistances of the copper tracks at 75 °C are

assessed with

$$R_{\mathrm{PCB},1} = R_{\mathrm{PCB},2} = 5\ \mathrm{m\Omega}. \tag{2.25}$$

The calculated resistances from the bridge-leg outputs at the PCB to node X in Fig. 2.5 are for a conductor temperature of 75 °C

$$R_{\mathrm{wc},1} = R_{\mathrm{wc},2} = 16\ \mathrm{m\Omega}, \tag{2.26}$$

and therefore

$$R_{\mathrm{w},1} = R_{\mathrm{PCB},1} + R_{\mathrm{wc},1} = R_{\mathrm{w},2} = R_{\mathrm{PCB},2} + R_{\mathrm{wc},2} = 21\ \mathrm{m\Omega}. \tag{2.27}$$

Comparing $R_{\mathrm{w},1}$ and $R_{\mathrm{w},2}$ to the differential resistance of the power semiconductors $R_{\mathrm{diff}} = 92\ \mathrm{m\Omega}$, it is noted that R_{diff} is dominant.

For the case at hand, the longitudinal current is $i_{\mathrm{LC,lf}} = i_{\mathrm{CI},1,\mathrm{lf}} + i_{\mathrm{CI},2,\mathrm{lf}} = 5.8\ \mathrm{A}$ [cf. Fig. 2.14(a)]. With (2.22) the steady-state low-frequency transverse current and thus the difference of $i_{\mathrm{CI},1}$ and $i_{\mathrm{CI},2}$ are computed to

$$i_{\mathrm{TC,lf}} \overset{(2.22)}{\approx} 0.48\ \mathrm{A} \quad \rightarrow i_{\mathrm{CI},1} - i_{\mathrm{CI},2} \approx 0.96\ \mathrm{A}, \tag{2.28}$$

From the above equation, it can be deduced that an error in the duty-cycle of just $\Delta\delta = 0.05\%$, leading to an average deviation in the bridge-leg voltages of 175 mV, results in an offset of the bridge-leg currents of nearly 1 A! This demonstrates a high sensitivity of the average bridge-leg currents on asymmetries in the bridge-legs for converters with small winding resistances and connection and / or parasitic component resistances, which have to be ensured in order to assure a high power conversion efficiency.

Remark: Assuming ideal switching, i.e. $\Delta\delta = 0$, and equal power semiconductor on-state voltage drops of both bridge-legs, a difference in the parasitic ohmic resistances $R_{\mathrm{w},1}$ and $R_{\mathrm{w},2}$ would also lead to an offset of the bridge-leg currents according to (2.18).

The longitudinal and transverse currents i_{LC} and i_{TC} as well as the voltages v_{LC} and v_{TC} are shown in **Fig. 2.14(c)**. The frequency of the longitudinal components is twice the switching frequency $f_{\mathrm{s,out}}$ of the bridge-legs due to the magnetic coupling of the two bridge-legs by the CI. The transverse components show a periodicity at $f_{\mathrm{s,out}}$. The magnetizing flux density in the CI core is plotted in **Fig. 2.14(d)** for open-loop and closed-loop control of the converter. Due to the offset in the two bridge-leg currents, also an offset in the magnetizing flux density

results. Accordingly, for a control scheme with only a single current controller, i.e. without active balancing of the bridge-leg currents, the CI must be designed with limited magnetic utilization of the core in order to prevent saturation.

Remark: Because of the good coupling ($k = 0.9987$) between the windings of the CI, the stray flux of both windings is negligible compared to the remaining flux in the core. Accordingly, the peak value of the magnetizing flux density is about equal to the maximum flux density in the core.

The spikes at the switching instants in Fig. 2.14(d) are resulting from current spikes due to the parasitic capacitance C_w between the windings [cf. **Fig. 2.16(a)**] and are not present in the actual (and not reconstructed) waveform of the magnetizing flux density. Due to the bifilar winding of the CI, C_w is increased, which causes larger current spikes and / or oscillations with a lower frequency than with other winding techniques. This is also recognized in [85, 95, 114, 115, 138].

The derivation of the equivalent circuit including the parasitics, as shown in Fig. 2.16(a), can be explained as follows. To model the capacitive energetic properties of a transformer or in this case of a CI, six capacitances are necessary (which can also have negative values) [139,140]. For a symmetrical coupling inductor as employed in Fig. 2.5, just one capacitance C_w, which represents the parasitic capacitance from winding 1 to winding 2, is sufficient to fully describe the capacitive energetic properties of the CI as depicted in Fig. 2.16(a). C_w can be determined from the input impedance $\underline{Z}_\mathrm{in}$ measurement of the CI shown in **Fig. 2.16(b)**. The first resonance frequency $f_{\mathrm{res},1} = 183.6$ kHz is determined by $2 \cdot L_\mathrm{TC} \approx 4 \cdot L$ and C_w. Consequently, the winding-to-winding capacitance C_w can by calculated as

$$C_\mathrm{w} = \frac{1}{\left(2 \cdot \pi \cdot f_{\mathrm{res},1}\right)^2 \cdot 2 \cdot L_\mathrm{TC}} \approx 191 \text{ pF}. \tag{2.29}$$

The second resonance occurs at $f_{\mathrm{res},2} = 18.6$ MHz and is determined, as explained in [141], by C_w and the inductance of the CI connecting wires, modeled with L'_σ in Fig. 2.16(a). **Fig. 2.17(d)** is a zoom of one switching transient. The oscillations at $f_{\mathrm{res},2} \approx 18.6$ MHz are damped by the relatively high resistance (ca. 11 Ω) at this frequency [cf. Fig. 2.16(b)]. In addition, considering Fig. 2.14(c), no current spikes are occurring in the longitudinal current $i_\mathrm{LC} = i_\mathrm{A1}$. Accordingly, C_w does not increase the noise level of the output voltage but may cause

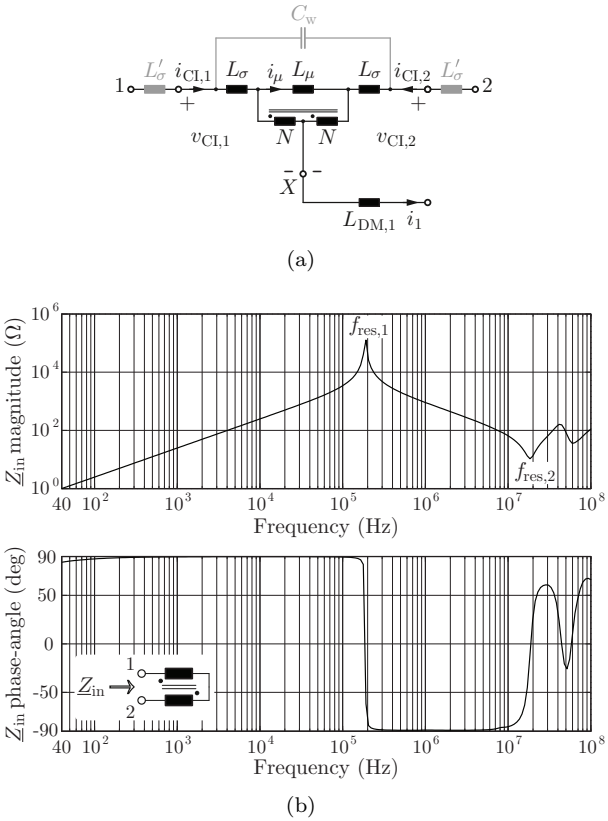
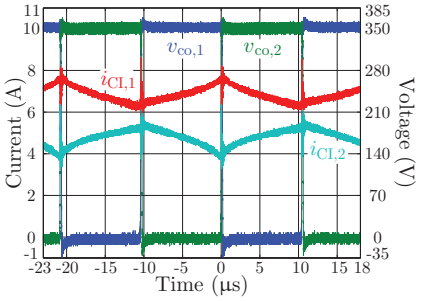


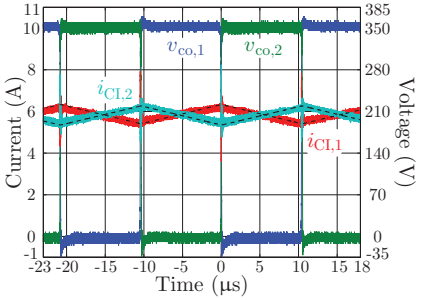
Figure 2.16: **(a)** Symmetrical equivalent circuit of the CI including the parasitic winding-to-winding capacitance C_w and the inductance in the connecting wires L'_σ and **(b)** measured (Agilent 4294A 40 Hz–110 MHz Precision Impedance Analyzer) input impedance $\underline{Z}_\mathrm{in}$ of the CI between 1 and 2.

higher capacitive switching losses of the converter bridge-legs.

Remark: The adverse impact of the CI's parasitic winding capacitance C_w could be diminished by splitting the filter inductor $L_{\mathrm{DM},1}$ into two individual inductors L_f [cf. Tab. 2.2, (b)] which are placed directly at the bridge-leg outputs. Alternatively, also the arrangement depicted in Tab. 2.2, (c) could be employed. Furthermore, no bifilar windings



(a)



(b)

Figure 2.17: Measurements for $V_{dc,n} = 700$ V with a nominal resistive load of $R_{A,load} = 15.9\ \Omega$ for a modulation index of $m_i = 0.5$: **(a)** bridge-leg output voltages $v_{co,1}$, $v_{co,2}$ and currents $i_{CI,1}$, $i_{CI,2}$ in open-loop; **(b)** $v_{co,1}$, $v_{co,2}$, $i_{CI,1}$, and $i_{CI,2}$ in closed-loop employing the control scheme depicted in Fig. 2.12 [the dashed-lines are the simulated bridge-leg currents and coincide with the measured waveforms]; **(c)** comparison between the magnetizing flux density in closed-loop $B_{\mu,closed\text{-}loop}$ and open-loop $B_{\mu,open\text{-}loop}$, computed with (2.17) based on $i_\mu = i_{TC} = (i_{CI,1} - i_{CI,2})/2$ [see remark in Fig. 2.14; the computed min. and max. peak values of ± 95.2 mT are indicated with dashed lines]; and **(d)** zoom of one switching transient in (b) employing the closed-loop control scheme. *Controller settings*: See Fig. 2.14.

could be used, which however would lower the coupling factor.

The measurements conducted on the hardware prototype for a modulation index of $m_i = 0.5$ are depicted in Fig. 2.17. The same conclusions hold as already stated in connection with Fig. 2.14. Additionally,

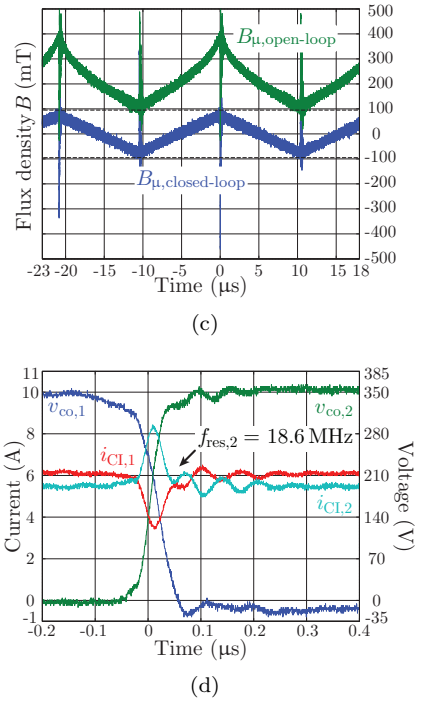
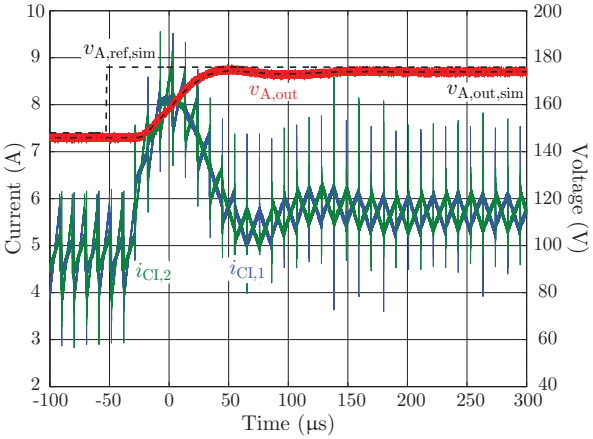


Fig. 2.17: Continued.

Fig. 2.17(c) illustrates that the CI core is already partially saturating for the converter operating in open-loop. This confirms the importance of a proper control of the bridge-leg currents $i_{\text{CI},1}$ and $i_{\text{CI},2}$ [e.g. with the control scheme depicted in Fig. 2.12].

In order to verify that the magnetizing flux density is bounded during transients, a step response was measured and is given in **Fig. 2.18(a)**. Since the peak-to-peak flux density in the CI core is the highest for a modulation index of $m_{\text{i}} = 0.5$, the voltage step is to an end level of 350 V/2 = 175 V. The step height is about 30 V. The figure verifies a very close agreement between the experimental and the simulation results.

The magnetizing flux during the output voltage transient is plotted in **Fig. 2.18(b)**. No overshoot or undershoot can be recognized in



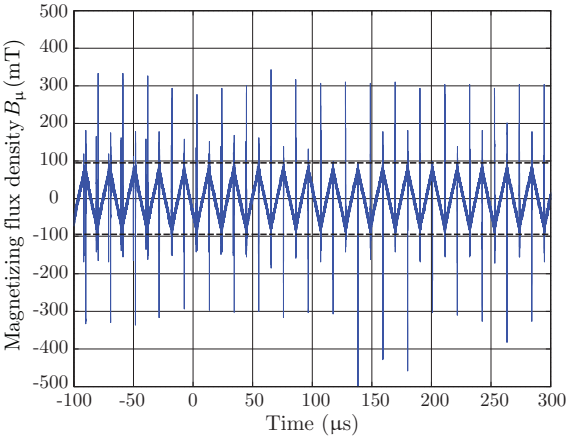
(a)

Figure 2.18: **(a)** Measurements for $V_{dc,n} = 700$ V and $R_{A,load} = 15.9\,\Omega$: step response $v_{A,out}$ of the closed-loop controlled system [cf. Fig. 2.12] to a step of 30 V to 175 V ($m_i = 0.5$) [dashed lines are simulated curves; the steady-state deviation between $v_{A,ref}$ and $v_{A,out}$ is nearly 2 V, which is less than 1% referred to 230 V]; and **(b)** corresponding magnetizing flux density B_μ in the CI core, computed with (2.17) based on $i_\mu = (i_{CI,1} - i_{CI,2})/2$ [see remark in Fig. 2.14; the computed min. and max. peak values of ±95.2 mT are given with dashed lines]. No overshoot/undershoot of B_μ occurs because of the fast current controllers. *Controller settings*: See Fig. 2.14.

the figure because the current controllers are fast enough. Fig. 2.18(b) also proves that the updates of the duty-cycle values are at the correct points in time [cf. Fig. 2.11(b)].

2.2.6 Summary

To increase the large-signal bandwidth of a 10 kW CVS module, i.e. to boost the frequency $f_{out,max}$ up to which the converter delivers full power, a higher CVS current-handling capability is required and hence each phase leg can be realized with two paralleled bridge-legs. According to literature and previous research, the volume of the *LC* output filter can be reduced if coupling inductors (CIs) are employed to magnetically couple the two bridge-leg outputs of each phase (cf. Fig. 2.5).



(b)

Fig. 2.18: Continued.

An equivalent circuit model of a symmetrical CI (self-inductances L and coupling factor k) with two equal leakage inductances $L_\sigma = L \cdot (1-k)$, a magnetizing inductance $L_\mu = 4 \cdot k \cdot L$ and an ideal transformer is derived [cf. Fig. 2.6(c)], which directly points out the coupling between the two bridge-legs and clearly shows that the two bridge-leg currents are theoretically identical for $L \to \infty$ and $k = 1$. In practice, this condition is approximatively given for $L \gg L_{\mathrm{DM},1}$ and $k \approx 1$, where $L_{\mathrm{DM},1}$ is the filter inductance of the first filter stage (cf. Fig. 2.5).

To analyze the influence of the CI on the power circuit, a separation of the bridge-leg output voltages and the CI currents into longitudinal and transverse (cross) components is introduced [cf. Fig. 2.9(b) and Fig. 2.9(d)]. The longitudinal voltage v_{LC} drives the longitudinal current i_{LC}, which is the current flowing to the output. The transverse voltage v_{TC} is responsible for the current i_{TC} which is flowing between the bridge-legs. From these considerations, it becomes very clear that both bridge-leg currents are equal if i_{TC} vanishes (hence $L \to \infty$ for $k \approx 1$). Nevertheless, the transverse current (excluding the part through the winding capacitance [cf. Fig. 2.16(a)]) is the magnetizing current $i_\mu = i_{\mathrm{TC}}$, that for $k \approx 1$ determines the maximum flux density amplitude in the CI core.

The CI is designed to achieve a good core utilization and thus the magnetization should be symmetrical. In order to avoid saturation of the CI core in all operating conditions, the following stationary and dynamic conditions must be satisfied:

- Asymmetries in the circuit may lead to an additional transverse current i_{TC} and hence to an offset of the CI core flux density and / or to a higher flux density peak value, if no direct control of the bridge-leg currents is provided. To guarantee a stationary symmetrical flux density, an I-type controller can be employed. During transients, the current controllers must be fast enough to avoid an overshoot/undershoot of the CI magnetizing flux density [cf. Fig. 2.18(b)]. Therefore, PI current controllers are potentially required.

- However, as the current measurements and the processing of the measurement values are not ideal, despite the current control, possibly a difference between the average (low-frequency) values of the two bridge-legs currents occurs. This difference leads again to a supplementary transverse current $i_{\mathrm{TC,lf}}$ and therefore to an increase of the peak flux density. As these inaccuracies cannot be compensated, the design of the CI has to consider a sufficient margin for the flux density in order to prevent saturation.

- Finally, the updates of the references of the PWM module must be performed at specific points in time. If the update always is at the beginning or at the end of a pulse half period (where the carriers reach either 0 or 1), the volt-seconds remain balanced and consequently the magnetizing flux density stays symmetrical [cf. Fig. 2.11(b)].

To limit the transverse peak-to-peak current ripple to low values, it is advantageous to select the self-inductance L of the CI as high as possible. The size of the CI and / or its losses are limiting the maximum L; however, two additional constraints need to be considered for a CI. Firstly, an increasing L augments the leakage inductance and hence may produce an adverse effect on the output voltage dynamics. Secondly, a larger L also results in an increased magnetizing inductance; thus errors in the current measurement setup, which occur in any real power electronic system, could saturate the CI's core more easily.

Extensive single-phase measurements have been conducted on a three-level T-type voltage source converter and a two-stage LC output filter with a CI. The experimental results prove the theoretical analysis as well as the modeling and are showing a very close match with the circuit simulations. Moreover, the measurements demonstrate the importance of a proper control of both bridge-leg output currents and / or CI winding currents (cf. Figs. 2.17 and 2.18). For the T-type converter, an error $\Delta\delta$ in the duty-cycle of the bridge-legs leads to a low-frequency transverse current $i_{\mathrm{TC,lf}}$ [cf. (2.22) and (2.24)]. For the considered hardware, a time difference of 10 ns between the switching instants of the bridge-legs leads to an error in the effective duty-cycle of $\Delta\delta \approx 0.05\%$. This error causes an average difference of 175 mV between the bridge-leg output voltages, which results for $\delta = 0.25$ in a difference of the CI winding currents of 1.1 A. This clearly demonstrates a high sensitivity of the average bridge-leg currents concerning asymmetries of the converter.

Finally, it should be noted that a good magnetic coupling between the bridge-legs, i.e. $k \approx 1$, results in a relatively large parasitic capacitance between the windings of the CI [cf. Fig. 2.16(a)]. In the case at hand, measurements showed that this leads to oscillations in the transverse current i_{TC} at the switching instants, which are not transferred to the filter output though.

The scientific work as presented in this section is published in [142] (see also "List of Publications" on page 337).

3

Converter Module Structure and Design

In the previous chapter, a three-level T-type bridge-leg topology with SiC MOSFETs and a switching frequency of 48 kHz are determined to be most suitable for the realization of the CVS. Based on these results, this part now determines the input and output stage's converter topologies, designs the EMI input and output filters, and develops the control structures for both stages.

The chapter is structured as follows: because the AC voltage source needs to be highly flexible regarding the possible connection of various types of loads, e.g. single- or balanced / unbalanced three-phase loads, each output phase is operated individually and a fourth output leg is employed as motivated in Section 3.1. With this finding the most suitable output filter topology and the output voltage control structure is identified in Section 3.2 and Section 3.3, respectively, based on single-phase considerations and by means of multi-objective optimizations such as the ρ–η Pareto Front (PF) trade-off analysis. The insights gained from the two mentioned sections are then applied to the three-phase four-leg realization of the output stage in Section 3.4. Section 3.5 completes the chapter by designing the input stage, especially focusing on a low-volume realization of the EMI input filter.

3.1 Decoupling of the Output Phases

As mentioned in Chapter 1, the CVS is intended to be used in a large number of different applications and hence it needs to be highly flexible

regarding the connection of possible loads. This includes linear loads, e.g. DC, single-phase AC, and three-phase AC (balanced and unbalanced) resistive and / or inductive loads [3, 8, 11, 30, 31], and non-linear loads, e.g. constant power loads [32, 33], diode rectifiers [3, 6, 30], and single-phase triac loads [8].

Single-phase loads could be connected between two output phase terminals of the CVS, however, the handling of unbalanced and / or non-linear three-phase loads requires to connect the load star-point back to a neutral terminal N of the CVS to allow a non-zero sum of the output phase currents flowing. This can be achieved by employing either a three-phase plus neutral conductor [143–147] or a three-phase four-leg converter [145, 146, 148–154] as depicted in **Fig. 3.1**.[1] The latter realization of the output stage converter [cf. **Fig. 3.1(b)**] adds complexity to the CVS, i.e. it requires four more switches and gate driving units as well as additional filter elements and current / voltage measurement and processing units. However, compared to the three-phase plus neutral conductor converter [cf. **Fig. 3.1(a)**] the extra bridge-leg allows reducing the capacitance value and hence the size of the DC link capacitors (for the same peak-to-peak voltage ripple) [145, 150, 151, 153]. Furthermore, it also achieves a higher DC link voltage utilization for the generation of three-phase symmetrical voltage systems applied to the load, i.e. the maximum phase load voltage amplitude is increased by 15.5% from $V_{\mathrm{dc}}/2$ to $V_{\mathrm{dc}}/\sqrt{3}$ [145, 150, 151, 153].[2] This can be seen by considering Fig. 3.1(b) and making a distinction between the output voltages $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$, $v_{\mathrm{C,out}}$, and $v_{\mathrm{N,out}}$ of the phases and the neutral (fourth) leg, respectively, and the load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ of the phases, i.e. the voltages applied to the load. The load voltages are measured between the output terminals of the phases A, B, C and the neutral terminal N and are built by the difference between the output voltages $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$, and $v_{\mathrm{C,out}}$ of the phases and the output voltage of the neutral leg $v_{\mathrm{N,out}}$, i.e. $v_{\mathrm{A,load}} = v_{\mathrm{A,out}} - v_{\mathrm{N,out}}$ for phase A. This clearly demonstrates that $v_{\mathrm{N,out}}$ acts as a zero-sequence voltage component of $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$, and $v_{\mathrm{C,out}}$, which allows increasing the range of the load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ and reducing the maximum bridge-leg output current ripples. For the aforementioned

[1] Exemplary the load star-points are grounded in Fig. 3.1, which, however, may not be the case for all loads considered in this work.

[2] It should be noted, that for a simultaneously grounded mains and load star-points the fourth leg cannot maximize the range of the phase load voltages (cf. Chapter 4).

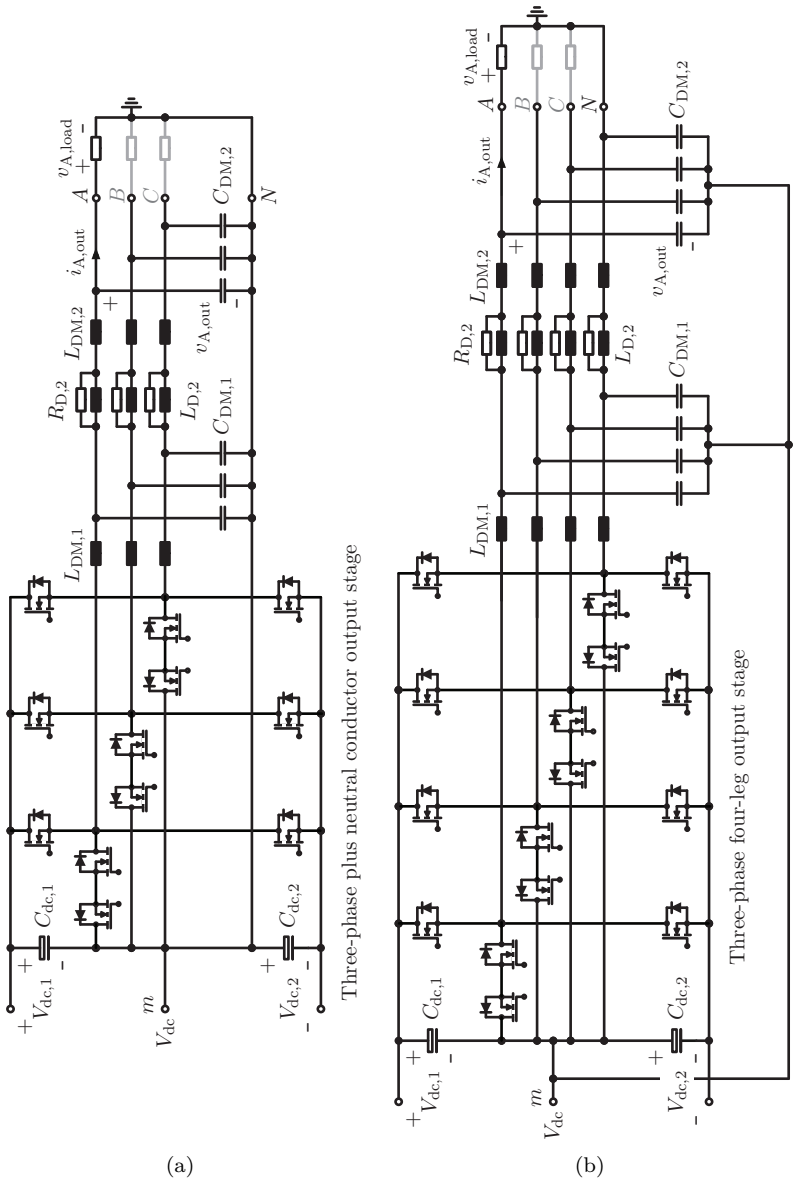


Figure 3.1: Realization of the output stage with **(a)** a three-phase plus neutral conductor and **(b)** a three-phase four-leg voltage source inverter.

reasons and because the fourth, i.e. neutral, bridge-leg adds a degree of freedom in the load voltage generation [145], the three-phase four-leg option is preferred to the three-phase plus neutral conductor realization of the output stage.

The modulation and control schemes for such four-leg converters, often proposed in literature, consider the generation of the output voltages as one unit. Space Vector Modulations (SVMs) using a three-dimensional representation of the voltage vectors and its realization with carrier-based PWM is proposed in [145,146,149,150] and [151], respectively. For the control structures, coordinate transformations using a static or rotating reference frame, representing the four-wire system as three single-phase systems, are employed [144,149,153,154].

However, because the common basis of all these approaches are three-phase sinusoidal voltages, they are not suitable and / or easily applicable for load voltage references that can have any programmable waveform, including DC components. It is reminded that the CVS can be used in a large number of different applications with diverse loads, including individual loads for the phases A, B, and C. In addition, to test power electronic equipment in laboratory or according to international standards, the CVS may need to generate individual harmonics and / or transients in the load voltage of each phase [3–5,155].

Thus, to achieve maximum flexibility for the generation of the load voltages, the voltages between the phase terminals A, B, C and the neutral terminal N [Fig. 3.1(b)] are controlled independently [156], which requires that the output filter is realized without any inductive and capacitive elements coupling and cross-coupling the phases, respectively. A minimum interaction between the phases and the neutral leg is obtained for the fully symmetrical filter structure given in Fig. 3.1(b), where, in anticipation of the results obtained in Section 3.2, a four-line two-stage LC filter is shown. Because $v_{\mathrm{N,out}}$ is common to the generation of all output voltages, each phase can still be considered to be operated individually.

3.2 Output Stage – Single-Phase Filter Design

The selected output stage topology of the CVS is shown in Fig. 3.1(b), where equal DC link voltages $V_{\mathrm{dc},1} = V_{\mathrm{dc},2} = V_{\mathrm{dc}}/2$ are assumed (cf. Section 4.1). As given in Chapter 1 and further explained in Section 3.2.1, the system needs to comply with specifications regarding qualities and transient responses of all three load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ and needs to achieve the efficiency specified at the nominal operating point (cf. **Tabs. 3.1** and **3.2**). Because the CVS actually is a switch-mode power supply, the amplitudes of the harmonics in the switched bridge-leg output voltages [e.g. v_{A0} in **Fig. 3.2**] need to be attenuated by an output filter to comply with the given requirements. In the simplest case, the output filter is implemented as a single-stage LC filter according to **Fig. 3.2(a)**. The component values used in the LC filter are restricted, not only in their minimum values, to fulfill the output voltage quality requirements, but also in their maximum values, to satisfy the dynamic specifications.

A literature survey reveals numerous publications on the design of the output filter with boundary conditions defined by specifications, which typically deal with only one aspect, such as conducted EMI [157, 158], output voltage ripple [159, 160], or current ripple [155, 161, 162]. For the case at hand, however, multiple requirements need to be satisfied. For this purpose, the concept of the Design Space (DS), first employed in [163] to design a single-stage LC filter for a 20 W synchronous buck converter in order to comply with static and dynamic output voltage regulation specifications, is considered most promising. The DS concept is based on multiple criteria that are derived from all dynamic and static specifications. In case of [163], these criteria define bounds on the values of L and C, which can be represented by boundary curves in an L–C plane. The intersection set of all boundary curves builds the DS. Thus, the strength of the DS approach is that all combinations of filter parameter values which comply with all specifications are identified. Another publication related to the DS concept details the implications of changing specifications and / or requirements on the DS calculated for a 0.6 W buck converter including PWM delays and filter resonances in voltage mode control [164]. Both references [163, 164] are limited to single-stage LC filters and do not detail any further optimization of the filter using the calculated DS, e.g. with respect to power

Table 3.1: Electrical specifications of the power converter considered for the realization of the output stage of the CVS. To generate an output voltage with high dynamics in the range of [±350 V], the DC link voltage is increased from $V_{\mathrm{dc,n}} = 700$ V to $V_{\mathrm{dc,max}} = 800$ V. Otherwise, $V_{\mathrm{dc,n}}$ is preferred to ensure a high efficiency of the CVS.
[1)] line-to-neutral; [2)] The output voltage's large-signal bandwidth of one phase-leg is limited to 300 Hz in order not to exceed the converter's current rating (cf. Section 3.3.3). To achieve the minimal required large-signal bandwidth of 1 kHz (cf. Tab. 1.1), f_{out} can be enlarged by paralleling bridge-legs as discussed in Section 2.2. [3)] In a first step, it is assumed that the total losses of the CVS are equally distributed to the input and output stages, i.e. $\eta_{\mathrm{out,n}} = \sqrt{\eta_{\mathrm{tot,n}}} = \sqrt{95\%} \approx 97.5\%$ (cf. Tab. 1.1).

Nominal output power, $P_{\mathrm{out,n}}$	10 kW
Nominal rms output voltage, $V_{\mathrm{A,out,n}}$ [1)]	230 V
Nominal peak output voltage, $V_{\mathrm{A,out,n,pk}}$ [1)]	325 V
Max. peak output voltage, $V_{\mathrm{A,out,max,pk}}$ [1)]	350 V
Nominal DC link voltage, $V_{\mathrm{dc,n}} = V_{\mathrm{dc,1,n}} + V_{\mathrm{dc,2,n}}$	700 V
Max. DC link voltage, $V_{\mathrm{dc,max}}$	800 V
Nominal rms output current, $I_{\mathrm{A,out,n}}$	14.5 A
Nominal peak output current, $I_{\mathrm{A,out,n,pk}}$	20.5 A
Output frequency, f_{out}	$0 - 300$ Hz [2)]
Output stage switching frequency, $f_{\mathrm{s,out}}$	48 kHz
Nominal efficiency, $\eta_{\mathrm{out,n}}$	$\geq 97.5\%$ [3)]

density or efficiency.

Subsequent to the identification of the DS, the filter can be optimized, e.g. by means of multi-objective optimization with respect to maximal power density, maximal efficiency, and / or minimal cost [165]. Two main approaches for multi-objective optimization exist: aggregate function techniques, which summarize all considered objective functions in a single objective function (for this the relative importance of all objective functions needs to be known a priori) and Pareto Front (PF) techniques, which do not weight the different objectives in advance [166]. In the present work the PF method is used, since high power density and high total efficiency are simultaneously desired and the relative importance of the two objective functions is not a priori known. Literature related to engineering specific multi-objective PF optimizations

Table 3.2: Required properties of the CVS.

Output voltage quality	$\mathrm{THD_v} < 2.5\%$ (cf. IEEE 1547 [53])
Output voltage slew rate	$SR \geq 203\ \mathrm{V/ms}$
Max. transient output voltage dip $\Delta v_{\mathrm{A,out}}$ due to a stepwise output current change $\Delta i_{\mathrm{A,out}}$	$\left\lvert \frac{\Delta v_{\mathrm{A,out}}}{\Delta i_{\mathrm{A,out}}} \right\rvert \leq \frac{28\ \mathrm{V}}{5\ \mathrm{A}} = 5.6\ \Omega$
Limited filter capacitor reactive power demand	$Q_{\mathrm{cap,max}} \leq 10\% \cdot \frac{P_{\mathrm{out,n}}}{3} = 333\ \mathrm{VA}$
Conducted EMI	CISPR 11, Class A [36]

commonly proposes the following three approaches: first, heuristic genetic / evolutionary algorithms [166–168]; second, algorithms with guaranteed convergence to the Pareto-optimal solution [169–171]; and third, iterative grid search algorithms with an appropriate discretization of the variables [172,173]. Because it is not guaranteed that the first category of heuristic algorithms finds Pareto-optimal solutions [174], i.e. minimal volume and / or maximum efficiency, the two latter categories are favored. Among these, the grid search algorithm is selected due to its numerical robustness and simplicity of implementation.

Remark: The DS concept is not limited to the design of *LC* filters. In [175], for example, the $\mathrm{ESR_C}$-C DS of the output capacitor of a fast switching (530 kHz) 9 W buck converter is calculated to meet constraints regarding the output voltage and the peak-to-peak inductor current ripples for different operating points. Furthermore, the DS concept is applied to controller designs [176,177], to outlay advanced digital low-pass filters [178], to devise linear compensators [179], and to assess the proper functioning of Random-Access Memory (RAM) cells [180].

In the present section a complete design procedure is proposed for a two-stage *LC* output filter, which is based on the DS concept and includes a final filter optimization with respect to power density ρ, and / or efficiency η, using the ρ–η PF. Furthermore, experimental results are presented. In the following, the requirements defined for the AC source output stage are described in Section 3.2.1. Section 3.2.2 discusses the implications of these specifications on the filter DS and details equations for the related constraints, which confine the search domain in the parameter space for any final filter design procedure. From all filter

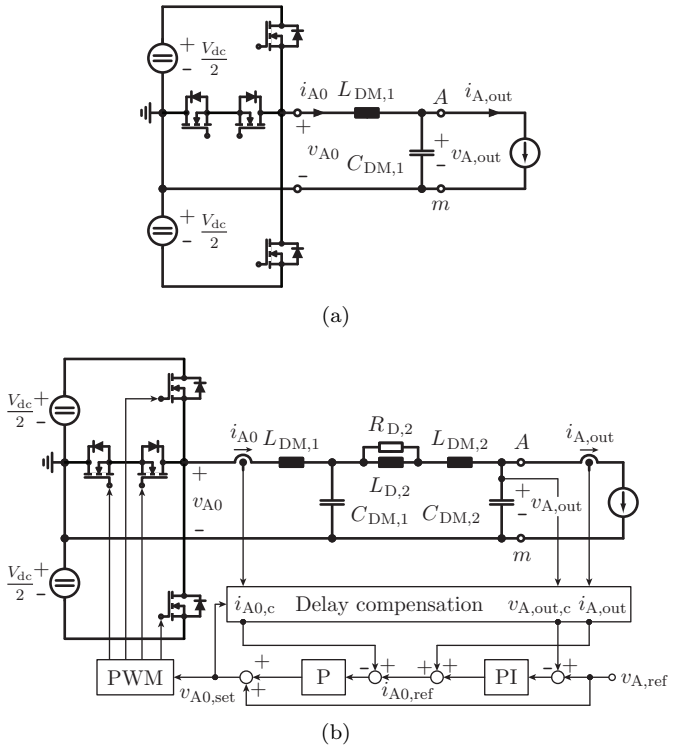


Figure 3.2: **(a)** Simplified single-phase equivalent circuit of the CVS for a single-stage LC output filter and **(b)** a two-stage LC output filter with a series $R_{D,2}L_{D,2}$ damping branch of the second filter stage. The load is represented as a current source. In (b), the control scheme employed in Section 3.2.4 is added to the equivalent circuit. It consists of an outer voltage control loop for $v_{A,out}$, with feedforward of the reference output voltage $v_{A,ref}$, an inner current control loop for i_{A0}, with feedforward of the load current $i_{A,out}$, and a sampling plus PWM delay compensation [181] to achieve a satisfactory control performance (cf. Section 3.2.4).

designs with component values in the DS, the final output filter is determined from a ρ–η PF analysis in Section 3.2.3. Finally, Section 3.2.4 verifies the calculated outcomes by means of experimental results for this two-stage LC filter.

3.2.1 Specifications of the AC Source

Fig. 3.1(b) depicts the output stage of the CVS, which is a four quadrant, three-phase four-leg, three-level T-type voltage source converter. As well-founded in Section 3.1, each phase of the output stage is operated individually. In a first step, the interaction between one leg and the others is neglected to simplify the design of the output filter in this section and later on to ease the realization of the output voltage control structure in Section 3.3, and hence the three-phase plus neutral conductor converter in Fig. 3.1(a) is considered. In a second step, the outlaid output filter and output voltage control structure are then applied to the three-phase four-leg converter as discussed in Section 3.4.

Accordingly, the filter design considerations in this section can be limited to a single-phase equivalent circuit [cf. Fig. 3.2(a)] and only phase A is considered in the following. The basic electrical specifications of the power converter shown in Fig. 3.1(a) are listed in Tab. 3.1, and as elaborated in Section 2.1 a switching frequency of 48 kHz is selected to achieve the dynamic performance requirements.

Furthermore, the output frequency range is $0 - 300$ Hz (cf. Section 3.3.3 and Tab. 3.2), with the main focus on $f_{\text{out}} = 50$ Hz since in many applications the CVS is used for emulating a 50 Hz grid. Tab. 3.2 lists additional requirements, which are summarized below.

Output voltage quality requirements are differently specified for sinusoidal and arbitrary output voltage waveforms: for sinusoidal output voltages, a Total Harmonic Distortion of $\text{THD}_\text{v} < 2.5\%$ (cf. IEEE 1547, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems [53]) is specified; for arbitrary output voltage waveforms, a minimum average slew rate, $SR_{\min}$ is defined. In this context, the *response of the converter to a reference voltage step* of $\Delta v_{\text{ref}} = 10\% \cdot V_{\text{out,n,pk}} = 32.5$ V is required to be completed after $t_{\text{step}} = 160$ µs [cf. **Fig. 3.3**]. This requirement is summarized using a minimum average slew rate:[3]

$$SR_{\min} = \frac{10\% \cdot 325 \text{ V}}{160 \text{ µs}} = 203 \text{ V/ms}. \tag{3.1}$$

[3]The definition of the average slew rate adopted in this section is different from the definition of the slew rate known from operational amplifiers (OpAmps). For OpAmps the slew rate is defined as the "maximum rate at which the output voltage of the OpAmp can change", i.e. $(\text{d}v/\text{d}t)_{\max}$, which is typically determined for a full-scale large-signal input voltage step [182].

Accordingly, with $SR_{\min}$, the converter can generate a sinusoidal output voltage reference with a frequency of 1 kHz and an amplitude of 32.3 V.[4] With this, and according to the results of the derivation presented in Section 3.2.2, a small signal bandwidth of the closed output voltage control loop of approximately 4 kHz is estimated, i.e. the CVS is capable of tracking a reference voltage which leads to an output voltage waveform that does not exceed the slew rate specified in (3.1) and contains frequency components up to 4 kHz.

An output voltage transient provoked by a step change of the voltage reference, $v_{\mathrm{A,ref}}$, generates also a bridge-leg output current transient, which, depending on the output current, possibly drives the converter in its current limitation. This would then lead to a nonlinear behavior of the controlled converter, which is undesired. Thus, for the slew rate calculation, it is assumed that the CVS can accordingly increase its output voltage without running into the current limitation. This is experimentally verified in Section 3.2.4, where the required increase of the bridge-leg output current is roughly 4 A.

The *maximum transient output voltage dip*, $\Delta V_{\mathrm{A,out,max}}$, that occurs *due to a stepwise output current change* $\Delta I_{\mathrm{A,out}}$, can be characterized by means of an impedance

$$Z_{\mathrm{step,max}} = \left| \frac{\Delta V_{\mathrm{A,out,max}}}{\Delta I_{\mathrm{A,out}}} \right| . \tag{3.2}$$

According to predefined requirements, $\Delta V_{\mathrm{A,out}}$ must not exceed 28 V (8% of $V_{\mathrm{A,out,max,pk}}$) for $\Delta I_{\mathrm{A,out}} = 5$ A, which yields $Z_{\mathrm{step,max}} = 5.6\ \Omega$ (cf. **Fig. 3.4**).

To limit the current stress on the components of the power circuit, the *maximum reactive power demand of all filter capacitors*, $|Q_{\mathrm{cap,max}}|$, must not exceed 10% of the nominal output power, $P_{\mathrm{out,n}}$, at nominal operating conditions, i.e. at $V_{\mathrm{out,n}} = 230$ V and $f_{\mathrm{out}} = 50$ Hz.

Furthermore, for preventing a disturbance of sensitive loads supplied by the CVS, the *levels of conducted EMI noise emissions* are restricted according to CISPR 11, Class A, i.e. in the frequency range between 150 kHz and 500 kHz, the conducted emissions need to be less than 79 dBµV and between 500 kHz and 30 MHz less than 73 dBµV [36].

[4] The $|\mathrm{d}v/\mathrm{d}t|$ of a sinusoidal function with amplitude V_{sig} and frequency f_{sig} is maximal at its zero crossings and can be calculated as $2 \cdot \pi \cdot f_{\mathrm{sig}} \cdot V_{\mathrm{sig}}$, which gives 203 V/ms for $V_{\mathrm{sig}} = 32.3$ V at $f_{\mathrm{sig}} = 1$ kHz. Accordingly, to change the output voltage by 32.3 V with an average rate of change of 203 V/ms leads to a required time interval of $\Delta t = t_{\mathrm{step}} = 32.3\ \mathrm{V}/203\ \mathrm{V/ms} = 159.1\ \mu\mathrm{s} \approx 160\ \mu\mathrm{s}$.

3.2.2 Design Space Constraints

In order to fulfill the requirements listed in Tab. 3.2 with the described inverter, a single-stage LC output filter, as shown in Fig. 3.2(a), could be considered at first. This output filter serves as an accompanying example throughout this part of the thesis, for which the dimensioning based on the DS approach is subsequently elaborated.

The parameters for the filter DS calculation include all possible values of all filter components and all possible values of further inverter parameters which are linked to the filter design, e.g. the switching frequency $f_{\mathrm{s,out}}$. For a single-stage LC filter four such parameters, i.e. $L_{\mathrm{DM,1}}$, $C_{\mathrm{DM,1}}$, $f_{\mathrm{s,out}}$, and V_{dc}, exist, which are restricted by

$$L_{\mathrm{DM,1}} > 0,\ C_{\mathrm{DM,1}} > 0,\ f_{\mathrm{s,out}} > 0, \text{ and } V_{\mathrm{dc}} > 0. \tag{3.3}$$

In the rest of the section, the switching frequency $f_{\mathrm{s,out}}$ is kept constant at 48 kHz and the DC link voltage is fixed to either $V_{\mathrm{dc}} = 700\,\mathrm{V}$ or $V_{\mathrm{dc}} = 800\,\mathrm{V}$ for each requirement. Accordingly, a two dimensional parameter space spanned by $L_{\mathrm{DM,1}}$ and $C_{\mathrm{DM,1}}$ is obtained for the single-stage LC output filter, shown in Fig. 3.2(a).

The given CVS specifications and requirements (discussed in Section 3.2.1 and listed in Tabs. 3.1 and 3.2), however, impose five restrictions on the values of $L_{\mathrm{DM,1}}$ and / or $C_{\mathrm{DM,1}}$. The calculation of the filter DS further includes a sixth constraint that limits the peak-to-peak ripple of the bridge-leg output current to prevent high-frequency winding and core losses in $L_{\mathrm{DM,1}}$. All six constraints are detailed below.

It is to be noted that, in this section, a constant output frequency f_{out} of 50 Hz is specified. If generation of output frequencies greater than 50 Hz would be required, a frequency dependent current derating of the CVS and / or one additional constraint needs to be considered. With these measures, the impacts of increased reactive currents in the filter capacitors at higher output frequencies on the current delivered by the power stage are taken into account. In this context, the need for a high output frequency accompanies the need for a high switching frequency: it can be shown that, in case of a single-stage LC filter, the ratio $f_{\mathrm{s,out}}/f_{\mathrm{out}}$ needs to satisfy

$$\frac{f_{\mathrm{s,out}}}{f_{\mathrm{out}}} = \frac{\pi}{4} \cdot \frac{k_{\mathrm{i}}/k_{\mathrm{v}}}{Q/P}, \tag{3.4}$$

where k_{i} denotes the ratio of maximum peak-to-peak inductor current ripple to peak output current, k_{v} the ratio of maximum peak-to-peak

output voltage ripple to peak output voltage, and Q/P denotes the specific reactive power demand of the filter. With $k_\mathrm{i} = 60\%$, $k_\mathrm{v} = 2\%$, and $Q/P = 10\%$, the switching frequency needs to be at least 236 times the output frequency, or, for $f_\mathrm{s,out} = 48$ kHz, a maximum output frequency $f_\mathrm{out,max}$ of approximately 200 Hz results. It is noted that $f_\mathrm{out,max}$ can be increased by paralleling bridge-legs (cf. Section 2.2).

Output Voltage Slew Rate

According to Section 3.2.1, the minimum average slew rate, SR_min, that must be achieved with the output filter is equal to 203 V/ms. This subsection derives the inequality for L and C that corresponds to this slew rate requirement. To simplify the analysis, idealized voltage control of the CVS is assumed, i.e. the controller applies the maximum possible voltage to the input of the filter network until the required filter output voltage is obtained, such that the maximum possible rate of change of the output voltage is achieved.

If an input voltage step $\Delta v_\mathrm{A0} > 0$ is applied to a single-stage LC filter [cf. Figs. 3.1(a) and 3.2(a)], the current through the filter inductor increases and subsequently the capacitor voltage, i.e. output voltage, starts to change as well. The presented result considers the response to a positive input voltage step (the bridge-leg constantly applies $+V_\mathrm{dc}/2$ until the output voltage reaches its new reference value) and neglects the implication of the changing capacitor voltage $v_\mathrm{A,out}$ on the inductor current i_A0, which, for $m_\mathrm{i} := v_\mathrm{A,out}/\frac{V_\mathrm{dc}}{2}$, gives

$$\Delta v_\mathrm{A,out} \approx \frac{V_\mathrm{dc}}{4 \cdot L_\mathrm{DM,1} \cdot C_\mathrm{DM,1}} \cdot (1 - m_\mathrm{i}) \cdot \Delta t^2. \tag{3.5}$$

[thin gray line labeled with "cf. (3.5)" in Fig. 3.3]. Accordingly, the idealized slew rate is

$$\begin{aligned} SR_0(\Delta v_\mathrm{A,out}) &= \sqrt{\frac{\Delta v_\mathrm{A,out}^2}{\Delta t^2}} \\ &= \sqrt{\frac{V_\mathrm{dc}}{4 \cdot L_\mathrm{DM,1} \cdot C_\mathrm{DM,1}} \cdot (1 - m_\mathrm{i}) \cdot \Delta v_\mathrm{A,out}}. \end{aligned} \tag{3.6}$$

The slew rate decreases for increasing modulation index m_i, since the voltage applied to the filter inductor decreases. Thus, the minimum

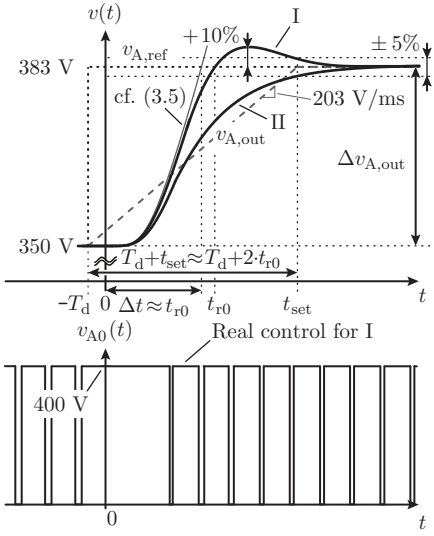


Figure 3.3: Visualization of the CVS' output voltage dynamic behavior resulting for idealized control (thin gray line labeled with "cf. (3.5)"; basis for the slew rate calculation) and resulting for a real control (solid lines). Options I and II of the dynamic behavior of $v_{\mathrm{A,out}}$ represent an underdamped and overdamped system, respectively. The voltage ripple is neglected for the depicted waveforms.

slew rate occurs for the maximum modulation index (cf. Tab. 3.1)[5]

$$m_{\mathrm{i,max}} = \frac{V_{\mathrm{A,out,max,pk}}}{V_{\mathrm{dc,max}}/2} = \frac{350\ \mathrm{V}}{400\ \mathrm{V}} = 0.875. \tag{3.7}$$

In a real system the slew rate calculated with (3.6) may not be achievable, in particular due to the time delay of the employed pulse width modulator and the limited control bandwidth of the closed output voltage control loop. The pulse width modulator is operated with double-update-mode and, thus, causes a time delay of $T_{\mathrm{d}} = 1/(2 \cdot f_{\mathrm{s,out}})$ $= 10.4\ \mu\mathrm{s}$. The limited bandwidth of the closed voltage control loop is

[5] $m_{\mathrm{i,max}}$ is obtained for $v_{\mathrm{A,out}}(t) = V_{\mathrm{A,out,max,pk}}$ and $V_{\mathrm{dc}} = V_{\mathrm{dc,max}}$, since the CVS' DC link voltage is increased to $V_{\mathrm{dc}} = 800$ V in case an output voltage in the range of [±350 V] must be generated with a high dynamic.

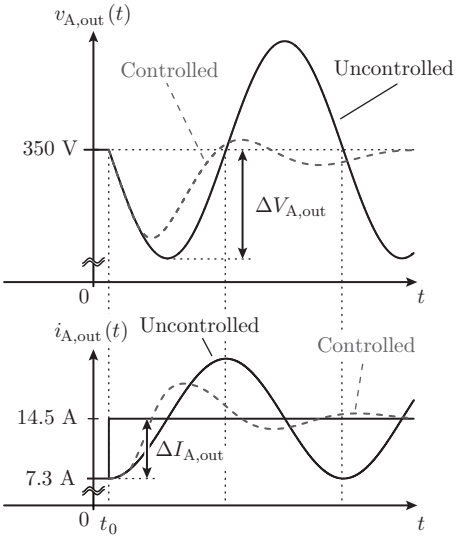


Figure 3.4: Illustration of the transient output voltage dip for a single-stage filter with $L_{\mathrm{DM},1} = 154\ \mu\mathrm{H}$ and $C_{\mathrm{DM},1} = 4.6\ \mu\mathrm{F}$ in case of $\Delta I_{\mathrm{A,out}} = 7.2\ \mathrm{A}$ resulting for an uncontrolled (solid line) and controlled output voltage (dashed line). The voltage ripple is neglected for the depicted waveforms.

considered based on the assumption that the required change of the output voltage, $\Delta v_{\mathrm{A,out}}$, is performed within the settling time $t_{\mathrm{set}} > t_{\mathrm{r0}}$ (cf. Fig. 3.3, for $t \geq t_{\mathrm{set}}$, $v_{\mathrm{A,out}}$ remains in a $\pm 5\%$ tolerance band of $v_{\mathrm{A,ref}}$) and that $t_{\mathrm{set}}/t_{\mathrm{r0}} \approx 2$ applies, which is justified based on a comparison of the dynamic characteristic of the CVS with a second order low pass filter with a damping ratio of $0.6 \leq \zeta \leq 1.2$. The solid black lines in Fig. 3.3, labeled I and II, denote the expected output voltage transients of the controlled system for $\zeta = 0.6$ (underdamped) and $\zeta = 1.2$ (overdamped), respectively, and include the time delay T_{d}. With this, the effective slew rate in presence of closed loop voltage control, SR (dashed line in Fig. 3.3), can be related to the required rise time of the filter, t_{r0},

$$SR = \frac{\Delta v_{\mathrm{A,out}}}{T_{\mathrm{d}} + t_{\mathrm{set}}} \approx \frac{\Delta v_{\mathrm{A,out}}}{T_{\mathrm{d}} + 2 \cdot t_{\mathrm{r0}}} = 203\ \mathrm{V/ms}, \tag{3.8}$$

which, for $\Delta v_{\mathrm{A,out}} = 10\% \cdot 325\ \mathrm{V} = 32.5\ \mathrm{V}$ [cf. (3.1) in Section 3.2.1],

yields

$$t_{\mathrm{r0}} = \frac{1}{2} \cdot \left(\frac{\Delta v_{\mathrm{A,out}}}{SR} - T_{\mathrm{d}} \right) \approx 75\ \mu\mathrm{s}. \tag{3.9}$$

Thus, the filter is required to realize an idealized slew rate, SR_0 [cf. (3.6) for $\Delta t = t_{\mathrm{r0}}$], of

$$SR_0 = \frac{\Delta v_{\mathrm{A,out}}}{t_{\mathrm{r0}}} \approx 434\ \mathrm{V/ms}. \tag{3.10}$$

Furthermore, (3.9) allows for the estimation of the achievable small-signal bandwidth of the closed voltage control loop, $f_{\mathrm{bw,ss}}$, according to [183],

$$f_{\mathrm{bw,ss}} \approx \frac{1.8}{2 \cdot \pi \cdot t_{\mathrm{r0}}} \approx 4\ \mathrm{kHz}. \tag{3.11}$$

Suitable values of $L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},1}$, for achieving the required minimum attainable filter slew rate, can be found with (3.6), (3.7), and (3.10) considering

$$SR_0 = 434\ \mathrm{V/ms} \leq \sqrt{\frac{V_{\mathrm{dc}}}{4 \cdot L_{\mathrm{DM},1} \cdot C_{\mathrm{DM},1}} \cdot \frac{1}{8} \cdot 32.5\ \mathrm{V}}. \tag{3.12}$$

Fig. 3.5 depicts the values of the maximum allowable filter inductances $L_{\mathrm{DM},1}$ that result for solving (3.12) for $L_{\mathrm{DM},1}$, i.e.

$$L_{\mathrm{DM},1} \leq \frac{V_{\mathrm{dc}}}{4 \cdot C_{\mathrm{DM},1}} \cdot \frac{32.5\ \mathrm{V}}{8 \cdot (434\ \mathrm{V/ms})^2} = L_{\mathrm{DM},1,\mathrm{max}}, \tag{3.13}$$

for $1\ \mu\mathrm{F} \leq C_{\mathrm{DM},1} \leq 30\ \mu\mathrm{F}$ (gray dashed line with label "Out. voltage slew rate"). The arrow points into the area where (3.12) is fulfilled. $L_{\mathrm{DM},1,\mathrm{max}}$ is directly proportional to the DC link voltage V_{dc} and inversely proportional to the filter capacitance $C_{\mathrm{DM},1}$.

An accurate value [instead of the simplified expression (3.6)] for the filter slew rate SR can be calculated with a numerical solver, by means of Laplace transformation. Fig. 3.5 compares $L_{\mathrm{DM},1,\mathrm{max}}$ obtained with the simplified [cf. (3.12), label "Approx."] and the accurate expressions [label "Exact"], respectively. The difference between the two lines results from the fact that the approximation assumes a constant voltage difference of $(1 - m_{\mathrm{i}}) \cdot V_{\mathrm{dc}}/2$ across the inductor $L_{\mathrm{DM},1}$ during the entire time interval Δt. In the real system, however, the voltage across

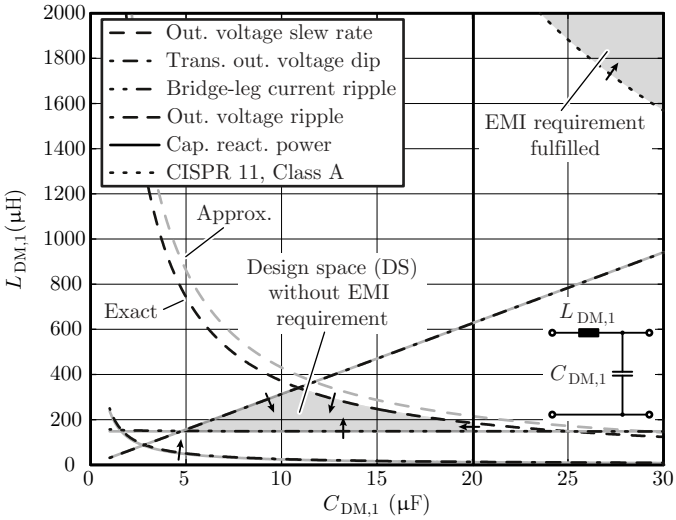


Figure 3.5: Design space (DS) analysis of a single-stage LC filter [cf. Fig. 3.2(a)] which leads to an empty DS because the compliance with CISPR 11, Class A (boundary depicted in the upper right corner) does not permit to achieve the required slew rate of 203 V/ms. Each arrow points toward the area where the corresponding requirement can be met. The black lines are obtained from the accurate computations and the gray lines result from the approximate expressions.

$L_{\mathrm{DM},1}$ reduces when the output voltage $v_{\mathrm{A,out}}$ increases. In this example the approximation leads to a mean relative error of 14%. For the DS of the two-stage LC filter (cf. **Fig. 3.7**), no simplified expressions are used and solely the accurate calculation based on the Laplace transformation is considered.

Transient Output Voltage Dip

A stepwise change in the output current of $\Delta I_{\mathrm{A,out}}$ leads to a transient in the output voltage $v_{\mathrm{A,out}}$, which, in the end, is compensated by the control of the CVS (controlled LC filter, dashed line in Fig. 3.4). However, due to the discrete-time control of the CVS, the compensating action of the control occurs with a time delay. Thus, the height of the voltage dip $\Delta V_{\mathrm{A,out}}$ is in a first approximation only determined by the

LC filter elements, i.e. the control does not reduce the voltage dip significantly (cf. Fig. 3.4) as also experimentally verified in Section 3.2.4 for the final realized filter design. Accordingly, $\Delta V_{\mathrm{A,out}}$ is directly obtained from

$$\Delta V_{\mathrm{A,out}} = \Delta I_{\mathrm{A,out}} \cdot \sqrt{\frac{L_{\mathrm{DM,1}}}{C_{\mathrm{DM,1}}}} = \Delta I_{\mathrm{A,out}} \cdot Z_{\mathrm{step}} \tag{3.14}$$

[uncontrolled single-stage LC filter, cf. Fig. 3.4]. Thus, to fulfill the requirements specified in Section 3.2.2, the DS is constrained according to

$$Z_{\mathrm{step}} = \sqrt{\frac{L_{\mathrm{DM,1}}}{C_{\mathrm{DM,1}}}} \leq Z_{\mathrm{step,max}} = 5.6\ \Omega, \tag{3.15}$$

or the maximum allowable inductance $L_{\mathrm{DM,1}}$ is limited according to

$$L_{\mathrm{DM,1}} \leq C_{\mathrm{DM,1}} \cdot (5.6\ \Omega)^2 = L_{\mathrm{DM,1,max}}. \tag{3.16}$$

In case of a more advanced filter structure, e.g. a two-stage LC filter (cf. Fig. 3.7), no closed-form solution for Z_{step} is available and Z_{step} is rather determined numerically in the time domain for an output current step of height $\Delta I_{\mathrm{A,out}}$ occurring at $t = t_0$:

$$\begin{aligned} \Delta V_{\mathrm{A,out}} &= V_{\mathrm{A,out,0}} - \min\left[v_{\mathrm{A,out}}(t)\right]\big|_{t > t_0}, \\ Z_{\mathrm{step}} &= \frac{\Delta V_{\mathrm{A,out}}}{\Delta I_{\mathrm{A,out}}}. \end{aligned} \tag{3.17}$$

For the approximate assumption of negligible influence of the control on $\Delta V_{\mathrm{A,out}}$, the actual value of the initial output voltage $V_{\mathrm{A,out,0}}$ has no effect on the value of Z_{step} due to the linear nature of the two-stage filter. Due to the same reason any step amplitude $\Delta I_{\mathrm{A,out}} > 0$ can be selected. It is noted from (3.16) that the maximum allowable inductance $L_{\mathrm{DM,1,max}}$ is directly proportional to $C_{\mathrm{DM,1}}$. $L_{\mathrm{DM,1,max}}\,(C_{\mathrm{DM,1}})$ is plotted in Fig. 3.5, based on the relation (3.16) and (3.17), respectively. The approximated and the exactly calculated results fit nicely.

Bridge-Leg Output Current Ripple

Provided that the output voltage ripple at the switching frequency is negligible, a triangular inductor current ripple results and the respective

peak-to-peak ripple value is equal to

$$\Delta I_{\mathrm{A0}} = \frac{m_{\mathrm{i}} \cdot (1 - m_{\mathrm{i}}) \cdot V_{\mathrm{dc}}}{2 \cdot L_{\mathrm{DM},1} \cdot f_{\mathrm{s,out}}} \underset{m_{\mathrm{i}}=0.5}{\leq} \frac{V_{\mathrm{dc}}}{8 \cdot L_{\mathrm{DM},1} \cdot f_{\mathrm{s,out}}} \leq 60\% \cdot I_{\mathrm{A,out,n,pk}} = 12.3\ \mathrm{A}. \tag{3.18}$$

A maximum peak-to-peak inductor current ripple of 12.3 A ($\pm 30\% \times I_{\mathrm{A,out,n,pk}}$) is defined for $V_{\mathrm{dc}} = V_{\mathrm{dc,n}} = 700$ V as compromise between the volume of $L_{\mathrm{DM},1}$ (and hence the size of the filter), the high-frequency copper and core losses in $L_{\mathrm{DM},1}$, and the achievable measurement accuracy when sampling the bridge-leg output current close to its average value.

Expression (3.18) can be rearranged for $L_{\mathrm{DM},1}$,

$$L_{\mathrm{DM},1} \geq \frac{V_{\mathrm{dc}}}{98.4\ \mathrm{A} \cdot f_{\mathrm{s,out}}} = L_{\mathrm{DM,1,max}}, \tag{3.19}$$

i.e. the minimum allowable $L_{\mathrm{DM},1}$ is proportional to the DC link voltage V_{dc}, inversely proportional to the switching frequency $f_{\mathrm{s,out}}$, and independent of $C_{\mathrm{DM},1}$. For more complex filter topologies, the value of ΔI_{A0} is calculated numerically in order to consider the voltage ripple across $C_{\mathrm{DM},1}$ at the switching frequency. The result of this accurate calculation is also given in Fig. 3.5; only marginal differences between the simplified (3.19) and the accurate expressions result for practical filter component values.

Output Voltage Ripple

At the nominal rms output voltage $v_{\mathrm{A,out}} = V_{\mathrm{A,out,n}} = 230$ V, $f_{\mathrm{out}} = 50$ Hz, and $V_{\mathrm{dc}} = 800$ V, the output voltage distortion remains within the specified limit of $\mathrm{THD_v} < 2.5\%$ (cf. IEEE 1547 [53]), if the peak-to-peak ripple $\Delta V_{\mathrm{A,out}}$ is lower than 22.8 V. With the triangular inductor current given by (3.18), $\Delta V_{\mathrm{A,out}}$ becomes

$$\Delta V_{\mathrm{A,out}} = \frac{m_{\mathrm{i}} \cdot (1 - m_{\mathrm{i}}) \cdot V_{\mathrm{dc}}}{16 \cdot L_{\mathrm{DM},1} \cdot C_{\mathrm{DM},1} \cdot f_{\mathrm{s,out}}^2} \underset{m_{\mathrm{i}}=0.5}{\leq} \frac{V_{\mathrm{dc}}}{64 \cdot L_{\mathrm{DM},1} \cdot C_{\mathrm{DM},1} \cdot f_{\mathrm{s,out}}^2} \leq 22.8\ \mathrm{V}, \tag{3.20}$$

which yields the inequality

$$L_{\mathrm{DM},1} \geq \frac{V_{\mathrm{dc}}}{1457.2\ \mathrm{V} \cdot C_{\mathrm{DM},1} \cdot f_{\mathrm{s,out}}^2} = L_{\mathrm{DM,1,min}}. \tag{3.21}$$

From the derived relation, it can be seen that the value of $L_{\mathrm{DM},1}$ has to be increased with the DC link voltage V_{dc}, and could be reduced for higher capacitances $C_{\mathrm{DM},1}$. Furthermore, there is a quadratic dependency on the switching frequency $f_{\mathrm{s,out}}$, as the impedance of $L_{\mathrm{DM},1}$ increases and the impedance of $C_{\mathrm{DM},1}$ decreases linearly with $f_{\mathrm{s,out}}$. For the two-stage filter topology (cf. Fig. 3.7), the value of $\Delta v_{\mathrm{A,out}}$ is only calculated numerically. The numerical computation of $L_{\mathrm{DM},1,\mathrm{min}}$ and its approximation by (3.21) agree well and are depicted in Fig. 3.5.

Capacitive Reactive Power

The reactive power demand caused by the filter capacitor of a phase at the output frequency f_{out} is given by

$$|Q_{\mathrm{cap}}| = 2 \cdot \pi \cdot f_{\mathrm{out}} \cdot C_{\mathrm{DM},1} \cdot V_{\mathrm{A,out,n}}^2 \leq |Q_{\mathrm{cap,max}}| = \frac{1\ \mathrm{kVA}}{3} \tag{3.22}$$

($|Q_{\mathrm{cap,max}}| = 10\% \cdot P_{\mathrm{out,n}}$). Thus, for $C_{\mathrm{DM},1}$, the inequality

$$C_{\mathrm{DM},1} \leq \frac{|Q_{\mathrm{cap,max}}|}{2 \cdot \pi \cdot f_{\mathrm{out}} \cdot V_{\mathrm{A,out,n}}^2} = C_{\mathrm{DM},1,\mathrm{max}} \tag{3.23}$$

applies, which is independent of $L_{\mathrm{DM},1}$. $C_{\mathrm{DM},1,\mathrm{max}}$ is shown in Fig. 3.5. In case of the two-stage filter, the value of $C_{\mathrm{DM},1}$ in (3.23) is replaced by the sum of all DM filter capacitors that belong to the considered phase A, i.e. $C_{\mathrm{DM},1}$ and $k \cdot C_{\mathrm{DM},1}$ (cf. Fig. 3.7).

Limits of Conducted EMI

This criterion compares the emitted levels of conducted DM EMI to the maximum levels allowed for the CISPR 11 norm, Class A (quasi-peak detector). **Fig. 3.6** depicts the noise source model that is employed to calculate the EMI emission: it consists of a voltage source $v_{\mathrm{A0}}(t)$, with edges of infinite slope, representing the inverter stage, the EMI filter, the Line Impedance Stabilization Network (LISN), and the test receiver. Only DM EMI noise is considered as the analysis in this section refers to single-phase considerations. A margin of 15 dB is included in the design of the filter to ensure that any CM emissions (resulting e.g. from parasitic capacitive coupling of the power transistors to ground, i.e. to the grounded heat sink [184]) could also be accommodated in the limits

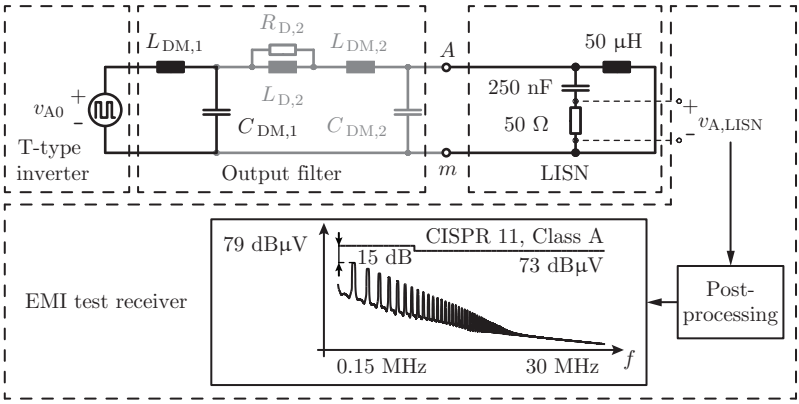


Figure 3.6: Equivalent circuit used to model the emitted conducted DM noise of the CVS. The model includes the noise source v_{A0}, the output filter, the LISN and the test receiver. In the "post-processing"-block the spectral components of $v_{A,LISN}$ (v_{A0} has edges with infinite slope) are computed and the worst-case output values of the EMI test receiver with quasi-peak detector are estimated according to (9) in [187].

of the CISPR 11 norm.[6] The EMI noise voltage is calculated based on the approach presented in [187], which employs a worst-case estimation.

Discussion

Fig. 3.5 shows the DS which is obtained for a single-stage LC output filter *excluding* the compliance with CISPR 11, Class A: for $C_{DM,1}$ ranging from 5 µF to 20 µF, all selected criteria can be satisfied. However, as clearly visible, the DS is empty if the EMI requirement should also be fulfilled. To obtain the required attenuation of conducted noise, increased values of $L_{DM,1}$ and $C_{DM,1}$ would be required, which would not allow fulfilling the slew rate requirement.

To overcome this issue, adding an LC stage to the single-stage filter, i.e. employing a two-stage LC output filter [cf. Fig. 3.2(b)], is identified to be most effective with respect to cost, construction volume, and efficiency. For defining the two-stage LC output filter, two variables, n

[6] If required, the model could be extended with respect to CM EMI noise using the approach presented in [185, 186].

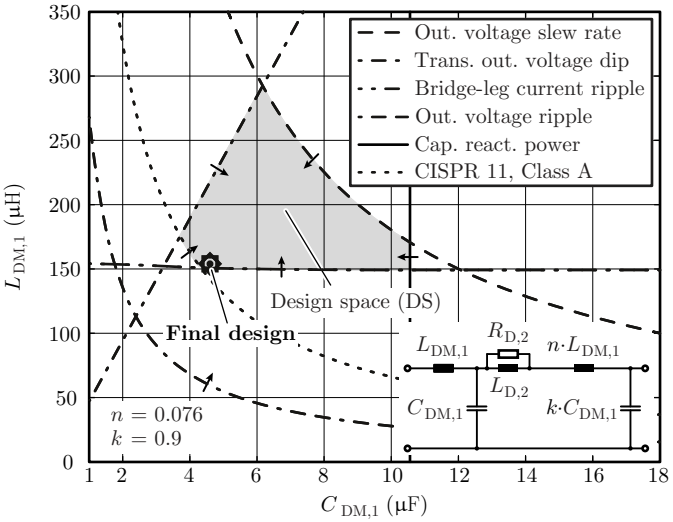


Figure 3.7: DS for a two-stage LC output filter [cf. Fig. 3.2(b)] for $n = L_{\mathrm{DM},2}/L_{\mathrm{DM},1} = 0.076$ and $k = C_{\mathrm{DM},2}/C_{\mathrm{DM},1} = 0.9$, as resulting from the optimization in Section 3.2.3 (cf. Tab. 3.4).

and k, are introduced:

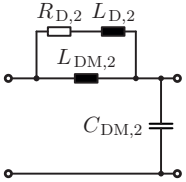
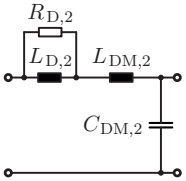
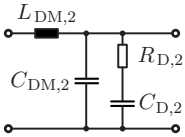
$$n := \frac{L_{\mathrm{DM},2}}{L_{\mathrm{DM},1}}, \quad k := \frac{C_{\mathrm{DM},2}}{C_{\mathrm{DM},1}}. \tag{3.24}$$

With $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k, a four-dimensional parameter space results.[7] To obtain a clear illustration of the DS, it is depicted in the $C_{\mathrm{DM},1}$–$L_{\mathrm{DM},1}$ plane for fixed n and k values as shown in Fig. 3.7 for $n = 0.076$ and $k = 0.9$. (The calculation of the DS illustrated in Fig. 3.7 is based on exact numerical computations of the different requirements as explained above.) According to Fig. 3.7, in case of a two-stage LC filter approach, dedicated values of $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k exist with which all requirements can be simultaneously fulfilled. The determination of n and k is detailed in Section 3.2.3 below.

In anticipation of the results presented in the following, the second

[7] For given $L_{\mathrm{DM},2} = n \cdot L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},2} = k \cdot C_{\mathrm{DM},1}$ the values of the damping components $L_{\mathrm{D},2}$ and $R_{\mathrm{D},2}$ are determined according to (3.25). Thus, $L_{\mathrm{D},2}$ and $R_{\mathrm{D},2}$ do not represent free parameters in this section.

Table 3.3: Damping resistance $R_{\mathrm{D},2,\mathrm{opt}}$ and minimal resonance gain A_{rr} for given values a and R_0 for a parallel RL (pRL), a series RL (sRL) and a parallel RC (pRC) damping of the second filter stage. For $A_{\mathrm{rr}} = 2$ the filter stage is of approximate Chebyshev type. Other designs of damping branches are for example discussed in [188–190].

Damping type	*pRL*	*sRL*	*pRC*
$R_{\mathrm{D},2,\mathrm{opt}}$	$R_0 \frac{\sqrt{2a(2a+1)}(a+1)}{2a+1}$	$R_0 \frac{2a}{\sqrt{2a^2+6a+4}}$	$R_0 \frac{\sqrt{2a^2+6a+4}}{2a}$
A_{rr}	$2a+1$	$\frac{a+2}{a}$	$\frac{a+2}{a}$
Remark	$a := \frac{L_{\mathrm{D},2}}{L_{\mathrm{DM},2}}$ $R_0 = \sqrt{\frac{L_{\mathrm{DM},2}}{C_{\mathrm{DM},2}}}$	$a := \frac{L_{\mathrm{D},2}}{L_{\mathrm{DM},2}}$ $R_0 = \sqrt{\frac{L_{\mathrm{DM},2}}{C_{\mathrm{DM},2}}}$	$a := \frac{C_{\mathrm{D},2}}{C_{\mathrm{DM},2}}$ $R_0 = \sqrt{\frac{L_{\mathrm{DM},2}}{C_{\mathrm{DM},2}}}$
Circuit			

LC filter stage cannot be actively damped. Thus, among the options shown in **Tab. 3.3** to passively damp this second stage, a series RL-branch is selected, because it leads to the smallest sum of the capacitance values of all capacitors of the two-stage filter. This result has been obtained by conducting the optimization presented in the following for the series RL damping branch for all three passive damping options. A low total capacitance value is targeted to achieve a large-signal bandwidth which is as high as possible. The optimal value $R_{\mathrm{D},2,\mathrm{opt}}$ of the damping resistor $R_{\mathrm{D},2}$ for a given damping inductance $L_{\mathrm{D},2}$ is computed such that the filter input-to-output transfer function leads to the smallest resonance gain A_{rr}, in contrast to [188], where $R_{\mathrm{D},2}$ is calculated to result in the minimal peak of the filter output impedance magnitude.

For the filter design

$$a = \frac{L_{\mathrm{D},2}}{L_{\mathrm{DM},2}} = 2, \text{ and}$$

$$R_{\mathrm{D},2} = R_{\mathrm{D},2,\mathrm{opt}} = \sqrt{\frac{L_{\mathrm{DM},2}}{C_{\mathrm{DM},2}}} \cdot \frac{2 \cdot a}{\sqrt{2 \cdot a^2 + 6 \cdot a + 4}} \tag{3.25}$$

are used to obtain a maximum A_{rr} of 6 dB and, as explained in the following, this selected second stage of the filter is of approximate Chebyshev type (with ripple factor $\epsilon = 0.12$ [191]). It is important to keep A_{rr} low, because the natural frequency $f_0 = 1/(2 \cdot \pi \cdot \sqrt{L_{\mathrm{DM},2} \cdot C_{\mathrm{DM},2}})$ of the second filter stage could be close to the switching frequency.[8] However, the lower A_{rr} (larger damping inductance $L_{\mathrm{D},2}$), the smaller also the -3 dB small-signal bandwidth $f_{\mathrm{bw,ss}}$ of the second filter stage. This trade-off between A_{rr} and $f_{\mathrm{bw,ss}}$ is similar to the conflict of objectives faced in a general filter design, where no ripple in the passband of the filter and an instantaneous transition from passband to stopband at the filter cut-off frequency is desired. The latter conflict of objectives can be solved by employing a Chebyshev filter of type I, as a compromise between Butterworth and elliptic filters [192]. Inspired by this idea, it is found that the poles of the second filter stage in the complex s-plane are located closely to the ones of a Chebyshev filter (type I of same order) for $A_{\mathrm{rr,max}} \approx 6$ dB, i.e. for $a = L_{\mathrm{D},2}/L_{\mathrm{DM},2} \approx 2$ [cf. (3.25)]. In Tab. 3.3, the values of $R_{\mathrm{D},2,\mathrm{opt}}$ are given for two other commonly employed damping branches as well.

3.2.3 Two-Stage Filter Design

The different criteria detailed in Section 3.2.2 constrain the DS of the two-stage LC output filter as, for example, shown in Fig. 3.7. However, in order to facilitate the realization of the most suitable output filter for the CVS, within the DS, an appropriate selection procedure has to be defined. In this work, a multi-objective filter optimization, based on the ρ–η PF [173], is conducted for the two-stage LC output filter depicted in Fig. 3.2(b). The loss and volume models needed for this optimization are summarized below. Furthermore, details about the optimization procedure are given and the calculated optimization results are discussed.

[8] For the final filter design $f_0 = 1/(2 \cdot \pi \cdot \sqrt{11.7\ \mu\mathrm{H} \cdot 4.1\ \mu\mathrm{F}}) = 23$ kHz results.

Losses and Volumes of Inductors and Capacitors

The inductor losses comprise copper and core losses. The calculation of the copper losses considers DC and AC losses (by reason of skin and proximity effects), which, for $L_{\mathrm{DM},1}$, are computed with

$$P_{\mathrm{cu}} = R_{\mathrm{dc}} \cdot I_{\mathrm{A,out,n}}^2 + \sum_{m=1}^{I_m \geq 5\% \cdot I_1} R_{\mathrm{ac},m} \cdot I_m^2, \tag{3.26}$$

where I_m is the rms value of the m^{th} harmonic of the inductor current ripple. R_{dc} and $R_{\mathrm{ac},m}$ are calculated according to [193, 194] for a temperature of 100°C. Eq. (3.26) considers all harmonics with an rms value larger than or equal to 5% of the rms value I_1 of the first harmonic occurring at $f_{\mathrm{s,out}}$ [operating point acc. (3.28)]. The calculations of the current ripples for the inductors of the second filter stage [cf. Fig. 3.2(b)] are based on the simplifying assumption that the high-frequency AC components of the current through $L_{\mathrm{DM},1}$, $i_{\mathrm{A0,ripple}}(t)$, can be represented by a single harmonic at the switching frequency with an rms value of

$$\begin{aligned} i_{\mathrm{A0,ripple,rms}} &= \sqrt{\frac{1}{T_{\mathrm{s,out}}} \cdot \int_0^{T_{\mathrm{s,out}}} i_{\mathrm{A0,ripple}}(t)^2 \cdot \mathrm{d}t} \\ &\underset{m_{\mathrm{i}}=0.5}{=} \frac{V_{\mathrm{dc,max}}}{\sqrt{3} \cdot 16 \cdot L_{\mathrm{DM},1} \cdot f_{\mathrm{s,out}}}. \end{aligned} \tag{3.27}$$

The current ripples through $L_{\mathrm{DM},2}$ and $L_{\mathrm{D},2}$ are then computed based on $i_{\mathrm{A0,ripple,rms}}$ and employing linear network analysis.

To realize the winding of the inductors, enameled copper wires are considered, because for the case at hand enameled wire leads to lower ohmic losses compared to litz wire due to the greater achievable winding area filling factor.

The core losses P_{fe} are calculated with the improved Generalized Steinmetz Equation (iGSE) according to [194, 195]. The Steinmetz parameters k, α, and β, needed for evaluating the iGSE, are given at a core temperature of 100°C in [127, 196] for the selected ferrite (N27 and N87 materials) E-cores from TDK EPCOS [197] to realize the inductors. Ferrite cores are utilized because of lower cost compared to nanocrystalline cores and due to a constant inductance over current compared to powder cores.

The evaluation of the copper and core losses requires the bridge-leg output current, $i_{\mathrm{A0,ripple}}(t)$, and the flux density in the core, $B(t)$, which are computed for the following worst case conditions:

$$\begin{aligned} &\text{max. DC link voltage:} && V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\ \mathrm{V}, \\ &\text{DC output current:} && I_{\mathrm{A,out}} = 17\ \mathrm{A}, \\ &\text{modulation index:} && m_{\mathrm{i}} = v_{\mathrm{A,out}} / \tfrac{V_{\mathrm{dc,max}}}{2} = 0.5 \\ & && \rightarrow\ \text{DC out. voltage } v_{\mathrm{A,out}} = 200\ \mathrm{V}. \end{aligned} \tag{3.28}$$

The modulation index $m = 0.5$ leads to the maximum current ripple ΔI_{A0} (cf. Section 3.2.2) and thus also to the maximum flux density ripple ΔB, which results in the maximum core losses according to the iGSE. To compute the current ripple ΔI_{A0} through $L_{\mathrm{DM,1}}$, the voltage across $C_{\mathrm{DM,1}}$ is assumed constant over one switching period $T_{\mathrm{s,out}}$. The current is increased from the nominal value $I_{\mathrm{A,out,n}} = 14.5$ A to $I_{\mathrm{A,out}} = 17$ A for the following reason. One application of the CVS could be the emulation of a low voltage mains (e.g. 230 V/400 V). The tolerance of the mains voltage is according to [37] (IEC standard voltages) $+10\%/-14\%$. Thus, to supply a load with $P_{\mathrm{A,out,n}} = 3.3$ kW for an emulated rms mains voltage of $230\ \mathrm{V} \cdot (1 - 0.14) = 198$ V leads to a rms current of $I_{\mathrm{A,out}} = 16.7\ \mathrm{A} \approx 17\ \mathrm{A}$.

Finally, to verify that the calculated winding losses P_{cu} and core losses P_{fe} do not lead to excessive temperature rises in the inductor, the maximum temperature $T_{\mathrm{L,max}}$ of the inductor is approximated with

$$T_{\mathrm{L,max}} = R_{\mathrm{th}} \cdot (P_{\mathrm{fe}} + P_{\mathrm{cu}}) + 40^{\circ}\mathrm{C} \tag{3.29}$$

assuming an ambient temperature of 40°C. The thermal resistance R_{th} is calculated with the empirical relation given in Fig. 2 of [198] for E-cores,

$$R_{\mathrm{th}} = \left(53 \cdot \left(V_{\mathrm{eff}}[\mathrm{cm}^3]\right)^{-0.54}\right) \frac{\mathrm{K}}{\mathrm{W}}, \tag{3.30}$$

where V_{eff} is the effective core volume.[9] Inductor designs which exceed $T_{\mathrm{L,max}} = 100^{\circ}\mathrm{C}$ are excluded from the Pareto optimization which is explained in the next subsection.

[9] The relation (3.30) is experimentally derived generating only winding losses in the components. However, as stated in Remark 2 of Section 2 in [198], the same relation was found while heating the core with only core losses.

The boxed volume of the inductor is calculated with the dimensions of the core and the estimated dimensions of the winding heads (including the bobbin dimensions) [197].

The capacitors of the output filter are realized with X2/305 V rated MKP (polypropylene) film capacitors from EPCOS [199]. Their dielectric losses are negligible compared to the inductor losses. The boxed volume of the capacitor with capacitance $C_{\mathrm{DM},i}$ $(i = 1, 2)$ is estimated with

$$V_{C_{\mathrm{DM},i,\mathrm{boxed}}} = 4.15 \, \frac{\mathrm{cm}^3}{\mu\mathrm{F}} \cdot C_{\mathrm{DM},i} \, [\mu\mathrm{F}] + 1.54 \, \mathrm{cm}^3. \tag{3.31}$$

This is a fit to the boxed volumes computed for the capacitors with a lead spacing of 27.5 mm given in [199], which are considered to be most suitable for the investigated output filter.

Filter Design and Optimization

The loss and volume models are employed to compute the ρ–η PF of the two-stage LC filter [cf. Fig. 3.2(b)] based on the four-dimensional DS with design variables $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k (detailed in Section 3.2.2). **Fig. 3.8** depicts the flow chart of the optimization procedure. In a first step, the different criteria for the CVS derived in Section 3.2.2 are evaluated for high numbers of values of $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k (box ① in Fig. 3.8). In order to achieve a constant relative (percentaged) change between adjacent values of inductances and capacitances, i.e. $L_{\mathrm{DM},1,i+1}/L_{\mathrm{DM},1,i} = \text{const.}$ and $C_{\mathrm{DM},1,j+1}/C_{\mathrm{DM},1,j} = \text{const.}$, geometric series are selected,

$$\begin{aligned} L_{\mathrm{DM},1,i} &= L_{\mathrm{DM},1,\min} \cdot 10^{\frac{i}{48}}, \\ & \quad L_{\mathrm{DM},1,\min} = 100 \ \mu\mathrm{H}, \ 0 \leq i \leq 32, \ i \in \mathbb{N}_0, \\ C_{\mathrm{DM},1,j} &= C_{\mathrm{DM},1,\min} \cdot 10^{\frac{j}{12}}, \\ & \quad C_{\mathrm{DM},1,\min} = 1 \ \mu\mathrm{F}, \ 0 \leq j \leq 16, \ j \in \mathbb{N}_0. \end{aligned} \tag{3.32}$$

With this, $L_{\mathrm{DM},1,i}$ and $C_{\mathrm{DM},1,j}$ are selected according to the commonly known E48 and E12 series of preferred values, respectively [200] (also known from the partitioning of ohmic values of commercially available resistors). Furthermore, a comparably high resolution is used for the inductors, due to the possibility of tuning inductances by altering the lengths of the air gap, and a reduced resolution is considered for the

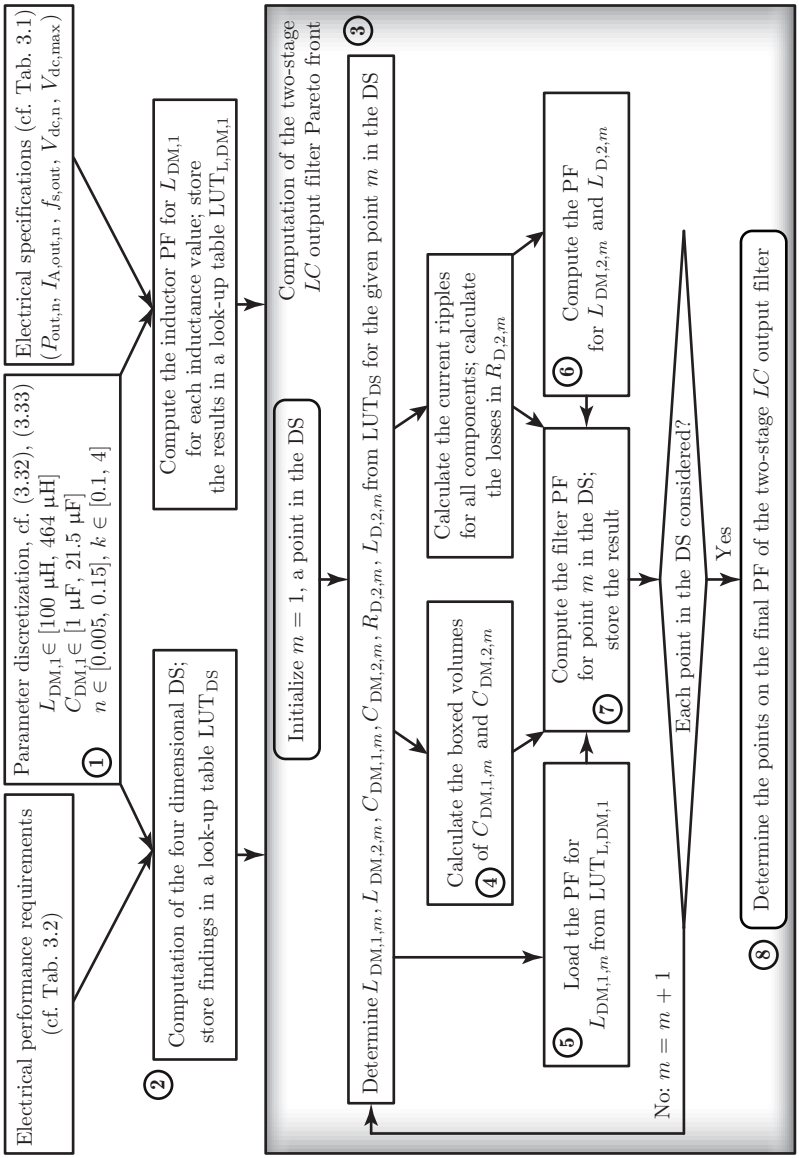


Figure 3.8: Flow chart to compute the ρ–η Pareto front (PF) for a two-stage LC output filter [cf. Fig. 3.2(b)].

capacitances, on the basis of available capacitance values. The values of n and k are selected based on linear distributions,

$$\begin{aligned} &n \in [0.005, 0.15],\ n_{\text{step}} = 0.005, \\ &k \in [0.1, 4],\ k_{\text{step}} = 0.05. \end{aligned} \tag{3.33}$$

In total $33 \times 17 \times 30 \times 79 \approx 1.3$ million points result.[10]

It is noted that the filter components have tolerances, which, however, are not considered in the presented computation because the focus is on the derivation of the DS and the ρ–η Pareto optimization.[11] The impact of these tolerances on the DS are elaborated in Section 3.2.5. If required, these implications can be included for a given confidence interval by means of worst case assumptions. The particular combination of component values that leads to the worst case, however, needs to be determined separately for each considered criterion that confines the DS.

The four-dimensional DS is calculated for the inductances and capacitances given with (3.32) and (3.33), which, for this particular application, results in 40'512 different quadruples of ($L_{\text{DM},1}$, $C_{\text{DM},1}$, n, k), which fulfill all criteria (box ② in Fig. 3.8).

In a second step, the ρ–η PF of the two-stage LC filter is calculated for the previously computed four-dimensional DS. The approach behind the PF computation is detailed for an arbitrary point in the middle of the DS given by

$$L_{\text{DM},1} = 205\ \mu\text{H},\ C_{\text{DM},1} = 6.5\ \mu\text{F},\ n = 0.076, \text{ and } k = 0.9, \tag{3.34}$$

leading to $L_{\text{D},2} = 31.2\ \mu\text{H}$ and $R_{\text{D},2} = 1.33\ \Omega$ [cf. (3.25), Fig. 3.7 and ③ in Fig. 3.8].

For this exemplary point in the DS, all filter capacitors are selected and all inductors are designed. It is assumed that capacitors with capacitance values of $C_{\text{DM},1} = 6.5\ \mu\text{F}$ and $C_{\text{DM},2} = k \cdot C_{\text{DM},1} = 5.9\ \mu\text{F}$ exist and thus the volumes $V_{C_{\text{DM},1}}$ and $V_{C_{\text{DM},2}}$ of $C_{\text{DM},1}$ and $C_{\text{DM},2}$ are calculated with (3.31) [④ in Fig. 3.8]. The inductors are designed with a dedicated design procedure, which considers 30 different ferrite

[10] It is remarked that different discretizations of $L_{\text{DM},1}$, $C_{\text{DM},1}$, n, and k can be used, based on particular needs, e.g. based on available or preferred component values.

[11] The final components could be selected carefully such that the measured and calculated component values fit closely (cf. Tab. 3.4).

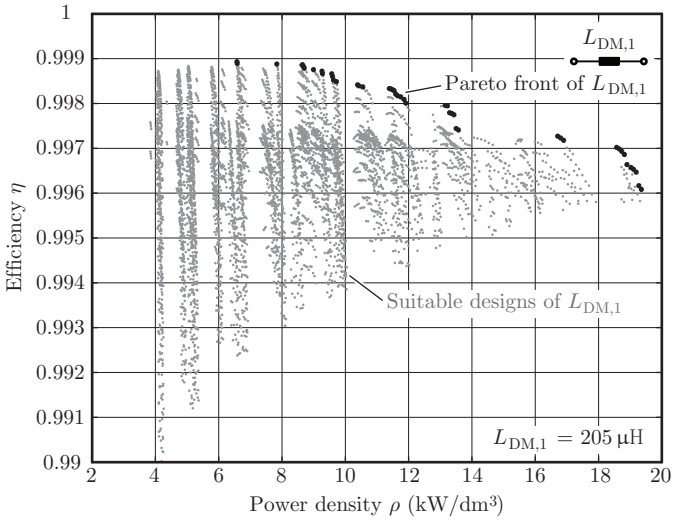


Figure 3.9: Exemplary ρ–η PF for inductor $L_{\mathrm{DM,1}}$ to achieve an inductance of 205 µH.

E-cores from EPCOS [197], up to 5 stacked cores, up to $N_{\max}$ turns, and wire diameters ranging from 0.1 mm to $d_{\mathrm{wire,max}}$ with a step size of $d_{\mathrm{wire,step}} = 0.1$ mm. The maximum number of turns $N_{\max}$ is determined such that the maximum air-gap length, indicated in the data sheet for each core [197], is not exceeded and $d_{\mathrm{wire,max}}$ is calculated based on the core and bobbin dimensions in order to fit the winding into the available volume.
This results in 5'848 suitable designs for $L_{\mathrm{DM,1}}$, 13'237 suitable designs for $L_{\mathrm{DM,2}}$, and 13'899 suitable designs for $L_{\mathrm{D,2}}$, obtaining also the losses $P_{L_{\mathrm{DM,1}}}$, $P_{L_{\mathrm{DM,2}}}$, and $P_{L_{\mathrm{D,2}}}$ and volumes $V_{L_{\mathrm{DM,1}}}$, $V_{L_{\mathrm{DM,2}}}$, and $V_{L_{\mathrm{D,2}}}$ of $L_{\mathrm{DM,1}}$, $L_{\mathrm{DM,2}}$, and $L_{\mathrm{D,2}}$ for all designs as explained in Section 3.2.3.

To get each and every possible two-stage LC filter realization, all suitable inductor designs for $L_{\mathrm{DM,1}}$, $L_{\mathrm{DM,2}}$, and $L_{\mathrm{D,2}}$ need to be combined with each other, leading to $108 \cdot 10^{10}$ filter realization options. An effective reduction of the number of different filter realizations is achieved if only the inductor designs are considered that give a high power density and / or efficiency. The corresponding inductor designs are directly obtained by taking those design results that form the PF

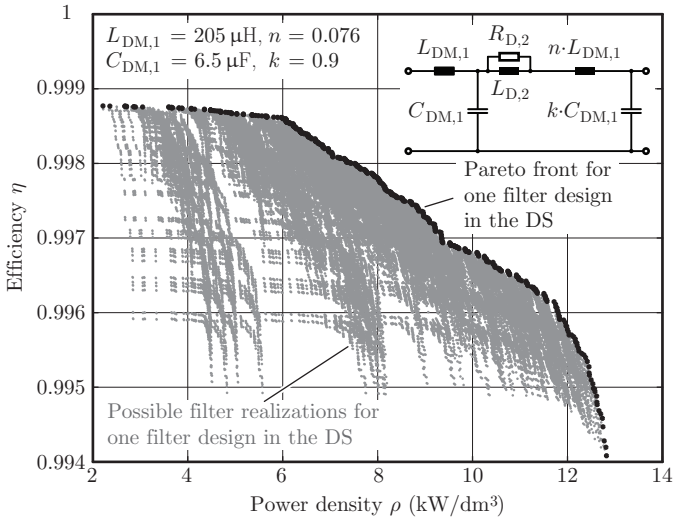


Figure 3.10: Exemplary ρ–η PF of the whole filter for one arbitrary selected filter design in the DS with parameters $L_{DM,1}$ = 205 µH, $C_{DM,1}$ = 6.5 µF, $n = 0.076$ and $k = 0.9$. The PF is calculated based on the three inductor PFs for $L_{DM,1}$, $L_{DM,2}$, and $L_{D,2}$.

in the respective ρ–η plane (cf. **Fig. 3.9**) for $L_{DM,1}$ [⑤ and ⑥ in Fig. 3.8].[12] An inductor design with ρ_j and η_j is on the PF if its η_j is greater than the efficiencies η of all other designs with a higher power density $\rho > \rho_j$.

To find filter realizations with minimal volume ($\rightarrow$ maximum power density) for a given efficiency and / or with minimum losses ($\rightarrow$ maximum efficiency) for a given volume, only the inductor designs on the corresponding inductor PF can be considered, because the inductor designs for given inductance values $L_{DM,1}$, $L_{DM,2}$, and $L_{D,2}$ are independent from each other, and the losses and volumes are strictly greater than zero, i.e. $P_{L_{DM,1}} > 0$, $P_{L_{DM,2}} > 0$, and $P_{L_{D,2}} > 0$ and $V_{L_{DM,1}} > 0$, $V_{L_{DM,2}} > 0$, and $V_{L_{D,2}} > 0$. Therefore, only 46 designs on the inductor PF are considered for $L_{DM,1}$, 51 for $L_{DM,2}$, and 51 for $L_{D,2}$, resulting

[12] Because the voltage across $C_{DM,1}$ is assumed to be constant, the inductor PFs for all inductance values of $L_{DM,1}$ are only computed once and stored in a look-up table (cf. Fig. 3.8).

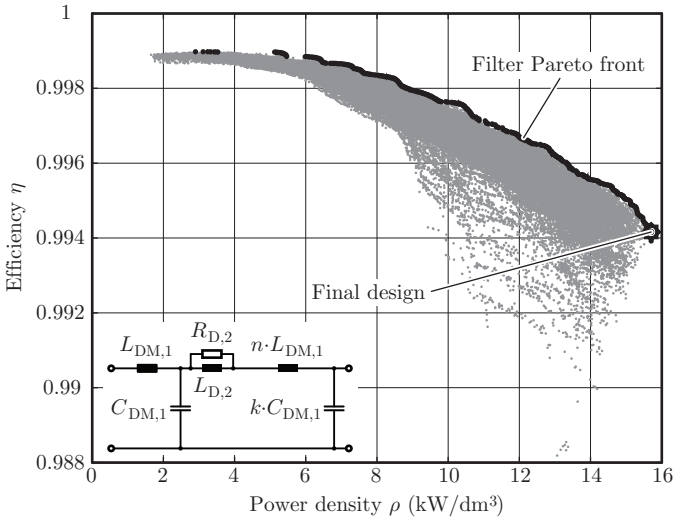


Figure 3.11: Result of the ρ–η Pareto optimization for a two-stage LC output filter [cf. Fig. 3.2(b)] in its four-dimensional design space [cf. Fig. 3.8] resulting in the filter Pareto front. The final design (cf. Tab. 3.4) is indicated and achieves a calculated power density of 15.7 kW/dm^3 for an efficiency of 99.4%. Compared to the initially considered arbitrary point in the DS [cf. (3.34)] leading to 12.8 kW/dm^3 for the same efficiency of 99.4% (cf. Fig. 3.10), the design on filter PF shows a 18% higher power density.

in $46 \times 51 \times 51 = 119'646$ two-stage filter realizations (gray points in **Fig. 3.10**). The power density ρ_q and efficiency η_q of a filter design q can be computed according to

$$\rho_q = \frac{P_{\mathrm{A,out,n}}}{V_{L_{\mathrm{DM},1},q} + V_{C_{\mathrm{DM},1},q} + V_{L_{\mathrm{DM},2},q} + V_{C_{\mathrm{DM},2},q} + V_{L_{\mathrm{D},2},q}}$$
$$\eta_q = \frac{P_{\mathrm{A,out,n}}}{P_{\mathrm{A,out,n}} + \left(P_{L_{\mathrm{DM},1},q} + P_{L_{\mathrm{DM},2},q} + P_{L_{\mathrm{D},2},q} + P_{R_{\mathrm{D},2},q}\right)}, \qquad (3.35)$$

where $P_{\mathrm{A,out,n}}$ is equal to 10 kW/3 and $P_{R_{\mathrm{D},2},q}$ denote the losses of the damping resistor $R_{\mathrm{D},2}$. To further reduce the number of filter realizations of the selected point in the DS ($L_{\mathrm{DM},1} = 205$ µH, $C_{\mathrm{DM},1} = 6.5$ µF, $n = 0.076$, and $k = 0.9$), again, only the resulting filter ρ–η PF as shown in Fig. 3.10, consisting of 559 points, is taken and stored [⑦ in Fig. 3.8].

Table 3.4: Two-stage LC output filter [cf. Fig. 3.2(b)] design resulting from the ρ–η Pareto optimization (cf. Fig. 3.8 and Fig. 3.11) and its hardware realization (cf. Section 3.2.3).
[1)] Measured with the Agilent impedance analyzer 4294A (40 Hz – 110 MHz) and without pre-magnetization for the inductors and DC voltage offset for the capacitors.

Component	*Pareto optimization result*	*Calculated boxed volume*	*Measured*[1)] *value at* 48 kHz	*Measured boxed volume*
$L_{\mathrm{DM},1}$	154 µH	146.8 cm^3	154.2 µH	157.3 cm^3
$C_{\mathrm{DM},1}$	4.6 µF	20.6 cm^3	4.7 µF	24.0 cm^3
$L_{\mathrm{DM},2}$	11.6 µH	9.4 cm^3	11.7 µH	10.2 cm^3
$C_{\mathrm{DM},2}$	4.1 µF	18.7 cm^3	4.1 µF	17.9 cm^3
$L_{\mathrm{D},2}$	23.1 µH	16.6 cm^3	22.4 µH	19.4 cm^3
$R_{\mathrm{D},2}$	1.36 Ω	Neglected	1.34 Ω	0.01 cm^3

As explained for the selected quadruple [cf. (3.34)], the filter PF for each quadruple in the DS is computed in the same manner, and the final ρ–η PF of the two-stage LC output filter, as shown in **Fig. 3.11** (black points), can be calculated from the filter PFs [⑧ in Fig. 3.8]. From all designs on this final filter PF, the filter design with the highest power density of $\rho = 15.7$ kW/dm^3 still has a reasonably high efficiency of $\eta = 99.4\%$ and hence is selected and realized as summarized in **Tab. 3.4**.

It it noted that the presented ρ–η PF calculation for the two-stage LC filter could be extended, in the same way as discussed in this subsection, also to LC filters with a higher number of stages.

3.2.4 Experimental Results

To validate the proposed filter design approach for the selected two-stage LC output filter (cf. Tab. 3.4), the compliance to the six requirements defined in Section 3.2.2 is verified (cf. **Tab. 3.5**) by employing the T-type converter detailed in [66], where the IGBTs are replaced by SiC MOSFETs (Cree's C2M0080120D) due to the switching frequency of 48 kHz.

According to Tab. 3.5 all requirements can be fulfilled and the nu-

Table 3.4: Continued.

Component	*Hardware realization*
$L_{\mathrm{DM},1}$	$4 \times 2 \times$ E 47/20/16 (ferrite N87, EPCOS) $N = 13$, $\varnothing_{\mathrm{cu}} = 2.5$ mm, $d_{\mathrm{air}} = 1.83$ mm
$C_{\mathrm{DM},1}$	4.7 $\mu\mathrm{F}_{\mathrm{rated}}$ || 0.68 $\mu\mathrm{F}_{\mathrm{rated}}$ X2/305 $\mathrm{V}_{\mathrm{rms}}$ AC B32924C3475M and B32923C3684M (MKP, EPCOS)
$L_{\mathrm{DM},2}$	$3 \times 2 \times$ E 20/10/6 (ferrite N27, EPCOS) $N = 8$, $\varnothing_{\mathrm{cu}} = 1.4$ mm, $d_{\mathrm{air}} = 1.03$ mm
$C_{\mathrm{DM},2}$	4.7 $\mu\mathrm{F}_{\mathrm{rated}}$ X2/305 $\mathrm{V}_{\mathrm{rms}}$ AC B32924C3475M (MKP, EPCOS)
$L_{\mathrm{D},2}$	$2 \times 2 \times$ E 25/13/7 (ferrite N27, EPOCS) $N = 14$, $\varnothing_{\mathrm{cu}} = 1.8$ mm, $d_{\mathrm{air}} = 1.78$ mm
$R_{\mathrm{D},2}$	2.67 Ω || 2.7 Ω = 1.34 Ω Thick film 2512 SMD 1 W resistors

merical calculations closely fit with the measured results. In this context, it should again be noted that a margin of 15 dB is included in the filter design to ensure a very low EMI noise level of the generated output voltage.

As can be seen by comparing columns three and five of Tab. 3.4, the boxed volumes of the built inductors $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$ are 7%, 8%, and 14% larger than the calculated ones, resulting in a measured power density of $\rho_{\mathrm{meas}} = 14.6\,\mathrm{kW/dm^3}$ ($239\,\mathrm{W/in^3}$) instead of $\rho = 15.7\,\mathrm{kW/dm^3}$ ($257\,\mathrm{W/in^3}$) [deviation of 7%]. The main reason is that each turn, with the wires of the selected wire diameters, requires a certain radius of curvature to be wound around the middle leg of the E-core.

To measure accurately the total losses of the output filter for the conditions given in (3.28), i.e. $I_{\mathrm{A,out}} = 17$ A and $V_{\mathrm{A,out}} = 200$ V for $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800$ V, resulting in a modulation index of $m_{\mathrm{i}} = 0.5$ and / or the maximum peak-to-peak bridge-leg output current ripple, the DC losses were measured separately from the AC losses. DC losses of 13.0 W were measured in the thermal equilibrium for a DC current $I_{\mathrm{A0}} = I_{\mathrm{A,out}} = 17$ A. The measured value results from the multiplication of the measured DC voltage and DC current at the input of the

Table 3.5: Comparison between the calculated and measured performance indices as defined in Section 3.2.2 (cf. Tab. 3.2) for the ρ–η Pareto optimized and realized two-stage LC output filter [cf. Fig. 3.2(b)] with the measured values as given in Tab. 3.4.
[1)] This value is calculated with $(230\ \mathrm{V})^2 / |\underline{Z}_{\mathrm{out}}|$ based on the measured output impedance $\underline{Z}_{\mathrm{out}} = 363\ \Omega \cdot \mathrm{e}^{-j \cdot 89.97^\circ}$ at $f_{\mathrm{out}} = 50$ Hz with the input of the filter being open.

Requirement	*Required min./ max. value*	*Calculated value*	*Measured value*
Output voltage slew rate SR	min. 203 V/ms	322 V/ms	324 V/ms
Transient output voltage dip $\rightarrow Z_{\mathrm{step}}$	max. 5.6 Ω	4.7 Ω	4.2 Ω
Bridge-leg current ripple Δi_{A0}	max. 12.3 A	12.0 A	12.2 A
Output voltage ripple $\Delta v_{\mathrm{A,out}}$	max. 22.8 V	2.5 V	2.6 V
Capacitive reactive power Q_{cap}	max. 333 VA	147 VA	146 VA[1)]
Conducted EMI level	max. 79 dBµV ($f < 500$ kHz)	62.4 dBµV @ 192 kHz	57.1 dBµV @ 192 kHz

filter for a shorted output. The voltage and the current were measured with Multimeters Fluke 189, which leads to an error of 1% [201] for the DC power (loss) measurement. The calculated DC losses of 12.8 W agree with the measured value (deviation of 2%). On the other hand, AC losses of 5.3 W were measured with a Yokogawa WT3000 power analyzer for no load, $V_{\mathrm{A,out}} = 200$ V and $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800$ V, and just after the entire filter was operated in the thermal equilibrium under the conditions of (3.28), in order to measure the losses for component temperatures corresponding to the mentioned conditions. According to the data sheet of the power analyzer [202], the error of this measurement is 11%. A comparison to the calculated value of 6.6 W reveals that the calculation overestimates the AC losses by 20%. Accordingly, the total measured losses of the filter are 13.0 W + 5.3 W = 18.3 W (measurement error of ±4%), which is in good agreement with the calculated losses of 12.8 W + 6.6 W = 19.4 W (deviation of 6%). Thus,

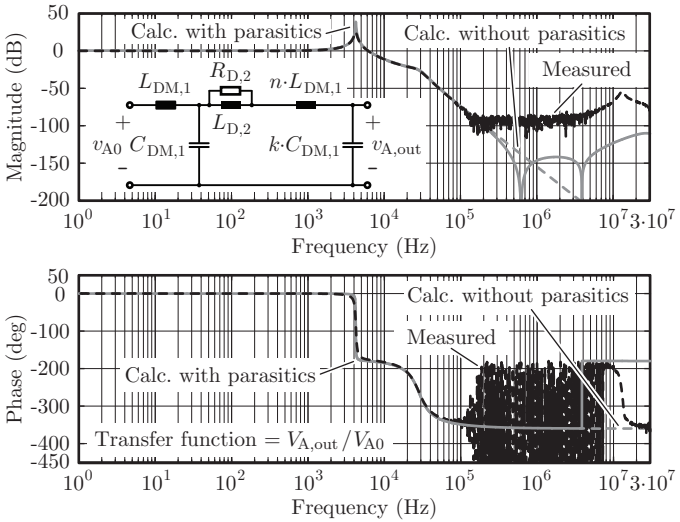


Figure 3.12: Measured (black dashed line) and calculated (gray lines) input-to-output transfer function of the realized two-stage LC filter with a series RL damping branch of the second stage (cf. Tab. 3.4). It is remarked that the first resonance peak at 4.2 kHz is actively attenuated by the current control loop [cf. Fig. 3.2(b)] and that the second resonance peak at 27 kHz is passively damped by the serial RL branch. For the dashed gray line ideal components are assumed, whereas for the solid gray line the parasitic capacitances and inductances of the inductors and capacitors (determined by separate measurements) are included. The measurement was conducted with a Bode 100 network analyzer (Omicron Lab, [203]) and shows a good agreement with the calculation until 100 kHz, where the noise floor of the measurement device is reached (specified as −100 dB in [203]).

the calculated and measured efficiencies are both 99.4%.

Moreover, the measured (black line) and calculated (gray lines) input-to-output transfer function ($v_{A,out}/v_{A0}$) of the realized two-stage LC filter with series RL damping branch of the second stage, is depicted in **Fig. 3.12**, showing a good agreement until 100 kHz, where the noise floor of the measurement device is reached for attenuations higher than 100 dB.

It is noted that the maximum inductor temperatures T_{meas} were

Table 3.6: Maximum measured inductor temperatures (occurring at the winding surface) at an ambient temperature of 30°C and for the conditions given by (3.28), i.e. $I_{\mathrm{A,out}} = 17$ A and $V_{\mathrm{A,out}} = 200$ V for $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800$ V. The temperatures were measured with a Fluke Ti9 thermal imager (emissivity of 0.95) and for the calculation the same ambient temperature of 30°C is used instead of 40°C, which is assumed for the ρ–η Pareto front optimization (cf. Section 3.2.3).

Inductor	*Max. measured temperature* T_{meas}	*Max. calculated temperature* T_{calc}
$L_{\mathrm{DM,1}}$	81.2°C	90.8°C
$L_{\mathrm{DM,2}}$	105.9°C	89.8°C
$L_{\mathrm{D,2}}$	94.5°C	86.4°C

only roughly measured as summarized in **Tab. 3.6** for the conditions as employed in the calculation given by (3.28), i.e. $I_{\mathrm{A,out}} = 17$ A and $V_{\mathrm{A,out}} = 200$ V for $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800$ V. The ambient temperature was $T_{\mathrm{a}} = 30$°C. The relative errors $(T_{\mathrm{meas}} - T_{\mathrm{a}})/(T_{\mathrm{calc}} - T_{\mathrm{a}})$ of the measurements compared to the calculated temperatures T_{calc} are −16%, 27%, and 14% for $L_{\mathrm{DM,1}}$, $L_{\mathrm{DM,2}}$, and $L_{\mathrm{D,2}}$, respectively, and are in the expected tolerance range. The measured higher temperatures for $L_{\mathrm{DM,2}}$ and $L_{\mathrm{D,2}}$ could be explained by the close proximity of $L_{\mathrm{DM,2}}$ and $L_{\mathrm{D,2}}$.

In the following, the measurement results for each requirement are discussed. It is anticipated, that for the measurement of the output voltage slew rate *SR*, transient output voltage dip, and bridge-leg output current Δi_{A0}, the load current source of Fig. 3.2(b) is replaced by a resistor of 97 Ω.[13]

Output Voltage Slew Rate Measurement

The measured output voltage step response from $v_{\mathrm{A,ref}} = 350$ V to $v_{\mathrm{A,ref}} = 384$ V is depicted in **Fig. 3.13**. The employed control architecture is shown in Fig. 3.2(b).[14]

The digital controller, implemented using a TMS320F2808 digital

[13] With a load resistor of 97 Ω, the output power is half of the nominal value of one of the three phases, i.e. $P_{\mathrm{A,out}} = 50\% \cdot P_{\mathrm{out,n}}/3 = (400\ \mathrm{V})^2/97\ \Omega = 1.65$ kW.

[14] Voltage controller $G_{\mathrm{v}} = k_{\mathrm{pv}} \cdot \frac{1+s \cdot T_{\mathrm{iv}}}{s \cdot T_{\mathrm{iv}}}$ with $k_{\mathrm{pv}} = 51$ mA/V, $T_{\mathrm{iv}} = 177$ µs; current controller $G_{\mathrm{i}} = k_{\mathrm{pi}}$ with $k_{\mathrm{pi}} = 6.4$ V/A.

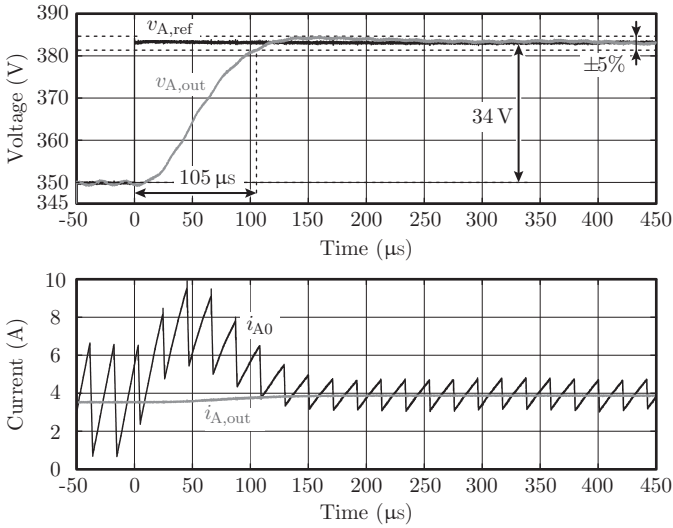


Figure 3.13: Measured reference voltage $v_{A,ref}$, output voltage $v_{A,out}$, bridge-leg output current i_{A0}, and load current $i_{A,out}$, resulting in a measured slew rate of $SR_{meas} = 34\ V/105\ \mu s = 324\ V/ms$, to verify the calculated SR of 322 V/ms. The output voltage reference $v_{A,ref}$ is determined from the voltage measured at a general purpose I/O pin of the employed DSP.

signal processor, generates the step of the output voltage reference and, at the same time, changes the logical state of one of its general purpose I/O pins. The time $\Delta t_{meas} = 105\ \mu s$ is measured from this instant until the output voltage enters the ±5% tolerance band and stays in the band [cf. Fig. 3.3] as depicted in Fig. 3.13. Accordingly, the measured slew rate is

$$SR_{meas} = \frac{34\ V}{105\ \mu s} = 324\ V/ms, \tag{3.36}$$

which is very close to the calculated value of 322 V/ms due to the proper controller tuning.

Transient Voltage Dip Measurement

To generate a load step of $\Delta I_{A,out} = 3.4$ A, a 100 Ω resistor chopper is connected in parallel to the 97 Ω load resistor. **Fig. 3.14** shows the

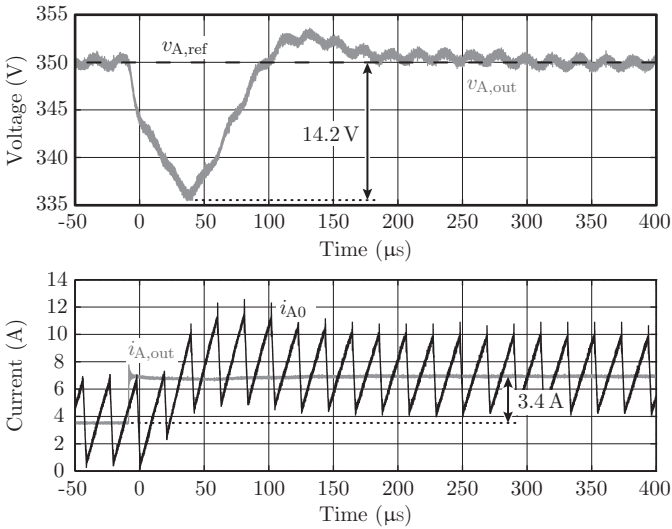


Figure 3.14: Measured output voltage $v_{\mathrm{A,out}}$, bridge-leg output current i_{A0}, and load current $i_{\mathrm{A,out}}$, resulting in a measured transient output voltage dip $\Delta V_{\mathrm{A,out,meas}} = 14.2$ V, verifying the calculated value of $\Delta V_{\mathrm{A,out}}$ of 16 V.

measured output voltage dip due to this change in the load current, which leads to

$$Z_{\mathrm{step,meas}} = \frac{14.2\ \mathrm{V}}{3.4\ \mathrm{A}} = 4.2\ \Omega. \tag{3.37}$$

This $Z_{\mathrm{step,meas}}$ is only 11% lower than the value, 4.7 Ω, obtained without control (cf. Tab. 3.5). The reason for this is the implemented controller design; a more aggressive voltage controller would reduce the transient output voltage dip, but would increase the overshoot of the output voltage step response and / or the settling time such that the specified limit could not be met anymore (cf. Section 3.2.2).

Bridge-Leg Output Current Ripple Measurement

The ripple of the bridge-leg output current i_{A0} is measured for a DC link voltage of $V_{\mathrm{dc}} = V_{\mathrm{dc,n}} = 700$ V and a constant modulation index of $m_{\mathrm{i}} = u_{\mathrm{A,out}} / \frac{V_{\mathrm{dc,n}}}{2} = 0.5$ (cf. Section 3.2.2). This modulation index

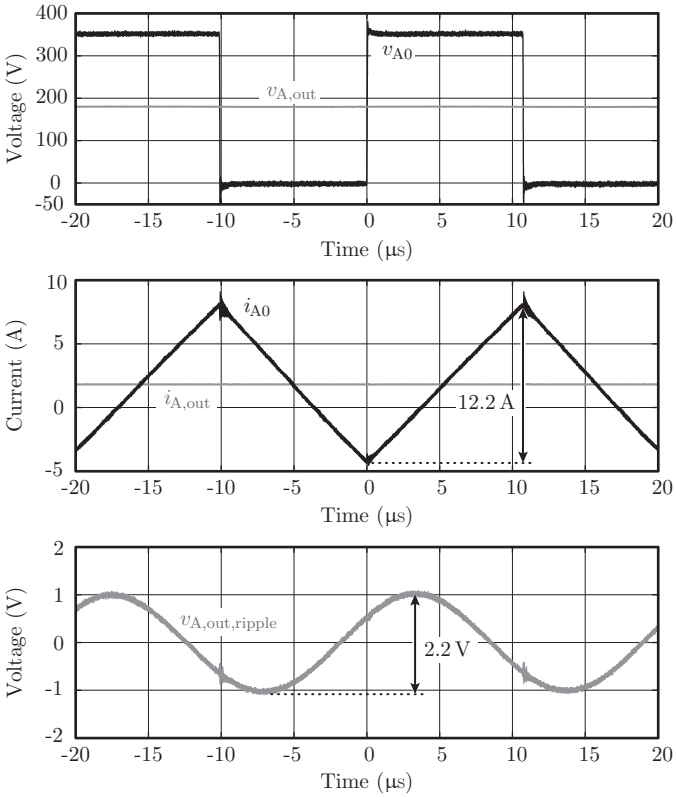


Figure 3.15: Measured bridge-leg output voltage v_{A0}, output voltage $v_{A,out}$, bridge-leg output current i_{A0}, and load current $i_{A,out}$, resulting in a peak-to-peak bridge-leg output current ripple $\Delta I_{A0,meas} = 12.2$ A, to verify the calculated ΔI_{A0} of 12.0 A. The output voltage ripple is measured with AC-coupling in the bottom graph and has a peak-to-peak value of 2.2 V. The reason for the slightly lower / higher voltage of v_{A0} at the end of the switching transients is that in the interlocking time the body diode of the MOSFET is conducting instead of its channel. This leads to a higher voltage drop over the switch till the MOSFET turns on and the current commutes to the channel.

is selected because the largest current ripple occurs for $m_i = 0.5$. The measurement result is given in **Fig. 3.15** and leads to a peak-to-peak

bridge-leg output current ripple of

$$\Delta I_{\mathrm{A0,meas}} = 12.2\ \mathrm{A}, \tag{3.38}$$

which matches closely with the computed value of 12 A (the inductance of $L_{\mathrm{DM},1}$ has been measured as 154.2 µH, i.e. deviates by only 0.1% from the value 154 µH assumed for the calculation (cf. Tab. 3.4); the DC link voltage is adjusted to 700 V with an error of 0.7%).

Output Voltage Ripple Measurement

The time behavior of the output voltage ripple is shown in Fig. 3.15 for $V_{\mathrm{dc}} = 700$ V. To measure the maximum output voltage ripple, the DC link voltage is increased to $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800$ V (cf. Section 3.2.2). A peak-to-peak voltage ripple of

$$\Delta V_{\mathrm{A,out,meas}} = 2.6\ \mathrm{V} \tag{3.39}$$

is obtained ($m_{\mathrm{i}} = 0.5$). The measured value is close to the calculated maximum voltage ripple of 2.5 V despite the tolerance of ±20% of the capacitance for the MKP capacitors for the two following reasons. First, a small capacitor rated at 0.68 µF was added to the capacitor rated at 4.7 µF to realize $C_{\mathrm{DM},1}$ (cf. Tab. 3.4). Thus, the measured capacitance of $C_{\mathrm{DM},1}$ deviates by only 2% from the calculated value. And second, for $C_{\mathrm{DM},2}$ an capacitor with an overrated capacitance (rated at 4.7 µF for a desired value of 4.1 µF) was selected to obtain an exact match between measured and calculated value (cf. Tab. 3.4). Furthermore, as shown in the previous subsection for $L_{\mathrm{DM},1}$, the measured filter inductances are also very close to the calculated values for $L_{\mathrm{DM},2}$ (1% deviation) and $L_{\mathrm{D},2}$ (3% deviation).

Maximum Capacitive Reactive Power Measurement

To assess the reactive power consumption of the filter at an output frequency of $f_{\mathrm{out}} = 50$ Hz, the output impedance $\underline{Z}_{\mathrm{out}}$ (open input) of the two-stage LC output filter is measured as shown in **Fig. 3.16**. At 50 Hz, the output impedance is nearly perfectly capacitive, $\underline{Z}_{\mathrm{out}} = 363\ \Omega \cdot \mathrm{e}^{-\mathrm{j} \cdot 89.97^{\circ}}$, and accordingly the measured capacitive reactive power of the filter is computed to

$$Q_{\mathrm{cap,meas}} = \frac{V_{\mathrm{A,out,n}}^2}{|\underline{Z}_{\mathrm{out}}|} = \frac{(230\ \mathrm{V})^2}{363\ \Omega} = 146\ \mathrm{VA}. \tag{3.40}$$

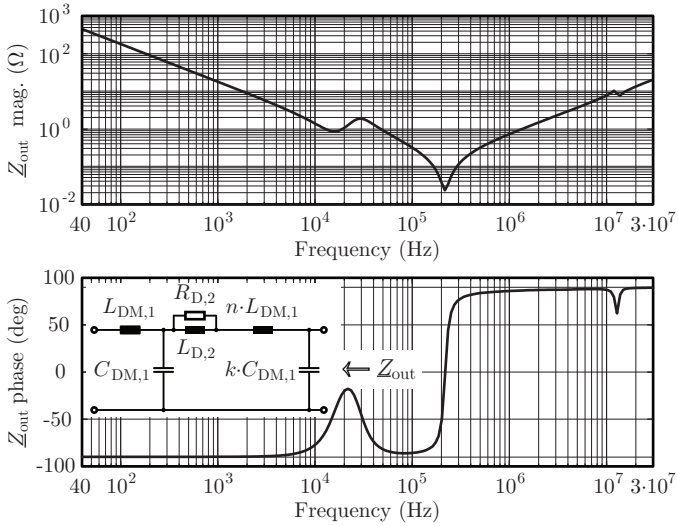


Figure 3.16: Measured (Agilent 4294A 40 Hz–110 MHz Precision Impedance Analyzer) output impedance $\underline{Z}_{\text{out}}$ of the designed two-stage *LC* filter (cf. Tab. 3.4) with an open filter input as indicated in the figure.

This value fits with the calculated reactive power of 147 VA (cf. Tab. 3.5) due to the accurate realization of the filter capacitances as indicated above.

Conducted EMI Measurement

The conducted noise emissions of the CVS are measured using the setup shown in **Fig. 3.17**. The attenuations of 10 dB of the LISNs (for increased accuracy) and of 10 dB of the impulse limiter (used to protect the test receiver) are compensated by the −20 dB of the EMI test receiver. In this work only DM emissions are considered (cf. Section 3.2.2) and thus a DM and CM noise separation is applied [204]. Still, two CM chokes [3 × T60006-L2050-W516 (Vacuumschmelze GmbH), 5 turns] are used for this measurement, as depicted in Fig. 3.17, keeping the difference between DM and CM noise smaller than 40 dB to achieve meaningful measurement results with the noise separator which shows a limited CM rejection ration (CMRR) [204].

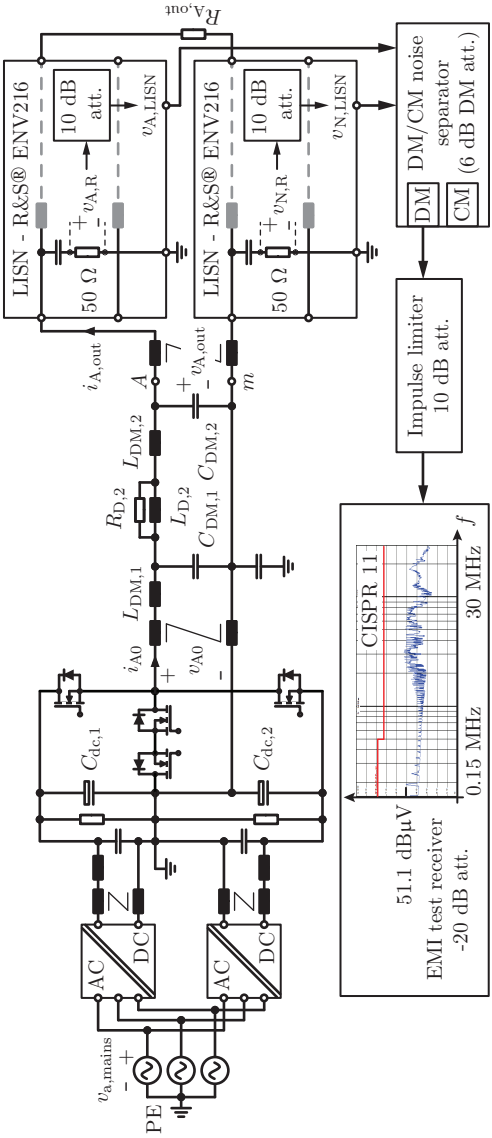


Figure 3.17: Conducted EMI measurement setup to measure the DM noise emission of the CVS employing two LISNs at the filter output and a DM / CM noise separator.

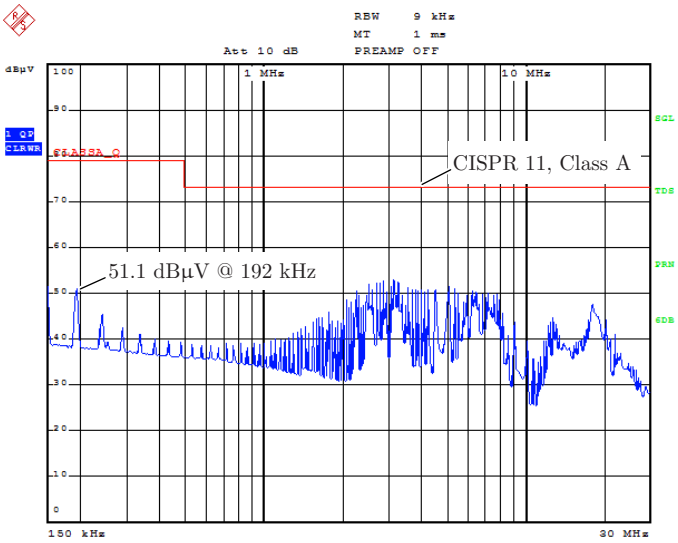


Figure 3.18: Measured DM noise emission of the CVS employing the experimental setup as given in Fig. 3.17 with a DM/CM noise separator. This separator generates an additional attenuation of 6 dB and thus the actual DM noise emission at the frequency of the fourth switching harmonic (= 192 kHz) is 51.1 dBµV + 6 dB = 57.1 dBµV. The attenuations of 10 dB of the LISN circuits and of 10 dB of the impulse limiter are compensated by the −20 dB of the EMI test receiver (cf. Fig. 3.17).

The CM choke at the output of the two-stage *LC* filter (cf. Fig. 3.17) adds 1.8 µH of DM filtering inductance through its leakage inductance. At the frequency of $4 \cdot 48$ kHz = 192 kHz, where the first peak of the measured DM noise occurs, this results in a impedance magnitude of $2 \cdot \pi \cdot 192\ \text{kHz} \cdot 1.8\ \mu\text{H} = 2.2\ \Omega$. This additional impedance is negligible compared to the 50 Ω of the LISNs.

As can be seen from **Fig. 3.18**, at 192 kHz (fourth switching frequency harmonic and / or first harmonic located in the EMI measurement range) the measured DM noise emission is

$$\text{Meas. DM noise (@ 192 kHz)} = 57.1\ \text{dB}\mu\text{V}. \tag{3.41}$$

The additional attenuation of 6 dB of the noise separator depicted in Fig. 3.17 is counterbalanced by adding 6 dB to the measurement results

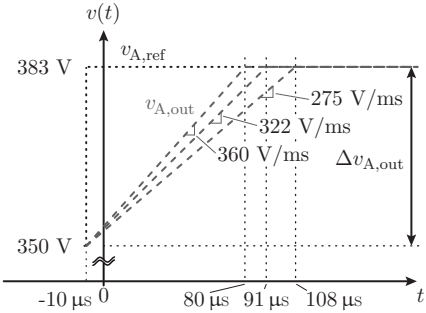


Figure 3.19: Best case, nominal case, and worst case slew rates, i.e. 360 V/ms, 322 V/ms, and 275 V/ms, respectively, obtained for the component values of the final filter design considering tolerances of ±10% for the inductances and ±20% for the capacitances. The tolerance of the damping resistor $R_{\mathrm{D},2}$ is neglected. It is noted that for the hardware realization of the filter the components were selected carefully such that the calculated and measured values fit closely as shown in Tab. 3.4. This minimizes the impact of component tolerances on the output filter performance leading to a good agreement between measured and calculated performance indices (cf. Tab. 3.5).

a posteriori (cf. Fig. 3.18). Thus, in (3.41), the actually generated noise level is given. The EMI measurement is conducted for a DC link voltage of $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800$ V, for an output voltage of $v_{\mathrm{A,out}} = V_{\mathrm{A,out,n}} = 230$ V (cf. Section 3.2.2) and at a reduced output power of 3.3 kW/6 = 550 W because the emitted noise spectrum is independent of the load current (the inductors are built with ferrite and an air-gap), i.e. show a largely linear behavior. The measured noise emission of 57.1 dBµV deviates by 5.3 dB from the calculated value of 62.4 dBµV (cf. Tab. 3.5), because the computation is based on a worst case consideration, for which all amplitudes of the harmonics are summed up within the 9 kHz band of the test receiver (cf. [187]).

3.2.5 Design Space with Component Tolerances

The values of the passive components of the investigated two-stage *LC* output filter, in particular inductances and capacitances, are subject to tolerances. The impacts of these tolerances on the resulting DS are

Table 3.7: Best case, nominal case, and worst case performance indices calculated for the component values of the final filter design, i.e. $L_{\mathrm{DM},1} = 154\ \mu\mathrm{H}$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F}$, $L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H}$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F}$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H}$, and $R_{\mathrm{D},2} = 1.34\ \Omega$ (cf. Tab. 3.4), and for inductance tolerances of ±10% and capacitance tolerances of ±20%. The last column summarizes the worst case component values. The tolerance of $R_{\mathrm{D},2}$ is neglected.

Requirement	*Best case*	*Nominal case*	*Worst case*
Out. voltage slew rate SR	360 V/ms	322 V/ms	275 V/ms
Trans. out. voltage dip → Z_{step}	4.1 Ω	4.7 Ω	5.4 Ω
Bridge-leg current ripple Δi_{A0}	10.8 A	12.0 A	13.4 A
Out. voltage ripple $\Delta v_{\mathrm{A,out}}$	1.4 V	2.5 V	5.6 V
Cap. reactive power Q_{cap}	117 VA	147 VA	175 VA
Conducted EMI limit	60.4 dBµV	62.4 dBµV	71.1 dBµV

disregarded in Sections 3.2.2 and 3.2.3, to focus on the derivation of the DS and the subsequent ρ–η Pareto optimization.[15] This subsection describes a method, which considers the implications of tolerances of the component values on the resulting DS.

To guarantee that all the required properties of the AC source (cf. Tab. 3.2) can be fulfilled for real components with tolerances, the calculation of the DS needs to include the variation of the component values, because higher or lower values than the nominal (or desired) values affect the filter performance indices (cf. Tab. 3.5), as exemplary shown in **Fig. 3.19** for the slew rate. The inductors and capacitors are assumed to have tolerances of ±10% and ±20%, respectively,[16] while

[15] The hardware realization of the two-stage LC output filter (cf. Tab. 3.4) uses carefully selected components, such that calculated and measured values agree. For this, the air-gaps of the inductors were tuned to achieve the calculated inductances and the capacitors with the best fitting capacitances were selected from a set of available capacitors.

[16] The inductor is realized with an air gap (cf. Tab. 3.4) and hence its inductance is roughly proportional to the length of the air gap. It is assumed that the air

Table 3.7: Continued.

Requirement	*Worst case component values*
Out. voltage slew rate SR	$L_{\mathrm{DM},1} = 154\ \mu\mathrm{H} + 10\%, L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H} + 10\%$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F} + 20\%$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F} + 20\%$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H} + 10\%$, $R_{\mathrm{D},2} = 1.34\ \Omega$
Trans. out. voltage dip $\rightarrow Z_{\mathrm{step}}$	$L_{\mathrm{DM},1} = 154\ \mu\mathrm{H} + 10\%, L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H} + 10\%$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F} - 20\%$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H} + 10\%$, $R_{\mathrm{D},2} = 1.34\ \Omega$
Bridge-leg current ripple Δi_{A0}	$L_{\mathrm{DM},1} = 154\ \mu\mathrm{H} - 10\%, L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H} - 10\%$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F} - 20\%$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H} - 10\%$, $R_{\mathrm{D},2} = 1.34\ \Omega$
Out. voltage ripple $\Delta v_{\mathrm{A,out}}$	$L_{\mathrm{DM},1} = 154\ \mu\mathrm{H} - 10\%, L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H} - 10\%$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F} - 20\%$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H} + 10\%$, $R_{\mathrm{D},2} = 1.34\ \Omega$
Cap. reactive power Q_{cap}	$C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F} + 20\%$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F} + 20\%$
Conducted EMI level	$L_{\mathrm{DM},1} = 154\ \mu\mathrm{H} - 10\%, L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H} - 10\%$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F} - 20\%$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H} + 10\%$, $R_{\mathrm{D},2} = 1.34\ \Omega$

the tolerance of the damping resistor $R_{\mathrm{D},2}$ is neglected. Thus, the two-stage output filter contains five components whose values vary by ±10% or ±20%. With these ranges of component value variation the best case (i.e. highest slew rate) and the worst case (i.e. lowest slew rate) can be determined as illustrated in Fig. 3.19 for the nominal filter values which result from the optimization procedure, i.e. $L_{\mathrm{DM},1} = 154\ \mu\mathrm{H}$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F}$, $L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H}$, $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F}$, $L_{\mathrm{D},2} = 22.4\ \mu\mathrm{H}$, and $R_{\mathrm{D},2} = 1.34\ \Omega$ (cf. Section 3.2.3 and Tab. 3.4). The worst case, for example, is obtained for the values of $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, $L_{\mathrm{D},2}$, $C_{\mathrm{DM},1}$, and $C_{\mathrm{DM},2}$ being 10% and 20% higher, respectively.

With the above mentioned component tolerances, the best and worst case of the performance indices can be calculated for each criteria as summarized in **Tab. 3.7**. In the last column, the filter component

gap length is 1 mm which can be adjusted within ±0.1 mm, i.e. within ±10%, and hence the tolerance of the inductance is ±10%. The tolerance of the capacitance is according to [199] ±20%.

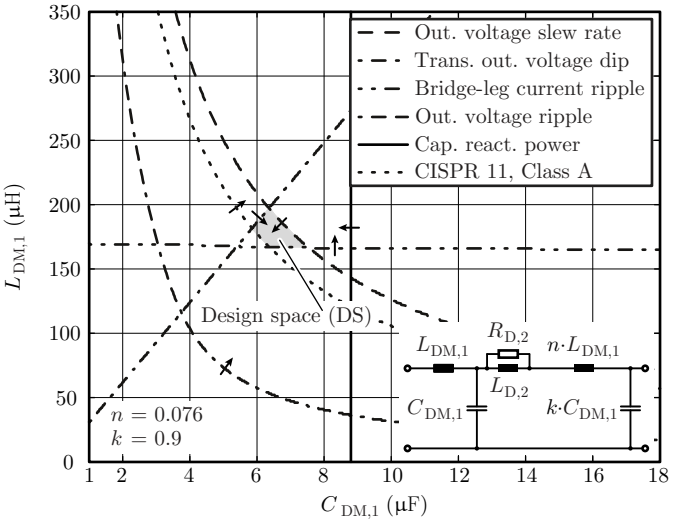


Figure 3.20: DS for the two-stage LC output filter [cf. Fig. 3.2(b)] for nominal $n = L_{DM,2}/L_{DM,1} = 0.076$ and $k = C_{DM,2}/C_{DM,1} = 0.9$, which results from the optimization in Section 3.2.3 (cf. Tab. 3.4) for the worst case combinations of component values, according to Tab. 3.7, if tolerances of ±10% are considered for the inductances and ±20% for the capacitances ($R_{D,2}$ has no tolerance). The resulting DS is considerably smaller than the DS calculated for the exact component values (cf. Fig. 3.7).

values for which the worst case is obtained are given for each criteria. It can be seen from Tab. 3.7 that the combination of the component's tolerances leading to the worst case is not the same for all criteria. Therefore, to ensure that all the required properties of the AC source can be met in any case, for each criteria the combination of component tolerances resulting in the worst case is considered in the calculation of the resulting DS given in **Fig. 3.20**. Compared to the DS calculated with the nominal (exact) component values (cf. Fig. 3.7), the DS with component tolerances (cf. Fig. 3.20) is considerably smaller.

3.2.6 Summary

In this section, the design space (DS) concept is utilized to provide a basis for the multi-objective optimization of the output filter of a 10 kW, four-quadrant, three-phase, switch-mode controllable AC voltage source (CVS) with $f_{\mathrm{s,out}} = 48\,\mathrm{kHz}$ and $[0, 350\,\mathrm{V}]$ output phase voltage range. The DS concept allows simultaneously considering multiple criteria that result from application-oriented specifications of the CVS such as

- minimum output voltage slew rate,
- maximum transient output voltage dip,
- maximum bridge-leg output current ripple,
- maximum output voltage ripple,
- maximum capacitive reactive power, and
- limits of conducted EMI noise emissions.

These specifications lead to corresponding limits for the output filter component values. The intersection set of all limits, for which all requirements can be fulfilled, defines the DS. The strength of the presented approach is that a clear graphical representation of the DS is obtained, e.g. the limits can be drawn in the L–C plane for a single-stage LC filter, which typically would be considered in a first step of the filter analysis. From the drawn limits, it can then directly be identified that, for the case at hand, the resulting DS of a single-stage filter is empty because the compliance to the limits of conducted EMI does not allow a common intersection of all limits. Thus, the number of degrees of freedom needs to be increased, which can be achieved by introducing a two-stage LC filter. This results in a nonempty four-dimensional DS. To fully exploit this DS, a multi-objective optimization is performed and the ρ–η Pareto front (PF) is determined, which allows identifying the most compact and / or most efficient filter designs among all possible filter realizations with parameters in the DS. The PF calculation of the two-stage LC output filter involves nearly $1.1 \cdot 10^{12}$ different filter designs. To drastically reduce this very high number, a design procedure benefiting from pre-optimized component designs is discussed in detail. From the optimization results, the Pareto optimal filter design with the

highest power density is selected, resulting in $\rho = 14.6\,\mathrm{kW/dm^3}$ for $\eta = 99.4\%$. As verified by measurements on a filter hardware demonstrator, the optimal filter ensures compliance to all specifications of the CVS.

The scientific results obtained in this section are printed in [205,206] (see also "List of Publications" on page 337).

Concerning an increase of the number of LC filter stages, i.e. leading to a three-, four-, etc. stage LC filter, it is remarked that, if a single LC filter stage is "distributed" to LC filter stages of equal component ratings (L/n, C/n), finally a lossless transmission line equivalent circuit model is obtained for $n \to \infty$. Such a circuitry would, however, no longer show a low-pass filter characteristic, which is required regarding conducted EMI noise suppression. Furthermore, the characteristic impedance of such a transmission line would be symmetrical, which may be too low considering the peak-to-peak bridge-leg output current ripple but too high regarding the filter output impedance seen by the load. As a consequence, multi-stage LC filters are usually dimensioned such that the characteristic impedances $Z_{0,i} = \sqrt{L_i/C_i}$ of the individual stages i are lowered from the filter input side towards the output side, as it is the case for the filter designed with the help of the elaborated approach (approximately same values of $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F}$ and $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F}$, but significantly lower inductance $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H}$ as compared to $L_{\mathrm{DM},1} = 154\,\mu\mathrm{H}$).

Moreover, in terms of output voltage control, it is often desired that the output voltage tightly follows the reference without a large overshoot in case of a reference step. A Bessel filter, which is characterized by no output voltage overshoot [182], would theoretically be the ideal solution. Unfortunately, a necessary condition to achieve such a filter type, for a resistive load $R_{\mathrm{A,load}}$, is that the characteristic impedances for a two-stage LC filter for instance fulfill

$$Z_{0,1} = \sqrt{\frac{L_{\mathrm{DM},1}}{C_{\mathrm{DM},1}}} = \frac{210 \cdot \left(1501 + 359 \cdot \sqrt{105}\right)}{704969} \cdot R_{\mathrm{A,load}}^2 \approx 1.5 \cdot R_{\mathrm{A,load}}^2 \tag{3.42}$$

and

$$Z_{0,2} = \sqrt{\frac{L_{\mathrm{DM},2}}{C_{\mathrm{DM},2}}} = \frac{2}{89} \cdot \left(61 + 7 \cdot \sqrt{105}\right) \cdot R_{\mathrm{A,load}}^2 \approx 3.0 \cdot R_{\mathrm{A,load}}^2, \tag{3.43}$$

where $L_{\mathrm{DM},1}$–$C_{\mathrm{DM},1}$ and $L_{\mathrm{DM},2}$–$C_{\mathrm{DM},2}$ build the LC stage at the filter input and output, respectively.[17] According to (3.42) and (3.43), it follows that $Z_{0,2} \approx 2 \cdot Z_{0,1}$, which may lead to a too low slew rate of the output voltage and / or a too high output voltage dip / rise after a load step[18] and which is in contradiction to the conclusion drawn in the paragraph above.

It should finally be noted that the resulting filter design is also advantageous concerning output voltage control. Because the resonant frequency of the first filter stage is by a factor of roughly 7 lower than the one of the second filter stage, the second filter stage can be omitted in a first step, i.e. the controller design can be carried out assuming a single-stage LC filter. The closed control loop will therefore show a limited gain at frequencies higher than the corner frequency of the first filter stage. Accordingly, the second filter stage cannot be dynamically compensated, which requires to add the passive RL damping.

[17] To achieve a Bessel type filter, in addition to (3.42) and (3.43), the ratios of the inductance and capacitance values of the two filter stages need to comply with $L_{\mathrm{DM},2}/L_{\mathrm{DM},1} = 4/\sqrt{105} \approx 0.4$ and $C_{\mathrm{DM},2}/C_{\mathrm{DM},1} = \left(4 \cdot (-840 + 121 \cdot \sqrt{105})\right)/7921 \approx 0.2$.

[18] Component values for a Bessel filter loaded with $R_{\mathrm{A,load}} = 15.9\,\Omega$ for (a) the same inductance $L_{\mathrm{DM},1} = 154\,\mu\mathrm{H}$ and (b) the same output capacitance $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F}$ than designed (cf. Tab. 3.4):
(a) $L_{\mathrm{DM},1} = 154\,\mu\mathrm{H}$, $C_{\mathrm{DM},1} = 395\,\mathrm{nF}$, $L_{\mathrm{DM},2} = 60\,\mu\mathrm{H}$, and $C_{\mathrm{DM},2} = 81\,\mathrm{nF}$;
(b) $L_{\mathrm{DM},1} = 7.9\,\mathrm{mH}$, $C_{\mathrm{DM},1} = 20\,\mu\mathrm{F}$, $L_{\mathrm{DM},2} = 3.1\,\mathrm{mH}$, and $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F}$.

3.3 Output Stage – Single-Phase Control

For the initially considered four-quadrant, three-phase plus neutral conductor, three-level T-type voltage source converter output stage given in Fig. 3.1(a) and the parameters of the two-stage LC filter calculated in the previous section, the most suitable control structure is derived in the following. In a next step and as presented in Section 3.4, the results obtained in this section are applied to the three-phase four-leg realization of the CVS's output stage [cf. Fig. 3.1(b)]. **Tab. 3.8** repeats the basic electrical specifications of this power converter and **Tab. 3.9** summarizes the values of the filter components.

The key components of the control structures optimized in this section are the controllers themselves, which are implemented on a digital control platform, i.e. only digital controllers are considered. The controllers finally provide the input signals to the PWM units that generate the gate signals for the transistors shown in **Fig. 3.26**. On the basis of [207], the controllers can be grouped into linear and non-linear controllers.

The most frequently used *linear controllers* in power electronics are proportional (P) and proportional-integral (PI) controllers [183, 208–210]. Commonly accepted reasons for their widespread uses are simplicity, as pointed out in [211], and the well understood and accepted control theory related to the design and the analysis of power electronic systems controlled with such controllers, e.g. system design with gain and phase margins [212]. Further linear controllers include dead beat [213, 214] and state feedback controllers [215], such as linear quadratic regulator (LQR) and linear quadratic Gaussian (LQG) controllers [212]. A dead beat controller is a digital single-input single-output controller, which features the fastest response of the controlled variable for a digital implementation [216]. Dead beat controllers, however, are sensitive to model uncertainties, parameter mismatches, and measurement noise [217], which may make additional measures necessary, e.g. employing disturbance observers [211, 217]. Great disturbances, furthermore, force the dead beat controller to output very high values of the actuating variable [218].

A different prominent member that belongs to the group of linear controllers is the linear state feedback controller. It determines its actuating variable based on the values of multiple states of the controlled system, obtained by means of measurements and / or estimation [215],

Table 3.8: Electrical specifications of the power converter considered for the realization of the CVS's output stage [cf. Fig. 3.1(a)]. The maximum DC link voltage, $V_{\mathrm{dc,max}} = 800$ V, is applied if the CVS is required to generate large-signal excitations with high dynamics. The nominal DC link voltage, $V_{\mathrm{dc,n}} = 700$ V, is used for less demanding operation and features a higher efficiency.
[1)] line-to-neutral; [2)] see Tab. 3.1.

Nominal output power, $P_{\mathrm{out,n}}$	10 kW
Nominal rms output voltage, $V_{\mathrm{A,out,n}}$ [1)]	230 V
Nominal peak output voltage, $V_{\mathrm{A,out,n,pk}}$ [1)]	325 V
Max. peak output voltage, $V_{\mathrm{A,out,max,pk}}$ [1)]	350 V
Nominal DC link voltage, $V_{\mathrm{dc,n}} = V_{\mathrm{dc,1,n}} + V_{\mathrm{dc,2,n}}$	700 V
Max. DC link voltage, $V_{\mathrm{dc,max}}$	800 V
Nominal rms output current, $I_{\mathrm{A,out,n}}$	14.5 A
Nominal peak output current, $I_{\mathrm{A,out,n,pk}}$	20.5 A
Output frequency, f_{out}	$0 - 300$ Hz [2)]
Switching frequency, $f_{\mathrm{s,out}}$	48 kHz
Sampling frequency, f_0	96 kHz
Efficiency, $\eta_{\mathrm{out,n}}$	$\geq 97.5\%$ [2)]

Table 3.9: Component values of the two-stage LC filter with passive series RL damping of the second filter stage [cf. Fig. 3.2(b)], as derived in Section 3.2.

$L_{\mathrm{DM,1}}$	154.2 µH
$C_{\mathrm{DM,1}}$	4.7 µF
$L_{\mathrm{DM,2}}$	11.7 µH
$C_{\mathrm{DM,2}}$	4.1 µF
$L_{\mathrm{D,2}}$	22.4 µH
$R_{\mathrm{D,2}}$	1.34 Ω

and allows the controller to simultaneously monitor and correct the values of multiple system states. This simultaneous kind of processing, however, complicates the design, tuning, and robustness analysis of the controller [212].

In addition to these control concepts, numerous references, includ-

ing [13, 155, 219–221], document the advantageous properties of repetitive and proportional-resonant controllers and synchronously working control concepts in the *dq* reference frame to eliminate steady-state errors and / or to achieve a frequency selective elimination of harmonics for systems generating periodic output signals. Such control concepts, however, are considered to be less suitable in this particular case, since the CVS needs to be capable of generating arbitrary (including heavily unbalanced three-phase or even single-phase) output voltages.

A multitude of different *non-linear controllers* are documented in the context of inverter control. This includes hysteresis [222], sliding mode [8, 223, 224], fuzzy [225, 226], non-linear state-space [227], predictive [8, 228–231], and adaptive controllers [226, 232–234]. Compared to the standard approach with P- and PI-controllers it becomes considerably more difficult for the engineer to design a non-linear controller and to verify the properties of the closed control loop, in particular with respect to stability and robustness[19] [183, 208].

A buck-type power converter, essentially present in Fig. 3.2(b), can, in principle, be controlled with solely an output voltage controller, e.g. a PI-controller, provided that the resonances of the output filter are sufficiently attenuated. In [236], it is shown that it is even possible to achieve almost time-optimal reactions to load transients if a single modified PI-controller controls the output voltage of a buck converter that is composed of a power stage and a single-stage *LC* filter (this modified PI-controller simultaneously considers the output voltage and an estimate of the filter capacitor current). In particular in the light of [236], further improvements possibly achievable with advanced control concepts remain unclear to a certain extent. Even though comparisons of control performances achieved with conventional PI-controllers to advanced controllers are found in literature, e.g. [226, 228, 231–233], the selected conventional realizations are either not explained in detail, not fully optimized, or the respective discussion reveals that the conventionally controlled system does not incorporate load current and reference voltage feedforwards and / or delay compensations, which, in this work, are both found to be crucial for obtaining fast responses with little output-voltage overshoots.

For this reason and due to P- and PI-controllers being well under-

[19] An exception is the hysteresis controller, which is not further considered in this work because, in its simplest form, a changing switching frequency results [222]. Constant switching frequency is only obtained if the hysteresis band is continuously adapted to the actual operating conditions [235].

stood and accepted by design engineers, this section details the optimizations of P and PI-controllers of three control structures suitable for the considered CVS such that, in the events of voltage reference and load steps, the output voltage is stabilized within the minimum possible duration (for a given maximum transient overshoot). In contrast to [236], this work investigates the control of an inverter circuit with a two-stage LC filter, i.e. an $LCLC$ filter, for a wide range of operating conditions and does not rely on the values of parasitic components. Since the CVS may be operated with a UPS [8], a solar inverter [9], or another CVS [1] being connected, the controller design takes different load conditions, including constant active power loads, into account. In this regard, the small-signal representations of constant-active-power loads are operating-point-dependent negative load resistances [33, 237–240], which are found to destabilize the output filter, and are, thus, of particular interest with respect to stable and robust converter operation.

In the following, Section 3.3.1 presents the derivations of the three considered control structures, which take the possible presence of a constant power load and the corresponding negative small-signal load resistance values [237,241] into consideration. The optimizations of the three control structures are detailed in Section 3.3.3 and verified by means of experimental results in Section 3.3.4. For the given specification and filter components, in particular for the given range of small-signal load resistances including negative values, it is shown that the controllers stabilize the output voltage within only a few switching periods.[20] The obtained results, thus, represent an excellent basis for industrial designs or for future comparisons to advanced, e.g. non-linear and / or adaptive, control concepts.

3.3.1 Derivation of the Investigated Control Structures

This subsection derives the control structures considered for each phase of the CVS with the two-stage LC filter depicted in Fig. 3.1(a). These control structures are the basis for the optimization detailed in Section 3.3.3. *Only phase A is considered throughout this section,* since each phase is controlled independently. The obtained results are di-

[20] Within 97 µs (approx. 4.7 switching periods) in the event of a reference voltage step at rated output power and within 49 µs (approx. 2.4 switching periods) in case of a load step ($R_{\mathrm{A,load}}$ changes from 22.2 Ω to 15.9 Ω).

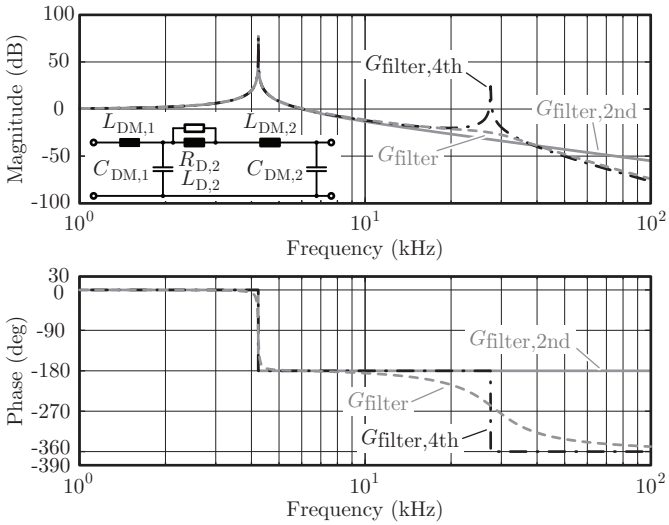


Figure 3.21: Bode plots of accurate and simplified input-to-output transfer functions of the filter without load: amplitude response (top) and phase response (bottom). G_{filter} refers to the accurate transfer function with series RL damping of the second filter stage [cf. Fig. 3.1(a)] $G_{\text{filter,2nd}}$ is the transfer function of a single undamped second-order LC low-pass filter stage (cut-off frequency is 4.2 kHz), and $G_{\text{filter,4th}}$ denotes the transfer function of two undamped second-order LC filter stages with cut-off frequencies of 4.2 kHz and 27.5 kHz, respectively.

rectly applicable to phases B and C.

The two-stage LC filter, optimized in Section 3.2, is essentially composed of two LC filter stages. Due to the relatively large value of $C_{\text{DM,2}} \approx C_{\text{DM,1}}$ (cf. Tab. 3.9) and the low inductances of the second filter stage, $L_{\text{DM,2}} + L_{\text{D,2}} \ll L_{\text{DM,1}}$, the two filter stages cannot be looked at independent from each other. **Fig. 3.21** depicts the Bode diagram of the two-stage LC filter's input-to-output voltage transfer function, G_{filter}, with a passive series $R_{\text{D,2}}L_{\text{D,2}}$ damping branch [cf. Fig. 3.1(a)]. At no load this transfer function has one real zero at -59.8×10^3 s^{-1}

and five poles at

$$\begin{aligned} s_1 &= -75.8 \times 10^3 \text{ s}^{-1}, \\ s_{2,3} &= (-49.1 \pm \text{j}\,173) \times 10^3 \text{ s}^{-1}, \\ s_{4,5} &= \left(-164 \pm \text{j}\,26.6 \times 10^3\right) \text{ s}^{-1}. \end{aligned} \tag{3.44}$$

The real pole, s_1, approximately compensates the real zero and the remaining complex conjugated pole pairs correspond to resonance frequencies of $f_1 = 4.2$ kHz and $f_2 = 27.5$ kHz, respectively. With the damping network being neglected, the considered output filter can be approximated with the series connection of two reactionless second-order low-pass filters according to

$$G_{\text{filter,4th}}(s) = \frac{1}{1 + \left(\frac{s}{2 \cdot \pi \cdot f_1}\right)^2} \frac{1}{1 + \left(\frac{s}{2 \cdot \pi \cdot f_2}\right)^2} \tag{3.45}$$

(cf. Fig. 3.21).

Besides these findings two further important properties are associated with this output filter.

1. The first crossover frequency, $f_1 = 4.2$ kHz, is less than the achieved control bandwidths for all considered control structures, which, in anticipation of the results presented in Section 3.3.3, are in the range between 6 kHz and 7 kHz. It is thus possible to attenuate the resonance at f_1 by means of active damping.

2. The second crossover frequency, $f_2 = 27.5$ kHz, is greater than the achieved control bandwidths and active damping cannot be applied. For this reason passive damping is considered, which is effectively achieved with the $R_{\text{D},2}L_{\text{D},2}$ damping network depicted in Fig. 3.21.

According to Fig. 3.21, a single second-order low-pass filter with cut-off frequency f_1, e.g. achieved with $L_1 = 161$ µH $\approx L_{\text{DM},1}$ and $C_1 = 8.8$ µF, can be used to approximate the transfer function of the output filter for frequencies up to the maximum of the achieved control bandwidth of 7.2 kHz. For this reason, the second filter stage is first disregarded in Section 3.3.1 to allow for a simplified derivation of the considered control structures. Still, the second filter stage introduces a phase shift between its input and output voltages, v_{A1} and $v_{\text{A,out}}$ in **Fig. 3.26(a)**, also at frequencies below 7.2 kHz, which is accounted for in Section 3.3.1 and leads to a refinement of the control structures.

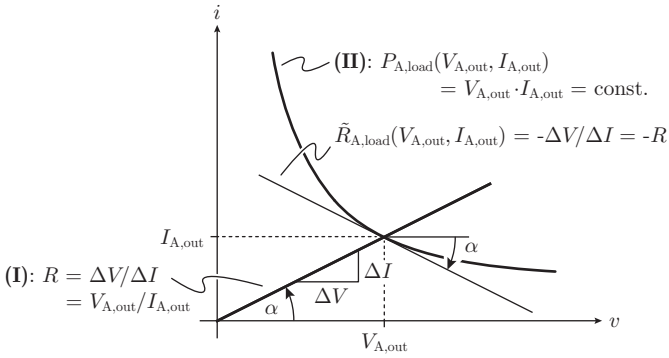


Figure 3.22: Voltage-current characteristic of **(I)** a resistor with resistance R and **(II)** a constant active power load with $P_{load} = \text{constant}$. The slope of the load characteristic, $\mathrm{d}V/\mathrm{d}I$, evaluated at the operating point defined with $V_{A,out}$ and $I_{A,out}$, gives the small-signal load resistance [237]. It can be shown that the small-signal resistance at the operating point ($V_{A,out}$, $I_{A,out}$) of the constant active power load is equal to the negative resistance of a linear load resistor with $R = V_{A,out}/I_{A,out}$.

The CVS may be operated with passive and active loads, e.g. constant power loads, within the limits specified in Tab. 3.8. By way of example, **Fig. 3.22** illustrates the voltage-current characteristic of a constant active power DC load connected to phase A of the CVS [curve (II) in Fig. 3.22] and the derivation of the corresponding negative and operating point dependent small-signal equivalent resistance,

$$\tilde{R}_{A,load} = \frac{\mathrm{d}v_{A,out}}{\mathrm{d}i_{A,out}} = -\frac{V_{A,out}^2}{P_{A,load}} = -\frac{V_{A,out}}{I_{A,out}} = -R \text{ [237]}. \qquad (3.46)$$

With $P_{A,load} = V_{A,out} \cdot I_{A,out}$ expression (3.46) can be converted to $\tilde{R}_{A,load} = -V_{A,out}/I_{A,out}$, i.e. the small-signal model of a constant active power load at a certain operating point, defined with $V_{A,out}$ and $I_{A,out}$, is a resistance and its value is equal to the negative resistance value of a load resistor, R, at the same operating point [curve (I) in Fig. 3.22].

A detailed investigation of the small-signal properties of three-phase AC loads and single-phase loads (DC and AC), reveals that the small-

signal load resistance, $\tilde{R}_{\mathrm{A,load}}$, changes within the range

$$\frac{1}{-15.9\ \Omega} \leq \frac{1}{\tilde{R}_{\mathrm{A,load}}} \leq \frac{1}{15.9\ \Omega}, \tag{3.47}$$

for converter operation with the following loads:

- three-phase symmetric resistive AC loads with $P_{\mathrm{load}} = P_{\mathrm{out,n}} = 10\,\mathrm{kW}$ and $V_{X,\mathrm{out}} \geq V_{X,\mathrm{out,n}} = 230\,\mathrm{V}$ ($X = A, B, C$; rms, line-to-neutral),
- three-phase symmetric constant active power AC loads[21] with $P_{\mathrm{load}} = P_{\mathrm{out,n}} = 10\,\mathrm{kW}$ and $V_{X,\mathrm{out}} \geq V_{X,\mathrm{out,n}} = 230\,\mathrm{V}$ ($X = A, B, C$; rms, line-to-neutral),
- single-phase resistive loads (AC or DC) with $P_{\mathrm{A,load}} = 3.33\,\mathrm{kW}$ (in average or continuous) and $V_{\mathrm{A,out}} \geq V_{\mathrm{A,out,n}} = 230\,\mathrm{V}$ (rms or DC, line-to-neutral),
- single-phase constant active power loads (AC or DC)[21] with $P_{\mathrm{A,load}} = 3.33\,\mathrm{kW}$ (in average or continuous) and $V_{\mathrm{A,out}} \geq V_{\mathrm{A,out,n}} = 230\,\mathrm{V}$ (rms or DC, line-to-neutral).

Simplified Investigation: Single-Stage *LC* Filter

The minimum imaginable control structure is a single-output voltage-control loop, depicted in **Fig. 3.23(a)**, where the PWM unit and the T-type bridge-leg are replaced by a controlled voltage source. The control structures are investigated in the Laplace domain, and, therefore, the following figures in this section with control parts use capital letters for all currents and voltages. In a first step and to obtain simple as well as comprehensive relationships between important system quantities, it is assumed that the time delay due to the digital control (cf. Section 3.3.1) can be perfectly compensated. Conventional P- and PI-controllers[22] cannot stabilize this system for all regarded load con-

[21] A constant active power load can be realized with a single- / three-phase converter which measures its input phase voltage / voltages v_{in} and adjusts its input phase current / currents i_{in} such that the instantaneous input power $p(t) = v_{\mathrm{a,in}}(t) \cdot i_{\mathrm{a,in}}(t) + v_{\mathrm{b,in}}(t) \cdot i_{\mathrm{b,in}}(t) + v_{\mathrm{c,in}}(t) \cdot i_{\mathrm{c,in}}(t) = \text{const.}$ for a three-phase system or the average input power $\langle p_{\mathrm{in}}(t) \rangle_{T_{\mathrm{f}}} = \langle v_{\mathrm{in}}(t) \cdot i_{\mathrm{in}}(t) \rangle_{T_{\mathrm{f}}} = \text{const.}$ (over one fundamental period T_{f}) for a single-phase system. It is assumed here that the adjustment of $i_{\mathrm{a,in}}$, $i_{\mathrm{b,in}}$, and $i_{\mathrm{c,in}}$ for the three-phase system is instantaneous, i.e. the converter has an infinite control bandwidth.

[22] Controllers with a derivative (D) component are usually avoided in power electronics, due to their sensitivity to measurement noise [209].

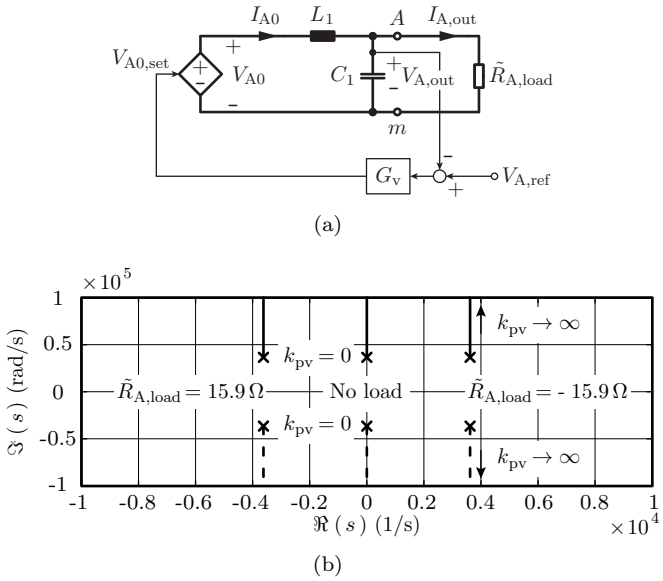


Figure 3.23: (a) Output voltage control structure with minimum complexity applied to a single-stage LC filter. The controller G_v alters the adjustable voltage source such that the output follows the desired reference voltage, $V_{A,ref}(s) = \mathcal{L}\{v_{A,ref}(t)\}$. **(b)** Root locus calculated for the closed-loop transfer function $V_{A,out}(s)/V_{A,ref}(s)$ for $L_1 = 161$ µH, $C_1 = 8.8$ µF, a P-controller, $G_v = k_{pv}$, and for different small-signal load resistances, $\tilde{R}_{A,load}$. Stable operation is only achievable for $\tilde{R}_{A,load} \geq 0$.

ditions (and assumed lossless filter components), due to the filter being undamped and due to possible negative load resistances [cf. (3.47)]. In case of a P-controller, $G_v = k_{pv}$, for example, and for $L_1 = 161$ µH and $C_1 = 8.8$ µF the root locus depicted in **Fig. 3.23(b)** is calculated for the closed voltage-control loop: for $\tilde{R}_{A,load} < 0$ a pole-pair in the right half-plane, of which the real part is independent of k_{pv}, results (for the PI-controller, a similar result is obtained). For this reason multi-loop control structures are considered in the following.

Two-Loop Control Structure The commonly used configuration depicted in **Fig. 3.24(a)** can be used to introduce active damping to

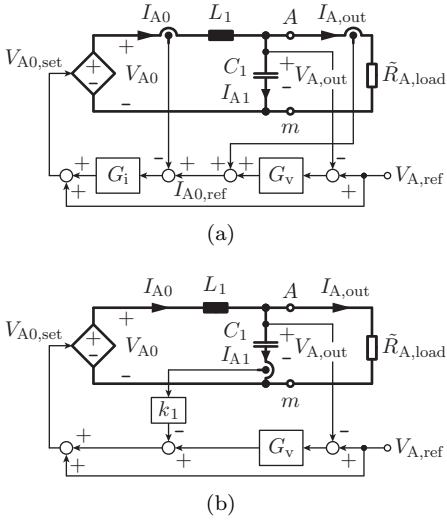


Figure 3.24: (a) Commonly employed configuration with an inner current control loop for I_{A0} and an outer voltage control loop for $V_{A,out}$ to introduce active damping. **(b)** In an alternative implementation, the capacitor current feedback loop emulates a (lossless) resistor that is connected in series to L_1, and, with this, achieves active damping [242].

an undamped LC filter stage [221, 243] and represents the basis of two of the control structures evaluated in the scope of this work. This configuration is composed of an inner current control loop that controls the inductor current I_{A0} and a superordinate output voltage control loop to control $V_{A,out}$. Fig. 3.24(a), furthermore, includes a load current feedforward and a reference voltage feedforward. The summation of the measured output current to the voltage controller's output value establishes the load current feedforward and allows the current controller, G_i, to quickly adapt to a changing load current. The reference voltage feedforward, which adds the reference voltage $V_{A,ref}$ to the output value of the current controller, takes advantage of V_{A0} being a rather linear adjustable voltage source (in terms of an averaged model) and improves the dynamic response of the output voltage when the reference voltage changes.

In the presence of positive and negative small-signal load resis-

tances $\tilde{R}_{\mathrm{A,load}}$, a detailed stability analysis conducted in **Appendix B** identifies a PI-controller to be unsuitable for current control and a P-controller is used, instead. For the voltage control loop a PI-controller is found to be more suitable than a P-controller. Furthermore, the maximum occurring negative load resistance value, here $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$, is identified to be a critical design parameter regarding stable converter operation.

Capacitor Current Feedback Control Structure The capacitor current is an AC current and is equal to the inductor current minus the load current. Its dynamic (AC) component is therefore closely related to the AC components of the inductor and load currents and for this reason overall good control performances (cf. Section 3.3.3) in case of reference and load changes are expected.[23] Furthermore, for the case of no load, the capacitor current feedback emulates a resistor, $R_1 = k_1$, connected in series to L_1, as given in **Fig. 3.25**. This emulated resistor causes no losses (except negligible losses in the current sensor) but still introduces damping. For this reason, stable closed-loop output voltage regulation is feasible with the concept shown in Fig. 3.24(b) even in the presence of a negative small-signal load resistance.

It is noted that the gain k_1 can be adjusted such that the *RLC* filter with transfer function

$$\frac{V_{\mathrm{A,out}}(s)}{V_{\mathrm{k1}}(s)} = \frac{1}{1 + k_1 \cdot C_1 \cdot s + L_1 \cdot C_1 \cdot s^2} = \frac{1}{1 + R_1 \cdot C_1 \cdot s + L_1 \cdot C_1 \cdot s^2} \tag{3.48}$$

shown in **Fig. 3.25(b)** represents a second order Butterworth or Bessel filter as indicated in **Fig. 3.25(c)**:

$$k_1 = \sqrt{2} \cdot Z_0\text{: Butterworth filter,} \tag{3.49}$$

$$k_1 = \sqrt{3} \cdot Z_0\text{: Bessel filter,} \tag{3.50}$$

[23] Alternatively, the measured capacitor current, scaled by k_1, can be considered like a differential (D) component of the output capacitor voltage controller G_{v}, because the capacitor current essentially represents the time derivative of the output voltage $v_{\mathrm{A,out}}$. In contrast to PD and PID controllers, however, this D component is directly obtained by measurement. For this reason, the above mentioned issue regarding the D component's sensitivity to measurement noise does not apply to this configuration.

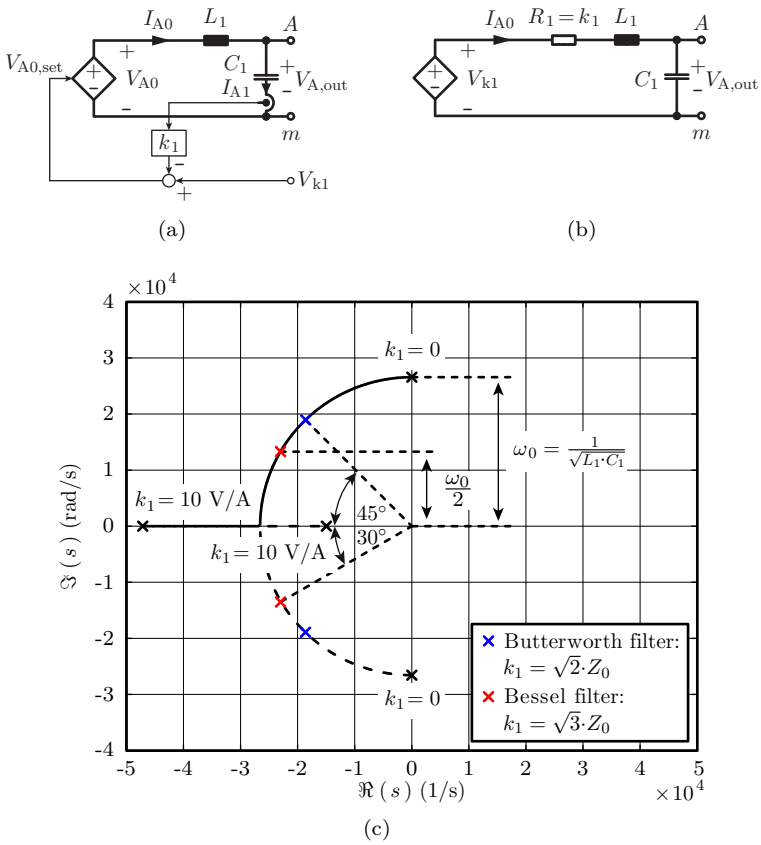


Figure 3.25: **(a)** Capacitor current feedback structure with gain k_1 for a unloaded single-stage LC filter and **(b)** equivalent circuit of (a) for the calculation of the transfer function $V_{A,out}(s)/V_{k1}(s)$ considering the emulated resistance $R_1 = k_1$ in series to L_1. **(c)** Poles of the RLC filter given in (b) for $R_1 = k_1$, $L_1 = 161$ µH, $C_1 = 8.8$ µF, and $k_1 = [0, 10$ V/A$]$.

where

$$Z_0 = \sqrt{\frac{L_1}{C_1}} \tag{3.51}$$

is the characteristic impedance of the LC filter stage.

A further advantage of the concept shown in Fig. 3.24(b) is the property of the capacitor current being a pure AC current, which allows the use of an AC current sensor. The capacitor current feedback control structure, however, features neither inductor nor output current limitation options, since the respective DC current components are unknown.

A detailed stability analysis conducted for this control structure presented in Appendix B reveals that the maximum occurring negative small-signal load resistance value, $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$, is most critical with respect to stable converter operation also for this control structure.

Detailed Investigation: Two-Stage *LC* Filter

According to Section 3.2, the CVS requires a two-stage LC output filter and, hence, additional state variables are available for the control of the output voltage. **Fig. 3.26** depicts the three control concepts considered for evaluation: Fig. 3.26(a) directly applies the control structure of Fig. 3.24(a) to the two-stage filter (in Section 3.3.1 a P-controller has been suggested for current control); **Fig. 3.26(b)** applies the control structure of Fig. 3.24(b) to the two-stage filter and considers both capacitor currents, $I_{\mathrm{A1}}(s)$ and $I_{\mathrm{A2}}(s)$ to take advantage of the additionally available capacitor current;[24] and **Fig. 3.26(c)** is based on the two-loop control structure of Fig. 3.24(a), which employs a P-controller in an inner current control loop and a second P-controller in a superordinate loop that controls the output voltage of the first filter stage, $V_{\mathrm{A1}}(s)$. According to the initial considerations detailed in this section, $V_{\mathrm{A,out}}(s) \approx V_{\mathrm{A1}}(s)$ applies for frequencies up to the output voltage control bandwidth. Any remaining gain and phase errors between $V_{\mathrm{A,out}}(s)$ and $V_{\mathrm{A1}}(s)$ are eliminated with the use of a second voltage controller (PI-controller) for $V_{\mathrm{A,out}}$. The proposed structure prefers the parallel operation of the two voltage controllers to a solution with a third control loop in order to not sacrifice the achievable closed-loop output voltage control bandwidth. For stabilizing $V_{\mathrm{A,out}}$, a PI-controller is used to eliminate steady-state errors of the output voltage. Only a P-controller stabilizes V_{A1} since, in a practical environment, it has been found that the control circuit does not work properly if two integrators are operated in parallel, i.e. the two integrators conflict with each other.

[24] It can be considered that the capacitor current $I_{\mathrm{A1}}(s)$ more reflects the AC component of the inductor current $I_{\mathrm{A0}}(s)$ and $I_{\mathrm{A2}}(s)$ more reflects the AC component of the load current $I_{\mathrm{A,load}}(s)$ due to the separating effects of $L_{\mathrm{DM,2}}$ and $L_{\mathrm{D,2}}$.

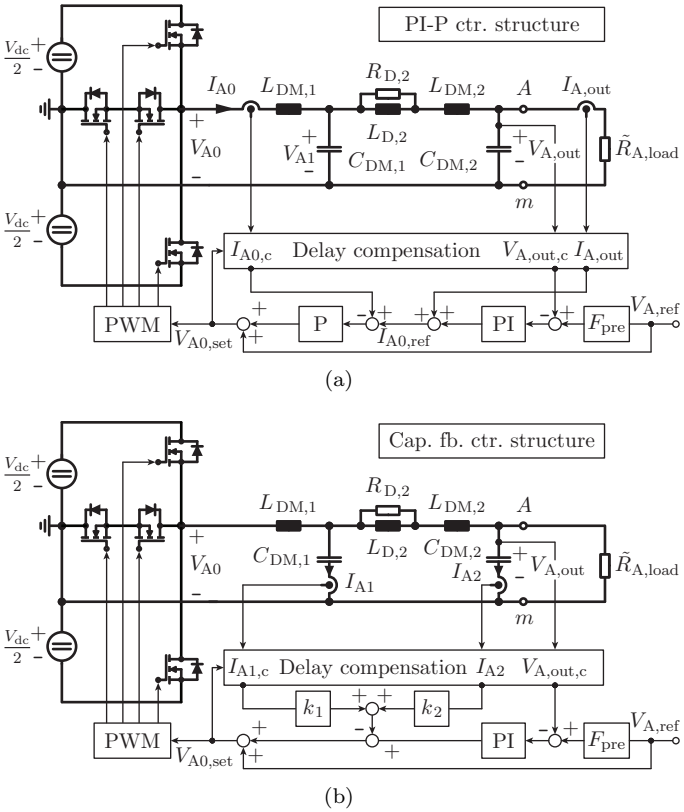
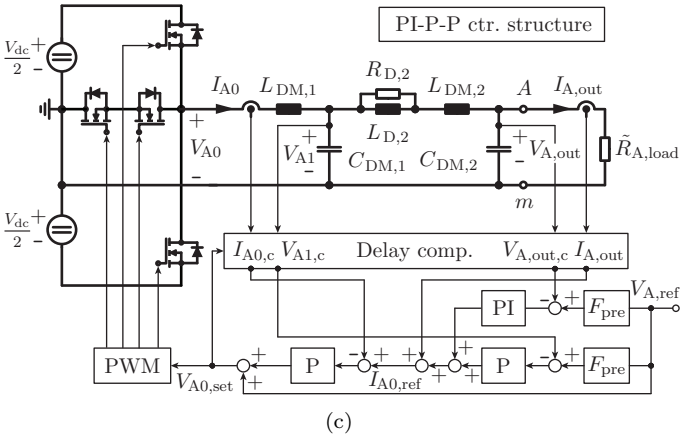


Figure 3.26: Control structures suitable for the two-stage *LC* filter identified in this work: **(a)** PI-P control structure, **(b)** capacitor current feedback control structure, and **(c)** PI-P-P control structure.

The final control structures, shown in Fig. 3.26, include delay compensations to lower the impacts of time delays caused by the digital control system on the achievable output voltage control bandwidth. The delay compensations are implemented according to [244] and detailed in the next subsection. The output current, $I_{A,out}$, is excluded from this prediction, since the output current is mainly used to react on a load change, which the employed algorithm cannot predicted. Moreover, a



(c)

Fig. 3.26: Continued.

prefilter F_{pre}, discussed below, is employed for all control structures of Fig. 3.26 to generate, in the first instance, similar transient errors for the voltage controller in case of a output voltage reference step than in case of a load step.

3.3.2 Small-Signal Modeling

The results of the optimization conducted in Section 3.3.3 are only meaningful if the small-signal models of the different parts of the control concepts depicted in Fig. 3.26 are known and verified. For this reason, this subsection details the small-signal models for the control part and the switching stage.

Digital Controllers, Time Delays, and Delay Compensations

A microcontroller, with Texas Instruments Inc.'s TMS320F28335 and Lattice Semiconductor Corp.'s LFXP2-5E-5TN144C, realizes the prefilter F_{pre}, the digital controllers, the delay compensations, and the PWM units. This work conducts the investigations of the transfer func-

tions in continuous-time and uses the Tustin approximation,

$$s = \frac{2}{T_{0,\mathrm{out}}} \cdot \frac{z-1}{z+1} \quad \Leftrightarrow \quad z = \frac{2 + s \cdot T_{0,\mathrm{out}}}{2 - s \cdot T_{0,\mathrm{out}}}, \tag{3.52}$$

with sampling time $T_{0,\mathrm{out}} = 1/(2 \cdot f_{\mathrm{s,out}})$, to approximately convert discrete-time transfer functions to continuous-time. Thus, all transfer functions that originate from the implementation on the digital control system are first modeled in the discrete-time domain and transformed to the continuous-time domain with (3.52).

The software implementation uses double-update-mode, the sampling time is therefore equal to half a pulse period, $T_{0,\mathrm{out}} = 1/(2 \cdot f_{\mathrm{s,out}})$ $= 10.4\ \mu\mathrm{s}$. The time delay caused by the microcontroller is equal to the sampling time, $T_{\mathrm{d},\mu\mathrm{C}} = T_{0,\mathrm{out}} = 10.4\ \mu\mathrm{s}$, and the corresponding z-transform is z^{-1}. The PWM unit adds another time delay, which, in double-update-mode and in average, is equal to half of the update period, i.e. one quarter of the pulse period, $T_{\mathrm{d,PWM}} \approx T_{\mathrm{s,out}}/4 = 5.2\ \mu\mathrm{s}$ [245, 246]. The z-transform corresponding to this time delay is obtained by means of a Thiran filter [247],

$$\mathcal{Z}\left\{\mathcal{L}^{-1}\left\{\mathrm{e}^{-s \cdot T_{0,\mathrm{out}}/2}\right\}\right\} \approx \frac{z+3}{3 \cdot z + 1}. \tag{3.53}$$

The prefilter is a first-order low-pass filter with time constant T_{pre} and the considered transfer function is

$$F_{\mathrm{pre}}(z) = \left(1 + \frac{2 \cdot T_{\mathrm{pre}}}{T_{0,\mathrm{out}}} \cdot \frac{z-1}{z+1}\right)^{-1}. \tag{3.54}$$

The transfer function of a PI-controller with gain k_{p} and integrator time constant T_{i} is obtained from the discrete time implementation with input e_k, internal summand x_k, and output y_k,

$$x_{k+1} = x_k + \frac{T_{0,\mathrm{out}}}{T_{\mathrm{i}}} \cdot e_{k+1}, \tag{3.55}$$

$$y_{k+1} = k_{\mathrm{p}} \cdot \left(e_{k+1} + x_{k+1}\right), \tag{3.56}$$

which gives the transfer function

$$G_{\mathrm{PI}}(z) = \frac{\mathcal{Z}\{y_k\}}{\mathcal{Z}\{e_k\}} = k_{\mathrm{p}} \cdot \left(1 + \frac{T_{0,\mathrm{out}}}{T_{\mathrm{i}}} \cdot \frac{z}{z-1}\right). \tag{3.57}$$

The implemented delay compensation is based on [244], which is a model-based approach, and predicts the filter currents and voltages that are expected at the time the output voltage changes, i.e.

$$T_\mathrm{d} = T_{\mathrm{d},\mu\mathrm{C}} + T_{\mathrm{d,PWM}} = 1.5 \cdot T_{0,\mathrm{out}} \tag{3.58}$$

ahead in time. This subsection exemplary details the functions implemented for the PI-P structure. **Appendix C** summarizes the functions employed for the capacitor current feedback and the PI-P-P structures.

For the PI-P control structure [cf. Fig. 3.26(a)] the inductor current and the output voltage need to be estimated. A system of two first-order differential equations can be used to describe $i_{\mathrm{A}0}(t)$ and $v_{\mathrm{A,out}}(t)$,

$$\frac{\mathrm{d}i_{\mathrm{A}0}(t)}{\mathrm{d}t} = \frac{v_{\mathrm{A}0}(t) - v_{\mathrm{A}1}(t)}{L_{\mathrm{DM},1}} \approx \frac{v_{\mathrm{A0,set}}(t) - v_{\mathrm{A,out}}(t)}{L_{\mathrm{DM},1}}, \tag{3.59}$$

$$\frac{\mathrm{d}v_{\mathrm{A,out}}(t)}{\mathrm{d}t} \approx \frac{i_{\mathrm{A}0}(t) - i_{\mathrm{A,out}}(t)}{C_{\mathrm{DM},1} + C_{\mathrm{DM},2}}, \tag{3.60}$$

which assumes $v_{\mathrm{A}0}(t) \approx v_{\mathrm{A0,set}}(t)$, $v_{\mathrm{A}1}(t) \approx v_{\mathrm{A,out}}(t)$, and $\mathrm{j} \cdot \omega \cdot (L_{\mathrm{D},2} + L_{\mathrm{DM},2}) \approx 0$ in the considered frequency range. The calculation further assumes that

$$\frac{\mathrm{d}i_{\mathrm{A}0}(t)}{\mathrm{d}t} \approx \frac{i_{\mathrm{A}0}(t + \Delta t) - i_{\mathrm{A}0}(t)}{\Delta t}, \tag{3.61}$$

and

$$\frac{\mathrm{d}v_{\mathrm{A,out}}(t)}{\mathrm{d}t} \approx \frac{v_{\mathrm{A,out}}(t + \Delta t) - v_{\mathrm{A,out}}(t)}{\Delta t} \tag{3.62}$$

apply. With (3.61),

$$t_i = t_0 + i \cdot \Delta t, \;\; 0 \leq i < n, \;\; i \in \mathbb{N}_0, \;\; n \in \mathbb{N}, \;\; \Delta t = \frac{T_\mathrm{d}}{n}, \tag{3.63}$$

and $t \to t_i$ the estimates obtained with (3.59) and (3.60) become

$$\underbrace{i_{\mathrm{A}0}(t_i + \Delta t)}_{\substack{\text{estimated value of} \\ i_{\mathrm{A}0} \text{ at } t \to t_{i+1}}} \approx i_{\mathrm{A}0}(t_i) + \frac{v_{\mathrm{A0,set}}(t_0) - v_{\mathrm{A,out}}(t_i)}{L_{\mathrm{DM},1}} \cdot \Delta t, \tag{3.64}$$

$$\underbrace{v_{\mathrm{A,out}}(t_i + \Delta t)}_{\substack{\text{estimated value of} \\ v_{\mathrm{A,out}} \text{ at } t \to t_{i+1}}} \approx v_{\mathrm{A,out}}(t_i) + \frac{i_{\mathrm{A}0}(t_i) - i_{\mathrm{A,out}}(t_0)}{C_{\mathrm{DM},1} + C_{\mathrm{DM},2}} \cdot \Delta t, \tag{3.65}$$

Table 3.10: Factors $k_{\mathrm{c},1} \ldots k_{\mathrm{c},8}$ [cf. Eqs. (3.66) and (3.67)] used for the delay compensation in the PI-P control structure [cf. Fig. 3.26(a)].

$k_{\mathrm{c},1}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{L_{\mathrm{DM},1}}$
$k_{\mathrm{c},2}$	$-\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{L_{\mathrm{DM},1}}$
$k_{\mathrm{c},3}$	$1 - \frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},4}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},5}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},6}$	$1 - \frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},7}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}+C_{\mathrm{DM},2}}$
$k_{\mathrm{c},8}$	$-\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}+C_{\mathrm{DM},2}}$

which assumes constant values of $v_{\mathrm{A0,set}}$ and $i_{\mathrm{A,out}}$ during $t_0 \leq t < t_0 + T_{\mathrm{d}}$.[25] The expressions given in (3.64) are evaluated n times in an iterative manner and the result can be summarized with

$$\begin{aligned} i_{\mathrm{A0}}(t_0 + T_{\mathrm{d}}) = {} & k_{\mathrm{c},1} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},2} \cdot v_{\mathrm{A,out}}(t_0) + \\ & k_{\mathrm{c},3} \cdot i_{\mathrm{A0}}(t_0) + k_{\mathrm{c},4} \cdot i_{\mathrm{A,out}}(t_0), \qquad (3.66) \\ v_{\mathrm{A,out}}(t_0 + T_{\mathrm{d}}) = {} & k_{\mathrm{c},5} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},6} \cdot v_{\mathrm{A,out}}(t_0) + \\ & k_{\mathrm{c},7} \cdot i_{\mathrm{A0}}(t_0) + k_{\mathrm{c},8} \cdot i_{\mathrm{A,out}}(t_0). \qquad (3.67) \end{aligned}$$

The factors $k_{\mathrm{c},1} \ldots k_{\mathrm{c},8}$ in (3.66) and (3.67) are constant factors, therefore (3.66) and (3.67) can be directly transformed to the z-domain by simply replacing the time domain quantities $v_{\mathrm{A0,set}}(t)$, $v_{\mathrm{A,out}}(t)$, $i_{\mathrm{A0}}(t)$, and $i_{\mathrm{A,out}}(t)$ by their respective z-domain quantities $V_{\mathrm{A0,set}}(z)$, $V_{\mathrm{A,out}}(z)$, $I_{\mathrm{A0}}(z)$, and $I_{\mathrm{A,out}}(z)$. **Tab. 3.10** lists the expressions for all factors, $k_{\mathrm{c},1} \ldots k_{\mathrm{c},8}$, in (3.66) and (3.67) and for $n = 2$, which has been found to yield useful predictions of i_{A0} and $v_{\mathrm{A,out}}$.

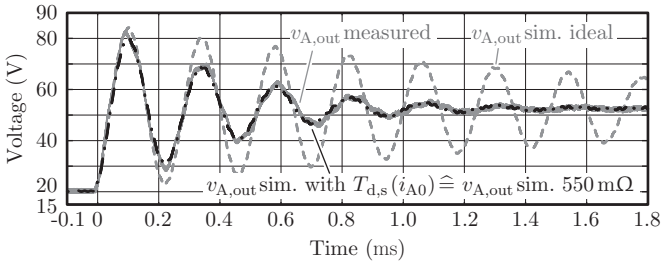


Figure 3.27: Simulated and measured step responses of $v_{A,out}(t)$ for $V_{dc} = 700$ V, the filter component values listed in Tab. 3.9, a step change of $v_{A0,set}(t)$ from 20 V to 52.5 V, and no load to clearly highlight the difference ($v_{A,out}$ is not controlled). The solid gray curve represents the measured $v_{A,out}$; the dashed gray curve is simulated ideally, i.e. without different time delays of the rising and falling edges of v_{A0} and the black dote-dashed curve includes the different delays based on separate measurements. The simulation result for a model resistor of $r_{A0,d} = 550$ mΩ is not explicitly shown in the figure because the curve would be almost perfectly similar to the black dote-dashed curve.

Small-Signal Model of the Power Stage

A simple small-signal model of the switching stage is obtained from an averaged model mainly considering the delay of the digital control system, $T_d = 15.6$ µs (cf. Section 3.3.2). Thus,

$$V_{A0}(z) \approx V_{A0,set}(z) \cdot \frac{1}{z} \cdot \frac{z+3}{3 \cdot z + 1} \tag{3.68}$$

is used to model the power stage [cf. Fig. 3.26]. The output filter then processes $\mathcal{L}\left\{\mathcal{Z}^{-1}\left\{V_{A0}(z)\right\}\right\}$ and provides the output voltage, $V_{A,out}(s)$.

According to the measurement result depicted in **Fig. 3.27**, however, (3.68) seems to inaccurately model the dynamic behavior of the power stage. This figure depicts simulated and measured step responses of $v_{A,out}(t)$ for $V_{dc} = 700$ V, the filter component values listed in Tab. 3.9, a step change of $v_{A0,set}(t)$ from 20 V to 52.5 V, and no load to clearly highlight the difference ($v_{A,out}$ is uncontrolled). The out-

[25] Both, the set-point bridge-leg output voltage $v_{A0,set}$ and the output current $i_{A,out}$ are not predicted to reduce the computing time and complexity (the estimation of $i_{A,out}$ would require a load estimator).

put voltages of both, simulated and measured waveforms, oscillate with a frequency of 4.2 kHz, however, different attenuations are found for measured and simulated step responses.

This difference between the measured and simulated waveforms shown in Fig. 3.27 originates from the switches' time delays $T_{\mathrm{d,s}}$, which have an impact on the bridge-leg output voltage. The observed effect has been intensively investigated for inverter topologies [248–256]. Early investigations determine the error of the bridge-leg output voltage if only the dead time is considered and disregard the additional turn-on and turn-off delays [248, 249]. Subsequent publications, beginning with [250, 251], include the contributions of turn-on and turn-off delays and the implications of the current ripple on the effective time delays [252, 253, 255]. The voltage drop at the bridge-leg output of the inverter is found to depend on the bridge-leg's output current, e.g. in [254]. Furthermore, for inverter operation and in the *dq*-frame, a corresponding effective average resistance is determined in [256]. The existing literature focuses on inverter applications, dead time compensation, and quality improvement of the bridge-leg output voltage rather than the investigation of the implications of delay times on the dynamic model at a particular operating point and DC–DC mode of operation.

Current Dependent Time Delays **Fig. 3.28** depicts the setup used to measure the time delay, $T_{\mathrm{d,s}}$, for one T-type half-bridge. The inductance L of the inductor connected to the output of the half-bridge is selected sufficiently large, such that i_{A0} remains approximately constant during the total duration of the measured switching operation. Only positive output voltages of the T-type half-bridge, $v_{\mathrm{A0}}(t) > 0$, are considered. Similar results are obtained for negative bridge-leg output voltages, due to the symmetry of the circuit. According to **Fig. 3.28(a)** the microcontroller turns off S_1 at $t = 0$ and turns on S_2 at $t = T_{\mathrm{dead}}$. This switching operation causes the bridge-leg output voltage, v_{A0}, to finally change from $V_{\mathrm{dc}}/2$ to zero. The actual instant when this change happens, however, depends on the value of the bridge-leg output current, i_{A0} [cf. **Fig. 3.28(b)**].

- For $i_{\mathrm{A0}} < 0$, the body diode of S_1 conducts during the dead time interval, $0 < t < T_{\mathrm{dead}}$, and, thus, the change of v_{A0} happens after the turn-on of S_2.

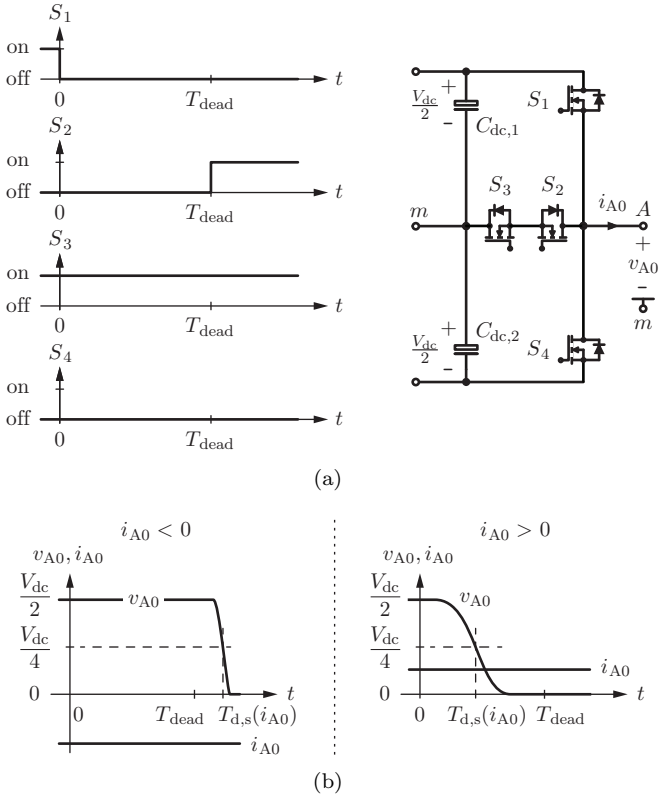


Figure 3.28: Measurement of the time delay introduced by the power semiconductor switches of the T-type half-bridge depicted in Fig. 3.26 (during the switching operation approximately constant bridge-leg output current is assumed, $i_{\text{A0}} \approx \text{const.}$): **(a)** gate signals used to determine $T_{\text{d,s}}$ for positive output voltages (S_3 remains in the on-state and S_4 in the off-state) and definition of $t = 0$, **(b)** definition of the time delay, $T_{\text{d,s}}$. A similar procedure can be used to determine $T_{\text{d,s}}$ for negative output voltages, however, due to symmetry reasons, the same time delay characteristic results. The preceding pulse sequence, used to generate the desired bridge-leg output current, is not shown in this figure.

- For $i_{\text{A0}} > 0$, the body diode of S_1 blocks at $t > 0$, the bridge-leg output current charges or discharges the parasitic effective

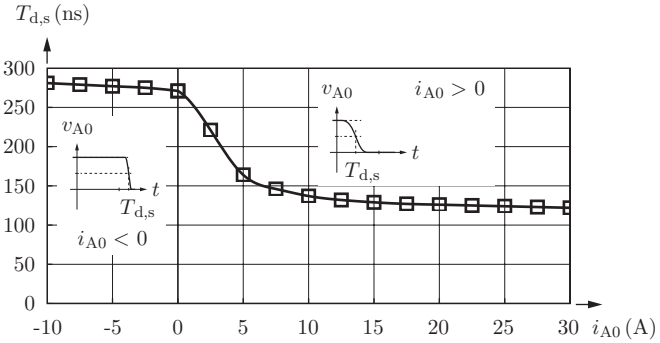


Figure 3.29: Time delays for different bridge-leg output currents, i_{A0}, and constant dead time, $T_{\mathrm{dead}} = 180$ ns, measured for S_1 at an ambient temperature of 25 °C. The rectangles denote actual measurement results obtained from the setup illustrated in Fig. 3.28.

output capacitances of the power semiconductors involved in the switching process, and the change of the bridge-leg output voltage can take place immediately after the turn-off of S_1.

The time delay, $T_{\mathrm{d,s}}$, is measured from the instant when the microcontroller turns off S_1 until the time when v_{A0} reaches $V_{\mathrm{dc}}/4$, which is half of the final bridge-leg output voltage. This procedure allows for a simplified measurement of $T_{\mathrm{d,s}}$, it, however, accepts minor errors at low positive values of i_{A0}, i.e. at bridge-leg output currents that are too small to completely charge or discharge the MOSFETs' effective output capacitances during the dead time.

Fig. 3.29 depicts the measurement results obtained for $T_{\mathrm{dead}} = 180$ ns, $V_{\mathrm{dc}} = 700$ V, and at an ambient temperature of 25 °C. The time delay decreases for increasing bridge-leg output current, since the discharging and charging of the parasitic effective output capacitances proceeds faster for higher currents, and reaches values of less than 130 ns for $i_{\mathrm{A0}} > 15$ A.

The negative gradient of $T_{\mathrm{d,s}}(i_{\mathrm{A0}})$, $\mathrm{d}T_{\mathrm{d,s}}(i_{\mathrm{A0}})/\mathrm{d}i_{\mathrm{A0}} < 0$, is even present for negative bridge-leg output currents, since the turn-on delay slightly increases for increasing MOSFET turn-on currents, i.e. for decreasing values of i_{A0}. The maximum time delay of 280 ns, thus, occurs for the maximum negative bridge-leg output current of -10 A.

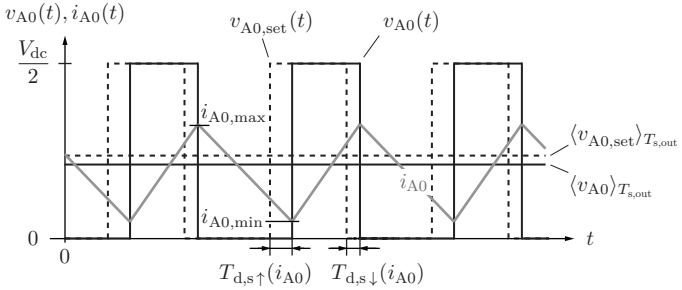


Figure 3.30: Qualitative representation of the effective (gray curve) and ideal assumed (dashed black curve) half-bridge output voltage v_{A0} for a positive bridge-leg output current i_{A0}. The different delay times, $T_{d,s\uparrow}$ for the rising edge and $T_{d,s\downarrow}$ for the falling edge of v_{A0}, occurring in a T-Type half-bridge, are exaggerated for the purpose of a better illustration.

During normal operation, each T-type half-bridge of the CVS generates a rectangular output voltage with a certain duty cycle. Without time delays of the switching operations, the relation between duty cycle and the theoretically present output voltage, for example, is given with

$$\delta_{A0,set}(k \cdot T_{s,out}) = \frac{\langle v_{A0,set}(k \cdot T_{s,out})\rangle_{T_{s,out}}}{V_{dc}/2},\ k \in \mathbb{Z}, \tag{3.69}$$

where $\langle x(t)\rangle_{T_{s,out}}$ denotes the average of $x(t)$ over one switching period $T_{s,out} = 1/f_{s,out}$. In a practical set-up, however, the current dependent time delays of the switching operations cause a difference between the theoretically and the actually present duty cycles $\delta_{A0,set}$ and δ_{A0},

$$\delta_{A0} = \delta_{A0,set} + \delta_{A0,d}, \tag{3.70}$$

with

$$\delta_{A0,d} = \frac{-T_{d,s\uparrow}(i_{A0,min}) + T_{d,s\downarrow}(i_{A0,max})}{T_{s,out}}, \tag{3.71}$$

where $T_{d,s\uparrow}(i_{A0,min})$ and $T_{d,s\downarrow}(i_{A0,max})$ denote the time delays in the events of rising and falling edges of $v_{A0}(t)$, cf. **Fig. 3.30** and [252]. $T_{d,s\uparrow}(i_{A0,min})$ and $T_{d,s\downarrow}(i_{A0,max})$ are obtained from the time delay func-

tion plotted in Fig. 3.29, according to

$$T_{\mathrm{d,s}\uparrow}(i_{\mathrm{A0,min}}) = T_{\mathrm{d,s}}(-i_{\mathrm{A0,min}}) \text{ and} \tag{3.72}$$

$$T_{\mathrm{d,s}\downarrow}(i_{\mathrm{A0,max}}) = T_{\mathrm{d,s}}(i_{\mathrm{A0,max}}). \tag{3.73}$$

The difference between $\delta_{\mathrm{A0,set}}$ and δ_{A0} leads to an average bridge-leg output voltage that deviates from the theoretically expected value,

$$\langle v_{\mathrm{A0}} \rangle_{T_{\mathrm{s,out}}} = \langle v_{\mathrm{A0,set}} \rangle_{T_{\mathrm{s,out}}} + \langle v_{\mathrm{A0,d}} \rangle_{T_{\mathrm{s,out}}}. \tag{3.74}$$

The voltage error that occurs during each switching period, $\langle v_{\mathrm{A0,d}} \rangle_{T_{\mathrm{s,out}}}$, can be calculated with (3.71),

$$\langle v_{\mathrm{A0,d}} \rangle_{T_{\mathrm{s,out}}} = \delta_{\mathrm{A0,d}} \cdot \frac{V_{\mathrm{dc}}}{2} = \frac{V_{\mathrm{dc}}}{2} \cdot \frac{[-T_{\mathrm{d,s}\uparrow}(i_{\mathrm{A0,min}}) + T_{\mathrm{d,s}\downarrow}(i_{\mathrm{A0,max}})]}{T_{\mathrm{s,out}}}, \tag{3.75}$$

and requires the values of $i_{\mathrm{A0,min}}$ and $i_{\mathrm{A0,max}}$. The minimum and maximum inductor currents are determined based on the peak-to-peak current ripple $\Delta I_{\mathrm{A0,pp}}$, which is considered to be constant during the investigated small-signal transient,

$$i_{\mathrm{A0,min}} = \langle i_{\mathrm{A0}} \rangle_{T_{\mathrm{s,out}}} - \frac{\Delta I_{\mathrm{A0,pp}}}{2} \quad \text{and} \quad i_{\mathrm{A0,max}} = \langle i_{\mathrm{A0}} \rangle_{T_{\mathrm{s,out}}} + \frac{\Delta I_{\mathrm{A0,pp}}}{2}. \tag{3.76}$$

The results obtained from (3.75) are in accordance to the results obtained with the expressions obtained in [255]. However, [255], evaluates the time delays based on analytical approximations and this works employs measured time delays to calculate $\langle v_{\mathrm{A0,d}} \rangle_{T_{\mathrm{s,out}}}$.

The relation between $\langle v_{\mathrm{A0,d}} \rangle_{T_{\mathrm{s,out}}}$ and the average bridge-leg output current, i.e.

$$\langle i_{\mathrm{A0}} \rangle_{T_{\mathrm{s,out}}} = \frac{i_{\mathrm{A0,min}} + i_{\mathrm{A0,max}}}{2}, \tag{3.77}$$

is non-linear. Thus, at a dedicated operating point a model resistance $r_{\mathrm{A0,d}}$ in series to $L_{\mathrm{DM,1}}$ can be obtained by means of linearization, i.e.

$$r_{\mathrm{A0,d}} = \frac{\mathrm{d}\langle -v_{\mathrm{A0,d}} \rangle}{\mathrm{d}\langle i_{\mathrm{A0}} \rangle} = \frac{V_{\mathrm{dc}}}{2} \cdot \frac{1}{T_{\mathrm{s,out}}} \cdot \left[\frac{\mathrm{d}T_{\mathrm{d}\uparrow}(i_{\mathrm{A0,min}})}{\mathrm{d}\langle i_{\mathrm{A0}} \rangle} - \frac{\mathrm{d}T_{\mathrm{d}\downarrow}(i_{\mathrm{A0,max}})}{\mathrm{d}\langle i_{\mathrm{A0}} \rangle} \right]. \tag{3.78}$$

For the operating point depicted in Fig. 3.27 this resistance is 550 mΩ, which leads to a nice fit between the calculated and measured results. It is noted that the relationship between the averaged bridge-leg output current $\langle i_{\mathrm{A0}} \rangle_{T_{\mathrm{s,out}}}$ and the voltage error $\langle v_{\mathrm{A0,d}} \rangle_{T_{\mathrm{s,out}}}$ is non-linear and that the model resistor is lossless (the physical explanation is that the energy absorbed by this resistor is not converted to heat but transferred back to the DC link capacitors). The implications of a transient change of the DC link voltage on the bridge-leg output current are neglected.

For illustration purpose an operating point with a high resistance was chosen (cf. Fig. 3.27). However, in the operating point for the experimental results (cf. Tab. 3.14) a resistance of $r_{\mathrm{A0,d}} = 22\ \mathrm{m\Omega}$ is determined based on the presented derivation. Moreover, 50 mΩ due to the filter losses (cf. Section 3.2.4) and 57 mΩ resulting from the MOSFET's on-state resistances ($R_{\mathrm{DS(on)}} = 40\ \mathrm{m\Omega}$ for each transistor)[26] are added to the resistance value of the model resistor, leading to a total resistance in series to $L_{\mathrm{DM},1}$ of $R_{\mathrm{DM},1} = 22\ \mathrm{m\Omega} + 50\ \mathrm{m\Omega} + 57\ \mathrm{m\Omega} = 129\ \mathrm{m\Omega}$, which is also assumed for the optimization of the control structures presented in Section 3.3.3 hereafter.

3.3.3 Optimized Controller Design

In the following, separate optimizations are conducted for each considered control structure, with respect to the four Evaluation Quantities (EQs) listed and with all conducted controller designs being subject to the boundary conditions given below. Furthermore, the optimization algorithm is explained and the obtained results are discussed.

- Reference tracking I — small-signal bandwidth, $f_{\mathrm{bw,ss}}$: The higher the small-signal −3 dB bandwidth of the control structure the better the reference tracking capability of the CVS. The CVS shall be capable of generating sinusoidal output voltages with harmonic components located at frequencies that are considerably higher than the mains frequency; therefore, a high small-signal bandwidth is of particular interest [50].

[26] On the one hand, if the output of the bridge-leg is connected to the positive DC link rail, one MOSFET (S_1) is conducting. On the other hand, if the bridge-leg's output is connected to the DC link midpoint, two MOSFETs (S_2 and S_3) are in the current path. Accordingly, the resulting on-state resistance is calculated by $40\ \mathrm{m\Omega} \cdot \delta + 80\ \mathrm{m\Omega} \cdot (1 - \delta) = 57\ \mathrm{m\Omega}$ for the given operating point (cf. Tab. 3.14), where $\delta = v_{\mathrm{A,out}}/(V_{\mathrm{dc}}/2) = 200\ \mathrm{V}/350\ \mathrm{V} = 0.57$ is the duty-cycle.

- Reference tracking II — integrated squared voltage error after a reference step, $e^2_{\mathrm{ev,vref}}$: The output voltage, $v_{\mathrm{A,out}}$, should follow the reference with the smallest possible deviation. A measure for this can be obtained by integrating the square of the voltage error, $e^2_{\mathrm{ev,vref}} = (v_{\mathrm{A,ref}} - v_{\mathrm{A,out}})^2$, until the output voltage remains within a certain tolerance band of the reference value [257],

$$e^2_{\mathrm{ev,vref}} = \int_0^{t_{\mathrm{set,vref}}} \left[\underbrace{v_{\mathrm{A,ref}}(t)}_{\text{step change}} - \underbrace{v_{\mathrm{A,out}}(t)}_{\text{changes due to change of } v_{\mathrm{A,ref}}} \right]^2 \mathrm{d}t, \tag{3.79}$$

  where $t_{\mathrm{set,vref}}$ denotes the point in time after which the output voltage stays within a deviation band of $\pm 1\%$,

$$\left| \frac{v_{\mathrm{A,out}}(t) - v_{\mathrm{A,ref}}(t)}{v_{\mathrm{A,ref}}(t)} \right| \leq 1\% \quad \forall \quad t \geq t_{\mathrm{set,vref}}. \tag{3.80}$$

  The optimization aims to keep $e^2_{\mathrm{ev,vref}}$ as small as possible.

- Disturbance rejection I — integrated voltage error squared after a step in the load current, $e^2_{\mathrm{ev,iload}}$: A load step triggers a transient change of the output voltage. The resulting difference between reference and output voltages, $v_{\mathrm{A,ref}} - v_{\mathrm{A,out}}$, should be as small as possible. This can be characterized by

$$e^2_{\mathrm{ev,iload}} = \int_0^{t_{\mathrm{set,iload}}} \left[\underbrace{v_{\mathrm{A,ref}}(t)}_{\text{remains unchanged}} - \underbrace{v_{\mathrm{A,out}}(t)}_{\text{changes due to load step}} \right]^2 \mathrm{d}t, \tag{3.81}$$

  where $t_{\mathrm{set,iload}}$ is the point in time after which the output voltage remains within a deviation band around the reference value of 1% [cf. (3.80)].

- Disturbance rejection II — output impedance, $Z_{\mathrm{A,out}}$, at $f = 3$ kHz:[27] The output impedance can be used to describe the im-

[27] A frequency much greater than the mains frequency (50 Hz or 60 Hz) is selected in order to take the technically more challenging capability of the CVS of generating output signals with higher frequencies into consideration. Still, this frequency is selected such that $Z_{\mathrm{A,out}}(f)$ is evaluated well inside the achieved control bandwidths (between 6 kHz and 7 kHz, cf. Tab. 3.11). For this reason, $f = 3$ kHz, 60 Hz $\ll f <$ 6 kHz, is found to be suitable for the purpose of a comparison.

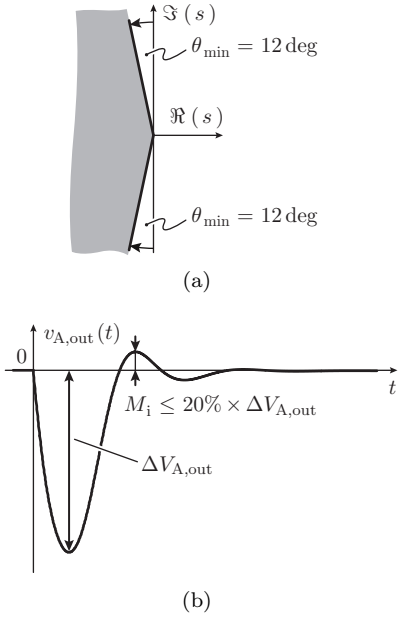


Figure 3.31: (a) The solid lines delimit allowed from forbidden locations of the poles of the closed current and voltage control loops in the Laplace domain to provide robustness to the control loops. $\theta_{\min} = 12\,\text{deg}$ leads to a reasonable compromise between a quick step response and adequate stability margin [183]. **(b)** Illustration of the disturbance rejection boundary condition, where the recovery peak in the output voltage $v_{\text{A,out}}$ is limited to 20% of the voltage dip $\Delta V_{\text{A,out}}$.

plication of the output current, $-I_{\text{A,out}}(\text{j}\omega)$, on the output voltage, $V_{\text{A,out}}(\text{j}\omega)$, with respect to magnitude and phase; $|Z_{\text{A,out}}| \ll |R_{\text{A,load}}|$ is needed in order for the output voltage to closely track the reference voltage. For this reason, the optimization algorithm aims for a low output impedance.

Considered Boundary Conditions

To make the controlled systems robustly stable, the poles of any closed-loop transfer function of the systems depicted in Fig. 3.26, i.e. the poles

of the closed-loop current and voltage transfer functions in case of the control system shown in Fig. 3.26(a), are located inside the gray shaded area depicted in **Fig. 3.31(a)**. The area is restricted by the linear boundary of $\theta_{\min} = 12$ deg, which guarantees stability and which is a reasonable compromise between a quick step response and adequate stability margin [183]; θ denotes the angle between the imaginary axis and a pole. Thus, the controller designs are based on pole placement, since the well-known gain- and phase-margin concepts may fail in presence of a negative small-signal load resistance (unstable transfer functions of the filter with load in Fig. 3.26).

For reference tracking, the maximum relative overshoot of the output voltage, excited by a reference voltage step, is limited to less than 10% to only consider controller designs which achieve a tight output voltage control. Furthermore, to avoid long settling times t_{set} in the range of 10 ms or longer, $t_{\text{set,vref}}$ of the output voltage should not exceed 1 ms after a reference voltage step.[28]

For disturbance rejection, it is also desired to achieve a tight output-voltage control after load steps, and hence the recovery output voltage overshoot M_{i} is limited to 20% of the height of the voltage dip $\Delta V_{\text{A,out}}$ as shown in **Fig. 3.31(b)**. Additionally, the settling time $t_{\text{set,iload}}$ after a load step is limited to 1 ms.

The pole placements, the voltage overshoots, and $t_{\text{set,vref}}$ are calculated for three different load situations, $\tilde{R}_{\text{A,load}} = [-15.9\ \Omega,\ 10\ \text{M}\Omega,\ 15.9\ \Omega]$ ($\tilde{R}_{\text{A,load}} = 10\ \text{M}\Omega$ approximates the no load situation). The amplitude of the reference voltage step is 20 V. For the load step, a current source type of load is employed and the step amplitude is $25\% \times I_{\text{A,out,n}} = 25\% \times 14.5\ \text{A} = 3.6\ \text{A}$. Thus, the calculated output voltage transients due to a load step are independent of the load situation.

Further constraints apply to the maximum gains of current and voltage controllers to keep random variations of the measured output voltage from the steady-state value, arising from measurement noise, smaller than ± 0.5 V. These limits have been determined by experiments carried out on the hardware prototype (cf. Section 3.3.4) and are

[28] Based on Section 3.2, it is expected that the output voltage transient after a reference step last roughly 100 µs until the output voltage reaches a tolerance band of ±5% around the reference value. However, to achieve a tighter output voltage control, the tolerance band in this work is reduced to ±1%, hence the maximum allowed settling time is set to 1 ms.

listed below.

$$\begin{gathered}\textit{PI-P control structure}:\\ k_{\mathrm{pv}} \cdot k_{\mathrm{pi}} \leq 4.6\ \mathrm{V/V} \text{ and } k_{\mathrm{pi}} \leq 10\ \mathrm{V/A}\\ \textit{Capacitor current feedback control structure}:\\ k_{\mathrm{pv}} \leq 4.6\ \mathrm{V/V},\ k_1 \leq 10\ \mathrm{V/A}, \text{ and } k_2 \leq 20\ \mathrm{V/A}\\ \textit{PI-P-P control structure}:\\ (k_{\mathrm{pv1}} + k_{\mathrm{pv2}}) \cdot k_{\mathrm{pi}} \leq 4.6\ \mathrm{V/V} \text{ and } k_{\mathrm{pi}} \leq 10\ \mathrm{V/A}\end{gathered} \tag{3.82}$$

For the PI-P-P control structure, k_{pv1} and k_{pv2} are the gains of the voltage controllers for v_{A1} and $v_{\mathrm{A,out}}$, respectively.

Optimization Procedure

Fig. 3.32 depicts the flowchart of the algorithm used to optimize the controllers of the PI-P control structure depicted in Fig. 3.26(a). This optimization algorithm essentially remains the same for all control structures investigated in this work, only the closed-loop transfer functions change.

The algorithm first initiates a discrete search space according to geometric series [cf. ①] in Fig. 3.32. For the PI-P control structure this is

$$\begin{aligned} k_{\mathrm{pv}} &= 10\ \mathrm{mA/V} \cdot 10^{\frac{i}{48}}, & 0 \leq i \leq 96, \quad & i \in \mathbb{N}_0,\\ T_{\mathrm{iv}} &= 10\ \mu\mathrm{s} \cdot 10^{\frac{i}{48}}, & 0 \leq i \leq 144, \quad & i \in \mathbb{N}_0\\ k_{\mathrm{pi}} &= 1\ \mathrm{V/A} \cdot 10^{\frac{i}{48}}, & 0 \leq i \leq 48, \quad & i \in \mathbb{N}_0,\\ T_{\mathrm{pre}} &= 10\ \mu\mathrm{s} \cdot 10^{\frac{i}{48}}, & 0 \leq i \leq 96, \quad & i \in \mathbb{N}_0 \end{aligned} \tag{3.83}$$

for the parameters of the controllers and

$$\tilde{R}_{\mathrm{A,load}} = [-15.9\ \Omega,\ 10\ \mathrm{M}\Omega,\ 15.9\ \Omega] \tag{3.84}$$

for the considered load situations, which gives a total of $97 \cdot 145 \cdot 49 \cdot 97 \cdot 3 = 201 \cdot 10^6$ different parameter sets. In Fig. 3.32 the address variable m accesses the currently processed controllers' parameter set without load resistance and n accesses one of the three small-signal load resistance values.

With a given set of the controllers' parameters the algorithm verifies in ② in Fig. 3.32 that the limits of the controller gains in (3.82) are not exceeded. Thereafter, the algorithm computes the transfer functions $L_{\mathrm{cl,i},m,n}$ and $L_{\mathrm{cl,v},m,n}$ of the closed current and voltage control loops in ③ for all considered small-signal resistances and analyzes the locations of the poles of both transfer functions. The algorithm continues

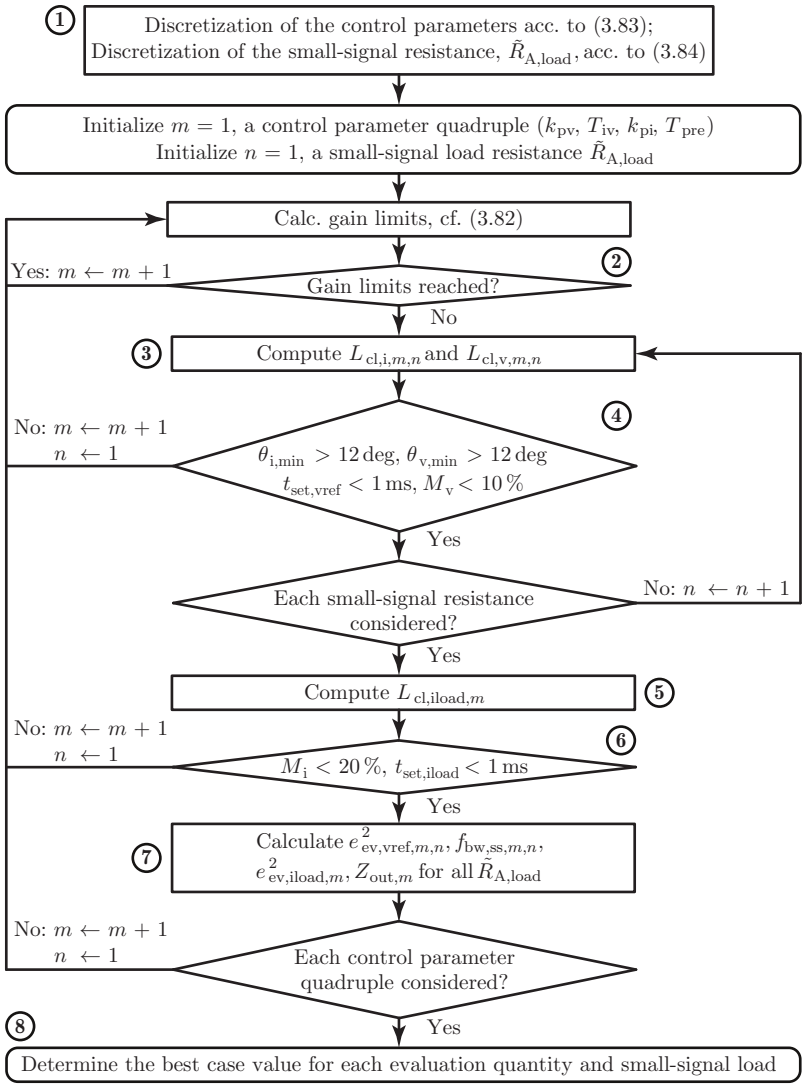


Figure 3.32: Flowchart of the algorithm used to optimize the PI-P control structure with respect to the evaluation quantities and the boundary conditions defined above. This optimization algorithm essentially remains the same for all control structures investigated in this work, only the closed-loop transfer functions, $L_{\mathrm{cl,i},m,n}$, $L_{\mathrm{cl,v},m,n}$, and $L_{\mathrm{cl,iload},m}$ change.

with the same controllers' parameter set if the above discussed boundary conditions for robustness and for reference tracking are fulfilled.

In a next step, the algorithm calculates the load current to output voltage transfer function $L_{\mathrm{cl,iload},m}$ in ⑤ and verifies the disturbance rejection boundary conditions in ⑥. If the considered parameter set also satisfies these conditions the algorithm calculates all EQs, $e^2_{\mathrm{ev,vref}}$, $f_{\mathrm{bw,ss}}$, $e^2_{\mathrm{ev,iload}}$, and $Z_{\mathrm{A,out}}(@\ 3\ \mathrm{kHz})$, for all small-signal resistances in ⑦, and continues with the next parameter set. The optimization procedure finally determines, which parameter sets lead to the best EQs for each considered load condition in ⑧.

Results of the Optimization

Tab. 3.11 lists the obtained results and the parameters of the controllers for which the values are reached for each EQ. According to Fig. 3.26, the value of the time constant of the prefilter, T_{pre}, has no effect on the output voltage response in the event of a load step. However, any valid parameter set must lead to a response of the system, which fulfills all boundary conditions discussed in Section 3.3.3. Due to this requirement, the listed valid ranges of T_{pre} result for the two EQs $e^2_{\mathrm{ev,iload}}$ and Z_{out}.

The capacitor current feedback control structure is most competitive with respect to the minimum achievable integrated and squared deviations of the output voltage due to a reference step ($14.9\ \mathrm{mV^2s}$) and a load step ($2.0\ \mathrm{mV^2s}$) and with respect to the minimum output impedance ($1.4\ \Omega$). The PI-P-P control structure leads with respect to the maximum small-signal bandwidth (7.2 kHz). The PI-P control structure is found to be least competitive for all EQs. The $f_{\mathrm{bw,ss}}$ and the $e^2_{\mathrm{ev,vref}}$ quantities are given for $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$, since, for a stable system with a maximum output voltage overshoot of 10%, this load condition has been identified to always lead to the worst-case values for $f_{\mathrm{bw,ss}}$ and $e^2_{\mathrm{ev,vref}}$. For the $e^2_{\mathrm{ev,iload}}$ and the $Z_{\mathrm{A,out}}$ quantities a constant current source type of load is assumed. For the given hardware prototype, the limitations due to measurement noise, given in (3.82), only become active for the PI-P-P control structure. If these limitations would not apply, the PI-P-P control structure would outperform the capacitor current feedback control structure. For completeness **Tab. 3.12** lists the EQs theoretically achievable for the PI-P-P control structure if the limitations according to (3.82) would not apply.

Table 3.11: Comparison of the four different evaluation quantities (EQs) used to evaluate the control performances of the three considered control structures for the respective optimal controller designs. The parameters of the controllers for which the values are reached are given for each EQ. For the PI-P-P control structure, k_{pv1} and k_{pv2} are the gains of the voltage controllers for V_{A1} and $V_{\mathrm{A,out}}$, respectively.

EQ	*PI-P control structure*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss}}$	5.8 kHz	$k_{\mathrm{pv}} = 0.40$ A/V, $k_{\mathrm{pi}} = 8.3$ V/A, $T_{\mathrm{iv}} = 750$ µs, $T_{\mathrm{pre}} = 30$ µs, $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	19.1 mV^{2}s	$k_{\mathrm{pv}} = 0.40$ A/V, $k_{\mathrm{pi}} = 8.3$ V/A, $T_{\mathrm{iv}} = 750$ µs, $T_{\mathrm{pre}} = 30$ µs, $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.9 mV^{2}s	$k_{\mathrm{pv}} = 0.40$ A/V, $k_{\mathrm{pi}} = 8.3$ V/A, $T_{\mathrm{iv}} = 953$ µs, $T_{\mathrm{pre}} = 30$ µs $-$ 147 µs, $\tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out} @ 3 kHz	1.7 Ω	$k_{\mathrm{pv}} = 0.40$ A/V, $k_{\mathrm{pi}} = 8.3$ V/A, $T_{\mathrm{iv}} = 953$ µs, $T_{\mathrm{pre}} = 30$ µs $-$ 147 µs, $\tilde{R}_{\mathrm{A,load}} \to \infty$
EQ	*Capacitor current feedback control structure*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss}}$	7.1 kHz	$k_{\mathrm{pv}} = 3.8$ V/V, $T_{\mathrm{iv}} = 787$ µs, $k_1 = 8.3$ V/A, $k_2 = 15.4$ V/A, $T_{\mathrm{pre}} = 14$ µs, $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	14.9 mV^{2}s	$k_{\mathrm{pv}} = 3.0$ V/V, $T_{\mathrm{iv}} = 402$ µs, $k_1 = 8.3$ V/A, $k_2 = 18.7$ V/A, $T_{\mathrm{pre}} = 0$, $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.0 mV^{2}s	$k_{\mathrm{pv}} = 3.7$ V/V, $T_{\mathrm{iv}} = 715$ µs, $k_1 = 8.3$ V/A, $k_2 = 19.6$ V/A, $T_{\mathrm{pre}} = 8$ µs $-$ 178 µs, $\tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out} @ 3 kHz	1.4 Ω	$k_{\mathrm{pv}} = 3.7$ V/V, $T_{\mathrm{iv}} = 95$ µs, $k_1 = 8.3$ V/A, $k_2 = 19.6$ V/A, $T_{\mathrm{pre}} = 8$ µs $-$ 178 µs, $\tilde{R}_{\mathrm{A,load}} \to \infty$

This work considers a high achievable small-signal bandwidth to

Table 3.11: Continued.

EQ	*PI-P-P control structure*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss}}$	7.2 kHz	$k_{\mathrm{pv2}} = 268$ mV/V, $T_{\mathrm{iv}} = 909$ µs, $k_{\mathrm{pv1}} = 0.37$ A/V, $k_{\mathrm{pi}} = 7.1$ V/A, $T_{\mathrm{pre}} = 17$ µs, $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	16.3 mV^{2}s	$k_{\mathrm{pv2}} = 9$ mV/V, $T_{\mathrm{iv}} = 65$ µs, $k_{\mathrm{pv1}} = 0.33$ A/V, $k_{\mathrm{pi}} = 7.9$ V/A, $T_{\mathrm{pre}} = 3$ µs, $\tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.2 mV^{2}s	$k_{\mathrm{pv2}} = 282$ mV/V, $T_{\mathrm{iv}} = 316$ µs, $k_{\mathrm{pv1}} = 0.37$ A/V, $k_{\mathrm{pi}} = 7.1$ V/A, $T_{\mathrm{pre}} = 19$ µs $- 170$ µs, $\tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out} @ 3 kHz	1.4 Ω	$k_{\mathrm{pv2}} = 294$ mV/V, $T_{\mathrm{iv}} = 953$ µs, $k_{\mathrm{pv1}} = 0.38$ A/V, $k_{\mathrm{pi}} = 6.8$ V/A, $T_{\mathrm{pre}} = 19$ µs $- 178$ µs, $\tilde{R}_{\mathrm{A,load}} \to \infty$

be of particular interest [50], therefore, all three control structures are parameterized with respect to the maximum small-signal bandwidth. With this set of the controllers' parameters the EQs are given in **Tab. 3.13** for all three control structures. In comparison to the best achievable EQs (cf. Tab. 3.11) it can be seen that the EQs remain almost the same for the parameters of the controllers selected in Tab. 3.13. Furthermore, the above mentioned advantages of the capacitor current feedback control structure compared to the other control structures remain.

Fig. 3.33 presents the calculated reference voltage and load step responses of the three investigated control structures for the parameters of the controllers listed in Tab. 3.13. In accordance to the values of $e^2_{\mathrm{ev,vref}}$ and $e^2_{\mathrm{ev,iload}}$ listed in Tab. 3.13, the reference and disturbance actions of the capacitor current feedback and the PI-P-P control structures are very similar and superior to those of the PI-P control.

Fig. 3.34 depicts the calculated small-signal reference tracking transfer functions of the three control structures and reveals the calculated small-signal bandwidths of 5.8 kHz, 7.1 kHz, and 7.2 kHz for the PI-P, the capacitor current feedback, and the PI-P-P control structures, respectively.

The computed small-signal output impedances for the different con-

Table 3.12: Values of the EQs obtained for the PI-P-P control structure if (3.82) would not apply, i.e. in case of no controller gain limitations due to measurement noise (the two other structures do not hit the gain limits). k_{pv1} and k_{pv2} denote the gains of the voltage controllers for V_{A1} and $V_{\mathrm{A,out}}$, respectively.

EQ	*PI-P-P ctr. struct. - w/o controller gain limitations*	
	Value	*Control parameters*
$f_{\mathrm{bw,ss}}$	8.1 kHz	$k_{\mathrm{pv2}} = 44\ \mathrm{mV/V}, T_{\mathrm{iv}} = 348\ \mu\mathrm{s}$, $k_{\mathrm{pv1}} = 0.51\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.8\ \mathrm{V/A}$, $T_{\mathrm{pre}} = 0, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,vref}}$	13.9 $\mathrm{mV^2s}$	$k_{\mathrm{pv2}} = 51\ \mathrm{mV/V}, T_{\mathrm{iv}} = 178\ \mu\mathrm{s}$, $k_{\mathrm{pv1}} = 0.47\ \mathrm{A/V}, k_{\mathrm{pi}} = 7.1\ \mathrm{V/A}$, $T_{\mathrm{pre}} = 0, \tilde{R}_{\mathrm{A,load}} = 15.9\ \Omega$
$e^2_{\mathrm{ev,iload}}$	2.1 $\mathrm{mV^2s}$	$k_{\mathrm{pv2}} = 387\ \mathrm{mV/V}, T_{\mathrm{iv}} = 10\ \mathrm{ms}$, $k_{\mathrm{pv1}} = 0.56\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.2\ \mathrm{V/A}$, $T_{\mathrm{pre}} = 18\ \mu\mathrm{s} - 196\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$
Z_{out} @ 3 kHz	1.3 Ω	$k_{\mathrm{pv2}} = 387\ \mathrm{mV/V}, T_{\mathrm{iv}} = 10\ \mathrm{ms}$, $k_{\mathrm{pv1}} = 0.56\ \mathrm{A/V}, k_{\mathrm{pi}} = 6.2\ \mathrm{V/A}$, $T_{\mathrm{pre}} = 18\ \mu\mathrm{s} - 196\ \mu\mathrm{s}, \tilde{R}_{\mathrm{A,load}} \to \infty$

Table 3.13: Values of the EQs obtained for those controllers' parameter sets given in Tab. 3.11, which lead to the maximum small-signal bandwidths.

Control structure	*EQ*			
	$f_{\mathrm{bw,ss}}$	$e^2_{\mathrm{ev,vref}}$	$e^2_{\mathrm{ev,iload}}$	Z_{out}@ 3 kHz
PI-P	5.8 kHz	19.1 $\mathrm{mV^2s}$	2.9 $\mathrm{mV^2s}$	1.7 Ω
Cap. fb.	7.1 kHz	16.8 $\mathrm{mV^2s}$	2.1 $\mathrm{mV^2s}$	1.4 Ω
PI-P-P	7.2 kHz	16.8 $\mathrm{mV^2s}$	2.2 $\mathrm{mV^2s}$	1.5 Ω

trol structures are shown in **Fig. 3.35**. The capacitor current feedback control structure features lowest impedances in the frequency range between 10 Hz and 10 kHz. For frequencies below 200 Hz the PI-P-P control structure has the highest output impedance, while in the frequency range between 200 Hz and 10 kHz the PI-P control structure gives the highest output impedance. The values of the output impedance at 3 kHz are given in Tab. 3.11 for all control structures.

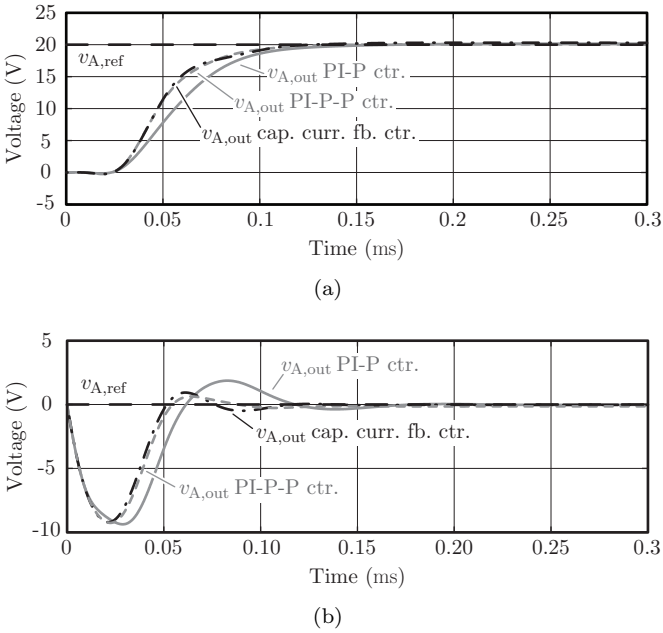


Figure 3.33: (a) Calculated output voltage step responses for a reference step of 20 V and a small-signal load resistance of 15.9 Ω for the three considered control structures, and **(b)** calculated output voltages due to a load step of 25% × $I_{A,out,n}$ = 25% × 14.5 A = 3.6 A for a current-source type of load. The parameters of the controllers are given in Tab. 3.13.

For a worst-case negative small-signal load resistance of −15.9 Ω, the calculated reference voltage responses are depicted in **Fig. 3.36** for the parameters of the controllers given in Tab. 3.13. As already noticed for a positive load resistance of 15.9 Ω, the capacitor current feedback and the PI-P-P control structures achieve a faster reference tracking action than the PI-P structure. **Fig. 3.37** depicts the small-signal frequency responses for $\tilde{R}_{A,load} = -15.9\ \Omega$. For this load resistance the control bandwidths extend to 10.6 kHz, 15.5 kHz, and 13.9 kHz for the PI-P, the capacitor current feedback, and the PI-P-P control structures, respectively.

So far only the small-signal capabilities of the CVS have been dis-

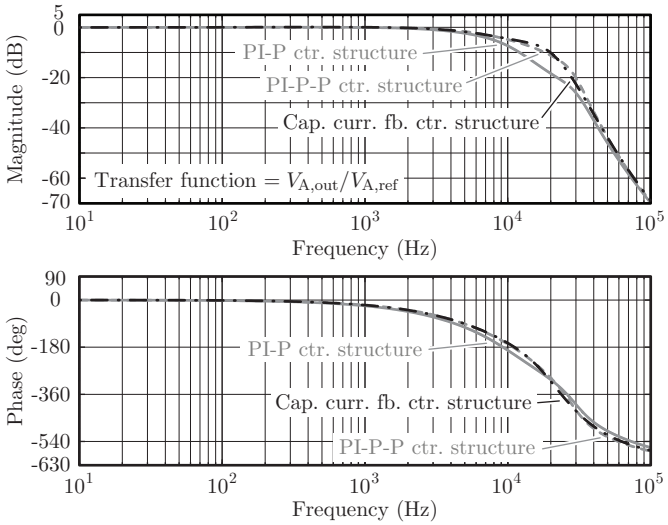


Figure 3.34: Calculated small-signal reference tracking transfer functions for a load resistance of 15.9 Ω for the three considered control structures and the parameters of the controllers given in Tab. 3.13.

cussed. To allow for a more complete picture, **Fig. 3.38** shows the large-signal capability of the CVS for the most suitable control structure (the capacitor current feedback structure), nominal load ($R_{A,load} = 15.9\ \Omega$), and for a hardware limited bridge-leg output current ($\max|i_{A0}(t)| = \sqrt{2}\cdot 17\ \text{A} = 24\ \text{A}$. **Fig. 3.38(a)** depicts the magnitude of the fundamental component of the output voltage $v_{A,out}$ for different modulation indices, $m_i = V_{A,ref,pk}/(V_{dc}/2)$ where $V_{A,ref,pk}$ is the peak value of the sinusoidal reference voltage, and **Fig. 3.38(b)** shows the phase shift between the fundamental component of $v_{A,out}$ and the reference voltage. With the maximum selected modulation index of $m_i = 93\%$ the nominal rms output voltage of 230 V results.

Full and half nominal active powers, i.e. 10 kW/3 = 3.33 kW and 1.67 kW, respectively, can be provided for frequencies up to 300 Hz (voltage amplitude of 325 V) and 840 Hz (voltage amplitude of 230 V), respectively, which has been verified by experiments. Without the limitation of $|i_{A0}|$ and $m_i = 93\%$ [gray curve in Fig. 3.38(a)], full nominal power is feasible up to a frequency of 1.2 kHz and at the small-signal

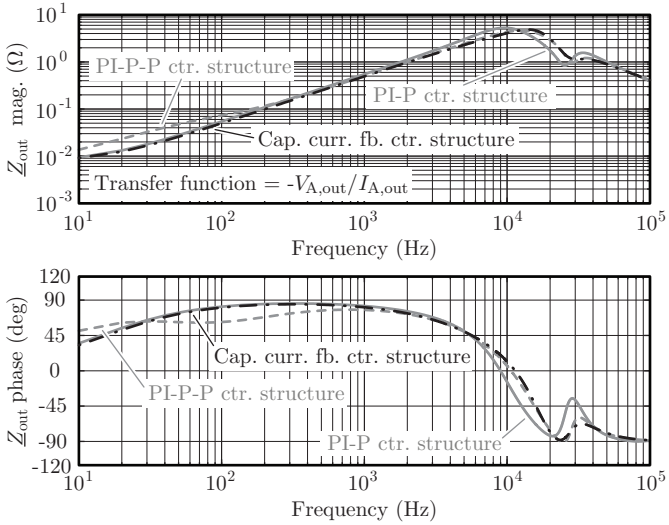


Figure 3.35: Calculated small-signal output impedances for the three considered control structures and the parameters of the controllers given in Tab. 3.13.

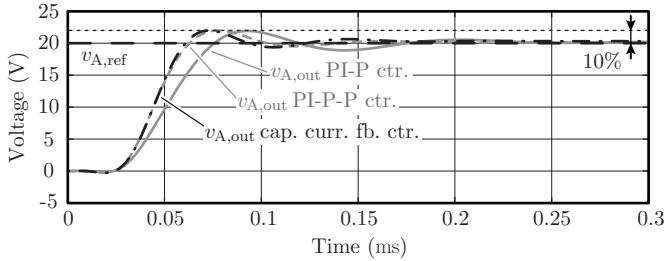


Figure 3.36: Calculated output voltage step responses for a reference step of 20 V, $\tilde{R}_{A,out} = -15.9\ \Omega$, the three considered control structures, and the parameters of the controllers given in Tab. 3.13.

bandwidth of 7.1 kHz, still, half nominal power can be provided. The calculated results further reveal identical large-signal phase responses for different m_i, which are comparable to the small-signal phase re-

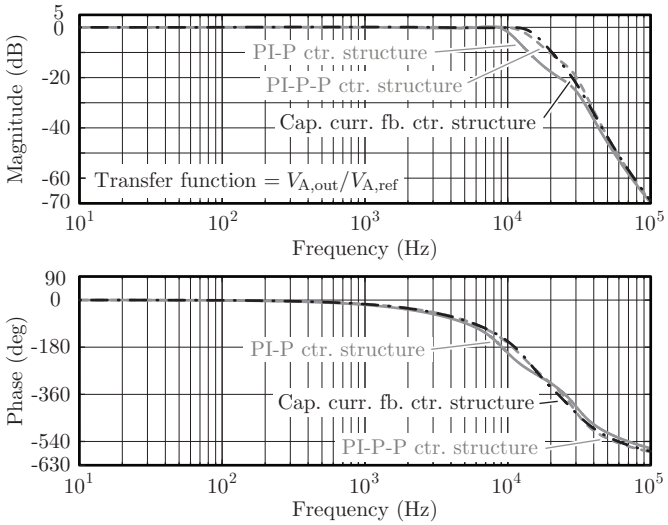


Figure 3.37: Calculated small-signal reference tracking transfer functions for $\tilde{R}_{A,out} = -15.9\,\Omega$, the three considered control structures, and the parameters of the controllers listed in Tab. 3.13.

sponse given in Fig. 3.34. **Fig. 3.38(c)** gives the calculated THD_v (considering ordinal numbers ≤ 40 as proposed in IEC 61000-3-2 [258] but including interharmonics), which is less than 1% or 4% for frequencies less than 5 kHz or 10 kHz for all modulation indices, respectively. It is remarked that the shown large-signal properties have been found to be characteristic for the inverter and the output filter with load and nearly independent of the selected control structure.

3.3.4 Experimental Verification

The hardware setup used to verify the theoretical results, depicted in **Fig. 3.39**, uses the filter component values listed in Tab. 3.9, SiC MOSFETs (Cree's C2M0025120D), and features the specifications given in Tab. 3.8. The fast switching SiC MOSFETs enable the use of a relatively short interlocking time of 180 ns. In addition, no compensation methods are implemented for reducing eventually present output voltage distortions that stem from the interlocking-time interval.

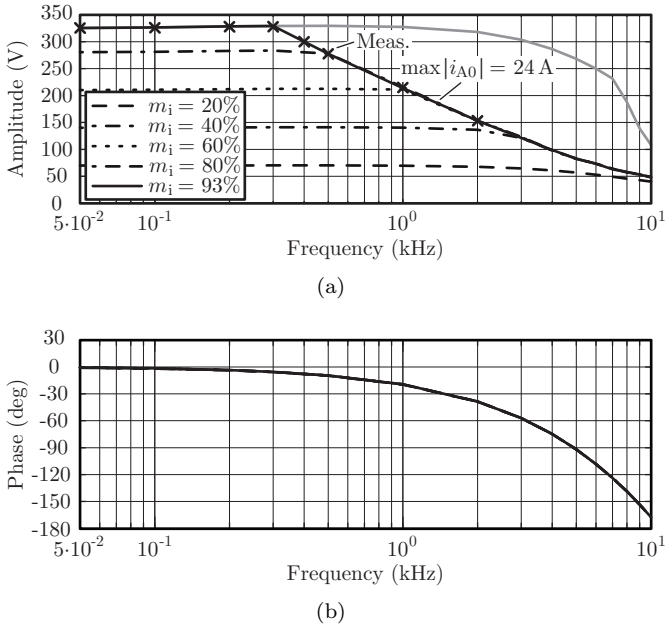
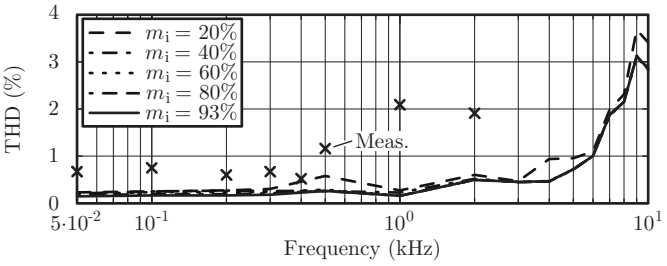


Figure 3.38: Results of large-signal calculations elaborated for the capacitor current feedback control structure, $R_{\mathrm{A,load}} = 15.9\ \Omega$, and a hardware limited bridge-leg output current i_{A0} of 24 A: **(a)** the magnitude of the fundamental component of the output voltage $v_{\mathrm{A,out}}$ for different modulation indices, $m_{\mathrm{i}} = V_{\mathrm{A,ref,pk}}/(V_{\mathrm{dc}}/2)$ where $V_{\mathrm{A,ref,pk}}$ is the peak value of the sinusoidal reference voltage, **(b)** phase shift between the fundamental component of $v_{\mathrm{A,out}}$ and the reference voltage, and **(c)** $\mathrm{THD_v}$ (including interharmonics) calculated for $v_{\mathrm{A,out}}(t)$. The gray curve in (a) is computed for no limitation of $|i_{\mathrm{A0}}|$ and $m = 93\%$ and shows a kink at the small-signal bandwidth of 7.1 kHz. A modulation index $m_{\mathrm{i}} = 93\%$ results in the nominal rms output voltage of 230 V. The measurements have been conducted for $m_{\mathrm{i}} = 93\%$.

Fig. 3.40 depicts the measured waveforms of unfiltered and filtered output voltages and output currents, v_{A0}, $v_{\mathrm{A,out}}$, i_{A0}, and $i_{\mathrm{A,out}}$, for the capacitive current feedback control structure in the event of a reference voltage step of $10\% \times v_{\mathrm{A,out}}(t = 0) = 10\% \times 200\ \mathrm{V} = 20\ \mathrm{V}$ and for the operating conditions given **Tab. 3.14** [$\langle i_{\mathrm{A0}}(t)\rangle_{T_{\mathrm{s,out}}}$ denotes the average of i_{A0} over one switching period]. **Fig. 3.40(b)** reveals that the output



(c)

Fig. 3.38: Continued.

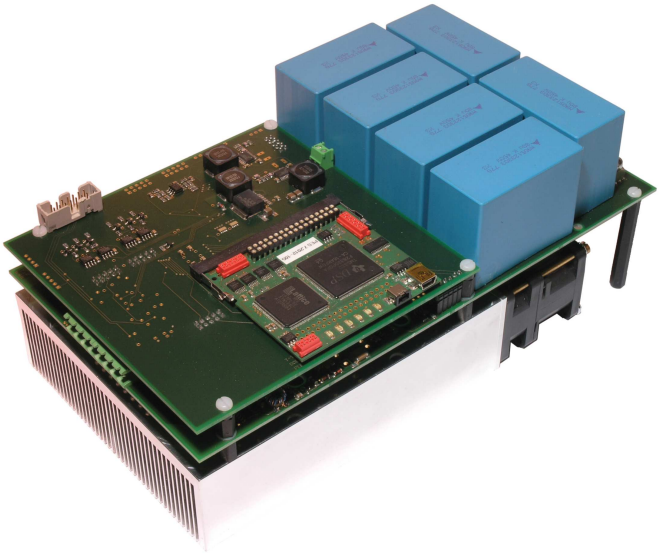


Figure 3.39: Three-phase three-level T-type inverter prototype with SiC MOSFETs C2M0025120D and a floating-point DSP TMS320F28335 as well as an FPGA LFXP2-5E-5TN144C featuring the specifications listed in Tab. 3.8.

filter modifies the dynamic properties of the bridge-leg output current of the CVS, $\langle i_{\mathrm{A0}}(t)\rangle_{T_{\mathrm{s,out}}}$, e.g. with respect to overshoot and time delay.

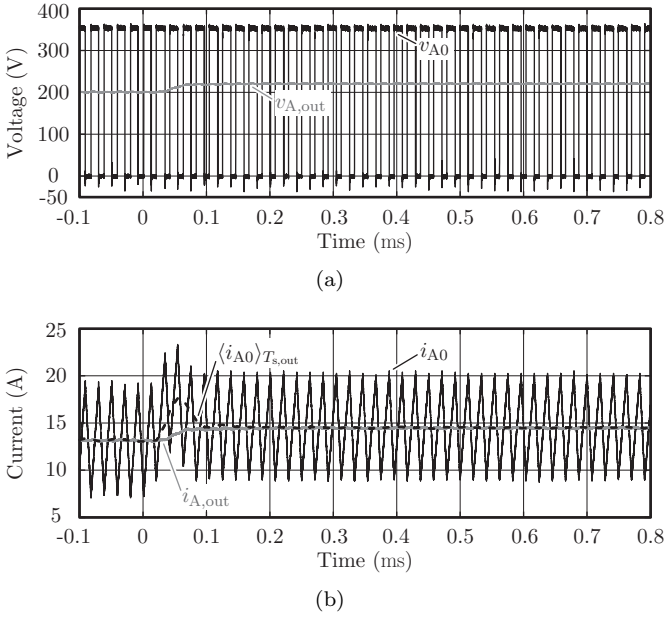
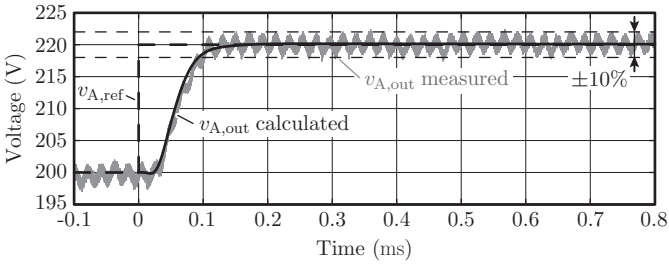


Figure 3.40: Measured waveforms of unfiltered and filtered output voltages and currents, v_{A0}, $v_{A,out}$, i_{A0}, and $i_{A,out}$ [cf. **(a)** and **(b)**], for the capacitive current feedback control structure, a reference voltage step of 20 V, and the operating conditions given in Tab. 3.14. Tab. 3.13 lists the controller settings.

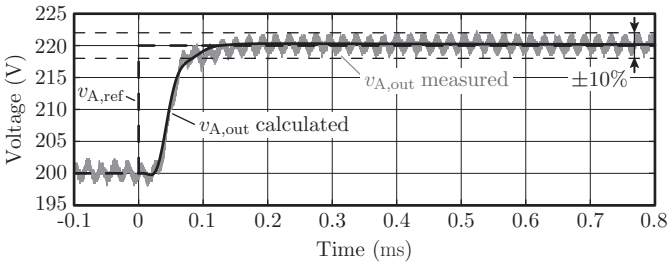
Table 3.14: Operating conditions for which the reference voltage and load steps shown in Figs. 3.40, 3.41, and 3.42 were measured (applies to all three control structures).

DC link voltage, V_{dc}	700 V
Switching frequency, $f_{s,out}$	48 kHz
Sampling frequency, $f_{0,out}$	96 kHz
Output voltage before the step, $v_{A,out}(t = 0)$	200 V
Output load, $R_{A,load}$ (reference step)	15.9 Ω
Output load, $R_{A,load}$ (load step)	22.2 Ω → 15.9 Ω

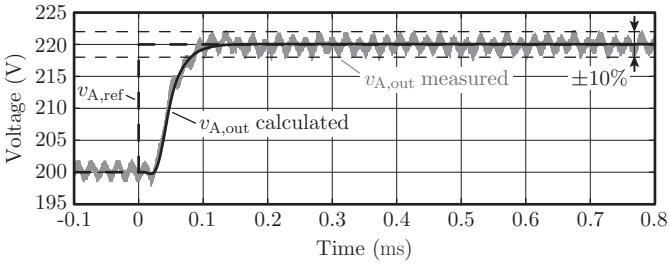
Fig. 3.41 compares calculated to measured reference voltage steps for all three control structures, a voltage step of $10\% \times v_{A,out}(t = 0) =$



(a) PI-P control structure



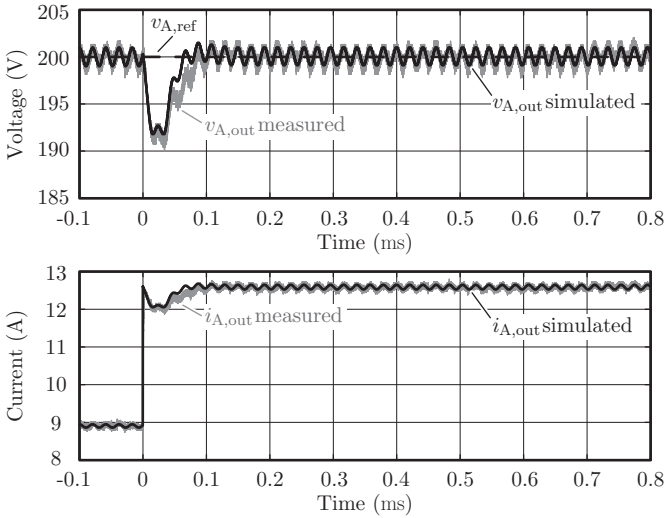
(b) Capacitor current feedback control structure



(c) PI-P-P control structure

Figure 3.41: Measured and calculated output voltages for a reference voltage step of 20 V and the operating conditions given in Tab. 3.14: **(a)** PI-P, **(b)** capacitor current feedback, and **(c)** PI-P-P control structures. The parameters of the controllers are listed in Tab. 3.13.

$10\% \times 200\ \text{V} = 20\ \text{V}$, and the operating conditions listed in Tab. 3.14. Small random variations of the measured output voltages from the

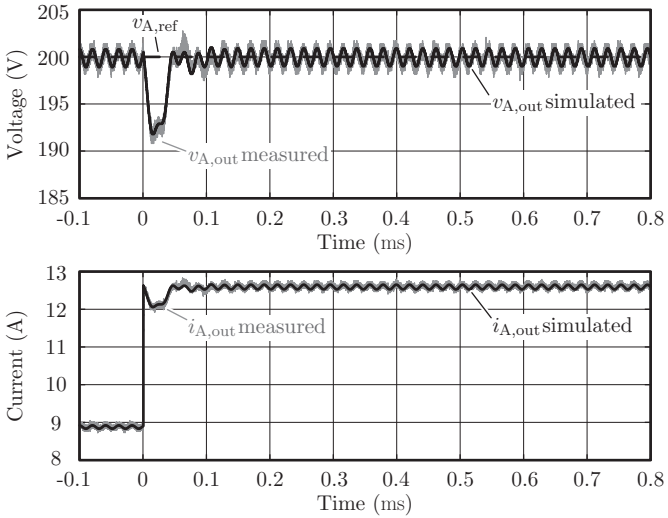


(a) PI-P control structure

Figure 3.42: Measured and simulated output voltages for a load step from 22.2 Ω to 15.9 Ω (leading to a load current step of 3.6 A) and the operating conditions given in Tab. 3.14: **(a)** PI-P, **(b)** capacitor current feedback, and **(c)** PI-P-P control structures. The parameters of the controllers are listed in Tab. 3.13.

steady-state values of at most ±0.5 V can be seen (especially in the measurements for the PI-P-P control structure) because of measurement noise. Apart from these minor errors the calculated and measured waveforms of $v_{A,out}(t)$ fit nicely.

Fig. 3.42 compares the simulated and measured transient changes of the CVS's output voltage if the connected load, $R_{A,load}$, changes from 22.2 Ω to 15.9 Ω (resulting in a current step of 3.6 A), for all three control structures, and for the operating conditions given in Tab. 3.14. In accordance with the corresponding calculated load steps, discussed in Section 3.3.3 and depicted in Fig. 3.33(b), the momentary decreases of the output voltage, approximately 8 V, are the same for all three control structures. However, with the capacitor current feedback and the PI-P-P control structures, the output voltages recover more quickly



(b) Capacitor current feedback control structure

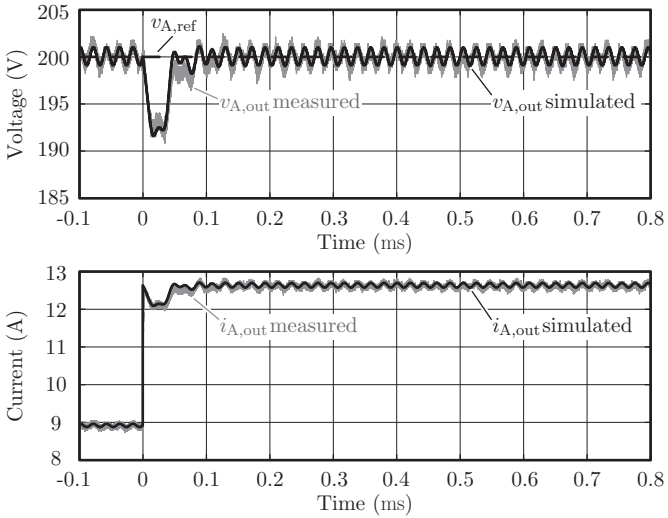
Fig. 3.42: Continued.

than with the PI-P control structure.

With the achieved high control bandwidth and the low input impedance, the presented control structures feature the generation of high-quality output voltages as indicated by **Fig. 3.43**. The measured output voltages for the capacitive current feedback control structure in the figure feature

- an amplitude of 328 V at a frequency of 50 Hz for an output power of 3.3 kW and with a THD_v of 0.67% [cf. **Fig. 3.43(a)**];
- an amplitude of 325 V at a frequency of 300 Hz for an output power of 3.3 kW and with a THD_v of 0.67% [cf. **Fig. 3.43(b)**];
- an amplitude of 151 V at a frequency of 2 kHz for an output power of 718 W and with a THD_v of 1.91% [cf. **Fig. 3.43(c)**].

As a comparison to the results obtained at 50 Hz, the measured THD_v at no load (for the same output voltage amplitude of 328 V) is 0.59%, which demonstrate that the value of the load resistance has only a small



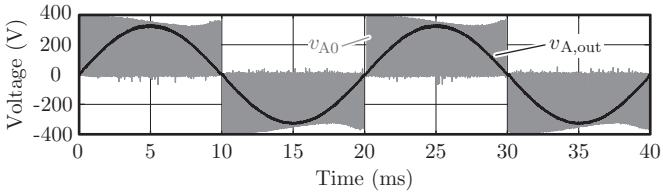
(c) PI-P-P control structure

Fig. 3.42: Continued.

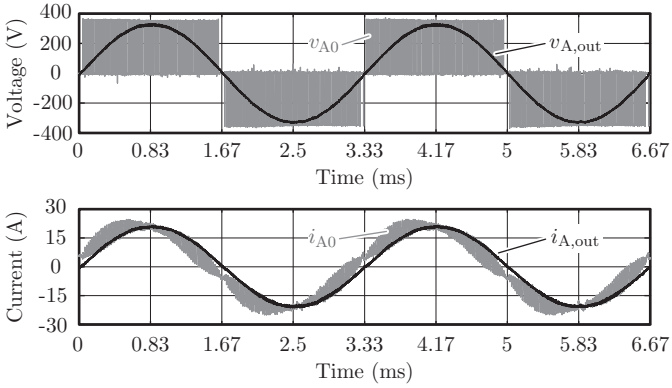
impact on the THD_v. Furthermore, for a converter operating in open-loop and for again 50 Hz, the THD_vs are both 0.48% for no load and full nominal load. This shows that the employed control scheme increases the THD_v by roughly 40% due to nonlinearities of the measurement and processing units of the employed hardware prototype.

Referring to Fig. 3.38(c), comparisons to simulations reveal that the reason for the higher THD_v at higher frequencies of 500 Hz, 1 kHz, and 2 kHz can be attributed to missing pulses in the bridge-leg output voltage v_{A0}, as recognized in Fig. 3.43(c) around the zero-crossing of the output voltage. This leads to a higher distortion of $v_{A,out}$. For these missing pulses the calculated on-times of the switches S_1 and S_4 by the DSP are hence shorter than the turn-on delay times of the switches and hence S_1 and S_4 do not turn on. It is hence noted that the higher THD_v values do not result from the closed-loop control structure.

Even in presence of non-linear loads, output voltages with low THD_v values are feasible. This is demonstrated for the capacitor current feedback control structure and a diode rectifier type of load, depicted in



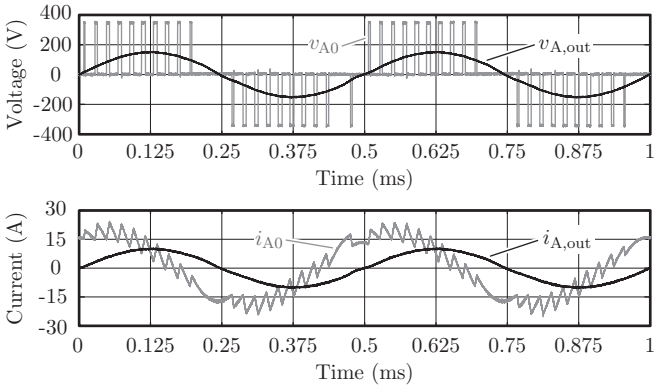
(a) $f_{out} = 50$ Hz



(b) $f_{out} = 300$ Hz

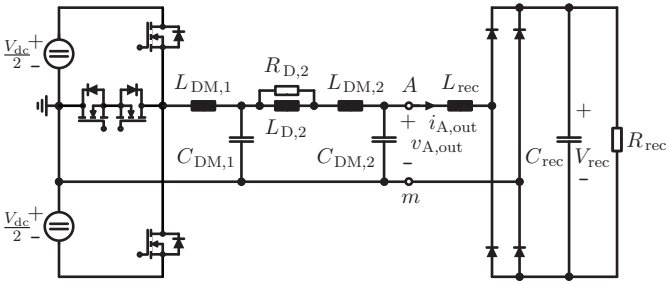
Figure 3.43: Measured waveforms of v_{A0}, $v_{A,out}$, i_{A0}, and $i_{A,out}$ for a sinusoidal output voltage $v_{A,out}$, for an output frequency of **(a)** 50 Hz, **(b)** 300 Hz, and **(c)** 2 kHz, and for the capacitive current feedback control structure.

Fig. 3.44(a), which comprises of $L_{rec} = 3.4$ mH, $C_{rec} = 3.8$ mF, and $R_{rec} = 88\ \Omega$, provides an output power of 1 kW, and a power factor of $\lambda = 0.7$ for $v_{A,out}$ being sinusoidal with a frequency of 50 Hz and a rms value of 230 V. L_{rec} is designed such that, at the output frequency of 50 Hz, $Z_{L,rec} = 2\% \times Z_{rec0}$ applies, with $Z_{L,rec} = 2 \cdot \pi \cdot 50\ \text{Hz} \cdot L_{rec}$ and



(c) $f_{out} = 2$ kHz

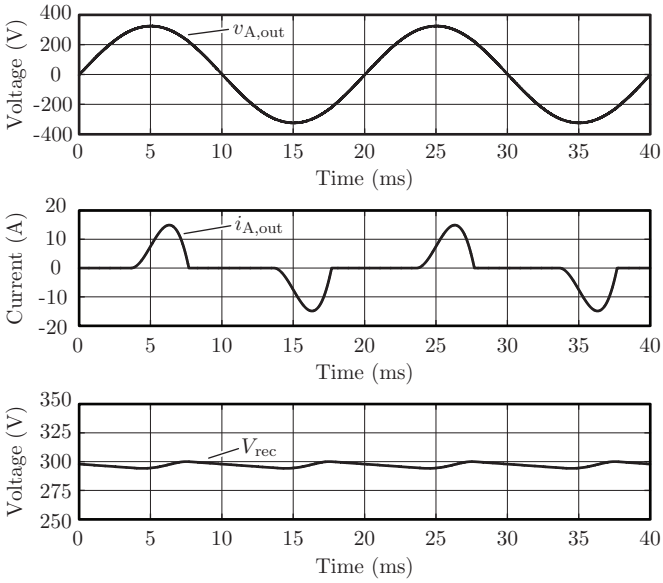
Fig. 3.43: Continued.



(a)

Figure 3.44: Non-linear load connected to the CVS: **(a)** single-phase diode-rectifier load with $L_{rec} = 3.4$ mH, $C_{rec} = 3.8$ mF, and $R_{rec} = 88\ \Omega$; **(b)** simulated waveforms of $v_{A,out}$, $i_{A,out}$, and V_{rec}. The capacitor current feedback control structure is used to control the CVS.

$Z_{rec0} = (230\text{ V})^2/1\text{ kW}$. The selected values of L_{rec} and C_{rec} lead to a relative voltage ripple of 2% at the rectifier's DC port. Due to the good matching of calculated, simulated, and measured results found in Figs. 3.41 and 3.42, the results obtained for the non-linear load, depicted in **Fig. 3.44(b)**, are obtained by way of accurate circuit simulation



(b)

Fig. 3.44: Continued.

that includes a model of the switching stage and correctly reproduces the turn-on and turn-off delays of the switches.

The output current of the output filter of the CVS, $i_{A,out}$ in Fig. 3.44(b), is clearly non-linear; its rms and peak values are 6.2 A and 14.9 A, respectively. Still, $v_{A,out}$ is close to a sinusoidal waveform, with a THD_v of 0.31% (obtained from the circuit simulator, i.e. this value does not consider the implication of slight distortions due to minor measurement errors in the voltage and current sensing circuits used on the hardware prototype; for comparison, at no load and for a single-phase resistive load with $P_{A,out} = 1$ kW THD_v values of 0.24% and 0.21%, respectively, are obtained from the simulator). Further investigations also reveal a negligible impact of the output impedance of the CVS on the obtained results: in this regard, the peak-value of the current in L_{rec} only increases from 14.9 A to 15.0 A if the CVS with output filter is replaced by an ideal AC voltage source.

3.3.5 Summary

This section motivates, models, and optimizes three different control structures composed of conventional P- and PI-controllers and suitable for the output stage of a 10 kW, four-quadrant, three-phase, switch-mode controllable AC voltage source (CVS) module with $f_{\mathrm{s,out}} = 48$ kHz and a two-stage LC output filter, with respect to reference tracking and disturbance rejection. These structures are characterized by means of four defined evaluation quantities (EQs) and for common boundary conditions, e.g. for a maximum overshoot of the output voltage of 10% in case of a reference voltage step. Each output phase of the CVS is operated individually to allow for maximum flexibility in the generation of the output phase voltages to supply a wide range of different types of load, such as DC, single-phase, and three-phase AC loads including loads with constant power characteristics featuring negative small-signal load resistance values.

It is emphasized that the use of accurate small-signal models features an excellent matching between the presented control structure models and the measurements. Further, it has been found that the achievable control performance, i.e. with respect to the values of the EQs defined in Section 3.3.3, strongly depends on the two aspects listed below:

1. *Delay compensation*: To achieve a high control bandwidth and tight output voltage control, it is found to be crucial to minimize the deteriorating impact of the system time delay T_{d}. For this reason all three control structures incorporate delay compensation algorithms, which estimate the expected values of the controlled variables at $t = t_0 + T_{\mathrm{d}}$ based on previous measurements.

2. *Feedforwards and prefilter*: The prefilter for the voltage reference and the feedforwards of the reference voltage and the load current are found to allow for a considerable improvement of the investigated EQs.

For the given hardware set-up and among the three structures depicted in Fig. 3.26, the capacitor current feedback control structure is identified to be most competitive considering the four EQs. This control structure realizes an output impedance of less than 500 mΩ for output frequencies below 1 kHz, a small-signal bandwidth between 7.1 kHz (for nominal load, $\tilde{R}_{\mathrm{load}} = 15.9\ \Omega$) and 15.5 kHz (for $\tilde{R}_{\mathrm{load}} = -15.9\ \Omega$, e.g. occurring for a constant active power load). At $\tilde{R}_{\mathrm{load}} = -15.9\ \Omega$,

the CVS completes a small-signal reference voltage step within five switching cycles (approximately 100 µs).

As a comparison, the small-signal bandwidth of available switch-mode products is typically limited to 5 kHz [42–44]. Accordingly, the elaborated capacitor current feedback control structure optimized with the multi-objective design procedure increase the small-signal bandwidth by 42% to 310% depending on the type of load. It is remarked that the small-signal bandwidth can even be further increased by paralleling bridge-legs (cf. Section 2.2).

The option to directly limit the bridge-leg output current within an inner control loop is an argument often given in favor of the PI-P control structure, where the reference for the inner current control loop is generated by an outer output voltage control loop. Frequently, it is overlooked though, that already a feedforward, which skips the inner current controller, abolishes the capability to fully limit the bridge-leg output current. The feedforward of the reference voltage, identified to enhance the output voltage dynamics, is such a feedforward. Accordingly, none of the investigated control structures features direct means to limit the bridge-leg output current. To achieve this limitation and hence to protect the hardware, an additional supervising control loop, which measures the bridge-leg output current (which would be the case for the PI-P and the PI-P-P control structures) and directly acts on the set-point output voltage of the bridge-leg, would be required. It is expected that if the bridge-leg output current needs to be limited during an output voltage transient which should achieve high dynamics, this supervising control loop would, however, reduce the achievable output voltage dynamics. It is therefore exactly in this context where a more advanced control concept would yield benefits.

Additionally, **Fig. 3.45** compares the output voltage step response obtained with the capacitor current feedback control structure to the response of an optimal trajectory control. The PWM pattern for tracking the optimal trajectory has been calculated off-line and minimizes the integrated squared output voltage error (including the boundary condition of a maximum overshoot of 10%). The resulting step response, thus, reveals that optimal trajectory control can decrease the response time by two to three switching cycles. Optimal trajectory control, however, requires an accurate model of the complete system inclusive load, which may, for example, be achieved with the use of a load estimator according to [259]. The fast step responses achieved with P- and

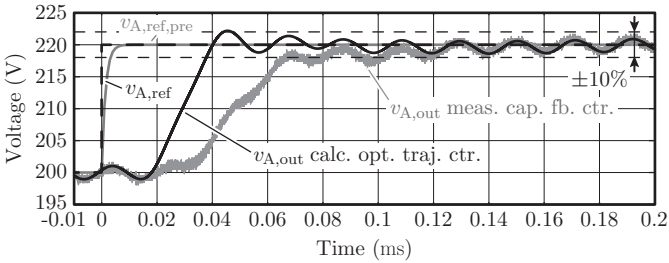


Figure 3.45: Output voltage due to a reference step of 20 V obtained for an optimal trajectory-based controller (black curve) and for the capacitor current feedback control structure (gray curve), which has been identified to be the most suitable structure for the CVS. In contrast to the optimal trajectory-based controller, the capacitor current feedback control scheme employs a prefilter [cf. (3.54)] which slightly increases the reaction time of $v_{A,out}$ to the reference step. The output of the prefilter, $v_{A,ref,pre}(t) = \mathcal{L}^{-1}\{V_{A,ref,pre}(s)\} = \mathcal{L}^{-1}\{F_{pre}(s) \cdot V_{A,ref}(s)\}$, is also given in the figure.

PI-controllers and the low complexities of the proposed control structures clearly support the use of well-known linear controllers, e.g. in an environment that is highly sensitive to other aspects like development time and costs. Still, the widespread use of digital control platforms and increasing computing capacity enable realizations of advanced control concepts that are expected to fill the gap between the two step responses depicted in Fig. 3.45.

Finally, it should be noted that the main scientific contributions of this section are published in [260–262] (see also "List of Publications" on page 337).

3.4 Three-Phase Four-Leg Output Stage

The output filter and the control scheme for the output voltages, e.g. $v_{\mathrm{A,out}}$, are designed in Sections 3.2 and 3.3, respectively, on the basis of single-phase considerations for the three-phase plus neutral conductor converter [cf. Fig. 3.1(a)]. In this part, the outcomes obtained from the previous sections are applied to the three-phase four-leg output stage converter as depicted in Fig. 3.1(b). Because, as motivated in Section 3.1, each output phase of the CVS is operated individually, a symmetrical four-line filter with minimum interactions between the lines is proposed, where the designed single-phase two-stage LC filter is employed for each phase and also the neutral leg. For this filter structure and for a connection of the load star-point to the neutral leg terminal N, the phase load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ are obtained with

$$\begin{aligned} v_{\mathrm{A,load}} &= v_{\mathrm{A,out}} - v_{\mathrm{N,out}}, \\ v_{\mathrm{B,load}} &= v_{\mathrm{B,out}} - v_{\mathrm{N,out}}, \\ v_{\mathrm{C,load}} &= v_{\mathrm{C,out}} - v_{\mathrm{N,out}}. \end{aligned} \tag{3.85}$$

Thus, $v_{\mathrm{N,out}}$ represents a zero-sequence voltage component of $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$, and $v_{\mathrm{C,out}}$ and can be utilized to increase the range of the load voltages [145, 150, 151, 153], preferably by controlling $v_{\mathrm{N,out}}$ to [151]

$$v_{\mathrm{N,ref}} = -\frac{\min\left(v_{\mathrm{A,ref}},\, v_{\mathrm{B,ref}},\, v_{\mathrm{C,ref}}\right) + \max\left(v_{\mathrm{A,ref}},\, v_{\mathrm{B,ref}},\, v_{\mathrm{C,ref}}\right)}{2}; \tag{3.86}$$

$v_{\mathrm{A,ref}}$, $v_{\mathrm{B,ref}}$, and $v_{\mathrm{C,ref}}$ are the references of the load voltages. For the generation of symmetrical three-phase voltages, the maximum amplitude of the load voltages can hence be increased by 15.5% from $V_{\mathrm{dc}}/2$ to $V_{\mathrm{dc}}/\sqrt{3}$ (if the load and mains star-points are not simultaneously grounded, cf. Section 4.2).

For the single-phase consideration, the output voltage $v_{\mathrm{A,out}}$ of phase A for instance is equal to the load voltage $v_{\mathrm{A,load}}$. However, for the three-phase four-leg output stage with the four-line two-stage LC filter, this is not the case [cf. (3.85)] and thus there exist basically two options to measure the voltages at the CVS's output for the purpose of their control:

1. measuring the four output voltages $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$, $v_{\mathrm{C,out}}$, and $v_{\mathrm{N,out}}$; or

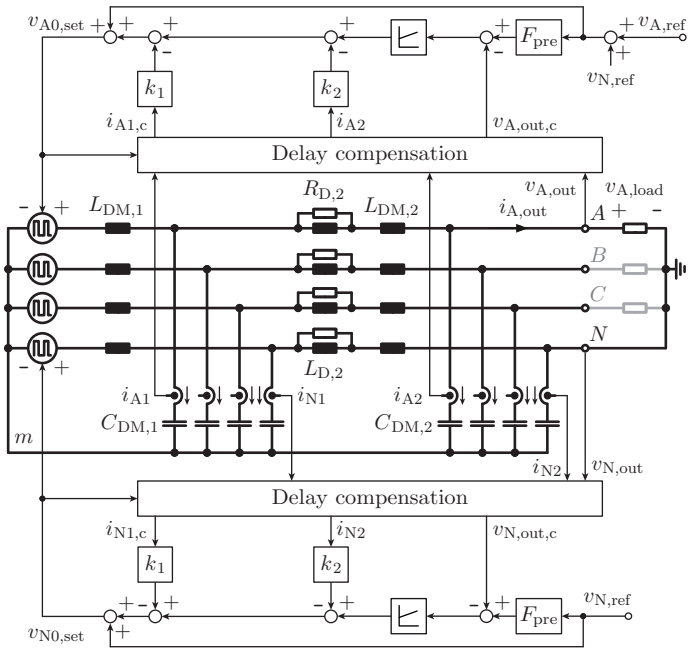


Figure 3.46: Output voltage control scheme for the three-phase four-leg output stage with a symmetrical four-line two-stage LC output filter based on the single-phase control structure given in Fig. 3.26(b). The control loops for the output voltages $v_{\mathrm{A,out}}$ and $v_{\mathrm{N,out}}$ of phase A and of the neutral leg N, respectively, are shown; the control loops for the output voltages $v_{\mathrm{B,out}}$ and $v_{\mathrm{C,out}}$ of phases B and C, respectively, are identical to the loops for $v_{\mathrm{A,out}}$.

2. measuring the three phase load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ and the neutral leg's output voltage $v_{\mathrm{N,out}}$.

The load voltage needs to be measured in the range of $\left[-V_{\mathrm{dc,max}}/\sqrt{3},\ V_{\mathrm{dc,max}}/\sqrt{3}\right]$, which is larger than the maximum measurement range, i.e. $[-V_{\mathrm{dc,max}}/2\,,\ V_{\mathrm{dc,max}}/2]$, of the output voltage. For the same number of bits of the Analog-to-Digital Converter (ADC) of the DSP, the first measurement option therefore achieves a higher resolution and is therefore selected. Accordingly, the single-phase control scheme given in Fig. 3.26(b) needs to be adjusted only slightly for the control of the

Table 3.15: Operating conditions for which the the circuit simulation results presented in this section are carried out.

DC link voltage, V_{dc}	700 V
Switching frequency, $f_{\mathrm{s,out}}$	48 kHz
Sampling frequency, $f_{0,\mathrm{out}}$	96 kHz
Load voltage of phase B, $v_{\mathrm{B,load}}$	200 V
Load voltage of phase C, $v_{\mathrm{C,load}}$	-200 V
Load resistance of phase B, $R_{\mathrm{B,load}}$	15.9 Ω
Load resistance of phase C, $R_{\mathrm{C,load}}$	15.9 Ω
Reference output voltage step (cf. Fig. 3.47)	
Load voltage of phase A before the step, $v_{\mathrm{A,load}}(t<0)$	200 V
Output voltage of the neutral leg, $v_{\mathrm{N,out}}$	acc. to (3.86)
Load resistances of phase A, $R_{\mathrm{A,load}}$	15.9 Ω
Small-signal bandwidth (cf. Fig. 3.48)	
Load voltage reference of phase A, $v_{\mathrm{A,ref}}$	$200\ \mathrm{V} + 20\ \mathrm{V} \cdot \sin(2 \cdot \pi \cdot f \cdot t)$
Output voltage of the neutral leg, $v_{\mathrm{N,out}}$	0
Load resistances of phase A, $R_{\mathrm{A,load}}$	15.9 Ω
Slew rate [cf. Eq. (3.87)]	
Load voltage of phase A before the step, $v_{\mathrm{A,load}}(t<0)$	350 V
Output voltage of the neutral leg, $v_{\mathrm{N,out}}$	0
Load resistances of phase A, $R_{\mathrm{A,load}}$	97 Ω
Transient output impedance [cf. Eq. (3.88)]	
Load voltage of phase A, $v_{\mathrm{A,load}}$	350 V
Output voltage of the neutral leg, $v_{\mathrm{N,out}}$	0
Load resistance of phase A, $R_{\mathrm{A,load}}$	97 Ω → 97 Ω || 100 Ω = 49 Ω

output voltages of the three-phase four-leg output stage as given in **Fig. 3.46**. The references for the output voltages are now obtained by adding the reference $v_{\mathrm{N,ref}}$ for the neutral leg's output voltage to the references $v_{\mathrm{A,ref}}$, $v_{\mathrm{B,ref}}$, and $v_{\mathrm{C,ref}}$ for the load voltages. It is noted that the same control scheme, as derived in Section 3.3, is implemented for all three phases A, B, C and for the neutral leg N.

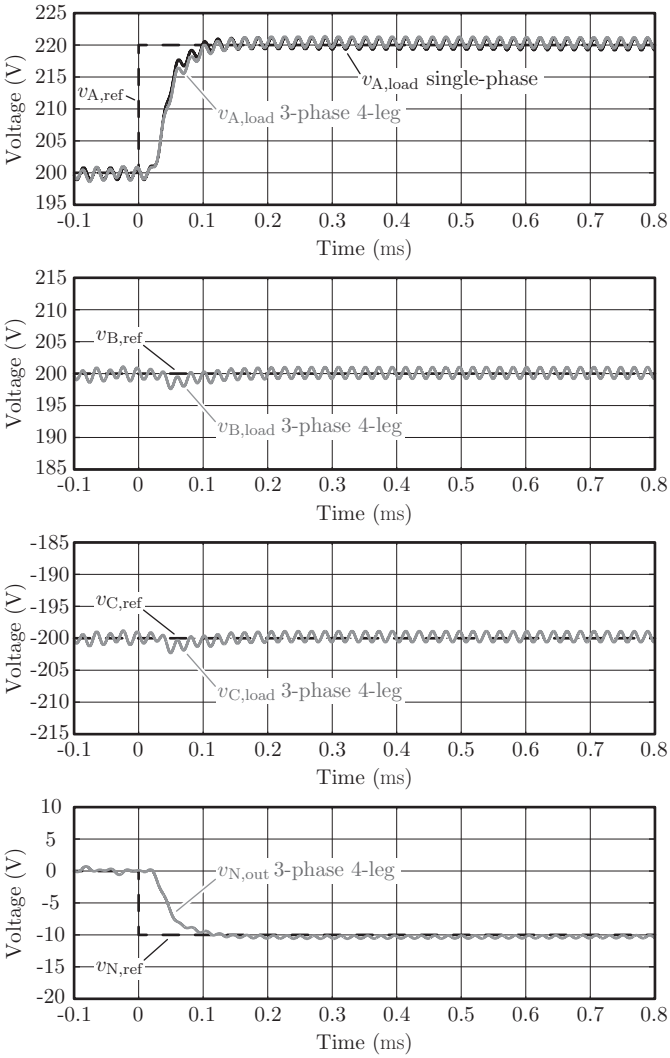


Figure 3.47: Simulated load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ and neutral leg output voltage $v_{\mathrm{N,out}}$ for a voltage reference step of 20 V for phase A and for the conditions given in Tab. 3.15. In the topmost graph the load voltage $v_{\mathrm{A,load}}$ is compared to the voltage obtained from the single-phase system [cf. Fig. 3.26(b)]. $v_{\mathrm{N,out}}$ in the lowermost graph is controlled to $v_{\mathrm{N,ref}}$ according to (3.86).

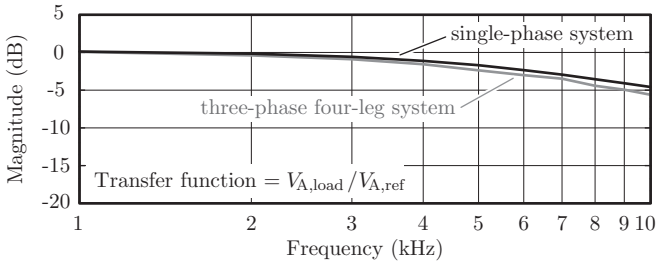


Figure 3.48: Magnitude of the small-signal transfer function $V_{A,load}(j\omega)/V_{A,ref}(j\omega)$ obtained by means of accurate circuit simulations for the three-phase four-leg realization of the output stage (cf. Fig. 3.46) and for the single-phase system [cf. Fig. 3.26(b)].

The phase output voltage $v_{A,out}$, considering phase A, complies to the given specifications as stated in Section 3.2.4. However, the load voltage of phase A is given by $v_{A,load} = v_{A,out} - v_{N,out}$, and hence it needs to be verified that also $v_{A,load}$ meets the specifications relating to the CVS' output.

For the operating conditions given in **Tab. 3.15** with nominal load, a voltage reference step of 20 V for $v_{A,ref}(t = 0) = 200$ V in phase A has been simulated and compared to the voltage reference step response of the single-phase system [cf. Fig. 3.26(b)] as shown in **Fig. 3.47**. It can be seen from the upper graph that the deviation in the load voltages $v_{A,load}$ is almost negligible and only occurs during the transient. Furthermore, it is recognizable that the load voltage step in phase A has nearly no impact on the other two phase load voltages $v_{B,load}$ and $v_{C,load}$. The control parameters for the three phases and the neutral leg are identical and are derived in Section 3.3.3 and summarized in Tab. 3.13.

Even though the simulated load voltage step response for the three-phase four-leg output stage matches nicely with the one resulting from the single-phase system, the additional neutral leg leads to a reduction of the small-signal bandwidth (-3 dB) of $v_{A,load}$ by 15.5%, from 7.1 kHz to 6 kHz, as demonstrated in **Fig. 3.48**. The figure shows the magnitudes of the small-signal transfer function $V_{A,load}(j\omega)/V_{A,ref}(j\omega)$ for the single-phase and the three-phase four-leg system, which have been obtained based on circuit simulations for the operating condition

given in Tab. 3.15. To calculate the magnitudes, the voltage reference $v_{\mathrm{A,ref}}(t) = 200\ \mathrm{V} + 20\ \mathrm{V} \cdot \sin(2 \cdot \pi \cdot f \cdot t)$, which superimposes a harmonic with an amplitude of 20 V at a frequency f on 200 V, has been applied to both systems and the resulting responses in the load voltages have been recorded. At a certain harmonic frequency f, the magnitude is given by $A_{\mathrm{f}}/20\ \mathrm{V}$, where A_{f} is the amplitude (computed by Fourier transformation) of the resulting harmonic in the load voltage $v_{\mathrm{A,load}}$. The deviation in the small-signal magnitudes of the three-phase and the single-phase system depicted in Fig. 3.48 is limited to 1 V, which is only 5% referred to the harmonic amplitude of 20 V.

Despite this reduction in the small-signal bandwidth, the simulated slew rate of $v_{\mathrm{A,load}}$, for the conditions as indicated in Section 3.2.4 and given in Tab. 3.15 with a reference voltage step of 34 V at $t = 0$, is

$$SR_{\mathrm{sim}} = \frac{34\ \mathrm{V}}{88\ \mu\mathrm{s}} = 386\ \mathrm{V/ms} > 203\ \mathrm{V/ms} \tag{3.87}$$

and hence greater than the value of 203 V/ms specified in Chapter 1. Moreover, the transient output impedance Z_{step} (as a measure of the transient voltage dip of $v_{\mathrm{A,load}}$ due to a stepwise change of $i_{\mathrm{A,out}}$) is, for the conditions indicated in Section 3.2.4 and in Tab. 3.15, increased by 11.9%, from 4.2 Ω to

$$Z_{\mathrm{step,sim}} = \frac{15.9\ \mathrm{V}}{3.4\ \mathrm{A}} = 4.7\ \Omega < 5.6\ \Omega, \tag{3.88}$$

which is though still lower than the required value of 5.6 Ω (cf. Tab. 1.2).

Furthermore, as it can be seen from Fig. 3.47, the three-phase four-leg output stage of the CVS does not lead to a higher load voltage ripple than the one resulting from the single-phase counterpart. Accordingly, since the single-phase system complies to the load voltage quality requirement given in Tab. 1.2 with quite a margin, it is self-evident that also the three-phase four-leg realization of the output stage fulfills the mentioned requirement (cf. Section 3.2.4).

It is noted that the above described slight degradation of the small-signal bandwidth and transient output impedance for the three-phase four-leg output stage can be avoided by employing a three-phase plus neutral conductor converter [cf. Fig. 3.1(a)] which, however, does not allow anymore maximizing the range of the load voltages.

3.4.1 Summary

In this section, the selected capacitor current feedback control structure, laid out based on single-phase considerations, is implemented for all three phases and the neutral leg of the output stage [cf. Fig. 3.1(b)], where the designed single-phase two-stage LC filter is employed for each phase and the neutral leg. With this four-line output filter, the load phase voltages, i.e. the voltages applied to the load for each phase, result from the differences between the phase output voltages and the neutral leg's output voltage, e.g. $v_{\mathrm{A,load}} = v_{\mathrm{A,out}} - v_{\mathrm{N,out}}$ for phase A. This leads to a slight adjustment of the capacitor current feedback control scheme as given in Fig. 3.46, where the output voltage reference of the phases is changed from $v_{i,\mathrm{ref}}$ (single-phase consideration) to $v_{i,\mathrm{ref}}+v_{\mathrm{N,ref}}$ (for $i = A, B, C$; $v_{\mathrm{N,ref}}$ is the output voltage reference of the neutral leg).

For this three-phase four-line converter the transient responses for $v_{\mathrm{A,load}}$ are showing slightly lower dynamics compared to the responses achieved for $v_{\mathrm{A,out}}$. The small-signal bandwidth is reduced by 15.5%, from 7.1 kHz to 6 kHz, but it is still higher than 5 kHz (specification), and the transient output impedance, due to a load step, is increased by 11.9%, from 4.2 Ω to 4.7 Ω, for instance. Nevertheless, all specifications for the output stage as summarized in Tab. 1.2 can be fulfilled with the three-phase four-leg converter and Fig. 3.47 shows an almost perfect conformity between the load voltage step response of the three-phase four-leg and the single-phase system. Simulative investigations revealed the same conclusion for other operating conditions, e.g. for the ones given in Tab. 3.15 with $v_{\mathrm{N,out}} = 0$. This strongly justifies first employing a single-phase approach for designing the output filter and the output voltage control scheme and then to apply the obtained results to the three-phase four-leg output stage in a second step.

Furthermore, the importance of a good disturbance rejection, as achieved with the designed control scheme in Section 3.3, becomes evident by considering the neutral leg of the three-phase four-leg converter. The output current of this leg is impressed by the phase load voltages and the load, which varies according to the demanded range of application of the CVS (cf. Chapter 1).

3.5 Input Stage

Three-phase voltage-source AC–DC converters with sinusoidal input current, also denominated as Power Factor Correction (PFC) rectifiers, are widely used, e.g. as input stages of telecommunication power supply modules [263], active front ends of variable speed drives [264], and / or uninterruptible power supplies [265].

The bidirectional converter system, also denominated as PWM rectifier, considered in this section is depicted in **Fig. 3.49** and is employed as input stage of the CVS. The electrical specifications for the CVS' input stage are summarized in **Tab. 3.16**.

Mains-connected converter systems need to comply with international standards limiting the amplitudes of the low-frequency and the high-frequency input current harmonics. The low-frequency harmonics standards usually consider only ordinal numbers ≤ 40, i.e. $f_{\mathrm{h}} \leq 2\,\mathrm{kHz}$ for 50 Hz systems (e.g. EN 61000-3-2 / EN 61000-3-12). Thus, for the selected switching frequency of the system of $f_{\mathrm{s,in}} = 48\,\mathrm{kHz}$ (cf. Tab. 3.16), these regulations can be fulfilled with a proper sinusoidal mains current control.

The standards limiting the amplitudes of the high-frequency spectral components specify the threshold in terms of conducted noise emission (measured in dBµV), i.e. for the case at hand in the frequency range of $[150\,\mathrm{kHz}, 30\,\mathrm{MHz}]$ for CISPR 11, Class A [36].[29] Hence, the multi-stage EMI input filter of the considered PWM rectifier system, with first and second stages comprising each DM and CM filter parts (cf. Fig. 3.49), needs to be designed such that the levels of the conducted emissions are below the specified limits. Additionally, the maximum peak-to-peak current ripple of the bridge-leg input currents, e.g. i_{a0} (cf. Fig. 3.49), is typically limited to 20%–60% of the nominal fundamental current amplitude, i.e. $\sqrt{2} \cdot I_{\mathrm{in,n}}$. This avoids a performance degradation of the control of the input currents i_{a0}, i_{b0}, and i_{c0} in case of small time deviations from the ideal sampling instants, and keeps the high-frequency winding and core losses of the inductive components (mainly $L_{\mathrm{dm,1}}$ and $L_{\mathrm{cm,1}}$) at reasonable values.

To be able to utilize the full (linear) modulation range, e.g. to maintain converter operation also for an increase of the mains voltage of 10%

[29] Radiated disturbances in the frequency range from 30 MHz to 1 GHz (measured in dBµV/m at a distance of 10 m) are limited by CISPR 11 as well. Typically, the compliance to the standard for this type of emissions can be achieved with a proper casing on the converter.

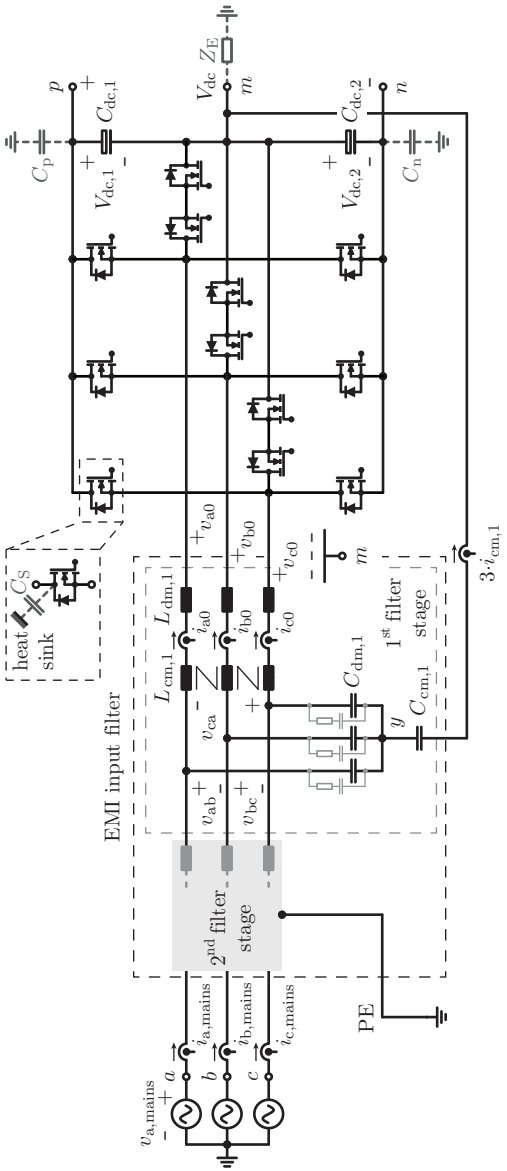


Figure 3.49: Bidirectional three-phase three-level PWM rectifier system with an EMI input filter, which builds the input stage of the CVS.

Table 3.16: Electrical parameters of the bidirectional three-phase PWM rectifier system shown in Fig. 3.49, which builds the input stage of the CVS. [1)] The input stage needs to cover the losses of the DC link and the output stage and hence the power rating needs to be higher than the one of the output stage, i.e. higher than $P_{\mathrm{out,n}} = 10$ kW (cf. Tab. 3.1). However, because the total losses of the output stage, including the DC link, are estimated to only 226 W, the input stage is still rated at $P_{\mathrm{in,n}} = 10.2$ kW ≈ 10 kW. [2)] The estimated efficiency of the output stage is $\eta_{\mathrm{out,n}} = 97.7\%$ and accordingly the required minimum efficiency of the input stage is $\eta_{\mathrm{in,n}} = \eta_{\mathrm{tot,n}}/\eta_{\mathrm{out,n}} = 95\%/97.7\% = 97.2\%$ (cf. Tab. 1.1).

Nominal input power, $P_{\mathrm{in,n}}$	10 kW[1)]
Mains voltage, V_{mains} (rms value)	400 V_{ll} (+10%, − 14% [37])
Nominal rms input current, $I_{\mathrm{in,n}}$	14.5 A
Nominal peak input current, $I_{\mathrm{in,n,pk}}$	20.5 A
Nominal DC link voltage, $V_{\mathrm{dc,n}}$	700 V
Mains frequency, f_{mains}	50 Hz
Switching (carrier) frequency, $f_{\mathrm{s,in}}$	48 kHz
Nominal efficiency, $\eta_{\mathrm{in,n}}$	$\geq 97.2\%$[2)]

(cf. Tab. 3.16), and to reduce the rectifier switching frequency input current ripple, a SVM or a carrier based sinusoidal modulation with a superimposed zero-sequence component can be employed. For simplicity of implementation, this section considers the latter scheme with a zero-sequence component equal to

$$v_{\mathrm{zs}} = -\frac{\max\left(v_{\mathrm{a}}, v_{\mathrm{b}}, v_{\mathrm{c}}\right) + \min\left(v_{\mathrm{a}}, v_{\mathrm{b}}, v_{\mathrm{c}}\right)}{2}, \tag{3.89}$$

which results for regular sampling in an equivalent performance than SVM with symmetrical modulation (always employing the nearest vectors to the reference vector) [78]. v_{zs} shows a triangular shape with fundamental period $3 \cdot f_{\mathrm{s,in}}$.

Because the rectifier bridge-leg input voltages v_{a0}, v_{b0}, and v_{c0} contain three discrete voltage levels, the sum of all rectifier voltages $v_{\mathrm{a0}} + v_{\mathrm{b0}} + v_{\mathrm{c0}}$ is in general not zero resulting in the formation of a CM voltage component. The definitions of CM and DM voltages and

currents are:

$$\begin{array}{lcl} v_{0,\mathrm{cm}} & = & \frac{v_{\mathrm{a0}}+v_{\mathrm{b0}}+v_{\mathrm{c0}}}{3}, \\ v_{\mathrm{a0,dm}} & = & v_{\mathrm{a0}} - v_{0,\mathrm{cm}}, \\ i_{0,\mathrm{cm}} & = & \frac{i_{\mathrm{a0}}+i_{\mathrm{b0}}+i_{\mathrm{c0}}}{3}, \\ i_{\mathrm{a0,dm}} & = & i_{\mathrm{a0}} - i_{0,\mathrm{cm}}. \end{array} \tag{3.90}$$

Thus, considering the selected modulation scheme and the voltage formation, the bridge-legs and the DC link in Fig. 3.49 can be replaced for each phase, e.g. phase a, by a low-frequency DM voltage source $v_{\mathrm{a0,dm,lf}}$ (at f_{mains}), a high-frequency DM voltage source $v_{\mathrm{a0,dm,hf}}$ (for harmonics around $n \cdot f_{\mathrm{s,in}}, n = 1,2,...$), a low-frequency CM voltage source $v_{0,\mathrm{cm,lf}}$ (at $n \cdot 3 \cdot f_{\mathrm{mains}}, n = 1,2,...$) and a high-frequency CM voltage source $v_{0,\mathrm{cm,hf}}$ (around $n \cdot f_{\mathrm{s,in}}, n = 1,2,...$) as shown in **Fig. 3.50**. Furthermore, a possible realization of the second EMI filter stage (cf. Fig. 3.49) as a DM and a CM LCL stage is depicted in Fig. 3.50. For a defined attenuation, however, the volume of a single-stage filter is considerably larger than the volume of a two-stage filter, cf. pp. 400–403 in [266]. Thus, in industrial applications, two-stage filters are of high interest.[30]

To comply to CISPR 11, the noise generated by the high-frequency voltage sources $v_{\mathrm{a0,dm,hf}}$ (DM) and $v_{0,\mathrm{cm,hf}}$ (CM) needs to be filtered. DM noise is bounded to the phases, while CM noise returns via ground and hence the filtering of DM and CM noise requires different strategies [184]. To filter the CM noise has gained special attention, not only for PWM rectifier systems with sinusoidal input current but also for variable speed drive systems, where the reduction of bearing currents is of primary concern [267]. The CM noise filtering can be achieved with either active and / or passive techniques [268]. Active methods employ active devices and control [268] and can basically be separated into five groups. First, PWM techniques which reduce the CM voltage $v_{0,\mathrm{cm,hf}}$ [269, 270]; second, concepts which generate by an additional power stage a compensating CM voltage[31] coupled to the filter

[30] It is additionally noted that typically the entire required DM and CM attenuations are not provided by only one filter stage, as this would require high inductance and / or capacitance values which would lead to physically large components with increased parasitic component values. Thus, such a filter stage would show a reduced attenuation at higher frequencies, which is undesired considering that the noise emissions need to be below the limits given in CISPR 11 in the frequency range [150 kHz, 30 MHz].

[31] The idea of these concepts is to ideally completely compensate the noise source CM voltage $v_{0,\mathrm{cm,hf}}$ (cf. Fig. 3.52), i.e. the remaining CM voltage, which drives a CM current through the LISN, would be zero and accordingly no CM current would be flowing.

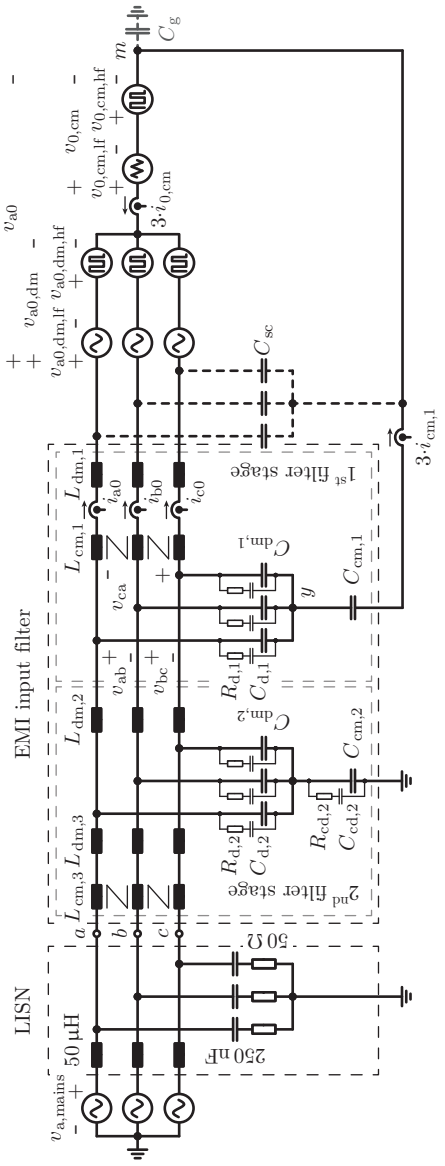


Figure 3.50: Equivalent circuit of the bidirectional three-phase three-level PWM rectifier system depicted in Fig. 3.49. The heat sink is connected to the midpoint of the DC link m.

through an inductive element [271–275]; third, structures which adjust the impedance in the CM path which returns to the noise source [276, 278, 279];[32] fourth, techniques which employ a fourth bridge-leg to actively provide zero CM voltage at the rectifier's input [280]; and fifth, topologies which inject a compensating CM current [277].

The use of additional active devices, i.e. an extra power stage and / or a fourth bridge-leg, increases the system's complexity and may cause deviations from the ideal CM waveforms due to measurement processing and / or switching delays. Often an reduction of the CM noise emission can be observed for frequencies lower than 500 kHz ... 2.5 MHz [271, 276–278]. For higher frequencies additional passive elements are required to sufficiently suppress the noise. It is noted that the method proposed in [280], in principle, requires no CM input filter, however, certain limitations would apply to the rectifier (freewheeling state cannot be used and the modulation index is limited to 66%). Concluding, active CM filters require additional active units (including their driving units), accurate measurement units with an extremely high bandwidth (to achieve the required attenuation for 150 kHz $< f <$ 30 MHz) and / or a very precise synchronization to the switching of the power converter and are, to the best knowledge of the author, for these reasons typically not considered in state-of-the-art industry applications, since the complexity added to the system may often not outweigh the potential benefits.

Passive techniques employ mainly inductors and capacitors to provide adequate filtering [184, 267, 281–283]. In [281, 283] for instance, a four-winding CM choke is employed for which the fourth winding is fed by a certain network, i.e. a passive RC network [281] or a three-phase inductor network [283]. The passive networks are either lossy and / or require, in case of the inductor network, three additional decoupling capacitors. Often, active techniques are combined with passive ones leading to hybrid filters [278, 279]. For its robustness and simplicity to be implemented on the hardware, an industry-oriented passive filtering is proposed in this work, although it may result in a larger volume of the EMI filter compared to a filter realized with an active and / or hybrid technique [268].

As elaborated in **Appendix D**, the bottleneck of conventional passive CM filters [cf. **Fig. 3.52(d)**], besides the incompletely known

[32] In [276] for instance, a voltage feedback structure is employed to emulate a high CM capacitance.

parasitic elements [184, 268], is the limited allowed capacitance of the Y-capacitors (a few tens of nanofarads) connected to ground in order not to exceed the maximum allowed protective conductor current against Protective Earth (PE)[33] and the maximum admissible touch current.[34] For this reason and to reduce the CM noise emissions, [286] and [282, 287] proposed for a three-phase PWM drive system inverter and for a three-phase PWM Vienna Rectifier I, respectively, to directly connect the star-point y of the first DM filter stage to the midpoint of the DC link m (cf. Fig. 3.49). With the same target, this CM filter structure was then adopted in [184] for a rectifier switching at 1 MHz and applied to motor driving inverters [267,288]. In this filter structure, the three DM capacitors $C_{\mathrm{dm},1}$ build the equivalent CM capacitance. To allow for an adjustment of the CM capacitance independent of the DM capacitance, it is preferred to achieve the filtering with an internal CM filter capacitor $C_{\mathrm{cm},1}$ that is connected between the star-point y of the DM capacitors $C_{\mathrm{dm},1}$ and the midpoint of the DC link m (cf. Fig. 3.49) [157]. $C_{\mathrm{cm},1}$ together with an additional CM inductor $L_{\mathrm{cm},1}$ in series to the DM boost inductors $L_{\mathrm{dm},1}$ builds then a CM LC filter stage. For $C_{\mathrm{cm},1}$ higher capacitance values can be employed compared to a Y-capacitor connected to PE and hence the low-frequency as well as a main share of the high-frequency CM currents, $i_{0,\mathrm{cm,lf}}$ and $i_{0,\mathrm{cm,hf}}$, are confined to the converter system. As further discussed in Sections 3.5.1 and 3.5.2, on the one hand, this has the advantages that most of the high-frequency current is kept apart from the load or converter system supplied by the rectifier, and thus the high-frequency fluctuation of the DC link midpoint potential with respect to ground is reduced significantly (reduced current through C_{g}, cf. Fig. 3.50). But on the other hand, the disadvantage is that the low-frequency CM current $i_{\mathrm{cm,1,lf}} = i_{0,\mathrm{cm,lf}}$ is increased because the impedance of the CM choke $L_{\mathrm{cm},1}$ is typically negligible compared to the impedance of

$$C_{\mathrm{cm,1,eff}} = \frac{C_{\mathrm{cm},1} \cdot 3 \cdot C_{\mathrm{dm},1}}{(C_{\mathrm{cm},1} + 3 \cdot C_{\mathrm{dm},1})} \approx C_{\mathrm{cm},1} \tag{3.91}$$

(assuming $C_{\mathrm{dm},1}$ to be at least one order of magnitude larger than $C_{\mathrm{cm},1}$) at $3 \cdot f_{\mathrm{mains}}$. In this way, the zero-sequence component of the

[33] According to EN 61140 for common aspects to protect against electrical shocks, the limit is 5 mA (rms value) [284].

[34] Referring to EN 60335-1 for household and similar electrical appliances or EN 60950-1 for information technology equipment, the limit is 3.5 mA (peak value) [285].

rectifier input voltage generated by the selected modulation scheme is directly applied to $C_{\mathrm{cm},1}$ [cf. **Fig. 3.52(b)**]. Thus, a lower impedance value of $C_{\mathrm{cm},1}$ at $3 \cdot f_{\mathrm{mains}}$, resulting from an increased capacitance of $C_{\mathrm{cm},1}$, increases the low-frequency CM current $i_{0,\mathrm{cm,lf}}$. Accordingly, to limit the amplitude of $i_{0,\mathrm{cm,lf}}$ to reasonable values, the capacitance of $C_{\mathrm{cm},1}$ cannot exceed a certain maximum value.

Remark: It is assumed above that the midpoint of the DC link m shows a parasitic capacitance C_{g} to ground and that the entire low-frequency CM current is flowing through the return path (from y to m) built by $C_{\mathrm{cm},1}$ - i.e. the magnitude of the impedance of $C_{\mathrm{cm,1,eff}}$ [cf. (3.91); damping elements neglected] is assumed to be much lower than the one of C_{g} at $3 \cdot f_{\mathrm{mains}}$ [cf. (3.96) and Fig. 3.52(b)], leading to $i_{\mathrm{cm,1,lf}} = i_{0,\mathrm{cm,lf}}$ in Fig. 3.50.

Moreover, the CM current ripple, which is mainly defined by the impedance of $L_{\mathrm{cm},1}$, superimposes on the DM current ripple. Hence, considering Fig. 3.50 and phase a, both, the DM current $i_{\mathrm{a0,dm}}$ as well as the CM current $i_{0,\mathrm{cm}}$ contribute to the maximum peak-to-peak bridge-leg input current ripple, i.e.

$$\begin{aligned} \Delta i_{\mathrm{a0,pp,max}} \quad = \quad & \max\left\{ i_{\mathrm{a0,dm,hf}}(t) + i_{0,\mathrm{cm,hf}}(t) \right\} \\ & - \min\left\{ i_{\mathrm{a0,dm,hf}}(t) + i_{0,\mathrm{cm,hf}}(t) \right\} \end{aligned} \tag{3.92}$$

(considered for a pulse period), where $i_{\mathrm{a0,dm,hf}}$ is generated by $v_{\mathrm{a0,dm,hf}}$ and $i_{0,\mathrm{cm,hf}}$ by $v_{0,\mathrm{cm,hf}}$. Therefore, if $\Delta i_{\mathrm{a0,pp,max}}$ should be kept constant, a weaker limitation of the peak value of $i_{\mathrm{a0,dm,hf}}$ (smaller inductance of $L_{\mathrm{dm},1}$) requires a stronger limitation of the peak value of $i_{0,\mathrm{cm,hf}}$ (higher inductance of $L_{\mathrm{cm},1}$) and vice versa. Accordingly, the ratio between $L_{\mathrm{dm},1}$ and $L_{\mathrm{cm},1}$ represents a degree of freedom in the filter design. For the theoretical case of $L_{\mathrm{dm},1} \to \infty$, the DM as well as the CM current ripple would be zero. On the other hand, for $L_{\mathrm{cm},1} \to \infty$ only the CM current ripple would vanish (neglecting the straying of the CM choke). This can be seen as the case for which $L_{\mathrm{cm},1}$ is large enough to almost completely suppress the CM current ripple (and for which the stray inductance $L_{\sigma,1}$ of $L_{\mathrm{cm},1}$, which provides DM filtering, is negligible compared to $L_{\mathrm{dm},1}$). Accordingly, there exists a minimum value of $L_{\mathrm{dm},1}$ to achieve a certain maximum peak-to-peak current ripple $\Delta i_{\mathrm{a0,pp,max}}$.

Furthermore, the boxed volume of the DM and CM inductors $V_{\mathrm{L,dm,1}}$ and $V_{\mathrm{L,cm,1}}$ scales with the inductance values $L_{\mathrm{dm},1}$ and $L_{\mathrm{cm},1}$ (assuming certain system specifications, cf. Tab. 3.16). Without loss of generality,

it can be written

$$V_{\mathrm{L,dm,1}} \propto k_{\mathrm{dm}} \cdot {L_{\mathrm{dm,1}}}^{\alpha_{\mathrm{dm}}}, \quad V_{\mathrm{L,cm,1}} \propto k_{\mathrm{cm}} \cdot {L_{\mathrm{cm,1}}}^{\alpha_{\mathrm{cm}}}, \tag{3.93}$$

where in a general case $k_{\mathrm{dm}} \neq k_{\mathrm{cm}}$ and $\alpha_{\mathrm{dm}} \neq \alpha_{\mathrm{cm}}$ and hence the volumes of the DM and CM inductors do not scale identically with $L_{\mathrm{dm,1}}$ and $L_{\mathrm{cm,1}}$, respectively. Hence, potentially an optimal ratio

$$k_{\mathrm{L,opt}} = \frac{L_{\mathrm{cm,1}}}{L_{\mathrm{dm,1}}} \tag{3.94}$$

exists which minimizes the total boxed volume $V_{1,\mathrm{tot}} = 3 \cdot V_{\mathrm{L,dm,1}} + V_{\mathrm{L,cm,1}} + 3 \cdot V_{\mathrm{C,dm,1}} + V_{\mathrm{C,cm,1}}$ of the first EMI input filter stage (cf. Fig. 3.49). Accordingly, the main focus of the following analysis is on the minimization of the boxed volume $V_{1,\mathrm{tot}}$ of the first EMI filter stage, which has not been discussed in literature so far. Section 3.5.1 motivates the structure of the first DM / CM LC stage of the EMI input filter shown in Fig. 3.49 including the discussion if the heat sink should be better connected to ground or to the midpoint of the DC link to achieve a higher CM filter attenuation. Section 3.5.2 explains the electrical side conditions, e.g. for the maximum peak-to-peak DM and CM voltage ripple across $C_{\mathrm{dm,1}}$ and $C_{\mathrm{cm,1,eff}}$ [cf. (3.91) and Fig. 3.50] respectively, to have a well-defined interface of this first filter stage to the second stage as well as to the rectifier. The proposed approach for minimization of the volume and / or to determine $k_{\mathrm{L,opt}}$ is presented in Section 3.5.3. Because the DM and CM inductor modeling is crucial for the optimization, Section 3.5.4 describes the detailed modeling of the two inductive filter components. Subsequently, the optimization results are presented in Section 3.5.5 and the design of the second filter stage, realized as a DM / CM LCL stage to comply with CISPR 11, is explained in Section 3.5.6. Finally, Section 3.5.7 successfully validates the proposed EMI filter design by experimental results including EMI measurements employing a three-phase DM / CM noise separator. In the end, conclusions are drawn in Section 3.5.8.

3.5.1 Structure of the First Stage of the EMI Input Filter

The equivalent circuit shown in Fig. 3.50 can be separated into single-phase DM and CM equivalent circuits [184] as depicted in **Figs. 3.51**

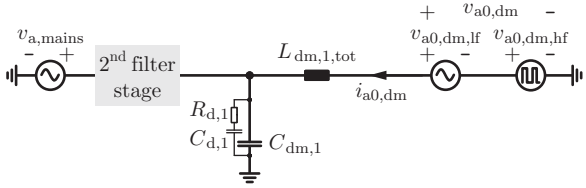


Figure 3.51: DM equivalent circuit of the three-phase three-level PWM rectifier system (cf. Figs. 3.49 and 3.50).

and **3.52(a)**. $L_{\mathrm{dm,1,tot}}$ and $L_{\mathrm{cm,1,tot}}$ are the total inductances which limit the DM and CM currents,

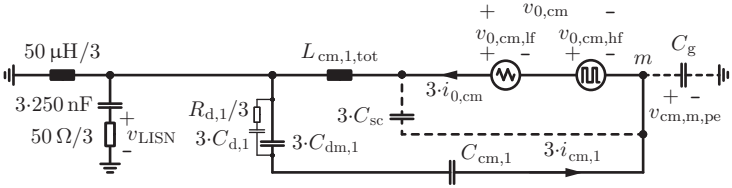
$$L_{\mathrm{dm,1,tot}} = L_{\mathrm{dm,1}} + L_{\sigma,1}, \quad L_{\mathrm{cm,1,tot}} = L_{\mathrm{cm,1}} + \tfrac{L_{\mathrm{dm,1}}}{3}, \tag{3.95}$$

where $L_{\mathrm{dm,1}}$ denotes the inductance of the DM inductor, $L_{\mathrm{cm,1}}$ is the CM inductance and $L_{\sigma,1}$ is the leakage inductance of the CM choke as further explained in Section 3.5.4.

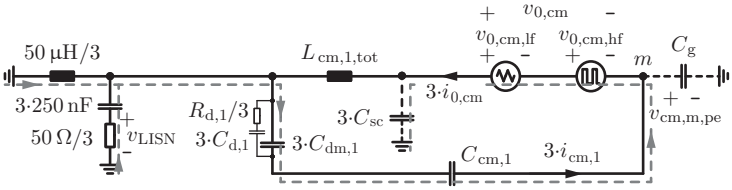
To compare the proposed filter structure comprising a capacitor $C_{\mathrm{cm,1}}$ connected between y and m to a conventional EMI filter where a Y-capacitor $C_{\mathrm{cm,1,pe}}$ is connected between y and ground (PE) in terms of achievable CM attenuation, the parasitic capacitances from the converter to ground and the heat sink (cf. Fig. 3.49 and [184]) need to be considered:

- C_{p} and C_{n}: parasitic capacitances of the positive and negative DC link rails to ground.
- Z_{E}: parasitic impedance of the DC link midpoint m to ground. Typically, this impedance is modeled by a capacitor, i.e. $Z_{\mathrm{E}} = \frac{1}{s \cdot C_{\mathrm{E}}}$ [184], and is mainly defined by the load and / or converter circuit supplied by the rectifier.
- C_{S}: parasitic capacitances of the SiC MOSFETs (including the internal antiparallel diodes) to the heat sink, which is common for all switches for the considered hardware (cf. Section 3.5.7). For the given T-type PWM rectifier the parasitic capacitance to the heat sink of each phase is $C_{\mathrm{sc}} = 2 \cdot C_{\mathrm{S}}$ (cf. Fig. 3.50).

The parasitic capacitances from the positive and negative DC link rails to ground as well as the capacitance from the DC link midpoint to



(a) Heat sink connected to m



(b) Heat sink connected to PE

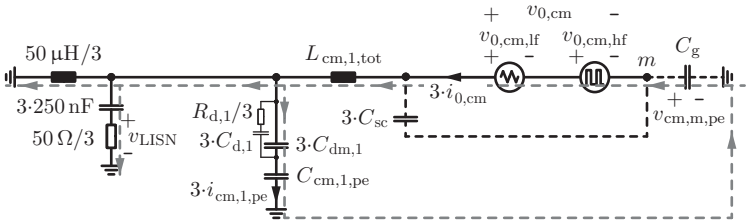
Figure 3.52: CM equivalent circuits of the three-phase three-level PWM rectifier system (cf. Figs. 3.49 and 3.50) with a LISN connected to the first filter stage (the second filter stage is not shown / omitted). For **(a)** and **(b)** an internal capacitor $C_{\mathrm{cm},1}$ between y and m is employed; **(c)** and **(d)** represents the conventional CM filtering with a Y-capacitor $C_{\mathrm{cm},1,\mathrm{pe}}$ between y and ground (PE); and **(e)** uses bypassing capacitors $C_{\mathrm{cm},0,\mathrm{pe}}$ from the bridge-leg inputs to PE. The heat sink is connected to m for (a) and (c); it is tied to PE for (b), (d), and (e).

ground are, in the CM equivalent circuit [cf. Fig. 3.52(a)], all in parallel (because $C_{\mathrm{dc},1} = C_{\mathrm{dc},2} \gg C_{\mathrm{p}}$ and C_{n}) and can, thus, be summarized to one capacitance

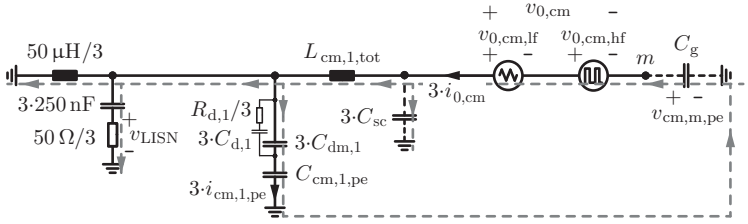
$$C_{\mathrm{g}} = C_{\mathrm{p}} + C_{\mathrm{n}} + C_{\mathrm{E}}, \tag{3.96}$$

which is typically in the range of several nF and, hence, much larger than C_{sc}, i.e. $C_{\mathrm{g}} \gg C_{\mathrm{sc}}$.

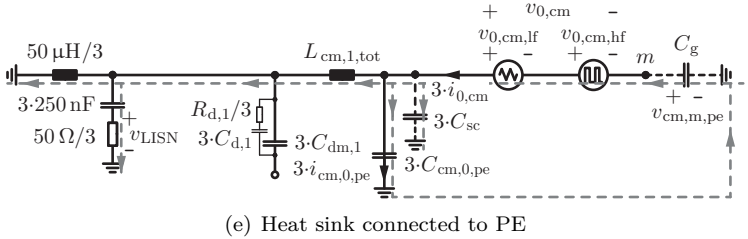
The heat sink can for both filter options, i.e. $C_{\mathrm{cm},1}$ between y and m and $C_{\mathrm{cm},1,\mathrm{pe}}$ between y and PE, either be connected to ground or to the midpoint m of the DC link. A grounded heat sink simplifies the assembly of the converter, i.e. the heat sink can directly be screwed to the grounded case (no isolation required). This results in four different CM equivalent circuits as depicted in Figs. 3.52(a) – 3.52(d). Typically, the conducted noise emissions are measured with a Line Impedance



(c) Heat sink connected to m



(d) Heat sink connected to PE



(e) Heat sink connected to PE

Fig. 3.52: Continued.

Stabilization Network (LISN) connected between mains and converter system, and thus for the following calculation, a 50 Ω/50 µH LISN is directly connected to the first filter stage (not considering the second filter stage, cf. **Fig. 3.52**).

Additionally to the four CM filtering options in Figs. 3.52(a) – 3.52(d), the filter topology shown in **Fig. 3.52(e)** represents an alternative approach. The idea is to provide, for the generated CM noise current through C_{g}, a low-impedance path back to the noise source immediately at the bridge-leg inputs by three Y-capacitors $C_{\mathrm{cm,0,pe}}$ connected from each phase to PE resulting in an effective CM capacitance

of $3 \cdot C_{\mathrm{cm,0,pe}}$. As it can be seen from Fig. 3.52(e), $3 \cdot C_{\mathrm{cm,0,pe}}$ and $3 \cdot C_{\mathrm{sc}}$ are in parallel for a grounded heat sink. Because the parasitic capacitance C_{sc} (in the range of pF) of the switches to the heat sink for each phase is typically much smaller than $C_{\mathrm{cm,0,pe}}$ (in the range of nF), i.e. $C_{\mathrm{cm,0,pe}} \gg C_{\mathrm{sc}}$, it follows that $3 \cdot C_{\mathrm{cm,0,pe}} + 3 \cdot C_{\mathrm{sc}} \approx 3 \cdot C_{\mathrm{cm,0,pe}}$ and hence the achievable attenuations with this filter structure do almost not change whether the heat sink is connected to PE or m. Accordingly, only the equivalent circuit with a grounded heat sink given in Fig. 3.52(e) is further considered.

It can be seen from **Fig. 3.53** that, depending on the CM filtering approach (cf. Fig. 3.52), the value of C_{g} can have a significant impact on the achievable CM attenuation (up to a difference of 32 dB). The larger the capacitance C_{g} the less attenuation is obtained. Typically a high capacitance results for motor drive systems. Referring to literature, C_{g} is in the range of 8.5 nF to 11 nF for three-phase 400 $\mathrm{V_{ll}}$ (rms) induction machines with a power between 3 kW and 15 kW [289, 290]. To keep the EMI emissions below the limits given by standards also for large C_{g}, the maximum capacitance of it is assessed to 25 nF (including a margin of nearly a factor of 2.5).

Additionally, the value of C_{g} also has a direct implication on the maximum allowable value of $C_{\mathrm{cm,1,pe}}$ [cf. **Figs. 3.52(c)** and 3.52(d)] and $C_{\mathrm{cm,0,pe}}$ [cf. Fig. 3.52(e)]: As it is derived in Appendix D, if the maximum touch current is limited to 3.5 mA according to EN 60335-1, the maximum allowable capacitances of $C_{\mathrm{cm,1,pe}}$ and $C_{\mathrm{cm,0,pe}}$ are

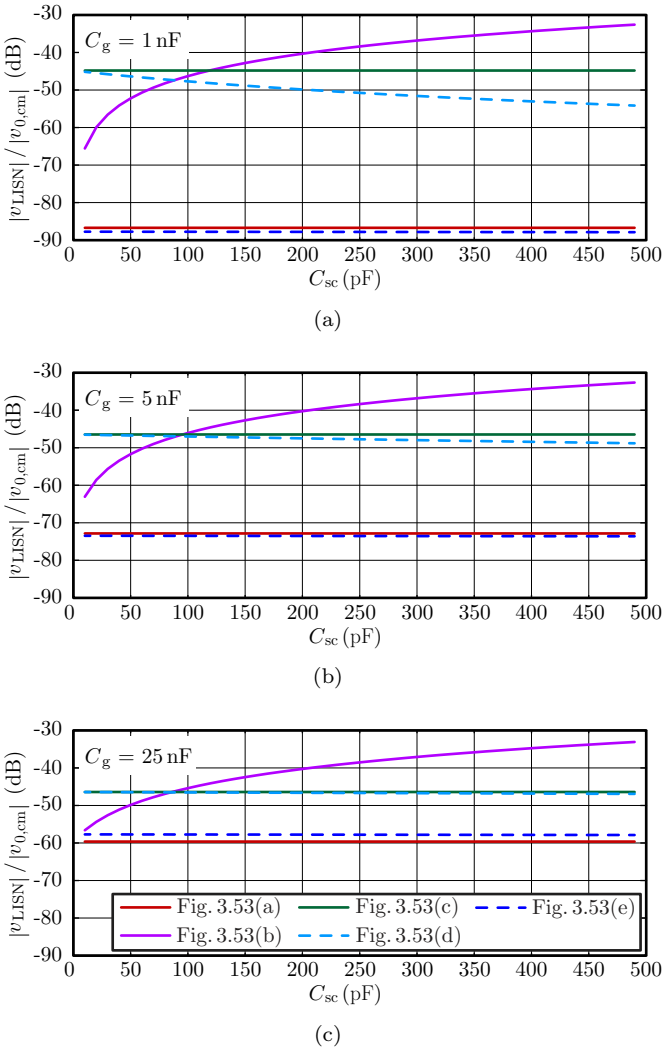
$$C_{\mathrm{cm,1,pe,max}} = \frac{3.5\ \mathrm{mA}}{\pi \cdot f_{\mathrm{mains}} \times 110\% \times \sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3}} - \frac{12}{\pi^2} \cdot C_{\mathrm{g}} \approx 31\ \mathrm{nF} \tag{3.97}$$

and

$$C_{\mathrm{cm,0,pe,max}} = \frac{C_{\mathrm{cm,1,pe,max}}}{2} \approx 15.5\ \mathrm{nF}, \tag{3.98}$$

assuming a +10% tolerance of the mains voltage and a parasitic capacitance of $C_{\mathrm{g}} = 25$ nF between the midpoint m of the DC link and ground (PE).

Thus, the maximum allowed touch current limits directly the maximum value of the CM Y-capacitors and accordingly their effectiveness concerning the achievable filter attenuation. It is noted that the CM capacitance $C_{\mathrm{cm,2}}$ of the second EMI filter stage (cf. Fig. 3.50) is limited according to (3.97) as well, i.e. $C_{\mathrm{cm,2,max}} = C_{\mathrm{cm,1,pe,max}}$ [cf. (3.97)],



(a)

(b)

(c)

Figure 3.53: CM attenuations of the first stage of the EMI filter for the five approaches shown in Fig. 3.52 and for different parasitic capacitances C_g between the DC midpoint m and PE: **(a)** $C_g = 1$ nF, **(b)** $C_g = 5$ nF, and **(c)** $C_g = 25$ nF. The attenuations are calculated at $f_{emi} = 192$ kHz, i.e. at the first harmonic frequency within the range [150 kHz, 30 MHz] which is relevant for the EMI emissions measurement. *Circuit parameters*: see Fig. 3.54.

because, besides a faulty PE, only one additional fault in the EMI filter needs to be considered at once (cf. Appendix D). [35]

The impact of the parasitic capacitances C_g and C_{sc} on the achievable CM attenuations of the CM filter structures in Fig. 3.52 are given in Fig. 3.53, which leads to the following conclusions for each individual CM filter:

- *Internal CM capacitor $C_{cm,1}$ between y and m, cf. Figs. 3.52(a) and 3.52(b)*: The higher the values of C_g, the lower the achieved attenuation (maximum reduction is 27 dB). Furthermore, C_{sc} has no impact on the attenuation for a heat sink connected to m (red solid lines in Fig. 3.53), meanwhile the attenuation reduces quite significantly with increasing C_{sc} for a heat sink connected to ground (magenta curves in Fig. 3.53). For the hardware at hand (cf. Section 3.5.7), which employs Hi-Flow™ 625 electrical insulation pads manufactured by The Bergquist Company, the measured parasitic capacitance between the switches (TO-247 packages) of one phase and the heat sink is $C_{sc} = 267$ pF. For this capacitance value, a connection of the heat sink to m instead of ground achieves an attenuation which is by 23 dB higher ($C_g = 25$ nF). This higher attenuation can be explained by the fact that for a grounded heat sink there exists an alternative path which bypasses the CM inductor $L_{cm,1}$ as depicted in Fig. 3.52(b). Accordingly, it is preferred to connect the heat sink to the midpoint of the DC link m, especially for high values of C_{sc}.

- *CM capacitor $C_{cm,1,pe}$ between y and PE, cf. Figs. 3.52(c) and 3.52(d)*: Increasing values of C_g are only perceivably reducing the achievable attenuation for higher values of C_{sc} and for a heat sink connected to PE (dashed light blue curves in Fig. 3.53): for $C_{sc} = 267$ pF, the attenuation is reduced by 4 dB if C_g is increased

[35] It is remarked, that the CM capacitance $C_{cm,1,pe}$ in Figs. 3.52(c) and 3.52(d) could also be realized by three Y-capacitors $C_{cm,1,pe,s} = C_{cm,1,pe}/3$ connected from each phase to PE. In order not to exceed the maximum touch current, the maximum allowable value of $C_{cm,1,pe,s}$ is limited to $C_{cm,1,pe,s,max} = C_{cm,1,pe,max}/2$ according to (3.98), leading to a maximum effective CM capacitance of $3 \cdot C_{cm,1,pe,s,max} = 3 \cdot C_{cm,1,pe,max}/2$ which is larger than $C_{cm,1,pe,max}$ obtained for the circuits in Figs. 3.52(c) and 3.52(d). However, the higher capacitance value for the filter realization with three Y-capacitors $C_{cm,1,pe,s}$ maximally increases the achievable attenuation by only 2 dB, compared to the filter with only one capacitor $C_{cm,1,pe}$, and hence does not, in the opinion of the author, justify the higher part count.

from 1 nF to 25 nF. Moreover, for a heat sink connected to m (green solid lines in Fig. 3.53), the attenuation is not affected by C_{sc}. However, for a grounded heat sink, the attenuation is increased for higher values of C_{sc}, especially for low values of C_{g}: for $C_{\mathrm{g}} = 1$ nF the attenuation is increased by 9 dB if C_{sc} is increased from 10 pF to 490 pF. Because the CM inductor $L_{\mathrm{cm},1}$ cannot be bypassed [in contrast to Fig. 3.52(b)], a higher attenuation, compared to a connection of the heat sink to m, is achieved in this case. Thus, for the conventional CM filtering with $C_{\mathrm{cm},1,\mathrm{pe}}$ tied to PE, it is preferred to connect the heat sink to PE, especially for high values of C_{sc} and low values of C_{g}.

- *Bypassing CM capacitor $C_{cm,0,pe}$ between the bridge-leg input of the phases and PE, cf. Fig. 3.52(e)*: The higher the values of C_{g}, the lower the attenuation provided by this filter structure (dashed blue lines in Fig. 3.53): for $C_{\mathrm{sc}} = 267$ pF, the attenuation is reduced by 30 dB if C_{g} is increased from 1 nF to 25 nF. Additionally, the value of C_{sc} has almost no influence on the achievable attenuation, because $C_{\mathrm{cm},0,\mathrm{pe}} \gg C_{\mathrm{sc}}$.

Among all CM filtering approaches given in Fig. 3.52, the filter structure with an internal capacitor $C_{\mathrm{cm},1}$ [heat sink connected to the DC midpoint m, cf. Fig. 3.52(a)] and the one with a bypassing capacitor $C_{\mathrm{cm},0,\mathrm{pe}}$ [heat sink connected to PE, cf. Fig. 3.52(e)] are the CM filtering approaches achieving the highest CM attenuation for $C_{\mathrm{g}} \in [1\text{ nF}, 25\text{ nF}]$ and $C_{\mathrm{sc}} \in [10\text{ pF}, 490\text{ pF}]$ (cf. Fig. 3.53). Their attenuations of the CM noise are almost identical, which are at minimum, i.e. for $C_{\mathrm{g}} = 25$ nF and $C_{\mathrm{sc}} = 267$ pF, by roughly 12 dB higher than the attenuation obtained for the conventional CM filtering with a Y-capacitor $C_{\mathrm{cm},1,\mathrm{pe}}$ between y and PE (heat sink tied to ground).

Even tough the performance in terms of a high CM attenuation is for the filtering approaches with $C_{\mathrm{cm},1}$ [cf. Fig. 3.52(a)] and $C_{\mathrm{cm},0,\mathrm{pe}}$ [cf. Fig. 3.52(e)] almost identical, there is a significant difference in the resulting high-frequency potential fluctuations of the midpoint m of the DC link with respect to PE, as demonstrated in **Fig. 3.54**. The proposed filter structure with the internal capacitor $C_{\mathrm{cm},1}$ achieves an amplitude of the voltage $v_{\mathrm{cm,m,pe}}$ (cf. Fig. 3.52), which is by 26 dB–28 dB (factors in 20–25) lower than the voltage magnitude obtained by employing the bypassing capacitor $C_{\mathrm{cm},0,\mathrm{pe}}$ (solid red vs. dashed blue lines in Fig. 3.54). The voltages $v_{\mathrm{cm,m,pe}}$ are computed at the switching

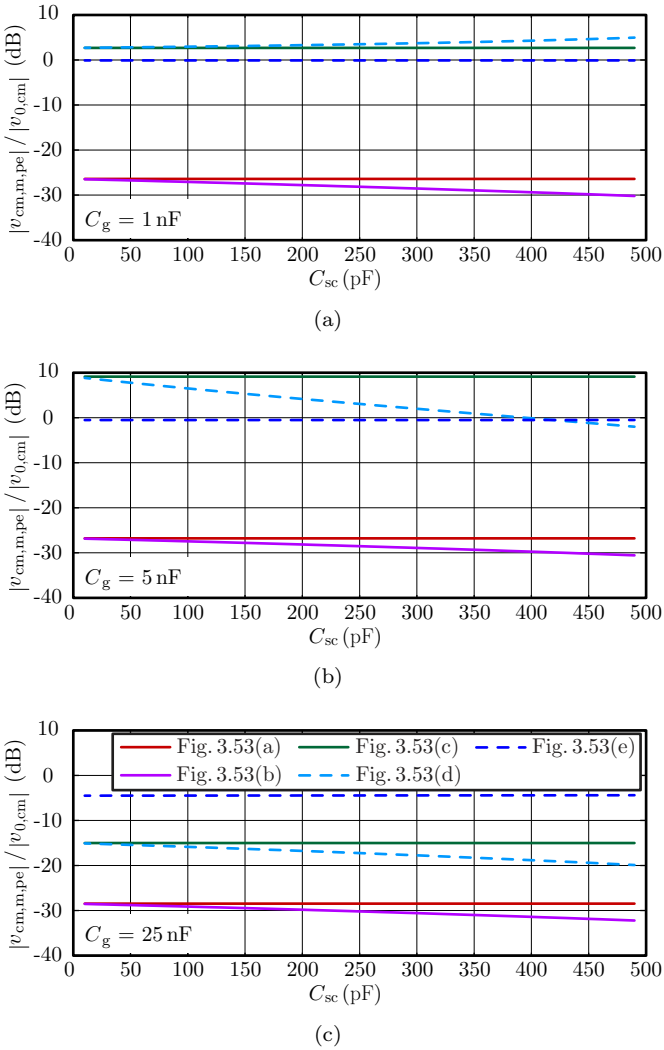


Figure 3.54: Voltage magnitudes $|v_{\mathrm{cm,m,pe}}|$ between the DC midpoint m and PE (i.e. across C_{g}) for the five CM filtering approaches shown in Fig. 3.52 and for **(a)** $C_{\mathrm{g}} = 1$ nF, **(b)** $C_{\mathrm{g}} = 5$ nF, and **(c)** $C_{\mathrm{g}} = 25$ nF. The voltages are calculated at $f_{\mathrm{s,in}} = 48$ kHz. *Circuit parameters (cf. Tab. 3.19)*: $L_{\mathrm{dm,1,tot}} = 169\,\mu\mathrm{H}$, $C_{\mathrm{dm,1}} = 850$ nF, $C_{\mathrm{d,1}} = 210$ nF, $R_{\mathrm{d,1}} = 66.1\,\Omega$, $L_{\mathrm{cm,1,tot}} = 2.9$ mH, $C_{\mathrm{cm,1}} = 100$ nF, $C_{\mathrm{cm,1,pe}} \rightarrow$ Eq. (3.97), $C_{\mathrm{cm,0,pe}} \rightarrow$ Eq. (3.98).

frequency $f_{\mathrm{s,in}} = 48$ kHz, because the major harmonic of $v_{0,\mathrm{cm,hf}}$ occurs at $f_{\mathrm{s,in}}$. For completeness, the voltage magnitudes $|v_{\mathrm{cm,m,pe}}|$ for the other three CM filtering approaches are given in Fig. 3.54.

Ideally, a steady DC midpoint potential, i.e. no high-frequency variations of $v_{\mathrm{cm,m,pe}}$, is of high interest because in this case the high-frequency current is kept away from the load and / or inverter system being supplied by the PWM rectifier. In conclusion, the internal connection of $C_{\mathrm{cm},1}$ between y and m (for a heat sink connected to m) confines the low-frequency as well as a main share of the high-frequency CM currents $i_{0,\mathrm{cm,lf}}$ and $i_{0,\mathrm{cm,hf}}$ to the converter system, which leads to the advantages pointed out above and thus clearly motivates this CM filter structure (cf. Fig. 3.49).

As the conventional CM filtering, where a Y-capacitor $C_{\mathrm{cm},1,\mathrm{pe}}$ is connected between y and ground (PE) [cf. Fig. 3.52(d)] is widely used in industry as well as academic research, the benefits of connecting $C_{\mathrm{cm},1}$ between the star-point y of the first DM filter stage and the DC output midpoint m [cf. Fig. 3.52(a)] should again be clearly pointed out as shown in **Fig. 3.55** for different values of $C_{\mathrm{cm},1}$ and C_{g} as well as for $C_{\mathrm{sc}} = 267$ pF. The findings are summarized below:

1. Higher attenuations at $f_{\mathrm{emi}} = 192$ kHz, i.e. at the first harmonic frequency within the range [150 kHz, 30 MHz] which is relevant for the EMI emissions measurement, for $C_{\mathrm{cm},1} \geq 1$ nF (which is valid for the case at hand, cf. Tab. 3.19) and $C_{\mathrm{g}} \leq 25$ nF [cf. **Fig. 3.55(a)**]. Thus, the second filter stage can be realized with smaller filter elements, potentially resulting in reduced volume, losses and values of parasitic elements of the components.

2. Higher reduction of the variations of the DC midpoint potential, i.e. lower voltage magnitudes $|v_{\mathrm{cm,m,pe}}|$, at the switching frequency is achieved for $C_{\mathrm{cm},1} \geq 10$ nF (which is valid for the case at hand, cf. Tab. 3.19) and $C_{\mathrm{g}} \leq 25$ nF [cf. **Fig. 3.55(b)**]. Therefore, a major part of the high-frequency current is kept away from the load and / or inverter system being supplied by the PWM rectifier.

3.5.2 Electrical Side Conditions for the Minimization of the Filter Volume

Before presenting the approach to find the minimal volume of the first EMI filter stage, the electrical side conditions, i.e. the voltages and

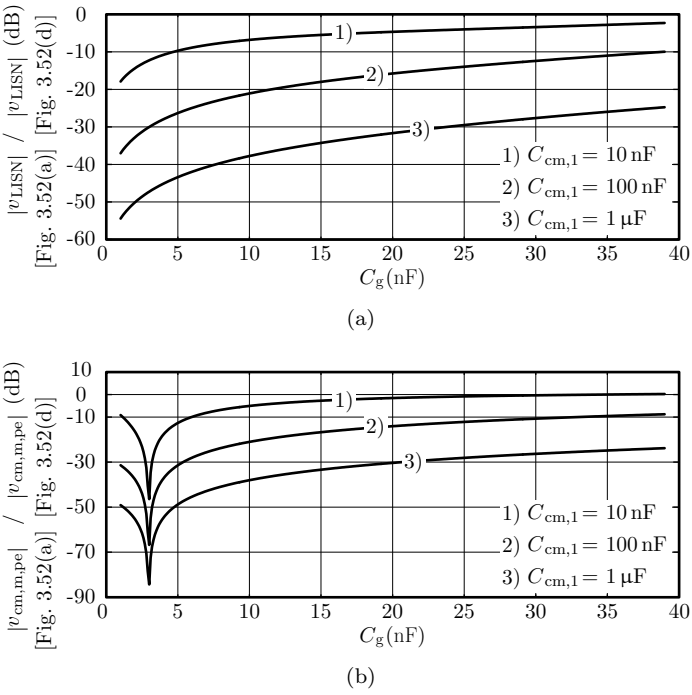


Figure 3.55: Comparison between the proposed filter structure of the first stage where $C_{\mathrm{cm},1}$ is connected between y and m [cf. Fig. 3.52(a)] and the conventional filter structure where a Y-capacitor $C_{\mathrm{cm},1,\mathrm{pe}}$ is connected between y and ground (PE) [cf. Fig. 3.52(d)] for different values of $C_{\mathrm{cm},1}$: **(a)** computed CM voltage magnitudes $|v_{\mathrm{LISN}}|$ at the LISN (LISN connected to the first filter stage) and at $f_{\mathrm{emi}} = 192$ kHz; and **(b)** computed magnitudes of the voltages $v_{\mathrm{cm,m,pe}}$ between the DC midpoint m and PE at the switching frequency $f_{\mathrm{s,in}} = 48$ kHz. *Circuit parameters (cf. Tab. 3.19)*: $L_{\mathrm{dm},1,\mathrm{tot}} = 169$ µH, $C_{\mathrm{dm},1} = 850$ nF, $C_{\mathrm{d},1} = 210$ nF, $R_{\mathrm{d},1} = 66.1\,\Omega$, $L_{\mathrm{cm},1,\mathrm{tot}} = 2.9$ mH, $C_{\mathrm{cm},1,\mathrm{pe}} \rightarrow$ Eq. (3.97), $C_{\mathrm{sc}} = 267$ pF.

currents at the interface of the first filter stage to the second stage and at the interface to the rectifier, are defined and motivated in this subsection. The side conditions are needed to guarantee, firstly, an electrically meaningful optimization result, and, secondly, to avoid that the first filter stage is optimized at the cost of the second stage. It is

the goal that with the subsequently derived side conditions, the second filter stage can be designed only knowing the CM and DM attenuations of the first filter stage but not the detailed structure / component values.

As explained in the introduction to this section, the certain maximum peak-to-peak bridge-leg input current ripple $\Delta i_{\mathrm{a0,pp,max}}$, depending on the DM inductance $L_{\mathrm{dm,1,tot}}$ and the CM inductance $L_{\mathrm{cm,1,tot}}$ [cf. Figs. 3.51 and 3.52(a)],[36] is usually limited to 20%–60% of $\sqrt{2} \cdot I_{\mathrm{in,n}}$. In this work, the limit is set initially to 25% (cf. **Tab. 3.17**).[37]

Moreover, the total EMI input filter (first + second filter stages) typically needs to provide roughly 80 dB–90 dB of DM as well as CM attenuations to comply with CISPR 11 (for the case at hand, and to be on the safe side, 90 dB are considered, cf. Section 3.5.6). Due to the approximately rectangular waveforms of the switched voltages, the envelopes of the spectra of conducted EMI noise are approximately proportional to $1/f$, cf. [291]. Within the frequency band specified in CISPR 11, $150\,\mathrm{kHz} < f < 30\,\mathrm{MHz}$, the greatest noise amplitudes are thus expected for the spectral EMI noise components at $4 \times 48\,\mathrm{kHz} = 192\,\mathrm{kHz}$. For the DM filtering, it is preferred to distribute the entire attenuation about equally to both filter stages, i.e. the first filter stage needs to provide 90 dB/2 = 45 dB of DM attenuation. The lower the cross-over frequency $f_{\mathrm{c,1}} = 1/(2 \cdot \pi \cdot \sqrt{L_{\mathrm{dm,1}} \cdot C_{\mathrm{cm,1}}})$ of the first filter stage, the higher the DM attenuation of this stage. Therefore, for a given $L_{\mathrm{dm,1}}$, a minimum capacitance of $C_{\mathrm{dm,1}}$ is required to achieve 45 dB of attenuation (at $f_{\mathrm{emi}} = 192\,\mathrm{kHz}$), which leads to a maximum peak-to-peak voltage ripple across $C_{\mathrm{dm,1}}$ (at $f_{\mathrm{s,in}} = 48\,\mathrm{kHz}$). Calculations for the case at hand showed that about 45 dB of DM attenuation are achieved if $\Delta v_{\mathrm{C,dm,1,pp,max}}$ (cf. Tab. 3.17) is limited to 6% of the nominal voltage (phase to neutral) fundamental amplitude $\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3}$.

For the CM filtering the same relation exists for $C_{\mathrm{cm,1}}$ in place of $C_{\mathrm{dm,1}}$: the higher the value of $C_{\mathrm{cm,1}}$ the larger the attenuation (for a fixed $L_{\mathrm{cm,1}}$). However, because of the limited value of the second filter stage's Y-capacitor $C_{\mathrm{cm,2}}$ connected to PE (cf. Sections 3.5.1 and 3.5.6),

[36] It is noted that the maximum peak-to-peak DM and CM current ripples $\Delta i_{\mathrm{a0,dm}}$ and $\Delta i_{\mathrm{0,cm}}$ (defined by $L_{\mathrm{dm,1,tot}}$ and / or $L_{\mathrm{cm,1,tot}}$) and / or the maximum voltage ripples $\Delta v_{\mathrm{C,dm,1}}$ across $C_{\mathrm{dm,1}}$ and $\Delta v_{\mathrm{C,cm,1}}$ across $C_{\mathrm{cm,1,eff}}$ do not occur at the same instants.

[37] Later on, to obtain a better magnetic material utilization, the permeability of the DM inductor's core material is allowed to be reduced to $40\% \times \mu_{\mathrm{i}}$ (where μ_{i} is the initial permeability at zero current), which would lead to a worst case peak-to-peak current ripple of $25\%/40\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 63\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} \approx 60\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 12.3\,\mathrm{A}$ (cf. Sections 3.5.4 and 3.5.5).

Table 3.17: Electrical specifications for the volume minimization of the first DM / CM *LC* stage of the EMI input filter. The assumed values are motivated in the text.
[1)] In a first step, $\Delta i_{\mathrm{a0,pp,max}}$ is limited to $25\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$. However, in the course of the optimization, a higher $\Delta i_{\mathrm{a0,pp,max}}$ of maximally $60\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 12.3$ A is allowed (cf. Section 3.5.4).

Max. peak-to-peak rectifier input phase current ripple $\Delta i_{\mathrm{a0,pp,max}} = 25\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ [1)]	5.1 A
Max. peak-to-peak DM voltage ripple across $C_{\mathrm{dm,1}}$ $\Delta v_{\mathrm{C,dm,1,pp,max}} = 6\% \times \sqrt{\frac{2}{3}} \cdot V_{\mathrm{mains}}$	19.5 V
Max. peak-to-peak CM voltage ripple across $C_{\mathrm{cm,1,eff}}$ $\Delta v_{\mathrm{C,cm,1,pp,max}} = 6\% \times \sqrt{\frac{2}{3}} \cdot V_{\mathrm{mains}}$	19.5 V
Max. capacitive reactive current amplitude $i_{\mathrm{C,dm,1,lf,max}} = 1\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$	0.21 A
Max. low-frequency $(3 \cdot f_{\mathrm{mains}})$ CM current amplitude $i_{\mathrm{cm,1,lf,max}} = 1\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$	0.21 A

an increased value of $C_{\mathrm{cm,1}}$ allows directly lowering the inductance value of the CM choke of the second filter stage (lower attenuation requirement), which potentially reduces the volume of the entire EMI filter. Accordingly, the CM attenuation provided by the first filter stage is increased to 60 dB (at $f_{\mathrm{emi}} = 192$ kHz), which is obtained if the maximum peak-to-peak voltage ripple $\Delta v_{\mathrm{C,cm,1,pp,max}}$ across $C_{\mathrm{cm,1}}$ (at $f_{\mathrm{s,in}} = 48$ kHz) is set to 6% of the nominal voltage (phase to neutral) fundamental amplitude $\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3}$.

Another issue to be considered is that, if the DM capacitance $C_{\mathrm{dm,1}}$ is increased, the capacitive reactive current drawn from the mains is increased as well. Thus, the maximum amplitude of the reactive current $i_{\mathrm{C,dm,1,lf,max}}$ is limited to 1% of the nominal fundamental current amplitude $\sqrt{2} \cdot I_{\mathrm{in,n}}$ (cf. Tab. 3.17). Therefore, it can be assumed that the additional ohmic losses in the mains and the EMI filter due to the capacitive reactive current are negligible, which also guarantees a higher efficiency of the PWM rectifier in the partial load range.

As previously explained, to benefit from a full utilization of the (linear) modulation range and to reduce the current ripple of the rectifier input phase currents, e.g. of i_{a0}, at the switching frequency, a carrier

based sinusoidal modulation with a superimposed zero-sequence component is employed [cf. (3.89)]. This results in a low-frequency CM voltage $v_{0,\mathrm{cm,lf}}$, with a dominant component at $3 \cdot f_{\mathrm{mains}}$, which drives a low-frequency CM current $i_{\mathrm{cm,1,lf}}$ that faces the same issue than the capacitive reactive current. Therefore, also the amplitude of the low-frequency CM current $i_{\mathrm{cm,1,lf,max}}$ (at $3 \cdot f_{\mathrm{mains}}$) is limited to 1% of the nominal fundamental current amplitude $\sqrt{2} \cdot I_{\mathrm{in,n}}$ (cf. Tab. 3.17).

Typically, damping elements, e.g. parallel $R_{\mathrm{d}}C_{\mathrm{d}}$ damping branches (cf. Fig. 3.50), are added to the EMI input filter to avoid a possible excitement of the filter's resonances [292]. However, for the optimization presented below, these damping elements are neglected because their volumes are small compared to the volumes of the other first filter stage components. The electrical side conditions, for which the minimal volume of the first EMI filter stage is computed in the following, are summarized in Tab. 3.17. The implication of changes in these boundary conditions (except for the maximum peak-to-peak current ripple) on the resulting minimum total boxed volume of the entire EMI filter (first + second filter stages) is analyzed in Section 3.5.6. It is anticipated that the minimum total volume could, in the best case, be reduced by only 3%, which shows a low sensitivity of the obtained results to the selected maximum values for the boundary conditions given in Tab. 3.17 (except for $\Delta i_{\mathrm{a0,pp,max}}$).

3.5.3 Volume Minimization Approach

As explained in the previous subsection, five electrical side conditions are to be considered when designing the first filter stage (cf. Tab. 3.17). Typically, the most compact filter realization results when all the side conditions are exactly met. However, in this case, because only four elements $L_{\mathrm{dm,1}}$, $L_{\mathrm{cm,1}}$, $C_{\mathrm{dm,1}}$, and $C_{\mathrm{cm,1}}$ need to be designed, the problem would be overdetermined. Thus, to minimize the filter volume, the two side conditions regarding the maximum capacitive reactive current amplitude and the maximum low-frequency CM current amplitude are set as an upper limit. Filter designs which exceed $i_{\mathrm{C,dm,1,lf,max}}$ and / or $i_{\mathrm{cm,1,lf,max}}$ are excluded from the optimization. The other side conditions are attempted to be fulfilled precisely.

The algorithm to find the filter design which results in the smallest boxed volume $V_{1,\mathrm{tot,min}}$ of the first filter stage is as follows:

1. Assumption of a certain total CM inductance $L_{\mathrm{cm,1,tot},i}$.

2. Computation of $L_{\mathrm{dm},1,\mathrm{tot},i}$ such that the maximum peak-to-peak phase current ripple $\Delta i_{\mathrm{a0,pp,max}}$ is met (cf. Tab. 3.17).

3. Calculation of the DM capacitance $C_{\mathrm{dm},1,i,\mathrm{ref}}$ and subsequently calculation of the CM capacitance $C_{\mathrm{cm},1,i,\mathrm{ref}}$ such that the maximum peak-to-peak voltage ripples given in Tab. 3.17 are not exceeded. Because only discrete capacitance values are commercially available, $C_{\mathrm{dm},1,i}$ and $C_{\mathrm{cm},1,i}$ are selected to fit $C_{\mathrm{dm},1,i,\mathrm{ref}}$ and $C_{\mathrm{cm},1,i,\mathrm{ref}}$ within a margin of $\pm 10\%$.

4. Computation of the required CM inductance value $L_{\mathrm{cm},1,i,\mathrm{ref}} = L_{\mathrm{cm},1,\mathrm{tot},i} - L_{\mathrm{dm},1,\mathrm{tot},i}/3$ and design of the CM choke (based on available cores) to obtain an inductance value $L_{\mathrm{cm},1,i}$ at the switching frequency which matches $L_{\mathrm{cm},1,i,\mathrm{ref}}$ with a deviation of $\pm 15\%$ (cf. Section 3.5.4).

5. Calculation of the required DM inductance $L_{\mathrm{dm},1,i,\mathrm{ref}} = L_{\mathrm{dm},1,\mathrm{tot},i} - L_{\sigma,1,i}$ where $L_{\sigma,1,i}$ is the leakage inductance of the CM choke. $L_{\mathrm{dm},1,i}$ at the switching frequency presents an accuracy of $\pm 5\%$ with respect to $L_{\mathrm{dm},1,i,\mathrm{ref}}$, since only available cores are employed for the DM inductor (cf. Section 3.5.4).

6. Iteration over all $L_{\mathrm{cm},1,\mathrm{tot},i}$ in steps of $L_{\mathrm{cm},1,\mathrm{tot,min}} \cdot 10^{\frac{i}{16}}$ with $L_{\mathrm{cm},1,\mathrm{tot,min}} = 100\,\mu\mathrm{H}$ and $5 \leq i \leq 36$, $i \in \mathbb{N}_0$ (geometric series with a constant relative increase between the values of 15%), which allow fulfilling the electrical side conditions given in Tab. 3.17.

Finally, from all made designs the one leading to the smallest boxed volume can be selected.

To realize $C_{\mathrm{dm},1}$ and $C_{\mathrm{cm},1}$, MKP X2 (305 V AC)[38] capacitors from TDK EPCOS are employed. Among all different combinations of paralleling capacitors of the same type to achieve the desired value $C_{\mathrm{dm},1,i,\mathrm{ref}}$ and $C_{\mathrm{cm},1,i,\mathrm{ref}}$, the one leading to the smallest volume is selected. The modeling of the DM and CM inductors is explained in more detail in the next subsection.

[38] Capacitance tolerance: M = ±20%, K = ±10% [293].

3.5.4 CM and DM Inductor Modeling

CM Inductor Modeling

For the design of the CM choke [cf. **Fig. 3.56(a)**], the available tape-wound toroidal cores with plastic casing from Vacuumschmelze GmbH (VAC) are considered [294]. The nanocrystalline core material can either be VITROPERM 250F or 500F.[39] These materials are selected for their high relative permeability ($5'000 \leq \mu_r \leq 100'000$), high saturation flux density ($B_{sat} \approx 1.2$ T) and reasonable losses [294].[40]

Generally, a valid CM inductor design needs to fulfill three conditions: first, it should provide the required inductance value $L_{cm,1,i,ref}$; second, the core should not saturate; and third, the inductor should not overheat. A CM choke design with Core_i from the list of the selected cores is valid if all three requirements are fulfilled. For the design of the CM choke with Core_i up to five stacked cores are considered.

The CM inductance $L_{cm,1}$ of a symmetrical three-phase CM choke is given by [295]

$$L_{cm,1} = L_{choke,1} \cdot \frac{1 + 2 \cdot k_{cm,1}}{3}, \tag{3.99}$$

where $k_{cm,1}$ denotes the coupling factor defined as

$$k_{cm,1} = \frac{L_{choke,1} - L_{\sigma,1}}{L_{choke,1}}; \tag{3.100}$$

$L_{choke,1}$ is the self-inductance of one phase winding and $L_{\sigma,1} = L_{choke,1} - M_{choke,1}$ is the leakage inductance of the CM inductor for one phase.[41] $M_{choke,1}$ is the mutual inductance between the windings on the CM choke core. The required CM inductance $L_{cm,1}$ is computed at the switching frequency and, thus, the frequency dependency of the core material's relative permeability is taken into account. Reference [295] derives an equation for $L_{\sigma,1}$ for a three-phase CM choke based on the work carried out in [296] for a single-phase CM choke. However, 3D Finite Element Method (FEM) simulations and measurements showed

[39] A_L-value tolerance: +45% / -25% [294].

[40] Nanocrystalline cores made of NANOPERM from Magnetec GmbH would be an alternative, which is, however, not further considered, since the core material specifications are very similar to the ones of VITROPERM.

[41] In this work, the term "leakage inductance" is employed for $L_{\sigma,1}$ to be consistent with the nomenclature in literature. However, in the opinion of the author, "effective DM phase inductance of the CM choke" would be a physically more clear naming.

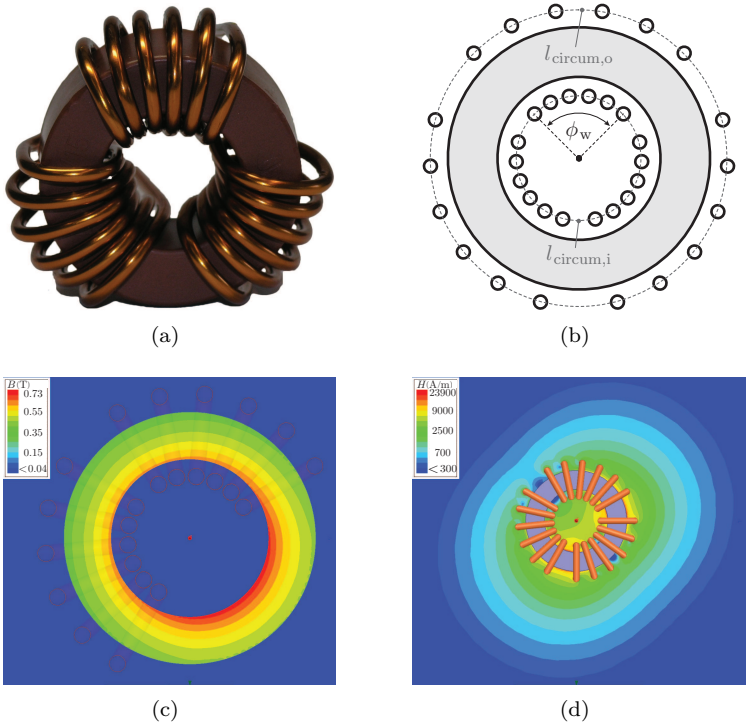


Figure 3.56: **(a)** Representative three-phase CM choke (T60006-L2040-W453, outer core diameter of 43.1 mm); **(b)** schematic cross section of the CM choke; **(c)** flux density distribution in the CM choke's core; and **(d)** magnetic field distribution around the CM choke as given in (a) for $i_{\mathrm{a}} = 26.6\ \mathrm{A} + 114\ \mathrm{mA}$ and $i_{\mathrm{b}} = i_{\mathrm{c}} = -13.3\ \mathrm{A} + 114\ \mathrm{mA}$ (currents as employed in the optimization, cf. Section 3.5.3). *Remark*: The maximum contribution of the DM currents (low- and high-frequency) to the maximum total core flux density of $B_{\mathrm{choke,1,max}} = 0.73\ \mathrm{T}$ is 0.07 T and thus less than 10% of $B_{\mathrm{choke,1,max}}$.

that the accuracy of the mentioned equation is not satisfactory for the considered CM choke cores. Thus, the leakage inductance for each core is computed with the help of Ansys Maxwell 3D simulations.

To achieve a high first self-resonance frequency of the CM choke,

only single-layer windings are taken into account. It is assumed that each winding spreads out equally over an angle of $\phi_\mathrm{w} = 90°$ [cf. **Fig. 3.56(b)**] to comply to international standards (e.g. EN 60950-1 [297]) pertaining minimum clearance and creepage distances between the windings of the CM choke. This is in good agreement with commercially available CM chokes from VAC, where the angle is typically $\phi_\mathrm{w} \approx 85°$–$95°$ for an outer diameter of the CM choke larger than 40 mm (which is the case for the obtained optimization results, cf. Section 3.5.5).

It is noted that a larger angle ϕ_w would improve the heat dissipation from the CM choke and it would facilitate the copper wire diameter selection. On the other hand, a smaller angle increases the leakage inductance of the CM choke, which is not desirable for a compact EMI filter realization, as further elaborated in Section 3.5.5.

The flux density in the core part covered by the windings [e.g. the winding of phase a, cf. Figs. 3.56(a) and **3.56(c)**] can be assessed by

$$\begin{aligned} B_{\mathrm{choke},1}(t) \quad = \quad & \tfrac{1}{N \cdot A_\mathrm{e}} \cdot \left[L_{\mathrm{cm},1,\mathrm{lf}} \cdot 3 \cdot i_{0,\mathrm{cm},\mathrm{lf}}(t) + \mathrm{VS}_{0,\mathrm{cm},1}(t) \right. \\ & \left. + L_{\sigma,1} \cdot \left(i_{\mathrm{a0,dm,lf}}(t) + i_{\mathrm{a0,dm,hf}}(t) \right) \right], \end{aligned} \tag{3.101}$$

where N is the number of turns of one phase, A_e denotes the magnetic effective core cross-section, $\mathrm{VS}_{0,\mathrm{cm},1}(t)$ are the high-frequency CM volt-seconds over one switching period and $L_{\mathrm{cm},1,\mathrm{lf}}$ is the low-frequency CM inductance which differs from $L_{\mathrm{cm},1,i}$ (designed at the switching frequency). A factor three is considered in front of $i_{0,\mathrm{cm},\mathrm{lf}}(t)$ since the CM current is referred to one phase [cf. definition in (3.90)]. The peak of the low- as well as high-frequency DM and CM currents and current ripples do not occur at the same instant and therefore the maximum of the flux density has to be assessed by considering the time behavior of the different quantities. To avoid saturation of the core the maximum flux density $B_{\mathrm{choke},1,\max} = \max\limits_{T_\mathrm{mains}} \left[B_{\mathrm{choke},1}(t) \right]$ should be below $0.7 \cdot 1.2\ \mathrm{T} = 0.84\ \mathrm{T}$ (where 1.2 T is B_sat of the material and the factor 0.7 provides a margin of 30%).

To compute the core losses P_fe, the flux density waveform is separated into a major loop (containing the frequency components at f_mains and $3 \cdot f_\mathrm{mains}$) and a minor loop (at $f_\mathrm{s,in}$) [298]. For both loops the improved Generalized Steinmetz Equation (iGSE) [195] is employed to compute the loop's associated core losses. To obtain the total core losses, the contributions of both loops are added; this is possible because $f_\mathrm{s,in}$ is by orders of magnitude higher than f_mains. The Stein-

metz parameters obtained from VAC resulting in typical core losses are employed and, according to the recommendation of VAC, the same Steinmetz parameters are used for the 250F and the 500F core material.

The winding losses P_{cu} are computed as presented in [298], summing up the loss contributions of the current harmonics over a mains period. For the computation of the high-frequency winding losses a separation into skin effect and proximity effect related losses is made. To calculate the proximity losses, the magnetic field H_{ext} through the turns of the windings is required. Based on the inspection of the magnetic field distribution computed with the help of 2D FEM simulations (with Femm 4.2 [299])[42] for different CM chokes, the following approach to assess the magnetic field H_{ext} is proposed.

At a certain harmonic frequency, the currents in the three phases a, b, and c are composed of either a differential or common mode component. For CM current harmonics $i_{0,\mathrm{cm,h}}$ the average magnetic field magnitude in the conductors (single-layer winding arrangement) can be approximated with the help of Ampère's Law by

$$\begin{aligned} H_{\mathrm{ext,i,avg}} &\approx \frac{3 \cdot N \cdot |i_{0,\mathrm{cm,h}}|/2}{l_{\mathrm{circum,i}} \cdot (\phi_{\mathrm{w}}/120°)}, \\ H_{\mathrm{ext,o,avg}} &\approx \frac{3 \cdot N \cdot |i_{0,\mathrm{cm,h}}|/2}{l_{\mathrm{circum,o}} \cdot (\phi_{\mathrm{w}}/120°)}, \end{aligned} \tag{3.102}$$

where $H_{\mathrm{ext,i,avg}}$ and $H_{\mathrm{ext,o,avg}}$ are the average magnetic field magnitudes on the inside and on the outside of the CM choke respectively; $l_{\mathrm{circum,i}}$ and $l_{\mathrm{circum,o}}$ are the mean inner and outer winding circumferences [cf. Fig. 3.56(b)]. Eq. (3.102) has been determined based on magnetic filed simulations carried out for different shapes of the toroidal cores and diverse single-layer winding arrangements, which lead to the adjustment term of $\phi_{\mathrm{w}}/120°$. The term $3 \cdot N \cdot \left|i_{0,\mathrm{cm,h}}\right|/2$ represents in a first approximation the total current orbited by a circle with $l_{\mathrm{circum,i}}$ or $l_{\mathrm{circum,o}}$. For DM current harmonics, e.g. $i_{\mathrm{a0,dm,h}}$, the average magnetic field in the conductors is computed with the 2D mirroring approach. This approach is for example explained in [193, 194]. In case of the CM choke, each conductor is mirrored once at the core part which is the closest to the conductor. Finally, the magnetic field in the conductors is computed by summing up the contributions of the actual and mirrored conductors.

Round Enameled Wire (EW) or Litz Wire (LW) are two common options to realize the windings. On the one hand, the high-frequency

[42] With the 2D FEM simulation the magnetic field distribution in the cross-section through the CM choke is computed [cf. Fig. 3.56(b)].

losses are more pronounced for EW than for LW, leading for the given specifications to predominantly proximity effect related losses that can be as high as 30%-35% of the total winding losses. On the other hand, LW can have a filling factor down to 50%, which would increase the low-frequency losses by a factor of two compared to EW (for the same outer diameter of the wire). Because the low-frequency losses are for the considered specifications typically higher than the high-frequency losses, it is preferred to realize the CM chokes with EW.

The winding losses computed with the proposed approach were compared to 2D FEM simulations and showed a maximum relative error of 7%. Overall, the relative error increases with a reduced number of turns per winding and a larger core diameter and thus for CM choke designs which are not optimal with respect to volume. However, for designs leading to a small boxed filter volume (cf. Section 3.5.5) the maximum relative error is reduced to 4%.

To avoid overheating of the choke, the maximum temperature of it $T_{\text{choke,max}}$ is limited to

$$T_{\text{choke,max}} = R_{\text{th}} \cdot (P_{\text{cu}} + P_{\text{fe}}) + 40\ ^{\circ}\text{C} = 120\ ^{\circ}\text{C}, \tag{3.103}$$

assuming an ambient temperature of 40 °C. On the one hand, CM inductor designs which exceed $T_{\text{choke,max}} = 120\ ^{\circ}\text{C}$ are discarded. On the other hand, if $T_{\text{choke,max}}$ is below 120 °C, to reduce the volume, the diameter of the enameled wire is reduced until approximately $T_{\text{choke,max}} \approx 120\ ^{\circ}\text{C}$ is reached. Inspired by [198], the thermal resistance R_{th} is roughly assessed by

$$R_{\text{th}} = \left(24 \cdot \left(V_{\text{eff}}[\text{cm}^3]\right)^{-0.49}\right) \frac{\text{K}}{\text{W}}, \tag{3.104}$$

where V_{eff} is the effective core volume. Eq. (3.104) results from a fit of the R_{th}'s provided by VAC in [300].

DM Inductor Modeling

As it can be seen from point 5) of the algorithm presented in Section 3.5.3, the DM inductance $L_{\text{dm},1,i,\text{ref}}$ depends on the leakage inductance of the CM choke. To find the global minimum of the boxed filter volume, a DM inductor is designed for each valid CM choke design with Core_i. Moreover, as indicated by (3.95), for a constant $L_{\text{dm,1,tot}}$, a higher leakage inductance $L_{\sigma,1}$ allows reducing $L_{\text{dm},1}$ and thus the volume of the DM inductor. However, in case the CM choke core saturates,

not only the CM inductance, but also the DM inductance provided by $L_{\sigma,1}$ drop to a few microhenries. Therefore, to limit the DM and CM current ripples under such circumstances and to provide a certain robustness, it is recommended to provide a minimum DM inductance, e.g. $L_{\mathrm{dm},1,\mathrm{min}} = 90\ \mu\mathrm{H}$ in the case at hand, by the DM inductor.

To realize the DM inductor, powder E-cores from Magnetics® based on the KoolMμ® core material,[43] listed in [302], are selected because of the soft-saturation characteristics of this core material and the absence of a concentrated air-gap (reduced stray field). The maximum allowed flux density in the DM inductor is set to $B_{\mathrm{coil},1,\mathrm{max}} = 1\ \mathrm{T}$ and the impact of the magnetic excitation on the relative permeability is accounted with the material type specific equations given in [302]. To obtain a better magnetic material utilization, the DM inductor is designed such that $L_{\mathrm{dm},1,i,\mathrm{ref}}$ (obtained at zero current, i.e. no excitation) achieves the desired maximum peak-to-peak rectifier input phase current ripple $\Delta i_{\mathrm{a0,pp,max}}$ of $25\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 5.1\ \mathrm{A}$ considering phase a (cf. Tab. 3.17). At the maximum fundamental mains phase current of $\sqrt{2} \cdot I_{\mathrm{max}} = 24.0\ \mathrm{A}$, the inductance is allowed to drop by 60%, i.e. achieves 40% of the value at zero current, which would lead to a worst case peak-to-peak current ripple of $25\%/40\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 63\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} \approx 60\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 51\% \times \sqrt{2} \cdot I_{\mathrm{max}} = 12.3\ \mathrm{A}$.[44] I_{max} is obtained for the nominal power $P_{\mathrm{in,n}} = 10\ \mathrm{kW}$, but for a mains voltage which is reduced by 14% compared to its nominal value, i.e. $(1 - 0.14) \cdot V_{\mathrm{mains}} = 344\ \mathrm{V}$ (cf. Tab. 3.16). However, because $\Delta i_{\mathrm{a0,pp,max}}$ does not occur at the maximum of the mains phase current fundamental (but 30 deg apart for the final realized filter design, cf. Fig. 3.65), the measured maximum peak-to-peak current ripple for nominal conditions is only 7.5 A (as demonstrated in Section 3.5.7), which represents an increase from 25% to 37% of $\sqrt{2} \cdot I_{\mathrm{in,n}}$.

To assess the core losses, the Steinmetz parameters are extracted from the equations given in [302] and the high-frequency winding losses are calculated as proposed in [298, 303]. Because of the low filling factors of litz wire mentioned in Section 3.5.4, round enameled wire is

[43] Composition: roughly 85% iron, 9% silicon, and 6% aluminum [301]; A_{L}-value tolerance: ±8% [302].

[44] It is noted that the nonlinear inductance results in a DM to CM noise conversion and vice versa. Furthermore, GeckoCIRCUITS [137] simulations revealed that the maximum total noise emissions of the converter system (with EMI filter) increased by approximately 7 dBμV due to the reduction of the DM inductance with the fundamental mains current instantaneous values.

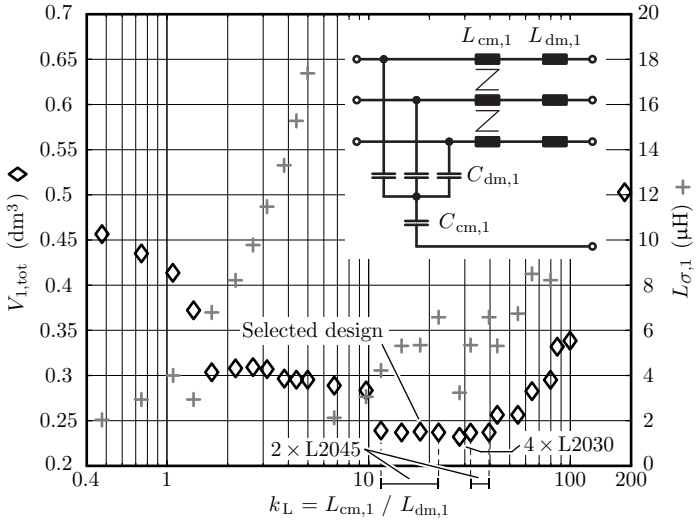


Figure 3.57: Total boxed volume $V_{1,\mathrm{tot}} = 3 \cdot V_{\mathrm{L,dm},1} + V_{\mathrm{L,cm},1} + 3 \cdot V_{\mathrm{C,dm},1} + V_{\mathrm{C,cm},1}$ of the first EMI filter stage (cf. Fig. 3.49) and leakage inductance $L_{\sigma,1}$ of the CM choke over the ratio k_{L} of CM inductance $L_{\mathrm{cm},1}$ to DM inductance $L_{\mathrm{dm},1}$ at the switching frequency [cf. (3.94)]. For $2 < k_{\mathrm{L}} < 5$, the CM choke's leakage inductance $L_\sigma \propto N^2$ is increasing for greater values of k_{L}, because the optimization always selects the same core to realize CM chokes with minimum possible volume, but increases the number of turns N to achieve higher CM inductance values.

employed to realize the winding of the DM inductors.[45] To assess the high-frequency losses due to the proximity effect, the computation of the average magnetic field for E-cores is based on the conductor mirroring approach as e.g. presented in [193]. This approach leads to a maximum relative error of 5.5% compared to 2D Femm simulations.

The maximum DM inductor temperature is assessed with the equa-

[45] The filling factor can be increased by employing a flat copper wire, i.e. a Helical Wound Technology (HWT, Schott Corp. [304]). However, this advantage is annulled by the higher high-frequency copper losses of such a winding for the investigated case.

tion given in [302]:

$$T_{\mathrm{coil,max}} = \left(\frac{(P_{\mathrm{cu}} + P_{\mathrm{fe}})\,[\mathrm{mW}]}{A_{\mathrm{coil}}[\mathrm{cm}^2]} \right)^{0.833} + 40\ ^{\circ}\mathrm{C}, \tag{3.105}$$

where A_{coil} is the open surface area of the inductor, i.e. the outer surface without the bottom surface. As for the CM chokes, designs which exceed $T_{\mathrm{coil,max}} = 120\ ^{\circ}\mathrm{C}$ are discarded. In case the temperature is below 120 °C, to reduce the volume, the diameter of the enameled wire is reduced until approximately $T_{\mathrm{coil,max}} \approx 120\ ^{\circ}\mathrm{C}$ is achieved.

3.5.5 Optimization Results

The results of the optimization are summarized in **Fig. 3.57**, where the total boxed filter volume $V_{1,\mathrm{tot}}$ of the first DM / CM LC filter stage is given as a function of k_{L} [cf. (3.94)]. **Tab. 3.18** repeats the electrical side conditions employed for the optimization as discussed in Section 3.5.2. It is revealed in Fig. 3.57 that for $10 < k_{\mathrm{L}} < 40$ a flat minimum of $V_{1,\mathrm{tot}}$ results: the absolute minimum occurs for $k_{\mathrm{L}} = 28$ and is 232 cm^3. This solution, however, requires four stacked cores and features only a slightly smaller filter volume (e.g. 237 cm^3 is achieved for $k_{\mathrm{L}} = 18$). The remaining results for $10 < k_{\mathrm{L}} < 40$ consider two stacked cores with same physical dimensions (T60006-L2045 by VAC) and different permeabilities (V101, V102, and V118 material specifications [294]). It is noted that some of the CM choke designs employ a reduced number of turns to achieve a reduced inductance, since the considered ring cores feature high permeabilities and cannot implement air-gaps, and, thus, do not fully exploit the available winding area (still, $V_{1,\mathrm{tot}}$ is close to the minimum, because the required $L_{\mathrm{dm},1}$, to achieve the same peak-to-peak current ripple for the reduced $L_{\mathrm{cm},1}$, is only increased marginally which leads to the same DM inductor design due to the accuracy of ±5% for $L_{\mathrm{dm},1}$, cf. Section 3.5.3).

It is remarked that for $L_{\mathrm{dm},1} = 382\ \mu\mathrm{H}$, $\Delta i_{\mathrm{a0,pp,max}} = 25\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ is achieved without the need of the CM choke $L_{\mathrm{cm},1}$, i.e. $L_{\mathrm{cm},1} = 0$ and accordingly $k_{\mathrm{L}} = 0$. In this case, the first filter would be realized without CM choke $L_{\mathrm{cm},1}$ achieving a calculated boxed volume of $V_{1,\mathrm{tot}} = 274$ cm^3.

For the realization, $k_{\mathrm{L}} = 18$ has been selected, which features a practically reasonable CM choke with two stacked cores (compared to four stacked cores for $k_{\mathrm{L}} = 28$) and achieves $V_{1,\mathrm{tot}} = 237$ cm^3. It

Table 3.18: Maximum allowed values of electric, magnetic, and thermal parameters employed for the minimization of the volume of the first EMI filter stage and parameter values obtained from the volume-optimized design (cf. Tab. 3.19). The parameters take a variation of the mains voltage according to Tab. 3.16 into consideration.

No.	*Parameter*
1(a)	Peak-to-peak bridge-leg input current ripple at zero current
1(b)	Peak-to-peak bridge-leg input current ripple due to no. 8
2	Peak-to-peak DM voltage ripple across $C_{\mathrm{dm},1}$
3	Peak-to-peak CM voltage ripple across $C_{\mathrm{cm},1}$
4	Amplitude of the low-frequency current through $C_{\mathrm{dm},1}$
5	Amplitude of the low-frequency current through $C_{\mathrm{cm},1}$
6	Peak flux density, CM choke
7	Peak flux density, DM inductor
8	Permeability reduction, DM inductor
9	Temperature of CM choke
10	Temperature of DM inductor
11	Angle ϕ_{w} which is covered by one CM choke's winding

is noted that the core material for this selection, i.e. property V118 (designs with $k_{\mathrm{L}} = 18, 22$), and the core material with property V101 (designs with $k_{\mathrm{L}} = 12, 15$) show a lower reduction of the permeability of the CM choke core at higher frequencies compared to the property V102 (designs with $k_{\mathrm{L}} = 32, 40$). This selected design of the first EMI filter stage is summarized in **Tab. 3.19**.

The optimization procedure minimizes the inductor volumes with respect to the specified thermal limitations, cf. Tab. 3.18, due to which the maximum inductor temperatures (118 °C and 119 °C) are very close to the limit of 120 °C (conditions 9 and 10 in Tab. 3.18). Moreover, the allowable reduction of the permeability of the DM inductor's core is fully utilized, which, for the given value of k_{L}, leads to a maximum relative peak-to-peak bridge-leg input current ripple of 49% instead of 25% (conditions 1(a) and 1(b) in Tab. 3.18). It is noted that the minimum allowed permeability ($40\% \times \mu_{\mathrm{i}}$; condition 8 in Tab. 3.18) together with the maximum peak-to-peak ripple specifications given in Tab. 3.18 define for each core shape and type of DM core material (e.g. KoolMμ® 60μ or 90μ) a maximum allowed magnetic field in the core which trans-

Table 3.18: Continued.
[1)]: $6\% \times (\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3})$ corresponds to $3\% \times V_{\mathrm{dc,n}}$; [2)]: μ_{i} = initial permeability, i.e. the permeability at zero current; [3)]: ambient temperature $T_{\mathrm{a}} = 40\ ^{\circ}\mathrm{C}$.

No.	*Boundary value*	*Selected design value*
1(a)	$25\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$	$25\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$
1(b)	max. $60\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$	$49\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$
2	$6\% \times (\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3})$ [1)]	$6\% \times (\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3})$ [1)]
3	$6\% \times (\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3})$ [1)]	$6\% \times (\sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3})$ [1)]
4	max. $1\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$	$0.6\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$
5	max. $1\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$	$0.03\% \times (\sqrt{2} \cdot I_{\mathrm{in,n}})$
6	max. $70\% \times 1.2$ T	$63\% \times 1.2$ T
7	max. 1 T	0.35 T
8	min. $40\% \times \mu_{\mathrm{i}}$ [2)]	$40\% \times \mu_{\mathrm{i}}$ [2)]
9	max. 120 °C [3)]	118 °C [3)]
10	max. 120 °C [3)]	119 °C [3)]
11	90 °	90 °

lates to a maximum flux density. For the selected DM coil, which employs the KoolMμ® 60μ material, this limits the maximum flux density to 0.35 T < 1 T (cf. condition 7 in Tab. 3.18). For the CM choke, the maximum flux density is close to the allowed maximum (condition 8 in Tab. 3.18). The optimized filter design considers capacitors, which fully utilize the maximum specified values of the high-frequency CM and DM voltage ripples and realize low-frequency capacitor currents that are well below the set limits, since, for selected CM and DM capacitances, the high-frequency and low-frequency conditions are coupled (conditions 2, 3 and 4, 5 in Tab. 3.18, respectively).

Fig. 3.58 depicts the volumes of the different filter components for the k_{L} values given in Fig. 3.57. According to this result, the capacitors have a minor contribution to the total filter volume and the volume of the DM inductor slightly decreases for increasing values of k_{L}. However, the characteristic of the volume of the CM inductor mainly affects the characteristic of $V_{\mathrm{1,tot}}$ and two ranges of k_{L} can be distinguished: $k_{\mathrm{L}} < 10$ and $k_{\mathrm{L}} > 40$. For $k_{\mathrm{L}} < 10$, low values of $L_{\mathrm{cm,1}}$ result and, due to the great A_{L}-values of the selected high permeability nanocrystalline cores,

Table 3.19: Optimized parameters of the first DM / CM *LC* EMI input filter stage (cf. Fig. 3.49) as well as CM and DM inductor data to obtain a practicably reasonable design with a small total boxed filter volume $V_{1,\mathrm{tot}}$ and a small CM choke's leakage inductance $L_{\sigma,1}$, i.e. $\leq 8\% \times L_{\mathrm{dm},1}$, of this stage (cf. Fig. 3.57). The subscript "ref" labels the reference values of the filter stage's inductors and capacitors, which the final values of the designed components need to match with the accuracy given in Section 3.5.3.

Circuit parameters	
$L_{\mathrm{dm},1}$ ($L_{\mathrm{dm},1,\mathrm{ref}}$)	163.5 µH (159.7 µH)
$L_{\mathrm{cm},1}$ ($L_{\mathrm{cm},1,\mathrm{ref}}$)	2.94 mH (2.73 mH)
$C_{\mathrm{dm},1,\mathrm{ref}}$ / $C_{\mathrm{cm},1,\mathrm{ref}}$	850 nF / 87 nF
$C_{\mathrm{dm},1}$ (B32923C3105K, EPCOS)	1.0 µF (nominal value)
$C_{\mathrm{cm},1}$ (B32921C3104M, EPCOS)	100 nF (nominal value)
CM choke – T60006-L2045-V118 (toroid, VITROPERM 500F – VAC)	
Number of turns / stacked cores	$N = 9$ / $n = 2$
Enameled wire	$\varnothing_{\mathrm{cu}} = 1.8$ mm
Leakage inductance	$L_{\sigma,1} = 5.3$ µH
Max. peak flux density	$B_{\mathrm{choke},1,\mathrm{max}} = 0.75$ T
Core / winding losses	$P_{\mathrm{fe}} = 5.6$ W / $P_{\mathrm{cu}} = 8.7$ W
Max. choke temperature	$T_{\mathrm{choke,max}} = 118$ °C
DM inductor – 00K3007E060 (E-core, KoolMµ® 60µ – Magnetics®)	
Number of turns / stacked cores	$N = 25$ / $n = 4$
Enameled wire	$\varnothing_{\mathrm{cu}} = 1.4$ mm
Max. peak flux density	$B_{\mathrm{coil},1,\mathrm{max}} = 0.35$ T
Core / winding losses	$P_{\mathrm{fe}} = 2.0$ W / $P_{\mathrm{cu}} = 10.9$ W
Max. coil temperature	$T_{\mathrm{coil,max}} = 120$ °C
Boxed volumina	
$V_{\mathrm{L,dm},1}$ / $V_{\mathrm{L,cm},1}$	35.6 cm^3 / 110.2 cm^3
$V_{\mathrm{C,dm},1}$ / $V_{\mathrm{C,cm},1}$	6.3 cm^3 / 1.4 cm^3

low numbers of turns. Accordingly, large cores are needed to avoid saturation. For $k_{\mathrm{L}} > 40$ large inductor cores are required to achieve

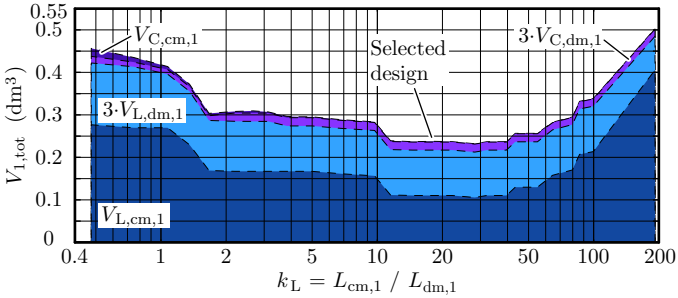


Figure 3.58: Total boxed volume $V_{1,\mathrm{tot}}$ of the first filter stage and its partitioning into the corresponding boxed volumes of the individual components over $k_{\mathrm{L}} = L_{\mathrm{cm,1}} \,/\, L_{\mathrm{dm,1}}$ [damping elements neglected, cf. Fig. 3.57].

high CM inductance values, e.g. $L_{\mathrm{cm,1}} = 15.0$ mH for $k_{\mathrm{L}} = 100$.

Furthermore, a small leakage inductance and / or magnetic stray field [which closes over air, cf. **Fig. 3.56(d)**] is of importance, as two additional points must be considered in a practical system:

1. the general impact of the CM choke's magnetic stray field on the surrounding (e.g. considering the parasitic coupling of the EMI filter components [305]); and

2. the impact of the filter enclosure and / or the magnetic shields between filter stages (cf. caption of Fig. 3.68) on the magnetic stray field of the CM choke for a compact design, especially at frequencies equal or higher than $f_{\mathrm{s,in}}$. In case of a metal enclosure and / or shields, eddy currents would reduce the CM choke's stray field, which would lead to a lower leakage inductance. This would result in a smaller total DM inductance $L_{\mathrm{dm,1,tot}}$ and accordingly in a higher peak-to-peak bridge-leg input current ripple.

Thus, the leakage inductance needs to be sufficiently small compared to $L_{\mathrm{dm,1}}$ and hence L_σ is limited to $\leq 8\% \times L_{\mathrm{dm,1}}$.[46] The leakage inductance for the selected filter design, $k_{\mathrm{L}} = 18$, is 5.3 µH and thus below $8\% \times L_{\mathrm{dm,1}} = 8\% \times 163$ µH $= 13.0$ µH.

It is observed that an alternative, more practical, approach to design the first filter stage would be the following [312]: for a given wire

[46] 8% corresponds to the A_{L}-value tolerance of the Kool Mµ core material [302].

diameter $d_{\mathrm{w},i}$ and CM choke core Core_i, the maximum number of turns N_i, that fit on the core, is calculated and, in case of core saturation, n_i cores are stacked to avoid saturation (up to five, otherwise the core is not considered). Therefore, a preliminary CM choke design, with N_i, n_i, and $d_{\mathrm{w},i}$, exists for each considered Core_i, for which the other filter component values are computed and the DM inductor can be designed. In a final step, simulated current and voltage waveforms are used to test the preliminary design against the boundary conditions of Tab. 3.18. The wire diameter $d_{\mathrm{w},i}$ can for example be selected such that the maximum current density in the wire is in 6.0 A/mm^2 ... 7.5 A/mm^2 (which corresponds to $d_{\mathrm{w}} = 1.7\,\mathrm{mm} \ldots 1.9\,\mathrm{mm}$). This approach leads to the same first filter stage designs with a small volume $V_{1,\mathrm{tot}}$ ($12 \leq k_{\mathrm{L}} \leq 40$) as identified with the proposed algorithm (cf. Section 3.5.3), since both methods target to maximally exploit the available winding area and the maximum allowed flux density in the core of the CM choke.

3.5.6 Design of the Second Filter Stage

As initially mentioned, a second stage of the EMI input filter is necessary to comply with CISPR 11, which is realized by a DM and a CM LCL stage (cf. Fig. 3.50). With GeckoCIRCUITS [137], the three rectifier input phase voltages are simulated and their CM and DM parts, i.e. $v_{0,\mathrm{cm}}$ and $v_{\mathrm{a0,dm}}$ (cf. Fig. 3.49), are computed. GeckoCIRCUITS provides an EMI evaluation block which computes the quasi-peak spectrum with which the noise level of the CM and DM voltages $v_{0,\mathrm{cm}}$ and $v_{\mathrm{a0,dm}}$ can be determined.[47] CISPR 11 specifies the maximum allowed noise emissions in the frequency range of [150 kHz, 30 MHz]. For the case at hand, the first switching frequency harmonic falling in the measurement range occurs at four times the switching frequency, i.e. at $f_{\mathrm{emi}} = 192$ kHz. The worst case noise source levels obtained from the simulation are: 144 dBµV for the conducted CM noise and 149 dBµV for the conducted DM noise (quasi-peak detection, cf. CISPR 16 [81]). The DM and CM worst case are obtained for the minimal mains voltage of $86\% \times 400\ \mathrm{V_{ll}} = 344\ \mathrm{V_{ll}}$ (rms) and the maximal mains voltage of $110\% \times 400\ \mathrm{V_{ll}} = 440\ \mathrm{V_{ll}}$ (rms), respectively (cf. Tab. 3.16). The limit given by CISPR 11, quasi-peak for Class A, is 79 dBµV [36] and hence the required attenuations which need to be provided by the EMI filter

[47] The GeckoCIRCUITS simulation has been conducted with the entire EMI filter connected to the LISN.

are

$$\begin{aligned} \mathrm{Att}_{\mathrm{dm,tot}} &= 149\ \mathrm{dB\mu V} - 79\ \mathrm{dB\mu V} + 15\ \mathrm{dB} = 85\ \mathrm{dB}. \\ \mathrm{Att}_{\mathrm{cm,tot}} &= 144\ \mathrm{dB\mu V} - 79\ \mathrm{dB\mu V} + 15\ \mathrm{dB} = 80\ \mathrm{dB}, \end{aligned} \tag{3.106}$$

In the above equations 15 dB are added which are composed by a safety margin of 6 dB (factor 2), a margin of 3 dB due to the nonlinear inductance values of the DM inductors with the current, and an additional margin of 6 dB because the CM and the DM noise (assuming to be of approximately equal magnitude) may constructively superimpose.

To obtain the required DM attenuation, an LC filter stage can be realized with lower volume than a pure L stage. However, because the mains inductance L_{mains} is not known exactly, the input impedance $\underline{Z}_{\mathrm{f,in}}$ of the filter is also changing with L_{mains} as shown in **Fig. 3.59**. More precisely, $\underline{Z}_{\mathrm{f,in}}$ is the impedance which is recognized at the bridge-leg inputs of the rectifier. If not designed carefully, it could happen that for a stiff mains ($L_{\mathrm{mains}} \approx 0$), a filter resonance of $\underline{Z}_{\mathrm{f,in}}$ is shifted to frequencies close to the switching frequency. Accordingly, the resonances of the filter could be excited for certain mains inductances resulting in undesired voltage and current oscillations. To guarantee that for practical mains inductances, and also for the worst case of $L_{\mathrm{mains}} = 0$, the filter resonances cannot be excited, and to avoid a large volume of the second filter stage, $L_{\mathrm{dm},2}$ and $L_{\mathrm{dm},3}$ are employed. This leads to a LCL structure of the 2$^{\mathrm{nd}}$ filter stage (cf. Fig. 3.50).

Referring to Section 3.5.2, RC damping branches are employed in parallel to the DM capacitors. To achieve a high power factor and to increase the efficiency of the converter in part load operation, the total capacitive reactive current (including the damping elements $C_{\mathrm{d},1}$ and $C_{\mathrm{d},2}$) is limited to $2\% \times \sqrt{2} \cdot I_{\mathrm{in,n}} = 0.41$ A[48] for the maximum mains voltage (cf. Tab. 3.16). With $a = C_{\mathrm{d},1}/C_{\mathrm{dm},1} = C_{\mathrm{d},2}/C_{\mathrm{dm},2} = 0.25$, it follows that $C_{\mathrm{dm},2} = 2.1\ \mu$F, $C_{\mathrm{d},1} = 212$ nF, and $C_{\mathrm{d},2} = 517$ nF. The optimal value of $R_{\mathrm{d},i,\mathrm{opt}}$, $i = 1, 2$ of the damping resistor $R_{\mathrm{d},i}$ for a given damping capacitance $C_{\mathrm{d},i}$ is calculated to result in the smallest resonance gain $A_{\mathrm{rr},i}$ of the filter input-to-output transfer function

[48] As for the first filter stage, the maximum reactive current drawn by the second stage is limited to $1\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ (cf. Table 3.17), i.e. which leads to an upper limit of the maximum allowed reactive current of $2\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ for the total EMI input filter.

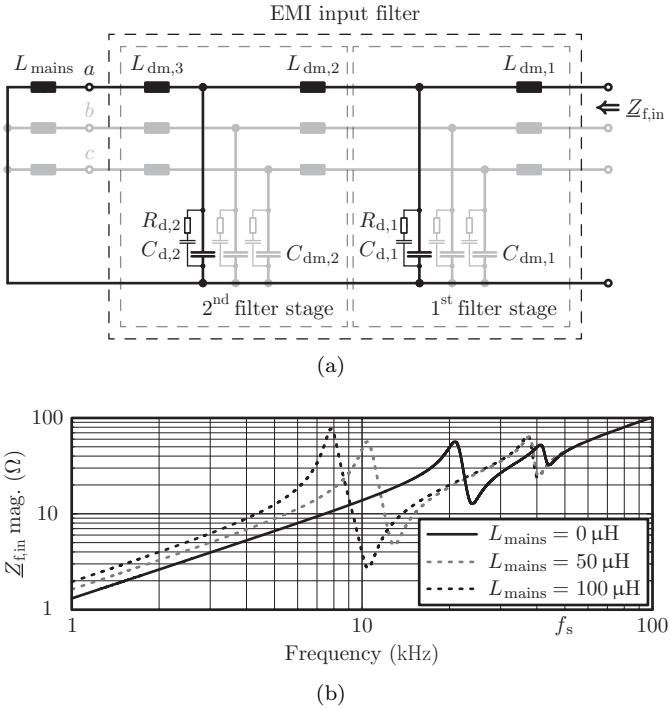


Figure 3.59: (a) DM equivalent circuit to illustrate the EMI input filter impedance $\underline{Z}_{\text{f,in}}$ seen from the rectifier switching stage AC side terminals and **(b)** magnitude of $\underline{Z}_{\text{f,in}}$ over the frequency for different mains inductance L_{mains}. The highest resonance frequency occurs for $L_{\text{mains}} = 0$.

(cf. Tab. 3.3). This leads to

$$R_{\text{d},i} = \sqrt{\frac{L_{\text{dm},i}}{C_{\text{dm},i}}} \cdot \frac{\sqrt{2 \cdot a^2 + 6 \cdot a + 4}}{2 \cdot a} \tag{3.107}$$

for a $A_{\text{rr},i}$ of 19 dB $\approx$ 20 dB and accordingly to $R_{\text{d,1}} = 66.1\,\Omega$ and $R_{\text{d,2}} = 17.8\,\Omega$.

The inductances of $L_{\text{dm,2}}$ and of $L_{\text{dm,3}}$ can then be determined such that the sum of $L_{\text{dm,2}} + L_{\text{dm,3}}$ is minimal (= smallest total volume with the assumption that the inductor volume is proportional to the

inductance) and that the highest EMI input filter resonant frequency is below 90% of the switching frequency (cf. Fig. 3.59) while still achieving enough DM attenuation $\mathrm{Att}_{\mathrm{dm,tot}}$ [cf. (3.106)]. This leads to $L_{\mathrm{dm,2,tot}} = 29\ \mu\mathrm{H}$ and $L_{\mathrm{dm,3,tot}} = 14\ \mu\mathrm{H}$. For the realization of these DM inductors the same core material as for $L_{\mathrm{dm,1}}$, i.e. KoolMμ® from Magnetics®, is employed (cf. Section 3.5.4).

Due to the limitation of the capacitance value of the CM Y-capacitor $C_{\mathrm{cm,2}} \leq 31$ nF (cf. Appendix D), and to achieve the required CM attenuation, an LCL stage can be realized with a smaller boxed volume than an LC (or L) CM filter stage. $C_{\mathrm{cm,2}}$ is connected to ground (PE), i.e. the local PE connection and / or ground wire which is also used for grounding the rectifier's enclosure, and not to the midpoint of the DC link m. This provides a converter confined path of return for high-frequency currents emitted through parasitic couplings (mainly capacitive) of filter elements to PE, which are not considered in the filter design. Because three-phase common mode chokes provide a source of parasitic coupling between the phases, it is preferred to realize $L_{\mathrm{cm,2}} = L_{\mathrm{dm,2}}/3$ by the DM inductors $L_{\mathrm{dm,2}}$, i.e. an explicit CM choke in series to $L_{\mathrm{dm,2}}$ is omitted. Because of the low value of $L_{\mathrm{cm,2}} = 29\ \mu\mathrm{H}/3 = 9.7\ \mu\mathrm{H}$, the resonance frequency of $C_{\mathrm{cm,2}}$ and $L_{\mathrm{cm,2}}$ would be 290 kHz for $C_{\mathrm{cm,2}} = 31$ nF, which is within the EMI relevant frequency range of [150 kHz, 30 MHz]. For this reason, an RC damping branch is additionally employed in parallel to $C_{\mathrm{cm,2}}$ (cf. Fig 3.50). This leads to $C_{\mathrm{cd,2}} = C_{\mathrm{cm,2}}/5 = 5$ nF, $C_{\mathrm{cm,2}} = 26$ nF, and $R_{\mathrm{cd,2}} = 199\ \Omega$, because $C_{\mathrm{cm,2}} + C_{\mathrm{cd,2}}$ is limited to 31 nF in order not to exceed the maximum touch current (cf. Appendix D). To reduce the inductance value of $L_{\mathrm{cm,3}}$ (and thus potentially also the component's volume), for a given filter cut-off frequency, the maximum capacitance value of $C_{\mathrm{cm,2}} + C_{\mathrm{cd,2}} = 31$ nF is employed. Typically the volume of $L_{\mathrm{cm,3}}$ is larger than the one of $C_{\mathrm{cm,2}}$.

To achieve the required total CM attenuation, a CM inductance of 0.8 mH is needed for $L_{\mathrm{cm,3}}$. In the calculation, a worst case parasitic capacitance of $C_{\mathrm{para}} = 50$ pF from the bridge-leg input to ground is assumed for each phase, assessed for the hardware setup explained in Section 3.5.7.As for $L_{\mathrm{cm,1}}$, $L_{\mathrm{cm,3}}$ is realized with nanocrystalline VITROPERM from VAC [294], which shows for most of the cores given in [294] an A_{L}-value which reduces by factors as the frequency increases and accordingly the inductance of $L_{\mathrm{cm,3}}$ is reduced at higher frequencies as well. This would lead to a reduced attenuation of the CM filter. To counteract this issue, a safety factor of 2.5 is introduced,

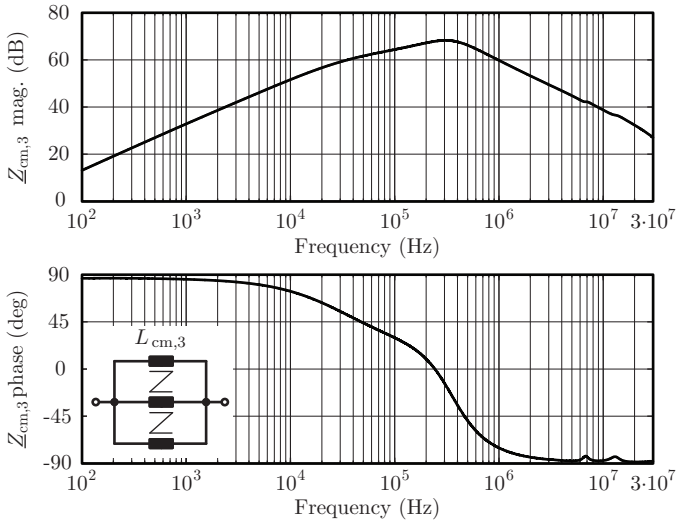


Figure 3.60: Measured impedance $\underline{Z}_{\mathrm{cm},3}$ of $L_{\mathrm{cm},3}$ for the realization as given in Tab. 3.20. The measurement was carried out with a Bode 100 network analyzer from Omicron Lab [203].

resulting in $L_{\mathrm{cm},3} = 2.5 \times 0.8\,\mathrm{mH} = 2.0\,\mathrm{mH}$. This factor can be justified by considering **Fig. 3.60**, where the measured impedance $\underline{Z}_{\mathrm{cm},3}$ of $L_{\mathrm{cm},3}$ as described in **Tab. 3.20** is depicted. From the measurement, the increasing damping with frequency of the employed VITROPERM material can clearly be seen for frequencies $\geq 10\,\mathrm{kHz}$. In a first approximation, the total CM impedance is effective for the filtering and hence an effective inductance $L_{\mathrm{cm},3,\mathrm{eff}}$ can be calculated which results in the same impedance magnitude $Z_{\mathrm{cm},3}$, i.e. $2 \cdot \pi \cdot f \cdot L_{\mathrm{cm},3,\mathrm{eff}} \approx Z_{\mathrm{cm},3}$. This effective inductance drops by a factor of 2.1 from the switching frequency to $f_{\mathrm{emi}} = 192\,\mathrm{kHz}$.[49]

Remark: The author is aware of that $C_{\mathrm{para}} = 50\,\mathrm{pF}$ represents a rather high parasitic capacitance value. However, in the course of the analysis, beforehand noise spectrum measurements and a comparison to the outcomes obtained from an accurate circuit simulation revealed

[49] It is not necessary to introduce a safety factor for $L_{\mathrm{cm},1}$ due to different material properties, i.e. the permeability of $L_{\mathrm{cm},1}$ reduces much less with frequency than it is the case for $L_{\mathrm{cm},3}$.

that these 50 pF led to a good agreement between experimental and simulative results. Unfortunately, C_{para} deteriorates the achievable CM attenuation in the same way than C_{sc} and hence the first CM filter stage achieves an attenuation of 50 dB instead of 60 dB [cf. Fig. 3.53(c)] as assumed ideally at the beginning of the filter design (cf. Section 3.5.2). Thus, the second CM stage of the EMI filter needs to achieve an attenuation of 30 dB instead of 20 dB.

Finally, with this CM filter design, the inductance values of the inductors of the second filter stage are obtained as $L_{\text{dm},2} = L_{\text{dm},2,\text{tot}} = 29\ \mu\text{H}$ (no CM choke in series to $L_{\text{dm},2}$) and $L_{\text{dm},3} = L_{\text{dm},3,\text{tot}} - L_{\sigma,3} = 14\ \mu\text{H} - 2.3\ \mu\text{H} = 11.7\ \mu\text{H}$.

Before the experimental results are presented in the next section, it is briefly analyzed to what extent the minimum total boxed volume $V_{\text{tot,min}}$ of the entire EMI filter varies, if, for the volume-optimization of the first filter stage, different sets of boundary conditions than the one given in Tab. 3.17 are assumed.

To start with, the maximum allowed bridge-leg input current ripple, e.g. $\Delta i_{\text{a0,pp,max}}$, is considered, which is specified at $25\% \times \sqrt{2} \cdot I_{\text{in,n}}$ for currents close to zero. Due to the reduction of the powder core's permeability of the DM inductors with the instantaneous phase current values, $\Delta i_{\text{a0,pp,max}}$ is limited to maximally $60\% \times \sqrt{2} \cdot I_{\text{in,n}}$, which is almost achieved for the selected filter design ($49\% \times \sqrt{2} \cdot I_{\text{in,n}}$, cf. Tab. 3.18). Potentially, a lower total filter volume could be achieved for a higher $\Delta i_{\text{a0,pp,max}}$, however, this is disregarded to avoid a performance degradation of the control of the input currents i_{a0}, i_{b0}, and i_{c0} in case of small time deviations from the ideal sampling instants. Thus, for the analysis presented below, the values of $L_{\text{dm},1}$ and $L_{\text{cm},1}$ are not varied and equal to the ones of the selected filter design (cf. Tab. 3.19).

In a next step, the partition of the total required DM attenuation $\text{Att}_{\text{dm,tot}}$ between the two filter stages is examined, which, initially, is distributed equally to the two stages, i.e. the first and the second stages achieve $\text{Att}_{\text{dm},1} = \text{Att}_{\text{dm,tot}}/2$ and $\text{Att}_{\text{dm},2} = \text{Att}_{\text{dm,tot}}/2$, respectively. A reduction of $\text{Att}_{\text{dm},1}$ is not further investigated, because it is typically preferred to have less attenuation of the filter stages from the converter towards the mains, considering the entire frequency range from 150 kHz to 30 MHz in which the compliance to CISPR 11 must be accomplished. In this case, from the rectifier towards the mains, physically smaller components can be used, which implicate lower parasitic component values and hence achieve higher attenuations at higher frequencies.

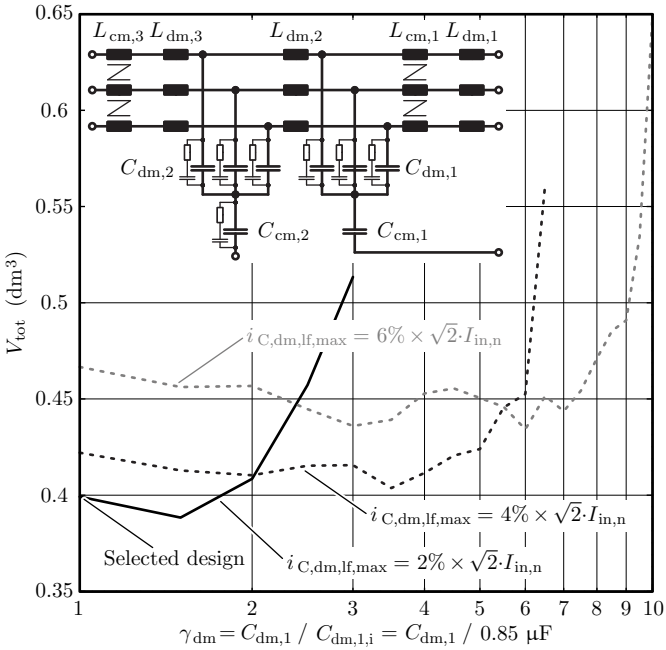


Figure 3.61: Total boxed volume V_{tot} of the entire EMI filter (first + second filter stages, cf. Fig. 3.50) over $\gamma_{dm} = C_{dm,1} / C_{dm,1,i}$, i.e. over increasing DM capacitance values $C_{dm,1}$ of the first stage compared to the selected design value $C_{dm,1,i} = 0.85$ µF (cf. Tab. 3.20). V_{tot} is computed for different maximally allowed capacitive reactive current amplitudes $i_{C,dm,lf,max} = i_{C,dm,1,lf,max} + i_{C,dm,2,lf,max}$ resulting from both filter stages (including the reactive current through the damping capacitors $C_{d,1}$ and $C_{d,2}$).

An increasing DM attenuation of the first filter stage is obtained by increasing the DM capacitance $C_{dm,1}$ ($L_{dm,1}$ is kept constant), which affects the total volume V_{tot} of the entire EMI filter (first + second stages) as shown in **Fig. 3.61** (solid black line for $i_{C,dm,lf,max} = 2\% \times \sqrt{2} \cdot I_{in,n}$).[50] In numbers, compared to the selected filter design with $\text{Att}_{dm,tot} = 85$ dB, $\text{Att}_{dm,1} = 45$ dB, and $\text{Att}_{dm,2} = 40$ dB for $V_{tot} =$

[50] The design of the second filter stage is for each $\gamma_{dm} = C_{dm,1}/0.85$ µF as explained above in this section.

400 cm^3 (cf. Tab. 3.20), an increase of $\mathrm{Att}_{\mathrm{dm},1}$ leads to:

$$\begin{aligned}\gamma_{\mathrm{dm}} = 1.5\text{:}\quad & \mathrm{Att}_{\mathrm{dm,tot}} = 88\ \mathrm{dB},\ \mathrm{Att}_{\mathrm{dm},1} = 50\ \mathrm{dB},\ \mathrm{Att}_{\mathrm{dm},2} = 38\ \mathrm{dB} \\ & \rightarrow V_{\mathrm{tot}} = 388\ \mathrm{cm}^3; \\ \gamma_{\mathrm{dm}} = 2.5\text{:}\quad & \mathrm{Att}_{\mathrm{dm,tot}} = 92\ \mathrm{dB},\ \mathrm{Att}_{\mathrm{dm},1} = 55\ \mathrm{dB},\ \mathrm{Att}_{\mathrm{dm},2} = 37\ \mathrm{dB} \\ & \rightarrow V_{\mathrm{tot}} = 457\ \mathrm{cm}^3. \end{aligned} \tag{3.108}$$

Accordingly, only a marginal reduction by 3% of the entire volume from 400 cm^3 to 388 cm^3 would be possible by increasing $\mathrm{Att}_{\mathrm{dm},1}$ by 5 dB (which could be considered in a second iteration of the filter design) and which justifies the selected initial partition of $\mathrm{Att}_{\mathrm{dm},2} \approx \mathrm{Att}_{\mathrm{dm},1} = \mathrm{Att}_{\mathrm{dm,tot}}/2$. In (3.108), the total attenuation $\mathrm{Att}_{\mathrm{dm,tot}}$ is increasing with increasing $\mathrm{Att}_{\mathrm{dm},1}$ because a higher value of $C_{\mathrm{dm},1}$ leads to a smaller capacitance $C_{\mathrm{dm},2}$ in order to not exceed the maximum allowed capacitive reactive current amplitude $i_{\mathrm{C,dm,lf,max}} = i_{\mathrm{C,dm,1,lf,max}} + i_{\mathrm{C,dm,2,lf,max}}$ resulting from both filter stages (including the reactive currents through the damping capacitors $C_{\mathrm{d},1}$ and $C_{\mathrm{d},2}$, cf. Fig. 3.51). Thus, higher inductance values of $L_{\mathrm{dm},2}$ and $L_{\mathrm{dm},3}$, than needed to achieve the minimum required total attenuation, are necessary to shift the DM resonance frequencies of the filter to frequencies less than $90\% \times f_{\mathrm{s,in}}$ (cf. design guidelines of the second stage on page 195).

As it can be seen from Fig. 3.61, no V_{tot} is calculated for $\gamma_{\mathrm{dm}} = C_{\mathrm{dm},1}/0.85\ \mu\mathrm{F} > 3$ and for $i_{\mathrm{C,dm,lf,max}} = 2\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$, because the total capacitive reactive current amplitude $i_{\mathrm{C,dm,lf}}$ of both filter stages would exceed the limit of $2\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ (i.e. the capacitive reactive current amplitude of the first stage is already larger than $2\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$). Thus, it could be that $i_{\mathrm{C,dm,lf,max}} = 2\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ is a too strict boundary condition and should be relaxed, i.e. a higher value of $i_{\mathrm{C,dm,lf,max}}$ should be allowed. However, Fig. 3.61 demonstrates that V_{tot} cannot be further reduced if $i_{\mathrm{C,dm,lf}}$ is increases, e.g. to $4\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ and $6\% \times \sqrt{2} \cdot I_{\mathrm{in,n}}$ (black and gray dotted curves). It is noted that, for the DM filter component values which form the basis of Fig. 3.61, the total CM attenuation provided by the EMI filter is changed by maximally 1 dB, i.e. the different realizations of the DM part of the filter influence the obtained CM attenuation, and accordingly the required CM component values, only marginally.

Finally, the boundary conditions related to the CM part of the EMI filter are considered. First, it is noted that due to the parasitic capacitance C_{para} from each bridge-leg input to ground (cf. explanation given on page 196), there exists an alternative path for the CM current by-

passing $L_{\mathrm{cm},1}$ (cf. Section 3.5.1). Due to this path, the achievable CM attenuation $\mathrm{Att}_{\mathrm{cm},1}$ of the first filter stage can only be increased with a high effort in terms of high capacitance values, i.e. $\mathrm{Att}_{\mathrm{cm},1}$ can only be increased by 4 dB if $C_{\mathrm{cm},1}$ is increased by a factor of 25 (for the same CM inductance $L_{\mathrm{cm},1,\mathrm{tot}}$). For this reason, the total volume V_{tot} of the entire EMI filter cannot be reduced for $\mathrm{Att}_{\mathrm{cm},1}$ higher than 50 dB. And second, it is remarked that the maximum value of the low-frequency $(3 \cdot f_{\mathrm{mains}})$ CM current amplitude $i_{\mathrm{cm},1,\mathrm{lf},\mathrm{max}}$ (cf. Section 3.5.2) is not reached during the process of optimization (cf. Section 3.5.3) and hence V_{tot} is not affected by allowing a higher value of $i_{\mathrm{cm},1,\mathrm{lf},\mathrm{max}}$.

Remark: It is observed that ideally, i.e. without the parasitic capacitance C_{para}, for an attenuation of the first filter stage of $\mathrm{Att}_{\mathrm{cm},1} = 78$ dB (for $C_{\mathrm{cm},1} = 1.5$ µF), $L_{\mathrm{cm},3}$ can be omitted and hence the boxed volume of the entire filter would be reduced to 380 cm^3, which is only 5% lower than 400 cm^3. However, such a filter design would not be practical because $\mathrm{Att}_{\mathrm{cm},1}$ would be reduced from 78 dB to 53 dB due to C_{para}.

In conclusion, the initially proposed partitioning of the DM and CM attenuations among the two filter stages is found to be an almost optimal choice and a very suitable starting point for a first design iteration.

3.5.7 Experimental Results

To validate the proposed filter design, the three-phase DM / CM $LCLCL$ EMI input filter PCB depicted in **Fig. 3.62** on top (the first filter stage is located to the front) was realized with the parameters summarized in Tab. 3.20, achieving a power density of 13.1 kW/dm^3. The realized filter achieves a boxed volume of 763 cm^3, which is more than one and a half times the sum of the boxed volumes of all components (483 cm^3).[51] This ratio of realized to calculated (summed-up) volumes is addressed to neglected parts of the filter, here the PCB, and unusable space (air), which appears due to different (incompatible) physical dimensions of the filter's components and typically requires most of the additional volume. The realized filter volume represents roughly 20% of the entire converter volume of 3.74 dm^3. It is recalled that the employed PWM rectifier is a three-phase three-level T-type VSC with Cree's C2M0025120D SiC

[51] 483 cm^3 is the measured boxed volume of all filter components, which differ from the calculated value of 400 cm^3, because each turn, with the wires of the selected wire diameters, requires a certain radius of curvature to be wound around the toroidal core for the CM choke or the middle leg of the E-core for the DM inductor.

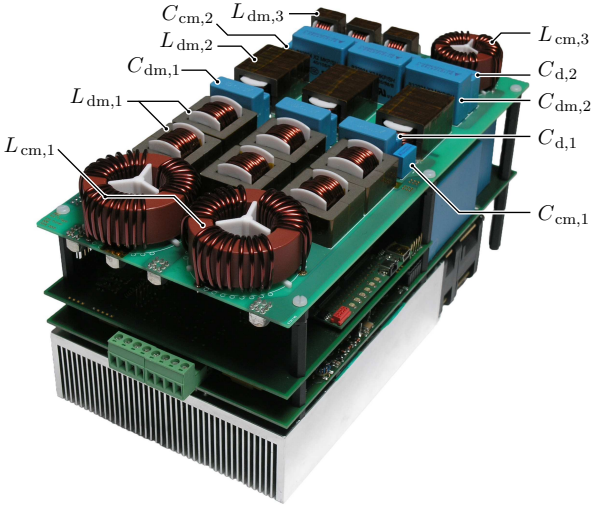


Figure 3.62: 10 kW three-phase PWM rectifier prototype, based on a three-level T-type VSC employing SiC MOSFETs (Cree's C2M0025120D), with a DM / CM *LCLCL* EMI input filter. The control of the rectifier (cf. Fig. 3.64) is implemented on a floating-point DSP TMS320F28335 and an FPGA LFXP2-5E-5TN144C. The specifications of the system are given in Tab. 3.16 and the parameters of the filter are summarized in Tab. 3.20. Converter dimensions: 240 mm × 130 mm × 120 mm (length × width × height).

MOSFETs (cf. Fig. 3.49). A nominal efficiency of 98.2% is achieved with this hardware setup.[52]

Hereafter, the correct operation of the PWM rectifier with sinusoidal input currents is demonstrated first, followed by the verification of the obtained optimization results (cf. Section 3.5.5). Finally, the entire filter design is validated by conducted EMI measurements.

PWM Rectifier Operation

Fig. 3.63 depicts the measured mains voltages and currents (cf. Fig. 3.49), at nominal operation for an input power of 10 kW (cf. Tab. 3.16). To achieve sinusoidal input currents which are in

[52] Measured with a Yokogawa WT3000 power analyzer and an error of ±0.07% [202].

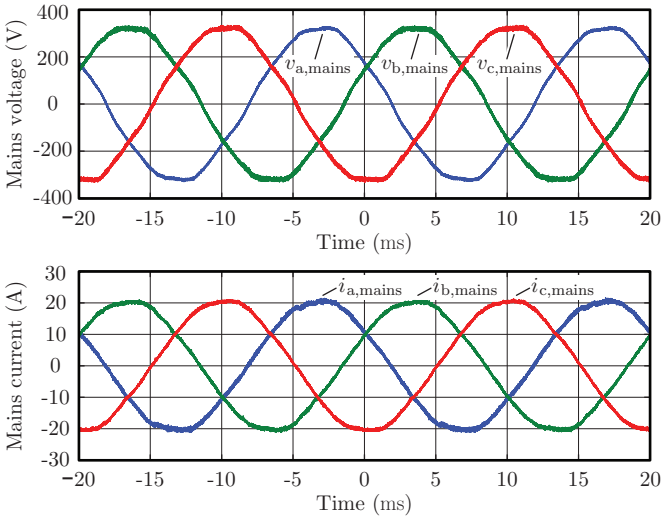


Figure 3.63: Measured mains voltages and mains currents (cf. Fig. 3.49), for an input power of 10 kW and for nominal operation as specified in Tab. 3.16. The measured voltages and currents are in phase due to the PFC control of the PWM rectifier as given in Fig. 3.64.

phase with the mains voltages (i.e. PFC) and a controlled DC link voltage, the phase-oriented control scheme given in **Fig. 3.64**, which does not require a Phase-Locked Loop (PLL) [306], was implemented on the hardware prototype due to its simplicity [307, 308]. The voltage proportional-integral (PI) controller is given by $G_{\mathrm{v}} = k_{\mathrm{pv}} \cdot (1 + s \cdot T_{\mathrm{iv}})/(s \cdot T_{\mathrm{iv}})$ with $k_{\mathrm{pv}} = 2$ mA/V^2 and $T_{\mathrm{iv}} = 20$ ms; and the current PI-controller is $G_{\mathrm{i}} = k_{\mathrm{pi}} \cdot (1 + s \cdot T_{\mathrm{ii}})/(s \cdot T_{\mathrm{ii}})$ with $k_{\mathrm{pi}} = 6.4$ V/A and $T_{\mathrm{ii}} = 336$ µs.

The low-pass filters shown in Fig. 3.64 are implemented as Finite Impulse Response (FIR) filters of type I and 3$^{\mathrm{rd}}$ order with a cut-off frequency of 1 kHz. Furthermore, the delay compensation is according to Section 3.3.2 employing a single inductance value of $L = L_{\mathrm{dm},1} + L_{\mathrm{dm},2} + L_{\mathrm{dm},3}$ (values at zero current).

According to Fig. 3.64, only two line-to-line mains voltages and two bridge-leg input currents are measured. The phase voltages required

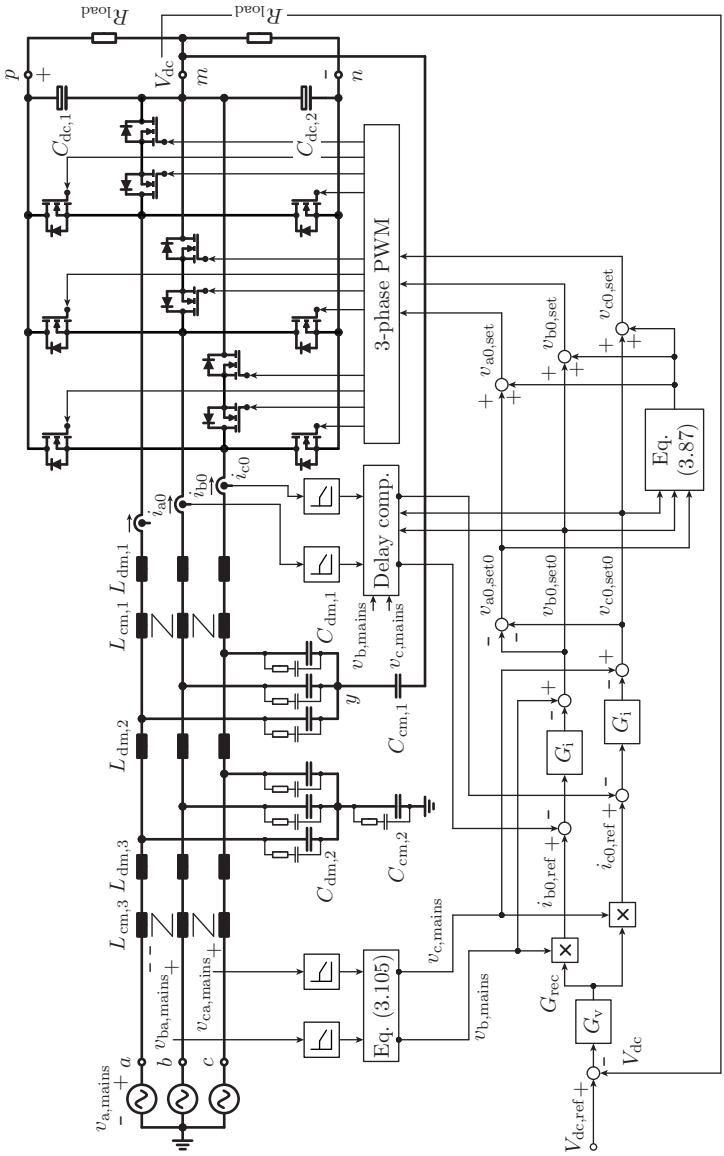


Figure 3.64: Phase-oriented control scheme implemented on the hardware prototype (cf. Fig. 3.62) to achieve sinusoidal input currents which are in phase with the mains voltages and a controlled DC link voltage V_{dc}.

for determining the phase current reference values are computed with

$$\begin{aligned} v_{\mathrm{b,mains}} &= \frac{2 \cdot v_{\mathrm{ba,mains}} - v_{\mathrm{ca,mains}}}{3}, \\ v_{\mathrm{c,mains}} &= \frac{2 \cdot v_{\mathrm{ca,mains}} - v_{\mathrm{ba,mains}}}{3}, \end{aligned} \tag{3.109}$$

where $v_{\mathrm{ba,mains}} = v_{\mathrm{b,mains}} - v_{\mathrm{a,mains}}$ and $v_{\mathrm{ca,mains}} = v_{\mathrm{c,mains}} - v_{\mathrm{a,mains}}$. In this way, any zero-sequence and / or CM part in the mains voltages is eliminated.

If for instance the DC link voltage needs to be increased, the PI DC link voltage controller G_{v} requires a higher rectifier conductance G_{rec}, which results in higher amplitudes of the bridge-leg input current references $i_{\mathrm{b0,ref}}$ and $i_{\mathrm{c0,ref}}$ according to

$$\begin{aligned} i_{\mathrm{b0,ref}} &= G_{\mathrm{rec}} \cdot v_{\mathrm{b,mains}}, \\ i_{\mathrm{c0,ref}} &= G_{\mathrm{rec}} \cdot v_{\mathrm{c,mains}} \end{aligned} \tag{3.110}$$

(cf. Fig. 3.64). Because the reactive capacitive currents of the DM EMI filter capacitors are kept below 2% of the amplitude of the nominal current (cf. Section 3.5.6), the mains phase currents and the bridge-leg input currents are almost equal, i.e. $i_{\mathrm{a0}} \approx i_{\mathrm{a,mains}}$ for phase a (neglecting the switching-frequency current ripple). With an accurate tracking of the current references with the PI current controllers G_{i}, the higher amplitudes of the bridge-leg input currents lead to a higher power flow into the DC link, which increases V_{dc}, since (3.110) ensures that the mains voltages and currents are in phase.

Remark: In Fig. 3.64, the actual and delay-compensated values of the bridge-leg input currents i_{b0} and i_{c0} are compared to the reference values $i_{\mathrm{b0,ref}}$ and $i_{\mathrm{c0,ref}}$ as given by (3.110). This is in contrast to the typical solution, where all three bridge-leg input currents are measured, the zero-sequence component due to the selected modulation with a superimposed zero-sequence voltage component [cf. (3.89)] is calculated, i.e. $i_{\mathrm{0,cm}} = (i_{\mathrm{a0}} + i_{\mathrm{b0}} + i_{\mathrm{c0}})/3$, and the pure DM currents $i_{\mathrm{b0}} - i_{\mathrm{0,cm}}$ and $i_{\mathrm{c0}} - i_{\mathrm{0,cm}}$ are then used for control. However, for the designed filter, $i_{\mathrm{0,cm}}$ is at maximum 57 mA (i.e. 0.03% of $\sqrt{2} \cdot I_{\mathrm{in,n}}$) and hence negligible, which leads to $i_{\mathrm{b0}} - i_{\mathrm{0,cm}} \approx i_{\mathrm{b0}}$ and $i_{\mathrm{c0}} - i_{\mathrm{0,cm}} \approx i_{\mathrm{c0}}$.

As stated above, mains voltages and currents shown in Fig. 3.63 are in phase, since the measured fundamental current-to-voltage displacement angle Φ is only 1.3 deg for phase a, 1.4 deg for phase b, and 1.5 deg for phase c. This results in a $\cos(\Phi) \approx 1$ for all phases. The $\mathrm{THD_i}$ of the mains currents is 2.4%, 2.1%, and 2.1% for phase a, b, and c, respectively, while the $\mathrm{THD_v}$ of the mains voltages is 2.4% for all phases. The

$\mathrm{THD_i}$ of the currents in phases b and c are lower than the $\mathrm{THD_v}$ of the voltages due to the low-pass filtering employed for the measurements of the voltages and currents on the hardware prototype (cf. Fig. 3.64). The measured $\mathrm{THD_i}$ of the currents are below the maximum value of 5% specified in IEEE 519 [309] for example. It is observed, that the current $\mathrm{THD_i}$ in the uncontrolled phase a is slightly higher than the one of the controlled phases b and c. Finally, the power factor [64]

$$\lambda = \frac{1}{\sqrt{1 + \mathrm{THD_i^2}}} \cdot \cos(\Phi) \tag{3.111}$$

is for each phase ≈ 1, as desired.

For nominal operation as given in Tab. 3.16, **Fig. 3.65** depicts the measured and simulated bridge-leg input current ripples of phase b over one mains period. The two ripples agree in their shape. Phase b has a lower measured inductance value of $L_{\mathrm{dm},1}$ than the other two phases (cf. Tab. 3.20), and thus a slightly higher current ripple for this phase results. For the measurement, the DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ were in average only deviating by 1 V from each other. The measured maximum peak-to-peak value $\Delta i_{\mathrm{b0,pp,max}}$ is 7.5 A (occurring at 30 deg and 210 deg assuming a cosine shape of the phase voltages) and hence agrees well with the simulated value of 7.6 A (deviation of 1.3%). The initial design guideline is to limit $\Delta i_{\mathrm{b0,pp,max}}$ to $\sqrt{2} \cdot I_{\mathrm{in,n}} = 5.1$ A. However, because of the reduction of the inductance values of the built coils with the instantaneous corresponding phase current values (powder cores are employed, cf. Section 3.5.4), the maximum $\Delta i_{\mathrm{b0,pp,max}}$ for nominal operation is increased to 37% of $\sqrt{2} \cdot I_{\mathrm{in,n}}$. The lower inductance values have also been considered in the simulation.

It is remarked that for the experimental results presented in this section, the DC link voltage controller of the control scheme depicted in Fig. 3.64 was not employed. Instead, the rectifier conductance G_{rec} has been set manually such that $V_{\mathrm{dc}} = 700$ V has been achieved. Nevertheless, after the measurement results presented in this section were recorded, the DC link voltage controller was successfully implemented on the hardware prototype to validate the proposed design.

Optimization Results Verification

To further verify the optimization results (cf. Section 3.5.5) the discrepancies between the modeling and the hardware realization are elabo-

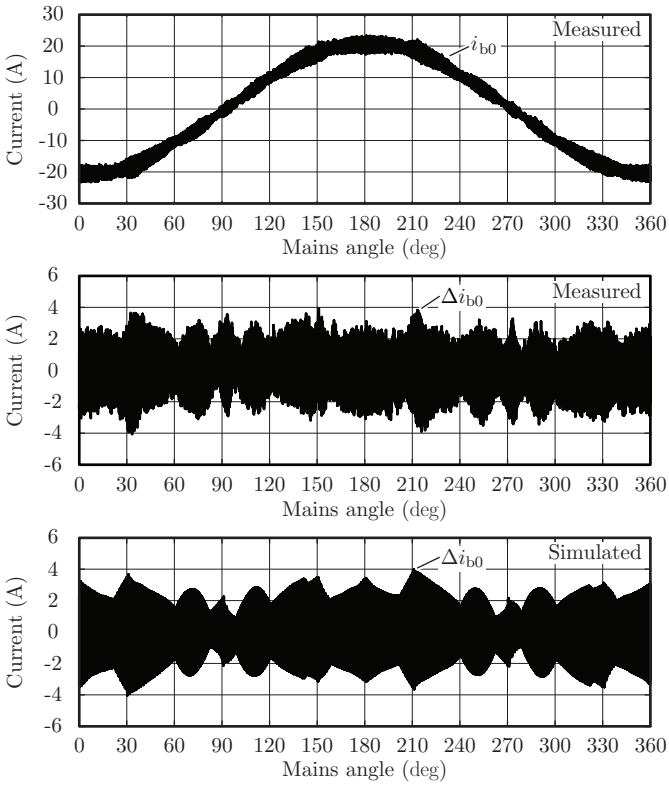


Figure 3.65: Measured bridge-leg input current $i_{b0}(t)$ of phase b over one mains period for nominal operation as specified in Tab. 3.16 (upper plot); current ripple $\Delta i_{b0}(t)$ reconstructed with the help of Fourier series from $i_{b0}(t)$ (middle plot) and comparison to the current ripple obtained from a Gecko-CIRCUITS simulation (lower plot).

rated next. From the measured filter component values listed in Tab. 3.20, it can be seen that the highest deviations from the design values are +40% and +38% and are obtained for $L_{cm,1}$ and $L_{cm,3}$, respectively. This is due to the magnetic value (A_L-value) tolerance of the VITROPERM VAC cores which can be as high as +45%. Thus, the measured $k_{L,meas}$ (based on the measured inductance values at 48 kHz) is 4.13 mH/160.0 µH ≈ 26, which is an increase of about 44% compared

Table 3.20: DM / CM *LCLCL* EMI input filter (cf. Fig. 3.50) design and its hardware realization (cf. Fig. 3.62) with the measured component values at 48 kHz (= switching frequency). The DM filter values of the phases show only very small differences.
[1)] Measured with the Agilent impedance analyzer 4294A (40 Hz–110 MHz) and without pre-magnetization for the inductors and DC voltage offset for the capacitors.

Comp.	*Design value*	*Measured value(s) at* 48 kHz[1)]
$L_{\mathrm{dm},1}$	163.5 µH	164.0 µH (ph. *a*), 157.5 µH (ph. *b*), 160.0 µH (ph. *c*)
$C_{\mathrm{dm},1}$	850 nF	992 nF (ph. *a*), 994 nF (ph. *b*), 989 nF (ph. *c*)
$L_{\mathrm{cm},1}$	2.94 mH	4.13 mH
$C_{\mathrm{cm},1}$	87 nF	87 nF
$C_{\mathrm{d},1}$	212 nF	219 nF (ph. *a*, *b*, *c*)
$R_{\mathrm{d},1}$	66.1 Ω	133 Ω || 133 Ω = 66.5 Ω (ph. *a*, *b*, *c*)
$L_{\mathrm{dm},2}$	29 µH	33.0 µH (ph. *a*), 33.5 µH (ph. *b*), 33.7 µH (ph. *c*)
$C_{\mathrm{dm},2}$	2.1 µF	2.19 µF (ph. *a*), 2.16 µF (ph. *b*), 2.17 µF (ph. *c*)
$C_{\mathrm{cm},2}$	26 nF	21.7 nF || 4.71 nF = 26.41 nF
$C_{\mathrm{d},2}$	517 nF	654 nF (ph. *a*, *b*, *c*)
$R_{\mathrm{d},2}$	17.8 Ω	35.7 Ω || 35.7 Ω = 17.9 Ω (ph. *a*, *b*, *c*)
$C_{\mathrm{cd},2}$	5 nF	4.71 nF
$R_{\mathrm{cd},2}$	199 Ω	390 Ω || 390 Ω = 195 Ω
$L_{\mathrm{dm},3}$	11.7 µH	11.5 µH (ph. *a*), 11.4 µH (ph. *b*), 11.3 µH (ph. *c*)
$L_{\mathrm{cm},3}$	2.0 mH	2.76 mH

to the selected value of $k_{\mathrm{L}} = 18$.

Moreover, the realized boxed volume of the first EMI filter stage is $3 \cdot 38.3\ \mathrm{cm}^3 + 123.2\ \mathrm{cm}^3 + 3 \cdot 6.3\ \mathrm{cm}^3 + 3 \cdot 2.4\ \mathrm{cm}^3 + 1.4\ \mathrm{cm}^3 = 265.6\ \mathrm{cm}^3$ (including the volumes of $C_{\mathrm{d},1}$; the volumes of $R_{\mathrm{d},1}$ are negligible), which is only 12% higher than the calculated volume of $3 \times 35.6\ \mathrm{cm}^3 + 110.2\ \mathrm{cm}^3 + 3 \times 6.3\ \mathrm{cm}^3 + 1.4\ \mathrm{cm}^3 = 237.3\ \mathrm{cm}^3$ (cf. Tab. 3.19). The main reason for the deviation in the volumes is that each turn, with the wires of the selected wire diameters, requires a certain radius of curvature to

Table 3.20: Continued.
[2)] To improve the high-frequency properties of the EMI filter, a 4.7 nF X1/250 V_{rms} AC ceramic capacitor from Johanson Dielectric Inc. (502S47W472KV3E-SC) is connected in parallel.

Comp.	*Hardware realization*
$L_{dm,1}$	cf. Tab. 3.19
$C_{dm,1}$	cf. Tab. 3.19[2)]
$L_{cm,1}$	cf. Tab. 3.19
$C_{cm,1}$	cf. Tab. 3.19[2)]
$C_{d,1}$	220 nF (rated value) X2 / 305 V_{rms} AC B32923C3224M (MKP, EPCOS)
$R_{d,1}$	2 × CRCW2512133RFKEGHP (in parallel) Thick film 2512 SMD 1.5 W resistor
$L_{dm,2}$	5 × 2 × 00K2510E060 (Kool Mμ 60μ Magnetics®) $N = 10$, $\varnothing_{cu} = 1.4$ mm
$C_{dm,2}$	2.2 μF (rated value) X2 / 305 V_{rms} AC B32924C3225K (MKP, EPCOS)[2)]
$C_{cm,2}$	22 nF (rated value) Y2 / 300 V_{rms} AC B32022B3223K (MKP, EPCOS) || 4.7 nF (rated value) Y2 / 250 V_{rms} AC 502S47W472KV3E-SC (X7R, Johanson Dielect.)
$C_{d,2}$	680 nF (rated value) X2 / 305 V_{rms} AC B32924C3684K (MKP, EPCOS)
$R_{d,2}$	2 × ERJ-1TNF35R7U (in parallel) Thick film 2512 SMD 1 W resistor
$C_{cd,2}$	4.7 nF (rated value) Y2 / 250 V_{rms} AC 502S47W472KV3E-SC (X7R, Johanson Dielect.)
$R_{cd,2}$	2 × 1206 SMD resistor (in parallel)
$L_{dm,3}$	2 × 2 × 00K1808E060 (Kool Mμ 60μ Magnetics®) $N = 11$, $\varnothing_{cu} = 1.4$ mm
$L_{cm,3}$	T60006-L2030-W514 (VITROPERM 500F, VAC) $N = 8$, $\varnothing_{cu} = 1.4$ mm, $L_{\sigma,3} = 2.3$ μH

be wound around the toroidal core for the CM choke or the middle leg of the E-core for the DM inductor.

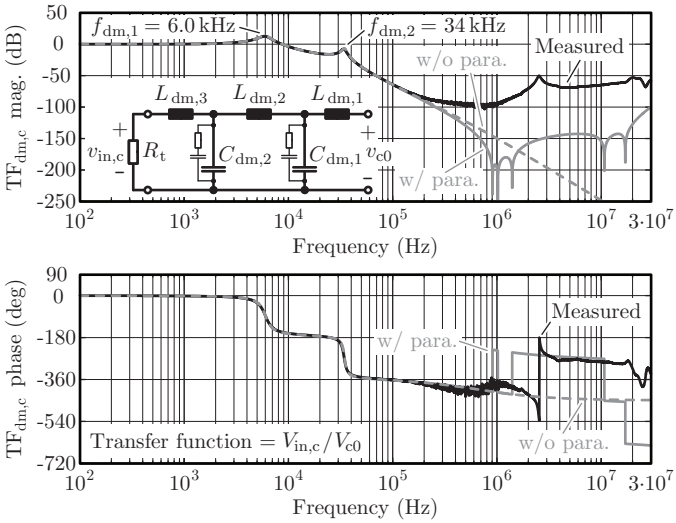
To roughly validate the thermal models of the CM choke and the DM inductor, i.e. (3.104) and (3.105), the maximum temperatures of

Table 3.21: Maximum measured CM choke and DM inductor temperatures (occurring at the winding surface) at an ambient temperature of $T_\mathrm{a} = 29\,^\circ\mathrm{C}$ for nominal operation as specified in Tab. 3.16. The relative error is defined as $(T_\mathrm{meas} - T_\mathrm{calc}) \,/\, (T_\mathrm{meas} - T_\mathrm{a})$. The temperatures were measured with a Fluke Ti9 thermal imager (emissivity of 0.95) and for the calculation the same ambient temperature of 29 °C is used instead of 40 °C, which is assumed for the optimization. It is noted that, after the optimization was conducted, $L_{\mathrm{dm},1}$ has been realized with two inductors that are located close to each other in order to improve the boxed volume of the filter.

Choke / inductor	*Max. measured temperature* T_{meas}	*Max. calculated temperature* T_{calc}	*Relative error*
$L_{\mathrm{cm},1}$	88.3 °C	75.5 °C	21.6%
$L_{\mathrm{cm},3}$	82.8 °C	82.8 °C	0%
$L_{\mathrm{dm},1}$	154.8 °C	116.2 °C	30.7%
$L_{\mathrm{dm},2}$	101.9 °C	95.3 °C	9.1%
$L_{\mathrm{dm},3}$	90.5 °C	87.3 °C	5.2%

all filter chokes and inductors are measured as presented in **Tab. 3.21** using the fully populated EMI filter PCB. The calculation always underestimates the measured temperatures and the simple temperature models achieve acceptable errors of less than 10% for the inductors of the second filter stage. However, the temperatures of the inductors of the first filter stage are underestimated by up to 30.7%, which can be explained by the close proximity of $L_{\mathrm{cm},1}$ and the two coils realizing $L_{\mathrm{dm},1}$ (cf. Fig. 3.62). The maximum measured temperature for $L_{\mathrm{dm},1}$ is obtained for the coil in the middle of the PCB, which is completely surrounded by other heated up components (cf. Fig. 3.62). Furthermore, due to the actual geometric properties, i.e. the surface part of the inductor touching the PCB and the part almost touching the other coil of $L_{\mathrm{dm},1}$ (cf. Fig. 3.62) are not included in the calculation of A_coil in (3.105); in contrast, in the course of the design, free space around the inductor was assumed.

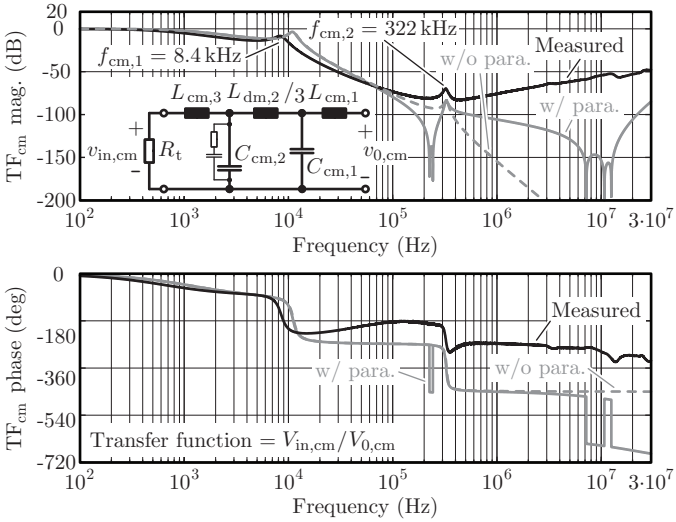
In this context, more detailed thermal models, e.g. as presented in [310], would feature improved accuracy, at the cost of a higher computational effort. Furthermore, the inductive components could be placed in an air stream to reduce their maximum surface temperatures. This, however, would require the use of an additional fan or a redesign of the



(a) DM transfer function

Figure 3.66: Measured (black line) and calculated (gray lines) $LCLCL$ EMI input filter transfer functions for **(a)** DM and **(b)** CM. The calculated transfer functions employ the measured values of the components as given in Tab. 3.20. For the dashed gray line ideal components are assumed, whereas for the solid gray line the parasitic capacitances and inductances of the inductors and capacitors (determined by separate measurements) are included. The two lower resonance frequencies of the measured transfer function for DM (a) and CM (b) result from an interaction of both filter stages. $f_{\mathrm{cm},1}$ and $f_{\mathrm{cm},2}$ in (b) can be approximated by $f_{\mathrm{cm},1} \approx 1/(2 \cdot \pi \cdot \sqrt{L_{\mathrm{cm},1} \cdot C_{\mathrm{cm},1}}) = 8.1$ kHz and $f_{\mathrm{cm},2} \approx 1/(2 \cdot \pi \cdot \sqrt{L_{\mathrm{cm},1} \cdot C_{\mathrm{cm},1}}) = 292$ kHz (measured inductance and capacitance values acc. Tab. 3.20), because $f_{\mathrm{cm},2} \gg f_{\mathrm{cm},1}$. The measurements were conducted with a Bode 100 network analyzer (Omicron Lab, [68]) for which the noise floor of the measurement device is reached at -100 dB.

converter to take advantage of the air streams generated by the existing cooling system, since the actual arrangement of the filter board is on top of the converter (cf. Fig. 3.62).



(b) CM transfer function

Fig. 3.66: Continued.

Conducted EMI Measurements

Before the EMI measurements are discussed for nominal operation, the measured DM and CM filter transfer functions, i.e. $\mathrm{TF}_{\mathrm{dm,c}} = v_{\mathrm{in,c}}/v_{\mathrm{c0}}$ (measured for phase c) and $\mathrm{TF}_{\mathrm{cm}} = v_{\mathrm{in,cm}}/v_{\mathrm{cm0}}$, are given in **Fig. 3.66** to verify that the filter provides the required attenuations.[53] For $\mathrm{TF}_{\mathrm{dm,c}}$ the CM chokes $L_{\mathrm{cm,1}}$ and $L_{\mathrm{cm,3}}$ were shorted and for $\mathrm{TF}_{\mathrm{cm}}$ the midpoint of the DC link m and PE were connected together (common measurement ground). Both transfer functions have been measured with a $R_{\mathrm{t}} = 50\,\Omega$ termination. The calculated $\mathrm{TF}_{\mathrm{dm,c}}$ fits nicely with the measured one up to a frequency of 160 kHz. At $f_{\mathrm{emi}} = 192$ kHz (first harmonic located in the EMI measurement range) the achieved attenuation is 84.3 dB, which agrees well with the desired value of 85 dB [cf. (3.106)] and differs only by 3.5 dB from the calculated attenuation of 87.8 dB.

[53] Measurements conducted with a Bode 100 network analyzer from Omicron Lab [203].

Because of the large A_L-value tolerances of up to +45%, the increasing loss component (associated with the imaginary part of the permeability) with frequency (cf. Fig. 3.60), and the frequency dependency of the permeability of the VITROPERM core material for the CM chokes $L_{cm,1}$ and $L_{cm,3}$, the measured and calculated TF_{cm} do not agree so well as for $TF_{dm,c}$ for frequencies below 100 kHz. At frequencies greater than 100 kHz, the parasitic couplings between the filter stages due to the geometrical arrangement of the components on the PCB cause additional differences between the measured and calculated value of $|TF_{cm}|$. Nevertheless, the achieved attenuation at $f_{emi} = 192$ kHz is 80.8 dB and therefore in good agreement with the desired attenuation of 80 dB [cf. (3.106)]. The calculated attenuation is 9.0 dB higher than the measured one.

The hardware setup to measure the conducted noise emissions of the PWM rectifier system is depicted in **Fig. 3.67**. The attenuations of 10 dB of the LISNs (for increased accuracy) and of 10 dB of the impulse limiter (used to protect the test receiver) are compensated by the −20 dB of the EMI test receiver. For the measurement of the total emission the DM / CM noise separator is omitted. The additional CM attenuation of 6 dB of the three-phase noise separator is counterbalanced by adding 6 dB to the measurement results a posteriori. Thus, in **Fig. 3.68(c)** the actually generated noise level is given.

To be able to separate the DM and CM noise, a three-phase noise separator [276] (which adds 6 dB of CM attenuation) and three LISNs (ENV216 from Rohde&Schwarz) are employed. Because the measured parasitic capacitance between the DC link midpoint m and PE is $C_{g,m} = 2.9$ nF, an explicit external Y2-capacitor with $C_{g,a} = 22$ nF (300 V_{rms} AC from EPCOS) was additionally connected between m and PE to obtain $C_g \approx 25$ nF (cf. Fig. 3.67), which was determined to be the worst case in Section 3.5.1 and hence considered in the course of the EMI filter design. The load resistance is $R_{load} = 24.5\,\Omega$ for each DC link capacitor.

The modulation of the PWM rectifier system has a major impact on the harmonic spectrum of the bridge-leg input voltages and thus it is quickly repeated here before the conducted noise measurement results are discussed. Two synchronized triangular carriers, which are in phase, are employed, one for positive and the other one for negative modulation indices. The reference is sampled at the beginning of every half pulse period (double-update-mode, cf. Fig. 2.4).

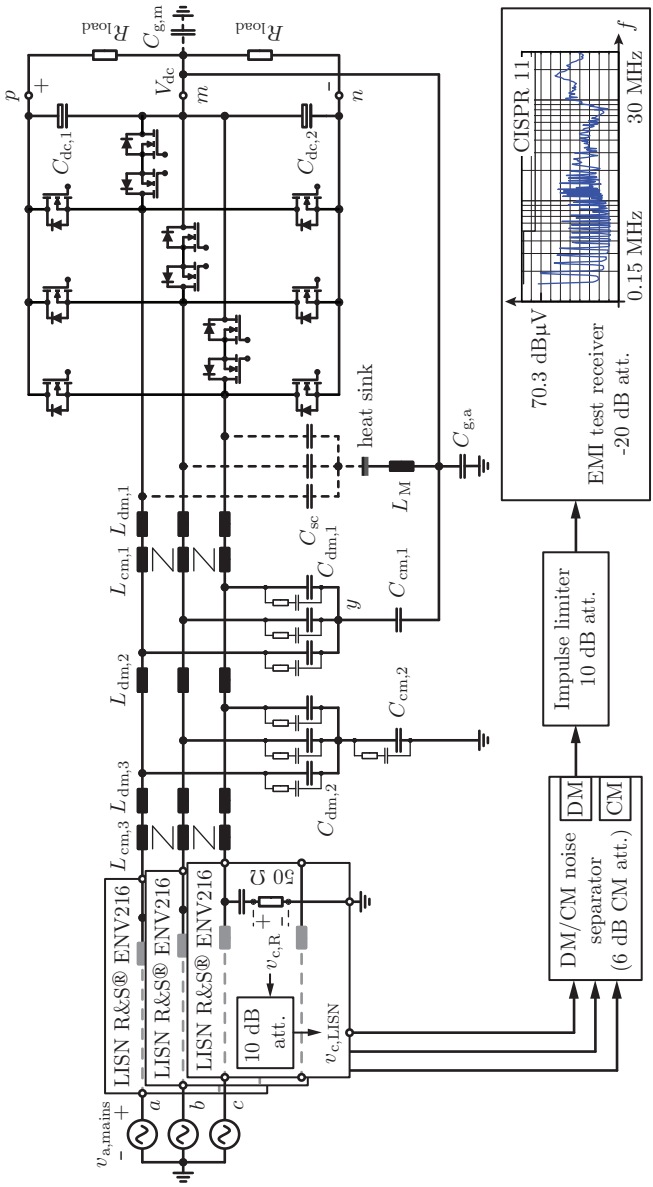
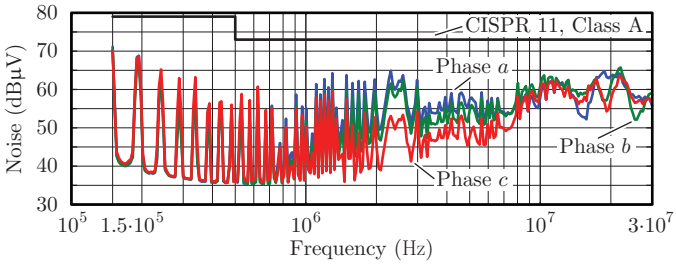


Figure 3.67: Conducted EMI hardware setup to measure the total (DM + CM), DM, and CM noise emissions.



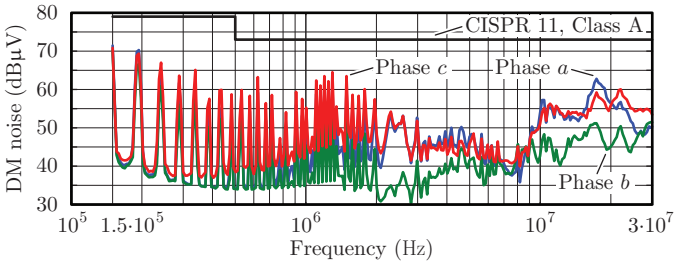
(a) DM + CM

Figure 3.68: Measured **(a)** total (DM + CM), **(b)** DM, and **(c)** CM noise spectra of the three-phase three-level PWM rectifier system with the designed DM / CM $LCLCL$ EMI input filter (cf. Fig. 3.62) employing the experimental setup depicted in Fig. 3.67. 50 μm thick μ-metal shields (VAC) were placed between the filter stages (transversely to the power flow direction) to avoid magnetic couplings between them. Meaningful measurement results are obtained from the DM / CM noise separator because the difference between DM and CM noise is less than 40 dB [187].

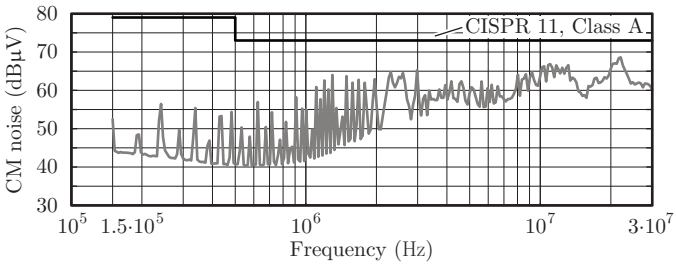
The measured conducted total (DM + CM), DM, and CM emissions are presented in **Fig. 3.68** and are obtained with a quasi-peak detector according to CISPR 16 [81] of the EMI test receiver.[54] The targeted limit, i.e. 79 dBμV in [150 kHz, 500 kHz] and 73 dBμV in [0.5 MHz, 30 MHz] as defined in CISPR 11, Class A [36], can be fulfilled for all phases as demonstrated by the measured total emissions in **Fig. 3.68(a)**. The choke L_{M} (T60006-L2012-W498 from VAC, outer core diameter of 14.3 mm, 2 turns) had to be connected between the heat sink and the DC link midpoint m (cf. Fig. 3.67) to attenuate the otherwise resulting emission peak of 73.7 dBμV at 5.5 MHz, which would be slightly higher than the allowed limit of 73 dBμV. It is emphasized that L_{M} leaves the emissions below 500 kHz unaffected, because $1/(2 \cdot \pi \cdot 500\ \mathrm{kHz} \cdot 3 \cdot C_{\mathrm{sc}}) = 396\ \Omega$ is still significantly larger than 74.3 Ω, the measured impedance of L_{M} at 500 kHz.

Furthermore, it is recognized that the emissions of the phases are slightly different from each other and that actually the maximum emission is obtained for 150 kHz (71.2 dBμV), which is however only 2.4 dB

[54] Rohde & Schwarz ESPI, 9 kHz ... 3 GHz.



(b) DM



(c) CM

Fig. 3.68: Continued.

higher than the emission at 192 kHz (68.8 dBµV). This observation can be explained by considering the harmonic spectrum of the bridge-leg input voltages v_{a0}, v_{b0}, and v_{c0}: the frequency range Δf_{side} of the sidebands around the center harmonic at three times the switching frequency, i.e. 144 kHz, is, due to the selected modulation (cf. page 159), wide enough such that harmonics with a relevant amplitude are recorded by the test receiver, which has a bandwidth of $\Delta f_{tr} = \pm 4.5$ kHz, i.e. 144 kHz + Δf_{side} > 150 kHz − $|\Delta f_{tr}|$. This issue could be eliminated by slightly lowering the switching frequency, e.g. to 47 kHz.

In the following, the measured total, DM, and CM emissions are compared, on the one hand, to accurate circuit simulations obtained from GeckoCIRCUITS [137] and, on the other hand, to the numerical calculations. Both, simulation and calculation employ the measured filter component values at the switching frequency (cf. Tab. 3.20). The measured emissions of the DM parts are given in **Fig. 3.68(b)** and are

at 192 kHz 70.3 dBµV (phase a), 66.6 dBµV (phase b), and 69.3 dBµV (phase c). For nominal operation the calculated noise source level is 146.5 dBµV and accordingly the calculation leads to 146.5 dBµV − 88.2 dB = 58.3 dBµV, where 88.2 dB is the attenuation provided by the DM part of the EMI filter (including the leakage inductances of the CM chokes).[55] The calculated value is 6.9 dB lower than the simulation result of 65.2 dBµV, which is explained by the reduced inductances of $L_{\mathrm{dm},1}$, $L_{\mathrm{dm},2}$, and $L_{\mathrm{dm},3}$ with the fundamental mains current instantaneous values (cf. Section 3.5.4) included in the simulation. This largely justifies the margin of 3 dB, which was included in the filter design, as explained in Section 3.5.6, and which could even be increased. The simulated value is by 5.1 dB lower than the maximum measured emissions of 70.3 dBµV (for phase a), which is within a margin of 6 dB compared to the simulated results. In conclusion, the theoretical analysis of the DM filter part is successfully verified by the measurements.

From the measured CM noise level shown in Fig. 3.68(c), it can be seen that for frequencies below 500 kHz, the maximum measured emission is 56.5 dBµV and is obtained for 240 kHz (fifth harmonic of the switching frequency) and not for 192 kHz (48.5 dBµV), as assumed for the design of the EMI filter. The same behavior is observed in the simulation, because 240 kHz is close to the resonance frequency of 322 kHz between $C_{\mathrm{dm},2}$ and $L_{\mathrm{dm},2}/3$, where the CM attenuation is lower than the one at 192 kHz [cf. Fig. 3.66(b)]. Nevertheless, the calcualted emitted CM noise of the rectifier is 139.7 dBµV at 192 kHz, which leads to a calculated CM noise at the LISN of 139.7 dBµV−92.7 dB = 47.0 dBµV. 92.7 dB is the calculated attenuation of the CM filtering, for which the parasitics (cf. Fig. 3.50) are included leading to a slightly higher CM attenuation than calculated above for the filter only. Even though the measured and calculated attenuation of the CM filter itself differ by 9 dB, the measured and calculated noise levels show only a difference of 48.5 dBµV − 47.0 dBµV = 1.5 dB. The simulation leads to a CM noise of 43.5 dBµV, which is lower than the calculated value. This can partially be explained by the CM to DM noise conversion resulting from the reduced inductances of the DM inductors with the fundamental mains current instantaneous values [184]. The measured and simulated values differ by 48.5 dBµV − 43.5 dBµV = 5.0 dB, which is lower than

[55] Because of the small leakage inductances $L_{\sigma,1}$ and $L_{\sigma,3}$ of the CM chokes $L_{\mathrm{cm},1}$ and $L_{\mathrm{cm},3}$, i.e. $L_{\mathrm{dm},1} \gg L_{\sigma,1}$ and $L_{\mathrm{dm},3} > L_{\sigma,3}$, the calculated DM attenuation with and without the leakage inductances differ only by 88.2 dB − 87.8 dB = 0.4 dB.

the included margin of 6 dB.

From the comparison of the DM and CM noise spectra, it is concluded that for frequencies $\leq$ 500 kHz the total noise is almost exclusively constituted by DM noise. At 192 kHz the difference between DM and CM noise is more than 20 dB and hence the margin of 6 dB, due to the possible constructive superposition of DM and CM noise with equal magnitude (cf. Section 3.5.6), could have been canceled for the filter design. Furthermore, the design of the CM filter is more challenging than the DM part because of the nonlinearity of VITROPERM with frequency and because of the large tolerances of the VAC cores' A_{L}-values. This leaded to a CM filter design which could be considered too conservative. Nevertheless, it is noted that the presented filter design could comply to CISPR 11, Class A (quasi-peak detector) in a first step with almost no changes. Only L_{M} in Fig. 3.67, which has the size of a fingertip, needed to be added to reduce the CM noise emission due to a resonance at 5.5 MHz.

3.5.8 Summary

In conventional EMI input filters of three-phase voltage source AC–DC converters with sinusoidal input current, the CM capacitance of the Y-capacitors is strongly limited (to a few tens of nanofarads) by the maximum allowed touch current of 3.5 mA (e.g. EN 60335-1 and / or EN 60950-1). To overcome this restriction, it is preferred to achieve the filtering with an internal CM filter capacitor, i.e. a capacitor $C_{\mathrm{cm},1}$ that is connected between the star-point y of the DM capacitors and the midpoint m of the DC link capacitors. A first CM LC filter stage is then realized in combination with a CM inductance $L_{\mathrm{cm},1}$ connected in series with the boost inductors $L_{\mathrm{dm},1}$. For $C_{\mathrm{cm},1}$, higher capacitance values can be employed and, therefore, the achieved CM attenuation can be increased. Moreover, the low-frequency as well as high-frequency CM currents (except the currents occurring due to the parasitic capacitance C_{sc} of the power semiconductors) remain confined to the PWM rectifier system, and a reduced high-frequency fluctuation of the DC output midpoint potential is ensured. However, it should be kept in mind that the benefits of the proposed filter stage depend strongly on the parasitic capacitances of the power semiconductors to the heat sink and of the DC output midpoint m to ground. Thus, the advantages of the proposed CM filter stage have to be investigated for each specific case. For the

considered hardware with a heat sink connected to the midpoint of the DC link, the demonstrated benefits though clearly motivate the proposed first CM LC filter stage with an internal $C_{\mathrm{cm},1}$.

The electrical side conditions to treat this first DM / CM LC stage of the EMI input filter separately from the rest of the circuit are discussed in detail in this section. These side conditions allow finding the optimal ratio $k_{\mathrm{L,opt}} = L_{\mathrm{cm},1}/L_{\mathrm{dm},1}$ of CM inductance to DM inductance, which minimizes the boxed volume $V_{1,\mathrm{tot}}$ of the first filter stage. Moreover, a detailed modeling of the CM choke as well as of the DM inductor is presented, including their thermal models which are validated by experimental results.

It is demonstrated, that $k_{\mathrm{L,opt}} \approx 10 \ldots 40$, i.e. a ratio that almost completely suppresses the high-frequency CM part of the bridge-leg input currents, should be selected to achieve a compact first DM / CM LC stage of the EMI input filter for a 10 kW PWM rectifier system. The selected design employs $k_{\mathrm{L}} = 18$ and the corresponding sum of the volumes of all filter components is 483 cm^3 (29.5 in^3). For this design, it is also verified that the leakage inductance of the CM choke $L_{\mathrm{cm},1}$ is advantageously kept at values lower than $10\% \times L_{\mathrm{dm},1}$ to avoid a

- significant reduction of the total DM filter inductance in case the CM choke core saturates;
- strong magnetic coupling of the CM choke's stray field to other filter components, which possibly lowers the achieved filter attenuation;
- massive reduction of the leakage inductance of the CM choke due to the shielding effect of magnetic shields between filter stages and / or the filter's enclosure.

To validate the proposed design, a DM / CM $LCLCL$ EMI input filter, with a power density of 13.1 kW/dm^3 (215 W/in^3), is realized and a phase-oriented control scheme is implemented on a three-phase three-level T-type rectifier prototype to achieve sinusoidal input currents. This scheme employs only three PI-controllers and convinces by its ease of implementation. With this hardware setup the compliance to CISPR 11, Class A (quasi-peak detector) is successfully demonstrated for nominal operation of 10 kW with almost no additional manipulations of the filter construction. Only magnetic shields made of μ-metal were introduced between the filter stages and a choke of the size of a

fingertip needed to be introduced between the heat sink and the midpoint of the DC output. The results of EMI measurements with a three-phase DM / CM noise separator fully support the presented EMI filter guidelines.

Finally, it should be highlighted that, differently to the DM inductor, the CM choke is not sufficiently characterized by the phase current and the inductance value; the CM choke also needs to be designed with respect to the CM voltage-time area generated by the investigated rectifier in order to avoid saturation of its core and, with this, the volume of the CM choke can be estimated.

The research results presented in this section are partly also published in [311, 312] (see also "List of Publications" on page 337).

4

Converter Module Operation

In the previous chapter the design and operation of the input and output stages are discussed separately. To run both stages together as one converter module (cf. **Fig. 4.1**), they need to be electrically interconnected, which, in the simplest form, can be achieved with a common split DC link composed of $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$. A special feature of the CVS is the individual operation of the phases of the output stage, which also allow a parallel connection of phases for supplying a single-phase load. For a grounded single-phase load and a star-point of the mains connected to ground, the output voltage $v_{\mathrm{N,out}}$ of the neutral leg is controlled to zero, as explained in Section 4.2.1, and therefore the neutral terminal N and the DC link midpoint m can be regarded as shorted for DC and low frequencies.

Under this circumstance the following problem arises: In case of a resistive DC load connected to the output terminal of phase A and the neutral leg terminal N in Fig. 4.1, which requires a positive load voltage $v_{\mathrm{A,load}} > 0$ leading to $i_{\mathrm{A,out}} > 0$, the energy to supply the load is taken only from the upper DC link capacitor $C_{\mathrm{dc},1}$, i.e. only $C_{\mathrm{dc},1}$ is loaded as indicated in **Fig. 4.2**.[1] With the proposed modulation for the input stage (cf. Section 3.5), which over one fundamental mains period charges the split DC link capacitors $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ equally, this continuously asymmetric loading of $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ would lead to DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ drifting apart over time. To solve this problem, i.e. to achieve in average balanced DC link voltages $V_{\mathrm{dc},1}$ and

[1] In a first step, it is assumed that the output of the fourth bridge-leg is continuously connected to m. For the actual operation the output N is actively controlled to zero, i.e. the bridge-leg is also connecting to the positive and negative rails with low duty-cycle for compensating the voltage drop over the output filter.

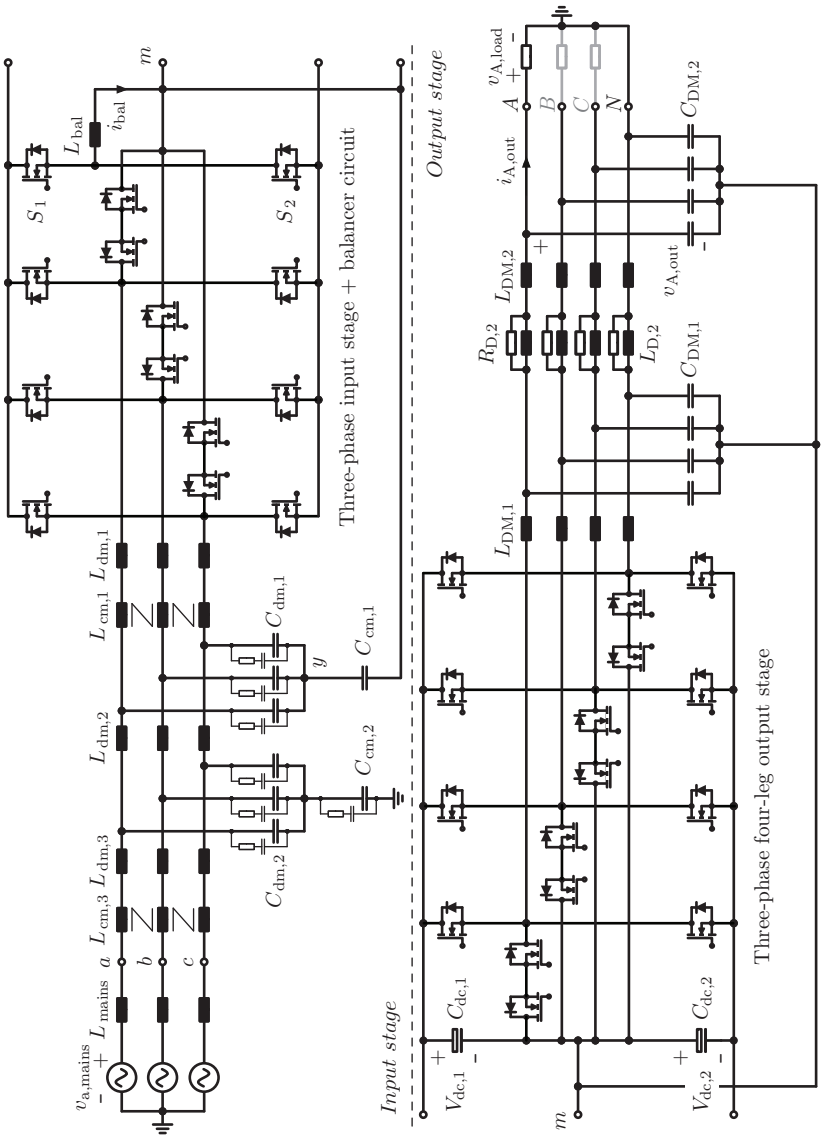


Figure 4.1: 10 kW CVS module with a three-phase input stage inclusive EMI filter, balancer circuit in the split DC link, and three-phase four-leg output stage comprising a four-line two-stage *LC* filter. Exemplary, the load star-point is grounded.

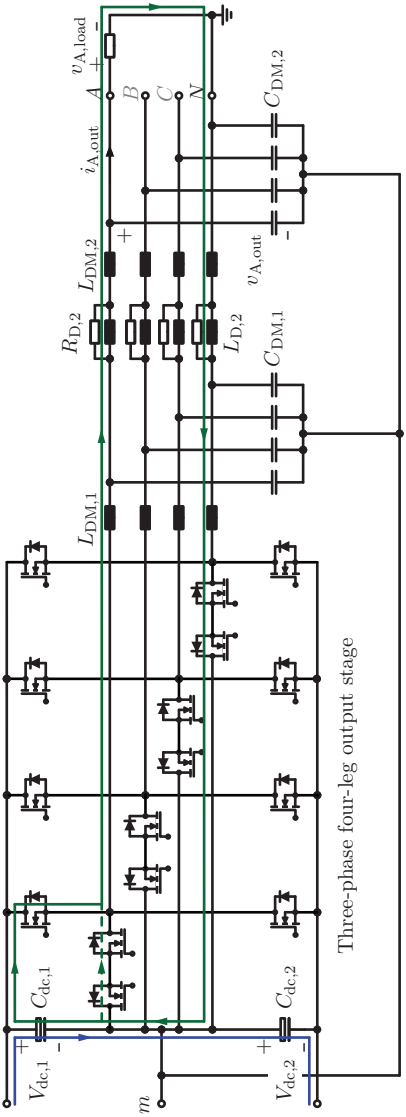


Figure 4.2: Output stage supplying a resistive single-phase DC load connected to phase A with $v_{\mathrm{A,load}} > 0$ and $v_{\mathrm{N,out}}$ controlled to zero.[1] The equal charging of the DC link capacitors by the input stage is highlighted in blue and the loading of only $C_{\mathrm{dc,1}}$ is pointed out in green.

$V_{\mathrm{dc},2}$, the balancer circuit [313–316] shown in Fig. 4.1, is added to the DC link as explained in Section 4.1.1. In this case, a symmetrizing resistor in parallel to each DC link capacitor [316], which would cause excessive power losses in case it would be designed for handling higher asymmetries, can be avoided.

It is noted, that the three-phase three-level PWM rectifier at the input stage has DC link voltage balancing capabilities, which, for reasonable operating points with modulation indices in the range of [280 V / 400 V, 358 V/350 V] $\approx [0.7, 1.0]$,[2] are however not sufficient to achieve the balancing in case only one DC link capacitor is loaded [317].

As explained in Section 3.5, a carrier-based sinusoidal modulation with superimposed low-frequency zero-sequence voltage component v_{zs} is employed to utilize the full (linear) modulation range of the input stage, because it is assumed that the potential of the DC link midpoint m is allowed to float with respect to ground. However, for grounded star-points of the mains and load, i.e. in case the star-point of the mains and the load are connected to PE, v_{zs}, which translates to a low-frequency part $v_{0,\mathrm{cm,lf}}$ of the CM voltage $v_{0,\mathrm{cm}}$ at the bridge-leg inputs of the input stage, leads to a low-frequency part $i_{\mathrm{gnd,lf}}$ of the ground current i_{gnd}, i.e. to a low-frequency zero-sequence current flowing through the module, the star-point of the load, via ground (PE), and finally into the star-point of the mains (see Fig. 4.1 with $v_{\mathrm{N,out}} = 0$, cf. Section 4.2). This current corresponds to the low-frequency sum of the mains input currents $i_{\mathrm{a,mains}}$, $i_{\mathrm{b,mains}}$, and $i_{\mathrm{c,mains}}$, is hence not related to the power transfer, and leads to a higher current stress of the components, to a distortion of the sinusoidal shape of the mains currents as well as to a risk of saturating the filter's inductive elements, especially of the CM chokes. Furthermore, because i_{gnd} flows through PE, the maximum allowed ground current for safety reasons and for a non-stationary device is limited by EN 61140 [318][3] to 5 mA (rms). Even if the standard refers to a different operating condition, the current limit can be considered meaningful also for the case at hand.

To avoid these issues and to comply to the mentioned standard, $i_{\mathrm{gnd,lf}}$ needs to be ideally zero, which could theoretically be achieved

[2] 280 V and 358 V correspond to a decrease and an increase of the mains voltage by 14% and 10%, respectively, due to the tolerances of the mains voltage; 350 V and 400 V are half of the nominal and maximal DC link voltages, respectively (cf. Tabs. 3.16 and 3.8).

[3] EN 61140: Protection against electric shock – common aspects for installation and equipment [318].

by employing a modulation scheme without a superposition of a zero-sequence voltage component, i.e. $v_{\mathrm{zs}} = 0$. However, even with $v_{\mathrm{zs}} = 0$, deviations in the formation of the bridge-leg input voltages v_{a0}, v_{b0}, and v_{c0} from the desired values $v_{\mathrm{a0,set}}$, $v_{\mathrm{b0,set}}$, and $v_{\mathrm{c0,set}}$ (e.g. due to turn-on / off delays of the switches and interlocking time) may lead to a low-frequency and / or even a DC part of the CM voltage $v_{0,\mathrm{cm}}$, which would accordingly result in a low-frequency and / or a DC part of the ground current i_{gnd}. Thus, v_{zs} needs to be actively adjusted such that $i_{\mathrm{gnd}} = 0$ results, which can be obtained with the new control scheme elaborated in Section 4.2. It is noted that the proposed control scheme eliminates the low-frequency and DC parts of the ground current i_{gnd}. The high-frequency (frequency $\geq f_{\mathrm{s,in}}$) part of i_{gnd} at the mains terminal is reduced by the input stage EMI filter (cf. also [267, 286, 319]). Despite the direct connection of m to ground (instead of $C_{\mathrm{g}} = 25$ nF considered for the EMI filter design), the EMI input filter (cf. Section 3.5) can in a first step be seen as sufficient for ensuring compliance to CISPR 11, Class A. Alternatively, i_{gnd} can also be controlled to zero with the help of the fourth output leg.

The insertion of a galvanic isolation is another option to eliminate i_{gnd}, which is preferably achieved with a high-frequency galvanically isolated DC–DC converter linking the input and the output stages. This reduces weight and volume compared to the conventional solution which employs a line-frequency transformer at the input of the CVS [320, 321]. Such DC–DC converters are widely discussed in literature (cf. [322–332] for example) and are hence not focused on at this point. However, in combination with the DC link voltage balancing and to reduce the number of power transistors of the CVS, the balancer circuit can be omitted and the DC link voltage balancing capability can be integrated into the galvanic isolated DC–DC converter. This novel concept is presented in Section 4.3 on the basis of a Series Resonant Converter (SRC).

Finally, the advantages and disadvantages of eliminating the ground current i_{gnd} by means of control compared to the option of avoiding i_{gnd} by inserting a galvanic isolation are discussed in Section 4.4, where also the correct operation of the entire CVS, as elaborated in Chapter 3 for the input and output stages separately, is verified.

4.1 DC Link Voltage Balancing

As mentioned in the introduction to Chapter 4, in case of a continuous unequal loading of the DC link capacitors $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$, a balancer circuit is used to achieve in average balanced, i.e. equal, DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ as explained in Section 4.1.1. For completeness it is elaborated in Section 4.1.2, that the neutral leg of the three-phase four-leg output stage has limited DC link voltage balancing capabilities. In anticipation of the results presented in the following, these capabilities, however, cannot be exploited for grounded mains and load star-points, because $v_{\mathrm{N,out}}$ in Fig. 4.1 is controlled to zero (cf. Section 4.2.1). $v_{\mathrm{N,out}} = 0$ is also assumed for the derivation presented in Section 4.1.1.

4.1.1 Balancer Circuit

The balancer circuit, composed of power transistors S_1, S_2 and a balancer inductor L_{bal}, is shown in **Fig. 4.3(a)** and convinces by its simplicity of operation as explained in the following. By redrawing the circuit, it is recognized from **Fig. 4.3(b)** that this balancer circuit actually represents a bidirectional inverting buck-boost converter.

In the equivalent circuit shown in Fig. 4.3(a), the equal charging of $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ by the input stage is represented by a current source $I_{\mathrm{dc,in}}$, which adjusts its value such that the total DC link voltage V_{dc} is regulated to the nominal value. The unequal loading of the DC link capacitors by the output stage is modeled by a DC current source $I_{\mathrm{dc,1,out}}$, which loads only $C_{\mathrm{dc},1}$, and the equal loading of $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ is given by a DC current source $I_{\mathrm{dc,out}}$.

On the one hand, if the switch S_1 is on (S_2 is off), $v_{\mathrm{bal}} = V_{\mathrm{dc},1} > 0$ is applied to the balancer inductor L_{bal} and therefore the current i_{bal} is increased. On the other hand, if S_2 is on (S_1 is off), $v_{\mathrm{bal}} = -V_{\mathrm{dc},2} < 0$ is applied to L_{bal} leading to a reduction of i_{bal}. Thus, with a proper driving of the switches S_1 and S_2, the balancer circuit can inject, in average over one switching period (i.e. neglecting the ripple), an arbitrary positive / negative current i_{bal} into the midpoint of the DC link m. i_{bal} is only limited by the maximum rating of the balancer circuit. For instance, a negative average of i_{bal} discharges $C_{\mathrm{dc},2}$ if S_2 is on and charges $C_{\mathrm{dc},1}$ if S_1 is on (vice versa for a positive average of i_{bal}) resulting in a redistribution of the energy among the two DC link capacitors.

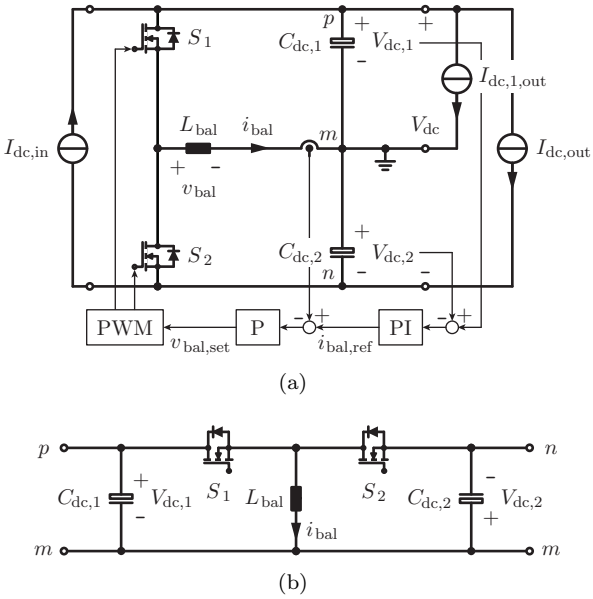


Figure 4.3: (a) Balancer circuit, composed of switches S_1, S_2 and balancer inductance L_{bal}, to achieve in average equal voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ of the split DC link; and **(b)** rearranged equivalent circuit of the balancer circuit given in (a) representing a bidirectional inverting buck-boost converter.

Because of this energy-redistribution capability of the balancer circuit, equal DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ can be achieved using the control scheme depicted in Fig. 4.3(a). A voltage PI-controller adjusts $V_{\mathrm{dc},2}$ to $V_{\mathrm{dc},1}$. If a positive voltage difference occurs, i.e. for $V_{\mathrm{dc},1} - V_{\mathrm{dc},2} > 0$, the current reference $i_{\mathrm{bal,ref}}$ is increased, which finally results in a higher balancing current i_{bal}. The higher average value of i_{bal} enhances the discharging of $C_{\mathrm{dc},1}$ and at the same time boosts the charging of $C_{\mathrm{dc},2}$, because the balancer circuit is operated with a duty-cycle of roughly 0.5 as explained below. In this manner $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ are adjusted to each other.

For balanced steady-state DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$, the average of i_{bal} is given by the difference in the currents loading the DC link capacitors, i.e. $-I_{\mathrm{dc},1,\mathrm{out}}$ and needs to be kept constant by the control

scheme given in Fig. 4.3(a). This leads to $T_1 \cdot V_{\mathrm{dc},1} - T_2 \cdot V_{\mathrm{dc},2} = 0$, where T_1 and T_2 are the on-times of the switches S_1 and S_2 within one pulse period, respectively. Therefore, ideally, $V_{\mathrm{dc},1} = V_{\mathrm{dc},2}$ and accordingly $T_1 = T_2$ results, which leads to a duty-cycle $\delta_{\mathrm{bal}} = 0.5$ of the two-level balancer bridge-leg. Except for the short duration of DC link voltage transients, the two-level balancer circuit is thus always operating with maximum ripple of i_{bal}.

The above considerations are given for an unequal DC loading of the DC link capacitors, represented by the current sources $I_{\mathrm{dc,out}}$ and $I_{\mathrm{dc,1,out}}$ in Fig. 4.3(a), and a perfect control of the entire DC link voltage V_{dc}. Even for this perfect voltage control (V_{dc} is controlled by the input stage, cf. Fig. 3.64), oscillations with three times the mains frequency ($3 \cdot f_{\mathrm{mains}} = 150$ Hz) result in the partial DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ also for equal DC loading of $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ without balancer circuit operation. The oscillations of $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ are caused by the selected modulation scheme for the input stage (cf. Section 3.5; no ground current control required) and are phase-shifted by 180 deg such that the sum $V_{\mathrm{dc}} = V_{\mathrm{dc},1} + V_{\mathrm{dc},2}$ is constant. With balancer circuit operation, these oscillations should not be amplified in amplitude and hence the control parameters of the DC link voltage equalization control system shown in Fig. 4.3(a) are tuned such that the resulting system dynamics permit reducing the amplitude of these oscillations.

In case a resistive single-phase AC load requiring a load voltage of 230 V (rms), a frequency of 50 Hz, and a power of 3.3 kW is supplied by one of the CVS' phases (cf. Fig. 4.1), the DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ would show a voltage swing at 50 Hz without balancer operation. However, with the proposed tuning of the controllers, the balancer circuit allows compensating this 50 Hz oscillation to a main extent and GeckoCIRCUITS simulations revealed that, for the given conditions, the peak value of i_{bal} is almost equal to the nominal peak output current value $I_{\mathrm{out,n,pk}} = \sqrt{2} \cdot 14.5\ \mathrm{A} = 20.5\ \mathrm{A}$. As for the output stage (cf. Section 3.2), the maximum peak-to-peak ripple of i_{bal} is therefore limited to 60% of $I_{\mathrm{out,n,pk}}$, which leads to $L_{\mathrm{bal}} = 308\ \mu\mathrm{H}$ for the selection of a high switching frequency $f_{\mathrm{s,bal}} = 48$ kHz of the balancer bridge-leg to allow for a small volume of L_{bal}. Considering the practical gain limitations given in (3.82), the control parameters as summarized in **Tab. 4.1** are determined from simulations. Furthermore, S_1 and S_2 could be realized with the same type of switch, i.e. SiC MOSFETs, as employed for the input and output stages.

Table 4.1: Parameters of the voltage and current controllers of the DC link voltage equalization control scheme depicted in Fig. 4.3(a).

Voltage PI-controller	$k_{\mathrm{pv}} = 1.5$ A/V, $T_{\mathrm{iv}} = 1$ ms
Current P-controller	$k_{\mathrm{pi}} = 3.0$ V/A

Table 4.2: Operating conditions for which the DC link voltages V_{dc}, $V_{\mathrm{dc},1}$, and $V_{\mathrm{dc},2}$ shown in Fig. 4.4 are simulated.

DC link voltage, V_{dc}	700 V
DC link capacitance, $C_{\mathrm{dc},1} = C_{\mathrm{dc},2}$	1.28 mF
Switching frequency, $f_{\mathrm{s,bal}}$	48 kHz
Sampling frequency, $f_{0,\mathrm{bal}}$	96 kHz
Load voltage of phase A, $v_{\mathrm{A,load}}$	230 V
Output voltage of the neutral leg, $v_{\mathrm{N,out}}$	0
Load resistance of phase A, $R_{\mathrm{A,load}}$	31.8 Ω $\rightarrow$ 15.9 Ω

The simulated DC link voltages V_{dc}, $V_{\mathrm{dc},1}$, and $V_{\mathrm{dc},2}$ are depicted in **Fig. 4.4** for the conditions given in **Tab. 4.2**, where a load step from half nominal power, i.e. 1.67 kW, to full nominal power, i.e. 3.3 kW, in output phase A is considered (the load is connected between A and N and is floating with respect to ground). The simulation has been conducted for the entire CVS module according to Fig. 4.1, for which the other two output phases are not operated and the output voltage $v_{\mathrm{N,out}}$ of the neutral leg is actively controlled to zero. The input stage is driven as explained in Section 3.5. Fig. 4.4 shows that balanced DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ are obtained with the help of the balancer circuit. Furthermore, the oscillations in the voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ due to the employed modulation scheme of the input stage can be recognized in the figure.

4.1.2 DC Link Voltage Balancing by the Fourth Output Leg

For the sake of completeness, it should be noted that the neutral bridge-leg of the three-phase four-leg realization of the output stage (cf. Fig. 4.1), has certain DC link voltage balancing capabilities. It is remarked, that in this case, the neutral leg cannot anymore be em-

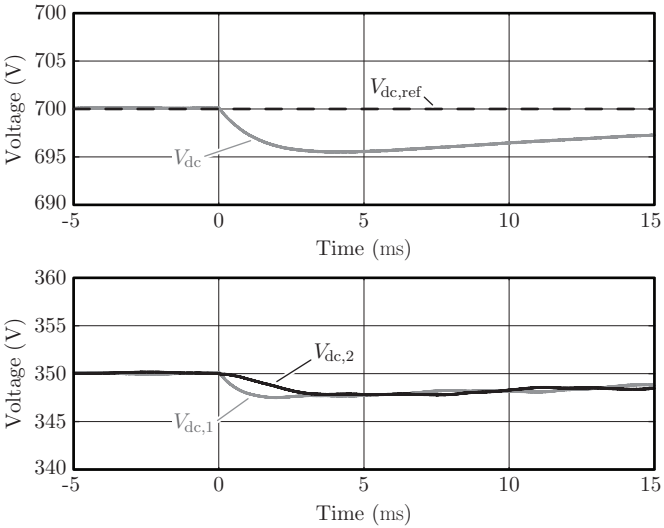


Figure 4.4: Simulated DC link voltages V_{dc}, $V_{dc,1}$, and $V_{dc,2}$, considering the entire CVS module (cf. Fig. 4.1), for the conditions given in Tab. 4.2, where a load step from half nominal power per phase, i.e. 1.67 kW, to full nominal power, i.e. 3.3 kW, in output phase A occurs at $t = 0$. *Remark*: No load on phases B and C.

ployed to maximize the range of the phase load voltages $v_{A,load}$, $v_{B,load}$, and $v_{C,load}$.

To derive a condition for the neutral leg to achieve DC link voltage balancing, the ripples of the bridge-leg output currents of all legs are neglected and constant output currents $i_{A,out}$, $i_{B,out}$, $i_{C,out}$, and $i_{N,out}$ are assumed. A generation of constant output voltages and no direct transitions of the bridge-leg output voltages from positive to negative values are further assumed. The load / loads is / are connected between the phase terminals A, B, and C and the neutral leg terminal N.

For an equal charging of the DC link capacitors $C_{dc,1}$ and $C_{dc,2}$ by the input stage, balanced DC link voltages are obtained for an equal loading of $C_{dc,1}$ and $C_{dc,2}$ by the output stage. This is the case for $I_{dc,out,1} = I_{dc,out,2}$ in **Fig. 4.5** and hence, for the mentioned conditions and assumptions, equal DC link voltages $V_{dc,1}$ and $V_{dc,2}$ (averaged over one switching period) can be achieved if the modulation index $m_{i,N}$ for

the neutral bridge-leg satisfies

$$|m_{\mathrm{i,A}}| \cdot i_{\mathrm{A,out}} + |m_{\mathrm{i,B}}| \cdot i_{\mathrm{B,out}} + |m_{\mathrm{i,C}}| \cdot i_{\mathrm{C,out}} + |m_{\mathrm{i,N}}| \cdot i_{\mathrm{N,out}} = 0 \text{ and } |m_{\mathrm{i,N}}| \leq 1, \tag{4.1}$$

where $m_{\mathrm{i,A}}$, $m_{\mathrm{i,B}}$, and $m_{\mathrm{i,C}}$ are the modulation indices at which the bridge-legs of the phases A, B, and C are operated, respectively. These modulation indices are defined as

$$m_{\mathrm{i},k} = \begin{cases} v_{k,\mathrm{out}}/V_{\mathrm{dc},1} & \text{if } \; v_{k,\mathrm{out}} \geq 0 \\ v_{k,\mathrm{out}}/V_{\mathrm{dc},2} & \text{if } \; v_{k,\mathrm{out}} < 0 \end{cases} \tag{4.2}$$

for $k = A, B, C, N$ and an ideal formation of the bridge-leg output voltages. Because the load / loads is / are all connected to the neutral terminal N, the output current $i_{\mathrm{N,out}}$ of the neutral leg is given by the sum of the output phase currents, i.e.

$$i_{\mathrm{N,out}} = -\left(i_{\mathrm{A,out}} + i_{\mathrm{B,out}} + i_{\mathrm{C,out}}\right), \tag{4.3}$$

assuming that the load star-point is not grounded (i.e. no ground current possible). Moreover, for (4.1) an equal charging of $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ by the input stage is assumed.

To give an example for an illustrative case, a positive output current $i_{\mathrm{A,out}} > 0$ and a modulation index $m_{\mathrm{i,A}}$ equal to 0.5 for phase A are assumed while phases B and C are not operated, for which a modulation index of the neutral leg of $m_{\mathrm{i,N}} = \pm m_{\mathrm{i,A}} = \pm 0.5$ follows directly from (4.1) [$i_{\mathrm{N,out}} = -i_{\mathrm{A,out}}$]. The operating point with $m_{\mathrm{i,N}} = 0.5$ leads to $v_{\mathrm{N,out}} = v_{\mathrm{A,out}}$ and hence to no load voltage generation, i.e. $v_{\mathrm{A,load}} = v_{\mathrm{A,out}} - v_{\mathrm{N,out}} = 0$, which obviously does neither load $C_{\mathrm{dc},1}$ nor $C_{\mathrm{dc},2}$. Accordingly, balanced DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ can be achieved by the input stage. For the other operating point, i.e. with $m_{\mathrm{i,N}} = -0.5$, the flowing direction of the currents through the bridge-legs of phase A and of the neutral leg N of the output stage are depicted in Fig. 4.5, from where it can immediately be seen that the DC link capacitors $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ are equally loaded by the output stage due to the fourth bridge-leg. For the interval $m_{\mathrm{i,A}} \cdot T_{\mathrm{s,out}} = 0.5 \cdot T_{\mathrm{s,out}}$, $i_{\mathrm{A,out}}$ is loading $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ equally (solid green path in Fig. 4.5), while for the interval $(1 - m_{\mathrm{i,A}}) \cdot T_{\mathrm{s,out}} = 0.5 \cdot T_{\mathrm{s,out}}$ the current $i_{\mathrm{A,out}}$ is circulating between the bridge-leg branches connected to the midpoint m (dashed green path in Fig. 4.5). Thus, balanced DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ can again be achieved by the input stage. Without the

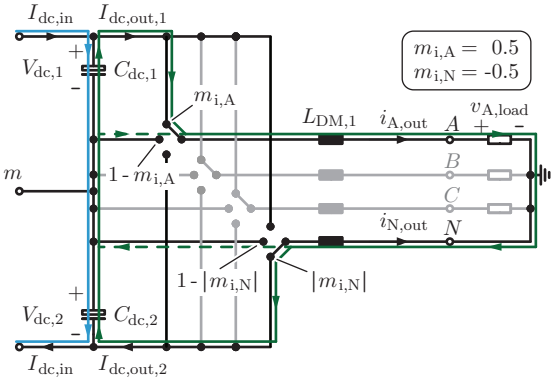


Figure 4.5: Flowing direction (accentuated in green) of the currents through the bridge-legs of phase A and of the neutral leg N of the output stage for the operation of only phase A with a modulation index of $m_{\mathrm{i,A}} = 0.5$ and for a positive output current, i.e. $i_{\mathrm{A,out}} > 0$, which leads to $m_{\mathrm{i,N}} = -m_{\mathrm{i,A}} = -0.5$ [cf. (4.1)]. For the solid green path, the bridge-leg output of phase A and the neutral leg N are connected to the positive and negative DC link rails, respectively, meanwhile both bridge-leg outputs are connected to the DC link midpoint for the dashed green path. This clearly points out that an equal loading of the DC link capacitors can be achieved with the neutral leg which leads to balanced DC link voltages. An equal charging of the DC link capacitors by the input stage with $I_{\mathrm{dc,in}}$ (highlighted in blue) is assumed. It is noted that because of $m_{\mathrm{i,N}} = -m_{\mathrm{i,A}}$, balanced DC link voltages can also be achieved for modulation indices which are different from $m_{\mathrm{i,A}} = 0.5$. The modulation scheme for all legs is as explained in Section 2.1 (the carriers of all legs are in phase, cf. Fig. 2.4). To concentrate on what counts most, a single inductor $L_{\mathrm{DM,1}}$ at the bridge-leg outputs is drawn instead of the two-stage LC filter.

fourth leg, the load star-point would be connected to the midpoint m of the DC link and accordingly only $C_{\mathrm{dc,1}}$ would be continuously loaded with $i_{\mathrm{A,out}}$ during the interval $m_{\mathrm{i,A}} \cdot T_{\mathrm{s,out}}$.

It is remarked that because of $|m_{\mathrm{i,N}}| = |m_{\mathrm{i,A}}|$ following from (4.1), the above drawn conclusions are also valid for modulation indices different from $m_{\mathrm{i,A}} = 0.5$.

Moreover, it is noted by considering Fig. 4.1 that the phase load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ are defined with respect to the neural terminal N and hence the phase output voltages $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$,

and $v_{\mathrm{C,out}}$, generated with reference to the DC link midpoint m, are obtained by adding the output voltage $v_{\mathrm{N,out}}$ of the neutral leg to the phase load voltages. This yields

$$\begin{aligned} v_{\mathrm{A,out}} &= v_{\mathrm{A,load}} + v_{\mathrm{N,out}}, \\ v_{\mathrm{B,out}} &= v_{\mathrm{B,load}} + v_{\mathrm{N,out}}, \\ v_{\mathrm{C,out}} &= v_{\mathrm{C,load}} + v_{\mathrm{N,out}} \end{aligned} \tag{4.4}$$

and demonstrates that the phase modulation indices $m_{\mathrm{i,A}}$, $m_{\mathrm{i,B}}$, and $m_{\mathrm{i,C}}$ defined in (4.2) all depend also on $v_{\mathrm{N,out}}$ and hence on $m_{\mathrm{i,N}}$.

To which extent the DC link voltage balancing is possible with the fourth bridge-leg for all kind of considered load voltage situations (within the specifications given in Tab. 1.1) and output loads as summarized on page 2 is a matter of further analysis. This analysis is omitted here, as a drawback of this DC link voltage balancing method, compared to the employment of the balancer circuit, can be derived considering the following possible loading of the CVS, where a resistive DC load is supplied with $v_{\mathrm{A,load}} = 300$ V by output phase A and output phase B needs to generate a constant load voltage of $v_{\mathrm{B,load}} = -300$ V without being loaded (phase C is not in operation). For this loading of the CVS, $i_{\mathrm{B,out}} = i_{\mathrm{C,out}} = 0$ is given and hence (4.1) simplifies with (4.3) to

$$|m_{\mathrm{i,A}}| \cdot i_{\mathrm{A,out}} - |m_{\mathrm{i,N}}| \cdot i_{\mathrm{A,out}} = 0 \quad \rightarrow \quad |m_{\mathrm{i,A}}| = |m_{\mathrm{i,N}}|\,, \tag{4.5}$$

which can be solved for $m_{\mathrm{i,N}}$ and leads to

$$m_{\mathrm{i,N}} = -m_{\mathrm{i,A}} \quad \rightarrow \quad \frac{v_{\mathrm{N,out}}}{V_{\mathrm{dc,2}}} = -\frac{v_{\mathrm{A,out}}}{V_{\mathrm{dc,1}}} = -\frac{v_{\mathrm{A,load}} + v_{\mathrm{N,out}}}{V_{\mathrm{dc,1}}}. \tag{4.6}$$

For equal DC link voltage $V_{\mathrm{dc,1}} = V_{\mathrm{dc,2}}$ this results in a neutral output voltage of $v_{\mathrm{N,out}} = -v_{\mathrm{A,load}}/2 = -150$ V, which means for phase B that its bridge-leg should set an average output voltage equal to $v_{\mathrm{B,out}} = v_{\mathrm{B,load}} + v_{\mathrm{N,out}} = -300\text{ V} - 150\text{ V} = -450$ V, which cannot be generated, even with the maximum DC link voltage $V_{\mathrm{dc,max}}$ of 800 V ($-400\text{ V} \leq v_{\mathrm{B,out}} \leq 400$ V for $V_{\mathrm{dc,max}} = 800$ V). Although the above case may seems to be of limited importance, similar conditions could occur in certain time intervals when individual AC loads are supplied by the CVS' output phases. These considerations clearly favor to balance the DC link voltages $V_{\mathrm{dc,1}}$ and $V_{\mathrm{dc,2}}$ with the balancer circuit given in Fig. 4.3(a).

4.1.3 Summary

A continuously asymmetric loading of the split DC link capacitors $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ results for a grounded DC load connected to only one output phase. This would lead to DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ that drift apart over time. Because the CVS must be able to handle this operating condition, two solutions to this problem have been investigated: the employment of an explicit balancer circuit and the utilization of the fourth bridge-leg of the output stage for balancing $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$.

Balancing $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ by the fourth bridge-leg would be an elegant solution, however, as demonstrated in Section 4.1.2, the concept does not allow to cover all targeted operating conditions of the CVS (cf. Tab. 1.1). Furthermore, this voltage balancing approach cannot be employed for grounded mains and load star-points, because $v_{\mathrm{N,out}}$ of the output stage's neutral leg (cf. Fig. 4.1) must be controlled to zero in this case (cf. Section 4.2.1).

On the other hand, a balancer circuit, consisting of only two power transistors (forming a two-level bridge-leg) and an inductor, provides a simple, robust, and efficient option to balance the DC link voltages, and does not suffer from the two drawbacks just mentioned. Accordingly, the balancer circuit is the preferred solution to solve the problem of a possible unbalance of $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$. The control of the balancer circuit is investigated by circuit simulations and simple design guidelines are given for the control scheme as well as for the balancer inductance.

4.2 Ground Current Control

As explained in the introduction of this chapter, a ground current i_{gnd}, which could contain low-frequency and / or DC components, results for grounded mains star-point and grounded load (e.g. star-point of a three-phase load or single-phase load connected to the neutral terminal N, cf. Fig. 4.1), because a zero-sequence current path through the CVS module and returning over ground exists.

To start the analysis, the zero-sequence equivalent circuit of the CVS module depicted in **Fig. 4.6** is considered. In this figure the input stage's bridge-legs, DC link capacitors, and PWM units are represented by a controllable zero-sequence voltage source $v_{0,\mathrm{cm,set}}$. In the interest of simplicity, the control of the neutral leg's output voltage $v_{\mathrm{N,out}}$ is assumed to be ideal. Furthermore, the formation of the averaged (over one switching cycle) zero-sequence input voltage $\langle v_{0,\mathrm{cm}} \rangle_{T_{\mathrm{s,in}}}$ is also idealized, i.e. $\langle v_{0,\mathrm{cm}} \rangle_{T_{\mathrm{s,in}}} = v_{0,\mathrm{cm,set}}$.

It is remarked that the total CM inductance at the input of Fig. 4.6 is given by

$$L_{\mathrm{cm,3,tot}} = L_{\mathrm{cm,3}} + \frac{L_{\mathrm{dm,3}}}{3} + \frac{L_{\mathrm{mains}}}{3} \tag{4.7}$$

and can be approximated to

$$L_{\mathrm{cm,3,tot}} \approx L_{\mathrm{cm,3}} \tag{4.8}$$

since $L_{\mathrm{cm,3}} \gg L_{\mathrm{mains}}/3 + L_{\mathrm{dm,3}}/3$ for the designed EMI input filter (cf. Tab. 3.20) and for mains inductances L_{mains} in the range of $[0, 500\ \mu\mathrm{H}]$. Thus, it can be assumed that L_{mains}, which is typically not exactly known, has a negligible impact on the formation of i_{gnd} and accordingly also the dynamics of the subsequently derived ground current control system is unaffected by L_{mains}.

Referring to Fig. 4.6, i_{gnd}, i.e. the sum of the input phase currents of the CVS, can be controlled to zero by adjusting the voltage $v_{\mathrm{C,cm,2}}$ across the CM capacitor $C_{\mathrm{cm,2}}$ of the second stage of the EMI input filter accordingly. $v_{\mathrm{C,cm,2}}$ occurs directly across the total CM input inductance $L_{\mathrm{cm,3,tot}}$ and thus immediately affects i_{gnd}. The voltage $v_{\mathrm{C,cm,2}}$ can be regulated by the zero-sequence voltage component $v_{0,\mathrm{cm,set}}$ formed by the input stage or by the neutral leg's output voltage $v_{\mathrm{N,out}}$. Thus, either $v_{0,\mathrm{cm,set}}$ or $v_{\mathrm{N,out}}$ can be adjusted to control i_{gnd} to zero. Variations of $v_{\mathrm{N,out}}$ slightly affect the phase load voltages because $v_{\mathrm{N,out}}$ is related to the generation of the load voltages according

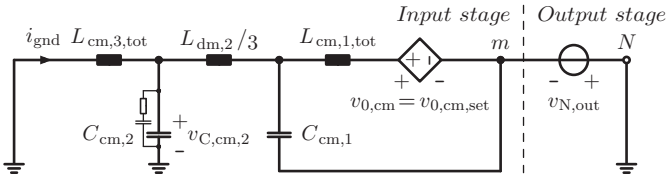


Figure 4.6: Zero-sequence equivalent circuit of the CVS module (cf. Fig. 4.1) for grounded mains star-point and grounded load. Because the capacitance values of the DM capacitors $C_{\mathrm{dm,1}}$ and $C_{\mathrm{dm,2}}$ are much larger than the ones of the CM capacitors $C_{\mathrm{cm,1}}$ and $C_{\mathrm{cm,2}}$ (cf. Tab. 3.20), $C_{\mathrm{dm,1}}$, $C_{\mathrm{dm,2}}$, and their corresponding parallel RC damping branches in series to $C_{\mathrm{cm,1}}$ and $C_{\mathrm{cm,2}}$, are omitted in the equivalent circuit.

to (3.85), and hence it is preferred to employ $v_{0,\mathrm{cm,set}}$ for controlling the ground current i_{gnd}.

In the following, the ground current control scheme is explained in Section 4.2.1 and its effectiveness to suppress i_{gnd} is verified in Section 4.2.2 by a circuit simulation. A short summary is given in Section 4.2.3.

4.2.1 Ground Current Control Scheme

The considerations above lead to the control scheme given in **Fig. 4.7**. The ground current i_{gnd}, respective the sum of the CVS input phase currents, is measured. An outer current control loop employing a PI-controller generates a reference $v_{\mathrm{cm,set}}$ for the CM voltage $v_{0,\mathrm{cm}}$, instead of adjusting a reference for $v_{\mathrm{C,cm,2}}$ (or alternatively for the voltage across the first CM filter capacitor $C_{\mathrm{cm,1}}$). This avoids an additional control loop which would generate $v_{\mathrm{cm,set}}$ from the reference for $v_{\mathrm{C,cm,2}}$.

To attenuate oscillations in i_{gnd} at the frequency of the input filter resonance of roughly 12 kHz [cf. Fig. 3.66(b)], active damping is provided by a capacitor current feedback loop employing the current $i_{\mathrm{cm,1}}$ through $C_{\mathrm{cm,1}}$ and the gain k_{g}. The output voltage $v_{\mathrm{N,out}}$ of the fourth bridge-leg of the output stage acts as a disturbance to the proposed control approach, which can be taken into account by employing $v_{\mathrm{N,out}}$ as a feedforward for $v_{0,\mathrm{cm,set}}$; alternatively, for avoiding a dynamic coupling, also $v_{\mathrm{N,ref}}$ could be considered (cf. Fig. 4.7).

The presented ground current control scheme employs the CM

bridge-leg input voltage $v_{0,\mathrm{cm,set}}$ to regulate i_{gnd} to zero and accordingly no zero-sequence voltage component v_{zs} [cf. (3.89)] can be superimposed on the carrier based sinusoidal modulation of the input stage to increase the linear modulation range. Furthermore, if the voltage $v_{\mathrm{N,out}}$ of the output stage's neutral leg is still employed to increase the range of the load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ [cf. (3.86)], the CM voltage $v_{0,\mathrm{cm,set}}$ needs to compensate $v_{\mathrm{N,out}}$, in order to ensure that no resulting source voltage is effective in the ground current loop of Fig. 4.6 which could drive a large i_{gnd}. For a ground current close to zero the voltage drops across the inductive elements of the input filter are negligible and hence $v_{0,\mathrm{cm,set}} \approx v_{\mathrm{N,out}}$ results. In this case, the bridge-legs of the input stage need to generate voltages which are all increased by $v_{\mathrm{N,out}}$, possibly requiring input voltages that in magnitude exceed the maximum voltage of $V_{\mathrm{dc}}/2$, because $v_{\mathrm{N,out}}$ is adjusted according to the requirements of the load voltage generations, which are independent of the needs of the input stage. To avoid this to happen, the DC link voltage could be increased, what, however, already increases the feasible range of the load voltages and hence $v_{\mathrm{N,out}}$ is potentially not required anymore for this purpose. Accordingly, the output voltage $v_{\mathrm{N,out}}$ of the neutral leg is controlled to zero ($v_{\mathrm{N,ref}} = 0$) in case the mains star-point and the load are grounded.

Remark: The proposed control scheme for the input stage given in Fig. 4.7 controls two bridge-leg input currents (phases b and c) and the sum of all three mains input phase currents, i.e. i_{gnd}, to suppress a zero-sequence current flowing through the module and returning in the opposite direction over ground. Alternatively, all three bridge-leg input currents (inclusive phase a) could be controlled to pure DM currents to eliminate the zero-sequence part of the three currents. However, it is expected that for this latter control approach the steady-state ground current is larger than the one obtained with the proposed control scheme, because i_{gnd} can be measured in the range of ±290 mA–725 mA (i.e. 2%–5% of $I_{\mathrm{in,n}} = 14.5$ A) for the proposed scheme and does not result from the sum of three bridge-leg input currents which are each measured in the range of ±25 A as it is the case for the alternative approach.

The control parameters of the ground current control scheme given in Fig. 4.7 have been determined from GeckoCIRCUITS simulations and are summarized in **Tab. 4.3**. The maximum values of the gains, i.e. $k_{\mathrm{pi,g}}$ and k_{g}, are restricted to maximally 10 V/A and 20 V/A, respectively,

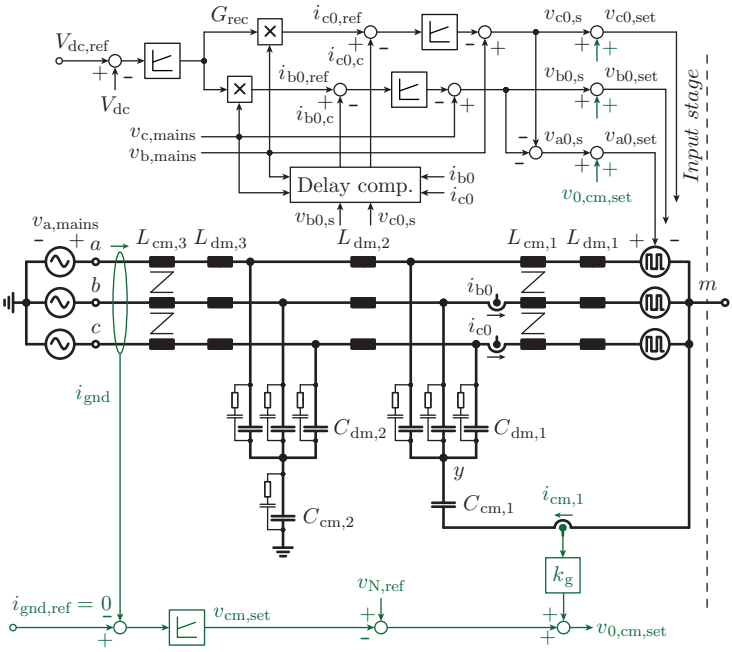


Figure 4.7: Entire control scheme for a single 10 kW CVS module (cf. Fig. 4.1), including a DC link voltage and a ground current control scheme for the input stage, and a phase-oriented control structure for the output stage of the module. The ground current control scheme is highlighted in green.

Table 4.3: Control parameters of the ground current control loops as given in Fig. 4.7.

Outer PI current controller	$k_{\mathrm{pi,g}} = 10$ V/A, $T_{\mathrm{ii,g}} = 70$ µs
Capacitor current feedback gain	$k_{\mathrm{g}} = 20$ V/A

according to the limits specified in (3.82).

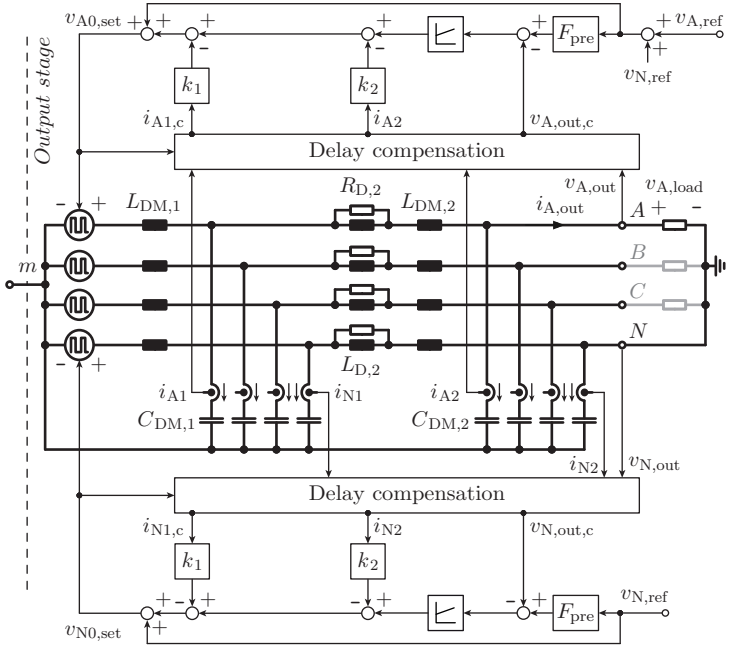


Figure 4.7: Continued.

4.2.2 Simulation Results

With the proposed ground current control scheme (cf. Fig. 4.7), a GeckoCIRCUITS simulation of the CVS module, as given in Fig. 4.1, has been performed for the following representative case, for which the CVS runs at nominal conditions:

- Connection of the mains star-point to PE and connection of the output neutral terminal N to PE; resistive symmetrical three-phase load of $R_{\text{load}} = 15.9\,\Omega$ with the load star-point connected to N. The output phases A, B, and C generate a symmetrical three-phase voltage system (with respect to the neutral terminal N) with 230 V (rms; line-to-neutral) and at 50 Hz. The output voltage of the neutral leg N is controlled to zero.

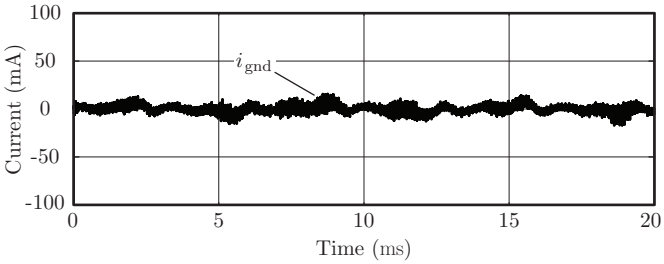


Figure 4.8: Remaining ground current for a single 10 kW CVS module flowing through the mains star-point for a resistive symmetric three-phase load $R_{load} = 15.9\ \Omega$ with grounded star-point and supplied by a three-phase voltage system with 230 V (rms; line-to-neutral) and 50 Hz.

Input and output stages are implemented as explained in Chapter 3 assuming a realistic mains inductance of $L_{mains} = 300\ \mu H$ and a mains voltage of 230 V (rms; line-to-neutral) at 50 Hz. The parameters of the balancer circuit with its control scheme are as elaborated in Section 4.1.1 and the DC link voltage is $V_{dc} = 700$ V.

The ground current i_{gnd} resulting for this case is shown in **Fig. 4.8**. The maximum of the absolute value of i_{gnd} is slightly less than 18 mA and the maximum amplitude of the low-frequency harmonics in i_{gnd} is 2.7 mA and occurs at 150 Hz. The rms value of i_{gnd} is 4.4 mA and hence the compliance to the standard EN 61140 [318], which specifies a maximum ground current of 5 mA (rms), is given. A delay compensation, as proposed in Sections 3.3.2 for the control of the output as well as input stages, could not lower the rms value of i_{gnd} and is therefore omitted.

4.2.3 Summary

For a simultaneously grounded mains star-point and load, the zero-sequence voltage $v_{0,cm}$ generated by the input stage and the output stage's neutral leg voltage $v_{N,out}$ (cf. Fig. 4.6) may drive an undesired ground current i_{gnd} flowing through the CVS module and returning over earth, especially at low frequencies including DC, if not properly adjusted. i_{gnd}, i.e. the sum of the input phase currents of the CVS, is not related to the power transfer, and leads to a higher current stress

of the components, potentially to a distortion of the sinusoidal shape of the mains currents and could cause saturation of the inductive elements of the filter stages, especially of the CM chokes.

Thus, in this section a ground current control scheme for the CVS is presented, which employs $v_{0,\mathrm{cm}}$ as actuating voltage to keep i_{gnd} close to zero and which sets $v_{\mathrm{N,ref}} = 0$. The output voltage of the neutral leg is not employed to increase / maximize the load voltage range for the following reason: To achieve $i_{\mathrm{gnd}} \approx 0$, the resulting exciting zero-sequence voltage in the ground loop should be close to zero as well. Because $v_{0,\mathrm{cm}}$ and $v_{\mathrm{N,out}}$ are the only two sources in this loop, $\langle v_{0,\mathrm{cm}} \rangle_{T_{\mathrm{s,in}}} \approx v_{0,\mathrm{cm,set}}$ would need to compensate for $v_{\mathrm{N,out}}$, i.e. $v_{0,\mathrm{cm,set}} \approx v_{\mathrm{N,out}}$. This then may lead to bridge-leg input voltages which are higher than the ones which can be generated for a given DC link voltage. Accordingly, the DC link voltage would need to be increased, which already increases the range of the load voltages. This annuls the benefits gained by using $v_{\mathrm{N,out}}$ to maximize the load voltage range.

To achieve sufficient damping with the control scheme, the outer ground current control loop is extended by an inner capacitor current feedback loop for the current through the first (internal) CM capacitor of the EMI input filter. With this scheme the remaining simulated i_{gnd} for a single 10 kW module is limited to 4.4 mA (rms), what is lower than the value of 5 mA (rms) specified in EN 61140 [318]. This low value of 4.4 mA is mainly due to the high gain k_{g} of the capacitor current feedback loop ($k_{\mathrm{g}} = 20\ \mathrm{V/A}$). It is noted that the feedback-quantity $k_{\mathrm{g}} \cdot i_{\mathrm{cm},1} = k_{\mathrm{g}} \cdot C_{\mathrm{cm},1} \cdot \mathrm{d}v_{\mathrm{C,cm},1}/\mathrm{d}t$, where $v_{\mathrm{C,cm},1}$ is the voltage across $C_{\mathrm{cm},1}$, is a derivative component of $v_{\mathrm{C,cm},1}$ with gain $k_{\mathrm{g}} \cdot C_{\mathrm{cm},1}$.

The main scientific contributions of this section are partially published in [333, 334] (see also “List of Publications” on page 337).

4.3 Integrated Isolation and Voltage Balancing Link

The previous section explains the ground current control scheme to adjust i_{gnd} to zero for grounded mains star-point and load. i_{gnd} can also be eliminated by inserting a high-frequency transformer into the DC link, resulting in a galvanically isolated DC–DC converter (cf. **Fig. 4.9**). The alternative isolation option, to insert a 50 Hz line-frequency transformer between the mains and the rectifier stage [335], is typically discarded as it would significantly increase the size and the weight of the system [336].

As mentioned in the introduction to this chapter, the AC source is also used to power DC loads. For example, a grounded resistive DC load connected between phase A and the (earthed) neutral leg N (cf. Fig. 4.1), which requires a positive voltage, takes its energy only from the upper DC link capacitor $C_{\mathrm{dc,3}}$ (cf. Fig. 4.9). The output voltage of the neutral leg, $v_{\mathrm{N,out}}$, is controlled to zero, as explained in the previous section, and hence the output terminal N and the DC link midpoint m can be regarded as shorted for DC and low frequencies.

The mentioned continuously unequal loading of $C_{\mathrm{dc,3}}$ and $C_{\mathrm{dc,4}}$ leads to DC link voltages $V_{\mathrm{dc,3}}$ and $V_{\mathrm{dc,4}}$ that would drift apart over time. One solution to avoid this voltage difference and to ensure balanced DC link voltages $V_{\mathrm{dc,3}}$ and $V_{\mathrm{dc,4}}$ in all operating points complying to the specifications given in Tab. 1.1 and for all loads enumerated on page 2, is proposed in Section 4.1, where a balancer circuit, as depicted in Fig. 4.3(a) is employed. Balanced rectifier-side DC link voltages $V_{\mathrm{dc,1}}$ and $V_{\mathrm{dc,2}}$ can then be achieved with proper control of the rectifier stage, consisting of a three-level T-type converter which allows controlling the neutral-point potential [337–339].

Another solution, which is elaborated in this section, is to integrate the balancer circuit into the galvanically isolated DC–DC converter. This option is explained in the following with the help of a SRC [322–324, 327, 330], with resonant elements C_{res} and L_{res}, shown in Fig. 4.9. In this topology, on the primary side, one terminal of the transformer is connected through the resonant capacitor and inductor to the primary-side bridge-leg output and the other terminal is connected to the DC link midpoint. On the secondary side, both terminals directly connect to the secondary-side bridge-leg input and the DC link midpoint, respectively. The system is operated in a half-cycle

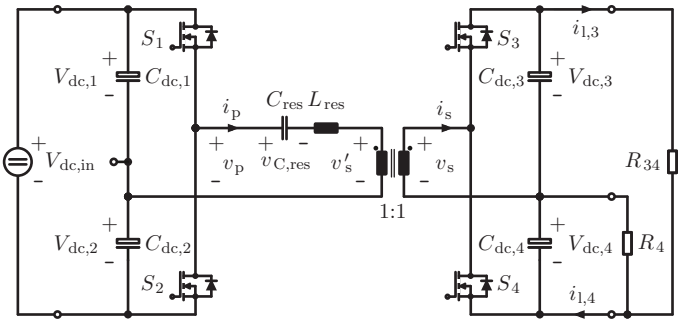


Figure 4.9: Proposed DC–DC converter to achieve a galvanic isolation and a DC link voltage balancing for split DC links. A series resonant converter (SRC) topology with only two active half-bridges is employed to reduce the number of power semiconductors and gate drive units. Illustratively, for representing an asymmetric load condition, the lower DC link capacitor $C_{\mathrm{dc},4}$ is additionally loaded by R_4. It is assumed that the voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ are balanced by the rectifier stage [337–339].

Table 4.4: Electrical specifications of the galvanically isolated DC–DC converter given in Fig. 4.9 interconnecting the input and output stages of a 10 kW CVS module.

Nominal power, P_{n}	10 kW
Nominal DC link voltage, $V_{\mathrm{dc,n}}$	700 V
Rectifier stage switching (carrier) frequency, $f_{\mathrm{s,in}}$	48 kHz
DC–DC converter switching frequency, f_{s}	20 kHz
Inverter stage switching (carrier) frequency, $f_{\mathrm{s,out}}$	48 kHz

discontinuous-conduction mode as further explained in Section 4.3.1 and features the specifications given in **Tab. 4.4**. The concept of the integration of galvanic isolation and DC link voltage balancing into a single DC–DC converter is not restricted to SRCs and can also be applied to Dual Active Bridge Converters (DABCs) [325–327, 329]. However, the SRC is preferred because of its simpler operation principle compared to the DABC.

The load and the inverter stage are in Fig. 4.9 represented by R_{34} and R_4 such that the same power flow through the DC–DC converter

occurs as if the inverter stage supplying an asymmetric load would be connected. The possible unequal average loading of the DC link capacitors $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$ is represented by the additional resistor R_4. The resistor R_{34} loads both capacitors $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$ equally.

For this unequal average loading of the DC link capacitors $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$, the average values of the load currents $i_{\mathrm{l},3}$ and $i_{\mathrm{l},4}$ are different and the high-frequency transformer establishes a magnetizing current which is in average equal to the average of $i_{\mathrm{l},4} - i_{\mathrm{l},3}$ as further elaborated in Section 4.3.1. Thus, the transformer must be realized with an air-gap and integrates the galvanic isolation and DC link voltage balancing.

For the DC–DC converter depicted in Fig. 4.9, two-level half-bridges instead of three-level T-type bridge-legs, as used for the rectifier and the inverter stages, are employed to reduce the number of power semiconductors and gate drive units.[4] Due to the SRC operation the switching losses can be kept low.

Section 4.3.1 analyzes in detail the operation of the proposed SRC for unequal loading of $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$. The design guidelines for a 1 kW proof-of-concept SRC prototype are presented in Section 4.3.2. The theoretical analysis of the converter is supported by measurements in Section 4.3.3, and Section 4.3.4 concludes this part.

A high bandwidth AC source is the targeted application of the analyzed DC–DC converter shown in Fig. 4.9. However, the isolated DC–DC converter could also be used for mobile systems such as trains [340], electric cars [340, 341], and aerospace applications [326].

4.3.1 HCDCM Operation Principle of the SRC with Half-Bridges and Unequal Loading

The operation principle of a SRC operated in Half-Cycle Discontinuous-Conduction Mode (HCDCM) with a half-bridge at the input and a full-bridge at the output, i.e. without the proposed DC link balancing feature, is investigated in [330]. To analyze the proposed system, in a first step, a symmetrical loading of the inverter-side DC link capacitors is assumed, i.e. $R_4 \to \infty$ in Fig. 4.9. Moreover, the magnetizing current and the transformer stray inductance are neglected ($L_\mu \to \infty$). With these assumptions, the primary and the secondary currents are identical for a transformer turns ratio of 1:1. The voltage source $V_{\mathrm{dc,in}}$ depicted

[4] The operation principle of a SRC with three-level T-type bridge-legs is analogous to the one presented in this section.

in Fig. 4.9 represents the DC link voltage controlled rectifier stage; the partial rectifier-side DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ are balanced by the three-level T-type rectifier stage.

For a power flow from the rectifier to the inverter stage, the primary-side bridge-leg with switches S_1 and S_2 (cf. Fig. 4.9) is actively switched with a duty-cycle δ of 50% (including the interlocking time). The gate signals for S_1 and S_2 are phase-shifted by 180°. This leads to the primary voltage v_{p} depicted in **Fig. 4.10(a)** over two switching periods $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$. Because of the switching, a resonant current pulse is generated. The positive resonant pulse is denoted by $i_{\mathrm{s,pp}}$ and charges the upper DC link capacitor $C_{\mathrm{dc},3}$; the negative pulse is denoted by $i_{\mathrm{s,np}}$ and charges the lower DC link capacitor $C_{\mathrm{dc},4}$. These pulses are shown in Fig. 4.10(a) and are defined as

$$i_{\mathrm{s,pp}} = \begin{cases} i_{\mathrm{s}} & \text{if } i_{\mathrm{s}} \geq 0 \\ 0 & \text{else} \end{cases} \quad \text{and} \quad i_{\mathrm{s,np}} = \begin{cases} i_{\mathrm{s}} & \text{if } i_{\mathrm{s}} \leq 0 \\ 0 & \text{else} \end{cases} . \tag{4.9}$$

On the secondary side, the switches S_3 and S_4 are not operated or operated with synchronous rectification, i.e. the secondary-side bridge-leg acts as a diode rectifier. In HCDCM, the resonant current pulses reach zero before a new current pulse is excited, i.e. $t_{\mathrm{psz}} \leq T_{\mathrm{s}}/2$ [cf. Fig. 4.10(a)], and hence the SRC is operated below the resonant frequency $f_{\mathrm{res}} = 1/\left(2 \cdot \pi \cdot \sqrt{L_{\mathrm{res}} \cdot C_{\mathrm{res}}}\right)$. Because of the diode rectification, once the current pulses reach zero after t_{psz}, the diodes avoid that the currents reverse direction. The secondary current remains zero until a new current pulse is excited.

The primary voltage v_{p}, the secondary voltage v_{s}, and the secondary current i_{s} are depicted in **Fig. 4.10(b)** for a finite magnetizing inductance (see the equivalent circuit of the transformer referred to the primary side as depicted in **Fig. 4.11**) and for an unequal loading of $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$. In steady-state, the average values of $i_{\mathrm{s,pp}}$ and $i_{\mathrm{s,np}}$ over T_{s} are equal to the positive average load current $i_{\mathrm{l},3,\mathrm{avg}}$ of $C_{\mathrm{dc},3}$ and the negative average load current $i_{\mathrm{l},4,\mathrm{avg}}$ of $C_{\mathrm{dc},4}$ over the same period respectively. Thus,

$$i_{\mathrm{s,pp,avg}} = i_{\mathrm{l},3,\mathrm{avg}}, \quad i_{\mathrm{s,np,avg}} = -i_{\mathrm{l},4,\mathrm{avg}} \tag{4.10}$$

and accordingly the average of the secondary current $i_{\mathrm{s,avg}}$ over T_{s} is given by (discontinuous-conduction-mode)

$$i_{\mathrm{s,avg}} = i_{\mathrm{s,pp,avg}} + i_{\mathrm{s,np,avg}} = i_{\mathrm{l},3,\mathrm{avg}} - i_{\mathrm{l},4,\mathrm{avg}}. \tag{4.11}$$

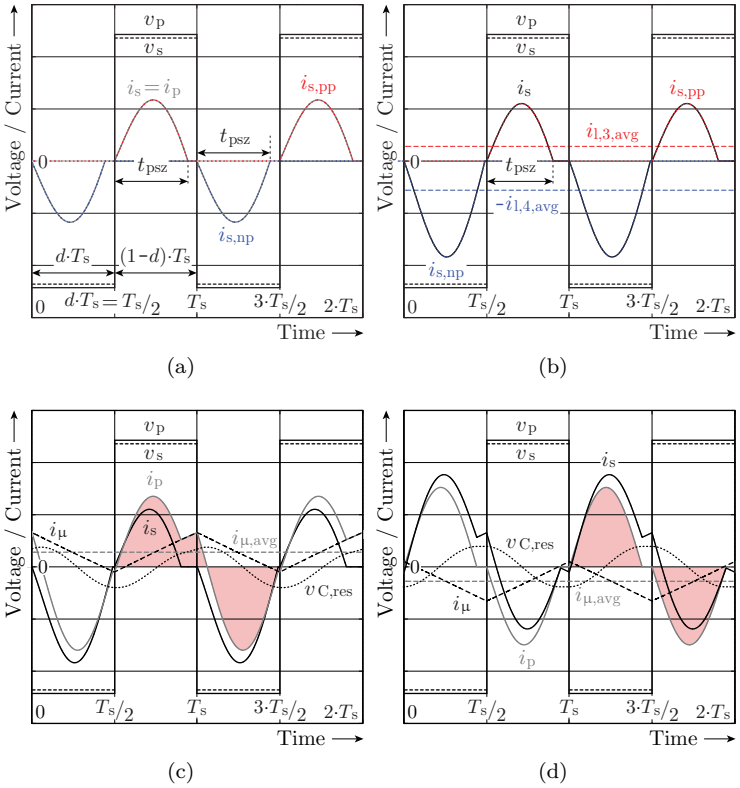


Figure 4.10: **(a)** Exemplary primary voltage v_p, secondary voltage v_s, primary current i_p, and secondary current i_s of the SRC given in Fig. 4.9 for $L_\mu \to \infty$ and equal average load currents $i_{\mathrm{l},3,\mathrm{avg}} = i_{\mathrm{l},4,\mathrm{avg}}$; **(b)** v_p, v_s, and i_s and **(c)** additionally i_p, resonant capacitor voltage $v_{\mathrm{C,res}}$, and magnetizing current i_μ for a finite magnetizing inductance L_μ and an unequal *loading* of the inverter-side DC link capacitors. **(d)** Exemplary v_p, v_s, i_p, i_s, $v_{\mathrm{C,res}}$, and i_μ for an unequal power *fed* into the inverter-side DC link capacitors. The red shaded areas for the positive and negative current pulses of i_p are equal in (c) as well as in (d), from which it is directly deduced that $i_{\mathrm{p,avg}} = 0$, i.e. zero average current through C_res. T_s denotes the switching period.

Because in the following the average values of the currents and voltages

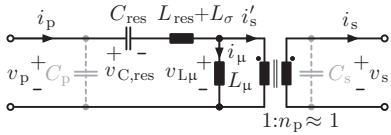


Figure 4.11: Equivalent circuit of the resonant components and the high-frequency transformer referred to the primary side.

of the SRC are always taken over one switching period T_s, the interval in time over which the averages are calculated is not explicitly mentioned anymore.

For the case shown in Fig. 4.10(b), $i_\mathrm{l,4,avg}$ is larger than $i_\mathrm{l,3,avg}$ and accordingly $i_\mathrm{s,avg}$ is negative [cf. (4.11)]. On the primary side, the average of the primary current i_p is zero in steady-state; otherwise, C_res would be continuously charged or discharged:

$$i_\mathrm{p,avg} = i_\mathrm{\mu,avg} + i'_\mathrm{s,avg} = 0. \tag{4.12}$$

It is at this point explicitly emphasized that C_res forces $i_\mathrm{p,avg} = 0$. This means that an average magnetizing current $i_\mathrm{\mu,avg}$ flows which compensates the average value of the secondary current i_s, and hence results as

$$i_\mathrm{\mu,avg} = -i'_\mathrm{s,avg} = i'_\mathrm{l,4,avg} - i'_\mathrm{l,3,avg}, \tag{4.13}$$

as depicted in **Fig. 4.10(c)**. In the above equation the secondary-side load currents are transformed to the primary side and accordingly assigned by a " ′ ". This notation is used throughout the rest of this section.

In steady-state, the average voltage

$$v_\mathrm{L\mu} = \frac{L_\mu}{L_\mu + L_\sigma + L_\mathrm{res}} \cdot \begin{cases} V_\mathrm{dc,1} - v_\mathrm{C,res} & 0 \le t < \frac{T_\mathrm{s}}{2} \\ -V_\mathrm{dc,2} - v_\mathrm{C,res} & \frac{T_\mathrm{s}}{2} \le t < T_\mathrm{s} \end{cases}, \tag{4.14}$$

applied to the transformer magnetizing inductance L_μ [cf. Fig. 4.11] is because of (4.12) also zero.

Thus, the DC link voltage balancing is achieved by the average magnetizing current $i_\mathrm{\mu,avg}$ and accordingly the magnetizing inductance of the high-frequency transformer takes over the functionality of the balancer inductance shown in Fig. 4.3(a). The SRC therefore integrates the DC link voltage balancing and the galvanic isolation. In the case at

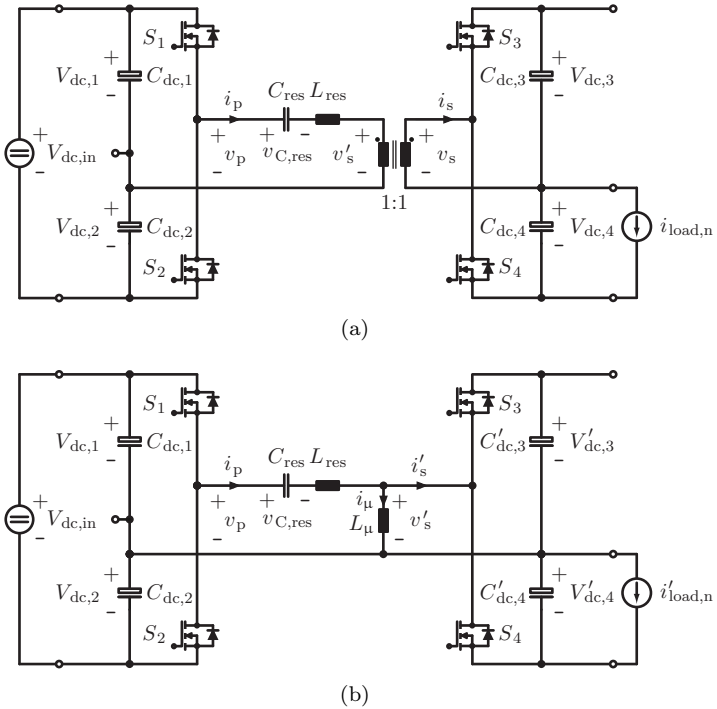
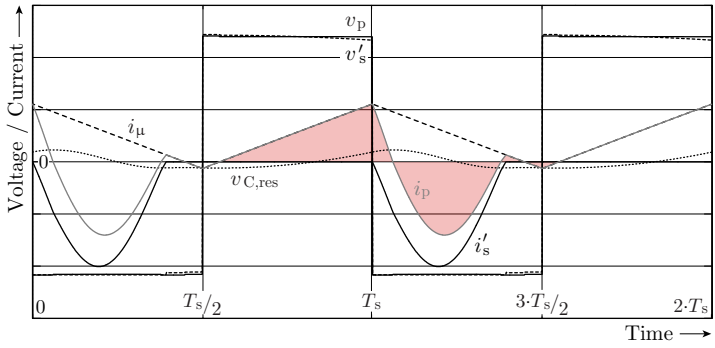


Figure 4.12: (a) SRC for a loading of only $C_{dc,4}$ with a constant current $i_{load,n}$, **(b)** simplified equivalent circuit of (a), where the transformer is represented by its magnetizing inductance L_μ, and **(c)** exemplary waveforms of v_p, v'_s, i_p, i'_s, i_μ, and $v_{C,res}$ ($i_{p,avg} = 0$ as indicated by the red shaded areas).

hand, no voltage step-down or step-up is required, thus, a transformer turns ratio of 1:1 is employed.

Because of the average magnetizing current $i_{\mu,avg} \neq 0$, the transformer needs to store energy and accordingly is preferably built with a low-permeability material or with a discrete air-gap. Alternatively, an inductor could be placed in parallel to the transformer primary or secondary winding which would take over a large part of the magnetizing current [cf. (4.13)], otherwise completely flowing through the transformer.

In steady-state, the capacitor C_{res} ensures that the primary current



(c)

Fig. 4.12: Continued.

is in average zero, i.e. $i_{p,avg} = 0$. In the case that only the lower inverter-side DC link capacitor $C_{dc,4}$ is loaded by a constant current $i_{load,n}$ as shown in **Fig. 4.12(a)**, respective **Fig. 4.12(b)**, the waveform of i_p is depicted in **Fig. 4.12(c)**. The positive and negative red shaded areas for i_p over one switching period compensate each other, i.e. $i_{p,avg} = 0$ with the help of C_{res} as explained in the following. If for instance $i_{p,avg} < 0$ (as it would be the case in Fig. 4.12(c) without i_μ), C_{res} would be discharged in average leading to $v_{C,res,avg} < 0$ and accordingly $v'_{s,avg} = -v_{C,res,avg} > 0$ [cf. Fig. 4.12(b)]. $v'_{s,avg} > 0$ applied to L_μ leads to an average magnetizing current which would increase ($i_{\mu,avg} > 0$). Once $i_{p,avg} = 0$ is reached, $i_{\mu,avg}$ continues to rise because of $v_{C,res,avg} < 0$ still being negative. Accordingly, i_μ and $v_{C,res}$ reach their steady-state values in an oscillatory manner (energy exchange between L_μ [$L_\mu \gg L_\sigma$ and L_{res}] and C_{res} with reduced amplitude of the oscillations over time due to the resistive parts in the circuit) leading finally to $i_{\mu,avg} = i_{load,n} > 0$ and $v_{C,res,avg} = 0$ for ideal switching, i.e. $v_{p,avg} = 0$ [cf. Fig. 4.12(c)]. Thus, the average rectifier-side DC link voltages $V_{dc,1,avg}$ and $V_{dc,2,avg}$ are due to the magnetizing current forced by C_{res} equally loaded in average.

From the above explanations is becomes clear that in case $L_\mu \to \infty$ (i.e. SRC without voltage balancing feature) no magnetizing current can be established, i.e. $i_\mu = 0$, leading to a continuous negative average of i_p which would discharge C_{res} until $v_{C,res} = -V_{dc,2} = -V_{dc,in}/2$ and

$V'_{\mathrm{dc},4} = 0$ ($V'_{\mathrm{dc},3} = V_{\mathrm{dc,in}}$).

It is noted that the SRC with DC link voltage balancing capabilities (cf. Fig. 4.9) always loads the rectifier side DC link capacitors $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$ equally. However, because of the capacitive coupling of the rectifier-side bridge-leg output to the transformer through C_{res}, no average balancing current can be provided and hence the resonance converter cannot guarantee fully balanced DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$. Accordingly, $V_{\mathrm{dc},1,\mathrm{avg}} = V_{\mathrm{dc},2,\mathrm{avg}}$ has to be ensured by the rectifier stage.

Based on the more detailed analysis carried out in Section 4.3.2, it is observed that the higher the load currents the lower the average inverter-side DC link voltages for fixed rectifier-side DC link voltages. The reason is that the average values of the resonant current pulses [cf. (4.9)] increase with the higher load currents. Accordingly, to generate resonant pulses with higher average values, larger voltage excitations are required [330] meaning lower average inverter-side DC link voltages. Thus, for unequal load currents $i_{\mathrm{l},3}$ and $i_{\mathrm{l},4}$, different average DC link voltages $V_{\mathrm{dc},3,\mathrm{avg}}$ and $V_{\mathrm{dc},4,\mathrm{avg}}$ result.

Ideally, i.e. without including the parasitic capacitances C_{p} and C_{s} [cf. Fig. 4.11] between the bridge-leg outputs and the corresponding midpoints, the largest average inverter-side DC link voltage difference is reached for $i_{\mathrm{l},3,\mathrm{avg}} \neq 0$ and $i_{\mathrm{l},4,\mathrm{avg}} = 0$ or vice versa. Including the mentioned capacitances, an oscillatory charge reversal of these capacitances occurs during a switching transient. If during the transient the voltage across C_{s} is in absolute value larger than the DC link voltage $V_{\mathrm{dc},3}$ or $V_{\mathrm{dc},4}$ plus the diode forward voltage drop v_{df}, the DC link capacitor $C_{\mathrm{dc},3}$ or $C_{\mathrm{dc},4}$ is slightly charged. Thus, $C_{\mathrm{dc},3}$ or $C_{\mathrm{dc},4}$ charges to the value of the transient peak voltage across C_{s} minus v_{df}. This problem can be diminished by placing symmetrizing resistors across all DC link capacitors, which are loading the capacitors just enough to compensate the slight charging. As demonstrated by measurements (cf. Section 4.3.3), symmetrizing resistors of 22 kΩ could be employed for the 1 kW prototype. Theses resistors are increasing the losses by about 1 W.

Another way to go around the issue is to actively switch the secondary-side bridge-leg in-phase with the primary-side bridge-leg, which would however generate additional losses. In case only a unidirectional power flow from the rectifier to the inverter stage is required, the secondary-side bridge-leg can be realized with only diodes, but in

this case symmetrizing resistors are necessary to avoid excessive voltages $V_{\mathrm{dc},3}$ and $V_{\mathrm{dc},4}$ at no and / or low load (due to the behavior of the circuit explained in the paragraph above).

It is noted that a further option to achieve $V_{\mathrm{dc},3,\mathrm{avg}} = V_{\mathrm{dc},4,\mathrm{avg}}$ would be to control the duty-cycle δ of the switches of the primary-side bridge-leg [cf. Fig. 4.10(a)], which would allow equalizing the inverter-side DC link voltages $V_{\mathrm{dc},3}$ and $V_{\mathrm{dc},4}$ (in average). For the case shown in Fig. 4.10(c), where $C_{\mathrm{dc},4}$ is loaded more than $C_{\mathrm{dc},3}$, i.e. $V_{\mathrm{dc},3}$ is higher than $V_{\mathrm{dc},4}$, the control unit sets a duty-cycle of $\delta = 0.5 + \Delta\delta$ ($\Delta\delta > 0$) which leads, over one switching period, to an average value $v_{\mathrm{p,avg}} = \Delta\delta \cdot V_{\mathrm{dc,in}}$ of the primary voltage v_{p} (assuming $V_{\mathrm{dc},1} = V_{\mathrm{dc},2} = V_{\mathrm{dc,in}}/2$). Because the resonance capacitor charges in average to $v_{\mathrm{p,avg}}$, i.e. $v_{\mathrm{C,res,avg}} = v_{\mathrm{p,avg}}$, the excitation voltages $v_{\mathrm{exc,pos}}$ and $v_{\mathrm{exc,neg}}$ for the positive and negative current pulses are affected, which are given by [cf. Fig. 4.10(c)]

$$\begin{aligned} v_{\mathrm{exc,pos}} &= V_{\mathrm{dc},10} - (v_{\mathrm{C,res,avg}} - v_{\mathrm{C,res0,pos}}) - V_{\mathrm{dc},30} \\ &= V_{\mathrm{dc},10} + v_{\mathrm{C,res0,pos}} - v_{\mathrm{p,avg}} - V_{\mathrm{dc},30} > 0, \\ v_{\mathrm{exc,neg}} &= V_{\mathrm{dc},20} + (v_{\mathrm{C,res,avg}} + v_{\mathrm{C,res0,neg}}) - V_{\mathrm{dc},40} \\ &= V_{\mathrm{dc},20} + v_{\mathrm{C,res0,neg}} + v_{\mathrm{p,avg}} - V_{\mathrm{dc},40} > 0. \end{aligned} \tag{4.15}$$

According to (4.15), the positive value of $v_{\mathrm{p,avg}} > 0$ reduces $v_{\mathrm{exc,pos}}$ and increases $v_{\mathrm{exc,neg}}$, which leads momentarily to positive and negative current pulses with lower and higher absolute average values, respectively. This discharges $V_{\mathrm{dc},3}$ and charges $V_{\mathrm{dc},4}$ until a new steady-state operating point with $V_{\mathrm{dc},3,\mathrm{avg}} = V_{\mathrm{dc},4,\mathrm{avg}}$ is reached.[5]

It is important to note that the resonant capacitor C_{res} needs to be placed on the side of the transformer where the DC link capacitors are equally loaded, i.e. the rectifier side for the case at hand where, ideally, a perfect DC link voltage balancing can be achieved. On the inverter side, the DC link voltages $V_{\mathrm{dc},3}$ and $V_{\mathrm{dc},4}$ are in average different from each other. However, because large resonant current pulses can be generated with a small excitation voltage, the voltage difference between $V_{\mathrm{dc},3,\mathrm{avg}}$ and $V_{\mathrm{dc},4,\mathrm{avg}}$ is for example at maximum 10% of $(V_{\mathrm{dc},3,\mathrm{avg}} + V_{\mathrm{dc},4,\mathrm{avg}})/2$ for the built proof-of-concept converter (cf. Section 4.3.3).

For feeding power back from the inverter to the rectifier side, the secondary-side bridge-leg is switched, impressing the voltage between

[5] It is remarked that the difference between $V_{\mathrm{dc},1,\mathrm{avg}} = V_{\mathrm{dc},2,\mathrm{avg}}$ and $V_{\mathrm{dc},3,\mathrm{avg}} = V_{\mathrm{dc},4,\mathrm{avg}}$ depends on the loading of $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$ on the inverter side. If necessary, the voltages $V_{\mathrm{dc},3,\mathrm{avg}}$ and $V_{\mathrm{dc},4,\mathrm{avg}}$ can be boosted by slightly increasing the turns ratio of the high-frequency transformer.

the secondary transformer terminals, and the primary-side bridge-leg is operated as a diode rectifier. The magnetizing inductance of the transformer directly acts again like a balancer inductor leading to a magnetizing current i_μ flowing on the secondary side, which balances the DC link voltage $V_{\mathrm{dc},3}$ and $V_{\mathrm{dc},4}$. Illustratively, the primary and secondary voltages as well as the primary and secondary currents are depicted in **Fig. 4.10(d)** for this case.

4.3.2 Design Guidelines for the SRC with Unequal Loading

The resonant current pulses [cf. Fig. 4.10(b)] are computed analytically in this subsection to provide physical insight into the operating behavior of the SRC depicted in Fig. 4.9. For the sake of brevity, the subsequent equations are shown for the positive current pulse $i_{\mathrm{s,pp}}$ of the secondary current [cf. Fig. 4.10(a)] and for a power flow from the rectifier to the inverter stage. The negative current pulse can be computed analogously. By superimposing the magnetizing current i_μ and the secondary current i'_s, the primary current i_p is obtained. The average of i_μ is given by the average difference between the load currents $i_{\mathrm{l,3,avg}}$ and $i_{\mathrm{l,4,avg}}$; the peak-to-peak current ripple of i_μ can be assessed using (4.14) while setting $V_{\mathrm{dc},1}(t) = V_{\mathrm{dc},2}(t) = V_{\mathrm{dc,in}}/2$ and neglecting $v_{\mathrm{C,res}}(t)$ considering $V_{\mathrm{dc,in}}/2 \gg v_{\mathrm{C,res}}(t)\ \forall\ t$.

As described in the last subsection, the SRC depicted in Fig. 4.9 differs from standard SRC (cf. [330] for example) by its much lower magnetizing inductance. Thus, the magnetizing inductance needs to be included into the modeling of the converter. Based on the approach explained in [330], the equivalent circuit in the frequency domain depicted in **Fig. 4.13** can be employed to compute the secondary current $I'_\mathrm{s}(s)$. Adding the magnetizing inductance in the modeling enforces to set an initial condition on the magnetizing current, i.e. $I_{\mathrm{L}\mu 0}$, and thus also on the primary current.

In the frequency domain, the current $I'_\mathrm{s}(s)$ can be computed using nodal and mesh equations. Transforming $I'_\mathrm{s}(s)$ into the time domain and assuming a constant load current, $I_{\mathrm{l},3} = \text{const.}$, leads to

$$\begin{aligned} i'_\mathrm{s}(t) = \quad & I'_{\mathrm{l},3} + \\ & I_{\mathrm{s},1} \cdot \sin(\omega_1 \cdot t) + I_{\mathrm{c},1} \cdot \cos(\omega_1 \cdot t) + \\ & I_{\mathrm{s},2} \cdot \sin(\omega_2 \cdot t) + I_{\mathrm{c},2} \cdot \cos(\omega_2 \cdot t)\,. \end{aligned} \tag{4.16}$$

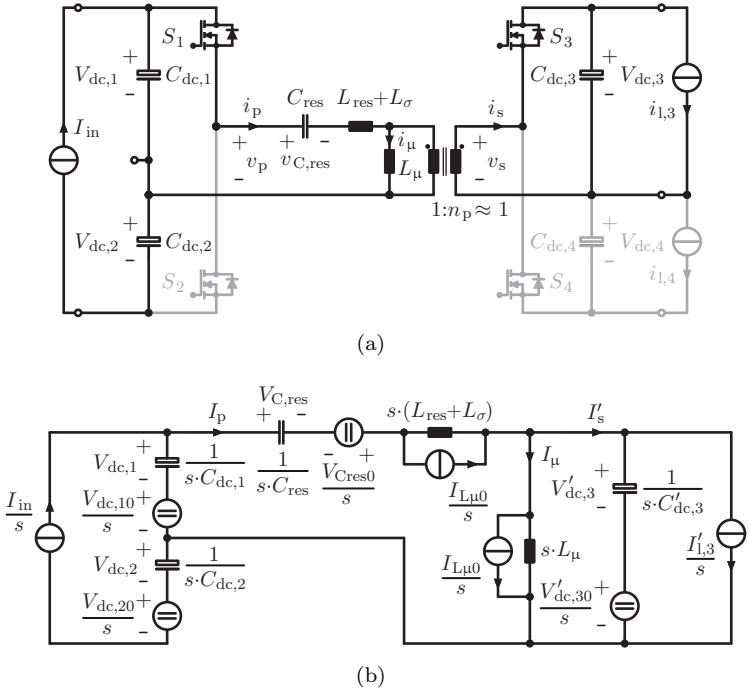


Figure 4.13: (a) Equivalent circuit employed for the theoretical analysis of the SRC of Fig. 4.9 for a positive resonant current pulse [cf. Fig. 4.10(b)], and **(b)** resulting equivalent circuit in the frequency domain based on the approach described in [330]. The equivalent circuits are only valid for $0 \leq t \leq t_{\mathrm{psz}}$ [cf. Fig. 4.10(b)]. The constant voltage and current sources in (b) result from the initial conditions (especially $I_{\mathrm{L}\mu 0} \neq 0$), which are marked with an additional "0". The input current $I_{\mathrm{in}} = P_{\mathrm{in}}/V_{\mathrm{dc,in}}$ and the load current $I_{\mathrm{l},3}$ are assumed to be constant.

In the above equation the two angular frequencies depend only on the circuit parameters and are with the simplification of $C_{\mathrm{dc},1} = C_{\mathrm{dc},2}$ given by

$$\begin{aligned} \omega_1 &= \sqrt{\frac{1}{2\cdot C_{1\mathrm{res}}\cdot L_{\sigma\mathrm{res}}} + \frac{L_{\sigma\mathrm{res}}+L_{\mu}-\tilde{L}}{2\cdot C'_{dc,3}\cdot L_{\sigma\mathrm{res}}\cdot L_{\mu}}}, \\ \omega_2 &= \sqrt{\frac{1}{2\cdot C_{1\mathrm{res}}\cdot L_{\sigma\mathrm{res}}} + \frac{L_{\sigma\mathrm{res}}+L_{\mu}+\tilde{L}}{2\cdot C'_{dc,3}\cdot L_{\sigma\mathrm{res}}\cdot L_{\mu}}}, \end{aligned} \tag{4.17}$$

where $L_{\sigma\mathrm{res}} = L_\sigma + L_\mathrm{res}$, $C_\mathrm{1res} = C_\mathrm{dc,1} \cdot C_\mathrm{res}/(C_\mathrm{dc,1} + C_\mathrm{res})$ and

$$\tilde{L} = \sqrt{L_{\sigma\mathrm{res}}^2 - 2 \cdot \tilde{C}_\mathrm{f1} \cdot L_{\sigma\mathrm{res}} \cdot L_\mu + \tilde{C}_\mathrm{f2}^2 \cdot L_\mu^2} \tag{4.18}$$

with the scaling factors

$$\begin{aligned} \tilde{C}_\mathrm{f1} &= \frac{C_\mathrm{dc,1} \cdot (C'_\mathrm{dc,3} - C_\mathrm{res}) + C'_\mathrm{dc,3} \cdot C_\mathrm{res}}{C_\mathrm{dc,1} \cdot C_\mathrm{res}} \text{ and} \\ \tilde{C}_\mathrm{f2} &= \frac{C_\mathrm{dc,1} \cdot (C'_\mathrm{dc,3} + C_\mathrm{res}) + C'_\mathrm{dc,3} \cdot C_\mathrm{res}}{C_1 \cdot C_\mathrm{res}}. \end{aligned} \tag{4.19}$$

The coefficients $I_\mathrm{s,1}$, $I_\mathrm{c,1}$, $I_\mathrm{s,2}$ and $I_\mathrm{c,2}$ are a function of the initial conditions:

$$\begin{aligned} I_{\mathrm{s},k} &= \frac{C'_\mathrm{dc,3} \cdot \left(\frac{V'_\mathrm{dc,30}}{C_\mathrm{1res}} + \left(L_\mu \cdot v_\mathrm{dc,p} - (L_{\sigma\mathrm{res}} + L_\mu) \cdot V'_\mathrm{dc,30} \right) \cdot \omega_k^2 \right)}{2 \cdot L_{\sigma\mathrm{res}} \cdot L_\mu \cdot C'_\mathrm{dc,3} \cdot \omega_k^3 - \left(L_{\sigma\mathrm{res}} + L_\mu \cdot \tilde{C}_\mathrm{f2} \right) \cdot \omega_k}, \\ I_{\mathrm{c},k} &= \frac{L_\mu \cdot \left(\frac{C_\mathrm{dc,1}}{C_\mathrm{res}} \cdot \left(i'_\mathrm{l,3} + i_{\mathrm{L}\mu 0} \right) + \left(i'_\mathrm{l,3} \cdot \left(1 - C_\mathrm{dc,1} \cdot L_{\sigma\mathrm{res}} \cdot \omega_k^2 \right) - \Delta i_\mathrm{in} \right) \right)}{\frac{C_\mathrm{dc,1}}{C'_\mathrm{dc,3}} \cdot \left(2 \cdot L_{\sigma\mathrm{res}} \cdot L_\mu \cdot C'_\mathrm{dc,3} \cdot \omega_k^2 - \left(L_{\sigma\mathrm{res}} + L_\mu \cdot \tilde{C}_\mathrm{f2} \right) \right)}, \end{aligned} \tag{4.20}$$

where $k = 1, 2$, $v_\mathrm{dc,p} = v_\mathrm{Cres0} + V_\mathrm{dc,10}$ and $\Delta i_\mathrm{in} = I_\mathrm{in} - i_{\mathrm{L}\mu 0}$. $I_{\mathrm{s},k}$ depends only on the initial conditions of the voltages and $I_{\mathrm{c},k}$ only on the initial conditions of the currents. Moreover, it is noted that the resonant current pulses contain two frequency components. For the built hardware (cf. Section 4.3.3), the frequencies are $f_1 = \omega_1/(2 \cdot \pi) \approx 1$ kHz and $f_2 = \omega_2/(2 \cdot \pi) \approx 24$ kHz. Furthermore, $i'_\mathrm{l,3} + I_\mathrm{c,1} + I_\mathrm{c,2} = 0$ follows directly from the fact that the current on the secondary side cannot reverse direction after a current pulse because of the secondary-side diodes. Moreover, (4.16) can be simplified to

$$i'_\mathrm{s}(t) = I'_\mathrm{l,3} + I_1 \cdot \sin(\omega_1 \cdot t + \phi_1) + I_2 \cdot \sin(\omega_2 \cdot t + \phi_2) \tag{4.21}$$

with $I_k = \sqrt{I_{\mathrm{s},k}^2 + I_{\mathrm{c},k}^2}$ and $\phi_k = \mathrm{atan2}(I_{\mathrm{c},k}, I_{\mathrm{s},k})$.

The time interval t_psz [cf. Fig. 4.10(b), exemplary shown for the positive resonant current pulse $i_\mathrm{s,pp}$] and defined by the time difference between the beginning of the resonant pulse and the point in time when the secondary current $i_\mathrm{s}(t)$ reaches zero can be computed numerically by equating (4.21) to zero. t_psz increases with the load current $i_\mathrm{l,3}$. Thus, the resonant elements C_res and $L_{\sigma\mathrm{res}}$ can be selected such that for the chosen switching frequency and for the maximum load current $i_\mathrm{l,3,max}$ or

$i_{\mathrm{l,4,max}}$ (i.e. for loading only $C_{\mathrm{dc,3}}$ or $C_{\mathrm{dc,4}}$), the resonant current pulses reach zero before a new current pulse is generated, i.e. $t_{\mathrm{psz}} \leq T_{\mathrm{s}}/2$.[6]

In conclusion, a first design of the SRC, which is supported by circuit simulations, can be obtained as follows. To reduce the switching losses, the switching frequency f_{s} can be chosen such that it is just higher than the highest audible frequency. For the prototype (cf. Section 4.3.3), $f_{\mathrm{s}} = 20\,\mathrm{kHz}$ is selected. In a next step, the maximum difference in the load current [cf. (4.13)] needs to be determined, which is given by the application in which the converter is employed. For the built 1 kW hardware, this maximum difference is set to $1\,\mathrm{kW}/3 = 333\,\mathrm{W}$. The capacitances of the DC link capacitors can be determined such that the DC link voltage ripple across one capacitor is limited, e.g. to 2.5% of $V_{\mathrm{dc,in}}/2$.

On the one hand, the larger the value of the transformer's magnetizing inductance the smaller the peak-to-peak ripple of i_{μ} and accordingly the lower the high-frequency copper losses. On the other hand, there is also an advantage in having a reduced magnetizing inductance, especially in case the switches are implemented with MOSFETs. For a power flow from the rectifier to the inverter stage [cf. Fig. 4.10(c)], a good option is, as done for the 1 kW prototype, to choose the magnetizing inductance L_{μ} just large enough that soft-switching (zero-voltage switching) can be achieved at turn-on in all operating points. Therefore, the magnetizing current has to become negative before the positive voltage is applied at the output of the primary-side bridge-leg and vice versa, as exemplary shown in Fig. 4.10(c). Thus, the peak-to-peak magnetizing current ripple $\Delta i_{\mu,\mathrm{pp}}$ needs to be slightly larger than two times the maximum average magnetizing current $i_{\mu,\mathrm{avg,max}}$, i.e.

$$\Delta i_{\mu,\mathrm{pp}} > 2 \cdot \left| i_{\mu,\mathrm{avg,max}} \right| = 2 \cdot \left| i'_{\mathrm{l,3,avg,max}} - i'_{\mathrm{l,4,avg,min}} \right| . \tag{4.22}$$

With the above condition, also soft-switching is obtained in all operating points for an inverse power flow from the inverter to the rectifier stage as exemplary given in Fig. 4.10(d).

To transfer the same amount of energy, the shorter the time t_{psz} the larger the peaks of the resonant current pulses for the same average DC link voltages and switching frequency f_{s}. This increases the primary and secondary rms currents and therefore also the copper losses.

[6] It is noted that the shape of the resonant current pulses and the time t_{psz} depend also on the parasitic resistive parts between one and the other split DC links and symmetrizing resistors connected across the DC link capacitors.

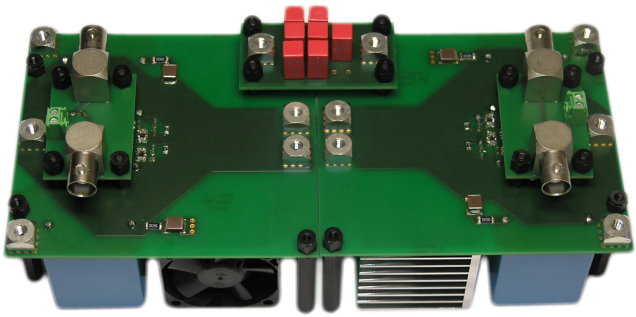


Figure 4.14: 1 kW series resonant converter (SRC) proof-of-concept prototype featuring the specifications given in Tab. 4.5 and employed to verify the theoretical analysis conducted in this part.

Accordingly, $t_{\mathrm{psz}} = T_{\mathrm{s}}/2$ is selected as longest duration of the resonant current pulses. In a next step, the resonant elements can be determined. To achieve a compact converter, L_{res} should be as small as possible. Therefore, $L_{\sigma\mathrm{res}}$ can be realized by only the stray inductance L_{σ} of the high-frequency transformer, i.e. $L_{\sigma\mathrm{res}} = L_{\sigma}$, as it is done for the prototype. L_{σ} is fixed depending on the transformer design and hence C_{res} can be calculated. For a compact realization of the converter, the values of L_{σ} and C_{res} should be determined simultaneously to avoid high C_{res} values resulting for low L_{σ}.

4.3.3 Experimental Verification

To verify the theoretically analyzed operation principle of the proposed SRC with integrated DC link voltage balancing and galvanic isolation, a 1 kW proof-of-concept prototype is built as shown in **Fig. 4.14**. The electrical specifications and the circuit parameters of the system are summarized in **Tab. 4.5**. The switched bridge-leg is realized with 200 V MOSFETs (OptiMOS$^{\mathrm{TM}}$3 IPP320N20N3 G from Infineon Technologies AG) and the secondary-side diode rectifier stage is implemented with Schottky Diodes (MBR40250TG from On Semiconductor®). MOSFETs are preferred to IGBTs because of the relatively large forward

Table 4.5: Electrical specifications and circuit parameters of the 1 kW SRC prototype with integrated DC link voltage balancing and galvanic isolation. [1)] To assess $L_{\sigma\mathrm{res}}$ (cf. Section 4.3.2), the inductances of the connecting wires, connectors and PCB tracks need to be considered as well. For the built hardware these inductances were calculated to 0.31 µH.

Electrical specifications	
Nominal power	1 kW
Max. asymmetrical loading	1 kW/3 = 333 W
Total DC link voltage	150 V
Switching frequency	20 kHz
Circuit parameters	
DC link capacitors $C_{\mathrm{dc},x}$, $x = 1, 2, 3, 4$	
Measured capacitance	133 µF (2 × 68 µF)
Type	EPCOS MKT 100 V_{DC}
Resonant capacitor C_{res}	
Measured capacitance	30.2 µF (7 × 4.7 µF)
Type	WIMA MKS 2 30 V_{AC}
High-frequency transformer	
Core	3 × 2 × E 42/21/15, EPCOS N27
Number of turns	$N_1 = N_2 = 17$ (bifilar windings)
Air-gap / coupling	1.7 mm / $k = 0.994 \rightarrow n_{\mathrm{p}} = 0.994$
Magnetizing / stray inductance	$L_\mu = 153.1$ µH / $L_\sigma = 1.8$ µH[1)]

voltage drops of IGBTs in comparison to the selected DC link voltage levels. Additionally, due to the zero-voltage switching, lower switching losses are expected for MOSFETs than for IGBTs.

For the measurements, the configurations depicted in **Fig. 4.15** are employed. Five cases are investigated: for the cases I-IV, the power flow is from the rectifier to the inverter stage [cf. **Fig. 4.15(a)**]; for case V, the power flow is in the opposite direction [cf. **Fig. 4.15(b)**].

- *Case I* - Operation at "no load" [cf. **Fig. 4.16(a)**]: as mentioned in Section 4.3.1, a minimum loading of $C_{\mathrm{dc},3}$ and $C_{\mathrm{dc},4}$ is necessary, which is achieved by setting $R_3 = R_4 \rightarrow \infty$ and $R_{34} = 22\,\mathrm{k\Omega}$. This case represents the idle case, when no load is connected to the output of the SRC.

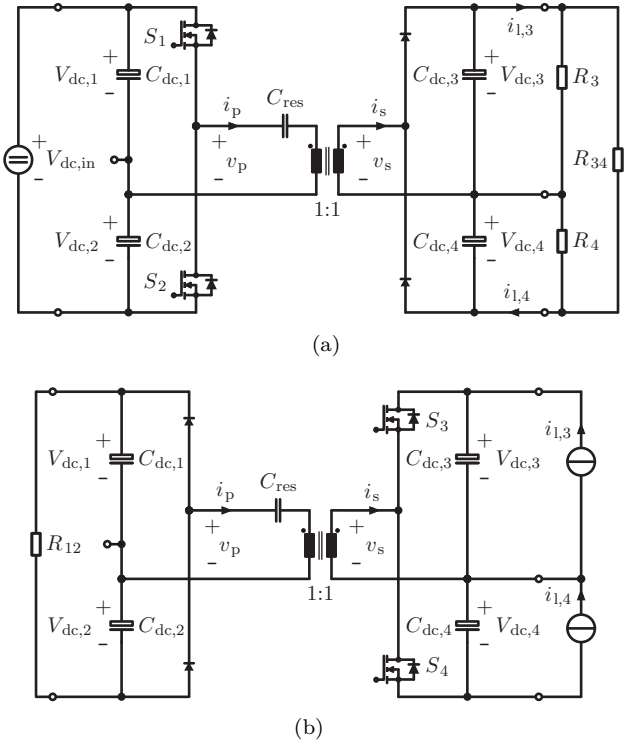
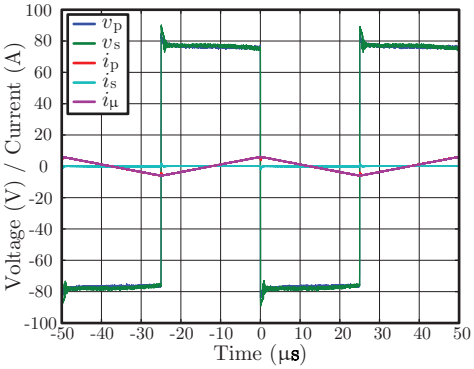


Figure 4.15: Circuit arrangements employed for the measurement setups: **(a)** for a power flow from the inverter stage to the rectifier stage, and **(b)** for a power flow from the inverter stage to the rectifier stage.

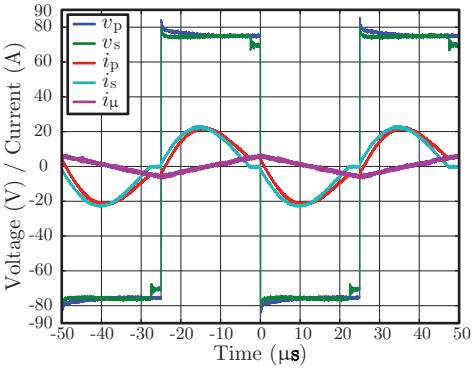
- *Case II* - Symmetrical operation at 1 kW [cf. **Fig. 4.16(b)**]: the inverter-side DC link capacitors are loaded with $R_3 = R_4 = 11.25\ \Omega$ ($R_{34} \to \infty$).

- *Case III* - Asymmetrical operation at 1 kW [cf. **Fig. 4.16(c)**]: $C_{dc,3}$ and $C_{dc,4}$ are loaded with $R_3 = 16.8\ \Omega$ ($\to 330$ W) and $R_4 = 8.4\ \Omega$ ($\to 660$ W) respectively ($R_{34} \to \infty$).

- *Case IV* - Asymmetrical operation at 330 W [cf. **Fig. 4.16(d)**]: the inverter-side DC link capacitors are loaded with $R_3 = 16.8\ \Omega$



(a) *Case I*: No load

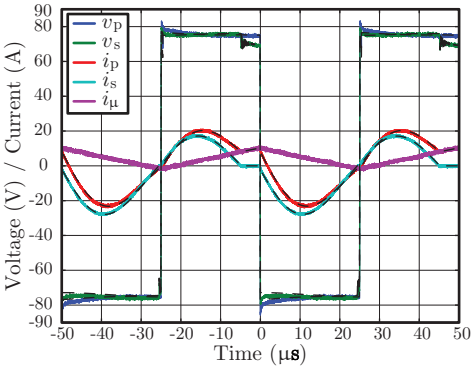


(b) *Case II*: 1 kW

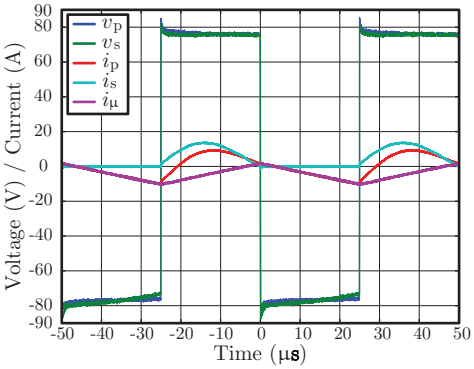
Figure 4.16: Primary voltage v_p, primary current i_p, secondary voltage v_s, and secondary current i_s (cf. Fig. 4.15) measured on the 1 kW prototype (cf. Tab. 4.5) for the five cases mentioned in the text: **(a)** case I, **(b)** case II, **(c)** case III, **(d)** case IV, and **(f)** case V. **(e)** DC link voltages ($V_{dc,1,avg}$ = 75.5 V, $V_{dc,2,avg}$ = 75.3 V, $V_{dc,3,avg}$ = 74.6 V, and $V_{dc,4,avg}$ = 81.2 V) for case IV. The transformer magnetizing current was calculated as $i_\mu = i_p - i'_s$.

($\rightarrow$ 330 W) and $R_4 = 22\,k\Omega$ ($R_{34} \rightarrow \infty$). Because of the issue mentioned in Section 4.3.1, $C_{dc,4}$ was slightly loaded.

- *Case V* - Asymmetrical operation at 820 W [cf. **Fig. 4.16(f)**]:



(c) *Case III*: 1 kW

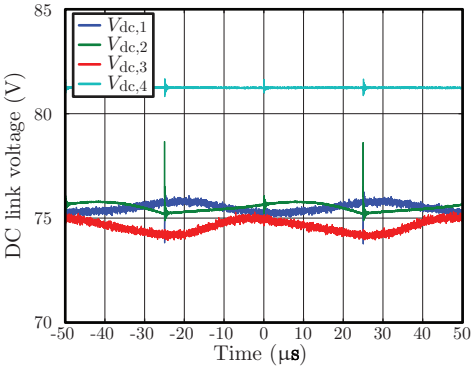


(d) *Case IV*: 330 W

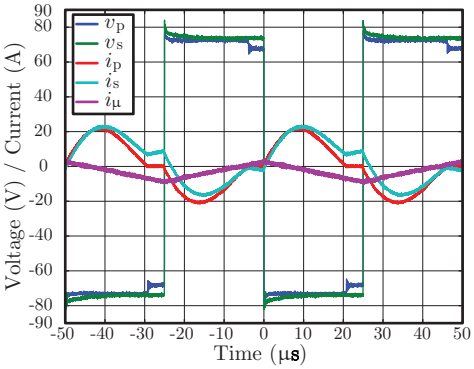
Fig. 4.16: Continued.

$i_{l,3} = 4$ A ($\rightarrow$ 300 W) and $i_{l,4} = 7.1$ A ($\rightarrow$ 520 W) is set. On the rectifier side, $C_{dc,1}$ and $C_{dc,2}$ are equally loaded by $R_{12} = 25\ \Omega$.

For the above mentioned cases, the measurement results are shown in **Fig. 4.16**. Comparing the experimental results to Fig. 4.10, the measured voltages and currents are in good agreement with the theoretical analysis conducted throughout this section. Furthermore, as exemplary depicted in Fig. 4.16(c), the measurements are matching with the circuit simulations (dashed black curves) carried out in GeckoCIRCUITS.



(e) *Case IV*: 330 W



(f) *Case V*: 820 W

Fig. 4.16: Continued.

For case IV, the DC link voltages $V_{dc,1}$, $V_{dc,2}$, $V_{dc,3}$, and $V_{dc,4}$ on the rectifier side and on the inverter side are given in **Fig. 4.16(e)**. As explained in Section 4.3.1, the maximum DC link voltage unbalance on the inverter side occurs when only one DC link capacitor is loaded. The average voltage difference between $V_{dc,4}$ and $V_{dc,3}$ is 6.6 V and therefore 8.5% referred to $(V_{dc,3,avg} + V_{dc,4,avg})/2 = 77.9$ V.

4.3.4 Summary

In this section, a series resonant DC–DC converter (SRC) integrating the galvanic isolation of the CVS input and output stages and the balancing of the DC link capacitor voltages is presented. The SRC interconnects the three-phase three-level rectifier stage with the three-phase four-leg, three-level inverter stage, which also needs to supply asymmetrical loads. The galvanic isolation avoids a ground current and is achieved with a high-frequency transformer. The proposed SRC is operated in half-cycle discontinuous-conduction-mode and consists of two half-bridges, from which always only one is switched depending on the power flow direction. The bridge-leg output and the DC link midpoint on the primary side are connected through the resonant capacitor, the resonant inductor, and the primary winding of the transformer; on the secondary side, the bridge-leg input and DC link midpoint are directly connected through the transformer secondary winding.

Supplying asymmetrical loads, the inverter-side DC link capacitors are not equally loaded simultaneously. In this case, the voltage balancing across the DC link capacitors is achieved by establishing an average (over one switching cycle) magnetizing current, which is equal to the difference of the load currents. Accordingly, the high-frequency transformer integrates the DC link voltage balancing and the galvanic isolation. It needs to store energy and hence should be realized with an air-gap or a low-permeability material for a low-volume realization.

Ideally, the DC link voltage balancing on the rectifier side can be achieved perfectly. On the inverter side, the difference of the DC link voltages depends on the average load currents. However, this voltage difference can be restricted to less than 10%, referred to the voltage across one DC link capacitor. Furthermore, design guidelines are presented showing that the SRC can achieve soft-switching (zero-voltage switching) at turn-on in all operating conditions if the peak-to-peak magnetizing current ripple is slightly larger than two times the maximum average magnetizing current (what corresponds to twice the maximum load current difference). Finally, the theoretical analysis is supported by measurements conducted on a 1 kW proof-of-concept prototype matching very well with the theory and the circuit simulations for no load, symmetrical loading, and asymmetrical loading and for a bidirectional power flow.

Finally, it is noted that the main research results of this section are published in [342, 343] (see also “List of Publications” on page 337).

4.4 CVS Module Operation

Compared to the option to control the ground current i_{gnd} to zero for simultaneously grounded mains and load star-points (cf. Fig. 4.7), the elimination of i_{gnd} by means of a galvanic isolation has the advantages that

- the input stage can still be operated with the superposition of a zero-sequence voltage component v_{zs} on the carrier based modulation to utilize the full (linear) modulation range, and that
- the neutral leg of the output stage can yet be employed, if required, to increase the range of the phase load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ (connection of the load star-point to the neutral terminal N, cf. Fig. 4.1).

Neither $v_{0,\mathrm{cm}}$ is employed for controlling i_{gnd} to zero nor $v_{\mathrm{N,out}}$ is adjusted to zero as explained in Section 4.2.1. Hence, for the generation of symmetrical three-phase voltage systems with maximal 230 V (rms; line-to-neutral), the nominal DC link voltage could be reduced by 15.5%, from 700 V to roughly 600 V (cf. Sections 3.4 and 3.5). On the one hand, this especially lowers the switching losses of all switches and the high-frequency losses in $L_{\mathrm{dm},1}$ and $L_{\mathrm{DM},1}$ (due to the reduced high-frequency current ripple), and on the other hand, it increases the high-frequency losses in the transformer [the amplitude of the current pulses (cf. Fig. 4.16) is increased by 15.5% for the same transmitted power]. Thus, a more detailed loss analysis (left for further investigations) is required to determine if, by lowering V_{dc} for the mentioned operating conditions, the efficiency of the CVS module with galvanic isolation is increased or decreased. However, compared to the realization without transformer, the SRC still requires two additional switches and DC link capacitors as well as a 10 kW high-frequency transformer, which add a significant part to the total volume and weight of the CVS.[7] Accordingly, it is preferred to realize the CVS unit without galvanically isolated DC–DC converter as depicted in Fig. 4.1. This however necessitates a balancer circuit and a ground current control scheme.

The CVS is thus operating as follow: without fixed connections of the mains star-point and / or the load (e.g. load star-point) to ground, the CM voltage $v_{0,\mathrm{cm}}$ of the bridge-leg input voltages is employed to

[7] It is expected, that the volume of the balancer inductor is much smaller compared to the one of the high-frequency transformer.

utilize the full (linear) modulation range and the output voltage $v_{\mathrm{N,out}}$ of the neutral leg is used to increase the range of the load voltages according to (3.86). However, for earthed mains and load star-points, $v_{0,\mathrm{cm}}$ is regulating the ground current i_{gnd} to zero and $v_{\mathrm{N,ref}} = 0$ is set. In both cases, to increase the CVS' efficiency, the DC link voltage is adjusted such that a minimal margin of 25 V exists between the maximum input / output voltage, which can be generated by the input / output stage, and the maximum mains / load voltage, to allow a small ripple of the DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$. Consequently, for the nominal peak input and output voltages of 325 V, the nominal DC link voltage yields $V_{\mathrm{dc,n}} = 700$ V. If a faster rise / reduction in the load voltages is required, the DC link voltage can be increased to maximally $V_{\mathrm{dc,max}} = 800$ V. The balancer circuit can be operated continuously or can be switched on if the absolute difference between the DC link voltages, i.e. $|V_{\mathrm{dc},1} - V_{\mathrm{dc},2}|$, exceeds a certain threshold.

For nominal operation with $V_{\mathrm{dc}} = 700$ V (cf. Tab. 1.1) a total efficiency $\eta_{\mathrm{tot,n}}$ of 95.0%, which is equal to the targeted efficiency is calculated for a 10 kW CVS module. The measured efficiency $\eta_{\mathrm{in,n}}$ of the input stage is 98.2%, the efficiency $\eta_{\mathrm{out,n}}$ of the output stage is estimated to 97.7% based on measurements, and an efficiency of 99% is assumed for the balancer circuit. Accordingly, the total efficiency results as $\eta_{\mathrm{tot,n}} = 98.2\% \times 99\% \times 97.7\% = 95.0\%$.

The operation of the input stage is explained in Section 3.5, where the compliance to the conducted EMI limits according to CISPR 11, Class A, is demonstrated by measurements. There, it is assumed that the entire output stage with load is represented by a worst case capacitance $C_{\mathrm{g}} = 25$ nF from the DC midpoint m to ground (PE). Given the good agreement between the measured and simulated EMI spectrum for frequencies ≤ 500 kHz in Section 3.5.7, the EMI spectrum at the input of the entire CVS module (as shown in Fig. 4.1) is simulated for the case specified on page 239 and the conditions given in Section 4.2.2 (i.e. nominal operation). To simulate the noise emissions of the CVS module, a three-phase LISN is connected to the CVS input (cf. Fig. 3.50). Moreover, parasitic capacitances $C_{\mathrm{S}} = 267\,\mathrm{pF}/2 = 134\,\mathrm{pF}$[8] to the

[8]The value of 267 pF is the measured parasitic capacitance of one bridge-leg output to the heat sink (all switches off), which comprises two capacitances C_{S} from the drain terminal of the switches to the heat sink (cf. Fig. 3.49). The voltage across C_{S} of the upper switch S_1 [cf. Fig. 2.3(b)] is given by $V_{\mathrm{dc},1}$ and the capacitance C_{S} of the middle switch S_3 [cf. Fig. 2.3(b)], being connected to the midpoint m, is shorted due to the heat sink tied to m. Accordingly only the capacitances C_{S} of the

heat sink for all switches (cf. Section 3.5.1) as well as parasitic capacitances of $C_{\text{para}} = 50\,\text{pF}$ (cf. Section 3.5.6) between the output terminals of all bridge-legs and ground are assumed. A common heat sink connected to the DC midpoint m is employed for all switches. The maximum noise emission of the CVS towards the mains is obtained at 150 kHz and is 69.4 dBµV, whereas the emission at 192 kHz is already reduced to 64 dBµV, demonstrating that the compliance to CISPR 11, Class A (quasi-peak limit of 79 dBµV for $[150\,\text{kHz}, 500\,\text{kHz}]$ and of 73 dBµV for $[500\,\text{kHz}, 30\,\text{MHz}]$) is given for frequencies in the range of $[150\,\text{kHz}, 500\,\text{kHz}]$.[9] For higher frequencies the GeckoCIRCUITS simulation model does not reflect the hardware setup correctly and accordingly EMI measurements are required to fully verify the compliance to CISPR 11, Class A.

The conducted EMI requirement, taken into account for the design of the output filter in Section 3.2, was based on single-phase considerations. Thus, to validate the proposed approach for the designed four-line two-stage LC output filter, the EMI spectrum at the output of the CVS is simulated and recorded by a LISN, placed between the CVS output and the load. The maximum resulting emission at the output in the range of $[150\,\text{kHz}, 500\,\text{kHz}]$ is 61.6 dBµV and is obtained at 240 kHz (phase A, cf. Footnote 9 below). The emissions at 150 kHz and 192 kHz are 59.2 dBµV and 56.2 dBµV, respectively. The compliance to the CISPR 11, Class A limit of 79 dBµV (quasi-peak) is hence given in $[150\,\text{kHz}, 500\,\text{kHz}]$ for the output stage as well. The conditions for these circuit simulation results are identical to the ones assumed to simulate the conducted EMI emissions at the input of the CVS (see paragraph above).

However, to fully verify the compliance to CISPR 11, Class A, EMI measurements are required, especially for frequencies $> 500\,\text{kHz}$. This then also allows determining if a four-line CM choke and / or CM filter is required at the output of the CVS to fulfill the standard.

remaining two switches S_2 and S_4 are charged / discharged during the commutation from one switching state to the next.

[9] The indicated emission levels are obtained for phase a and are identical to the ones obtained for phases b and c, because the component values and the values of the parasitic elements are in the circuit simulation equal for all phases.

5

Parallel Operation of Two Converter Modules

The architecture of one 10 kW CVS module is elaborated in Chapter 4, where a converter topology without galvanic isolation is proposed. To increase the power level of the CVS and for the reasons given in Chapter 1, it is often preferred to connect several modules in parallel. For the considered 100 kW high bandwidth CVS, ten 10 kW CVS modules must be paralleled as given in Fig. 1.1. The full schematic of two parallel connected modules is depicted in **Fig. 5.1**.

However, the disadvantage of operating CVS modules without galvanic isolation in parallel consists in the formation of undesired inter-module circulating currents, i.e. currents e.g. flowing in forward direction over a module and closing in reverse direction over the parallel connected module. This is due to the fact that the hardware realization of the CVS units typically show small differences in the component values, controller and measurement gains, and time delays of the gate driving and switching devices. The problem of circulating currents has been discussed in the literature considering the transformerless parallel connection of voltage source rectifiers [26, 320, 344–348], current source rectifiers [349, 350], voltage source inverters [25, 27, 351–356], and the back-to-back connection of voltage source converters [29, 357, 358].

Inter-module circulating currents can be separated into zero-sequence and DM currents, which need to be treated separately.[1] The former type of currents is not related to the power transfer of the

[1] It is noted that, as for the ground current (cf. Section 4.2), the following explanations refer to the DC and low-frequency part of the zero-sequence and DM currents.

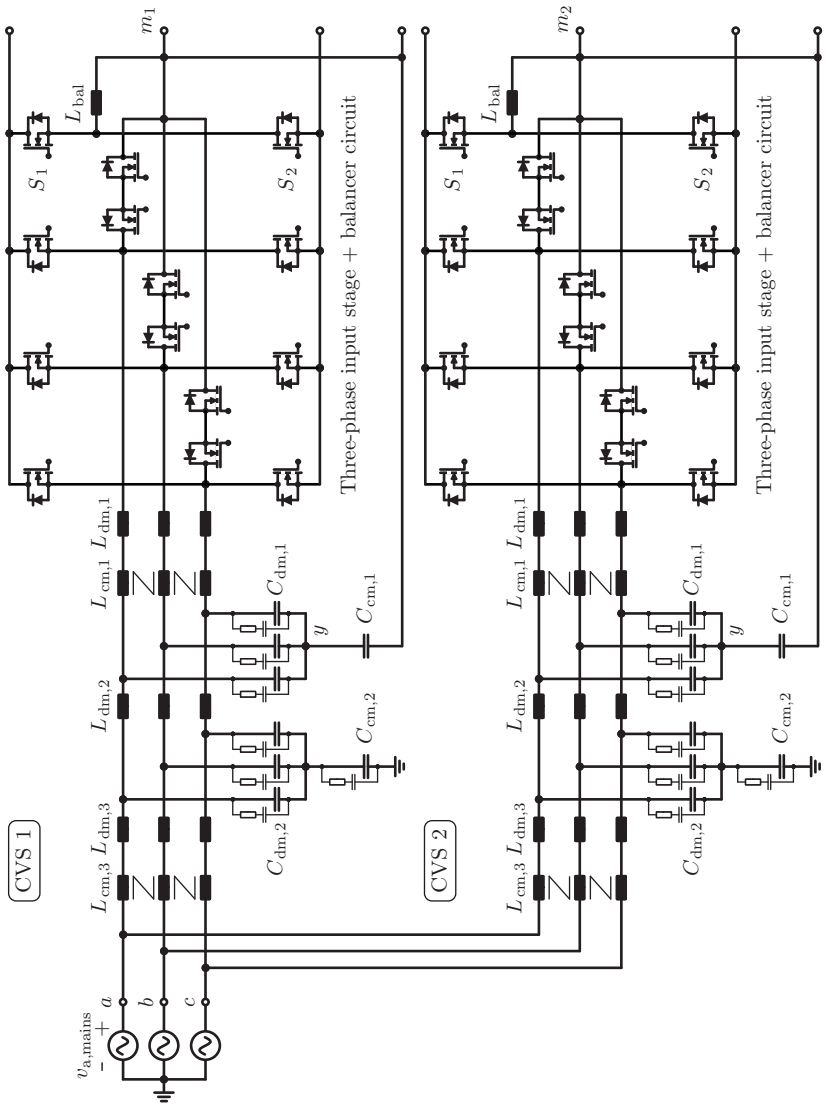


Figure 5.1: Circuit structure of two parallel connected 10 kW CVS modules. Each unit consists of an input stage with an EMI filter, a balancer circuit, and an output stage comprising a four-line two-stage *LC* filter. Exemplary, the load star-point is grounded.

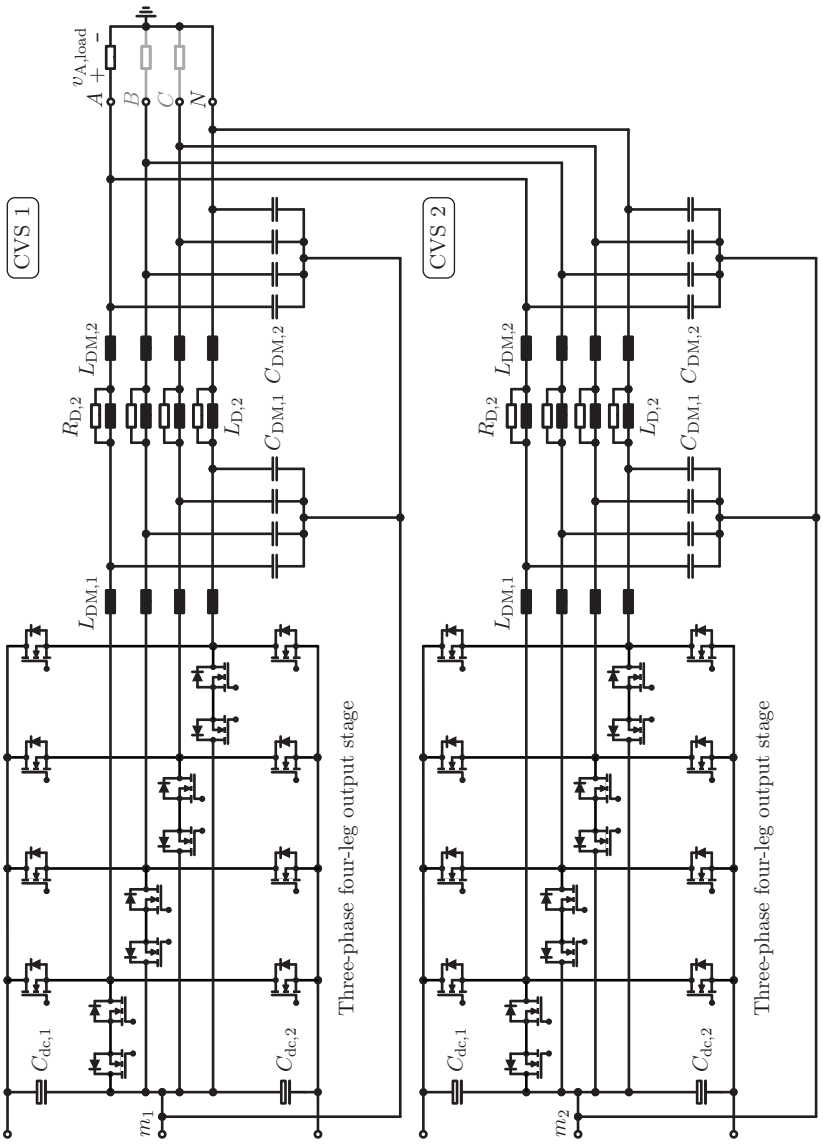


Figure 5.1: Continued.

CVS modules and may lead to distortions of the sinusoidal waveform of the module input currents and / or to a higher current stress of the modules' components. This potentially reduces the efficiency of all involved modules and may results in saturation of inductive elements (especially of the CM chokes). The driving sources for this type of currents are, as for the ground current (cf. Section 4.2), the zero-sequence components $v_{0,\mathrm{cm}}$ and the neutral leg's output voltages $v_{\mathrm{N,out}}$ of the parallel connected units. This leaves two options: controlling the zero-sequence circulating currents to zero by the voltages $v_{0,\mathrm{cm}}$ [26, 29, 31, 320, 344, 346, 348, 353–355, 358, 359] or by the voltages $v_{\mathrm{N,out}}$. As motivated in Section 4.2, $v_{0,\mathrm{cm}}$ is preferred for this purpose, which leads to the following scheme of operation of n parallel connected CVS units. For grounded mains star-point and grounded load, each module controls its zero-sequence input current $i_{\mathrm{in,zs}}$ to zero by adjusting $v_{0,\mathrm{cm}}$. Preferably, the control scheme proposed in Section 4.2.1 and given in Fig. 4.7 is used for this purpose. In this way not only the zero-sequence circulating currents are prohibited, but also the ground currents of all modules. For the reasons mentioned in Section 4.2.1, the voltage $v_{\mathrm{N,out}}$ of all modules is regulated to zero.

In case the mains star-point and the load are not simultaneously connected to ground, only $n-1$ modules need to actively control their zero-sequence input current $i_{\mathrm{in,zs}}$ to zero because all zero-sequence module input currents sum to zero. Moreover, all modules employ v_{zs} according to (3.89) for the modulation of the input stage (cf. Section 3.5) and $v_{\mathrm{N,out}}$ of all units can be employed to maximize the load voltage range according to (3.86), as explained in the following. Incipiently, this may be surprising because for DC or low frequencies, one paralleled module represents for another unit a low-impedance CM connection between the input terminals a, b, c and the neutral leg terminal N of the output stage. For instance, the magnitude of the CM impedance of one module between a, b, c and N is only $2 \cdot \pi \cdot 150\ \mathrm{Hz} \cdot (L_{\mathrm{cm,1,tot}} + L_{\mathrm{dm,2}}/3 + L_{\mathrm{cm,3,tot}}) = 2 \cdot \pi \cdot 150\ \mathrm{Hz} \cdot 7.0\ \mathrm{mH} = 6.6\ \Omega$, at a frequency of three times f_{mains} (cf. Fig. 4.6). Thereby, taking into account the finding of $v_{0,\mathrm{cm,set}} \approx v_{\mathrm{N,out}}$ for the ground current control of a single unit in Section 4.2.1, the same result is expected to be valid for parallel connected modules. However, considering the zero-sequence equivalent circuit of two paralleled CVSes in **Fig. 5.2**, the voltages $v_{\mathrm{N,out,1}}$ and $v_{\mathrm{N,out,2}}$ cancel each other along the indicated loop, because the two voltages are controlled to the same reference $v_{\mathrm{N,ref}}$.

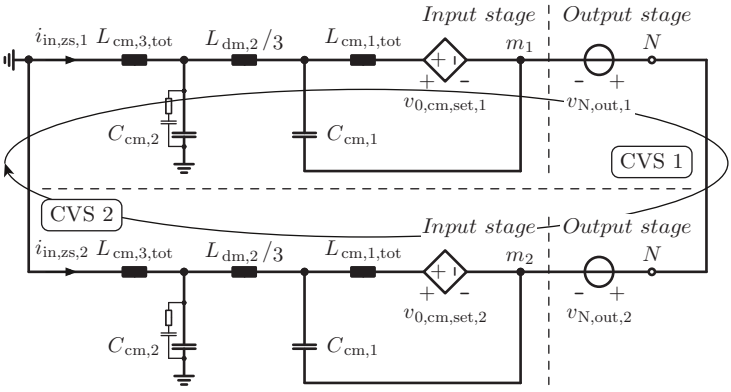


Figure 5.2: Zero-sequence equivalent circuit of two paralleled CVS modules (cf. Fig. 5.1) for grounded mains star-point and a floating load.

Accordingly, $v_{0,\mathrm{cm,set},1}$ does not need to compensate $v_{\mathrm{N,out},1}$ or $v_{\mathrm{N,out},2}$ and hence the problem recognized in Section 4.2.1 for $v_{0,\mathrm{cm,set}} \approx v_{\mathrm{N,out}}$ does not appear for parallel connected modules without simultaneously grounded mains star-point and load. Moreover, $v_{0,\mathrm{cm,set},2}$ can even be utilized to boost the linear modulation range of the input stage [cf. (3.89)] given that $v_{0,\mathrm{cm,set},1}$ can compensate for $v_{0,\mathrm{cm,set},2}$ and add a small voltage to control $i_{\mathrm{in,zs},1}$ to zero. Thus, considering the loop indicated in Fig. 5.2, the feedforward of $v_{\mathrm{N,ref}}$ ($\approx v_{\mathrm{N,out}}$) for the ground current control scheme given in Fig. 4.7 needs to be changed to $v_{0,\mathrm{cm,set},2} + v_{\mathrm{N,out},1} - v_{\mathrm{N,out},2} \approx v_{0,\mathrm{cm,set},2} + v_{\mathrm{N,ref},1} - v_{\mathrm{N,ref},2} = v_{0,\mathrm{cm,set},2}$ for either floating mains star-point or load. For $i_{\mathrm{in,zs}} \approx 0$, which is the desired objective, there are no relevant voltage drops across the inductive elements of the input filter.

For the two considered paralleled modules, CVS 1 and CVS 2 employ v_{zs}[2] for the modulation of the input stage. However, only one module, e.g. CVS 1, controls $i_{\mathrm{in,zs}}$ to zero by accordingly adjusting $v_{0,\mathrm{cm,set},1}$ around v_{zs} ($v_{0,\mathrm{cm,set},2} = v_{\mathrm{zs}}$ is used on the CVS 1 as a feedforward, as aforementioned). Finally, for the output stages of CVS 1 and CVS 2, the

[2]If the hardware setup (power circuit and measurement units) and the digital implementation of the input stage control scheme of CVS 1 and CVS 2 do not show significant differences, it follows that $v_{\mathrm{zs},1} \approx v_{\mathrm{zs},2} \approx v_{\mathrm{zs}}$, because both devices are supplied by the same mains.

output voltages $v_{\mathrm{N,out,1}}$ and $v_{\mathrm{N,out,2}}$ of the neutral leg are individually adjusted to the same reference $v_{\mathrm{N,ref}}$.

DM circulating currents lead to a unequal current sharing of the different modules and hence the current stress of some modules is increased, possibly above the allowed limits of the units.[3] To avoid this problem, a defined current partition between the modules is required. For the concept elaborated in the following, an equal current sharing is targeted, which, however, can be easily modified to achieve an arbitrary current distribution among the modules, if desired.

Basic methods to achieve a defined current partitioning between paralleled units can be classified into droop-based methods [24, 25, 28, 360–365] and active current-sharing methods [23,25,28,347,351,356,357, 361, 366–369]. Droop-based methods do not require a communication between the modules and achieve the current sharing according to a droop characteristic, implemented on each module, which emulates an internal resistance R_{i} in series to the outputs of the module. Typically, the droop characteristics of all modules are not completely equal in reality and accordingly, because the methods operate open-loop, tight output voltage control ($R_{\mathrm{i}} \to 0$) and an equal current sharing ($R_{\mathrm{i}} \to \infty$) is not possible at the same time [24, 361, 362, 365].

Thus, an active current-sharing method is preferred, where the equal current partitioning is forced by closed-loop control structures. To best introduce into the topic, the PI-P control structure given in Fig 3.26(a) without feedforwards and for only one phase, i.e. phase A, is considered. It is repeated that each phase and the neutral leg are controlled independently with identical control approaches.

For this structure, an outer output voltage control loop generates a reference $i_{\mathrm{A0,ref}}$ for an inner bridge-leg output current control loop. For parallel connected modules, the load voltage $v_{\mathrm{A,load}}$ is equal for all units und hence its control task can be executed by only one entity. This entity can either be an additional centralized control unit or the control unit of one of the modules, which leads to the basic distinction between central-mode and Master-Slave control concepts, respectively [23, 25, 28, 347, 351, 356, 357, 366–369]. For the first concept, the centralized control unit regulates the load voltage $v_{\mathrm{A,load}}$. The output of the voltage controller is the reference $i_{\mathrm{A0,ref}}$ for the sum of all bridge-leg output currents of all modules and can hence be divided by the number of

[3] It is noted that this type of currents cannot, in contrast to the zero-sequence circulating current, be eliminated by employing a galvanic isolation (cf. Section 4.3).

paralleled units n to result in equal bridge-leg output current references for all modules, i.e. $i_{\mathrm{A0,ref},k} = i_{\mathrm{A0,ref}}/n$ for the k^{th} CVS. These bridge-leg output current reference is communicated to all units, which then adjust their bridge-leg output current, in average over one switching cycle, to the reference within the inner control loop. If all averages of the bridge-leg output currents are identical, also the output current is shared equally among all modules.

For the Master-Slave control concept, the task of controlling $v_{\mathrm{A,load}}$ is implemented on one module, i.e. the Master module, which then also determines equal bridge-leg output current references for itself and for all other modules, i.e. the Slave modules. Because each module also needs to work as a stand-alone device, the drawback of the central-mode control concept is that the communication delay between the centralized control unit and the modules increases the time delay in the load voltage (respective output voltage) control loop, deteriorating the values of the EQs achieved in Section 3.3.3. The Master-Slave control concept proposed in Section 5.1 does not suffer from this problem and is accordingly selected for the active current-sharing control of parallel connected CVS units. The analysis is presented for two paralleled modules as shown in Fig. 5.1, i.e. a Master and a Slave module, and can easily be extended to more Slave units by implementing the control scheme explained below on all Slave CVSes. Circuit simulation results for two characteristic cases are presented in Section 5.2, and Section 5.3 summarizes the contributions of this chapter.

5.1 Master-Slave Control Concept

In contrast to the exemplary mentioned PI-P control structure above, the output of the voltage controller for the selected capacitor current feedback control approach in Section 3.3 (cf. Fig. 3.46) does not generate a reference for the bridge-leg output current i_{A0}. Instead, it produces a set point voltage $v_{\mathrm{A0,set,v}}$, from which $k_1 \cdot i_{\mathrm{A1}}$ and $k_2 \cdot i_{\mathrm{A2}}$ are subtracted, to achieve damping, and to which the output voltage reference $v_{\mathrm{A,ref}} + v_{\mathrm{N,ref}}$ is added to result in the set point value $v_{\mathrm{A0,set}}$ for the bridge-leg output voltage v_{A0}. It is hence recognized that the capacitor current feedback structure incorporates no direct or indirect control of i_{A0} or $i_{\mathrm{A,out}}$, which both could be used to achieve an equal current sharing among paralleled units. Accordingly, as explained in the following, slight modifications of the selected control structure are required for

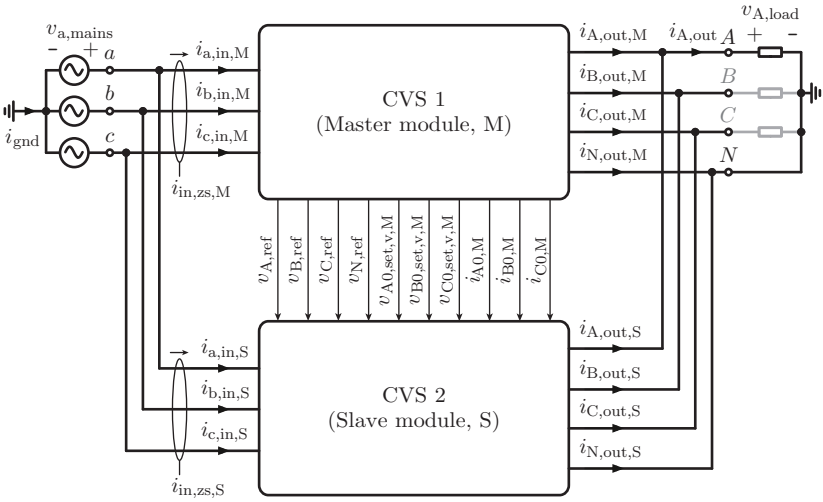


Figure 5.3: Master-Slave control scheme showing the transferred data from the Master module (M) to the Slave module (S). Exemplary, the load star-point is grounded.

connecting CVS modules in parallel and controlling them based on the Master-Slave concept as shown in **Fig. 5.3**.

It is in this context remarked that from the point of view of operating multiple CVS modules in parallel, a phase output voltage control structure which includes a direct measurement of the bridge-leg output current or of the phase output current (which is required for the current sharing between the modules as explained in the following) would lead to a lower realization effort compared to the proposed control scheme, which additionally demands to measure the currents of the filter capacitors.

The idea of the proposed control concept is given in **Fig. 5.4** (accentuated in green), where also a zero-sequence current control at the input (highlighted in blue) besides the phase-oriented control at the output of each module is included. The input stage control system is given for a simultaneously grounded mains star-point and load. It is emphasized that the DC link midpoints m_{M} and m_{S} in Fig. 5.4 interconnect the corresponding input and output stages and are not electrically connected.

The Master module (M) implements the capacitor current feedback structure as proposed in Fig. 3.46 without changes and transmits the output of the voltage controller $v_{\mathrm{A0,set,v,M}}$ as well as the references $v_{\mathrm{A,ref}}$ and $v_{\mathrm{N,ref}}$ to the Slave module (S) [cf. Fig. 5.3]. The latter module then achieves the damping by employing its own capacitor currents and utilizes $v_{\mathrm{A,ref}} + v_{\mathrm{N,ref}}$ as a feedforward. Moreover, to achieve an equal current distribution of $i_{\mathrm{A,out}}$ between the Master and the Slave units, a current controller is added on the Slave module (cf. Fig. 5.4). This controller adjusts, in average over one switching cycle and within the bandwidth of its control loop, identical bridge-leg output currents $i_{\mathrm{A0,M}}$ and $i_{\mathrm{A0,S}}$ of the Master and the Slave module, respectively. Its output is a correction voltage $\Delta v_{\mathrm{A0,S}}$ (cf. Fig. 5.4) which adds to $v_{\mathrm{A0,set,v,M}}$ and leads to the set point for the Slave bridge-leg output voltage according to

$$v_{\mathrm{A0,set,S}} = v_{\mathrm{A0,set,v,M}} - k_1 \cdot i_{\mathrm{A1,c,S}} - k_2 \cdot i_{\mathrm{A2,S}} + v_{\mathrm{A,ref}} + v_{\mathrm{N,ref}} + \Delta v_{\mathrm{A0,S}}. \tag{5.1}$$

The bridge-leg output current $i_{\mathrm{A0,M}}$ of the Master module is thus transferred to the Slave CVS too, as depicted in Fig. 5.3.

Because the zero-sequence circulating current and / or the ground current are / is suppressed by the input stage of each CVS, the output current of the neutral leg of each module is given by $i_{\mathrm{N,out},j} = -(i_{\mathrm{A,out},j} + i_{\mathrm{B,out},j} + i_{\mathrm{C,out},j})$, where $j = \mathrm{M}, \mathrm{S}$.[4] is Accordingly, no current measurement or symmetrizing control is needed for the neutral leg's bridge-leg output current; the voltage $v_{\mathrm{N,out}}$ is controlled by both modules to $v_{\mathrm{N,ref}}$ independent of each other (cf. Fig. 5.4).

To reduce the voltage ripple of $v_{\mathrm{A,load}}$ compared to a single unit, the PWM carrier signals of the Master and Slave devices, which are assumed to be synchronized, are phase-shifted by 180 ° such that the harmonics of the output voltage ripples of both modules at each multiples of the switching frequency cancel each other out.

The transmission of the data from the Master CVS to the Slave CVS (as given in Fig. 5.3) is not instantaneous and requires a certain time T_{t}. With the assumption that $T_{\mathrm{t}} < T_0 = 1/(2 \cdot f_{\mathrm{s,out}})$ and that the PWM carrier signals of the Master and Slave modules are synchronized, i.e. the sampling of both units occurs at the same instant, the Slave device receives data values of $i_{\mathrm{A0,M}}$, $v_{\mathrm{A0,set,v,M}}$, $v_{\mathrm{A,ref}}$, and $v_{\mathrm{N,ref}}$ which are delayed by T_0. To compensate this delay for $v_{\mathrm{A,ref}}$ and $v_{\mathrm{N,ref}}$, the

[4] It is noted that there is no electrical connection between the DC link midpoints m_{M} and m_{S} of the Master and Slave devices, respectively.

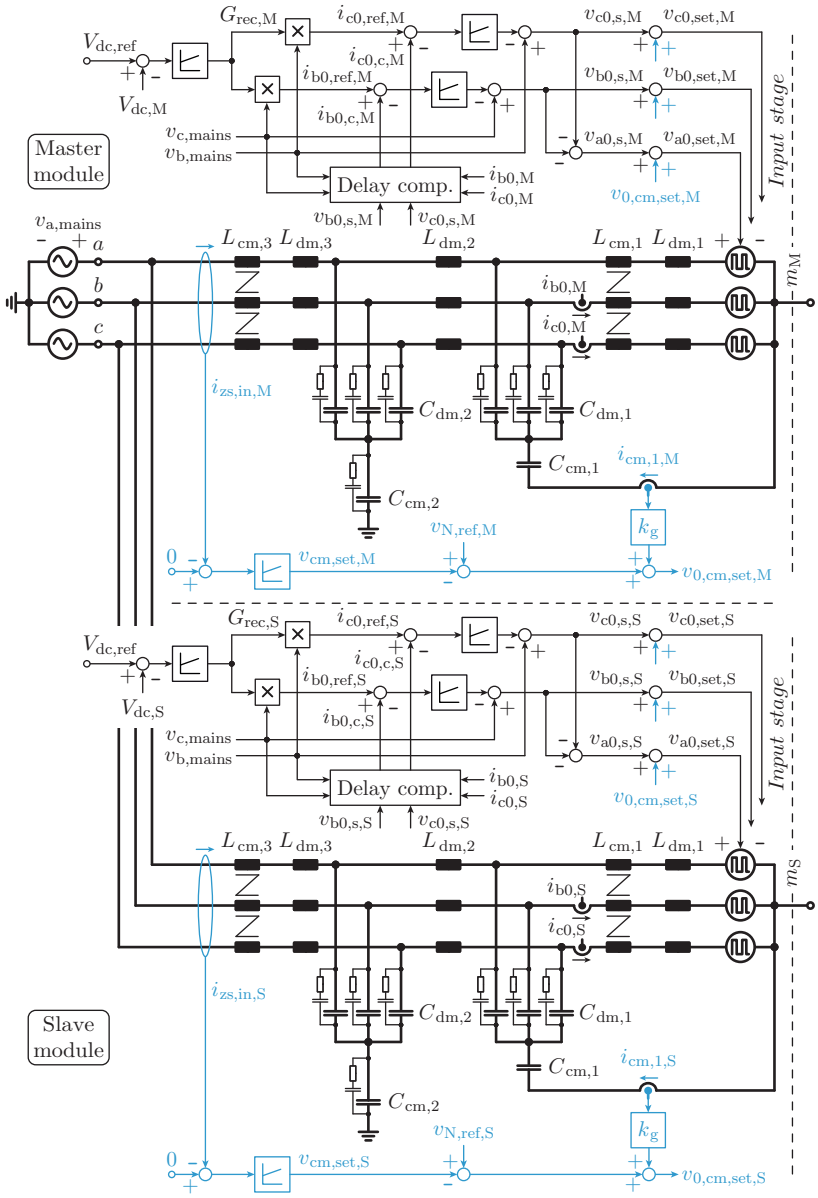


Figure 5.4: Master-Slave control scheme for two paralleled 10 kW CVSes.

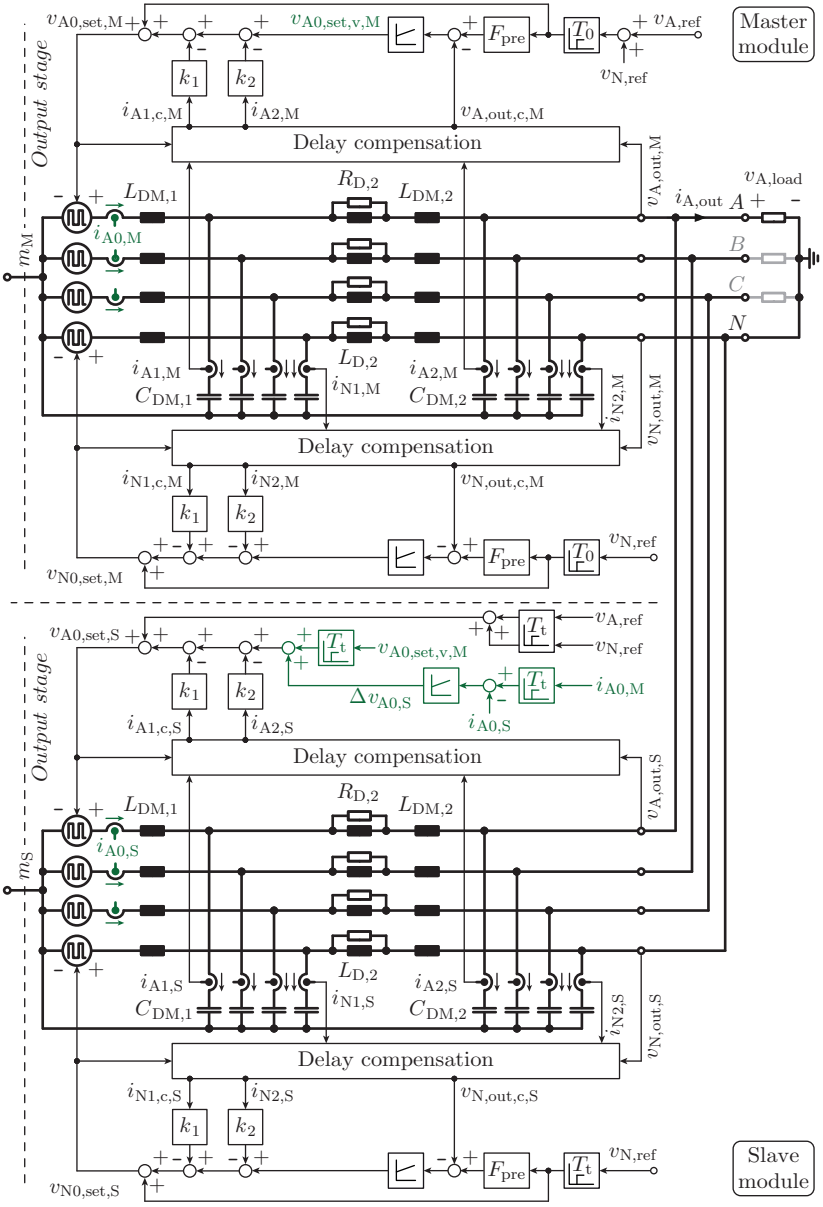


Figure 5.4: Continued.

Table 5.1: Parameters of the bridge-leg output current controller (cf. Fig. 5.4) to achieve an equal current sharing between the Master and the Slave CVSes.

Current controller gain	$k_{\mathrm{pi}} = 6.8$ V/A
Current controller time constant	$T_{\mathrm{ii}} = 750$ µs

Table 5.2: Operating conditions for which the reference voltage steps depicted in Fig. 5.5 are simulated for a single CVS and two parallel connected converters.

DC link voltage, V_{dc}	700 V
Load voltage of phase A before the step, $v_{\mathrm{A,load}}(t < 0)$	200 V
Load voltage of phase B, $v_{\mathrm{B,load}}$	200 V
Load voltage of phase C, $v_{\mathrm{C,load}}$	−200 V
Output voltage of the neutral leg, $v_{\mathrm{N,out}}$	0
Load resistances, $R_{\mathrm{A,load}}$, $R_{\mathrm{B,load}}$, $R_{\mathrm{C,load}}$	15.9 Ω (single CVS) / 7.9 Ω (two CVSes)

Master module sends the reference voltages to the Slave and delays them by one sampling period T_0 before they take effect on the Master module itself (cf. Fig. 5.4). In this way, the Slave and the Master unit react at the same instant on changes in the references. For the following study $T_{\mathrm{t}} = T_0$ is assumed.

No compensation of the delay introduced by the data transmission is proposed for $i_{\mathrm{A0,M}}$ and $v_{\mathrm{A0,set,v,M}}$. Such a compensation would require to predict future values with an estimator, which includes an estimation of the load, and hence is related to a high implementation effort. In the opinion of the author, such an effort is not justified considering the good agreement between the load voltages simulated for one and two CVSes shown in **Fig. 5.5** and between $i_{\mathrm{A,out,M}}$ and $i_{\mathrm{A,out,S}}$ given in **Fig. 5.6**.

The parameters of the bridge-leg output current controller, as summarized in **Tab. 5.1**, have been tuned by circuit simulations (on the basis of the parameters obtained for the PI-P control structure, cf. Tab. 3.11). With the proposed Master-Slave control concept and

for the operating conditions given in **Tab. 5.2**, a voltage reference step of 20 V for $v_{\mathrm{A,ref}}(t < 0) = 200$ V in phase A has been simulated for two paralleled CVSes. The comparison to the load voltage step response of a single module is shown in Fig. 5.5. The voltage differences for all phases and the neutral leg are almost negligible (except for the voltage ripple). The load resistance is decreased to $R_{p,\mathrm{load}}/2 = 15.9\ \Omega/2 = 7.9\ \Omega$ ($p = A$, B, C) for the two paralleled systems to load each unit to the same amount than the single counterpart. The output currents of the Master and the Slave devices are depicted in Fig. 5.6 for the mentioned reference step and reveal a good current sharing between the two units. The maximum deviation between $i_{\mathrm{A,out,M}}$ and $i_{\mathrm{A,out,S}}$ is less than 1.8 A, i.e. $< 9\%$ of the nominal peak output current of 20.5 A for one module and occurs only during the transient.

5.2 Simulation Results

A GeckoCIRCUITS simulation of two CVS modules, as given in Fig. 5.1, has been performed with the proposed Master-Slave control concept (cf. Fig. 5.4) and for the following two representative cases, for which each CVS unit runs at nominal conditions:

- Case I: Connection of the mains star-point to PE and connection of the output neutral terminal N to PE; resistive symmetrical three-phase load of $R_{p,\mathrm{load}} = 7.9\ \Omega$ ($p = A$, B, C) with the load star-point connected to N. The output phases A, B, and C generate a symmetrical three-phase voltage system (with respect to the neutral terminal N) with 230 V (rms; line-to-neutral) and at 50 Hz. The output voltages of the neutral legs N are controlled to zero. Both modules control their input zero-sequence current $i_{\mathrm{in,zs},j}$ ($j = \mathrm{M}$, S) to zero employing $v_{\mathrm{N,ref}}$ as a feedforward.
- Case II: Connection of the mains star-point to PE and floating output neutral terminal N with respect to PE; resistive symmetrical three-phase load of $R_{p,\mathrm{load}} = 7.9\ \Omega$ ($p = A$, B, C) with the load star-point connected to N. The output phases A, B, and C generate a symmetrical three-phase voltage system (with respect to the neutral terminal N) with 230 V (rms; line-to-neutral) and at 50 Hz. The output voltages of the neutral legs N are controlled according to (3.86) to maximize the load voltage range. The Master module controls its zero-sequence input current $i_{\mathrm{in,zs,M}}$ to zero

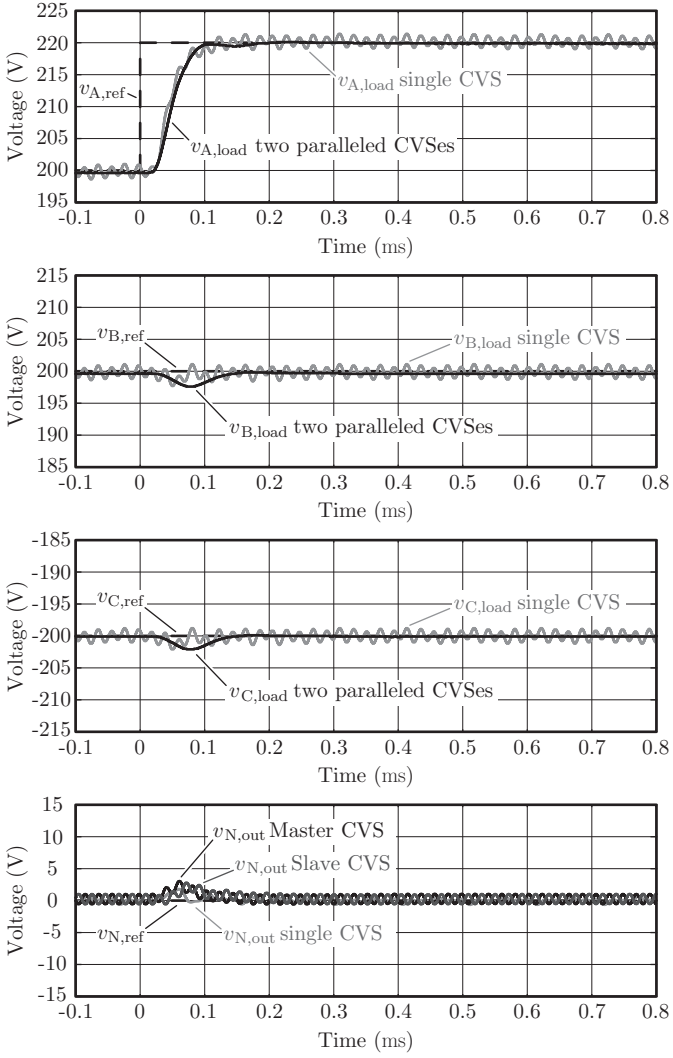


Figure 5.5: Simulated load voltages $v_{A,load}$, $v_{B,load}$, $v_{C,load}$ and neutral leg output voltages for a voltage reference step of 20 V in phase A, for the conditions given in Tab. 5.2, and for two paralleled CVS modules controlled with the proposed Master-Slave concept (cf. Fig. 5.4). The load voltages and the neutral leg's output voltages are compared to the simulated voltages for a single CVS converter (cf. Fig. 4.7).

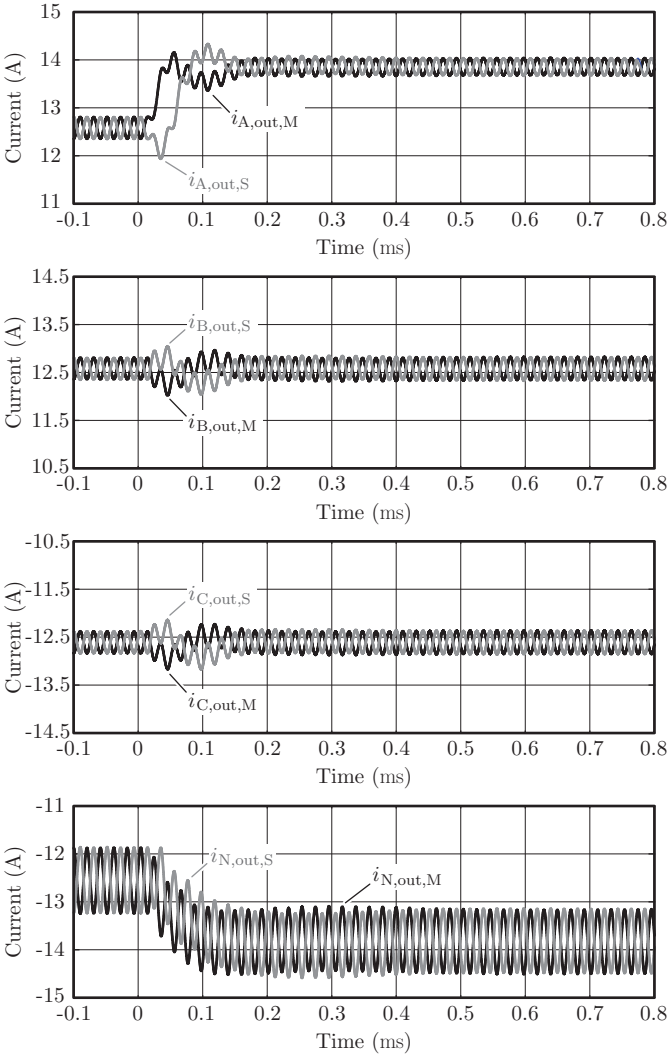


Figure 5.6: Simulated output currents of the Master module and the Slave module for the conditions given in Tab. 5.2 and for two paralleled CVS devices controlled with the proposed Master-Slave concept (cf. Fig. 5.4). The output currents are defined as given in Fig. 5.3 and the parameters of the bridge-leg output current controllers on the Slave unit are as given in Tab. 5.1.

employing v_{zs} according to (3.89) as a feedforward and the Slave module sets v_{zs} as given by the same equation (3.89).

The mains voltage is 230 V (rms; line to neutral) at 50 Hz and a realistic mains inductance of $L_{mains} = 300\ \mu H$ is assumed. The parameters of the balancer circuit with its control scheme are as elaborated in Section 4.1.1, and the DC link voltage is $V_{dc} = 700$ V.

In **Figs. 5.7** and **5.9**, the CVS load voltages $v_{p,load}$ of the three phases $p = A, B, C$, the neutral leg output voltages $v_{N,out,M}$ and $v_{N,out,S}$, and the output currents $i_{p,out}$ ($p = A, B, C, N$) of the Master and Slave modules are shown for Cases I and II, respectively. The quantities in the figures are labeled in Fig. 5.3. The output currents $i_{p,out}$ of both units are almost equal for either cases: for a peak value of the output phase currents of 41 A, the maximum absolute deviations between the phase output currents of the Master and the Slave modules are 1.1 A and 1.3 A for Case I and Case II, respectively. These are maximum deviations of 2.7% and 3.2%, which are, in the opinion of the author, negligible und thus the proposed control scheme achieves the goal to sufficiently avoid differences in the output currents of the two CVSes.

From **Figs. 5.8** and **5.10**, it can be seen that the CVS input voltages $v_{q,mains}$ ($q = a, b, c$) and currents $i_{q,in}$ of the Master and the Slave modules are in phase for both investigated cases (the phase shift between the current and the voltage is negligible). Thus, an ohmic behavior results at the mains terminals. Additionally, the input current sharing between the two units is equal for Cases I and II (almost no difference could be traced in the simulation). The small differences (maximum 2.7% / 3.2%) in the output stage currents of the Master and the Slave CVS are not enough to result in a significant difference in the average power delivered by the two modules. In both cases, a remaining maximum peak-to-peak ripple in the input voltages $v_{q,mains}$ of about 6 V results, which is only 1.9% of $V_{out,n,pk} = 325$ V (cf. Tab. 3.16).

Furthermore, for Case I it can be seen from Fig. 5.7 that the voltages $v_{N,out,M}$ and $v_{N,out,S}$ are controlled in average to zero with a maximal voltage amplitude of 0.7 V for Master and Slave modules. The zero-sequence input currents $i_{in,zs,M}$ and $i_{in,zs,S}$ of the two units and the remaining ground current i_{gnd} are depicted in Fig. 5.8 (lowest graph) with rms values of 4.3 mA, 4.4 mA, and 7.0 mA. The corresponding maximum absolute values of $i_{in,zs,M}$, $i_{in,zs,S}$, and i_{gnd} are 18.1 mA, 16.9 mA, and 26.4 mA, respectively. Even though these three currents are very

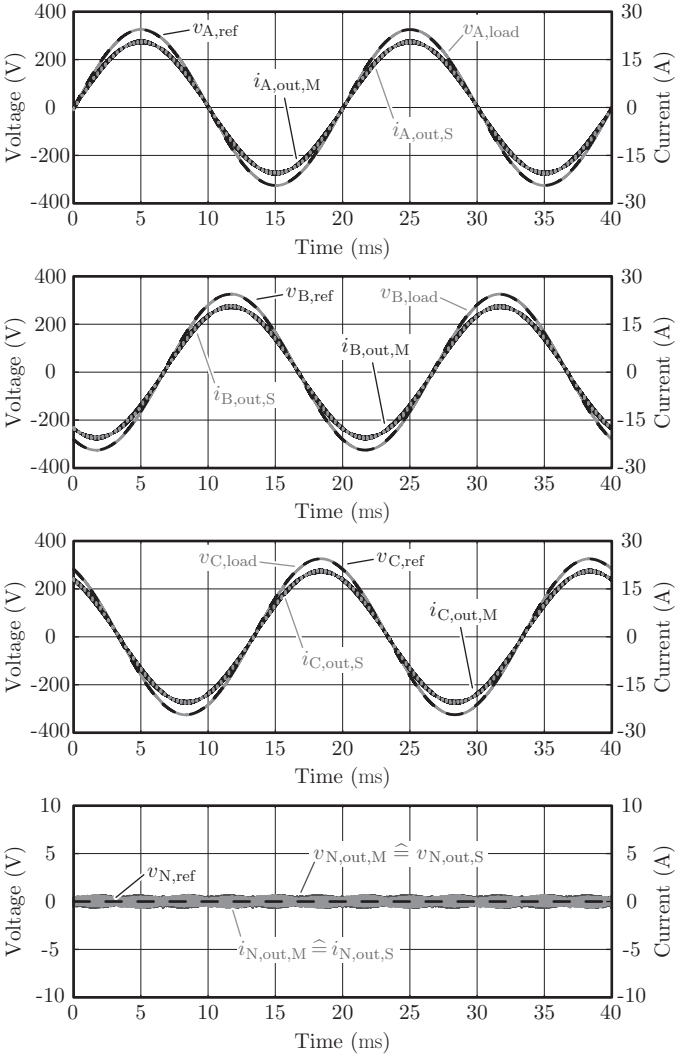


Figure 5.7: CVS phase load voltages and output currents of the Master and Slave modules for all three phases and the neutral leg for Case I. The shown quantities are defined as given in Figs. 5.3 and 5.4. It is noted that the axes for the voltage (on the left) and for the current (on the right) have different scales.

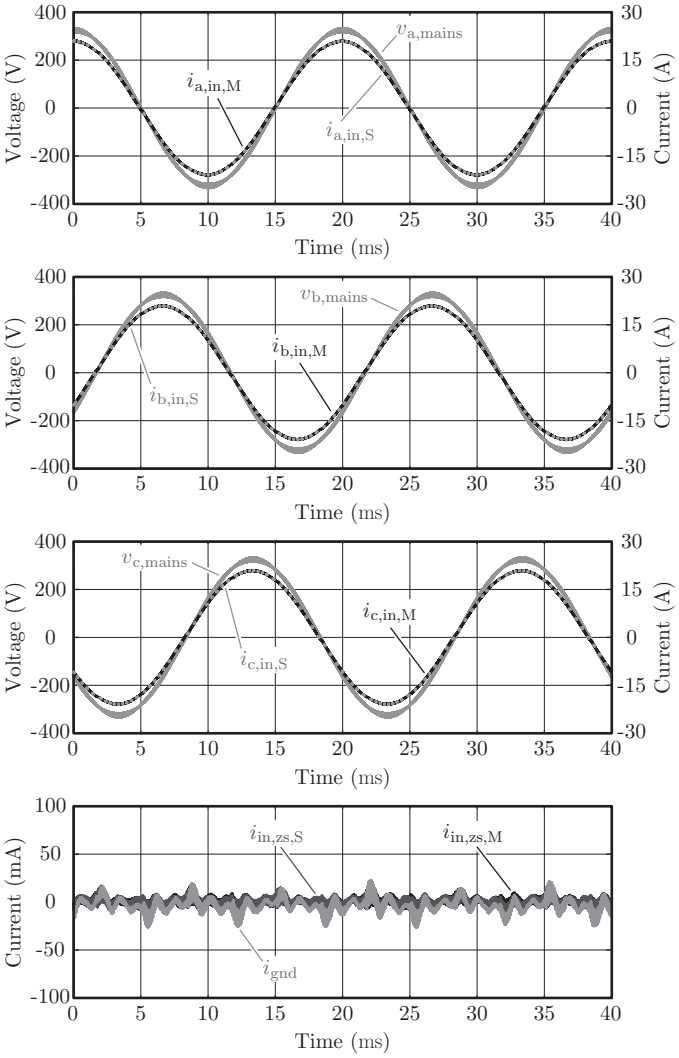


Figure 5.8: CVS input voltages and input currents of the Master and Slave modules for all three phases for Case I. The shown quantities are defined as given in Fig. 5.3. It is noted that the axes for the voltage (on the left) and for the current (on the right) have different scales.

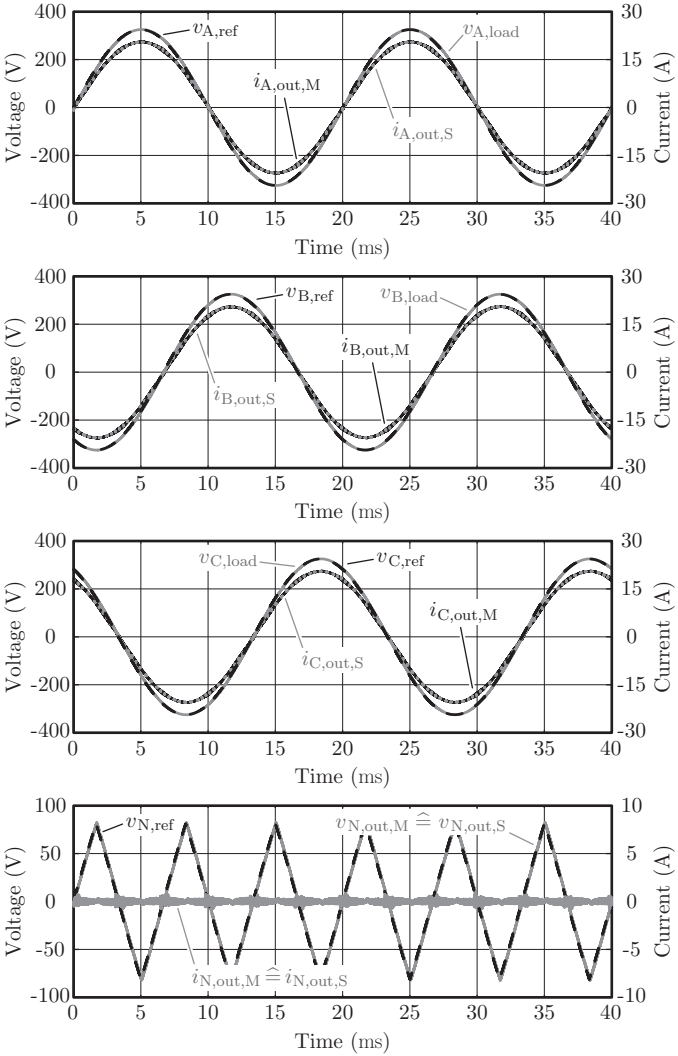


Figure 5.9: CVS phase load voltages and output currents of the Master and Slave modules for all three phases and the neutral leg for Case II. The shown quantities are defined as given in Figs. 5.3 and 5.4. It is noted that the axes for the voltage (on the left) and for the current (on the right) have different scales.

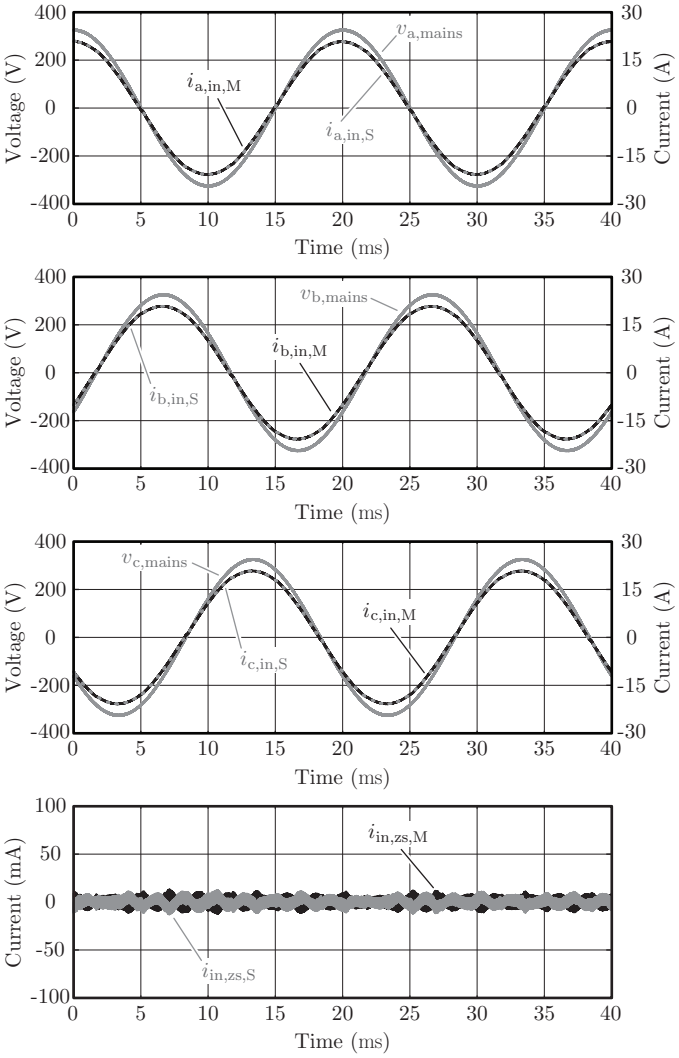


Figure 5.10: CVS input voltages and input currents of the Master and Slave modules for all three phases for Case II. The shown quantities are defined as given in Fig. 5.3. It is noted that the axes for the voltage (on the left) and for the current (on the right) have different scales.

small, the i_{gnd}'s rms value of 7.0 mA is higher than for a single module (4.4 mA, cf. Section 4.2.2) and especially above the limit of 5 mA allowed by EN 61140 [318]. This problem can be solved by permanently connecting the CVS to the mains; as the CVS then is stationary, the limit is higher, i.e. 10 mA [318].

Finally, the lowest graph of Fig. 5.10 gives the zero-sequence input currents $i_{\mathrm{in,zs,M}}$ and $i_{\mathrm{in,zs,S}}$ for Case II. Their rms and maximum absolute values are both 4.2 mA and 12.8 mA, respectively, and are hence negligible compared to the peak value of the nominal input current of $I_{\mathrm{in,n,pk}} = 20.5$ A.

5.3 Summary

In this chapter, a converter topology without galvanic isolation is proposed for the realization of a 10 kW CVS module. For parallel connected units, this, however, allows for DC and / or low-frequency inter-module circulating currents, which need to be suppressed by means of control. (Zero-sequence circulating currents can be eliminated with the ground current control scheme derived in Section 4.2.) Possible control concepts to restrict DM circulating currents, which result in an unequal current sharing between the modules, are reviewed and a Master-Slave control concept is identified to be most suitable.

The Master-Slave control concept is explained with the help of two parallel connected CVS modules and for simultaneously grounded mains star-point and load as well as for a floating load and / or a high-resistance grounded mains. Restricting the explanations to one phase, i.e. phase A, the Master module (M) employs the capacitor current feedback structure without changes, and transmits the output of the voltage controller $v_{\mathrm{A0,set,v,M}}$ as well as the references $v_{\mathrm{A,ref}}$ and $v_{\mathrm{N,ref}}$ to the Slave module (S). The Slave module then achieves the damping by employing its own capacitor currents and utilizes $v_{\mathrm{A,ref}} + v_{\mathrm{N,ref}}$ as a feedforward. Moreover, to achieve an equal distribution of the output current $i_{\mathrm{A,out}}$ between the Master and the Slave units, a current controller is added on the Slave module. This controller adjusts, in average over one switching cycle and within the bandwidth of its control loop, identical bridge-leg output currents $i_{\mathrm{A0,M}}$ and $i_{\mathrm{A0,S}}$ of the Master and the Slave units (the bridge-leg output current $i_{\mathrm{A0,M}}$ of the Master module has to be transferred to the Slave). To minimize the effect of the delay, caused by the data transmission from the Master device to

the Slave device, the output voltage references $v_{\mathrm{A,ref}}$ and $v_{\mathrm{N,ref}}$ are sent to the Slave unit and retarded on the Master module, such that both CVSes react at the same instant to changes in the references.

A load voltage step response of two parallel connected CVS modules reveals almost no voltage differences compared to the response of a single CVS, except for the voltage ripple, which can be reduced by properly synchronizing and phase-shifting the carriers of the two units. Furthermore, two characteristic cases are investigated based on accurate circuit simulations, which reveal an almost perfect current sharing between the units. The maximum deviation between the input / output phase currents of the Master and Slave devices occurs at the output and is 1.3 A, which is only 3.2% referred to the maximum peak output phase current of 41 A.

The main findings of this chapter are published in [333, 334] (see also "List of Publications" on page 337).

6 Conclusion & Outlook

6.1 Conclusion

In this Ph.D. thesis, a general purpose, low-voltage, 100 kW, four-quadrant, three-phase, switch-mode controllable AC voltage source (CVS) is researched and designed to achieve a high efficiency, a small construction volume, a very high output voltage control bandwidth, and a very low output voltage ripple. The CVS is realized by connecting ten 10 kW modules in parallel, each of the modules being implemented as an AC–DC–AC converter, consisting of a three-phase AC-DC rectifier input stage, a voltage DC link, and a three-phase four-leg DC-AC inverter output stage.

With a bidirectional three-phase active front end, the DC link voltage is regulated to 700 V–800 V to generate output phase voltages with high dynamics in the range of [±350 V]. For the nominal conditions, the DC link voltage is reduced to $V_{\mathrm{dc,n}} = 700$ V to enhance the efficiency of the CVS.

Because of the large potential application area of such a CVS, it needs to be highly flexible regarding the connection of possible loads, such as linear, e.g. DC, single-phase AC, and three-phase AC (balanced and unbalanced) resistive, inductive, and non-linear loads. Accordingly, the output stage is realized as a three-phase four-leg inverter, to boost the DC link voltage utilization, and each phase as well as the fourth leg (i.e. neutral leg) are operated and controlled individually. This also demands a four-line output filter which features a minimum interaction between the lines.

As a compromise between circuit complexity, efficiency of the CVS

module, converter volume, input and output voltage quality specifications, and dynamic requirements for the output voltage, each bridge-leg of the input and output stages is realized by a three-level T-type topology and switches at 48 kHz, employing the newest generation of Silicon Carbide (SiC) MOSFETs.

To increase the large-signal bandwidth of one 10 kW CVS module, i.e. to increase the frequency $f_{\mathrm{out,max}}$ up to which the converter is able to deliver full power, a higher CVS current-handling capability is required and hence each phase leg can be realized with two paralleled bridge-legs. According to literature and previous research, the volume of the LC output filter can be reduced if coupling inductors (CIs) are employed to magnetically couple the two bridge-leg outputs of each phase.

An equivalent circuit model of a symmetrical CI (self-inductances L and coupling factor k) with two equal leakage inductances $L_\sigma = L \cdot (1-k)$, a magnetizing inductance $L_\mu = 4 \cdot k \cdot L$ and an ideal transformer is derived, which directly points out the coupling between the two bridge-legs and clearly shows that the two bridge-leg currents are theoretically identical for $L \to \infty$ and $k = 1$. In practice, this condition is approximatively given for $L \gg L_{\mathrm{DM,1}}$ and $k \approx 1$, where $L_{\mathrm{DM,1}}$ is the filter inductance of the first filter stage.

To analyze the influence of the CI on the power circuit, a separation of the bridge-leg output voltages and the CI currents into longitudinal and transverse (cross) components is introduced. The longitudinal voltage v_{LC} drives the longitudinal current i_{LC}, which is the current flowing to the output. The transverse voltage v_{TC} is responsible for the current i_{TC} which is flowing between the bridge-legs. From these considerations, it becomes very clear that both bridge-leg currents are equal if i_{TC} vanishes (hence $L \to \infty$ for $k \approx 1$). Nevertheless, the transverse current (excluding the part through the winding capacitance) is the magnetizing current $i_\mu = i_{\mathrm{TC}}$, that for $k \approx 1$ determines the maximum flux density amplitude in the CI core.

The CI is designed to achieve a good core utilization and thus the magnetization should be symmetrical. In order to avoid saturation of the CI core in all operating conditions, the following stationary and dynamic conditions must be satisfied:

- Asymmetries in the circuit may lead to an additional transverse current i_{TC} and hence to an offset of the CI core flux density and / or to a higher flux density peak value, if no direct control

of the bridge-leg currents is provided. To guarantee a stationary symmetrical flux density, an I-type controller can be employed. During transients, the current controllers must be fast enough to avoid an overshoot/undershoot of the CI magnetizing flux density. Therefore, PI current controllers are potentially required.

- However, as the current measurements and the processing of the measurement values are not ideal, despite the current control, possibly a difference between the average (low-frequency) values of the two bridge-legs currents occurs. This difference leads again to a supplementary transverse current $i_{\mathrm{TC,lf}}$ and therefore to an increase of the peak flux density. As these inaccuracies cannot be compensated, the design of the CI has to consider a sufficient margin for the flux density in order to prevent saturation.

- Finally, the updates of the references of the PWM module must be performed at specific points in time. If the update always is at the beginning or at the end of a pulse half period (where the carriers reach either 0 or 1), the volt-seconds remain balanced and consequently the magnetizing flux density stays symmetrical.

To limit the transverse peak-to-peak current ripple to low values, it is advantageous to select the self-inductance L of the CI as high as possible. The size of the CI and / or its losses are limiting the maximum L; however, two additional constraints need to be considered for a CI. Firstly, an increasing L augments the leakage inductance and hence may produce an adverse effect on the output voltage dynamics. Secondly, a larger L also results in an increased magnetizing inductance; thus errors in the current measurement setup, which occur in any real power electronic system, could saturate the CI's core more easily.

Extensive single-phase measurements prove the theoretical analysis as well as the modeling and are showing a very close match with the circuit simulations. Moreover, the measurements demonstrate the importance of a proper control of both bridge-leg output currents and / or CI winding currents. For the T-type converter, an error $\Delta\delta$ in the duty-cycle of the bridge-legs leads to a low-frequency transverse current $i_{\mathrm{TC,lf}}$. For the considered hardware, a time difference of 10 ns between the switching instants of the bridge-legs leads to an error in the effective duty-cycle of $\Delta\delta \approx 0.05\%$. This error causes an average difference of 175 mV between the bridge-leg output voltages, which results for $\delta = 0.25$ in a difference of the CI winding currents of 1.1 A.

This clearly demonstrates a high sensitivity of the average bridge-leg currents concerning asymmetries of the converter.

However, a good magnetic coupling between the bridge-legs, i.e. $k \approx 1$, results in a relatively large parasitic capacitance between the windings of the CI. In the case at hand, measurements showed that this leads to oscillations in the transverse current i_{TC} at the switching instants, which are however not transferred to the filter output.

To design the output stage's filter, adapted from single-phase considerations, the design space (DS) concept is utilized, which provides a basis for the multi-objective optimization of the filter. The DS concept allows simultaneously considering multiple criteria that result from application-oriented specifications of the CVS such as

- minimum output voltage slew rate,
- maximum transient output voltage dip,
- maximum bridge-leg output current ripple,
- maximum output voltage ripple,
- maximum capacitive reactive power, and
- limits of conducted EMI noise emissions.

These specifications lead to corresponding limits for the output filter component values. The intersection set of all limits, for which all requirements can be fulfilled, defines the DS. The strength of the presented approach is that a clear graphical representation of the DS is obtained, e.g. the limits can be drawn in the L–C plane for a single-stage LC filter, which typically would be considered in a first step of the filter design. From the drawn limits, it can then directly be identified that, for the case at hand, the resulting DS of a single-stage filter is empty because the required compliance to the limits of conducted EMI does not allow a common intersection of all limits. Thus, the number of degrees of freedom needs to be increased, which can be achieved by introducing a two-stage LC filter. This results in a nonempty four-dimensional DS. To fully exploit this DS, a multi-objective optimization is performed and the ρ–η Pareto front (PF) is determined, which allows identifying the most compact and / or most efficient filter designs among all possible filter realizations with parameters in the DS. The PF

calculation of the two-stage LC output filter involves nearly $1.1 \cdot 10^{12}$ different filter designs. To drastically reduce this very high number, a design procedure benefiting from pre-optimized component designs is discussed in detail. From the optimization results, the Pareto optimal filter design with the highest power density is selected, resulting in $\rho = 14.6\,\mathrm{kW/dm^3}$ ($239\,\mathrm{W/in^3}$) for $\eta = 99.4\%$. As verified by measurements on a filter hardware demonstrator, the optimal filter ensures compliance to all specifications of the CVS.

Concerning an increase of the number of LC filter stages, i.e. leading to a three-, four-, etc. stage LC filter, it is remarked that, if a single LC filter stage is "distributed" to LC filter stages of equal component ratings (L/n, C/n), finally a lossless transmission line equivalent circuit model is obtained for $n \to \infty$. Such a circuitry would, however, no longer show a low-pass filter characteristic, which is required regarding conducted EMI noise suppression. Furthermore, the characteristic impedance of such a transmission line would be symmetrical, which may be too low considering the peak-to-peak bridge-leg output current ripple but too high regarding the filter output impedance seen by the load. As a consequence, multi-stage LC filters are usually dimensioned such that the characteristic impedances $Z_{0,i} = \sqrt{L_i/C_i}$ of the individual stages i are lowered from the filter input side towards the output side, as also resulting for the filter designed with the help of the elaborated approach.

Moreover, in terms of output voltage control, it is often desired that the output voltage tightly follows the reference without a large overshoot in case of a reference step. A Bessel filter, which is characterized by no output voltage overshoot, would theoretically be the ideal solution. Unfortunately, a necessary condition to achieve such a filter type, for a resistive load R_{load}, is that the characteristic impedances for a two-stage LC filter for instance fulfill $Z_{0,1} = \sqrt{L_{\mathrm{DM},1}/C_{\mathrm{DM},1}} \approx 1.5 \cdot R_{\mathrm{load}}^2$ and $Z_{0,2} = \sqrt{L_{\mathrm{DM},2}/C_{\mathrm{DM},2}} \approx 3.0 \cdot R_{\mathrm{load}}^2$, where $L_{\mathrm{DM},1}C_{\mathrm{DM},1}$ and $L_{\mathrm{DM},2}C_{\mathrm{DM},2}$ build the LC stage at the filter input and output, respectively. Accordingly, it follows that $Z_{0,2} \approx 2 \cdot Z_{0,1}$, which may generate a too high bridge-leg output current ripple and / or may lead to a too high output voltage dip / rise after a load step and which is in contradiction to the conclusion drawn in the paragraph above.

It should finally be noted that the resulting filter design is also advantageous concerning output voltage control. Because the resonant frequency of the first filter stage is by a factor of roughly 7 lower than

the one of the second filter stage, the second filter stage can be omitted for the controller design in a first step, i.e. the controller design can be carried out assuming a single-stage LC filter. The closed control loop will therefore show a limited gain at frequencies higher than the corner frequency of the first filter stage. Accordingly, the second filter stage cannot be dynamically compensated, which requires to add a passive RL damping.

For the designed output filter, three different control structures, composed of conventional P- and PI-controllers, are then motivated, modeled and optimized with respect to reference tracking and disturbance rejection. These structures are characterized by means of four defined evaluation quantities (EQs) and for common boundary conditions, e.g. for a maximum overshoot of the output voltage of 10% in case of a reference voltage step. It should be recalled that each output phase of the CVS is operated individually to allow for maximum flexibility in the generation of the output phase voltages to supply a wide range of different types of load, such as DC, single-phase and three-phase AC loads including loads with constant-power characteristics featuring negative small-signal load resistance values.

It is emphasized that the use of accurate small-signal models features an excellent matching between the presented control structure models and the measurements. Further it has been found that the achievable control performance, with respect to the values of the defined EQs, strongly depends on the two aspects listed below:

1. *Delay compensation*: To achieve a high control bandwidth and tight output voltage control, it is found to be crucial to minimize the deteriorating impact of the system time delay T_d. For this reason all three control structures incorporate delay compensation algorithms, which estimate the expected values of the controlled variables at $t = t_0 + T_\mathrm{d}$ based on previous measurements.

2. *Feedforwards and prefilter*: The prefilter for the voltage reference and the feedforwards of the reference voltage and the load current are found to allow for a considerable improvement of the investigated EQs.

For the given hardware set-up and among the three selected structures, the capacitor current feedback control structure is identified to be

most competitive considering the four EQs. This control structure realizes an output impedance of less than 500 mΩ for output frequencies below 1 kHz, a small-signal bandwidth between 7.1 kHz (for nominal load, $\tilde{R}_{\text{load}} = 15.9\ \Omega$) and 15.5 kHz (for $\tilde{R}_{\text{load}} = -15.9\ \Omega$, e.g. occurring for a constant active power load). At $\tilde{R}_{\text{load}} = -15.9\ \Omega$, the CVS completes a small-signal reference voltage step within five switching cycles (approximately 100 µs).

As a comparison, the small-signal bandwidth of available switch-mode CVSes is typically limited to 5 kHz. Accordingly, the elaborated capacitor current feedback control structure optimized with the multi-objective design procedure increase the small-signal bandwidth by 42% to 310% depending on the type of load. It is remarked that the small-signal bandwidth can even be further increased by paralleling bridge-legs.

The option to directly limit the bridge-leg output current within an inner control loop is an argument often given in favor of the PI-P control structure, where the reference for the inner current control loop is generated by an outer output voltage control loop. Frequently, it is overlooked though, that already a feedforward, which skips the inner current controller, abolishes the capability to fully limit the bridge-leg output current. The feedforward of the reference voltage, identified to enhance the output voltage dynamics, is such a feedforward. Accordingly, none of the investigated control structures features direct means to limit the bridge-leg output current. To achieve this limitation and hence to protect the hardware, an additional supervising control loop, which measures the bridge-leg output current (which would be the case for the PI-P and the PI-P-P control structures) and directly acts on the set-point output voltage of the bridge-leg, would be required. It is expected that if the bridge-leg output current needs to be limited during an output voltage transient which should achieve high dynamics, this supervising control loop would, however, reduce the achievable output voltage dynamics. It is therefore exactly in this context where a more advanced control concept would yield benefits.

Additionally, an optimal trajectory control, with a off-line calculated PWM pattern to minimize the integrated squared output voltage error (including the boundary condition of a maximum overshoot of 10%), reveals that the reaction time to a reference step is decreased by two to three switching cycles compared to the response of the capacitor current feedback control structure. Such a control, however, requires

an accurate model of the complete system inclusive load, which may, for example, be achieved with the use of a load estimator.

The fast step responses achieved with P- and PI-controllers and the low complexities of the proposed control structures clearly support the use of well-known linear controllers, e.g. in an environment that is highly sensitive to other aspects like development time and costs. Still, the widespread use of digital control platforms and increasing computing capacity enable realizations of advanced control concepts that are expected to fill the gap between the step responses obtained for the capacitor current feedback control structure and the optimal trajectory control.

In a next step, the selected capacitor current feedback control structure, laid out based on single-phase considerations, is implemented for all three phases and the neutral leg of the output stage, where the designed single-phase two-stage LC filter is employed for each phase and the neutral leg. With this four-line output filter, the load voltages of the phases, i.e. the voltages applied to the load for each phase, result from the differences between the phase output voltages and the neutral leg's output voltage, i.e. $v_{i,\mathrm{load}} = v_{i,\mathrm{out}} - v_{\mathrm{N,out}}$ for phases $i = A, B, C$. This leads to a slight adjustment of the capacitor current feedback control scheme by changing the output voltage reference of the phases from $v_{i,\mathrm{ref}}$ (single-phase consideration) to $v_{i,\mathrm{ref}} + v_{\mathrm{N,ref}}$ ($v_{\mathrm{N,ref}}$ is the output voltage reference of the neutral leg).

For this three-phase four-line converter the transient responses for $v_{i,\mathrm{load}}$ are showing slightly lower dynamics compared to the responses achieved for $v_{i,\mathrm{out}}$. The small-signal bandwidth is reduced by 15.5%, from 7.1 kHz to 6 kHz, but it is still higher than 5 kHz (specification), and the transient output impedance, due to a load step, is increased by 11.9%, from 4.2 Ω to 4.7 Ω, for instance. Nevertheless, all specifications for the output stage can be fulfilled with the three-phase four-leg converter and accurate circuit simulations revealed an almost perfect conformity between the load voltage step response of the three-phase four-leg and the single-phase system. This strongly justifies first employing a single-phase approach for designing the output filter and the output voltage control scheme and then to apply the obtained results to the three-phase four-leg output stage in a second step.

Furthermore, the importance of a good disturbance rejection, as achieved with the designed control scheme, becomes evident by consid-

ering the neutral leg of the three-phase four-leg system. The output current of this leg is impressed by the phase load voltages and the load, which varies according to the demanded range of application of the CVS.

To energize the output stage, a bidirectional three-phase voltage source AC–DC converter with sinusoidal input current is employed, which requires an EMI input filter to comply to international standards, e.g. CISPR 11. In conventional EMI input filters, the CM capacitance of the Y-capacitors is strongly limited (to a few tens of nanofarads) by the maximum allowed touch current of 3.5 mA (e.g. EN 60335-1 and / or EN 60950-1). To overcome this restriction, it is preferred to achieve the filtering with an internal CM filter capacitor, i.e. a capacitor $C_{\mathrm{cm},1}$ that is connected between the star-point y of the DM capacitors and the midpoint m of the DC link capacitors. A first CM LC filter stage is then realized in combination with a CM inductance $L_{\mathrm{cm},1}$ connected in series with the boost inductors $L_{\mathrm{dm},1}$. For $C_{\mathrm{cm},1}$, higher capacitance values can be employed and, therefore, the achieved CM attenuation can be increased. Moreover, the low-frequency as well as a main share of the high-frequency CM currents remain confined to the PWM rectifier system leading to a reduced high-frequency fluctuation of the DC output midpoint potential. However, it should be kept in mind that the benefits of the proposed filter stage depend strongly on the parasitic capacitance of the power semiconductors to the heat sink and of the DC output midpoint m to ground. Thus, the advantages of the proposed CM filter stage have to be investigated for each case separately. For the considered hardware with a heat sink connected to the midpoint of the DC link, the demonstrated benefits though clearly motivate the proposed first CM LC filter stage with an internal $C_{\mathrm{cm},1}$.

The electrical side conditions to treat this first DM / CM LC stage of the EMI input filter separately from the rest of the circuit are discussed in detail. These side conditions allow finding the ratio $k_{\mathrm{L,opt}} = L_{\mathrm{cm},1}/L_{\mathrm{dm},1}$ of CM inductance to DM inductance, which minimizes the boxed volume $V_{1,\mathrm{tot}}$ of the first filter stage. Moreover, a detailed modeling of the CM choke as well as of the DM inductor is presented, including their thermal models which are validated by experimental results.

It is demonstrated, that $k_{\mathrm{L,opt}} \approx 10 \ldots 40$, i.e. a ratio that almost completely suppresses the high-frequency CM part of the bridge-leg input currents, should be selected to achieve a compact first DM / CM

LC stage of the EMI input filter for a 10 kW PWM rectifier system. The selected design employs $k_{\mathrm{L}} = 18$ and the corresponding sum of the volumes of all filter components is 483 cm^3 (29.5 in^3). For this design, it is also verified that the leakage inductance of the CM choke $L_{\mathrm{cm},1}$ is advantageously kept at values lower than $10\% \times L_{\mathrm{dm},1}$ to avoid a

- significant reduction of the total DM filter inductance in case the CM choke core saturates;
- strong magnetic coupling of the CM choke's stray field to other filter components, which possibly lowers the achieved filter attenuation;
- massive reduction of the leakage inductance of the CM choke due to the shielding effect of magnetic shields between filter stages and / or the filter's enclosure.

To validate the proposed design, a DM / CM *LCLCL* EMI input filter, with a power density of 13.1 $\mathrm{kW/dm}^3$ (215 $\mathrm{W/in}^3$), is realized and a phase-oriented control scheme is implemented on a three-phase three-level T-type rectifier prototype to achieve sinusoidal input currents. This scheme employs only three PI-controllers and convinces by its ease of implementation. With this hardware setup, the compliance to CISPR 11, Class A (quasi-peak detector) is successfully demonstrated for nominal operation of 10 kW with almost no additional manipulations of the filter construction. Only magnetic shields made of μ-metal were introduced between the filter stages and a choke of the size of a fingertip needed to be introduced between the heat sink and the midpoint of the DC output. The results of EMI measurements with a three-phase DM / CM noise separator fully support the presented EMI filter guidelines.

Finally, it should be highlighted that, differently to the DM inductor, the CM choke is not sufficiently characterized by the phase current and the inductance value; the CM choke also needs to be designed with respect to the CM voltage-time area generated by the investigated rectifier in order to avoid saturation of its core and, with this, the volume of the CM choke can be estimated.

Up to this point, the input and output stages were investigated separately. To operate both stages together as one converter module, the

stages need to be interconnected at the DC side, which, in the simplest form, can be achieved via a common split DC link with $C_{\mathrm{dc},1}$ and $C_{\mathrm{dc},2}$. However, a continuously asymmetrical loading of the split DC link capacitors results for a grounded DC load connected to only one output phase. This would lead to DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ drifting apart over time. Because this load condition could occur in course of the operation of the CVS, two solutions to this problem have been investigated: the employment of a balancer circuit and the utilization of the fourth bridge-leg of the three-phase four-leg output stage.

On the one hand, to balance the DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ by the fourth / neutral bridge-leg of the output stage would be an elegant solution, which, however may not satisfactory work for all targeted operating conditions of the CVS. Furthermore, this voltage balancing approach cannot be employed for grounded mains and load star-points, because $v_{\mathrm{N,out}}$ of the output stage's neutral leg must be controlled to zero in this case.

On the other hand, the balancer circuit, consisting of only two power transistors (forming a two-level bridge-leg) and of an inductor, provides a simple, robust, and efficient option to balance the DC link voltages, which does not suffer from the two drawbacks just mentioned. Accordingly, the balancer circuit is the preferred solution to solve the problem of a possible unbalance of the DC link voltages. The control of the balancer circuit is investigated by accurate circuit simulations, and simple design guidelines are given for the control scheme as well as for the balancer inductance.

For a simultaneously grounded mains and load star-points, the zero-sequence voltage sources $v_{0,\mathrm{cm}}$ of the input stage and $v_{\mathrm{N,out}}$ of the output stage's neutral leg may drive an undesired large ground current i_{gnd} flowing through the CVS module and returning via earth, especially at low frequencies and / or DC, if not properly adjusted. i_{gnd}, i.e. the non-zero sum of the input phase currents of the CVS, is not related to the power transfer, and leads to a higher current stress of the components, potentially to a distortion of the sinusoidal shape of the mains currents, and could drive inductive elements of the filter stages into saturation, especially the CM chokes.

Thus, a ground current control scheme is elaborated, which employs $v_{0,\mathrm{cm}}$ as actuating quantity to keep i_{gnd} close to zero and which sets $v_{\mathrm{N,ref}} = 0$. The output voltage of the neutral leg is then not employed

to increase / maximize the load voltage range for the following reason: To achieve $i_{\mathrm{gnd}} \approx 0$, the resulting exciting zero-sequence voltage in the ground loop should be close to zero as well. Because $v_{0,\mathrm{cm}}$ and $v_{\mathrm{N,out}}$ are the only two sources in this loop, $\langle v_{0,\mathrm{cm}} \rangle_{T_{\mathrm{s,in}}} = v_{0,\mathrm{cm,set}}$ would need to compensate for $v_{\mathrm{N,out}}$, i.e. $v_{0,\mathrm{cm,set}} \approx v_{\mathrm{N,out}}$. This then may lead to bridge-leg input voltages that are higher than the ones which can be generated for a given DC link voltage. Accordingly, the DC link voltage would need to be increased, what already increases the range of the load voltages. This annuls the benefits gained by using $v_{\mathrm{N,out}}$ to maximize the load voltage range.

To achieve sufficient damping with the control scheme, the outer ground current control loop is extended by an inner capacitor current feedback loop for the current through the first (internal) CM capacitor of the EMI input filter. With this scheme the remaining simulated i_{gnd} for a single 10 kW module is limited to 4.4 mA (rms), what is lower than the value of 5 mA (rms) specified in EN 61140. This low value of 4.4 mA is mainly due to the high gain k_{g} of the capacitor current feedback loop ($k_{\mathrm{g}} = 20$ V/A).

The ground current can also be eliminated by incorporating a galvanic isolation into the CVS module. This is preferably realized with a high-frequency isolated DC–DC converter linking the input and the output stages to reduce weight and volume compared to the conventional solution, which employs a line-frequency transformer at the input of the CVS. Thus, a galvanically isolated series resonant DC–DC converter (SRC), which also integrates the split DC link voltage balancing for unequal loadings of the DC link capacitors, is analyzed. For this option, the balancer circuit can be omitted.

The proposed SRC is operated in half-cycle discontinuous-conduction-mode and consists of two half-bridges. The bridge-leg output and the DC link midpoint on the primary side are connected through the resonant capacitor, the resonant inductor, and the primary winding of the transformer; on the secondary side, the bridge-leg input and the DC link midpoint are directly connected through the transformer secondary winding.

Supplying asymmetrical loads, the inverter-side DC link capacitors are not equally loaded simultaneously. In this case, the voltage balancing across the DC link capacitors is achieved by establishing an average (over one switching cycle) magnetizing current, which is equal

to the difference of the load currents. Accordingly, the high-frequency transformer integrates the DC link voltage balancing and the galvanic isolation. It needs to store energy and hence should be realized with an air-gap or a low-permeability material for a low-volume realization.

Ideally, the DC link voltage balancing on the rectifier side can be achieved perfectly. On the inverter side, the difference of the DC link voltages depends on the average load currents. However, this voltage difference can be restricted to less than 10%, referred to the voltage across one DC link capacitor. Furthermore, design guidelines are presented showing that the SRC can achieve soft-switching (zero-voltage switching) at turn-on in all operating conditions if the peak-to-peak magnetizing current ripple is slightly larger than two times the maximum average magnetizing current (what corresponds to twice the maximum load current difference). Finally, the theoretical analysis is supported by measurements conducted on a 1 kW proof-of-concept prototype matching very well with the theory and the circuit simulations for no load, symmetrical loading, and asymmetrical loading and for a bidirectional power flow.

Compared to the option to control the ground current i_{gnd} to zero for simultaneously grounded mains star-point and load, the elimination of i_{gnd} by means of a galvanic isolation has the advantages that

- the input stage can still be operated with the superposition of a zero-sequence voltage component v_{zs} on the carrier based modulation to utilize the full (linear) modulation range, and that
- the neutral leg of the output stage can yet be employed, if required, to increase the range of the phase load voltages $v_{\mathrm{A,load}}$, $v_{\mathrm{B,load}}$, and $v_{\mathrm{C,load}}$ (connection of the load star-point to the neutral terminal N).

In summary, neither $v_{0,\mathrm{cm}}$ has to be employed for controlling i_{gnd} to zero, nor $v_{\mathrm{N,out}}$ is adjusted to zero. But, compared to the realization without transformer, the SRC requires two additional switches and DC link capacitors as well as a 10 kW high-frequency transformer, which add a significant part to the total volume and weight of the CVS module. Accordingly, it is preferred to realize the CVS unit without galvanically isolated DC–DC converter. This however requires a balancer circuit and a ground current control scheme for grounded mains star-point and load.

The CVS is thus operating as follow: without fixed connections of the mains star-point and / or the load (e.g. load star-point) to ground, the CM voltage $v_{0,\mathrm{cm}}$ of the input (rectifier) stage is employed to utilize the full (linear) modulation range and the output voltage $v_{\mathrm{N,out}}$ of the neutral leg is used to increase the range of the load voltages according to

$$v_{\mathrm{N,ref}} = -\frac{\min\left(v_{\mathrm{A,ref}},\, v_{\mathrm{B,ref}},\, v_{\mathrm{C,ref}}\right) + \max\left(v_{\mathrm{A,ref}},\, v_{\mathrm{B,ref}},\, v_{\mathrm{C,ref}}\right)}{2}. \quad (6.1)$$

However, for grounded mains and load star-points, $v_{0,\mathrm{cm}}$ regulates the ground current i_{gnd} to zero while $v_{\mathrm{N,out}}$ is controlled to zero. In both cases, to increase the CVS' efficiency, the DC link voltage is adjusted such that a minimal margin of 25 V exists between the maximum input / output voltage, which can be generated by the input / output stage, and the maximum mains / load voltage, to allow a small ripple of the DC link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$. Consequently, for the nominal peak input and output voltages of 325 V, the nominal DC link voltage yields $V_{\mathrm{dc,n}} = 700$ V. If a faster rise / reduction in the load voltages is required, the DC link voltage can be increased to maximally $V_{\mathrm{dc,max}} = 800$ V. The balancer circuit can be operated continuously or can be switched on if the absolute difference between the DC link voltages, i.e. $|V_{\mathrm{dc},1} - V_{\mathrm{dc},2}|$, exceeds a certain threshold.

The entire 100 kW CVS is realized by ten 10 kW modules in parallel. Because a converter topology without galvanic isolation is employed for each unit, the paralleling allows for DC and / or low-frequency inter-module circulating currents, which need to be suppressed by means of control. Zero-sequence circulating currents can be eliminated with the derived ground current control scheme. Possible control concepts to restrict DM circulating currents, which result in an unequal current sharing between the modules, are reviewed and a Master-Slave control concept is identified to be most suitable.

The Master-Slave control concept is explained with the help of two parallel connected CVS modules and for simultaneously grounded mains and load star-points as well as for a floating load and / or a high-resistance grounded mains. Restricting the explanations to one phase, i.e. phase A, the Master module implements the capacitor current feedback structure without changes, and transmits the output of the voltage controller $v_{\mathrm{A0,set,v,M}}$ as well as the references $v_{\mathrm{A,ref}}$ and $v_{\mathrm{N,ref}}$ to the Slave module. The latter module then achieves the damping by

employing its own capacitor currents and utilizes $v_{\mathrm{A,ref}} + v_{\mathrm{N,ref}}$ as a feedforward. Moreover, to achieve an equal current distribution of the output current $i_{\mathrm{A,out}}$ between the Master and the Slave units, a current controller is added on the Slave module. This controller adjusts, in average over one switching cycle and within the bandwidth of its control loop, identical bridge-leg output currents $i_{\mathrm{A0,M}}$ and $i_{\mathrm{A0,S}}$ of the Master and the Slave units, respectively. The bridge-leg output current $i_{\mathrm{A0,M}}$ of the Master module is thus transferred to the Slave too. To minimize the effect of the delay, caused by the data transmission from the Master device to the Slave device, the output voltage references $v_{\mathrm{A,ref}}$ and $v_{\mathrm{N,ref}}$ are sent to the Slave unit and retarded on the Master module, such that both CVSes react at the same instant on changes in the references.

A load voltage step response of two parallel connected CVS modules has been performed, revealing almost no voltage differences compared to the response of a single CVS, except for the voltage ripple, which can be reduced by properly synchronizing and phase-shifting the carriers of the two modules. Furthermore, two characteristic cases are investigated based on accurate circuit simulations, which reveal an almost perfect current sharing between the units. The maximum deviation between the input / output phase currents of the Master and Slave occurs at the output and is 1.3 A, which is only 3.2% referred to the maximum peak output phase current of 41 A.

6.2 Outlook

Concerning further research, the experimental proof of the developed ground current control scheme and Master-Slave control concept for parallel connected CVS modules should be performed in the first place. Then, going back to the very beginning, where a hybrid, i.e. a combination of switch-mode and linear, amplifier structure for the CVS module realization has been disregarded for the reason of elevated circuit and control complexity, a detailed analysis of the achievable performance (in terms of efficiency, volume, output voltage quality, and dynamics of the output voltage control) of such a hybrid converter system and a comprehensive comparison to the performance indices obtained for the switch-mode CVS elaborated in this thesis should be carried out.

To design the single-phase output voltage control structure, a small-signal load model has been required. For a three-phase constant power load, which tends to destabilize the system, the small-signal model for a balanced three-phase disturbance is well known. However, further investigations are necessary to derive a model in case of a disturbance in a single-phase. Moreover, the small-signal model of a constant three-phase reactive power load / source for both stated disturbance scenarios are still no covered in literature.

With regard to the development of the CVS towards an industrial system, it would be desired to incorporate bridge-leg output current limiting capabilities into the output stage's control scheme to protect the converter. Furthermore, the start-up of the converter should be examined, with special focus on the ground current control loop.

Pertaining to the extension from the single-phase system to the three-phase four-leg realization of the output stage, a refinement of the control structure design, based on small-signal considerations simultaneously taking all four legs into account, could bring the transient load voltage responses of the three-phase four-leg system even more in line with the ones obtained for the single-phase case. Especially, the cross-coupling between the three phases resulting for an asymmetric load with star-point connected to the neutral terminal could be introduced as a supplementary evaluation criterion. In addition, it should be analyzed if the fourth leg needs to be realized with the same filter component values and needs to use the same control parameters than the three phases.

For power amplifiers, the audio susceptibility defines how strong the noise at the amplifier's input is attenuated at its output [22]. This quantity could also be calculated for the designed CVS and would indicate by which amount the amplitude of harmonics in the mains voltage would appear in the output voltage.

Finally, further research can be conducted for the DC link. On the one hand, this would include the optimization of the balancer circuit's control scheme (based on a small-signal model) with respect to the current stress of the balancer circuit components and the effectiveness to equalize the split DC link voltages. On the other hand, the analytical calculation of the maximum current stress of the split DC link capacitor, which considers the operation of the balancer circuit and the output stage's neutral leg, would be the main topics. Moreover, the control of the DC link voltage by the rectifier input stage would need to be improved in order to deliver a satisfactory behavior also for AC single-phase and heavily unbalanced three-phase loads. Such loads are characterized by a pulsating output power which generates oscillations in the DC link voltage. If these voltage swings are within the bandwidth of the DC link voltage control loop, the oscillations pass to the bridge-leg input currents and accordingly lead to objectionable distortions of the mains currents. One straightforward solution to this issue is to lower the bandwidth of the control loop by reducing the controller gain, which, however, would result in a slow transient response of the DC link voltage. A more promising option is to implement a variable controller gain depending on the absolute deviation of the DC link voltage to its reference. Outside a certain outer tolerance band around the reference, the gain is high. As soon as the absolute voltage error enters this band, the gain is reduced. The reduction is the larger the smaller the error becomes. When the absolute error hits a second, inner tolerance band, the gain is not further decreased and kept constant within this second band.

Appendices

A

Coupling Inductor Literature Overview

According to [370], the first publications dealing with CIs date back to the early 1920's. Two CIs were used to create two parallel bypasses around a load, for reducing the voltage ripple at the load supplied from an AC mains [371]. Later, the CI was used in DC–DC converters as a building block to form a LCL-filter (the coupled inductor filter) with only two components, if properly designed, instead of three components in the endeavor to achieve zero current ripple [370]. In the past decade, research on CIs covers a wide topical area including DC–DC and DC–AC converters of different voltage levels ($\sim$ 1 V [98, 372] – 10 kV [83]) as well as power levels (10 W [131] – 60 MW [83]) [93, 113]. The main reasons mentioned in literature for employing CIs are:

- improvement of the transient voltage response at the output of the device (increased dynamic performance) [87, 98, 99, 101, 102, 106, 107, 111, 117, 123, 124, 373–382];
- reduction of the filter capacitance value [117, 125, 383];
- reduction of the size (volume and weight) of the passive filter components [83, 86, 88, 90, 91, 99, 103–106, 114, 116, 128, 138, 373, 377, 379, 380, 384–392];
- reduction of the peak-to-peak current ripple [85, 87, 90, 98, 99, 101, 103, 112, 113, 117, 119, 120, 123, 128, 129, 131, 138, 370, 374, 375, 380–382, 384, 387, 391, 393–399];

- reduction of the loop/circulating/cross/transverse current amplitude in paralleled bridge-leg converters [107,116,130,376,384,387, 395,400,401];
- phase current ripple steering (ripple cancelation; 'zero'-ripple filter) [85,90,138,370,393,394,396];
- increase of the number of voltage levels at the output of the converter and therefore reducing the harmonic content of the output voltage [92,98,107,121,135,376,386,390–392,402–407];
- enhancement of the system's efficiency (thus, reduction of the power losses) [83,86–88,90,91,94,97,102,103,105,106,114,117, 120,125,126,129,374,375,378,382,384,389,400,408–410];
- increase of the system's power density [102,114,124];
- decrease of the component count to build the converter [86,88, 102–104,135,400,411,412];
- total converter cost reduction [88,94,102,105,116,129,386,388].

A short survey about the very wide application area of CIs in power electronic systems is presented in the following:

- Voltage Regulator Modules (VRMs) [86,87,98,101,106,108,112, 115,117,123,125,131,132,375,376,380,383,385,397,413] - e.g. microprocessor power supplies [131,132,374,375,408,413] or buck converters for digital signal processors - for example coupling four phases [372] - in desktop, notebook and server applications [97, 118] or DC–DC converter in portable electronic devices such as laptops [124];
- power factor correction circuitry [90,130,384,412] and shunt active power filters [133,388,390];
- Uninterruptible Power Supplies (UPSs) applications [101,130,381, 395,398], e.g. in telecommunication [138,414];
- converters for renewable energy generation, e.g. DC–DC boost converters to supply loads from batteries with low output voltages [410], converters for photovoltaic modules or fuel cells [118, 381,389,396], or converters for wind energy conversion systems [389,390];

- automotive applications [104, 128, 129] and variable speed drive systems [116, 120, 130, 135, 386, 390, 393, 401, 406, 407, 415, 416], e.g. for pure/hybrid electric vehicles [91, 105, 114, 414, 417], for fuel cell vehicles [91, 114], for permanent-magnet based flywheel battery systems [392], or for the powering of electric trains [118];

- aerospace applications (where weight, volume, and efficiency are important) [418], supplies of high-intensity discharge lamps [381, 414], or high bandwidth class-D switch-type audio amplifiers [92];

- high power applications, such as DC arc furnaces, electrochemical processes, plasma power supplies, and high voltage transmissions [401], e.g. static VAR compensators, Flexible AC Transmission Systems (FACTS) [390], and High Voltage Direct Current (HVDC) applications [393];

- pulsed power supply of the synchrotron particle accelerator at CERN (Conseil Européen pour la Recherche Nucléaire) [83].

E.g. [83] compares the volume, weight, and efficiency of the magnetic devices with individual inductors to the ones when coupling inductors are employed for powering the particle accelerator. The results are that the volume of the entire magnetic components could be reduced by 44%, the weight by 64%, and the efficiency increased by 7% (= 14.4 kW). This concrete application example points out how large the advantage of employing CIs can be.

In this respect, synonyms for a CI are "coupled inductors", "coupling transformer", "smoothing transformer", "autotransformer", "current sharing reactors", "integrated magnetics" (magnetic integration technology, which however is also applicable to other magnetic devices), "InterCell Transformer (ICT)", "interphase inductor/reactor", and "InterPhase Transformer (IPT)". Finally, [88] separates "coupled inductors" from "decoupled inductors" and, dependent on the direction of the magnetic flux in the core, labels them as inverse or alternate couplings. The reference defines a decoupled inductor as a structure, where two extra limbs without windings are added to a coupled inductor core.

Some papers make the distinction between "directly coupled inductors" (direct coupling inductor) and "inversely coupled inductors" (inverse coupling inductor) [87,110,118,123,379] which physically differ in the direction of the windings. In Section 2.2.2, the difference between

both arrangements is further explained. ICTs and IPTs always refer to inversely coupled inductors.

Seen all the different definitions for the device "coupling inductor", the author's motivations for the naming "CI" are the following: By a CI, the two bridge-legs are magnetically coupled, in the sense that a change in the current/voltage on one side affects the other side through the magnetic flux. Thus, the denomination "coupling" is preferred. Additionally, an ideal transformer in principle is not an energy storing device and thus has no filtering abilities. However, a general CI represents an inductance for the longitudinal current and limits the transverse (cross) current between parallel bridge-legs through its effective transverse inductive behavior. Moreover, the power flow in a transformer is from the primary to the secondary side and vice versa, which again does not hold for CIs. For these reasons, the naming "inductor" is preferred to "transformer" in this work.

Remark: Common-mode chokes basically could also be seen as members of the category of "coupling inductors" (cf. [133]). However, due to the extensive discussion of this type of chokes in the literature, the considerations of this part are limited to CIs interconnecting parallel connected bridge-legs (i.e. for the case at hand, the CI is part of the DM output filter of the controllable AC voltage source).

To complete the literature review and to emphasize the diversity of CIs related research, selected papers are listed in the following: The differences between CIs and transformers are addressed in [419, 420] and a general model of a multiple-winding coupling inductor is described in [394]. References [94, 395, 398] explain that CIs offer a better magnetic material utilization. The design of coreless coupling inductors is investigated in [126, 382], while [399] focuses on design guidelines for an ICT with zero-sequence voltage injection (which increases the magnetic flux in the core). An application summary of coupling inductors in DC–DC converters is given in [381].

Zero-voltage switching is achieved with CIs in [94, 381, 417] and a CI is employed in a boost converter to achieve zero-current transition in [410]. According to [421], a CI is employed in a passively clamped quasi resonant DC link inverter. Additionally, the leakage inductance of the CI is employed to control the diode current falling rate and therefore helps to alleviate the reverse-recovery losses in the rectifier diodes of DC–DC converters [381, 408]. Moreover, extreme duty cycles can be avoided by CIs in high step-up or step-down voltage conversions [381].

E.g. [414] and [422] focus on a switched-coupling inductor cell for DC–DC converters (e.g. for a boost converter) with large conversion ratios.

In [423], a CI is used in an EMI input filter of a three-phase buck-type PWM rectifier and [424] uses modified CIs to construct a band-pass filter. Supplementary, a circuit configuration which magnetically couples four phases of a buck converter with a switchable unique secondary loop for all phases is explained in [375]. The aim of the proposed topology is to reduce the length of the main power windings.

Reference [103] evaluates and verifies experimentally the influence of phase failures in multi-phase coupling inductors on the magnetic flux in the core and [104] analyzes the impact of input and output voltage perturbations on the system behavior, respectively on the unbalance of the currents of paralleled bridge-legs, in a multi-phase inverter with CIs. [397] describes a practical CI concept for interleaved converters and [115] examines the optimal (with respect to losses and volume) number of commutation cells in a multi-cell interleaved flyback converter. Aside from this, the optimal (referred to efficiency, complexity, and filter capacitance value) setup to magnetically connect four [108] and six phases [125] by means of CIs are analyzed and experimentally reviewed in the mentioned references. A CI integrating ten or twelve phases on the same core is presented in [111] or [400], respectively.

According to [118], a CI in a boost converter allows increasing the bandwidth of the peak current-mode control scheme and [413] identifies that the output voltage control bandwidth for a two-phase buck converter could be enlarged by a factor of two by employing a CI instead of single inductors. CI power losses are compared for different modulation schemes of a three-level [406] as well as of five-level converter in [135] and [120] identifies that the phase and phase opposite disposition modulation strategies are advantageous for the reduction of the harmonic content in the output voltage and the resulting DM current (transverse/cross current) between the bridge-legs, respectively.

Reference [398] makes a comparison between using coupling or single inductors. A distinction between monolithic [101, 113] and separate coupling inductors is mentioned in [93, 398]. Different filter structures with coupling inductors for a paralleled three-phase converter are analyzed in [105]: CIs are employed to couple the phases with either one or three additional filter inductors or by integrating the filtering action into the CIs by the use of the leakage inductances. Finally, a complete comparison between the usage of single and coupling inductors,

including the inverter, is presented in [84].

B

Stability Analysis for a Single-Stage *LC* Filter

B.1 Two-Loop Control Structure

The stability analysis for the single-stage LC filter and the two-loop control scheme depicted in Fig. 3.24(a), initially only considers the inner current loop without the feedforward of the load current, $I_{\mathrm{A,out}}$, and assumes a P-controller, $G_{\mathrm{i}} = k_{\mathrm{pi}}$. This analysis is based on the block diagram depicted in **Fig. B.1**, for which the time delay due to the digital control and the PWM unit is assumed to be perfectly compensated by the delay compensation (cf. Section 3.3.2). Accordingly, the inductor current is

$$I_{\mathrm{A0}}(s) = I_{\mathrm{A0,ref}}(s) \cdot \underbrace{\frac{G_{\mathrm{i}} \cdot H_{\mathrm{V0\to I0}}}{1 + G_{\mathrm{i}} \cdot H_{\mathrm{V0\to I0}}}}_{L_{\mathrm{cl,i}} = \dfrac{I_{\mathrm{A0}}}{I_{\mathrm{A0,ref}}}} + V_{\mathrm{A,ref}}(s) \cdot \underbrace{\frac{H_{\mathrm{V0\to I0}}}{1 + G_{\mathrm{i}} \cdot H_{\mathrm{V0\to I0}}}}_{L_{\mathrm{ff,Vref}} = \dfrac{I_{\mathrm{A0}}}{V_{\mathrm{A,ref}}}}, \tag{B.1}$$

which defines the loop transfer functions $L_{\mathrm{cl,i}}$ and $L_{\mathrm{ff,Vref}}$ in the Laplace domain based on the system transfer function

$$H_{\mathrm{V0\to I0}} = \frac{I_{\mathrm{A0}}(s)}{V_{\mathrm{A0}}(s)} = \frac{1 + \tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}} \cdot s}{L_{\mathrm{DM,1}} \cdot C_{\mathrm{DM,1}} \cdot \tilde{R}_{\mathrm{A,load}} \cdot s^2 + L_{\mathrm{DM,1}} \cdot s + \tilde{R}_{\mathrm{A,load}}}. \tag{B.2}$$

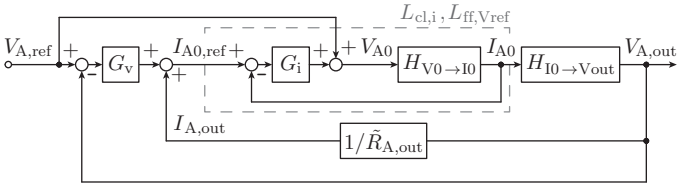


Figure B.1: Block diagram for a simplified PI-P control structure for controlling the output voltage of a single-stage LC filter without prefilter for the voltage reference [cf. (3.54)], delays caused by the microcontroller and the PWM unit (cf. Section 3.3.2), and delay compensation [cf. (3.66) and (3.67); perfect compensation of the delay] and with feedforwards of the reference voltage $V_{\mathrm{A,ref}}$ and the load current $I_{\mathrm{A,out}}$.

With a P-controller, the results for $L_{\mathrm{cl,i}}$ and $L_{\mathrm{ff,Vref}}$ are

$$L_{\mathrm{cl,i}} = k_{\mathrm{pi}} \cdot \frac{\omega_{01}^2}{\tilde{R}_{\mathrm{A,load}}} \cdot \frac{1 + s \cdot \tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}}}{s^2 + a_1 \cdot s + a_2} \tag{B.3}$$

and

$$L_{\mathrm{ff,Vref}} = \frac{L_{\mathrm{cl,i}}}{k_{\mathrm{pi}}} \tag{B.4}$$

with

$$a_1 = \frac{k_{\mathrm{pi}}}{L_{\mathrm{DM,1}}} + \frac{1}{\tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}}}, \quad a_2 = \omega_{01}^2 \cdot \left(\frac{k_{\mathrm{pi}}}{\tilde{R}_{\mathrm{A,load}}} + 1 \right) \tag{B.5}$$

and

$$\omega_{01} = \frac{1}{\sqrt{L_{\mathrm{DM,1}} \cdot C_{\mathrm{DM,1}}}}, \tag{B.6}$$

i.e. $L_{\mathrm{ff,Vref}}$ is directly proportional to $L_{\mathrm{cl,i}}$. For $\tilde{R}_{\mathrm{A,load}} < 0$ the transfer function $H_{\mathrm{V0\rightarrow I0}}$ [cf. (B.2)] shows a Right Half Plane (RHP) complex conjugated pole pair. Thus, for negative small-signal load resistances, the current control loop needs to stabilize the unstable plant.

A necessary and sufficient condition for a second order transfer function to be stable is that both coefficients, a_1 and a_2, of the denominator

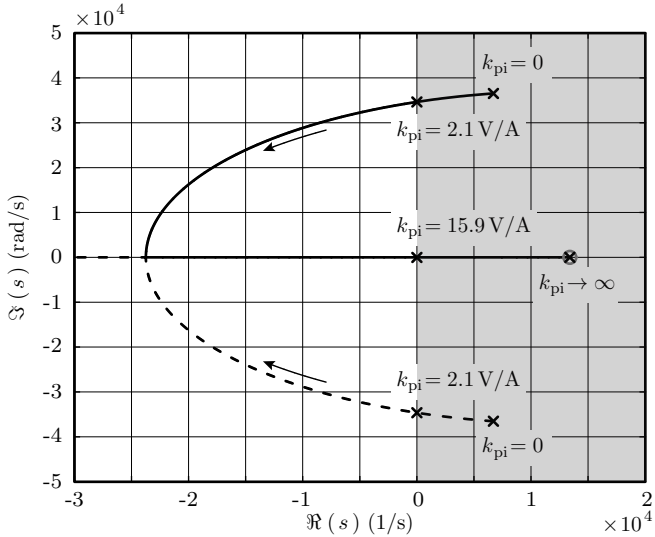


Figure B.2: Root locus of $L_{\mathrm{cl,i}}$ for $L_{\mathrm{DM},1} = 154.2\ \mu\mathrm{H}$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F}$, and $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$ showing that the current control loop is only stable for certain gain values, i.e. for $2.1\ \mathrm{V/A} < k_{\mathrm{pi}} < 15.9\ \mathrm{V/A}$. Poles and zeros are marked with "x" and "o", respectively. The location of the zero is independent of k_{pi}.

of $L_{\mathrm{cl,i}}$ are strictly positive, i.e. $a_1 > 0$ and $a_2 > 0$ applies. With this and (B.6) the conditions

$$a_1 > 0 \rightarrow k_{\mathrm{pi}} > \frac{{Z_0}^2}{-\tilde{R}_{\mathrm{A,load}}} \tag{B.7}$$

$$a_2 > 0 \rightarrow \begin{cases} k_{\mathrm{pi}} > & -\tilde{R}_{\mathrm{A,load}} \quad \text{for} \quad \tilde{R}_{\mathrm{A,load}} > 0 \\ k_{\mathrm{pi}} < & -\tilde{R}_{\mathrm{A,load}} \quad \text{for} \quad \tilde{R}_{\mathrm{A,load}} < 0 \end{cases} \tag{B.8}$$

result, where $Z_0 = \sqrt{L_{\mathrm{DM},1}/C_{\mathrm{DM},1}}$ is the characteristic impedance of the first filter stage. According to (B.7) and (B.8) any value of k_{pi} stabilizes the system in case of positive load resistances, $\tilde{R}_{\mathrm{A,load}} > 0$, if only positive controller gains, $k_{\mathrm{pi}} > 0$, are considered. In case of negative load resistance values, however, lower and upper gain boundaries exist

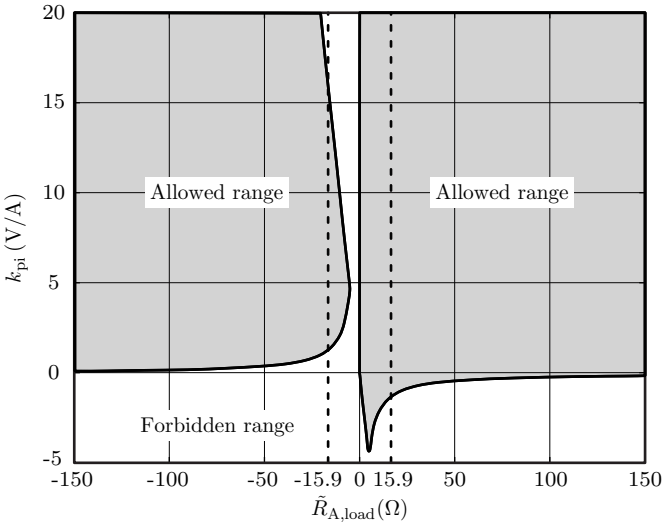


Figure B.3: Stability region (gray shaded area) of the current control loop given in Fig. B.1 dependent on the small-signal load resistance $\tilde{R}_{\mathrm{A,load}}$ and the gain of the current controller k_{pi}.

for stable current control,

$$\frac{{Z_0}^2}{-\tilde{R}_{\mathrm{A,load}}} < k_{\mathrm{pi}} < -\tilde{R}_{\mathrm{A,load}}. \tag{B.9}$$

This, in addition, implies $\tilde{R}_{\mathrm{A,load}} < -Z_0$ for $\tilde{R}_{\mathrm{A,load}} < 0$, otherwise a P-controller cannot stabilize the system. **Fig. B.2** shows the root locus of $L_{\mathrm{cl,i}}$ for $L_{\mathrm{DM,1}} = 154.2\ \mu\mathrm{H}$, $C_{\mathrm{DM,1}} = 4.7\ \mu\mathrm{F}$, and $\tilde{R}_{\mathrm{A,load}} = -15.9\ \Omega$ and the lower and upper boundaries of k_{pi}, $k_{\mathrm{pi,min}} = 2.1\ \mathrm{V/A}$ and $k_{\mathrm{pi,max}} = 15.9\ \mathrm{V/A}$, respectively, for stable operation of the closed current control loop. **Fig. B.3** is a graphical representation of (B.9) and shows, for $L_{\mathrm{DM,1}} = 154.2\ \mu\mathrm{H}$ and $C_{\mathrm{DM,1}} = 4.7\ \mu\mathrm{F}$, the gains k_{pi} that guarantee stability for different values of $\tilde{R}_{\mathrm{A,load}}$.

For a PI-controller

$$G_{\mathrm{i}} = k_{\mathrm{pi}} + \frac{k_{\mathrm{ii}}}{s}, \tag{B.10}$$

the closed current control loop transfer function $L_{\mathrm{cl,i}}$ has the form

$$L_{\mathrm{cl,i}} = \frac{\mathrm{Num}_{L\mathrm{cl,i}}(s)}{s^3 + a_1 \cdot s^2 + a_2 \cdot s + a_3}. \tag{B.11}$$

A necessary condition for stability is that all coefficients of the denominator polynomial are strictly positive, i.e. $a_i > 0 \; \forall \; i \in \{1,\, 2,\, 3\}$. The expression calculated for a_3,

$$a_3 = \frac{\omega_{01}^2 \cdot k_{\mathrm{ii}}}{\tilde{R}_{\mathrm{A,load}}} > 0, \tag{B.12}$$

implies that the signs of k_{ii} and $\tilde{R}_{\mathrm{A,load}}$ must be the same,

$$\begin{array}{ll} k_{\mathrm{ii}} > 0 & \text{for} \;\; \tilde{R}_{\mathrm{A,load}} > 0, \\ k_{\mathrm{ii}} < 0 & \text{for} \;\; \tilde{R}_{\mathrm{A,load}} < 0. \end{array} \tag{B.13}$$

For this reason, a constant value of k_{ii} (gain of the integral part) cannot stabilize the current control loop for all load situations detailed in Section 3.3.1, in particular when the sign of the small-signal load resistance can be positive as well as negative. Thus, a P-controller is used to stabilize the current control loop.

In the next step, the outer voltage control loop is investigated with respect to stability and, for this, a P-controller, $G_{\mathrm{v}} = k_{\mathrm{pv}}$, is first considered. The analysis is split into two parts in order to achieve a more comprehensible presentation: the output current feedforward, which leads to a feedback branch in Fig. B.1, is first not considered and is included in a second step.

Without the output current feedforward, $V_{\mathrm{A,out}}$ is obtained from Fig. B.1 with

$$V_{\mathrm{A,out}} = \underbrace{\left[\underbrace{\left(V_{\mathrm{A,ref}} - V_{\mathrm{A,out}}\right) \cdot G_{\mathrm{v}}}_{=I_{\mathrm{A0,ref}}} \cdot L_{\mathrm{cl,i}} + V_{\mathrm{A,ref}} \cdot L_{\mathrm{ff,Vref}} \right]}_{=I_{\mathrm{A0}}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}} \tag{B.14}$$

being solved with respect to $V_{\mathrm{A,out}}$, which gives the closed-loop voltage transfer function,

$$L_{\mathrm{cl,v}} = \frac{V_{\mathrm{A,out}}}{V_{\mathrm{A,ref}}} = \frac{G_{\mathrm{v}} \cdot L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}} + L_{\mathrm{ff,Vref}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}}{1 + G_{\mathrm{v}} \cdot L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}} \tag{B.15}$$

with

$$H_{\mathrm{I0}\rightarrow\mathrm{Vout}} = \frac{V_{\mathrm{A,out}}}{I_{\mathrm{A0}}} = \frac{\tilde{R}_{\mathrm{A,load}}}{1 + s \cdot \tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}}}. \tag{B.16}$$

According to (B.16), $H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$ has a RHP pole pair for negative values of $\tilde{R}_{\mathrm{A,load}}$. In (B.15), however, $H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$ only appears in the product terms $L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$ and $L_{\mathrm{ff,Vref}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$. Together with (B.3) the unstable pole pair cancels,

$$\begin{aligned} L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}} &= k_{\mathrm{pi}} \cdot \frac{\omega_{01}^2}{\tilde{R}_{\mathrm{A,load}}} \cdot \frac{1 + s \cdot \tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}}}{s^2 + a_1 \cdot s + a_2} \cdot \\ &\qquad \frac{\tilde{R}_{\mathrm{A,load}}}{1 + s \cdot \tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}}} = \frac{k_{\mathrm{pi}}\, \omega_{01}^2}{s^2 + a_1 \cdot s + a_2}, \end{aligned} \tag{B.17}$$

$$L_{\mathrm{ff,Vref}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}} = \frac{\omega_{01}^2}{s^2 + a_1 \cdot s + a_2} \tag{B.18}$$

and, thus, both, $L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$ and $L_{\mathrm{ff,Vref}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$, are stable, because k_{pi} has previously been selected such that the real parts of the roots of the polynomial $s^2 + a_1 \cdot s + a_2$ are negative.[1] With this, the closed-loop voltage transfer function

$$L_{\mathrm{cl,v}} = \frac{(1 + k_{\mathrm{pv}} \cdot k_{\mathrm{pi}}) \cdot \tilde{R}_{\mathrm{A,load}}}{b_{2,\mathrm{v}} \cdot s^2 + b_{1,\mathrm{v}} \cdot s + b_{0,\mathrm{v}}}, \tag{B.19}$$

where

$$\begin{aligned} b_{0,\mathrm{v}} &= k_{\mathrm{pi}} + \tilde{R}_{\mathrm{A,load}} \cdot (1 + k_{\mathrm{pv}} \cdot k_{\mathrm{pi}}), \\ b_{1,\mathrm{v}} &= \left(k_{\mathrm{pi}} \cdot \tilde{R}_{\mathrm{A,load}} \cdot C_{\mathrm{DM,1}} + L_{\mathrm{DM,1}}\right), \\ b_{2,\mathrm{v}} &= L_{\mathrm{DM,1}} \cdot C_{\mathrm{DM,1}} \cdot \tilde{R}_{\mathrm{A,load}}, \end{aligned} \tag{B.20}$$

results, with a second order denominator polynomial. Thus, $L_{\mathrm{cl,v}}$ is stable if the coefficients of the denominator polynomial are strictly pos-

[1] In a similar approach it can be shown that $L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$ and $L_{\mathrm{ff,Vref}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}$ remain stable if a measurement filter is considered in the current control loop, which corresponds to a transfer function in the feedback path of the inductor current.

itive, which is the case for

$$k_{\mathrm{pi}} > \frac{{Z_0}^2}{-\tilde{R}_{\mathrm{A,load}}}, \tag{B.21}$$

$$k_{\mathrm{pv}} > -\frac{1}{\tilde{R}_{\mathrm{A,load}}} - \frac{1}{k_{\mathrm{pi}}}. \tag{B.22}$$

It is interesting to note that (B.21) limits the gain of the current controller in order to allow for a stable closed-loop voltage transfer function. However, (B.9) already covers the condition of (B.21). Expression (B.22) solely limits k_{pv} in case of negative load resistances, if only positive controller gains, $k_{\mathrm{pi}} > 0$ and $k_{\mathrm{pv}} > 0$, are considered.

If the output current feedforward is considered, the closed-loop voltage transfer function

$$L_{\mathrm{cl,v}} = \frac{G_{\mathrm{v}} \cdot L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}} + L_{\mathrm{ff,Vref}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}}{1 + \left(G_{\mathrm{v}} - \tilde{R}^{-1}_{\mathrm{A,load}}\right) \cdot L_{\mathrm{cl,i}} \cdot H_{\mathrm{I0}\rightarrow\mathrm{Vout}}} \tag{B.23}$$

results, which, for a voltage P-controller, is stable for

$$k_{\mathrm{pi}} > \frac{{Z_0}^2}{-\tilde{R}_{\mathrm{A,load}}}, \tag{B.24}$$

$$k_{\mathrm{pv}} > -\frac{1}{k_{\mathrm{pi}}}. \tag{B.25}$$

Thus, with ideal feedforward of $I_{\mathrm{A,out}}$, the critical gain of the voltage controller becomes independent of the load.

The voltage P-controller may be replaced by a PI-controller,

$$G_{\mathrm{v}} = k_{\mathrm{pv}} \cdot \left(1 + \frac{1}{s \cdot T_{\mathrm{iv}}}\right), \tag{B.26}$$

in order to reduce the steady state error of the output voltage. With this, and with the reference voltage and output current feedforwards being considered, a closed-loop voltage transfer function of the form

$$L_{\mathrm{cl,v}} = \frac{V_{\mathrm{A,out}}}{V_{\mathrm{A,ref}}} = \frac{\mathrm{Num}_{L\mathrm{cl,v}}(s)}{s^3 + a_{1,\mathrm{v}} \cdot s^2 + a_{2,\mathrm{v}} \cdot s + a_{3,\mathrm{v}}} \tag{B.27}$$

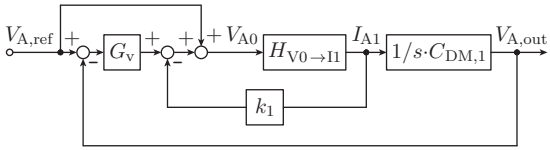


Figure B.4: Block diagram for a simplified capacitor current feedback control structure for a single-stage *LC* filter without prefilter for the voltage reference [cf. (3.54)], delays caused by the microcontroller and the PWM unit (cf. Section 3.3.2), and delay compensation [cf. (C.4) and (C.5); perfect compensation of the delay] and with a feedforward of the reference voltage $V_{\mathrm{A,ref}}$.

results. The sufficient conditions for stability are obtained from the Routh stability criterion [183],

$$k_{\mathrm{pi}} > -\frac{Z_0^2}{\tilde{R}_{\mathrm{A,load}}}, \tag{B.28}$$

$$\frac{k_{\mathrm{pi}}}{T_{\mathrm{iv}}} > 0, \tag{B.29}$$

$$k_{\mathrm{pv}} > -\frac{1}{k_{\mathrm{pi}}} - \left[k_{\mathrm{pi}} \cdot \omega_{01}^2 \cdot \left(\frac{L_{\mathrm{DM,1}}}{\tilde{R}_{\mathrm{A,load}}} + C_{\mathrm{DM,1}} \cdot k_{\mathrm{pi}}\right) \cdot T_{\mathrm{iv}} - k_{\mathrm{pi}}\right]^{-1}. \tag{B.30}$$

Thus, in contrast to the current control loop, the integrator of the voltage controller does not destabilize the system in the presence of negative and positive small-signal resistances $\tilde{R}_{\mathrm{A,load}}$.

B.2 Capacitor Current Feedback Control Structure

The stability analysis of the capacitor current feedback control structure is conducted based on the block diagram depicted in **Fig. B.4** and in the same manner as the analysis for the two-loop control structure presented in Appendix B.1. The inner control loop with the feedback

of the capacitor current, I_{A1}, is stable for

$$k_1 > -\frac{Z_0^2}{\tilde{R}_{\mathrm{A,load}}}. \tag{B.31}$$

The outer loop, which controls the output voltage, additionally requires

$$k_{\mathrm{pv}} > -1 \tag{B.32}$$

for stable operation with a voltage P-controller, $G_{\mathrm{v}} = k_{\mathrm{pv}}$. In case of a voltage PI-controller, $G_{\mathrm{v}} = k_{\mathrm{pv}} \cdot \left[1 + (s \cdot T_{\mathrm{iv}})^{-1}\right]$, the sufficient conditions for stability of the closed voltage control loop,

$$k_1 > -\frac{Z_0^2}{\tilde{R}_{\mathrm{A,load}}}, \tag{B.33}$$

$$T_{\mathrm{iv}} > 0, \tag{B.34}$$

$$k_{\mathrm{pv}} > -1 - \left[T_{\mathrm{iv}} \cdot \left(\frac{1}{C_{\mathrm{DM,1}} \cdot \tilde{R}_{\mathrm{A,load}}} + \frac{k_1}{L_{\mathrm{DM,1}}}\right) - 1\right]^{-1}, \tag{B.35}$$

are again obtained from the Routh stability criterion [183].

C

Delay Compensation for the Capacitor Current Feedback and the PI-P-P Control Structures

The delay compensation for the capacitor current feedback and the PI-P-P control structures can be derived in the same manner as explained in Section 3.3.2 for the PI-P structure. For the capacitor current feedback control structure [cf. Fig. 3.26(b)] the following compensation is proposed

$$\underbrace{i_{\mathrm{A1}}(t_i+\Delta t)}_{\substack{\text{estimated value of}\\ i_{\mathrm{A1}} \text{ at } t\to t_{i+1}}} \approx i_{\mathrm{A1}}(t_i)+\frac{v_{\mathrm{A0,set}}(t_0)-v_{\mathrm{A,out}}(t_i)}{L_{\mathrm{DM,1}}}\cdot\Delta t, \tag{C.1}$$

$$\underbrace{v_{\mathrm{A,out}}(t_i+\Delta t)}_{\substack{\text{estimated value of}\\ v_{\mathrm{A,out}} \text{ at } t\to t_{i+1}}} \approx v_{\mathrm{A,out}}(t_i)+\frac{i_{\mathrm{A1}}(t_i)+i_{\mathrm{A2}}(t_i)}{C_{\mathrm{DM,1}}+C_{\mathrm{DM,2}}}\cdot\Delta t, \tag{C.2}$$

with

$$t_i=t_0+i\cdot\Delta t,\ \ 0\le i<n,\ \ i\in\mathbb{N}_0,\ \ n\in\mathbb{N},\ \ \Delta t=\frac{T_{\mathrm{d}}}{n}, \tag{C.3}$$

and hence for $n = 2$

$$\begin{aligned} i_{\mathrm{A1}}(t_0 + T_\mathrm{d}) &= k_{\mathrm{c},1} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},2} \cdot v_{\mathrm{A,out}}(t_0) + \\ &\quad k_{\mathrm{c},3} \cdot i_{\mathrm{A1}}(t_0) + k_{\mathrm{c},4} \cdot i_{\mathrm{A2}}(t_0) \qquad \text{(C.4)} \\ v_{\mathrm{A,out}}(t_0 + T_\mathrm{d}) &= k_{\mathrm{c},5} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},6} \cdot v_{\mathrm{A,out}}(t_0) + \\ &\quad k_{\mathrm{c},7} \cdot i_{\mathrm{A1}}(t_0) + k_{\mathrm{c},8} \cdot i_{\mathrm{A2}}(t_0). \qquad \text{(C.5)} \end{aligned}$$

where T_d is the total delay in the control loops caused by the digital implementation and the PWM unit and the factors $k_{\mathrm{c},1} \ldots k_{\mathrm{c},8}$ are given in **Tab. C.1**. In a similar manner, the delay compensation for the PI-P-P control structure [cf. Fig. 3.26(c)] can be described by

$$\underbrace{i_{\mathrm{A0}}(t_i + \Delta t)}_{\substack{\text{estimated value of} \\ i_{\mathrm{A0}} \text{ at } t \to t_{i+1}}} \approx i_{\mathrm{A0}}(t_i) + \frac{v_{\mathrm{A0,set}}(t_0) - v_{\mathrm{A1}}(t_i)}{L_{\mathrm{DM},1}} \cdot \Delta t, \qquad \text{(C.6)}$$

$$\underbrace{v_{\mathrm{A1}}(t_i + \Delta t)}_{\substack{\text{estimated value of} \\ v_{\mathrm{A1}} \text{ at } t \to t_{i+1}}} \approx v_{\mathrm{A1}}(t_i) + \frac{i_{\mathrm{A0}}(t_i) - i_{\mathrm{A,out}}(t_0)}{C_{\mathrm{DM},1}} \cdot \Delta t, \qquad \text{(C.7)}$$

$$\underbrace{v_{\mathrm{A,out}}(t_i + \Delta t)}_{\substack{\text{estimated value of} \\ v_{\mathrm{A,out}} \text{ at } t \to t_{i+1}}} \approx v_{\mathrm{A,out}}(t_i) + \frac{i_{\mathrm{A0}}(t_i) - i_{\mathrm{A,out}}(t_0)}{C_{\mathrm{DM},1} + C_{\mathrm{DM},2}} \cdot \Delta t, \qquad \text{(C.8)}$$

leading to

$$\begin{aligned} i_{\mathrm{A1}}(t_0 + T_\mathrm{d}) &= k_{\mathrm{c},1} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},2} \cdot v_{\mathrm{A1}}(t_0) + \\ &\quad k_{\mathrm{c},3} \cdot i_{\mathrm{A0}}(t_0) + k_{\mathrm{c},4} \cdot i_{\mathrm{A,out}}(t_0) \qquad \text{(C.9)} \\ v_{\mathrm{A1}}(t_0 + T_\mathrm{d}) &= k_{\mathrm{c},5} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},6} \cdot v_{\mathrm{A1}}(t_0) + \\ &\quad k_{\mathrm{c},7} \cdot i_{\mathrm{A0}}(t_0) + k_{\mathrm{c},8} \cdot i_{\mathrm{A,out}}(t_0) \qquad \text{(C.10)} \\ v_{\mathrm{A,out}}(t_0 + T_\mathrm{d}) &= k_{\mathrm{c},9} \cdot v_{\mathrm{A0,set}}(t_0) + k_{\mathrm{c},10} \cdot v_{\mathrm{A1}}(t_0) + k_{\mathrm{c},11} \cdot v_{\mathrm{A,out}}(t_0) + \\ &\quad k_{\mathrm{c},12} \cdot i_{\mathrm{A0}}(t_0) + k_{\mathrm{c},13} \cdot i_{\mathrm{A,out}}(t_0). \qquad \text{(C.11)} \end{aligned}$$

with the factors as given in Tab. C.1.

Table C.1: Factors $k_{\mathrm{c},1} \ldots k_{\mathrm{c},8}$ used for the delay compensations in the capacitor current feedback control structure [cf. Fig. 3.26(b) and Eqs. (C.4) and (C.5)] and factors $k_{\mathrm{c},1} \ldots k_{\mathrm{c},13}$ employed for the PI-P-P control structure [cf. Fig. 3.26(c) and Eqs. (C.9), (C.10), and (C.11)]. $T_{0,\mathrm{out}}$ denotes the sampling time.

Capacitor current feedback control structure	
$k_{\mathrm{c},1}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{L_{\mathrm{DM},1}}$
$k_{\mathrm{c},2}$	$-\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{L_{\mathrm{DM},1}}$
$k_{\mathrm{c},3}$	$1 - \frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},4}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},5}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},6}$	$1 - \frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},7}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}+C_{\mathrm{DM},2}}$
$k_{\mathrm{c},8}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}+C_{\mathrm{DM},2}}$
PI-P-P control structure	
$k_{\mathrm{c},1}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{L_{\mathrm{DM},1}}$
$k_{\mathrm{c},2}$	$-\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{L_{\mathrm{DM},1}}$
$k_{\mathrm{c},3}$	$1 - \frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{C_{\mathrm{DM},1} \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},4}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{C_{\mathrm{DM},1} \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},5}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{C_{\mathrm{DM},1} \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},6}$	$1 - \frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{C_{\mathrm{DM},1} \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},7}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}}$
$k_{\mathrm{c},8}$	$-\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}}$
$k_{\mathrm{c},9}$	$\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},10}$	$-\frac{9}{16} \cdot \frac{T_{0,\mathrm{out}}^2}{(C_{\mathrm{DM},1}+C_{\mathrm{DM},2}) \cdot L_{\mathrm{DM},1}}$
$k_{\mathrm{c},11}$	1
$k_{\mathrm{c},12}$	$\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}+C_{\mathrm{DM},2}}$
$k_{\mathrm{c},13}$	$-\frac{3}{2} \cdot \frac{T_{0,\mathrm{out}}}{C_{\mathrm{DM},1}+C_{\mathrm{DM},2}}$

D

Maximum Touch Current

Power electronic equipment with a protective earthing conductor connected to protective earth (PE) need, for safety reasons, to comply to standards limiting the maximum protective conductor current and the maximum touch current.[1] According to EN 60990 [427], the overall current flowing against PE in normal operating mode is denoted as protective conductor current [427]. This current is e.g. caused by the parasitic capacitance C_g for a low-frequency potential variation of the DC link midpoint with respect to PE, as given for a carrier based sinusoidal modulations with a superimposed zero-sequence component according to

$$v_\mathrm{zs} = -\frac{\max\left(v_\mathrm{a}, v_\mathrm{b}, v_\mathrm{c}\right) + \min\left(v_\mathrm{a}, v_\mathrm{b}, v_\mathrm{c}\right)}{2}. \tag{D.1}$$

The touch current is an "electric current through a human body or through an animal body when it touches one or more accessible parts of an installation or of equipment" [427] and is according to the standard EN 60990 unweighted (electric burns), weighted for "perception and reaction" and weighted for "let-go". Typically, the limit for the touch current weighted for perception and reaction is the most restrictive one [285].

Furthermore, the regulation EN 60990 specifies that the protective conductor current and the touch current are measured under normal and faulty operation, respectively. Typically and for the case at hand, limiting the touch current (3.5 mA according to EN 60335-1 for

[1] The naming adopted in this appendix is according to international standards, e.g. EN 60950-1 [297] and EN 60990 [427].

Class I protection) according to international standards is more restrictive than setting limits on the maximum protective conductor current (e.g. 5 mA). Thus, only the touch current measurement setup and the applicable fault conditions are discussed next. It is highlighted that the fault conditions change depending on the power distribution system (e.g. TN-S, TN-C, or IT [285, 427]) the three-phase PWM rectifier system is connected to.

If an equipment is not reliably earthed (no industrial plug and socket outlet according to e.g. IEC 60309 [297]), the touch current of a system must be measured with a faulty protective earthing conductor, i.e. when the protective earthing conductor is no longer connected to PE [427] and / or the enclosure of a converter is not grounded anymore, together with an additional fault in the EMI input filter. In this case, if somebody would touch the enclosure, the connection to ground would be made through its (human) body. The worst case touch current is obtained for a defect DM capacitor (i.e. the DM capacitor represents an open-circuit because of its self-healing property).[2] For the purpose of simplification and as a worst case assessment, a defect in $C_{\mathrm{dm},1}$ and in $C_{\mathrm{d},1}$ of one phase, e.g. phase a, are simultaneously assumed as depicted in **Fig. D.1**.[3]

In the described case as shown in Fig. D.1 and by considering the CM equivalent circuit given in **Fig. D.2** (for e.g. a TN-C or a IT power distribution system connected in star configuration), the voltage $v_{\mathrm{Ccm1,pe}}$ across the CM capacitor $C_{\mathrm{cm,1,pe}}$ results from a capacitor voltage divider between $2 \cdot C_{\mathrm{DM},1}$ and $C_{\mathrm{cm,1,pe}}$. Thus, neglecting the inductive voltage drops in the second filter stage, $v_{\mathrm{Ccm1,pe}}$ is given by

$$v_{\mathrm{Ccm1,pe}} = -\frac{C_{\mathrm{DM},1}}{2 \cdot C_{\mathrm{DM},1} + C_{\mathrm{cm,1,pe}}} \cdot v_{\mathrm{a,mains}}. \tag{D.2}$$

[2] Typically and for the considered case, a faulty DM capacitor leads to a higher touch current than unequal capacitances $C_{\mathrm{dm},i}, i = 1{,}2$ in the phases due to the capacitance tolerances of up to ±20% [293].

[3] Typically, to protect the converter and the filter against over-voltages from the mains, varistors are placed at the mains terminals. Thus, it should be taken into account that according to EN 60950-1, it is not allowed to place a varistor (i.e. a voltage dependent resistor) between one phase (power line) and ground (PE), i.e. to bypass the basic insulation, if the equipment is not reliably earthed (i.e. no industrial plug and socket outlet according to e.g. IEC 60309) [297]. Accordingly, a short-circuit of one phase to ground does not need to be considered to assess the worst case for measuring the touch current. Line-to-line over-voltage protection by a varistor is always possible.

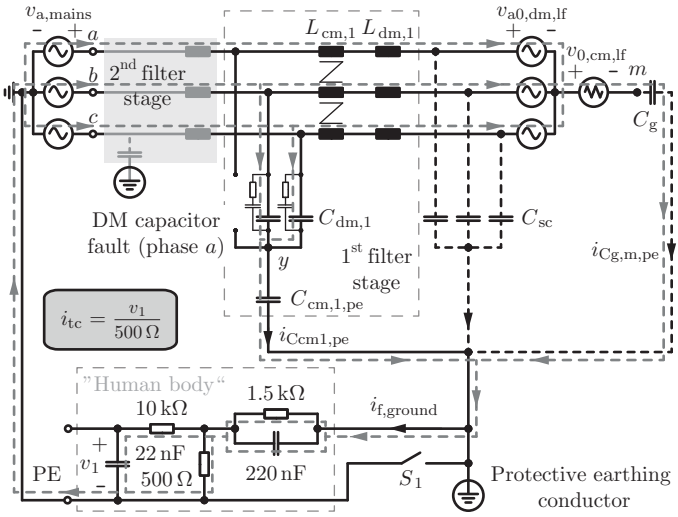


Figure D.1: Equivalent circuit of the three-phase three-level PWM rectifier with a conventional CM filtering (Y-capacitor $C_{\mathrm{cm,1,pe}}$) and measuring circuit according to EN 60990 [427] to measure the touch current i_{tc} weighted for perception and reaction after EN 60990, if a fault of the protective earthing conductor (i.e. switch S_1 is open) as well as a fault in $C_{\mathrm{dm,1}}$ and $C_{\mathrm{d,1}}$ of one phase, i.e. phase a, is assumed (worst case). Accordingly, $C_{\mathrm{dm,1}}$ and $C_{\mathrm{d,1}}$ in phase a represents an open-circuit. Exemplary a TN-C power distribution system is depicted.

Typically and as it is also the case for the EMI input filter designed in Section 3.5, $C_{\mathrm{DM,1}} \gg C_{\mathrm{cm,1,pe}}$ and accordingly (D.2) gives

$$v_{\mathrm{Ccm1,pe}} = -\frac{v_{\mathrm{a,mains}}}{2}, \tag{D.3}$$

i.e. half of the line-to-neutral voltage is applied across $C_{\mathrm{cm,1,pe}}$. This leads to a line-frequency current $i_{\mathrm{Ccm1,pe}}$ through $C_{\mathrm{cm,1,pe}}$ with amplitude

$$i_{\mathrm{Ccm1,pe,pk}} = 2 \cdot \pi \cdot f_{\mathrm{mains}} \cdot C_{\mathrm{cm,1,pe}} \cdot \frac{\sqrt{2} \cdot V_{\mathrm{mains}}}{2 \cdot \sqrt{3}} \tag{D.4}$$

flowing to ground. Additionally, the ground current $i_{\mathrm{Cg,m,pe}}$ through C_{g}, due to the selected modulation scheme with superposition of v_{zs}

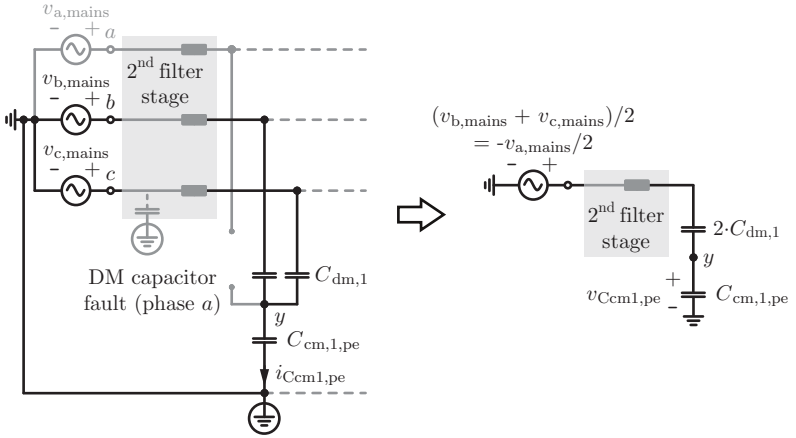


Figure D.2: Simplified CM equivalent circuit of Fig. D.1, which results by only considering the CM current $i_{Ccm1,pe}$ through $C_{cm,1,pe}$ flowing to ground caused by the DM capacitor fault in phase a (i.e. the DM capacitor represents an open-circuit; damping elements neglected).

[cf. (D.1)], needs to be considered. v_{zs} is analytically calculated in [78] and shows a triangular shape with a peak value of

$$v_{zs,pk} = \frac{V_{mains}}{2 \cdot \sqrt{6}}. \tag{D.5}$$

From the Fourier series of v_{zs}, the amplitude of the fundamental component, occurring at $3 \cdot f_{mains}$, can be calculated as

$$v_{zs,pk,3} = \frac{8}{\pi^2} \cdot v_{zs,pk} = \frac{4}{\sqrt{6} \cdot \pi^2} \cdot V_{mains}. \tag{D.6}$$

Assuming that the amplitudes of the higher-order harmonics in v_{zs} are negligible compared to amplitude of the fundamental component,[4] the

[4]The second harmonic (at $9 \cdot f_{mains}$) of v_{zs} has an amplitude of 7.4 V, which is only 11% of the fundamental component $v_{zs,pk,3} = 66.5$ V for $V_{mains} = 400$ V_{ll} (rms), therefore justifying the made assumption.

amplitude of the current through C_g can be assessed with

$$i_\mathrm{Cg,m,pe,pk} = 6 \cdot \pi \cdot f_\mathrm{mains} \cdot C_\mathrm{g} \cdot v_\mathrm{zs,pk,3} = \frac{4 \cdot \sqrt{6}}{\pi} \cdot f_\mathrm{mains} \cdot C_\mathrm{g} \cdot V_\mathrm{mains}, \tag{D.7}$$

and accordingly, the resulting current flowing to ground is

$$i_\mathrm{f,ground} = i_\mathrm{Ccm1,pe} + i_\mathrm{Cg,m,pe}, \tag{D.8}$$

where both currents (showing different frequencies, i.e. f_mains and $3 \cdot f_\mathrm{mains}$) are positively superimposing and have the amplitudes as given in (D.4) and (D.7).

To measure $i_\mathrm{f,ground}$, EN 60990 specifies the network shown in Fig. D.1, which should emulate the human body. The measured current is weighted for perception and reaction and named touch current i_tc, and is the peak value of the voltage v_1 divided by 500 Ω. It is reminded that this type of touch current is typically of major importance [285].

The measurement circuit given in Fig. D.1 shows a low-pass characteristic of the transfer function from $i_\mathrm{f,ground}$ to i_tc with a cut-off frequency (−3 dB) of approximately 687 Hz. Thus, the harmonics due to the switching of the power semiconductors with $f_\mathrm{s,in} = 48$ kHz are attenuated by 37 dB and more, and, accordingly, the measured touch current i_tc is equal to $i_\mathrm{f,ground}$ for the following consideration, i.e.

$$i_\mathrm{tc} \cong i_\mathrm{f,ground} \quad \forall \quad f_\mathrm{s,in} \gg 687 \text{ Hz}. \tag{D.9}$$

The maximum value of the touch current can therefore be determined by

$$i_\mathrm{tc,pk} = \pi \cdot f_\mathrm{mains} \cdot \left(C_\mathrm{cm,1,pe} + \frac{12}{\pi^2} \cdot C_\mathrm{g} \right) \cdot \frac{\sqrt{2} \cdot V_\mathrm{mains}}{\sqrt{3}}, \tag{D.10}$$

which results in a maximum capacitance value of the Y-capacitor $C_\mathrm{cm,1,pe}$ of

$$C_\mathrm{cm,1,pe,max} = \frac{3.5 \text{ mA}}{\pi \cdot f_\mathrm{mains} \times 110\% \times \sqrt{2} \cdot V_\mathrm{mains}/\sqrt{3}} - \frac{12}{\pi^2} \cdot C_\mathrm{g} \approx 31 \text{ nF}, \tag{D.11}$$

if the maximum touch current is limited to 3.5 mA according to EN 60335-1. A +10% tolerance of the mains voltage and a parasitic capacitance of $C_\mathrm{g} = 25$ nF between the midpoint of the DC link and ground

(PE) are assumed. Thus, the maximum allowed touch current limits directly the maximum value of the CM Y-capacitor and accordingly the effectiveness of its ability to filter. It is noted that (D.11) applies analogous to $C_{\mathrm{cm},2}$ of the second filter stage (cf. Fig. D.1), i.e. $C_{\mathrm{cm},1,\mathrm{pe}} \leq 31$ nF and $C_{\mathrm{cm},2} \leq 31$ nF, because only one additional fault in the EMI filter needs to be considered at once (cf. EN 60990 [427]).

Furthermore, it is observed that for the selected switching frequency of $f_{\mathrm{s,in}} = 48$ kHz, the unweighted touch current for consideration of electrical burn has to be verified as well. The limit for this kind of touch current is according to EN 61010-1 500 mA (rms value under fault conditions) [427], which is substantially higher, i.e. 500 mA, than the limit of 3.5 mA (peak value) imposed by the touch current weighted for perception and reaction. Hence, complying with the specification concerning perception and reaction limits the capacitance value of $C_{\mathrm{cm},1,\mathrm{pe}}$ more than ensuring an unweighted touch current of less than 500 mA. Furthermore, it is remarked that with the proposed CM filter structure, where the internal CM capacitor $C_{\mathrm{cm},1}$ is connected between y and m [cf. Fig. 3.52(a) and Section 3.5], the unweighted touch current can be reduced by a factor of 2.3 (3.1 mA versus 7.2 mA) compared to the conventional CM filtering with a Y-capacitor connected to ground [cf. Fig. 3.52(d)].

Finally, it is referred to Fig. 3.52(e), where, in the equivalent circuit, the CM capacitance from the bridge-leg inputs to ground is realized by three Y-capacitors $C_{\mathrm{cm},0,\mathrm{pe}}$ connected from each phase to ground. In this case and in analogy to the DM capacitor fault considered above, the highest peak value of the touch current is obtained for an additional fault of a CM capacitor $C_{\mathrm{cm},0,\mathrm{pe}}$, i.e. $C_{\mathrm{cm},0,\mathrm{pe}}$ represents an open-loop, for one phase, e.g. phase a, as shown in **Fig. D.3**. For this fault scenario, the phase currents through $C_{\mathrm{cm},0,\mathrm{pe}}$ do not sum up to zero, which leads to a line-frequency current $i_{\mathrm{Ccm0,pe,f}}$ with amplitude

$$i_{\mathrm{Ccm0,pe,f,pk}} = 2 \cdot \pi \cdot f_{\mathrm{mains}} \cdot C_{\mathrm{cm},0,\mathrm{pe}} \cdot \frac{\sqrt{2} \cdot V_{\mathrm{mains}}}{\sqrt{3}} \tag{D.12}$$

flowing to ground (neglecting the typically very small inductive voltage drops of the EMI input filter). Considering the contribution of $i_{\mathrm{Cg,m,pe}}$ to the entire low-frequency current flowing to ground as explained above, the peak value of the touch current is given by

$$i_{\mathrm{tc,pk}} = 2 \cdot \pi \cdot f_{\mathrm{mains}} \cdot \left(C_{\mathrm{cm},0,\mathrm{pe}} + \frac{6}{\pi^2} \cdot C_{\mathrm{g}} \right) \cdot \frac{\sqrt{2} \cdot V_{\mathrm{mains}}}{\sqrt{3}}. \tag{D.13}$$

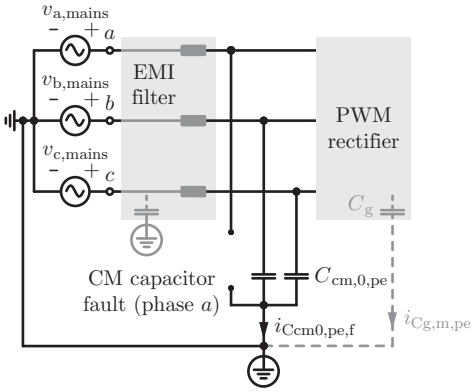


Figure D.3: Low-frequency equivalent circuit for three CM Y-capacitors connected between each phase and ground to assess the line-frequency current $i_{\mathrm{Ccm0,pe,f}}$ flowing to ground for a CM capacitor fault in phase a (i.e. the CM capacitor represents an open-circuit).

This results in a maximum capacitance value of the Y-capacitor $C_{\mathrm{cm,0,pe}}$ of

$$\begin{aligned} C_{\mathrm{cm,0,pe,max}} &= \frac{3.5\ \mathrm{mA}}{2 \cdot \pi \cdot f_{\mathrm{mains}} \times 110\% \times \sqrt{2} \cdot V_{\mathrm{mains}}/\sqrt{3}} - \frac{6}{\pi^2} \cdot C_{\mathrm{g}} \\ &= \frac{C_{\mathrm{cm,1,pe,max}}}{2} \approx 15.5\ \mathrm{nF}, \end{aligned} \tag{D.14}$$

if the maximum touch current is limited to 3.5 mA according to EN 60335-1. A +10% tolerance of the mains voltage and a parasitic capacitance of $C_{\mathrm{g}} = 25$ nF between the midpoint of the DC link and ground (PE) are again assumed.

List of Publications

Different parts of the research findings presented in this dissertation and of other research projects carried out in parallel have already been published or will be published in international scientific journals, conference proceedings, and / or have been protected by patents. The publications and patents developed in the course of this Ph.D. thesis are listed below.

Journal Papers

- D. O. Boillat, F. Krismer, and J. W. Kolar, "Design space analysis and ρ–η Pareto optimization of *LC* output filters for switch-mode AC power sources," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6906–6923, 2015. DOI: 10.1109/TPEL.2015.2393151 [PDF]
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